Studies of electrical and optoelectronic properties of Ge-ion-implanted SiO2 thin films

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NANYANG TECHNOLOGICAL UNIVERSITY

STUDIES OF ELECTRICAL AND OPTOELECTRONIC PROPERTIES OF GE-ION-IMPLANTED SiO_2 THIN FILMS

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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This thesis is dedicated to my parents.

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SUMMARY

It is the intent of this work to present a systematic investigation on the electrical and optoelectronic properties of SiO_2 thin films embedded with Ge nanocrystals (nc-Ge) for the potential applications in non-volatile memories as well as light emitting devices. The Ge nanocrystals embedded in SiO_2 have been synthesized with low-energy (2 – 16 keV) Ge ion implantation technique which is fully compatible with modern complementary-metal-oxide-semiconductor (CMOS) technology and has the advantage of being able to precisely control the nc-Ge concentration and depth distribution by adjusting the implant energy and Ge ion dose. The synthesized SiO_2 thin films embedded with nc-Ge have been characterized by the techniques of transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), x-ray photoelectron spectroscopy (XPS), current-voltage (*I-V*), capacitance-voltage (*C-V*) and electroluminescence (EL).

The current conduction behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been studied. The characteristics of gate current density versus oxide field at various temperatures have been investigated, and the different transport mechanisms dominating in different oxide field regions have been identified. Appropriate models used to explain the current transport behavior have been proposed. On the other hand, the conduction of the Ge-ion-implanted SiO_2 can be switched to a higher- or lower-conductance state with ultra-violet (UV) illumination. Such photon-induced conduction modulation phenomenon is caused by the charging and discharging of nc-Ge due to the UV illumination.

The charge trapping and retention behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been studied. The dependence of trapped charges on the polarity and magnitude of the charging voltage as well as the charging time has been studied. Besides, the influences of thermal annealing temperature, implant energy and implant dose on the charge trapping and charge retention behavior have been investigated, and the results are well correlated to the changes in the structural properties of the Ge-ion-implanted SiO_2 thin films. In addition, the charge loss caused by the lateral charge transfer along the nc-Ge distributed region and the charge leakage to the Si substrate has also been studied.

The metal-oxide-semiconductor (MOS) capacitance of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been modeled using an approach based on the calculation of effective dielectric constant using the sub-layer method and the Maxwell-Garnett effective medium approximation (EMA) for each sub-layer. Both the distribution of nc-Ge in SiO_2 and the reduced dielectric constant corresponding to the nanometer size of nc-Ge have been taken in account during the calculation. Using this approach, the influences of implant energy and dose on the MOS capacitance have been studied, and the static dielectric constant of nc-Ge embedded in SiO_2 has been determined. The calculated results have been compared with the experimental data showing that good agreement exists over a wide range of nc-Ge distribution.

Light-emitting devices based on a structure of indium tin oxide (ITO) / SiO_2 embedded with nc-Ge / *p*-Si substrate have been fabricated. Visible electroluminescence (EL) with a dominant EL band at 2.1 eV and two shoulder bands

at 1.6 and 2.5 eV has been obtained from the light-emitting structures based on the Ge-ion-implanted SiO_2. The EL mechanisms have been discussed. In addition, the effects of implant energy and dose on the EL behavior have been investigated. The enhanced EL intensity with the implant energy has been explained by the enhanced current conduction caused by the alteration of the nc-Ge distribution in the SiO_2 as well as the increase of implant-generated luminescence centers in the SiO_2.

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NOMENCLATURES

CMOS	Complementary Metal Oxide Semiconductor
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DRAM	Dynamic Random Access Memory
EEPROM	Electrical Erasable/Programmable Read Only Memory
EFM	Electrostatic Force Microscopy
EL	Electroluminescence
EMA	Effective Medium Approximation
EPROM	Erasable and Programmable Read Only Memory
EQE	External Quantum Efficiency
FELED	Field-Effect Light-Emitting Device
FET	Field-Effect Transistor
FG	Floating-Gate
FIB	Focused Ion Beam
FN	Fowler-Nordheim
FWHM	Full Width at Half Maximum
GODC	Germanium Oxygen Deficiency Center
HRTEM	High Resolution Transmission Electron Microscopy
ITO	Indium Tin Oxide
ITRS	International Technology Roadmap for Semiconductor
I-V	Current-Voltage
LPCVD	Low Pressure Chemical Vapor Deposition
MBE	Molecular Beam Epitaxy

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSLED	Metal Oxide Semiconductor Light Emitting Device
N^2FC	Nanyang NanoFabrication Center
NBOHC	Non-Bridging Oxygen Hole Center
nc-Ge	Ge nanocrystals
nc-Si	Si nanocrystals
NOV	Neutral Oxygen Vacancy
NVM	Non-Volatile Memory
ONO	Oxide Nitride Oxide
P/E	Program / Erase
PECVD	Plasma Enhanced Chemical Vapor Deposition
PF	Poole-Frenkel
PL	Photoluminescence
PLD	Pulse Laser Deposition
PMT	Photomultiplier Tube
RF	Radio Frequency
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscope
SET	Single Electron Tunneling
SIMS	Secondary Ion Mass Spectroscopy
SMU	Source Measurement Unit
SRIM	Stopping and Range of Ions in Matter
TCAD	Technology Computer Aided Design
TEM	Transmission Electron Microscopy

UHVCVD	Very High Vacuum Chemical Vapor Deposition
ULSI	Ultra Large Scale Integration
UV	Ultra-Violet
VLSI	Very Large Scale Integration
WORM	Write Once Read Many Times
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction

Chapter 1 Introduction

This thesis studies the electrical and optoelectronic properties of Ge-ion-implanted SiO_2 thin films embedded with Ge nanocrystals (nc-Ge) for applications in non-volatile memories and light-emitting devices. This chapter introduces the background, motivation, objective and major contributions of this thesis. Details of this study are presented in the following chapters.

1.1 Brief introduction to non-volatile memory devices

Non-volatile memory represents a class of solid-state memory whose contents are retained even if the electric power is turned off. That is in contrast to the volatile memory, e.g., dynamic random access memory (DRAM), which will lose the stored information without the electric power. The history of non-volatile memory started in mid-1960s with the invention of the first non-volatile memory cell by Kahng and Sze [1]. Since then, various non-volatile memory structures have been invented, including erasable and programmable read only memory (EPROM) [2], electrical erasable/programmable read only memory (EEPROM) [3], and Flash memory [4]. Starting from the mid-1990s, the development of Flash memory and the expansion of battery-supplied consumer electronic appliances such as mobile phones, digital music players and digital cameras have ignited the dramatic growth of the non-volatile memory market, which is dominated by the Flash memory. In 2009, the worldwide sales of Flash are predicted as $15.9 billion US dollars, which accounts for 8% percent

of the total semiconductor sales [5]. Flash is also projected to grow over the next five years with an average annual growth of 17% until it reaches an estimated $34.3 billion US dollars by 2014 [5].

The current Flash memory structure is based on the floating-gate (FG), which is a polycrystalline silicon layer completely surrounded by the gate dielectric of a field-effect transistor (FET). During the device operations, charges can be injected into or removed from the FG by the applied electric field. The amount of charges stored in the FG can be easily detected since it is directly proportional to the threshold voltage. The two most common types of Flash memory, NOR Flash [6] and NAND Flash [7, 8], are based on the FG design. According to the 2008 International Technology Roadmap for Semiconductors (ITRS), the FG-based Flash technology has reached the 40 nm node with a cell size of 0.0064 μm^2 for the NAND Flash, and 50 nm node with a cell size of 0.025 μm^2 for the NOR Flash [9]. Following the ITRS, several prototypes, such as the 120 mm^2 16 Gb 4-level NAND flash using 43 nm technology [10], 16 Gb 16-level NAND Flash with a cell size of 0.006 μm^2 using 70 nm technology [11], and the NOR Flash with a cell size of 0.024 μm^2 using 45 nm technology [12], have been demonstrated.

1.2 Brief introduction to Si-compatible optoelectronic devices

Optical technology for the use of handling information has been around for several decades. For example, the optical fiber communication is an indispensable technique for dealing with the growing demand for data transfer, communications and network system. Another example is the success of various portable optical storage

mediums such as CD and DVD which offer low-cost and high-density information storage. Traditionally, several optoelectronic functional units, such as light source, modulator, switch and detector, are coupled electrically and/or optically with many other components to realize system functions needed for practical applications. Recently, the constantly growing demand of compact systems capable of performing new and increased numbers of operations has encouraged the integration of these optoelectronic devices with other optical and electronic circuits [13]. The optoelectronic integration can reduce the manufacturing cost and improve the system reliability. The future trend of optoelectronic integration would be the realization of optical interconnects for the chip-to-chip and intra-chip communication, because the traditional electrical interconnects based on metal wires are now suffering from substantial propagation delay, high power consumption, and low bandwidth as the line width of the wires reduce [14].

Si is the choice of material for modern microelectronics, and Si-based microelectronic devices, which are fabricated by the mainstream complementary metal-oxide-semiconductor (CMOS) technology, constitute over 95% of the market of semiconductor devices [15]. Thus, the optoelectronic integration on Si substrates using CMOS-compatible technology is the most cost-effective approach. Using CMOS-compatible technology also allows very large scale integration (VLSI) with great flexibility in device geometries including nanostructures, optical cavity and motion structures [16]. However, the current optoelectronic devices use a wide range of different materials, and most of them are not CMOS-compatible. For example, common light source and photodiodes are mainly based on Group III-V

semiconductor materials, while modulators and switches are based on $LiNbO_3$ or $BaTiO_3$ [17]. Therefore, to realize the CMOS-compatible optoelectronic integration on Si substrate, the fabrication of individual optoelectronic devices using existing CMOS technology is important.

1.3 Nanocrystals

Nanotechnology, which presents a collection of technologies that operates, analyzes and controls materials at the nano-scale regime, is beginning to be seen in products in our daily life [18]. The semiconductor nanocrystal, which consists of a few tens to a few tens of thousands of atoms aligned in a crystalline form and has a typical size of 1 – 10 nm, is one of the essential building blocks in nanotechnology. Recently, SiO_2 films embedded with Si nanocrystals (nc-Si) and Ge nanocrystals (nc-Ge) have attracted much attention for their promising applications in non-volatile memories as well as Si-compatible optoelectronic devices.

1.3.1 Roles of nanocrystals for next-generation non-volatile memories

The modern electronic applications demand the down scaling of non-volatile memory devices in pursuit of larger capacity, smaller device area, lower power consumption and higher operating speed. However, the conventional FG design has a limited potential for the continued scaling of the device structures. The limitation mainly results from the extreme requirements on the tunnel oxide separating the FG and the Si substrate [19]. In a FG-based structure, the tunnel oxide has to be thin in order to achieve program / erase operations with fast speed and low voltage (i.e., low

power consumption). However, the reduction of tunneling oxide thickness causes the degradation of retention performance and raises reliability issues. To achieve data retention time of 10 – 20 year and a lifetime of 10^5 cycles as requested by the industry, the Flash manufacturers have to compromise at a tunnel oxide thickness of 7 – 9 nm which is expected to remain constant from 2007 to 2015 [9]. As a result, the performance of conventional FG-based non-volatile memory has only limited improvement with device scaling, and the semiconductor manufacturers and researchers are constantly exploring new device structures to replace conventional FG design.

To overcome the limitation in conventional FG-based memory design, the use of nanocrystals to replace conventional FG has been proposed by Tiwari *et al.* [20]. In a nanocrystal-based memory, discrete charge storage nodes made of nanocrystals are embedded in the gate dielectric (typically SiO_2) of a field effect transistor. Each nanocrystal is surrounded by the gate dielectric and is located at a small tunneling distance away from the Si substrate. To program the device, electrons are injected from the inversion layer in the Si substrate into nanocrystals via tunneling when the control gate is positively biased with respect to the Si substrate. Due to the smaller bandgap of the nanocrystal material, i.e., Si or Ge, as compared to the surrounding SiO_2 barriers, long-term charge storage in the nanocrystal is achieved. Although each nanocrystal only stores a few electrons, the collective effect of many charged nanocrystals shifts the threshold voltage of the device. The nanocrystal-based memory has the potential to use a thinner tunnel oxide without sacrificing the performance of charge retention. Moreover, the nanocrystal-based non-volatile memory is more robust

and fault-tolerant due to the nature of discrete charge storage as well as the Coulomb blockage effect which limits the removal of an electron from the nanocrystal.

1.3.2 Roles of nanocrystals for Si-compatible optoelectronic devices

The integration of photonic and optoelectronic functional units into mainstream microelectronic circuits using Si-based CMOS technology has generated much research interest. Many promising demonstrations, such as optical modulators [21, 22], switches [23, 24], detectors [25, 26], and low-loss waveguides [27, 28], have been reported. However, it still remains a challenge to build a CMOS-compatible light emitter. It is known that bulk crystalline Si and Ge are poor in light emission at room temperature, mainly because of their indirect bandgaps which result in a phonon-mediated recombination process with low probability. In addition, fast non-radiative processes such as Auger or free carrier absorption prevent the population inversion for silicon optical transitions at the high pumping rates needed to achieve optical amplification. Thus, a Si-compatible light emitter is still under extensive research.

Among many solutions to build a Si-compatible light emitter, the use of Group-IV nanocrystals (i.e., nc-Si or nc-Ge) embedded in SiO_2, which was motivated by the early work on visible light emission from porous silicon [29, 30], has recently attracted great interest. The major reason for using nanocrystals is the three-dimensional quantum confinement effect which leads to the expansion of the optical bandgap as a result of the size reduction of nanocrystals [31]. That provides a possible way to relax the momentum conservation requirement and allows Group IV semiconductors with indirect bandgap to possess efficient light emission properties.

Besides, the defects induced by the nanocrystal synthesis techniques could also contribute to the light emission from SiO_2 embedded with nanocrystals.

1.3.3 Ge nanocrystals

To meet the demand of design, development and eventually manufacturing of non-volatile memories as well as Si-compatible light-emitting devices based on Group-IV nanocrystals, extensive research must be carried out to understand the synthesis, physics and device behavior of nanocrystals embedded in SiO_2. Although the initial research activities on Group-IV nanocrystals were mainly focused on nc-Si, nc-Ge is also of great interest. Bulk Ge has a smaller bandgap, smaller electron and hole effective masses and a larger dielectric constant as compared to bulk Si. In addition, in bulk Ge the direct gap (E_0 ~ 0.88 eV) is close to the indirect gap (E_g ~ 0.75 eV) [32]. Thus, it is considered that quantum size effects would appear more pronounced in nc-Ge than in nc-Si [33]. As a result, as compared to Si, Ge is a more promising choice of material for the nanocrystal-based applications in non-volatile memories and Si-compatible light-emitting devices. Many studies have demonstrated that the synthesis of nc-Ge embedded in SiO_2 is fully compatible with the CMOS technology.

1.4 Motivation

In view of the important roles of nc-Ge in non-volatile memory devices and Si-compatible light-emitting devices, the electrical and optoelectronic properties of nc-Ge deserve more thorough investigation. Nc-Ge embedded in SiO_2 can be synthesized by

many techniques [34-38], which have their own advantages and disadvantages. Among them, Ge ion implantation into SiO_2 films, followed by the high temperature annealing, is deemed as one of the most promising candidates for producing electrically and chemically stable nc-Ge embedded in SiO_2. The ion implantation technique is fully compatible with the existing CMOS technology and is able to control the nc-Ge concentration and depth distribution by adjusting the implant energy and Ge ion dose [39]. For example, an orderly 2-D array or a narrow distribution of nc-Ge in SiO_2 is usually required for the non-volatile memory device application [40], and that can be achieved by the use of low-energy (e.g., 2 – 8 keV) ion implantation. On the other hand, to produce nc-Ge dispersed in SiO_2 which is occasionally required by some optoelectronic applications [41], a higher implant energy could be used. Besides its flexibility, the ion implantation process also provides good homogeneity and good reproducible profiles. As a result, in this thesis we focus on SiO_2 thin films embedded with nc-Ge synthesized by a Ge ion implantation technique.

The conventional SiO_2 film has long been studied since the fabrication of the first metal-oxide-semiconductor field-effect transistor (MOSFET) in 1960 [42], and it is well accepted that the current transport in the SiO_2 system depends on many factors, e.g., the material composition, fabrication process, film thickness, trap density, and so on. However, the current transport behavior of Ge-ion-implanted SiO_2 thin films has not been studied in detail. Ge-ion-implanted SiO_2 thin films differ from the pure SiO_2 in many aspects: 1) nc-Ge are formed in the SiO_2 matrix [41, 43-45], 2) defects / traps are created in the bulk of oxide film in a way similar to those cases of Cs- and B-ion-implanted oxide films [46]. For the applications of non-volatile memory and light-

emitting devices, the Ge-ion-implanted SiO_2 embedded with nc-Ge serves as a gate dielectric layer sandwiched by the gate electrode and the Si substrate. Since both the charge storage and the light emission are caused by the charge injection into the Ge-ion-implanted SiO_2, an understanding of the current transport behavior of the Ge-ion-implanted SiO_2 is necessary.

Besides the current transport behavior, the successful operation of non-volatile memory devices based on nc-Ge relies on the charge trapping and charge retention in the SiO_2 embedded with nc-Ge. Although the Ge-ion-implanted SiO_2 samples embedded with nc-Ge have been previously demonstrated to possess memory effects [43, 47, 48], their charge trapping and charge retention behavior has not been systematically studied. One of the advantages of the Ge ion implantation technique is the precise control of the density and depth distribution of the implanted ions by the process parameters such as implant energy, implant dose and annealing temperature. Thus, it is essential to understand the influences of these process parameters on the charge trapping and charge retention behavior. Besides, since the implanted Ge atoms can dissolve and diffuse in the SiO_2 matrix [49], excess Ge atoms are expected to be found in the oxide between adjacent nc-Ge particles as well as in the tunnel oxide separating the nc-Ge and the Si substrate. These dissolved Ge atoms could act as charge transfer sites and cause charge loss from the nc-Ge. It is important to understand how these dissolved Ge atoms affect the retention of charges trapped in nc-Ge.

For the Ge-ion-implanted SiO_2 thin films, due to the inclusion of nc-Ge in SiO_2, the dielectric properties of SiO_2 will be modified. The possible contributing factors

include the depth and the distribution of nc-Ge in SiO_2 and the change in the dielectric constant of nc-Ge as a result of the reduced size. As a consequence, the capacitance of the metal-oxide-semiconductor (MOS) structure is affected by the nc-Ge embedded in SiO_2. Experimentally, it is possible to measure the MOS capacitance using the conventional capacitance-voltage (*C-V*) technique. However, for the sake of design and modeling of memory structures based on nc-Ge, a modeling approach to determine the influence of nc-Ge on the MOS capacitance is essential. Such an approach is still not available in the literature.

Electroluminescence (EL) is an important optoelectronic property which is directly related to light-emitting applications. Studies on the visible EL from the Ge-ion-implanted SiO_2 films have been reported [50-54]. However, in these previous studies, the Ge ion implantation has been carried out at high energies (75 – 350 keV) and the SiO_2 thickness is in the range of few hundred nanometers. Indeed, for practical EL applications, a thinner Ge-implanted SiO_2 film is required to achieve a lower operation voltage and higher injection efficiency. Hence lower implant energy should be used. In addition, a proper understanding about the relationship between the EL and the ion implantation conditions, i.e., implant energy and dose, is essential for the design and integration of light-emitting devices based on the Ge ion implantation technique. Such a relationship has not yet been systematically investigated for the Ge-implanted SiO_2 thin films.

1.5 Objective and scope of research

In this thesis, Ge ion implantation followed by high-temperature annealing has been used to synthesize nc-Ge embedded in SiO_2 thin films. The main objective of this thesis is to investigate the electrical and optoelectronic properties of the Ge-ion-implanted SiO_2 thin films for applications in non-volatile memory and Si-compatible light-emitting devices. The scope of the research and the approach are as follows:

(1) Synthesis of nc-Ge embedded in SiO_2 thin films using Ge ion implantation followed by high temperature annealing. Various distributions of nc-Ge in SiO_2 thin films are achieved by varying the implantation energy and Ge ion dose.

(2) Characterization of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge using transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), and x-ray photoelectron spectroscopy (XPS). The obtained structural and chemical properties are used for the analysis of electrical and optoelectronic properties.

(3) Investigation of the current transport behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge using the current-voltage (*I-V*) measurement under various temperatures.

(4) Characterization of the charge storage behavior, including charge trapping and charge retention of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge using conventional capacitance-voltage (*C-V*) methods.

(5) Investigation on the influences of various synthesis conditions, including the annealing temperature, implant energy and Ge ion dose, on the charge trapping and charge retention behavior. The structural and chemical properties of nc-Ge

embedded in SiO_2 thin films synthesized by different conditions are correlated to the electrical behavior obtained from the *C-V* measurements.

(6) Investigation of the charge loss as a result of the lateral charge transfer along the nc-Ge distributed region and the charge leakage to the Si substrate.

(7) Development of an approach to calculate the MOS capacitance of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge. The calculated capacitances for various nc-Ge distributions are compared with the measurement data.

(8) Fabrication of light-emitting devices based on a structure of indium tin oxide (ITO) / SiO_2 embedded with nc-Ge / *p*-Si substrate.

(9) Investigation of the EL and the current conduction behavior of the light-emitting devices based on nc-Ge.

1.6 Major contributions of the thesis

The major contributions of this thesis are listed as follows:

(1) Current transport behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been investigated.

a) Identified the different conduction mechanisms dominating in different oxide field regions for the narrow distribution of nc-Ge near the SiO_2 surface synthesized by low implant energy as well as the broad distribution of nc-Ge throughout the SiO_2 synthesized by high implant energy.

b) Proposed appropriate models to explain the current transport behavior.

c) Reported the conduction modulation of SiO_2 embedded with nc-Ge induced by the ultraviolet (UV) illumination. Charging and discharging in the nc-Ge

caused by UV illumination have been identified as the cause of the conduction modulation.

(2) Charge trapping and charge retention behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been investigated.

a) Investigated the dependences of the amount of trapped charges on the polarity and magnitude of the charging voltage as well as the charging time. The retention behavior of trapped charges after charging has also been studied.

b) Investigated the influence of annealing on the charge trapping and charge retention behavior. The structural and chemical properties of the nc-Ge embedded in SiO_2 thin films have been correlated to the electrical behavior.

c) Investigated the influences of the implant energy and implant dose on charge trapping and charge retention behavior.

d) Determined the roles of the lateral charge transfer along the nc-Ge distributed region and the charge leakage to the Si substrate in the charge retention.

(3) Calculation of the MOS capacitance of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been performed

a) Proposed an approach to model the MOS capacitance including consideration of the distribution of nc-Ge in SiO_2 and the reduction in the static dielectric constant of nc-Ge as a result of the nanometer size.

b) Determined the influence of implant energy and dose on the MOS capacitance.

c) Determined the static dielectric constant of nc-Ge embedded in SiO_2 based on the proposed approach.

(4) EL behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been investigated.

a) Fabricated the light-emitting structures based on the SiO_2 thin films embedded with nc-Ge.

b) Demonstrated visible EL from the Ge-ion-implanted SiO_2 thin films.

c) Investigated EL and current conduction behavior and discussed the related EL mechanisms.

d) Investigated the enhancement in both the EL intensity and external quantum efficiency by changing the implant conditions, i.e., implant energy and Ge ion dose.

1.7 Organization of the thesis

This thesis is mainly focused on the studies of electrical and optoelectronic properties of Ge-ion-implanted SiO_2 thin films embedded with nc-Ge and their applications. **Chapter 1** briefly introduces the roles of Ge nanocrystals in non-volatile memory devices and Si-compatible light-emitting devices. The motivation, objective and scope of the research and the major contributions of this thesis are also given in this chapter.

Chapter 2 presents a literature review of the research on nc-Ge. It begins with discussion of the ion implantation technique and other common techniques for the synthesis of nc-Ge embedded in SiO_2. After that, the common techniques used to

characterize the structural, material, electrical and optoelectronic properties of nc-Ge embedded in SiO_2 are reviewed. Finally, the applications of nc-Ge in non-volatile memory devices and Si-compatible light-emitting devices are discussed in detail.

In **Chapter 3**, the current transport behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge is investigated. The characteristics of gate current density versus oxide field at various temperatures are obtained, and the different transport mechanisms dominating in the different oxide field regions are discussed. Appropriate models are proposed to explain the current transport behavior. In addition, a conduction modulation effect in SiO_2 thin films embedded with nc-Ge caused by UV illumination is reported.

In **Chapter 4**, the charge trapping and charge retention behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge is investigated. The dependences of trapped charges on the polarity and magnitude of the charging voltage and the charging time are studied. Besides, the influences of thermal annealing, implant energy and implant dose on the charge trapping and charge retention behavior are investigated. In addition, the charge loss caused by the lateral charge transfer along the nc-Ge distributed region and charge leakage to the Si substrate is also studied.

Chapter 5 presents an approach to calculate the MOS capacitance of the Ge-ion-implanted SiO2 thin films embedded with nc-Ge. Based on this approach, the influences of implant energy and dose on the MOS capacitance are studied, and the static dielectric constant of nc-Ge embedded in SiO_2 is determined. The calculated

capacitances for various nc-Ge distributions and the measurement results are compared.

In **Chapter 6**, light-emitting devices based on an ITO / SiO_2 embedded with nc-Ge / *p*-Si substrate structure are fabricated. The EL properties of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge are investigated. The EL mechanisms are discussed. The dependence of the EL properties on the implant energy and dose is also investigated.

Finally, **Chapter 7** summarizes the research work carried out in this thesis. Recommendations for future work are also given in this chapter.

Chapter 2 Literature Review

2.1 Introduction

Although the market share of non-volatile memories based on floating-gate (FG) has been continuously growing, the conventional FG design has a limited potential for continuing device scaling. The invention of a nanocrystal-based memory structure in 1995 by Tiwari *et al.* [20, 55] has been considered as one of the most promising solutions to overcome the scaling limit of conventional FG-based non-volatile memories [19]. With the Group-IV nanocrystals embedded in the gate oxide of a memory cell, the nanocrystal-based memory design preserves the conventional operating principle of FG-based memories. Moreover, the fabrication is fully compatible with mainstream complementary-metal-oxide-semiconductor (CMOS) technology. As a result, it would be easy for the industry to migrate from the conventional design to the nanocrystal-based memory structure.

Nanocrystals also find potential applications in Si-compatible light-emitting devices. This has been motivated by the early work on visible light emission from porous silicon [29, 30]. Although Group-IV semiconductors are indirect bandgap materials which are inefficient for emission of light, the nanocrystals of Group-IV semiconductors possess properties different from their bulk counterparts as a result of the three-dimensional quantum confinement of carriers, which modifies the band structures and leads to the expansion of optical bandgap [31]. By embedding the

Group-IV nanocrystals into a robust dielectric layer such as SiO_2, many researchers have demonstrated light emission, which open up new possibilities of integrating the light emitter into an optoelectronic circuit with all functional units fabricated by mainstream CMOS-compatible technology [51].

Initially, studies were mainly focused on Si nanocrystals (nc-Si) embedded in SiO_2. However, when compared to nc-Si, Ge nanocrystals (nc-Ge) are expected to possess more pronounced quantum size effects due to the smaller bandgap, smaller electron and hole effective masses as well as the larger dielectric constant [33]. As a result, the interest in nc-Ge embedded in SiO_2 has grown recently. In this chapter, we briefly review the synthesis, characterizations and device applications of nc-Ge embedded in SiO_2.

2.2 Synthesis techniques for nc-Ge embedded in SiO_2

The promising applications of nc-Ge embedded in SiO_2 have motivated researchers and industry to search for suitable nc-Ge synthesis techniques. Many techniques have been demonstrated [34-38], and each of them has its own advantages and disadvantages. One important consideration is the effective integration with mainstream CMOS technology. Besides, the parameters like the size, density and depth distribution of nanocrystals have to be properly controlled in order to meet the stringent requirements imposed by the application of nc-Ge embedded in SiO_2. The common techniques used to synthesize nc-Ge embedded in SiO_2 are reviewed in this section. First of all, the ion implantation technique, which was employed to fabricate

the samples for this thesis, is discussed. After that, other common techniques are reviewed. A comparison is also given for the techniques discussed in this section.

2.2.1 Ion implantation technique

Ion implantation is a process whereby energetic dopant ions are made to impinge on the target, resulting in the penetration of these ions below the target surface and thereby giving rise to controlled, predictable dopant distributions [56]. Fig. 2-1 illustrates the basic principle of an ion implantation process. The ions produced from the source are selected by a mass separator and accelerated by a high voltage to form a high-velocity beam of ions which can penetrate the surface of substrate films. The implanted ions can eventually lose their energy as a result of the collision with the target atoms. The stopping of ions is a controllable process, and the distance of ion stopping follows a Gaussian distribution. The ion implantation is usually carried out in a vacuum chamber at a very low pressure (10^4 – 10^5 Torr). Because of the advantages of masking flexibility, high throughput, good extendibility to larger wafers, and the ability to form impurity profiles which are not possible with simple diffusion process, ion implantation is a major process in modern semiconductor manufacturing [57].

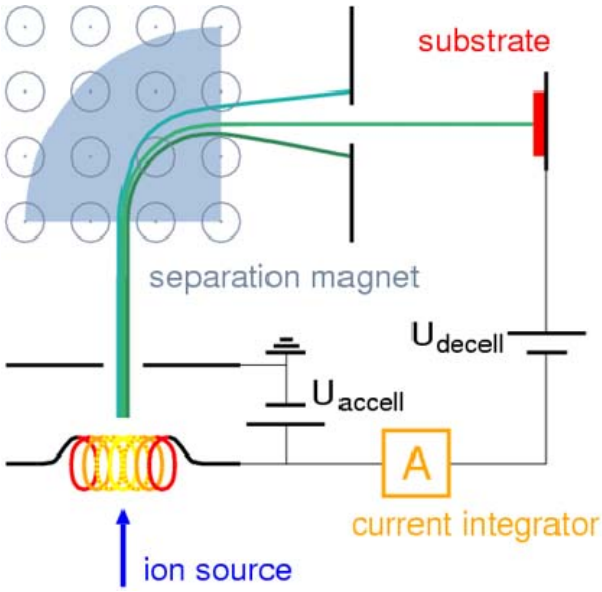

Fig. 2-1 Illustration of the basic principle of the ion implantation process.

Ion implantation combined with a subsequent thermal anneal has been demonstrated as a promising technique to synthesize nc-Ge in SiO_2 [34, 41, 47, 50, 52, 58-60]. In a typical fabrication process, Ge ions are implanted into the thermally grown SiO_2 film. After that, high-temperature annealing in a pure N_2 or Ar ambient is carried out to induce the precipitation of nc-Ge in SiO_2. The key advantage of such a technique is its flexibility in controlling the density and depth distribution of the nc-Ge in SiO_2, because the implanted Ge profile can be precisely and reproducibly controlled by the implant energy and dose. For example, a broad distributions of nc-Ge embedded in relatively thick (in the range of few hundred nanometers) SiO_2 films has been achieved by ion implantation at high energies from 75 - 450 keV [34, 50-52, 58]. On the other hand, an orderly two-dimensional array of nc-Ge embedded in thin SiO_2 film has also been demonstrated by using a low-energy (typically < 10 keV) Ge ion implantation [40].

2.2.2 Other synthesis techniques

Due to the promising applications of nc-Ge in non-volatile memory and optoelectronic devices, various other techniques to synthesize nc-Ge have been reported. Besides the ion implantation technique, other common techniques to synthesize the nc-Ge embedded in SiO_2 include solution-based processes using the sol-gel method [35, 61, 62], low-pressure chemical vapor deposition (LPCVD) of nc-Ge onto a SiO_2 surface followed by the deposition of a capping SiO_2 layer [36, 63, 64], co-sputtering of Ge and SiO_2 [37, 65-70] and selective oxidation of $Si_{1-x}Ge_x$ [38, 71-79]. In this section, these common techniques are briefly reviewed.

2.2.2.1 Sol-gel technique

The sol-gel process is a wet-chemical technique commonly used to prepare semiconductor and metal nanoparticles dispersed in a SiO_2 layer. It can produce glasses of unusual composition at temperatures lower than those required by the conventional melting technique. Using the sol-gel method, CdS, CuCl, CdTe, PbS, Ag and Au nanoparticles embedded in SiO_2 glasses have been synthesized [80-85]. The preparation of nc-Ge embedded in SiO_2 glass using the sol-gel method was first reported by Nogami and Abe [35]. In their process, silica glass containing 7 wt% Ge was prepared by the sol–gel method using $Si(OC_2H_5)_4$ (i.e., tetraethyl orthosilicate, or TEOS) and $GeCl_4$ as starting materials. After the heat treatment, nc-Ge with sizes of ~ 5 nm embedded in the SiO_2 glass can be obtained. However, due to the rapid hydrolysis rate of $GeCl_4$, it is difficult to control the reaction and the nc-Ge size. An improved sol-gel method using TEOS and 3-trichlorogermanium propanoic acid (Cl_3–

Ge–C_2H_4–COOH) as starting materials was proposed by Yang *et al.* [61, 62]. The nc-Ge size can be varied from 1 – 13 nm. The SiO_2 glasses embedded with nc-Ge exhibit visible PL [35, 62], thus they have potential optical applications. However, for the sol-gel method, so far there is still no report on the synthesis of nc-Ge embedded SiO_2 in the form of thin films. It is still questionable whether the solution-based technique can be integrated into the mainstream CMOS process.

2.2.2.2 Low-pressure chemical vapor deposition

Chemical vapor deposition (CVD) technique makes use of one or more gaseous precursors which react and decompose on the substrate surface to deposit the desired film. The low-pressure chemical vapor deposition (LPCVD) operates at sub-atmospheric pressures in order to reduce unwanted gas-phase reactions and improve film uniformity across the wafer. The direct deposition of an orderly two-dimensional array of nanocrystals on the SiO_2 surface without the need of thermal annealing has been reported by some research groups [36, 86-89]. The principle is to terminate the deposition process in the early stage before the formation of a continuous film. An additional deposition of capping SiO_2 (i.e., control oxide) is required to make the nanocrystals embedded in SiO_2. Several groups have reported the growth of Si nanocrystals onto a SiO_2 surface [86-89]. However, the growth of nc-Ge onto a SiO_2 surface is difficult because the gaseous precursor GeH_4 does not react with SiO_2. Baron *et al.* have demonstrated a two-step process for the direct growth of nc-Ge on SiO_2 [36]. As shown in Fig. 2-2, the technique requires the deposition of small Si nuclei on the SiO_2 surface using SiH_4, followed by the selective growth of nc-Ge on these Si nuclei using GeH_4. The nc-Ge density can be adjusted in between 10^9 to 10^{12}

cm^{-2}, while the nc-Ge size varies between 5 and 50 nm. Since the thickness of the tunnel oxide underneath the nanocrystal layer, the thickness of the control oxide between the nanocrystal layer and the poly-Si gate as well as the density and size of the nanocrystals can be well controlled, the direct growth of nanocrystals onto a SiO_2 surface using a LPCVD technique is practically attractive for non-volatile memory applications. Studies on the memory behavior of nc-Ge embedded in SiO_2 synthesized by LPCVD have been reported [63, 64]. However, the two-step deposition of nc-Ge on SiO_2 introduces additional complexity to the fabrication process.

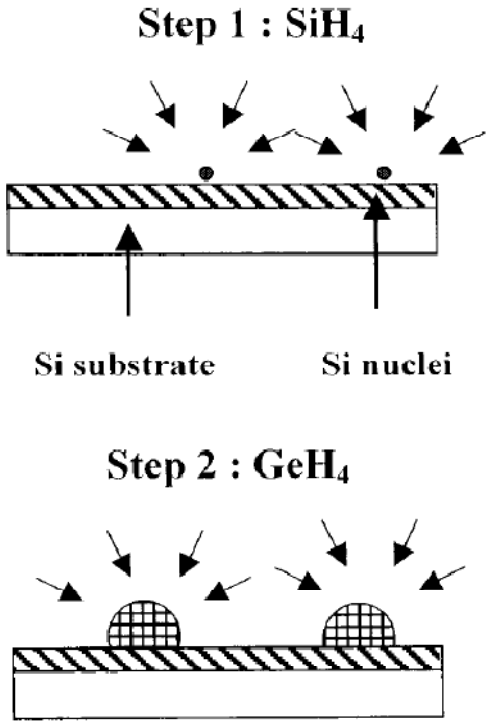

Fig. 2-2 Schematics of the two-step technique to grow nc-Ge on SiO_2 surface (from Ref. [36]).

2.2.2.3 Co-sputtering technique

In a sputtering process, the energetic ions, usually Ar^+, are accelerated toward the target surface by the high-voltage bias between anode and cathode, causing the target material to be sputtered out in a gaseous form and deposited onto the sample surface as a thin film. For a radio-frequency (RF) sputtering system, the sign of the anode-cathode bias is varied at a high rate such that the charge build-up on the insulating target can be avoided. The RF sputtering works well to produce insulating oxide films, such as SiO_2. The simultaneous deposition of two different target materials as a mixture can be achieved by the co-sputtering of either two individual sputtering targets or one primary target attached with small pieces of secondary targets. The synthesis of nc-Ge embedded into SiO_2 has been demonstrated by the co-sputtering of small pieces of Ge wafers attached onto the pure SiO_2 target, followed by furnace annealing at 800 ºC for 30 minutes [65, 66]. Spherical nc-Ge dispersed in the SiO_2 matrix with a mean size of ~ 6.1 nm can be achieved. To avoid the long process duration of conventional furnace annealing, rapid thermal annealing (RTA) has been employed for the synthesis of nc-Ge using the co-sputtering technique [37, 67-70]. At an annealing temperature of 750 ºC, the minimum annealing time can be significantly reduced to 160 s. Studies on the memory effect and luminescence behavior of the co-sputtered SiO_2 thin films embedded with nc-Ge have been reported [37, 66, 68, 90-92].

2.2.2.4 Selective oxidation of $Si_{1-x}Ge_x$

Selective oxidation of a thin polycrystalline $Si_{1-x}Ge_x$ layer is an effective technique to synthesize nc-Ge embedded into SiO_2 [38, 71-79]. This technique usually

starts with the deposition of a layer of $Si_{1-x}Ge_x$ film, followed by dry or wet oxidation with optimized process parameters. The deposition of $Si_{1-x}Ge_x$ film can be performed by many methods, including the co-sputtering of Si and Ge [38, 71, 72], LPCVD [73-76], ultra high vacuum CVD (UHVCVD) [77], ion implantation [78] and molecular beam epitaxy (MBE) [79]. The formation of nc-Ge embedded in SiO_2 replies on the principle that Si in $Si_{1-x}Ge_x$ film can be preferentially oxidized as compared to Ge due to its greater free energy. Using Raman spectroscopy, three distinct stages were observed during the oxidation: 1) growth of SiO_2 (no Ge-Ge bonds) for a short oxidation time, 2) formation of Ge-Ge bonds and segregation of nc-Ge from the $Si_{1-x}Ge_x$ film for a longer oxidation time; and 3) complete oxidation for a very long oxidation time [76]. The annealing ambient, i.e., dry or wet oxidation also affects the formation of nc-Ge as well as the luminescence properties of the thin film [73]. Thus, proper control of the annealing conditions, e.g., ambient, temperature and duration, is crucial for the synthesis of nc-Ge in SiO_2 using the selective oxidation of $Si_{1-x}Ge_x$.

2.2.3 Comparison of various nc-Ge synthesis techniques

Besides the abovementioned techniques, others techniques such as e-beam evaporation [93-95], pulsed laser deposition (PLD) [96-98] and nano-patterning using focused ion beam (FIB) [99, 100], have also been demonstrated for the synthesis of nc-Ge in the SiO_2 matrix or on the SiO_2 surface. Each of them has its own advantage and disadvantages. Two important factors, namely the size and distribution of nc-Ge in SiO_2, affect the device applications of nc-Ge [101]. Table 1 summarizes the size and distribution produced by the common nc-Ge synthesis techniques.

Table 1 Comparison of various nc-Ge synthesis techniques.

Synthesis Technique	**Distribution of nc-Ge in SiO_2**		**Size of nc-Ge**
	Dispersed in SiO_2	**Confined in an orderly 2-D array**	
Ion implantation	√	√	6 nm [34] 3 – 6 nm [102]
Sol-gel	√		5 nm [35] 1 – 13 nm [61, 62]
LPCVD (direct deposition)		√	5 – 50 nm [36]
Co-sputtering	√	√	6 nm [37, 66] 2.1 – 25.4 nm [91]
Oxidation of $Si_{1-x}Ge_x$		√	5.5 nm [75] 10 nm [71]
E-beam evaporation		√	6 nm [94] 11 nm [93]
PLD		√	3 nm [97]
Nano-patterning using FIB		√	20 nm [99] 25 – 28 nm [100]

As summarized in Table 1, all techniques can produce Ge particles at the nanometer size. However, good control of the size distribution is crucial to avoid complication in the characterization of quantum confinement effects. For a specific synthesis technique, the size and size distribution of nc-Ge are greatly affected by the synthesis conditions. On the other hand, the requirements for the distribution of nc-Ge

in SiO_2 depend on the specific device application. For non-volatile memory device applications, an orderly 2-dimensional (2-D) array or a narrow distribution of nc-Ge in SiO_2 with a good control over the size and uniformity of areal nanocrystal density is usually required [40], while for optoelectronic device applications, the nc-Ge particles are usually dispersed in the SiO_2 [41]. As shown in Table 1, some of the synthesis techniques, such as ion implantation and co-sputtering technique, are capable of producing both dispersed and confined distributions of nc-Ge in SiO_2. Other techniques are only suitable for one kind of nc-Ge distribution. As compared to the sputtering process, ion implantation is preferred in terms of good reproducibility and masking flexibility, high throughput, good extendibility to larger wafers, and good process control for a mass production propose [57, 101]. In addition, the synthesis of nc-Ge using Ge ion implantation is fully compatible with mainstream CMOS technology, thus it can be easily integrated into the existing process flow. In this work, Ge ion implantation has been employed for all the fabrications.

2.3 Common characterization techniques

Most of the techniques to characterize nanocrystals embedded in SiO_2 are based on the existing semiconductor characterization techniques. However, the emphasis has to be shifted from the bulk properties to the properties associated with particles with nanometer scale. In Section 2.3.1, the structural and material characterizations which provide essential information for the analysis of experimental results obtained from the electrical and optoelectronic characterizations are reviewed. As far as the semiconductor nanocrystals are concerned, the main objectives of structural and

material characterizations are to describe the physical dimensions, shape and crystal orientation of the nanocrystals and to reveal the atomic and chemical composition of the films embedded with nanocrystals. In Section 2.3.2, the common electrical characterization techniques are discussed. The main purpose is to analyze the charge trapping, charge retention and current transport behavior associated with the SiO_2 embedded with nanocrystals. In Section 2.3.3, the techniques to study the light emission behavior from the SiO_2 embedded with nanocrystals are discussed.

2.3.1 Structural and material characterizations

2.3.1.1 Secondary ion mass spectroscopy

Secondary ion mass spectroscopy (SIMS) is a widely used technique for the identification as well as the depth profiling of elements of a thin solid film. In a typical SIMS measurement, the sample surface is sputtered by a beam of focused energetic primary ions, and the generated secondary ions are accelerated away from the sample surface by a high voltage (typically 4500 V). A fraction of the secondary ions is accepted for the analysis by a mass spectrometer and is collected from a circular image area centered in the scanning region. After passing through the analyzers, the secondary ions are detected. Since the sample surface is sputtered in a controlled way with a known sputter rate, the depth profiles of the detected ions are obtained. SIMS is often used to accurately obtain the doping profiles of boron or phosphorus in Si substrate [103]. For the case of nanocrystals synthesized by the ion implantation technique, SIMS is widely used to determine the depth distribution of nanocrystals

embedded in SiO_2 [104-108]. Fig. 2-3 shows a typical SIMS depth profile of Ge in SiO_2.

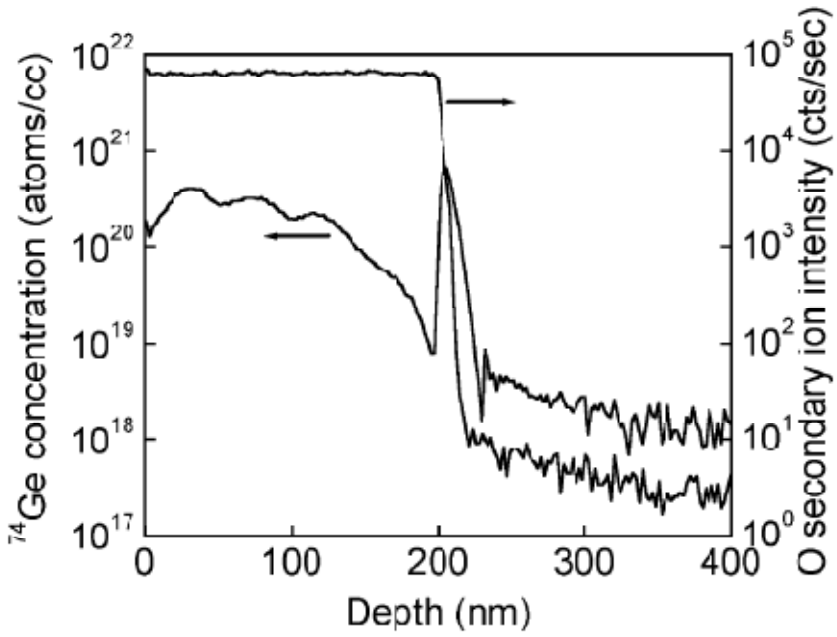

Fig. 2-3 A typical SIMS depth profile of Ge in SiO_2 [108].

If the actual measurement using SIMS is not available, an alternative way to estimate the depth profile of the implanted specie is to use the stopping and range of ions in matter (SRIM) program, which is based on a quantum mechanical treatment of ion-atom collisions [109]. The SRIM simulation provides a reasonable agreement with the actual depth profile measured by SIMS technique [109], and has been employed for the purpose of modeling [110, 111].

2.3.1.2 Transmission electron microscopy

Transmission electron microscopy (TEM) is the major tool for microstructure characterization of materials. During the TEM measurement, a thin specimen is

irradiated with an electron beam. The image formed by the electrons transmitted through the specimen is magnified and recorded via the fluorescent screen coupled by a fiber-optic plate to a CCD camera. Because the De Broglie wavelength of electrons is many orders of magnitude smaller than that of light, the spatial resolution of the TEM is much higher than that in conventional optical microscopy. In a state-of-the-art high-resolution TEM (HRTEM), the spatial resolution is as small as 0.2 nm for an electron energy of 200 keV, and approaches 0.15 nm for an electron energy of 400 keV [112]. For nanocrystals with the size of few nanometers, the HRTEM is an important technique to determine the crystallinity, external shapes, size and distribution of the nanocrystals [113-118]. The electron diffraction pattern which reflects the scattering of electrons by atoms offers additional information about the crystal structure of nanocrystals. Fig. 2-4 shows typical cross-sectional HRTEM images (operated at an electron energy of 200 KeV) of nc-Ge embedded in SiO_2 synthesized by the co-sputtering technique. The microstructure, size and distribution of nc-Ge in SiO_2 can be clearly observed in the HRTEM images.

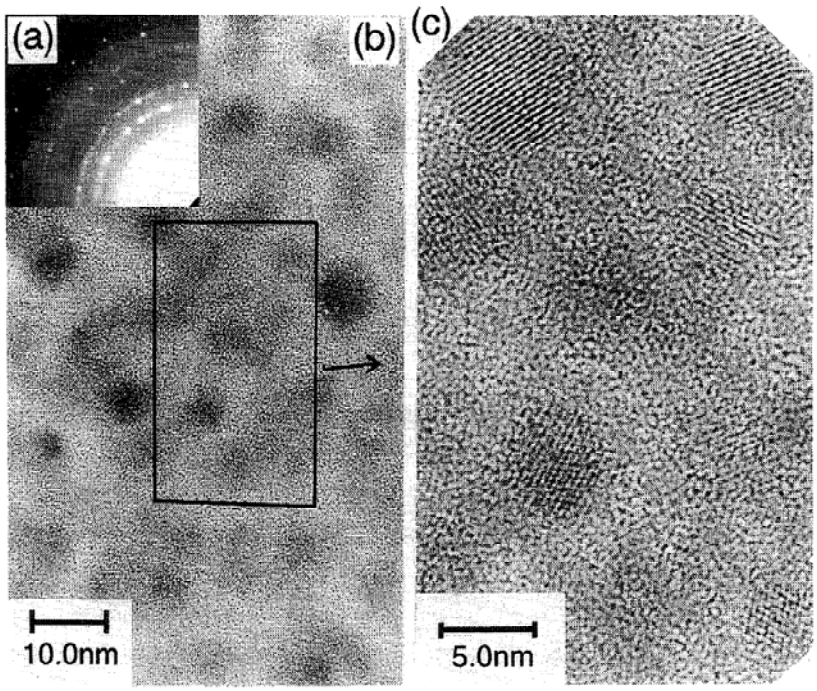

Fig. 2-4 Electron diffraction pattern (a), and cross-sectional HRTEM image for a typical SiO_2 embedded with nc-Ge synthesized by the co-sputtering technique (from Ref. [65]).

2.3.1.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. It is based on the photoemission process whereby photoelectrons are emitted from the material as a result of the absorption of a photon. The XPS spectra are obtained by irradiating the material surface with a beam of x-rays (normally monochromatic Al Kα x-ray corresponding to the photo energy of 1486.71 eV) while simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 to 10 nm of the

material. The XPS technique is useful for determining the chemical structures of dielectric thin films embedded with nanocrystals. The co-existence of elemental Ge and Ge oxides in the SiO_2 embedded with nc-Ge has been revealed by the XPS technique [33, 68, 102]. Fig. 2-5 shows a typical XPS analysis of the nc-Ge embedded SiO_2 thin film deposited by the CVD method. From this example, the changes in the chemical structure after thermal annealing can be clearly identified as the reduction of GeO_x and the formation of elemental Ge. Moreover, the XPS analysis also yields useful information about changes in the electronic structure of nanocrystals which are manifested as variations in the core-level biding energies. Shifts in the binding energy with the reduction of particles size have been reported [105, 119-122].

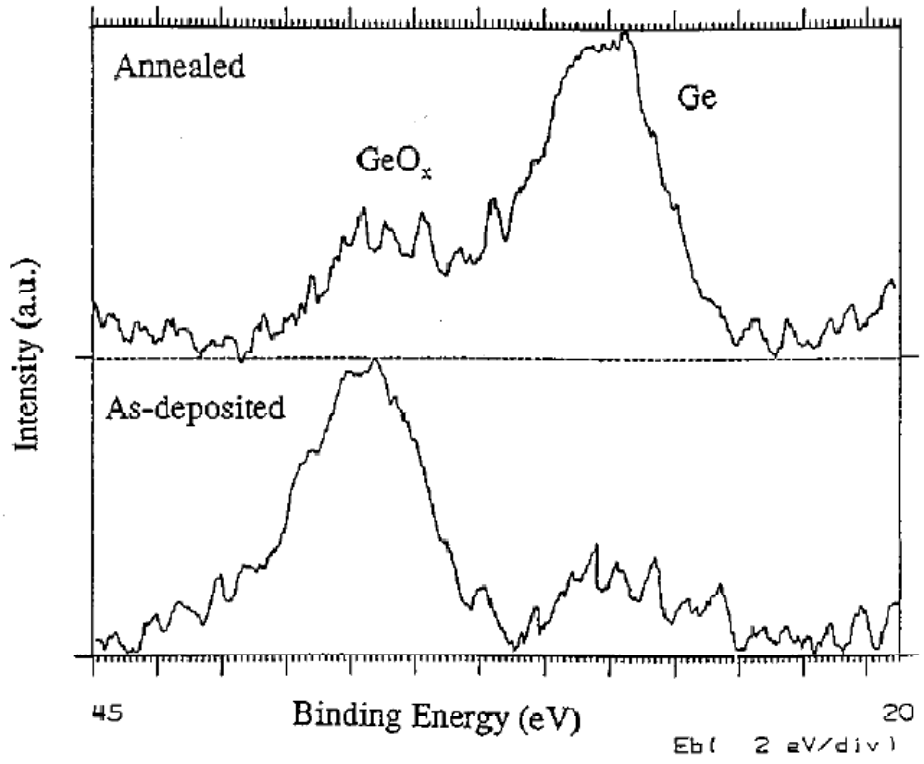

Fig. 2-5 Typical XPS spectra for the as-deposited and annealed nc-Ge in SiO_2 (from Ref. [33]).

2.3.1.4 X-ray diffraction

X-ray diffraction (XRD) is a non-destructive analytical technique to reveal information about the crystallographic structure, chemical composition, and physical properties of materials and thin films. It is based on the principle that diffraction occurs as x-ray interacts with a regular lattice structure whose inter-atomic distance is about the same order as the wavelength of the x-ray. From the XRD spectra, the specific crystal orientations of nanocrystals formed in the dielectric film can be identified [90, 102]. Besides, many studies have also demonstrated that XRD is effective in determining the average size of nanocrystals embedded in dielectric films [123-127]. That is because for the diffraction of a monochromatic x-ray beam from nanocrystals which are finite in size (less than 100 nm), the number of parallel planes available is too small for a sharp diffraction maximum to build up. As a result, the peak in the diffraction pattern becomes broadened. The mean size (D) of nanocrystals embedded inside a SiO_2 matrix can be estimated from the x-ray diffraction measurement using Scherer's equation [128]

$$D = \frac{K\lambda}{\Delta\theta\cos(\theta_B)} \tag{2.1}$$

where λ is the wavelength of the x-ray, $\Delta\theta$ is the full width at half maximum (FWHM) of the Bragg peak, θ_B is the Bragg angle, and K is a constant (~ 1). The exact value of K depends on the specific shape and size distribution of the nanocrystals as well as the crystallographic orientations of the nanocrystals [124]. Fig. 2-6 shows typical XRD patterns for the nc-Ge embedded in SiO_2. The peaks in the XRD spectra correspond to

the (111) and (311) oriented nc-Ge. The existence of GeO_2 is also revealed in the XRD spectra. From the spectrum, the average size of nc-Ge is determined as 7 – 8 nm.

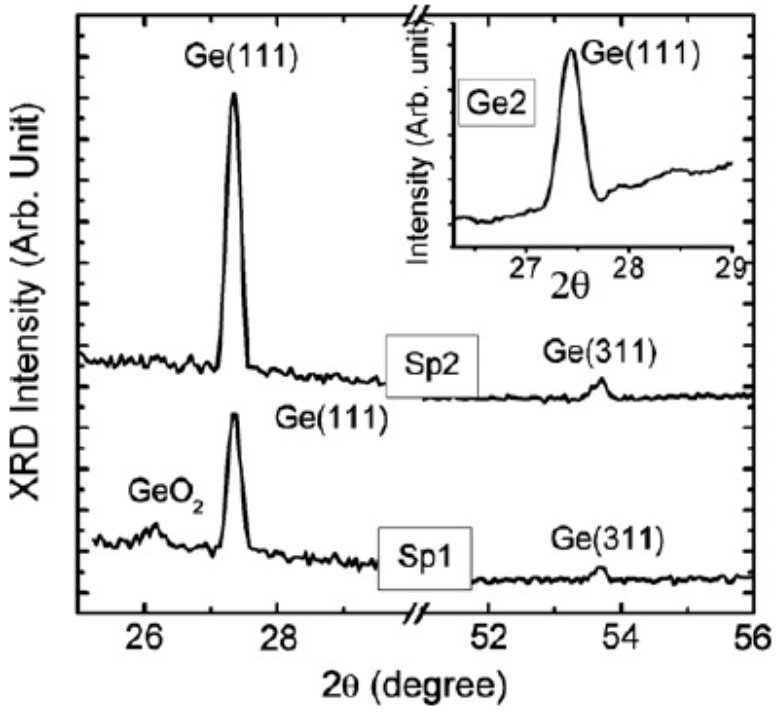

Fig. 2-6 Typical XRD patterns showing the formation of (111) and (311) orientated nc-Ge embedded in SiO_2 (from Ref. [90]).

2.3.1.5 Scanning electron microscopy

The scanning electron microscope (SEM) is an electron microscope that images the sample surface by scanning it with a high-energy electron beam in a raster scan pattern. The electrons interact with the atoms that make up the sample and produce signals that contain information about the surface topography, composition and other properties such as electrical conductivity. The SEM is useful for determining the size and distribution of nanocrystals on the sample surface [63, 129-132]. Occasionally, the

SEM technique can also be used to observe the cross-sectional structure of nanocrystals [133]. In Fig. 2-7, a 2-D array of nc-Ge deposited on the SiO_2 surface has been clearly observed by the SEM technique.

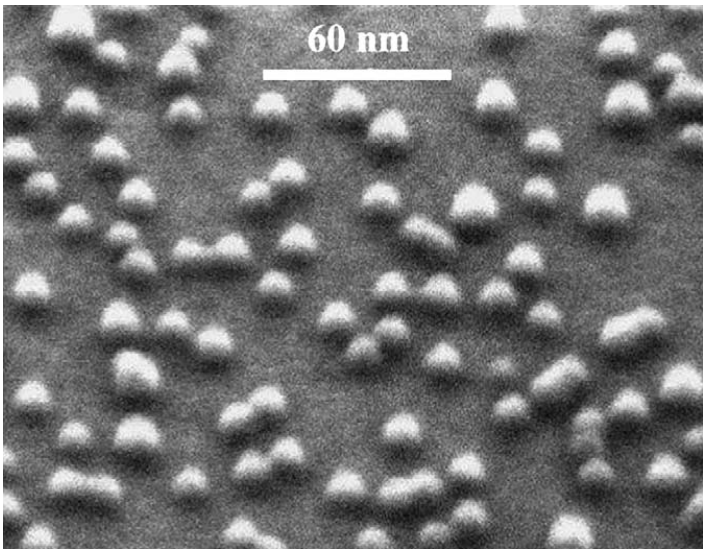

Fig. 2-7 A typical SEM image of nc-Ge deposited on the SiO_2 surface (from Ref. [63]).

2.3.2 Electrical characterizations

2.3.2.1 Capacitance-voltage measurement

The capacitance-voltage (*C-V*) measurement is one of the common techniques for the characterization of semiconductor materials and devices. For a metal-oxide-semiconductor (MOS) capacitor, properties such as gate oxide thickness, substrate doping concentration, threshold voltage, and flat-band voltage can be determined from the *C-V* measurement [134]. The *C-V* curve is usually measured with a *C-V* meter which applies a DC bias voltage and a small sinusoidal signal to the MOS capacitor and measures the capacitive current with an AC ammeter. The flat-band voltage (V_{FB}) of the MOS capacitor is sensitive to the existence of charges at the SiO_2 / Si interface

or in the bulk SiO_2. Thus, the behavior of various traps present in the SiO_2 can be investigated based on the flat-band voltage shift (ΔV_{FB}). The *C-V* measurement has been used to study the charge trapping associated with nanocrystals acting as isolated traps embedded in SiO_2 [43, 47, 96, 135-138]. Fig. 2-8 shows the typical *C-V* characteristics of a MOS capacitor with nc-Ge embedded in the gate oxide. After the charge injection, the shift in V_{FB} can be clearly observed. The ΔV_{FB} is used to determine the amount of charges trapped in the oxide.

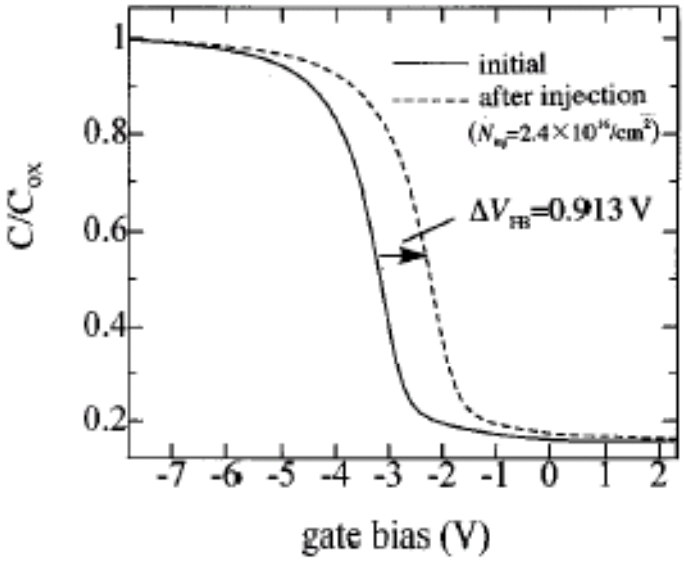

Fig. 2-8 *C-V* characteristics showing the ΔV_{FB} after the charge injection (from Ref. [47]).

2.3.2.2 Current-voltage measurement

The MOS capacitor is also frequently studied using a current-voltage (*I-V*) measurement. For an ideal gate oxide which is an insulator, the current conduction is assumed to be zero. However, for an actual gate oxide, the leakage current is non-zero, and the conduction mechanisms identified from the *I-V* measurements reveal the

properties of the interfaces (i.e., metal / oxide interface and oxide / Si interface) as well as the bulk oxide itself [139]. From the *I-V* measurements of MOS capacitors with nanocrystals embedded in the gate oxide, the hysteresis effect due to charging and discharging of nanocrystals has been observed [140-142]. Besides, the single electron effects in nanocrystals observed at both low-temperature (e.g., at 7 K) and room-temperature have been revealed by the *I-V* measurements [143-145].

2.3.3 Optoelectronic characterizations

2.3.3.1 Photoluminescence

Photoluminescence (PL) is a standard technique for the characterization of semiconductor materials. In a typical PL measurement, the sample is excited by the excitation source such as a laser, and the re-emission of light from the sample is detected by a spectrometer. The PL from a semiconductor is normally caused by the emission of a photon due to the inter-band transition when an electron that has been excited into the conduction band drops back to the valence band. Also, PL can be caused by the transition between the excited states and ground states of impurities or defects present in the material. The observation of PL is an indication of the potential optical and optoelectronic applications. PL is also a sensitive and nondestructive method to analyze the dopant and impurity levels present in the energy bandgap of a semiconductor. PL has been observed from Si and Ge nanocrystals embedded in SiO_2 [33, 62, 66, 68, 73, 146-151]. The quantum size effects and the information about the impurities and defects associated with the nanocrystals can be extracted from the PL studies.

2.3.3.2 Electroluminescence

Electroluminescence (EL) is the process by which luminescence is generated while an electrical current flows through the material. To obtain EL, devices such as *p-n* junction light emitting diode or MOS structure with ITO gate have to be made. The EL mechanism depends on the device structure and the material type. Generally, the EL is caused by the radiative recombination of excess electrons and holes injected electrically into the active layer of the device. The recombination takes place either across the bandgap of the semiconductor or via luminescence impurities / defects present in the bandgap. The EL can also be attributed to the impact ionization of high-energy electrons with impurities or defects under a high electric field [152]. Efficient EL can be used for the light-emitting diodes or laser. The EL from light-emitting devices based on Si and Ge nanocrystals embedded in SiO_2 have been demonstrated [38, 53, 91, 153-163].

2.4 Memory devices based on nanocrystals embedded in SiO_2

2.4.1 Conventional floating-gate memory structure

Solid-state non-volatile memory devices in which the stored information can be retained even when the power is off are critical components in present day electronic applications. The dominant non-volatile memory design is the FG-based memory structure in which the polycrystalline silicon (poly-Si) FG is completely isolated within the gate dielectric of a field-effect transistor (FET), as shown in Fig. 2-9. The FG acts as a potential well and charges are stored in the FG. The amount of charges

stored in the FG is proportional to the threshold voltage of the FET. Although the conventional FG design has made a huge commercial success, it has a limited potential for the continuing scaling of the device structure. The limitation mainly results from the extreme requirements on the tunnel oxide separating the FG and the Si substrate [19]. In a FG-based non-volatile memory structure, the tunnel oxide has to be thin to allow fast program / erase (P/E) operation under a low electric field. On the other hand, in order to provide sufficient isolation to prevent charge leakage and disturbance during the long-term charge retention and extensive P/E cycling, the tunnel oxide has to be sufficiently thick. Since the demands for fast speeds and low-operating voltages have to be compromised by the needs of long charge retention and good reliability, the device scaling is constrained by the tunnel oxide thickness. Moreover, one leakage path or one weak spot in the tunnel oxide is sufficient to cause a fatal loss of trapped charges because the FG is a continuous single node.

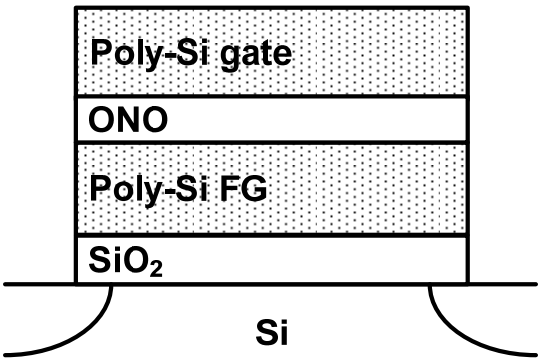

Fig. 2-9. Schematic representation of a conventional FG non-volatile memory cell (from Ref. [19]). The ONO is oxide-nitride-oxide gate dielectric stack used as the control oxide.

2.4.2 Nanocrystal-based non-volatile memory devices

Knowing the limitation of conventional FG-based non-volatile memory design, the semiconductor manufacturers and researchers are exploring alternative structures for non-volatile memory applications. Tiwari *et al.* proposed the nanocrystal-based non-volatile memory structure using a threshold voltage shift induced by the charge storage in isolated nanocrystals [20]. In the proposed structure, as shown in Fig. 2-10, the conventional FG is replaced by a layer of isolated semiconductor nanocrystals acting as charge storage nodes. Each nanocrystal is surrounded by the gate dielectric and located at a small tunneling distance away from the Si substrate. To program the device, electrons are injected from the inversion layer of the Si substrate into the nanocrystals via tunneling when the control gate is positively biased with respect to the Si substrate. Due to the smaller bandgap of the nanocrystal material, i.e., Si or Ge, as compared to the surrounding SiO_2 barriers, the long-term charge storage in the nanocrystals is achieved. Although each nanocrystal only stores a few electrons, the collective effect of many charged nanocrystals shifts the threshold voltage of the device. Fig. 2-11 shows a typical shift in threshold voltage of the nanocrystal-based non-volatile memory after a program operation. The erase operation is achieved by a negatively biased gate voltage. The advantage of a nanocrystal-based memory is the potential to use a thinner tunnel oxide without sacrificing the charge retention performance. Moreover, due to the nature of discrete charge storage as well as the Coulomb blockage effect which limits the removal of an electron from the nanocrystals, the nanocrystal-based non-volatile memory is more robust and fault-tolerant [20].

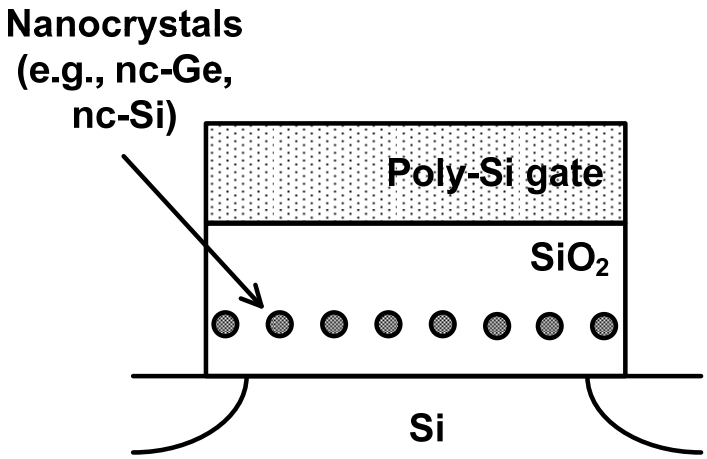

Fig. 2-10 Schematic representation of a nanocrystal-based non-volatile memory cell (from Ref. [19]).

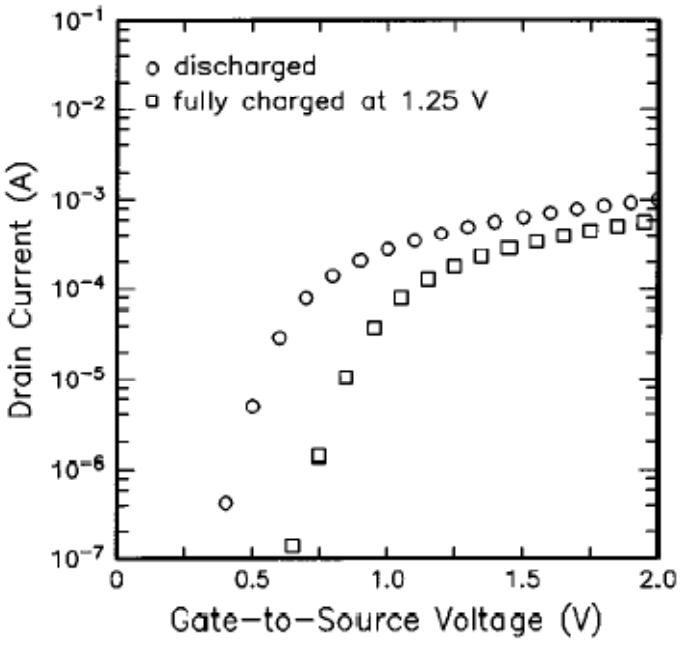

Fig. 2-11 Typical transfer characteristics of the nanocrystal-based non-volatile memory under the program operation. The shift in threshold voltage due to the electron storage in nanocrystals is ~ 0.25 V (from Ref. [20]).

In the pioneer work of Tiwari *et al.*, the charge storage nodes were made of nc-Si synthesized by the CVD method [20]. Several groups have also demonstrated the memory characteristics of non-volatile memory devices based on nc-Si synthesized by various methods [115, 138, 164, 165]. The bulk Ge has a smaller bandgap, smaller electron and hole effective masses and a larger dielectric constant than bulk Si. Then, it is considered that quantum size effects would appear more pronounced in nc-Ge than in nc-Si [33]. As a result, as compared to Si, Ge is expected to be a more promising choice of material for the charge storage nodes in nanocrystal-based memory devices. King *et al.* have demonstrated the non-volatile memory device based on nc-Ge synthesized by the oxidation of $Si_{1-x}Ge_x$ [78]. As shown in Fig. 2-12(a), a memory window of 0.4 V was achieved using a fast P/E speed of 100 ns. The endurance was found to be better than 10^9 P/E cycles with negligible degradation in the electrical characteristics, as shown in Fig. 2-12(b). Only a 5% reduction in the threshold voltage window was observed after waiting for 10^5 s. Despite the promising results delivered by this work, many fundamental problems related to the charge storage in nc-Ge are still not clear. The origin of the charge trapping and charge retention, which could be associated with the storage of electrons at the conduction band of nc-Ge [20, 95], the deep traps [166] or the interfacial traps of nanocrystals [72], is still under debate. Moreover, the correlations between memory performance and various controlling parameters in a specific synthesis technique have not been well addressed. The precise control of the memory behavior is important for the design and integration of nc-Ge based non-volatile memory in mainstream

microelectronic circuits. Thus, memory devices based on nc-Ge embedded in SiO_2 are still intensively investigated.

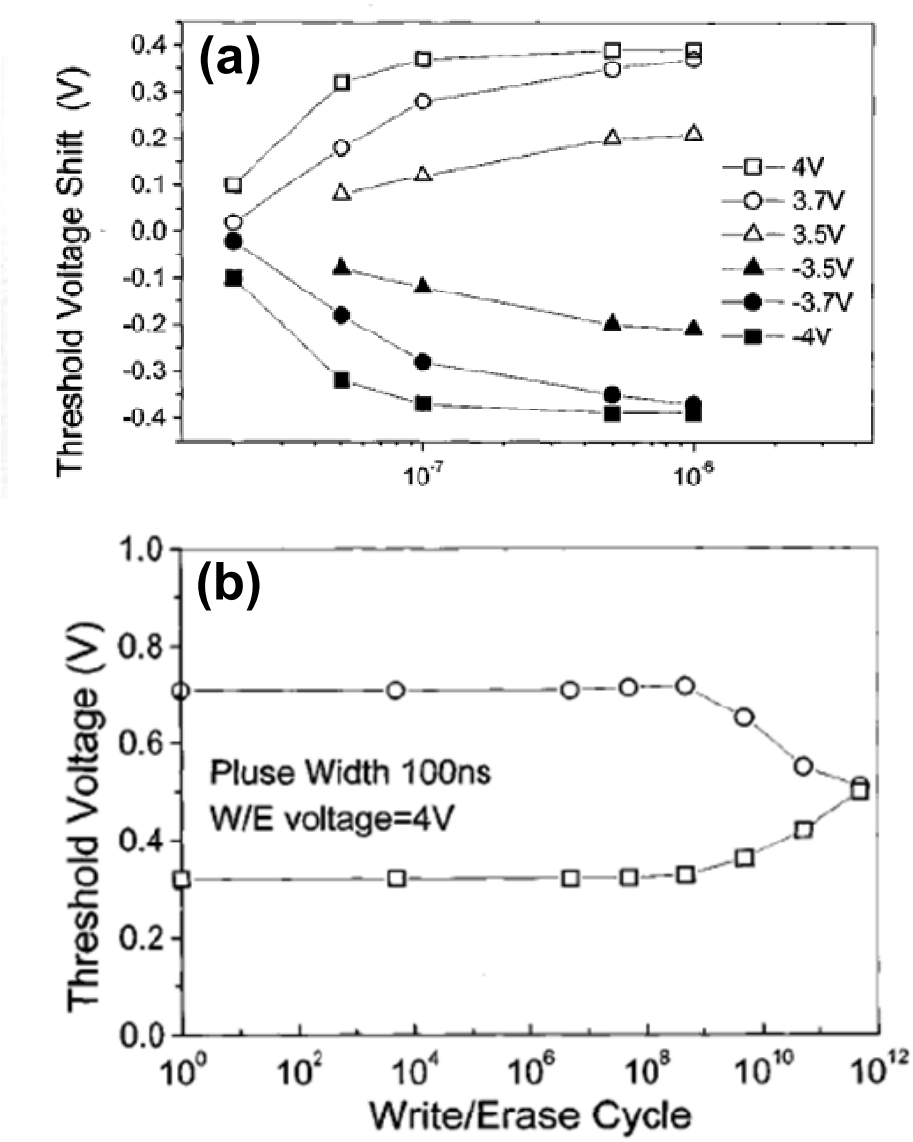

Fig. 2-12 Typical memory performance of the non-volatile memory cell based on nc-Ge: (a) threshold voltage shifts under various the program / erase (P/E) time and voltage, and (b) endurance of the cell tested with +4 V/ -4 V P/E pulse (from Ref. [78]).

2.5 Light-emitting devices based on nanocrystals embedded in SiO_2

2.5.1 Overview of direct and indirect bandgap materials

The conventional solid-state light-emitting devices are mainly based on Group III-V semiconductors which are direct bandgap materials. Fig. 2-13(a) illustrates the energy band structure for direct band-gap materials, in which the momentum of electrons at the bottom of the conduction band and that of holes at the top of the valence band are equal. The emission of a photon via the radiative recombination of excited electron and hole across the bandgap does not require the assistance of a phonon to conserve the momentum. As a result, the light emission process in a direct bandgap material is a first-order process with a much shorter radiative lifetime (~ 10^{-9} – 10^{-8} s) and a much higher luminescence efficiency. On the other hand, Group IV semiconductors, such as Si and Ge, are indirect bandgap materials. As shown in Fig. 2-13(b), for indirect bandgap materials, the momentum of electrons at the bottom of the conduction band is different from that of holes at the top of the valence band, and the excited electron populated in the conduction band needs to undergo a change in momentum state before it can recombine with a hole in the valence band. Thus, the conservation of momentum demands that the electron-hole recombination must be accompanied by the emission of a phonon. Since the light emission process which requires a change in both energy and momentum is a second-order process with a long radiative lifetime (~ 10^{-5} – 10^{-3} s), indirect bandgap semiconductors are highly inefficient in light emission.

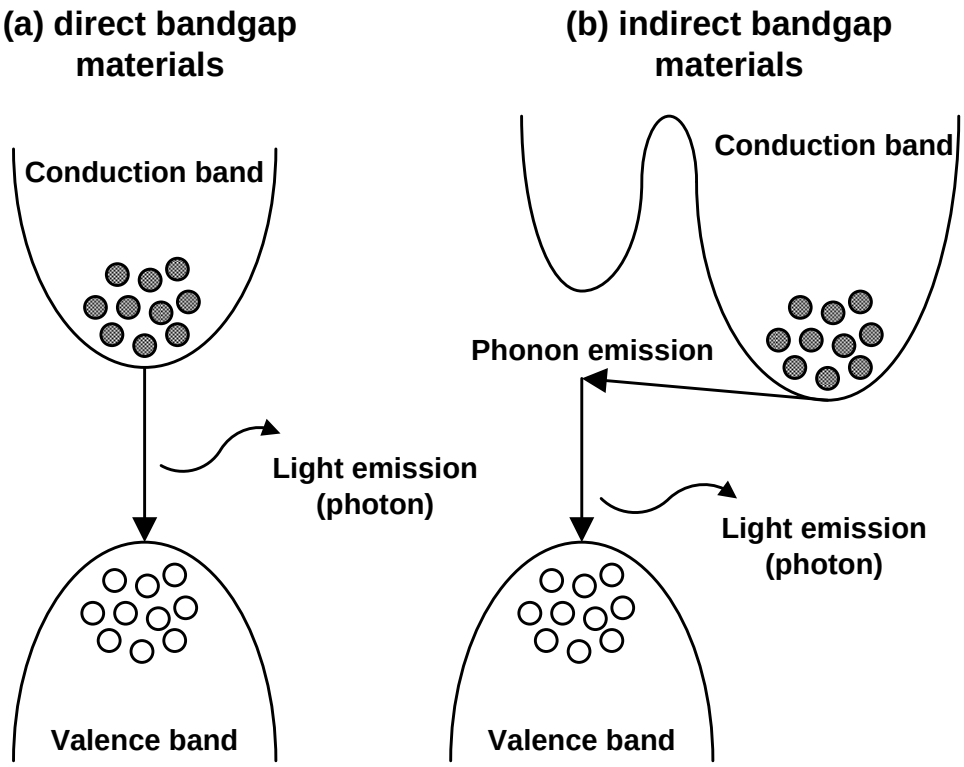

Fig. 2-13 Schematic of band-to-band radiative transitions in (a) direct bandgap materials, and (b) indirect bandgap materials.

2.5.2 Photoluminescence from SiO_2 embedded with nanocrystals

The integration of photonic and optoelectronic functional units into mainstream microelectronic circuits using Si-compatible technology has always been a great research interest. Various photonics components, such as optical modulators [21, 22], switches [23, 24], detectors [25, 26], and low-loss waveguides [27, 28], have been fabricated with Si technology. However, the challenge is to build a light emitter compatible with existing Si technology, because bulk Si and Ge are indirect bandgap materials which are inefficient for the emission of light.

Many strategies have been proposed to overcome these material limitations for fabricating Si-compatible light emitters. The most successful one is based on the exploitation of low dimensional Si nanostructures in which the optical and electronic properties of free carriers are modified by quantum confinement effects. Of all the types of low dimensional silicon, porous Si has received the most intensive research attention in the early years. The discovery of the visible photoluminescence (PL) from porous Si in 1990 [29] has triggered a large research effort in the field of porous Si and other Si nanostructures. It has been shown, as well, that luminescence wavelength can be tuned over a wide range and relatively high quantum efficiencies could be obtained, improving the prospect of using Si for light-emitting devices.

However, it is not reliable to utilize porous silicon in optoelectronic devices because of its unstable light emission [167], structural fragility [147], and incompatibility with conventional CMOS technology [168]. Therefore, nanocrystals are considered to be the preferable strategy for overcoming these challenges. The major reason for using nanocrystals is the three-dimensional quantum confinement effect which leads to the expansion of the optical bandgap as a result of the size reduction of nanocrystals [31]. That provides a possible way to relax the momentum conservation requirement and allows Group IV semiconductors with an indirect bandgap to possess efficient light emission properties. Studies on the visible PL from nc-Si and nc-Ge as a result of the radiative recombination of quantum-confined electron/hole pairs have been presented by many researchers [29, 66, 98, 147, 149, 150, 169-173]. Besides, the argument that the light emission from the SiO_2 embedded

with nanocrystals is primarily due to luminescence defects present in the SiO_2 matrix is also supported by many studies [157, 174-177].

The first observation of visible PL from nc-Ge embedded in the SiO_2 matrix was reported by Maeda *et al.* in 1991 [66]. In the SiO_2 film containing co-sputtered nc-Ge particles with a size of 6 – 8 nm, a broad PL spectrum ranging from 500 to 700 nm with the peak centered at about 570 nm (2.18 eV) was observed, as shown in Fig. 2-14. The origin of this visible PL was attributed to the three-dimensional quantum confinement of the electron-hole pair in the nc-Ge, based on the comparison with a theoretical calculation of the lowest energy separation of the electron-hole pair. The emission mechanism related to the quantum confinement effect in nc-Ge has also been supported by many findings [33, 35, 98, 172, 173]. Ma *et al.* found the size-dependent PL spectra for the annealed samples under different annealing temperature and time [98]. Giri *et al.* provided experimental evidence of a fast radiative recombination in nc-Ge using time-revolved PL measurements [172].

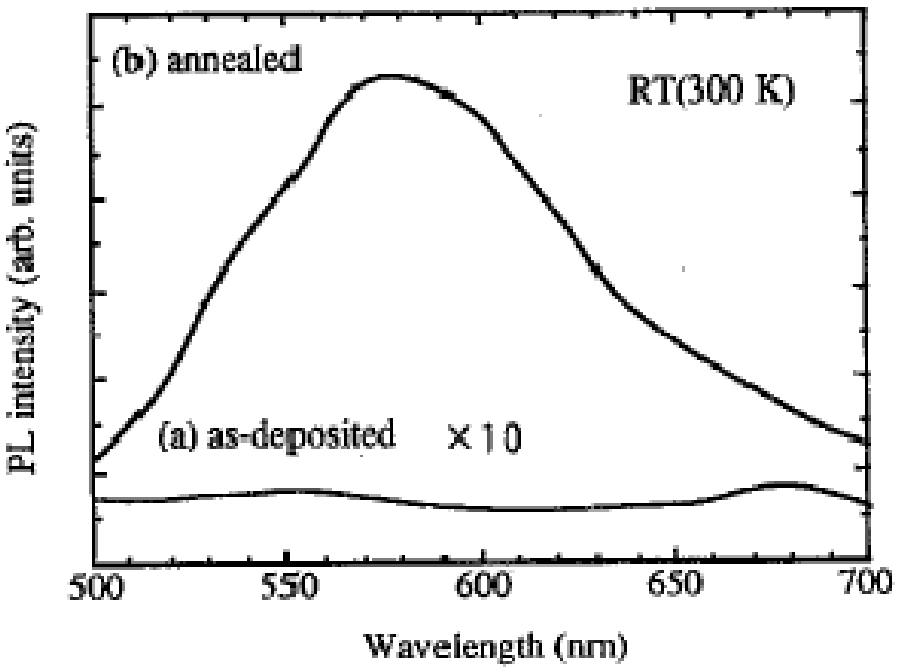

Fig. 2-14 Typical PL spectra at the visible wavelength region (from Ref. [66]).

The role of defects in the light emission from SiO_2 embedded with nc-Ge has also been supported by some studies [54, 76, 177]. In the work of Min *et al.* [177], the correlations between nc-Ge size as well as the PL peak energy and PL lifetime were not found. As shown in Fig. 2-15, the PL peak energy is independent of the nc-Ge size, and does not agree with the calculated bandgap energy using the quantum confinement theory. Thus, the PL mechanism of radiative recombination of electron / hole pairs in nc-Ge may not be applicable. Instead, a similar PL in samples implanted with Xe was observed, and the PL intensity was suppressed after defect passivation using deuterium annealing. Based on these results, the observed PL can be attributed to the radiative defect centers in the SiO_2 matrix.

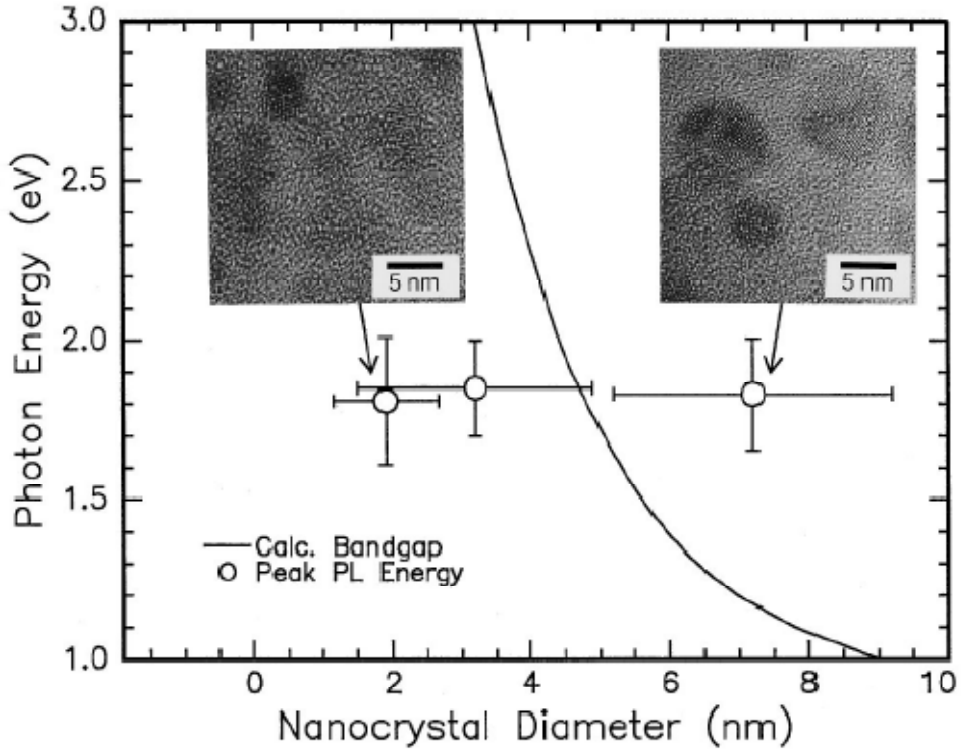

Fig. 2-15 Comparison between PL peak energy with the calculated bandgap energy as a function of nanocrystal diameter for nc-Ge embedded in SiO_2 (from Ref. [177]). TEM images are also shown to confirm the nanocrystal diameter.

2.5.3 Electroluminescence from SiO_2 embedded with nanocrystals

Conventional solid-state light-emitting devices are based on the *p-n* junction structure in which holes and electrons are supplied by the *p*-type and *n*-type semiconductor, respectively [153, 178, 179]. In order to study the EL properties, the SiO_2 films embedded with nanocrystals have to be incorporated into the light emitting devices. One approach is to use the structure of metal-oxide-semiconductor light-emitting device (MOSLED) in which the gate oxide is embedded with nanocrystals, and the "metal gate" is made of semitransparent and conductive materials such as

indium tin oxide (ITO), highly doped polycrystalline Si or Au. Fig. 2-16 shows a typical MOSLED structure with nc-Si embedded in the gate oxide. The bias voltage can be applied to the "metal gate", and the light emission from gate oxide embedded with nanocrystals can be transmitted through the "metal gate" and analyzed by the spectrometer.

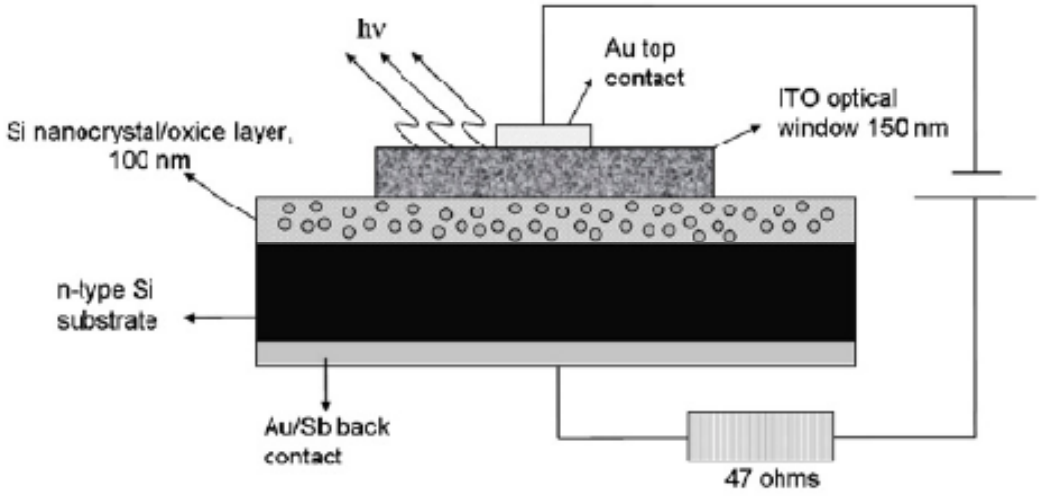

Fig. 2-16 Typical schematic diagram of a MOSLED for the characterization of EL from the SiO_2 thin film embedded with nanocrystals (from Ref. [161]).

Due to the simplicity in the device fabrication as well as the characterization, the MOSLED structure has been commonly used for the studies of EL from SiO_2 films embedded with nc-Si [153-161] as well as nc-Ge [38, 53, 91, 162, 163]. Similarly to the PL, the EL from SiO_2 embedded with nc-Ge could be related to the inter-band recombination of quantum-confined electron / hole pairs in nanocrystals. Shen *et al.* have demonstrated that the EL intensity from the co-sputtered SiO_2 embedded with nc-Ge depends on the size of nc-Ge [91]. The EL has been attributed to the direct

inter-band recombination of electron / hole pairs in small nc-Ge, and it has been found that the transport properties are influenced by the discrete energy levels in the nc-Ge, which result in the dependence of EL intensity on the size of nc-Ge. On the other hand, the EL could also be associated with luminescence defects. Shchegiov *et al.* have demonstrated visible EL from the Ge-implanted p^+-Si / SiO_2 / n^+-Si structure [163]. Based on observations that the EL occurred at a negatively biased condition near the breakdown regime, and no EL was observed with the opposite polarity of bias voltage, the EL has been attributed to the excitation of luminescence defects in the oxide layer by the hot carriers under a high electric field. Indeed, the radiative recombination in nc-Ge due to quantum confinement effects and the defect-related luminescence are not mutually exclusive. In the study of Zhang *et al.*, the EL from the Au / SiO_2 / *p*-Si (MOS) structure with nc-Ge embedded in SiO_2 has been reported [52]. Different mechanisms have been proposed to explain the different EL spectra between the positive- and negative-biased conditions as shown in Fig. 2-17. The common EL band at 400 nm under both bias conditions has been attributed to the germanium oxygen deficiency center (GODC) defect. Besides, the 600 nm band which was only observed under the positive-biased condition has been attributed to the radiative recombination of the quantum-confined electron / hole pairs in nc-Ge.

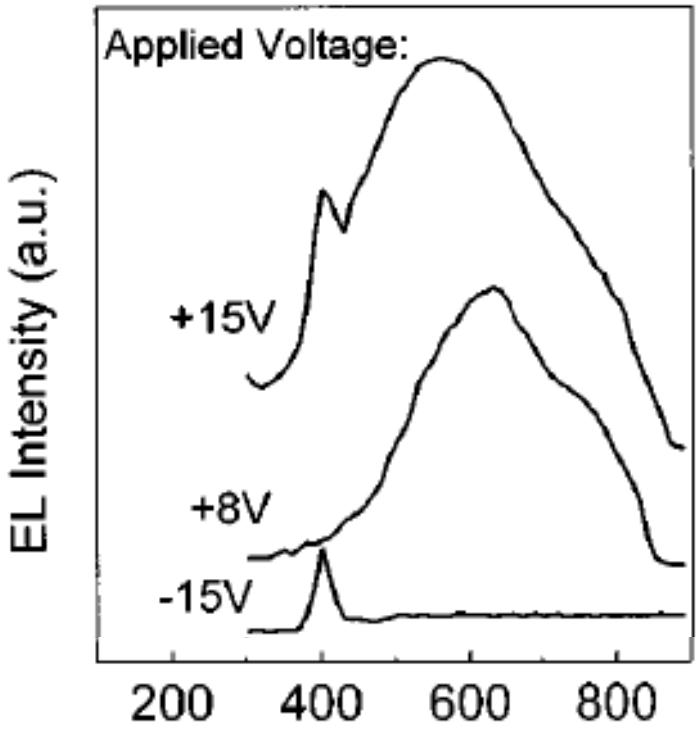

Fig. 2-17 Different EL spectra obtained from the Au / SiO_2 / *p*-Si structure with nc-Ge embedded in SiO_2 under different bias conditions (from Ref. [52]).

Besides the commonly used MOSLED structure, Walters *et al.* have proposed a field-effect light-emitting device (FELED) using a three-terminal structure where nc-Si are embedded in the gate oxide of a conventional MOSFET [180]. As shown in Fig. 2-18, electrons and holes are injected sequentially into the nanocrystals embedded in the gate oxide from the channel of the MOSFET by a sequence of alternating positive and negative pulses applied to the gate. The sequential accumulation of electrons and then holes within the nanocrystals thereby results in radiative recombination, leading to light emission.

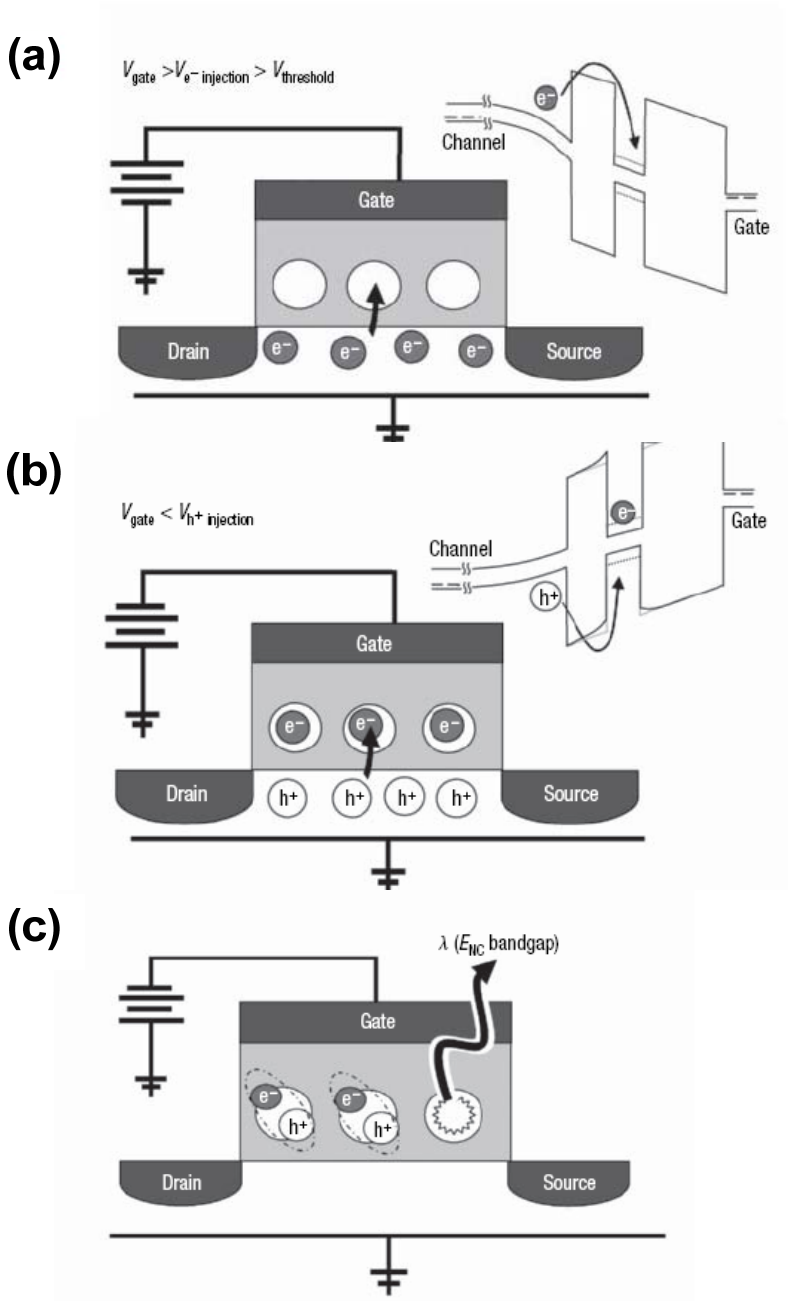

Fig. 2-18. Schematic diagrams showing the carrier injection in a FELED (from Ref. [180]): (a) electrons are injected into nanocrystals under a positive pulse, (b) holes are injected into nanocrystals under a negative pulse, (c) recombination of electrons and holes in nanocrystals leads to light emission.

The key advantage of the approach of Walters *et al.* is that the carriers are injected from only one side of the nanocrystal-embedded matrix. This relaxes the constraints on the device fabrication, because the carrier tunneling efficiency is only governed by the distance between the nanocrystals and the channel, and not by their density or the total matrix thickness. Moreover, as the techniques needed to make ultra-thin tunneling oxides as well as all the other components of such device are already commercially mature, the integration of nanocrystals with conventional silicon-chip production is straightforward. Lastly, because the field necessary to produce light in the FELED is much lower than that for the two-terminal devices, issues of oxide degradation can be minimized, improving the prospects for a long-term device operation. However, further studies of such device structure have not been reported so far. That could be due to the complexity in fabricating the FELED structure as well as the complicated operating conditions which require a pulsed signal with a frequency of 10 kHz or above.

2.6 Summary

In this chapter, a literature review of the research on nc-Ge has been presented. First of all, common synthesis techniques for nc-Ge embedded into SiO_2 films have been reviewed. Although each synthesis technique has its own advantages and disadvantages, the ion implantation technique which is good at controlling the density and depth distribution of nc-Ge in SiO_2 and is suitable for both applications of non-volatile memories and Si-compatible light-emitting devices has been chosen for this study. Also, the most common characterization techniques for the structural, material,

electrical and optoelectronic properties of nc-Ge embedded in SiO_2 have been reviewed. Lastly, the applications of nc-Ge in non-volatile memory devices as well as Si-compatible light-emitting devices have been discussed in detail.

Chapter 3 Current Transport in Ge-ion-implanted SiO_2 Thin Films

3.1 Introduction

Ge-ion-implanted SiO_2 thin films have opened up new possibilities for fabricating novel non-volatile memories [43, 47, 48, 59, 181] and Si-compatible light-emitting devices [52, 54, 182]. In both applications, the Ge-ion-implanted SiO_2 embedded with nc-Ge acts as a gate dielectric layer sandwiched by the gate electrode and the Si substrate. Since both the charge storage and the light emission are caused by the charge injection into the Ge-ion-implanted SiO_2, an understanding of the current transport behavior of the Ge-ion-implanted SiO_2 is indispensable. The conventional SiO_2 film has been studied since the fabrication of the first metal-oxide-semiconductor field-effect transistor (MOSFET) in 1960 [42]. However, the Ge-ion-implanted SiO_2 differs from the conventional SiO_2 in many aspects. From the previous studies on Cs- and B-ion-implanted SiO_2, it is known that ion implantation modifies the SiO_2 by creating defects / traps in the bulk of oxide film [46]. For the case of Ge ion implantation, besides the implantation-induced defects, the formation of Ge nanocrystals (nc-Ge) in the SiO_2 matrix has also been observed in many previous studies [41, 43-45]. Thus, the current transport of Ge-ion-implanted SiO_2 is different from that of the conventional SiO_2 and demands an in-depth study.

In this chapter, the current transport behavior of the Ge-ion-implanted SiO_2 thin films is investigated. The focus of this chapter is to understand the different transport mechanisms dominating in the different oxide field regions based on the gate current density (J_{GATE}) versus oxide field (E_{OX}) characteristics measured at various temperatures. Two different distributions of nc-Ge in the SiO_2 thin films were fabricated. The low implant energy of 2 – 8 keV leads to a narrow distribution of nc-Ge near the SiO_2 surface. On the other hand, the high implant energy of 16 keV results in a broad distribution of nc-Ge throughout the SiO_2. The structural properties of the Ge-ion-implanted SiO_2 thin films obtained from the secondary ion mass spectroscopy (SIMS) and cross-sectional transmission electron microscopy (TEM) are presented in Section 3.4. The J_{GATE}-E_{OX} characteristics of the SiO_2 thin films containing a narrow distribution of nc-Ge near the SiO_2 surface are presented in Section 3.5. Furthermore, the effects of implant energy and dose on the current transport behavior are also presented. In Section 3.6, the J_{GATE}-E_{OX} characteristics of the SiO_2 thin films containing nc-Ge throughout the SiO_2 are studied. For both cases, appropriate models are proposed to explain the current transport behavior.

3.2 An overview of common conduction mechanisms

Due to the variation in the material, fabrication process, film thickness, and trap density of the dielectric layer, there are many conduction mechanisms for the current transport in the SiO_2 system [183-186] as well as other dielectric materials which are important for the ultra-large-scale-integration (ULSI) processes [187, 188]. This

section briefly reviews the conduction mechanisms used for the analysis of current transport behavior in this study.

3.2.1 Fowler-Nordheim tunneling

Fowler-Nordheim (FN) tunneling is a process to describe the tunneling of electrons through a triangular barrier into the conduction band of SiO_2 in the presence of an intense electric field. As pointed out by Lenzlinger and Snow [183], electrical conduction in a thermally grown SiO_2 is an electrode-limited process rather than the bulk-limited process that is often observed in organic films or silicon nitride, because SiO_2 has a large bandgap (~ 9 eV), a low density of traps in the bandgap [189], and a relatively high mobility in the conduction band [190]. The electrical conduction of a thermally grown SiO_2 can be described by the FN tunneling of electrons [183]. Fig. 3-1(a) illustrates the energy-band diagram of a MOS structure without a bias voltage. The energy barrier Φ_e for electrons from the Si conduction band to the SiO_2 conduction band is ~ 3.25 eV, while the energy barrier Φ_h for holes from the silicon valence band to the SiO_2 valence band is ~ 3.8 eV. The barrier height Φ_M for electrons in the metal depends on the Fermi level of the metal. The SiO_2 behaves as a good insulator at zero bias. However, under a large external gate bias (which results in an intense electric field across the SiO_2), the electrons see a triangular barrier whose effective width is dependent upon the magnitude of the applied field. As shown in Fig. 3-1(b), under a large positive gate bias, the FN tunneling of electrons from the vicinity of the Si conduction band edge to the SiO_2 conduction band occurs. Similarly, as shown in Fig. 3-1(c), under a large negative gate bias, the FN tunneling of electrons from the vicinity of the electrode Fermi level to the SiO_2 conduction band occurs. In

the mean time, the FN tunneling of holes from the valence band of the Si to the SiO_2 conduction band is also possible to happen. However, the hole tunneling is a less favorable process compared to the electron tunneling, because of the relatively larger barrier height (Φ_h = 3.8 eV) for holes.

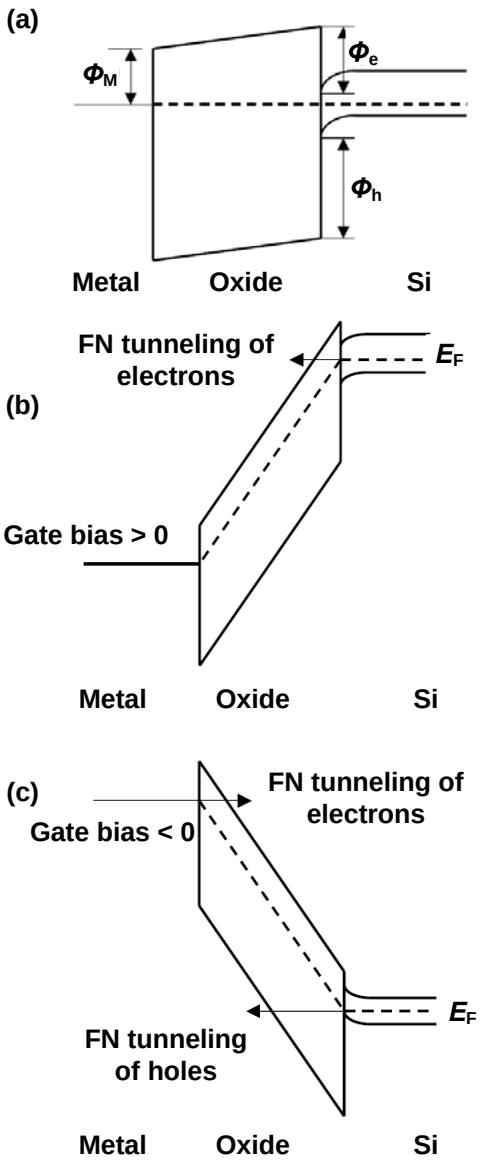

Fig. 3-1 Energy-band diagram of a MOS structure (a) at zero bias, (b) with a large positive gate bias, and (c) with a large negative gate (after Ref. [183]).

The expression of FN tunneling current (J_{FN}) through the SiO_2 is given by [183]

$$J_{\mathrm{FN}} = A_{\mathrm{FN}} {E_{\mathrm{i}}}^2 exp\left(-\frac{B_{\mathrm{FN}}}{E_{\mathrm{i}}}\right) \tag{3.1}$$

where E_{i} is the external applied electric field across the dielectric layer, and A_{FN} and B_{FN} are two constants given by

$$A_{\mathrm{FN}} = \frac{q^3}{16\pi^2 \hbar \Phi_{\mathrm{FN}}} \tag{3.2}$$

$$B_{\mathrm{FN}} = \frac{4}{3}\frac{(2m^*)^{1/2}}{q\hbar} {\Phi_{\mathrm{FN}}}^{3/2} \tag{3.3}$$

where q is the electronic charge, m^* is the effective mass of electrons (or holes) in the oxide layer, $\hbar$ is the reduced Planck constant, and Φ_{FN} the tunneling barrier height for electrons or holes. From Eq. (3.1), it is obvious that $\ln\left(J_{\mathrm{FN}}/{E_{\mathrm{i}}}^2\right)$ is a linear function of $1/E_i$ with a slope of $-B_{\mathrm{FN}}$. Therefore, the barrier height Φ_{FN} can be determined from the slope of the straight line in a FN plot, i.e., plot of $\ln\left(J_{\mathrm{FN}}/{E_{\mathrm{i}}}^2\right)$ versus $1/E_i$. It should be noted that a standard FN tunneling current is independent of the measurement temperature. This allows one to quickly distinguish FN tunneling from other temperature-dependent current conduction mechanisms. In typical Flash non-volatile memory devices based on floating-gate design, FN tunneling is a common programming mechanism. An injection field of > 7 MV/cm is required to achieve sufficient current levels (~ 10^7 A/m^2) for the programming of such memory devices.

3.2.2 Schottky emission

Schottky emission is essentially a thermionic process in which the thermal energy of the electrons is sufficient for them to overcome the metal-dielectric or dielectric-semiconductor barrier [139, 191]. As shown in Fig. 3-2, the electrons from the conduction band of Si encounters a potential barrier (Φ_B). In the presence of the external electric field, the Φ_B is lowered by the image force due to the electrons polarizing the surface of the electrode from which they were ejected [192]. Thus, the electrons are thermally excited over the reduced barrier to the conduction band of the dielectric layer.

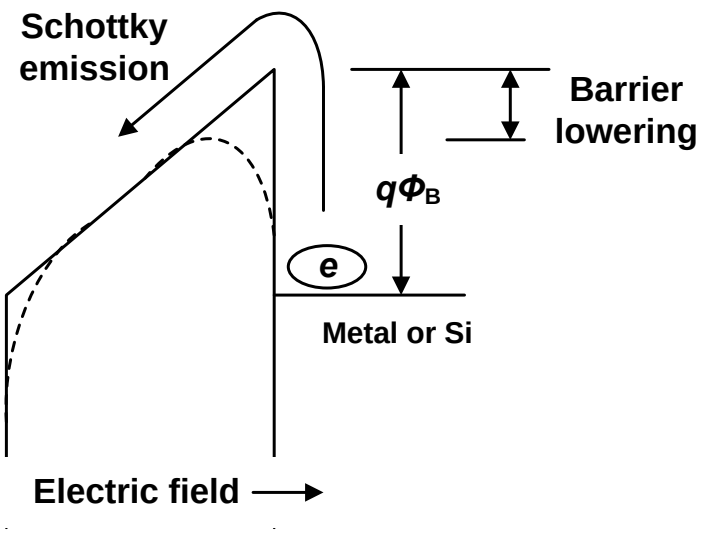

Fig. 3-2 Energy band diagram showing the Schottky emission of electrons over the potential barrier in the presence of an electric field (after Ref. [191]).

The expression of Schottky emission current (J_{Schottky}) is given by [139]

$$J_{\text{schottky}} = A^{*}T^{2}exp\left\{-\frac{q}{k_{\text{B}}T}\left[\Phi_{\text{B}} - \left(\frac{qE_i}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2}\right]\right\} \tag{3.4}$$

where A^{*} the effective Richardson constant, T is the temperature in K, q is the electronic charge, k_{B} is the Boltzmann constant, Φ_{B} is the barrier height of the metal / dielectric or dielectric E_{i} is the applied electric field across the dielectric layer, ε_0 is the permittivity of free space, and ε_i is the dielectric constant. The term $[qE_i/(4\pi\varepsilon_0\varepsilon_i)]^{1/2}$ is the amount of barrier lowering caused by the Schottky effect. Apparently, the Schottky emission current strongly depends on the measurement temperature. Based on Eq. (3.4), the linear relationship between $\ln\left(J_{\text{schottky}}/T^2\right)$ and $E_i^{1/2}/T$ is given by

$$\ln\left(\frac{J_{\text{schottky}}}{T^2}\right) = A_{\text{schottky}} + B_{\text{schottky}}\frac{E_i^{1/2}}{T} \tag{3.5}$$

where A_{schottky} (i.e., the y-intercept of the linear relationship) and B_{schottky} (i.e., the slope of the linear relationship) are given by

$$A_{\text{schottky}} = \ln A^{*} - \frac{q}{k_{\text{B}}T}\Phi_{\text{B}} \tag{3.6}$$

$$B_{\text{schottky}} = \frac{q}{k_{\text{B}}}\left(\frac{q}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2} \tag{3.7}$$

Therefore, the barrier height Φ_{B} and dielectric constant ε_i can be extracted from the linear relationship between $\ln\left(J_{\text{schottky}}/T^2\right)$ and $E_i^{1/2}/T$.

3.2.3 Poole-Frenkel emission

The classic Poole-Frenkel (PF) effect describes the thermal emission of electrons from a localized trap to the conduction band of a dielectric layer under the application of an external electric field [193]. As shown in Fig. 3-3, driven by an external electric field, the barrier height on one side of the trap is lowered and the trapped electrons can escape from the trap to the conduction band due to thermal excitation. The PF emission is a bulk analogue of the Schottky emission [192].

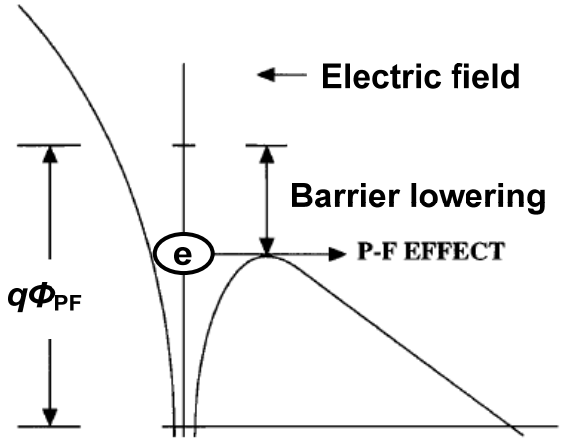

Fig. 3-3 Energy band diagram showing the PF emission of an electron from a trap in the dielectric layer in the presence of an external electric field (from Ref. [194]).

The PF emission has been frequently used for the current conduction in a dielectric layer with traps. At moderately high temperature and a fairly high electric field, the current transport in dielectric layers with traps is governed by the capture and emission process caused by the high density of traps close to the conduction band edge. Sze demonstrated that the current transport of Si_3N_4 films under high electric field follows the PF emission [195]. The PF emission was also observed in SiO_2

contains traps, e.g., the nitrided SiO_2 [196] or the evaporated SiO_2 [185]. Besides, for the ultra-thin SiO_2, PF emission was used to account for the stress induced leakage current [197, 198].

The expression of PF current density (J_{PF}) is given by [139]

$$J_{\mathrm{PF}} = C_{\mathrm{PF}} E_i exp\left\{-\frac{q}{k_{\mathrm{B}}T}\left[\Phi_{\mathrm{PF}} - \left(\frac{qE_i}{\pi\varepsilon_0\varepsilon_i}\right)^{1/2}\right]\right\} \tag{3.8}$$

where C_{PF} is a proportionality constant, E_i is the applied electric field across the dielectric layer, q is the electronic charge, k_{B} is the Boltzmann constant, T is the temperature in K, Φ_{PF} is the barrier height measuring the depth of the trap potential well, ε_0 is the permittivity of free space, and ε_i is the dielectric constant. The term $[qE_i/(\pi\varepsilon_0\varepsilon_i)]^{1/2}$ accounts for the barrier reduction caused by the PF effect. The derivation of Eq. (3.8) assumes the Boltzmann approximation for the electron energy distribution, and only one ionization energy, i.e., one trapping level, in the material is considered [194]. It is apparent that the PF mechanism is sensitive to the measurement temperature, and such temperature-dependence is useful to distinguish the PF mechanism from other temperature-independent mechanisms, e.g., the FN tunneling mechanism. The PF current follows a straight line in the PF plot, i.e., the plot of $\ln(J_{\mathrm{PF}}/E_i)$ versus ${E_i}^{1/2}$, because Eq. (3.8) can be rewritten as

$$\ln\left(\frac{J_{\mathrm{PF}}}{E_i}\right) = A_{\mathrm{PF}} + B_{\mathrm{PF}}\,{E_i}^{1/2} \tag{3.9}$$

where A_{PF} (i.e., the y-intercept of the straight line) and B_{PF} (i.e., the slope of the straight line) are given by

$$A_{\mathrm{PF}} = \ln C_{\mathrm{PF}} - \frac{q}{k_{\mathrm{B}}T}\Phi_{\mathrm{PF}} \tag{3.10}$$

$$B_{\mathrm{PF}} = \frac{q}{k_{\mathrm{B}}T}\left(\frac{q}{\pi\varepsilon_0\varepsilon_i}\right)^{1/2} \tag{3.11}$$

Based on the linear relationship between $\ln(J_{\mathrm{PF}}/E_i)$ and ${E_i}^{1/2}$, the barrier height Φ_{PF} and the dielectric constant ε_i can be extracted.

3.2.4 Ohmic conduction

At low applied electric field, the current transport of an insulating film can be ascribed to the hopping conduction of thermally excited electrons from one isolated state to another [199]. The ohmic conduction current (J_{ohmic}) is given by [139]

$$J_{\mathrm{ohmic}} = CE_i \exp\left(\frac{-\Delta E_{\mathrm{ac}}}{k_{\mathrm{B}}T}\right) \tag{3.12}$$

where C is the a constant, E_i is the electric field across the dielectric layer, ΔE_{ac} is the activation energy of electrons, k_{B} is the Boltzmann constant, and T is the temperature in K. Eq. (3.12) indicates that the ohmic conduction current exponentially depends on the measurement temperature with an activation energy of ΔE_{ac}. From the linear relationship between $\ln(J_{\mathrm{ohmic}}/E_i)$ and T^{-1}, the activation energy ΔE_{ac} can be determined. For the Si_3N_4 thin film at low field, an activation energy of 0.1 eV was reported [195].

3.3 Sample fabrication and experimental details

3.3.1 Fabrication of Ge-ion-implanted SiO_2 thin films

The sample fabrication began with the standard Piranha clean of the *p*-type <100> Si substrates (resistivity is 9 – 12 Ω-cm), followed by an HF clean to remove the native oxide. Dry oxidation at 950 °C was then performed to grow ~ 30 nm SiO_2 thin films on the Si substrates. Ge ions were then implanted into the SiO_2 thin films with various combinations of energy and dose to create different distributions of Ge ions in SiO_2. Table 2 summarizes the implant energies and doses used in the Ge ion implantation.

Table 2 Summary of various implant conditions for the study of electrical properties.

Group	Label	Implant energy (keV)	Implant dose (cm^{-2})
Group I	Ge2-2E15	2	2×10^{15}
	Ge4-2E15	4	
	Ge6-2E15	6	
	Ge8-2E15	8	
Group II	Ge4-3E14	4	3×10^{14}
	Ge4-2E15		2×10^{15}
	Ge4-1E16		1×10^{16}
Group III	Ge16-1E16	16	1×10^{16}

As summarized in Table 2, the samples in Group I were implanted using the same dose of 2×10^{15} cm^{-2} but different energies ranging from 2 – 8 keV, while the samples in Group II were fabricated using the same energy of 4 keV but different doses from 3×10^{14} – 1×10^{16} cm^{-2}. As simulated by the stopping and range of ions in matter (SRIM) program [200], the implant energy of 2 – 8 keV results in a Gaussian distribution of Ge ions with a peak at ~ 4 – 10 nm away from the SiO_2 surface. Thus, the implanted Ge ions for samples in Group I and II are distributed near the surface of SiO_2. On the other hand, the samples in Group III were fabricated with an energy of 16 keV and a dose of 1×10^{16} cm^{-2}, corresponding to a distribution of Ge ions throughout the SiO_2. A pure SiO_2 sample and several as-implanted samples without thermal annealing were also prepared. To induce the formation of nanocrystals, all samples were annealed at 800 ºC for 1 hour using the horizontal tube furnace system. Since the nanocrystals are formed by the crystallization of the excess Ge in SiO_2, the distributions of nc-Ge in the Ge-ion-implanted SiO_2 thin films can be generally divided into two categories: 1) low implant energies of 2 – 8 keV lead to nc-Ge distributed in a narrow layer near the SiO_2 surface, and 2) high implant energy of 16 keV leads to nc-Ge distributed throughout the SiO_2. All the fabrication processes were done by the CMOS facilities in the Nanyang NanoFabrication Centre (N^2FC) at Nanyang Technological University, Singapore.

3.3.2 SIMS and TEM characterizations

In this study, secondary ion mass spectroscopy (SIMS) was employed to reveal the depth profiles of Ge ions in the SiO_2 thin films. During the SIMS measurements, Cs^+ was used as the primary beam to sputter off the atomic layer of the sample surface.

Cross-sectional transmission electron microscopy (TEM) technique was used to observe the structural properties of the thin films and to confirm the formation of nanocrystals. Both techniques provide essential information to understand the current transport behavior of the Ge-ion-implanted SiO_2.

3.3.3 Fabrication of MOS structures

To study the electrical behavior, metal-oxide-semiconductor (MOS) structures based on Ge-ion-implanted SiO_2 thin films were prepared. Fig. 3-4(a) shows the schematic diagram of the MOS structure containing a narrow layer of nc-Ge near the SiO_2 surface, while Fig. 3-4(b) corresponds to the MOS structure containing nc-Ge distributed throughout the SiO_2.

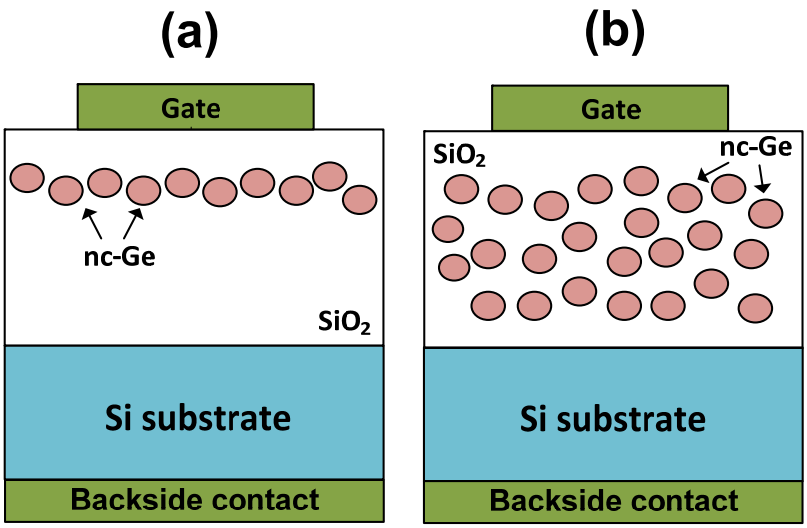

Fig. 3-4 Schematic diagrams showing the MOS structure with (a) nc-Ge confined in one narrow layer near the surface of SiO_2, and (b) nc-Ge distributed throughout the SiO_2.

Samples with Al gate electrodes (diameter = 160 μm, thickness = 250 nm) formed by e-beam evaporation were prepared. Other samples with indium tin oxide (ITO) gate electrodes (diameter = 1 mm, thickness = 130 nm) were also prepared. The ITO gate, which is a semi-transparent and electrically conductive material deposited using the sputtering technique, allows the penetration of UV illumination during the electrical measurement. For all the MOS structures, the Al backside contact (thickness = 250 nm) was formed by e-beam evaporation system.

3.3.4 Electrical characterization

Current-voltage (*I-V*) and high-frequency (1 MHz) capacitance-voltage (*C-V*) measurements were performed with a Keithley 4200 Semiconductor Characterization System. The measurement temperature was varied from 25 ºC (room-temperature) to 175 ºC. For the study of UV-induced conduction modulation, the UV illumination was carried out with an Oriel-66011 arc lamp together with an Oriel-77250 monochromator. The wavelength used for the UV illumination was 365 nm.

During the electrical characterization, the flat-band voltage (V_{FB}) of a MOS structure is an important parameter. The V_{FB} depends on the metal-semiconductor work function difference and the charges present in the oxide. A typical ion implantation in the SiO_2 will generate additional charges / defects, thus the deviation in V_{FB} from that of a pure SiO_2 has to be taken into account. In this study, the V_{FB} was determined experimentally using a differentiation technique introduced by Schroder based on the high-frequency *C-V* measurement [201, 202]. In this technique, the V_{FB} corresponds to the position of the lower knee in the plot of $1/C^2$ versus V_{GATE}, as

shown in Fig. 3-5(a). To determine the exact value of V_{FB}, the first differentiation of $1/C^2$ against V_{GATE} is drawn first, as shown in Fig. 3-5(b). From the smoothed data of this differentiated curve, the second differentiation of $1/C^2$ against V_{GATE} is drawn, as shown in Fig. 3-5(c). The V_{FB} is clearly identified as a single sharp peak in Fig. 3-5(c).

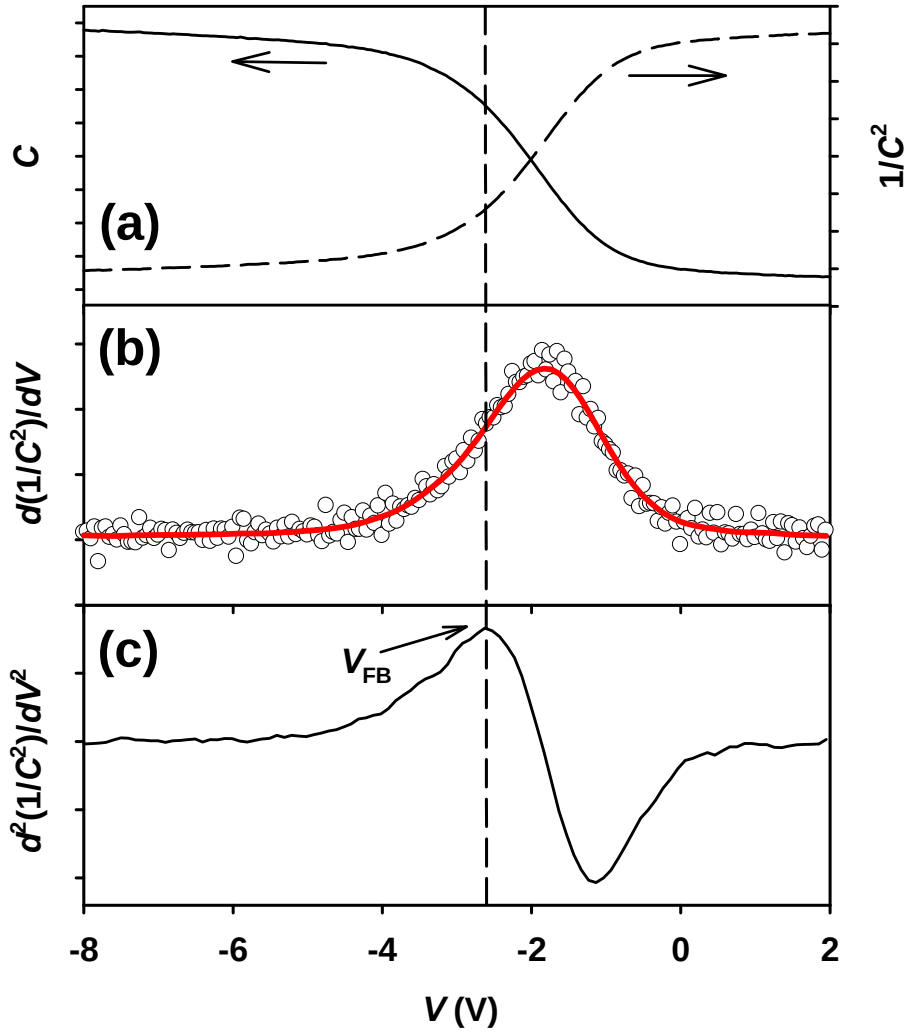

Fig. 3-5 A differentiation technique to determine the V_{FB} from a C-V curve. In (a), (b) and (c), plots of C, $1/C^2$, $d(1/C^2)/dV$ and $d^2(1/C^2)/dV^2$ are shown against V. The V_{FB} is determined from this technique as a single sharp peak in (c).

3.4 Structural properties of Ge-ion-implanted SiO_2 thin films

3.4.1 Ge nanocrystals distributed in a narrow layer near the SiO_2 surface

Fig. 3-6 shows the SIMS depth profiles of Ge atoms in SiO_2 for Group I samples after thermal annealing. A Gaussian-like distribution of Ge in SiO_2 is observed for each sample. Since the implanted Ge ions are confined in the SiO_2, loss of Ge atoms from the SiO_2 surface to the annealing ambient is negligible. As such, the Ge depth profile for each sample was quantified using the ion dose of 2×10^{15} cm^{-2}, which is the number of implanted Ge ions per unit area of the SiO_2 thin film.

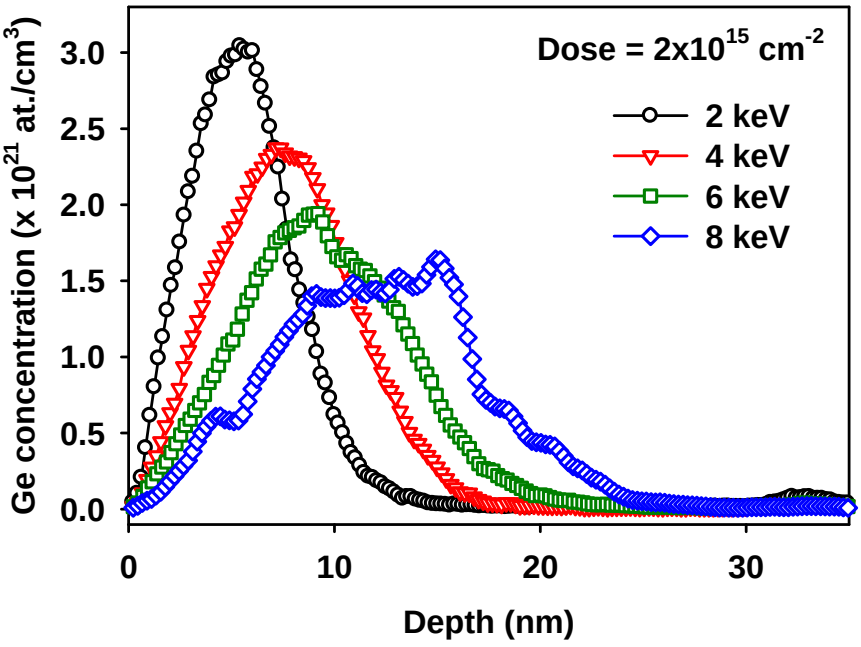

Fig. 3-6 SIMS depth profiles of Ge ions in SiO_2 thin films for various implant energies after thermal annealing.

As shown in Fig. 3-6, when the implant energy increases from 2 keV to 8 keV, the Ge distribution becomes broader, the location of Ge peak shifts toward the Si

substrate, and the Ge peak concentration reduces from 3.0×10^{21} cm^{-3} to 1.6×10^{21} cm^{-3}. The reduction of the Ge peak concentration is because of the identical implant dose used for these samples with different implant energies.

The Ge depth profile can be virtually divided into two regions. In the Ge-ion-implanted region near the SiO_2 surface, the crystallization of nc-Ge is expected to happen because this region contains most of the implanted Ge atoms forming a highly saturated state [34, 45, 49, 203]. On the other hand, it is known that the Ge can dissolve in the SiO_2 matrix without forming nc-Ge, and these Ge atoms dissolved in SiO_2 behave like free diffusing monomers with high mobility [34]. Thus, the SiO_2 region near the Si substrate contains a small amount of Ge atoms which are due to the tail of the Ge implantation profile as well as the diffusion of Ge atoms from the high-concentration-region after the thermal annealing. As the implant energy increases, the amount of Ge atoms present in the SiO_2 region near the Si substrate also increases because of the broadening of the implantation profile.

Fig. 3-7 shows the TEM image of the Ge4-2E15 sample annealed at 800 ºC for 1 hour, which is a typical sample with Ge atoms implanted near the SiO_2 surface. A narrow layer of nc-Ge distributed close to the SiO_2 surface can be observed in the TEM image. The TEM image is consistent with the Ge depth profile measured by SIMS.

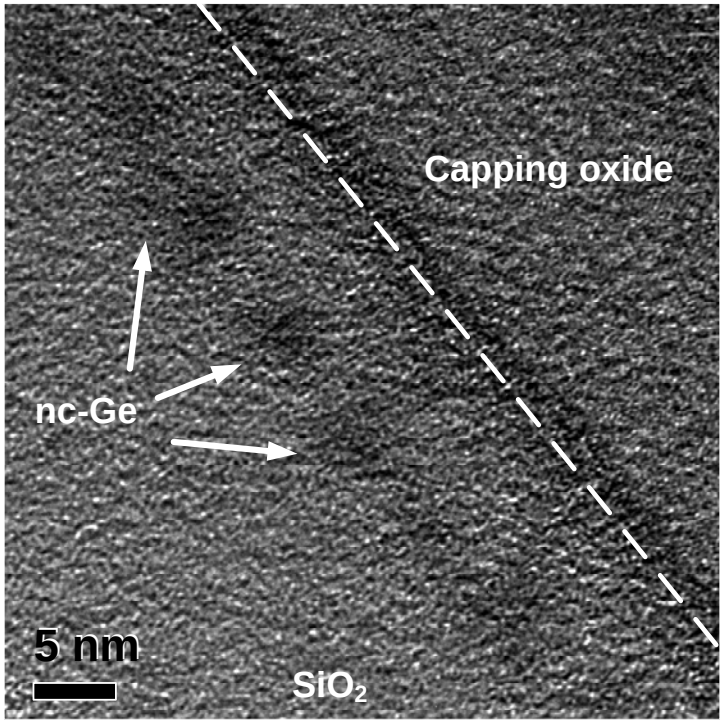

Fig. 3-7 A cross-sectional TEM image for the annealed Ge4-2E15 sample showing a narrow layer of nc-Ge located close to the SiO_2 surface.

3.4.2 Ge nanocrystals distributed throughout the SiO_2

Unlike the implant energies of 2 – 8 keV which lead to narrow distributions of Ge atoms in the SiO_2 close to the oxide surface, implant energy of 16 keV results in a broad distribution of Ge atoms throughout the SiO_2. The SIMS depth profiles of Ge and Si for the as-implanted Ge16-1E16 sample are shown in Fig. 3-8. The Ge depth profile was quantified using the total ion dose of 1×10^{16} cm^{-2}. Besides, the Si depth profile was quantified using the well-defined silicon atomic density of 5×10^{22} at./cm^3 at the Si substrate. The Ge atoms follow a Gaussian distribution in the SiO_2 with a peak at ~ 15 nm away from the SiO_2 surface and a full-width-at-half-maximum (FWHM) of ~ 14.3 nm. The location of Si / SiO_2 interface is determined as ~ 30 nm

away from the SiO_2 surface based on the abrupt increase of Si intensity. The result indicates that, for the implant energy of 16 keV, the distribution of Ge atoms is throughout the entire 30 nm SiO_2 thin film. The Ge depth profile simulated by the SRIM program is also shown in Fig. 3-8. Good agreement between the SIMS and SRIM profiles can be observed. Since the SRIM simulation provides an accurate estimation of the Ge distribution after the ion implantation, it can be used to determine the distribution of implanted Ge ions when SIMS is not available.

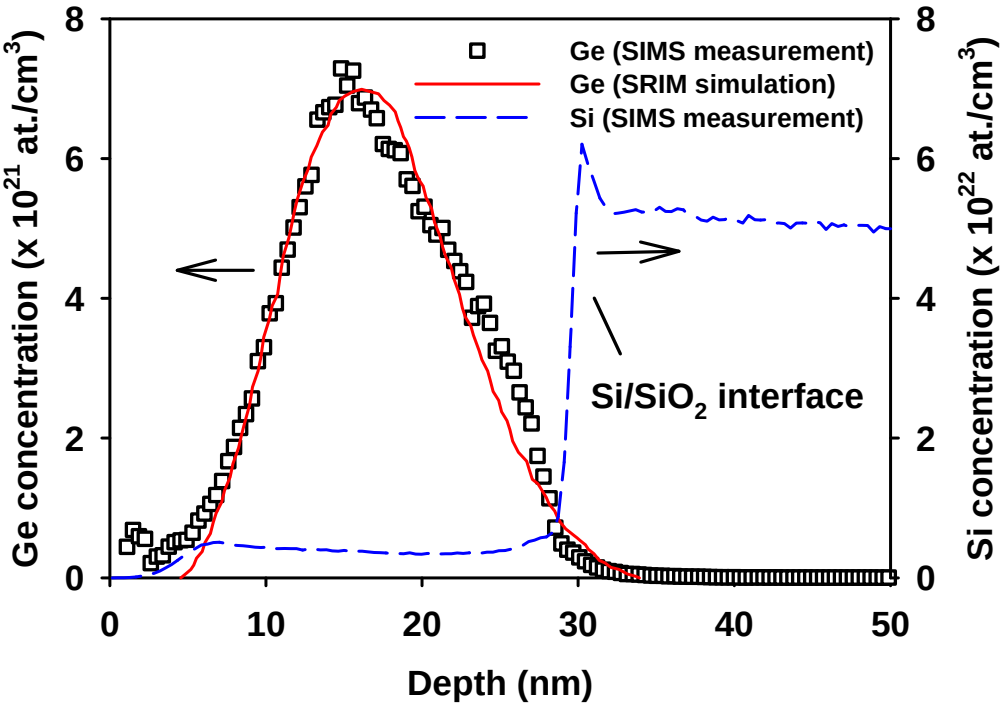

Fig. 3-8 SIMS and SRIM depth profiles of Ge in SiO_2 thin film for the as-implanted Ge16-1E16 sample. The SIMS profile for Si is also shown to identify the Si / SiO_2 interface.

Fig. 3-9 shows the SIMS depth profile of Ge in SiO_2 for the Ge16-1E16 sample after thermal annealing at 800 ºC for 1 hour. The depth profiles of Ge and Si were

quantified by similar methods used for Fig. 3-8. A Gaussian-like distribution of Ge in SiO_2 is still preserved during annealing, but the Ge peak concentration drops to ~ 3.2×10^{21} at./cm^3. A second Ge peak with a peak concentration of ~ 1.6×10^{21} at./cm^3 also appears at the SiO_2 / Si interface. The as-implanted SiO_2 contains high concentration of excess Ge. According to von Borany *et al.* [49], during the initial period of annealing, the Ge-ion-implanted system is in a highly super-saturated state and its excess free energy is lowered by the crystallization of nc-Ge. Meanwhile, some Ge atoms are dissolved in the SiO_2 and behave as free diffusing monomers with high mobility in the SiO_2. Thus, the redistribution of Ge atoms occurs as a result of the diffusion of these dissolved Ge in SiO_2. The accumulation of Ge at the interface is also associated with the Ge diffusion, because the SiO_2 / Si interface acts as an effective sink for the dissolved and diffused Ge [49].

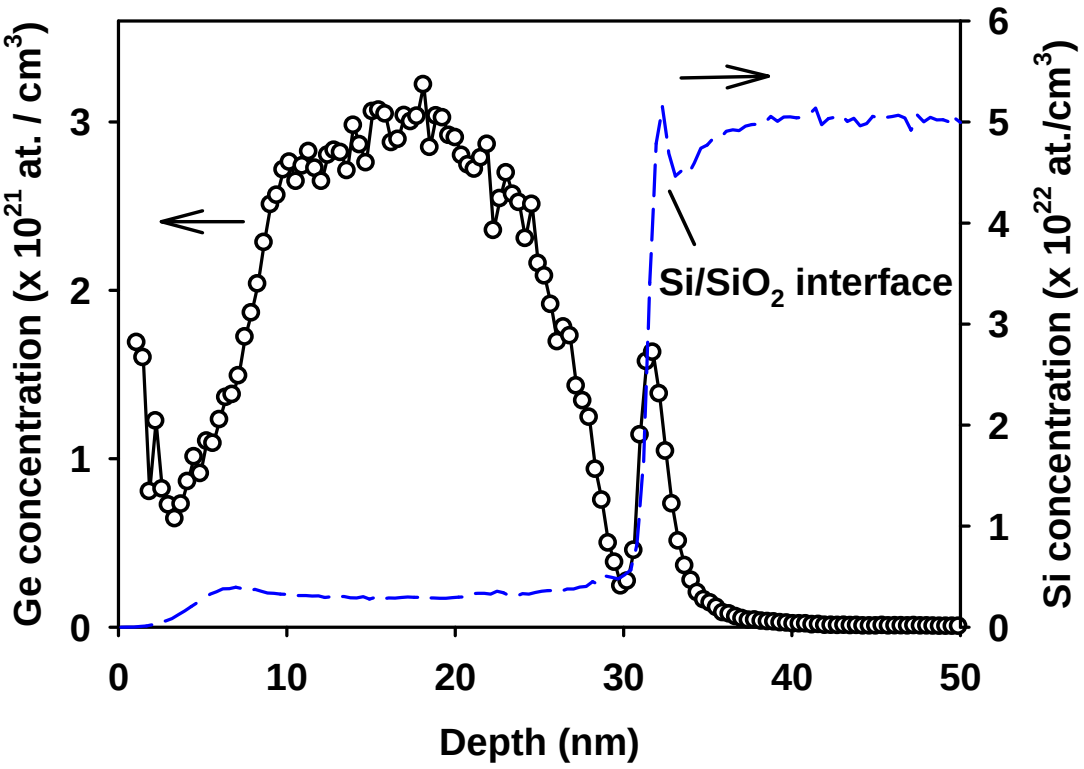

Fig. 3-9 SIMS depth profile of Ge in SiO_2 for the Ge16-1E16 sample annealed at 800 ºC for 1 hour.

Fig. 3-10 shows the TEM images of the annealed Ge16-1E16 sample. During the preparation of the TEM sample, a thick capping oxide (typical thickness is ~ 0.5 μm) was deposited by the PECVD technique. The Ge-ion-implanted SiO_2 thin film sandwiched by the capping oxide and the Si substrate can be observed. The thickness of the thin film is determined as ~ 31.6 nm, which is consistent with the result obtained from SIMS measurement. The high-resolution TEM image in Fig. 3-10(b) shows the existence of nc-Ge distributed throughout the SiO_2. The average size of the nc-Ge particles is ~ 5 nm.

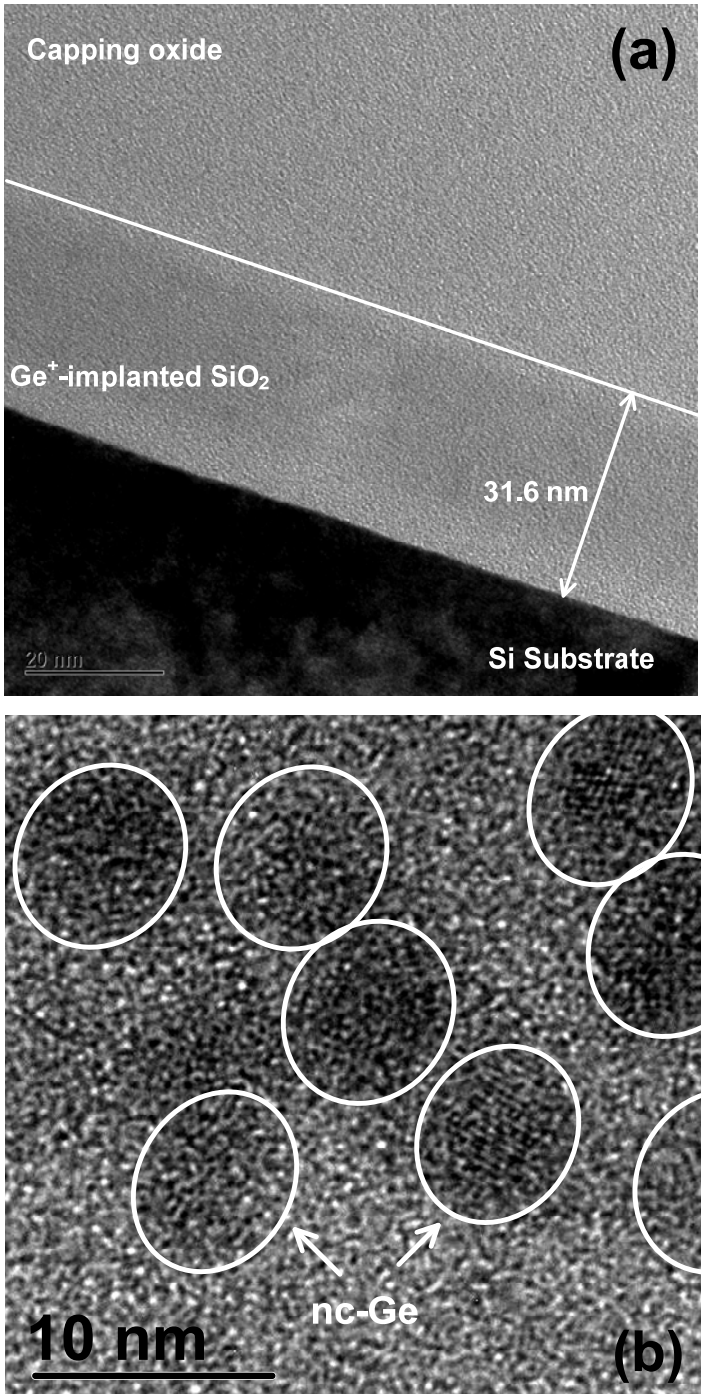

Fig. 3-10 (a) A cross-sectional TEM image of the annealed Ge16-1E16 sample; (b) A high-resolution TEM image for the same sample showing the existence of nc-Ge distributed throughout the SiO_2.

3.5 Current transport in SiO_2 with nc-Ge distributed in a narrow layer near the SiO_2 surface

In this section, the current transport behavior of the Ge-ion-implanted SiO_2 thin films containing nc-Ge distributed in a narrow layer near the SiO_2 surface is studied. The current conduction mechanisms dominating in different oxide field regions are identified. The results are explained by a two-region conduction model based on the structure of the Ge-ion-implanted SiO_2 thin film. In addition, the effect of implantation conditions, i.e., implant energy and dose, on the effective tunneling barrier height is discussed.

3.5.1 Characteristics of gate current density versus electric field

The study of current transport behavior is based on the measurement of *C-V* and *I-V* characteristics of the MOS structure. With the actual area of the gate electrode measured by the optical microscope, the gate current density (J_{GATE}) can be obtained from the measured gate current. The electric field (E_{OX}) across the oxide can be calculated from the applied gate voltage (V_{GATE}) using the relationship

$$E_{\mathrm{OX}} = \frac{V_{\mathrm{GATE}} - V_{\mathrm{FB}}}{d_{\mathrm{OX}}} \tag{3.13}$$

where V_{FB} is the flat-band voltage, and d_{OX} is the total oxide thickness.

The V_{FB} of a MOS structure can be obtained from the *C-V* measurement. Fig. 3-11 shows the typical *C-V* characteristics for the pure SiO_2 and the annealed Ge4-1E16 sample. It is clear that these two samples have different V_{FB}. Based on the

technique mentioned in Section 3.3.4, the V_{FB} can be determined as -2.12 and -5.61 V for the pure SiO_2 and the annealed Ge4-1E16 sample, respectively. The smaller V_{FB} of the Ge4-1E16 sample indicates the existence of more positive charges in the oxide. This phenomenon has been observed in Cs-implanted oxide [46] and Si-implanted oxide [204]. It is believed that the positive charges are related to the trapped Ge ions in the oxide [204]. Because of the difference in V_{FB}, the E_{OX} in the pure SiO_2 and Ge4-1E16 under the same applied V_{GATE} are not the same. To achieve the same amount of E_{OX}, Ge4-1E16 requires a smaller V_{GATE} as compared to the pure SiO_2. Thus, the current transport behavior of these two samples can be compared based on the J_{GATE}-E_{OX} curves where the effect of V_{FB} is ruled out, instead of the J_{GATE}-V_{GATE} curves.

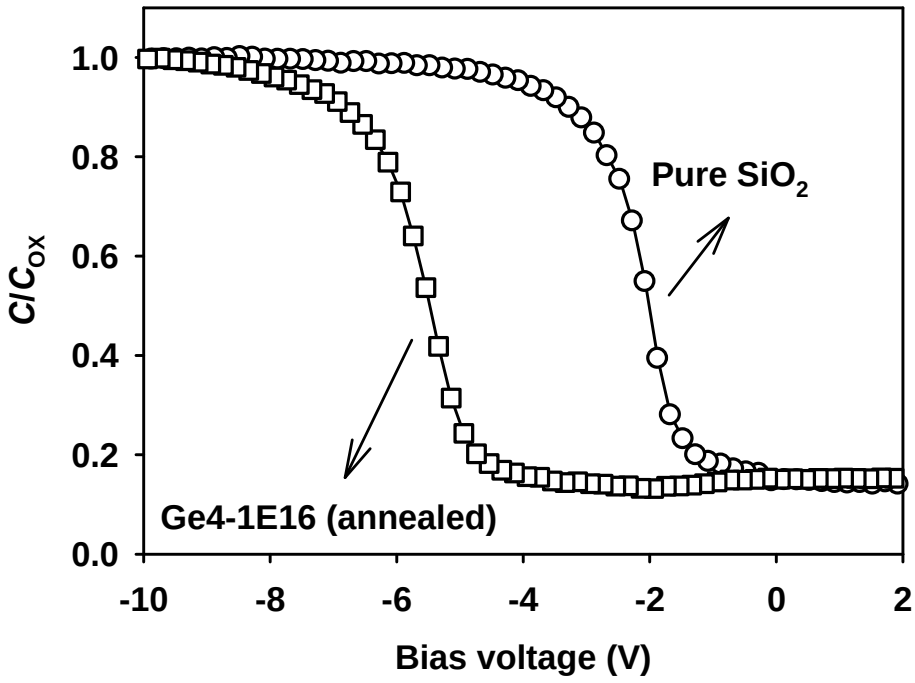

Fig. 3-11 *C-V* characteristics for the pure SiO_2 and the annealed Ge4-1E16 sample.

Fig. 3-12 shows the J_{GATE}-E_{OX} characteristics for the pure SiO_2 and the annealed Ge4-1E16 sample. For the pure SiO_2 sample, the J_{GATE} is insignificant (out of the measurement range of the machine) when E_{OX} is low. That is because for the low E_{OX}, the relatively thick SiO_2 with a thickness of 32 nm prevents any direct tunneling current that is commonly observed for the low-field leakage current in an ultra-thin SiO_2 (typically less than 4 nm) [205, 206]. The trap-assisted tunneling current [187, 188] is also not present because of the absence of significant amount of traps / defects in the thermally grown SiO_2. Thus, the pure SiO_2 sample shows no appreciable J_{GATE} when the E_{OX} is low.

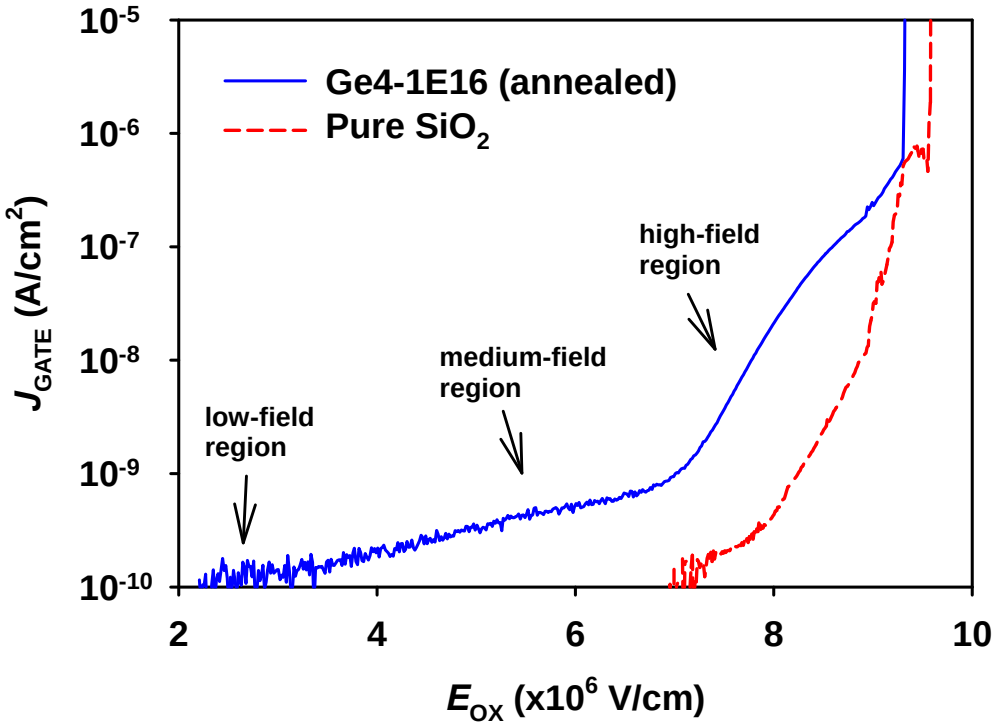

Fig. 3-12 Room-temperature J_{GATE}-E_{OX} characteristics for the pure SiO_2 and the annealed Ge4-1E16 sample.

As shown in Fig. 3-12, the J_{GATE} for the pure SiO_2 increases rapidly when the E_{OX} reaches an onset value of ~ 8 MV/cm. It is well-known that when the E_{OX} is sufficiently high, a thermally grown SiO_2 exhibits the FN tunneling of electrons through the triangular barrier into the SiO_2 conduction band [139, 183]. Fig. 3-13 shows the FN plot of the J_{GATE}-E_{OX} characteristic for the pure SiO_2 sample. A linear relationship between $\ln\left(J_{GATE}/{E_{OX}}^2\right)$ and $1/E_{OX}$ can be observed for E_{OX} > 8 MV/cm. The result confirms the occurrence of FN tunneling in the pure SiO_2 sample. Based on Eq. (3.1)-(3.3), the tunneling barrier height Φ_{FN} can be derived from the slope of the straight line in the FN plot. Using $m^* = 0.33m_0$ [184, 207], the Φ_{FN} for the pure SiO_2 sample was calculated as 3.24 eV, which is in good agreement with the commonly used barrier height of 3.25 eV for electrons from the Si conduction band to the SiO_2 conduction band [183].

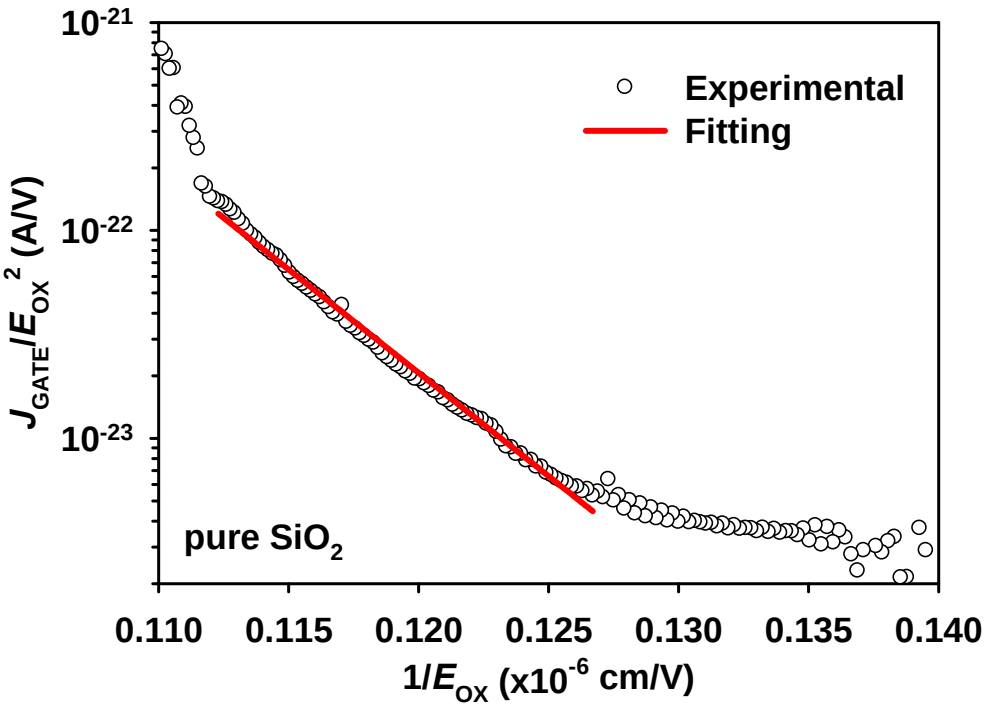

Fig. 3-13 FN plot (i.e., semi-log plot of J_{GATE}/E_{OX}^2 versus $1/E_{OX}$) of the pure SiO_2 sample.

In Fig. 3-12, it is apparent that the current transport of the Ge4-1E16 sample is different from that of the pure SiO_2 sample. For the annealed Ge4-1E16 sample, the J_{GATE}-E_{OX} curve can be generally divided into a low-field region below 3 MV/cm, a medium-field region from 3 – 7 MV/cm, and a high-field region above 7 MV/cm. As compared to the pure SiO_2, the Ge4-1E16 shows a more prominent J_{GATE} in the order of 10^{-10} A/cm^2 in the low- and medium-field regions, and a smaller onset field of ~ 7 MV/cm for the abrupt increase of J_{GATE} in the high-field region. The result indicates that the inclusion of a narrow distribution of nc-Ge near the surface of the SiO_2 thin film modifies the current transport behavior. For the Ge4-1E16 sample, the abrupt

increase of J_{GATE} in the high field region could be attributed to the FN tunneling. Since the Ge ion implantation is effective in creating defects in the implanted SiO_2, it is possible that the PF emission of trapped electrons can happen at high electric fields. It is known that while the FN tunneling current has little dependence on temperature, the PF emission current shows a strong temperature dependence [139]. To identify the current conduction mechanisms of the Ge-ion-implanted SiO_2 thin film, measurements of J_{GATE}-E_{OX} characteristics at different temperatures are necessary.

Fig. 3-14 shows the J_{GATE}-E_{OX} characteristics for the annealed Ge4-1E16 sample measured under different temperatures from 25 ºC (room-temperature) to 150 ºC. Under each temperature, the measurement was conducted on a fresh device. As shown in the figure, in the low- and medium-field region, the slowly increasing J_{GATE} shows a strong temperature dependence, i.e., the J_{GATE} under the same E_{OX} increases with temperature. However, as E_{OX} reaches 7 MV/cm, the J_{GATE}-E_{OX} curves tend to converge. In the high field region, the J_{GATE}-E_{OX} curves measured under different temperatures show an abrupt increase in J_{GATE} without any obvious dependence on the measurement temperature. Apparently, more than one conduction mechanisms are present in the Ge4-1E16 sample under different E_{OX}. It should be noted that when E_{OX} is beyond 9 MV/cm, increasing temperature causes a slight increase of the J_{GATE}, and dielectric breakdown occurs for some devices. At such a high electric field, the current transport in a dielectric layer is affected by effects such as impact ionization, trap generation, oxide degradation and dielectric breakdown [40, 41]. In the present study, only the current transport behavior for $E_{OX} < 9$ MV/cm is investigated.

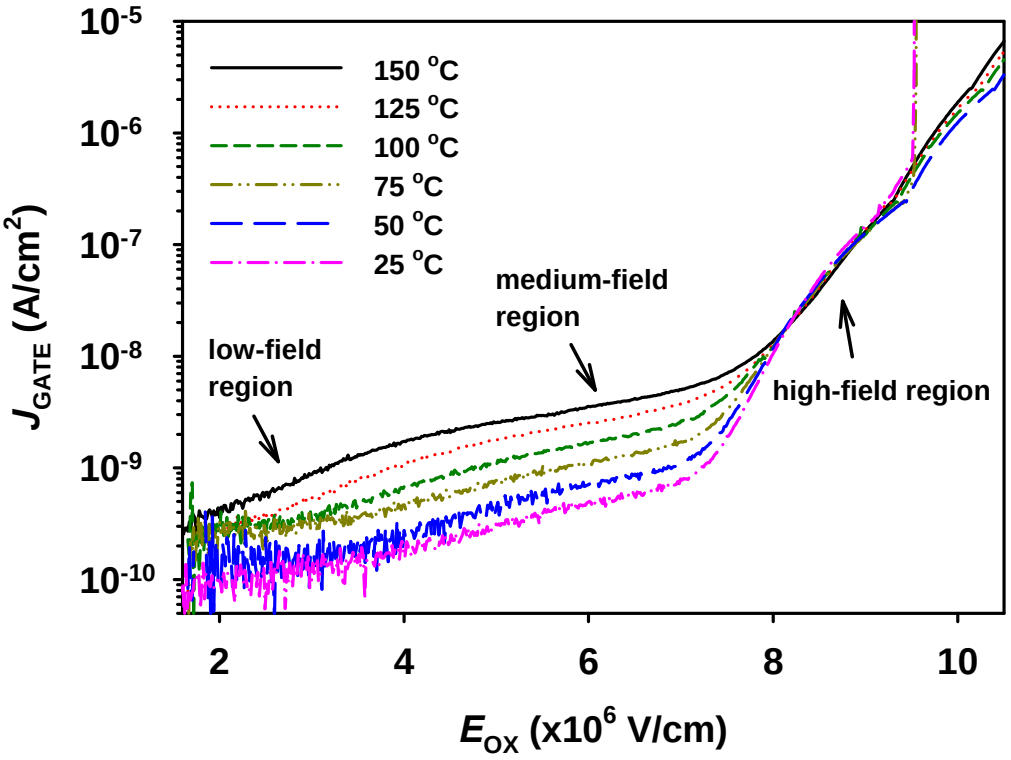

Fig. 3-14 J_{GATE}-E_{OX} characteristics for the annealed Ge4-1E16 sample under various measurement temperature from 25 ºC (room-temperature) to 150 ºC.

3.5.2 Conduction mechanism in the high-field region

The temperature-independent J_{GATE} in the high-field region is investigated first by fitting to a FN tunneling mechanism. Fig. 3-15(a) shows the semi-log plots of J_{GATE}/E_{OX}^2 versus $1/E_{OX}$, i.e., FN plots, for the Ge4-1E16 sample under various temperatures. In the high-field region, these FN plots almost overlap, and a linear relationship in the semi-log plots of J_{GATE}/E_{OX}^2 and $1/E_{OX}$ can be observed. The results confirm that the high-field conduction mechanism for the Ge4-1E16 sample is FN tunneling. The possibility of PF emission can be ruled out because there is no temperature dependence. Based on Eq. (3.1) – (3.3), Φ_{FN} can be derived from the

slope of the FN plots. Fig. 3-15(b) shows the Φ_{FN} for the Ge4-1E16 sample at different measurement temperatures, using $m^* = 0.33m_0$. The Φ_{FN} has a constant value of ~ 2.45 eV, which is independent of the measurement temperature. Note that for the Ge4-1E16 sample, the calculated Φ_{FN} is an effective barrier height for the electrons to enter into the conduction band of the Ge-ion-implanted SiO_2 from the Si conduction band. The calculated Φ_{FN} has a value lower than the barrier height (3.24 eV) at a pure SiO_2 / Si interface. Wolters and Peek proposed that the lowering of the FN barrier height is associated with the existence of traps and is due to the capture of electrons by the traps prior to tunneling [208]. The lowering of the FN tunneling barrier height has also been observed in As^+-implanted oxide [208] and Si^+-implanted oxide [209]. For the case of Ge-ion-implanted SiO_2, it is believed that the barrier lowering is due to the implantation-induced traps, since the oxide contains nc-Ge as well as the dissolved Ge atoms. It will be shown later that the Ge-ion-implantation conditions, i.e., implant energy and dose, have strong effects on the calculated Φ_{FN}.

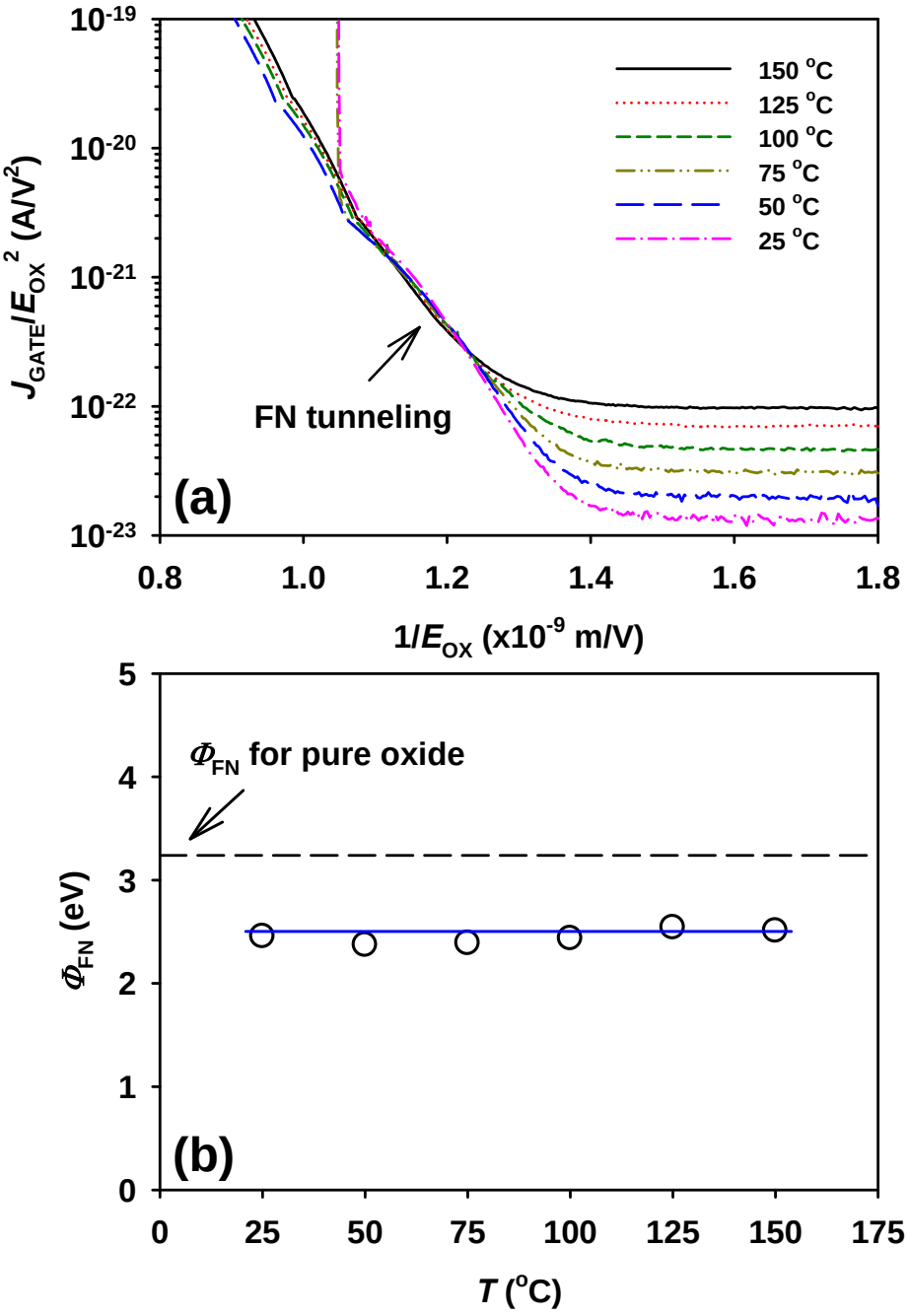

Fig. 3-15 (a) FN plots of J_{GATE}/E_{OX}^2 versus $1/E_{OX}$ for the annealed Ge4-1E16 sample measured at various temperatures. The linear relationship in high-field region of the semi-log plots indicates the occurrence of FN tunneling. (b) The calculated effective barrier height (Φ_{FN}) as a function of the measurement temperature.

3.5.3 Conduction mechanism in the medium-field region

The J_{GATE} in the medium-field region increases as the measurement temperature increases. The strong temperature-dependence of J_{GATE} suggests that the possible current conduction mechanism could be Schottky emission, PF emission or ohmic conduction [139]. The analysis was performed by fitting the experimental data in Fig. 3-14 to the respective current transport mechanisms. According to Eq. (3.4), if the current conduction mechanism is due to Schottky emission, $\ln(J_{GATE}/T^2)$ and $E_i^{1/2}/T$ should follow a linear relationship with a temperature-dependent y-intercept and a temperature-independent slope. Fig. 3-16(a) shows that the medium-field current transport before the occurrence of the FN tunneling can be fitted by the Schottky emission mechanism. The y-intercept [Fig. 3-16(b)] and slope [Fig. 3-16(c)] obtained from the fitting are consistent with Eq. (3.6) and (3.7), respectively. However, the calculated dielectric constant ε_{OX} and barrier height Φ_B are 43.4 and 0.252 eV, respectively. The value of ε_{OX} is not valid, because an appropriate dielectric constant for the SiO_2 embedded with nc-Ge should have a value between 3.9 (i.e., dielectric constant of SiO_2) and 16.2 (i.e., dielectric constant of Ge), based on the approach of effective medium approximation [210]. As pointed out by Sze [195], only the self-consistent value of the dielectric constant can ensure that the current conduction is due to Schottky emission or PF emission. The fitting to the PF emission did not produce a valid value for ε_{OX} as well. Therefore, neither the Schottky emission nor PF emission are deemed as the appropriate mechanisms for the temperature-dependent J_{GATE} in the low-field. Indeed, both the Schottky emission and PF emission require a higher electric field across the oxide [211].

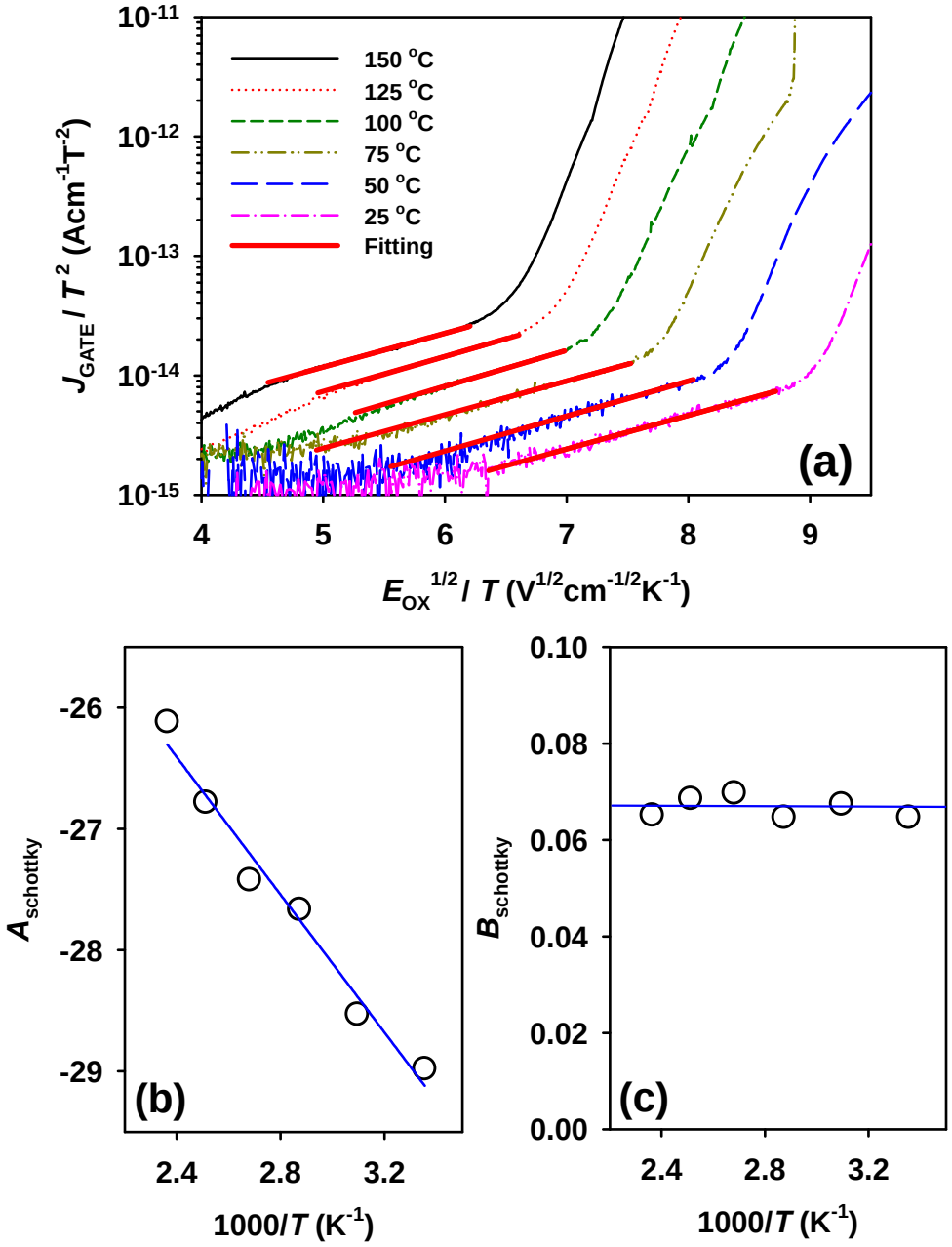

Fig. 3-16 (a) Semi-log plots of J_{GATE}/T^2 versus $E_{OX}^{1/2}/T$ for the annealed Ge4-1E16 sample. The fitting yields a straight line in the medium-field region for each temperature. In (b) and (c), the fitting parameters, $A_{schottky}$ (i.e., y-intercept) and $B_{schottky}$ (i.e., slope), as a function of 1000/T are shown.

On the other hand, as shown in Fig. 3-17, the J_{GATE}-E_{OX} characteristics in the medium-field region before the occurrence of FN tunneling can also be fitted by a linear relationship, implying a possible Ohmic conduction in the medium-field region. According to Eq. (3.12), the slope, i.e., $d(J_{GATE})/d(E_{OX})$, obtained from the linear fitting is a function of ΔE_{ac} (i.e., the activation energy) and temperature. As shown in Fig. 3-18, the relationship between the slope and the temperature agrees with Eq. (3.12). From the figure, ΔE_{ac} is determined as 133 meV. The result indicates that the current transport in the medium-field region is associated with the thermal excitation of electrons from one isolated shallow state / trap to the next. The trap levels, which are created by Ge ion implantation, could be ~ 133 meV below the conduction band of the SiO_2.

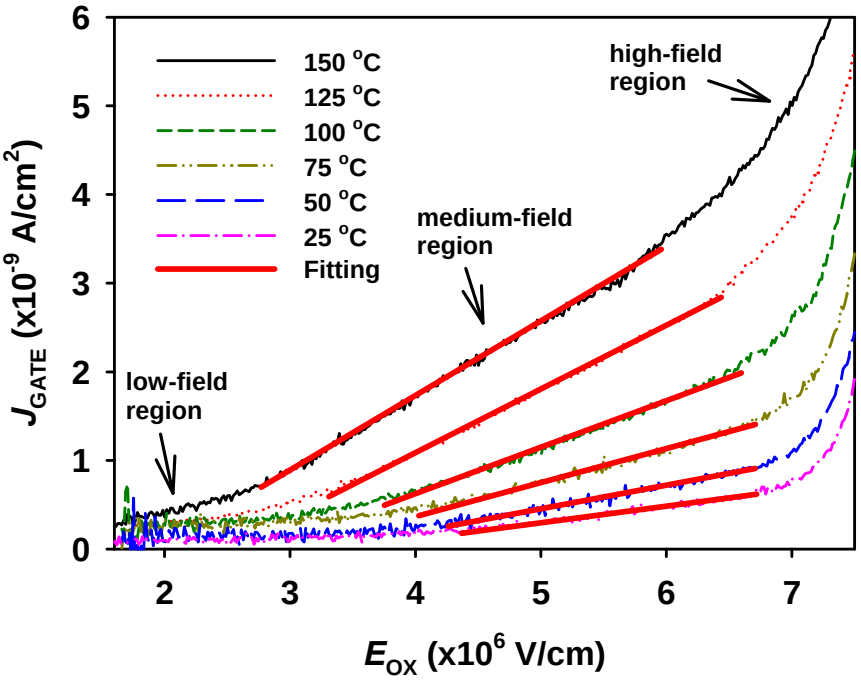

Fig. 3-17 J_{GATE}-E_{OX} plots for the Ge4-1E16 sample. The fitting of the medium-field region indicates the linear relationship between J_{GATE} and E_{OX} for each temperature.

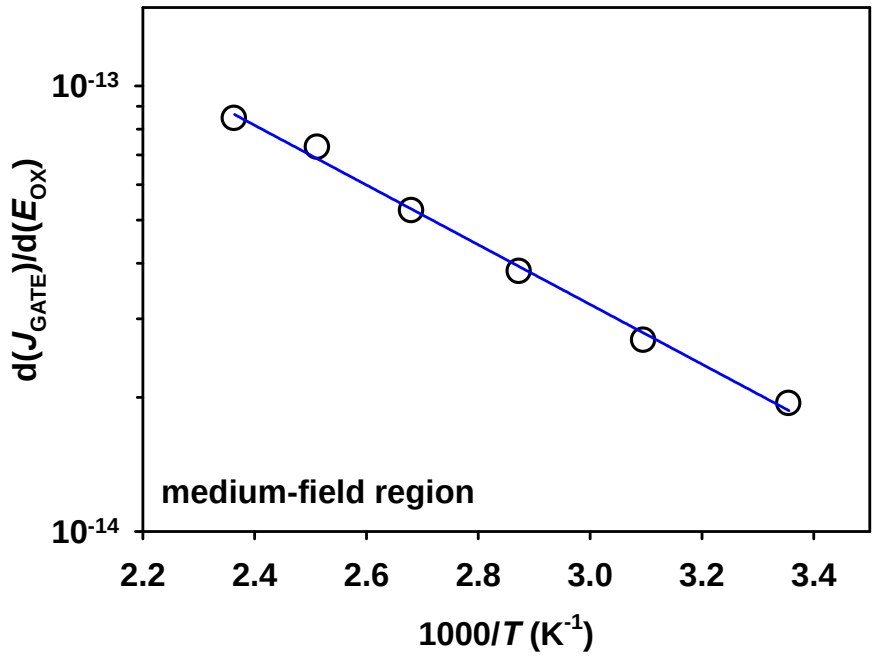

Fig. 3-18 $d(J_{GATE})/d(E_{OX})$ as a function of $1000/T$ obtained from the fitting of the medium-field region in the J_{GATE}-E_{OX} characteristics.

3.5.4 Conduction mechanism in the low-field region

Fig. 3-17 also demonstrates that the J_{GATE}-E_{OX} plot in the low-field region for each temperature can also be roughly seen as a straight line. As the temperature increases, the slope of the straight line also increases, indicating that the transport in the low-field region also follows an Ohmic conduction. As shown in Fig. 3-19, the plot of slope versus $1000/T$ is consistent with the relationship given by Eq. (3.12), and the ΔE_{ac} can be calculated as 248 meV. Note that for each temperature, the slope of the low-field region is lower than that of the medium-field region. The result indicates that in the low-field region, the conductance is lower (i.e., the resistance is higher) than that in the medium-field region.

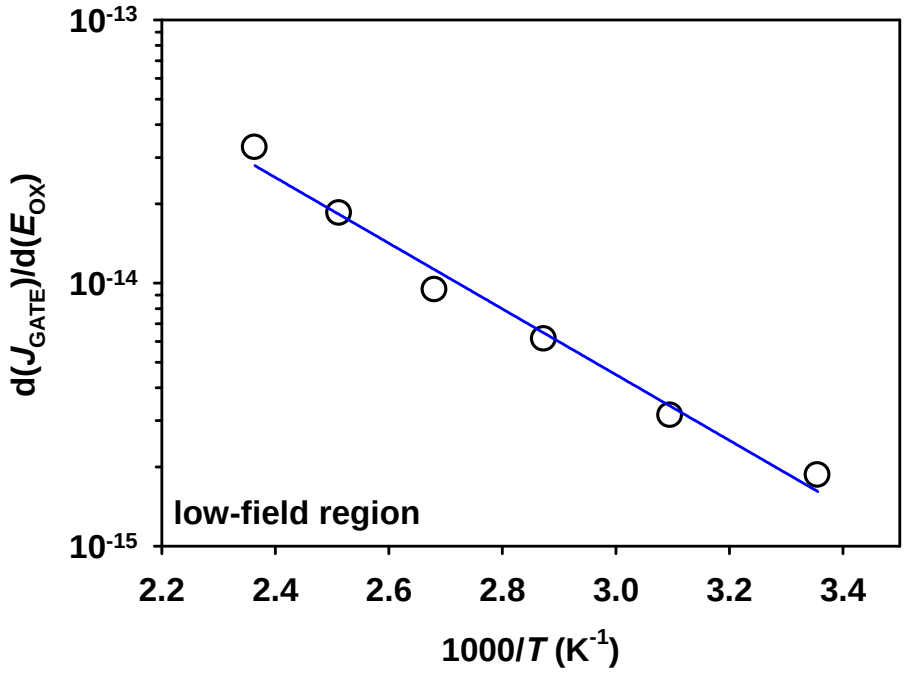

Fig. 3-19 $d(J_{GATE})/d(E_{OX})$ as a function of $1000/T$ obtained from the fitting of the low-field region in the J_{GATE}-E_{OX} characteristics.

3.5.5 Discussions

3.5.5.1 A two-region structure for the explanation of conduction behavior

The current transport behavior of the Ge-ion-implanted SiO_2 thin film with nc-Ge distributed near the SiO_2 surface can be explained as follows. According to the SIMS and TEM results shown in Fig. 3-6 and Fig. 3-7, the Ge-implanted SiO_2 thin film can be virtually divided into two regions in series with each other. As shown in Fig. 3-20, Region 1 is the nc-Ge distributed SiO_2 region containing most of the implanted Ge near the SiO_2 surface, and Region 2 is the "pure SiO_2" region near the Si substrate containing a small amount of dissolved Ge atoms. For the annealed Ge4-

1E16 sample, the thickness of Region 1 is 10 nm and the thickness of Region 2 is 20 nm.

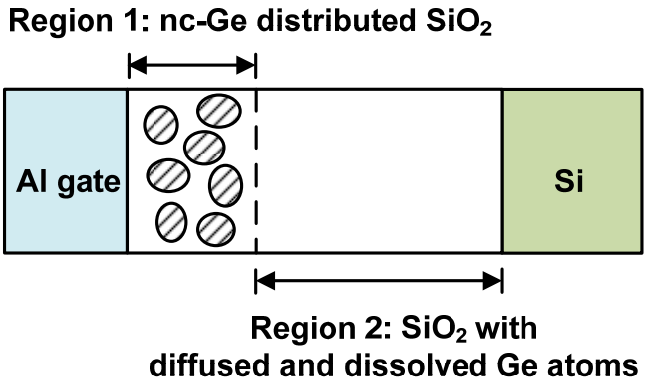

Fig. 3-20 Schematic diagram of the two-region structure for the Ge-ion-implanted SiO_2 containing nc-Ge near the SiO_2 surface.

Because of the different material composition of Region 1 and 2, the transport behavior in Region 1 and 2 is different. The transport behavior of Region 1 and 2 is described as follows. In Region 1, the nanocrystals are separated by the SiO_2 matrix which also contains defect states generated by the Ge ion implantation. For a low electric field across Region 1, the transport of electrons in the SiO_2 matrix is through the thermal excitation of electrons via the defect states in the SiO_2 matrix. Thus, the electron transport is still limited by the SiO_2 matrix and shows an Ohmic conduction. That leads to a large resistance (R_1^{Large}) in Region 1. However, as the electric field across Region 1 increases, the nanocrystals start to contribute to the current transport. The transport of electrons in the nc-Ge distributed SiO_2 becomes easier to happen via nc-assisted conduction, such as the tunneling of electrons from one nc-Ge to the next across the small distance between two adjacent nc-Ge, or the PF emission of electrons

from nc-Ge to the SiO_2 conduction band. The nc-assisted conduction results in a smaller resistance (R_1^{Small}) for Region 1. Note that R_1^{Large} and R_1^{Small} only represent the typical oxide resistances when the electric field is low and high, respectively. Because of the small distance between adjacent nc-Ge, a relatively low electric field is sufficient for Region 1 to change its resistance from R_1^{Large} to R_1^{Small}. On the other hand, Region 2 is the "pure SiO_2" region containing a small amount of dissolved Ge atoms which behave as defect states in the SiO_2 and contribute to the electron transport. Therefore, the transport of electrons in Region 2 is similar to that in a pure SiO_2, which exhibits an enhanced conduction (i.e., a reduction in the resistance) when the electric field increases. For a low electric field across Region 2, the conduction of electrons in Region 2 is limited by the SiO_2, which results in an Ohmic conduction with a large resistance (R_2^{Large}). However, the existence of Ge atoms acting as defect states causes the resistance to be lower than in the pure SiO_2, because the electron conduction is through the thermal excitation of electrons via the defect states caused by the Ge atoms. When the electric field across Region 2 is sufficiently high, the FN tunneling of electrons across the SiO_2 / Si barrier occurs, resulting in a significantly enhanced conduction with a small resistance (R_2^{Small}). Apparently, as compared to Region 1, Region 2 requires a much higher electric field to change the oxide resistance from R_2^{Large} to R_2^{Small}, because of the relatively thick SiO_2 (~ 20 nm). Based on this two-region structure, the observed current transport behavior can be understood.

3.5.5.2 Current transport behavior in the low-field region

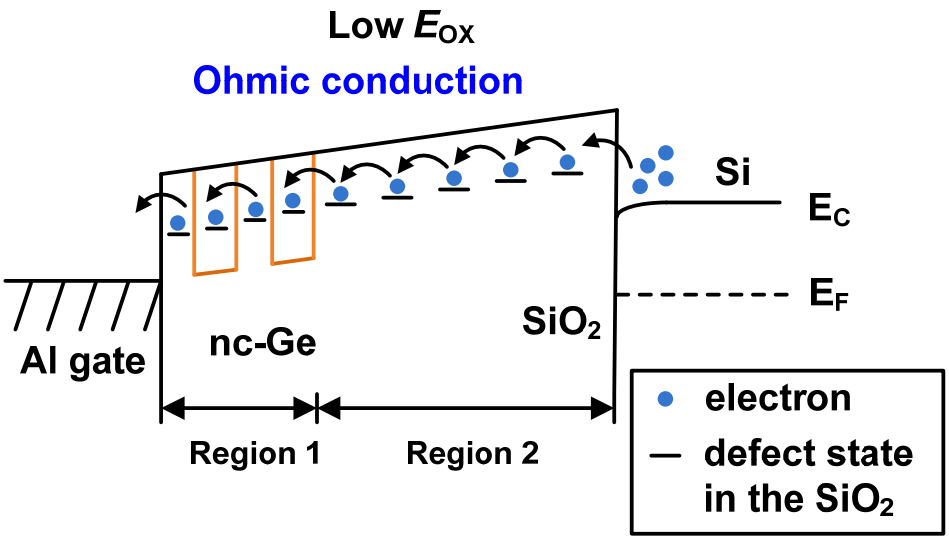

Fig. 3-21 Energy band diagram of the Ge-ion-implanted SiO_2 under a low E_{OX} (i.e., in the low-field region).

As shown in Fig. 3-21, for a low E_{OX} (i.e., in the low-field region), the electric fields across both Region 1 and 2 are low. Since the electric field across Region 1 is not sufficient to cause the nc-assisted conduction, the current transport in Region 1 is limited by the Ge-ion-implanted SiO_2 matrix. The electron transport in Region 1 is through the thermal excitation of electron from one implanted-generated defect state to the next, leading to Ohmic conduction with a large resistance of R_1^{Large}. Meanwhile, the electric field across Region 2 is not high enough for FN tunneling to occur, thus the current transport in Region 2 is also Ohmic with a large resistance of R_2^{Large}. The electron transport in Region 2 is associated with the defect states caused by the dissolved Ge atoms. Therefore, in the low-field region, the small leakage current of

the Ge-ion-implanted SiO_2 thin film arises from the Ohmic conduction in Region 1 and 2 with a total resistance of $R_1^{Large} + R_2^{Large}$.

3.5.5.3 Current transport behavior in the medium-field region

Fig. 3-22 shows the situation for a medium E_{OX} (i.e., in the medium-field region). As described previously, due to the small separation of the nc-Ge in Region 1, the electric field required for the nc-assisted conduction is not very high. Therefore, under a medium E_{OX}, the electric field across Region 1 is high enough to cause a great enhancement of conduction in Region 1 due to the nc-assisted conduction. That leads to a small resistance, i.e., R_1^{Small}, for Region 1. On the other hand, since the electric field across Region 2 is still not high enough to cause the onset of FN tunneling across the ~ 20 nm "pure SiO_2" region, the conduction in Region 2 still follows an Ohmic conduction process with a large resistance of R_2^{Large}, which is much larger than R_1^{Small}. Therefore, in the medium-field region, the electron transport in the entire Ge-ion-implanted SiO_2 thin film is mainly limited by the conduction in Region 2. Once the transported electrons reach Region 1, they can be easily injected into the Al gate by the nc-assisted conduction. That explains the observed Ohmic conduction in the medium-field region. The total oxide resistance of the Ge-ion-implanted SiO_2 thin film in the medium-field region is $R_1^{Small} + R_2^{Large}$. Apparently, the conductance in the medium-field region is higher (or the resistance is lower) than that in the low-field region, which has a total resistance of $R_1^{Large} + R_2^{Large}$. That agrees with the previous result that the activation energy ΔE_{ac} for the medium-field region is lower than that of the low-field region.

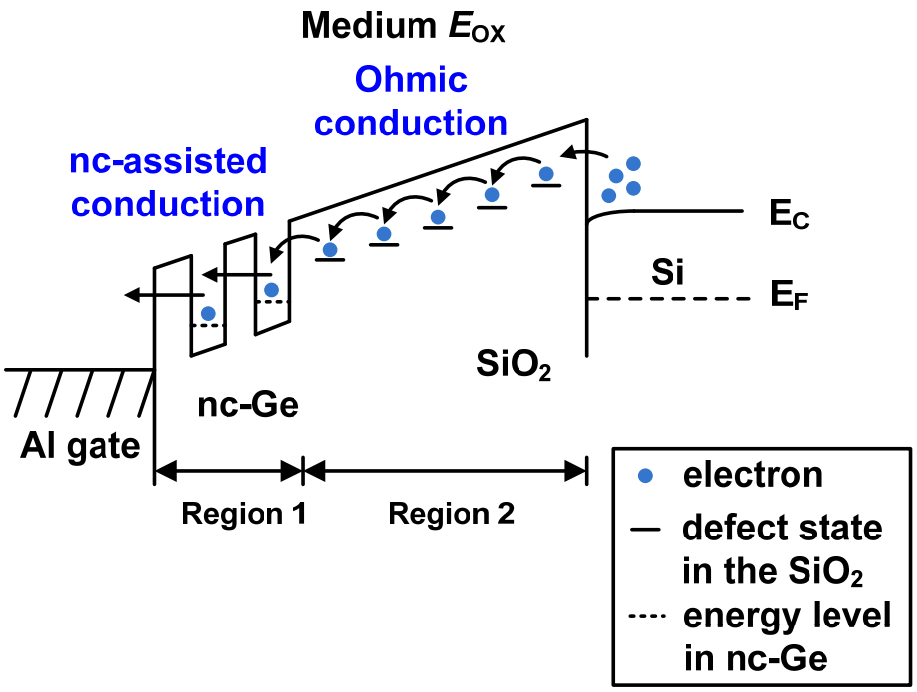

Fig. 3-22 Energy band diagram of the Ge-ion-implanted SiO_2 under a medium E_{OX} (i.e., in the medium-field region).

3.5.5.4 Current transport behavior in the high-field region

Fig. 3-23 shows the situation for a high E_{OX} (i.e., in the high-field region). Under this condition, the electric field across Region 1 is high enough for the nc-assisted conduction to happen, leading to a good conduction in Region 1. As a result, the overall current transport in the Ge-ion-implanted SiO_2 mainly depends on the electron transport in Region 2. As the E_{OX} increases, the electric field across Region 2 also increases. When the electric field across Region 2 is sufficiently high, electrons are injected from the Si substrate into the conduction band of the SiO_2 (Region 2) by the FN tunneling of electrons across the triangular barrier at the SiO_2 / Si interface.

The injected electrons can then be easily injected into the Al gate through the nc-assisted conduction in Region 1. Therefore, under a high E_{OX}, a significant increase in the current that follows the FN tunneling mechanism is observed.

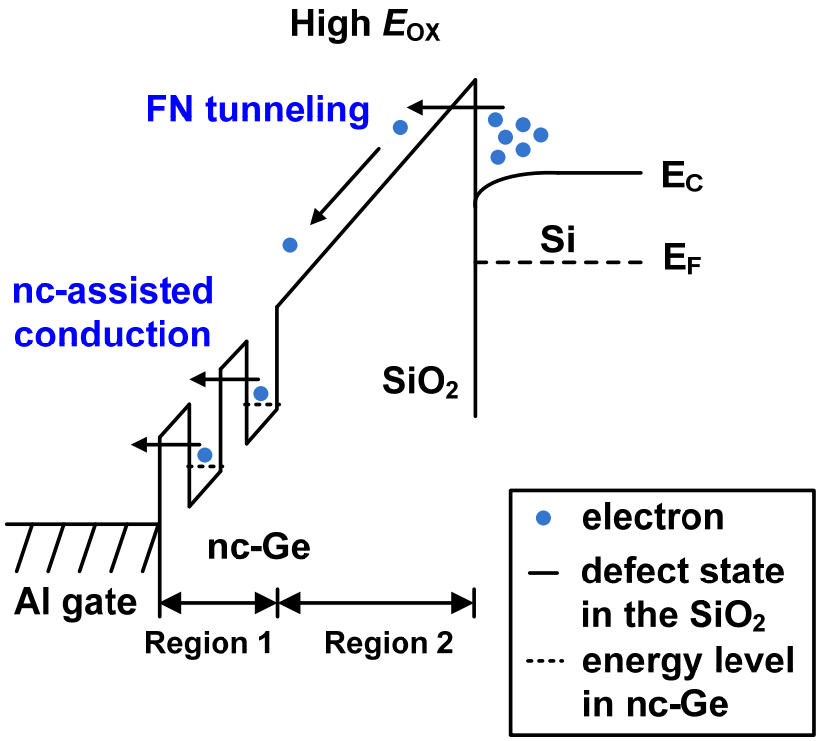

Fig. 3-23 Energy band diagram of the Ge-ion-implanted SiO_2 under a high E_{OX} (i.e., in the high-field region).

3.5.5.5 Effects of implant dose and energy on the effective tunneling barrier height

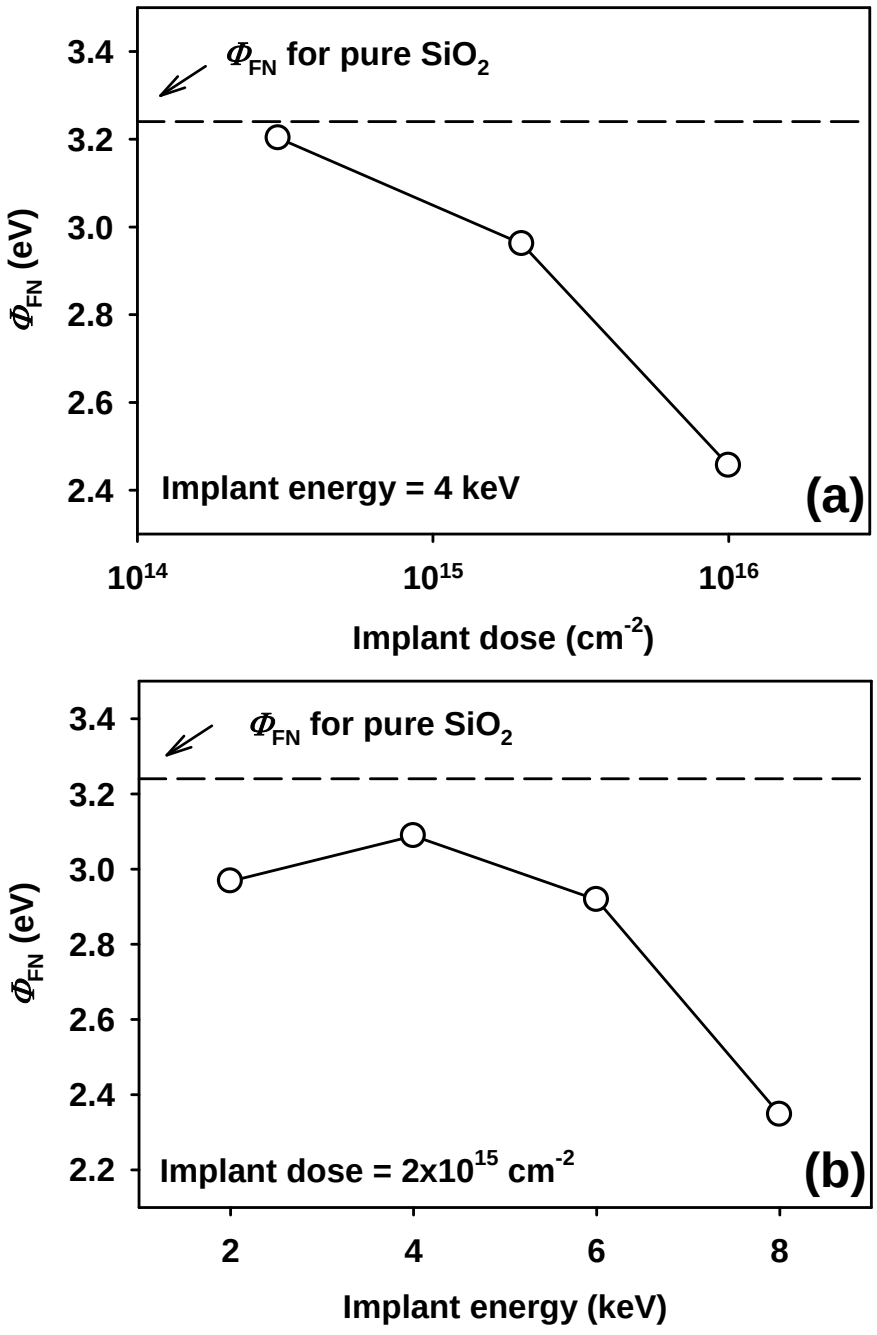

Fig. 3-24 Effective FN tunneling barrier height (Φ_{FN}) as functions of (a) the implant dose, and (b) the implant energy for the SiO_2 thin films containing near-surface nc-Ge.

Fig. 3-24(a) shows the effect of the implant dose on the effective tunneling barrier height Φ_{FN} for Group II samples, i.e., samples with the same implant energy of 4 keV but different implant doses. The Φ_{FN} values were extracted from the temperature-independent high-field region in the FN plots for each sample. As shown in the figure, the Φ_{FN} drops from 3.2 to 2.4 eV when the implant dose increases from 3×10^{14} to 1×10^{16} cm^{-2}. On the other hand, Fig. 3-24(b) shows the effect of the implant energy on Φ_{FN} for Group I samples, i.e., samples with the same implant dose of 2×10^{15} cm^{-2} but different implant energies. When the implant energy increases from 2 to 4 keV, the Φ_{FN} slightly increases from 3 to 3.1 eV. However, further increase in the implant energy from 4 to 8 keV leads to the reduction of Φ_{FN} from 3.1 to 2.3 eV.

As mentioned previously in Section 3.5.5.4, under a high E_{OX}, the observed conduction behavior of the SiO_2 thin film containing nc-Ge distributed near the SiO_2 surface can be described by the tunneling of electrons from the Si substrate through the two-region structure. Due to the distribution of the nc-Ge in Region 1 near the SiO_2 surface and the presence of defect states (i.e., traps) created by the dissolved Ge atoms in Region 2 near the Si substrate, the tunneling of electrons becomes easier. As a result, the effective barrier height Φ_{FN} is lower than that of the pure SiO_2. When more traps are present in the oxide, a more significant lowering of Φ_{FN} is expected. Thus, the observed relationship between the calculated Φ_{FN} and the implant conditions can be explained. For samples with the same implant energy but different implant doses, the nc-Ge concentration in Region 1 increases with the implant dose. Besides, the amount of dissolved Ge atoms in Region 2 also increases with the implant dose, because more Ge atoms are diffused from the Ge-implanted region toward the Si

substrate along the concentration gradient. Thus, more traps are available in the oxide, leading to a decrease of Φ_{FN} when the implant dose increases. On the other hand, for the samples with the same implant dose but different energies, as mentioned previously in Section 3.4.1, the Ge concentration in Region 1 reduces with the implant energy as a result of the constant implant dose. That leads to fewer traps in Region 1 and Φ_{FN} tends to increase. However, the amount of dissolved Ge atoms in Region 2 also increases with the implant energy because of the broader Ge distribution. That leads to more traps in Region 2 and Φ_{FN} tends to decrease. Thus, as the implant energy increases from 2 to 4 keV, Φ_{FN} increases, suggesting that the reduction of Ge concentration in Region 1 plays a dominant role for the case of lower implant energy. However, further increase in the implant energy from 4 to 8 keV reduces Φ_{FN}, suggesting that the increase of the amount of dissolved Ge atoms in Region 2 near the SiO_2 / Si interface plays a more important role for the case of higher implant energy.

It should be noted that the effective tunneling barrier height is also affected by the defect states present at the SiO_2 / Si interface. It is well-known that the SiO_2 thin film grown by the dry oxidation tends to produce a good Si / SiO_2 interface with a low density of interface states [139]. However, it has been reported that when the distribution of implanted Ge atoms is close to the Si substrate, the diffusion of Ge atoms during the high-temperature annealing process tends to result in an accumulation of Ge atoms at SiO_2 / Si interface [49, 212]. That can alter the interface property and lead to the interface charge injection due to the additional interface states. In the present discussion, the contribution of the interface charge injection as a result of the Ge accumulation at the SiO_2 / Si interface is not considered. That is because the

implanted Ge ions are confined in the SiO_2 thin film near the SiO_2 surface. As revealed by the SIMS profiles in Fig. 3-6, no additional Ge peak can be observed at the SiO_2 / Si interface, suggesting that the interface charge injection caused by the Ge accumulation at the SiO_2 / Si interface is negligible in our samples.

3.5.5.6 Dielectric strength of the Ge-ion-implanted SiO_2

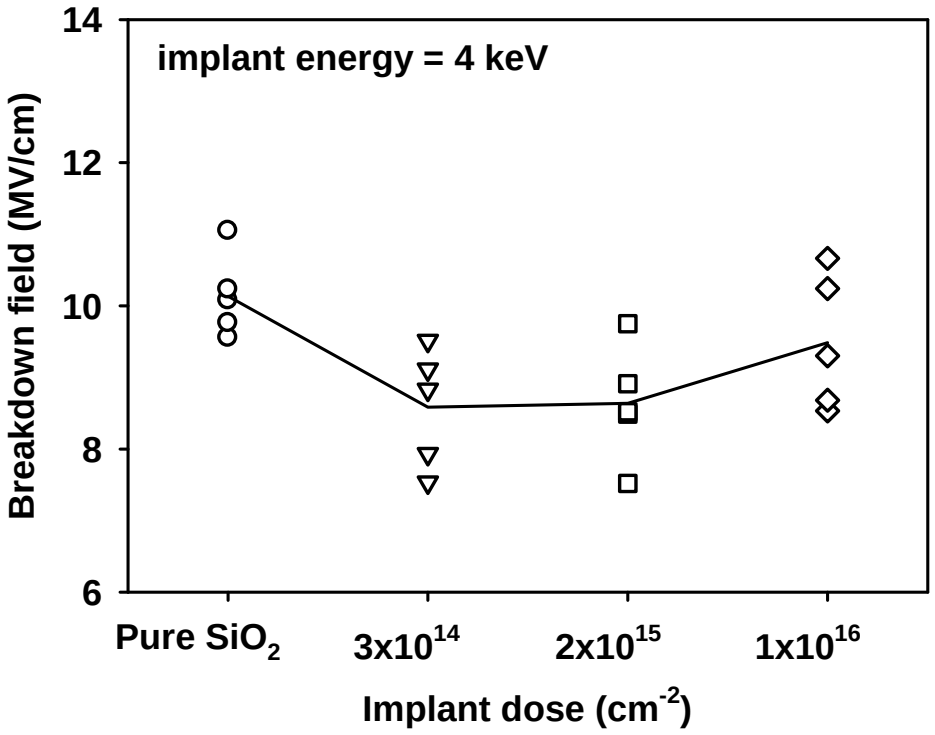

Fig. 3-25 Breakdown fields for the pure SiO_2 and samples with different implant doses. Each sample was measured 5 times on different pads.

The dielectric strength of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge is important to the operation and reliability of a non-volatile memory device based on nc-Ge. In Fig. 3-12, it is apparent that the dielectric breakdown occurs for

both the pure SiO_2 and the Ge-ion-implanted SiO_2 when the E_{OX} is larger than 9 MV/cm. The breakdown fields for the pure SiO_2 and Group II samples (i.e., samples with the same implant energy of 4 keV but different implant doses) were obtained from the *I-V* measurements at a ramp rate of ~ 55.2 mV/s. Each sample was measured 5 times on different pads. As shown in Fig. 3-25, the average breakdown field for the pure SiO_2 is 10.14 MV/cm. For an implant dose of 3×10^{14} cm^{-2}, the average breakdown field drops to 8.58 MV/cm. However, further increase in the implant dose increases the dielectric strength. The average breakdown field for an implant dose of 1×10^{16} cm^{-2} is 9.48 MV/cm.

The dielectric breakdown behavior of a pure SiO_2 has been extensively studied [139, 213, 214]. The catastrophic breakdown has been attributed to the random generation of defects by injected energetic electrons / holes and the subsequent formation of a conduction path connecting the gate electrode and the Si substrate when the defects are dense enough. The observed dependence of the breakdown field on the implant dose can be explained as follows. When the SiO_2 thin film is implanted with Ge ions, the dielectric strength is weaken because of the implantation-induced damage in SiO_2. When the implant dose increases, the breakdown field could be reduced because more damages are created. On the other hand, trapping of electrons in the nc-Ge also occurs during the *I-V* measurement with positive gate voltages. Due to the Coulomb interaction between the trapped electrons in nc-Ge and the injected electrons from Si substrate to the gate electrode, fewer defects are generated in the vicinity of nc-Ge, and the possibility of forming a conduction path that leads to a catastrophic breakdown is reduced. Thus, the increase in the implant dose could also

lead to an increase in the breakdown field because more nc-Ge are formed in the SiO_2 thin film. For the 3×10^{14} cm^{-2} sample, the electron trapping in nc-Ge is not significant because the nc-Ge density is low. Thus, the breakdown field is lowered due to the damages caused by the implantation. However, for higher implant doses, e.g., 2×10^{15} cm^{-2} and 1×10^{16} cm^{-2}, the electron trapping in nc-Ge is more significant because the nc-Ge density is much higher. Thus, the dielectric strength is recovered, and the breakdown field increases with the implant dose.

3.5.6 Conclusion

In this section, the current transport behavior of the SiO_2 thin films containing nc-Ge in a narrow layer near the SiO_2 surface has been investigated. From the J_{GATE}-E_{OX} characteristics measured at various temperatures, it has been found that the J_{GATE} is temperature-dependent under low and medium E_{OX}, but becomes temperature-independent under high E_{OX}. To explain the current transport behavior, a model using a two-region structure has been proposed: Region 1 is the nc-Ge distributed region near the oxide surface and Region 2 is the SiO_2 region containing dissolved Ge atoms close to the Si substrate. The different conduction mechanisms dominating in different oxide field regions have been discussed. For the low E_{OX}, the temperature-dependent J_{GATE} has been explained by Ohmic conduction in both Region 1 and Region 2. For the medium E_{OX}, the temperature-dependent J_{GATE} has been explained by the nc-assisted conduction in Region 1 and the Ohmic conduction in Region 2. Lastly, for the high E_{OX}, the temperature-independent J_{GATE} has been explained by the nc-assisted conduction in Region 1 and the FN tunneling of electrons from the Si substrate across Region 2. Moreover, the effects of Ge ion implantation conditions, i.e., implant dose

and energy, on the lowering of the effective FN tunneling barrier height has been discussed. It has been found that the tunneling barrier height is strongly affected by the distribution of the implanted Ge in the SiO_2. The dielectric breakdown behavior of the Ge-ion-implanted SiO_2 thin films has also been discussed.

3.6 Current transport in SiO_2 with nc-Ge distributed throughout the SiO_2

The current transport behavior of the Ge-ion-implanted SiO_2 thin films fabricated with low implant energies (2 – 8 keV) has been described by the aforementioned two-region model which consists of a nc-Ge distributed SiO_2 region near the Al gate and a SiO_2 region containing dissolved Ge atoms near the Si substrate. However, for a higher implant energy (e.g., 16 keV), the distribution of implanted Ge is much broader, resulting in the formation of nc-Ge throughout the SiO_2. It is found that the current transport behavior for the implant energy of 16 keV is different from the situation for low implant energies of 2 – 8 keV. In this section, the current transport behavior of the SiO_2 thin film containing nc-Ge distributed throughout the SiO_2 is investigated.

3.6.1 Characteristics of gate current density versus electric field

In this part, the annealed Ge16-1E16 sample implanted with an energy of 16 keV and a Ge ion dose of 1×10^{16} cm^{-2}, is studied. Fig. 3-26 shows the J_{GATE}-E_{OX} characteristics of the annealed Ge16-1E16 sample measured at different temperatures. The J_{GATE}-E_{OX} curves can be generally divided into two regions, i.e., a low-field

region for E_{OX} smaller than 6 MV/cm and a high-field region for E_{OX} larger than 6 MV/cm. In the low-field region, the magnitude of J_{GATE} is small (i.e., in the order of 10^{-9} – 10^{-10} A/cm^2). J_{GATE} increases with applied E_{OX} and shows a strong temperature-dependence. Under the same E_{OX}, J_{GATE} is enhanced as the measurement temperature increases. On the other hand, in the high-field region, a rapid increase in J_{GATE} can be observed. J_{GATE} in the high-field region also shows a strong temperature-dependence, i.e., J_{GATE} becomes larger as the temperature increases. The observed current transport of the Ge16-1E16 sample is different from that of the Ge4-1E16 sample. In particular, in the high-field region, the Ge16-1E16 sample shows a temperature-dependent J_{GATE}, while the Ge4-1E16 sample shows a temperature-independent J_{GATE}.

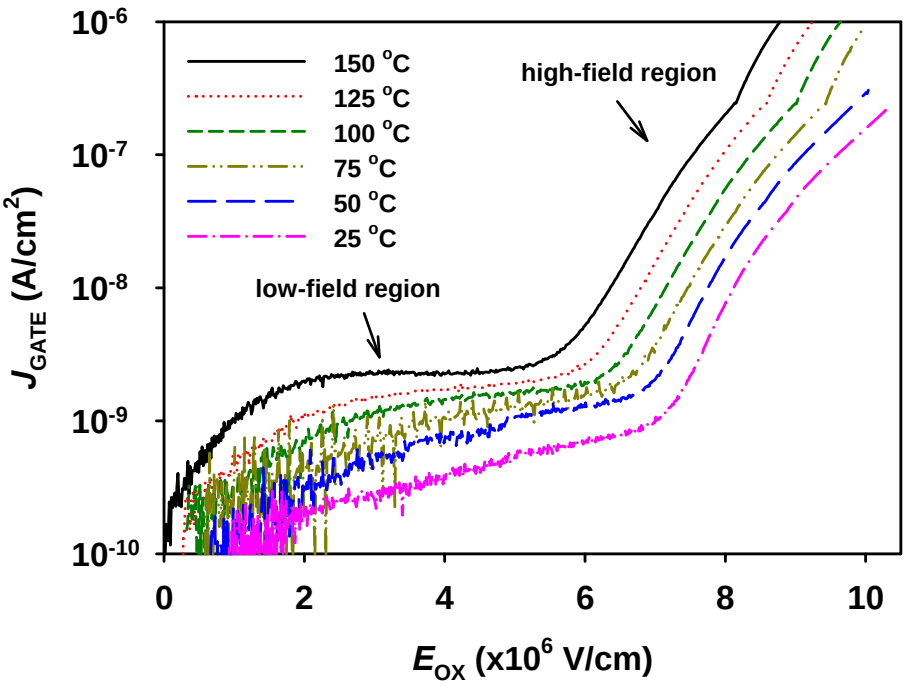

Fig. 3-26 J_{GATE}-E_{OX} characteristics for the annealed Ge16-1E16 sample under various measurement temperature from 25 ºC (room-temperature) to 150 ºC.

3.6.2 Conduction mechanism in the high-field region

In the high-field region, the J_{GATE}-E_{OX} characteristics of the annealed Ge16-1E16 sample show strong temperature-dependence, implying a possible PF emission [193]. As shown in Fig. 3-27(a), for each temperature, a straight line can be observed in the high-field region of the semi-log plot of J_{PF}/E_{OX} versus $E_{OX}{}^{1/2}$ (i.e., the PF plot). Based on Eq. (3.9), it is known that a linear relationship between $\ln(J_{PF}/E_{OX})$ and $E_{OX}{}^{1/2}$ is an indication of PF emission. From the fitting, the y-intercept and slope of the straight line can be obtained. In Fig. 3-27(b), it can be observed that the y-intercept linearly depends on 1000/T, which is consistent with Eq. (3.10). The barrier height Φ_{PF} can be extracted as 1.08 eV. Thus the energy level corresponding to the PF emission of electrons is at ~ 1.08 eV below the SiO_2 conduction band. On the other hand, as shown in Fig. 3-27(c), the slope of the straight line in Fig. 3-27(a) is also a linear function of 1000/T. Based on Eq. (3.11), the ε_{OX} can be determined as 5.19. A self-consistent dielectric constant is required for an appropriate fitting using the PF emission [195]. The value of ε_{OX} is consistent with the dielectric constant of the SiO_2 embedded with nc-Ge, as predicted by the effective medium approximation [210], which yields an ε_{OX} in between 3.9 (the dielectric constant of SiO_2) and 16.2 (the dielectric constant of bulk Ge).

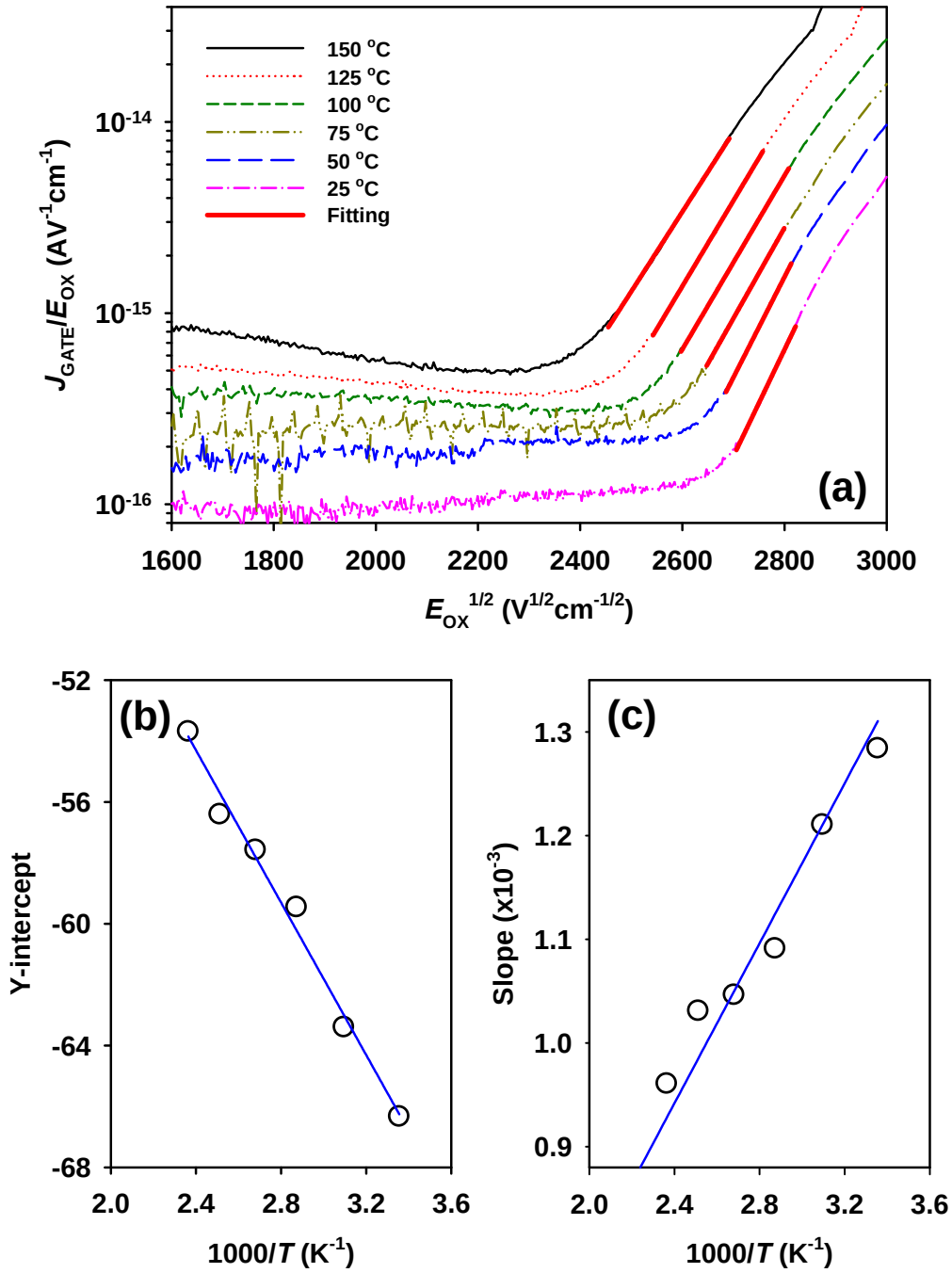

Fig. 3-27 Semi-log plots of J_{GATE}/E_{OX} versus $E_{OX}^{1/2}$ for the annealed Ge16-1E16 sample measured at various temperatures. The fitting in the high-field region yields a straight line for each temperature. The temperature-dependent y-intercept and slope obtained from the fitting of PF plots are shown in (b) and (c), respectively.

3.6.3 Conduction mechanism in the low-field region

The J_{GATE}-E_{OX} characteristics for the annealed Ge16-1E16 sample in the low-field regions also show a strong temperature-dependence. As shown in Fig. 3-28(a), at 25 ºC (room-temperature), the J_{GATE}-E_{OX} curve below E_{OX} = 6 MV/cm (i.e., the onset of the PF emission) can be fitted by a straight line, implying that the current transport in the low-field region could be attributed to Ohmic conduction. For higher temperatures, part of the low-field region can still be fitted by a straight line. Fig. 3-28(b) shows the slope obtained from the linear fitting as a function of the measurement temperature. The relationship between the slope and the temperature is consistent with Eq. (3.12), which yields a ΔE_{ac} of 165 meV. Thus, the defect states responsible for the Ohmic conduction are at 165 meV below the conduction band of SiO_2. In Fig. 3-28(a), it can also be observed that the range of linear relationship between J_{GATE} and E_{OX} becomes smaller when the temperature increases. For example, the 75 ºC curve shows a linear relationship between J_{GATE} and E_{OX} from 0 to 5 MV/cm. However, for the case of 150 ºC, the linear relationship can only be observed from 0 to 2 MV/cm, after which the increase of J_{GATE} becomes slower. When the E_{OX} is in the range of 3 – 5 MV/cm, a reduction in J_{GATE} with E_{OX} can be observed. The result suggests that a process with the effect of reducing the current conduction happens at high temperature when the E_{OX} is in the low-field region before the onset of PF emission. This will be explained in the following discussion.

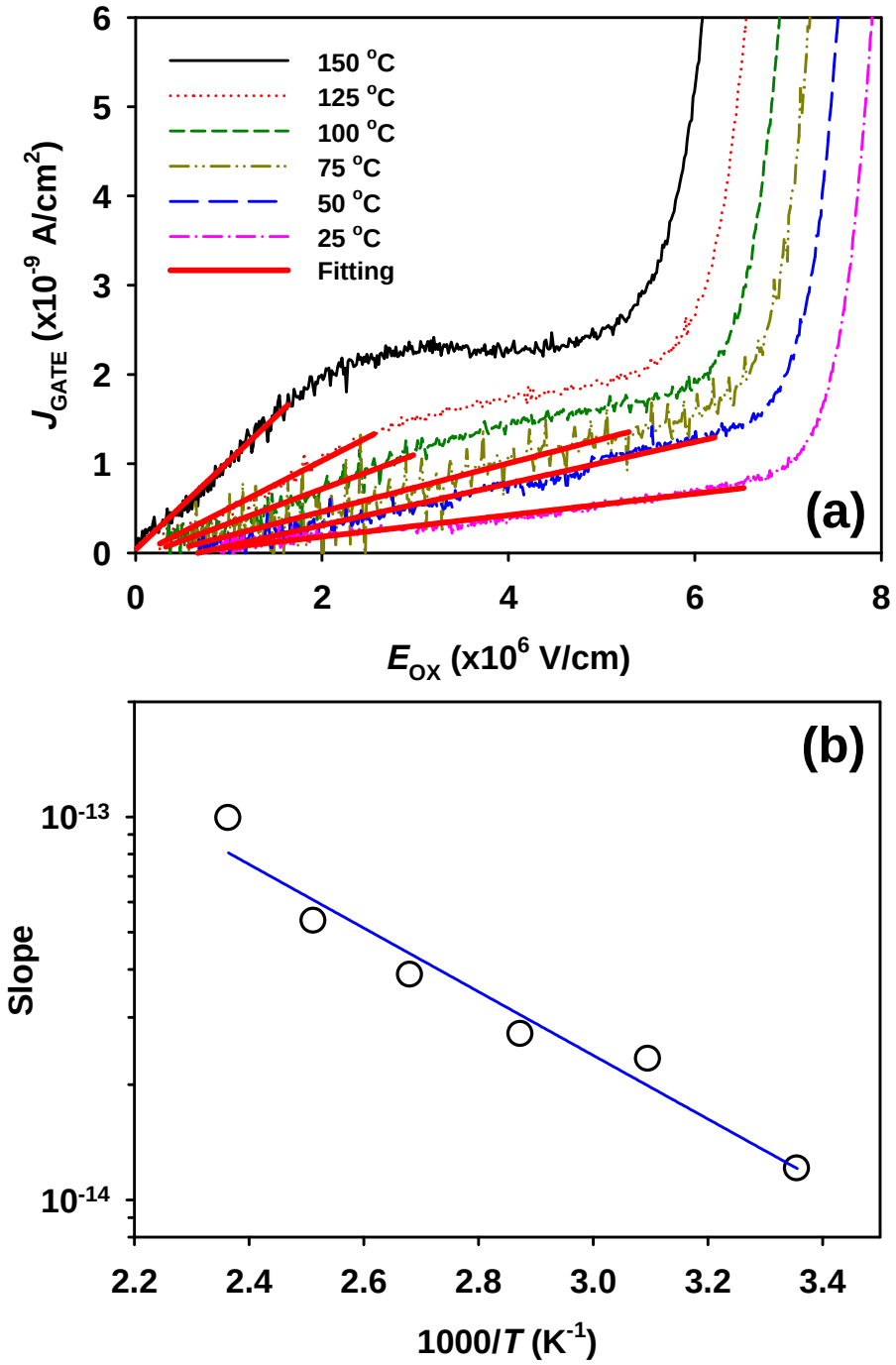

Fig. 3-28 Plots of J_{GATE} versus E_{OX} for the annealed Ge16-1E16 sample measured at various temperatures. The low-field region can be partially fitted by a straight line. In (b), the slope as a function of 1000/T obtained from the linear fitting is shown.

3.6.4 Discussions

3.6.4.1 A one-region structure for the explanation of conduction behavior

Fig. 3-29 shows the schematic diagram of the annealed Ge16-1E16 sample, which is a typical Ge-ion-implanted SiO_2 thin film containing nc-Ge distributed throughout the SiO_2 matrix. The formation of nc-Ge in the SiO_2 matrix has been confirmed previously by the TEM image (as shown in Fig. 3-10). Besides the formation of nc-Ge, the ion implantation also creates defects in the SiO_2 matrix [46]. Since the high implant energy of 16 keV results in a broad distribution of Ge ions in the entire SiO_2, the implantation-induced defects are also expected to be distributed throughout the entire SiO_2 matrix. Using this one-region structure containing the SiO_2 matrix distributed with nc-Ge and implantation-induced defect states, the current transport behavior of the Ge-ion-implanted SiO_2 thin film containing thoroughly distributed nc-Ge can be explained.

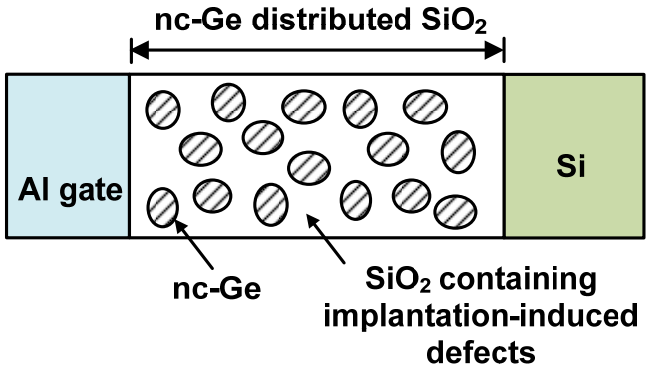

Fig. 3-29 Schematic diagram showing the nc-Ge distributed throughout the SiO_2 thin film.

3.6.4.2 Current transport behavior in the low-field region

As shown in Fig. 3-30, when E_{OX} is low (i.e., in the low-field region), the transport of electrons is limited by the SiO_2 matrix, in which the thermal excitation of electrons happens via the implantation-induced defects / traps. That leads to the observed Ohmic conduction, and J_{GATE} linearly increases with E_{OX}. The Ohmic conduction of electrons in the nc-Ge particles distributed SiO_2 could be accompanied by the charging of nc-Ge due to the multiple confinement of free carriers in nc-Ge [95]. Since the nc-Ge are distributed throughout the SiO_2, the charging of nc-Ge indeed reduces the conduction of the SiO_2 matrix due to the Coulomb interaction between the transported electrons and the charged nc-Ge. At room-temperature (e.g., 25 ºC), the charging effect of nc-Ge is not significant because of the low magnitude of J_{GATE}. Thus, the Ohmic conduction of electrons is not affected by the charging of nc-Ge, and the entire low-field region can be fitted to the linear relationship. However, as the temperature becomes higher, the charging of nc-Ge under the same E_{OX} becomes more significant because J_{GATE} is enhanced. As a result, the charging of nc-Ge occurs at a lower E_{OX}, and the Ohmic conduction of electrons in the low-field region is more significantly affected by the charging of nc-Ge. That explains the observation of smaller range for the linear relationship between J_{GATE} and E_{OX} when the temperature increases. For 150 ºC, the reduction of J_{GATE} with E_{OX} in the range of 3–5 MV/cm is due to the significant charging in the nc-Ge caused by the large J_{GATE}.

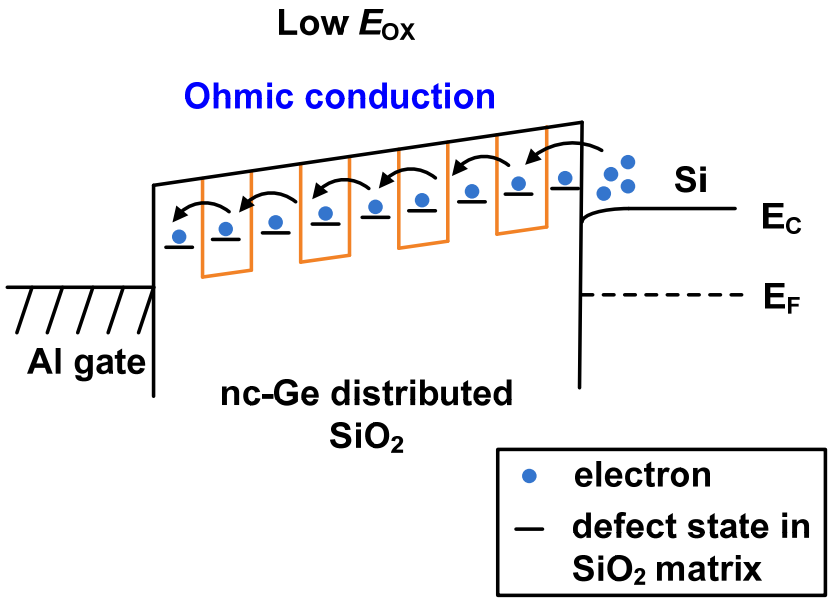

Fig. 3-30 Energy band diagram of the Ge-ion-implanted SiO_2 under a low E_{OX} (i.e., in the low-field region).

3.6.4.3 Current transport behavior in the high-field region

Fig. 3-31 illustrates the current transport behavior when a high E_{OX} is applied (i.e., in the high-field region). Due to the large band bending of SiO_2 caused by the high electric field, the potential barrier of an electron in the conduction band of nc-Ge is modified by the PF effect [193], leading to the thermal excitation of electrons from the nc-Ge to the SiO_2 conduction band. The excited electrons move along the conduction band toward to the Al gate. Because the density of nc-Ge is high, the enhancement in J_{GATE} by PF emission is significant. As the temperature increases, the PF effect which is a field-enhanced thermal excitation becomes more prominent, leading to a strong temperature-dependent J_{GATE}. It should be noted that besides PF emission, the FN tunneling of electrons from the Si substrate into the SiO_2 conduction band is also possible under a high E_{OX}. However, the strong temperature-dependence

of J_{GATE} indicates that the PF emission is the dominant conduction mechanism in the nc-Ge distributed SiO_2 under a high E_{OX}. In this case, the FN tunneling can only play a minor role.

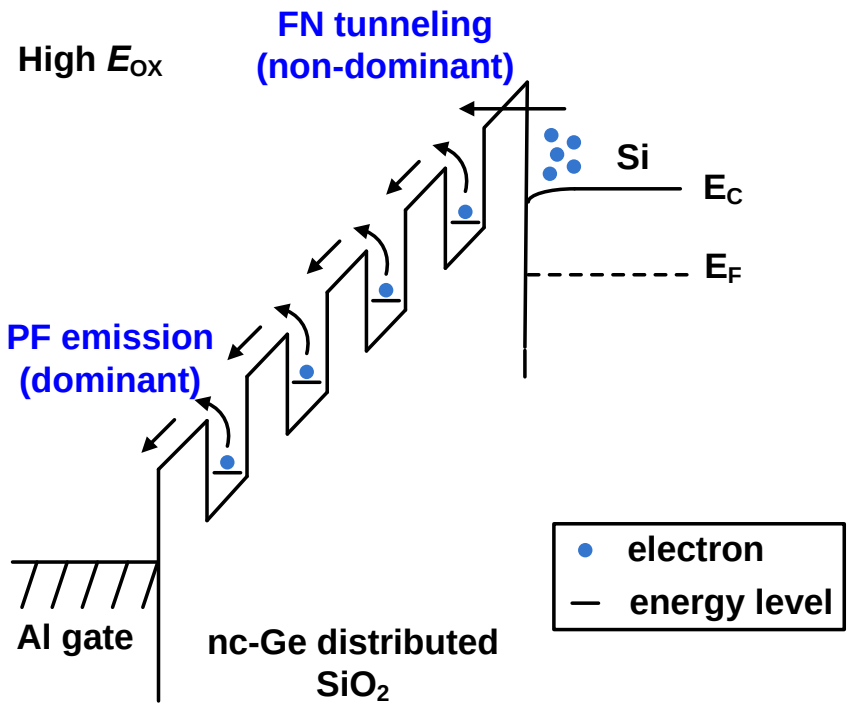

Fig. 3-31 Energy band diagram of the Ge-ion-implanted SiO_2 under a high E_{OX} (i.e., in the high-field region).

3.6.5 Conclusion

The current transport behavior of the SiO_2 thin films distributed with nc-Ge throughout the SiO_2 has been investigated. From the J_{GATE}-E_{OX} characteristics measured at various temperatures, it has been found that the J_{GATE} is temperature-dependent in all E_{OX} regions. A one-region structure with nc-Ge and the implantation-induced defect states distributed throughout the SiO_2 matrix has been proposed to explain the current transport behavior. It has been found that the temperature-

dependent J_{GATE} in the low-field region follows an Ohmic conduction caused by the thermal excitation of electrons via the implantation-induced defect states in the SiO_2 matrix. It has also been found that the Ohmic conduction is affected by the charging of nc-Ge. On the other hand, the temperature-dependent J_{GATE} in the high-field region has been attributed to PF emission caused by the thermal excitation of electrons from the nc-Ge to the SiO_2 conduction band.

3.7 Conduction modulation of SiO_2 embedded with nc-Ge caused by UV illumination

3.7.1 Overview

Ultra-violet (UV) illumination is known to cause the excitation of electrons in semiconductor devices due to its large photon energy. Observations of UV-illumination-induced charging effect in Si nanocrystals and Ag nanoparticles have been reported [215-217]. In this section, the effect of UV illumination on the current conduction of SiO_2 (i.e., gate oxide) embedded with nc-Ge is investigated. The SiO_2 thin film was implanted with Ge ions at 6 keV and an ion dose of 2×10^{15} cm^{-2}. As revealed by the SIMS and TEM analysis, the distribution of nc-Ge is from the SiO_2 surface to a depth of ~ 20 nm in the SiO_2. Unlike the previous MOS structure with an Al gate electrode, a semitransparent ITO layer was used as the gate electrode in order to allow the UV light to penetrate into the SiO_2 embedded with nc-Ge. The results reveal the UV-illumination-induced charging and discharging of nc-Ge, leading to the conduction modulation of the SiO_2 thin film embedded with nc-Ge. Such a new

phenomenon has potential applications in Si-compatible optoelectronic memory devices.

3.7.2 Results and discussions

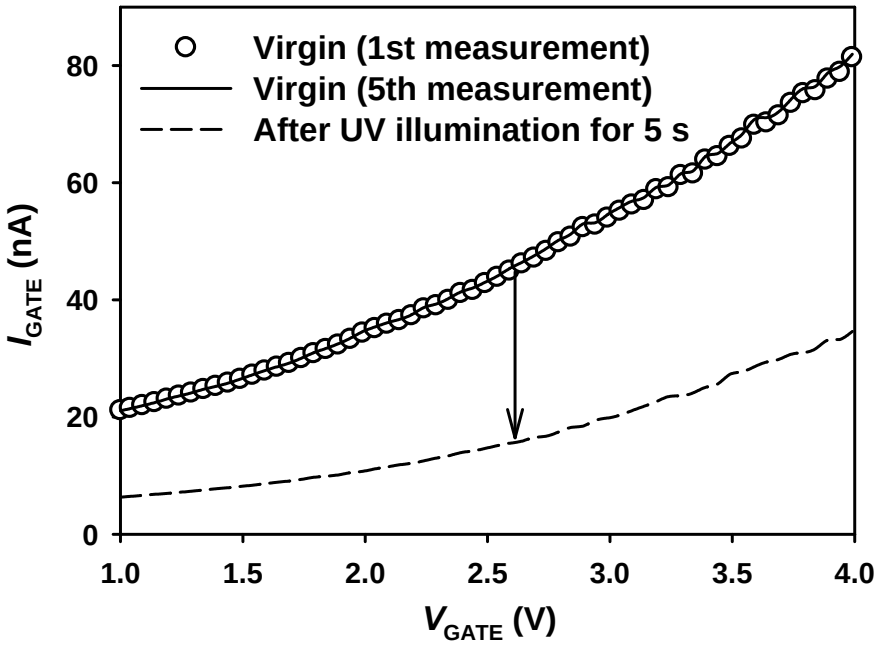

Fig. 3-32 Current-voltage (*I-V*) characteristics before and after UV illumination for 5 s. The repeated *I-V* measurements without UV illumination are also shown.

Fig. 3-32 shows the *I-V* characteristics of the structure with nc-Ge embedded in SiO_2 before UV illumination. Note that the maximum voltage of the *I-V* measurement was set to 4 V, which is low enough to avoid any charging / discharging effect caused by the electrical measurement itself. As can be seen in Fig. 3-32, the repeated measurements did not cause a significant change in the *I-V* characteristic. This indicates that no significant charging or discharging in nc-Ge occurs during the *I-V*

measurement and the conduction of the SiO_2 embedded with nc-Ge was not affected by the measurement itself. However, after an exposure to UV illumination, the *I-V* characteristic is found to change drastically. As can be seen in Fig. 3-32, the current is reduced by more than 50% after UV illumination. The reduction in the current indicates a large increase in the DC resistance (or decrease in the conductance) of the SiO_2 embedded with nc-Ge.

The increase in the DC resistance can be explained in terms of the breaking of some tunneling paths due to charging in some nc-Ge caused by UV illumination. As discussed previously, in the nc-Ge distributed region, the electron conduction can take place between adjacent uncharged nc-Ge via tunneling or other mechanisms under the influence of the external electric field, and a large number of such nc-Ge embedded in the oxide can form many conductive tunneling paths which significantly increase the conductance of SiO_2 embedded with nc-Ge, as shown in Fig. 3-33(a). However, if some of the nc-Ge are charged up, the tunneling paths related to the charged nc-Ge will be blocked due to the Coulomb blockade effect, as shown in Fig. 3-33(b). As a result of the charging in the nc-Ge, the conductance of SiO_2 embedded with nc-Ge decreases. When the sample is exposed to UV illumination, some of the electrons generated by the UV illumination could be trapped in the nc-Ge, leading to a reduction in the oxide conductance. At the same time, the UV illumination could cause the release of the trapped electrons from the nc-Ge also, resulting in an increase in the oxide conductance.

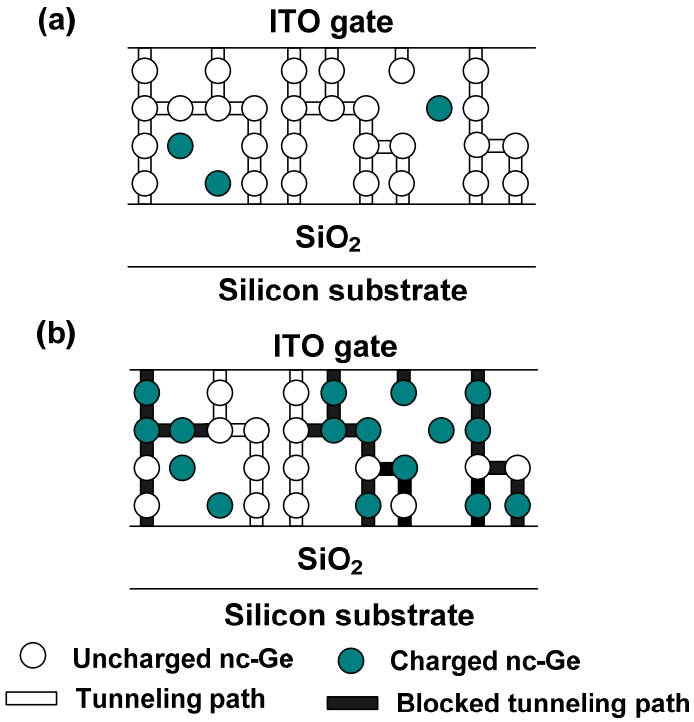

Fig. 3-33 A proposed model of the effect of charging and discharging in nc-Ge on the current conduction of the gate oxide. (a) Conductive paths formed by uncharged nc-Ge; and (b) blocked paths due to charging in nc-Ge.

The charging and discharging in the nc-Ge caused by UV illumination are two competing processes which occur simultaneously. If the charging process is dominant, the oxide conductance is reduced; however, if the discharging process is dominant, the oxide conductance is increased. Both of these two situations have been observed in our experiment. As shown in Fig. 3-32, an UV illumination for 5 seconds leads to a large reduction in the oxide conductance; however, a further UV illumination for 200 seconds results in an increase (a partial recovery) in the conductance as compared to the conductance of the 5-seconds illumination, as shown in Fig. 3-34(a). On the other hand, as shown in Fig. 3-34(b), the oxide conductance can recover almost to the level

of the virgin situation after a low-temperature annealing at 150 ºC for 15 minutes in addition to the UV illumination for 200 seconds. This indicates that almost all the charges trapped in the nc-Ge due to the first UV illumination can be released after the second UV illumination and the low-temperature annealing.

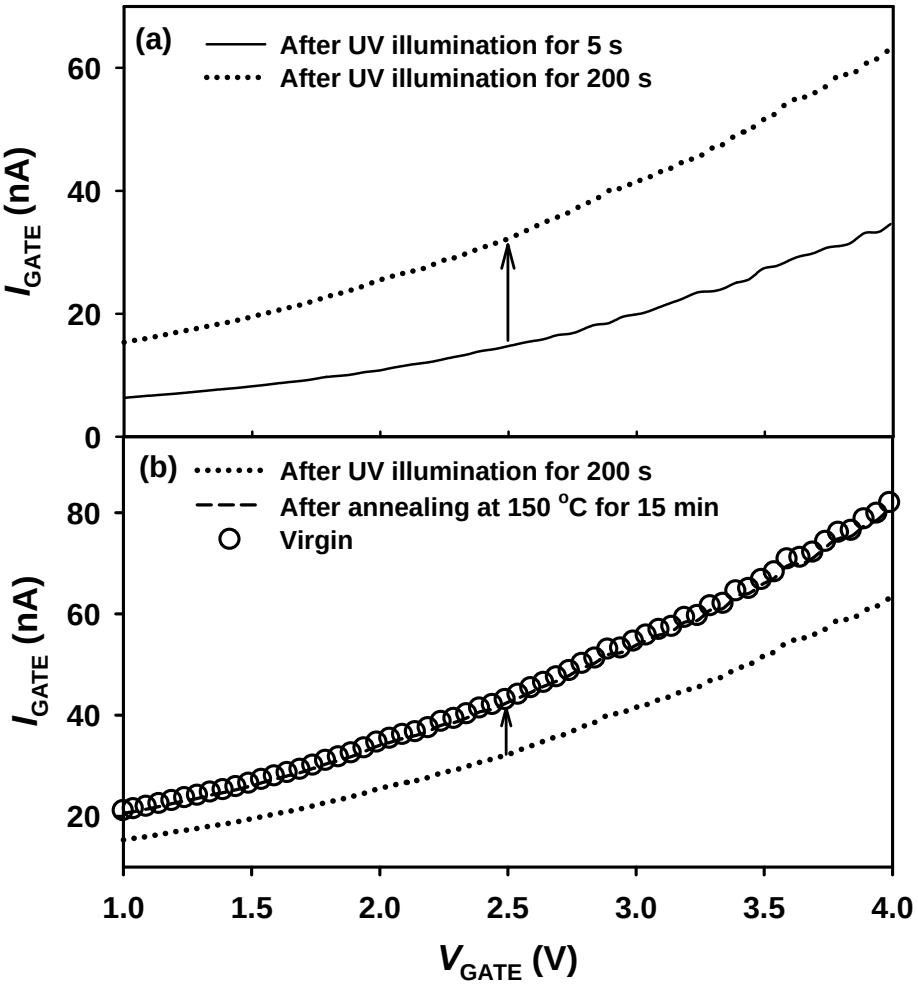

Fig. 3-34 (a) Partial recovery of the gate current after another UV illumination for 200 s from the situation of the UV illumination for 5 s. (b) Full recovery of the gate current after an annealing at 150 ºC for 15 min in addition to the UV illumination for 200 s.

Because the charging and discharging in nc-Ge can occur simultaneously under the UV illumination, the conduction of the SiO_2 embedded with nc-Ge can be modulated by the UV illumination in a time-domain measurement at a constant measurement voltage. This is confirmed by Fig. 3-35, which shows the time-domain DC resistance measured at a gate voltage of 4 V. As can be seen from Fig. 3-35(a), no significant resistance change is observed, indicating that no significant charging and discharging in the nc-Ge occurs during the measurement without UV illumination. However, the DC resistance is modulated under the UV illumination. As can be seen from Fig. 3-35(b), after the first UV illumination for 4 s, the resistance is switched from a low-resistance state (State 1) which corresponds to the situation of no charge trapping in the nc-Ge to a high-resistance state (State 2) as a result of charging in the nc-Ge due to the UV illumination. State 2 is maintained for about 120 s, and then the resistance is switched to a new state (State 3) which has a resistance much lower than that of State 2 but slightly higher than that of State 1. This indicates that not all of the trapped charges associated with State 2 have been released and thus only a partial recovery of the conduction is achieved. After staying at State 3 for about 370 s, the resistance is switched back to State 2 as the charging process is dominant again. If the timescale is extended, the switching between different states, which is a random event, can be observed continuously. However, it is generally observed that for a virgin sample a short UV exposure leads to a switching to a high-resistance state (i.e., the charging process is dominant) while a further exposure could cause a switching back to a low-resistance state (i.e., the discharging process is dominant) depending on the exposure duration.

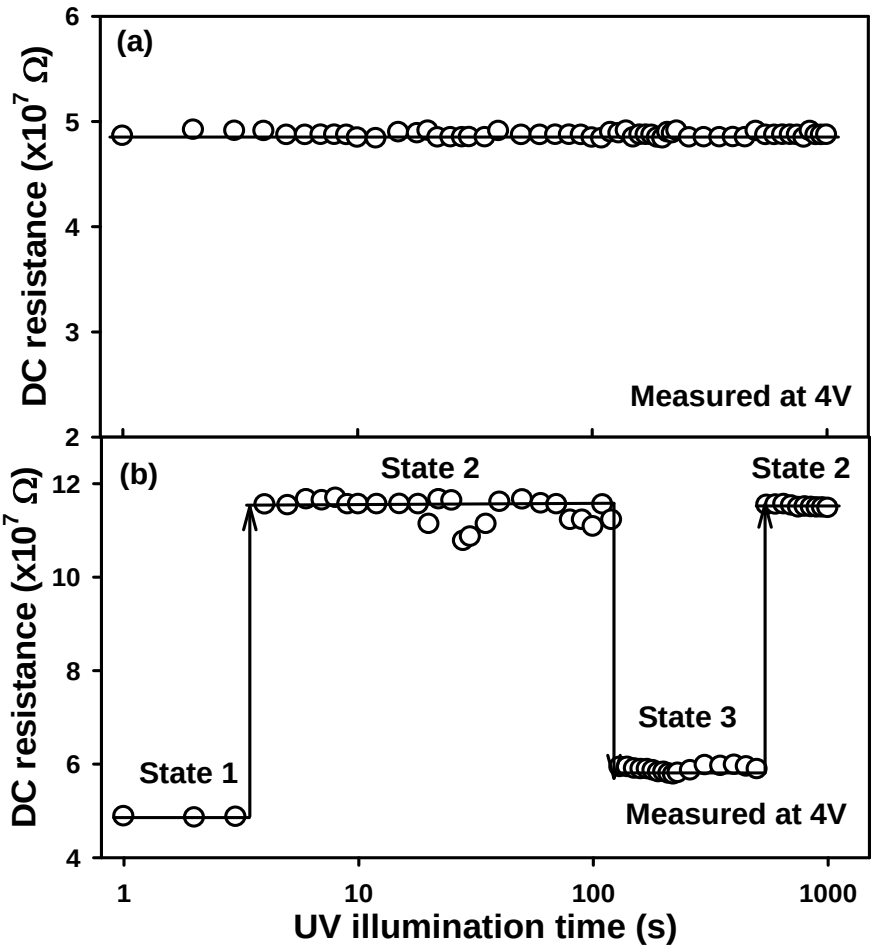

Fig. 3-35 Time-domain measurement of the DC resistance of the oxide: (a) without UV illumination; and (b) with UV illumination. The DC resistance was measured at a gate voltage of 4 V.

The phenomenon that the oxide resistance (or oxide conduction) can be changed by the UV illumination and low-temperature annealing could be used in optoelectronic memory device applications where information can be stored as a high- or low-resistance state. For example, an optoelectronic write-once-read-many-times (WORM) memory could be realized based on this phenomenon. The memory could be

programmed with the UV illumination for a short duration and erased with a low-temperature annealing.

3.7.3 Conclusion

In conclusion, we have observed a new phenomenon of UV-illumination-induced conduction modulation of the SiO_2 thin film embedded with nc-Ge synthesized by the ion implantation technique. The modulation of the oxide conduction is due to the charging and discharging in the nc-Ge caused by UV illumination. The charging and discharging in the nc-Ge are two competing processes which occur simultaneously. If the charging process is dominant, the oxide conductance is reduced; however, if the discharging process is dominant, the oxide conductance is increased. As the conduction can be modulated by UV illumination, it could have potential applications in silicon-based optoelectronic memory devices, such as an optoelectronic WROM device.

3.8 Summary

In this chapter, the current transport behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been investigated. Two different distributions of nc-Ge in the SiO_2 thin films have been prepared: 1) a narrow distribution of nc-Ge near the SiO_2 surface using low implant energy of 2 – 8 keV, and 2) a broad distribution of nc-Ge throughout the SiO_2 using high implant energy of 16 keV. The structural properties of the samples have been characterized by SIMS and TEM techniques. The characteristics of gate current density (J_{GATE}) versus oxide field (E_{OX}) at various

temperatures have been investigated, and the different transport mechanisms dominating in different oxide field regions have been identified. The current transport behavior has been explained by appropriate models. In addition, a conduction modulation effect in SiO_2 thin films embedded with nc-Ge caused by ultra-violet (UV) illumination has been reported. The conduction modulation has been attributed to the charging and discharging in the nc-Ge caused by UV illumination.

Chapter 4 Charge Trapping and Charge Retention in Ge-ion-implanted SiO_2 Thin Films

4.1 Introduction

Nanocrystal-based non-volatile memory structure is the potential candidate to overcome the scaling limit of the conventional floating-gate (FG) based memory devices [20, 55]. By replacing the conventional FG with Ge nanocrystals (nc-Ge) acting as discrete charge storage nodes, King *et al.* have demonstrated the improved memory performance such as fast program/erase speed, long data retention time and good endurance in their memory cell based on nc-Ge [78]. The write operation of the memory device is accomplished by the application of an external electric field, which leads to the charge injection from the Si substrate or the gate electrode into the SiO_2 embedded with nc-Ge. The injected charges are trapped by the conduction band or valence band of the nanocrystal [20, 95], the deep traps within the nanocrystal bandgap [166] or the interfacial traps of the nanocrystals [72]. To retain the memory state, the trapped charges are expected to remain in the charge storage sites for a long time. However, the non-volatility of the memory cell is affected by the loss of trapped charges from nc-Ge, which has been experimentally measured [59, 96, 212, 218]. For the successful operations of non-volatile memory devices based on nc-Ge, a better understanding of the charge trapping and charge retention behavior is necessary.

The SiO_2 thin films embedded with nc-Ge synthesized by Ge ion implantation have been demonstrated to possess memory effect [43, 47, 48]. However, their charge trapping and charge retention behavior has not been systematically studied. The advantage of the Ge ion implantation technique is that the density and depth distribution of the implanted Ge can be precisely controlled by those process parameters such as implant energy, implant dose and annealing temperature. Thus, it is essential to understand the influences of these process parameters on the charge trapping and charge retention behavior. Besides, it is known that the implanted Ge atoms can dissolve and diffuse in the SiO_2 matrix [49], resulting in the presence of Ge atoms in the oxide between adjacent nc-Ge particles as well as in the tunnel oxide separating the nc-Ge and the Si substrate. The roles of these dissolved Ge ions in the charge retention have not been studied.

This chapter presents a systematic study on the charge trapping and charge retention behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge. The samples were fabricated using different implant energies, implant doses and annealing temperatures. In Section 4.3, the dependence of charge trapping on the polarity and magnitude of the charging voltage as well as the charging time is studied based on a typical MOS structure with Ge-ion-implanted SiO_2 thin film. Besides, the charge retention behavior is also presented. Section 4.4 investigates the influence of the annealing temperature on the charge trapping and charge retention behavior. The electrical behavior is correlated to changes in the structural and chemical properties of the nc-Ge embedded SiO_2 caused by the thermal annealing. Section 4.5 studies the influences of implant energy and dose on the charge trapping and charge retention

behavior. In Section 4.6, metal-oxide-semiconductor (MOS) structures with and without a lateral charge transfer channel are described. The charge trapping and charge retention behavior of these two structures is compared. The charge loss as a result of the lateral charge transfer along the nc-Ge distributed region and the charge leakage to the Si substrate is investigated.

4.2 Sample fabrication and experimental details

4.2.1 Sample fabrication

The Ge-ion-implanted SiO_2 thin films with low implant energies of 2 – 8 keV which lead to a narrow layer of nc-Ge distributed near the SiO_2 surface are studied in this chapter. The details of the fabrication procedure have been mentioned previously in Section 3.3.1. Group I samples (see Table 2) were fabricated using the same implant dose but different implant energies, while Group II samples were fabricated using the same implant energy but different implant doses. The samples in Group I and II were annealed in N_2 ambient at 800 ºC for 1 hour. In order to study the effect of annealing temperature on the charge trapping and charge retention behavior, the Ge4-1E16 sample (i.e., sample with an implant energy of 4 keV and a dose of 1×10^{16} cm^{-2}) was also annealed in N_2 ambient for 1 hour at different temperatures ranging from 800 to 1100 ºC. MOS structures based on all the samples were formed by the deposition of Al top electrodes and an Al backside contact using an Edwards electron-beam evaporator.

4.2.2 Characterization techniques

Secondary ion mass spectroscopy (SIMS) and cross-sectional transmission electron microscope (TEM) were used to obtain the structural properties of the Ge-ion-implanted SiO_2 thin films. X-ray photoemission spectroscopy (XPS) using a Kratos AXIS spectrometer with monochromatic Al Kα (1486.71 eV) X-ray radiation was also used to analyze the oxidation states in the nc-Ge distributed region. For the electrical characterization, a Keithley 4200 Semiconductor Characterization System was used for the capacitance-voltage (C-V) measurements. All measurements were performed at room-temperature in the dark.

4.3 Charge trapping and retention in SiO_2 thin film with nc-Ge distributed near the SiO_2 surface

In this section, the charge trapping and charge retention behavior of a typical Ge-ion-implanted SiO_2 thin film with nc-Ge distributed in a narrow layer near the gate is presented.

4.3.1 Device structure

The conventional structure of gate / control oxide / nc-Ge layer / tunnel oxide / Si substrate for the charge trapping study of the nc-Ge was usually formed with the nc-Ge layer located near the Si substrate [218-220]. In the present study, the deposition of the control oxide was eliminated and the above structure was simplified by using a single low-energy (2 – 8 keV) ion implantation into a SiO_2 thin film. In this simplified structure, the nc-Ge is distributed in a narrow layer in the gate oxide near

the gate rather than the substrate, as shown in Fig. 4-1(a). This simplified structure shows a memory effect and exhibits some interesting behavior of charge trapping and charge retention. The sample studied here is a Ge4-1E16 sample, which has an implant energy of 4 keV, a Ge ion dose of 1×10^{16} cm^{-2} and a post-implantation thermal annealing at 800 ºC for 40 minutes. As shown previously from the SIMS result in Fig. 3-6, the implant energy of 4 keV leads to a narrow distribution of implanted Ge ions near the surface of the SiO_2. Fig. 4-1(b) shows the TEM image for the sample with the nc-Ge distributed in the SiO_2 thin film. The inset of Fig. 4-1(b) shows the TEM image of a single nc-Ge with a size of ~ 4 nm. A narrow layer of nc-Ge near the surface of the SiO_2 film can be clearly observed. Based on the TEM image, the width of the nc-Ge layer is about 10.5 nm, the oxide thickness between the nc-Ge layer and the Si substrate is about 25 nm, and the oxide thickness between the surface of the SiO_2 film and the nc-Ge layer is about 4 nm.

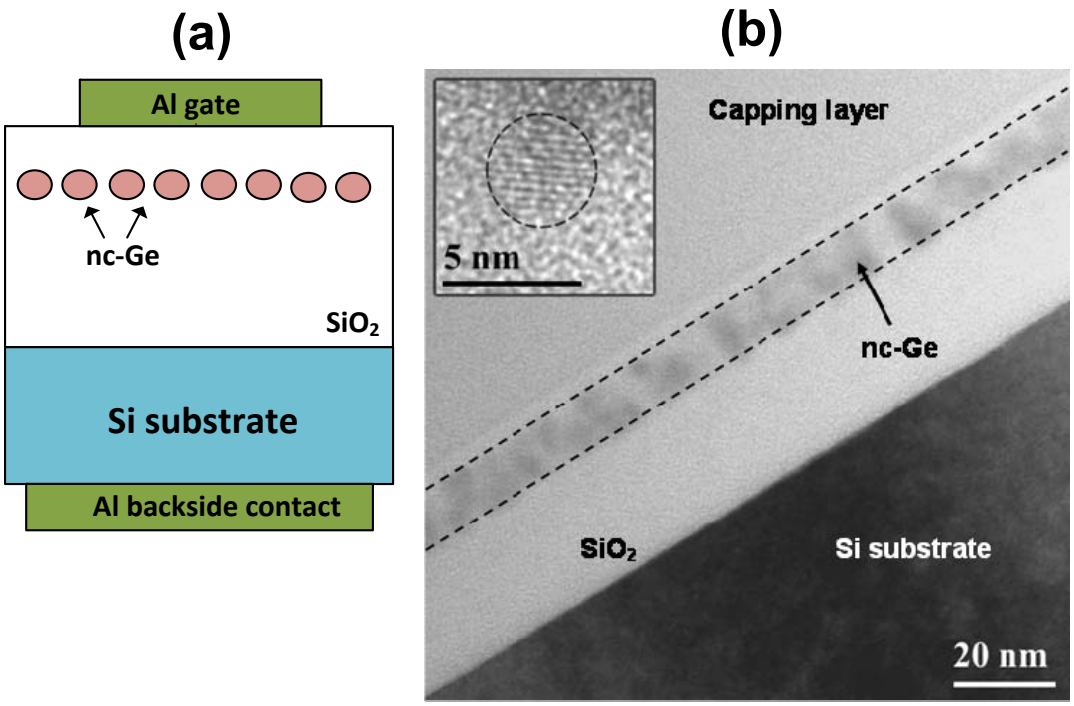

Fig. 4-1 (a) Schematic diagram showing the MOS structure with nc-Ge confined in a narrow layer near Al gate, and (b) Cross-sectional TEM image showing a narrow layer of nc-Ge located in the surface region of the SiO_2. The inset shows the TEM image of a single nc-Ge.

4.3.2 Charge trapping behavior

Shifts in the *C-V* characteristic after the application of a constant charging voltage (V_{CHARGE}) to the gate electrode were used to study the charge trapping behavior of the Ge-ion-implanted SiO_2 thin film. Fig. 4-2 shows typical *C-V* shifts for charging by +25 V and –25 V for 1 s. A clear flat-band voltage shift (ΔV_{FB}) with respect to the initial *C-V* curve indicates the memory effect of the device structure. It is interesting to notice that both V_{CHARGE} (i.e., +25 V and –25 V) cause a shift in the

flat-band voltage towards the positive side, suggesting that both of them lead to a build-up of negative charges in the thin film structure.

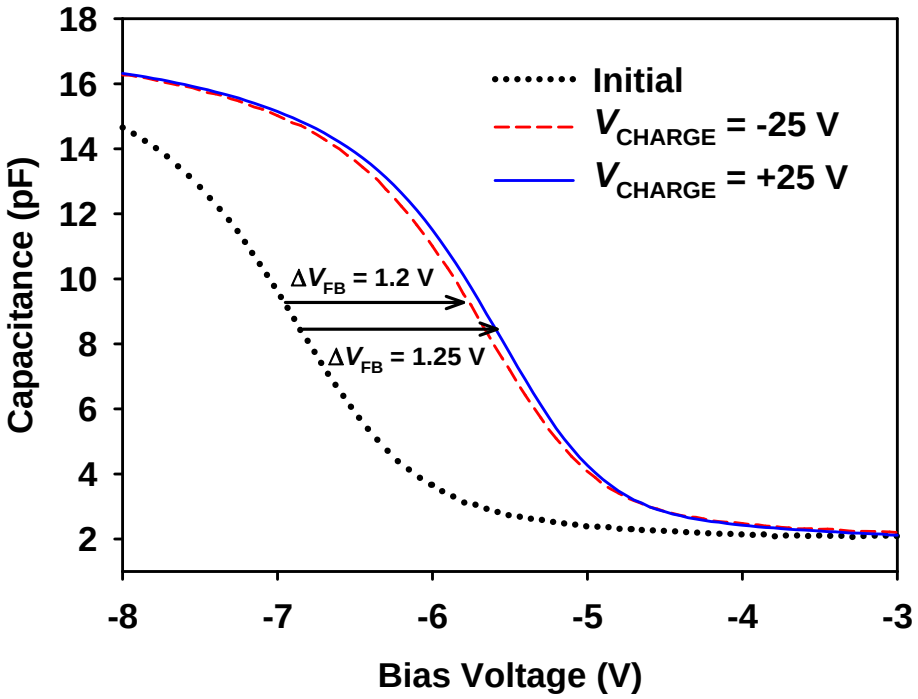

Fig. 4-2 Shifts in the high-frequency (1 MHz) *C-V* characteristics after the charging at V_{CHARGE} = +25 V or –25 V for 1 s.

Since no ΔV_{FB} can be observed for the control sample without the nc-Ge, the positive shift in the flat-band voltage is attributed to the trapping of electrons in the nc-Ge distributed in the SiO_2 film. The ΔV_{FB} can be related to the density of charges trapped in the nc-Ge by [20]

$$\Delta V_{FB} = -\frac{Q_{nc-Ge}}{\varepsilon_{SiO_2}}\left(t_C + \frac{1}{2}\frac{\varepsilon_{SiO_2}}{\varepsilon_{Ge}} d_{nc-Ge}\right) \quad (4.1)$$

where Q_{nc-Ge} is the density of the charges trapped in the nc-Ge, ε_{SiO_2} and ε_{Ge} represent the permittivity of the SiO_2 and Ge respectively, t_C is the oxide thickness

between the gate electrode and the nc-Ge layer, and $d_{\mathrm{nc-Ge}}$ is the dimension of the nc-Ge. Note that the negative sign in Eq. (4.1) accounts for the fact that the trapping of negative charges in the nc-Ge leads to a positive ΔV_{FB}. As examples, the $Q_{\mathrm{nc-Ge}}$ estimated with Eq. (4.1) is -9.62×10^{-7} and -9.23×10^{-7} C/cm^2 for V_{CHARGE} = +25 and –25 V, respectively.

4.3.3 Influence of polarity and magnitude of charging voltage

To study the influence of both the polarity and magnitude of the charging voltage on the charge trapping in the nc-Ge, $Q_{\mathrm{nc-Ge}}$ was measured for both positive and negative V_{CHARGE} with a magnitude varying from 7 to 30 V at a fixed charging time of 1 s. The results are shown in Fig. 4-3. It is evident from Fig. 4-3 that the charging behavior for positive V_{CHARGE} is different to that for negative V_{CHARGE}. As shown in the figure, a positive V_{CHARGE} always results in a negative $Q_{\mathrm{nc-Ge}}$ regardless of the voltage magnitude. In contrast, a negative V_{CHARGE} leads to either a positive or a negative $Q_{\mathrm{nc-Ge}}$ depending on the magnitude of the voltage. In the case of positive V_{CHARGE}, for V_{CHARGE} less than +21 V, the $Q_{\mathrm{nc-Ge}}$ remains at a small negative value with a magnitude less than 1×10^{-7} C/cm^2, indicating that only a small amount of electrons are trapped in the nc-Ge. However, when the V_{CHARGE} goes beyond +21 V, the $Q_{\mathrm{nc-Ge}}$ is still negative, but its magnitude increases rapidly (for example, $Q_{\mathrm{nc-Ge}}$= -27×10^{-7} C/cm^2 for V_{CHARGE} = +30 V) and is approximately a linear function of the V_{CHARGE}. As discussed later, the rapid increase in the magnitude of $Q_{\mathrm{nc-Ge}}$ is due to the strong electron injection from the Si substrate under the influence of a large positive gate voltage. On the other hand, in the case of negative V_{CHARGE}, the $Q_{\mathrm{nc-Ge}}$ is positive when the magnitude of V_{CHARGE} is less than 19 V, and the maximum

$Q_{\mathrm{nc-Ge}}$ (3.2×10^{-7} C/cm^2) occurs at V_{CHARGE} = –16 V. When the magnitude of V_{CHARGE} is larger than 19 V, the $Q_{\mathrm{nc-Ge}}$ becomes negative and its magnitude rapidly increases as the magnitude of the V_{CHARGE} further increases. It is obvious that in the case of negative V_{CHARGE} both hole trapping and electron trapping in the nc-Ge occur. As discussed in the following section, under a negative V_{CHARGE}, the hole trapping and electron trapping are two competing processes, and the magnitude of the V_{CHARGE} determines which one is dominant. This behavior is different from the situation of a conventional memory structure where the nc-Ge layer is located near the Si substrate [43]. In a conventional structure, the electron trapping caused by a negative V_{CHARGE} is insignificant because the thick control oxide prevents the electron injection from the gate.

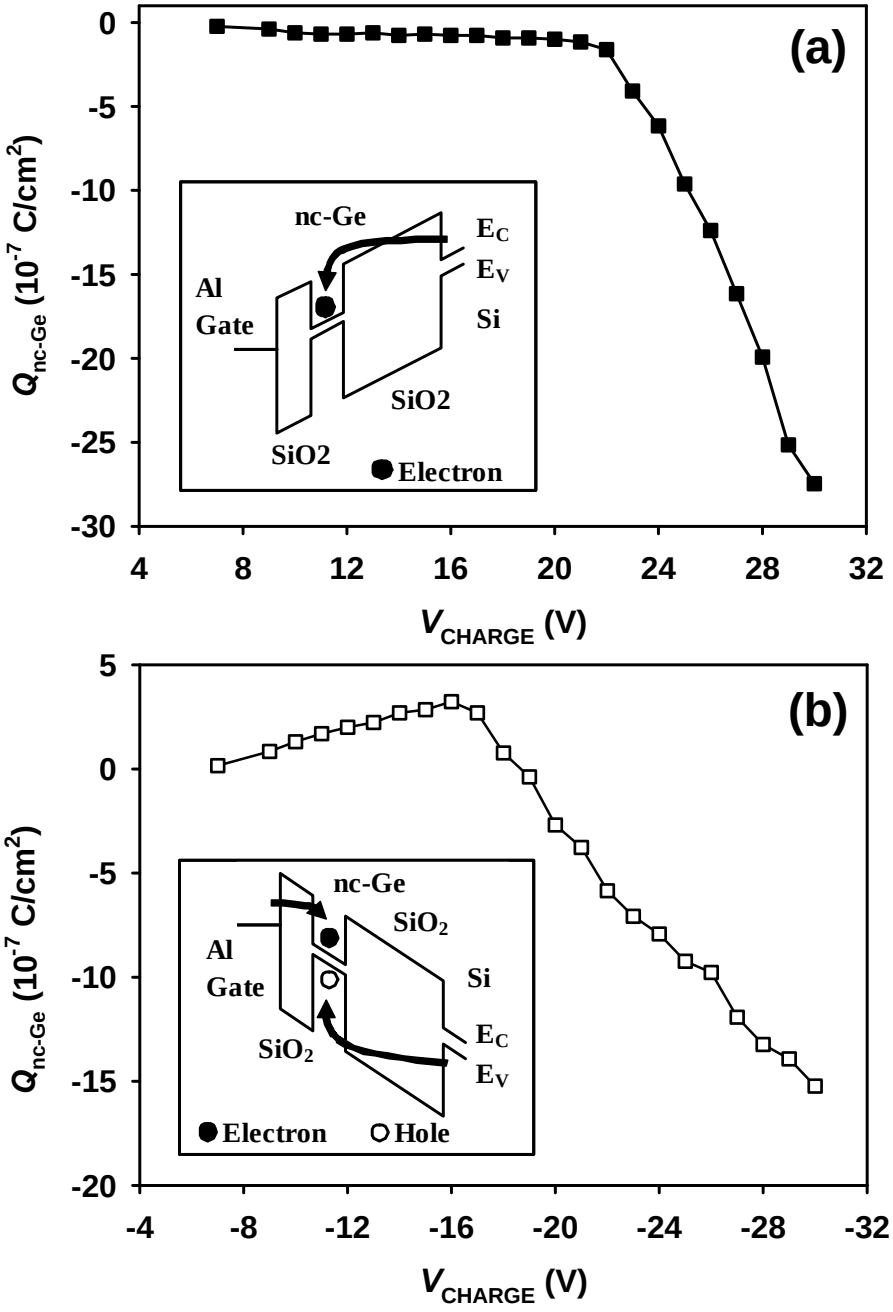

Fig. 4-3 Density ($Q_{nc\text{-}Ge}$) of trapped charges as a function of the charging voltage (V_{CHARGE}): (a) positive charging voltage; and (b) negative charging voltage. The charging time is fixed at 1 s. The insets show the charging mechanisms under a positive or negative V_{CHARGE}.

The results shown in Fig. 4-3 can be explained as follows. As shown in the inset of Fig. 4-3(a), under the influence of a positive V_{CHARGE}, electrons are injected from the Si substrate and trapped in the nc-Ge. When the magnitude of V_{CHARGE} is larger than 21 V, the electric field in the oxide between the Si substrate and the nc-Ge layer is high enough to cause FN tunneling across the oxide. Therefore, the electron injection is drastically enhanced, resulting in a rapid increase in the electron trapping in the nc-Ge.

On the other hand, as shown in the inset of Fig. 4-3(b), under the influence of a negative V_{CHARGE}, the injection of the holes from the Si substrate and the injection of electrons from the gate occur simultaneously, leading to the trapping of both holes and electrons in the nc-Ge. In this case, the density of the net trapped charges in the nc-Ge is given by

$$Q_{\mathrm{nc-Ge}} = Q_{\mathrm{hole}} - Q_{\mathrm{electron}} \tag{4.2}$$

where the Q_{hole} and Q_{electron} are the trapped-hole density and trapped-electron density, respectively. The behavior shown in Fig. 4-3(b) is a consequence of the competition between these two charging processes. Obviously, $Q_{\mathrm{nc-Ge}}$ is positive if hole trapping dominates, and it is negative if electron trapping dominates. Fig. 4-3(b) indicates that in the case of a negative V_{CHARGE}, when its magnitude is less than 18 V, hole trapping is dominant, but the electron trapping increases rapidly when the magnitude of V_{CHARGE} is larger than 16 V. The rapid increase in electron trapping is due to the occurrence of electron tunneling from the gate electrode. When the magnitude of the negative V_{CHARGE} is larger than 18 V, the electron tunneling from the

gate surpasses the hole injection from the substrate, leading to a net negative charge trapping in the nc-Ge. This situation is in contrast to that of a conventional memory device where the nc-Ge is located near the substrate. For a conventional memory device, a negative V_{CHARGE} is usually used during the erasing process to expel the trapped electrons from the nc-Ge, and the negative V_{CHARGE} itself does not cause the electron trapping in the nc-Ge because of the thick control oxide which can effectively suppress the electron tunneling from the gate (note that only the trapping of positive charges in the nc-Ge is observable in the case of over-erasing).

4.3.4 Influence of charging time

Further investigation of the charge trapping behavior was carried out by varying the charging time from 5 μs to 5 s for a given V_{CHARGE}. The results are consistent with the above-mentioned charging behavior. As shown in Fig. 4-4, Q_{nc-Ge} is always negative regardless of the charging time for a positive V_{CHARGE}. This is because only electron injection from the substrate occurs under a positive V_{CHARGE}. It can be observed in Fig. 4-4 that for V_{CHARGE} = +25 V the electron trapping in the nc-Ge starts to increase rapidly when the charging time is longer than 1 ms. This starting time is prolonged when the V_{CHARGE} is reduced. Obviously, this is related to the V_{CHARGE} dependence of the electron injection from the substrate. For V_{CHARGE} = 20 V, a relatively long charging time (~ 1 s) is required to achieve a significant amount of electron trapping. However, for larger V_{CHARGE} (e.g., 23 and 25 V), the charging time required to achieve a significant amount of electron trapping is reduced.

It should be noted that in Fig. 4-4, no saturation of $Q_{\mathrm{nc-Ge}}$ occurs for a longer charging time. The saturation phenomenon is also absent in Fig. 4-3(a) which shows the dependence of $Q_{\mathrm{nc-Ge}}$ on positive V_{CHARGE} for a fixed charging time of 1 s. The results indicate that the nanocrystals embedded in SiO_2 are not fully charged up by the injected electrons within the given charging time. For the case of a positive V_{CHARGE}, a larger magnitude of V_{CHARGE} or a longer charging time results in more electrons trapping in the nc-Ge.

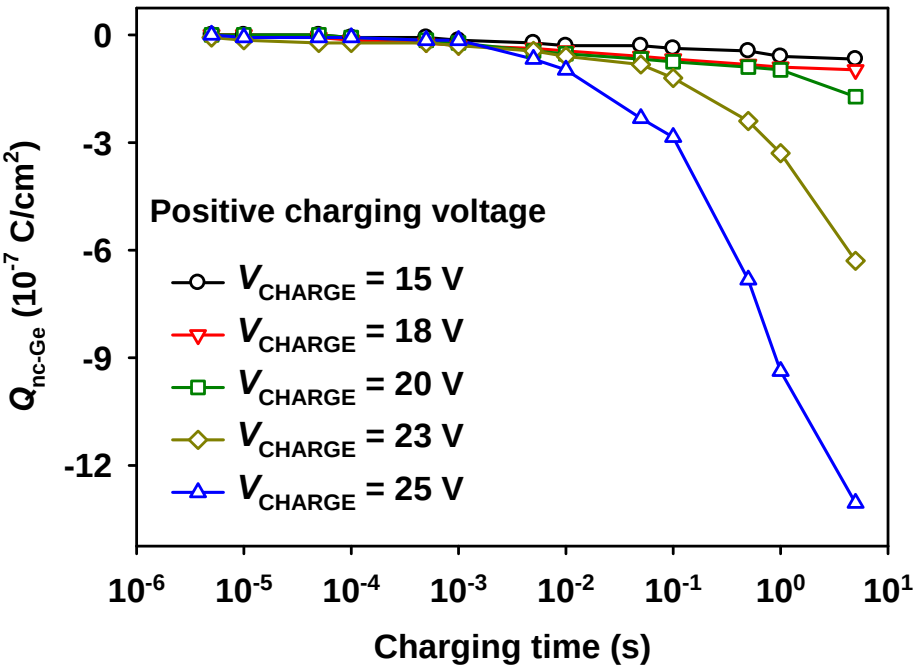

Fig. 4-4 Density ($Q_{\mathrm{nc\text{-}Ge}}$) of trapped charges as a function of the charging time for different positive V_{CHARGE}.

On the other hand, as shown in Fig. 4-5, for charging by a negative V_{CHARGE}, both positive and negative $Q_{\mathrm{nc-Ge}}$ could be observed depending on the magnitude of the V_{CHARGE} and the charging time. As discussed earlier, under a negative V_{CHARGE}, the

two competing processes (i.e., the hole injection from the substrate and the electron injection from the gate) occur simultaneously. For V_{CHARGE} = –15 and –18 V, Q_{nc-Ge} is positive (i.e., hole trapping is dominant) and increases gently with the charging time. The increase of Q_{nc-Ge} with charging time for V_{CHARGE} = –15 V is even faster than that for V_{CHARGE} = –18 V. This is because the electron injection under V_{CHARGE} = –15 V is less significant. For V_{CHARGE} = –20 V, a small amount of positive charge trapping could be observed for a charging time shorter than 1 ms, but electron trapping becomes dominant when the charging time is longer than 1 ms. For V_{CHARGE} = –23 V and –25 V, electron trapping is dominant, and the amount of Q_{nc-Ge} increases with charging time when the charging time is shorter than 1 s.

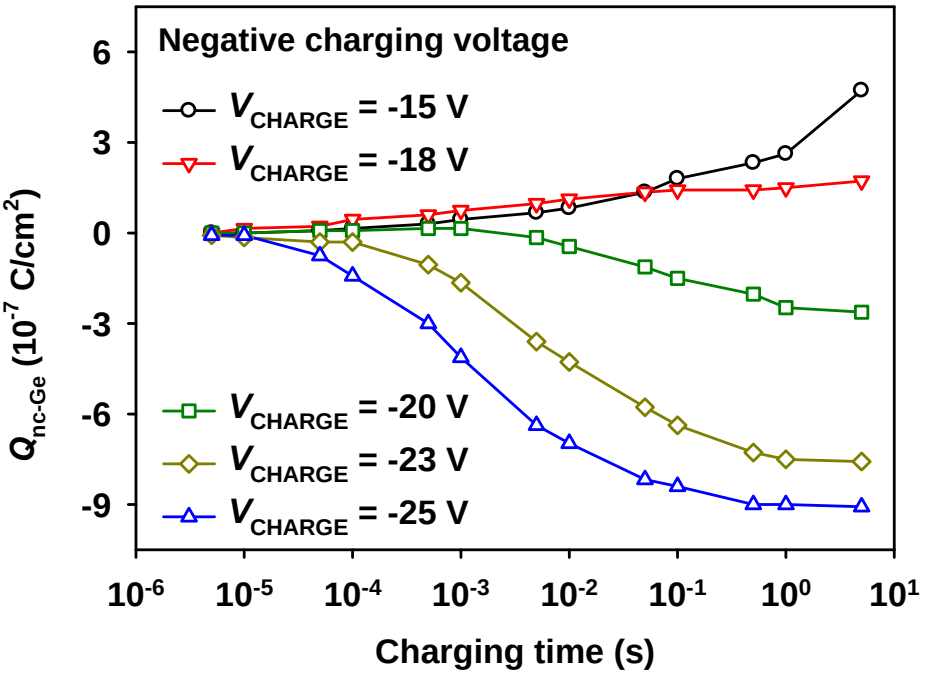

Fig. 4-5 Density (Q_{nc-Ge}) of trapped charges as a function of the charging time for different negative V_{CHARGE}.

In Fig. 4-5, it is shown that the amount of $Q_{\mathrm{nc-Ge}}$ for V_{CHARGE} < –20 V is saturated when the charging time is longer than 1 s. Under negative V_{CHARGE}, both electrons and holes are injected into the nc-Ge. Based on Eq. (4.2), the net charge injection rate is given by

$$\frac{dQ_{\mathrm{nc-Ge}}}{dt} = \frac{dQ_{\mathrm{hole}}}{dt} - \frac{dQ_{\mathrm{electron}}}{dt} \tag{4.3}$$

From Eq. (4.3), it can be known that the saturation in $Q_{\mathrm{nc-Ge}}$, i.e., $dQ_{\mathrm{nc-Ge}}/dt = 0$, could be due to two reasons: (1) the nanocrystals are fully charged up, or (2) the electron injection rate equals to the hole injection rate. In Fig. 4-3, the $Q_{\mathrm{nc-Ge}}$ under a negative V_{CHARGE} can reach up to -15×10^{-7} C/cm^2 without any saturation. Thus, the situation that all nanocrystals are fully charged up can be ruled out. The saturation phenomenon is explained as follows. For a short charging time, the electron injection rate is larger than the hole injection rate because the nc-Ge are close to the gate electrode. However, for a long charging time, more electrons are trapped in nc-Ge, and the electron injection rate is reduced due to the strong Coulomb interaction between the trapped electrons in the nc-Ge and the negatively biased gate electrode. Thus, the saturation in $Q_{\mathrm{nc-Ge}}$ occurs for a long charging time when the electron injection rate equals to the hole injection rate. The maximum saturated $Q_{\mathrm{nc-Ge}}$ shown in Fig. 4-5 is -9×10^{-7} C/cm^2. This amount does not represent the maximum capacity of charge trapping in nc-Ge. The saturation in$Q_{\mathrm{nc-Ge}}$ is not observed in Fig. 4-4(b) which shows the dependence of $Q_{\mathrm{nc-Ge}}$ on negative V_{CHARGE} for a fixed charging time of 1 s. Since both electron injection rate and hole injection rate increase when the magnitude of V_{CHARGE} increases, the saturation condition is not satisfied.

4.3.5 Charge retention behavior

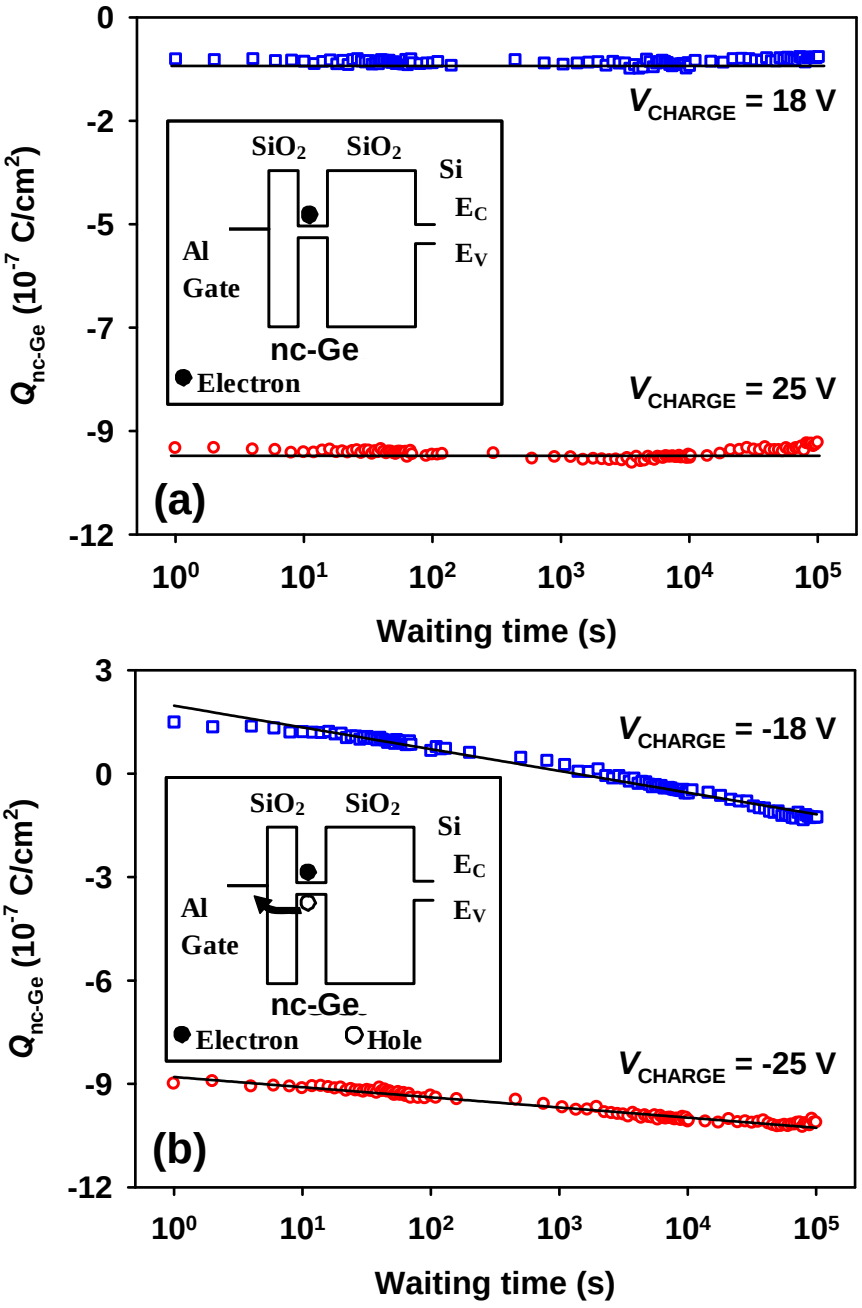

Fig. 4-6 Charge retention characteristics for positive charging voltages (a) and negative charging voltages (b). The charging time is fixed at 1 s. The insets show the energy band diagrams during the retention experiment.

The charge retention experiment was carried out for both positive V_{CHARGE} [Fig. 4-6 (a)] and negative V_{CHARGE} [Fig. 4-6(b)] with a fixed charging time of 1 s. For charging under a positive V_{CHARGE}, as discussed above, only electrons are trapped in the nc-Ge, and thus the Q_{nc-Ge} behavior in the charge retention experiment is simple, i.e., Q_{nc-Ge} remains negative and a decrease in its magnitude could be observed. As can be seen in Fig. 4-6(a), for both the charging voltages of +18 and +25 V, Q_{nc-Ge} remains unchanged for a waiting time up to 10^4 s, and then only a slight loss of the trapped electrons is observed. The result indicates that the two oxide layers sandwiching the nc-Ge layer as shown in the inset of Fig. 4-6(a) have a good capability to prevent the release of the trapped electrons. However, the charge retention behavior for a negative charging voltage is quite different. As shown in Fig. 4-6(b), for V_{CHARGE} = –18 V, the Q_{nc-Ge} is positive when the waiting time is shorter than 10^3 s, but later it becomes negative and shifts continuously towards a more negative value (i.e., its magnitude increases) with waiting time. For V_{CHARGE} = –25 V, the Q_{nc-Ge} is always negative regardless of the waiting time, and it also shifts continuously towards a more negative value with waiting time. However, the rate of the change in Q_{nc-Ge} for V_{CHARGE} = –25 V is lower than that for V_{CHARGE} = –18 V. As discussed earlier, both electrons and holes are trapped in the nc-Ge under a negative charging voltage. However, the above results indicate that the loss of the trapped holes is much faster than that of the trapped electrons. Therefore, with the faster loss of the trapped holes, Q_{nc-Ge} can change from positive to negative as observed in the case of charging by V_{CHARGE} = –18 V, and it shifts continuously toward a more negative value with time. As the hole trapping for V_{CHARGE} = –18 V is more significant than that for

V_{CHARGE} = –25 V, the rate of the change in Q_{nc-Ge} for V_{CHARGE} = –18 V is larger than that for V_{CHARGE} = –25 V as mentioned above. The faster loss of the trapped holes could be due to the fact that the trapped holes can easily recombine with the electrons moving from the Al gate electrode.

4.3.6 Conclusion

In this section, the charge trapping and charge retention behavior of the Ge-ion-implanted SiO_2 thin film containing a narrow layer of nc-Ge distributed in the gate oxide near the gate has been investigated. For a positive V_{CHARGE}, only electron trapping occurs, which is due to the electron injection from the p-type substrate. The electron trapping depends strongly on the magnitude of V_{CHARGE} and the charging time. It increases rapidly with V_{CHARGE} when the FN tunneling across the oxide between the nc-Ge layer and the substrate occurs. However, for a negative V_{CHARGE}, both the hole trapping due to the hole injection from the substrate and the electron trapping due to the electron injection from the gate occur, and these two competing mechanisms determine whether the net charge trapping in the nc-Ge is positive or negative. Hole trapping could be dominant if the magnitude of V_{CHARGE} is small and the charging time is short, and electron trapping becomes dominant when the magnitude of V_{CHARGE} is large and the charging time is sufficiently long. For a positive V_{CHARGE}, the electron trapping shows good retention. In contrast, for a negative V_{CHARGE}, due to the easier loss of the trapped holes, the net charge trapping in the nc-Ge shows a continuous shift towards a more negative value with waiting time, and the shift strongly depends on the magnitude of V_{CHARGE} and the charging time.

4.4 Influence of annealing temperature on charge trapping and charge retention behavior

The thermal annealing is a critical step in the synthesis of nc-Ge embedded in the SiO_2 thin films using the Ge ion implantation technique. It has been reported that a post-implantation thermal annealing can eliminate the implantation-induced damages in the SiO_2 film [221] and remove the positive charges trapped in the oxide caused by the ion implantation as well [204]. Since implanted Ge atoms can dissolve and diffuse in the SiO_2 matrix [49], thermal annealing can also cause the redistribution of Ge atoms in the oxide, which could affect the electrical properties. In this section, the influence of the thermal annealing on the charge trapping and charge retention behavior is investigated. The structural and chemical properties of the nc-Ge embedded in SiO_2 thin films synthesized by different conditions are studied by the SIMS, TEM and XPS techniques, and the results are correlated to the electrical behavior deduced from the *C-V* measurements.

4.4.1 Influence of annealing temperature on structural properties of Ge-ion-implanted SiO_2

The structural properties of the Ge-ion-implanted SiO_2 thin films with identical implant conditions (i.e., a constant implant energy of 4 keV with a constant dose of 1×10^{16} cm^{-2}) but different annealing temperatures were analyzed by SIMS and TEM techniques. The SIMS profile of Ge atoms in the as-implant SiO_2 thin film approximately follows a Gaussian distribution with a full-width-at-half-maximum (FWHM) of ~ 8.8 nm and a concentration peak located at ~ 5.8 nm underneath the

SiO_2 surface. After thermal annealing, the SIMS profiles still show a Gaussian-like shape, but the distributions are broadened. The FWHMs and the peak locations obtained from the Gaussian curve fitting of the as-implanted and annealed samples are shown in Fig. 4-7.

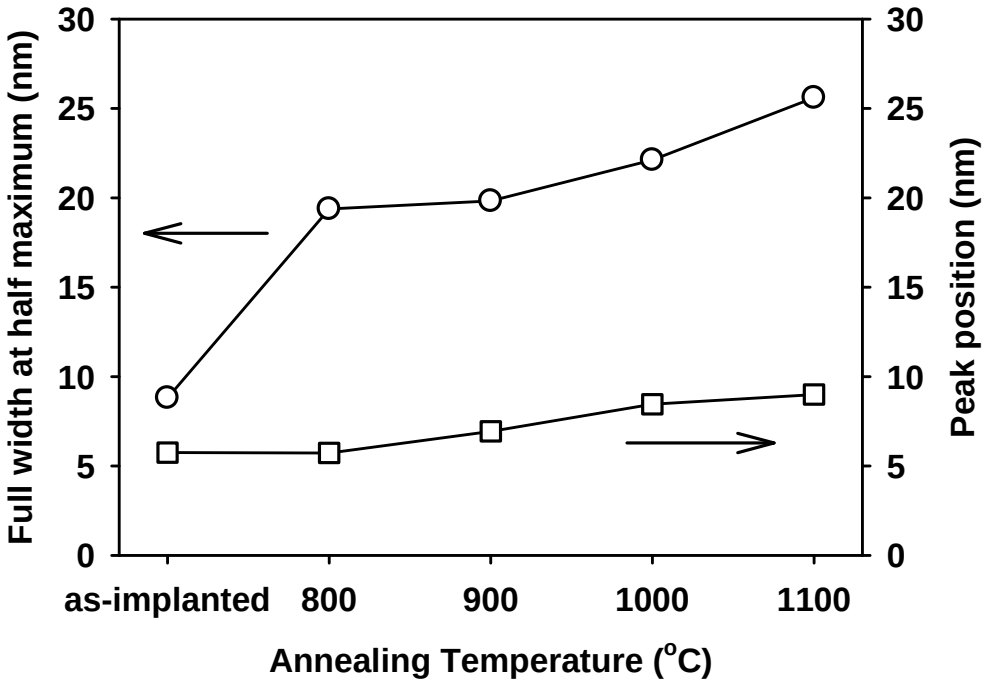

Fig. 4-7 FWHMs and peak locations of the Ge distributions in the SiO_2 thin films as functions of annealing temperature obtained from the Gaussian fittings to the SIMS depth profiles.

As shown in Fig. 4-7, the peak locations for these samples are within the range of 6 to 10 nm and exhibit only a slight increase as the annealing temperature increases from 800 °C to 1100 °C. On the other hand, a more significant increase in the FWHMs of the Ge profiles can be observed as the annealing temperature increases. The FWHMs (e.g., 25.6 nm for the 1100 °C annealing) for the annealed samples are much larger than the FWHM (8.8 nm) for the as-implanted sample. The broadening of

the Ge distributions clearly shows the diffusion of Ge ions in the SiO_2 thin films as a result of annealing.

Based on the Gaussian-like distribution of Ge atoms in SiO_2, the SiO_2 thin film can be virtually divided into two regions, i.e., the region with a high Ge concentration near the SiO_2 surface and a region with a low Ge concentration near the Si substrate. A high temperature annealing results in the crystallization of Ge in the SiO_2 region with a high Ge concentration. Besides, a small amount of elemental Ge can dissolve in the SiO_2 [222], and these dissolved Ge atoms in SiO_2 behave as free diffusing monomers with high mobility [34]. During the high temperature annealing, these Ge monomers have the tendency to diffuse along the concentration gradient. As a result, the Ge monomers tend to diffuse toward the Si substrate, resulting in the region with a low Ge concentration. Obviously, the diffusion of Ge monomers is enhanced with annealing temperature. This explains the broadening of the FWHM and the increase of the Ge concentration near the Si substrate with annealing temperature. Note that in the region with high Ge concentration, the free diffusing Ge monomers can also exist between adjacent nc-Ge. The abovementioned two-region structure agrees with the high-resolution TEM observations. Fig. 4-8 shows the typical TEM images for the samples annealed at 800 °C and 1000 °C, respectively. As shown in Fig. 4-8(a), the formation of nc-Ge with crystalline features can be observed near the SiO_2 surface for the case of 800 °C annealing. The inset of Fig. 4-8(a) shows one crystalline nc-Ge with clear lattice fringes for the sample annealed at 800 °C. The size of the nc-Ge is less than 5 nm. On the other hand, as observed in Fig. 4-8(b), the sample annealed at 1000 °C do not show clear lattice fringes in the nanoclusters near the SiO_2 surface.

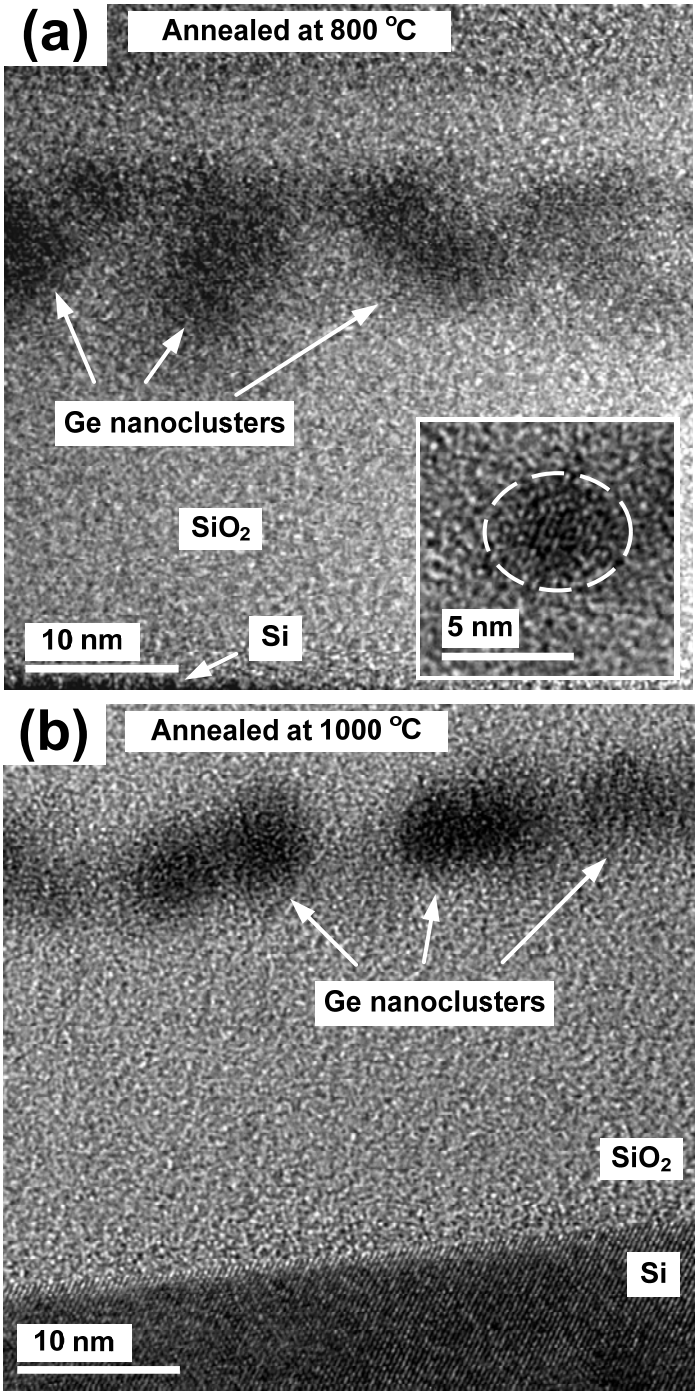

Fig. 4-8 Cross-sectional TEM images for the samples annealed at (a) 800 °C and (b) 1000 °C, respectively.

4.4.2 Influence of annealing temperature on the local chemical properties of Ge-ion-implanted SiO_2

Fig. 4-9(a) shows the typical Ge *3d* XPS spectra taken at a depth of 8 nm (note that the Ge concentration peak is located at this depth) underneath the SiO_2 surface for the as-implanted and annealed samples. The charging effect induced by the photoemission was corrected using the C *1s* reference (284.5 eV) [121]. A dominant peak corresponding to the elemental Ge (29.3 eV) can be observed. Besides, the hump at a higher binding energy (~ 31 – 34 eV) indicates the existence of oxidized Ge which has a higher binding energy than the elemental Ge [223]. The XPS spectra for all the samples with different annealing temperatures indicate that the percentages of elemental Ge and oxidized Ge change with annealing temperature. Gaussian peak deconvolution was performed for all the XPS spectra. Five oxidation states (Ge^{n+}, n = 0, 1, 2, 3, and 4) can be found in the oxidized Ge, and the energy shifts for Ge^{1+}, Ge^{2+}, Ge^{3+} and Ge^{4+} with respect to the elemental Ge (i.e., Ge^{0}) peak are 0.8 eV, 1.8 eV, 2.6 eV and 3.4 eV, respectively [223]. While the elemental Ge and Ge^{4+} (i.e., the stoichiometric GeO_2) peaks can be clearly identified, the other Ge oxidation states (i.e., the Ge sub-oxides, or GeO_x where $x < 2$) are not well resolved and therefore they are considered as the third Gaussian peak. The FWHM for each peak and the binding energy for the Ge sub-oxide peak were not fixed in the fitting. As an example, Fig. 4-9(a) shows the typical Gaussian peak deconvolution of the Ge *3d* core level for the sample annealed at 800 °C. The spectral fittings based on the Gaussian peak deconvolution for all the annealing temperatures are shown in Fig. 4-9(a).

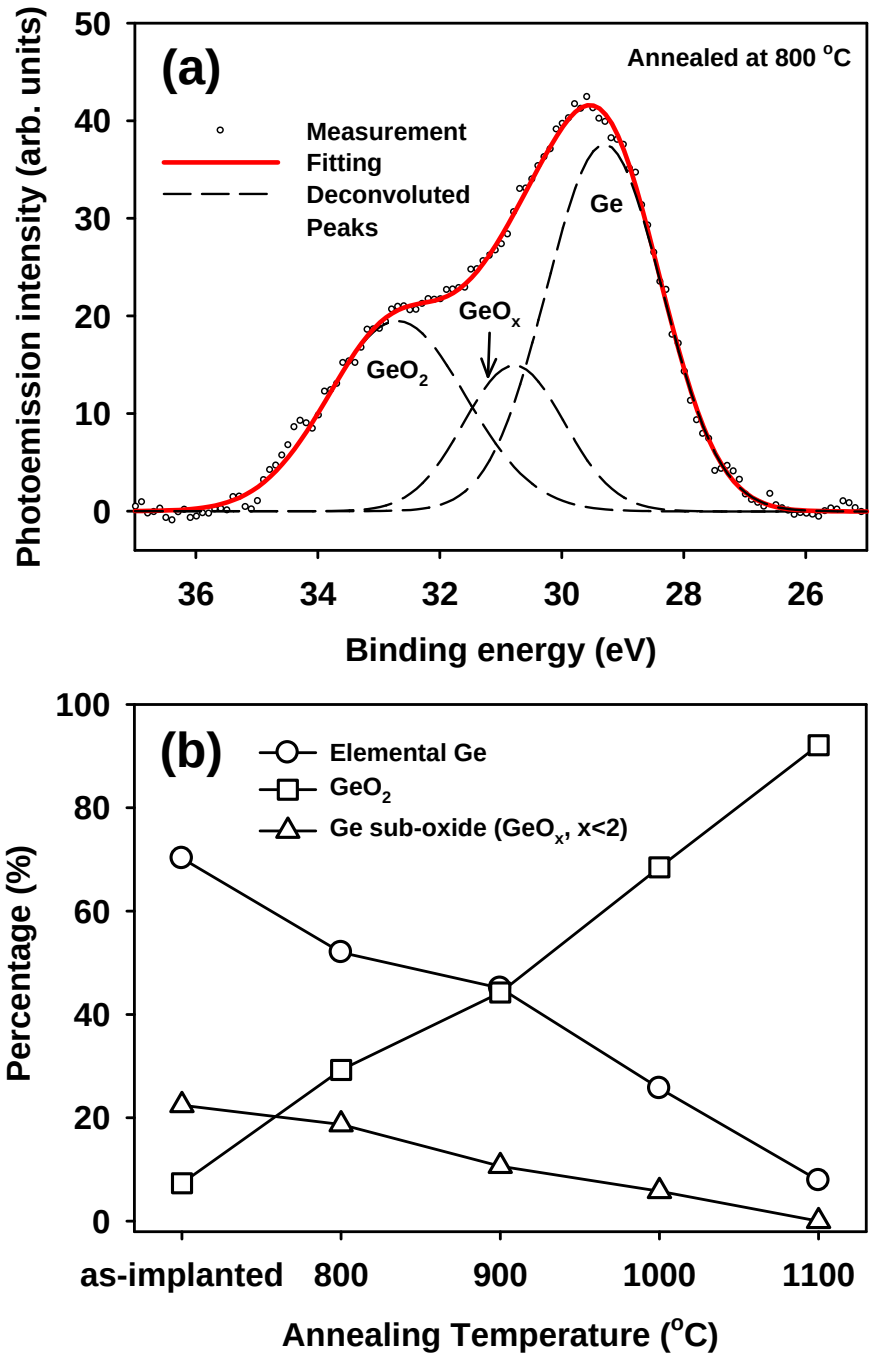

Fig. 4-9 (a) Typical peak deconvolution of the Ge *3d* core level for the sample annealed at 800 °C; (b) Atomic percentages of elemental Ge, stoichiometric Ge oxide (GeO_2) and Ge sub-oxides (GeO_x, x<2) as functions of annealing temperature.

With the fitting procedures, the atomic percentages of the elemental Ge, GeO_2 and Ge sub-oxides can be calculated based on the ratios of the area of each peak to that of the overall spectrum. Fig. 4-9(b) shows the evolution of the atomic percentages with annealing temperature. For the as-implanted sample, almost 30% of the Ge atoms are in the oxidized state; among the oxidized specie, most of them are sub-oxides while only ~ 7% is GeO_2. The percentage of elemental Ge decreases as the annealing temperature increases, indicating that more Ge atoms are oxidized at a higher temperature. On the other hand, the percentage of GeO_2 increases while the percentage of Ge sub-oxides decreases. A high degree of oxidation is observed for the sample annealed at 1100 °C, where ~ 92% of the implanted Ge atoms are converted to stoichiometric GeO_2 and the Ge sub-oxides are almost eliminated. The TEM observation is consistent with the XPS results. For annealing at 800 ^{o}C, more elemental Ge exists, and thus the TEM image as shown in Fig. 4-8(a) shows clear lattice fringes in the nc-Ge; however, for annealing at 1000 ^{o}C, as most of the Ge are oxidized, the TEM image shown in Fig. 4-8(b) does not show clear lattice fringes.

The oxidation of Ge in the annealed samples can be explained as follows. In the study by Arai *et al*. [41], the oxidation phenomenon in their multiple-implanted samples by high energies (10 – 50 keV) was attributed to the local excess oxygen atoms caused by collision of Ge atoms and recoil of oxygen atoms in the SiO_2 matrix during the implantation. The location of the excess oxygen can be predicted by Stopping and Range of Ions in Matter (SRIM) simulation, and the result indicates that the distribution of oxygen recoil is near the surface along the trajectory of the implanted Ge ions [41]. This mechanism can also explain the oxidation behavior

observed in the present study. The oxygen impurity in the annealing ambient should not be the major contributor because there is no obvious increase of oxide thickness when the bare Si wafer was annealed together with the samples used in this study. During the high-temperature annealing, the precipitation and nucleation of nc-Ge happens. At the same time, the local excess oxygen atoms near the nc-Ge could diffuse into the nanocrystals and oxidize the Ge. When the annealing process is completely stopped, some nanocrystals could be completely oxidized (becomes oxidized Ge nanoclusters) while the others could be partially oxidized due to the difference in size and location of these nanocrystals. Such partially oxidized Ge nanoclusters become a mixture of elemental Ge, stoichiometric Ge oxide and Ge sub-oxides.

The proposed mechanism for the oxidation of Ge in the annealed samples can be supported by the XPS analysis of the hosting SiO_2 matrix. During the measurement of the Ge *3d* core level at a depth of ~ 8 nm underneath the SiO_2 surface, the Si *2p* and O *1s* core levels were also measured. The procedures for the correction of charging effect and the Gaussian peak deconvolution are similar to the case of Ge *3d* core level. Fig. 4-10(a) shows the typical Si *2p* core level for the sample annealed at 800 ºC. It is known that the implanted SiO_2 contains five oxidation states (Si^{n+}, n = 0, 1, 2, 3, and 4) [121, 224]. As shown in the figure, the stoichiometric SiO_2 (i.e., Si^{4+}) is dominant. Besides, Si sub-oxides (i.e., Si^{1+}, Si^{2+}, and Si^{3+}) and a small amount of elemental Si can be found. As shown in Fig. 4-10(b), the as-implanted sample contains the highest amount (~ 25%) of Si sub-oxides. The annealing reduces the percentage of Si sub-oxides. As the annealing temperature increases, the percentage of Si sub-oxides

reduces while the percentage of stoichiometric SiO_2 increases. The relatively high amount of Si sub-oxides in the as-implanted sample supports the proposed mechanism for the generation of local excess oxygen atoms in the SiO_2 matrix. The recovery in the SiO_2 matrix during annealing is caused by the local oxygen atoms in a process similar to the oxidation of the Ge nanoclusters.

Fig. 4-11(a) shows the typical O *1s* core level for the sample annealed at 800 °C. The peak deconvolution of the XPS spectrum shows a dominant peak at ~ 532.2 eV, corresponding to the O^{2-} in Si and Ge oxides [225]. It has been reported that the core level of O^{2-} in the oxide shifts to a lower binding energy when the oxide matrix is off-stoichiometric [225]. In Fig. 4-11(b), the dependence of the binding energy of the dominant O^{2-} peak on the annealing temperature is shown. For the as-implanted sample, the O^{2-} peak is located at ~ 531.8 eV. As the annealing temperature increases, the binding energy shifts to a higher value. Such a core level shift agrees with the oxidation of the Ge nanoclusters as well as the SiO_2 matrix during annealing. Besides, a minor peak located at ~ 531.3 eV is also present in Fig. 4-11(a). That is attributed to the local excess O atoms in the Ge-ion-implanted SiO_2 matrix. In Fig. 4-11(b), it is shown that the as-implanted sample has the highest amount of local excess O atoms, and the percentage of local excess O atoms decreases as the annealing temperature increases. The results support the above explanation that the oxidation of Ge nanoclusters is mainly caused by the local excess O atoms in the SiO_2 matrix.

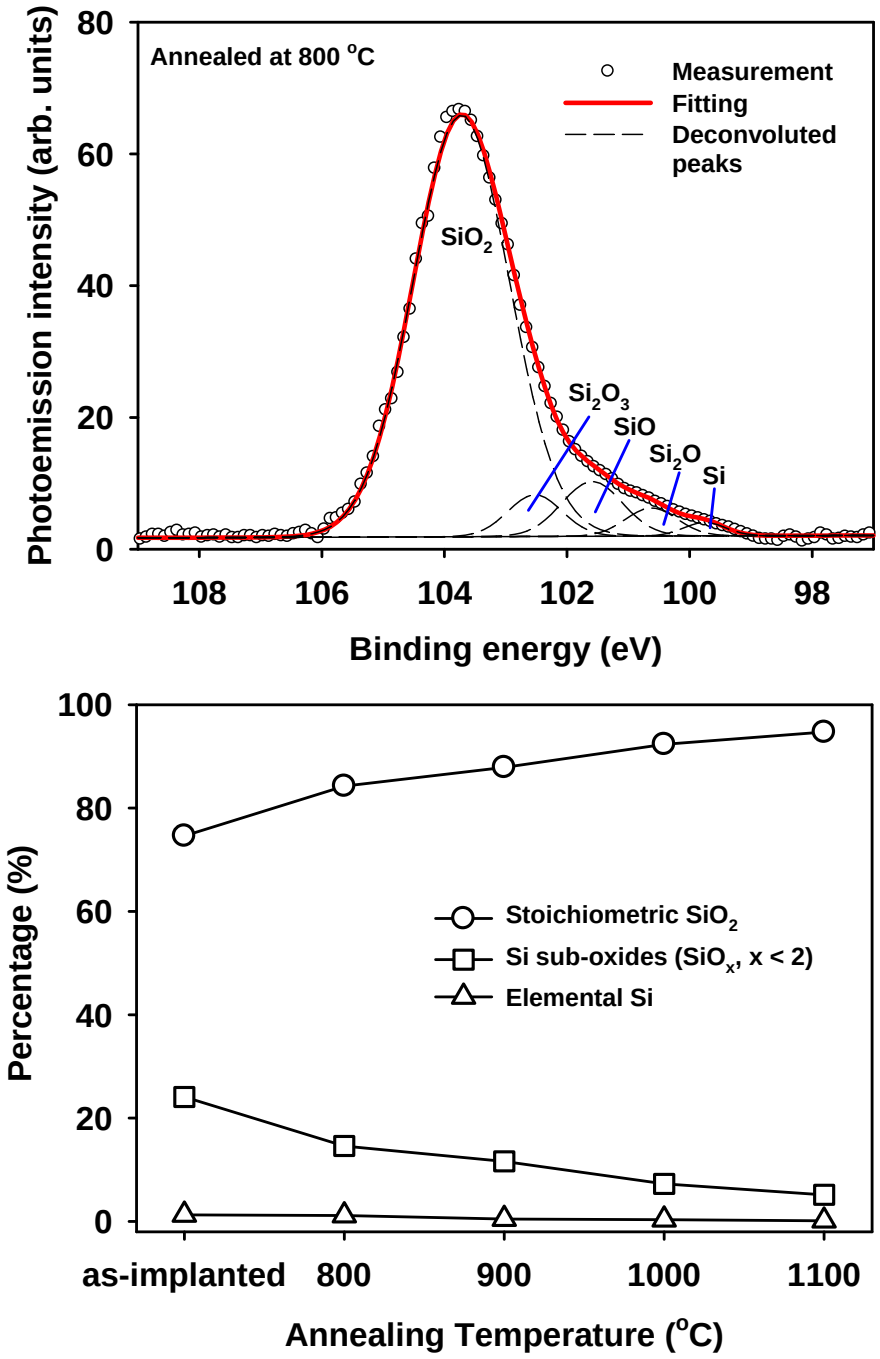

Fig. 4-10 Typical peak deconvolution of the Si *2p* core level for the sample annealed at 800 °C; (b) Atomic percentages of stoichiometric SiO_2, Si sub-oxides (SiO_x, x<2) and elemental Si as functions of the annealing temperature.

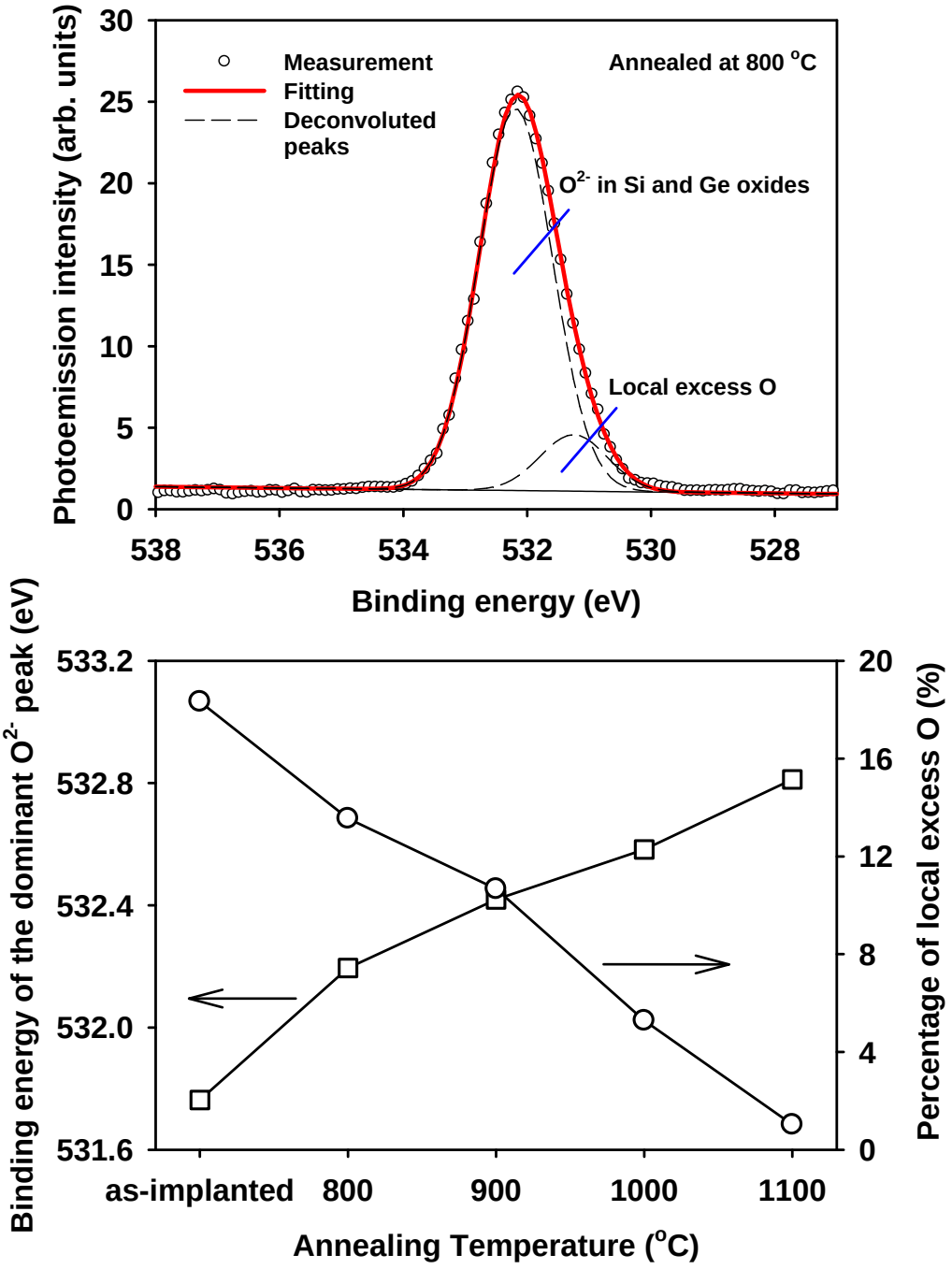

Fig. 4-11 Typical peak deconvolution of the O *1s* core level for the sample annealed at 800 °C; (b) Binding energy of the dominant O^{2-} peak and the percentage of local excess O atoms as functions of the annealing temperature.

4.4.3 Charge trapping behavior

C-V measurements were used to investigate the charge trapping behavior of the samples annealed at different temperatures. Similar to the typical *C-V* characteristics shown in Fig. 4-2, the ΔV_{FB} after applying a V_{CHARGE} to the gate electrode indicates the memory effect of these samples. Fig. 4-12 shows the ΔV_{FB} as a function of V_{CHARGE} for all the samples annealed at different temperatures. It can be found that the amount of trapped electrons depends on the magnitude of V_{CHARGE} as well as the annealing temperature. Indeed, a similar trend can be observed for all the four samples annealed at different temperature. As shown in Fig. 4-12, when the magnitude of V_{CHARGE} increases from 10 V to a more positive value, the ΔV_{FB} initially remains at values less than 0.2 V. When V_{CHARGE} reaches a certain voltage level (~ 21 to 23 V depending on the annealing temperature), the ΔV_{FB} starts to increase rapidly. Under a positive V_{CHARGE}, electrons are injected from the Si substrate into the charge storage sites (i.e., nc-Ge) through the tunneling oxide with a low Ge concentration. The rapid increase in the ΔV_{FB} is attributed to a large increase in the electron injection as a result of the FN tunneling occurring at a sufficiently high electric field.

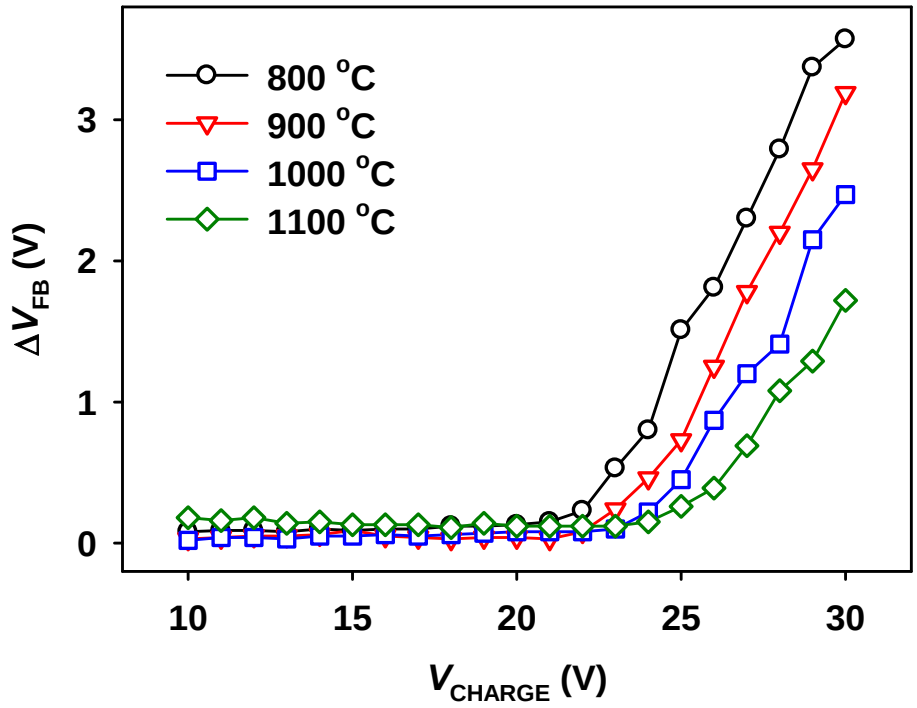

Fig. 4-12 ΔV_{FB} as a function of the positive V_{CHARGE} for different annealing temperatures. The charging duration is 1 s.

Fig. 4-12 also shows the influence of annealing temperature on the magnitude of ΔV_{FB} which is proportional to the amount of trapped electrons. The effect of annealing temperature is not obvious when V_{CHARGE} is small; however, at a large V_{CHARGE} (e.g., V_{CHARGE} is larger than the onset voltage of FN injection as discussed above), the sample annealed at a higher temperature has an obvious reduction in the ΔV_{FB}, indicating that a smaller number of electrons are trapped. The relationship between the annealing temperature and the electron trapping can be explained based on the oxidation of the charge storage sites. As discussed previously, annealing at a higher temperature results in more oxidation of Ge and hence a smaller amount of nc-Ge that

can store the injected electrons. Since the conduction band of nc-Ge is responsible for the electron storage, as discussed previously in Section 4.3.3, the reduction in the amount of nc-Ge indeed leads to fewer charge storage sites. During the FN tunneling of electrons under the application of a large V_{CHARGE}, the electron trapping is limited by the available number of charge storage sites, hence the charge trapping degrades with increasing annealing temperature. As for a smaller V_{CHARGE}, no significant difference in the ΔV_{FB} can be observed for different temperatures, because the electron injection is insignificant before the occurrence of the FN tunneling.

4.4.4 Charge retention behavior

The charge retention behavior for all the annealed samples is shown in Fig. 4-13. A suitable V_{CHARGE} was selected for each sample to obtain a similar level of initial ΔV_{FB}. As shown in the inset of the figure, the charge loss is faster for a higher annealing temperature up to 1000 ºC. For example, the charge loss after 3×10^4 s is 7% for the sample annealed at 800 °C, but it significantly increases to 16% for annealing at 1000 °C. However, the charge loss for the sample annealed at 1100 ºC drops to only 9%, which is significantly smaller than that annealed at 1000 ºC.

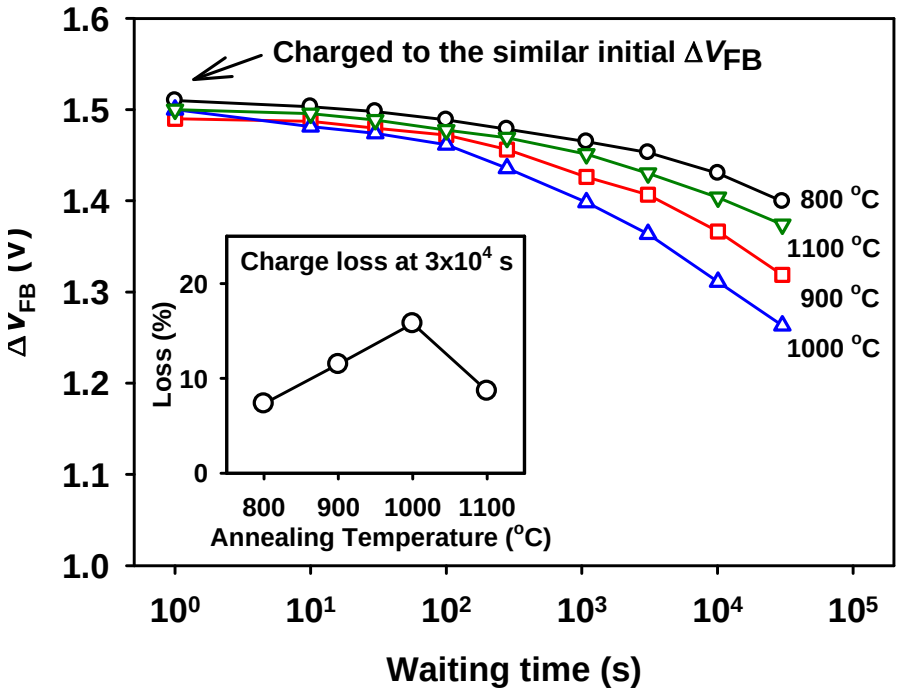

Fig. 4-13 Charge retention behavior for different annealing temperatures. All the samples were charged to a similar level of initial ΔV_{FB}. The inset shows the percentages of charge loss after 3×10^4 s for all the samples.

The charge retention behavior can be explained by taking into account the charge leakage from the charge storage sites to the Si substrate and the gate electrode. As shown in the schematic diagram in Fig. 4-14, Region 1 is the SiO_2 region near the surface containing most of the nc-Ge or Ge nanoclusters formed by the high concentration of Ge atoms, and Region 2 is the SiO_2 region near the Si substrate contains the diffusing Ge monomers distributed in the SiO_2. Both the nc-Ge and Ge monomers act as the leakage sites for the trapped electrons, forming the leakage paths between the charge storage sites and the Si substrate or the gate electrode, as shown in Fig. 4-14(a). The annealing temperature could affect the charge retention in two ways.

Firstly, a higher annealing temperature leads to a wider distribution of Ge atoms in the gate oxide, especially in Region 2. In other words, more leakage paths can be formed in Region 2 for a higher annealing temperature, leading to easier charge escape to the Si substrate. Secondly, the Ge oxidation increases with annealing temperature. While the non-oxidized / partially oxidized nc-Ge and the non-oxidized diffused Ge monomers can act as the charge leakage sites through which the leakage paths are formed, the completely oxidized nc-Ge / monomers (i.e., the stoichiometric Ge oxide) are not able to transfer charges. As shown in Fig. 4-14(b), a leakage path is blocked when one nc-Ge or monomer in the leakage path is completely oxidized. Therefore, the loss of trapped electrons is suppressed as a result of more Ge oxidation. Both of these competing mechanisms affect the charge retention. For annealing temperatures from 800 ºC to 1000 ºC, the first mechanism plays a dominant role; hence the charge loss is more severe for a higher annealing temperature. However, the second mechanism is more important for the 1100 ºC annealing. This explains why the charge loss for the 1100 ºC annealing is smaller than that for the 1000 ºC annealing.

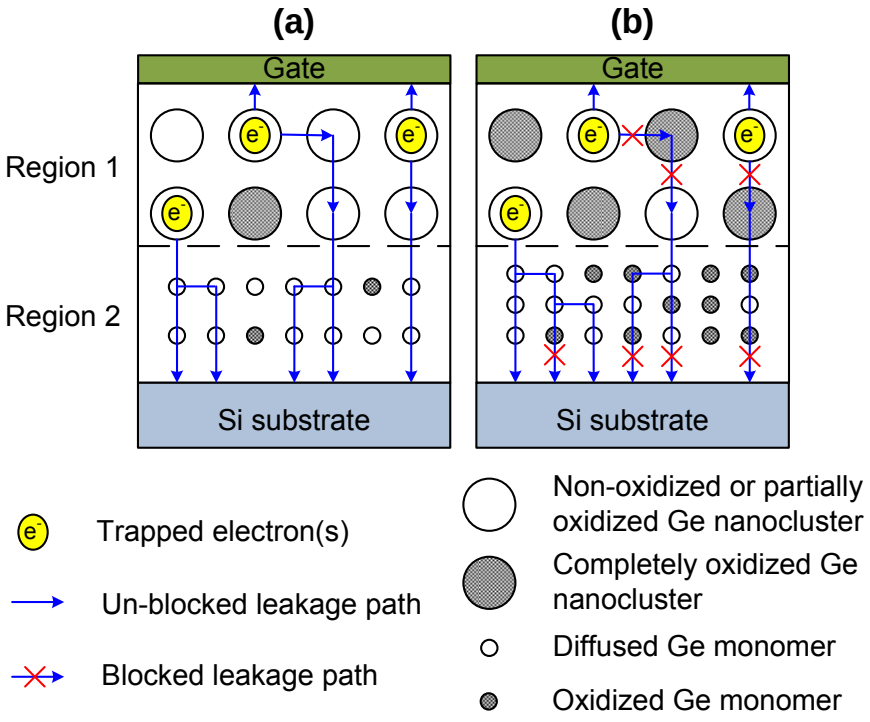

Fig. 4-14 Schematic diagrams showing the two competing mechanisms that affect the charge retention: (a) formation of leakage paths by the Ge leakage sites (nc-Ge and Ge monomers); and (b) blocking of the leakage paths due to the oxidation of the Ge leakage sites.

4.4.5 Conclusion

In conclusion, the influence of annealing temperature (i.e., from 800 to 1100 ºC) on the charge trapping and charge retention have been studied. The enhancement in the Ge diffusion toward to the Si substrate and the Ge oxidation has been revealed by the SIMS and XPS analysis, respectively. From the electrical measurements, it has been found that the electron trapping capability decreases with annealing temperature. This phenomenon is explained in terms of the increase of the Ge oxidation with

annealing temperature. On the other hand, it has been found that the charge retention is worsened when the annealing temperature increases in the range up to 1000 ºC, but it is improved at 1100 ºC. Such phenomenon has been explained by the following two competing mechanisms involved in an annealing: 1) the formation of leakage paths by the diffusion of Ge atoms in the SiO_2 and 2) the blocking of leakage paths due to the oxidation of Ge leakage sites.

4.5 Influences of implant energy and dose on charge trapping and charge retention behavior

For the ion implantation technique, the implant energy and implant dose are two important parameters to control the density and depth distribution of the implanted Ge ions. As a result, the electrical behavior is affected by the implant conditions. In this section, the influence of the implant energy and dose on the charge trapping and charge retention behavior of the Ge-ion-implanted SiO_2 thin films is presented. The samples studied here are MOS structures based on Group I and II samples, in which the nc-Ge are distributed in a narrow layer near the SiO_2 surface.

4.5.1 Charge trapping behavior

From the *C-V* measurements, it can be observed that all the samples with different implant conditions exhibit a memory effect in terms of ΔV_{FB} after charging by a constant V_{CHARGE} for 1 s. The shift in the C-V characteristics has been described previously in Section 4.3.1. The positive ΔV_{FB} for a positive V_{CHARGE} indicates the trapping of electrons in the nc-Ge. However, the magnitude of ΔV_{FB} under the same

charging condition is affected by the implant conditions. As shown in Fig. 4-15, the ΔV_{FB} for Group II samples (i.e., the samples with the same implant energy but different implant doses) are compared. For V_{CHARGE} = 20 V, the ΔV_{FB} is very small (i.e., ~ 0 V) because the applied V_{CHARGE} is not sufficient to cause the FN tunneling of electrons across the tunneling oxide, i.e., the oxide separating the nc-Ge layer and the Si substrate. For V_{CHARGE} = 26 V and 30 V, the ΔV_{FB} becomes much larger than in the case of V_{CHARGE} = 20 V because the electrons are injected from the Si substrate into the nc-Ge by the process of FN tunneling. In Fig. 4-15, it can be observed that the magnitude of ΔV_{FB} increases with the implant dose. As the implant dose increases, the Q_{nc-Ge} in Eq. (4.1) (i.e, the expression of ΔV_{FB}) becomes larger because more charge storage sites (i.e., nc-Ge) are available in the nc-Ge distributed region as a result of the higher Ge concentration in SiO_2. Thus, the ΔV_{FB} increases with the implant dose.

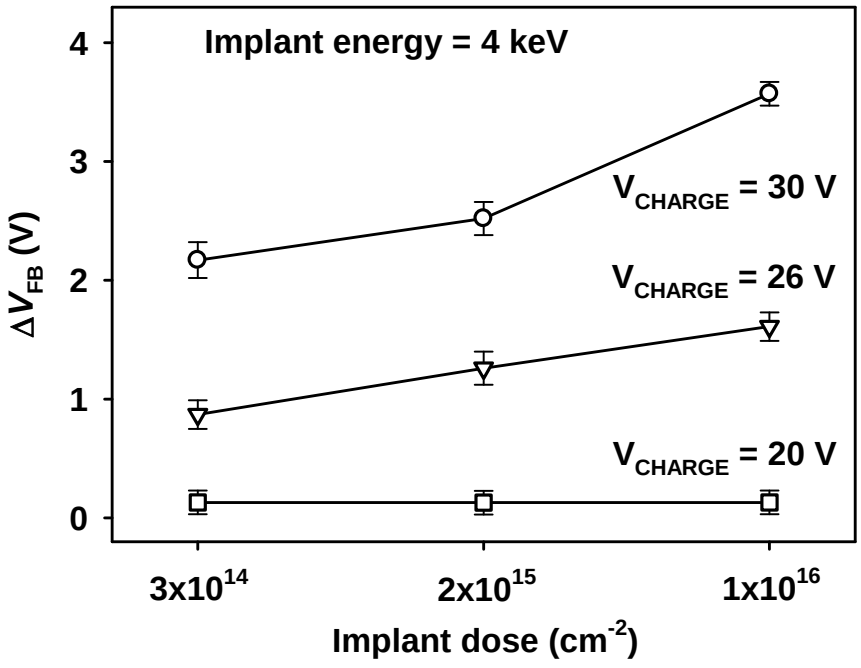

Fig. 4-15 Influence of the implant dose on ΔV_{FB} under various charging voltages.

On the other hand, the ΔV_{FB} for Group I samples (i.e., the samples with the same implant dose but different implant energies) are shown in Fig. 4-16. For V_{CHARGE} = 26 V and 30 V, the ΔV_{FB} increases with the implant energy, but it shows a saturation when the energy reaches ~ 6 to 8 keV. The SIMS depth profiles of Ge in SiO_2 thin films for the samples with different implant energies have been shown previously in Fig. 3-6. As the implant energy increases from 2 to 8 keV, the Ge distribution becomes broader, the location of the Ge peak shifts toward the Si substrate and the Ge peak concentration reduces from 3.0×10^{21} cm^{-3} to 1.6×10^{21} cm^{-3}, however the implanted Ge atoms are still confined in the SiO_2 layer due to the low implant energy. Although the Ge peak concentration decreases with the implant energy, the Ge concentration in the SiO_2 region near the Si substrate increases due to the broadening of the Ge distribution. With the SIMS results, the relationship between ΔV_{FB} and the implant energy can be understood. For higher implant energy, the t_C in Eq. (4.1) becomes larger because the distribution of the charge storage sites (i.e., nc-Ge) is closer to the Si substrate. However, when the implant energy increases, the Ge concentration in the nc-Ge distributed region reduces because the implant dose for Group II samples is the same. That leads to a lower density of charge trapping sites, i.e., a lower Q_{nc-Ge}. While the increase in t_C leads to a larger ΔV_{FB}, the drop in Q_{nc-Ge} tends to reduce the ΔV_{FB}. Thus, when the implant energy increases from 2 keV to 6 keV, the increase in t_C (i.e., the reduction in the tunneling oxide thickness) plays a major role, thus the ΔV_{FB} increases. However, the ΔV_{FB} saturates when the implant energy further increases, because of the reduction in Q_{nc-Ge}.

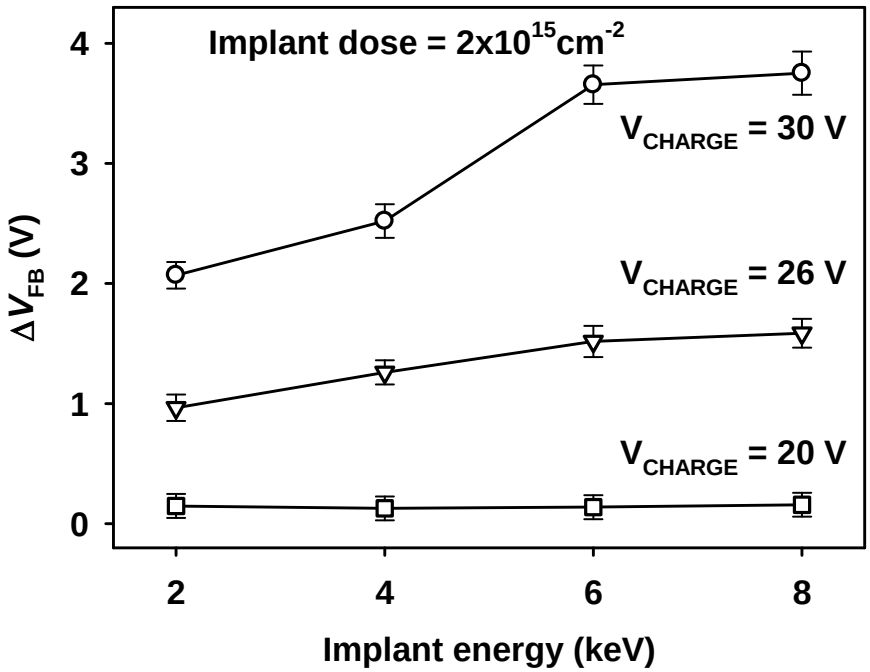

Fig. 4-16 Influence of the implant energy on the ΔV_{FB} under various charging voltages.

4.5.2 Charge retention behavior

The charge retention behavior for all the samples was obtained based on the similar method as described in Section 4.3.5. Fig. 4-17 and Fig. 4-18 show the charge retention behavior for the samples with different implant conditions. Typically, the change in ΔV_{FB} is not significant for the first 100 to 500 s after charging, but a reduction in ΔV_{FB} can be observed after 500 s waiting time. The reduction in ΔV_{FB} indicates the loss of trapped electrons. The degree of charge loss depends on the sample fabrication conditions, i.e., the implant energy and dose. As shown in Fig. 4-17, for samples with the same implant energy, a larger implant dose leads to a more severe charge loss. The inset of Fig. 4-17 clearly indicates that the charge loss after 3×10^4 s increases from ~ 3% to ~ 6% when the dose increases from 3×10^{14} to 1×10^{16} cm^{-2}.

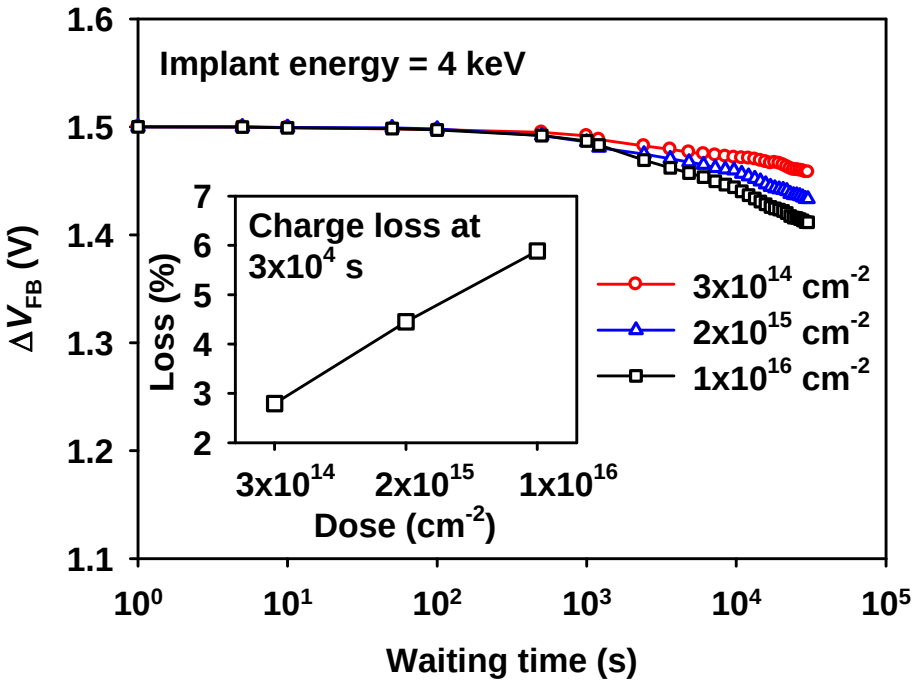

Fig. 4-17 ΔV_{FB} as a function of waiting time for samples with the same implant energy but different doses. All the samples were charged to the same level of initial ΔV_{FB}. The insets show the charge loss after 3×10^4 s for different implantation conditions.

On the other hand, Fig. 4-18 shows the situation for samples with the same implant dose but different implant energies. As the implant energy increases, the charge loss becomes less. The inset of Fig. 4-18 shows that the charge loss after 3×10^4 s is ~ 10% for the 2 keV sample, but it reduces to less than 2% for the 8 keV one. In other words, for the same implant dose, an increase in the implant energy leads to better charge retention.

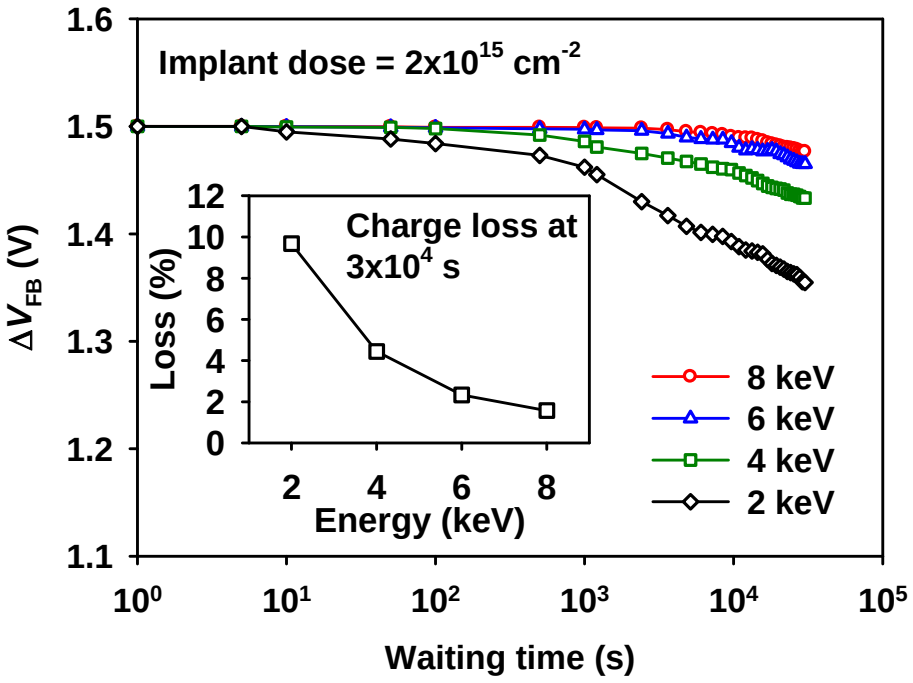

Fig. 4-18 ΔV_{FB} as a function of waiting time for samples with the same implant dose but different energies. All the samples were charged to the same level of initial ΔV_{FB}. The insets show the charge loss after 3×10^4 s for different implantation conditions.

The charge retention behavior is explained as follows. In the MOS structure containing the nc-Ge distributed as one layer in the gate oxide, the loss of trapped electrons could be due to the leakage from the nc-Ge to the Si substrate and the Al gate electrode, or the lateral charge leakage to the adjacent nanocrystals [96], as shown in Fig. 4-19. Both mechanisms could contribute to the charge loss during the retention experiments. For samples with identical implant energy, their nc-Ge regions are located at a similar location in the SiO_2 due to the same implant energy. However, since a higher implant dose leads to a higher nc-Ge concentration, the possibility of lateral charge leakage increases, leading to a more significant charge loss. This

explains the poorer charge retention observed in the samples with a higher implant dose. On the other hand, for samples with a constant implant dose, as the implant energy increases, the distance between the nc-Ge layer and the Al gate also increases, making the charge leakage to the Al gate more difficult. In addition, the reduction in the nc-Ge concentration also reduces the probability of lateral charge leakage. Hence, for higher implant energy with the same implant dose, the charge retention is improved. It is worth mentioning that although the charge leakage to the Si substrate is possible, it should be much less significant as compared to the leakage to the Al gate, because the nc-Ge layer is much closer to the Al gate.

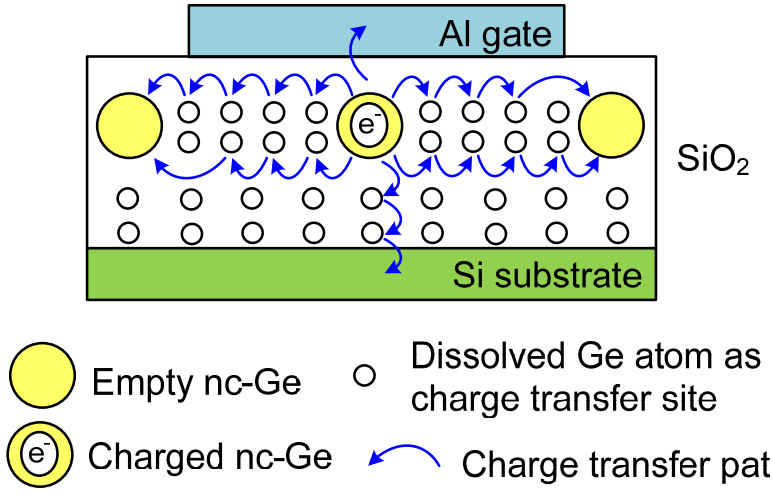

Fig. 4-19 Schematic diagram showing two charge transfer paths: 1) leakage to Al gate / Si substrate, 2) lateral charge transfer.

4.5.3 Conclusion

In this section, it has been demonstrated that the ion implantation conditions, i.e., implant energy and dose, have a strong influence on the memory window as well as

the long-term charge retention. By increasing either the implant dose or the implant energy, a larger flat-band voltage shift can be achieved, indicating the enhanced charge trapping. That has been explained by the locations and concentration of the charge trapping sites supported by Ge depth profiles measured by the SIMS technique. The smaller charge loss, i.e., a better charge retention, can be achieved by decreasing the implant dose or increasing the implantation energy. That has been explained by the co-existence of two competing mechanisms: 1) the charge leakage to the Al gate electrode and 2) the lateral charge loss to the adjacent nc-Ge. The results are important for the design and application of the ion-implantation-synthesized nanocrystal-based non-volatile memory devices.

4.6 Role of lateral charge transfer in the charge retention

For the memory structures based on Ge-ion-implanted SiO_2 thin films, the memory operation relies on the charge storage in the isolated nc-Ge formed in the excess-Ge-distributed region. However, the loss of trapped charges from nc-Ge degrades the memory performance. It is known that a small amount of Ge atoms can dissolve in SiO_2 [49], resulting in the presence of dissolved Ge atoms in the oxide separating adjacent nc-Ge. As a result, a channel of lateral charge transfer could exist in the excess-Ge-distributed region, and charges stored in one nc-Ge could transfer to adjacent ones during the long-term charge retention. Charge leakage to the Si substrate could also happen. In this section, MOS structures with and without a channel of lateral charge transfer are purposely prepared. The charge loss caused by the lateral charge transfer along the nc-Ge distributed region and charge leakage to the Si

substrate is investigated. This study aims to confirm the existence of the lateral charge transfer in the excess-Ge-distributed region and to identify the role of lateral charge transfer in the charge retention.

4.6.1 Experimental details

4.6.1.1 Sample fabrication

The samples studied in the previous part of this chapter are 30 nm SiO_2 thin films implanted with Ge ions under various implant conditions. Although the additional deposition of a capping SiO_2 layer (i.e., control oxide) is not required, charge leakage to both the Al gate and the Si substrate could occur. For the study of lateral charge transfer, a structure with a relatively thick control oxide and a narrow nc-Ge layer close to the Si is preferred. In such a structure, two charge transfer mechanisms, namely the lateral charge transfer along the excess-Ge-distributed layer [96] and the leakage of trapped charges from the nc-Ge to the Si substrate across the tunnel oxide [226, 227], can be identified, while the charge leakage to the Al gate can be eliminated by the thick control oxide.

The fabrication began with the growth of an 11 nm SiO_2 thin film by dry oxidation at 850 °C on the *p*-type (100) Si substrate with the resistivity of 9 – 12 Ω-cm. Ge ions were then implanted into the thermal oxide at 2 keV with a dose of 3×10^{16} cm^{-2}. Subsequently, about 30 nm SiO_2 was deposited on the Ge-ion-implanted SiO_2 using the plasma-enhanced chemical vapor deposition (PECVD) technique with SiH_4 and N_2O as precursor gases. To induce the formation of nc-Ge, high-temperature

annealing at 800 ºC in N_2 (purity: 99.99%) ambient was performed for 30 minutes. An as-implanted sample without annealing was also prepared.

4.6.1.2 Structural characterization

The depth profiles of Ge in SiO_2 for the as-implanted and annealed samples obtained from the SIMS measurement are shown in Fig. 4-20. The Si depth profiles are also shown to highlight the oxide / Si interface. As shown in Fig. 4-20(a), for the as-implanted sample, the Ge atoms approximately follow a Gaussian distribution with a peak concentration of 6.7×10^{22} cm^{-3} at ~ 33 nm away from the oxide surface. After thermal annealing at 800 ºC, as shown in Fig. 4-20(b), two well-separated Ge concentration peaks can be clearly observed. The dominant Ge peak remains at a depth of ~ 33 nm, but its concentration drops to about half of the as-implanted value. Another Ge concentration peak is located beneath the oxide / Si interface with a lower concentration as compared to the dominant peak. During the initial period of the annealing process, the crystallization of nc-Ge occurs in the thermal oxide region with a high Ge concentration. Meanwhile, some Ge atoms are dissolved in the oxide and behave as free diffusing monomers with high mobility in the oxide [49]. During the annealing, these dissolved Ge atoms can diffuse along the concentration gradient from the high concentration region to the Si substrate. Due to the presence of an oxide / Si interface, the diffused Ge atoms tend to accumulate and form another Ge concentration peak at the interface [49, 212].

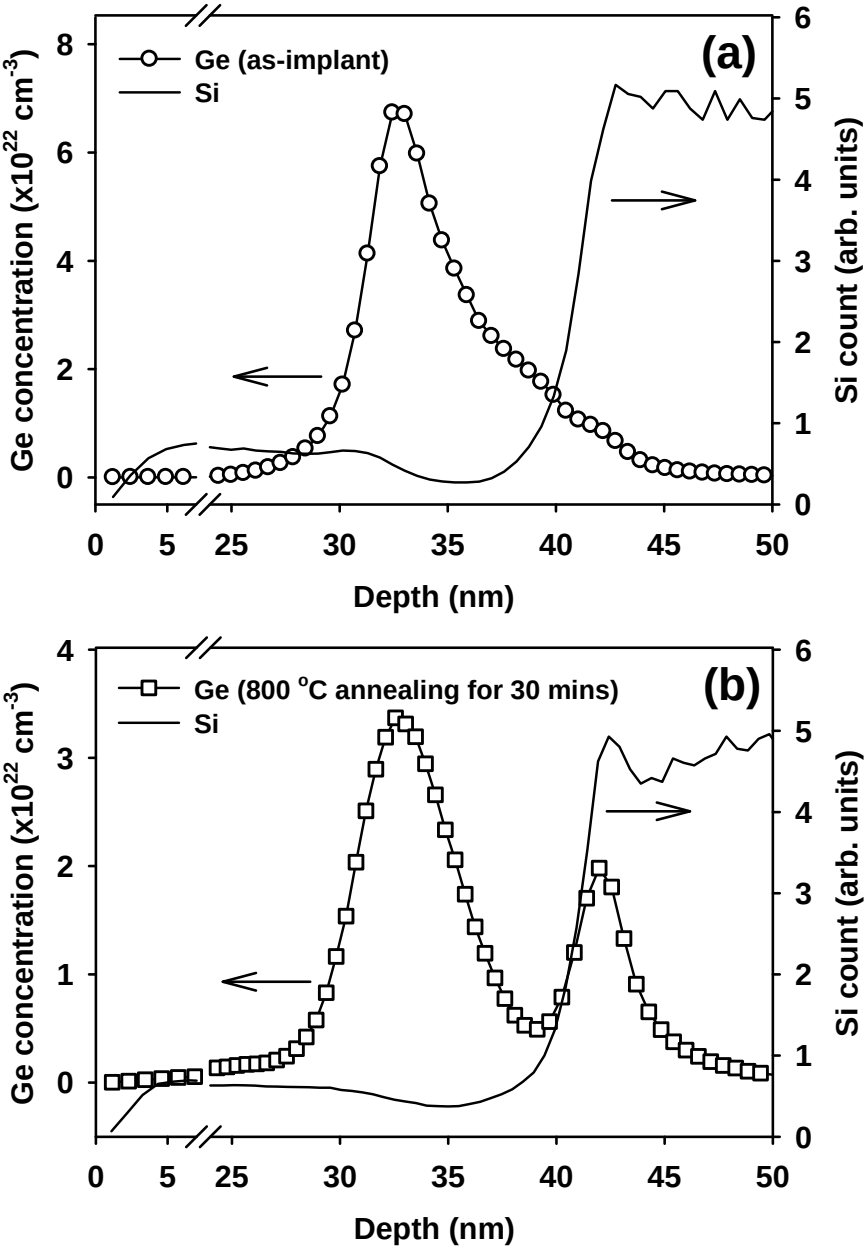

Fig. 4-20 SIMS depth profiles of Ge in the as-implanted sample (a) and the annealed sample (b). The Si depth profiles are also shown to identify the oxide / Si interface.

The microstructure of the Ge-ion-implanted SiO_2 was observed by cross-sectional TEM. The existence of a layer of evenly distributed nc-Ge with an average size of ~ 5 nm is clearly observed in the TEM image, as shown in Fig. 4-21. The location of this nc-Ge layer agrees with the position of the dominant Ge peak in the SIMS profile. The tunnel oxide thickness (i.e., the distance between the nc-Ge layer and Si substrate) and the control oxide thickness (i.e., the distance between the nc-Ge layer and the oxide surface) are ~ 5 nm and ~ 31 nm, respectively. As compared to the region of the pure oxide near the oxide surface, both the tunnel oxide and the oxide between two nearby nc-Ge particles show slightly darker contrast in the TEM image, suggesting the existence of dissolved Ge atoms in these oxide regions. Besides, a homogenous layer with a thickness of ~ 3.5 nm is observed beneath the oxide / Si interface. Clearly, this layer corresponds to the Ge concentration peak near the oxide / Si interface observed in the SIMS profile. This layer is a Si_xGe_y layer because the accumulated Ge can react with the Si substrate and form the Si_xGe_y alloy during the high-temperature annealing [228].

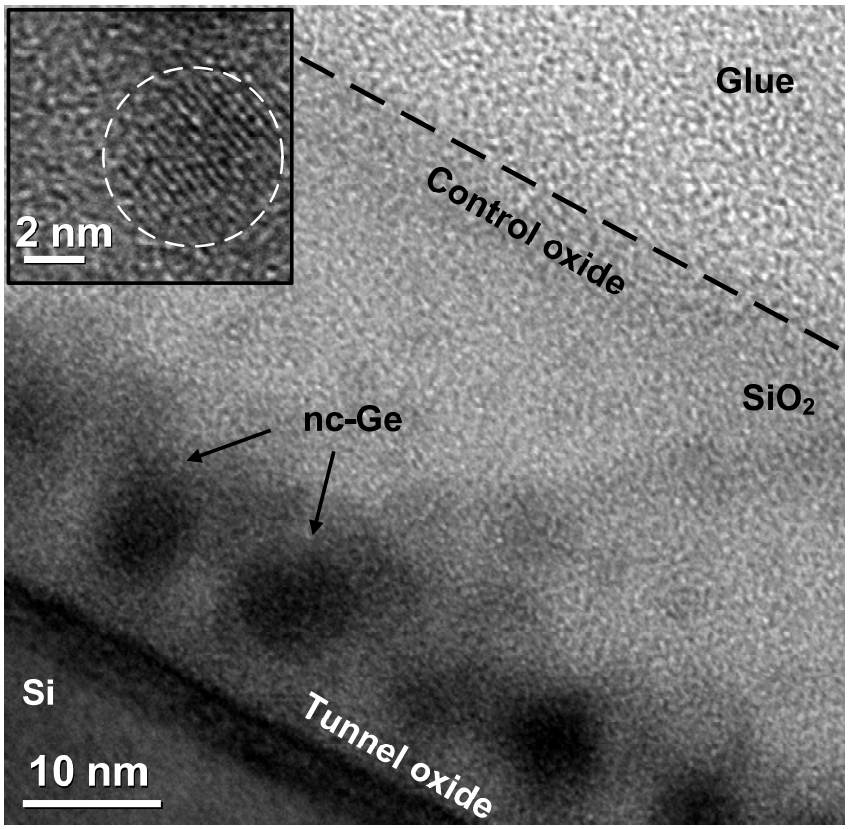

Fig. 4-21 Cross-sectional TEM image showing a layer of nc-Ge embedded in the gate oxide near the Si substrate. The inset shows the TEM image of a single nc-Ge.

4.6.1.3 Electrical characterization

In this study, the MOS structures were characterized by a Keithley 4200 Semiconductor Characterization System at room-temperature in a light-shielded environment. Two MOS structures, i.e., non-isolated and isolated MOS structures, were fabricated. Fig. 4-22(a) shows the non-isolated MOS structure created by the deposition of an array of Al gate electrodes directly on the Ge-ion-implanted SiO_2 thin film. Each gate electrode is circular in shape with a diameter of 160 μm and a thickness of 250 nm. The wafer backside was coated with a 250 nm Al layer as the

backside contact. Since the Ge ion implantation was carried out over the entire SiO_2 layer, the oxide of the areas not covered by the gate electrodes also contains Ge. Thus, each MOS structure is not isolated from its surrounding nc-Ge and dissolved Ge atoms. It will be shown later that the charge transfer in the oxide of a non-isolated MOS structure is affected by its surrounding nc-Ge and dissolved Ge atoms. Fig. 4-22(b) shows the isolated MOS structure. The deposition of the Al gate electrodes and the Al backside contact was identical to that of the non-isolated MOS structure. However, the Ge-ion-implanted oxide which is not covered by the Al gate electrodes was purposely removed by an anisotropic dry-etching step using CF_4 as the etchant. By doing this, each MOS structure is isolated from its surrounding Ge-ion-implanted oxide.

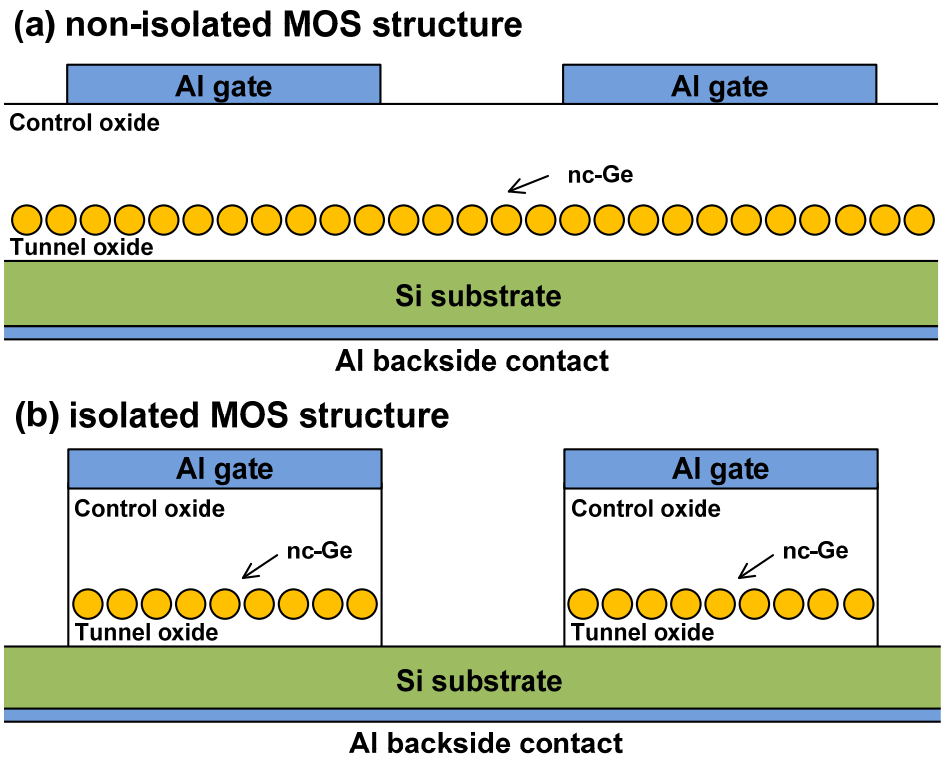

Fig. 4-22 Schematic diagrams for the non-isolated (a) and the isolated MOS (b) structures.

4.6.2 Charge trapping behavior

To study the charge transfer behavior, charge injection was performed by applying a constant V_{CHARGE} to the gate electrode of the MOS structure for 1 s while the backside contact was grounded. Fig. 4-23 shows the typical high-frequency (1 MHz) *C-V* characteristics of the non-isolated MOS structure with the Ge-ion-implanted SiO_2 thin film annealed at 800 °C for 30 minutes. As shown in the figure, for V_{CHARGE} of 10 and 18 V, the ΔV_{FB} is 0.7 V and 2.1 V, respectively. The positive ΔV_{FB} indicates electron-trapping in the conduction band of nc-Ge [20, 229]. For the isolated MOS structure, a similar charge injection behavior can also be observed, which is expected because the nc-Ge distributed oxide for the non-isolated and isolated sample is identical. For both the non-isolated and isolated MOS structures, the ΔV_{FB} is related to the trapped electron density ($Q_{\mathrm{nc-Ge}}$) in nc-Ge by Eq (4.1). For example, using the values of t_C and $d_{\mathrm{nc-Ge}}$ as determined from the TEM image, $Q_{\mathrm{nc-Ge}}$ is 7.6 × 10^{-8} C/cm^2 and 2.3 × 10^{-7} C/cm^2 for V_{CHARGE} = 10 and 18 V, respectively.

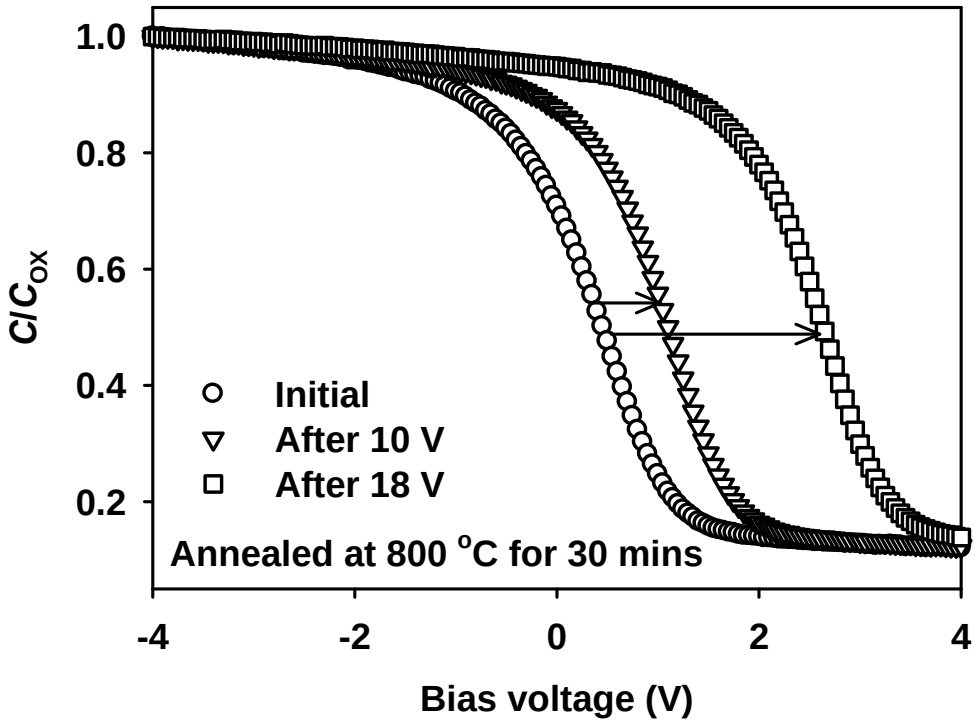

Fig. 4-23 Shifts in the *C-V* characteristic caused by the charging at V_{CHARGE} = 10 and 18 V for 1 s.

Fig. 4-24 shows Q_{nc-Ge} as a function of the V_{CHARGE} for both non-isolated and isolated MOS structures with the Ge-ion-implanted SiO_2 thin film. As the magnitude of V_{CHARGE} increases, Q_{nc-Ge} also increases due to the enhanced electron injection with a higher electric field across the nc-Ge embedded oxide. Not much difference in the characteristics of the Q_{nc-Ge} versus V_{CHARGE} can be observed between the non-isolated and isolated MOS structures. The result indicates that the isolation step does not change the density of the trapping sites (i.e., nc-Ge) in the Ge-ion-implanted SiO_2 thin film.

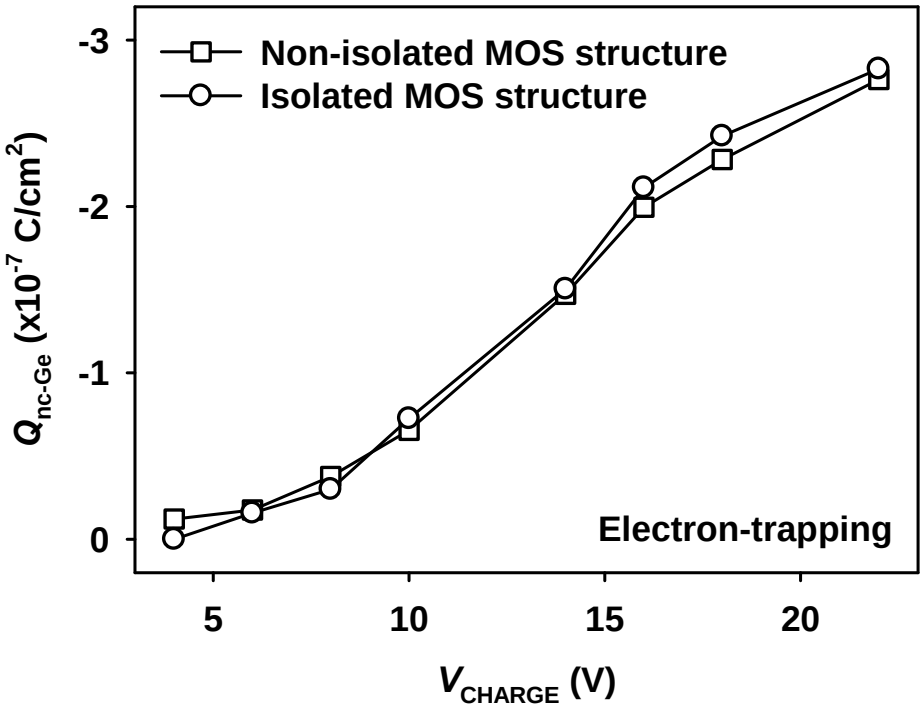

Fig. 4-24 Density ($Q_{\text{nc-Ge}}$) of trapped electrons as a function of V_{CHARGE} for (a) the non-isolated and (b) isolated MOS structures. The charging time is 1 s.

4.6.3 Charge retention behavior

Although the isolation step does not affect the charge trapping, it affects the retention of trapped charges. For the charge retention measurements, each MOS structure was charged to an identical amount of initial $Q_{\text{nc-Ge}}$, and the change in $Q_{\text{nc-Ge}}$ with waiting time was monitored. The gate electrode and backside contact were grounded during the waiting period between two consecutive *C-V* measurements. The results for both non-isolated and isolated MOS structures are shown in Fig. 4-25. The relationship between $Q_{\text{nc-Ge}}$ and the waiting time is different between the non-isolated and isolated samples. For the non-isolated MOS structure, the decay curve of

$Q_{\mathrm{nc-Ge}}$ exhibits two distinct regions, including a faster initial decay over the first 100 s and a relatively slower decay after the first 100 s. Over the first 100 s, the charge loss in $Q_{\mathrm{nc-Ge}}$ is ~ 19%. After the first 100 s, the dependence of $Q_{\mathrm{nc-Ge}}$ on the waiting time (t) in the charge decay curve can be fitted by a logarithmic relationship

$$Q_{\mathrm{nc-Ge}}(t) = a + b \ln t \tag{4.4}$$

where a and b are the fitting parameters. The overall charge loss after 5×10^4 s for the non-isolated MOS structure is ~ 43%. On the other hand, the isolated MOS structure exhibits only a continuous logarithmic decay over the entire waiting period, as shown in Fig. 4-25. The logarithmic relationship between $Q_{\mathrm{nc-Ge}}$ and waiting time can also be confirmed by fitting using Eq. (4.4). Since there is no fast initial decay component, the isolated MOS structure has less charge loss than the non-isolated one. For the isolated MOS structure, the overall charge loss after 5×10^4 s is only ~ 18%.

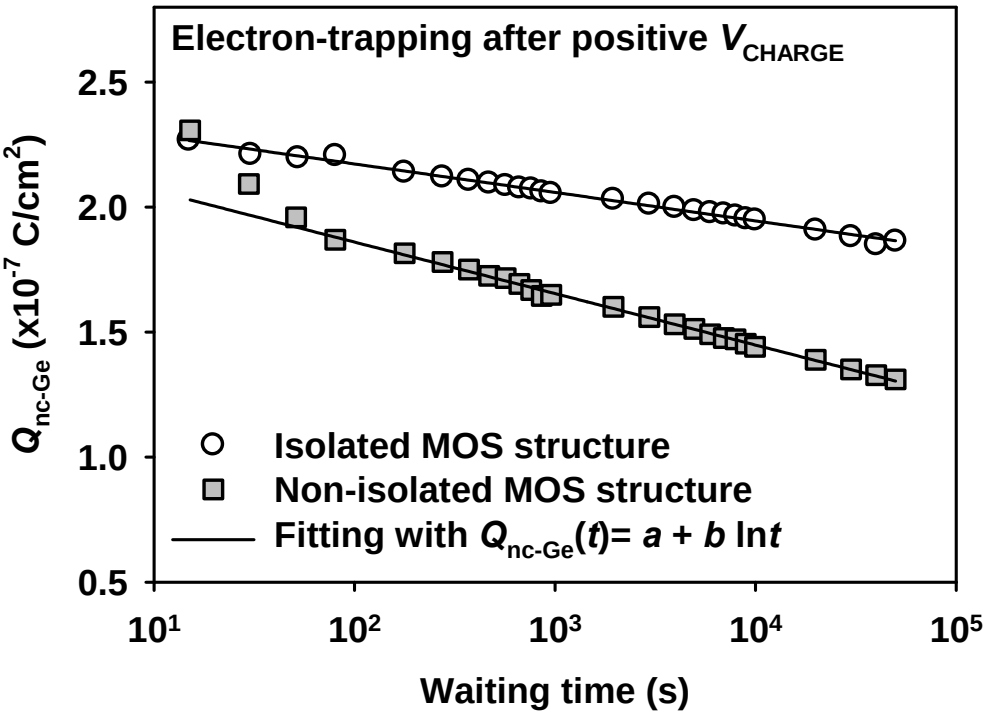

Fig. 4-25 Density of trapped electrons ($Q_{nc\text{-}Ge}$) as a function of the waiting time for the non-isolated (a) and isolated (b) MOS structures.

The following two charge transfer mechanisms could be responsible for the charge loss in the non-isolated MOS structure. The first mechanism is the leakage of trapped charges from the nc-Ge to the Si substrate across the 5 nm tunnel oxide [226, 227]. Such a mechanism usually leads to a logarithmic decay of trapped charges with time [227]. As shown previously by the SIMS results, the tunnel oxide contains dissolved Ge atoms. These dissolved Ge atoms act as charge transfer sites and contribute to the charge transfer from the nc-Ge to the Si substrate. The second mechanism is the lateral charge transfer along the nc-Ge distributed layer, as pointed out by Kim [96]. The lateral charge transfer results in an exponential decay of trapped charges with time, which has been observed by previous electrostatic force

microscopy (EFM) studies [227, 230, 231]. In the Ge-ion-implanted oxide, since the oxide separating the nc-Ge contains dissolved Ge atoms, charge transfer could easily happen between adjacent nc-Ge via the charge transfer sites, leading to lateral charge transfer along the nc-Ge distributed layer. Since the Ge-ion-implanted oxide in one MOS structure is not isolated from its surrounding nc-Ge, the existence of the lateral charge transfer effectively causes the extension of charge distribution from one charged MOS structure to its surrounding uncharged nc-Ge outside the MOS structure. On the other hand, in the isolated MOS structure, the lateral charge transfer does not exist because the Ge-ion-implanted oxide outside the MOS structure has been purposely removed. Thus, the only possible charge transfer mechanism is the leakage of trapped charges to the Si substrate across the tunnel oxide.

With the aforementioned charge leakage mechanisms, the charge retention behavior for the non-isolated and isolated MOS structures as observed in Fig. 4-25 can be understood. For the non-isolated MOS structure, the decay of $Q_{\mathrm{nc-Ge}}$ is caused by both the lateral charge transfer along the nc-Ge layer and the leakage of trapped charges from the nc-Ge to the Si substrate. The initial fast decay component can be attributed to the lateral charge transfer, because it is not observed in the case of the isolated MOS structure. The result also suggests that during the initial stage (within ~ 100 s), the lateral charge transfer is faster than the leakage of trapped electrons to the Si substrate. This is because the amount of dissolved Ge atoms acting as the charge transfer sites between nc-Ge in the Ge-ion-implanted oxide is higher than that in the tunnel oxide, resulting in faster charge diffusion along the continuous Ge-ion-implanted oxide layer. During the charge diffusion process, the charges move from the

nc-Ge in the charged MOS structure to the surrounding uncharged nc-Ge, resulting in more electrons in those surrounding uncharged nc-Ge and fewer electrons in those initially charged nc-Ge. Thus, the charge diffusion process will slow down. After the initial fast charge loss through the lateral charge transfer, the leakage of charges to the Si substrate across the tunnel oxide plays a major role during the long-term charge retention. This explains the logarithmic dependence of $Q_{\mathrm{nc-Ge}}$ on the waiting time in the charge decay curve for the non-isolated MOS structure after 100 s. Such a logarithmic relationship between $Q_{\mathrm{nc-Ge}}$ and the waiting time as given in Eq. (4.4) is consistent with the work of Busseret *et al.* [227]. For the isolated MOS structure, due to the removal of the channel of lateral charge transfer, the charge retention is significantly improved. The logarithmic dependence of $Q_{\mathrm{nc-Ge}}$ over the entire waiting period suggests that the charge loss in the isolated MOS structure is only due to the leakage of charges to the Si substrate across the tunnel oxide.

From the above discussions, it is clear that for the non-isolated MOS structure, the decay of $Q_{\mathrm{nc-Ge}}$ during the initial 100 s is due to two charge transfer mechanisms. After the initial 100 s, the decay is mainly due to one charge transfer mechanism. As a result, by using proper curve fittings, the two charge transfer mechanisms can be separated. For the purpose of clarity, in the following discussion, Mechanism A is used to denote the lateral charge transfer along the nc-Ge layer, and Mechanism B is used to denote the leakage of trapped charges from nc-Ge to the Si substrate.

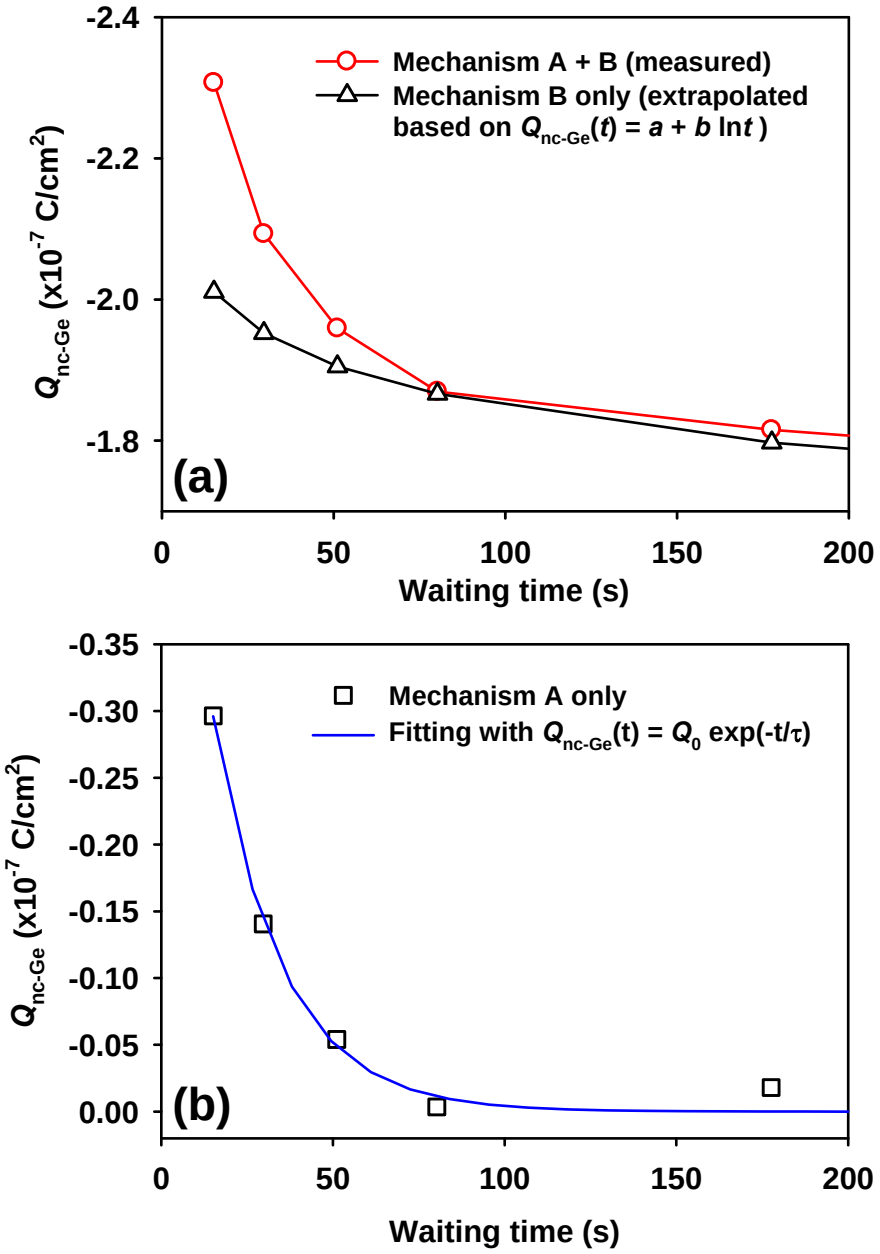

Fig. 4-26 (a) Density of trapped electrons ($Q_{nc\text{-}Ge}$) as a function of the waiting time for the non-isolated MOS structure. The charge decay due to Mechanism B is extrapolated; (b) Exponential charge decay corresponding to Mechanism A obtained from the difference between the two charge decay curves in (a).

As shown previously in Fig. 4-25, the charge decay after the first 100 s can be fitted by a logarithmic relationship using Eq. (4.4), which indicates that the dominant charge transfer mechanism is Mechanism B (i.e., the charge leakage to Si substrate). Based on this, the charge decay corresponding to Mechanism B for the initial 100 s can be extrapolated using Eq. (4.4). The extrapolated curve is shown in Fig. 4-26(a). Clearly, the extrapolated curve is different from the measured charge decay curve, which is a consequence of the co-existence of both Mechanism A and B. Therefore, the contribution of Mechanism A to the charge decay can be obtained from the difference between these two curves in Fig. 4-26(a). As shown in Fig. 4-26(b), the charge decay corresponding to Mechanism A (i.e., the lateral charge transfer) within the initial 100 s is an exponential function of the waiting time given by

$$Q(t) = Q_0 \exp(-t/\tau) \tag{4.5}$$

where Q_0 is the amount of initial charge and τ is the time constant, which is determined as 19.9 s from the fitting. The exponential relationship in Eq. (4.5) has also been observed in some previous electrostatic force microscopy (EFM) studies of lateral charge decay [227, 230, 231]. The result confirms the existence of the lateral charge transfer in the non-isolated MOS structure during the initial waiting period. For the case of the isolated MOS structure, the lateral charge transfer cannot be observed, because the channel of lateral charge transfer was purposely removed.

4.6.4 Conclusion

In this section, the low-energy (2 keV) Ge ion implantation with a high dose (3×10^{16} cm^{-2}) has been employed to synthesize a single layer of nc-Ge in the SiO_2 thin

film. The charge trapping and charge retention behavior of the MOS structures with and without the channel of lateral charge transfer has been studied. It has been found that besides charge leakage from the nc-Ge to the Si substrate, the lateral charge transfer along the Ge-distributed layer also contributes to the charge loss. For the non-isolated MOS structure, the lateral charge transfer mainly results in an initial fast decay within the initial 100 s, while the leakage of charges to the Si substrate across the tunnel oxide plays a major role after the initial fast decay. The charge decay contributed by the lateral charge transfer follows an exponential relationship with the waiting time with a time constant of 19.9 s. On the other hand, for the isolated MOS structure, the charge loss is only due to the leakage of charges to the Si substrate, because the channel of lateral charge transfer does not exist.

4.7 Summary

In this chapter, the charge trapping and charge retention behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been investigated. The dependences of charge trapping and charge retention on the polarity and magnitude of the charging voltage have been studied. For a positive charging voltage, only electron trapping occurs, and the trapped electrons show a long retention time. However, for a negative charging voltage, both the hole trapping and electron trapping occur simultaneously, and the hole trapping is dominant if the magnitude of the charging voltage is small or the charging time is short. Due to the relatively easier loss of the trapped holes, the net charge trapping in the nc-Ge exhibits a continuous shift towards a more negative value with the waiting time. Besides, the influences of the synthesis

process on the charge trapping and charge retention behavior have been investigated. The changes in the structural and chemical properties of the Ge-ion-implanted SiO_2 caused by thermal annealing have been found to seriously affect the charge storage behavior in the nc-Ge. Moreover, it has also been demonstrated that the ion implantation conditions, i.e., implantation energy and dose, have strong influences on the charge trapping as well as the long-term charge retention. Lastly, the charge loss caused by the lateral charge transfer along the Ge-distributed layer and charge leakage from the nc-Ge to the Si substrate has been studied. The existence of the lateral charge transfer has been confirmed, and the role of lateral charge transfer in the charge retention has been determined.

Chapter 5 Capacitance of Ge-ion-implanted SiO_2 Thin Films

5.1 Introduction

Ge nanocrystals (nc-Ge) have attracted much attention for the next-generation non-volatile memory devices due to their extended scalability and improved memory performance, such as low operating voltages, fast program / erase speeds, good endurance and long data retention time [59, 70, 78, 218]. The current transport and memory behavior (i.e., charge trapping and charge retention) of the Ge-ion-implanted SiO_2 thin films has been studied in Chapter 3 and Chapter 4, respectively. Due to the inclusion of nc-Ge in SiO_2, the dielectric properties of SiO_2 are modified. As a result, the gate capacitance of the metal-oxide-semiconductor (MOS) structure is affected by the nc-Ge embedded in SiO_2. The accurate determination of the MOS capacitance is important for the oxide thickness extraction [232], metallurgical channel length determination [233], mobility measurement [234] and interface trap characterization [235]. Although the MOS capacitance can be experimentally measured by the conventional capacitance-voltage (*C-V*) technique, a modeling approach to calculate the MOS capacitance as well as to determine the influence of nc-Ge on the MOS capacitance is essential for the design and modeling of the memory structures based on nc-Ge. Such a modeling approach should take into account the depth and distribution of the nc-Ge in the SiO_2, which can be precisely controlled by the Ge ion

implantation. Besides, due to the nanometer size of nc-Ge embedded in the SiO_2 matrix, the dielectric constant of nc-Ge is different from that of bulk crystalline Ge [236-240]. The influence of the dielectric constant of the nc-Ge on the MOS capacitance should also be considered in the modeling approach.

In this chapter, an approach to calculate the capacitance of the MOS structure based on a Ge-ion-implanted SiO_2 thin film embedded with nc-Ge is presented. This approach is based on the calculation of the effective dielectric constant of the SiO_2 embedded with nc-Ge using the sub-layer model for the nc-Ge distributed region and the Maxwell-Garnett effective medium approximation (EMA) for each sub-layer. Both the distribution of the nc-Ge in the SiO_2 and the dielectric constant corresponding to the nanometer size of the nc-Ge are taken into account in the calculation. In Section 5.4.3, the influence of implant energy and dose on the MOS capacitance is obtained using this modeling approach. In Section 5.4.4, the calculation is compared to the measurement of samples with various implant energies and doses. This modeling approach is useful for the design and modeling of the memory structures based on SiO_2 thin film embedded with nc-Ge.

5.2 Modeling of MOS capacitance

For a standard MOS capacitor based on a uniform gate dielectric layer, the MOS capacitance per unit area (C) under the strong accumulation condition is given by

$$C = \frac{\varepsilon_{\mathrm{FILM}}\varepsilon_0}{T_{\mathrm{FILM}}} \tag{5.1}$$

where $\varepsilon_{\mathrm{FILM}}$ is the dielectric constant of the gate dielectric layer, ε_0 is the permittivity of free space, and T_{FILM} is the thickness of the gate dielectric layer. For example, the capacitance of a pure SiO_2 can be calculated by Eq. (5.1). However, when the SiO_2 is embedded with nc-Ge, its dielectric constant is modified by the inclusion of the nc-Ge. For the case of Ge-ion-implanted SiO_2 thin films embedded with nc-Ge, since the distribution of nc-Ge in SiO_2 is not uniform, the MOS capacitance cannot be simply modeled by Eq. (5.1).

To model the MOS capacitance of the Ge-ion-implanted SiO_2 thin films, the information about the distribution of nc-Ge in the SiO_2 is required. That can be obtained from the simulation using the stopping and range of ions in matter (SRIM) program. As shown in Fig. 5-1, a low implant energy (i.e., 2 – 8 keV) leads to a partial distribution of nc-Ge in the SiO_2 near the metal gate, while a high implant energy (i.e., 16 keV) leads to a full distribution of nc-Ge in the SiO_2. The results of SRIM simulation are consistent with the actual Ge depth profiles obtained from the SIMS measurement (see Fig. 3-6). The SiO_2 with partial distribution of nc-Ge can be virtually divided into two regions: 1) the nc-Ge distributed region near the metal gate, and 2) the "pure SiO2" region near the *p*-Si substrate. As the implant energy increases, the nc-Ge distributed region expands while the "pure SiO_2" region becomes narrower. For the SiO_2 with a full distribution of nc-Ge, there is no "pure SiO_2" region and the nc-Ge particles are distributed over the entire SiO_2.

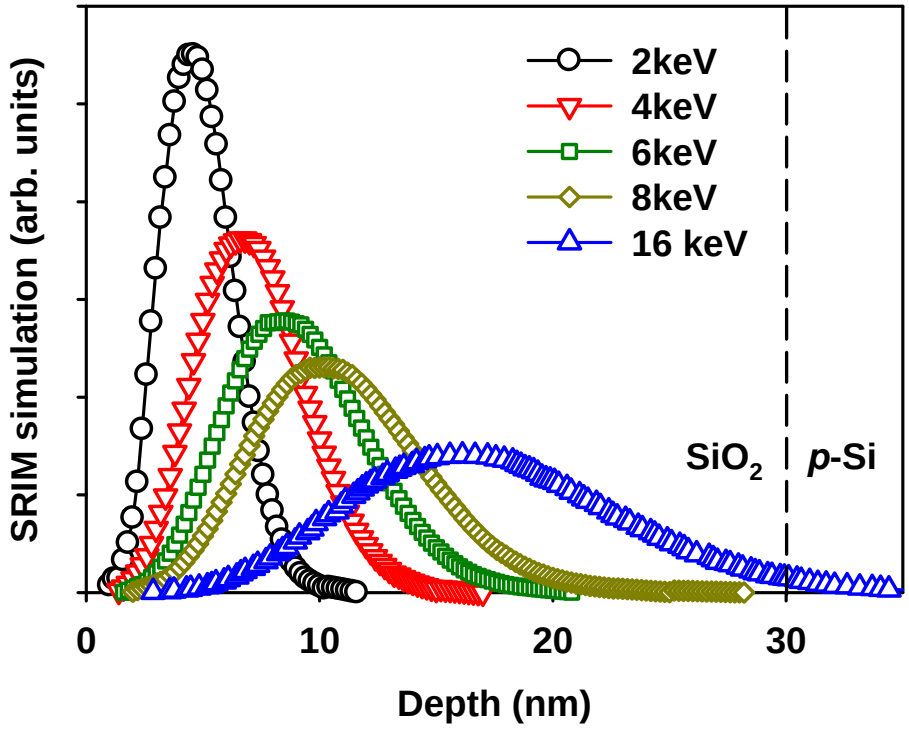

Fig. 5-1 SRIM simulation of the distribution of nc-Ge in the SiO_2 for different implant energies.

Based on the SRIM simulation, the depth distribution of the volume fraction of nc-Ge in SiO_2 can be obtained. The volume fraction (f) at a given depth x can be expressed as

$$f(x) = \frac{Q_{\mathrm{DOSE}} I(x)}{N_{\mathrm{Ge}} \int_0^{d_{\mathrm{MAX}}} I(x)dx} \tag{5.2}$$

where Q_{DOSE} is the implant dose, $I(x)$ is the SRIM intensity, N_{Ge} is the atomic density of Ge (N_{Ge} = 4.42×10^{22} atoms/cm^3), and d_{MAX} is the maximum depth of the nc-Ge distributed region. In the case of the full distribution of nc-Ge in the SiO_2, d_{MAX} equals to the total SiO_2 thickness. Obviously, the volume fraction of nc-Ge in SiO_2

varies with the depth, because the distribution of the nc-Ge in the SiO_2 is not uniform. To calculate the effective dielectric constant of a given SiO_2 with the inclusion of nc-Ge, our approach is to divide the nc-Ge distributed region with a non-uniform distribution of nc-Ge into m sub-layers with an equal thickness of d_{MAX}/m for each sub-layer. Each sub-layer has a constant volume fraction of nc-Ge in SiO_2 and a constant dielectric constant. As the implant energy changes from 2 to 16 keV, the value of m increases from 7 to 20, resulting in an approximately constant d_{MAX}/m for each implant energy. For example, as shown in Fig. 5-2, for an implant energy of 4 keV (implant dose is 1×10^{16} cm^{-2}), the nc-Ge distributed region near the SiO_2 surface is ~ 17 nm and it can be divided into 10 sub-layers with a constant volume fraction within each sub-layer.

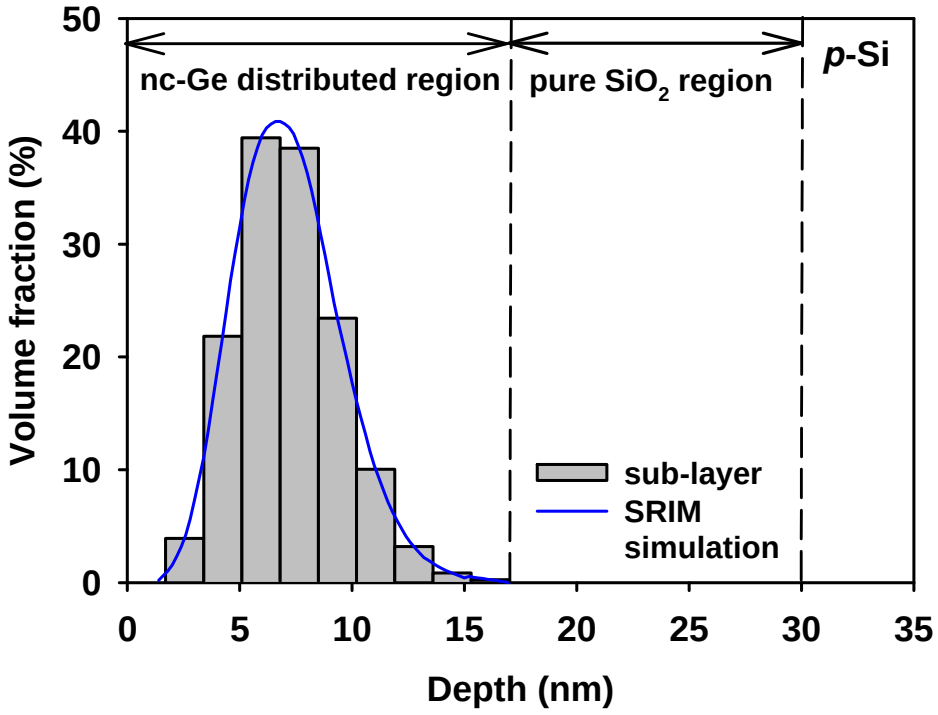

Fig. 5-2 A typical depth profile of volume fraction of nc-Ge in SiO_2. The nc-Ge distributed region is divided into 10 sub-layers.

Since each sub-layer can be treated as an effective medium in which the SiO_2 is the host matrix and nc-Ge is an inclusion embedded in the SiO_2 matrix, the effective dielectric constant ε_i (i = 1, 2, …, m) of the i^{th} layer is related to the volume fraction f_i (i = 1, 2, …, m) by the Maxwell-Garnett effective medium approximation (EMA) as given by [151, 210, 241-243]

$$\frac{\varepsilon_i - \varepsilon_{\text{SiO}_2}}{\varepsilon_i + 2\varepsilon_{\text{SiO}_2}} = f_i \frac{\varepsilon_{\text{nc-Ge}} - \varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{nc-Ge}} + 2\varepsilon_{\text{SiO}_2}} \tag{5.3}$$

where $\varepsilon_{\text{SiO}_2}$ and $\varepsilon_{\text{nc-Ge}}$ are the dielectric constant of SiO_2 and nc-Ge, respectively. From Eq. (5.3), it is known that when $f_i = 0$ (i.e., pure SiO_2), ε_i is equal to $\varepsilon_{\text{SiO}_2}$. However, when $f_i > 0$ (i.e., SiO_2 embedded with nc-Ge), ε_i is always larger than $\varepsilon_{\text{SiO}_2}$, but smaller than $\varepsilon_{\text{nc-Ge}}$. In addition, it is known that the dielectric constant of a semiconductor nanocrystal decreases with the particle dimension [236-240]. Thus, the $\varepsilon_{\text{nc-Ge}}$ is different from the dielectric constant of the bulk crystalline Ge. The details of the $\varepsilon_{\text{nc-Ge}}$ used in the modeling of MOS capacitance will be discussed later.

With the calculated dielectric constant ε_i (i = 1, 2, …, m) for each sub-layer, the total MOS capacitance of the Ge-ion-implanted SiO_2 thin film containing nc-Ge at the accumulation region can be determined. For the implant energy of 2 – 8 keV which leads to a partial distribution of nc-Ge in the SiO_2 near the gate, the total MOS capacitance per unit area (C_{TOTAL}) is given by

$$\frac{1}{C_{\text{TOTAL}}} = \sum_{i=1}^{m} \left(\frac{\varepsilon_i \varepsilon_0}{d_{\text{MAX}}/m} \right)^{-1} + \left(\frac{\varepsilon_{\text{SiO}_2} \varepsilon_0}{T_{\text{OXIDE}} - d_{\text{MAX}}} \right)^{-1} \tag{5.4}$$

where T_{OXIDE} is the thickness of the entire SiO_2. On the other hand, for the implant energy of 16 keV which leads to a full distribution of nc-Ge in the SiO_2, C_{TOTAL} can be expressed as

$$\frac{1}{C_{\mathrm{TOTAL}}} = \sum_{i=1}^{m} \left(\frac{\varepsilon_{\mathrm{i}} \varepsilon_0}{T_{\mathrm{OXIDE}}/m} \right)^{-1} \tag{5.5}$$

Eq. (5.4) and (5.5) are only valid for the situation that the nc-Ge themselves are not charged or discharged by the small ac signal during the *C-V* measurement. The capacitance of a pure SiO_2 can also be represented by the extreme case of Eq. (5.4) or (5.5) when ε_{i} is equal to $\varepsilon_{\mathrm{SiO_2}}$ as a result of the zero volume fraction of nc-Ge in SiO_2. Since ε_{i} is always larger than $\varepsilon_{\mathrm{SiO_2}}$ for a non-zero volume fraction of nc-Ge in SiO_2, the modeling approach predicts that the capacitance of the MOS structure containing nc-Ge in the gate oxide is always larger than that of a pure SiO_2 with the same oxide thickness.

5.3 Experimental measurement of MOS capacitance

In order to verify the above modeling approach, it is necessary to experimentally measure the MOS capacitance of the Ge-ion-implanted SiO_2 thin films. The sample preparation began with the implantation of Ge ions into 30 nm thermally grown SiO_2 thin films at various energies and doses. The details of the implant conditions are summarized in Table 3. While the implant energy of 2 – 8 keV leads to a partial distribution of nc-Ge near the SiO_2 surface, the implant energy of 16 keV results in a full distribution of nc-Ge in the SiO_2. All of the samples were annealed at 800 ºC in N_2

ambient for 1 hour. The formation of nc-Ge in the SiO_2 has been confirmed by the TEM images shown in Section 3.4. The size of nc-Ge is ~ 4 – 5 nm. A pure SiO_2 sample without nc-Ge was also prepared. The Al gate electrodes (with a diameter of ~ 160 μm) and backside contact were deposited on each sample to form the MOS structure. The capacitance-voltage (*C-V*) measurement was performed at a frequency of 1 MHz using a Keithley 4200 Semiconductor Characterization System. The bias voltage during the *C-V* measurement was swept from –10 to 2 V, while the ac small signal level was set to 15 mV. To determine the capacitance per unit area, the pad size of each measured MOS structure was measured by an optical microscope.

Table 3 Summary of various implant conditions for the modeling of capacitance.

Group	**Label**	**Implant energy (keV)**	**Implant dose (cm^{-2})**
Group A (partial distribution)	Ge2-3E14	2	3×10^{14}
	Ge2-2E15		2×10^{15}
	Ge8-1E16		1×10^{16}
Group B (partial distribution)	Ge4-3E14	4	3×10^{14}
	Ge4-2E15		2×10^{15}
	Ge4-1E16		1×10^{16}
Group C (partial distribution)	Ge2-2E15	2	2×10^{15}
	Ge4-2E15	4	
	Ge6-2E15	6	
	Ge8-2E15	8	
Group D (full distribution)	Ge16-1E15	16	1×10^{15}
	Ge16-1E16		1×10^{16}
	Ge16-1.6E16		1.6×10^{16}

5.4 Results and discussions

5.4.1 *C-V* characteristics of MOS structures with and without nc-Ge

Fig. 5-3 shows the typical *C-V* characteristic of the MOS structure with nc-Ge embedded in the gate oxide (i.e., Ge4-1E16). The measured capacitance was converted to the capacitance per unit area using the actual pad size of the MOS structure. In the strong accumulation region, the MOS capacitance per unit area is 111.27 nF/cm^2. The *C-V* characteristic of the pure SiO_2 with the same oxide thickness is also shown in Fig. 5-3. The MOS capacitance per unit area under strong accumulation is 102.34 nF/cm^2. Apparently, the inclusion of nc-Ge in the SiO_2 leads to an increase in the MOS capacitance per unit area under strong accumulation. That agrees with the prediction that the capacitance of the MOS structure containing nc-Ge in the gate oxide is always larger than that of a pure SiO_2 with the same oxide thickness. Indeed, all MOS structures embedded with nc-Ge show larger MOS capacitances under the accumulation condition as compared to the pure SiO_2. These measured capacitance values will be compared to the calculated MOS capacitance using the aforementioned approach. Besides, in Fig. 5-3, the flat-band voltage of the structure with nc-Ge is more negative than that of a pure SiO_2. That is due to the initial positive charges induced by the Ge ion implantation into the SiO_2 [204].

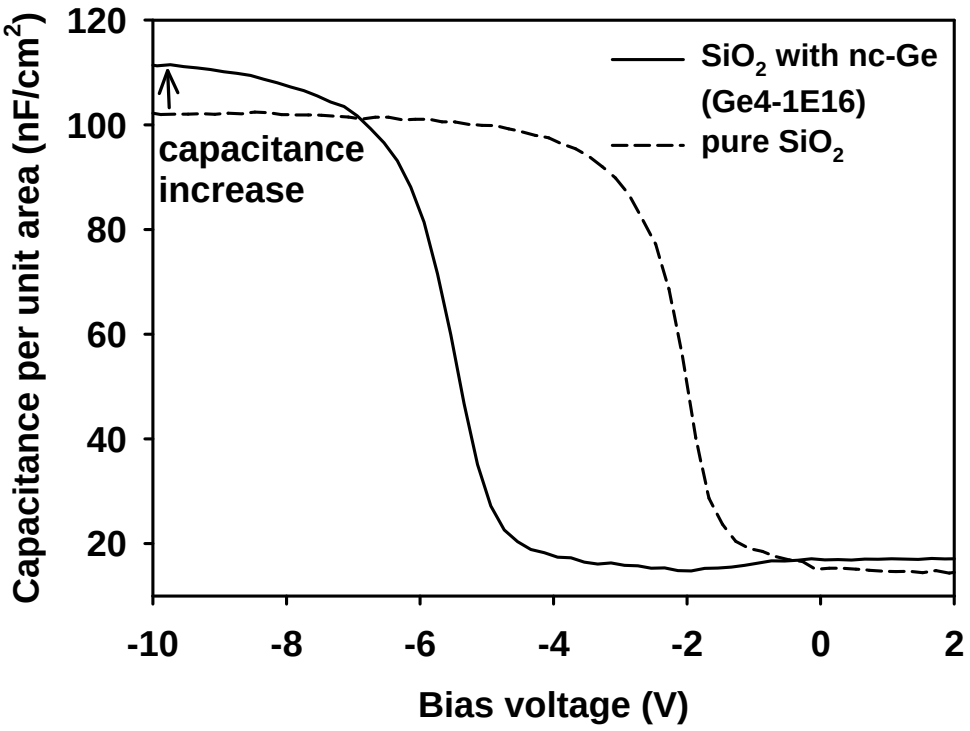

Fig. 5-3 Comparison of *C-V* characteristics between MOS structures with and without nc-Ge.

5.4.2 Static dielectric constant of nc-Ge

For a semiconductor nanocrystal, the reduction of its dielectric constant with the size has been demonstrated by several calculations [236-240]. Such a phenomenon is often attributed to the bandgap increase inside the nanocrystal. However, Delerue *et al.* demonstrated that the dielectric suppression is due to the breaking of polarizable bonds at the surface, instead of the increase of bandgap induced by the confinement [238]. Sun *et al.* proposed that the dielectric suppression originates from the enhancement of the crystal field due to surface bond contraction and the rise of the surface-volume ratio with decreasing particle size [240]. Although the origin of the

dielectric suppression is still under debate, the reduced dielectric constant can increase the Coulomb interaction between electrons, holes, and ionized shallow impurities in nano-scale devices [238]. During the calculation of the capacitance of a MOS structure with nc-Ge embedded in SiO_2, the dielectric constant of nc-Ge, $\varepsilon_{\mathrm{nc-Ge}}$, is one of the important parameters. As discussed previously in Section 5.2, for a given distribution of nc-Ge in SiO_2, the volume fraction of nc-Ge in each sub-layer is known. Thus, the dielectric constant of each sub-layer can be determined by Eq. (5.3), and the MOS capacitance can be calculated by Eq. (5.4) or (5.5). Due to the nanometer size of the nc-Ge, the $\varepsilon_{\mathrm{nc-Ge}}$ in Eq. (5.3) is different from the dielectric constant of bulk crystalline Ge. For a successful calculation of the MOS capacitance, it is necessary to know the $\varepsilon_{\mathrm{nc-Ge}}$ corresponding to the nanometer size of the nc-Ge.

Fig. 5-4 shows the calculated MOS capacitance as a function of $\varepsilon_{\mathrm{nc-Ge}}$ for the partial distribution of nc-Ge in SiO_2 fabricated by an implant energy of 4 keV and a dose of 1×10^{16} cm^{-2} (i.e., the Ge4-1E16 sample). It can be observed that the calculated MOS capacitance reduces with $\varepsilon_{\mathrm{nc-Ge}}$. Since the reduction in $\varepsilon_{\mathrm{nc-Ge}}$ is due to the reduction in the nc-Ge dimension, the result indicates that for a smaller nc-Ge, the calculated MOS capacitance becomes smaller. Based on the measured MOS capacitance per unit area of the Ge4-1E16 sample under the strong accumulation condition, the $\varepsilon_{\mathrm{nc-Ge}}$ can be determined from the calculated relationship between the MOS capacitance and the $\varepsilon_{\mathrm{nc-Ge}}$. As shown in Fig. 5-4, the measured capacitance per unit area is 111.27 nF/cm^2, corresponding to $\varepsilon_{\mathrm{nc-Ge}}$ = 14.78 for the nc-Ge embedded in SiO_2 of the Ge4-1E16 sample. The $\varepsilon_{\mathrm{nc-Ge}}$ is smaller than the bulk value of 16.2, since the size of nc-Ge is ~ 4 – 5 nm as determined from the TEM image in Fig. 4-1(b).

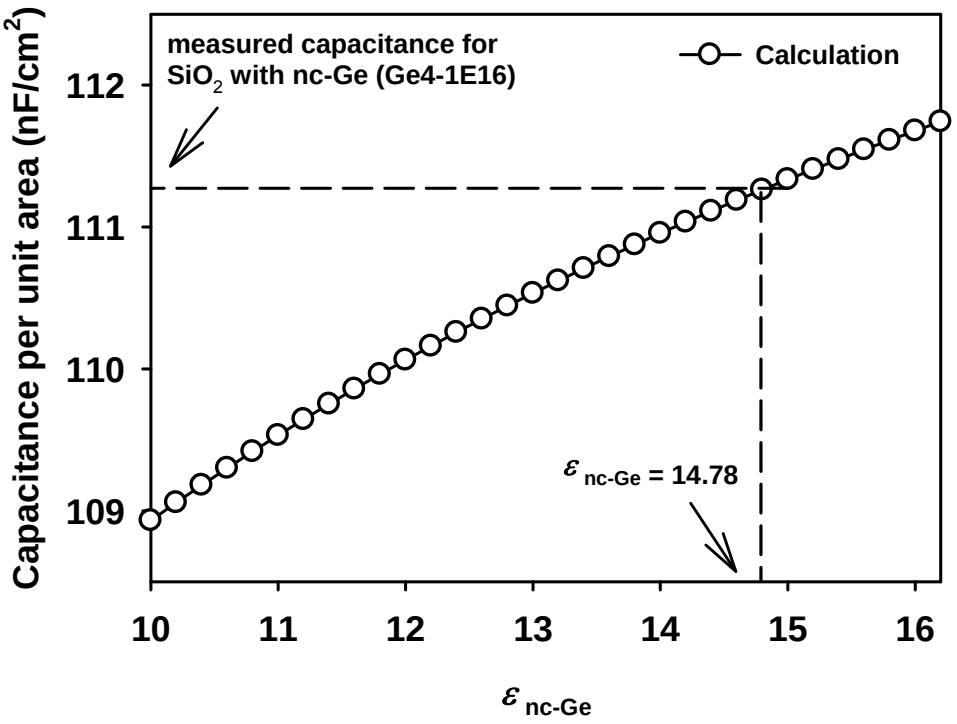

Fig. 5-4 Calculated MOS capacitance as a function of $\varepsilon_{\text{nc-Ge}}$ for the Ge4-1E16 sample. Based on the measured MOS capacitance, the $\varepsilon_{\text{nc-Ge}}$ corresponding to the nc-Ge embedded in SiO_2 of the Ge4-1E16 sample can be estimated.

The obtained $\varepsilon_{\text{nc-Ge}}$ can be compared to the theoretical calculation based on a modified Penn model which takes into account the quantum confinement effect induced discrete energy states [236]. Based on this model, for a given nanocrystal with a sphere radius of a, the size-dependence dielectric constant $\varepsilon_{\text{NC}}(a)$ can be expressed as

$$\varepsilon_{\text{NC}}(a) = 1 + \frac{\varepsilon_{\text{BULK}} - 1}{1 + \left(\frac{\pi\hbar^2 k_{\text{F}}}{2mE_g}\frac{1}{a}\right)^2} \tag{5.6}$$

where $\varepsilon_{\mathrm{BULK}}$ is the bulk dielectric constant, $\hbar$ is the reduced Planck constant, m is the free electron mass, E_g is the energy gap which is a fitting parameter in the original Penn model [244], and k_{F} is the valence Fermi momentum which is related to the concentration of valence electrons by [245]

$$n_0 = \frac{{k_{\mathrm{F}}}^3}{3\pi^2} \tag{5.7}$$

For the case of nc-Ge, E_g equals to 3.4 eV based on the optical constants of Ge [246], k_{F} can be calculated using Eq. (5.7) with the valence electron concentration of $4\times4.42\times10^{22}$ cm^{-3}, and $\varepsilon_{\mathrm{BULK}}$ is 16.2. Thus, the theoretical prediction of $\varepsilon_{\mathrm{nc-Ge}}$ for a given nc-Ge size can be obtained from Eq. (5.6). For a nc-Ge with a radius of ~ 2 nm as observed in the TEM image, the $\varepsilon_{\mathrm{nc-Ge}}$ can be calculated as 14.90. This number is in good agreement with the $\varepsilon_{\mathrm{nc-Ge}}$ = 14.78 which is extracted from Fig. 5-4 for the nc-Ge embedded in SiO_2. It should be noted that the modified Penn model is a simple calculation of one oscillator in a quantum-confinement situation. Other approaches, including the empirical pseudopotential calculation [237] and the self-consistent linear screening calculation [247], have also been reported for the modeling of the size-dependent dielectric constant. It has been shown that the modified Penn model can nicely describe the experimental data and is consistent with other complicated approaches [236]. Although the foundation of this simple calculation is still under debate, the modified Penn model servers as an effective mean to indicate the reasonable accuracy of our extracted $\varepsilon_{\mathrm{nc-Ge}}$.

The effective dielectric constant of the SiO_2 embedded with nc-Ge is different from that of a pure SiO_2. Based on the extracted value of $\varepsilon_{\mathrm{nc-Ge}}$ and the depth profile of the nc-Ge volume fraction in SiO_2, the depth profile of the effective dielectric constant can be calculated. Fig. 5-5 shows the calculated effective dielectric constant as a function of the depth in the 30 nm SiO_2. For the partial distribution of nc-Ge in SiO_2, as shown in Fig. 5-5(a), the peak effective dielectric constant in the nc-Ge distributed region is ~ 6.8, which is much larger than the dielectric constant of a pure SiO_2 ($\varepsilon_{\mathrm{SiO_2}}$ = 3.9). Besides, for the case of a full distribution of nc-Ge in SiO_2, as shown in Fig. 5-5(b), the peak dielectric constant is also larger than the dielectric constant of a pure SiO_2 by ~ 1. Thus, it can be known that as compared to a pure SiO_2 with the same thickness, the increase in the MOS capacitance of the SiO_2 embedded with nc-Ge is a consequence of the increase in the effective dielectric constant.

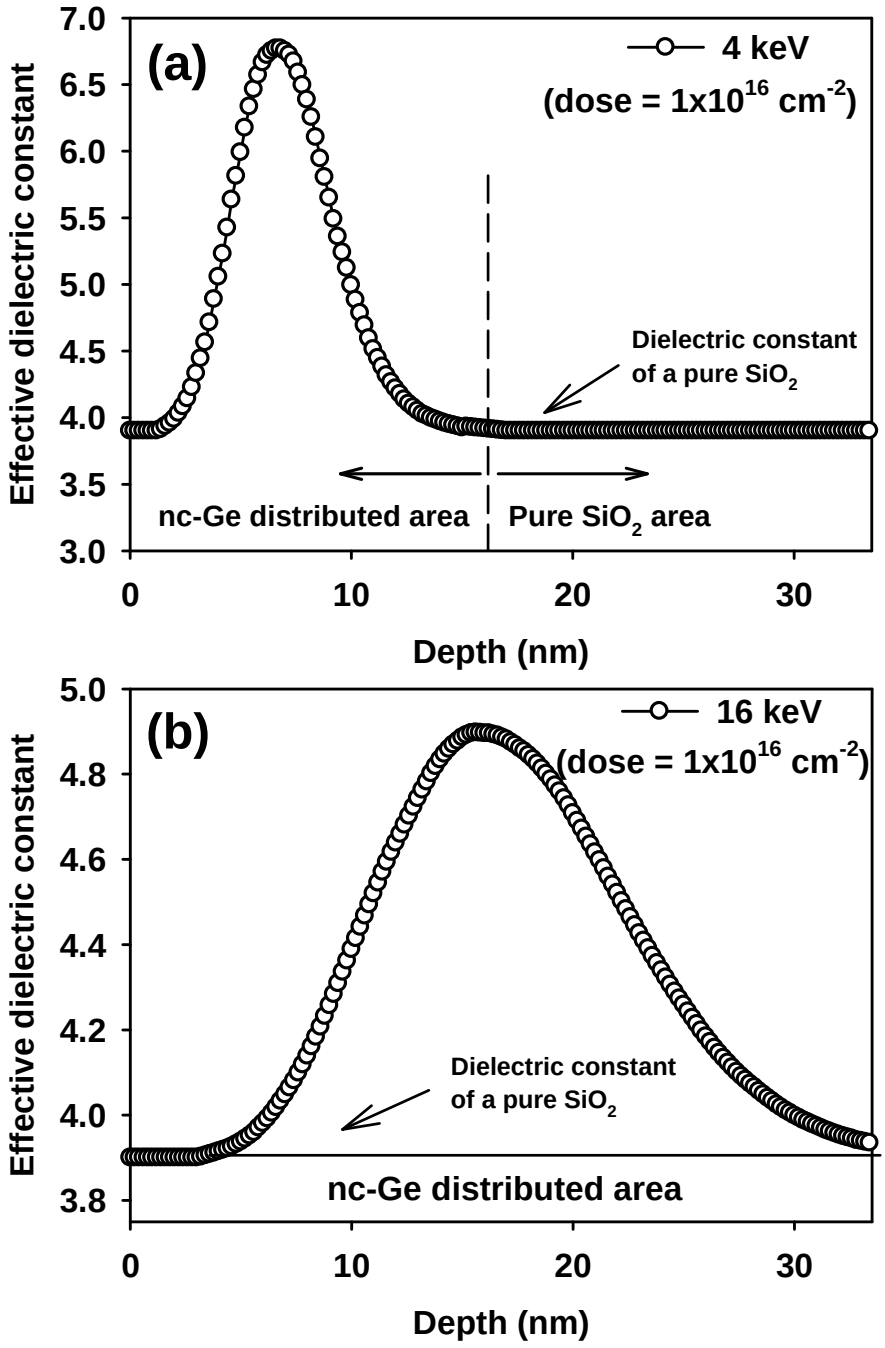

Fig. 5-5 Depth distribution of the effective dielectric constant of SiO_2 embedded with nc-Ge: (a) partial distribution of nc-Ge near the SiO_2 surface under the implant energy of 4 keV, and (b) full distribution of nc-Ge under the implant energy of 16 keV.

5.4.3 Influence of implant energy and dose on MOS capacitance

In the approach to model the MOS capacitance of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge, the implant energy and dose are explicitly taken into account. As described in Section 5.2, the implant energy determines the depth and distribution of the nc-Ge in SiO_2, which can be simulated by the SRIM program. On the other hand, the implant dose determines the concentration of nc-Ge in SiO_2, which is reflected in Eq. (5.2) as the volume fraction of nc-Ge in SiO_2. Thus, the influence of implant energy and dose on the calculated MOS capacitance can be obtained for a constant gate oxide thickness. Since no significant change in the nc-Ge size with the implant conditions is observed, the value of $\varepsilon_{\mathrm{nc-Ge}}$ was fixed at 14.78 during the calculation.

Fig. 5-6 shows the calculated MOS capacitance as a function of the implant energy. The influence of the implant energy is most prominent for the case of a high implant dose, i.e., 1×10^{16} cm^{-2}, which leads to a maximum of ~ 10% increase in the MOS capacitance as compared to the capacitance of a pure SiO_2. As the implant energy increases from 2 to 12 keV, the thickness (d_{MAX}) of the nc-Ge distributed region increases, and the thickness of the pure SiO_2 region reduces. As a result, the capacitance per unit area increases with the implant energy. However, further increase in the implant energy (i.e., from 12 – 20 keV) results in a full distribution of nc-Ge in the SiO_2, and some Ge ions are implanted in the Si substrate. As the implant energy increases, the nc-Ge distributed region does not vary with the implant energy (i.e., the thickness of the nc-Ge distributed region equals the total SiO_2 thickness), but the nc-Ge volume fraction reduces because more Ge ions are implanted into the Si substrate.

As a result, the calculated MOS capacitance per unit area becomes saturated and then reduces with implant energy for the full distribution of nc-Ge in SiO_2. For the case of a low implant dose (i.e., 2×10^{15} cm^{-2} and 3×10^{14} cm^{-2}), the effect of the implant energy on the MOS capacitance per unit area is small. Hence, in Fig. 5-6, no obvious dependence of MOS capacitance on the implant energy can be observed.

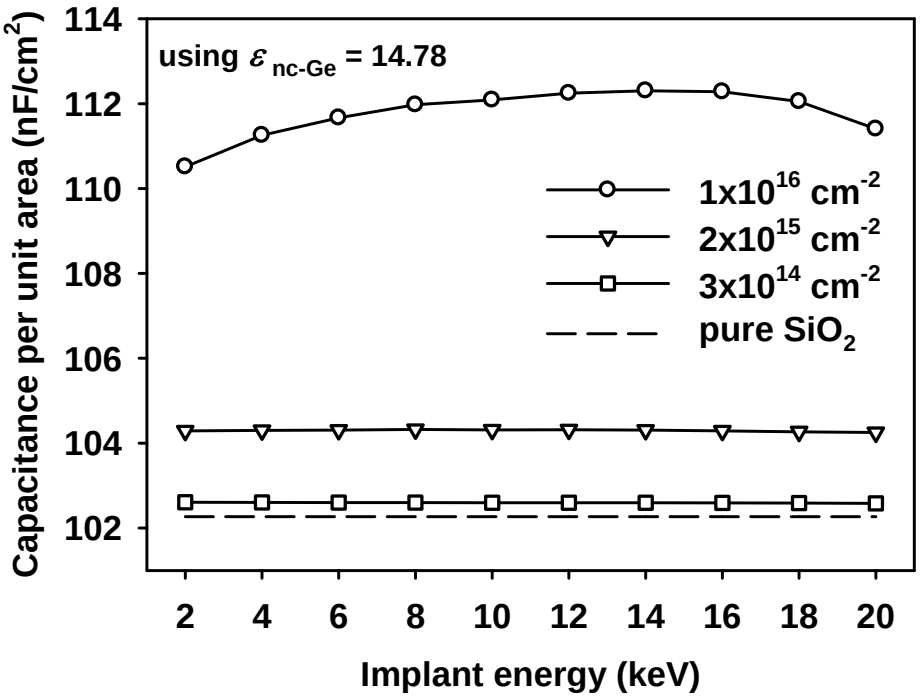

Fig. 5-6 Influence of the implant energy on the calculated MOS capacitance.

Fig. 5-7 shows the calculated MOS capacitance as a function of the implant dose for a constant implant energy of 4 keV. It can be observed that the calculated MOS capacitance per unit area increases with the implant dose. This is due to the increase of the effective dielectric constant as a result of the increase in the nc-Ge volume fraction with the dose.

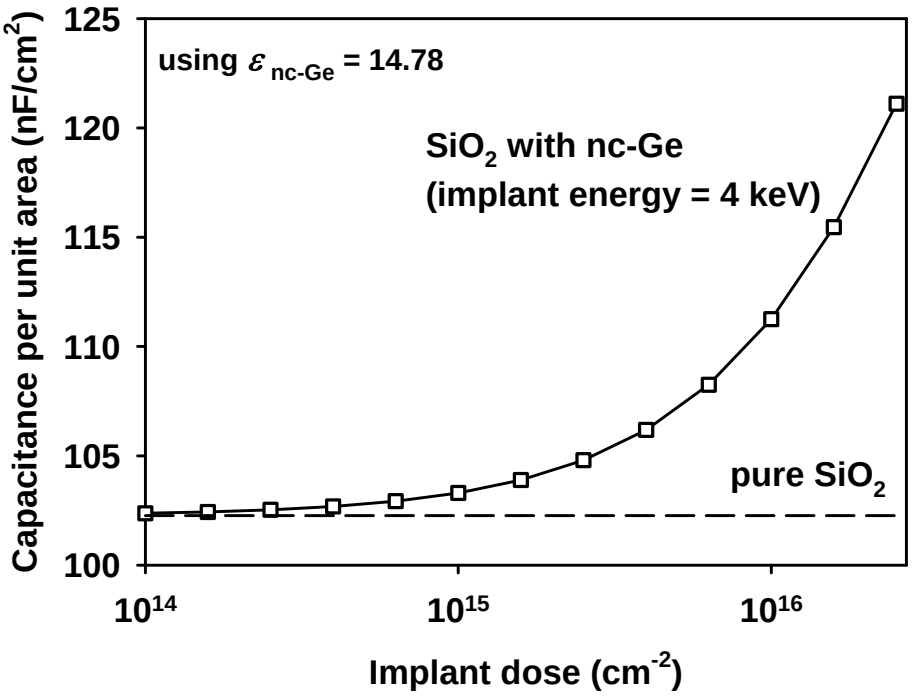

Fig. 5-7 Influence of the implant dose on the calculated MOS capacitance.

The relationship between the calculated MOS capacitance and the volume fraction of nc-Ge in SiO_2 is shown in Fig. 5-8. Based on Eq. (5.2), it can be known that for a given implant condition, the volume fraction of the nc-Ge in SiO_2 is not a constant. Instead, the volume fraction follows a Gaussian distribution, as shown in Fig. 5-2. The peak volume fraction is determined by the implant dose and the distribution of the implanted Ge ions in SiO_2. As shown in Fig. 5-8, for a constant implant energy, the calculated MOS capacitance increases with the peak volume fraction as a result of the increased effective dielectric constant. As the implant energy increases, the MOS capacitance corresponding to a given volume fraction also increases. That is due to the higher dose used to achieve the same peak volume fraction.

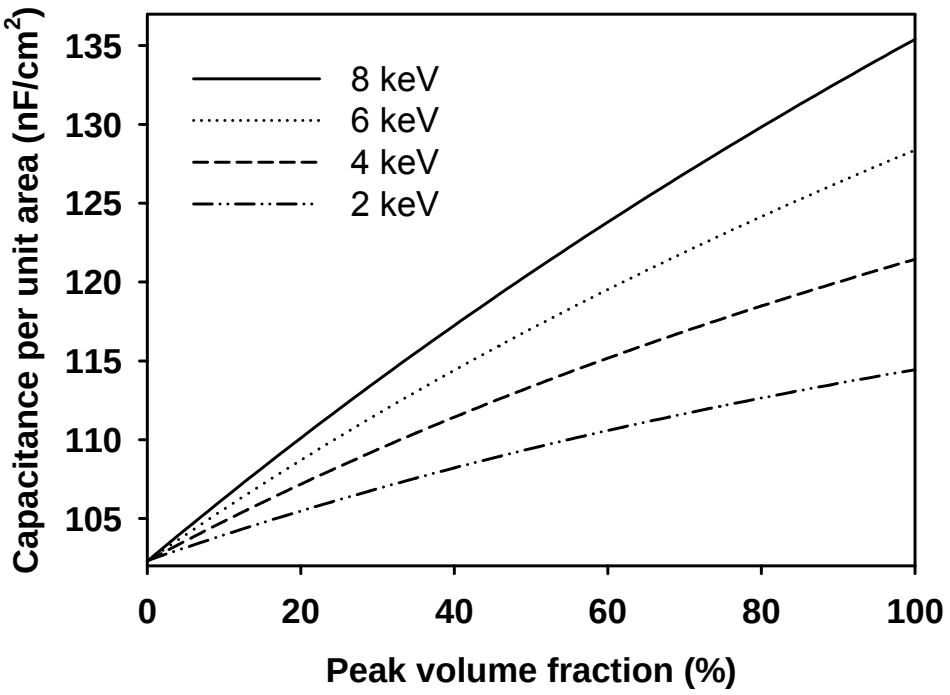

Fig. 5-8 Calculated MOS capacitance as a function of the peak volume fraction of the nc-Ge in SiO_2 for different implant energies.

5.4.4 Comparison between calculated and measured MOS capacitances

To verify the modeling approach as described in Section 5.2 as well as to confirm the correctness of using $\varepsilon_{\mathrm{nc-Ge}}$ = 14.78 during the calculation, the MOS capacitances of the Ge-ion-implanted SiO_2 thin films under various implanted conditions were measured under strong accumulation conditions. The details of the measurements have been described previously in Section 5.3. The comparison between the calculation using $\varepsilon_{\mathrm{nc-Ge}}$ = 14.78 and the measurement is shown in Table 4. An excellent agreement between the calculated and measured MOS capacitances can be observed for each distribution.

Table 4 Comparison between calculated and measured MOS capacitances for samples with various implant conditions.

Group	Label	Implant energy (keV)	Implant dose (cm^{-2})	Calculated capacitance (nF/cm^2)	Measured capacitance (nF/cm^2)
Group A (partial distribution)	Ge2-3E14	2	3×10^{14}	102.6067	102.6343
	Ge2-2E15		2×10^{15}	104.2892	104.2048
	Ge8-1E16		1×10^{16}	110.5127	110.6044
Group B (partial distribution)	Ge4-3E14	4	3×10^{14}	102.6009	102.6790
	Ge4-2E15		2×10^{15}	104.3000	104.2098
	Ge4-1E16		1×10^{16}	111.2534	111.2735
Group C (partial distribution)	Ge2-2E15	2	2×10^{15}	104.2892	104.2048
	Ge4-2E15	4		104.3000	104.2098
	Ge6-2E15	6		104.3080	104.2632
	Ge8-2E15	8		104.3206	104.3779
Group D (full distribution)	Ge16-1E15	16	1×10^{15}	103.2794	102.9394
	Ge16-1E16		1×10^{16}	112.2821	112.3406
	Ge16-1.6E16		1.6×10^{16}	118.0468	118.1142

In Fig. 5-9, the measured MOS capacitances are compared with the calculation using $\varepsilon_{\mathrm{nc-Ge}}$ = 16.2 (i.e., dielectric constant of the bulk crystalline Ge) and $\varepsilon_{\mathrm{nc-Ge}}$= 14.78 for various implant energies. Obviously, $\varepsilon_{\mathrm{nc-Ge}}$= 14.78 yields an excellent agreement between the calculation and the measurement. For $\varepsilon_{\mathrm{nc-Ge}}$ = 16.2, the calculated MOS capacitance is larger than the measured value. The result indicates that the modeling approach using $\varepsilon_{\mathrm{nc-Ge}}$ = 14.78 which corresponds to the nc-Ge size of ~ 4 – 5 nm is reliable and accurate.

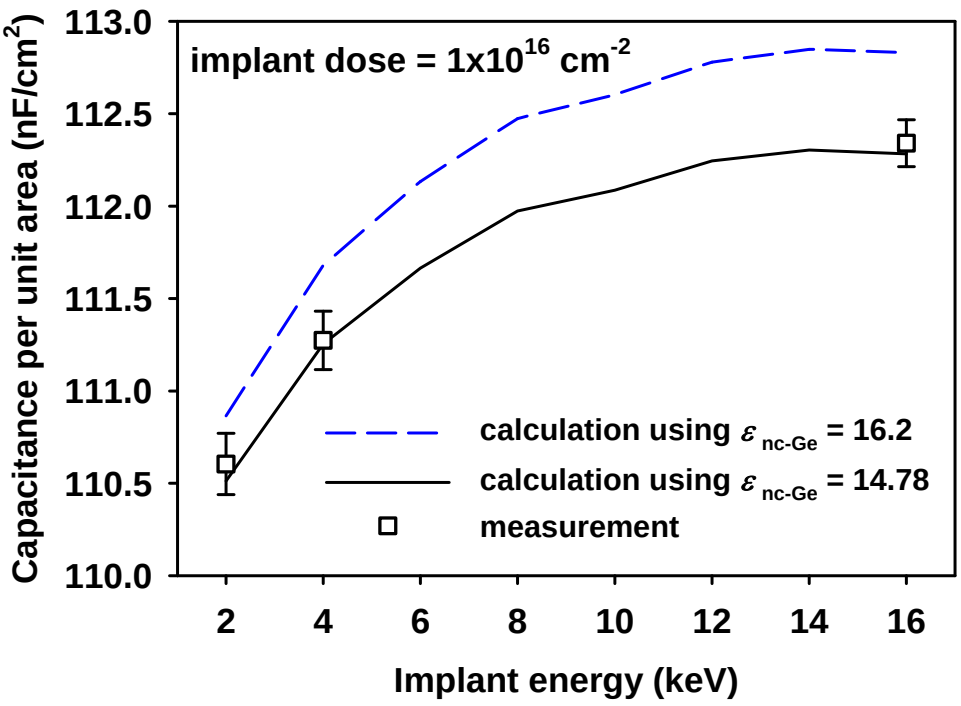

Fig. 5-9 Calculated MOS capacitance using $\varepsilon_{nc\text{-}Ge}$ = 16.2 (i.e., dielectric constant of the bulk crystalline Ge) and $\varepsilon_{nc\text{-}Ge}$ = 14.78 as a function of the implant energy. The measured MOS capacitance is consistent with the calculation using $\varepsilon_{nc\text{-}Ge}$ = 14.78.

5.5 Conclusion

A modeling approach to calculate the MOS capacitance of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been presented in this chapter. In this approach, the nc-Ge distributed region is divided into several sub-layers, and the effective dielectric constant for each sub-layer is calculated using the Maxwell-Garnett EMA. Both the distribution of nc-Ge in SiO_2 and the reduced dielectric constant corresponding to the nanometer size of nc-Ge have been considered during the calculation. Using this approach, the influence of implant energy and dose on the

MOS capacitance has been investigated, and the static dielectric constant of nc-Ge embedded in SiO_2 has been determined. The calculated capacitances for various nc-Ge distributions have been compared with the measurement results. Good agreement between the calculated and measured MOS capacitances has been achieved.

Chapter 6 Electroluminescence from Ge-ion-implanted SiO_2 Thin Films

6.1 Introduction

The development of communication technology has created a high demand for optoelectronic devices able to generate, modulate and process optical signals and to be integrated with mainstream Si-based microelectronic circuits [51]. Although light-emitting devices based on compound semiconductor materials have been well established, their integration with Si-based microelectronic circuits remains a challenge. Although Si and Ge are known to be poor light emitting materials due to their indirect bandgap, the discovery of visible photoluminescence (PL) from porous Si [248] has inspired a large research effort to investigate light-emitting devices based on Si or Ge nanostructures. In particular, SiO_2 with embedded Ge nanocrystals (nc-Ge) has undergone extensive studies because such films exhibit visible PL and electroluminescence (EL) [50, 52, 54, 66, 98, 163]. Among the various techniques for fabricating luminescent SiO_2 thin films embedded with nc-Ge, the ion implantation technique is quite promising because of its good control over the nc-Ge distribution and its full compatibility with mainstream Si technology [51].

In most of the previous studies about the EL from Ge-implanted SiO_2 films, the Ge ion implantation has been carried out at a high energy (75 - 350 keV) and the SiO_2

thickness is in the range of a few hundred nanometers [50-54]. However, for practical EL applications, a thinner Ge-implanted SiO_2 film is required to achieve a lower operation voltage, hence lower implant energy should be used. In addition, a proper understanding about the relationship between the EL and the ion implantation conditions, i.e., implant energy and dose, is essential for the design and integration of light-emitting devices based on the Ge ion implantation technique. Such a relationship has not yet been systematically investigated for the Ge-implanted SiO_2 thin films. In this chapter, low-energy (2 – 8 keV) Ge ion implantation is employed to synthesis the nc-Ge embedded in thin SiO_2 films (~ 30 nm). The light-emitting devices based on a structure of ITO / SiO_2 embedded with nc-Ge / *p*-Si substrate are fabricated. The EL properties of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge are investigated. The influences of the implant dose and energy on the EL behavior are also studied.

6.2 Sample fabrication and experimental details

6.2.1Sample fabrication

Ge ions were implanted into the thermally grown 30 nm SiO_2 thin films with various combinations of implant energy and dose. The details of the fabrication of Ge-ion-implanted SiO_2 thin films have been described previously in Section 3.3.1. As shown in Table 2, Group I samples have a constant implant dose of 2×10^{15} cm^{-2} but different implant energies ranging from 2 – 8 keV. On the other hand, Group II samples have the same implant energy of 4 keV, but different implant doses of 3×10^{14}, 2×10^{15} and 1×10^{16} cm^{-2}, respectively. To induce the formation of nc-Ge in the Ge-ion-

implanted SiO_2, all the samples were annealed at 800 ºC for 1 hour. Based on the Ge-ion-implanted SiO_2 thin films, the light-emitting devices with a structure of ITO / Ge-ion-implanted SiO_2 / *p*-Si substrate / Al backside contact were fabricated. The schematic diagram of the light-emitting device is shown in Fig. 6-1. The ITO electrodes with a radius of 1.2 mm and a thickness of 130 nm were deposited on the surface of the Ge-ion-implanted SiO_2 film through a hard shadow mask by sputtering. Because of its conductivity and high transparency over the visible to infrared range, the ITO film acts as both the gate electrode and the EL emission window. The wafer backside contact was formed by the deposition of a 250 nm Al layer using an e-beam evaporation system.

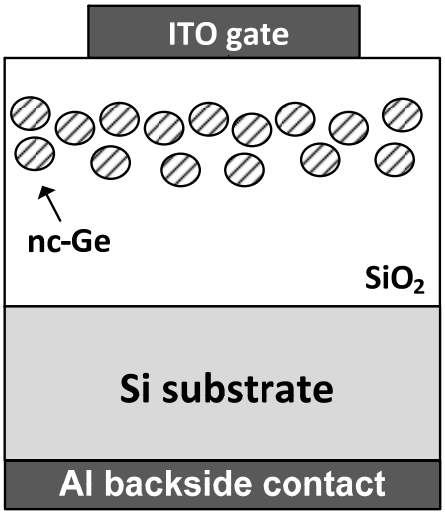

Fig. 6-1 Schematic diagram of the light-emitting device with a structure of ITO / Ge-ion-implanted SiO_2 / Si substrate / Al backside contact.

6.2.2 Electroluminescence characterization system

To study the EL properties from light emitting devices based on the Ge-ion-implanted SiO_2 thin films, an EL characterization system that is capable of applying

constant voltage / current onto the gate electrode and collecting the light emission from the same gate electrode is required. Fig. 6-2 illustrates the setup of such an EL characterization system.

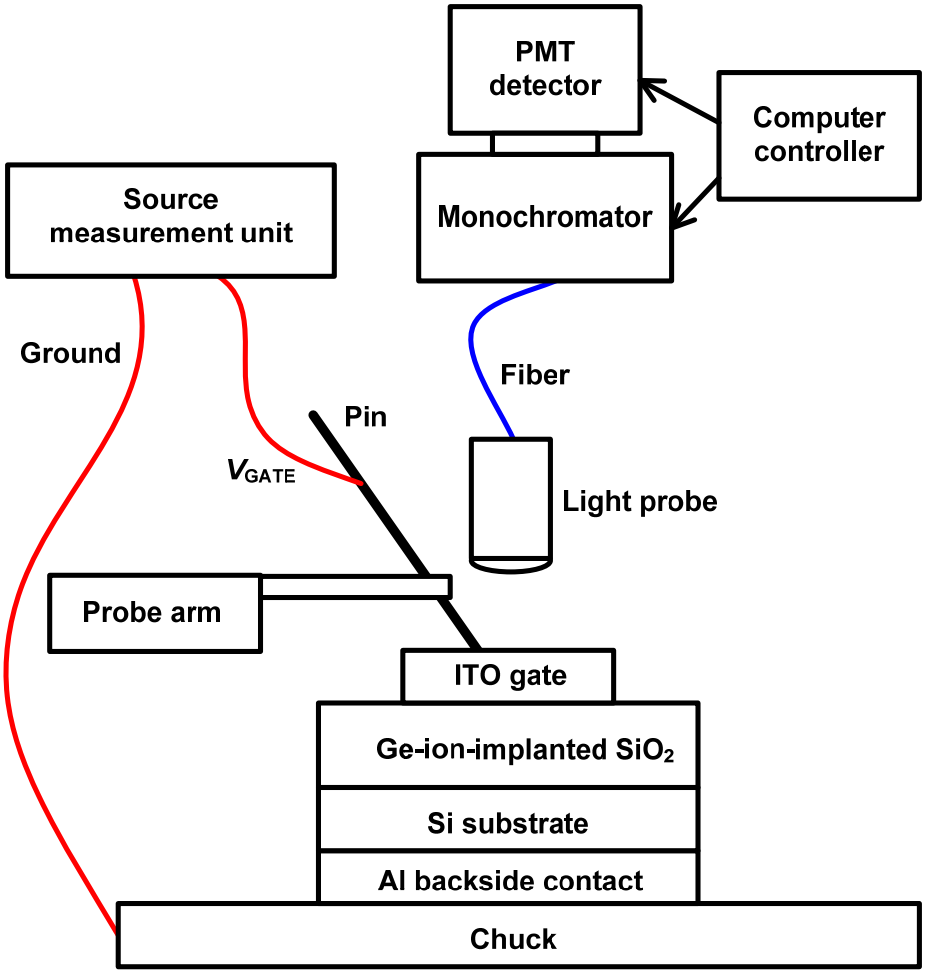

Fig. 6-2 Schematic diagram for the setup of an EL characterization system.

During the EL measurement, a Keithley 2400 source measurement unit (SMU) was used to apply voltage / current to the ITO gate of the light-emitting device via the probe arm of a probe station. The current-voltage characteristics of the light-emitting device were also measured by the Keithley 2400 SMU. On top of the light-emitting device, a light probe connected to a low-loss fiber was used to collect the emitted light

from the ITO gate. The spectrum of the light emission was then analyzed by a computer-controlled Dongwoo Optron DM150i monochromator (wavelength range: 185 – 1600 nm; resolution: 0.2 nm) equipped with a Dongwoo Optron PDS-1 photomultiplier tube (PMT) detector. The whole system was placed in a light-tight enclosure to avoid the influence of the ambient light.

6.3 Visible electroluminescence

In this section, the EL behavior of the light-emitting device based on a typical Ge-ion-implanted SiO_2 thin film containing nc-Ge near the SiO_2 surface is investigated. The EL spectra showing a yellow light emission are presented. The dependence of current transport and EL intensity on the applied gate voltage is discussed. Based on a Gaussian peak deconvolution of the EL spectra, the possible luminescence centers contributing to the EL are identified.

6.3.1 Structure of Ge-ion-implanted SiO_2 thin film

The typical Ge-ion-implanted SiO_2 thin film studied in this section was implanted with a dose of 2×10^{15} cm^{-2} at 6 keV, i.e., the Ge6-2E15 sample. As revealed by the SIMS depth profile in Fig. 6-3(a), the excess Ge atoms are distributed from the oxide surface to a depth of ~20 nm. The 30 nm Ge-ion-implanted SiO_2 thin film can be divided into the following two regions: 1) the excess-Ge-distributed region with a large amount of nc-Ge close to the ITO gate electrode; and 2) the "pure SiO_2" region without nc-Ge or with a very small amount of dissolved Ge atoms close to the Si

substrate. The formation of nc-Ge in the excess-Ge-distributed region near the SiO_2 surface can be confirmed by the TEM image shown in Fig. 6-3(b).

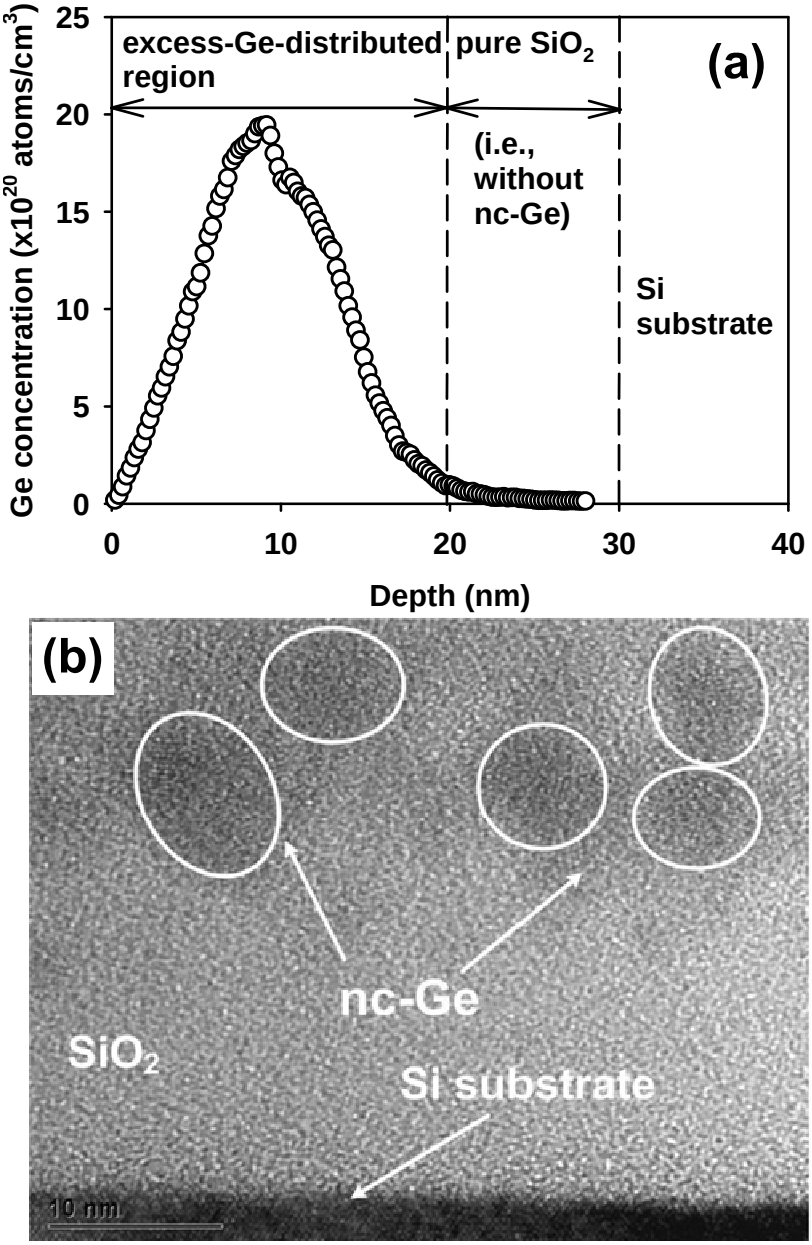

Fig. 6-3 (a) Distribution of implanted Ge in SiO_2 obtained from SIMS measurement for the annealed Ge6-2E15 sample, and (b) Cross-sectional TEM image of nc-Ge embedded in SiO_2 for the annealed Ge6-2E15 sample.

6.3.2 EL spectra

The light-emitting device based on the Ge-ion-implanted SiO_2 thin film exhibits a visible EL with a yellow color when a negative gate voltage (V_{GATE}) is applied to the ITO gate electrode. Fig. 6-4 shows typical EL spectra at different V_{GATE}. A broad EL band extending from 400 nm to 850 nm can be clearly observed, and the EL intensity becomes stronger as the magnitude of the negative V_{GATE} increases. The EL peak is located at ~ 600 nm (~ 2.1 eV). The EL emission is not measurable by our characterization system until the magnitude of the negative V_{GATE} is larger than 5 V. When the polarity of V_{GATE} is positive, no EL can be induced regardless of the magnitude of V_{GATE}. The EL cannot be due to the ITO gate electrode itself, because the light emission from the gate electrode usually happens as a result of the impact of hot electrons to the gate electrode biased with a positive gate voltage [249]. In our case, the ITO electrode was negatively biased to supply electrons during the EL measurement. Therefore, the Ge-ion-implanted SiO_2 thin film is responsible for the visible EL.

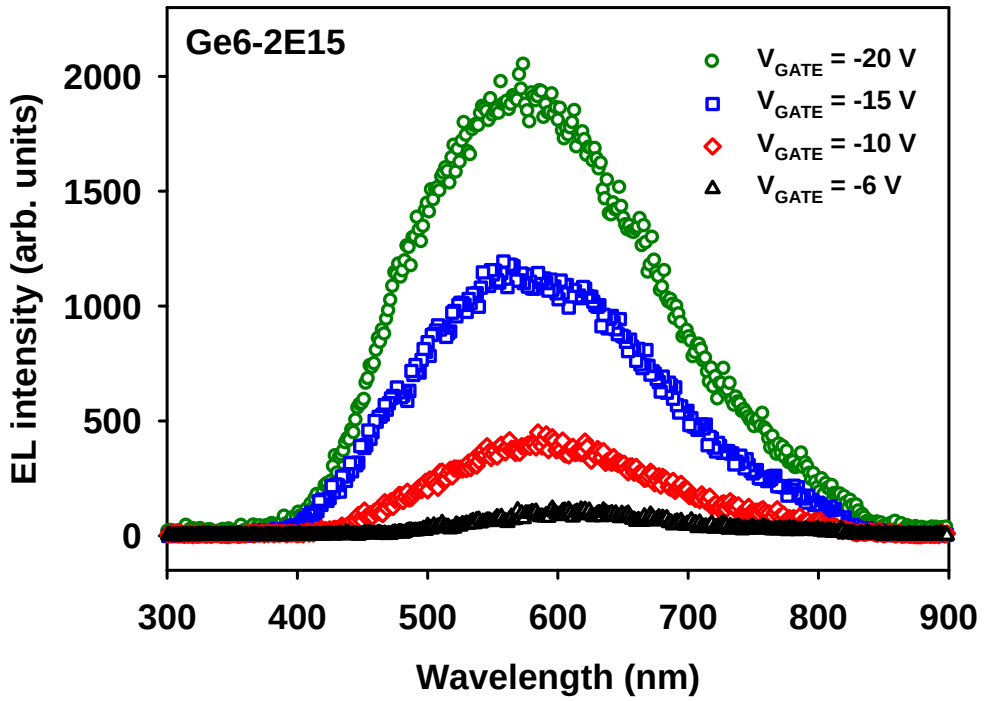

Fig. 6-4 Typical EL spectra obtained from the Ge-ion-implanted SiO_2 thin film (Ge6-2E15 sample annealed at 800 ºC for 1 hour) under different V_{GATE}.

6.3.3 Gate voltage dependence of gate current density and integrated EL intensity

The current conduction behavior of the light-emitting device based on a Ge-ion-implanted SiO_2 thin film was studied using the *I-V* measurement in order to understand the EL behavior. Fig. 6-5 shows the gate current density (J_{GATE}) as a function of the magnitude of the V_{GATE}. The curve fitting suggests that the J_{GATE} and V_{GATE} have a power-law relationship

$$J_{GATE} = \alpha_0 V_{GATE}{}^{\zeta} \tag{6.1}$$

where α_0 is a coefficient, and ζ is the scaling exponent. From the curve fitting, it is found that the scaling exponent $\zeta \approx 1.7$. The power-law behavior of current transport has been reported for arrays of small metallic dots [250] and metal nanocrystal arrays [251]. The value of the scaling exponent ($\zeta \approx 1.7$) is within the range of 1.66 to 2.26 for a two-dimensional (2-D) array of quantum dots [250, 251]. Note that ζ is affected by the concentration and distribution of nanocrystals as well as the charge trapping in the nanocrystals [252, 253]. In particular, ζ could be changed by the application of a voltage or even an *I-V* measurement itself due to the change in the charging state [252].

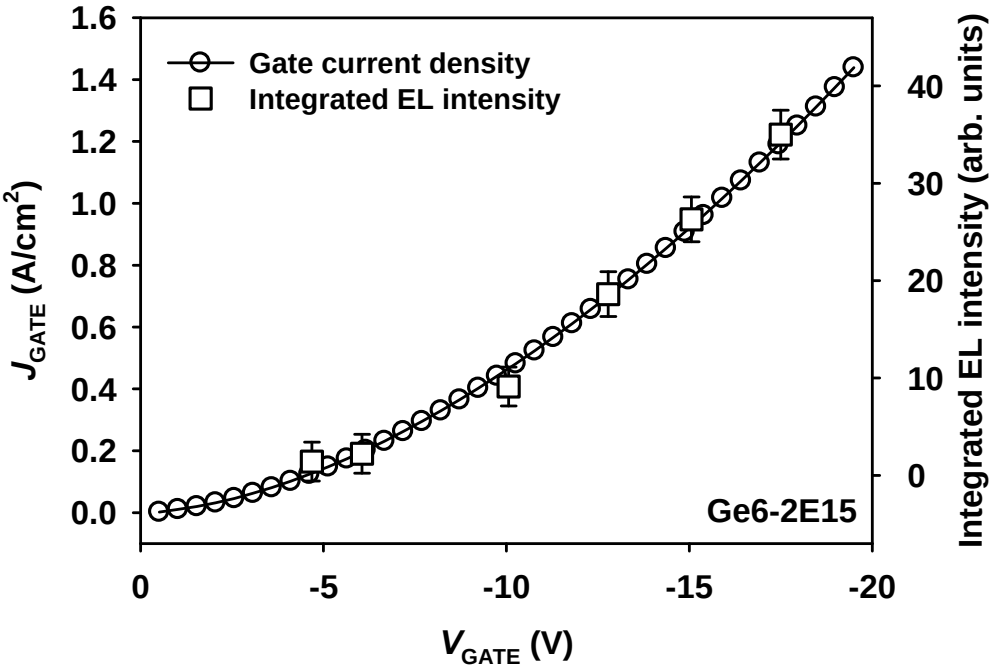

Fig. 6-5 Dependence of the gate current density (J_{GATE}) and the integrated EL intensity on the V_{GATE}.

When a negative V_{GATE} is applied, electrons are injected into the Ge-ion-implanted SiO_2 thin film from the ITO gate, while holes are injected into the Ge-ion-

implanted SiO_2 thin film from the *p*-type Si substrate. The current conduction behavior can be explained as follows. As shown previously by the SIMS results in Fig. 6-3(a), the Ge-ion-implanted SiO_2 thin film can be divided into the excess-Ge-distributed SiO_2 region near the ITO gate and the "pure SiO_2" region (i.e., tunneling oxide) near the Si substrate. Both the current conduction in the excess-Ge-distributed region and the tunnel current through the "pure SiO_2" play roles in the current transport. For the range of V_{GATE} required for the measurable EL emission, the current transport is mainly limited by the conduction in the excess-Ge-distributed region, because the carriers can be easily transported through the 10 nm "pure SiO_2" region by tunneling. The transport of carriers in the excess-Ge-distributed SiO_2 region can be explained by the percolation concept [252, 254]. Similar to the situation of the tunneling paths formed by neutral oxide traps in SiO_2 thin films [254], conductive paths can be formed by the tunneling of carriers between adjacent implantation-induced defects or nc-Ge in the excess-Ge-distributed SiO_2 region. With the presence of many implantation-induced defects or nc-Ge, a network of conductive paths is formed in the excess-Ge-distributed region, leading to the observed power-law behavior.

The integrated EL intensity as a function of the magnitude of the V_{GATE} is also shown in Fig. 6-5. As can be observed from the figure, the dependence of the EL intensity on the V_{GATE} also follows a power-law which has the same trend as that of the current transport, showing a linear relationship between the current transport and the EL intensity. The result indicates that the light emission is directly related to the carrier transport in the thin film rather than in the ITO gate or at the interface between

the ITO gate (or the *p*-Si substrate) and the thin film. Since both the injected electrons and holes move along tunneling paths in the excess-Ge-distributed SiO_2, radiative recombination of the injected electrons with the injected holes is likely to occur along the conduction paths via some luminescence centers. This explains why the current transport and the EL intensity have a similar power-law dependence on the applied V_{GATE}. The result also implies that, both the current transport and the luminescence centers contributing to the EL could be associated with the implantation-induced defects and nc-Ge, which form a network of conduction paths in the excess-Ge-distributed region.

6.3.4 EL mechanisms

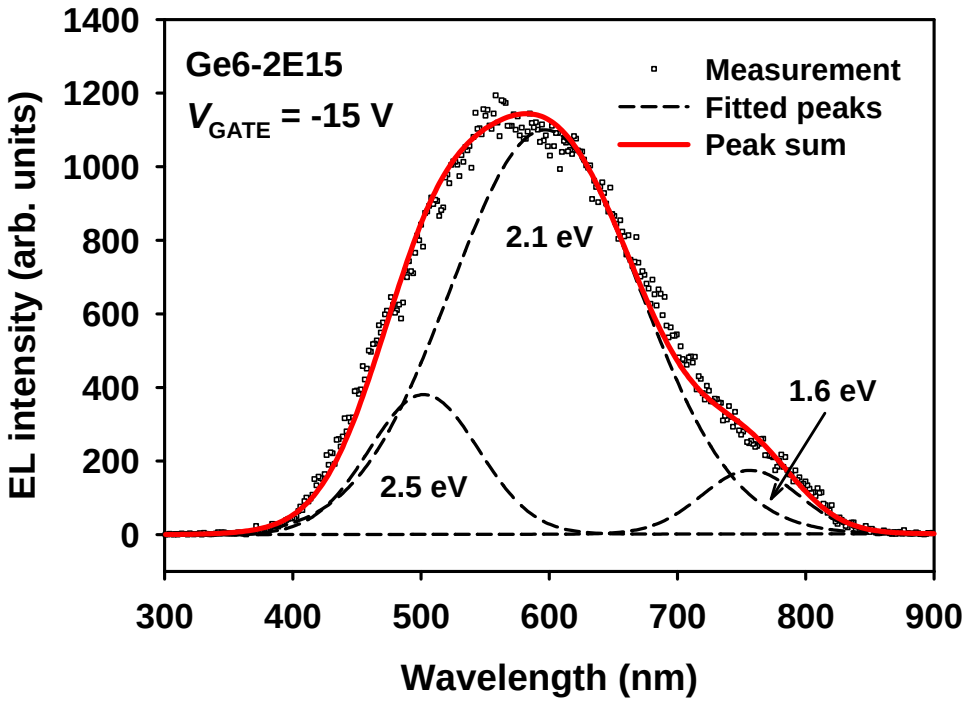

Fig. 6-6 A typical EL peak deconvolution for the annealed Ge6-2E15 sample under V_{GATE} = -15 V showing the contribution of three EL bands.

In order to understand the possible luminescence centers contributing to the EL from the Ge-ion-implanted SiO_2 thin film, a Gaussian peak deconvolution was performed on the EL spectra using a computer program (XPSPeak 4.1). Fig. 6-6 shows the typical Gaussian peak deconvolution of the EL spectrum for V_{GATE} = -15 V. It is found that the EL spectrum consists of three EL bands, including one dominant band at ~ 600 nm (2.1 eV) and two shoulder bands at ~ 500 nm (2.5 eV) and ~ 760 nm (1.6 eV). Fig. 6-7 showing the peak wavelengths of the three EL bands obtained at different V_{GATE}. The result indicates that the positions of the three EL bands are independent of the applied V_{GATE}.

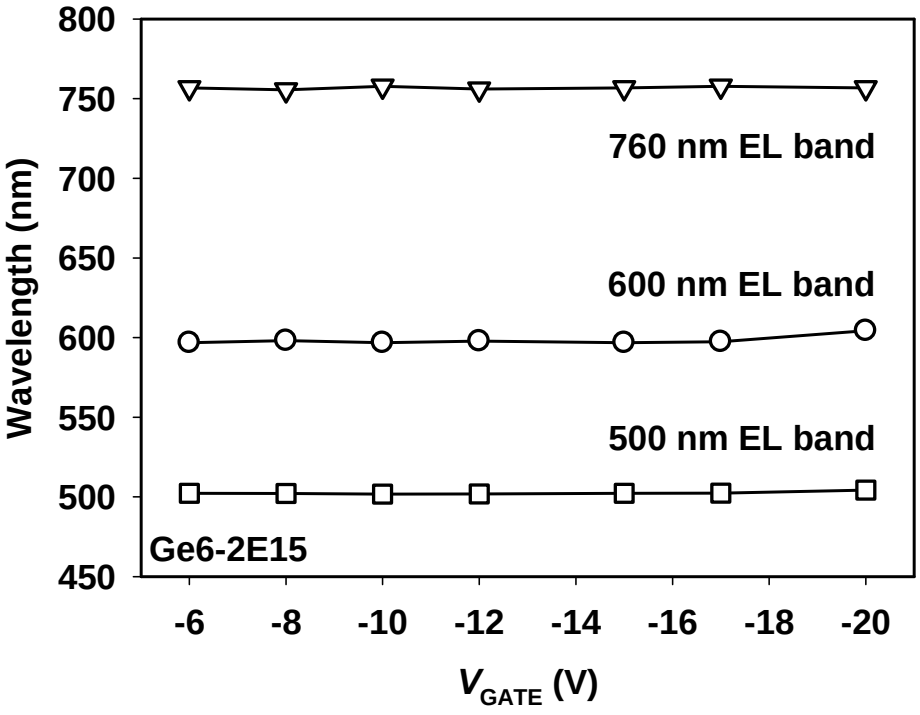

Fig. 6-7 Evolution of the peak wavelength of each EL band with the V_{GATE} for the annealed Ge6-2E15 sample.

The radiative recombination of electron-hole pairs at the luminescence centers located in the thin film is commonly used to describe the EL from the MOS-like light-emitting devices [50, 52, 255]. For the light-emitting device in this study, the visible EL can mainly be attributed to the radiative recombination of injected electrons and holes via the luminescence centers located in the excess-Ge-distributed region of the SiO_2 thin films implanted with low-energy Ge ions. These luminescence centers are basically defect states created during the ion implantation [51]. The dominant EL band at ~ 600 nm (~ 2.1 eV) can be attributed to the non-bridging oxygen hole centers (NBOHCs) ($\cdot O - Si \equiv$) [256-258], which arise from the breaking of $Si - O$ bonds in the SiO_2 matrix by the implanted Ge ions [51]. The EL band at ~ 500 nm (~ 2.5 eV) could be related to the Si dangling bond centers which produce the 2.4 – 2.6 eV luminescence [50, 259]. In the work of Chen *et al.*, the 2.4 eV EL peak was also attributed to the Si dangling bond centers [50].

On the other hand, the EL band at ~ 760 nm (~ 1.6 eV) can be attributed to the radiative recombination of quantum-confined electron-hole pairs (i.e., excitons) in the nc-Ge embedded in SiO_2 [33, 66, 98, 172, 173]. Based on a recent calculation of the quantum confinement effect on excitons in quantum dots of indirect bandgap materials [260], the photon energy of excitons in nc-Ge as a function of the nanocrystal diameter is shown in Fig. 6-8. As the nc-Ge diameter reduces, the photon energy increases, indicating a stronger quantum confinement effect. From the figure, the nanocrystal diameter corresponding to the photon energy of 1.6 eV can be found as 5.3 nm. That is in good agreement with the average nc-Ge size of ~ 5 nm in our samples. The result supports the assignment of the 760 nm peak to the nc-Ge

embedded in the SiO_2.

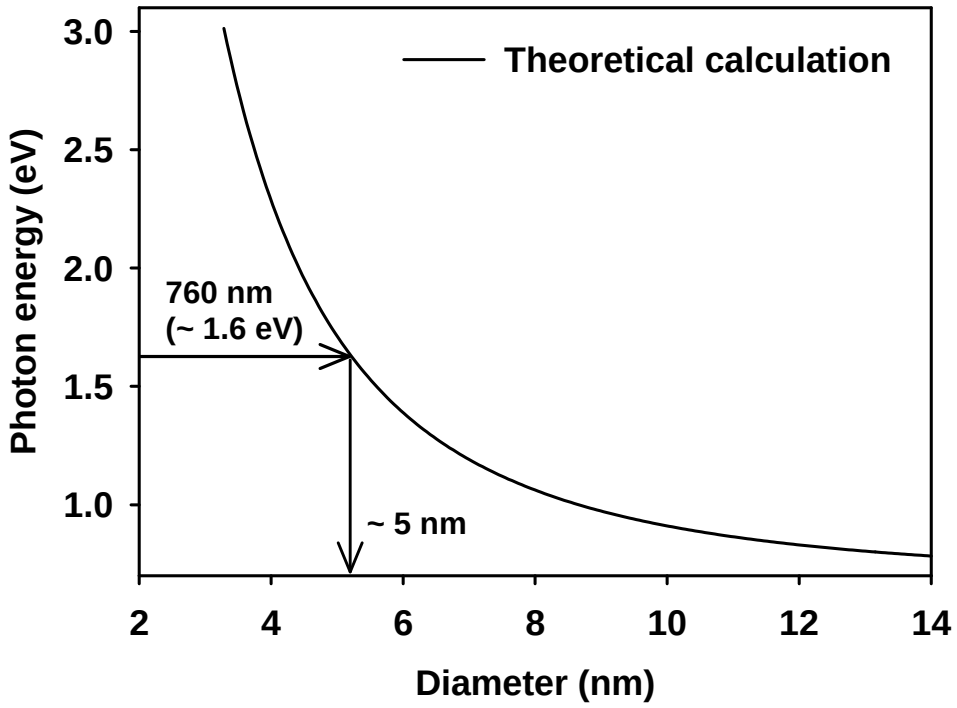

Fig. 6-8 Calculated photon energy of excitons in nc-Ge as a function of the nanocrystal diameter based on the quantum confinement theory (from Ref. [260]).

From the EL spectrum, it can be observed that about 80% of the EL is contributed by the NBOHCs. The result indicates that the NBOHCs are the dominant luminescence centers during the EL. The nc-Ge with quantum-confined excitons and other luminescence defects in the Ge-ion-implanted SiO_2 only play minor roles during the EL. One possible reason is that the amount of NBOHCs surpasses other luminescence centers. Another possible reason is that the excitation energy for the NBOHC defects could be much lower than that of other luminescent centers, and the

energy distribution of injected carriers can easily satisfy the requirement for the excitation of the NBOHC defects.

6.3.5 Conclusion

A broad EL spectrum with a dominant band at ~ 600 nm (2.1 eV) and two shoulder bands at ~ 500 nm (2.5 eV) and ~ 760 nm (1.6 eV) has been obtained from the light-emitting device based on a typical Ge-ion-implanted SiO_2 thin film embedded with nc-Ge. A linear relationship between the EL and the current transport has been observed, and both the current transport and the EL intensity have been found to exhibit a power-law dependence on the gate voltage. These results have been explained in terms of the formation of tunneling paths in the excess-Ge-distributed region and the radiative recombination of the injected electrons and holes via the luminescence centers along the tunneling paths. In addition, EL mechanisms for the three luminescence bands have been discussed. The dominant EL band located at ~ 600 nm has been attributed to the NBOHCs, while the 500 nm and 760 nm EL bands have been explained by the Si dangling bond centers and the nc-Ge with quantum-confined excitons, respectively.

6.4 Influences of implant dose and energy on EL behavior

In the previous section, visible EL from the light-emitting device based on a typical Ge-ion-implanted SiO_2 thin film has been demonstrated. In this section, the influences of implant conditions, i.e., implant dose and energy, on the EL behavior are investigated. The samples studied here are the light-emitting devices based on Group I

and Group II samples fabricated with various implant conditions. The details of the sample fabrication and structural properties have been discussed previously in Section 3.3.1.

6.4.1 Dependence of EL intensity on implant dose and energy

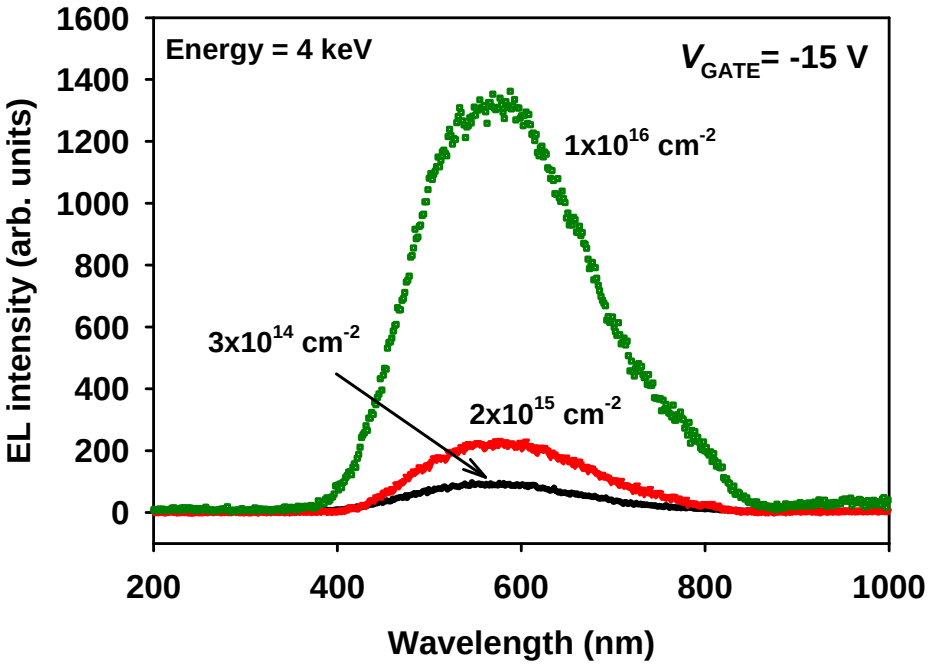

Fig. 6-9 EL spectra corresponding to samples with different implant doses obtained under the constant voltage injection at V_{GATE} = -15 V. The implant energy is 4 keV.

All of the light-emitting devices fabricated with different implant doses and energies exhibit visible EL when a negative V_{GATE} is applied to the ITO gate. Fig. 6-9 shows the EL spectra excited by a constant voltage injection at V_{GATE} = -15 V for samples with a constant implant energy but different implant doses from 3×10^{14} to 1×10^{16} cm^{-2}. As shown in the figure, the EL spectra with a dominant EL band at ~ 600 nm are similar in shape, but the EL intensity is significantly enhanced when the

implant dose increases. For example, under the same injection condition of V_{GATE} = -15 V, the 1×10^{16} cm^{-2} sample shows an EL intensity ~ 6 times stronger than the 2×10^{15} cm^{-2} sample and ~ 15 times stronger than the 3×10^{14} cm^{-2} sample.

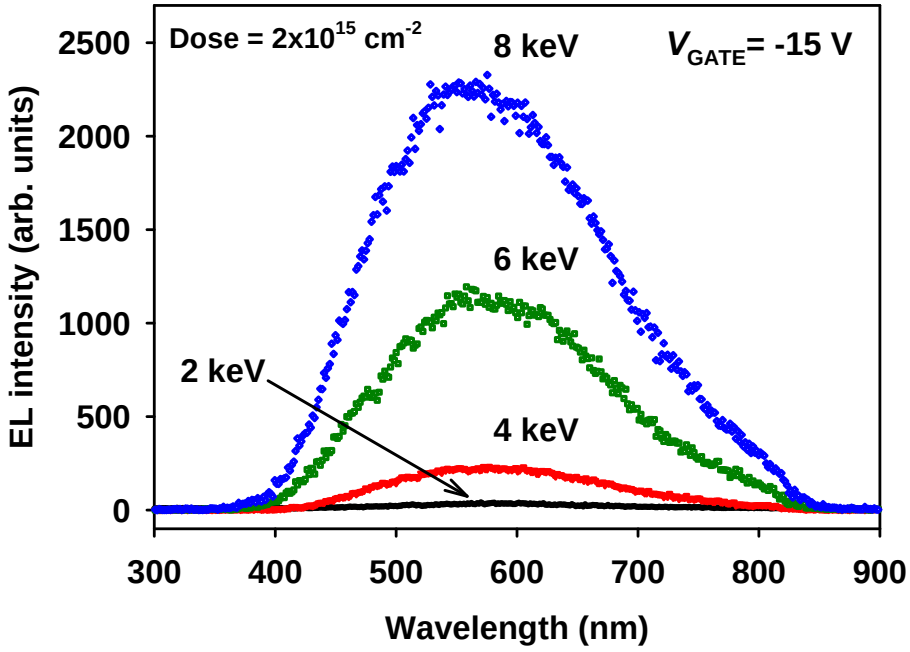

Fig. 6-10 EL spectra corresponding to samples with different implant energies obtained under the constant voltage injection at V_{GATE} = -15 V. The implant dose is 2×10^{15} cm^{-2}.

The enhancement of EL intensity under the same V_{GATE} can also be observed when the implant energy increases. Fig. 6-10 shows the EL spectra excited by a constant voltage injection at V_{GATE} = -15 V for samples with an identical implant dose but different implant energies from 2 – 8 keV. A broad EL spectrum peaked at ~ 600 nm can be clearly observed regardless of the implant energy. Although the EL spectra for the different implant energies are similar in shape, their intensity strongly depends

on the implant energy. As shown in Fig. 6-10, the EL intensity is significantly enhanced when the implant energy increases. For example, under the same injection condition of V_{GATE} = -15 V, the EL intensity of the 8 keV sample is ~ 2 times of that of the 6 keV sample, while the 6 keV sample shows an EL intensity ~ 40 times stronger than the 2 keV sample.

6.4.2 Dependence of current conduction on implant dose and energy

Fig. 6-11 shows the J_{GATE}-V_{GATE} characteristics under a forward biased condition (i.e., $V_{GATE} < 0$) for all the light-emitting devices with various implant doses and energies. As shown in Fig. 6-11(a), when the implant energy is a constant, the current conduction is enhanced as the implant dose increases. Similarly, as shown in Fig. 6-11(b), when the implant dose is a constant, the current conduction is enhanced as the implant energy increases. As a result of the increase in the current conduction, more electrons from the ITO gate and more holes from the *p*-type Si substrate are injected into the Ge-ion-implanted region, leading to an increase in the radiative recombination of the injected electrons and holes and thus an enhancement in the EL intensity as observed in Fig. 6-9 and Fig. 6-10.

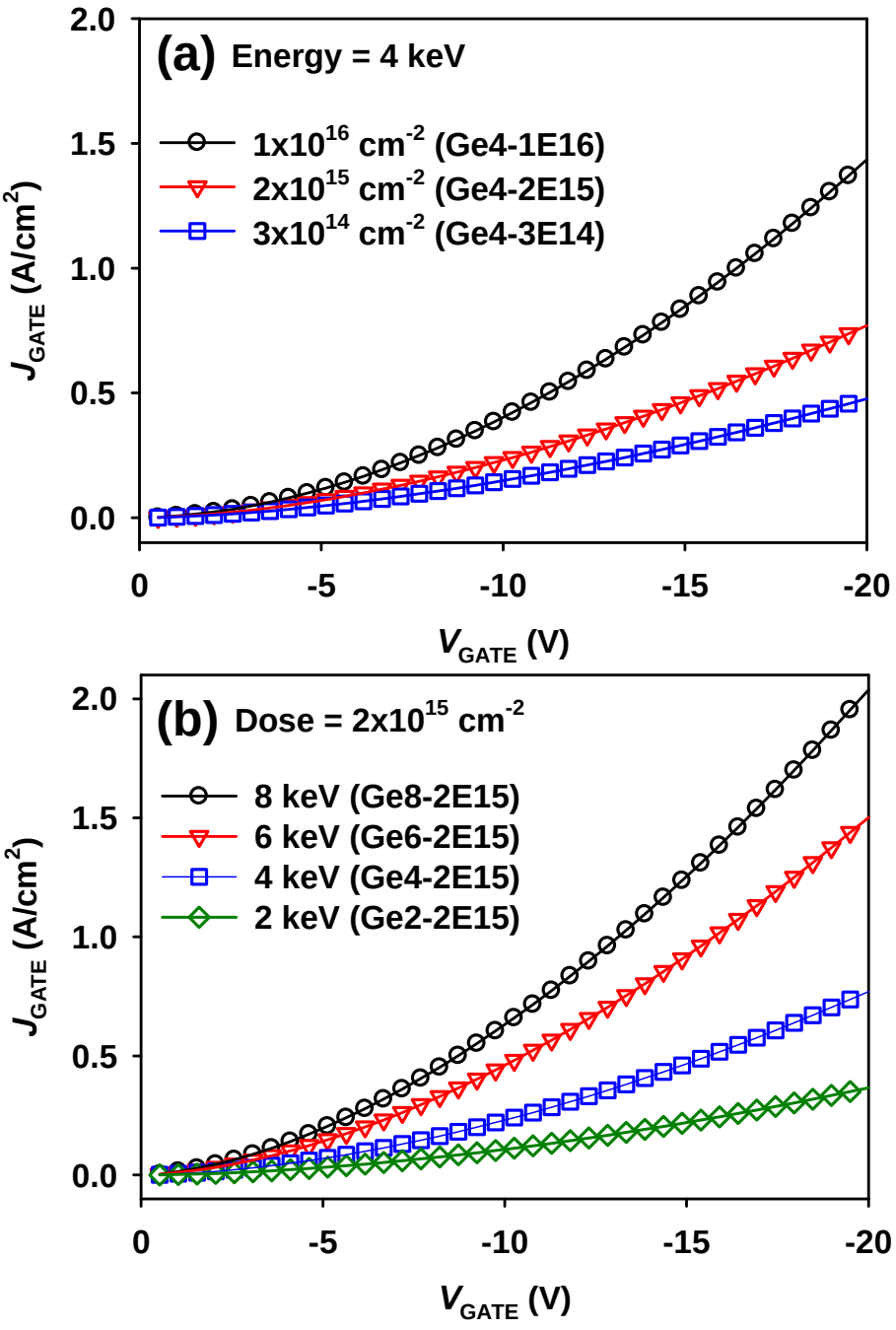

Fig. 6-11 Gate current density versus gate voltage (J_{GATE}-V_{GATE}) characteristics for (a) samples with a constant implant energy and various implant doses, and (b) samples with a constant implant dose and various implant energies.

From the curve fitting, it can be found that all of the J_{GATE}-V_{GATE} characteristics shown in Fig. 6-11 can be described by a power-law relationship as given by Eq. (6.1). The results indicate that the transport of carriers in the light-emitting devices fabricated by various implant conditions can be explained by the current conduction model as discussed previously in Section 6.3.3. Under the application of a negative V_{GATE}, the current transport is due to the carrier conduction through a network of conductive percolation paths in the excess-Ge-distributed SiO_2 region near the ITO gate and the carrier tunneling across the "pure SiO_2" region near the Si substrate.

For those samples with a constant implant energy (i.e., Group II samples), the thickness of the "pure SiO_2" region is not significantly affected by the implant dose, because most of the implanted Ge ions are still confined into the 20 nm region (i.e., the excess-Ge-distributed region) near the gate. However, the increase in the implant dose leads to the formation of more conductive percolation paths in the excess-Ge-distributed region because of the higher amount of nc-Ge and implantation-induced defects in this region. As a result, the conduction of the excess-Ge-distributed region is enhanced. This explains the enhanced current conduction with implant dose for a given V_{GATE}, as observed in Fig. 6-11(a).

On the other hand, for those samples with a constant implant dose (i.e., Group I samples), the enhanced current conduction with the implant energy can be explained as follows. According to the SIMS results in Fig. 3-6, when the implant energy increases, the excess-Ge-distributed region expands while the "pure SiO_2" region becomes narrower. For example, in the 2 keV sample, the thickness of the excess-Ge-distributed region and the "pure SiO_2" region is ~ 11 and 19 nm, respectively.

However, in the 8 keV sample, their thickness becomes ~ 24 and 6 nm, respectively. As a result, the conduction in the "pure SiO_2" region is enhanced due to the easier tunneling of carriers. For the excess-Ge-distributed region, the conduction depends on the amount of conductive percolation paths, which are associated with the implantation-induced defects and nc-Ge. In a typical ion-implanted oxide film, the amount of implantation-induced defects should be proportional to the number of displacement events which occur when the transferred energy from the implanted ions is greater than the displacement energy during a collision event [261]. The total number of displacements in the host matrix caused by the ion implantations can be obtained from the stopping and range of ions in matter (SRIM) simulation [261].

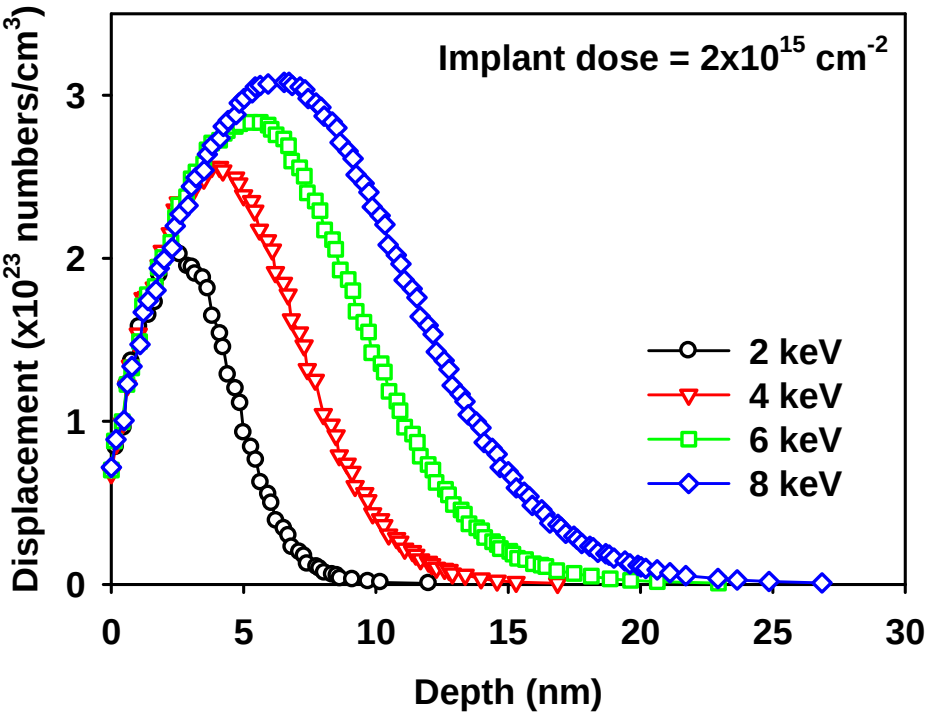

Fig. 6-12 Depth profiles of the number of displacements in the Ge-implanted SiO_2 thin film for various implant energies obtained from the SRIM simulation.

As shown in Fig. 6-12, when the implant energy increases, the total amount of displacements in the Ge-implanted SiO_2 becomes larger, suggesting a higher amount of implantation-induced defects in the excess-Ge-distributed region. As a result, the conduction in the excess-Ge-distributed region is also enhanced with the implant energy, because more conductive percolation paths are formed in this region. Since both the excess-Ge-implanted region and the "pure SiO_2" region exhibit an enhanced conduction when the implant energy increases, the overall current conduction in the Ge-ion-implanted SiO_2 thin film increases with the implantation energy, as observed in Fig. 6-11(b).

6.4.3 Dependence of external quantum efficiency on implant dose and energy

The effects of implant conditions on the EL behavior were further investigated by examining the external quantum efficiency (EQE), which describes the EL intensity under the constant current injection (i.e., under an identical J_{GATE}), among samples with different implant doses and energies. The EQE of a light-emitting device is defined as

$$\mathrm{EQE} = \frac{P_{\mathrm{OPT}}/E_{\mathrm{PHOTON}}}{J_{\mathrm{GATE}}/q} \tag{6.2}$$

where P_{OPT} is the output power of the light emission, E_{PHOTON} is the photon energy of the light emission, J_{GATE} is the gate current density, and q is the electronic charge. From the EL spectra shown in Fig. 6-9 and Fig. 6-10, it is known that all the samples with different implant conditions show a similar E_{PHOTON} at ~ 2.1 eV. Besides, when

an identical measurement setup is used, the P_{OPT} is approximately proportional to the measured integrated EL intensity (I_{EL}). Thus, the EQE of the light-emitting device can be estimated by

$$\mathrm{EQE} = C\frac{I_{\mathrm{EL}}}{J_{\mathrm{GATE}}} \tag{6.3}$$

where C is a proportionality constant. Although the absolute value of EQE for our light-emitting devices cannot be determined due to the lack of a calibrating device with a known output power, the relative EQE among different devices can be compared using Eq. (6.3). Fig. 6-13 shows the normalized EQE for different implant doses under either constant voltage injection or constant current injection. As shown in the figure, for both constant voltage injection and constant current injection, the EQE increases with the implant dose.

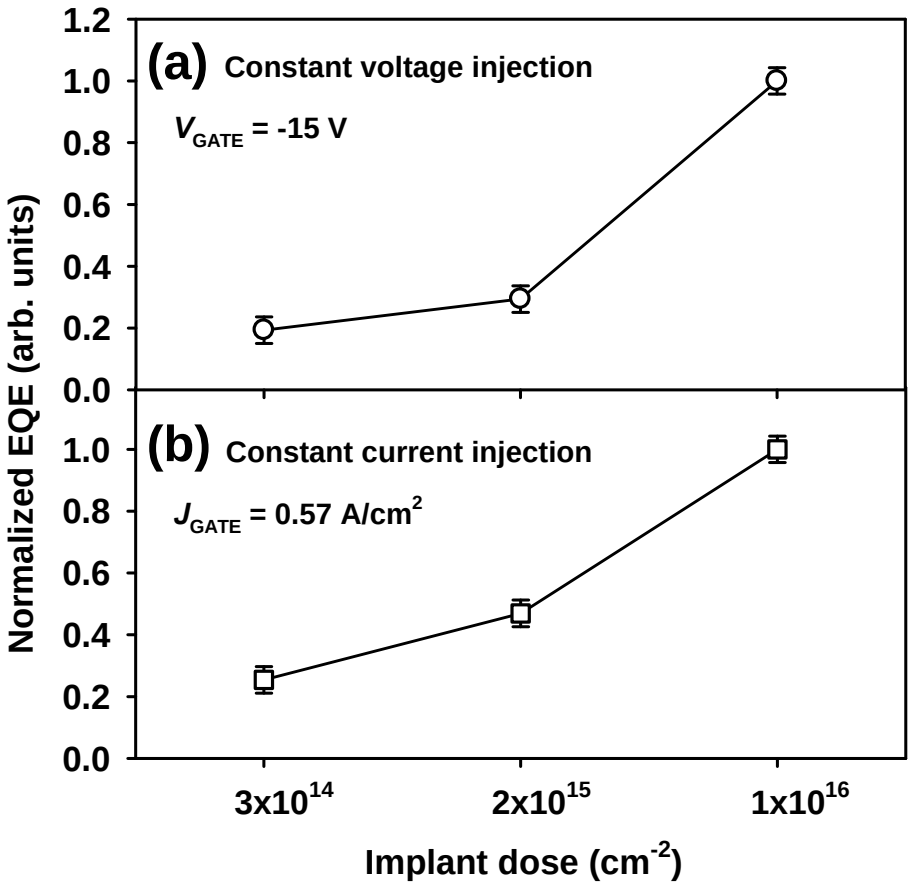

Fig. 6-13 Dependence of the external quantum efficiency (EQE) on implant dose: (a) constant voltage injection at V_{GATE} = -15 V; and (b) constant current injection at J_{GATE} = 0.57 A/cm^2.

The situation for samples with different implant energies is shown in Fig. 6-14. Similarly, for both constant voltage injection and constant current injection, the EQE increases with the implant energy. The results suggest that under identical J_{GATE}, the EL intensity still depends on the implant dose and energy. Obviously, the enhancement in the current conduction cannot explain the increase of EQE with the implant dose and energy.

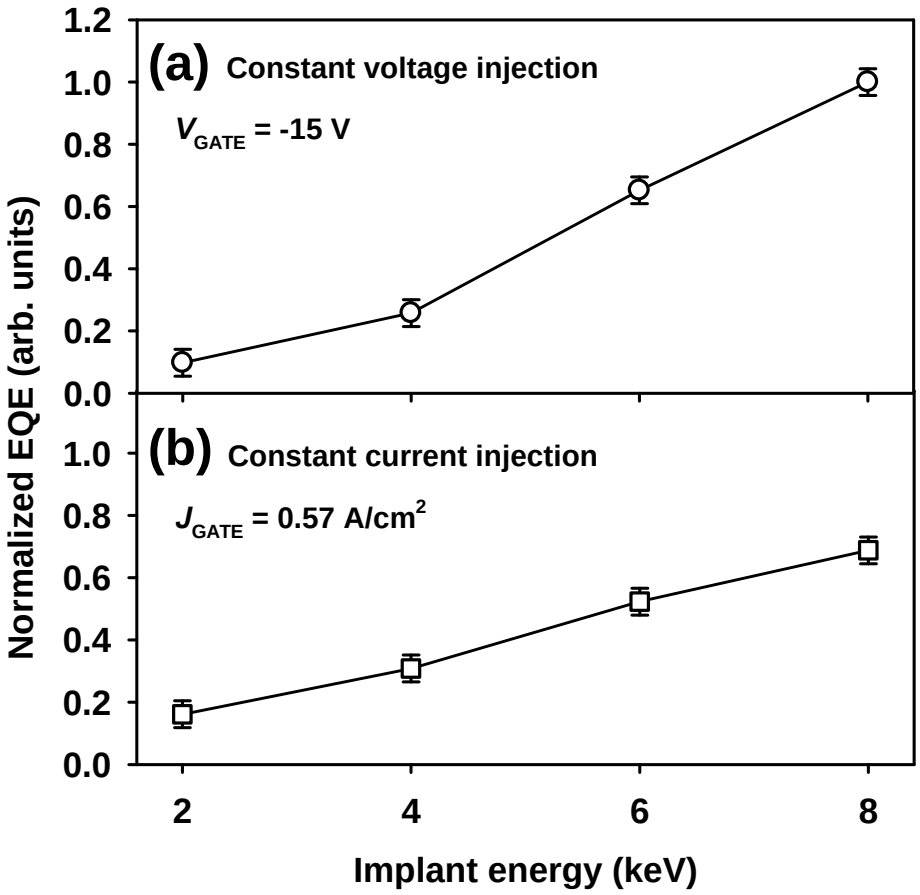

Fig. 6-14 Dependence of the external quantum efficiency (EQE) on implant energy: (a) constant voltage injection at V_{GATE} = -15 V; and (b) constant current injection at J_{GATE} = 0.57 A/cm^2.

The increase of EQE with implant dose and energy can be attributed to the creation of more luminescence centers in the oxide by the ion implantation. Previously, it has been shown that the EL spectra for all the samples can be deconvolved into three EL bands at ~ 600 nm (2.1 eV), ~ 500 nm (2.5 eV) and 760 nm (1.6 eV), which are associated with the NBOHCs, Si dangling bond centers and the radiative recombination of quantum-confined excitons in nc-Ge, respectively. Fig. 6-15(a) shows the integrated intensity for each luminescence band as a function of the implant

dose under the constant current injection at J_{GATE} = 0.57 A/cm^2. The enhancement in the intensity of all the three EL bands can be observed as the implant dose increases from 3×10^{14} to 1×10^{16} cm^{-2}. Similarly, in Fig. 6-15(b), the integrated intensity for each luminescence band as a function of the implant energy under the constant current injection at J_{GATE} = 0.57 A/cm^2 is shown. The enhancement in the intensity of all the three EL bands can also be observed as the implant energy increases from 2 to 8 keV. Among these three EL bands, the dominant 600 nm band shows the strongest enhancement, while the 500 nm band shows the lowest enhancement. The results indicate that the creation of all the three types of luminescence centers increases with the implant dose and energy, and the increase in the creation of NBOHCs plays the dominant role in the overall EL enhancement.

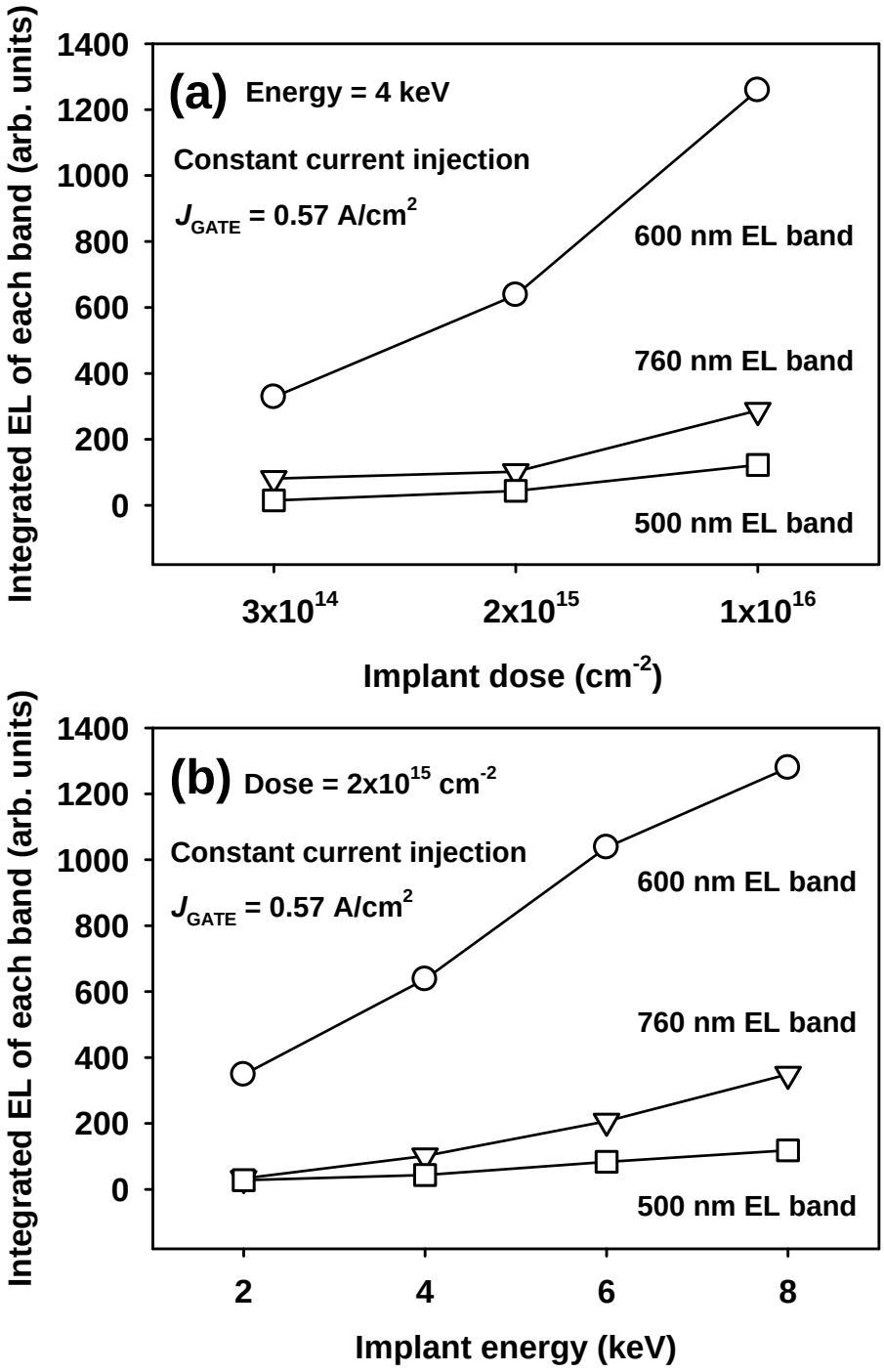

Fig. 6-15 Integrated intensity of each EL band as a function of (a) implant dose, and (b) implant energy. The EL measurements were conducted under constant current injection at J_{GATE} = 0.57 A/cm^2.

The increase in the creation of luminescence centers with the implant dose and energy is explained as follows. For the 500 nm and 600 nm EL bands, since the luminescence centers are defect states created by the ion implantation [51], the amount of created luminescence centers should be proportional to the number of total displacements in the host matrix caused by the ion implantations. For a constant implant energy, the number of displacements in the SiO_2 matrix increases with the implant dose because more ions are implanted into the SiO_2, resulting in more collision events. For a constant implant dose, as the implant energy increases, the amount of displacements in the Ge-implanted SiO_2 also increases. That is because for a Ge ion implanted into the SiO_2 lattice, higher implant energy leads to more collision events before this ion stops, and hence more displacements in the SiO_2 are created. The increase of the total amount of displacements with the implant energy has been confirmed by the SRIM simulation as shown previously in Fig. 6-12., On the other hand, the 760 nm EL band is associated with the nc-Ge embedded in the SiO_2. The increase of the implant dose under the same implant energy leads to a higher density of nc-Ge. Thus, more luminescence centers are present in the SiO_2, leading to a stronger 760 nm EL band as the implant dose increases. However, the increase of the implant energy under the same implant dose cannot create more nc-Ge. The enhancement of the 760 nm EL band with the implant energy could be explained as follows. As the implant energy increases, the distribution of nc-Ge in the SiO_2 is broadened, and the distance between adjacent nc-Ge increases. That leads to a stronger localization of injected electrons and holes in the nc-Ge, which enhances the efficiency of radiative recombination of electrons and holes in the nc-Ge. Thus, as the

implant energy increases, the integrated EL intensity for the 760 nm EL band also becomes stronger.

6.4.4 Conclusion

Light-emitting devices based on Ge-ion-implanted SiO_2 thin films have been fabricated, and the influences of implant dose and energy on the EL behavior have been investigated. It has been found that the EL intensity is significantly enhanced as the implant dose and energy increases. The enhancement in EL intensity has been partially attributed to the enhanced current conduction in the Ge-ion-implanted SiO_2 as a result of the formation of more conductive percolation paths. In addition, the external quantum efficiency has also been found to increase with the implant dose and energy. The result has been attributed to the increase of implantation-induced luminescence centers in the Ge-ion-implanted SiO_2.

6.5 Summary

In this chapter, light-emitting devices based on a structure of ITO / SiO_2 embedded with nc-Ge / *p*-Si substrate have been fabricated. The EL properties of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge have been investigated. A broad EL spectrum with a dominant band at ~ 600 nm (2.1 eV) and two shoulder bands at ~ 500 nm and ~ 760 nm has been obtained. Both the current transport and the EL intensity have been found to exhibit a power-law dependence on the gate voltage. The EL behavior has been explained in terms of the formation of tunneling paths in the excess-Ge-distributed region and the radiative recombination of the injected

electrons and holes via the luminescence centers along the tunneling paths. The EL mechanisms have also been discussed. In addition, the influences of implant dose and energy on the EL properties have been investigated. It has been found that the EL intensity is significantly enhanced as the implant dose and energy increases. The enhancement in EL intensity has been partially attributed to the enhanced current conduction in the oxide. Besides, the external quantum efficiency has also been found to increase with the implant dose and energy. That has been attributed to the increase of implantation-induced luminescence centers in the Ge-ion-implanted SiO_2.

Chapter 7 Conclusion and Recommendations

7.1 Conclusion

Modern electronic applications aggressively demand the down scaling of non-volatile memory devices in pursuit of larger capacity, smaller device area, lower power consumption and higher operating speed. However, the limited potential in continuous scaling of the conventional memory structure based on a floating-gate urges the search for new memory structures. In addition, the constantly growing demand of compact systems capable of performing new and increased numbers of operations brings on the development of Si-compatible light-emitting devices to fulfill the integration of optoelectronic devices with other optical and electronic circuits. SiO_2 embedded with Ge nanocrystals (nc-Ge) is considered as a promising candidate for the next-generation non-volatile memories and Si-compatible light-emitting devices. In this thesis, the synthesis of nc-Ge embedded in SiO_2 has been successfully demonstrated using the Ge ion implantation technique which is fully compatible with modern CMOS technology and has the advantage of being able to precisely control the nc-Ge concentration and depth distribution by adjusting the implant energy and Ge ion dose. The electrical and optoelectronic properties of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge have been investigated in detail. The results presented in this thesis enhance our understanding of the properties of SiO_2 embedded with nc-Ge synthesized by the Ge ion implantation technique, and open up new possibilities to fabricate next-generation non-volatile memory devices and Si-

compatible light-emitting devices. This section briefly summarizes the overall work presented in this thesis.

7.1.1 Current transport behavior

The current transport behavior of Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been investigated. Two different distributions of nc-Ge in the SiO_2 thin films have been prepared: 1) a narrow distribution of nc-Ge near the SiO_2 surface using low implant energy of 2 – 8 keV, and 2) a broad distribution of nc-Ge throughout the SiO_2 using a high implant energy of 16 keV. The structural properties of the samples have been characterized. The characteristics of the gate current density versus oxide field at various temperatures have been investigated, and the different transport mechanisms dominating in the different oxide field regions have been identified. The current transport behavior has been explained by appropriate models. In addition, a conduction modulation effect for SiO_2 thin films embedded with nc-Ge caused by UV illumination has been reported. The conduction modulation has been attributed to the charging and discharging in the nc-Ge induced by the UV illumination.

7.1.2 Charge trapping and charge retention behavior

The charge trapping and charge retention behavior of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been investigated. The dependences of charge trapping and charge retention on the polarity and magnitude of the charging voltage have been studied. For a positive charging voltage, only electron trapping occurs, and the trapped electrons show a long retention time. However, for a negative charging

voltage, both the hole trapping and electron trapping occur simultaneously, and the hole trapping is dominant if the magnitude of the charging voltage is small or the charging time is short. Due to the relatively easier loss of the trapped holes, the net charge trapping in the nc-Ge exhibits a continuous shift towards a more negative value with waiting time. Besides, the influences of nc-Ge synthesis process on the charge trapping and charge retention behavior have been investigated. The changes in the structural and chemical properties of the Ge-ion-implanted SiO_2 caused by thermal annealing have been found to seriously affect the charge storage behavior in the nc-Ge. Moreover, it has also been demonstrated that the ion implantation conditions, i.e., implantation energy and dose, have a strong influence on the memory window as well as the long-term charge retention. Lastly, the charge loss caused by the lateral charge transfer along the Ge-distributed layer and charge leakage from the nc-Ge to the Si substrate has been studied. The existence of the lateral charge transfer has been confirmed, and the role of lateral charge transfer in the charge retention has been determined.

7.1.3 Calculation of MOS capacitance

A modeling approach to calculate the MOS capacitance of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge has been presented. In this approach, the nc-Ge distributed SiO_2 region is divided into sub-layers, and the effective dielectric constant for each sub-layer is calculated using the Maxwell-Garnett effective medium approximation (EMA). Both the distribution of nc-Ge in SiO_2 and the reduced dielectric constant corresponding to the nanometer size of nc-Ge have been considered during the calculation. Using this approach, the influences of implant energy and dose

on the MOS capacitance have been investigated, and the static dielectric constant of nc-Ge embedded in SiO_2 has been determined. The calculated capacitances for various nc-Ge distributions have been compared with the measurement results. Good agreement between the calculated capacitances and measured data has been achieved.

7.1.4 EL behavior

Light-emitting devices based on a structure of ITO / SiO_2 embedded with nc-Ge / *p*-Si substrate have been fabricated. The EL properties of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge have been investigated. A broad EL spectrum with a dominant band at ~ 600 nm (2.1 eV) and two shoulder bands at ~ 500 nm and ~ 760 nm has been obtained. Both the current transport and the EL intensity have been found to exhibit a power-law dependence on the gate voltage. The EL behavior has been explained in terms of the formation of tunneling paths in the excess-Ge-distributed region and the radiative recombination of the injected electrons and holes via the luminescence centers along the tunneling paths. The EL mechanisms have also been discussed. In addition, the influences of implant dose and energy on the EL properties have been investigated. It has been found that the EL intensity is significantly enhanced as the implant dose and energy increases. The enhancement in EL intensity has been partially attributed to the enhanced current conduction in the oxide. Besides, the external quantum efficiency has also been found to increase with the implant dose and energy. That has been attributed to the increase of implantation-induced luminescence centers in the Ge ion-implanted SiO_2.

7.2 Recommendations

The work presented in this thesis has added more understanding about the electrical and optoelectronic properties of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge, and opens up new possibilities for their applications in non-volatile memories and Si-compatible light-emitting devices. To make the research more complete, the following research could be done.

7.2.1 Synthesis of nc-Ge embedded in SiO_2 using other techniques

Besides the ion implantation technique, other techniques such as co-sputtering, LPCVD and e-beam evaporation can also be used to prepare the nc-Ge embedded in SiO_2. Although the Ge ion implantation technique surpasses others in terms of good reproducibility and good control over the depth distribution of nc-Ge in SiO_2, other techniques have their own advantages. Some properties could be exclusively associated with a particular synthesis technique. The future work should include the synthesis of nc-Ge embedded in SiO_2 using techniques other than the Ge ion implantation. The electrical and optoelectronic properties of samples synthesized by different techniques can be compared, and the results can lead to the proper understanding about the relationship between the synthesis technique and the electrical and optoelectronic properties.

7.2.2 Investigation of methods to improve the performance of devices based on Ge-ion-implanted SiO_2

Methods to improve the performance of non-volatile memory devices and light emitting devices based on Ge-ion-implanted SiO_2 can be systematically investigated in the future work. For a practical non-volatile memory device, a low operating voltage with a large memory window is desired. In Chapter 4, it has been shown that under the same charging voltage, a larger memory window can be achieved by increasing the implant energy or ion dose. However, for the present device structure, the charging voltage should be larger than 20 V to result in a significant flatband voltage shift (ΔV_{FB}). One way to achieve a lower charging voltage and a wider memory window is to reduce the total oxide thickness, such that the electric field across the oxide is sufficiently high at low operating voltages. However, the charge retention time could be scarified due to the easier charge leakage to the Si substrate. That could be improved by inserting a low-k dielectric material as the blocking layer in between of the Ge-ion-implanted SiO_2 and the Si substrate. On the other hand, for the light emitting device, the enhancement in the external quantum efficiency (EQE) by varying the implant condition (i.e., the implant energy and the ion dose) has been discussed in Chapter 6. Besides, the EQE could be affected by the thermal annealing which alters the amount of luminescence centers in the Ge-ion-implanted SiO_2 thin films. The improvement in EQE could also be achieved by changing the device structure. For example, a hole-injection buffer layer could be introduced in between of the ITO gate and the Ge-ion-implanted SiO_2 to enhance the hole injection efficiency under a negative bias condition.

7.2.3 Investigation of single-electron charging in nc-Ge

Nanocrystals are promising candidates for single-electron devices because of their discrete energy states in the conduction band and valence band. The operation of single-electron charging / discharging relies on the Coulomb blockade effect, which is due to the discrete changes in the charging energy of an isolated conducting island. When one or more electrons are trapped by a nanocrystal, an additional electron needs to overcome the Coulombic repulsion from those initial electrons trapped in the nanocrystal. In order for the single-electron charging phenomenon to be observable, the temperature has to be low enough so that the charging energy is larger than the thermal energy of the electron. One important future work is to investigate the single-electron charging effect of the Ge-ion-implanted SiO_2 thin films embedded with nc-Ge using the *I-V* and *C-V* measurements at low temperature (i.e., using a cryogenic system with liquid Helium). The electrostatic energy of the nc-Ge can be determined. In addition, the effects of size and distribution of nc-Ge on the single-electron charging can be studied.

7.2.4 Simulation of non-volatile memory cell based on nc-Ge

Technology computer-aided design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor processes and devices. The fabrication and device performance of non-volatile memory cells based on nc-Ge (i.e., MOSFETs with nc-Ge embedded in the gate oxide) can be simulated using the TCAD software. The simulation is important for the actual device fabrication, because numerous important properties, such as threshold voltage, memory window and local electric field around nc-Ge, can be predicted from the simulation. In addition, the program / erase mechanisms of the memory cell can be studied. The effects of tunnel

oxide thickness, control oxide thickness and the size and distribution of nc-Ge on the memory performance can also be investigated using the TCAD simulation.

7.2.5 Development of an empirical formula for the dielectric constant of nano-composite systems

The current study presents an approach to calculate the MOS capacitance of a Ge-ion-implanted SiO_2 thin film. The reduced dielectric constant of the nc-Ge has been taken into account in the modeling approach. Due to the limitation of the ion implantation technique, the resultant nanocrystals do not show much variation in their size when the fabrication condition is changed. Indeed, the current modeling approach is also applicable to nano-composite systems fabricated by other methods which are effective in producing nanocrystals with different sizes. The further study needs to model the nano-composite systems fabricated by different methods. An empirical formula can then be derived to accurately describe the dependence of the dielectric constant on various properties of the nano-composite system, such as nanocrystal size, distribution, volume fraction, etc. The relationship would be useful for the design and simulation of devices based on these nano-composite systems.

7.2.6 Development of Si-compatible integrated optoelectronic devices

In the current study, the light emission properties of the Ge-implanted SiO_2 thin films embedded with nc-Ge have been investigated using a simple structure of ITO / SiO_2 embedded with nc-Ge / *p*-Si substrate. With the recent development of Si-compatible optoelectronic devices, it is possible for future work to demonstrate the integration of several optoelectronic devices on one single Si wafer using existing

CMOS technology. For example, with the proper design and layout, light emission from the SiO_2 embedded with nc-Ge can be transmitted through the wave-guide based on SiO_2, and be detected by a Si-based photodiode. Such optoelectronic integration could be used as the inter-chip optical interconnect. More sophisticated operations can be achieved by adding a Si-based light modulator, switch and other optoelectronic functional blocks.

7.2.7 First-principle calculation of electronic properties of nc-Ge

The future work can also include the first-principle calculation, which a useful method to theoretically predict the electronic structures of nano-scale materials such as nc-Ge surrounded by SiO_2. The information about the band gap expansion and the dielectric suppression of nc-Ge can be obtained from the first-principle calculation. The calculation results can also be compared with the experimental results obtained in this work.

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Journals:

[1] **M. Yang**, T. P. Chen, J. I. Wong, C. Y. Ng, Y. Liu, L. Ding, A. D. Trigg, C. H. Tung, C. M. Li, and S. Fung, "Charge trapping and retention behaviors of Ge nanocrystals distributed in the gate oxide near the gate synthesized by low-energy ion implantation", *Journal of Applied Physics*, vol. 101, pp. 124313, 2007.

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