Top-down design verification of subranging pipelined analog-to-digital converter

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**TOP-DOWN DESIGN VERIFICATION OF SUBRANGING
PIPELINED ANALOG-TO-DIGITAL CONVERTER**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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A thesis submitted to the Nanyang Technological University
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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

1 June 2010

Date

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Abstract

High-speed high resolution analog-to-digital converter (ADC) is the key design blocks in mixed-signal chip design since the ADC is an interface between digital signal processing systems and the analog world. With the rapid advancement of CMOS fabrication technology, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. This has recently generated a great demand for low-power ADCs that can be realized in a mainstream deep sub-micrometer CMOS technology.

On the other hand, since analog circuits tend to be sensitive to fluctuations in temperature and the fabrication process, circuit designers are forced to allow for a wide margin to ensure the desired operation of all the chips under various conditions. Therefore, if the margins can be minimized, both reduction of power dissipation and a higher yield in mass production can be achieved.

To tap onto the waves of the rapid booming wireless communication markets, high resolution and high speed A/D converter is required at very low power consumption. Providing the wanted resolution at the required speed for the minimum power consumption and silicon cost is what's driving the use of specific A/D architectures [1]. Architectures that have been applied include

flash, subranging, successive approximation, sigma-delta and pipelined. Each of these architectures has their specific advantages and drawbacks. Pipelined architecture poised as a suitable candidate since the power consumption will be an order of magnitude better comparing to flash ADC, subranging ADC, successive approximation ADC and oversampling ADC. Moreover, a correction algorithm can be employed to compensate for the errors in the sub-ADC. Shooting for even higher speed, parallelism is required to be incorporated into pipelined structure. Hence, in this work, a feasibility study of a novel subranging pipelined A/D converter with 100 MS/s and 8-bit resolution is conducted.

This research describes the design of a 8-bit 100 MS/s subranging pipelined analog-to-digital converter(ADC) suitable for wide-range applications. To achieve the wide-range performance, this work purposes a novel architectural design at both system and circuit levels.

At the device level, device modeling and active components characterisations are carefully studied. Thin gate oxide, NFET is fabricated in Chartered 90nm CMOS process. The results showed that the models used in SPICE simulation correlate well with the measured results except at the end of high VDD where breakdown is seen in the measured results but not during simulation. At the circuit level, a 3-bit coarse ADC and a 6-bit fine ADC are developed. Logic designs are also carried out. At the system level, this work investigates the effects of ADC design parameters such as DNL and INL in the static DC aspects and SFDR and ENOB in the dynamic AC aspects. A top-down design methodology is adopted in this work. The behavioral modelling results verify the success of the proposed architecture. The simulation results showed that the designed ADC is able to achieve a 7.4 effective bits out of 8 bit resolution.

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Chapter 1

Introduction

1.1 Motivation and Background

CMOS technologies move steadily toward finer geometries, which provide higher digital capacity, lower dynamic power consumption, and smaller area. This results in integration of whole systems, or large parts of systems, on the same chip (system on chip, or SoC). For such systems the key parameters for the building blocks are often low power dissipation and small silicon area. Analog-to-digital converters (ADCs) are important building blocks in many of the SoC applications. Therefore, ADCs provided as Intellectual Property (IP) blocks goes into a wide range of applications, spanning from imaging to ultrasound and communication systems. This means that the ADC has to occupy small area and have low power dissipation. Further, it has to be designed for the same technology as the rest of the system. This means that the supply voltage is low and subsequently the maximum signal swing is lowered compared to older technologies. Therefore, it is necessary to keep the noise and distortion of the ADC itself low.

Additionally, to minimize the cost of the total SoC system, the IP block should be implemented in a pure digital process, avoiding use of costly analog process options [1]. ADCs that have a power consumption which scales with sampling rate can significantly reduce production costs as a single ADC can be used to target multiple applications with different performance requirements, thereby reducing development costs and time to market [2]. Among various ADC architectures, pipelined converter is widely used in Nyquist sampling applications that require a combination of high resolution and high throughput [3] [4] [5].

With the rapid scaling of CMOS process, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. Digital design methodology has proven to be successful due to the fact that logic circuits may be accurately simulated with a high degree of abstraction, and from that transistor implementation may be automatically synthesized using a library of leaf cells, which are placed and routed automatically [6]. However, these advantages are difficult to transfer to analog and mixed signal design. One of the main reason is that analog design automation is far beyond the digital one, due to the inherent complexity of analog systems. The general belief is that behavioral modeling overly simplifies the complexities of analog circuit operation thought to be necessary to validate its operation. To increase innovation in analog and mixed-signal design, very often, a new concept or architecture is needed to be proven first at the early stage of the design process far before the transistor implementation. High descriptive behavioral models are required to reliably simulate and verify complex analog systems, thus saving silicon iterations and make all the difference in timely arrival to market.

To allow top-down design and bottom up verification, it is important to be able to simulate a cascade of blocks, each with a different view. That is, some blocks represented as behavioral models, others at the transistor level, yet others as abstract logic cells. This project will focus on a new approach to high speed pipelined A/D converter design. In this work, a top-down design methodology will be developed that is suitable to verify a proposed ADC architecture for deep sub-micron CMOS process.

1.2 Objectives

The main objective of this work is to expand the applicability of the top-down design methodology to the design of a A/D converter system in deep sub-micron CMOS process. This new design approach that starts with the highest level of an idea and works its way down to the lowest level of detail allows us to validate a new ADC architecture with a high level of integration. A principal part of this work has been the design of the A/D converter architecture which consists of subranging and pipelining techniques.

This work is split up into five main subjects:

1. Comparison of the various A/D converter architectures.
2. Analysis of the errors due to imperfect circuit components and process issues.
3. Proposal of a new ADC architecture suitable for deep sub-micron CMOS process.
4. Validation of the proposed ADC using a top-down design methodology

which supports a design process where non-ideal effects can be incorporated in an incremental way.

5. Behavioral simulation of the dynamic performance of the converter before it is fabricated.

The results from these investigations are used in the circuit design and realisation of the A/D converter.

1.3 Major Contributions

A number of contributions have been made in this work. The contributions are summarized as follows:

1. The study of designing an 8-bit 100 MS/s A/D converter with subranging pipelined architecture is proposed.
2. In the system design contributions, a top-down design verification based on reuse modular and parametric behavioral modeling for proposed sub-ranging pipelined ADC is achieved. The behavioral model of each module/block is designed, written and modeled using high level description language, Verilog-AMS. The non-ideal effects are incorporated in an incremental way in each block and enables each block to be reused and simulated.
3. In the circuit design contributions, sub-building blocks which included a 3-bit flash ADC, a pipelined ADC and logic circuits are built and designed.
4. The thesis contributes the analysis of non-ideal effects on the single pipelined

stage which is identified as one of the critical building block for high speed pipelined ADC design.

5. At the device level contributions, device modeling and components characteristic are carefully studied and active devices are characterised.

1.4 Organization of the Thesis

This thesis is divided into eight chapters. It is organized as follows.

Chapter 1 contains a brief introduction on the background of ADCs and the existing problems and challenges faced in the design of ADCs. The objectives and contributions of this thesis are also introduced.

Chapter 2 gives a brief review on several high speed CMOS A/D converter architectures and highlights its limitations. Related techniques and development are introduced.

Chapter 3 discusses the non-idealities in pipelined A/D architecture.

Chapter 4 gives an overview of the various issues that must be considered to successfully design analog and mixed-signal IPs in deep sub-micron CMOS technology. Understanding the devices' performance on advanced process is extremely important especially during the selection process in the early stage of the design phase.

Chapter 5 presents the proposed subranging pipelined ADC architecture.

Chapter 6 describes design implementation of the proposed 8-bit 100 MS/s Subranging Pipelined ADC.

Chapter 7 discusses the top-down design methodology and presents the sim-

ulation results and discussions.

Chapter 8 concludes this thesis. Some recommendations on future work are discussed in this chapter.

Chapter 2

Review of High Speed A/D Converter Architectures

2.1 Introduction

In this chapter, several ADC architectures are presented. A survey of the field of current A/D converters research reveals that a majority of effort has been directed to four different types of architectures: pipelined, flash, successive approximation and over-sampled ADCs. Each has benefits that are unique to that architecture and span the spectrum of high speed and resolution.

Most ADC applications today can be classified into 4 broad market segments: data acquisition, precision industrial application, voice band/audio and high speed application. The classification in Figure 2.1 shows in a general way how these application segments and the associated typical architectures relate to ADC resolution (vertical axis) and sampling rate (horizontal axis).

Some architectures are preferred over others for certain applications. Three

Figure 2.1: ADC architectures, applications, resolution, and sampling rates.

architectures stand out for three important areas of applications. For example, the oversampling converter is exclusively used to achieve high resolution above 12-bit level at low frequencies. The difficulty in achieving better than 12-bit matching in conventional techniques gives a fair advantage to the oversampling techniques. For medium speed with high resolution, pipelined or multi-step ADCs are promising. At extremely high frequencies, only flash and folding ADCs survive, but with low resolution. Figure 2.2 is a resolution-versus-speed plot showing this trend [7]. As semiconductor process and design technologies advances, the performance envelop will be pushed further. The demand for higher resolution at higher sampling rates is a main driver of this trend.

Among many types of A/D architectures, the pipelined architecture has the advantages of lower power, high throughput and relatively high resolution. Hence, pipelined architecture poises as potential candidate architecture to challenge these limits. To achieve even higher speed, parallelism can to be introduced.

Figure 2.2: ADC architecture is a compromise between resolution and speed.

2.2 Flash (Parallel) ADC

The most straightforward of making an ADC is to compare the input with all the divided levels of the references simultaneously. Such a converter is called a flash ADC and the conversion occurs in one step. The flash ADC is the fastest among all ADCs. The flash ADC concept can be explained with a N -bit flash ADC as shown in Figure 2.3. When the continuous-time continuous-value input signal is applied, the input sample-and-hold (S/H) circuit first samples the signal and holds the sampled amplitude constant for a period of time. During this time, comparators compare the held signal with reference voltages generated from the resistor string and the resulting thermometer code from the comparator outputs is encoded into a digital binary representation. Then the S/H circuit samples a new input voltage and the whole conversion procedure repeats for the next sample.

The transfer curve of this ADC corresponds to the ADC with quantization error centered about $+ 1/2$ LSB as shown in Figure 2.4. To shift the curve

Figure 2.3: N-Bit Flash ADC.

by $1/2$ LSB so that the code transitions occur around the LSB values and the quantization error is centered around 0 LSB, the value of the last resistor in the string would have to be adjusted to $0.5R$ and the value of the MSB resistor, closest to the reference voltage, would have to be made $0.5R$ [8]. Then the first code transition would occur at $V_{in} = 0.0625$ V and the last code transition would occur at $V_{in} = 0.9375$ V and so the transfer curve would exactly match that of Figure 2.5.

The obvious advantage of this converter is the speed with which one conversion can take place. Each clock pulse generates an output digital word. The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N -bit output by only a few gate delays on top of that, so the process is very fast.

Figure 2.4: (a) Transfer curve for an ideal ADC and (b) its corresponding quantization error.

Figure 2.5: (a) Transfer curve for an ideal 3-bit ADC with (b) quantization error centered about zero.

However, the advantage of having high speed is counterbalanced by the doubling of area with each bit of increased resolution. In practical implementation, the limit is the exponential growth of comparators and resistors. For example, an N -bit flash consists of $2^N - 1$ comparators and 2^N resistors arranged as in Figure 2.3. Furthermore, for the Nyquist-rate sampling, the input needs an S/H to freeze the input for comparison. As the number of bits grows, the comparators bank presents a significant loading to the input S/H, diminishing the speed advantage of this architecture. Also the control of the reference divider accuracy and the comparator resolution degrades and the power consumption becomes prohibitively high.

Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators (especially at sampling rates greater than 50 MS/s), and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators, so the voltage reference has to source quite large currents (typically > 10 mA). As a result, flash converters with more than 10-bit resolution are rare. Flash ADCs are commonly used as coarse quantizers in the pipelined or multi-step ADCs. Table 2.1 shows the truth table of a 3-bit flash ADC.

2.3 Two-Step Flash (Subranging) ADC

Another type of flash converter is called the two-step flash converter or subranging converter. Instead of making all the bit decisions at once, resolving a few bits at a time makes the system simpler and more manageable. It also

Table 2.1: Truth Table of 3-Bit Flash ADC.

V_{in}	C7	C6	C5	C4	C3	C2	C1	B0	B1	B2
$V_{in} < 0.125$	0	0	0	0	0	0	0	0	0	0
$0.125 < V_{in} < 0.25$	1	0	0	0	0	0	0	0	0	1
$0.25 < V_{in} < 0.375$	1	1	0	0	0	0	0	0	1	0
$0.375 < V_{in} < 0.5$	1	1	1	0	0	0	0	0	1	1
$0.5 < V_{in} < 0.625$	1	1	1	1	0	0	0	1	0	0
$0.625 < V_{in} < 0.75$	1	1	1	1	1	0	0	1	0	1
$0.75 < V_{in} < 0.875$	1	1	1	1	1	1	0	1	1	0
$V_{in} > 0.875$	1	1	1	1	1	1	1	1	1	1

enables us to use a digital error correction concept. The simplest subranging ADC concept is explained in Figure 2.6 for the two-step conversion case. It is a straightforward subranging since one subrange out of the $2M$ subranges is chosen in the coarse M -bit conversion. Once one subrange is selected, the N -bit fine decision can be done using a fine reference ladder interpolating the selected subrange.

The basic block diagram of a two-step converter with digital error correction is seen in Figure 2.7. The operation of this two-step converter is as follows. The 4-bit MSB A/D determines the first four MSBs. To determine the remaining LSBs, the quantization error is found by reconvverting the 4-bit digital signal to an analog value using the 4-bit D/A and subtracting that value from the sampled input signal, this gives a residue. To ease the requirements in the circuitry for finding the remaining LSBs, the residue is first multiply by 8 using the gain amplifier and the LSBs are determined using the 7-bit LSB A/D. With this approach, rather than requiring 1024 comparators as in a 10-bit Flash converter, only 144 comparators are required for a two-step A/D. However, this

Figure 2.6: Coarse and fine reference ladders for two-step subranging ADC.

straightforward approach would require all components to be at least 10-bit accurate. To significantly ease the accuracy requirements of the 4-bit MSB A/D converter, digital error correction is commonly used and is discussed next.

The analog input V_{in} is first sampled and held steady by a sample-and-hold (S/H), while the flash ADC in stage one quantizes it to 4 bits. The 4-bit output is then fed to a 4-bit DAC (accurate to about 10 bits), and the analog output is subtracted from the input. This "residue" is then gained up by a factor of 8 and fed to the next stage (second stage). Because the bits from the first stage are determined at different points in time from the second stage, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note that as soon as a first stage finishes processing a sample, determining the bits and passing the residue to the second stage, it can start processing the next sample due to the sample-and-hold embedded in front of the stage. This action accounts for the high throughput.

Figure 2.7: An 10-bit two-step A/D converter with digital error correction.

Most modern two-step ADCs employ a technique called "digital error correction" to greatly reduce the accuracy requirement of the flash ADCs (and thus the individual comparators). In Figure 2.7, notice that the 4-bit residue at the summation-node output has a dynamic range one-sixteenth that of the original stage-one input (V_{in}), yet the subsequent gain is only 8. Therefore, the input to stage two occupies only half the range of the expected 4-bit range when there is no error in the first 4-bit conversion in stage one.

If one of the comparators in the first 4-bit flash ADC has a significant offset, when an analog input close to the trip point of this comparator is applied, an incorrect 4-bit code and thus an incorrect 4-bit DAC output would result, producing a different residue. But, as long as this gained-up residue doesn't over-range the subsequent 7-bit ADC, the LSB code generated by the second stage when added to the incorrect 4-bit MSB code will give the correct ADC output code. The implication is that none of the flash ADC in Figure 2.7 has to be as accurate as the entire ADC. In fact, the 4-bit flash ADC in first stage

requires only about 4 bits of accuracy.

The digital error correction will not correct for errors made in the second stage 7-bit flash conversion. However, any error made in the first stage is associated with the 4th bit in the 4-bit MSB. The explanation is as followed.

If the residue, Vq , after multiplying by 8 is within the range between $1/4 V_{FS}$ to $3/4 V_{FS}$ it then implies that the first stage has performed with no error. If the residue, Vq , after multiplying by 8 exceed $3/4 V_{FS}$ it then implies that the first stage has performed with an error, hence the digital correction works by subtracting 1 from the previous decision, e.g. if the 4 bits MSB read 1001, it will be corrected to 1000. On the other hand, if the residue, Vq , goes below $1/4 V_{FS}$ after multiplying by 8, then again it implies that the first stage has performed with an error, hence the digital correction works by adding 1 to the previous decision, e.g. if the 4 bits MSB read 1001, it will be corrected to 1010.

2.4 Pipelined ADC

The principle of subranging ADC can be pushed to the limit of having only one bit per stage. At this point, each flash ADC is nothing more than a simple comparator. Also, the data is transferred in a pipelined fashion: when the data is sent to the second stage, another sampled data is fed to the first stage. The result is a latency delay equal to the numbers of stages. A block diagram of a pipelined ADC is shown in Figure 2.8. The analog stage consists of a 2 bits flash ADC, a 2-bit DAC and an adder/gain stage. The output is called the residue and is sent to the next stage.

The term "pipelined" architecture refers to the ability of one stage to process

Figure 2.8: Typical Pipelined A/D Architecture.

2.4. Pipelined ADC

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Figure 2.9: Clock Issues in Pipelined ADCs.

data from the previous stage during any given clock cycle. At the end of each phase of a particular clock cycle, the output of a given stage is passed on to the next stage using the S/H functions and new data is shifted into the stage. This means that the digital outputs of all but the last stage in the pipeline must be stored in the appropriate number of shift registers so that the digital data arriving at the correction logic corresponds to the same sample.

Figure 2.9 shows a timing diagram of a typical pipelined ADC. The phases of the clocks to the S/H amplifiers are alternated from stage to stage such that when a particular S/H in the ADC enters the hold mode it holds the sample from the preceding S/H, and the preceding S/H returns to the sample mode. The held analog signal is passed along from stage to stage until it reaches the final stage in the pipelined ADC, in this case, a flash ADC.

2.5 Study of Previous Works

It is desirable to understand the performance of the ADC in the context of power, technology and performance. The ADC performance is often represented by a figure of merit, FOM which is defined as $FOM = 2N \times f_s / P$, where N is the number of bits, f_s is the sampling rate in MS/s and P is the power consumption in mW. The higher the FOM is, the more bits are obtained at higher speed with lower power.

In general, the main criteria of choosing ADC architecture are resolution and speed, but auxiliary requirements such as power, chip area, supply voltage, latency, operating environment, or technology often limit the choices. The current trend is toward low-cost integration without using expensive discrete technologies such as thin film and laser trimming. Therefore, a growing number of ADCs are being implemented using VLSI technologies such as CMOS or BiCMOS.

Table 2.2 shows the recent research for high-speed ADC with different CMOS process technologies. It is observed that their resolutions are between 6-10 bits and at a conversion rate of higher than 100 MHz. There is always a tradeoff between conversion rate and resolution. For example, the one with 1000 MS/s conversion rate only attains 6-bit resolution, whilst others with 10-bit resolution only have conversion rate in the range of 100 MS/s $\sim$ 200 MS/s.

For low resolution of less than 6-bit, the flash architecture is considered the best. Even gigahertz rates can be achieved using the state of the art CMOS technologies. It is clearly stated that the fastest architecture can provide 6-7 bits resolution range with a sampling rate of several hundred MHz or above

Table 2.2: Performance of High-Speed ADCs.

References	Conversion Rate [MS/s]	Resolution [Bit]	Supply Voltage [V]	Power Consumption [mW]	CMOS Process	Architecture	FOM
[2]Wang-2005	12	10	1.2	3.3	90nm	Pipelined	3723.6
[9]Grace-2004	80	12	2.5	755	0.25um	Pipelined	434.0
[10]Sumanen-2001	200	10	3.0	280	0.5um	Parallel Pipelined	731.4
[1]Andersen-2005	110	12	1.8	97	0.18um	Pipelined	4644.9
[11]Pan-2000	50	12	3.3	850	0.6um	Pipelined	240.9
[12]Chiu-2004	12	14	1.8	98	0.18um	Pipelined	2006.2
[13]Opris-2000	5	14	5.0	320	0.5um	Pipelined	256.0
[14]Arias-2004	40	10	2.5	12	0.25um	Pipelined	3413.3
[15]Yoo-2001	1000	6	2.5	66.87	0.25um	Flash	957.1
[16]Yu-2001	900	6	2.5	450	0.25um	Pipelined	128.0
[17]Kim-2001	200	8	3.0	210	0.35um	Pipelined	243.8
[18]Nairn-2000	100	10	3.0	310	0.35um	Pipelined	330.3
[19]Yoo-2004	120	10	2.5	208	0.25um	Pipelined	590.8
[20]Li-2004	100	10	1.8	67	0.18um	Pipelined	1528.4
[21]Yoon-2000	125	8	3.3	110	0.35um	Folding	290.9
[22]Taft-2001	100	8	2.2	75	0.4um	Subranging	341.3
[23]Wang-2000	150	8	3.3	395	0.6um	Subranging	97.2
[24]Ou-2005	2.5	9	1.0	15	0.35um	Pipelined	85.3

GHz.

Folding ADCs can be realized without linear precision subtraction and the circuit area is rather small. However, the speed of folding ADC is limited by the folding circuit despite achieving higher resolution than subranging. For sampling rate 100 MS/s and above, the resolution is limited to 8-bit. However, subranging ADC can achieve sampling frequency higher than 100 MS/s. The next generation WLAN radios are required to be low cost and flexible if they are to meet a variety of emerging standards. For wireless communication applications, they demand low power converters that can accept variable input bandwidths ($\sim$ tens of MHz) at moderate of 8-10 bits resolution. Pipelined architectures in deep sub- micrometer CMOS technologies are viable candidates for achieving such converters. They benefit from calibration schemes that can increase in sophistication with CMOS process scaling.

Therefore, in view of sampling rate, technology and power consumption, the pipelined ADC is identified as one of the good choices for compromising the performance parameters in high-speed ADC design [3]. The table has confirmed the viability of effective ADC design in sub-micrometer CMOS process. Hence, it leads to the investigation of improved pipelined ADC design as one of the main objectives in this research work.

Chapter 3

Study of Pipelined A/D Converter Architecture

3.1 Introduction

Typically, each stage of a pipelined converter employs a Flash Quantizer and a Multiplying Digital-to-Analog Converter (MDAC) that performs also the Sample-and-Hold function, as shown in Figure 3.1. Digital correction logic is often employed in order to relax the specifications of the basic building blocks of the Flash Quantizer as explained further on in this Chapter. A generic stage i processes the input signal on two phases and it is responsible for the extraction of B_i bits. In the first phase, the input voltage is sampled and the corresponding value is stored in the MDAC, while the B_i quantization is performed by the Flash Quantizer. In the second phase, the residue voltage, $V_{res,i}$, obtained by subtracting the D/A reconstruction of the coarse quantization from the held input voltage $V_{in,i}$, is amplified by a factor smaller or equal to 2^{B_i} . This amplified

Figure 3.1: Block diagram of a generic stage i in a pipelined ADC architecture.

signal, is then held and applied to the next stage where, identical operations are performed. In this chapter, how different error sources affect the performance of the pipelined converter are studied.

3.2 Error Sources in Single Pipelined

The following four non-ideal error sources can affect the performance of the multi-step or pipelined ADCs: comparator offsets, nonideal DAC reference level, gain error of the residue amplifier and inaccurate settling of the residue amplifier. The offset of the residue amplifier does not affect the linearity but it appears as a system offset. Among these four error sources, the first three are static but the residue amplifier settling is dynamic. If the residue amplifier is assumed to settle within one clock phase, three static error sources are limiting the linearity performance [25].

Figure 3.2: Transfer curve of a pipelined stage with comparator offset.

3.2.1 Comparator Offsets

The accuracy limitation of most ADC architectures is a function of various forms of comparator offset errors, which limits the resolution of the ADC. However, a 1.5 bit per-stage pipelined ADC can be made insensitive to comparator offset errors, by resolving 1 bit per stage, and reserving 0.5 bits for error correction, resulting in relaxed offset requirements for the comparator. One extra bit resolution in flash ADC allows the comparator offset to be $\pm V_{ref}/4$ [26].

Figure 3.2 shows the transfer curve of a pipelined stage with comparator offset. Everything but the comparator threshold is assumed to be ideal. We see that a wrong decision is made and the amplified residue of this stage is out of the range of the input of next stage. As a result, missing codes occurs.

Figure 3.3: Transfer curve of a pipelined stage with nonideal DAC references.

3.2.2 Nonideal DAC Reference Level

After the input is digitized by the flash ADC, a DAC is used to convert the code back to analog signal. The level of the analog signal depends on the level of the DAC reference levels. The shift of DAC reference levels results in out-of-range output and hence missing codes. Figure 3.3 shows the transfer curve of a pipelined stage with nonideal DAC reference levels. The source of the nonideal DAC reference levels is capacitor mismatch.

3.2.3 Gain Error of Residue Amplifier

The difference of the input signal and the output of DAC is amplified by a opamp-based switch capacitor circuit. The gain is determined by the capacitor ratio and opamp DC gain. Figure 3.4 shows the transfer curve of a pipelined stage with nonideal residue gain.

Figure 3.4: Transfer curve of a pipelined stage with nonideal residue gain.

The resolution limits of the ADC, then are set by thermal noise limits (kT/C) and inter-stage amplification error, which can generally be classified into two sections; capacitor mismatch errors and amplifier errors (Input referred offset, incomplete settling, and finite gain errors).

As discussed above, one of the dominant sources of error in a pipelined ADC is capacitor mismatch. However this source of error has some characteristics which make it suitable for calibration in a modern ADC scheme. Firstly, capacitor mismatch errors result in a linear error, meaning that if the mismatch can be measured, then the results of this error will be predictable over the entire voltage range of the amplifier.

Secondly this is predominantly caused by a physical size mismatch which will not drift with temperature, supply, or clock speed variation. These two characteristics yield an error that is very suitable for calibration correction, and several previous works have demonstrated this. Hence, in a calibrated system, the capacitor sizes can be reduced until the thermal noise starts to dominate.

Figure 3.5: Over-range 2-bit residue versus input: (a) ideal and (b) ADC errors.

3.2.4 Digital Error Correction Techniques

Any multi-step or pipelined ADC system can be made insensitive to the ADC error if the ADC error is digitally corrected. The residue normally going out of the full range can still be digitized by the following if the residue amplifier gain is reduced. That is, if the residue amplifier gain is set to $2N - 1$ instead of $2N$, the residue plots are as shown in Figure 3.5. If the residue is bounded with the full range 0 to V_{ref} , the inner range from $V_{ref}/4$ to $3V_{ref}/4$ is the normal conversion range, and two redundant outer ranges are used to cover the residue error resulting from the inaccurate coarse conversion. Now the problem is that this redundancy requires extra resolution to cover the overrange. The half ranges on both sides are used to cover the residue error in this 2-bit case. That is, one full bit of extra resolution is necessary for redundancy in the 2-bit case. However, the amount of redundancy depends on the ADC error range to be corrected in the multi-bit case. In general, it is a tradeoff between comparator resolution and redundancy.

The range marked as B is the normal range, and A and C indicate the

Figure 3.6: Half-bit shifted 2-bit residue versus input: (a) with and (b) without ADC threshold-level shift.

correction ranges in Figure 3.5(b). The digital correction works by subtracting 1 from the previous decision if the residue exceeds $3V_{ref}/4$, as in the case marked as A. on the other hand, if the residue goes below $V_{ref}/4$, as in the case marked as C, 1 is added from the previous decision. Although the digital subtraction is simple, biasing the ADC threshold levels by half the ideal interval has an advantage. Figure 3.6 compares the residue plots for two cases with and without the ADC threshold shift by $V_{ref}/8$. This is to fully utilize the ADC conversion range from 0 to V_{ref} . The shift of $V_{ref}/8$ makes the residue start from 0 and end at V_{ref} in Figure 3.6(b), contrary to the previous case where the residue starts from $V_{ref}/4$ and ends at $3V_{ref}/4$. This results in saving one comparator. The former case needs $2N - 1$ comparators, while the latter case needs $2N - 2$. The only mirror issue is that the latter exhibits a half LSB systematic offset due to this shift.

This half-bit-level shift makes the ADC error occur only with the same polarity. As a result, only the addition is necessary for digital correction in the case of Figure 3.6(b). This half interval shift is valid for stages resolving any number

Table 3.1: Comparison of original coding and digital error correction with modified coding.

	Original Coding	Digital Error Correction with Modified Coding
Input Range	$[-1, 1]$	$[-1, 1]$
Flash ADC Threshold Levels	$-1/2, 0, 1/2$	$-1/4, 1/4$
DAC Reference Levels	$-3/4, -1/4, 1/4, 3/4$	$-1/2, 1/2$
Digital Codes	00, 01, 10, 11	00, 01, 10
Stage Gain	4	2
Bits/Stage	2	2

of bits. Overall, the digital error correction enables fast data conversion using inaccurate comparators. However, the DAC resolution and the residue gain error still remain as the fundamental limits in multi-step and pipelined ADCs. The currently known ways to overcome these limits are either trimming or self calibration. Table 3.1 shows the comparison of the original coding and digital error correction with modified coding.

Figure 3.7 shows the effect of comparator threshold offset and nonideal DAC reference level with digital error correction. From the plot we see that the maximum offset we can tolerate is $1/4 V_{ref}$. The requirement of the accuracy of the comparators is thus greatly relaxed.

3.3 Summary

In this chapter, the function and error sources in a single pipelined stage are discussed. The errors discussed include, static errors such as comparator offsets, non-ideal DAC reference level, gain error of residue amplifier and dynamic error

Figure 3.7: Effect of Comparator Threshold Offset And Nonideal DAC Reference Level With Digital Error Correction.

such as inaccurate settling of residue amplifier. The principle of digital error correction technique is also reviewed. With digital error correction, the influence of errors in the comparators is significantly reduced. Hence the dominating error sources are DAC errors and errors in the residue amplifier.

Chapter 4

Mixed-signal Circuit Design in Deep Sub-micron Processes

4.1 Introduction

Mixed-signal design on more advanced process (0.13 μm and below) poses a new host of design issues that must be considered during the initial architectural phase as well as during the implementation cycle. Many new products incorporate analog and mixed-signal components along with larger digital circuits. Microprocessors are a good example of this trend, since they typically include data converters, phase-locked loops (PLLs) and frequency synthesizers. Given that the bulk of the die area is comprised of high speed digital logic, the process is typically developed to address issues associated with digital circuits. This process choice forces analog and mixed-signal designers to develop specialized methodologies to ensure that circuits can meet stringent requirements without the advantage of specialized process. An overview of the various issues

that must be considered to successfully design analog and mixed-signal integrated circuits (ICs) on deep-submicron processes is discussed in this chapter, along with recommendations for avoiding various pitfalls [27].

4.2 Design Considerations

For the technology to continue to progress towards smaller and smaller geometries, several significant advancements have been implemented. These advancements include extremely thin gate oxide [physical thickness or equivalent oxide thickness (EOT) ranges from 1.5 to 2.2 nm for 130-nm node and 1.1 to 1.7 nm for the 90-nm node], shallow source and drain diffusions, shallow trench isolation, multiple oxide thickness, multiple threshold voltages for a given oxide thickness, and multiple metal thickness. All of these process advancements have allowed for an explosive growth in the semiconductor marketplace but at a price of increasing complexity in the design methodology and tools required to develop new products successfully. Some of the issues facing mixed-signal designers include:

- Model accuracy
- Leakage current (both source-drain and gate)
- OD stress effects
- Process variation (device to device, die to die, wafer to wafer, lot to lot and fabrication to fabrication)
- Supply headroom effects

- Device performance
- Noise isolation
- Power

4.3 Device Modeling

Device modeling has become more complex to accurately reflect the physical performance of circuits given the aggressive design targets for the next-generation processes. At 90 nm and beyond, enhanced device models are required to design mixed-signal ICs successfully. These models must incorporate several new factors neglected on earlier generations, such as 0.13 μm , in addition to enhancing the modeling of current parameters. These model issues include:

- Shallow trench isolation (STI) stress-induced effect
- Gate leakage current
- Gate-induced drain leakage (GIDL)
- Stressed-induced diode leakage
- Polysilicon gate depletion effects
- Shallow source-drain series resistance
- Negative bias temperature instability (NBTI)

4.4 Passive Components

Passive components, including resistors, capacitors, varactors and inductors, are frequently used in analog and mixed-signal design. Resistors have not changed significantly with the shrinking process except for a resistivity shift from the previous generation because of changing doping densities. The primary concern is always with obtaining accurate models and understanding the variability with process, temperature, and applied voltage. In most cases, resistors need to be modelled as multiple resistances to accurately reflect end resistance as well as parasitic capacitances.

Capacitors can offer a host issues with shrinking technologies, depending on the structure used. In some cases, metal-insulator-metal (MIM) capacitors are available if a mixed-signal process is being used. These are typically constructed using a thin nitride insulator between two metal layers and result in a capacitance of approximately 1 to 4 fF/ μm^2 . One of the major benefits of MIM capacitors is their high Q value (up to 150) since the parasitic resistance can be minimized and their capacitance is constant regardless of the voltage applied.

Another common capacitor structure is the metal comb capacitor, which is really just a variation on metal plate-metal plate capacitors. The comb structures can produce a high capacitance per unit area with a high Q value since they are constructed from metal. These capacitors rely on the interconnect capacitance inherent in the close proximity of two adjacent metal lines. A single layer of metal may be used, if the absolute value of the capacitance is critical although the capacitance per unit area may not be as high as in multilayered capacitors. The use of low- k dielectric will also reduce the capacitance per unit area of these structures. The effects of the copper process must also be consid-

ered when designing metal layer capacitors since metal density rules must be followed and metal thickness variation as a function of the metal density must be considered when calculating the true capacitance value. Metal density effects can easily add 2 to 5% error in metal thickness. Given all of the variability of metal capacitors, they are typically used in applications where absolute value is not critical. Even in these cases, it is best to include test wafers in any process characterization, to verify the actual capacitance value. Additional structures may be found in [28] and [29].

4.5 Design Methodology

To design mixed-signal circuits successfully for advanced processes requires that careful architecture studies be performed prior to implementation. Several important steps should be taken to ensure that design of specific circuits is possible in these processes. To ensure that the design of specific circuits is possible, a characterization of test structures of NFET (thin oxide) transistor is carried. This device characterization test is to investigate the model accuracy and the dependence of device performance on layout

In this work, a series of NFET transistors schematics are simulated using the device models provided from the foundry. Several different layouts of transistor were drawn in CSM 90 nm Low Power CMOS process. The layout of theses transistors are then tape out to the foundry.

The key in this study is to keep the cells simple to allow the process to be evaluated. This aspect is especially important as the test chips are run early during the process development when models are immature and potentially

inaccurate. It is also important to look at device-matching issues for a range of device sizes and configurations to evaluate proximity effects. This allows trade-off studies to be made when deciding which devices will be used for a certain function. Although test chips are the best way to verify a design, having a series of schematics that can be simulated using device models can provide critical insight into potential issues with the process.

A comparison is made between the simulation results and the measured results. It is found out that both matches well except at the end of high VDD. Where breakdown is seen in the measured results but not in the simulated results.

4.6 Active Components

4.6.1 Design Using Thin Oxide Devices

One of the key decisions that must be made is whether to design the analog and mixed-signal portions of the overall system using thin oxide devices or one of the thicker oxide devices. Neither approach is without its drawbacks. Consider the option of using thin oxide devices. This will require that all the device issues discussed previously be considered to ensure that the design can be implemented successfully.

Supply headroom can become a major issue. Realistically, the threshold voltage on these more advanced processes is approaching 0.3 V. If the supply voltage is on the order of 1.0 to 1.2 V, a designer must keep all circuits below three threshold voltages once temperature and supply variation are included.

Figure 4.1: The short-channel NFET I_{ds} - V_{ds} characteristics in CSM 90 nm Low Power process for several different values of V_{gs} . The solid curve shows the measured results from test structures and the dotted line exhibits the simulated results from available models.

Figure 4.2: The short-channel NFET I_{ds} - V_{gs} characteristics at $V_{ds}=1.2V$ in CSM 90 nm Low Power process.

Figure 4.3: The short-channel NFET G_m - V_{gs} characteristics in CSM 90 nm Low Power process.

Some supply headroom may be recovered by using lower-threshold thin oxide devices (assuming that this is an option for the process), but this approach results in added complexity in the process corners that must be simulated. If two devices are being used with only the threshold voltage different, the models should be partially correlated. Both devices should experience similar poly critical dimension (CD) control and oxide thickness, but the threshold voltage implant can be different but is still partially correlated. Understanding how the models correlate can become difficult. For this reason, it is best to avoid using multiple threshold devices in critical circuits if at all possible.

Some of the benefits of using thin oxide devices include a possible reduction in the total area of the mixed-signal block, assuming that a portion is digital, such as the digital correction logic block of a pipelined A/D converter.

4.6.2 Design Using Thick Oxide Devices

A second option is to use the thicker oxide devices for the analog blocks and possibly some of the digital blocks and then level-shift to the lower core voltage. This approach can increase the headroom for an analog circuit, permitting cascoding of current mirrors and gain stages to increase the noise immunity. Gate leakage problems are reduced significantly, as is the source-drain leakage current. Two problems can occur with this approach. First, the analog or mixed-signal block will probably interface with the core at some point. This will require a level shifter to be implemented. For a data converter, these level shifters may not pose a problem, but the entire system must be considered.

4.7 Summary

In this work, after careful consideration of the factors above, thick oxide devices are chosen for all the analog and digital blocks. Level shifters are then used to bring the digital output voltage of 2.5 V to a core voltage of 1.2 V.

Chapter 5

Proposed Subranging Pipelined A/D Converter Architecture

5.1 Introduction

This chapter describes the architectural design of the proposed Subranging Pipelined A/D converter.

5.2 Proposed Architecture Design

It is well-known that the flash ADC is the fastest architecture. This architecture design employs parallelism to improved speed. Instead of a single-stage flash ADC design, coarse and fine quantizers can be employed as shown in Figure 5.1.

To design an 8-bit pipelined ADC, 8 stages are required. This results in a latency delay of 8. However in this proposed architecture, by employing parallelism, the coarse ADC (3-bit flash ADC) can be designed to synchronize

Figure 5.1: Coarse and fine quantizers.

with the fine ADC (stage 1 of pipelined architecture). Hence, effectively there is only 6-latency delay for 6 stages instead of 8. To build pipelined ADC's with large tolerance to component nonidealities, redundancy is introduced by making the sum of the individual stage resolutions greater than the total resolution. When the redundancy is eliminated by a digital correction algorithm, it can be used to eliminate the effects of sub-ADC nonlinearity and interstage offset on the overall linearity [30] [31]. Figure 5.2 shown the block diagram of the proposed ADC architecture.

The coarse quantizer block is a simple 3-bit flash ADC, which quickly compares the input with the reference voltages to give 8 resistive segments. It generates the first 3 MSBs. These 3-bit MSBs control the fine multiplexer (FMUX) so as to select the proper resistor segment from the reference ladder for fine conversion. Finally, the pipelined fine ADCs compare the input voltage with the fine reference voltages to generate the 6-bit LSBs. Stage 6 only includes a flash ADC. With an output register, the total 8-bit output is achieved which represent the input voltage relative to the reference voltages.

Figure 5.2: Proposed ADC architecture.

The overlap between the coarse and fine conversion ranges and the corresponding digital correction algorithm are described. In this 8-bit A/D converter, it is assumed that the offset of the coarse-quantizer comparators never exceeds 32 LSB ($1V/8 = 0.125 \text{ mV}$) and the fine-quantizer is designed for 6-bit resolution in order to digitize as large as 64 LSB.

Unlike a two-step ADC, the fine and coarse bits are generated synchronously. This allows the pipelined architecture to have speed comparable to flash ADC. However, performing the operations in parallel introduces timing challenges, since the coarse bits reach the output before the fine pipelined bits do. To correct this, a correction logic block is used after the coarse ADC. The coarse ADC is designed to resolve the three most significant bits as illustrated in Figure 5.3. Voltage comparators are used in a traditional flash architecture. The correction logic block resolves timing differences that occur between the output of the

Figure 5.3: Synchronization between coarse and fine bits.

fine and coarse bits. In this work, a bit-synchronization scheme is proposed to correct the errors caused by the delay difference between the coarse and fine quantizer paths.

In this way, the three most significant bits are not derived directly from the coarse quantizer; instead, they are determined by the bit-sync signal, which comes from the fine quantizer, thus the offsets of the coarse quantizer comparators are not critical.

Chapter 6

Design of a 8-bit 100 MS/s Subranging Pipelined A/D Converter

6.1 Introduction

This chapter describes the circuit implementation of the proposed 8-bit 100 MS/s Subranging Pipelined A/D converter architecture in 90 nm Lower Power CMOS process. The system consists of an input Sample-and-Hold amplifier (SHA) followed by a 3-bit coarse ADC and a 6-bit fine pipelined stages. The design can be divided into two separated tasks: a 3-bit coarse ADC using flash architecture and a 5-stage 6-bit fine ADC employing a minimum 1.5-bit per stage architecture. All issues related to designing switch-capacitor blocks such as capacitance values, amplifier design and switch sizing are addressed in this Chapter as well.

Table 6.1: Specifications for the A/D conversion system

Parameter	Target
Technology	90 nm Low Power CMOS
Resolution	8 Bits
Sampling Frequency	100 MS/s
Analog Power Supply Voltage	2.5 V +/- 10%
Digital Power Supply Voltage	1.2 V +/- 10%
Differential Input Range	1.0 V _{pp}
Current Consumption	25 mA typical
Core Cell Area	0.8 mm ²
Spurious Free Dynamic Range	> 45 dB
DNL	+/- 0.5 LSB
INL	+/- 1 LSB

6.2 Specifications and Architecture of the Overall Conversion System

6.2.1 Specifications

A 90 nm Lower Power CMOS process provided by Chartered Semiconductor was the target technology. The system should operate with a 2.5 V power supply within a temperature range from -40 to +125 °C. The main specifications for the A/D conversion system are summarized in Table 6.1.

6.2.2 Architecture

Figure 6.1 shows a simplified block diagram of the overall architecture of the 8-bit A/D conversion system. The system consists of an input front-end fully differential SHA followed by 3-bit coarse ADC and a 6-bit fine ADC. The entire design can be divided into two independent designs. The most critical part

Figure 6.1: Proposed 8-bit Subranging Pipelined ADC.

employs a 3-bit flash ADC. The second part comprises a 5-stages 6-bit fine pipelined ADC, where each stage employs a 1.5-bit Flash Quantizer and a 1.5-bit MDAC, except the last stage which uses a 2-bit Flash Quantizer.

6.3 Design of the Basic Building Blocks

6.3.1 Design of the 6-bit 100 MS/s Fine ADC

As shown in Figure 6.2, the 6-bit fine ADC uses an architecture employing 5 stages with a stage resolution of 1.5 bit in order to minimize overall power dissipation [32]. The basic building blocks are the 1.5-bit MDAC and the 1.5-bit Flash Quantizer which comprise, respectively, one amplifier and two comparators, except the last stage, which is a 2-bit Flash Quantizer using 3 comparators.

With an inter-stage gain of 2 in the 1.5-bit MDAC during the residue amplification phase, each stage contributes 1 bit towards the overall resolution and the remaining 0.5 bit is redundant to eliminates the effects of the 1.5-bit Flash Quantizer non-idealities and inter-stage offset on overall linearity. Digital cor-

Figure 6.2: Architecture used in the 6-bit Fine ADC.

rection logic eliminates the redundancy producing the expected 6-bit output bits.

In this fine pipelined A/D converter, in order to reduce design complexity, the scaling of the capacitance values from the first 1.5-bit MDAC up to the last 1.5-bit MDAC of the chain was not used. Hence, the overall power dissipation of the conversion system could be further reduced.

6.3.1.1 The 1.5-bit MDAC

Figure 6.3 shows the schematic of the 1.5-bit MDAC, which consists of an opamp, four equal sized capacitors and 15 switches. Correlated double-sampling techniques are being employed here.

ϕ_1 and ϕ_2 are two non-overlapping clocks and ϕ_{1D} is a delayed version of ϕ_1

Figure 6.3: Schematic of the 1.5-bit MDAC.

but still non-overlapping with ϕ_2 . By turning off $S1$ switches first, the signal processing is only affected by the charge injection from these switches and not by the charge injection from switches $S3$ or $S4$ since the input nodes of the opamp become effectively high impedance nodes.

During ϕ_1 (sampling phase) the two pairs of capacitor C_S and C_F sample the difference between the input differential voltage, V_{in} , and the offset voltage of the opamp, V_{offset} generated at the output of the amplifier by the auto-zero configuration. Thus, these capacitors are charged up to $V_{in} - V_{offset}$. Next, during ϕ_2 (residue amplification phase), the opamp is taken out of auto-zeroing mode, and the capacitors, C_F , form the feedback loop of the opamp while the bottom plates of the sampling capacitors are connected to each other, to the positive reference or to the negative reference depending on the state of digital inputs X, Y, Z . Assuming $C_S = C_F = C$ and a non-ideal opamp with finite DC gain, A and the offset voltage, V_{offset} , at the end of ϕ_2 , the value of the amplified residue to be processed by the next stage of the pipelined is given approximately by:

$$V_{out} = \begin{cases} 2 \cdot V_{in} + V_{ref}, & \text{if } -V_{ref} < V_{in} < \frac{-V_{ref}}{4} \iff Y = 1, \\ 2 \cdot V_{in}, & \text{if } \frac{-V_{ref}}{4} < V_{in} < \frac{+V_{ref}}{4} \iff Z = 1, \\ 2 \cdot V_{in} - V_{ref}, & \text{if } \frac{+V_{ref}}{4} < V_{in} < V_{ref} \iff X = 1 \end{cases} \quad (6.1)$$

Where X, Y and Z are the encoded digital outputs provided by the 1.5-bit Flash Quantizer.

Noise consideration is also an important factor. The preceding SC gain am-

plifier uses correlated double-sampling (CDS) techniques to minimize errors due to finite offset voltage, $1/f$ flicker noise, and finite opamp gain. The elimination of the input offset voltage of the opamp is important for reducing $1/f$ noise. Large $1/f$ noise can be a dominant noise source and can therefore be troublesome. However, when a circuit cancels DC offset voltages, the circuit has, in fact, a high-pass response from the input terminals of the opamp to its outputs. Thus, the $1/f$ noise is also a high-pass filtered and hence reduced.

A fundamental limitation now on the SC circuits is imposed by the thermal noise in the circuit. The noise voltage power spectral density of a switch is

$$S_v(f) = 4kTR_{on} \quad (6.2)$$

where R_{on} is the switch on-resistance, k is the Boltzmann's constant and T is the absolute temperature. The total noise power can be calculated as the spectral density times the noise bandwidth, i.e.

$$v_n^2 = S_v(f) \times BW_n = S_i(f) \cdot \frac{\omega_{-3dB}}{4} = 4kTR_{on} \cdot \frac{R_{on}}{4C_s} = \frac{kT}{C_s} \quad (6.3)$$

where BW_n is the noise bandwidth and C_s is the sampling capacitor. Assuming a sinusoidal input signal and the signal power can be calculated as [33]

$$v_{in,rms}^2 = \frac{v_a^2}{2} \quad (6.4)$$

where v_a is the amplitude of the sinusoid.

The dynamic range (DR) of the ADC can be calculated as

$$DR = \frac{v_a^2}{2kT} \cdot C_S \quad (6.5)$$

The minimum size of the capacitors C_S and C_F is dictated, on the one hand, by the KT/C thermal noise and, on the other hand, by the matching accuracy consideration. In this design, the first 1.5-bit MDAC in the fine ADC must satisfy the expression

Where $T = 398.15$ K, $V_{ref} = 1$ V and $N = 7$. Due to thermal noise constraints, the capacitance values of C_S and C_F can be made extremely small, to guarantee a minimum matching accuracy compatible with 6 bits of resolution, capacitance values of 250 fF are used for C_S and C_F .

To minimize the thermal noise generated from the opamp, n-channel input transistors are used instead of p-channel input transistors.

In order to achieve large output swing using a power supply of 2.75 V (worst case), with a nearly constant DC gain larger than 60 dB, a folded-cascode OTA was preferred to telescopic-cascode topology with a single current branch. It allows the DC level of the output signal to be the same as the DC level of the input signal. For controlling the output common-mode voltage, a switched-capacitor circuit was employed.

6.3.1.2 Switches

Switches are used to select different inputs, enable or disable feedback and to short outputs together to hasten overdrive recovery. The voltages that the switches pass are typically near 1.25 V in magnitude, or mid-supply. Thus, complementary switches were used to minimize switch resistance, as shown in

Figure 6.4: A complementary switch.

Figure 6.4. An added benefit is that complementary switches partially cancel charge injection, which is a substantial source of error, particularly at the input because any differential error gets amplified as if it were a signal. At one particular input voltage, charge injection cancellation is perfect, but at other input voltages the cancellation is less complete. The width of the NMOS transistor was selected to make the voltage about 1.25 V, reducing the circuit sensitivity to voltage-dependent charge injection.

6.3.1.3 The 1.5-bit Flash Quantizer

As previously mentioned, in a pipelined ADC, the function of the Flash Quantizer is to convert the held input of the previous stage into a low-resolution digital code. Typical N -bit Flash structures employ a resistor-string for the division of the reference voltage for defining the decision levels combined with $2^N - 1$ comparators and hence, a 1.5-bit Flash Quantizer uses only 2 comparators in its implementation. A 1.5-bit pipelined stage is shown in Figure 6.5.

In high resolution A/D converters, precision comparators consume DC power

Figure 6.5: A 1.5-bit Pipelined Stage.

since low-offset pre-amplification stages are required to amplify the signal before an accurate comparison is made. These precise high-speed comparators typically have at least one pre-amplification stage followed by a positive-feedback track-and-latch stage [33] and they are usually known as latched comparators. In pipelined stages with stage resolutions below 3 bits, a dynamic latched comparator can be used and, hence, its static power dissipation is saved. For a 1.5-bit Flash Quantizer a comparator offset up to $\pm V_{ref}/4$ can be corrected through digital correction. Therefore, with the differential reference voltage, $V_{ref} = 1$ V used in this conversion system, an offset in the comparators up to ± 250 mV can be tolerated.

In Figure 6.5, the threshold voltages for the two comparators are $\pm V_{ref}/4$. In this design, the differential V_{ref} is 1 V and its common-mode voltage is 1.25 V. Thus, the corresponding reference voltages for V_{ref+} and V_{ref-} in Figure 6.3 are 1.5 V and 1 V respectively.

Figure 6.6: A comparator block diagram.

Figure 6.7: A differential difference preamplifier.

Figure 6.6 shows the schematic diagram of a comparator used in all the pipelined stages. The comparator is composed of a single stage pre-amplifier, followed by a regenerative latch [34]. A simple differential-difference amplifier (DDA) [35] [36] is used here as the pre-amplifier. The pre-amplifier is used to minimize the effect of kickback noise. In order to maximize the speed of the comparator, this pre-amplifier has a low gain differential pair with diode connected PMOS loads. This identical pre-amplifier is used for all the comparators in the design. Figure 6.7 shows the topology of this pre-amplifier. Common-mode feedback is not necessary because the diode connected loads cause the outputs voltages to nominally sit at $V_{DD} - (V_{GS} - V_{TH}) = 1.25$ V. The differential gain of a diode-connected single stage op-amp is given by

$$A = \frac{g_{m1}}{g_{m7}} = \sqrt{\frac{\mu_n \frac{W_1}{L_1}}{\mu_n \frac{W_7}{L_7}}} = 2 \quad (6.6)$$

A regenerative latch was selected for this design. The advantage of this kind of latch is that there is no static power dissipation. Figure 6.8 shows the topology of the latch circuit. It consists of an input amplifier whose output is feed to a clocked latch. The output are pre-charged when V_{clk} is low, removing possible memory effects at the expense of extra power. The regeneration from the cross-coupled transistors, both NMOS and PMOS, make the latch fast. A potential downside of the latch architecture is that the data from the latch is only valid while V_{clk} is high. Symmetric buffer inverters were added to the regenerative nodes to increase the speed of switching the load capacitance.

Figure 6.8: A regenerative latch.

6.3.2 Design of the 3-bit 100 MS/s Coarse ADC

6.3.2.1 The 3-bit Flash Quantizer

As described in Chapter 2, a typical architecture of a 3-bit Flash Quantizer requires a bank of 7 comparators to achieve 3 bits of resolution. Fully differential comparators are required in order to filter out even-number harmonic distortions. In this structure, shown Figure 6.9 in the bank of comparators compares the differential input voltage, V_{in} , with a set of 7 differential reference tap voltages, obtained through a resistive voltage divider employing 8 resistors. The outputs of the comparators produce a thermometer-code, which is subsequently converted into binary using a digital encoder.

Figure 6.9: 3-bit Flash Quantizer architecture.

6.3.2.2 Digital Logic Design

However, this kind of architecture usually suffers from a critical problem normally called "bubbles". For fast input signal, small timing differences between the response time of the comparators and the intrinsic offset voltages in the comparator can produce a "0" near the top of the column of "1s" thermometer code, which is called a "Bubble" in the thermometer code. A bubble detector (and bubble suppressor) can simply be implemented with a three-input digital NOR gate. As illustrated in Figure 6.10, this method can easily suppress a single bubble that may exist, avoiding the possibility of generating erroneous output codes. Then a ROM encoder, Figure 6.11 is employed to convert the thermometer code into binary code.

Figure 6.10: (a) Thermometer-code without bubble; (b) Thermometer-code with one bubble.

Figure 6.11: ROM encoder.

Chapter 7

Design Methodology, Results and Discussions

7.1 Introduction

In the previous chapters, the proposed subranging pipelined A/D architecture was discussed. In this chapter, the simulation results of the proposed architecture based on behavioral modeling was presented. This is to highlight and validate the applicability of the top-down design methodology.

7.2 Top-Down Design Methodology

A well designed top-down design process methodically proceeds from architecture to transistor-level design. Each level is fully designed before proceeding to the next and each level is fully leveraged in the design of the next. In doing so, this acts to partition the design into smaller and well defined blocks [37]. The

flow chart of top-down design approach is given in Figure 7.1.

Traditionally, analog and mixed signal blocks modeling, as data converters, has been realised at device level or at a low functional level. This allows accuracy and good modeling of the non-ideal effects presented in the data converter (noise, distortion, mismatching, etc) but the simulation time increases drastically. Moreover, technology and architecture independence can be lost. However, with the increasing complexity of designs, the need for accurate and speedy models has produced a change to the current trend towards high functional level designs. The main advantage of the behavioral level description is the reduction in the simulation speed and the process independence [38].

Following a top-down design methodology also reduces the impact of changes that come late in the design cycle. If, for whatever reason, the circuit needs to be partially redesigned, the infrastructure that was put in place as part of the methodology allows the change to be made quickly. The models can be updated and the impact of on the rest of the system can be quickly evaluated. The simulation plan and infrastructure for mixed-level simulations is already available and can be quickly applied to verify any changes.

In the primitive top-down design process commonly used today, the system designers use a different design representation than the circuit designers. For example, the system designers might use a spreadsheet, Matlab, Simulink or System View while the circuit designers would use Verilog, VHDL, or SPICE. This causes a myriad of problems. The most important being that they are using different tools to explore the design and that make it difficult for them to share what they learn during the design process.

In this work, a common design representation such as Verilog-AMS is chosen.

The architectural-level description of the design is constructed from behavioral models and each of the blocks is then evaluated by the circuit design. In this way, the circuit design starts by receiving an executable example of what is expected to design. The ready availability of behavioral models of the blocks that acts as executable examples greatly reduces the need for onerous specifications that describes the desired behavior of each block, specifications that are often poorly written and that frequently go unread.

7.2.1 Simulation Results

This section analyses the technical aspects related to the developed pipelined ADC such as Verilog-AMS model and simulation results. In this work, the tool used that support Verilog-AMS descriptions is AMS Designer. All the models have been described in Verilog-AMS using AMS Designer version 5.5.1 for compilation and simulation. Verilog-AMS is a very extensive and powerful language. It is a modeling language for mixed-signal systems. As such, Verilog-AMS is a language that supports the descriptions of both digital and analog components. This model has been realised using a complete Verilog-AMS description. The proposed architecture is partitioned into smaller blocks and non-ideal effects such as offset and mismatch are added in an incremental manner. To validate the proposed architecture, the behavioral description of the complete system model is described in Verilog-AMS using Cadence AMS Designer. System level simulations verify the usefulness of the proposed architecture and the simulation results are shown as follow. The differential nonlinearity (DNL), was measured using a code-density test with a slow input ramp. The proposed 8-bit ADC achieved a DNL of ± 0.2 LSB as shown in Figure 7.2. The dynamic linearity

Figure 7.1: Top-down design flow.

Figure 7.2: DNL versus ADC output codes.

of the ADC was characterized by analyzing a fast Fourier transform (FFT) of the output code with respect to a pure sinusoid wave [39]. Shown in Figure 7.3, the measured peak SNDR reaches 46.5 dB with a 0.46-MHz input which is equivalent to 7.43 effective number of bits (ENOB). It can also be seen that the peak SFDR is 69.9 dB. Figure ?? depicts the simulation results with gain error. As can be seen, the architecture worked according to the design demonstrating that subranging techniques can be integrated into pipelined ADC.

7.3 Summary

In summary, the technical aspects related to the developed subranging pipelined ADC are analyzed, namely the static and dynamic performance of the ADC.

Figure 7.3: FFT spectrum of the proposed 8-bit ADC.

Figure 7.4: FFT spectrum of the proposed 8-bit ADC with non-linearity.

Chapter 8

Conclusions and Recommendations

In this thesis, one of the main focuses is to design efficient and robust top-down design verification scheme for the proposed subranging pipelined ADC architecture. In previous chapters, the research works for this purpose have been presented. In this chapter, the main development of this thesis is summarized in section 8.1. Several recommendations are discussed for the future work in section 8.2.

8.1 Conclusions

This work has presented a top-down design verification based on modular and parametric behavioral modeling to test the feasibility of a novel 8-bit 100 MS/s subranging pipelined ADC before circuit design is carried out. The modularity and the high degree of parameterization of the models increase their reusabil-

ity. The working principle of a subranging pipelined ADC was discussed. The ability of integrating subranging techniques into pipelined architecture was presented. By using Verilog-AMS, a standard hardware description language, the models can be easily exchanged and simulated with standard electronic design automation (EDA) tools. The simulation is very fast and produces very accurate results, with the inclusion of non-ideal effects in models. The AMS simulations show that a new concept can be studied and verified in the early stage of design cycle. It verifies the usefulness of system simulation to circuit design.

8.2 Recommendations for Future Work

There are many interesting research topics in ADC design. Although some research topics have already been studied in this thesis, some possible extensions of the work in this thesis may be considered for future research studies. One area to explore is the optimization of each stage of the pipelined ADC to further reduce the power consumption of the overall ADC system.

Author's Publications

Conference papers

1. J. Wang and L. Siek, "A Top-Down Design Verification Based on Reuse Modular and Parametric Behavioral Modeling for Subranging Pipelined Analog-to-Digital Converter," *Proc. IEEE Int. Symp. Integrated Circuits (ISIC'07)*, Sept 26-28, 2007, pp 418-421, ISBN:1-4244-0797-4.

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