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Zeng, R. (2010). Studies on high-frequency noise characteristics in deep submicron NMOSFETs. Doctoral thesis, Nanyang Technological University, Singapore.

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STUDIES ON HIGH-FREQUENCY NOISE CHARACTERISTICS IN DEEP SUBMICRON NMOSFETS ZENG RONG 2010

Studies on High-frequency Noise Characteristics in Deep Submicron NMOSFETs

ZENG RONG

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2010

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STUDIES ON HIGH-FREQUENCY NOISE CHARACTERISTICS IN DEEP SUBMICRON NMOSFETS

ZENG RONG

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2010

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ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to all those who gave me the possibility to complete this thesis.

I am deeply indebted to my supervisor Prof. Wang Hong who, stimulating suggestions and encouragement, helped me in all the time of research for and writing of this thesis. I am grateful to Prof. K. Radhakrishnan for his guidance and encouragement. I have furthermore to thank Dr. Daniel Lubrich who looked closely at the final version of the thesis for English style and grammar, correcting both and offering suggestions for improvement.

I would like to thank all my colleagues for their valuable comments and concern. I greatly appreciate my research colleagues Mr. Neo Wah Peng, Mr. Yuan Kai Hua, Mr. Tan Chee Leong, Mr. Yang Hong, Mr. Cheong Wai Chye, Ms. Bu Jing, Ms. Liu Yu Wei, Ms. Ng Chai Wah, Mr. Liu Zhi Hong and other research staffs and students for their assistance and helpful discussions.

I would like to specially thank our Clean Room and Characterization Lab technicians, Mr. Foo Tai Ho, Ms. Yong Puay Peng, Mr. Muhd Fauzi Bin Abdullah. All of them have offered invaluable help to my work and have made my stay at NTU enjoyable.

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SUMMARY

RF noise characteristics of deep sub-micrometer MOSFETs are investigated in this work.

The direct matrix method to extract the channel thermal noise and induced gate noise is analyzed. In deep sub micron NMOSFETs, the contributions from some extrinsic elements are small and can be neglected. The procedure can therefore be simplified to a one-step matrix calculation. The obtained noise currents from the new method are in good agreement with those calculated from classical methods.

The impact of Fowler–Nordheim (FN) stress and oxide breakdown on high frequency noise characteristics in 0.18 μm NMOSFET has been studied. Noise characteristics of the devices at different leakage levels and breakdown hardness are compared. The results show a strong dependence of degradation of noise parameters on the gate leakage. The degradation mechanisms are analyzed by extraction of the channel and gate noise using a noise equivalent circuit model. It has been found that gate shot noise, which is commonly ignored in NMOSFETs, plays a dominant role in determining the high frequency noise in the post-oxide breakdown NMOSFETs.

The relation between the location of gate oxide breakdown in deep submicron MOSFETs and noise characteristics has been studied. RF Noise in the frequency range of 2 to 18 GHz of the devices with oxide breakdown at different locations are characterized and compared. The results show that

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degradation of noise parameters subject to gate oxide breakdown is not only related to breakdown hardness but also the oxide breakdown path. For similar breakdown hardness, formation of the breakdown path closer to source side may result in a larger degradation of device RF noise performance.

RF noise in 0.18-μm NMOSFETs concerning the contribution of carrier heating and hot carrier effect is characterized and analyzed in detail. A novel approach is used to modulate the channel carrier heating and number of hot carriers using body bias. We confirm qualitatively a negligible role of hot carrier effect on the channel noise in deep-sub micrometer MOSFETs. For a device under reverse body bias (V_b), even though the increase in hot carrier population is clearly characterized by DC measurements, the device high-frequency noise is found to be irrelevant to the increase in the channel hot carriers. Experimental results show that the high-frequency noise is slightly reduced with the increase in body bias, and can be qualitatively explained by secondary effects such as the suppression of nonequilibrium channel noise and substrate induced noise. The reduction of minimum noise figure with the increase in body bias may provide a possible methodology to finely adjust the device high-frequency noise performance for circuit design.

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Chapter 2 Introduction

1.1 CMOS technology for RFIC applications

RF integrated circuits in CMOS (Complementary metal–oxide–semiconductor) technologies have a strong presence in the commercial world. For applications such as wireless Local Area Network (LAN) and Bluetooth, they are dominant, and in areas such as Global System for Mobile (GSM) cellular transceivers and Global Positioning System (GPS) receivers, they are making inroads. Driving force for this are advances in CMOS fabrications.

Modern CMOS technologies have resulted in deep submicron transistors with higher transit frequencies and lower noise figures. The cut-off frequency of NMOSFETs can be higher than 100Ghz at a channel length of 90nm, while the minimum noise figure can be as low as 0.1dB (Figure 1.1). This advanced performance of deep sub-micron MOSFETs is attractive for high-frequency (HF) integrated circuit (IC) design. Designers have already started to explore the use of CMOS technology in radio-frequency (RF) circuits. Furthermore, great advances in CMOS technology have made possible the development of system-on-a-chip design, where digital, mixed-signal base-band and HF transceiver blocks are integrated on a single chip. In addition, by eliminating expensive packaging and processing silicon wafers in high volume, cost can be greatly reduced. Other advantages like the low power consumption of MOSFETs make them suitable for portable applications.

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However, when transistors operate at high frequencies, noise generated within the device itself will play an increasingly important role in the overall sensitivity characteristics, dynamic range and signal-to-noise ratio of a system. Figure 1.2 shows a typical output curve of an amplifier. The minimum input power that can be recognized by the amplifier system is decided by the noise floor present in the system. The noise floor is the measure of the signal created from the sum of all the noise sources and unwanted signals within a measurement system. The lower the noise floor, the higher the sensitivity of the system is and the wider the dynamic range of the amplifier is. Low noise design is one of the key issues in most of the RF circuits. To reduce design cycles and to achieve first time success in implementation, acurate modelling of noise is a prerequisite.

A majority of the RF integrated circuits used in wireless systems are very sensitive to device parameter variations. In addition, compared to their long-channel counterparts, deep sub-micron MOSFETs are reported to have a strong enhancement in thermal noise. Lack of understanding of noise in deep submicron MOSFETs presents a substantial barrier to the modelling of MOSFETs and implementation of RF circuit design. It is indispensable to understand the physical phenomena of noise in deep sub-micron MOSFET and to incorporate this information into the models.

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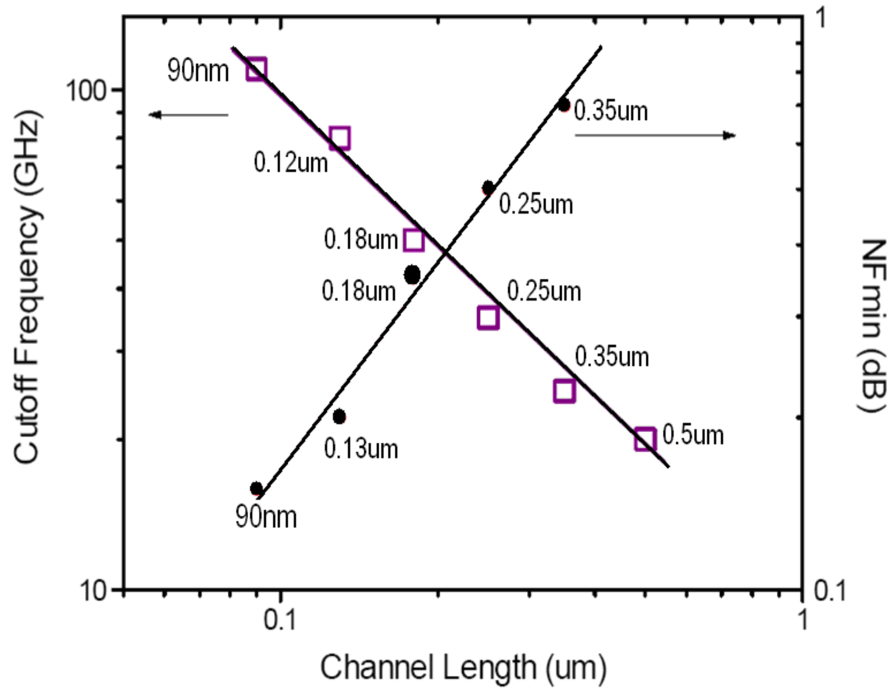

Figure 2.1 CMOS technology trend: cutoff frequency and NF_{min} [1]

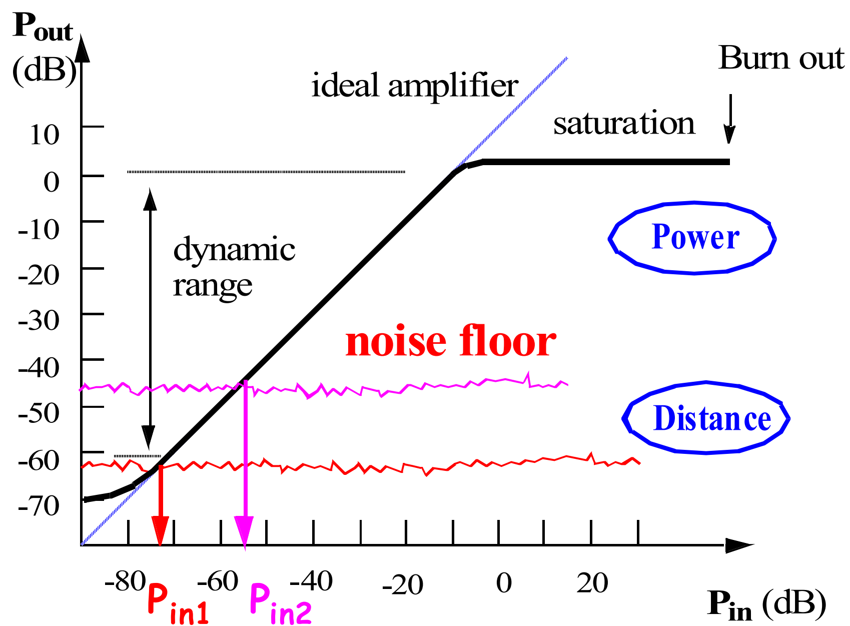

Figure 2.2 Typical power curve of an amplifier with different noise floors [2]

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1.2 Objectives

Thermal noise is a major source of noise in MOSFETs. Knowledge of the channel thermal noise and induced gate noise is required in most noise analysis and studies of MOSFETs, hence significant efforts have been made to extract them. Generally the procedure involves the extraction of small-signal parameters separately at each bias point followed by complex matrix computations. Part of the research work presented in this thesis is on methods to quickly calculate noise currents in deep-sub micrometer MOSFETs without the need to extract small-signal parameters.

To minimize the switching power dissipation of integrated circuits, the supply voltages have been steadily reduced as a result of scaling. In order to maintain performance and control short channel effects, a reduction in the transistor oxide thickness is required to provide sufficient current drive at the reduced supply voltages. At the 65*nm* technology node, CMOS processes will have oxide thicknesses of 1.2*nm* to 1.6*nm*. Since electric fields in the gate oxide are expected to rise with scaling, the long-term reliability of thin oxides becomes an important concern in modern, deep-submicron devices. The gate oxide wear-out and eventual breakdown is considered to be one of the major reliability issues for deep submicron MOSFETs. However, the effect of device degradation on the RF noise in NMOSFETs has not yet been fully addressed. In this work, the relationship between the MOSFET degradation and stress is discussed.

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Several authors have shown that the most severe breakdowns are those located near the source/drain overlap regions [3]. The impact of the oxide breakdown on the device operation is thus controlled by two breakdown variables: the hardness and the location. It has been found that the drastic increase of device high frequency noise after gate oxide breakdown can be attributed to the significant increase in the contribution of gate shot noise. However, it was still unclear how hard breakdown in a sub-micron MOSFET can influence operation of low noise RF circuits. Part of the research work in this thesis is on the relation between the location of breakdown in deep sub-micron MOSFET and noise characteristics.

As compared to long channel devices, different RF noise behavior in deep-submicron MOSFET has been observed. Different theories have been proposed to explain these phenomena but many remain controversial. The mechanisms of noise currents in MOSFETs are not yet well understood. The experimental evaluation of the effect of carrier heating on channel noise in sub micrometer MOSFETs is carried out to gain a fundamental understanding of RF noise in NMOSFETs.

1.3 Major contributions

The work described in this thesis was motivated by the desire to understand the mechanism of MOSFET noise and the impact of device degradation, such as gate oxide breakdown, on RF noise characteristics. The major contributions are summarized as follows:

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(i) A new procedure is introduced to quickly evaluate the channel and induced gate noise currents in deep sub-micron MOSFET devices. The method only requires extracting the gate resistance. Noise parameters (NF_{min}, R_n, and G_{opt}) are measured and noise currents are then obtained using one simple matrix calculation, without the need to deduce additional device parameters. The extracted noise currents calculated with our method are comparable to those obtained using classic network matrix methods.

(ii) The microwave noise performance of NMOSFET during FN stress and subsequent breakdown is studied. Degradation of high frequency noise characteristics in 0.18 μm NMOSFET induced by gate oxide breakdown is characterized in the frequency range of 2 to 14 GHz. Noise characteristics of the devices with different breakdown hardness are compared. A serious degradation of microwave noise performance is observed. The degradation mechanisms are analyzed by extraction of the channel and gate noise using a noise equivalent circuit model. It is found that gate shot noise, which is commonly ignored in the as-processed NMOSFET, plays a dominant role in determining the microwave noise performance in the post-oxide breakdown NMOSFET.

(iii) The relationship between the breakdown location and RF noise degradation of deep sub-micron devices is addressed. The results for the dependence of device DC and high-frequency noise performance on breakdown location are provided. The results show the effect on degradation of noise

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parameters from the gate leakage (breakdown hardness) and the breakdown location.

(iv) The impact of body bias on RF noise behavior in deep-sub micrometer NMOSFETs is investigated to understand if carrier heating and hot carrier effects are the root causes of the excess channel thermal noise observed in short-channel MOSFETs. Using a novel approach that modulates the channel carrier heating and the number of hot carriers through reverse body bias without causing significant changes to other device parameters, the postulation of enhancement of high-frequency noise in deep-sub micrometer MOSFETs due to channel carrier heating is directly assessed. We confirm qualitatively a negligible role of hot carrier effect on the channel noise in deep-sub micrometer MOSFETs. For a device under reverse body bias (Vb), even though the increase in hot carrier population is clearly characterized by dc measurements, the device high-frequency noise is found to be irrelevant to the increase in the channel hot carriers. Experimental results show that the high-frequency noise is slightly reduced with the increase in $|V_b|$, and can be qualitatively explained by secondary effects such as the suppression of non-equilibrium channel noise and substrate induced noise. The reduction of NF_{min} and R_{n} with the increase in $|V_b|$ may provide a possible methodology to finely adjust the device high-frequency noise performance for circuit design.

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1.4 Organization of this thesis

The following chapters provide extensive and detailed information about MOSFET noise both in terms of device physics and detailed modeling and analysis.

The theoretical background related to the device noise properties and device physics is investigated in Chapter 2. Small signal and noise modeling and parameter extraction method used in the research are presented. In addition a literature review is conducted. In Chapter 3, noise measurement methodology is addressed and the devices used in the research are introduced. A simplified noise currents extraction method is discussed in Chapter 4. In Chapter 5, effect of FN stress and gate oxide breakdown on high frequency noise is analyzed. In Chapter 6, the relation between RF noise and gate oxide breakdown location in deep sub-micron MOSFETs is examined. Carrier heating on channel noise in deep sub-micron NMOSFETs via body bias is studied in Chapter 7. Finally, in Chapter 8, the conclusion is presented and recommendations for future work are proposed.

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Chapter 3 Theoretical investigation of noise in MOSFET and device physics

2.1 Small signal model of MOSFET

MOSFET models are widely used for modern electronic design work. There is a large economic incentive to get the design working without any iteration. Complete and accurate models allow a large percentage of designs to work the first time.

Small-signal or linear models are used to evaluate stability, gain, noise and bandwidth, etc. The small-signal condition for a transistor can be described as follows. A dc operating point is specified by a dc bias condition (i.e. V_{ds}, V_{gs} and V_{bs}), and small signals (ac signals) are superimposed to such a dc condition [4]. Under the small-signal condition, a MOSFET can be described by a small-signal equivalent circuit with lumped elements. The terminal voltages (V_{gs}, V_{ds} and V_{bs}) are assumed to change by a small amount. The resulting changes in currents are analyzed to derive the parameters for each path (gate-to-drain, gate-to-source, drain-to-source, etc.). The small signal equivalent circuit can be obtained by combining all the parameters together [5].

Different equivalent circuits have been proposed in the literature. Generally, two kinds of models are widely made use of: commercial MOS compact models such as BSIM4 [6], MOS model 9, 11 [7], or EKV (developed by C. C. Enz, F. Krummenacher, and E. A. Vittoz) [8] with or without

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consideration of parasitic components; and the equivalent circuit derived from classical MESFET models (T-model or π-model). One crucial difference between these two kinds of models is the method to extract circuit elements values.

For the commercial compact model, a set of model equations are used to describe the behavior of the device. A simulation result is the evaluation of the equations given the values of the model parameters. The extraction of the model parameters is from the process of optimization. First, the initial model parameters are preset. The optimizer is used to adjust the initial model parameter values in an iterative process. The algorithm of the optimization process works follows:

1. The simulation goals are preset before the simulation and optimization. The simulation goals usually the RMS error between a set of measured parameters (for example: S-parameters, noise parameters) and the simulated parameters from the model.

$$RMSerror = \sqrt{\frac{\sum_{i=1}^{n}[(sim_i - mea_i)^2 / N]}{(\sum_{i=1}^{n} meas_i^{\ 2}) / N}}$$

where:

sim_i = the ith simulated data point;

$meas_i$ = the ith measured data point;

N = the total number of data points.

2. The optimizer invokes the simulator to obtain a set of simulated data

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corresponding to the measured data used in the extraction process. This step is called function evaluation.

3. The optimizer compares the simulated and measured data and calculates the RMS error between them.

4. Based on the results, the optimizer calculates a new set of model parameter values and again compares the simulated and measured data. This process continues with another function evaluation until the RMS error between the simulated and measured data either falls within a specified range, or no further improvement is possible. Most of the extraction procedure is completed by the software. In most cases this is very time consuming.

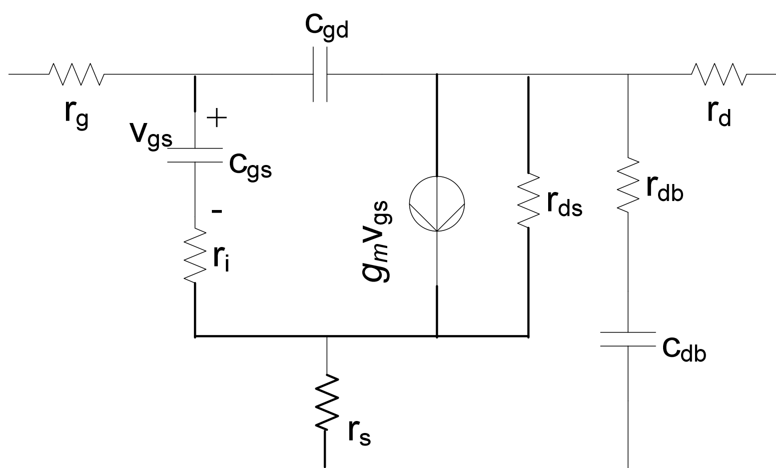

Figure 3.1 The equivalent high-frequency small-signal model for MOSFETs

As a counterpart, an equivalent circuit is comprised of a set of lumped circuit elements (R, L, C and current/voltage controlled current or voltage sources, etc.). The high frequency model used in this work is based on the

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classical MESFET model proposed in [9]. Figure 2.1 shows the equivalent circuit for a grounded substrate MOSFET operating in the saturation region. In this model the circuit elements associated with the substrate and source are excluded because in the experiments as well as in most high-frequency applications the substrate is always effectively short-circuited to the source. When the excitation signal appears either at the drain or gate, the substrate spreading bulk resistance between the source and the substrate has a negligible effect in activating the substrate controlled current generator. The equivalent circuit can be divided into two parts:

1. the intrinsic elements, g_m, r_{ds}, C_{gs}, C_{gd}, r_i, which are functions of the biasing conditions;
2. the extrinsic elements, r_g, r_s, r_d, r_{db}, C_{db}, which are weakly dependent on the biasing conditions.

In this model, C_{gs} is the gate-to-source capacitance and C_{gd} is gate-to-drain capacitance. The bulk spreading resistance is designated as r_{db}, the drain-source resistance rds. g_m represents the device transconductance. The resistance r_i represents the effective channel resistance seen by the signal flowing from gate to source. It consists of the distributed resistance of the channel and spreading bulk resistance capacitively coupled to the channel, and is responsible for the real part of intrinsic input y-parameter. This element is important to input impedance matching in analogue circuit designs. The r_d, r_s, r_g are respectively the drain-to-channel resistance (including contact resistance),

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source-to-channel resistance (including contact resistance) and gate-metal resistance.

By taking *y*-parameters of the equivalent circuit in the linear region, the extracted terminal resistances (r_d, r_s, r_g) for V_{ds}=0 V are: [10]

$$\begin{aligned} r_g &= \left| \frac{\mathrm{Re}\{Y_{12}\}}{\mathrm{Im}\{Y_{11}\}\,\mathrm{Im}\{Y_{12}\}} \right| \\ r_d &= \left| \frac{\mathrm{Re}\{Y_{21}\} - \mathrm{Re}\{Y_{12}\}}{\mathrm{Im}\{Y_{12}\}^2} \right| \\ r_s &= \left| \frac{\mathrm{Re}\{Y_{11}\}}{\mathrm{Im}\{Y_{11}\}^2} - r_g - \frac{C_{gd}^2}{C_{gg}^2} r_d \right| \frac{C_{gg}^2}{C_{gs}^2} \end{aligned} \quad , \tag{2.1}$$

where $Y_{\square}$ are the *y*-parameters of the equivalent circuit, Re {} and Im {} denote for the real and imaginary part of the matrix elements, C_{gg} is the total gate capacitance and is given by:

$$C_{gg} = \left| \frac{\mathrm{Im}(Y_{11})}{\omega} \right|. \tag{2.2}$$

In most of the MOS transistor applications at RF, the transistor is biased in the saturation region in order to achieve higher voltage gain and a larger dynamic range. The rest of the parameters will be extracted from the *y*-parameters in the saturation region. Since only the imaginary parts are needed for determining the intrinsic capacitances, the extraction method for C_{gg} can also be applied to the saturation region [8]. C_{gs} and C_{gd} can be determined from the *y*-parameters in the saturation region:

$$\begin{aligned} C_{gd} &= \left| \frac{\mathrm{Im}(Y_{12})}{\omega} \right| \\ C_{gs} &= C_{gg} - C_{gd} \end{aligned} \quad . \tag{2.3}$$

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To extract the equivalent admittance of the substrate coupling network, the series resistances r_g and r_d are subtracted from input and output ports followed by transforming the Z-matrix into the Y-matrix. Thus:

$$Y' = (Z')^{-1} = (Z + \begin{bmatrix} r_g & 0 \\ 0 & r_d \end{bmatrix})^{-1}, \tag{2.4}$$

where Z is the Z-parameter matrix of the whole device in the saturation region. The equivalent substrate admittance Y_{sub} is derived as

$$Y_{sub} = \frac{1}{r_{db} + \dfrac{1}{j\omega C_{db}}} = Y_{22}^{'} - j\omega C_{gd} - g_{ds}. \tag{2.5}$$

Here g_{ds} is extracted from the value of $(\dfrac{1}{\text{Re}(Y_{22}^{'})} - r_s)^{-1}$ at low frequency («1 GHz).

2.2 Sources of noise

2.2.1 Definition of noise

The general definition of noise is “loud, confused, or senseless shouting or outcry” or “any sound that is undesired or interferes with one’s hearing of something” [11]. In electronics, noise is usually referred to as an opposite term to the signal. Thus noise can be defined as “everything except for the desired signal” [12]. Several types of noise sources are observed in electron devices, such as thermal, shot, generation-recombination, and flicker noise. A MOSFET mainly contains three noise types: thermal noise, flicker noise and shot noise.

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2.2.2 Thermal noise

The random thermal motion of electrons inside a piece of conductive material leads to a temporary agglomeration of carriers at one of the ends of the material. From a macroscopic standpoint this means that the potential on one end will be more negative than the potential on the other end. Hence a potential difference appears, the thermal noise voltage. While its mean value is zero, its polarity and magnitude are fluctuating.

2.2.3 Thermal noise in electron devices

At any temperature above absolute 0 K, the motion of the electrons will produce random instantaneous currents. These currents will produce random instantaneous voltages, and this leads to noise power. The random fluctuation of electrons in a resistance rises as the temperature increases. This is because the electron velocities and the frequency of collisions increase with higher temperatures. The noise voltage is expressed as an auto correlation of the instantaneous voltage over a time period T [13]:

$$\langle v^2 \rangle = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} v^2(t)dt \,. \tag{2.6}$$

Nyquist's theorem [14] states that for linear resistances in thermal equilibrium at temperature T, the current of voltage fluctuations are quite independent of the conduction mechanisms, type of material, and shape and geometry of the resistor. The generated noise depends exclusively upon the value of the resistance and its temperature T (given in Kelvins [15]).

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Therefore, under open-circuit conditions the noise voltage spectral density is a constant quantity given by [13]

$$S_{v_n} = \frac{\overline{v_n^2}}{\Delta f} = 4kTR \qquad (\mathrm{V^2/Hz}). \tag{2.7}$$

Under short-circuit condition, the noise current spectral density is a constant quantity, given by [13]

$$S_{i_n} = \frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R} = 4kTG \qquad (\mathrm{A^2/Hz}), \tag{2.8}$$

where G denotes the conductance and k is Boltzmann's constant. Δf is the bandwidth within which the noise is measured.

2.2.4 Thermal noise in MOSFETs

Historically MOS devices have been used for low frequency applications due to the limited carrier mobility of silicon. Consequently, the most important noise source was channel thermal noise and flicker noise. At high frequencies, channel thermal noise is still the key noise source. In addition other thermal noise sources, such as induced gate noise and parasitic resistance thermal noise become important.

Commonly sources of high frequency noise are classified as intrinsic and extrinsic. The noise originating within the active region of a MOS device channel is defined as intrinsic noise. It includes channel thermal noise and induced gate noise. Channel thermal noise is associated with carriers within the channel. According to Nyquist's theorem and the gradual channel

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approximation, the short circuit thermal noise current at drain terminal $\overline{i_d^2}$ is given by [16]

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f \,, \tag{2.9}$$

where k is the Boltzmann constant, T is the absolute temperature, and g_{d0} is the channel conductance at zero drain source voltage. γ is a bias dependent factor. For long channel devices, the value of 2/3 holds when the MOSFET is in the saturation region, and the value of 1 is valid in the linear region [16]. This model agrees well with long channel MOSFETs down to 1.7 μ m. Substantial increases have been observed in γ for MOSFETs with shorter channel lengths owing to both velocity saturation and hot electrons. A simple thermal noise model has been proposed to account for these two effects by [103]

$$\gamma \cong \gamma_L (1 + \frac{1}{G} \frac{v_{sat}\tau_f}{L_{eff}}) \tag{2.10}$$

where v_{sat} is the saturation velocity, τ_f is a relaxation time (of the order of *ps*) used as a fitting parameter, G is the normalized G_m/I_D ratio, and γ_L is the γ-factor for the long-channel device. This noise model assumes that the carrier velocity is saturated and that the lateral field is equal to the critical field all along the channel from source to drain. These assumptions are questionable, but it can cover device operation regions from weak to strong inversions and fit the measured data over different biases and geometries.

Induced gate noise is another type of intrinsic noise. At moderately higher frequencies, the random motion of the free carriers in the channel

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generates not only an output drain current noise, but also an input gate current noise due to the capacitive coupling effect via the gate-channel capacitance. The gate current noise is approximately given by [17]

$$\overline{i_g^2} = 4kT\beta \frac{(\omega C_{gs})^2}{g_{d0}} \Delta f \,, \tag{2.11}$$

where C_{gs} is the gate-source capacitance of the MOSFET. Similar to factor γ , β is also dependent on basic transistor parameters and bias conditions. It is equal to 4/3 for a long-channel device in saturation. Since induced gate noise also originates from the random motion of the carriers in the channel, the two noise currents $\overline{i_d^2}$ and $\overline{i_g^2}$ are correlated and the correlation can be described by [16]

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2} \cdot \overline{i_d^2}}} \,, \tag{2.12}$$

where c is the correlation factor.

Aside from the intrinsic noise sources, various parasitic elements will contribute to the overall noise measured at the terminals of the devices at high frequencies. These types of noise source elements are classified as extrinsic noise sources.

MOSFET poly gate resistivity is usually very large. Even though a silicide process is normally adopted to form the gate, reducing the gate resistance becomes more difficult when the gate length is further. The resistive gate contributes to thermal noise at the gate node. The mean-square noise current of the gate resistance is described by [16]

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$$\overline{i_G^2} = 4kT\Delta f / r_g \,, \qquad (2.13)$$

where $\overline{i_g^2}$ represents the current noise source of gate resistance, and r_g is the effective noise resistance of the gate. Because of the distributed effect of gate resistance, r_g is given by [16]

$$r_g = \frac{R_{g-sh}}{3}(\frac{W_g}{L_g}) \,, \qquad (2.14)$$

where $R_{g\text{-}sh}$ is gate sheet resistance, W_g is the width of the gate, and L_g is the gate length. Equation (2.12) is only valid when the gate is connected at one end.

The source and drain parasitic resistors also contribute to thermal noise. These noise contributions are modeled by the following equations: [16]

$$\begin{aligned} \overline{i_s^2} &= 4kT\Delta f / r_s \\ \overline{i_D^2} &= 4kT\Delta f / r_d \end{aligned} \,, \qquad (2.15)$$

where $\overline{i_s^2}$ and $\overline{i_D^2}$ represent the current noises of source and drain resistances. The noises generated by the source and drain resistances are also important. However, they are a strong function of the materials used to form the source/drain as well as processing. If not designed properly, their contribution to the noise figure of the whole device can be significant.

It is known that distributed substrate resistance is another noise source [18]. An accurate calculation of this noise source is complex, whereas it can be simply expressed as [16]

$$\overline{i_{dB}^2} = 4kT\alpha \frac{d}{W} g_{mb}^2 \Delta f \qquad (2.16)$$

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where α is a constant, d is the space size between gate and bulk contact, W is the gate width, and g_{mb} is the bulk transconductance which depends on the bulk to source voltage V_{BS}.

2.2.5 Shot noise

Shot noise was first described by Schottky in 1918 [19] as:

$$\langle i^2 \rangle = 2qI_0\Delta f \, , \tag{2.17}$$

where I_0 is the DC current flowing across the device and q is the charge of an electron. It is white noise and occurs when quantized carriers cross barriers with random spacing as in Schottky diodes or p-n junctions.

The arrival of one unit charge at a boundary is independent from the time at which the previous unit arrived or the next unit will arrive. Therefore, two conditions are required for shot noise to occur: a flow of direct current and a potential barrier over which the carriers are crossing. Thus linear devices do not generate shot noise.

The only source of shot noise in a MOSFET is associated with the current tunnelling through the gate oxide, which is negligible in most cases.

2.2.6 Flicker noise

In principle, flicker noise is a low-frequency noise and it mainly affects the low frequency performance of the device, so it can be ignored at very high frequency. However, the contribution of flicker noise should be considered in designing some radiofrequency (RF) circuits such as mixers, oscillators, or

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frequency dividers that up-convert the low-frequency noise to higher frequency and deteriorate the phase noise or the signal-to-noise ratio. Typically this frequency ranges from 100 Hz to 10 kHz.

2.2.7 Equivalent noise circuit model

From the above analysis, thermal noise is the major contributor for the origin of high-frequency noise in the MOSFET drain current. After including all the thermal noise sources into the small signal model in Figure 2.1, Figure 2.2 shows the small-signal equivalent noise circuit of the grounded substrate MOSFET.

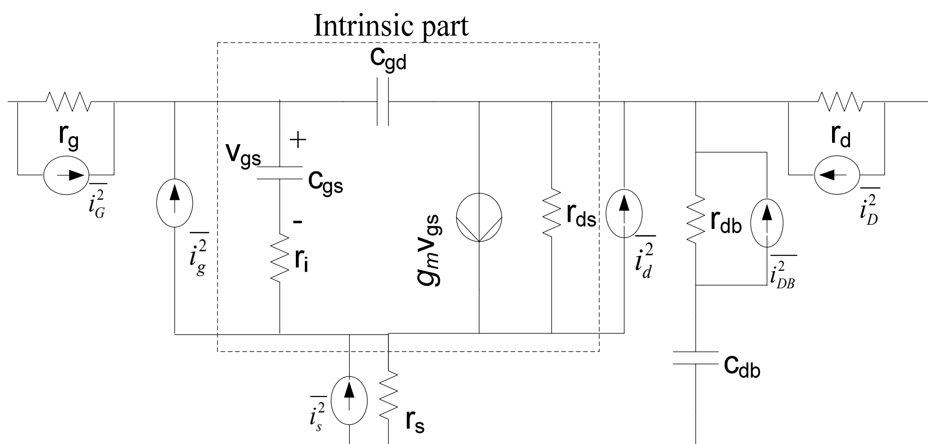

Figure 3.2 small-signal equivalent noise circuit of grounded substrate MOSFET

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2.3 Noise parameters and noise two-port network

A noisy two-port may be described by a noise-free two-port and two current noise sources in three different representations as shown in Figure 2.3. These two noise sources are usually correlated with each other.

A matrix formulation for the representation C_Y in Figure 2.3(a) is given by [21]:

$$C_Y = \frac{1}{2\Delta f}\begin{bmatrix} \langle i_1 i_1^* \rangle & \langle i_1 i_2^* \rangle \\ \langle i_2 i_1^* \rangle & \langle i_2 i_2^* \rangle \end{bmatrix}. \tag{2.18}$$

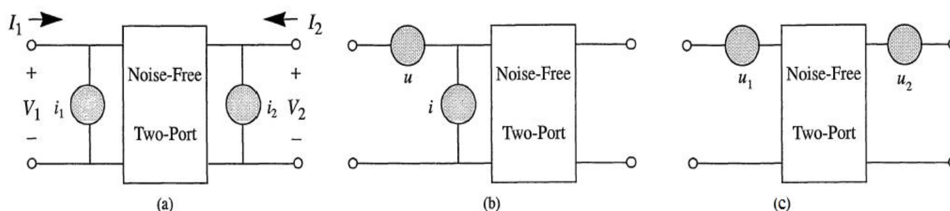

Figure 3.3 Different representations of a noisy two-port network [20]

Based on the *Y*-parameters of the two-port and the noise source information (i_1, i_2 and their correlation term $\langle i_1 i_2^* \rangle$), we may evaluate the noise parameters of the two-port by transforming the noisy two-port to a noise-free two-port with a noise current and a noise voltage sources at the input side of the two-port (Figure 2.3(b)). The correlation matrix C_A is given by [21]:

$$C_A = \frac{1}{2\Delta f}\begin{bmatrix} \langle uu^* \rangle & \langle ui^* \rangle \\ \langle iu^* \rangle & \langle ii^* \rangle \end{bmatrix}. \tag{2.19}$$

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The correlation matrix C_Z of the impedance representation in Figure 2.3(c) is given by [21]:

$$C_Z = \frac{1}{2\Delta f}\begin{bmatrix} \langle u_1 u_1^* \rangle & \langle u_1 u_2^* \rangle \\ \langle u_2 u_1^* \rangle & \langle u_2 u_2^* \rangle \end{bmatrix}. \tag{2.20}$$

The three representations can be transformed into each other by simple transformation operations. C_A and C_Y are correlated by equation [21]:

$$C_Y = T_Y C_A T_Y^\dagger , \tag{2.21}$$

where the † in $T_Y^\dagger$ denotes Hermitian conjugation (transpose and complex conjugate) and the transformation matrix $\boldsymbol{T_Y}$ is given by [21]

$$T_Y = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}, \tag{2.22}$$

where Y_{11} and Y_{21} are Y-parameters of the two-port network. A set of matrices covering all possible transformations can be found in [21].

For applications in noise analysis, interconnections of two two-ports either in parallel, in series or in cascade are of particular interest. The resulting correlation matrices can be determined by [21]

$$\begin{aligned} C_Y &= C_{Y1} + C_{Y2} && \text{(parallel)} \\ C_Z &= C_{Z1} + C_{Z2} && \text{(Series)} \\ C_A &= A_1 C_{A2} A_1^+ + C_{A1} && \text{(Cascade)} \end{aligned} \tag{2.23}$$

Any network A can be decomposed into a few basic two-ports. These basic two-port networks then consist of only a few elements and the noise currents and electrical matrices (C_A, C_Z or C_Y) of each element are easily

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calculated or measured. Once all matrices are known, the basic two-ports are successively interconnected so that network *A* is obtained. As an example, in the equivalent circuit in Figure 2.2, the network can be divided into five basic two-ports: intrinsic part, gate resistance, source resistance, substrate network and drain resistance. The matrices of the parasitic elements (gate/source/drain resistance and substrate network) can be calculated. With knowledge of the intrinsic noise currents, the noises currents of the whole equivalent circuit can be calculated by the above direct matrix analysis or vice versa.

The noise power spectral density is widely used in noise modelling and circuit design as a measure for the noise output in a device. However, in measurements, the RF noise is usually characterized by several other parameters: the minimum noise factor (or minimum noise figure), the input referred noise resistance and the optimum source admittance at which the minimum noise figure is obtained. It is necessary to connect these parameters with the RF noise characteristics of the device.

Noise figure (*NF*) is a measure of degradation of the signal to noise ratio. It has been defined in a number of different ways. The most commonly accepted definition is

$$\text{Noise figure } (NF) = \frac{SNR_{in}}{SNR_{out}}, \tag{2.24}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output, respectively. It is also called the noise factor with the term noise figure applied to $10log_{10}$ (noise factor).

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The noise figure is a measure of how much the SNR degrades as the signal passes through a system. If a system has no noise, then SNR_{out}=SNR_{in}, regardless of the gain. This is because both the input signal and the input noise are amplified or attenuated by the same factor and no additional noise is introduced. Therefore the noise figure of a noiseless system is equal to 1. On the other hand a noisy system degrades the SNR, yielding NF>1. A low noise figure means that very little noise is added by the network. The concept of noise figure only fits networks (with at least one input and one output port) that process signals.

The noise figure of a two-port network is given by [20]

$$NF = NF_{\min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2, \quad (2.25)$$

where G_s is the source conductance, B_s is the source susceptance, G_{opt} is the optimized source conductance, B_{opt} is the optimized source susceptance. From (2.23), it is shown that the four noise parameters – the minimum noise figure (NF_{min}), the optimum source (input) impedance for the NF_{min}, and the equivalent noise resistance (R_n) which characterizes how the noise figure increases if the source impedance deviates from the optimum value – will decide how noisy a two-port network will be. NF_{min}, R_n, and G_{opt} are frequently referred to as the “noise parameters”, and it is their determination which is called “noise characterization”. When G_s is plotted on a Smith chart for a set of constant noise factors NF, the results are “noise circles” (Figure 2.4). Noise

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circles are a convenient format to display the complex relation between source impedance and noise figure.

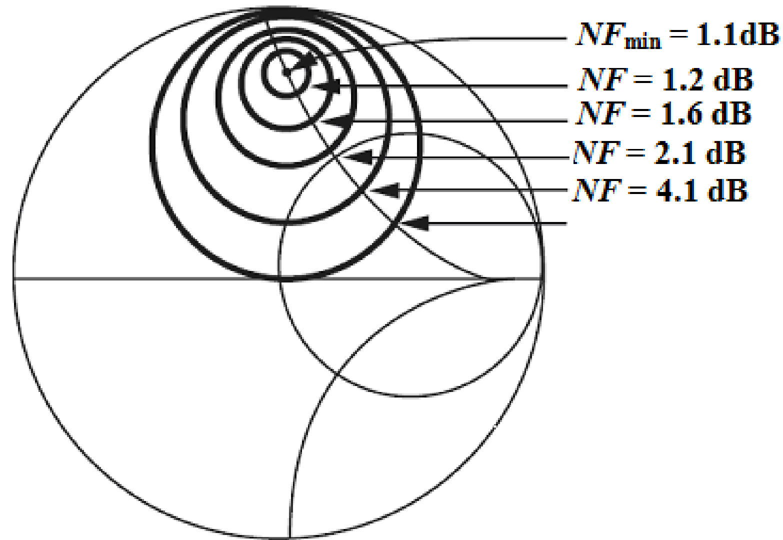

Figure 3.4 Noise circles of a typical transistor. The noise circles are used to display the complex relation between source impedance and noise figure.

The correlation matrix C_A can be calculated from the four measured noise parameters [20]:

$$C_A = \begin{pmatrix} R_n & \frac{F_{\min} - 1}{2} - R_n . Y_{opt}^* \\ \frac{F_{\min} - 1}{2} - R_n Y_{opt} & R_n \left| Y_{opt} \right|^2 \end{pmatrix}, \tag{2.26}$$

where the asterisk denotes the complex conjugate.

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2.4 Extraction of noise parameters

The induced gate noise, channel noise, and their correlation in MOSFETs can be extracted by using the following steps from measured noise parameters (NF_{min}, R_n, and G_{opt})[22].

1). Calculate the correlation matrix $\boldsymbol{C_{Adev}}$ of the intrinsic device from measured noise parameters of the device [22]

$$C_{Adev} = \begin{bmatrix} R_{n,dev} & \dfrac{NF_{\min,dev} - 1}{2} - R_{n,dev}(Y_{opt,dev})^* \\ \dfrac{NF_{\min,dev} - 1}{2} - R_{n,dev}(Y_{opt,dev}) & R_{n,dev}\left|Y_{opt,dev}\right|^2 \end{bmatrix}. \quad (2.27)$$

2). Calculate the four-port admittance matrix $\boldsymbol{Y_{extr}}$ of the extrinsic part in the RF transistor model by excluding C_{GS}, C_{GD}, g_m, R_{DS}, and R_i [23]

$$Y_{extr} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix}, \quad (2.28)$$

where the submatrixes $\boldsymbol{Y_{ee}}$, $\boldsymbol{Y_{ei}}$, $\boldsymbol{Y_{ie}}$, and $\boldsymbol{Y_{ii}}$ are 2×2 matrixes.

3). Calculate the two-port admittance $\boldsymbol{Y_{intr}}$ of the intrinsic part in the RF transistor model.

4). Calculate a matrix $\boldsymbol{D}$ as follows [22]:

$$D = -Y_{ei}(Y_{ii} + Y_{\mathrm{int}r})^{-1}. \quad (2.29)$$

5). Convert the noise correlation matrix $\boldsymbol{C_{Adev}}$ to its admittance form $\boldsymbol{C_{Ydev}}$ by using [22]

$$C_{Ydev} = T_Y C_{Adev} T_Y^{\dagger}. \quad (2.30)$$

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where the † in $T_Y^{\dagger}$ denotes Hermitian conjugation (transpose and complex conjugate) and the transformation matrix $\boldsymbol{T_Y}$ is given by

$$T_Y = \begin{bmatrix} -Y_{11,dev} & 1 \\ -Y_{21,dev} & 0 \end{bmatrix}. \tag{2.31}$$

6). Calculate the admittance noise correlation matrix $\boldsymbol{C_{Yextr}}$ of the extrinsic part by [24]

$$C_{Yextr} = kT(Y_{extr} + Y_{extr}^{\dagger})$$

$$\text{Or}\, C_{Yextr} = 2kT\Re(Y_{extr}), \tag{2.32}$$

where T is the device temperature, $\Re()$ denotes for the real part of the matrix elements and partition $\boldsymbol{C_{Yextr}}$ as [22]

$$C_{Yextr} = \begin{bmatrix} C_{ee} & C_{ei} \\ C_{ie} & C_{ii} \end{bmatrix},$$

where the submatrixes $\boldsymbol{C_{ee}}$, $\boldsymbol{C_{ei}}$, $\boldsymbol{C_{ie}}$, and $\boldsymbol{C_{ii}}$ are 2×2 matrixes.

7). Calculate the admittance correlation matrix $\boldsymbol{C_{Yintr}}$ of the intrinsic part in the RF transistor model from [22]

$$C_{Y\,\mathrm{int}\,r} = D_i(C_{Ydev} - C_{ee})D_i^{\dagger} - C_{ie}D_i^{\dagger} - D_i C_{ei} - C_{ii}, \tag{2.33}$$

where $D_i = D^{-1}$.

8). Convert $\boldsymbol{Y_{intr}}$ to its chain representation $\boldsymbol{A_{intr}}$ using the conversion formula [22]:

$$A_{\mathrm{int}\,r} = \frac{-1}{Y_{21,\mathrm{int}\,r}} \begin{bmatrix} Y_{22,\mathrm{int}\,r} & 1 \\ Y_{11,\mathrm{int}\,r}Y_{22,\mathrm{int}\,r} - Y_{12,\mathrm{int}\,r}Y_{21,\mathrm{int}\,r} & Y_{11,\mathrm{int}\,r} \end{bmatrix}, \tag{2.34}$$

9). Convert $\boldsymbol{C_{Yintr}}$ to its chain matrix form $\boldsymbol{C_{Aintr}}$ by using [22]

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$$C_{A\,\text{int}\,r} = T_A C_{Y\,\text{int}\,r} T_A^{\dagger}, \tag{2.35}$$

where T_A is given by

$$T_A = \begin{bmatrix} 0 & A_{12,\text{int}\,r} \\ 1 & A_{22,\text{int}\,r} \end{bmatrix}. \tag{2.36}$$

10). Calculate the noise parameters NF_{min}, Y_{opt}, and R_n of the intrinsic part in the RF transistor model from the noise correlation matrix $\boldsymbol{C_{Aintr}}$ by using (2.35), where $\Im()$ stands for the imaginary part of elements and j is the imaginary unit [22].

$$NF_{\min} = 1 + \frac{1}{kT_0}(\Re(C_{12A,\text{int}\,r} + \sqrt{C_{11A,\text{int}\,r}C_{22A,\text{int}\,r} - (\Im(C_{12A,\text{int}\,r}))^2})$$

$$Y_{opt} = \frac{\sqrt{C_{11A,\text{int}\,r}C_{22A,\text{int}\,r} - (\Im(C_{12A,\text{int}\,r}))^2} + j\Im(C_{12A,\text{int}\,r})}{C_{11A,\text{int}\,r}} \quad \text{And}$$

$$R_n = \frac{C_{11A,\text{int}\,r}}{2kT_0}. \tag{2.37}$$

11). Calculate the power spectral density of the channel noise $\overline{i_d^2}$, induced gate noise $\overline{i_g^2}$, and their correlation $\overline{i_g i_d^*}$ from [22]

$$\frac{\overline{|i_d|^2}}{\Delta f} = 4kT_0 R_n |Y_{21,\text{int}\,r}|^2 \tag{2.38}$$

$$\frac{\overline{|i_g|^2}}{\Delta f} = 4kT_0 R_n \times \{|Y_{opt}|^2 - |Y_{11,\text{int}\,r}|^2 + 2\Re[(Y_{11,\text{int}\,r} - Y_{cor})Y_{11,\text{int}\,r}^*]\} \tag{2.39}$$

And

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$$\frac{\overline{i_g i_d^*}}{\Delta f} = 4kT_0 (Y_{11,\text{int}\,r} - Y_{cor}) R_n Y^*_{21,\text{int}\,r} \tag{2.40}$$

where Y_{cor} is given by

$$Y_{cor} = \frac{NF_{\min} - 1}{2R_n} - Y_{cor} \tag{2.41}$$

2.5 Gate oxide breakdown

2.5.1 Gate oxide breakdown and noise

Gate-oxide breakdown is defined as the time when a cluster of connected bonds, beginning from a "seed" at one interface of the gate-oxide, reaches the opposite interface [25]. Defects within the gate oxide are usually called traps. Gate-oxide breakdown begins when traps form in the gate-oxide. At first the traps are non-overlapping and thus do not conduct, but as more and more traps are created in the gate-oxide, traps start to overlap creating a conduction path [26]. Once these traps form a conduction path from the gate to the channel, breakdown occurs [26]. This type of breakdown is called Soft Breakdown (SBD). Once there is conduction, new traps are created by thermal damage, which in turn allows for increased conductance [27]. The cycle of conduction leading to increased heat and increased heat leading to increased conduction leads to thermal runaway [27] and finally to a lateral propagation of the breakdown spot [28]. The silicon within the breakdown spot starts to melt,

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and oxygen is released, and a silicon filament is formed in the breakdown spot [27]. This type of breakdown is called Hard Breakdown (HBD).

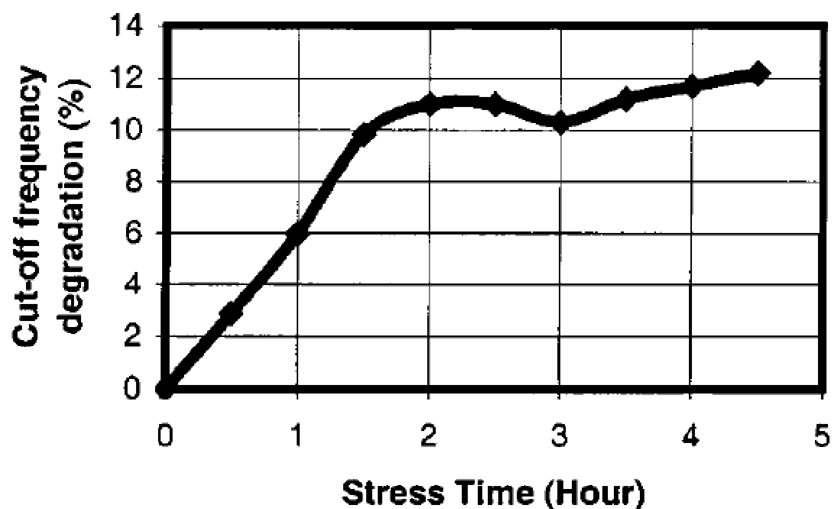

Figure 3.5 Measured cut-off frequency degradation versus stress time [34]

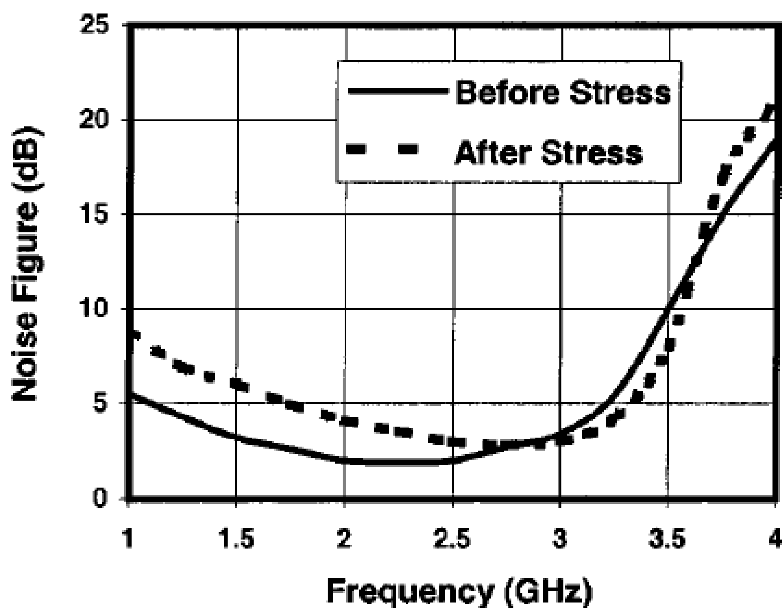

Figure 3.6 Noise figure versus frequency before and after stress [34]

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The gate oxide wear-out and eventual breakdown is considered as one of the major reliability issues for deep-sub micrometer MOSFETs [29]. The impact of gate oxide breakdown on device *I-V* characteristics has been the subject of numerous studies over the past few decades. Oxide breakdown in the devices with relatively thick (>10 nm) oxides used in earlier technologies normally results in a catastrophic failure of the circuit after SBD or HBD. In [38], it has been shown that even soft breakdown can produce a strong decrease of the drain current and transconductance in MOSFETs with small *W*. This is due to the formation of a localized oxide damaged region likely trapping negative charge over a large portion of the channel width, around the soft breakdown conductive path. However, recent studies on advanced devices with thin gate oxide reveal that the oxide breakdown does not cause the device to fail destructively, and the circuit may still continue to function properly after breakdown [30, 31, 36]. In some cases, even if a hard breakdown (HBD) has occurred, this may not necessarily cause a failure of the circuit. In [106], it was found that a region of the channel surrounding the breakdown spot is physically damaged by the high current and can no longer carry current from drain to source. The radius of the damaged region can be evaluated between 1.4 and 1.8 μm. This result shows that devices having large W/L ratio can be still operative after breakdown. Hence, if the functioning of the circuit is chosen as the only reliability criterion, then it may be possible to relax oxide reliability requirements [36].

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On the other hand, the improved high frequency performance of deep submicron MOSFETs in conjunction with the capability of very large scale integration (VLSI) provides a great opportunity to use Si MOSFET for low noise radio frequency integrated circuits (RFICs) or microwave monolithic integrated circuits (MMICs). The impact of gate oxide breakdown on the RF characteristics of NMOSFET has attracted some attention [32, 33, 34]. It has been shown that the cut-off frequency and noise factors are degraded after stress (Figure 2.5 and 2.6). 1/*f* noise level in the MOSFET clearly increases after gate oxide breakdown. It is said that holes injected in the oxide can be a dominant source of the noise degradation [107]. Recently it has suggested that *N*MOSFETs noise at 2 GHz may not be thermal in origin. [35]

2.5.2 Gate oxide breakdown and location

The results of HBD and SBD are quite different, and thus they will manifest themselves differently when they occur in transistors will thus be dealt with separately.

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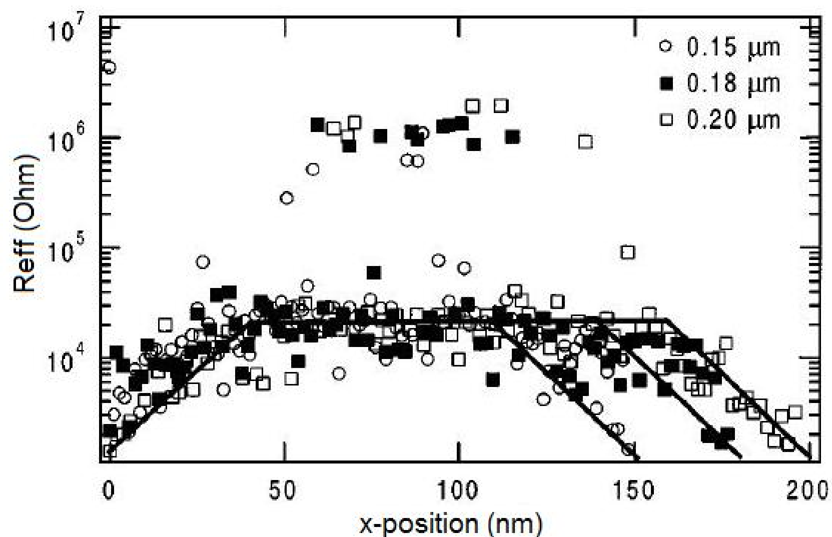

Figure 3.7 Effective gate post breakdown resistance as a function of the breakdown spot location along the channel in three short-channel NMOSFETs [29]

After HBD has occurred, there is a current path from the gate to the channel. The current path is generally characterized by a gate post-breakdown resistance defined as $R_{eff} = V_G/I_G$ [36]. The current through the gate is orders of magnitude larger than before breakdown. Thus to characterize the effects of HBD it becomes important to be able to find R_{eff}. In [20], the authors show that R_{eff} is dependent on the position of the breakdown along the length of the transistor. For a 0.2μm long transistor the post-breakdown resistance versus the position of the breakdown is shown in Figure 2.7. In regions in which the breakdown occurs over the source and drain extensions, R_{eff} increases linearly. Otherwise, if the breakdown occurs over the channel, R_{eff} is relatively constant. The linear increase in R_{eff} over the source/drain extensions is due to the resistance of the length of the n-doped region in the extension where the

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breakdown occurred. When the breakdown happens over the channel, it is as if current is injected from the gate through the breakdown path into the channel which then continues to the drain and the source. Regarding the magnitude of the current, it has been shown that after HBD near the source or drain, there is an increase of two orders of magnitude when the transistor is on, and an increase of six orders of magnitude when the gate voltage is near $0V$ [26]. In addition, increases of gate current of many orders of magnitudes, depending on the state of the transistor, have been observed [24]. The specific increase in current depends on many factors including the size of the transistor, and the size and location of the breakdown.

Unlike HBD, apart from increased leakage current in it's off state, SBD generally does not affect the performance of the transistor much [37]. With technologies that have thin t_{ox} the gate tunnelling leakage is large enough that any increase in gate current due to SBD in the transistor's on-state are not important. However, when the transistor is off, and if SBD occurs near the drain extension there is an increase in Gate-Induced Drain Leakage (GIDL) of five orders of magnitude. This increase in GIDL is due to the negative charge trapping in the oxide over the overlap region. SBD at other locations of the gate has very minimal effect on the operation of the transistor. Also, as the drain extension forms a much smaller percentage of the total transistor length, long-channel transistors are less likely to have any SBD effects, SBD does however affect circuit performance for transistors with low W/L. Since the gate area is very small, the SBD region composes a considerable portion of the gate area.

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Under such circumstances, the transconductance g_m of the transistor drops by 50% and the saturation current falls to 30% of its original value [38].

2.6 Carrier heating and channel noise in sub-micron MOSFET

Hot carriers can be trapped at the Si-SiO2 interface or within the oxide itself and hence interface states are generated in the process, forming space charges (volume charges) that increase over time as more carriers are trapped. These trapped charges shift some of the characteristics of the device, such as its threshold voltage (V_{th}).

Injected carriers that do not get trapped in the gate oxide become gate current. On the other hand, the majority of the holes from the e-h pairs generated by impact ionization flow back to the substrate, comprising a large portion of the substrate's drift current. Excessive substrate current may therefore be an indication of hot carrier degradation. In gross cases, abnormally high substrate current can upset the balance of carrier flow and facilitate latch-up.

Hot-carrier effects are among the main concerns when shrinking FET dimensions into the deep sub micrometer regime. Experiments have shown that, in short-channel devices, the measured drain current noise is much higher than the one predicted by the long-channel model. The most popular explanation for the excess channel thermal noise observed in sub micrometer MOSFETs is based on the postulation of carrier heating and hot carriers. It is expected that the increase of mobility with reduced gate bias enhances carrier velocity and

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consequently the value of the noise factor γ since high γ is due to phenomena like velocity saturation and hot electrons [32].

However, recent modeling results reported from different research groups [39, 40] do not support the above postulation. Scholten *et al.* [29] suggest that it is possible to predict the excess noise without invoking carrier heating based on a surface-potential-based compact MOS model with improved descriptions of carrier mobility and velocity saturation. Chen and Deen [30] demonstrated that the excess channel noise in deep-sub micrometer MOSFETs could be modeled by considering channel length modulation. Furthermore, simulation based on a non-stationary transport model [41] suggests that the source side of the channel is responsible for most of the excess noise. This obviously does not support the explanations related to carrier heating and velocity saturation where the drain side of the channel is associated with these phenomena. It is noted that all the aforementioned studies were based on complicated RF modeling, and some ambiguities could arise during the definition of device models and parameter extraction. This, in turn, influences the direct understanding of the various physical origins of RF noise in sub micrometer devices. To date, however, solid evidence of the dependence of channel noise on carrier heating is still lacking.

On the other hand, recent studies on deep-sub micrometer MOSFETs with reverse body bias (V_b) reveal that a reverse V_b increases the electric field of the drain–substrate junction which then induces secondary impact ionization by the enhanced heating of holes [42, 43, 44]. This then substantially increases the

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population of high-energy (hot) carriers. This was confirmed by Monte Carlo simulation [45] and light emission measurement [46]. The carrier heating in sub micrometer NMOSFETs by reverse V_b provides a possible means to directly verify the contribution of carrier heating to channel noise by modulating the number of high-energy electrons.

2.7 Summary

In this chapter, a small signal equivalent circuit of RF MOSFETs is introduced. The small signal modeling methods are reviewed. This is followed by a detailed description of a procedure to extract the parameters in the equivalent circuit. Noise sources in electronic devices are investigated. Three major noise sources exist in MOSFETs, thermal noise, shot noise and flicker noise. The physical origins are studied and their manifestations in MOSFETs are presented with equations to describe their behaviors. Noise parameters are defined, which are used to describe noise performances of a device. After that, noise two-port networks and direct matrix operations are used to extract noise currents in MOSFETs directly from noise and small-signal measurements. In the final part, previous work on the relationship of gate oxide breakdown and noise, gate oxide breakdown and location, hot carrier heating and hot carrier effect and channel noise is reviewed.

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Chapter 4 Experiments

3.1 Devices

The devices used for the tests in this work are n-MOSFETs fabricated using a commercial dual gate oxide process with shallow trench isolation (STI). The N-MOSFETs had 16 or 8 gate fingers with a drawn channel length and width of 0.18 μm and 5 μm respectively. The gate oxide was ~29 Å thick containing ~1% nitrogen, grown via rapid thermal oxidation and N_2O annealing.

3.2 Measurements

Device characterizations were carried out using a semi-auto Cascade probe station. An HP4156B semiconductor parameter analyzer was used for DC measurements. Device S-parameters were measured using an HP8510B network analyzer with a frequency of up to 50 GHz.

All noise parameters were measured using Agilent NP5 noise parameter measurement system. The NP5 measurement system was used to characterize two-port devices for S-parameter and noise parameter measurements as a function of source impedances. All of these measurements can be made in a single contact of the device, eliminating the need to load and re-contact the device on individual measurement stands. The measurement test plan is user definable allowing combinations of measurement types, frequencies, and biases.

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The system has a modular architecture for configuration flexibility and consists of several separate core components which perform the functions critical to small signal measurements: an NP5 Mainframe, a Mismatch Noise Source (MNS), and a Remote Receiver Module (RRM). These core components are combined with a suite of test equipment (network analyzer, noise figure meter, computer, and various other accessories) to complete the system (Figure 3.1).

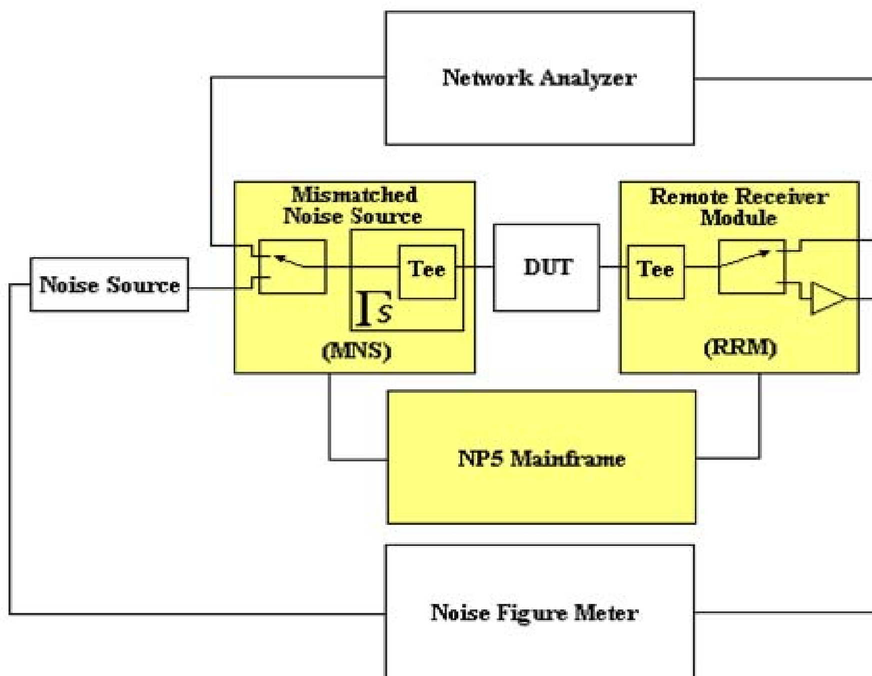

Figure 4.1 NP5 system block diagram

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Before each measurement, the system was calibrated. This enables the placing of the calibration reference planes directly at the DUT without explicit knowledge of the test fixture or test probe S-parameters. Figure 3.2 shows simplified diagrams of NP5 system calibration and device-under-test (DUT) reference planes. The reference planes are labeled RP1 through RP2.

These reference planes are suitable for performing a coaxial S-parameter calibration. RP1 and RP2 are the reference planes for the DUT evaluation. At RP1, source admittance is tuned to find the matching point for minimum noise figure of the device. RP2 is the reference plane where the coaxial calibration standards (Short/Open/Load or S/O/L) and the coaxial power meter interface are connected.

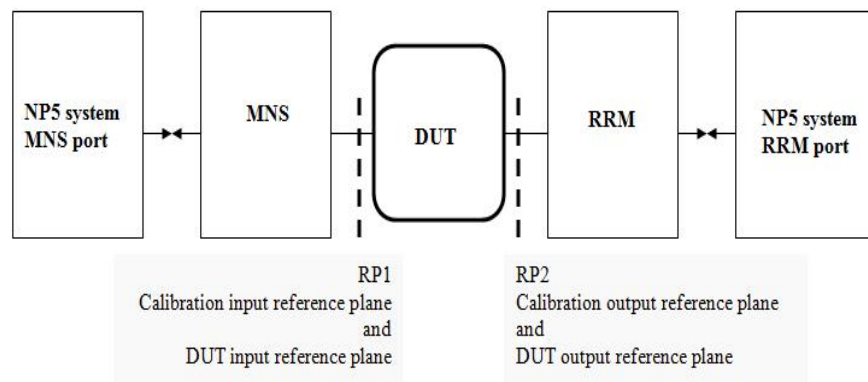

Figure 4.2 Schematic for on-wafer noise calibration.

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3.3 De-embedding

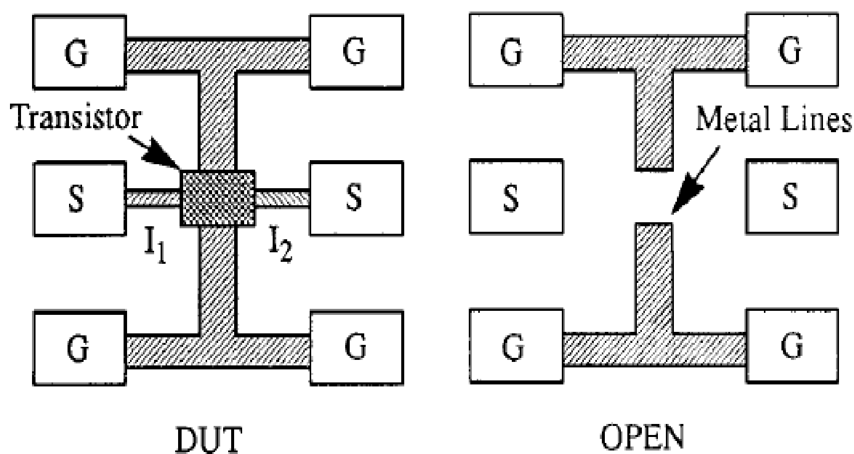

Figure 4.3 Device and dummy layout for parasitics de-embedding [47]

A measurement result from a calibrated probe is the response of the tested device, including parasitics associated with probe pads. In order to get the DUT response from measurement, the parasitics of the pad must be removed. Layout patterns, one including the DUT while the other (dummy) excluding it, are fabricated on the same wafer as shown in Figure 3.3. The correction of measurement results for pad parasitics is often called "pad de-embedding".

The topology of the pads parasitics with the intrinsic transistor is a parallel configuration as shown in the following Figure 3.4:

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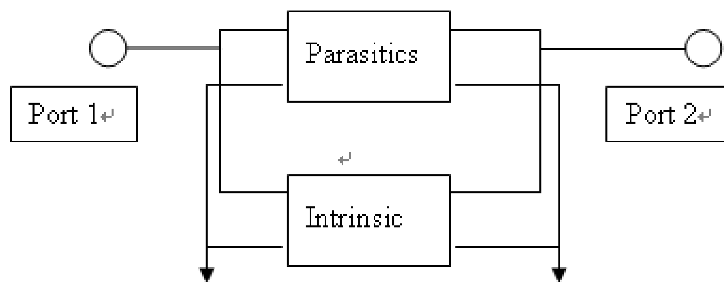

Figure 4.4 Topology of the pads parasitics with the intrinsic transistor

From the S-parameter measurement of the device and the pads, we define the two-port extrinsic S-parameter matrix as

$$S_E = \begin{pmatrix} S11_E & S12_E \\ S21_E & S22_E \end{pmatrix}. \tag{3.1}$$

The pads parasitic S-parameter matrix is defined as

$$S_P = \begin{pmatrix} S11_P & S12_P \\ S21_P & S22_P \end{pmatrix}. \tag{3.2}$$

S_p matrix can be transformed to the Y-parameters. We calculate the noise correlation matrix of the pad's parasitic, C_p, from the Y-parameters. Using the equivalent circuit transformations from ABCD to Y format, we extract the admittance matrix of the intrinsic device by:

$$Y_I = Y_E - Y_P \tag{3.3}$$

and noise correlation matrix in admittance format of the intrinsic device by:

$$C_I^Y = C_E^Y - C_P^Y. \tag{3.4}$$

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C_Y can be calculated from Equations (2.19), (2.20) and (2.24) after the four noise-parameters are measured.

Finally, we use the equivalent circuit transformations from the *Y* to the *S* format to calculate the intrinsic *S*-parameter matrix and the intrinsic noise parameters.

3.4 Summary

In this chapter, devices used in our research work are introduced and the test equipments and methodology are investigated. Agilent NP5 noise measurement system, assembled with network analyzer, is used to measure *S*-parameters and noise parameters. This system can characterize small-signal and noise figures of a two-port device as a function of source impedances. Calibration and de-embedding methods are presented.

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Chapter 5 Simplified Extraction of Channel Noise and Induced Gate Noise in Submicron RF MOSFETs for Fast Wafer Level RF Noise Measurements

4.1 Introduction

The continued downscaling of CMOS technologies has resulted in strong improvements in the performance of MOS devices in the radio-frequency (RF) region. Consequently CMOS has become a viable option for analogue RF applications and RF systems on a chip. For the application of modern CMOS technologies in low-noise RF circuits, accurate modelling of device noise is required. A crucial procedure in noise analysis is to extract channel and induced gate noise currents directly from RF noise measurements. Several noise models and extraction methods have been presented [48, 49, 50]. All of these classic network matrix type methods require the time-consuming extraction of small-signal parameters at each bias point separately. Complex matrix computations are also involved in [49]. Furthermore, because of high gate voltages commonly applied in the cold modelling used for the extraction of parasitic parameters, the device being tested may be heavily stressed or even destroyed during measurements. These make fast extraction of channel and induce gate noises during fast wafer level testing stage to be a difficult task.

In this chapter, a simplified method to calculate the induced gate noise and channel noise is proposed and evaluated based on characteristics of deep

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submicron RF MOSFETs. By carefully evaluating a typical noise equivalent circuit of RF MOSFET which includes the noise contribution from the following five subnetwork: the intrinsic part, the source resistance, the substrate network, the drain resistance and gate resistance network. A simplified procedure with only one step matrix calculation is proposed, which is detailed in section 4.2. In section 4.3, the extraction of noise current from a 0.18μm multiple-finger RF MOSFET using our method is compared with the results obtained using the traditional method. The extraction errors at different frequencies and DC bias conditions are studied.

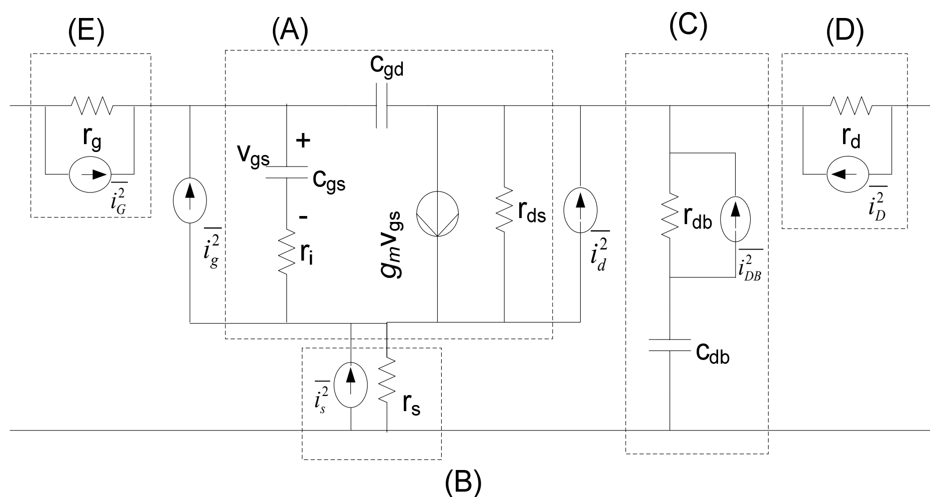

Figure 5.1 Small signal equivalent noise circuit of substrate grounded MOSFET with five subnetworks: (A) the intrinsic part of the transistor (B) the source resistance (C) the substrate network (D) the drain resistance and (E) the gate resistance network

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4.2 Extraction method

Figure 4.1 shows a model of a substrate grounded MOSFET suitable for RF low noise application [9]. The principles of the analysis procedure are explained with reference to Figure 4.2. A decomposition of the equivalent circuit into basic two-ports **A**, **B**, **C**, **D** and **E** is carried out. Each two-port represents a sub-network comprising the equivalent circuit: the intrinsic part of the transistor (**A**), the source resistance (**B**), the substrate network (**C**), the drain resistance (**D**) and gate resistance network (**E**). All of the two-ports are specified by their electrical and correlation matrices. The equivalent circuit of the MOSFET is obtained in a matter that the five sub two-ports are successively interconnected shown in Figure 4.2. Two-port **A** and **B** are interconnected in series to form a noiseless network **N2** with two current noise sources at two ports each, followed by interconnections with two-port **C**, **D** and **E** in cascade. $\overline{i_g^2}$ And $\overline{i_d^2}$ are intrinsic noise currents. All the contributions from parasitic or external elements (**B**, **C**, **D** and **E**) are added to the intrinsic noise currents in term of the network connection to obtain the representation of the whole circuit (**N5**). For example, **N2** results from interconnecting **A** and **B** in series. The matrices characterizing two-port **N2** are determined by the following two-step procedure: 1) the matrices of **A** and **B** are transformed into impedance representation which is the appropriate representation for serial interconnection; 2) adding the electrical matrices of **A** and **B** yields the electrical matrix of **N2**, and adding the correlation matrices of **A** and **B** yields the correlation matrix of

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N2 (Figure 4.2 a). In this similar manner, the calculated noise currents of the formed networks are compared with the intrinsic currents in each step. The simplified method is proposed based upon the derivation. In the following parts, we are going to derive and discuss each two port network representations in details.

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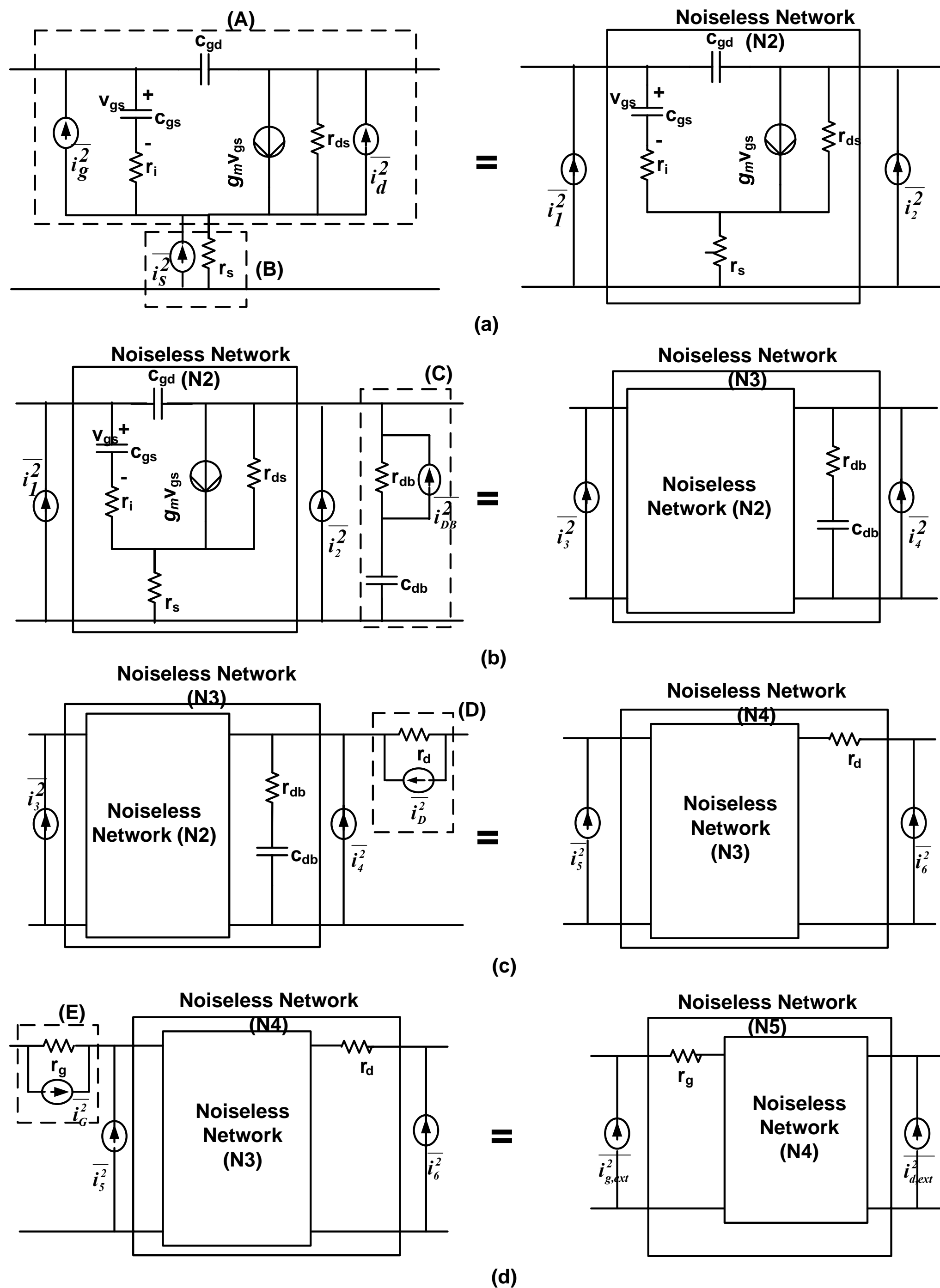

Figure 5.2 Network representation of the equivalent circuit: (A) the intrinsic part of the transistor (B) the source resistance (C) the substrate network (D) the drain resistance and (E) the gate resistance network

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4.2.1 Source resistance noise

Consider the network representation in Figure 4.2(a), which is composed of the intrinsic elements and source resistance R_s. We define Z_{in} as the impedance matrix, Y_{in} as the admittance matrix and C_{iny} as the admittance correlation matrix of **A**, respectively and C_{ze} as the impedance correlation matrix of **B** and r_s as the source resistance. The network representations can be given by:

$$Z_{in} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix},$$

$$Y_{in} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix},$$

$$C_{iny} = \begin{bmatrix} C_{y11} & C_{y12} \\ C_{y21} & C_{y22} \end{bmatrix}, \text{ And}$$

$$C_{ze} = 4kT\begin{bmatrix} R_s & R_s \\ R_s & R_s \end{bmatrix} = 4kTZ_e. \tag{4.1}$$

The connection of two two-ports in series results in an impedance correlation matrix C_z given by:

$$C_z = C_{zin} + C_{ze} = Z_{in}C_{iny}Z_{in}^H + C_{ze}, \tag{4.2}$$

where H of Z_{in}^H denotes the Hermitian conjugate.

The admittance correlation matrix C_y of **N2** can be transformed from:

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$$
\begin{aligned}
C_y &= (Z_{in} + Z_e)^{-1} C_z ((Z_{in} + Z_e)^{-1})^H \\
&= (Z_{in} + Z_e)^{-1} (Z_{in} C_{iny} Z_{in}^H + C_{ze})((Z_{in} + Z_e)^{-1})^H \\
&= (Z_{in} + Z_e)^{-1} Z_{in} C_{iny} Z_{in}^H ((Z_{in} + Z_e)^{-1})^H + (Z_{in} + Z_e)^{-1} C_{ze} ((Z_{in} + Z_e)^{-1})^H
\end{aligned}
\quad (4.3)
$$

For the first item at the right side of the equation, if r_s is very small comparing with the intrinsic Z-parameters, it can be simplified as $C_{iny.}$ In fact, this condition is very easily satisfied in advanced MOSFET.

Typically the source and drain resistance without including any bias dependence can be estimated by [51]:

$$
\begin{aligned}
R_s &= R_{s0} + \frac{r_{sw}}{N_f W_f} \\
R_d &= R_{d0} + \frac{r_{dw}}{N_f W_f}
\end{aligned}
\quad (4.4)
$$

where r_{sw} and r_{dw} are the parasitic source and drain resistances in unit width, R_{s0} and R_{d0} account for the part of the series resistances without the width dependence. Considering the MOSFETs for low noise RF circuit applications, for easy noise and maximum power gain matching in low noise amplifier design, a multi-finger designed with large total gate width is required [52]. Therefore, the drain and source resistances of a MOSFET for low RF noise circuits with multiple gate design can be quite small. Table 4.1 lists some published results [53]. It can be seen that, for the devices with multiple gate design, the drain and source ressitances are much smaller than 1Ω.

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Table 5.1 Typical drain and source resistances

No	W_f (μm)	No. of fingers (N_f)	r_d (Ω)	r_s (Ω)
1	12.5	16	0.02	0.02
2	12.5	8	0.01	0.01
3	12.5	4	0.05	0.05

Small drain and source resistances are also confirmed in the 0.18μm devices used in this study. The extracted r_d and r_s and Z-parameters of the devices are listed in Table 4.2.

Table 5.2 The Z-parameters and extracted r_d and r_s of two RF devices

W/L (μm)	320/0.18		80/0.18	
$r_s(r_d)$ (Ω)	*0.25*		*0.8*	
freq	*f*=2 GHz	*f*=5 GHz	*f*=2 GHz	*f*=5 GHz
Z_{11}	26.05-j29.4	22.88-j18.56	74.45-j99.66	74.89-j67.48
Z_{12}	5.87+j0.78	5.99+j1.34	20.72 -j0.41	20.47-j1.43
Z_{22}	94.19+j443.34	67.1+j233.55	83.86 -j17.69	291.37+j924.48
Z_{22}	20.83-j0.53	20.21+j0.58	83.86 -j17.69	77.58-j16.9

It can be seen that r_s (r_d) <<Z-parameters. Hence Equation (4.3) can be simplified as:

$$
\begin{aligned}
C_y &= C_{iny} + (Z_{in} + Ze)^{-1} C_{ze}((Z_{in} + Z_e)^{-1})^H \\
&= C_{iny} + \frac{4kT}{|\mathrm{K}|^2}\begin{bmatrix} Z_{22} + R_s & -Z_{12} - R_s \\ -Z_{21} - R_s & Z_{11} + R_s \end{bmatrix} \times \begin{bmatrix} R_s & R_s \\ R_s & R_s \end{bmatrix} \times \begin{bmatrix} Z_{22}^* + R_s & -Z_{21}^* - R_s \\ -Z_{12}^* - R_s & Z_{11}^* + R_s \end{bmatrix} \\
&= C_{iny} + \frac{4kT}{|\mathrm{K}|^2}\begin{bmatrix} R_s(Z_{22} - Z_{12})(Z_{22}^* - Z_{12}^*) & R_s(Z_{22} - Z_{12})(Z_{11}^* - Z_{21}^*) \\ R_s(Z_{11} - Z_{21})(Z_{22}^* - Z_{12}^*) & R_s(Z_{11} - Z_{21})(Z_{11}^* - Z_{21}^*) \end{bmatrix}
\end{aligned}
$$

,

(4.5)

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where $\mathrm{K} = (Z_{11} + R_s)(Z_{22} + R_s) - (Z_{12} + R_s)(Z_{21} + R_s)$.

$\overline{i_1^2}$ and $\overline{i_2^2}$ can be determined as:

$$\frac{\overline{i_1^2}}{\Delta f} = C_{y11} + \frac{4kT}{|\mathrm{K}|^2} R_s |Z_{22} - Z_{12}|^2 = \frac{\overline{i_g^2}}{\Delta f} + \frac{4kT}{|\mathrm{K}|^2} R_s |Z_{22} - Z_{12}|^2$$
$$\frac{\overline{i_2^2}}{\Delta f} = C_{y22} + \frac{4kT}{|\mathrm{K}|^2} R_s |Z_{11} - Z_{21}|^2 = \frac{\overline{i_d^2}}{\Delta f} + \frac{4kT}{|\mathrm{K}|^2} R_s |Z_{11} - Z_{21}|^2$$

(4.6)

The gate current noise is often defined as:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\beta \frac{(\omega c_{gs})^2}{g_{d0}} \quad , \qquad (4.7)$$

It can be inferred that

$$\frac{4kT}{|K|^2} r_s |Z_{22} - Z_{12}|^2 = 4kTr_s |Y_{11} + Y_{12}|^2 \approx 4kTr_s \frac{(\omega c_{gs})^2}{1 + (\omega c_{gs})^2}$$

(4.8)

where ω is the frequency and c_{gs} is the gate-source capacitance.

For sub-micron MOSFETs at a few GigaHerz frequency, the condition of $r_s << \beta / g_{d0}$ is satisfied. Therefore, the term $4kTr_s \frac{(\omega c_{gs})^2}{1 + (\omega c_{gs})^2}$ can be neglected in the calculation of $\overline{i_1^2}$. The extrinsic noise current $\overline{i_1^2}$ is approximately equal to intrinsic current $\overline{i_g^2}$. Since the induced gate noise is far less than the thermal noise and the second term on the right hand of the

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equation for $\overline{i_2^2}$ is on the same order of the second term for $\overline{i_1^2}$, the extrinsic current $\overline{i_2^2}$ can be considered equal to $\overline{i_d^2}$. Hence

$$\overline{i_1^2} = \overline{i_g^2}$$

$$\overline{i_2^2} = \overline{i_d^2} \tag{4.9}$$

4.2.2 Substrate network noise

Figure 4.2b shows a network including **N2** (intrinsic part and source resistant) and substrate network. The ABCD-matrix A_1 for Network **N2** and chain correlation matrix C_{A2} for two-port **C** can be defined as follows:

$$A_1 = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \text{ and}$$

$$C_{A2} = 4kT\begin{bmatrix} 0 & 0 \\ 0 & \dfrac{r_{db}}{|Z|^2} \end{bmatrix}, \tag{4.10}$$

where $Z = r_{db} + \dfrac{1}{j\omega C_{db}}$.

The chain correlation matrix of network **N3** is calculated by:

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$$
\begin{aligned}
C_A &= A_1 C_{A2} A_1^H + C_{A1} \\
&= 4kT\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}\begin{bmatrix} 0 & 0 \\ 0 & \dfrac{r_{db}}{|Z|^2} \end{bmatrix}\begin{bmatrix} A_{11}^* & A_{21}^* \\ A_{12}^* & A_{22}^* \end{bmatrix} + C_{A1} \\
&= 4kT\begin{bmatrix} \dfrac{r_{db}|A_{12}|^2}{|Z|^2} & \dfrac{A_{12}A_{22}^* r_{db}}{|Z|^2} \\ \dfrac{A_{22}A_{12}^* r_{db}}{|Z|^2} & \dfrac{r_{db}|A_{22}|^2}{|Z|^2} \end{bmatrix} + C_{A1}
\end{aligned}
\tag{4.11}
$$

Therefore the correlation matrix C_y in admittance form of **N3** is:

$$C_y = TC_A T^H \tag{4.12}$$

where $T = \begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}$ is the transformation matrix and y_{11} and y_{21} are *y*-parameters of network **N3**. From the definition of the *y*-parameters, it can be inferred that y_{11} and y_{21} of network **N3** are equal to y_{11} and y_{21} of Network **N2**, respectively.

Substituting (4.11) into (4.12), we can get:

$$
\begin{aligned}
C_y &= \begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}\left(4kT\begin{bmatrix} \dfrac{r_{db}|A_{12}|^2}{|Z|^2} & \dfrac{A_{12}A_{22}^* r_{db}}{|Z|^2} \\ \dfrac{A_{22}A_{12}^* r_{db}}{|Z|^2} & \dfrac{r_{db}|A_{22}|^2}{|Z|^2} \end{bmatrix} + C_{A1}\right)\begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}^H \\
&= 4kT\begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}\begin{bmatrix} \dfrac{r_{db}|A_{12}|^2}{|Z|^2} & \dfrac{A_{12}A_{22}^* r_{db}}{|Z|^2} \\ \dfrac{A_{22}A_{12}^* r_{db}}{|Z|^2} & \dfrac{r_{db}|A_{22}|^2}{|Z|^2} \end{bmatrix}\begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}^H + C_{y1}
\end{aligned}
\tag{4.13}
$$

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where C_{y1} is the admittance correlation matrix of Network **N2**.

From the ABCD-matrix definition, it can be obtained that:

$$A_{12} = \frac{-1}{y_{21}}, \qquad A_{22} = -\frac{y_{11}}{y_{21}} \tag{4.14}$$

Substituting (4.14) to (4.13) and apply matrix operation gives:

$$C_y = C_{y1} + 4kT\begin{bmatrix} 0 & 0 \\ 0 & \frac{r_{db}}{|Z|^2} \end{bmatrix}. \tag{4.15}$$

Hence

$$\begin{aligned} &\frac{\overline{i_3^2}}{\Delta f} = \frac{\overline{i_1^2}}{\Delta f} = \frac{\overline{i_g^2}}{\Delta f} \\ &\frac{\overline{i_4^2}}{\Delta f} = \frac{\overline{i_2^2}}{\Delta f} + 4kT\frac{r_{db}}{|Z|^2} = \frac{\overline{i_d^2}}{\Delta f} + 4kT\frac{r_{db}}{|Z|^2} = 4kT(\gamma g_{d0} + \frac{r_{db}}{|Z|^2}) \end{aligned}. \tag{4.16}$$

where γ is a constant higher than 1 for deep submicron MOSFETs and g_{d0} is the channel conductance at zero drain source voltage. The second term in Equation (8) can be neglected because $\frac{r_{db}}{g_{d0}}$ is much smaller than $|Z|^2$ (i.e. $\frac{r_{db}}{g_{d0}} << |Z|^2$) in the low GigaHertz frequency range. This can be confirmed by published data as well as the extracted results from our devices, which are shown in Table 4.3.

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Table 5.3 Extracted parameters from small signal equivalent circuits

r_{db} (Ω)	c_{db} (fF)	g_m (mS)	$\frac{r_{db}}{\lvert Z\rvert^2 g_{d0}}$	
			f=2GHz	f=5GHz
191 [54]	80	20	0.0022	0.0019
85[55]	105	10.1	0.0037	0.0034
15	60.2	42	0.0002	0.0012

Therefore, we have

$$\begin{aligned} \overline{i_3^2} &= \overline{i_g^2} \\ \overline{i_4^2} &= \overline{i_d^2} \end{aligned}. \tag{4.17}$$

4.2.3 Drain resistance noise

The drain resistance is connected to network **N3** in series (Figure 4.2c). Applying the same method, the chain correlation matrix of network **D** can be calculated as:

$$C_{A2} = 4kT\begin{bmatrix} R_d & 0 \\ 0 & 0 \end{bmatrix}. \tag{4.18}$$

The ABCD-matrix A_1 of network **N3** is defined as:

$$A_1 = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}. \tag{4.19}$$

The chain correlation matrix of network **N4** is calculated by:

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$$C_A = A_1 C_{A2} A_1^H + C_{A1}$$
$$= 4kT\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}\begin{bmatrix} R_d & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} A_{11}^* & A_{21}^* \\ A_{12}^* & A_{22}^* \end{bmatrix} + C_{A1} , \quad (4.20)$$
$$= 4kT(\begin{bmatrix} R|A_{11}|^2 & A_{11}A_{21}^*R \\ A_{21}A_{11}^*R & R|A_{21}|^2 \end{bmatrix}) + C_{A1}$$

where C_{A1} is the chain correlation matrix of network **N3**.

Therefore the correlation matrix C_y in admittance form of **N4** is:

$$C_y = TC_A T^H , \quad (4.21)$$

where $T = \begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}$ is the transformation matrix and y_{11} and y_{21} are y-parameters of network **N4**. r_d is negligible comparing with Z_{22} of network **N3**, the ABCD-parameters of **N4** can be considered equal to the ABCD-parameters of the network **N3**. Then we can substitute the ABCD-matrix of **N4** to equation (21) and we can have:

$$C_y = 4kT\begin{bmatrix} |y_{12}|^2 R_d & y_{12}y_{22}^* R_d \\ y_{22}y_{12}^* R_d & |y_{22}|^2 R_d \end{bmatrix} + C_{y1} . \quad (4.22)$$

where C_{y1} is the admittance correlation matrix of Network **N3**.

Therefore

$$\frac{\overline{i_5^2}}{\Delta f} = \frac{\overline{i_g^2}}{\Delta f} + 4kT|y_{12}|^2 R_d . \quad (4.23a)$$

$$\frac{\overline{i_6^2}}{\Delta f} = \frac{\overline{i_d^2}}{\Delta f} + 4kT|y_{22}|^2 R_d \quad (4.23b)$$

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Since $|y_{12}| \approx \omega c_{gd}$ and $r_d << \beta / g_{d0}$, the term $4kT|y_{12}|^2 r_d$ can thus be neglected in the calculation of $\frac{\overline{i_5^2}}{\Delta f}$ by the same inference as in the analysis of source resistance noise. Again the induced gate noise is far less than the thermal noise in advanced RF MOSFETs and the second term on the right hand of the equation for $\overline{i_6^2}$ is on the same order of the second term for $\overline{i_5^2}$. Thus we have

$$\overline{i_6^2} = \overline{i_d^2} \tag{4.24a}$$

Furthermore, the second term is very small comparing with the first one on the right side of Equ.(4.23a). Hence

$$\overline{i_5^2} = \overline{i_g^2} \tag{4.24b}$$

4.2.4 Gate resistance noise

In the classical network matrix method to extract the intrinsic noise currents, the extraction of parameters in the equivalent circuit is aimed to remove the extrinsic elements. As we can see that, since the contributions from some extrinsic elements are small in RF MOSFETs, the lengthy extraction procedure is not crucial. However the contribution from gate resistance to the noise extraction can not be neglected [48]. Its contribution can be calculated as

$$\overline{v_g^2} = 4kTr_g\Delta f \tag{4.25}$$

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where $\overline{v_g^2}$ represents the voltage noise source of gate resistance, and r_g is the effective noise resistance of the gate. Because of the distributed effect of gate resistance, r_g is given by [16]

$$r_g = \frac{R_{g-sh}}{3}(\frac{W_g}{L_g}) \tag{4.26}$$

where $R_{g\text{-}sh}$ is gate sheet resistance, W_g is the width of the gate, and L_g is the gate length. Fortunately, r_g or $R_{g\text{-}sh}$ can be obtained from the on-wafer DC electrical test structure.

4.3 Experimental verification and discussion

From the analysis above, the whole MOSFET can be simplified as two cascaded connected two-port networks. The first network just includes gate resistance r_g (**E**) and the second part includes all the elements except r_g (**N4**) as in Figure 4.2d. For the cascaded connection, the correlation matrix of the device C_A is related to the correlation matrices of the two networks by

$$C_A = A_1 C_{A2} A_1^+ + C_{A1}, \tag{4.27}$$

where A_1 and C_{A1} are the ABCD-parameter and correlation matrix of network **E** respectively, and C_{A2} is the matrix for **N4**. C_A can be calculated directly from the noise measurements. As a result, the noise currents can be determined from admittance correlation matrix C_{Y2} with very simple matrix transformation and computation as below:

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$$C_{Y2} = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix} C_{A2} \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}^H$$

$$\overline{i_g^2} = C_{Y11} \tag{4.28}$$

$$\overline{i_d^2} = C_{Y22}$$

The Y-parameters in the above equations are the Y-parameters of **N4**.

This method was verified by a MOSFET device with drawn channel dimensions of L/W = 0.18μm/5μm and multiple gate layout. The data shown here were measured from the devices with eight gate fingers.

The intrinsic noise currents were extracted using the method in [56] to compare with the noise currents calculated based on the simplified method in this chapter. The channel noise currents and induced gate noise currents are shown in Figure 4.3 and Figure 4.4 respectively. The extracted channel noise and induced gate noise currents follow the general trend, that is, the channel noise is frequency independent and the induced gate noise is proportional to f^2.The difference between two channel noise currents from two methods is also shown in Figure 4.3. It can be found that the channel noise currents calculated from Equation (4.28) and the extracted intrinsic noise currents from [56] have small discrepancy at frequencies below 10GHz. The higher discrepancy at higher frequencies can be explained from equations (4.16), which is rewritten here.

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$$\frac{\overline{i_3^2}}{\Delta f} = \frac{\overline{i_1^2}}{\Delta f} = \frac{\overline{i_g^2}}{\Delta f}$$

$$\frac{\overline{i_4^2}}{\Delta f} = \frac{\overline{i_2^2}}{\Delta f} + 4kT\frac{r_{db}}{|Z|^2} = \frac{\overline{i_d^2}}{\Delta f} + 4kT\frac{r_{db}}{|Z|^2} = 4kT(\gamma g_{d0} + \frac{r_{db}}{|Z|^2})$$

where $Z = r_{db} + \frac{1}{j\omega C_{db}}$.

When the frequency increased, the network impedance Z becomes smaller. From this equation, the contribution to the device noise from substrate network therefore increases.

The comparison of the extracted induced gate noise currents from the simplified method and the traditional method is shown in Figure 4.4. The induced gate noise is low in GHz range. The calculated noise currents from both methods are distributed narrowly along the f^2 line. At high RF frequencies, the data from both methods show a clearer trend with frequency and the currents from the simplified method agree well with those from the traditional procedure. From Equation (4.16), the substrate network does not contribute to the induced gate noise. At high frequencies, the noise currents from our method agree well with the intrinsic noise extracted from the classic method. It can be noticed that the difference at low to medium frequency (<6GHz) is more apparent than at higher frequencies. At low to medium frequencies, the gate induced noise ($<10^{-24}$ A^2/Hz) is extremely low. The calculation error can have an important effect on the final results, which is shown in [105] too.

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For the bias dependence of the calculated noise sources, Figures 4.5 and 4.6 show the $\overline{i_d^2}$ and $\overline{i_g^2}$ versus V_{gs} with bias voltage of V_{ds}=1.1V at frequency 3 and 10 GHz, respectively. It is shown that $\overline{i_d^2}$ has a strong bias dependence and increases the trend to saturate when V_{gs} increases, but $\overline{i_g^2}$ has a weak dependence on V_{gs}. The increase of channel noise with gate bias can be explained by the increase of g_{d0} [57]. The gate source capacitance is not sensitive to gate bias [54]. In saturation region, the channel noise currents can be well predicted from the extrinsic noise calculated from our method. But there's a big gap at gate bias at 0.7V. This difference is due to small g_{d0} at low gate bias [58]. At low gate bias, the term of substrate noise in Equation (4.16) cannot be ignored and therefore the effect of substrate must be taken into account in the calculation of channel noise calculation. Since most of the low noise amplifier is designed in saturation to take full advantage of low noise figure of MOSFET, our method can be widely used in practical applications. Meanwhile, substrate doesn't contribute to induced gate noise from Equation (4.16) so no big discrepancy is observed in Fig. 4.6.

Finally, Figures 4.7 and 4.8 show the extracted $\overline{i_d^2}$ and $\overline{i_g^2}$ versus V_{ds} characteristics at V_{gs}=1.1V. Again, excellent agreement of the results from our method and standard procedure is observed.

Extraction of channel noise and induced noise currents is necessary in most of the noise analysis. A usual procedure is to measure the RF noise with a

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noise measurement system followed by small signal modeling parameters and noise extraction procedure at different bias points. The complicate small signal parameter extraction of the MOSFETs generally requires human interaction. It is difficult to extract channel and induced gate noises using a fully automatic approach during fast wafer level measurements. The proposed one-step matrix extraction in this chapter makes it possible to integrate the extraction procedure into the noise testing system and therefore provide an effective means to quick evaluate the noise currents after the collection of noise parameters by the testing system. This helps facilitate the noise analysis and change the testing schedules from the real-time noise currents. Furthermore, for the new generation of RF MOSFETs fabricated using more advanced processes, the source resistance r_s and drain resistance r_d become even smaller than those of their longer channel counterparts. The method evaluated based on 0.18 μm technology should be able to extend for the new device generations.

4.4 Summary

In this chapter, a simplified procedure for quick extraction of channel and induced gate noise in RF MOSFET has been presented. It has been found that, for RF MOSFETs, which have reasonably small source and drain resistances, the channel and induced gate noise can be simply extracted using one step matrix calculation based on measured noise parameters (NF_{min}, R_n, and G_{opt}) without involving small signal equivalent parameter extraction. The main advantage of the simplified extraction is the possibility to carry out channel and

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induced gate noise extraction during the fast wafer level measurements. By using the proposed method, it is possible with reasonable accuracy in GHz frequency range. Experimental results demonstrate that effectiveness of the proposed approach for characterization of MOSFETs with multiple gate fingers and large gate width designed for low noise RF applications.

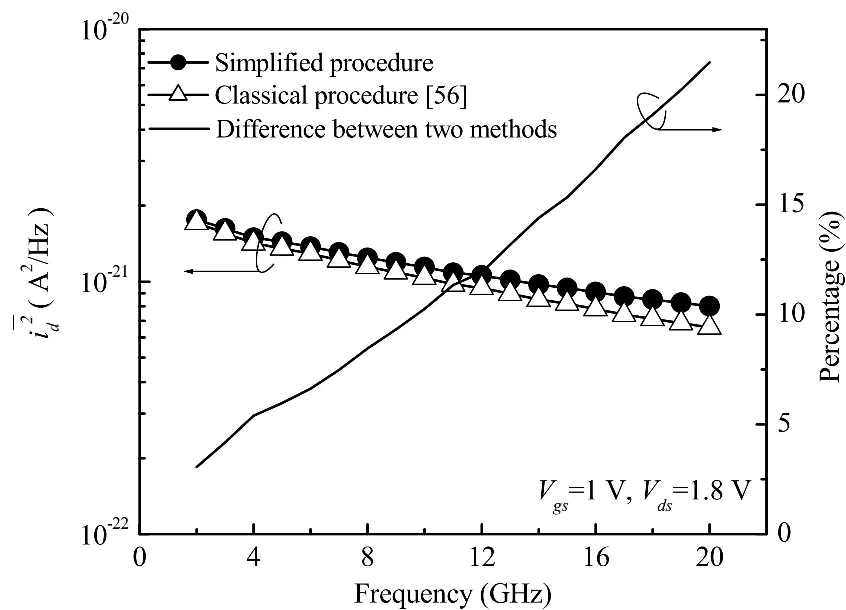

Figure 5.3 Drain current thermal noise versus frequency at V_g=1V, $V_{D=}$1.8V

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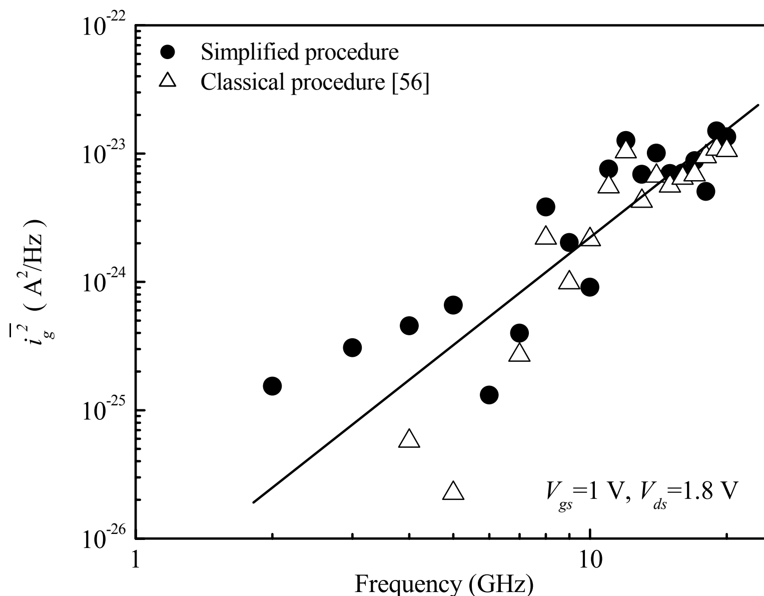

Figure 5.4 Induced gate noise versus frequency at V_g=1V, $V_{D=}$1.8V

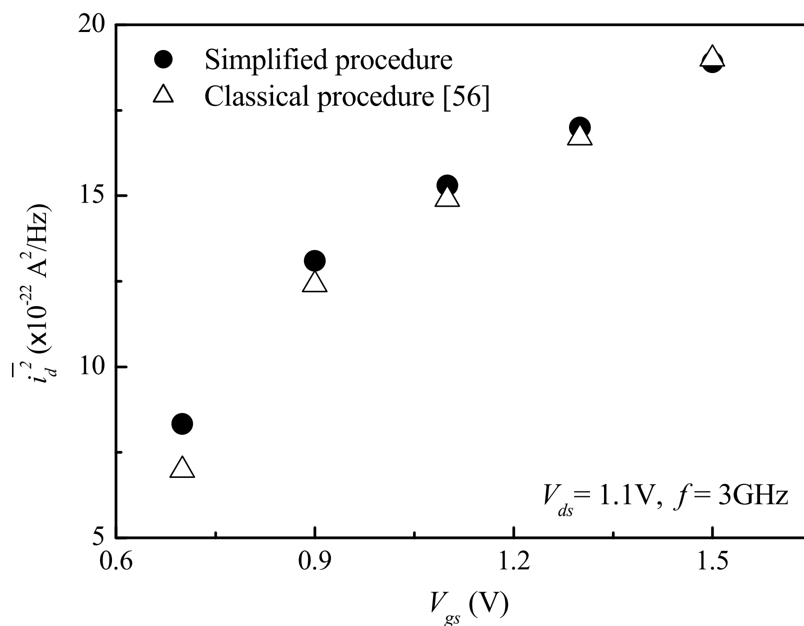

Figure 5.5 Drain curent thermal noise versus V_{gs} at V_{ds} = 1.1 V and f =3 GHz

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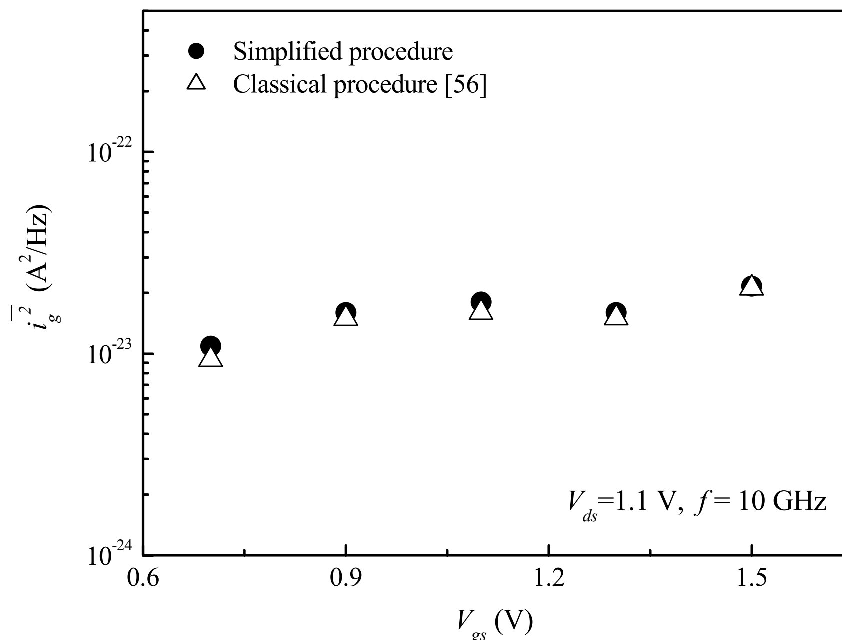

Figure 5.6 Induced gate noise versus V_{gs} at V_{ds} = 1.1 V and f =10 GHz

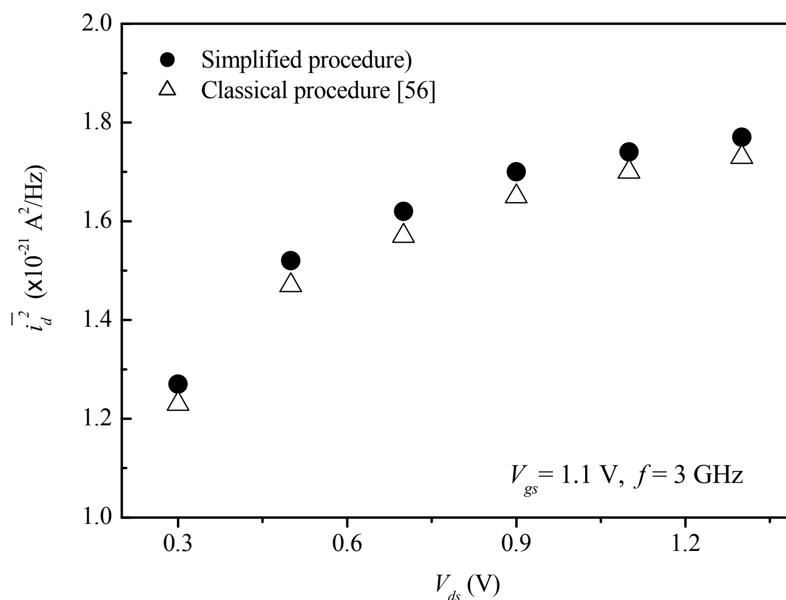

Figure 5.7 Drain current thermal noise versus V_{ds} at V_{gs} = 1.1 V and f =3 GHz

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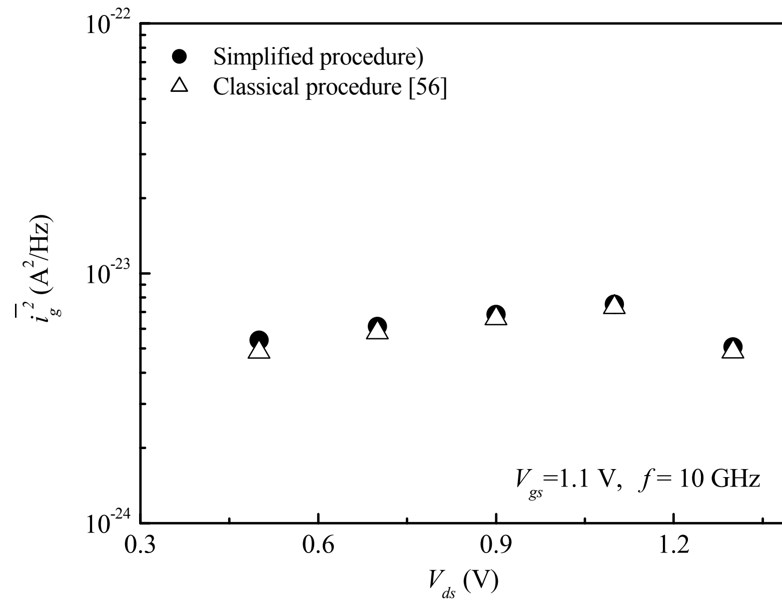

Figure 5.8 Induced gate noise versus V_{ds} at V_{gs} = 1.1 V and f =10 GHz

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Chapter 6 Effect of FN stress and gate oxide breakdown on high frequency noise

5.1 Introduction

Scaling of MOSFETs towards deep-sub micrometer region significantly enhances the device high frequency performance, making the MOS technology an attractive alternative for RFIC applications. Recently, degradation of deep submicron MOSFETs performance by hot carrier stress or oxide breakdown has been studied from an RF or microwave perspective. It has been found that the degradation of device RF performance could be induced by hot-carrier stress and gate oxide breakdown [59, 60, 61].

On the other hand, with the continued downwards scaling of MOS technology, reduction of gate oxide thickness for deep submicron MOSFETs may subsequently weaken the intrinsic oxide reliability, which limits the further scaling of oxide thickness. Considering the great potential of deep submicron NMOSFETs for low power and low noise RF or microwave applications, a study on the effect of oxide breakdown on microwave noise performance for MOSFETs is necessary. However, comprehensive understanding of the impact of oxide breakdown on the microwave noise in sub-quarter micrometer MOSFETs is still lacking [61, 62]. In this chapter, the effect of gate oxide breakdown on the microwave noise performance of NMOSFETs is investigated.

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5.2 Experiments

A constant stress voltage was applied to the gate with the source, drain and substrate connected to ground. All the devices were stressed at positive gate voltage. Electrons are injected in the oxide from either the source and drain extension region underneath the gate, or from the transistor inversion layer. The positive voltage stress is selected because this condition is typical for a NMOSFETs operation in a RF circuit. Different stress voltages (4 to 5.3 V) with different current limits in the range of 200 nA to 2 μA were used to introduce gate oxide breakdown events with different breakdown hardness and leakage levels [63]. The higher gate voltage is carefully chosen for an accelerated stress [106].

5.3 Results and Discussions

Figure 5.1 shows gate current measured during sequential 4.75 V constant voltage stress. The device *I-V* characteristics and RF noise before oxide breakdown were measured at predetermined interruption time. The stress was also stopped when a large variation in gate current was detected to avoid catastrophic breakdown and functional failures. Soft breakdown (SBD) occurred after about 1300 second-stress. The spikes seen in the pre-breakdown trace named as A to D are due to the interruptions during the stress. Figure 5.2 compares the gate leakage at different stress interruptions. Notice that, for high stress voltage, the current limit was not able to sufficiently protect the device

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due to overshoot [64]. For example, gate leakage measured at the second SBD interruption (SBD2) is around 4.5 μA at V_g=3 V which far beyond the current limit of 250 nA. Stressing the device further with an increased current limit of 2 μA then results in a hard breakdown (HBD) at ~1600 s. Again, high post breakdown current indicates the overshoot occurred during HBD. In

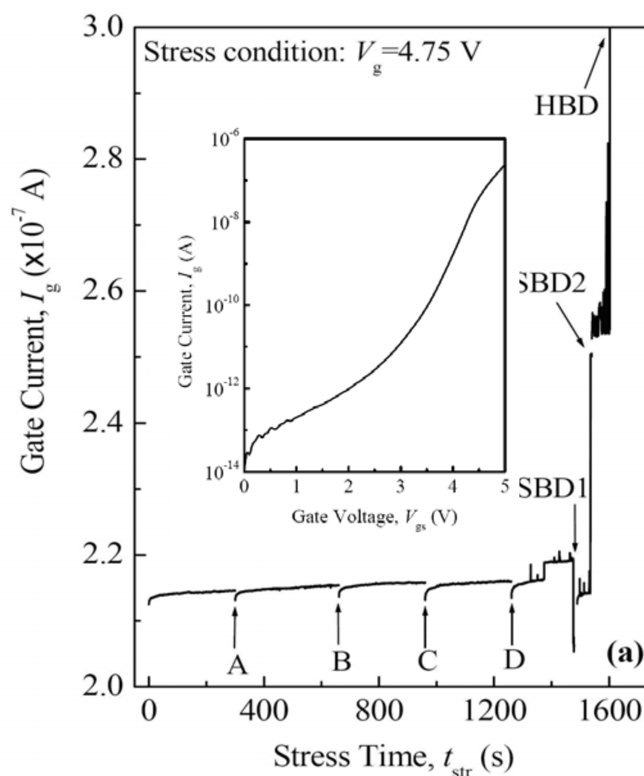

Figure 6.1 Gate current as a function of stress time. The spikes shown in the pre-breakdown trace named as A to D are due to the interruptions during the stress, and SBD1, SBD2 and HBD are corresponding to the sequential soft and hard breakdowns in the device.

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general, lower stress voltage results in less overshoot. Threshold voltage (V_{th}), transconductors (g_{m}) and drain saturation current ($I_{\text{d,sat}}$) were measured at different stages during the stress. The three parameters were tested when the device is operated at saturation region where channel current is much higher than the gate leakage current even after the breakdown. Although continuous drifts of these three typical device DC parameters were seen during the stress, both SBD and HBD events do not induce any drastic changes on the aforementioned parameters as illustrated in Figure 5.3. The oxide BD occurred in the gate-source region appears benign in the off-current characteristics. However, for the device with BD location close to drain, a much higher off-current was observed. This is similar to the previous study [65]. For both cases, no severe degradation of the DC parameters at saturation region was found due to the breakdown events.

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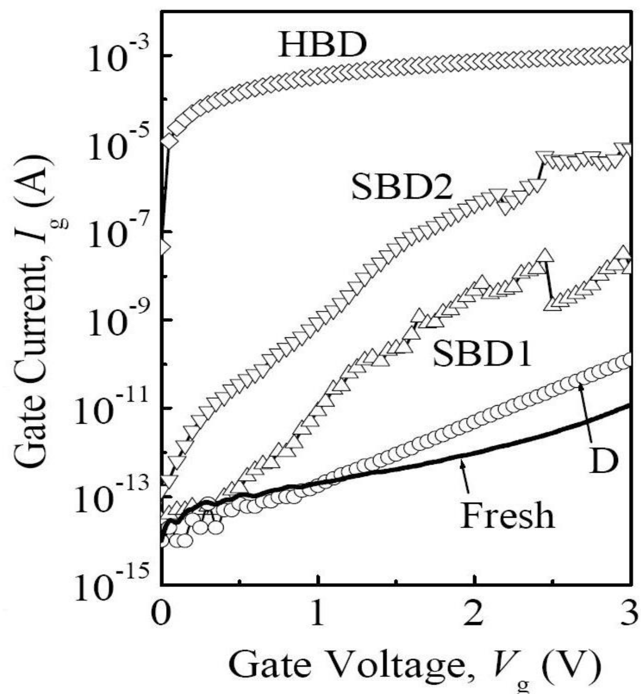

Figure 6.2 Gate leakage measured at different stress interruptions.

Even if the gate oxide breakdown at the prescribed gate leakage levels does not produce a significant change on the device DC characteristics, the RF performance degradation is more significant than DC performance degradation. Figure 5.4 shows the measured *S*-parameters before and after hard breakdown. The *S*-parameters have been measured at V_{gs}=0.9V and V_{ds}=1.1V.

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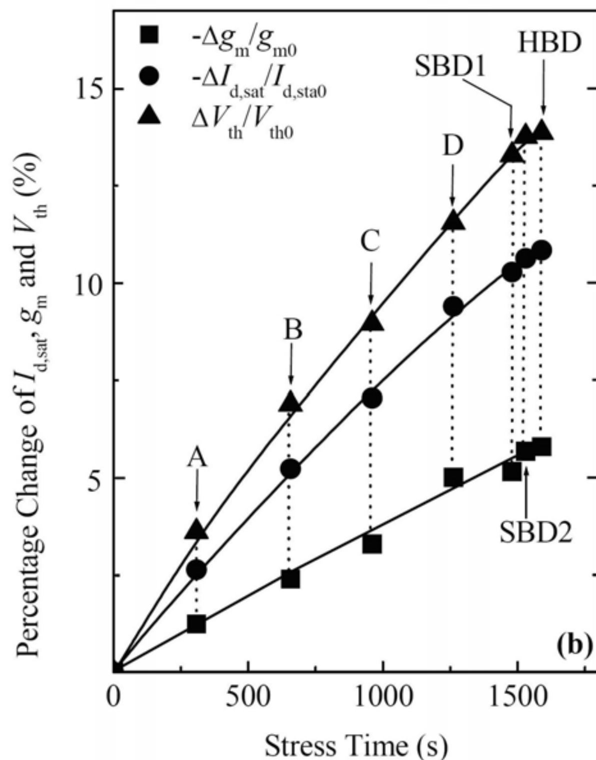

Figure 6.3 Fractional degradation of the saturation drain current ($\Delta I_{\mathrm{d,sat}} / I_{\mathrm{d0,sat}}$), transconductance ($\Delta g_{\mathrm{m}} / g_{m0}$), and threshold voltage ($\Delta V_{th} / V_{th0}$) as a function of stress time. No drastic changes are induced by the oxide breakdown events.

The degradation of S_{21} and S_{22} can be explained by the decrease of g_m and the increase of R_{ds} which results in the change of reflected parameters at output port. The degradation of S_{11} can be due to the change of effective channel resistance R_{i}. Some of the parameters of the small-signal equivalent circuits are shown in Table 5.1.

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Table 6.1 Element values extracted for an operation point in saturation (V_{gs}=0.9V, V_{ds}=1.1V)

Element	Value (Before Stress)	Element (After Stress)
R_g	3.47 Ω	3.47 Ω
R_{ds}	588.6 Ω	644.7 Ω
g_m	42 *mS*	34.5 *mS*
R_i	0.88 Ω	9.67 Ω
R_d	2.55 Ω	1.57 Ω
R_s	2.64 Ω	1 Ω
C_{db}	60.2 fF	63.4 fF
R_{db}	14.6 Ω	9.33 Ω
C_{gs}	21.3 fF	54.6 fF
C_{dg}	51.6 fF	47.4 fF

The degradation of the cut-off frequency (f_T) and maximum frequency (f_{max}) are shown in Figure 5.5. f_T and f_{max} have been defined as the frequency where the current gain is 0 dB and the frequency where the maximum available gain (MAG) is 0 dB, respectively. The cut off frequency (f_T) of the device presents a marginal degradation of up to 15 %. For example, f_T is reduced from 45 GHz to 42 GHz at V_g=0.9 V and V_d=1.1.

Generally, f_T and f_{max} for FET can be expressed as follows:

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \quad (5.1)$$

$$f_{max} = \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + g_{ds} R_{in}}} \quad (5.2)$$

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where C_{gd} and C_{gs} are gate to drain and the gate to source capacitance; g_{ds} is output conductance; R_g is gate resistance; R_{in} is input resistance consisting of gate, source, and channel components.

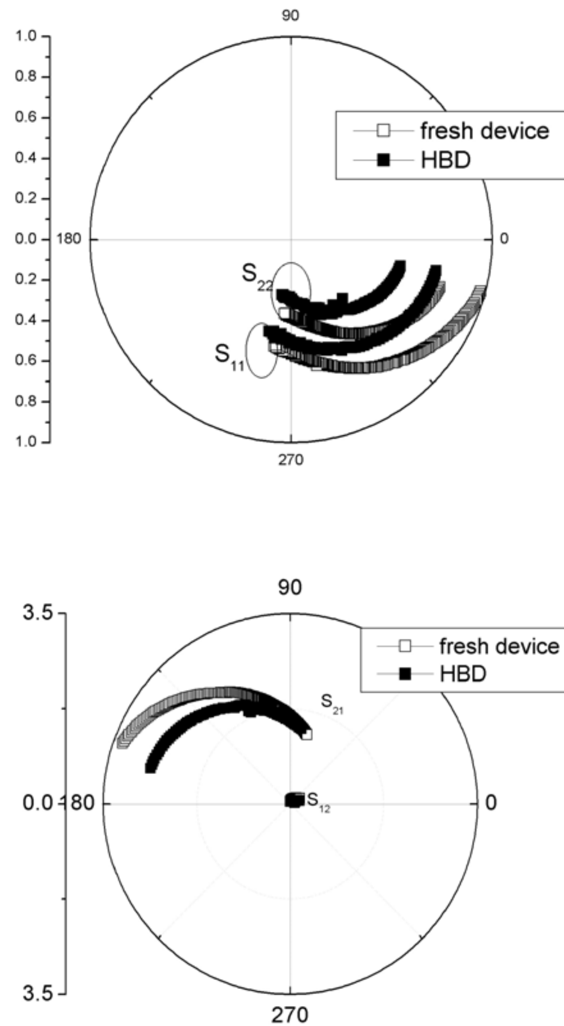

Figure 6.4 Measured S-parameters before and after stress

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As can be seen in Equations (5.1) and (5.2), f_T and f_{max} will be decreased due to the decrease of transconductance after stressing. Since g_m, C_{gd} and g_{ds} are degraded due to the interface state generation after stress, RF performances should be degraded due to the same degradation mechanism [66].

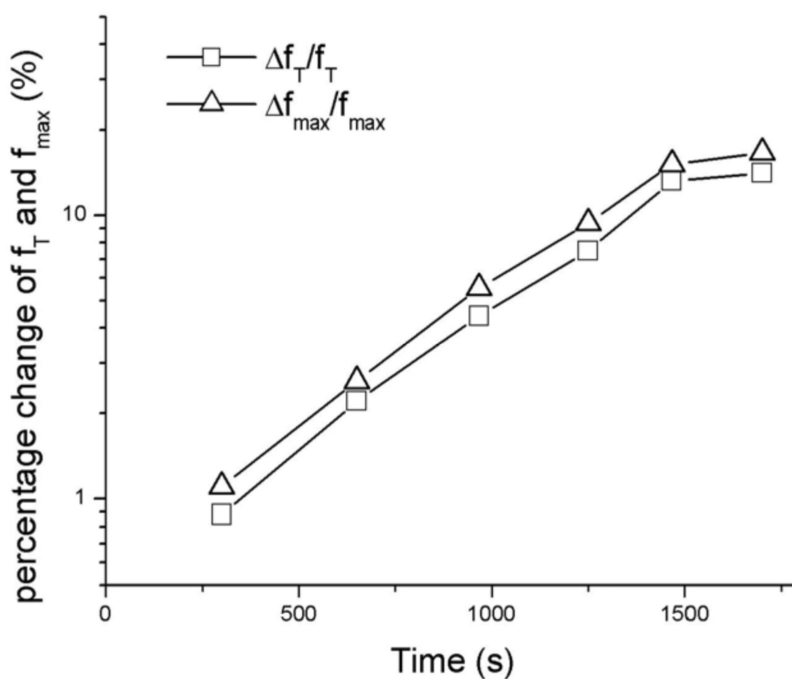

Figure 6.5 Degradation of the cut-off frequency ($\Delta f_T / f_T$) and maximum frequency ($\Delta f_{\max} / f_{\max}$) as a function of stress time

Similarly, a large deterioration of RF noise characteristics has been observed. Figure 5.6 compares the de-embedded minimum noise figures ($NF_{\min}$) of the 0.18 μm n-MOSFET as a function of frequency measured at different

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stress stages. For the sake of clarity, the data measured at interruptions A to C are not plotted. The parasitic pad effects were directly de-embedded from the measured noise parameters following the method proposed by Deen *et al* [67]. The fresh device exhibits typical frequency dependence for NF_{min} – increase of NF_{min} with the increase of frequency, which is similar to the observations reported on different generations of MOSFET [68, 69]. The NF_{min} measured at V_{g}=V_{d}=1 V for the frequency of 2 GHz is around 0.3 dB and is increased to 1.8 dB when the frequency reaches 18 GHz. In contrast, a drastic increase in NF_{min} with a significant difference in its frequency dependence was measured from the device after oxide breakdown. NF_{min} of 4.75 dB and 3.6 dB were measured at frequencies of 2 GHz and 18 GHz, respectively. A downwards trend for the frequency dependence of NF_{min} which is different from the one for the fresh device is presented suggesting possible different noise mechanism in the post-breakdown device. Although the ~10% variations on DC (e.g. V_{th}, g_{m} and $I_{\mathrm{D,SAT}}$, etc.) and microwave parameters (f_{T} and f_{max} etc.) may not significant affect circuit function if a large enough margin of circuit design is provided, such drastic increase in NF_{min} could suspend any useful applications of the device for low noise circuits. Another important feature revealed by Figure 5.6 is that no significant increase in NF_{min} is occurred during FN stress and sequential SBDs. In other words, the interface and oxide defects build-up may not have great impact on NF_{min}. This observation seems to be in direct contradiction with the

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report by Pantisano *et al*.[70], but favorable to pure thermal noise model such as the one by Scholten *et al* [71].

Figure 5.7 and 5.8 compare the de-embedded minimum noise figures (NF_{min}) and noise resistance (R_n) of the 0.18 μm n- MOSFET versus frequency as a function of gate bias voltage measured before and after gate oxide breakdown. Increase of gate bias results in a slight increase of the NF_{min}. After oxide breakdown, the NF_{min} becomes more sensitive to gate bias. Notice that, different from NF_{min}, the trends for the frequency dependence of R_n, shown in Figure 5.8, remain no change.

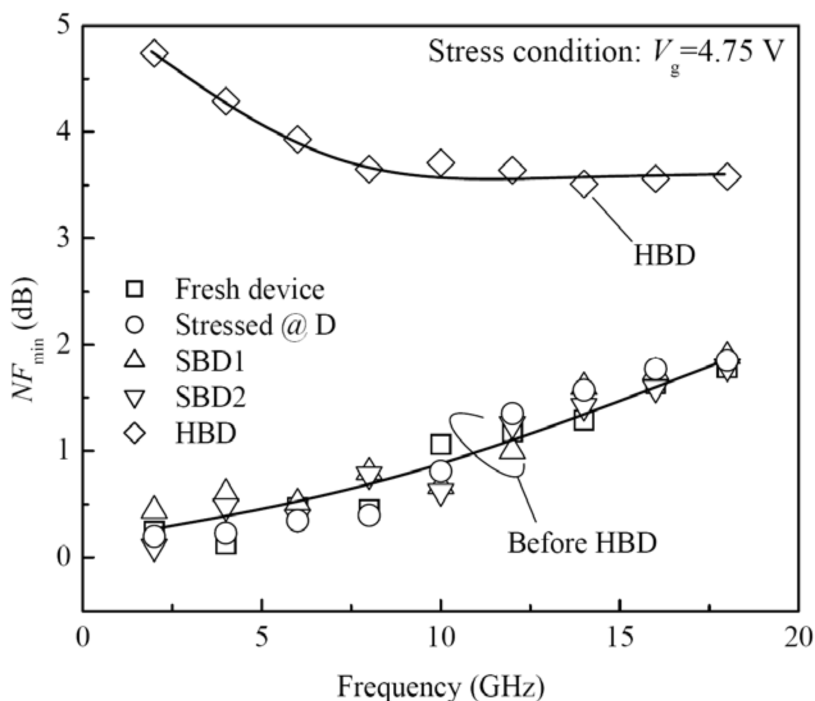

Figure 6.6 NF_{min} as a function of frequency measured during the stress.

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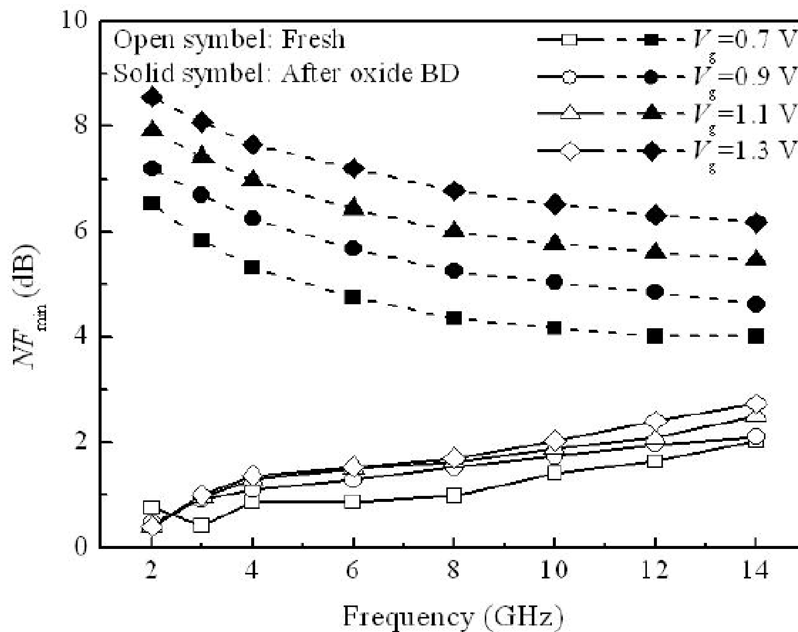

Figure 6.7 De-embedded NF_{min} of a 0.18 μm n-MOSFET versus frequency as a function gate bias voltage measured before and after gate oxide breakdown.

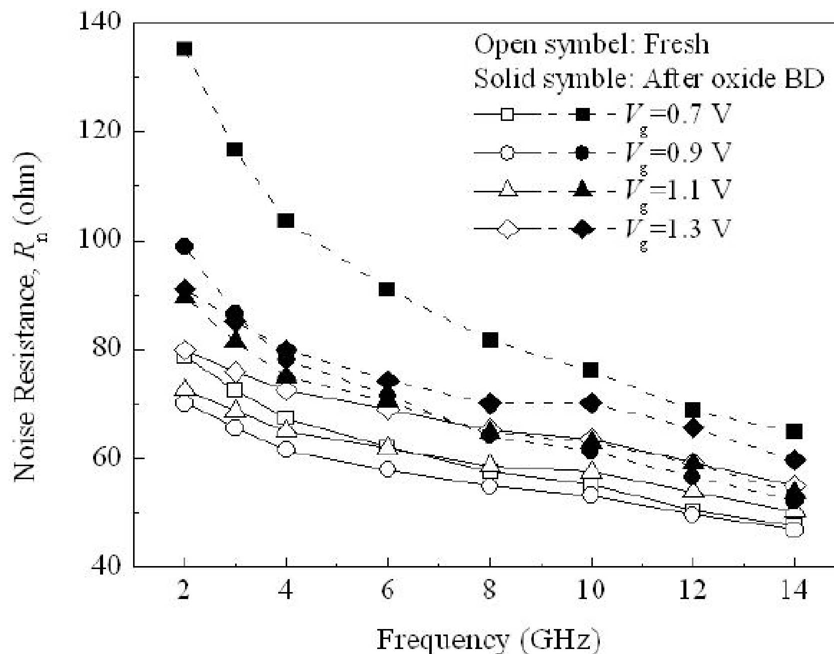

Figure 6.8 De-embedded R_n of a 0.18 μm n-MOSFET versus frequency as a function gate bias voltage measured before and after gate oxide breakdown.

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One of the possible explanations could be due to the difference in test setup between the two experiments. In reference [70], Pantisano *et al*. did not attempt to match the MOSFET input impedance with the frequency synthesizer and significant reflection occurred. Considering the well-known noise figure equation pertaining to a linear noisy two-port

$$F = F_{min} + \frac{R_n}{G_s} | Y_s - Y_{opt} |^2, \tag{5.3}$$

where $Y_s = G_s + jB_s$ is the signal source admittance, drift of optimum admittance Y_{opt} and/or R_n due to the stress without changing the F_{min} may cause the change of apparent noise F. The point can be verified by measuring the noise figures at 50 ohm impedance machining conditions (NF_{50}) instead of NF_{min} shown in Figure 5.9. The increase in NF_{50} during stress could be attributed to the possible drift of Y_{opt} and increase in R_n [see the inset of Figure 5.9]. The drastic change of NF_{min} due to HBD could be qualitatively explained using established analytical expressions considering the increased contribution from gate shot noise [72]:

$$R_n = \frac{\gamma}{\alpha g_m} \tag{5.4}$$

$$\begin{aligned} F_{min} &\approx 1 + 2R_n G_{OPT} \\ &= 1 + 2R_n \omega C_{gs} \sqrt{\delta(1 - c_G^2)\alpha^2 / (5\gamma) + 2qI_G g_m \alpha / (4kT\gamma\omega^2 C_{gs}^2)} \end{aligned} \tag{5.5}$$

where $\alpha \cong g_m / g_{d0}$, with g_{d0} being the drain conductance for V_{DS}=0. γ, δ and c_G are parameters for drain and induced gate noise. From the above equations, we can see that the R_n is dominated by the drain (channel) thermal noise and g_m,

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while the $F_{\min}$ is not only determined by R_n but also induced gate noise [term of $\delta(1-c_G^2)\alpha^2/(5\gamma)$ under the square root of in (5.5)] and gate shot noise [term of $2qI_G g_m \alpha/(4kT\gamma\omega^2 C_{gs}^2)$ under the square root of in (5.5)]. Therefore, the different post-breakdown frequency dependences between $NF_{\min}$ and R_n may indicate additional noise contribution from the gate terminal such as a significant increase in gate shot noise, which would largely affect the $F_{\min}$ with limited impact on R_n.

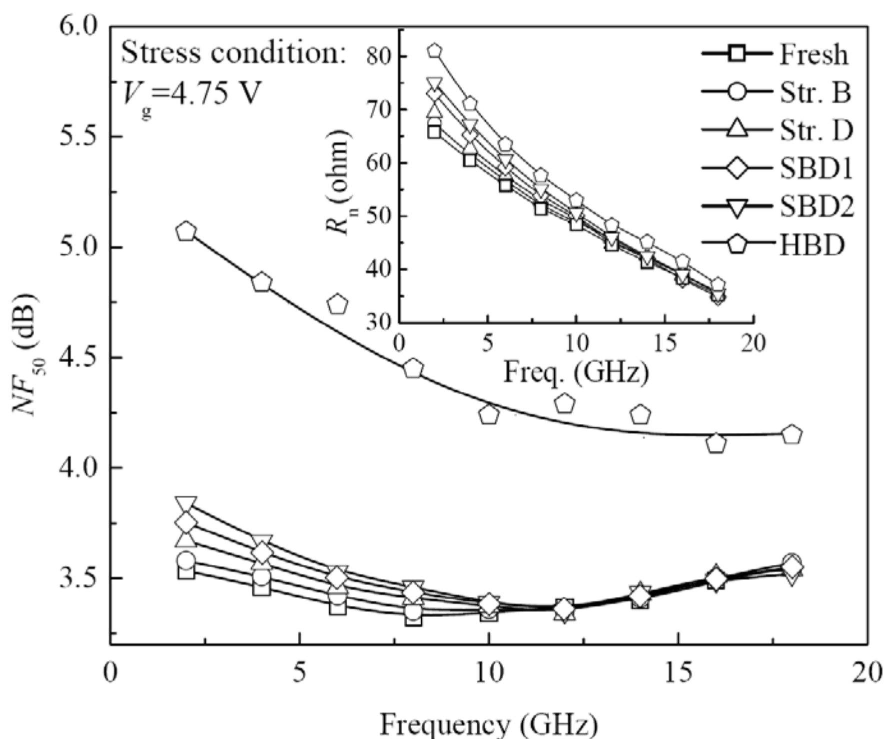

Figure 6.9 NF_{50} as a function of frequency measured at different stress interruptions. Inset: comparison of noise resistance (R_n) measured at different stress interruptions including HBD.

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To gain a better insight on the degradation of device microwave noise characteristics, the experimental results were modeled by using the approach given in [73]. The drain (channel) thermal noise $\overline{i_d^2}$ and gate noise $\overline{i_g^2}$ for the device stressed at different stages are extracted and shown in Figure 5.10. It can be seen that the channel noise, in general, is frequency independent and almost unaffected by the stress and breakdown. However, by introducing an oxide breakdown event, a drastic increase in $\overline{i_g^2}$ with change of its frequency dependence is presented. For the fresh and pre-HBD device, the extracted $\overline{i_g^2}$ roughly follows an f^2 relationship as illustrated in the figure while much weaker frequency dependence is seen after oxide breakdown. The $\overline{i_g^2} \propto f^2$ relation in the pre-HBD device can be easily explained if we assume that the gate noise in the pre-HBD device is dominated by induced gate noise $\overline{i_{g_ind}^2}$. While, the weak frequency dependence with significant increase of $\overline{i_g^2}$ in the pre-HBD devices suggests the additional contribution from gate shot noise. Its spectral density can be calculated by

$$\overline{i_{g_shot}^2} = 2qI_g \text{ (A}^2\text{/Hz)} \tag{5.6}$$

where I_g is the gate leakage current. The decrease in $\overline{i_g^2}$ with frequency in the frequency range of 2 to 4 GHz after HBD is possibly due to a flicker noise component, which is related to the charge exchange between the channel

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electrons and oxide traps in a range close to oxide silicon interface [71]. Further studies will be carried out to quantify this noise source. For the device plotted in Figure 5.10, a post-breakdown I_g of 337 μA (J_G=4.2 μA/μm, which is about 3% of channel current) measured at V_g=V_d=1 V gives a gate shot noise of 1.08×10^{-22} A^2/Hz. Plotting the calculated $\overline{i_{g_shot}^2}$ in Figure 5.10 shows that the estimated $\overline{i_{g_shot}^2}$ is fairly close to the extracted $\overline{i_g^2}$. Figure 5.11 plots the gate noise as a function of gate leakage extracted from devices with different leakage levels (breakdown hardness) and breakdown locations. A transition of the gate noise from an induced gate noise dominant region to gate shot noise dominant region can be clearly observed. In general, the gate noise is found to directly relate to the gate leakage regardless of the breakdown hardness and location. From the plot, we can see that the contribution of gate shot noise in post-breakdown device becomes non-negligible if the gate leakage is higher than ~3 μA. This value is close to the high end of oxide leakage in a device with SBD (Typical leakage in SBD oxide is in the range of 10 nA to 1 μA.). Considering the further reduction of the induced gate noise in advanced device generations [74], shot noise induced by gate oxide breakdown (even a SBD) in further scaled devices should be carefully monitored.

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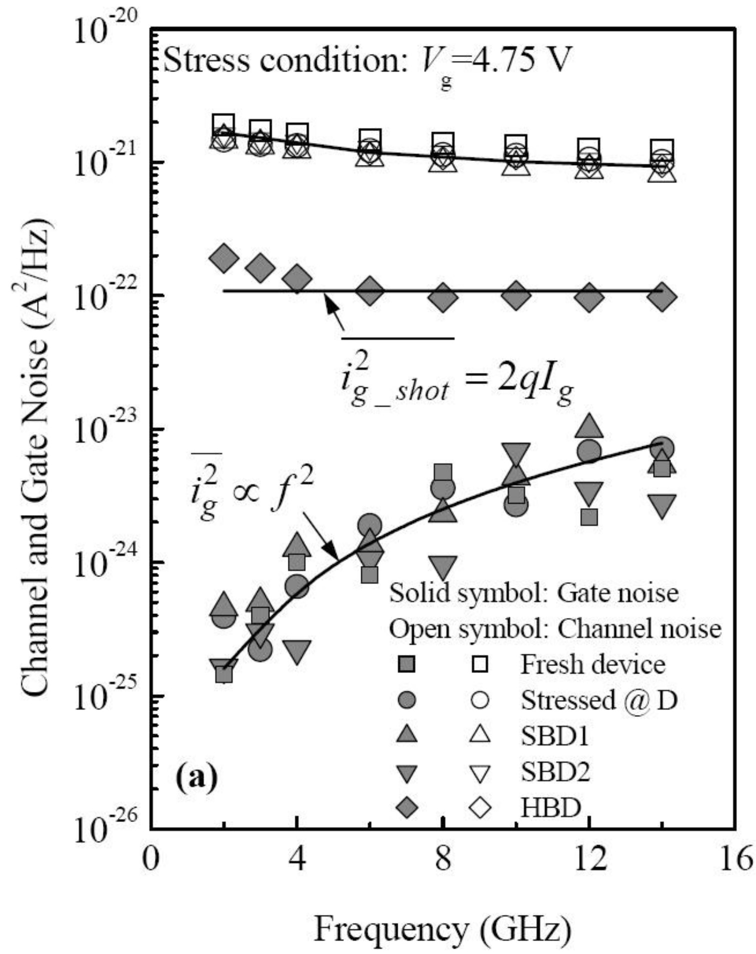

Figure 6.10 Extracted drain (channel) thermal noise $\overline{i^2_d}$ and gate noise $\overline{i^2_g}$ for an NMOSFET at different stress stages.

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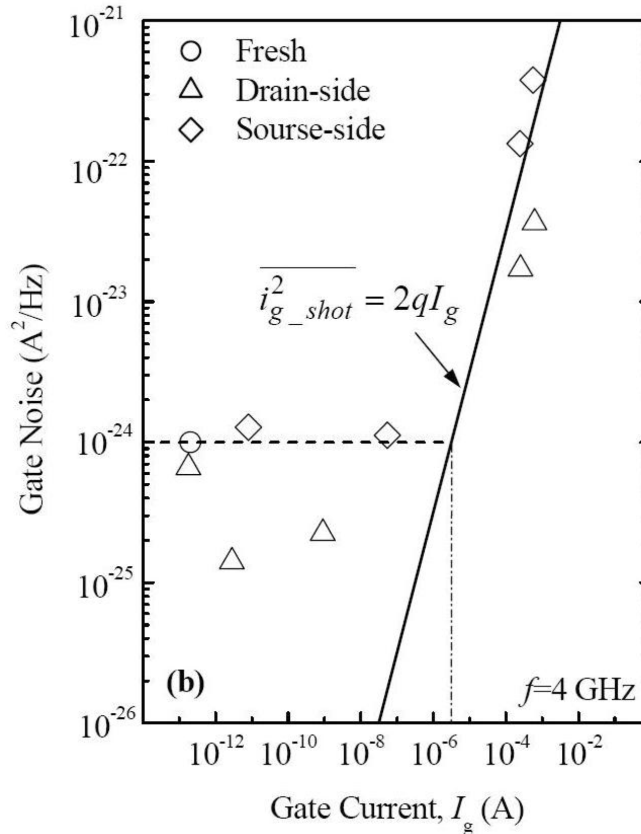

Figure 6.11 Gate noise versus gate leakage extracted from devices with different leakage levels (breakdown hardness) and breakdown locations. The stress voltage V_g is in the range of 4 to 5.3 V. The gate shot noise $\overline{i_{g_shot}^2} = 2qI_g$ is plotted in the figure for reference.

5.4 Summary

The effect of FN stress and oxide breakdown on high-frequency noise performance for NMOSFETs has been comprehensively studied. The degradation of the typical noise parameters in a 0.18 μm NMOSFET such as noise figure, equivalent noise resistance induced by oxide breakdown are characterized in the frequency range of 2 to 14 GHz. DC and RF characteristics

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of the devices at different leakage levels and breakdown hardness are compared. Even if the gate oxide breakdown at different gate leakage levels does not produce a significant change on the device DC characteristics, the RF and noise performances can be deteriorated. A serious degradation of microwave noise parameters with more than 5 dB increment of NFmin at 2 GHz has been observed. The results have shown a strong dependence of degradation of noise parameter on the gate leakage.

The degradation mechanisms are investigated by the parameter extraction using a noise equivalent circuit model. It has been found that the drastic increase of device high frequency noise after gate oxide breakdown can be attributed to the significant increase in the contribution of gate shot noise, which is believed to be negligible in as-processed 0.18 μm NMOSFETs. Considering the great impact of oxide leakage on the RF MOSFETs, determining a gate leakage limit as a criterion for the post-breakdown oxide is necessary.

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Chapter 7 Impact of gate oxide breakdown location on high frequency noise

6.1 Introduction

Ultra thin gate-oxide reliability is an urgent issue in deep submicron silicon CMOS integrated circuit technology. It is a potential showstopper [75, 76, 77, 78] for continued downward scaling. By scaling the oxide thickness to only a few nanometres, further complications have come about as different breakdown modes, soft and hard breakdown, are observed. Recently, the relation between breakdown location and circuit failure has attracted some attention. A method was introduced to determine the position of the breakdown in short-channel transistors and demonstrated the relation between the breakdown mode (soft/hard) and the location of the breakdown [79]. It was found that the breakdown near the source/drain-to-gate overlap region causes more server degradation of DC characteristics [80].

On the other hand, the improved high frequency performance of deep submicron MOSFETs in conjunction with the capability of very large scale integration (VLSI) provides a great opportunity to use Si MOSFET for low noise radio frequency integrated circuits (RFICs) or microwave monolithic integrated circuits (MMICs). The effect of FN stress and oxide breakdown on high-frequency noise performance for NMOSFETs has been studied in [81, 82]. The relationship between the device noise parameters (such as NF_{min} and R_n,

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etc.) and different noise spectral densities, contributed from different noise sources such as channel noise, induced gate noise and gate shot noise are discussed intensively. It has been found that the drastic increase of device high frequency noise after gate oxide breakdown can be attributed to the significant increase in the contribution of gate shot noise. However, it was still unclear how hard breakdown in a sub-micron MOSFET can influence operation of low noise RF circuits and whether and along which lines a designer can reduce the impact of breakdown on device RF performance. In this chapter, the relation between the location of breakdown in deep sub-micron MOSFET and noise characteristics is discussed.

6.2 Experiments

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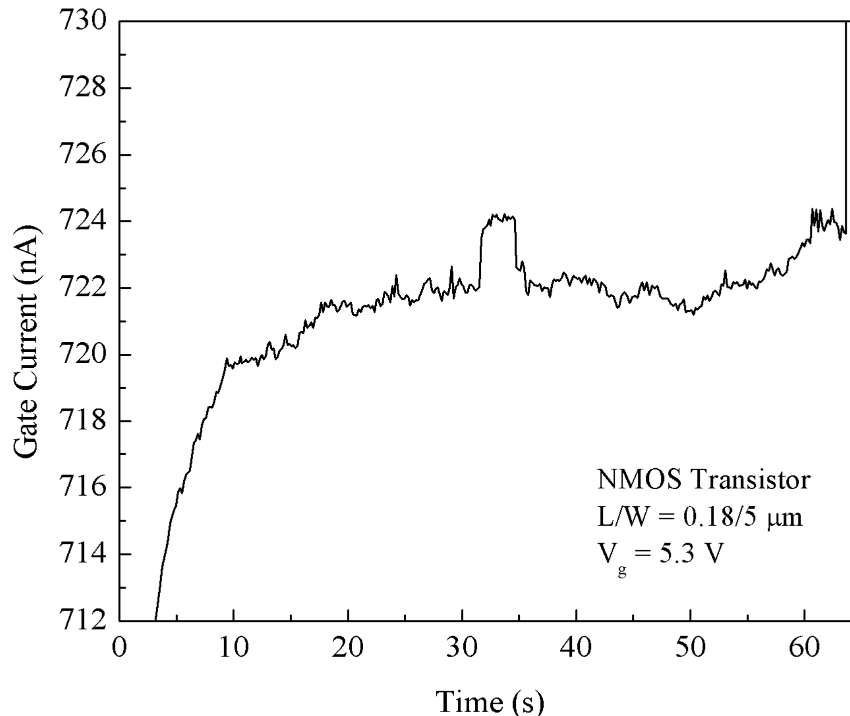

Figure 7.1 Example of gate current versus time for a 5.3-V stress.

A constant positive stress voltage was applied to the gate with the source, drain and substrate connected to ground. It can be demonstrated that the entire oxide area is stressed uniformly [83].The stress was stopped immediately after first breakdown occurred to avoid further damage generation in the oxide. Breakdown was detected by the first significant increase of the gate current noise. Basically, the breakdown detection concept elaborated in detail in [83] was followed. Consequently, random telegraph signal (RTS)-like features that occur abundantly during the stressing, are not considered as breakdowns. These pre-breakdown events are typical in very small area devices. An example of a

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typical gate-current versus time curve recorded on one of the small transistors is presented in Figure 6.1. After breakdown, the currents at the gate terminal I_g, source terminal I_s, drain I_d and substrate I_{sub} were measured in the range of V_g = -1.5 to 1.5 V and $V_s = V_d$ = 0. This limited measurement range is to avoid generation of additional damage in the FET or alteration of the physical nature of the created breakdown.

6.3 Dependence of DC and RF noise performance on breakdown

It has been demonstrated that breakdowns can be classified as close to the source or drain region or in the channel region by observing the source or drain current at negative gate bias. Depending on whether the current path after breakdown is from gate to source or from gate to drain, one can distinguish between a source-to-gate and drain-to-gate breakdown, respectively. Degraeve *et al.* introduced a simple methodology to locate a nanometer-precision breakdown spot along the channel length. It was shown that the probability of finding a breakdown in any interval dx along the channel is constant. He calculated the percentage of drain leakage current in the total leakage current Id/(Id+Is) at negative Vg and Vs=Vd=0V. also found that both breakdowns that occurred over the source and drain extension regions destroyed device functionality [79, 80]. It was shown that hard breakdown and catastrophic device failure occurred more frequently as the channel length of the device was decreased. This was explained as a result of the source and drain regions

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dominating more of the channel area as the channel length is decreased, increasing the probability of a breakdown occurring the source and drain. However, studies by Linder [84] and Kaczer [85] showed that short channel MOSFETs would probably survive and circuits continue to function.

All of the above conclusions are derived mainly from the observations of device DC functionality and digital circuit performance. In [82], DC characteristics of devices which are stressed until breakdown at different regions of the device are measured. It has been found that both soft breakdown and hard breakdown events do not induce any drastic changes on the important DC parameters such as threshold voltage (V_{th}), transconductance (g_m) and drain saturation current ($I_{d,sat}$). However, drastic increase of device high frequency noise after gate oxide breakdown is observed. It is illuminated that the RF performance of a stressed device may be not in accordance with the DC characteristics. In this section, the DC and RF noise performance of a device after drain/source-to-gate breakdown are compared and analyzed.

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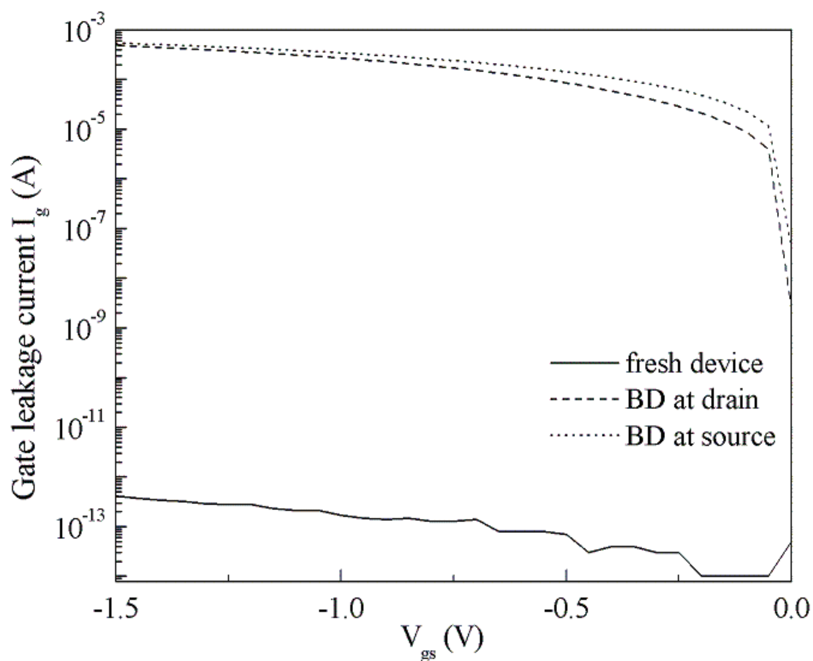

Figure 7.2 Typical leakage current at gate for fresh and post-breakdown devices. Gate-to-drain/source breakdowns shown in the figures

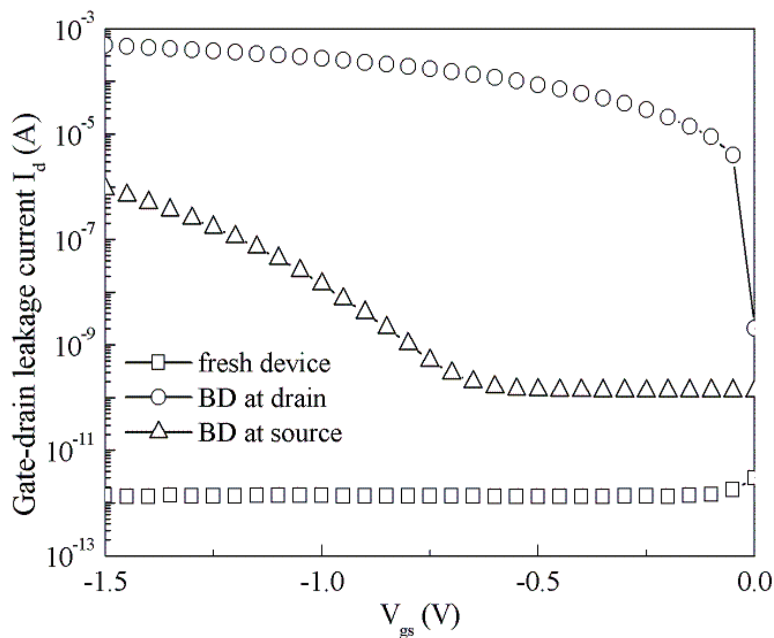

Figure 7.3 Typical leakage current at drain for fresh and post-breakdown devices

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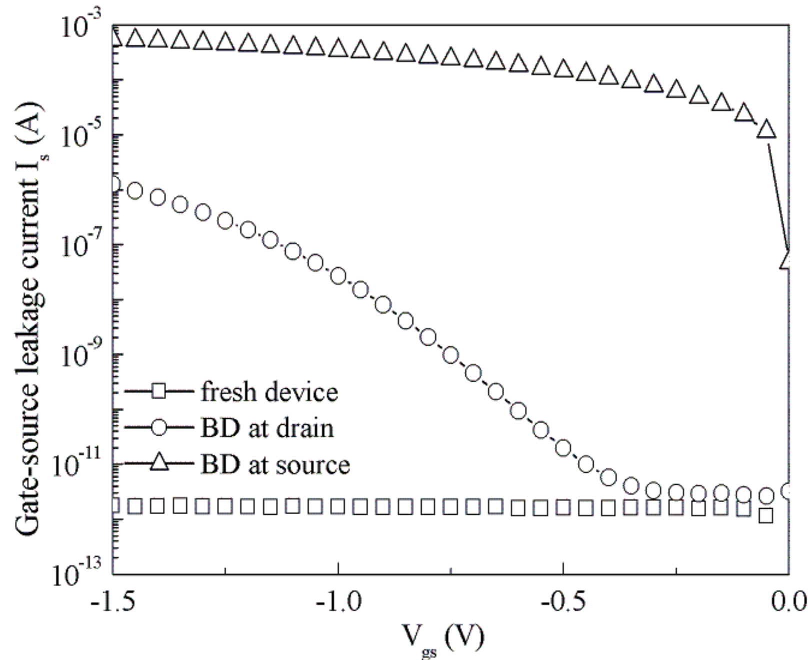

Figure 7.4 Typical leakage current at source for fresh and post-breakdown devices

Figure 6.2 to 6.4 show typical current curves at drain, source and gate terminals for fresh and stressed devices with V_d=V_s=V_b=0V. Only current versus negative gate voltage was presented here since the breakdown location has little influence of current at positive gate voltages. For device shown in Figure 6.2 to 6.4, the location of breakdown is determined by using the charge separation measurement technique. The oxide breakdown occurred in the gate-source region appears benign in the off-current characteristics. However, for the device with breakdown location close to drain, a much high off-current was observed. The gate leakage current in these two cases are almost the same and therefore cannot show difference for the two stressed devices. Other important DC

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parameters also are measured for both devices, fresh and post-breakdown. No severe degradation of the DC parameters at saturation region was found due to the breakdown events. It shows that the two devices have same performance after stress from point view of DC. Devices with similar post breakdown gate leakage were selected to ensure similar degree of oxide breakdown. Consistent with the previous report [86], measurements of device transfer characteristics indicate that the oxide BD occurred in the gate-source region appears benign in the off-current characteristics. However, for the device with BD location close to drain, a much high off-current was observed. Except the off-current, no severe difference of the DC parameters at saturation region was found between the devices with source and drain side breakdown.

RF noise parameters are measured at V_g = V_d = I V (bias condition to provide lowest NF_{min} for the given devices) for fresh devices and devices after oxide breakdown. Figure 6.5 compares the de-embedded minimum noise figures (NF_{min}) of the 0.18 μm n-MOSFET as a function of frequency. The fresh device exhibits typical frequency dependence for NF_{min}. In contrast, drastic increase in NF_{min} was measured from the device after oxide breakdown. NF_{min} of 2.5 dB and 3 dB were measured at frequencies of 2 and 18 GHz for the device with oxide breakdown at drain side, while even high NF_{min} of 4.8 dB at 2GHz and 3.5 dB at 18 GHz were obtained from the device where breakdown occurs at source side. However, a significant difference in its frequency dependence for breakdown close to drain or source region can be observed. The noise figure for device with drain-to-gate breakdown can approximately follow

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the trend that noise figure increases with increased frequency although at low frequencies, the curve is a little flat. But when the breakdown occurred over source region, the trend has been inversely proportional to frequency with a much higher value than that over drain. This shows that breakdown at source side in a common-source construction may be more catastrophic than at drain side.

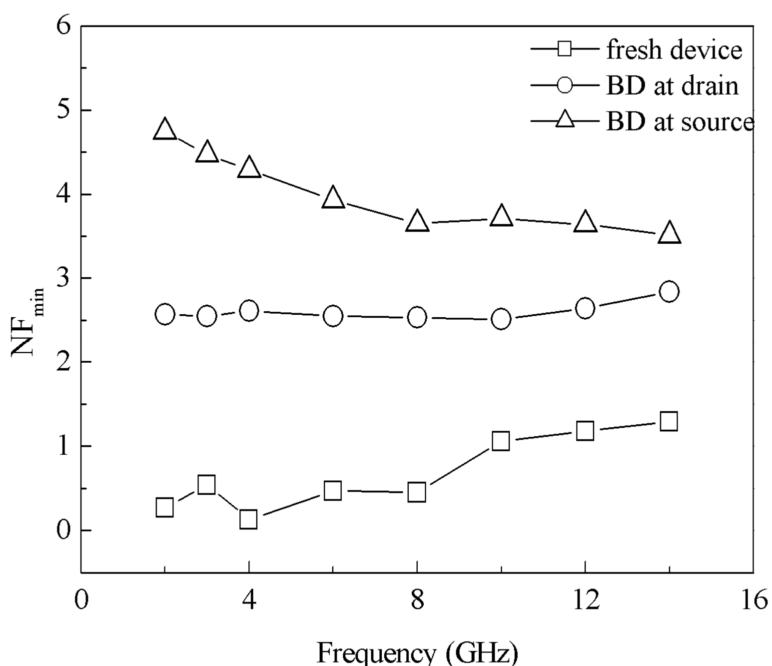

Figure 7.5 De-embedded minimum noise figures ($NF_{\min}$) as a function of frequency for fresh device and after drain/source breakdown with $V_g = V_d = 1$V

Other parameters, equivalent noise resistance (R_n) and optimum reflection coefficient Γ_{opt} at minimal noise figure, are shown in Figures 6.6 – 6.9. The drain side breakdown almost has no influence on the phase of optimum

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reflection coefficient and noise resistance while source side breakdown causes drift of phase of Γ_{opt}. The percentage of the change of phase of Γ_{opt} is shown in Figure 6.8. The magnitude of optimum reflection coefficient has been changed much after breakdown, which is shown in Figure 6.9. Considering the well-known noise-figure equation pertaining to a linear noisy two-port, which is rewritten here,

$$F = F_{\min} + \frac{R_n}{G_s} | Y_s - Y_{opt} |^2 , \tag{6.1}$$

where $Y_s = G_s + jB_s$ is the signal source admittance and the optimum admittance Y_{opt} is correlated to Γ_{opt} through $\Gamma_{opt} = \frac{1 - Y_{opt} Z_0}{1 + Y_{opt} Z_0}$. Since device will not operate at optimum reflection coefficient after breakdown, the second item of Equation (6.1) becomes important at other input impedance where $Y_s \neq Y_{opt}$. The more the magnitude of optimum reflection coefficient is changed from fresh device, the bigger the second item at the right hand of the above formula. This definitely causes a much higher noise level of the device. This further confirms that the source side breakdown is much worse than the drain side breakdown.

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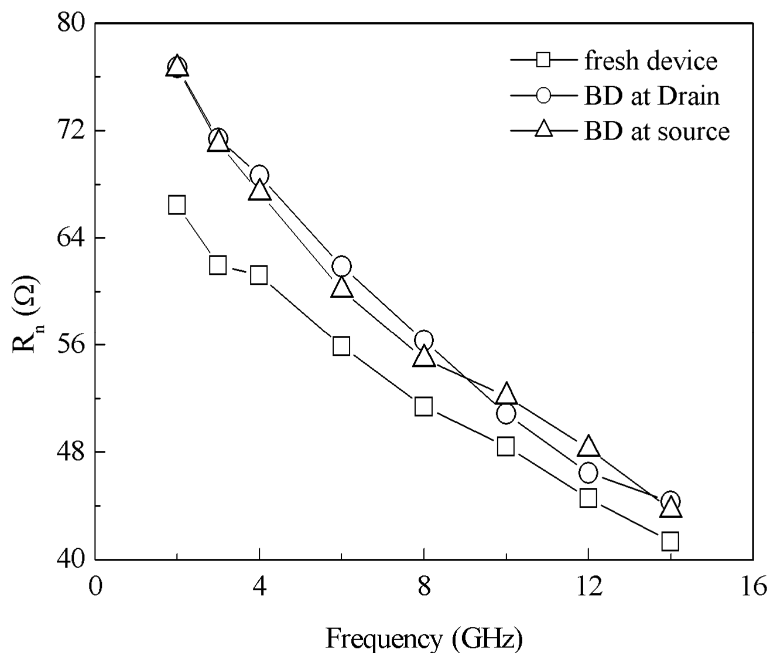

Figure 7.6 Noise resistance R_n as a function of frequency for fresh device and after drain/source breakdown with $V_g = V_d = 1$V

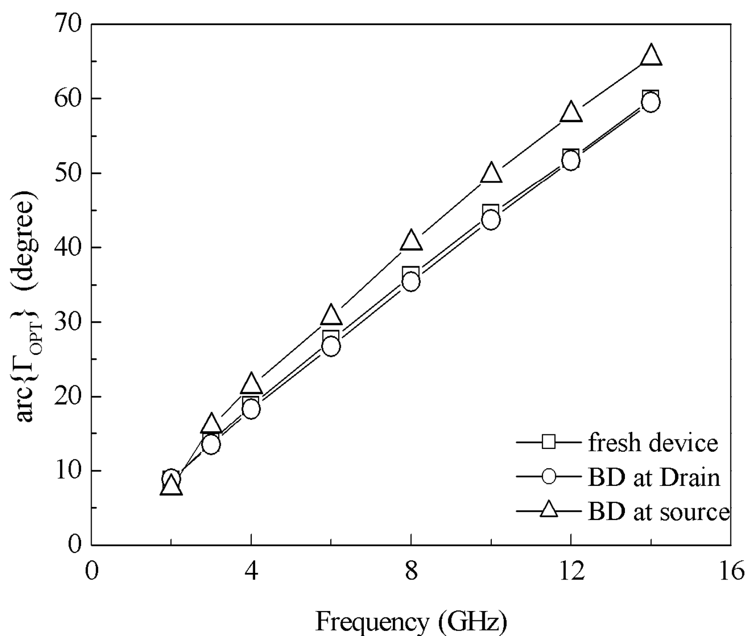

Figure 7.7 Phase of optimum reflection coefficient Γ_{opt} as a function of frequency for fresh device and after drain/source breakdown with $V_g = V_d = 1$V

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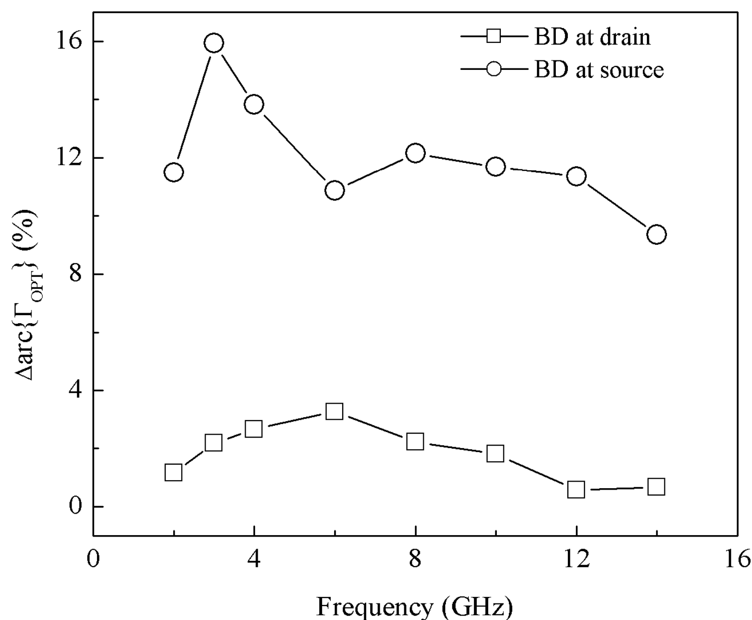

Figure 7.8 Percentage of change of phase of Γ_{opt} as a function of frequency before and after device breakdown at source and drain side

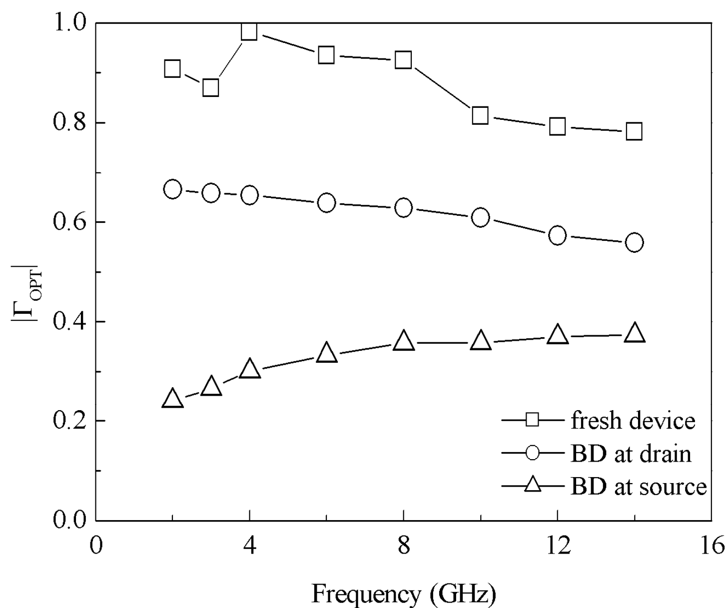

Figure 7.9 Magnitude of optimum reflection coefficient Γ_{opt} as a function of frequency for fresh device and after drain/source breakdown with $V_g = V_d = 1$V

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6.4 Results and discussions

To gain a better insight on the degradation of device microwave noise characteristics, the experimental results were modeled by using the approach given in [108,109]. Figure 6.10 shows the small-signal equivalent circuit for a grounded substrate MOSFET operating in saturation region with added resistors (r_{gs} and r_{gd}). These two incremental resistors r_{gs} and r_{gd} are used to model the gate leakage currents. The simulation results of the model show that little variation of other circuit elements after device breakdown wherever the breakdown location is, except the significant decrease of resistances r_{gs} and r_{gd}. The drain (channel) thermal noise $\overline{i_d^2}$ and gate noise $\overline{i_g^2}$ for the device stressed at different breakdown locations are extracted and shown in Figure 6.11. It can be seen that the channel noise, in general, is frequency independent and almost unaffected by the stress and breakdown. However, by introducing an oxide breakdown event, a drastic increase in $\overline{i_g^2}$ with change of its frequency dependence is presented. For the fresh and pre-HBD device, the extracted $\overline{i_g^2}$ roughly follows an f^2 relationship as illustrated in the figure while much weaker frequency dependence is seen after oxide breakdown. As shown in Chapter 5, the drastic increase of device high frequency noise after gate oxide breakdown can be attributed to the significant increase in the contribution of gate shot noise, which is believed to be negligible in as-processed 0.18 μm NMOSFETs.

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Plotting the calculated $\overline{i_{g_shot}^2}$ in Figure 6.11 shows that the estimated $\overline{i_{g_shot}^2}$ for source side breakdown is fairly close to the extracted $\overline{i_g^2}$. Since the gate shot noise for drain side breakdown is closer to the induced gate noise at high frequencies, the shot noise is less than the gate noise as shown. The small-signal equivalent circuit has shown that the circuit elements keep the same values after device breakdown. So the induced gate noise should be the same for device after breakdown. The total contribution from the shot noise calculated from Equation (5.6) and extracted induced gate noise are also drawn in Figure 6.11. It can be seen that it is very close to the extracted gate noise current. The much lower gate noise can explain why the noise performance of drain breakdown is better than the source side breakdown. The noise figure of the device after breakdown largely depends on the gate leakage current from the extracted noise currents. Although the gate leakage current during stress is the same, the leakage at operating DC bias may be different because of different breakdown location of the two devices. When gate voltage is equal to drain voltage as in the above noise measurement, gate-drain leakage current diminishes to zero. Only leakage from gate to source plays a role in the shot noise contribution. Since gate-drain leakage accounts for an overwhelming majority of gate leakage in the case of drain-to-gate breakdown, the equal voltage of drain and gate can largely diminish the practical leakage current. However, when breakdown occurs over source region, the gate-drain leakage is almost negligible comparing with gate-source leakage, the voltage potential of

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drain and gate cannot impose any influence on the noise currents. The location where the breakdown occurs, together with the total gate leakage current, determines the shot noise which dominates the gate noise of a device after breakdown.

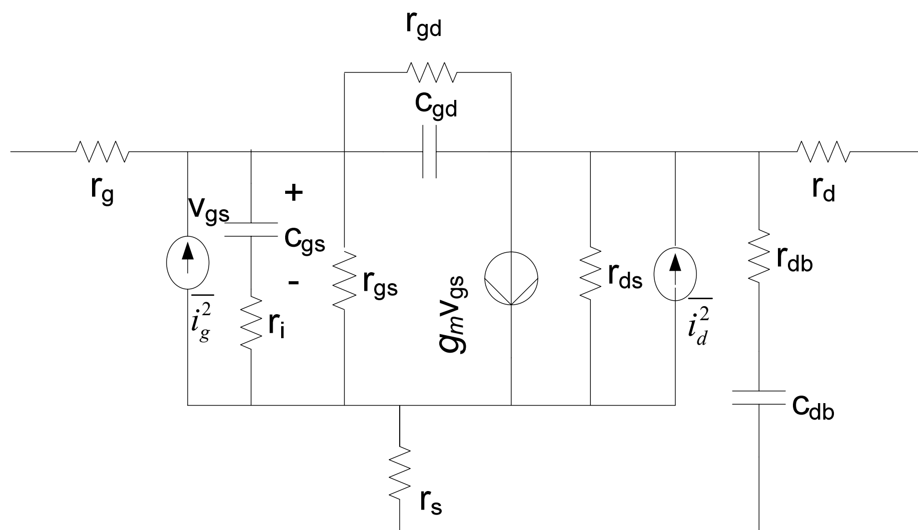

Figure 7.10 Small-signal equivalent circuit of RF MOSFET with grounded substrate. r_{gd} and r_{gs} can be considered as infinite for a fresh device.

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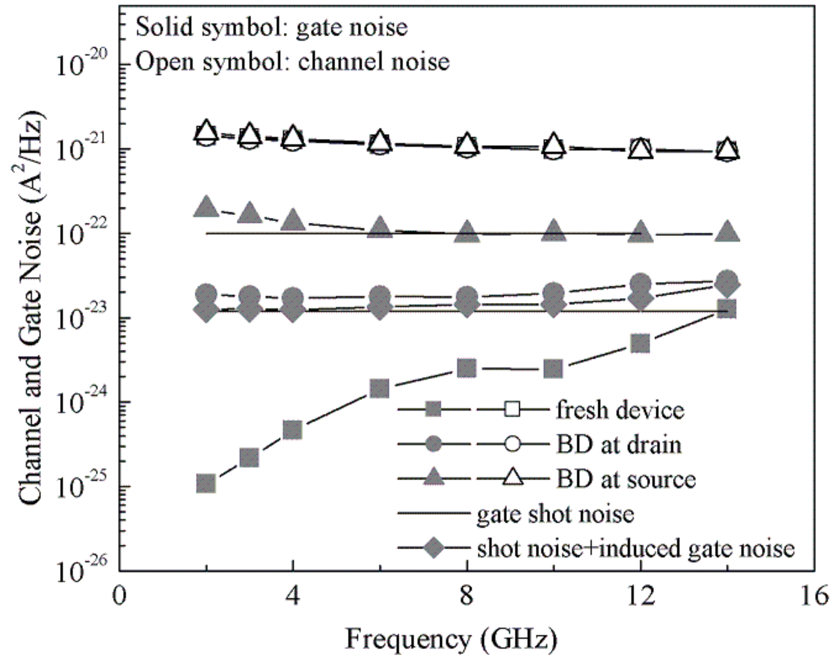

Figure 7.11 Extracted drain (channel) thermal noise $\overline{i_d^2}$ and gate noise $\overline{i_g^2}$ for the NMOSFETs with oxide breakdown at source and drain side. The gate shot noise $\overline{i_{g_shot}^2} = 2qI_g$ is plotted in the figure for reference

6.5 Design Consideration from Breakdown Location

Finally, we will illustrate how the findings might help improve the sustainability of the circuit considering the relation between RF noise performance and breakdown location. From the analysis in previous sections, the drain voltage will not have much effect on the device noise figure for source-to-gate breakdown. The impact of the breakdown on noise performance is ruinous. The noise characteristics of a device after drain-to-gate breakdown are, nevertheless, dependent on the drain voltage at which the device is biased. Figure 6.12 shows the minimum noise figure of the two devices after breakdown at different drain voltages V_d = 1V and V_d = 1.8V with V_g = 1V. It

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can be shown that the minimum noise figures of two breakdowns measured at V_g = 1V and V_d = 1.8V behave similarly, which are much larger than the noise of drain breakdown device at $V_g = V_d$ = 1V.

It becomes clear that the bias selection is important for the noise performance of device after breakdown. The gate shot noise will be comparable with induced gate noise when the gate-source leakage is about several micron amperes for 0.18 μm NMOSFETs. The noise parameters may have little change when the breakdown spot is on drain side and gate-source leakage is in this range.

The above results can be applied to the MOSFET low noise circuit design. For MOSFET working in saturation region, the noise figure is not sensitive to drain voltage for a fresh device. It is not the case for a device after breakdown. The difference between gate and drain voltages will largely increase the noise contribution of the resistance r_{gd} (because the current passing the resister is increased) and therefore the noise level of the whole circuit. It means that, if the drain voltage can be chosen to near gate voltage, it can help mitigate the impact of breakdown on the device noise and the probability of circuit failure can be decreased because possible gate-to-drain breakdown may not ruin the functionality of the circuit RF performance. With further reduction of induced gate noise and the increase of leakage current in the new generation of devices, shot noise in further scaled devices should be carefully monitored. Considering this, careful bias selection can also effectively decrease the impact of shot noise on the circuit and finally improve noise characteristics.

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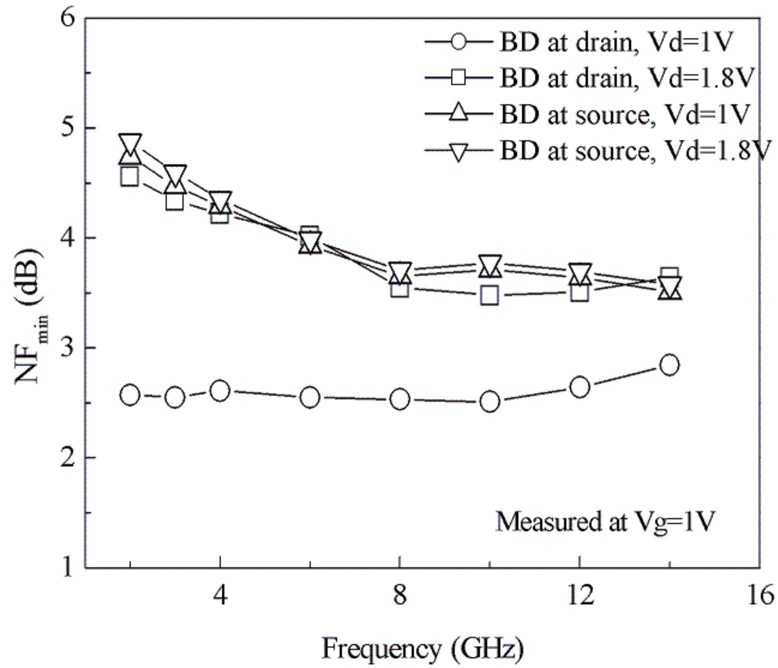

Figure 7.12 De-embedded minimum noise figures ($NF_{\min}$) as a function of frequency for device after drain/source breakdown with V_g = 1V and V_d = 1V & 1.8V

6.6 Summary

The relation between the location of gate oxide breakdown in deep sub-micron NMOSFETs and noise characteristics has been studied. RF Noise characteristics of the devices with different breakdown locations and bias conditions are compared. The results show a strong dependence of degradation of noise parameter both on the gate leakage (breakdown hardness) and the breakdown location. It has been found that, for similar breakdown hardness, the source-side oxide breakdown results in a larger increase in device high

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frequency NFmin as compared to drain-side breakdown. A much larger change in the magnitude of Γ_{opt} is also observed in the device with source-side breakdown. Detailed noise modelling suggests that the increase in gate shot noise after oxide breakdown could be the dominant mechanism for the large increase in NF_{min}. The higher NF_{min} in the devices with source-side breakdown can be attributed to the high gate leakage and thus large gate shot noise in the devices due to the high oxide electric field at source side under the device operation bias conditions. Therefore, concerning on the degradation of RF noise in a post oxide breakdown MOSFET, both oxide breakdown hardness and breakdown location are important criteria. For similar breakdown hardness, formation of the breakdown path closer to source side may result in a larger degradation of device RF noise performance.

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Chapter 8 An Experimental Study of Influence of Carrier Heating on Channel Noise in Deep-Submicrometer NMOSFETs Via Body Bias

7.1 Introduction

As the downscaling of CMOS technology makes CMOS transistors an important option for microwave and RF applications, the analysis and modeling of RF noise in deep-sub micrometer MOSFETs have become critical issues, particularly for low-noise circuits. Significant efforts have been made in the characterization and modeling of the device's high-frequency noise behavior. Although it is now widely accepted that the channel thermal noise could play a dominant role in determining the overall RF noise behavior in sub micrometer NMOSFETs, some controversies still remain as to the physical mechanism involved in deep-sub micrometer devices. The primary emphasis in this chapter is to provide an experimental evaluation of the effect of carrier heating on channel noise in sub micrometer NMOSFETs and investigate if carrier heating has a great impact on RF noise in deep-sub micrometer MOSFETs. Furthermore, since the body (or substrate)-to-source bias has been demonstrated to provide an effective fine control of device and circuit performance such as circuit frequency and low-frequency properties [88, 89, 90], a comprehensive analysis and understanding of the effect of body bias on the device microwave

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(or RF) noise behavior is important for the potential use of CMOS technology in high-frequency low-noise circuits.

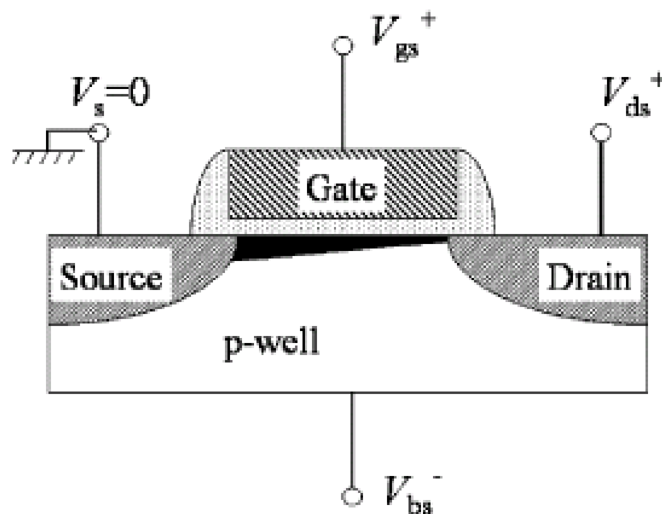

Figure 8.1 Schematic representation of an NMOSFET under reverse body bias used in the experiments described in this study.

7.2 Experiments

The data shown here were measured from the devices with eight gate fingers. Contacts to the p-Si well allow for adjustment of the body bias to vary the electric field between the channel and substrate. For a MOSFET with reverse V_b, it is also called Channel Initiated Secondary Electron (CHISEL) injection. This is schematically depicted in Figure 7.1. The CHISEL mode allows for variation of the electron energy distribution in the device with less impact on the oxide electric field (gate-to-source voltage) and other device parameters. In contrast, for the NMOSFETs under conventional bias (V_{bs} = 0), a

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higher V_{ds} is frequently used to increase the channel electric field and heat up the carrier. However, this may also cause a significant change in the oxide field, which, in turn, induces large variations in other device parameters.

7.3 Effect of Reverse Body Bias on DC and RF Noise Performance

Monte Carlo simulation suggests that the electrons in short channel MOSFETs could be heated up by applying a negative bias to the substrate through an impact ionization feedback process [91]. It has been found that, under an increased vertical field, the additional hot electrons could be generated by the hot holes as they traverse the substrate from the point near the drain, inducing an increased hot carrier population in the device. This results in an improved programming efficient for high-speed low-power nonvolatile memories (NVMs). The carrier heating via reverse body bias can be easily probed by monitoring the change of substrate and gate currents [92, 93, 94, 95] or spectroscopic photon emission measurements [96]. Since the experiment has confirmed that the number of hot carries and their energy could be modulated by increasing the reverse V_b of an NMOSFET, we will limit our characterization and analysis of high-frequency noise in the reverse V_b regime to directly assess the impact of carrier heating on channel noise in NMOSFETs.

A. Effect of Reverse Body Bias on DC and Microwave Characteristic

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Figure 7.2 shows the typical substrate current I_b and drain current I_d versus V_g for different reverse V_b values. Increasing V_b from 0 to -1.8V results in an approximate 30% increase in $I_{b,}$ suggesting an increase in the number of hot carrier population in the channel. The increase of threshold voltage with the increase of $|V_b|$ is due to body effect. Considering the increasingly large V_{th}, which lowers the I_d for a given V_g, an even larger increase in hot carrier population, defined as the ratio of I_b/I_d, could be expected. Figure 7.3 plots the I_b and I_b/I_d ratio versus $V_g - V_{th}$ to illustrate the enhancement of hot carrier population by increasing $|V_b|$. The use of $V_g - V_{th}$ instead of V_g alone is to exclude the body effect, which can also be similarly plotted with respect to I_d, as illustrated in Figure 7.4. In the later part, a similar approach will be used for plotting the noise data so that the body effect can be excluded. It can be seen from Figure 7.3 that, at $V_g - V_{th}$ =0.4 V, increasing $|V_b|$ from 0 to 1.8 V results in a 48% increase in the ratio of I_b/I_d, suggesting a drastic carrier heating in the channel.

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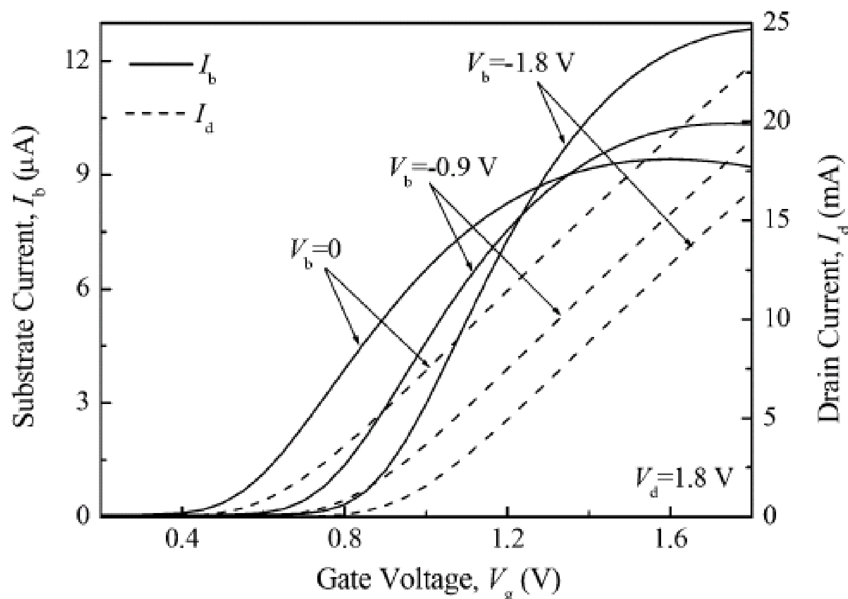

Figure 8.2 Substrate (I_b) and drain (I_d) currents as functions of gate voltage V_g with different substrate voltages V_b as the parameter. The drain voltage V_d is 1.8 V.

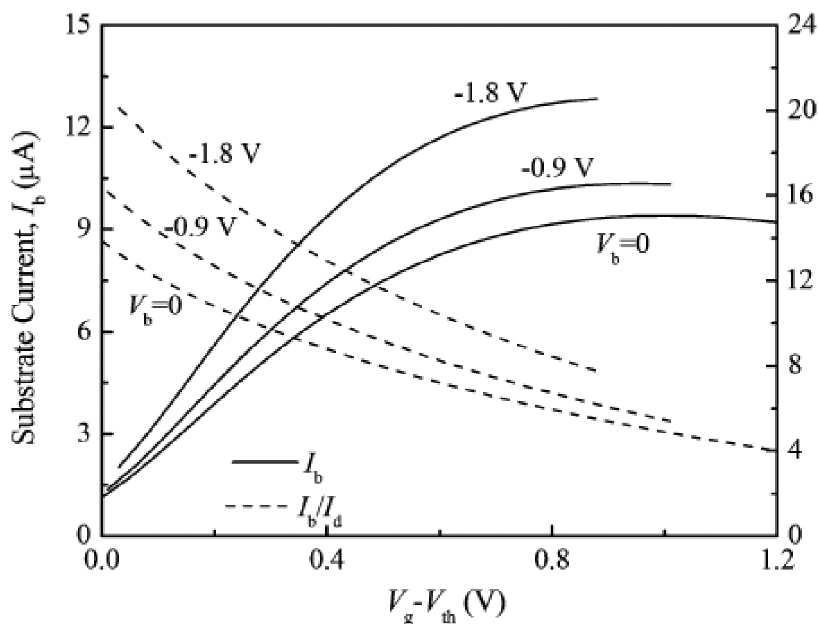

Figure 8.3 Plot substrate current I_b and ratio of I_b /I_d versus V_g -- V_{th}

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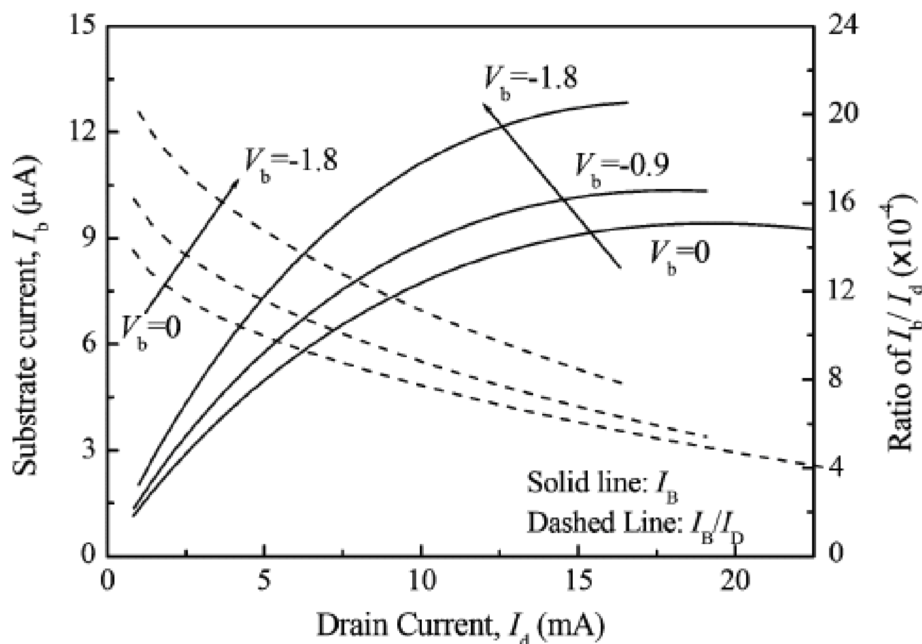

Figure 8.4 Plot substrate current I_b and ratio of I_b /I_d versus I_d to exclude the body effect. The increase in I_b and I_b /I_d suggests the carrier heat via negative body bias.

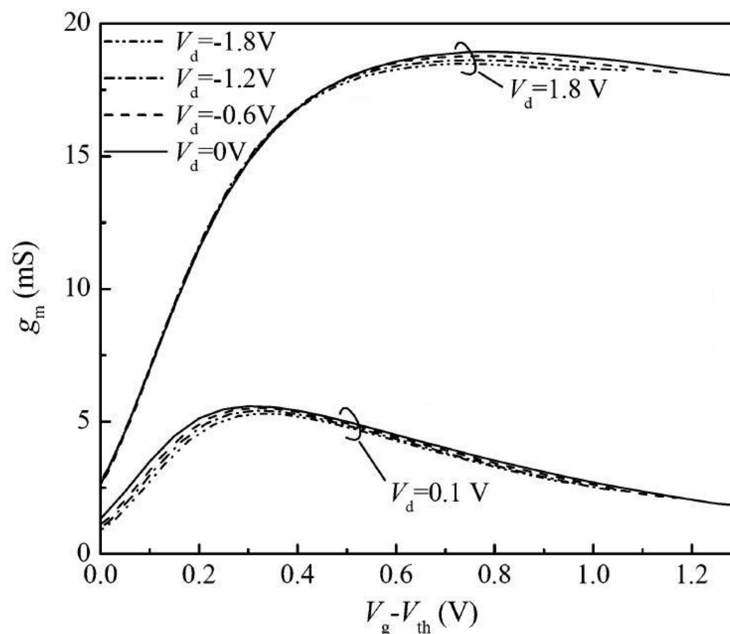

Figure 8.5 Saturation and linear transconductances (g_m) as a function of $V_g - V_{th}$ with different body bias.

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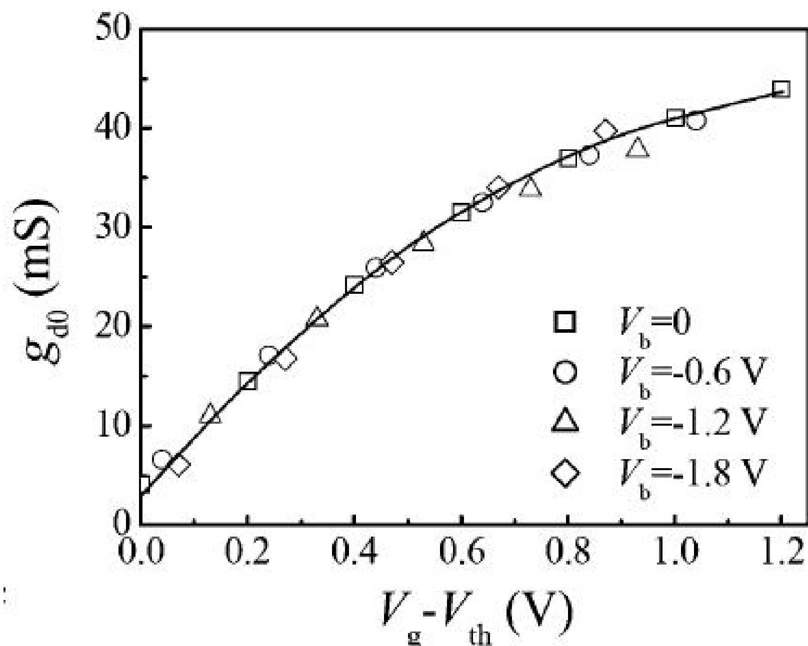

Figure 8.6 Output conductance at zero drain source bias (g_{d0}) as a function of V_g -V_{th} with different body bias. Both g_m and (g_{d0}) are insensitive to V_b

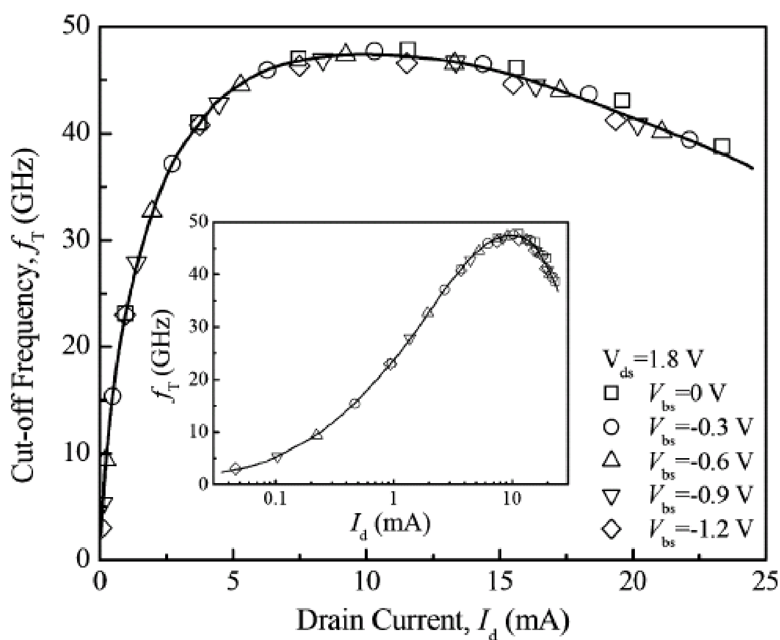

Figure 8.7 Cutoff frequency f_T versus drain current as a function body bias. The V_{ds} was set to 1.8 V during the measurements. Inset: Plot the same curve in a log scale of I_d to illustrate the low I_d region.

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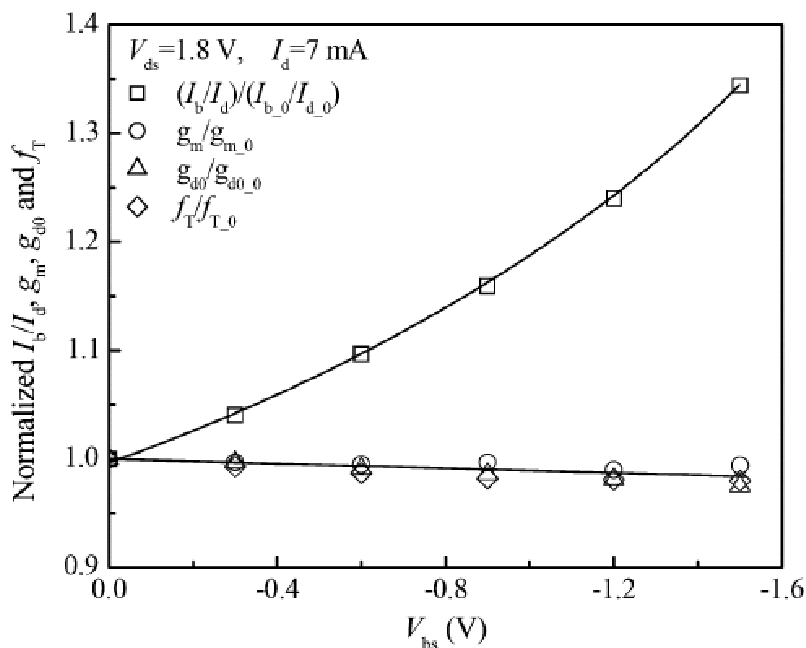

Figure 8.8 Comparison of the variations of I_b /I_d; g_m; g_{d0}, and f_T with the increase in body bias. The increase in |V_b| results in drastic increase in the ratio of I_b /I_d with negligible impact on the other parameters.

However, it is interesting to see that the impact of body bias on other important parameters such as transconductance (g_m) and output conductance at zero drain source bias (g_{d0}) is trivial. Note that these parameters could also largely affect the device noise behavior. Figure 7.5 compares the linear and saturation g_m of an NMOSFET measure at different body bias. It is noted that only a negligible decrease in g_m is observed. The slight reduction of g_m with the increase in |V_b| could be explained by the increase in surface scattering of the channel electrons. This is because the application of a negative body bias on the NMOSFET could make the channel electron move toward the region closer to the surface. The dependence of g_{d0} on the body bias is illustrated in Figure 7.6.

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The variation of g_{d0} with different body bias up to V_b = -1.8 V is negligible. Furthermore, the effect of body bias on device microwave performance was also evaluated by comparing the cutoff frequencies (f_T), which are shown in Figure 7.7 and its inset. Again, a plot of f_T versus drain current as a function of V_b suggests a negligible influence of body bias on the device microwave performance. In general, the device dc and microwave characteristics such as g_m, g_{d0} and f_T are insensitive (<3%) to negative body bias if the body effect is excluded. In contrast, applying a negative body bias results in a drastic increase in the ratio of I_b/I_d, i.e., carrier heating, as illustrated in Figure 7.8. This confirms that the application of a reverse V_b may only have a minimal impact on oxide field and, subsequently, device operation, except carrier heating.

B. Effect of Reverse Body Bias on RF Noise at 2 GHz

At high frequencies, channel thermal noise is the major noise source. Besides the channel thermal noise, induced gate noise, gate resistance noise, and substrate noise could also contribute to the overall noise. To emphasize the channel noise and simplify our analysis, an intermediate frequency (f = 2GHz, and $f/f_T < 0.1$) is chosen to minimize the influence of low-frequency noise such as $1/f$ noise and induced gate noise, which is important at high frequency. The gate resistance noise, which is determined by the poly gate resistance, is hardly affected by body bias, and can be treated as a constant noise source for different $|V_b|$. Figure 7.9(a) shows a typical set of minimal noise figure (NF_{min}) at 2 GHz for different V_{gs} measured under different body biasing voltages. For low values

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of V_{gs}, the minimum noise decreases in value with the increase in V_{gs}. At certain V_{gs}, increase in the V_{gs} causes the minimum noise to increase in value. This is due to the variation of g_m for different V_{gs}. In the low V_{gs} regime, g_m is increased with the increase in V_{gs}, while g_m starts to saturate at V_{gs} which the minimum noise figure reaches its minima. Increase in reverse V_b causes a shift NF_{min} minima toward high V_{gs}. This, again, could be attributed to the shift of device turn-on due to body effect, which is confirmed by re-plotting NF_{min} NF_{min} as a function of I_d instead of V_{gs} itself, as shown in Figure 7.9(b). It is clear that an increase in reverse V_b not only causes the shift of NF_{min} minima, but also causes a slight decrease in value. Similar trends were observed for the noise figures when the measurements were switched to the 50-Ω system. NF_{50} is dominated by device drain current thermal noise and much larger than NF_{min}, which ensures better noise de-embedding accuracy and eliminates the possible errors induced by the noise measurements. The measurements of NF_{50} are shown in Figure 7.10. Measured NF_{50} shows a ~0.4-dB decrease when the body bias is changed from 0 to -1.2 V.

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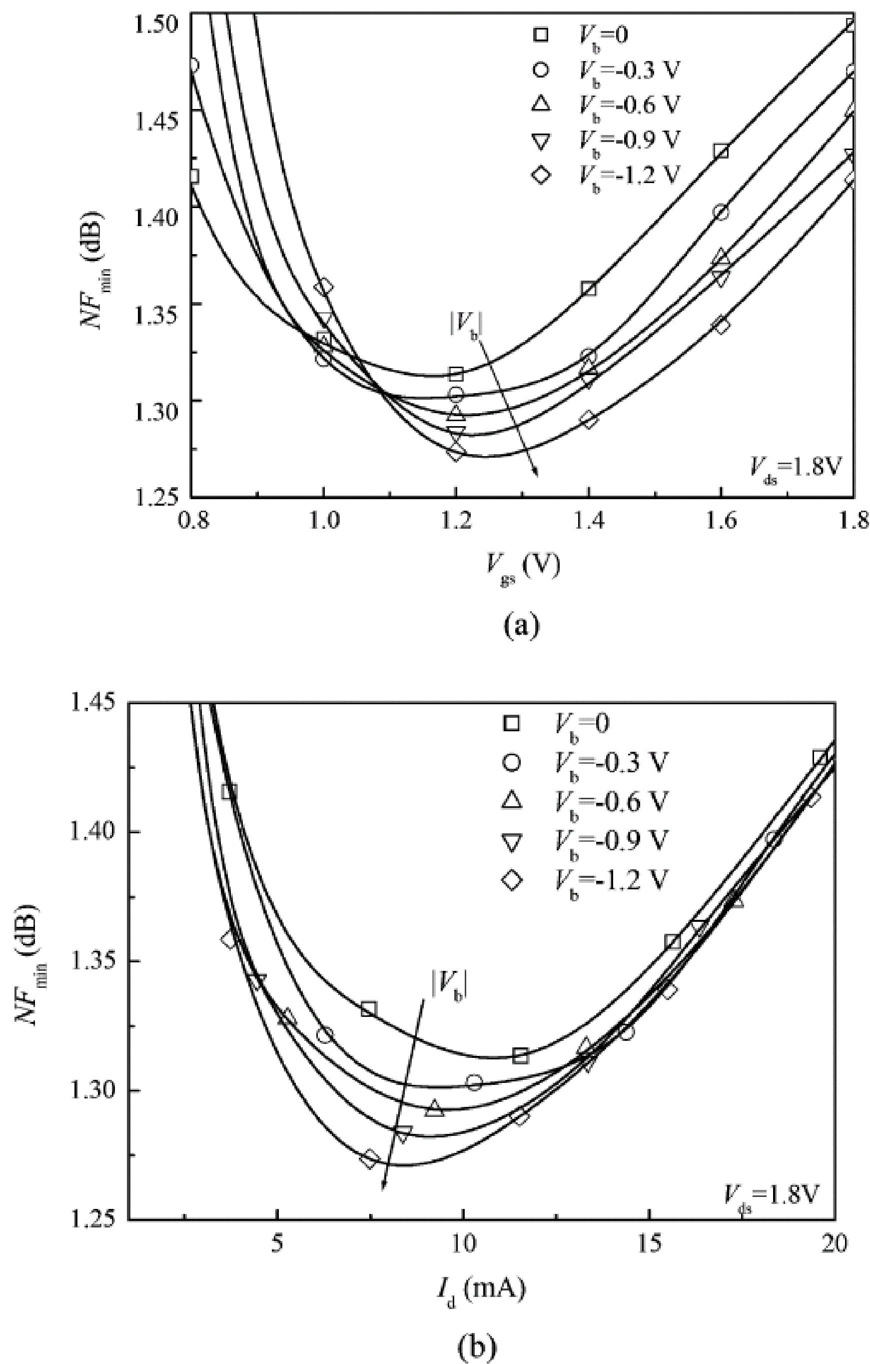

Figure 8.9 Minimum noise figure NF_{min} versus gate bias: (a) V_{gs} and (b) drain current I_d as function of body bias. A slight decrease in NF_{min} with the increase of $|V_b|$ is measured.

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The dependence of equivalent noise resistance (R_n) on the body bias shown in Figure 7.11 reveals a trend similar to those for noise figures. R_n is decreased from 148 to 131 Ω when V_b is varied from 0 to -1.2 V. To a first order, if the contribution of substrate noise is small [97], the noise parameters R_n and F_{min} for the MOS devices can be written as [98, 99]

$$F_{\min} = 1 + 2R_n \omega C_{gs} \sqrt{\delta(1 - c_G^2)\alpha^2 / (5\gamma)} \tag{7.1}$$

$$R_n = \frac{\gamma}{\alpha g_m} \tag{7.2}$$

where $\alpha \equiv g_m/g_{d0}$, δ, γ and c_G are parameters of the models for channel noise and induced gate noise. Notice that R_n is dominated by the channel (drain) noise current, while F_{min} is related to the contributions from the channel (drain) noise current and gate-induced noise current (term under the square root). The reduction of channel noise could affect both R_n and noise figures (NF_{min} and NF_{50}).

It is worth noting that the reduction of NF_{min} and R_n would be beneficial to low-noise circuit design. Considering the well-known noise-figure equation pertaining to a linear noisy two-port,

$$F = F_{\min} + \frac{R_n}{G_s} | Y_s - Y_{opt} |^2 , \tag{7.3}$$

where $Y_s = G_s + jB_s$ is the signal source admittance, smaller F_{min} results in smaller F. Furthermore, for a design with imperfect noise matching, i.e., Y_s is not exactly equal to Y_{opt}, a decrease in R_n by applying a reverse V_b could reduce the noise contributed by mismatching. The reflection coefficient Γ_{opt} at a

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minimal noise figure, instead of the optimum admittance Y_{opt}, is often used in noise measurement as follows:

$$\Gamma_{opt} = \frac{1 - Y_{opt} Z_0}{1 + Y_{opt} Z_0}, \tag{7.4}$$

where the characteristic impedance Z_0 = 50 Ω. Figure 7.12 and 7.13 show the magnitude and angle of the optimum coefficient versus drain current at 2 GHz as a function of body bias. Both the magnitude and angle of the optimum coefficient are insensitive to body bias. The weak dependence of magnitude and angle of the optimum coefficient to the body bias indicates that the variation of the device equivalent-circuit element values at different V_b is small.

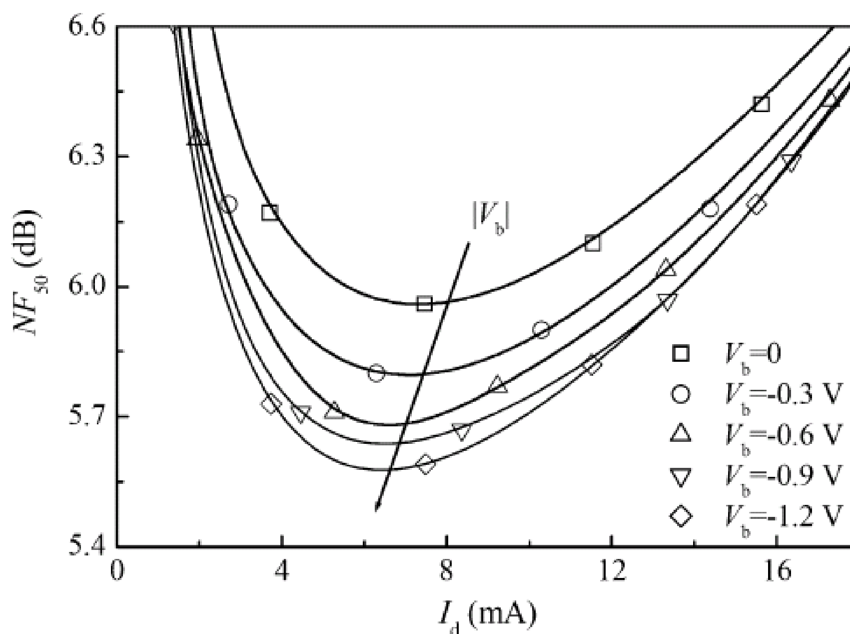

Figure 8.10 Noise figure at 50-Ω generator impedance NF_{50} as a function drain current I_d. Increase of $|V_b|$ from 0 to 1.2 V results in ~0.4-dB reduction of NF_{50}.

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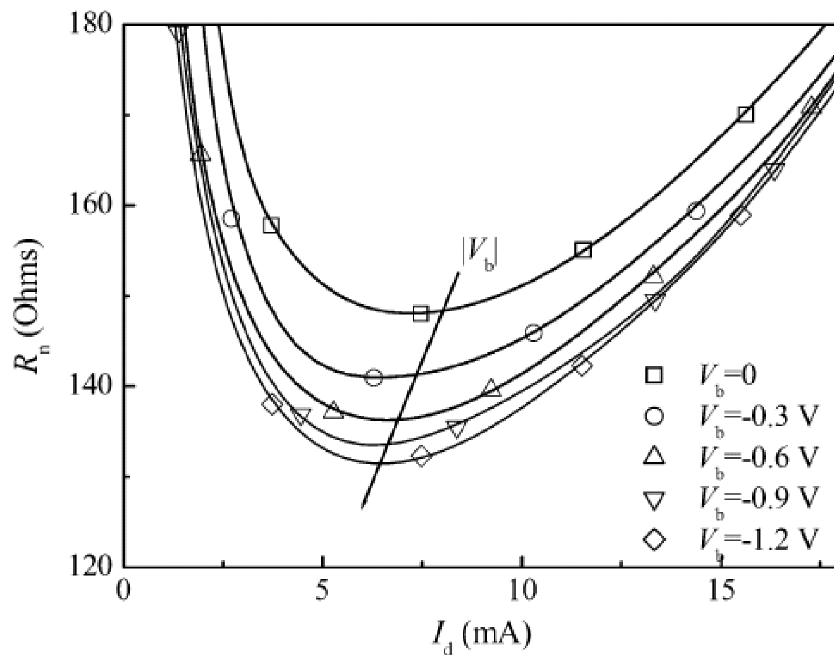

Figure 8.11 Noise resistance R_n versus drain current I_d as a function of body bias V_b.

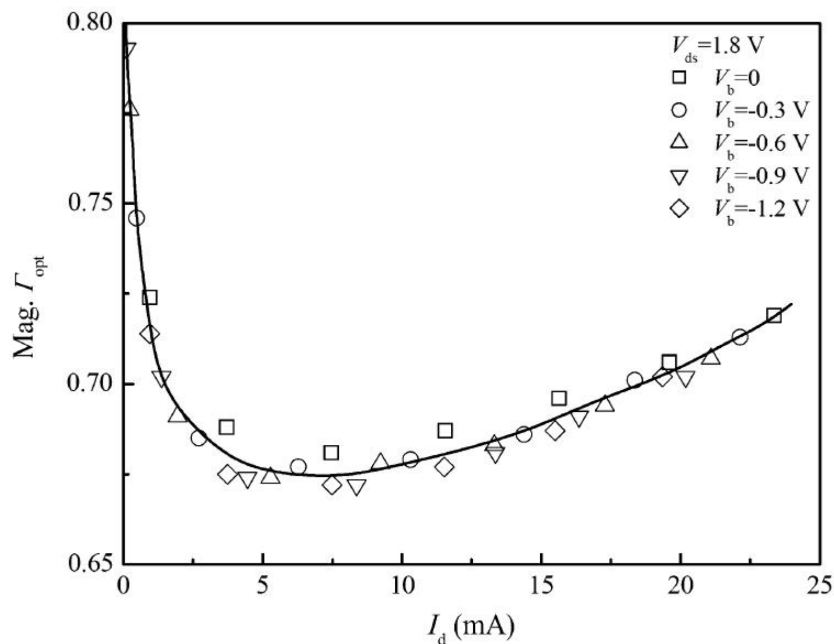

Figure 8.12 Magnitude of the optimum coefficient versus drain current at 2 GHz as a function of body bias.

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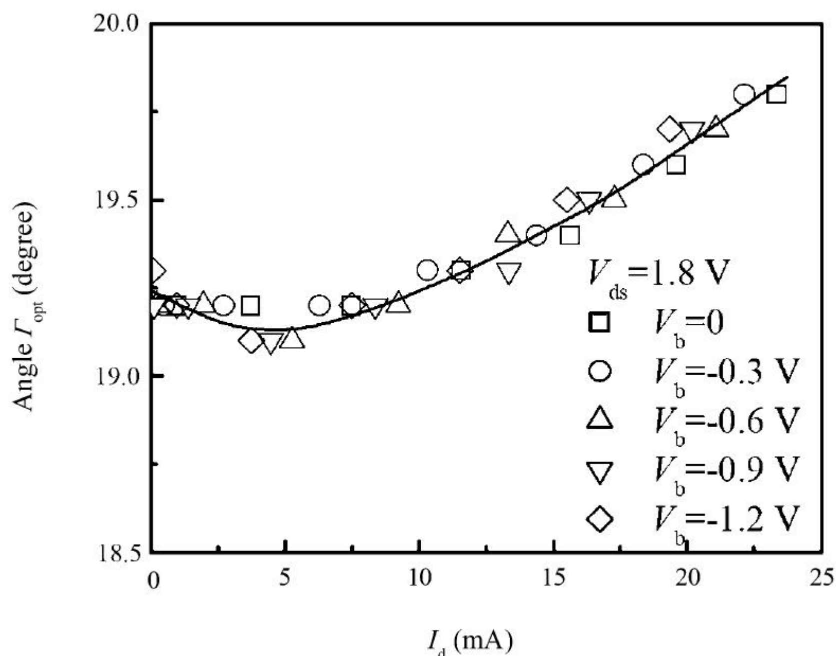

Figure 8.13 Angle of the optimum coefficient versus drain current at 2 GHz as a function of body bias.

7.4 Discussion

If carrier heating plays an important role in determining channel thermal noise, the application of a negative body bias to increase the hot carrier population would cause an increase in the white noise γ-factor, and subsequently, F_{min} and R_n. However, the noise measurements given in Figures 7.9 and 7.11 show otherwise another picture. NF_{min} and R_n are weakly dependent on V_b and, in fact, slightly decrease with the increase in $|V_b|$, indicating that carrier heating may not play a dominant role in determining the excess channel noise in deep-sub micrometer MOSFETs. Considering that it is

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unaffected by $|V_b|$, following the (7.2), the decrease in R_n with the increase in $|V_b|$ (shown in Figure 7.11) would suggest a slight reduction of the γ factor with carrier heating. This clearly does not agree with the postulation of the increase of γ by hot carriers.

Two possible models based on different physical mechanisms could be used to explain our experimental observation. One is the nonequilibrium noise theory proposed by Navid and Dutton [100]. It was proposed that, in deep-sub micrometer MOSFETs, the channel noise should include not only the usual thermal noise component, but also a partially suppressed shot noise term associated with the limited number of inelastic scattering events in the channel. Simulation studies indicated that reducing the channel length or increasing the mean free path to reduce the number of inelastic scattering events to the orders of ten could significantly enhance the contribution of this nonequilibrium noise. For an NMOSFET with gate length shorter than 0.7 μm, the nonequilibrium noise could not be ignored. Applying the nonequilibrium noise theory to our experimental data, the reduction of the channel noise can be easily explained. As we increase $|V_b|$ to increase the body potential, more scattering events are expected due to the surface scattering mechanism. This causes a reduction of nonequilibrium noise components and, consequently, reduces the total channel noise. Mathematically, the drain noise can be expressed as

$$S_{I_d} = S_{I_d}^{Eq} + C(V_{gs}, V_{ds}, V_{bs}) \cdot 2qI_d, \tag{7.5}$$

where S^{Eq}_{Id} is the equilibrium noise term, and the coefficient $C(V_{gs}, V_{ds}, V_{bs})$ is deliberately indicated in a generic form to indicate that the proportionality

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factor depends in a complex way on the gate, drain, and body biasing voltages. In our case, if more scattering events are induced by increasing $|V_b|$ due to surface scattering, the contribution from nonequilibrium noise could be suppressed or even vanished, which then reduces the drain noise. Note that, although a qualitative explanation can be given based on the aforementioned nonequilibrium noise model, a theoretical prediction and calculation of device noise including the nonequilibrium effect is difficult, unless the correlation between the coefficient *C* and device bias can be determined.

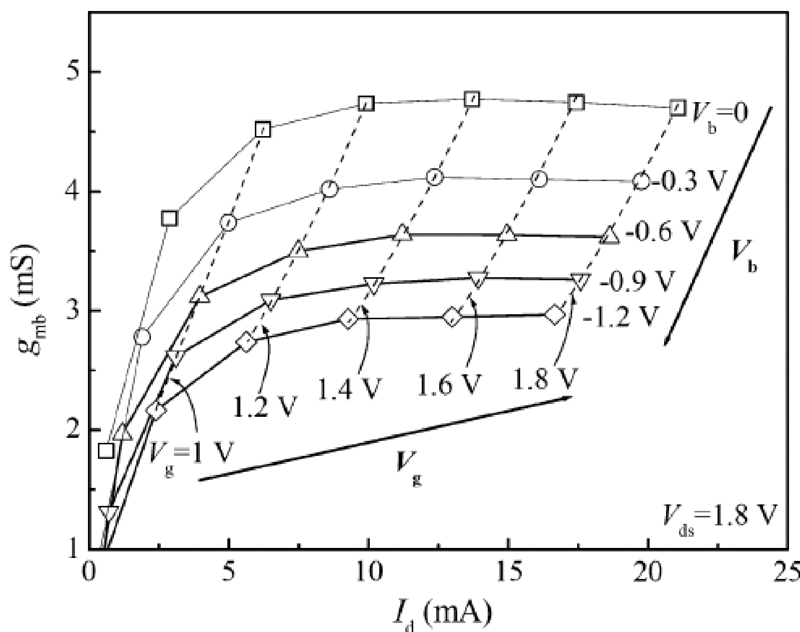

Figure 8.14 Bulk transconductance (g_{mb}) as a function of I_d for different V_b. Reduction of g_{mb} from ~4.7 to 2.9 *mS* when $|V_b|$ is increased from 0 to 1.2V.

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An alternative explanation can be proposed by considering the substrate noise. Although it is generally believed that substrate noise generated from the distributed substrate resistance could be considered as a second-order effect on the device overall noise [97], and the substrate resistance [101] and substrate induced noise [102] are not very sensitive to device bias conditions, ignoring the impact of the contribution from the substrate by (7.2) could still be oversimplified. For example, according to [103], the substrate noise will probably play a considerably important role when the gate resistance is reduced to a small value by the multiple-finger layout. The substrate noise can be qualitatively expressed as [104]

$$\bar{i}_b^2 = 4kTm\frac{d}{W}g_{mb}^2\Delta f \;, \tag{3.6}$$

where m is a constant, d is the space size between gate and bulk contact, W is the gate width, and g_{mb} is the bulk transconductance, which depends on V_{bs}. Indeed, Figure 7.14 shows a reduction of g_{mb} from ~4.7 to 2.9 mS with the $|V_b|$ increased from 0 to 1.2 V. Due to the unknown constant m, an accurate calculation of this substrate noise is difficult. However, by considering the substrate noise, following the method given in [103], a quantitative estimation of R_n is possible by modifying (3.2) with a factor of D_c as

$$R_n = \frac{\gamma}{\alpha g_m}D_c \text{ with } \alpha \equiv g_m / d_{d0} \,. \tag{7.7}$$

For the device biased in a strong inversion region, D_c is given by

$$D_c \cong 1 + \alpha_g + \alpha_{sub} = 1 + \frac{g_m R_g}{1.3\gamma} + \frac{g_{mb}^2 R_{sub}}{1.3\gamma g_m}, \tag{7.8}$$

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where R_g and R_{sub} are the gate and substrate resistances, respectively. Substituting (7.7) into (7.8), the new expression for equivalent noise resistance becomes

$$R_n = \frac{\gamma}{\alpha g_m} + \frac{R_g}{1.3\alpha} + \frac{g_{mb}^2 R_{sub}}{1.3\alpha g_m^2}. \tag{7.9}$$

Therefore, if the parameters such as γ, g_m, g_{d0}, R_g and R_{sub} are independent to body bias, we would expect a parabolic behavior of R_n with g_{mb} at different V_b. Plotting R_n versus g_{mb} in Figure 7.15 well follows this trend. Thus, the possibility of suppression of substrate noise at high $|V_b|$ can also qualitatively justify the reduction of device noise.

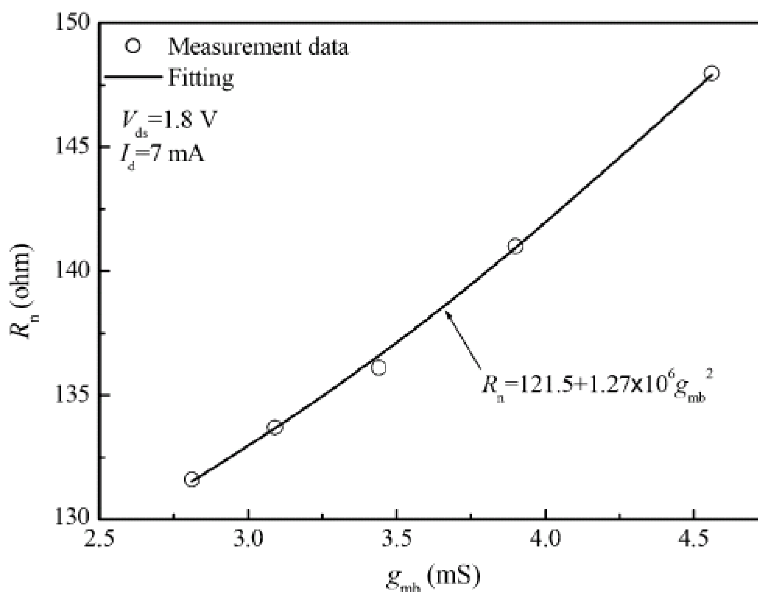

Figure 8.15 Plotting R_n versus g_{mb} shows a parabolic relation. The values R_n and g_{mb} were extracted from Figures 7.11 and Figure 7.14 at I_d = 7 mA for different V_b.

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7.5 Conclusions

In summary, this work has investigated the impact of body bias on RF noise behavior in deep-sub micrometer NMOSFETs to understand if carrier heating and hot carrier effect are the root causes of the excess channel thermal noise observed in short-channel MOSFETs. Using a novel approach that modulates the channel carrier heating and number of hot carriers through reverse body bias without causing significant changes to other device parameters, the postulation of enhancement of high-frequency noise in deep-sub micrometer MOSFETs due to channel carrier heating is directly assessed. Even though the increase in hot carrier population in the 0.18- μm NMOSFETs by reverse V_b was confirmed by dc characteristics, the device high-frequency noise is found to be irrelevant to the increase in channel hot carriers in the explored bias conditions.

Clear evidence was found, instead, that high-frequency noise is slightly reduced with the increase in $|V_b|$, and can be qualitatively explained by secondary effects such as the suppression of nonequilibrium channel noise or substrate induced noise. Our experimental result does not support the postulation that invokes the enhancement of channel noise in deep-sub micrometer NMOSFETs by the hot carrier effect. At least in the bias conditions for conventional operation, the contribution of carrier heating to high frequency is nevertheless too insignificant and could be masked by those second-order effects. This is consistent with some of the recent findings based on the extraction of RF noise models. We further notice that the reduction of NF_{min}

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and R_n with the increase in $|V_b|$ outlined in this work provides a possible methodology to finely adjust the device high-frequency noise performance.

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Chapter 9 Conclusion and Recommendation

8.1 Conclusion

The noise characteristics and modeling of deep sub-micron MOSFETs have been demonstrated. The physical mechanism of channel thermal noise current and FN stress on noise performance are investigated. The important findings from these studies are summarized below:

(1) A straight forward one-step direct matrix method is proposed to extract channel thermal noise and induced gate noise in deep submicron NMOSFETs. Good agreement between results from this method and the classical method is observed. It has been shown that this method can be well applied to the future technology.

(2) The effect of FN stress and oxide breakdown on high-frequency noise performance for NMOSFETs has been studied. The noise characteristics of the devices at different leakage levels and breakdown hardness are compared. The results have shown a strong dependence of degradation of noise parameter on the gate leakage. It has been found that the drastic increase of device high frequency noise after gate oxide breakdown can be attributed to the significant increase in the contribution of gate shot noise, which is believed to be negligible in as-processed 0.18 μm NMOSFETs. Considering the great impact of oxide leakage on the RF MOSFETs, determining a gate leakage limit as a criterion for the post-breakdown oxide is necessary.

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(3) The relation between the location of gate oxide breakdown in deep submicron MOSFETs and noise characteristics has been investigated. RF Noise of the devices with oxide breakdown at different locations are characterized and compared. It has been shown that degradation of noise parameters subject to gate oxide breakdown is not only related to breakdown hardness but also the location of the oxide breakdown path.

(4) The role of carrier heating and hot carrier effect on the excess channel thermal noise observed in short channel MOSFET is assessed via a novel approach that modulates the channel carrier heating and number of hot carriers using substrate bias. The experimental evidence shown indicates that hot carrier effect does not show too much impact on the channel noise of deep submicron MOSFETs, which does not support the widely adopted postulation that enhancement of channel noise in deep submicron NMOSFETs by hot carrier effect.

8.2 Recommendation for future works

Based on the above research results which have been achieved, further studies to comprehensively analyze the effect of FN stress on device RF performance and the mechanism behind these observations are necessary. The work to be pursued is listed below:

(1) A reversed frequency dependence of minimum noise figure in the frequency range of 2 to 6 GHz was revealed in our submicron meter NMOSFETs after oxide breakdown. Similar behavior was also reported in the

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literatures. Currently, there is no clear answer for the mechanism behind this phenomenon. Modeling the device simply based on the increase in gate shot noise induced by oxide breakdown could not provide a solid prediction in this frequency region. Further studies can be carried to gain a better understanding on the physical mechanism of the change in frequency dependent minimum noise figure in this frequency range in the post oxide breakdown devices. In particularly, a detailed RF noise modeling can be performed to see whether there are any other noise sources aroused by the oxide breakdown, and how they influence the overall device noise.

(2) Considering that the device is practically operated under AC or RF signal in analogue or RF circuits. It is important to extend our current study to the device undergoing AC stress. The AC or RF signal instead of DC bias can be used to perform stress tests. The degradation of the RF noise performance in deep sub micrometer MOSFETs subjected to AC or RF stress can be characterized and analyzed.

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