Advanced control methodologies of DC-DC converters

He, Yi

2008

He, Y. (2008). Advanced control methodologies of dc-dc converters. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/4119>

<https://doi.org/10.32657/10356/4119>

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Advanced Control Methodologies of Dc-dc Converters

He Yi

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2008

ACKNOWLEDGMENTS

I would like to express my deep gratitude to my supervisor, Associate Professor Luo Fang Lin for his invaluable guidance, help, and encouragement throughout my research. Without his support, I can not finish my thesis.

The research work would not be possible without the financial support provided by Nanyang Technological University in the form of a research scholarship. For this I am most grateful.

I am indebted to many people who assisted me in the fulfillment of this research work. Special thanks should be given to Associate Professor Luo Fang Lin's other Ph. D students who are Mr. Pan Zhiyang, Mr. Liu Yu and Mr. Zhu Miao.

I am also deeply thankful to Mr. Yeoh Tiow Koon, Mr. Lee Ting Yeng and Ms Chew-Sim Annie for the technical support they have given me in the course of my research.

Last but not at least, to my wife, Yanqin, for her unfailing support, patience, and cooperation that have made the completion of the research work possible, and also my family for their invaluable support and understanding over these three years or so of my graduate program.

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SUMMARY

Study of dc-dc converters has always being a hot research area due to many reasons which include (a) the technical challenges keep coming due to the wide application of dc-dc converters, and (b) they are highly nonlinear systems which pose a lot of trouble in modeling and control. The main research directions for dc-dc converters fall into three categories. Firstly, as energy issue becomes more and more critical so far, a lot of efforts have been paid on development of new topologies which can achieve higher power conversion efficiency or higher voltage transfer gain (VTG). Second, modeling of dc-dc converters involves many difficulties due to its high switching frequency. Finally, control of dc-dc converters also gains much interest as the regulated output voltage is always desired in dc-dc converters, where wide variations of input voltage and load resistance are very common.

The investigation in this thesis begins with modeling of Luo converters under steady state using ripple approximate theorem. The steady state analysis gives a clearer insight of the characteristics of Luo converters under both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Especially, the influence of voltage lift circuit (VLC) circuit has been carefully examined and the results are extended to the family of the Luo converters with voltage lift circuit.

Based on the steady state analysis of Luo converters, a small-signal state-space equation of high-order Luo converter has been derived, which forms the basis for designing a closed loop control system for Luo converters. In order to reduce the current overshoot during start up of the converter, a new SM controller has been proposed in this thesis. The analysis shows that the proposed controller can achieve better dynamic response than the traditional SM controller. Simulation and experiments results have been given to verify the analysis.

In practical realization, the traditional SM control causes troubles in filter designs due to its variable switching frequency and high cost for implementation of the hysteresis

controller. The investigation is then continued on design a constant switching frequency SM controller. As a result, the equivalent SM control has been proposed for controlling Luo converters. The analysis shows the proposed controller can achieve constant switching frequency and it can also retain the other advantages of traditional SM control at the same time, such as large signal stability and fast dynamical response. Simulations and experiments also show that equivalent SM control has some disadvantages such as non-zero steady state error and high cost due to the divider used in the control circuit.

In Chapter 5, the adaptive control has been introduced into the equivalent SM controller. By modeling most of the power losses in dc-dc converters with a single resistor, the adaptive algorithm can be easily designed to estimate the power losses in the circuit. By doing so, the output steady state error can be eliminated.

The one-cycle control (OCC) concept has also been applied into the equivalent SM controller for the purpose of saving the divider. This is achieved by replacing the divider function with a comparator based on a voltage controlled saw-tooth waveform generator. The analysis also shows that the controller performance will not be affected by such replacement.

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LIST OF SYMBOLS

A :	State matrix for a state-space averaged model
A_S :	State matrix for a small-signal state-space averaged model
B :	State matrix for a state space averaged model
B_m	viscous friction coefficient, $N \cdot m \cdot s$
B_S :	State matrix for a small-signal state-space averaged model
C_n :	Capacitance of capacitor n
D :	Constant duty cycle (duty ratio) and $D = \frac{T_{on}}{T_{on} + T_{off}}$
d :	Instantaneous value of duty cycle (duty ratio)
D_X :	Diode X
f :	Switching frequency
f_C :	Cross-over frequency in a bode-plot
$G_d(s)$:	Duty cycle to output transfer function
$G_{ref}(s)$:	Reference-to-output transfer function
$G_{vin}(s)$:	Input-to-output transfer function
g_i :	Coefficient for current variable in a sliding function
g_v :	Coefficient for voltage variable in a sliding function
I_X, V_X :	Average current and voltage of component X
i_a	armature current, A
i_O, I_O :	Output current of the converter
i_{in}, I_{in} :	Input current of the converter
i_X, v_X :	Instantaneous current and voltage of component X
J	motor and load inertia, $kg \cdot ms^{-2}$
K_T	motor torque constant, $N \cdot m \cdot A^{-1}$
K_E	motor EMF constant, $V \cdot rad^{-1} \cdot s$
L_a	armature inductance, H
L_n :	Inductance of inductor n
M :	Value of voltage transfer gain of a dc-dc converter
M_X :	Voltage transfer gain for dc-dc converter with name X

R :	Resistance of the load resistor
R_a	armature resistance, Ω
R_L :	Power loss coefficient in Buck converter
S :	<i>Laplace</i> translator
T :	Switching period and $T = 1/f$
T_d	Developed torque
T_f	coulomb friction coefficient, $N \cdot m$
T_L	load torque, $N \cdot m$
T_{on} :	On time during one period for the switch
T_{off} :	Off time during one period for the switch $T = T_{on} + T_{off}$
u :	Discrete control output of a traditional sliding-mode controller
u_{eq} :	Equivalent control output of a traditional sliding-mode controller
v_{in}, V_{in} :	Input voltage of the converter
v_O, V_O :	Output voltage of the converter
v_{emf}	motor electromotive force
v_m	terminal voltage of the motor, V
X :	State vectors in the state-space models
$X _{condition}$:	Value of X under the condition
X_{eq} :	Equivalent point of state vector X in steady state
x_n :	The n^{th} component of state vector X
$\dot{x}$:	Differential of x regarding to time
$Z_{out}(s)$:	Output impedance of the closed-loop controlled dc-dc converter
α :	Current coefficient in the sliding function
β :	Voltage coefficient in the sliding function
γ_C :	Critical adaptive speed coefficient
δX :	Small-signal variations of state vector X
ε :	Value for hysteresis band
ε_{norm} :	Normalized value for hysteresis band in an adaptive version
κ_i :	Coefficients used in the sliding mode controller in motor drives
λ_i :	VLC coefficient in Luo converters
$\sigma(X, t)$:	Sliding function as functions of time and circuit variables
$\Delta i_X, \Delta v_X$	Variations of changing current and voltage variables

List of Symbols

$\xi :$	Filling efficiency of dc-dc converters working in DCM
$\zeta :$	Boundary criteria for dc-dc converters working between CCM and DCM
ω_m	motor angular speed, $rad \cdot s^{-1}$

LIST OF ABBREVIATIONS

CCM:	Continuous conduction mode
DCM:	Discontinuous conduction mode
EMI :	Electro-magnetic interference
FET:	Field-effect transistor
FLC:	Fuzzy logic control, fuzzy logic controllers
LHP:	Left half plane
MOSFET:	Metal-oxide-silicon field-effect transistor
NOSLL converter:	Negative output self-lift Luo converter
OCC:	One-cycle control
PFM:	Pulse frequency modulation
PID:	Proportional-integral-differential
PM:	Permanent Magnetic
POEL converter:	Positive output elementary Luo converter
POSL converter:	Positive output super-lift converter
POSSL converter:	Positive output self-lift Luo converter
PORLL converter:	Positive output re-lift Luo converter
PWM:	Pulse width modulation
RHP:	Right half plane
RP:	Representing point
SCMC:	Sensorless current mode control
SL	Super lift
SM:	Sliding Mode
SMPS:	Switch mode power supply
VTG:	Voltage transfer gain
VL:	Voltage lift
VLC:	Voltage lift circuit
VSC:	Variable structure control

Chapter 1 Introduction

1.1 Introduction

The energy issue is very important in the world. How to use energy wisely and efficiently is of much interest to researchers. Power Electronics is the technology dealing with the efficient electric power conversion using power semiconductor devices [1-2]. Power Electronics has been widely used in many areas, such as electric motor drives, uninterruptible power supplies, high-voltage DC transmissions, and regulated power supplies for computers, telecommunication equipments and other electronic devices. Based on the forms of input and output electric power, studies of power electronics can be classified into four categories [3-4]: ac-dc conversion, dc-dc conversion and ac-ac conversion and dc-ac conversion. Products of the first two kinds of conversions contribute to most of the world switch mode power supply (SMPS) market, especially the dc-dc converters [5].

In recent investigation it is found that the production of dc-dc converters has occupied 68 % of the Power Electronics production world market, which is nearly US\$3.3 billion in 2005 and will increase to US\$5.4 billion in 2010 [4]. It is therefore necessary to pay more attention on the studies of dc-dc converters. A general representation of a dc-dc power processing unit is shown in Figure 1-1. It is seen that a dc-dc power conversion unit includes the converter and the control circuits. Accordingly, the studies of dc-dc converters are almost spent on those areas.

The main challenges existing in the present control systems of dc-dc converters can be classified as:

- With the development of communication and information technology, lower and lower voltage level is used. The ripple voltages and voltage variations during

transients in the output voltage of dc-dc converters should be kept at a relatively low level for stable operations [6-7].

- The efficiency of the conversions should be increased so that smaller heat sinks can be used to increase power-density of dc-dc converters.
- Other requirement for dc-dc conversions such as higher reliabilities and lower costs.

Figure 1-1 A general representation of dc-dc power conversion system

In an ideal condition, the output of dc-dc converters is easily calculated according to the input voltage and duty cycle. However, in practice, open-loop control can not guarantee high reliability and satisfactory dynamic response. Closed-loop control is often needed. The reasons include:

- Due to the uncertainties and power losses of the converters, the desired duty cycle can not be calculated with high accuracy [8]. Output steady state error often exists in open-loop control;
- The parasitic effects of passive components and un-ideal switches in the circuit are difficult to be measured. Therefore, it is not easy to be considered in the open loop control [8];

- Open loop properties of dc-dc converters are not acceptable in various aspects [1]. For example, the overshoot of output voltage and the stress for electric components during start up are very high;
- When the circuit conditions change, such as input voltage variations, load resistance variations and even circuit fault, open-loop control can not provide acceptable dynamic performance and safe operations.

From the 1960's, the studies of the control systems for dc-dc converters have been attracting much attention. The control issues treated in dc-dc converters fall into two main categories:

- **Control performance** [9]: This issue refers to the accuracy, robustness, and stability of the controller, and also the complexity of the controller in terms of the sensors and computational requirements. It also refers to the dynamic performance of the controller. It includes the disturbance rejection, the ripple content, and the response to an input transient, especially, the disturbances originated from the input voltage variations and the load variations. It also includes the reference-to-output transfer function, which is the controller dynamic performance in tracking a reference change. The rising time, overshoot and settling time in the output voltage waveform are also important indexes when evaluating the performance of a controller.
- **Nonlinear phenomena** [10-11]: Dc-dc converters are nonlinear systems due to the nonlinear components (e.g., the power diodes) and control methods (e.g., PWM). The nonlinear phenomena includes the bifurcations (sudden changes in operating mode), coexisting attractors (alternative stable operating mode), and chaos (apparently random behavior).

Control performance of the controllers is the main concern in this thesis. They can be examined through analyzing the system transfer functions under different conditions. Little attention is given to the nonlinear phenomena in this thesis, which are left for future

study. In addition, modeling of dc-dc converters will also be studied in this project. The development of the converter topologies and control methods will be reviewed in next section.

1.2 Literature Review

1.2.1 Dc-dc Converter Topologies

Many dc-dc converters have been developed since the invention of the first dc-dc converter. Each topology has unique properties which make it best suited for certain applications. For example, less than one watt dc-dc converters for on-board applications; tens, hundreds, or thousands of watts in power supplies for computers and telecommunication devices; and several kilo-watts for electrical motor drives [2].

According to the classification in [4], various converter topologies can be grouped into six main categories. The dc-dc converter family tree is shown in Appendix A.

The first-generation converters, also named as classical/traditional converters, perform in a single quadrant mode and in low power range (up to around 100 W). Other generations of converters include multi-quadrant converters, switched component converters, soft-switching converters, multi-element resonant converters, and synchronous converters. In this thesis, the main concern is the first-generation converters.

Among the first generation converters, Buck, Boost, and Buck-boost converters, shown in Figure 1-2, are three fundamental converters [3]. The Buck converter performs a voltage step-down application. The Boost converter carries out a step-up function. The Buck-boost converter is aimed to give invert-polarity dc power supply. Almost all other dc-dc converter topologies are derived from these three basic types. The development includes adding transformer isolation, using more inductors and capacitors, using more switches, etc [4].

The fundamental converters can provide step-up or down voltage transfer and their output voltage ripples are relatively high. More advanced converters have been developed for wider applications. For example, the output voltage ripples can be decreased to as low as 2% by including a low-pass filter to the fundamental converters. The developed converters can also provide wider range output voltage levels, either higher or lower than the input voltage. Typical examples of developed converters are Luo converters [12-13], shown in Figure 1-3 and Cúk converter [14] shown in Figure 1-4.

Figure 1-2 Three fundamental dc-dc converters

Voltage lift technique [4] is a widely used method in dc-dc converters. Using this method, the output voltage can be easily lifted by ten to hundred times. Voltage lift converters can be classified into self-lift, re-lift, triple-lift, quadruple-lift, and high-stage lift converters according to the number of voltage lift circuit (VLC) used. According to the basic

converter topologies used, there are three series voltage lift converters: series positive output Luo converters, series negative output Luo converters and series double output Luo converters. The configurations of the self-lift circuit of series positive output Luo converters [13] is shown in Figure 1-5 and the re-lift circuit [13] is shown in Figure 1-6. In the remaining part of the thesis, these two circuits are abbreviated as POSLL and PORLL converters, respectively. Similarly, self-lift circuit of the negative output Luo converters [15] is abbreviated as NOSLL converter.

(a) Positive output Luo converter: elementary circuit

(b) Negative output Luo converter: elementary circuit

Figure 1-3 P/O and N/O Luo converters

Figure 1-4 Cúk converter

Figure 1-5 Positive output self-lift Luo converter

Figure 1-6 Positive output re-lift Luo converter

However, the output voltage of these converters increases stage by stage just along the arithmetic progression. An excellent approach, super lift (SL) [16-17] technique, therefore has been developed, which can increase the VTG stage by stage along the geometric progression. This method effectively enhances the VTG in power-law. So far there are four series of super lift converters. The basic one, the elementary circuit of the positive output super lift (POSL) converter [16] is shown in Figure 1-7.

Figure 1-7 Positive output super-lift converter

1.2.2 Modeling and Control Solutions for Dc-dc Converters

The dc-dc converters are nonlinear, time-invariant systems. The straightforward analysis tools such as the Laplace transform and the Nyquist plot can not be applied directly. Therefore, a major goal in the study of these systems has been the development of modeling techniques. The study is always dealing with nonlinear problems and has attempted to explore methods not normally used in other circuit design areas. The state-space averaging [18, 19], sampled data modeling [20, 21], quasi-linear modeling [22], and phase-plane trajectory analysis [10] are several examples that have been derived. For complex converters, there are also some developed modeling methods as shown in references [23-26].

In fact, different models are needed for different stages or aspects of the control design. Even for a specific stage of the design, there are likely to be several possible models differing from their explicitness, complexity, and accuracy, domain of definition, flexibility, and tractability. Several examples are given here: Energy factor modeling [27] is aimed to approximate high-order dc-dc converters with a second order system; the authors of [28] proposed to include impedance of un-resistive load for exact prediction of circuit performance; and authors of [29] included the parasitic components into the averaged circuit models. Nevertheless, almost all modeling methods, including the most popular one, state-space averaging, will result in a multi-variables system with state-space equations, ideal or un-ideal, linear or nonlinear, in steady state or for dynamic purpose.

The small-signal analysis and frequency domain design method are important since many control objectives are evaluated through them. The dc-dc converter's small-signal model can be represented as in Figure 1-8. A dc-dc converter may encounter condition variations mainly from three sources: the input voltage, the output load, and the control signal. Three transfer functions can be defined as below regarding the converter performance under these cases.

Figure 1-8 Small-signal model of a dc-dc converter

The system state-space equation is represented as

$$\dot{X} = A(X, d) + B(d)V_{in} \quad (1-1)$$

where X is the state vector, d is duty cycle, $A(X, d)$ and $B(d)$ are the state matrices.

The small signal equation can be written as

$$\delta \dot{X} = A\delta X + B\delta V_{in} + B_D\delta D \quad (1-2)$$

The last variable of X is considered as the output voltage. Therefore, the output equation is written as

$$\begin{aligned} v_o &= C\delta X \\ C &= [0 \quad 0 \quad \dots \quad 1] \end{aligned} \quad (1-3)$$

The control-to-output transfer function $G_d(s)$ [2] is found by setting $\hat{v}_{in}(s)$ and $\hat{i}_o(s)$ to zero, and then solving for the transfer function from control to output as

$$G_d(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = C \bullet (sI - A)^{-1} \bullet B_D \quad (1-4)$$

s is the *Laplace* operator and I is the unity matrix. This transfer function describes how the control input variations influent the output voltage. Under the condition of closed-loop control, this is the main concern to controller designs. It specifies the system capability in tracking the reference input.

The input-to-output transfer function $G_{vin}(s)$ [2] is derived by setting $\hat{i}_o(s)$ and $\hat{d}(s)$ to zero

$$G_{in}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = C \bullet (sI - A)^{-1} \bullet B \quad (1-5)$$

It is also called the audio-susceptibility of dc-dc converters. It describes how the input voltage variations influence the output voltage. It is of great interest since there are always some input voltage variations caused by the undesired harmonics sourced from AC power line.

To find the output impedance $Z_{out}(s)$ [2], the output current should be written into the equation in replacement of the load resistance. Then, it is found that by setting $\hat{d}(s)$ and $\hat{v}_{in}(s)$ to zero, and then solving for

$$Z_{out}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} \quad (1-6)$$

The output impedance $Z_{out}(s)$ describes how the load variations influence the output voltage. It is especially important in dc-dc converters used in computer power supplies, where some parts of the loads are switched on and off regularly.

Although the controllers of dc-dc converters are different, their control performance can be evaluated through the above criteria in most conditions. And small-signal perturbations method is often used to analyze the closed-loop system.

Normally, various controllers for dc-dc converters can be sorted into two groups: linear and nonlinear ones. Linear control methods refer to those based on linearized small-signal models, such as the PI compensator and the pole-placement controller. Any controller which incorporates nonlinear theory can be viewed as a nonlinear one. Sliding mode (SM) control, fuzzy logic control (FLC), adaptive control, and robust control are the nonlinear control methods often used for dc-dc converters. It is difficult to give clear boundaries for various control methods. For example, adaptive control can be combined with sliding mode control to gain a better performance. Reference [30] has introduced several nonlinear control methods and shown some possible combinations. The review of these controllers in this thesis is categorized in following groups: traditional linear controllers, nonlinear controllers using feedback linearization, H^∞ controllers, FLC, SM control, and adaptive control.

❖ Voltage-mode control

The traditional linear control solutions for dc-dc converters are based on the linearized small-signal state-space equations. A general small-signal state-space equation is shown as

$$\begin{aligned}\delta\dot{X} &= A\delta X + B_D\delta d \\ \delta y &= C\delta X\end{aligned}\tag{1-7}$$

There are two typical controllers. One is the voltage-mode controller shown in Figure 1-9 [1].

Figure 1-9 Voltage-mode controlled Buck converter

The control equation of voltage-mode control is

$$\hat{d}(s) = g(s)e(s)\tag{1-8}$$

In this scheme, the output voltage is subtracted from the reference voltage to generate an error signal $e(s)$. Then this signal is given to the compensator to achieve an optimal desired duty cycle. The compensator $g(s)$ can be a proportional type (P), proportional-integral (PI) or proportional-integral-differential (PID) type.

The other linear control scheme is based on the pole-placement control [7, 33-34]. Full state information is feedback to calculate the control input and therefore the system performance can be regulated by specifying the system pole locations. The closed-loop control scheme of pole-placement control is shown in Figure 1-10.

Figure 1-10 Pole-placement control scheme

The traditional linear control solutions are based on the linearized small-signal models. They are still widely used in industrial applications. However, such models are only valid in a small region around any specified operating point. The validity region in the state-space of the small-signal perturbation is unknown. When the perturbations are large, the anti-disturbance capability of traditional linear controllers often deteriorates. Also it is known that the maximum range of the duty cycle is 0 to 1, which is the input limitation of dc-dc converters. The frequency domain design methods do not always consider such limitations. As a result, the actual system performance is not the same as and most likely worse than the predicted characteristics in the frequency domain.

❖ Nonlinear transformation

Since linear controller can not give satisfactory performance, nonlinear control theory applied on dc-dc converters has gained much attention. In order to apply the linear control techniques on dc-dc converters in large signal mode, the feedback linearization has been studied in many publications. The main idea of this approach is to algebraically transform a nonlinear system dynamics into a fully or partly linear one so that the linear control techniques can be applied. References [35, 36] gave many applications on dc-dc converters. There are inherited disadvantages of such method: the full state variables must be measured. No robustness can be guaranteed in the presence of parameter uncertainty or un-modeled dynamics.

Many references have focused on the application of the state transformation on the control of dc-dc converters. Sira-remirez [37] has proposed a so-called pseudo-linearization method which can determine the nonlinear transformations of the state

variables and control inputs. Then the tangent model (small-signal linearization) of the transformed system is in phase with the canonical form. The advantage of this approach is that it can stabilize an entire class of equilibrium. However, the global stability and the large signal behavior of control system cannot be ensured using this method.

References [38, 39] have applied the nonlinear state transformation to the state-averaged model in large-signal form. The new state variables are the energy function of the original system and its derivatives. The controller can be obtained by steadily decreasing the energy function to its least value corresponding to the equilibrium point. Lyapunov theory is applied in the derivation of such controllers. Similar method can be found in [40, 41], where exact dynamical feedback linearization is used to get the nonlinear feedback controller. For stability problems, it is by regulation of other state variables such as input current to gain output regulations in [42, 43]. Since the output voltage with such a strategy is only controlled indirectly, additional effort is required to treat with the load variations. Generally, most methods using nonlinear or linear transformation can get linear relation between the newly defined control input and output. The problem of the methods is that it requires the exact information of the circuit components. Large quantity of calculations is also needed. They are not suitable for practical use considering cost, performance, and robustness.

❖ Input voltage feed-forward

Reference [44] gave a simple nonlinear feedback controller

$$d = \frac{1}{V_{in}} w \quad (1-9)$$

where w is the control input. The resulted system is a large-signal linear one and independent to input voltage variations. The pole-placement method is then used to derive the feedback compensator. To decrease the output impedance, it is also suggested that the output capacitor current is used as the state variable. It is in fact a kind of input voltage feed forward control. This controller needs to be combined with other possible feedback to gain good output regulation as well.

References [45, 46] have examined the input voltage feed-forward in open-loop control. It is shown that input voltage feed-forward significantly decreases the influence of input voltage variations. The input audio-susceptibility is also reduced. However, the output characteristics are not changed.

OCC [47, 48] is a nonlinear approach to avoid the input voltage variations. It is shown below, that OCC is actually similar to the input voltage feedforward. An example of one-cycle controlled Buck converter is shown in Figure 1-11.

Figure 1-11 One-cycle controlled Buck converter

In OCC, the switch is turned off when the integration of the diode voltage reaches the reference value

$$\frac{1}{T} \int_0^{T_{ON}} v_D dt = V_{ref} \quad (1-10)$$

where T is the switching period and T_{ON} is the switch on period. The diode voltage is equal to input voltage V_{in} when switch is turned on. If the input voltage is constant, then (1-10) becomes

$$V_{in} \frac{T_{ON}}{T} = V_{ref} \quad (1-11)$$

This is the open-loop characteristic of a Buck converter. The OCC actually uses the diode voltage observer instead of the input voltage feed-forward. It can adjust the duty cycle in one switching period in case of the input voltage variations. However, like other input voltage feedforward controllers, it can not enhance the converter output performance. If a step change occurs in the input voltage, the duty cycle quickly changes to a new value.

The output performance is the same as the open-loop response, which is not satisfactory in most cases. In addition, the OCC is not globally stable for more complex converters. Then in [49], necessary modification is proposed to limit of the duty cycle and ensure the stability of Cúk converter. Reference [50] has examined the possibility of applying the OCC on other types of dc-dc converters. To enhance the output characteristic of OCC, reference [51] has used a direct reference voltage with a PI controller, whose input is the error between the output voltage and the reference voltage. Similar research results can also be found in [52]. The resulted closed-loop systems can achieve better response than the original OCC in case of load variations.

❖ Fuzzy logic control

As the performance of traditional linear control based on the small-signal model is influenced by the variation of operating point, nonlinear PI controller can be designed to incorporate such changes. Reference [53] addressed a nonlinear PI controller designed based on the extended linearization theory. This, in structure, is similar to a nonlinear PI controller based on fuzzy logic theory.

FLC [54] has also been widely used to design such nonlinear controllers. Reference [55] fuzzifies the error and differential of the error of the output voltage and the Sugeno fuzzy system gives out the change in duty ratio. Reference [56] has proposed a practical implementation of a Mamdani type fuzzy controller with micro-processor. Reference [57] also used a very similar Mamdani system. For these methods, the changes of duty ratio are directly determined by the de-fuzzifying the output of the controller. Reference [58] summarized the advantages of such fuzzy controller over the traditional PI controller in control of the Boost converter.

Reference [59] has proposed another type of fuzzy PI controller for Cúk converter. The input of the fuzzy controller is the error and change rate of the output voltage error. The coefficients of the proportional and integral gains are the result of the fuzzy controller. Alternatively, in [60], it has been proposed using the error of both the output voltage and the input inductor current as the fuzzy base.

It is shown that the fuzzier and de-fuzzier are generally needed to implement a fuzzy controller. Micro-processors or other digital storage devices are therefore needed to implement such complex computation. The analog implementation of a fuzzy logic controller for the Boost converter has been reported in [61] .

❖ Current-mode control

Much attention has also been paid to the current-mode control [1, 11, 62-64]. By indirectly regulating the input inductor current, it is possible to control the output voltage to a desired level. The reference current can be calculated from the reference voltage and load. The passivity approach can be used to get the current reference as well [65].

Simple current-mode control often suffers from the steady-state error caused by the parameter uncertainties. In addition, it has been pointed out that its capability in shaping the tracking response of output voltage is unacceptable. Output voltage feedback and compensator are therefore needed to generate the reference current, which results in a so-called multi-loop control scheme as shown in Figure 1-12 [1, 66].

Figure 1-12 Current-mode controlled Buck converter

It is found in Figure 1-12 that a clock signal is needed in order to maintain a finite switching frequency. At the beginning of each switch period, the switch is turned on. When the inductor current is larger than the reference current, the switch is turned off. Normally, only one switch change is permitted in each switch cycle and then the switch frequency is determined by the input clock signal. Under such a case, an oscillation or

unstable behavior may occur when the corresponding duty cycle is larger than 0.5. This issue has been well studied [1] and it is found that additional ramp compensation should be added to avoid such unstable behavior. The sensor information of the current-mode control can also be used to protect the switch from over-current.

One advantage of current-mode control is its simple dynamic. As the dynamic response of the inner current loop is much faster than the outer voltage loop, the control scheme can be viewed as a proportional block. Then, the small-signal control-to-output transfer function is equal to the transfer function from the input inductor current to the output voltage, which is a first order one in case of a Buck converter. The disadvantage of current-mode control is that it can be affected by the noise of the input inductor current, which can cause fault switch action. The PI compensator used in the current mode control may also bring some problems, which will be discussed in detail in the review of sliding mode control.

❖ Sliding mode control

Current-mode control is a typical type of SM control. In current-mode control, the sliding surface is the straight line where the current reference is constant. The SM control theory was firstly proposed in 1970's [67, 68] for variable structure systems and it is also a kind of variable structure control (VSC). The most distinguished feature of VSC is that it can achieve robust control system. Currently, VSC is also applied in a wide range [69-74]. Dc-dc converters are also one kind of variable structure systems due to their switch properties. SM control has been widely applied to such systems since 1980's [75].

The basic idea of SM control can be explained using Buck converter as an example. The phase portraits of Buck converter during switch on and off are shown in Figure 1-13. The solid lines are the phase portrait of Buck converter during switch on, and the dotted lines are the phase portrait during switch off. The axes are the error item of the capacitor voltage and the inductor current corresponding to their operating points. A sliding surface is often defined as

$$\sigma(X, t) = 0 \quad (1-12)$$

The sliding surface divides the whole state plane into two separated parts, which are corresponding to the two switch positions: ON and OFF. The system operating state can often be represented as a point in the state space, which is called Representing Point (RP) in this thesis. The state trajectory of Buck converter is then decided according to the system RP's position in the state plane. The sliding surface can be selected to achieve different control objectives. There are normally three phases of system motion under sliding mode control: reach phase, sliding mode and steady state. Figure 1-14 shows the start-up performance of Buck converter using the sliding mode control.

Figure 1-13 Buck converter phase portraits under sliding mode control

Figure 1-14 Buck converter's start-up performance under sliding mode control

If the switching frequency is infinite, the system can be kept on the sliding surface. However it can not be achieved in reality and a hysteresis is used in practice to limit the

switching frequency. The system RP will slide across the sliding surface repeatedly, which is called the system in sliding mode.

The analysis of sliding mode control includes examination of three conditions: the reaching condition, existence condition and characteristics in sliding mode [74, 76]. The first two conditions can be examined using derivative of system equations. When in sliding mode, the system performance is guaranteed by the sliding surface. Five methods have been proposed to analyze the system performance under sliding mode [69]. All of them describe how to derive differential equation of system under sliding mode.

It has been proven that the sliding mode control has several advantages:

- a) By forcing the system to stay on the sliding surface, a better dynamic response can be achieved.
- b) The system is less sensitive to parameter variations. It can ensure stability even under large parameter changes.
- c) By choosing a second-order sliding surface, sliding mode control can achieve first-order response. This second order sliding surface can be readily applied to higher-order systems, which greatly simplifies the implementation of the controllers.

A lot of papers have been published on applying the sliding mode control to dc-dc converters. Reference [77] has examined the stabilization of the lossless switched power electronic circuits, whose states evolve on a generalized sphere. The theory background is constructed in this paper for the use of sliding mode control to govern the system's transition from one state configuration to another in the state plane. In [78], the author has used the geometric approach to analyze the stabilization of such system.

In [75], the error of inductor current and capacitor voltage on their operating point has been used to define the sliding surface. The authors of [36] have proposed the exact linearization technique in state transformation to obtain new state variables. Reference [79] proposed the extended linearization. Reference [38] has addressed a nonlinear state transformation method. All these methods require additional computations. The design

procedure is therefore complicated and the global stability of the controllers can not be guaranteed because of state transformation.

Using the original state variables such as the inductor current and the capacitor voltage has been given much attention. The sliding surface with only output voltage is applicable for Buck converter. For other dc-dc converters, additional variables are needed. Authors of [80-82] have analyzed various sliding surfaces, which include one, two or three state variables for a simplified Cúk converter under ideal condition. It is then suggested that more state variables can offer more flexibility and more complexity at the same time, to design controller. Using only one state variable such as the input inductor current can also control dc-dc converters, which has been explained in [40, 76] from the energy point of view. A sliding mode controller has also been reported in [40, 76], which only used the inductor current as the state variable. The stability of the controller is proven through the direct Lyapunov method.

The dynamic performance of a sliding mode controller with inductor current feedback is satisfactory under ideal conditions. In case of parameter uncertainties, additional information is needed. Generally, the output voltage can be sensed to eliminate the steady state error, which is similar to using a PI compensator in the output voltage loop of the current-mode control.

There are other versions of sliding mode controllers which use two variables. References [75, 83] have proposed to use the output voltage and its derivative, the output capacitor current, to implement the sliding surface. In references [84, 85], high-pass filter is used to get the error signal of the input inductor current, while the error of output voltage is obtained by subtracting output voltage from the reference voltage. Therefore, the reference current is not needed. The approach simplifies the design process and the controller is also insensitive to parameter variations. Reference [86] has analyzed such controller using the small signal method. Figure 1-15 shows the configuration of the sliding mode controller which uses one current and one voltage sensors.

To obtain the switch signal according to the sliding function value, a sign function is introduced

$$s(x) = 0.5(1 + \text{sign}(x)) = \begin{cases} 0 & \text{when } x < 0 \\ 1 & \text{when } x > 0 \end{cases} \quad (1-13)$$

Figure 1-15 Buck converter controlled by SM controller with two state variables feedback

Under such case, a clock signal is needed to stabilize and limit the switching frequency. There are five methods of implementing the switching function as [87]:

- a) **Hysteresis:** A symmetrical or asymmetrical neighborhood of the sliding surface is established. When in the neighborhood, the switching function is kept unchanged. The switching function regulates its output according to the direction when the sliding function goes outside of the neighborhood. The width of the neighborhood determines the switching frequency.
- b) **Constant sampling frequency:** The sliding function is captured at constant time instants, and the switch position changes can only be made at the sampled time instant.
- c) **Constant on Time:** Every time the switch is turned on, it will be kept for a constant time period. Then the switching function checks the sliding function and decides when to turn off the switch.
- d) **Constant switching frequency:** The switch off action can only happen at time instants kT_{SW} when the sliding function is less than zero. T_{SW} determines the desired switching frequency.

- e) **Limited maximum switching frequency:** Either switch states will take place at least for a period T_M .

Only methods (a) and (b) can obtain nearly constant switching frequency at steady state. However, in case of parameter changes, the switching frequency will change as well. This is a disadvantage of sliding mode control. Therefore many approaches have been reported in order to limit the switching frequency.

One method is to encode the ramp signal into the discontinuous switching function of the controller [85]. The advantage of this method is that it is straightforward and simple to implement. However, this comes at an expense of additional hardware circuitries, as well as deteriorated transient response caused by the superposition of the ramp function upon the switching function.

Adaptive hysteresis band control has been proposed in [88], which can adjust the hysteresis band according to different parameter variations. However, such a band is sensitive to the inductance and input voltage. In case of a too large or too small band, the control performance will deteriorate and it is also not easy for implementation in practice.

The authors of [59] proposed a sliding mode like controller designed for Buck converter. The error of output voltage and its derivative are used as the input of a fuzzy based controller. The output of the fuzzy controller is incremental value of the duty cycle. By implementing hard-band saturation on the incremental value, the duty cycle is limited between 0 and 1. Therefore, a constant switching frequency can be achieved. However, the controller often needs excessive duty cycle in order to achieve the desired performance. Because the duty cycle is hard limited, the actual control performance is always worse than predicted.

The authors of references [88-90] tried to use the concept of equivalent control of sliding mode control. Only output voltage feedback is used in these controllers. Unfortunately, only control output in discrete manner was presented. The switching frequency will also change during transients.

An equivalent control scheme for Buck converter is shown in Figure 1-16. The advantage of this method is that there is no need of additional hardware circuitries since the switching function is replaced by the PWM modulator and the transient response is not deteriorated. The drawback is that the computations to obtain the equivalent control input are very complicated. This method will be analyzed in details in this thesis to show that the above drawbacks can be overcome by choosing adequate sliding surface and combining with other control approaches.

Figure 1-16 Equivalent control version of sliding mode controlled Buck converter

Another type of equivalent control methods is presented in [91]. The sliding surface only includes the output voltage and the converging rate is defined as the control objective shown in (1-14).

$$\begin{aligned}\sigma &= v_o - v_r \\ \dot{\sigma} &= -\lambda(v_o - v_r)\end{aligned}\tag{1-14}$$

λ is the coefficient, which controls the converging rate of the output voltage. The advantage of this method is that the equivalent control is only represented by the output voltage and reference input. During derivation of the equivalent control, other state variables are considered as constant. The disadvantage is that the output voltage response is also limited by the circuit parameters. It can not change as rapidly as that defined by the converging coefficient. Therefore, overshoot and long period oscillation exist in the output voltage response.

The method described above is actually a kind of typical synergetic control [93][93, 94]. In synergetic control theory, the first step is to define a macro-variable as function of the state variables.

$$\psi = \psi(x) \quad (1-15)$$

Then, it tries to get the control output by forcing the trajectory of the pre-defined function to follow

$$T\dot{\psi} + \psi = 0 \quad (1-16)$$

where T is the design parameter specifying the convergence speed to the manifold specified by $\psi = 0$. The control input can be solved using the state-space equation. The synergetic control can satisfy various requirements by defining a macro-variable, such as adding an integral part. However, it needs much more computations than the traditional sliding mode control. The performance is also not satisfactory due to the limitation of the circuit response speed and saturation problems.

The sliding functions described above are all of first order. In [95], it has been proposed to use a second order sliding function. The proposed switching surface can enhance the tangential velocity of the trajectories along the switching surface. The converter therefore exhibits better transient behaviors. However, computation task increases a lot. The sliding mode control technique has also been used for tracking AC reference voltages. The details can be found in [96-98].

❖ Sensorless current mode control

Traditional multi-loop controller uses two sensors. One is current sensor and the other is voltage sensor. In order to reduce the cost, it has been proposed to use a state-observer instead of the current sensor, which is called the sensorless current mode control (SCMC) [99]. Since the change rate of the inductor current is decided by its voltage, the inductor current can be obtained by sensing the inductor voltage. References [100][100, 101] have given the small signal analysis and application criteria for SCMC. It is found that typical transient errors exist in the output voltage waveform during input variations. Reference [102] uses a duty feedback scheme to solve such problems. Better audio-susceptibility is found in the revised version of SCMC scheme. Reference [103] has used the same technique but replacing the current item with its observer in the sliding surface.

❖ Adaptive control and other control methods

The normal two-variable sliding mode control is similar to the current mode control with PI compensator in the output voltage loop. The coefficients of PI compensator thus can be modified through a fuzzy based control, which has been proposed in [104]. This technique can be viewed as varying the sliding surface under different regions of the state space, which is similar to the idea of adaptive control. Reference [105] showed that fuzzy control can also be treated as sliding mode control with nonlinear adaptive sliding coefficients.

Adaptive control is a useful approach to control systems which have unknown or slowly-varying uncertain parameters [106]. The basic idea is to estimate the uncertain plant parameters (or, equivalently, the corresponding controller parameters) on-line based on the measured system signals. The estimated parameters are then used in the control input computation. Systems with varying control parameters can be viewed as adaptive controller. Since the loads of dc-dc power supplies are various, adaptive control can be used to estimate the unknown load impedance [65]. The global stability of such control scheme is also analyzed in this reference. The main advantage of this approach is that it can eliminate the steady state error of the output voltage.

Reference [107] has tried to adjust the control parameters and achieve satisfied dynamic performance under the input voltage variations. For the different input voltage, different pole-placement control coefficients are calculated and used to obtain the same dynamic response.

The authors of [108] have examined using the adaptive control for both the input voltage and load variations. A state plane with x axis as the load resistance and y axis as the input voltage is built. Grid-point theory has been used to divide the state plane into different pieces around the operating point. Then, according to the locations, different control parameters can be designed. PI controller has been chosen as an example in the paper to verify the effectiveness of the control scheme. Reference [109] has proposed an adaptive version of fuzzy logic controller. By using a scaling factor as a function of the duty cycle, the scheme can achieve the same dynamic performance under various operating points.

Reference [110] has considered the case where the output voltage should be adjustable while the load is unknown. Extended linearization and PI control scheme have been used in the paper. An adaptive version of sliding mode control is reported in [28] to achieve better dynamic performance under load variations. Through the load estimation and output voltage feedback, gain scheduling scheme [111, 112] has been used to determine the slope of the sliding line. It has been shown that the steady state error can be significantly reduced. However, the output voltage needs longer time to reach the desired level in case of step up change of the load resistance.

Reference [113] has proposed a controller design method based on the H^∞ control theory [114]. It is shown that the output impedance of the converter can be set as the direct design goal of the controller. The designed controller is the same order as that of the converter. Reference [115] has analyzed the advantages of such approach, for example, the output impedance and the audio-susceptibility. In [116], a similar nonlinear H^∞ controller has been proposed for Cúk converter.

The digital control scheme of dc-dc converters can be found in [117-120]. Most of them are using sliding mode control. Since there are parameter uncertainties and immeasurable parasitic effects in dc-dc converters, robust stability analysis has also been examined in [121, 122].

❖ Summary

In this section, many control methods have been reviewed. A summary can be given as follows. The linear control methods, although widely used, shall be replaced by advanced control scheme gradually because linear control methods can not cater with the increasing requirements driven by more and more applications of digital circuits. Nonlinear transformation methods are not applicable as the robustness can not be guaranteed. Fuzzy logic control is also not suitable in its current status. The design of such control scheme is complex and requires a lot of experience. The implementation of a fuzzy logic controller is also of higher cost. Further research in the fuzzy logic control is still needed.

Sliding mode control and current mode control will be possible direction for the near future as they can offer better performance and simple implementation. The problems of SM control mainly include variable switching frequency, non-zero steady state error, and sensitivity to noise because of the hysteresis control. The implementation of hysteresis control is also a little bit more expensive compared to current simple PWM based current mode control.

Other control methods such as input voltage feedforward, OCC, adaptive control and SCMC can actually be combined with other control schemes to improve the over all system performance.

1.3 Motivation

The studies on new topologies of dc-dc converters are to achieve various VTG, higher efficiency and more economical schemes [4]. By using voltage lift and super lift techniques, Luo converters [12-13, 15-17, 123] can offer high VTG, which is one of the highly desirable features for dc-dc converters. Luo converters had been proposed during the last few years. However in the current publications, only basic operation principles of Luo converters are available. Many of their properties are not examined so far, for example, the VLC effect on the converter VTG. In order to take the many advantages of Luo converters and also drive the practical application of Luo converters, this thesis chooses Luo converters as the research objective. A few topics on modeling and control of Luo converters are studied in the thesis.

Chapter 2 gives a detailed analysis of Luo converters operating characteristics in both CCM and DCM. The influence of VLC on the circuit overall performance is also examined in Chapter 2. The theoretical analysis provides the basic criterion for parameter selecting when designing Luo converters in practical applications. Dynamic models of Luo converters with VLC are also derived in Chapter 2. Based this model, dynamic characteristics of Luo converters are analyzed, which is valuable for designing closed-loop control scheme for Luo converters.

As stated in the previous section, the control techniques are critical for the application of dc-dc converters. The techniques suitable for Luo converters must be able to handle their intrinsic nonlinearity and high complexity and can ensure stability in any operating points while providing fast dynamic response. After examining the characteristics of Luo converters under both steady state and transient state, the closed loop control scheme for Luo converters is then designed. In Chapter 3, a new SM control scheme has been proposed for Luo converters. Among the various control schemes, SM Control shows many advantages: the ability to shape the response in the time domain and to maintain robustness in case of parameter uncertainties. There are also many problems associated with SM Control. For example, large current overshoot during start-up. This can be as high as 300% to 400% of its normal value for fourth-order Luo converters. Therefore, in Chapter 3, a new sliding surface is proposed to reduce the current overshoot during start up. For the proposed sliding surface, the system RP is right on the sliding surface when the converter starts up. Therefore the reaching time of the system response can be reduced and the current overshoot during start up is decreased accordingly.

Another disadvantage of SM Control is the varying switching frequency, which is undesirable as it causes a lot of trouble in filtering the electro-magnetic noise. Therefore in Chapter 4, an equivalent SM control scheme for Luo converters is proposed to achieve constant switching frequency. So far the equivalent control has been widely used for the analysis of SM controlled system dynamic performance. The equivalent control is of the same meaning of duty cycle, which provides the theoretical basis to use the equivalent control with tradition PWM technique.

However, the controller proposed in Chapter 4 show two disadvantages. Firstly, steady state error exists in the output voltage. Secondly, the cost of control circuit is high due to the use of divider IC. Chapter 5 therefore tries to provide improvements on the above two aspects. In order to remove the steady state error, an adaptive algorithm is proposed to integrate into equivalent SM controller. The adaptive part is able estimate the power losses under various operation conditions. In order to save the divider in the control circuit, an OCC method is combined into the proposed controller in Chapter 5.

1.4 Major Contributions of the Thesis

As a result of this research work, the following original contributions have been made:

1. Analysis of a family of Luo converters with voltage lift circuit: The influence of VLC on the overall performance of Luo converters is studied. It is found that VLC capacitance, switching frequency and load resistance can affect the VTG and the boundary between CCM and DCM. A VTG formula is therefore derived for Luo converters. The above-mentioned influences are all addressed using the proposed formula. Simulation and experimental results verify the prediction with this formula. The ripple approximation method is also applied to analysis Luo converters in DCM. As a result, modified formulas for calculating the filling efficiency and the boundary between CCM and DCM are derived. The formulas are also verified with simulation and experimental results. In addition, state-space model of POSLL converter in CCM is derived. Such a model is valuable in investigating its dynamic performance. The simulation results are given to verify the accuracy of the proposed model.
2. Analysis and design of a sliding mode controller for higher-order Luo converters: Higher-order Luo converters can achieve high VTG with less components and switches. SM control is suitable for control of high order dc-dc converters as stated in last section. However, a common existing issue for SM controlled dc-dc converters is the high current overshoot during start up. Traditional solution is to use a current-mode controller with PI compensator and slow down the dynamic response of the converters. In Chapter 3, a new sliding surface for the control of higher-order Luo converters is proposed. Such a scheme shows excellent start-up response and also good dynamic performance around the operating point. The rising speed of the output voltage is about two times of the natural oscillation duration of the output filter. The current overshoot during start-up is significantly decreased to an acceptable level. The steady state and dynamic performance of the new controller are also analyzed using the small-signal perturbation method in the frequency domain. Design procedure and considerations are also given for the application of such controllers. All the theoretical analysis is verified by simulation and experiment results.

3. Analysis of the equivalent SM controller for Luo converters: Variable switching frequency and high implementation cost are main issues for traditional SM controllers. An equivalent SM control with a constant-switching-frequency is therefore proposed in Chapter 4. The proposed controller uses the equivalent control input of SM control as a duty cycle signal. Its switching frequency is determined by the input clock signal, which can be kept constant under various operation conditions. Besides, the proposed control scheme can also retain the advantages of traditional SM control. Small-signal perturbation method is used to examine the dynamic response of the proposed controller. Based on the theoretical analysis results, the practical design procedure for the closed loop controller is investigated and the results are verified by simulation and experimental results. The proposed equivalent SM control is proven to be applicable for other dc-dc converters.

4. Improvements on equivalent SM control using adaptive control and OCC concept: In Chapter 4, Luo converters are modeled under idea condition. Power losses are ignored. Steady state error in the output voltage exists in the proposed equivalent SM control. In Chapter 5, an adaptive algorithm is designed for online estimation of the power losses and the steady state error can be removed. The proposed method is verified using a simple but representative Buck converter. Simulation and experimental results prove the feasibility and excellent performance of the proposed method. In Chapter 5, the OCC concept is also introduced into the equivalent SM control for the purpose of saving cost. With such a scheme, the high cost divider for deriving the desired duty cycle in the control circuit can be replaced by a voltage controlled saw-tooth waveform generator. It is also proven that the new method can provide same dynamic performance as the original equivalent SM control. Both improvements are then implemented on the POSLL converters. Simulation and experiment results are given to verify the theoretical analysis.

Much of the above contributions are also reported in the author's publications [1] – [5] listed on page 212.

1.5 Summary

In this chapter, brief introduction has been given to the current research status of dc-dc converters. A historic perspective has been given to the research works pertaining to the modeling and control of dc-dc converters. In this chapter, it is also attempted to classify the different control methods. The advantages and disadvantages of each method have been introduced at the best of our knowledge.

Through analyzing the current research work, several problems about the control scheme of dc-dc converters have been summarized, which are therefore the main research areas of this thesis. The major contributions of this thesis are also presented. In the following parts of the thesis, the main findings of this thesis are explained in detail. In next chapter, the focus is given to the steady state analysis of Luo converters.

Chapter 2 Analysis of Luo Converters with Voltage Lift Circuit

As pointed out in Chapter 1, Luo converters are the first generation of dc-dc converters. They have advantages such as high VTG and low ripple components both in current and voltage waveforms. Super-lift converters can be easily cascaded to gain even higher VTG, which increases in the power rate [16-17]. Currently, the research work of Luo converters is limited to their basic operations. For example, the authors of [12-13, 15] have analyzed the filling efficiency of Luo converters. However the analysis given in these references is not of high accuracy. Further study is thus needed for industry applications.

The core ideas of lifting voltage in series Luo converters are VL technique and SL technique. Among them, VLC is the main approach. Basic VLC includes a passive switch realized with a diode and a capacitor. For example, if a VLC including a diode and a capacitor is added to the POEL converter (Figure 1-3), the POSLL converter (Figure 1-5) can be obtained. The VLC increases its VTG from $dV_{in}/(1-d)$ to $V_{in}/(1-d)$.

However, in the pioneer analysis of these circuits, it is assumed that the capacitance is sufficiently large and the voltage variation of VLC capacitor can be ignored. Considering the capacitance in the analysis, it can be found that the VLC has various influences on the converter performance. It makes the VTG a function of the load resistance and the switching frequency. The boundary between CCM and DCM is also influenced by the VLC parameters. The circuit performance in DCM have been analyzed here in a different way from [4, 12-13], more accurate prediction can be obtained using the proposed approach.

In this chapter, the influences of VLC on the converter performance will be analyzed in detail. Luo converters with one VLC are analyzed firstly. Then Luo converters with two VLCs are examined. A general description of series Luo converters is given finally. In

each section, simulation and experiment results will be given to verify the theoretical analysis.

2.1 Luo Converters with one VLC

Luo converters with one VLC include POSLL converter, NOSLL converter and POSL converter. In this section, detailed analysis will be given to POSLL converter. A new method for calculating the filling efficiency is also given in this section. The theoretical analysis is verified with simulation and experimental results.

2.1.1 Positive Output Self-lift Luo Converter

The POSLL converter is shown in Figure 1-5. L_1 and L_2 have the same inductance. The VLC consists of a capacitor C_2 and a diode D_1 . Figure 2-1 shows the equivalent circuits of POSLL converter under various switching states.

2.1.1.1 Circuit analysis in CCM

Capacitor C_1 in POSLL converter is a pump capacitor. It transfers the energy from the inductor to the output port. The average voltage V_{C1} is equal to the output voltage V_O [13]. The pump capacitor C_1 is discharged by the current i_{L2} during switch-on period and charged by the current i_{L1} during switch-off period. The capacitor charge balance of capacitor C_1 is

$$\int_0^{dT} i_{L2} dt = \int_{dT}^T i_{L1} dt \quad (2-1)$$

Applying the charge balance on capacitor C_3 , it is obtained the average current I_{L2} is equal to the average output current I_O , and $I_O = V_O/R$. Thus, from (2-1), the average current through inductor L_1 is obtained as

$$I_{L1} = \frac{d}{1-d} I_O \quad (2-2)$$

Figure 2-1 Equivalent circuits of POSLL converter

In the VLC, the voltage v_{C2} across capacitor C_2 is equal to V_{in} soon after the switch is turned on. When the switch S is turned off, v_{C2} decreases while the current flows out from it. The waveform v_{C2} of in CCM is shown in Figure 2-2.

Figure 2-2 Voltage waveform with enlarged variation for VLC capacitor during CCM

The current flowing through the diode D_2 and the capacitor C_2 is the sum of i_{L1} and i_{L2} during switch-off period. Therefore, the average value of current i_{C2} during the switch-off period can be derived as

Chapter 2 Analysis of Luo Converters with Voltage Lift Circuit

$$I_{C2} \Big|_{t \in (dT, T)} = I_{L1} + I_{L2} = \frac{V_O}{R(1-d)} \quad (2-3)$$

Using (2-2), the voltage drop on the capacitor C_2 during the switch-off period is therefore given as

$$\Delta v_{C2} = \frac{1}{C_2} \int_{dT}^T i_{C2} dt = \frac{V_O}{RC_2 f} \quad (2-4)$$

During the switch-on period the voltage across inductor L_1 is V_{in} , and during the switch-off period, the voltage across L_1 is $v_{C1} - v_{C2}$. Using the inductor volt-second balance theory [2], it is obtained

$$\int_0^{dT} V_{in} dt + \int_{dT}^T (v_{C2} - v_{C1}) dt = 0 \quad (2-5)$$

The waveform of the capacitor voltage v_{C2} during the switch-off period can be approximated as a straight line. Considering (2-4), it is obtained

$$\int_{dT}^T v_{C2} dt = (V_{in} - \frac{V_O}{2RC_2 f})(1-d)T \quad (2-6)$$

Replacing the integration of v_{C1} in (2-5) with (2-6), and knowing that $V_{C1} = V_O$, it is found that the VTG of POSLL converter in CCM is

$$M_{POSLL} = \frac{V_O}{V_{in}} = \frac{1}{1 + \frac{1}{2RC_2 f}} \frac{1}{1-d} \quad (2-7)$$

The ideal VTG [13] is

$$\tilde{M}_{POSLL} = \frac{V_O}{V_{in}} = \frac{1}{1-d} \quad (2-8)$$

It is seen that the VTG in (2-7) decreases if either the load resistance (R), the capacitance (C_2) or the switching frequency (f) decreases. As the POSLL converter has only one VLC, the ratio between its ideal and real VTG values is then defined as the VLC coefficient λ_l , which is

$$\lambda_l = \frac{\tilde{M}_{POSLL}}{M_{POSLL}} = 1 + \frac{1}{2RC_2 f} \quad (2-9)$$

2.1.1.2 Circuit analysis in DCM

When the circuit operates in DCM, during switch-off period, the current flowing through the capacitor C_2 reaches zero at time t_1 before the next switch-on period. Three current waveforms of POSLL converter in DCM are shown in Figure 2-3.

Figure 2-3 Current waveforms with enlarged variations for POSLL converter in DCM

The filling efficiency ξ [13], $0 < \xi \leq 1$, can be defined as

$$\xi = \frac{t_1 - dT}{(1-d)T} \quad (2-10)$$

It means that after $\xi(1-d)T$ from switch-off instant, the current flowing through diode D_2 is zero and the equivalent circuit under this state is shown in Figure 2-1c. However, being in DCM does not mean the two inductor currents will also go to zero before next switch cycle begins. In other words, a residual current still flows through the two inductors in DCM after $\xi(1-d)T$. The average value of the current is named as I_r , which is reasonable to be assumed constant during the time period from $\xi(1-d)T$ to T because the capacitor voltages V_{C1} and V_{C3} are equal. If the direction of current i_{L2} is defined as positive, the current flowing through L_1 is then $-I_r$. Whether the inductor current i_{L1} will change direction during DCM is determined by the circuit parameters and the duty cycle.

As shown in Figure 2-3, the variations of current i_{L1} and i_{L2} are equal in DCM, which is $\Delta i = \Delta i_{L1} = \Delta i_{L2}$. This current variation can also be represented as

Chapter 2 Analysis of Luo Converters with Voltage Lift Circuit

$$\Delta i = \frac{dV_{in}}{L_1 f} \quad (2-11)$$

During the switch-on period, C_1 is discharged by the current i_{L2} . From dT to t_l , C_1 is charged by the current i_{L1} . From t_l till the switch is turned on again, the capacitor is discharged by the residual current I_r . Thus, the charge balance of pump capacitor C_1 leads to

$$-\int_0^{dT} i_{L2} dt + \int_{dT}^{t_l} i_{L1} dt - \int_{t_l}^T I_r dt = 0 \quad (2-12)$$

Based on the current waveforms shown in Figure 2-3, (2-12) can be solved as

$$I_r = \frac{\Delta i}{2} (\xi(1-d) - d) \quad (2-13)$$

To satisfy the charge balance of the output capacitor C_3 in DCM during one switching cycle, the average current of inductor L_2 should be also equal to the output current. Then,

$$\frac{1}{T} \int_0^T i_{L2} dt = I_o \quad (2-14)$$

(2-14) leads to

$$I_o = I_r + \frac{\Delta i}{2} (\xi(1-d) + d) \quad (2-15)$$

Combining (2-13) and (2-15), it is obtained

$$I_o = \Delta i \xi(1-d) \quad (2-16)$$

Replacing I_o by V_o/R and Δi by dTV_{in}/L , the first equation for VTG of POSLL converter in DCM can be obtained

$$\frac{V_o}{V_{in}} = \frac{Rd}{fL_1} \xi(1-d) \quad (2-17)$$

Figure 2-3 shows that the capacitor C_2 is discharged with the current $(i_{L2} + i_{L1})$ from time dT to t_l . Therefore, the variation of the capacitor voltage v_{C2} during the period from dT to $\xi(1-d)T$ is obtained as

$$\Delta v_{C2} = \int_{dT}^{t_l} (i_{L1} + i_{L2}) dt = \frac{V_o}{RC_2 f} \quad (2-18)$$

The waveform of the voltage v_{C2} in DCM is shown in Figure 2-4. It can be derived that the voltage variation of v_{C2} in DCM can also be given by (2-4).

Figure 2-4 Voltage waveform with enlarged variation for VLC capacitor during DCM

The voltage across L_1 is V_{in} during switch-on period. From the time the switch is turned off to the time t_1 , the voltage across L_1 is $v_{C2} - v_{C1}$. According to the volt-second balance of the inductor L_1 , it is derived that

$$\int_0^{dT} V_{in} dt + \int_{dT}^{t_1} (v_{C2} - v_{C1}) dt = 0 \quad (2-19)$$

Combining (2-18) and (2-19) and knowing that $V_{C1} = V_O$, the second equation for VTG of POSLL converter in DCM is then derived as

$$\frac{V_O}{V_{in}} = \frac{1}{\lambda_1} \left(1 + \frac{d}{\xi(1-d)} \right) \quad (2-20)$$

The VLC coefficient λ_1 in (2-20) is same as that shown in (2-9).

Define the normalized load as

$$Z_N = R / fL_1 \quad (2-21)$$

Considering (2-17) and (2-20), the filling efficiency ξ can be derived as

$$\xi = \frac{1 + \sqrt{1 + 4\lambda_1 d^2 Z_N}}{2\lambda_1 d(1-d)Z_N} \quad (2-22)$$

Though the filling efficiency ξ shown above has the same meaning as defined in [13], both the deriving method and result given in this chapter are different. Let $\xi = 1$, the boundary condition between the CCM and DCM is derived as

$$Z_N \lambda_1 d(1-d)^2 = 1 \quad (2-23)$$

In summary, the VTG of POSLL converter is shown as

$$M_{POSLL} = \begin{cases} \frac{1}{\lambda_1(1-d)} \cdots \cdots \cdots Z_N \lambda_1 d(1-d)^2 < 1 & \text{in CCM} \\ \frac{1}{\lambda_1(1+\frac{d}{\xi(1-d)})} \cdots \cdots \cdots Z_N \lambda_1 d(1-d)^2 \geq 1 & \text{in DCM} \end{cases} \quad (2-24)$$

The filling efficiency ξ can be solved from (2-22). It is shown that (2-9) is valid in DCM as well. If the VLC effects are negligible, which means $\lambda_I = 1$, (2-24) is then the same as that derived in [13].

It is also found from (2-23) that the least normalized load required for the POSLL converter to go into DCM occurs when $d = 0.33$. In order to show the VLC effects on the converter properties, the boundaries between CCM and DCM versus the normalized load is shown in Figure 2-5 under the condition that $d = 0.33$. The VTG versus normalized load is also shown in the figure. The dotted curves in the figure are drawn based on the condition: $\lambda_I = 1$. The solid curves are calculated under the condition $\lambda_I = 1.2$. It shows that the boundary between CCM and DCM moves left-down due to the VLC effect. The ratio of the ideal VTG over its real value is constant in CCM. However, this relation does not exist in DCM. The dots in Figure 2-5 are the experimental result of the VTG versus the normalized load when $\lambda_I = 1.2$. It shows that the practical VTG is smaller than the predicted value because the parasitic effect and un-ideal switches.

2.1.1.3 Simulation and experimental results

In the simulations and experiments, the circuit parameters are chosen as: $V_{in} = 20$ V, $L_1 = L_2 = 1$ mH, $C_2 = 2.2$ μ F, $C_1 = C_3 = 20$ μ F, $d = 0.3$, and $f = 20$ kHz. According to (2-21) and (2-23), it is known that when $R = 124.7\Omega$ the circuit is operated under the critical DCM, which means $\xi = 1$. From (2-9), it is obtained that $\lambda_I = 1.091$. Therefore, the output voltage can be derived from (2-24), which is $V_O = 26.2$ V. Figure 2-6 shows the simulation waveforms of the POSLL converter under the critical DCM condition. Figure 2-7 shows the simulation waveforms of the POSLL converter when load resistance is 200 Ω .

Figure 2-5 POSLL converter's boundary and VTG versus the normalized load

Dotted curves: ideal circuit without considering VLC effect and $\lambda_I = 1$
 Solid curves: considering VLC effect and $\lambda_I = 1.2$
 Dots: experimentally measured VTG normalized load at $d = 0.33$

Figure 2-6 Simulation waveforms of POSLL converter under critical DCM ($d = 0.3$ and $R = 124.7 \Omega$)

Figure 2-7 Simulation waveforms of POSLL converter under DCM ($d = 0.3$ and $R = 200 \, \Omega$)

In the experiments, the n-channel MOSFET is realized using 2SK2267 [124]. The drain-source ON resistance R_{ds-on} is $8 \, \text{m}\Omega$, which is near the ideal condition. The diodes D_1 and D_2 are realized using MBR6045WT [125], the forward voltage drop of them is $0.6 \, \text{V}$. Due to these non-ideal conditions; the measured output voltage in the experiment is smaller than the predicted value.

When $R = 22 \, \Omega$, the POSLL converter operates in CCM. The VLC coefficient is calculated as $\lambda_I = 1.517$, which also gives that $V_O = 18.8 \, \text{V}$ and $\Delta v_{C2} = 19.4 \, \text{V}$. Figure 2-8 and Figure 2-9 show the experimental results. In Figure 2-8, CH1 is the gate-source voltage of the MOSFET (v_{gs}) and CH2 is the output voltage v_O . It is seen that the practical value is smaller than the calculated one, which coincides with the previous analysis. Figure 2-9 shows waveforms of v_{C2} and i_{C2} at the same condition.

Theoretically, the capacitor voltage will increase very fast to the source voltage at the instance of switching on. However, considering the dynamical characteristic of the diode, the stray inductance and series resistance, the charging current of the capacitor C_2 cannot rise at infinite rate. In addition, as the capacitance is small, v_{C2} increases very fast to V_{in} , soon after which the current decreases. Thus, the maximum capacitor charging current is limited to a relatively small value. It is verified by Figure 2-8 where the maximum capacitor current is about $12 \, \text{A}$.

Figure 2-8 Waveforms of POSLL converter with $d=0.3$, $R=22\ \Omega$, (CH1: v_{gs} ; CH2: v_o)

Figure 2-9 Waveforms of POSLL converter with $d=0.3$, $R=22\ \Omega$, (CH1: v_{C2} ; CH2: i_{C2} [50 A/V])

When $R = 200\ \Omega$, POSLL converter operates in DCM. It can be calculated that: $\lambda_I = 1.057$; $\xi = 0.72$; $V_O = 30.2\text{ V}$; $\Delta v_{C2} = 3.4\text{ V}$. Figure 2-10 shows the waveforms of output voltage and the MOSFET gate-source voltage v_{gs} . Figure 2-11 shows waveforms of the VLC capacitor voltage v_{C2} and the VLC capacitor current i_{C2} . Due to the diode voltage drop, the capacitor voltage cannot be charged to the input voltage.

Figure 2-10 Waveforms of POSLL converter with $d=0.3$, $R = 200 \Omega$, (CH1: v_{gs} ; CH2: v_o)

Figure 2-11 Waveforms of POSLL converter with $d=0.3$, $R = 200 \Omega$, (CH1: v_{C2} ; CH2: i_{C2} [50 A/V])

2.1.2 Negative Output Self-lift Luo Converter

The NOSLL converter shown in Figure 2-12 is derived from the elementary circuit of negative output Luo converters [15]. The VLC in the NOSLL converter consists of capacitor C_1 and diode D_1 . Capacitor C_2 is the pump capacitor. The two inductors L_1 and L_2 are of the same inductance. Figure 2-13 shows the equivalent circuits of NOSLL converter under various switch states.

Figure 2-12 Negative output self-lift Luo converter

Figure 2-13 Equivalent circuits of NOSLL converter

2.1.2.1 Circuit analysis in CCM

Using similar analytical method as the one used in Section 2.1.1, the following equations can be obtained

$$I_{L2} = I_O \quad (2-25)$$

$$I_{L1} = \frac{1}{1-d} I_O \quad (2-26)$$

The voltage waveform of the capacitor C_1 is the same as the one shown in Figure 2-2. During switch off, only the current i_{L1} flows through it. Therefore, the variation of v_{C1} in CCM is

$$\Delta v_{C1} = \frac{1}{C_1} \int_{dT}^T i_{L1} dt = \frac{V_O}{RC_1 f} \quad (2-27)$$

According to the volt-second balance of L_1 , the VTG for NOSLL converter in CCM is

$$M_{NOSLL} = \frac{V_O}{V_{in}} = \frac{1}{\lambda_1} \frac{1}{1-k} \quad (2-28)$$

In (2-28), the VLC coefficient λ_1 of the NOSLL converter is the same as the one for POSLL converter as both circuits have only one VLC.

2.1.2.2 Circuit analysis in DCM

The DCM of NOSLL converter means that the inductor current i_{L1} reaches zero during the switch-off period before the next switch-on period. The time when i_{L1} reaches zero is defined as t_l and the filling efficiency ξ is same as defined in (2-10). Under DCM condition, the current waveforms of i_{L1} , i_{L2} and i_{C2} are shown in Figure 2-14.

The variation (peak to peak) of current i_{L1} is

$$\Delta i = \frac{dT V_{in}}{L_1} \quad (2-29)$$

According to the charge balance for pump capacitor C_2 , it is derived

$$\Delta i = \frac{2}{\xi(1-d)} \frac{V_O}{R} \quad (2-30)$$

Substituting (2-30) into (2-29), the first equation for VTG of NOSLL converter in DCM can be derived as

$$\frac{V_O}{V_{in}} = \frac{\xi R d (1-d)}{2 f L_1} \quad (2-31)$$

Figure 2-14 Current waveforms with enlarged variations for NOSLL converter in DCM

The waveform of the capacitor voltage v_{C1} in DCM is the same as the one shown in Figure 2-4. The variation of v_{C1} can also be obtained and it is the same as that derived in (2-27).

According to the volt-second balance of the inductor L_1 , and using the same approximation method for integration of v_{C1} and knowing that $V_{C2} = V_O$, the second equation for VTG of NOSLL converter in DCM is derived as

$$\frac{V_O}{V_{in}} = \frac{1}{\lambda_1} \left(1 + \frac{d}{\xi(1-d)} \right) \quad (2-32)$$

The VLC coefficient is the same as that shown in equation (2-9).

The normalized load Z_N for the NOSLL converter is defined the same as in (2-21). Combining (2-31) and (2-32), the filling efficiency ξ can be derived

$$\xi = \frac{1 + \sqrt{1 + 2\lambda_1 Z_N d^2}}{\lambda_1 Z_N d(1-d)} \quad (2-33)$$

Let $\xi=1$, the boundary condition between CCM and DCM is derived as

$$\lambda_1 Z_N d(1-d)^2 = 2 \quad (2-34)$$

In summary, the VTG of NOSLL converter is

$$M_{NOSLL} = \begin{cases} \frac{1}{\lambda_1(1-d)} \dots\dots\dots Z_N \lambda_1 d(1-d)^2 < 2 & \text{in CCM} \\ \frac{1}{\lambda_1(1+\frac{d}{\xi(1-d)})} \dots\dots\dots Z_N \lambda_1 d(1-d)^2 \geq 2 & \text{in DCM} \end{cases} \quad (2-35)$$

The parameters in (2-35) are the same as those in (2-24), except that the filling efficiency ξ is defined by (2-33). If $\lambda_I = 1$, (2-35) is the same as the one given in reference [15].

Equation (2-34) shows that when $d = 0.33$, NOSLL converter goes into DCM with the least Z_N . The same as POSLL converter, the comparison on the VTGs of the NOSLL converter with and without the VLC effects is shown in Figure 2-15. The dotted lines are calculated based on the condition $\lambda_I = 1$ and the solid curves are drawn when $\lambda_I = 1.2$. The dots in Figure 2-15 are the experimental measurements of VTG versus the normalized load.

2.1.2.3 Simulation and experimental results

The circuit parameters for simulations and experiments are given as $V_{in} = 20$ V, $L_1 = L_2 = 1$ mH, $C_1 = 2.2$ μ F, $C_2 = C_3 = 20$ μ F, $d = 0.3$ and $f = 20$ kHz. From (2-34), it is known that when $R = 260.7$ Ω the circuit is under the critical DCM condition. $\lambda_I = 1.2$ and $V_O = 27.4$ V can be obtained. Figure 2-16 shows the simulation waveforms of the NOSLL converter under the critical DCM condition.

Figure 2-15 NOSLL converter's boundary and VTG versus the normalized load

Dotted curves: ideal circuit without considering VLC effect and $\lambda_I = 1$
 Solid curves: considering VLC effect and $\lambda_I = 1.2$
 Dots: experimentally measured VTG versus normalized load at $d = 0.33$

Figure 2-16 Simulation waveforms of NOSLL converter under critical DCM ($d = 0.3$ and $R = 260.7 \Omega$)

In the experiments, the MOSFET and diodes are the same as those used in the POSLL converter. When $R = 22 \Omega$, the circuit operates in CCM. It can be obtained that: $\lambda_I = 1.517$; $V_o = 18.8 \text{ V}$ and $\Delta v_{CI} = 19.4 \text{ V}$. Figure 2-17 shows the waveforms of v_{gs} and output voltage. Figure 2-18 shows the waveforms of v_{gs} and the VLC capacitor voltage v_{CI} .

Figure 2-17 Waveforms of NOSLL converter with $d=0.3$, $R=22\ \Omega$, (CH1: v_{gs} ; CH2: v_o)

Figure 2-18 Waveforms of NOSLL converter with $d=0.3$, $R=22\ \Omega$, (CH1: v_{gs} ; CH2: v_{cl})

When $R = 300\ \Omega$, the circuit operates in DCM condition. It can be calculated that $\lambda_1=1.038$; $\xi = 0.90$; $V_o = 28.4\text{ V}$; $\Delta v_{cl} = 2.15\text{ V}$. The experimental waveforms v_{gs} and the output voltage are given in Figure 2-19. The waveforms of the VLC capacitor voltage v_{cl} and v_{gs} are shown in Figure 2-20.

Figure 2-19 Waveforms of NOSLL converter with $d=0.3$, $R = 300 \Omega$, (CH1: v_{gs} ; CH2: v_o)

Figure 2-20 Waveforms of NOSLL converter with $d=0.3$, $R = 300 \Omega$, (CH1: v_{gs} ; CH2: v_{cl})

2.1.3 Positive Output Super-Lift Converter

Positive output super-lift (POSL) converter [16] is a newly derived DC-DC converter, which is shown in Figure 1-7. The converter has one VLC, which includes the diode D_1 and the capacitor C_1 . Figure 2-21 shows the equivalent circuits of NOSLL converter under various switch conditions.

Chapter 2 Analysis of Luo Converters with Voltage Lift Circuit

2.1.3.1 Circuit analysis in CCM

During switch-on period, the voltage v_{C1} across C_1 increases to V_{in} in a short duration. At this moment the diode D_2 will be blocked and $i_{D2} = 0$. During switch-off period, the inductor current i_{L1} flows through C_1 and D_2 and to the output port.

Figure 2-21 Equivalent circuits of POSL converter

According to the charge balance of the output capacitor C_2 , it should satisfy

$$I_{L1} = \frac{1}{1-d} I_O \quad (2-36)$$

The voltage variation of the VLC capacitor C_1 can be obtained as

$$\Delta v_{C1} = \frac{1}{C_1} \int_{dT}^T i_{L1} dt \Rightarrow \Delta v_{C1} = \frac{V_O}{RC_1 f} \quad (2-37)$$

The VTG of POSL converter in CCM can be obtained as

$$M_{POS L} = \frac{1}{\lambda_1} \frac{2-d}{1-d} \quad (2-38)$$

where λ_1 is the same as the one defined in (2-9) except that C_2 is replaced by C_1 .

2.1.3.2 Circuit analysis in DCM

POSL converter operates in DCM means that the current i_{L1} reaches zero during switch-off period before the next period begins. The time t_1 is defined as the time when the current i_{L1} reaches zero and the filling efficiency ξ is defined the same as that shown in (2-10). The current waveforms of i_{L1} , i_O and i_{D2} in DCM are drawn in Figure 2-22.

Figure 2-22 Current waveforms with enlarged variations for POSL converter in DCM

According to the capacitor charge balance of C_2 , it should satisfy

$$\Delta i_{L1} = \frac{2}{\xi(1-d)} I_O \quad (2-39)$$

The variation of the inductor current i_{L1} is also known from the input side as

$$\Delta i_{L1} = \frac{dV_{in}}{L_1 f} \quad (2-40)$$

Substituting (2-40) into (2-39), the first equation for VTG of POSL converter in DCM is obtained

$$\frac{V_O}{V_{in}} = \frac{R\xi d(1-d)}{2fL_1} \quad (2-41)$$

Chapter 2 Analysis of Luo Converters with Voltage Lift Circuit

The waveform of the capacitor voltage v_{CI} in DCM is the same as that shown in Figure 2-4. According to the volt-second balance of the inductor L_1 in DCM, the second equation for VTG of POSL converter during DCM is obtained as

$$\frac{V_O}{V_{in}} = \frac{1}{\lambda_1} \left(2 + \frac{d}{\xi(1-d)} \right) \quad (2-42)$$

Define the normalized load for POSL converter as

$$Z_N = \frac{R}{fL_1} \quad (2-43)$$

Combining (2-41) and (2-42), it is obtained

$$\xi = \frac{2 + \sqrt{4 + 2\lambda_1 Z_N d^2}}{\lambda_1 Z_N d(1-d)} \quad (2-44)$$

The boundary between CCM and DCM for POSL converter is

$$\frac{\lambda_1 Z_N d(1-d)^2}{2(2-d)} = 1 \quad (2-45)$$

The VTG of POSL converter can be summarized as

$$M_{POSL} = \begin{cases} \frac{2-d}{\lambda_1(1-d)} \dots \dots \dots \frac{Z_N \lambda_1 d(1-d)^2}{2(2-d)} < 1 & \text{in CCM} \\ \frac{1}{\lambda_1} \left(2 + \frac{d}{\xi(1-d)} \right) \dots \dots \dots \frac{Z_N \lambda_1 d(1-d)^2}{2(2-d)} \geq 1 & \text{in DCM} \end{cases} \quad (2-46)$$

When $d = 0.38$, POSL converter requires the least value of Z_N to reach DCM. Figure 2-23 shows the VLC effects on the VTG and the boundary between CCM and DCM of POSL converter. In the figure, all curves are drawn with $d = 0.38$. Two dotted curves show the VTG and the boundary between CCM and DCM versus Z_N without VLC effects. Two solid curves are the VTG and the boundary between CCM and DCM with $\lambda_l = 1.2$. The dots in Figure 2-23 are the experimental results of VTG versus the normalized Z_N .

Figure 2-23 POSL converter's boundary and VTG versus the normalized load

Dotted curves: ideal circuit without considering VLC effect and $\lambda_I = 1$
 Solid curves: considering VLC effect and $\lambda_I = 1.2$
 Dots: experimentally measured VTG versus normalized load at $d = 0.38$

2.1.3.3 Simulation and experimental results

The circuit parameters used in simulation and experiment are given as below: $V_{in} = 20$ V, $L_1 = 1$ mH, $C_1 = 2.2$ μ F, $C_2 = 20$ μ F, $d = 0.3$ and $f = 20$ kHz. It is obtained that the circuit is under critical DCM with $R = 451.2$ Ω , which means: $\lambda_I = 1.025$; $V_O = 47.4$ V. Figure 2-24 shows the simulation waveforms of POSL converter operated under critical DCM.

Figure 2-24 Simulation waveforms of POSL converter under critical DCM ($d = 0.3$ and $R = 451.2$ Ω)

Chapter 2 Analysis of Luo Converters with Voltage Lift Circuit

In the experiments, the MOSFET and diodes used are the same as those used in POSLL converter. When $R = 22\ \Omega$, POSL converter operates in CCM. The critical parameters can be obtained as $\lambda_1 = 1.517$; $v_o = 32.0\text{ V}$; $\Delta v_{C1} = 33\text{ V}$. Figure 2-25 shows the waveforms of v_{gs} and the output voltage. Figure 2-26 shows the waveforms of v_{gs} and the VLC capacitor voltage v_{C1} .

Figure 2-25 Waveforms of POSL converter with $d=0.3$, $R = 22\ \Omega$, (CH1: v_{gs} ; CH2: v_o)

Figure 2-26 Waveforms of POSL converter with $d=0.3$, $R = 22\ \Omega$, (CH1: v_{gs} ; CH2: v_{C1})

When $R = 500\Omega$, the circuit enters DCM. Key parameters are obtained as $\lambda_1 = 1.023$; $\xi = 0.92$; $V_o = 48.2\text{ V}$; $\Delta v_{C1} = 2.2\text{ V}$. Figure 2-27 shows the experimental waveforms of v_{gs} and the output voltage. Figure 2-28 shows the experimental waveforms of v_{gs} and v_{C1} .

Figure 2-27 Waveforms of POSL converter with $d=0.3$, $R = 500 \Omega$, (CH1: v_{gs} ; CH2: v_o) Figure 2-28 Waveforms of POSL converter with $d=0.3$, $R = 500 \Omega$, (CH1: v_{gs} ; CH2: v_{cl})

2.2 Luo Converters with Two VLCs

Three converters have been examined in Section 2.1. Each converter includes one VLC. It is also found that the VLC effects on the VTGs of those converters can be described with the same equation. In this section, positive output re-lift Luo (PORLL) converter [12, 13] with two VLCs will be analyzed.

PORLL converter is shown in Figure 1-6. The PORLL converter has two switches S and $S1$ which are turned on and off at the same time. Two capacitors, C_1 and C_2 , are of the same capacitance. Selection of inductance will be discussed later. The equivalent circuits of PORLL converter during switch-on and switch-off periods are shown in Figures 2-29a and 2-29b. Figure 2-29c shows the equivalent circuit of the converter in DCM.

Figure 2-29 Equivalent circuits of PORLL converter

2.2.1 Circuit Analysis in CCM

During switch-on period, the voltages across the two inductors L_1 and L_3 are equal to V_{in} . Capacitors C_2 and C_3 are charged rapidly to the source voltage V_{in} . The average value of the voltage across the inductor L_3 is also equal to V_{in} during this period.

$$\begin{cases} i_{L1}(dT) = i_{L1}(0) + \frac{dT V_{in}}{L_1} \\ i_{L2}(dT) = i_{L2}(0) + \frac{dT V_{in}}{L_2} \\ i_{L3}(dT) = i_{L3}(0) + \frac{dT V_{in}}{L_3} \end{cases} \quad (2-47)$$

According to Figure 2-29b, i_{L1} and i_{L3} flow through inductor L_2 after both switches are turned off. As the inductor current i_{L2} can not be changed discontinuously, the current difference between $i_{L2}(dT)$ and $i_{L1}(dT) + i_{L3}(dT)$ should flow through the diode D_2 until the difference is zero. If $i_{L2}(dT)$ is smaller than $i_{L1}(dT) + i_{L3}(dT)$, the circuit changes to another working state as shown in Figure 2-30.

Figure 2-30 The extra operating state of PORLL converter

To avoid this problem, it should be maintained that

$$i_{L2}(dT) = i_{L1}(dT) + i_{L3}(dT) \quad (2-48)$$

Combining (2-47) and (2-48) leads to

$$L_2 = L_1 // L_3 = \frac{L_1 L_3}{L_1 + L_3} \quad (2-49)$$

In order to avoid the phenomena that D_2 can not be turned off during switch-off period, (2-49) should be satisfied when a PORLL converter is designed. The normalized inductance L is defined to be equal to L_2 for PORLL converter. Normally, L_1 is chosen equal to L_3 and therefore $L = L_2 = 0.5L_1$.

The charge balance of the output capacitor C_4 shows that $I_{L3} = I_o$. During switch-on period, the capacitor C_1 is discharged with the current i_{L3} and charged with the current i_{L1} during switch-off period. For the charge balance of the pump capacitor C_1 , it can be derived that

$$I_{L1} = \frac{d}{1-d} I_o \quad (2-50)$$

$$I_{L2} = \frac{1}{1-d} I_o \quad (2-51)$$

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During switch-off period, capacitors C_2 and C_3 are discharged with the current i_{L2} . The waveforms of v_{C2} and v_{C3} are the same as that shown in Figure 2-2. The variations of the capacitor voltage can be obtained with the same approximation method mentioned in Section 2.1.1.

$$\Delta v_{C2} = \Delta v_{C3} = \Delta v = \frac{1}{C_2} \int_{dT}^T i_{L2} dt = \frac{V_O}{RC_2 f} \quad (2-52)$$

From Figure 2-28b, it can be obtained that in CCM from the time dT to T ,

$$V_{L1-off} \Big|_{t \in [dT, T]} = V_{L3-off} \Big|_{t \in [dT, T]} \quad (2-53)$$

or

$$L_1 \frac{di_{L1}}{dt} = L_3 \frac{di_{L3}}{dt} \quad (2-54)$$

In addition, the derivative of the current i_{L2} is sum of the derivatives of current i_{L1} and i_{L3} . Thus, the voltage across L_2 can be expressed as

$$\begin{aligned} L_2 \frac{di_{L2}}{dt} &= \frac{L_1 L_3}{L_1 + L_3} \left(\frac{di_{L1}}{dt} + \frac{di_{L3}}{dt} \right) \\ &= \frac{L_3}{L_1 + L_3} L_1 \frac{di_{L1}}{dt} + \frac{L_1}{L_1 + L_3} L_3 \frac{di_{L3}}{dt} \\ &= L_1 \frac{di_{L1}}{dt} = L_3 \frac{di_{L3}}{dt} \end{aligned} \quad (2-55)$$

Combining (2-54) and (2-55) leads to that the voltages across three inductors during switch-off period are the same. Thus, from time dT to T ,

$$V_{L1-off} \Big|_{t \in [dT, T]} = V_{L2-off} \Big|_{t \in [dT, T]} = 0.5(V_O - V_{C2} - V_{C3}) \Big|_{t \in [dT, T]} \quad (2-56)$$

According to the volt-second balance of inductor L_1 , it is derived from (2-56) that

$$V_{in} dT + 0.5 \int_{dT}^T (v_{C2} + v_{C3} - v_O) dt = 0 \quad (2-57)$$

which leads to

$$M_{PORLL} = \frac{V_O}{V_{in}} = \frac{1}{\lambda_2} \frac{2}{1-d} \quad (2-58)$$

As PORLL converter contains two voltage lift circuits, the VLC coefficient is therefore defined as λ_2 which is shown in (2-59).

$$\lambda_2 = 1 + \frac{1}{RC_2 f} \quad (2-59)$$

2.2.2 Circuit Analysis in DCM

PORLL converter operating in DCM means that the current flowing through the diode D_3 reaches zero before next switch-on period. Define t_l as the time when i_{D3} reaches zero. The filling efficiency ξ can be derived and it is the same as the one given in (2-10). The current waveforms of i_{L1} , i_{L2} and i_{L3} are drawn in Figure 2-31, where I_r is the residual current.

The variations of inductor currents can be solved as

$$2\Delta i_{L1} = 2\Delta i_{L3} = \Delta i_{L2} = \frac{V_{in} dT}{L} \quad (2-60)$$

Considering $I_{L3} = I_O$, it is obtained

$$I_O = I_r + \frac{\xi(1-d) + d}{2} \Delta i_{L1} \quad (2-61)$$

In DCM, during switch-on period, the capacitor C_1 is discharged by i_{L3} . During switch-off period, the capacitor C_1 is charged by i_{L1} till the diode current i_{D3} reaches zero. Then C_1 is discharged by the residual current I_r . According to the charge balance of capacitor C_1 , it can be obtained as

$$-\int_0^{dT} i_{L3} dt + \int_{dT}^{t_l} i_{L1} dt - \int_{t_l}^T I_r dt = 0 \quad (2-62)$$

or

$$I_r = \frac{\xi(1-d)}{2} \Delta i_{L3} - \frac{d}{2} \Delta i_{L1} \quad (2-63)$$

Substituting (2-63) into (2-61) leads to

$$I_O = \frac{\xi(1-d)}{2} \Delta i_{L2} \quad (2-64)$$

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Knowing that $I_o = V_o / R$, (2-64) leads to the first equation for VTG of the PORLL converter under DCM condition.

$$\frac{V_o}{V_{in}} = \frac{R\xi d(1-d)}{fL} \quad (2-65)$$

Figure 2-31 Current waveforms with enlarged variations for PORLL converter under DCM

In DCM condition, the voltage variations of the capacitor C_1 and C_2 is derived as

$$\Delta v = \Delta v_{C2} = \Delta v_{C3} = \frac{1}{C_2} \int_{dT}^{t_1} i_{L2} dt = \frac{V_o}{RC_2 f} \quad (2-66)$$

As (2-56) is also valid during switch-off period before the current i_{D3} reaches zero, the volt-second balance of the inductor L_1 leads to

$$\begin{aligned} dTV_{in} + \frac{1}{2} \int_{dT}^{t_1} (v_{C2} + v_{C3} - v_o) dt &= 0 \\ \Rightarrow \frac{V_o}{V_{in}} &= \frac{1}{\lambda_2} \left(\frac{2d}{\xi(1-d)} + 2 \right) \end{aligned} \quad (2-67)$$

Define the normalized load for PORLL converter as

$$Z_N = \frac{R}{fL} \quad (2-68)$$

The filling efficiency is obtained as

$$\xi = \frac{2 + \sqrt{4 + 4\lambda_2 Z_N d^2}}{\lambda_2 Z_N d(1-d)} \quad (2-69)$$

The condition for PORLL converter entering DCM is obtained

$$\lambda_2 Z_N d(1-d)^2 \geq 4 \quad (2-70)$$

The VTG of PORLL converter can be summarized as

$$M_{PORLL} = \begin{cases} \frac{2}{\lambda_2(1-d)} \dots\dots\dots Z_N \lambda_2 d(1-d)^2 < 4 & \text{in CCM} \\ \frac{1}{\lambda_2} \left(2 + \frac{2d}{\xi(1-d)}\right) \dots\dots\dots Z_N \lambda_2 d(1-d)^2 \geq 4 & \text{in DCM} \end{cases} \quad (2-71)$$

The least normalized load Z_N for PORLL converter to enter DCM occurs when $d = 0.33$. Figure 2-32 shows the boundaries between CCM and DCM for PORLL converters. The VTGs versus Z_N for PORLL converter with and without the VLC effects are also shown in Figure 2-32. Two dotted curves show the VTG and boundary without considering VLC effect. Two solid curves show the VTG and boundary under the condition $\lambda_2 = 1.2$. In addition, the dots in Figure 2-32 are the experimental results of the VTG versus the normalized load.

2.2.3 Simulation and Experimental Results

The circuit parameters are chosen as below: $V_{in} = 20$ V, $L_1 = L_3 = 1$ mH, $L_2 = 0.5$ mH. $C_2 = C_3 = 2.2$ μ F, $C_1 = C_4 = 20$ μ F, $d = 0.3$ and $f = 20$ kHz. The normalized inductance L is 0.5 mH. It is obtained that PORLL converter works under critical DCM condition when $R = 249.4\Omega$. It can be calculated that: $\lambda_2 = 1.091$; $V_O = 52.37$ V. Figure 2-33 shows the simulation waveforms of PORLL under critical DCM.

Figure 2-32 PORLL converter's boundary and VTG versus the normalized load

Dotted curves: ideal circuit without considering VLC effect and $\lambda_2 = 1.0$
 Solid curves: considering VLC effect and $\lambda_2 = 1.2$
 Dots: experimentally measured VTG versus normalized load at $d = 0.33$

Figure 2-33 Simulation waveforms of PORLL converter under critical DCM ($d = 0.3$ and $R = 249.4 \Omega$)

In the experiments, the MOSFET and diodes are the same as those used in POSLL converter. When $R = 50 \Omega$, PORLL converter works in CCM. It is then obtained: $\lambda_2 = 1.455$, $V_O = 39.3 \text{ V}$ and $\Delta v_{C1} = \Delta v_{C2} = 18.0 \text{ V}$. Figure 2-34 shows the experimental waveforms of v_{gs} (CH1) and the output voltage V_O (CH2). Figure 2-35 shows the experimental waveforms of v_{C2} and v_{C3} .

Figure 2-34 Waveforms of PORLL converter with $d=0.3$, $R=50\ \Omega$, (CH1: v_{gs} ; CH2: v_o)

Figure 2-35 Waveforms of PORLL converter with $d=0.3$, $R=50\ \Omega$, (CH1: v_{C3} ; CH2: v_{C2})

When $R=300\ \Omega$, the circuit operates DCM. It is also obtained: $\lambda_2=1.023$, $\zeta=0.88$, $V_o=55.3\ \text{V}$ and $\Delta v_{C1}=\Delta v_{C2}=4.2\ \text{V}$. Figure 2-36 shows the experimental waveforms of v_{gs} and the output voltage. Waveforms of the VLC capacitor voltages are given in Figure 2-37.

Figure 2-36 Waveforms of PORLL converter with $d=0.3$, $R = 300 \Omega$, (CH1: v_{gs} ; CH2: v_o)

Figure 2-37 Waveforms of PORLL converter with $d=0.3$, $R = 300 \Omega$, (CH1: Δv_{C3} ; CH2: Δv_{C2})

2.3 The Generalized Formula

From the analysis in Sections 2-1 and 2-2, it is found that VLC reduces the VTGs of Luo converters under both CCM and DCM, which is mainly due to the voltage drops on the VLC capacitor. The effects of VLC also change the boundary condition which determines whether the converters are operated under CCM or DCM.

To derive the general formula for these Luo converters with VLCs, some common parameters are defined as follows. The load resistance of each Luo converter is assumed as R , the capacitance in each VLC is C , and the switching frequency of converters is f . For Luo converters which contain VLC, the formula of VTG can be represented as

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$$M_{\text{mod}} = \frac{1}{\lambda} M_{\text{origin}} \quad (2-72)$$

The definition of M_{origin} for each Luo converter can be found in [4]. λ is the generalized VLC coefficient.

For Luo converters with one VLC, such as POSLL converter, it can be derived that

$$\lambda = \lambda_1 = 1 + \frac{1}{2RCf} \quad (2-73)$$

For Luo converters with two VLCs, the VLC coefficient λ_2 can be expressed as

$$\lambda = \lambda_2 = 1 + \frac{1}{RCf} \quad (2-74)$$

For positive output Luo converters, the VTG with VLC can be summarized as

$$M_n = \frac{1}{\lambda_n} \frac{n}{1-d} \quad (2-75)$$

$$\lambda_n = 1 + \frac{n}{2RCf} \quad (2-76)$$

where n is the number of VLC contained in the converters: $n = 1$ for the self-lift circuit, $n = 2$ for the re-lift circuit and $n = 3$ for the triple-lift circuit, and etc.

It is known that the boundary condition between CCM and DCM is equivalent to the condition when the filling efficiency ξ is equal to 1. The boundary condition between CCM and DCM for positive output Luo converters is summarized as

$$\xi = \frac{Z_N d(1-d)}{M_n} \geq 1 \quad (2-77)$$

where $Z_N = R/fL$ is the normalized load and L is the normalized inductance.

For negative output Luo converters, the formula of VTG is the same as that given in (2-75) except that the output voltage is negative. The boundary condition between CCM and DCM for negative output Luo converters is

$$\xi' = \frac{Z_N d(1-d)}{2M_n} \geq 1 \quad (2-78)$$

where $Z_N = R/fL$ is the normalized resistance. L is the normalized inductance and n is the number of VLC in the converter.

In references [12], the filling efficiency was suggested to be the reciprocal of ζ . In this thesis, it is found that such a definition is not of high accuracy. Another method has been proposed in Sections 2-1 and 2-2. It can be summarized as follows:

- a) When the circuit works in DCM, there should be at least one current (for example: i_{D2} for POSLL converter and i_{L1} for POSL converter) reducing to zero after switching is turned off. The ripple of this current can be solved based on any of the two equations derived from the input voltage or output voltage. Equaling the two equations gives the first equation for the VTG as function of the filling efficiency;
- b) According to the volt-second balance of one inductor (for example, L_1 in POSLL converter and L_1 in PORLL converter), another equation can be derived to describe the relation between input and output voltage as function of filling efficiency;
- c) Combining the above two equations, the VTG and filling efficiency ζ can be solved. The boundary condition between CCM and DCM can also be derived by letting $\zeta = 1$.

It is found that the proposed method shows higher accuracy. The theoretical analysis is also verified through circuit simulation.

2.4 Summary

The VLC's influences on the properties of series Luo converters are analyzed in this chapter. The converters are assumed working at steady state and the ripple approximation methods are used in the analysis. Because of the voltage drop on VLC capacitor (s), the VTGs of Luo converters under both CCM and DCM are reduced. Inclusion of VLC effect also changes the boundary conditions between CCM and DCM for Luo converters.

It is also found that the VLC effects are related to circuit parameters including switching frequency, load resistance and the VLC capacitance. A general formula expressing such effects is summarized for Luo converters with various numbers of VLCs.

Chapter 2 Analysis of Luo Converters with Voltage Lift Circuit

In addition, a new method for derivation of the filling efficiency is proposed in this chapter. The simulation results show that this method is more accurate than the published one. Such analysis is valuable in calculating the boundary conditions which determine whether Luo converters are operated under CCM or DCM conditions. This will be useful for the design of Luo converters in practical applications.

Chapter 3 State-Space Modeling and Sliding-Mode Control for POSLL Converter

The steady state characteristics of series Luo converters have been analyzed in Chapter 2. The analysis gives a clear understanding of operation principle of Luo converters. It also forms the basis for investigation on the modeling and controller design of Luo converters, which is the main focus of Chapter 3. In this chapter, mathematic modeling and sliding mode control of POSLL converter will be addressed.

POSLL converter is chosen as the research objective in this Chapter. The first reason is because it is a high order one. There is less attention on control of high order converters. Possible reason could be the analysis of high order converters involving many complexities. But high order converter show advantages in achieving higher VTG with lower cost compared to cascaded low-order converters. It is therefore worthwhile to offer some effort to analyze and get more insight understanding of high order Luo converters. Another reason of choosing POSLL converter is that it includes one VLC, which makes POSLL converter quite representative for Luo converters.

In this chapter, state-space model of POSLL converter is developed. This model is useful in analyzing the dynamic response of POSLL converter. Based on the mathematic model, a novel sliding mode controller is proposed and a design example will be given. Simulation and experiments are also done to verify the theoretical analysis.

3.1 State-Space Modeling of POSLL Converter

3.1.1 State-space Models of POSLL Converter

Chapter 3 State-Space Modeling and Sliding-Mode Control for POSLL Converter

A POSLL converter and its equivalent circuits are redrawn in Figure 3-1. When the switch S is on, the current for charging capacitor C_2 is exponentially decreased. The decay time constant of this current is decided by the circuit stray resistance and C_2 , which is normally quite small compared with the switching period. As a result, this current can not be treated as a constant one. However for state-space averaging method, the current is normally assumed to be constant for derivation of the voltage variation of v_{C2} during switching on period. In such a condition, voltage v_{C2} can not be represented by the capacitor charge balance method [2]. Therefore, this voltage will not be chosen as a state variable in the following analysis, which means POSLL converter is modeled as a fourth-order system in this thesis.

The state variables are chosen as

$$X = [i_{L1} \quad v_{C1} \quad i_{L2} \quad v_{C3}]^T \quad (3-1)$$

Figure 3-1 POSLL converter

Chapter 3 State-Space Modeling and Sliding-Mode Control for POSLL Converter

When the switch S is on, the capacitor voltage v_{C2} is charged to input voltage rapidly and it has no influence to the other state variables of the circuit. In this condition it is not necessary to model it in the state-space equation. This further explains why the state vector is chosen of 4th order. When S is on, the system state-space equation can be written as

$$\begin{aligned} \dot{X} &= A_{ON} X + B_{ON} v_{in} \\ A_{ON} &= \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_1} & 0 \\ 0 & \frac{1}{L_2} & 0 & \frac{-1}{L_2} \\ 0 & 0 & \frac{1}{C_3} & \frac{-1}{RC_3} \end{bmatrix} \\ B_{ON} &= \begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_2} & 0 \end{bmatrix}^T \end{aligned} \quad (3-2)$$

When the switch S is off, the equivalent circuit of POSLL converter is shown in Figure 3-1c. From the result derived in Chapter 2, the voltage v_{C2} has an initial value V_{in} . C2 is discharged through inductor currents i_{L1} and i_{L2} . Define the switching frequency as f and the duty cycle d . The off period is therefore $(1-d)/f$. The average voltage of v_{C2} during switching off period can be obtained as

$$\begin{aligned} \bar{v}_{C2-off} &= v_{in} - \alpha(i_{L1} + i_{L2}) * (1-d) \\ \alpha &= \frac{1}{2C_2 f} \end{aligned} \quad (3-3)$$

At steady state, (3-3) leads to

$$\begin{aligned} \bar{V}_{C2-off} &= V_{in} - (\lambda_1 - 1)V_{C3} \\ \lambda_1 &= (1 + \frac{1}{2RC_2 f}) \end{aligned} \quad (3-4)$$

Depending on which equation, (3-3) or (3-4), is used to model the capacitor voltage v_{C2} , two models in off state can be obtained.

Based on (3-3), the state-space equations during switch off period is derived as

$$\dot{X} = A_{1OFF} X + B_{1OFF} v_{in} \quad (3-5)$$

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$$A_{1OFF} = \begin{bmatrix} \frac{-\alpha(1-d)}{L_1} & \frac{-1}{L_1} & \frac{-\alpha(1-d)}{L_1} & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{-\alpha(1-d)}{L_2} & \frac{1}{L_2} & \frac{-\alpha(1-d)}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & \frac{1}{C_3} & \frac{-1}{RC_3} \end{bmatrix}$$

$$B_{1OFF} = \begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_2} & 0 \end{bmatrix}^T$$

The first state-space averaged model of POSLL converter is then obtained by combining equations (3-2) and (3-5), which is named as Model 1.

$$\dot{X} = A_1 X + B_1 v_{in} \quad (3-6)$$

$$A_1 = \begin{bmatrix} \frac{-\alpha(1-d)^2}{L_1} & \frac{-(1-d)}{L_1} & \frac{-\alpha(1-d)^2}{L_1} & 0 \\ \frac{1-d}{C_1} & 0 & \frac{d}{C_1} & 0 \\ \frac{-\alpha(1-d)^2}{L_2} & \frac{d}{L_2} & \frac{-\alpha(1-d)^2}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & \frac{1}{C_3} & \frac{-1}{RC_3} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_2} & 0 \end{bmatrix}^T$$

If (3-4) is used, another state-space equation during switch off period is obtained as

$$\dot{X} = A_{2OFF} X + B_{2OFF} v_{in} \quad (3-7)$$

$$A_{2OFF} = \begin{bmatrix} 0 & \frac{-1}{L_1} & 0 & \frac{-(\lambda_1-1)}{L_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & \frac{-1-(\lambda_1-1)}{L_2} \\ 0 & 0 & \frac{1}{C_3} & \frac{-1}{RC_3} \end{bmatrix}$$

$$B_{2OFF} = \begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_2} & 0 \end{bmatrix}^T$$

Similarly, the second model can be obtained by combining equations (3-2) and (3-7), which is named as Model 2.

$$\dot{X} = A_2 X + B_2 v_{in} \quad (3-8)$$

$$A_2 = \begin{bmatrix} 0 & \frac{-(1-d)}{L_1} & 0 & \frac{-(\lambda_1-1)(1-d)}{L_1} \\ \frac{1-d}{C_1} & 0 & \frac{d}{C_1} & 0 \\ 0 & \frac{d}{L_2} & 0 & \frac{-1-(\lambda_1-1)(1-d)}{L_2} \\ 0 & 0 & \frac{1}{C_3} & \frac{-1}{RC_3} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_2} & 0 \end{bmatrix}^T$$

It is also found that both models represented in (3-6) and (3-8) give the same steady-state operating point, which is shown in (3-9) by assuming constant input voltage V_{in} , duty cycle D and switching frequency f .

$$X_{op} = \begin{bmatrix} \frac{DV_{in}}{\lambda_1(1-D)^2} & \frac{V_{in}}{\lambda_1(1-D)} & \frac{V_{in}}{\lambda_1 R(1-D)} & \frac{V_{in}}{\lambda_1(1-D)} \end{bmatrix}^T \quad (3-9)$$

Based on the above steady state operating point, the small signal model of POSLL converter can be derived. The small signal model is essential in analyzing the dynamic response of POSLL converter. Define the small variations of system parameters as

$$\begin{aligned} X &= X_{op} + \delta X \\ d &= D + \delta d \\ v_{in} &= V_{in} + \delta v_{in} \\ i_o &= \frac{V_{C3}}{R} + \delta i_o \end{aligned} \quad (3-10)$$

Substituting above variables into (3-6), the small-signal state-space equation for Model 1 can be obtained as

$$\delta \dot{X} = A_{1S} \delta X + B_{1vin} \delta v_{in} + B_{1d} \delta d + B_{1iO} \delta i_o \quad (3-11)$$

$$\begin{aligned}
 A_{1S} &= A_1|_{d=D} \\
 B_{1vin} &= B_1 \\
 B_{1d} &= \begin{bmatrix} \frac{V_{in}(2\lambda_1 - 1)}{\lambda_1 L_1 (1-D)} & -\frac{V_{in}}{\lambda_1 R C_1 (1-D)^2} & \frac{V_{in}(2\lambda_1 - 1)}{\lambda_1 L_2 (1-D)} & 0 \end{bmatrix}^T \\
 B_{1iO} &= \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{C_3} \end{bmatrix}^T
 \end{aligned}$$

Similarly, the small-signal state-space equation for Model 2 is also derived as

$$\delta \dot{X} = A_{2S} \delta X + B_{2vin} \delta v_{in} + B_{2d} \delta d + B_{2iO} \delta i_O \quad (3-12)$$

$$\begin{aligned}
 A_{2S} &= A_2|_{d=D} \\
 B_{2vin} &= B_2 \\
 B_{2d} &= \begin{bmatrix} \frac{V_{in}}{L_1 (1-D)} & -\frac{V_{in}}{\lambda_1 R C_1 (1-D)^2} & \frac{V_{in}}{L_2 (1-D)} & 0 \end{bmatrix}^T \\
 B_{2iO} &= \begin{bmatrix} -\frac{\alpha(1-D)}{L_1} & 0 & -\frac{\alpha(1-D)}{L_2} & \frac{-1}{C_3} \end{bmatrix}^T
 \end{aligned}$$

3.1.2 Simulation Results for Small Signal State-space Models

In section 3.1.1, two small signal state-space equations for POSLL converter have been derived. In Model 1, the voltage drop of C2 is represented as function of the two inductor currents, which is more accurate. However, it can be seen from (3-6) that this model involves the second order of duty cycle d . This may cause lots of trouble in controller design and implementation. Model 2 is derived by assuming constant voltage drop on C2. This model may not be so accurate in modeling system response during transients.

In order to obtain more deep understanding of these two models and also to examine which model is suitable for controller design, computer simulations are done for both models. The circuit parameters of POSLL converter used for computer simulation are shown in Table 3-1. The nominal operation condition of this converter is: $V_{in} = 12$ V, $V_O = 24$ V and $R = 36$ Ω .

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Table 3-1 Parameters of POSLL converter

$V_{in} = 10\sim 14\text{ V}$	$C_2 = 10\text{ }\mu\text{F}$
$V_O = 20\sim 28\text{ V}$	$C_3 = 100\text{ }\mu\text{F}$
$L_1 = 1\text{ mH}$	$R = 24 \sim 240\text{ }\Omega$
$L_2 = 0.5\text{ mH}$	$f = 50\text{ kHz}$
$C_I = 10\text{ }\mu\text{F}$	$D = 0.5\text{ (for open loop)}$

The circuit simulation is performed using software PSim [126]. The simulation time step is 100 ns, which is same for all simulations. Since the state-space models are based on small signal analysis, all the simulations are conducted in the vicinity of the nominal operation point.

Firstly the system response under a step change of input voltage is examined. In this example, input voltage is increased from 12V to 13V. Figure 3-2a shows the simulated waveform of output voltage using PSim. Figure 3-2b and 3-2c show the calculated output voltage waveform at the same condition based on the state-space models given in (3-6) and (3-8) using Matlab [127]. The figures clearly show the response based on circuit simulation is more coincided with the Model 1's result; the result derived from Model 2 shows more oscillations during the transient compared to the circuit simulation result.

Then the system response under a step change of duty cycle is examined. Duty cycle is increased from 0.5 to 0.51 in this example. Figure 3-3a is the PSim simulation waveform of output voltage. Figures 3-3b and 3-3c shows the calculated output voltage waveforms based on mathematics models. Similar as Figure 3-2, circuit simulation result is similar to the result based on Model 1. Model 2 gives more oscillations and large overshoot on output voltage.

Figure 3-4 is the system response under a step change of output load current, which is increased from 0.67A to 0.77A. Figure 3-4a is the circuit simulation result. Figures 3-4b and 3-4c are calculated results based on two models. Again it is found that the circuit simulation is almost the same as Model 1's result.

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Figure 3-2 POSLL converter's response to step change of input voltage

Figure 3-3 POSLL converter's response to step change of duty cycle

Figure 3-4 POSLL converter's response to step change of output current

The examples shown in Figures 3-2 to 3-4 confirm that Model 1 can give a more predictable and reliable result as it is more coincided with the actual circuit simulation result. Results from Model 2 show more oscillation during start up and longer settling time, although it gives the same VTG during steady state as Model 1 does.

All those observations can be confirmed by analyzing the poles location of both models [128]. For Model 2, its four poles are $-24.1 \pm 9462j$ and $-114.8 \pm 2393j$. For model 1, the four poles are $-95.4 \pm 9449j$ and $-418.5 \pm 2362j$. It is seen that both systems have similar nature frequency, which can be obtained from the imaginary part of the poles. In theory, the natural frequency is determined by the circuit energy-storage components including C1, L1, C3 and L2. As both models are based on the same parameters, it is reasonable that both models show similar natural frequencies. However, the poles of Model 1 have much bigger real parts than poles of Model 2 do, which means the damping effect of Model 1 is more than Model 2. This explains why model 1 has smaller overshoot and shorter settling time than Model 2. In general, if ignoring the dynamic performance, Model 2 is still reasonable to represent the real system in terms of steady state gain and

nature frequency. However Model 1 is definitely more accurate and it is suitable for modeling the system performance in both transients and steady state.

3.2 The Sliding-Mode Control

SM controller can develop a first-order response for high order systems. This is desirable for dc-dc converters, especially for high-order ones. SM controllers with two state variables feedback have been proven to have several advantages over traditional linear controllers [84-86]. The most attractive point is that the complexity of the control scheme will not increase when system order increases.

Sliding mode control theory has been briefly reviewed in Chapter 1. It is known that the control input of SM controller is in discrete levels, 0 or 1 and the converter model used for SM controller designing is normally bilinear state-space equations. In this section, attentions are given to the control scheme design procedure, which is normally implemented through three steps. Firstly, select a switching surface. Then, design a suitable switching law which ensures the system can reach and remain on the sliding surface. Finally, analyze the system performance at the operation point. Small-signal analysis method is commonly used for such analysis.

A typical bilinear system can be represented as

$$\dot{X} = f(X, t, u) = \begin{cases} f_0(X, t) \cdots \cdots u = u^- \\ f_1(X, t) \cdots \cdots u = u^+ \end{cases} \quad (3-13)$$

where X is an n^{th} order state vector, f is a bilinear function vector with dimension n , and u is the discrete control input which is zero or one.

The sliding surface is defined when the sliding function is zero in the state space

$$\sigma(X, t) = GX - G_R = 0 \quad (3-14)$$

where $\sigma(X, t)$ is the sliding function. G is an $(1 \times n)$ matrix. G_R is the scalar reference value. This sliding surface normally divides the system state space into two separated parts.

The switching law is often designed according to the value of the sliding function as shown in (3-15)

$$u = \begin{cases} u^+ & \dots \sigma > 0 \\ u^- & \dots \sigma < 0 \end{cases} \quad (3-15)$$

Movement of the system RP is controlled by the switching law. In practice, due to the finite switching frequency, the system RP cannot stay on the sliding surface but slide from one side to another side. This movement of system RP is constrained in the vicinity of the sliding surface, which is clearly shown in Figure 1-14. Three conditions should be satisfied to ensure the stability of a sliding mode controller, which are existence condition, reaching condition and stability condition under sliding mode.

3.2.1 Existence Condition

This condition ensures the system can slide in the vicinity of the sliding surface. In other words, system trajectories of the two substructures should be directed toward the sliding surface. Mathematically, the existence condition can be represented as

$$\lim_{\sigma \rightarrow 0^+} \dot{\sigma}(X, t) < 0 < \lim_{\sigma \rightarrow 0^-} \dot{\sigma}(X, t) \quad (3-16)$$

3.2.2 Reaching Condition

This condition ensures that the system RP can eventually reach the sliding surface starting from any point in the state space. For second-order system, this condition can always be evaluated graphically. However, graphical method is not suitable for high-order systems due to the increased complexity of state space. It has been proposed in [71] that the reaching condition of high-order systems can be verified by examining the derivative value of the sliding function. For example, if the system RP has negative sliding function value, according to the switching law and the system state equation shown in (3-13), the switch can be set as $u = u^+$. It is then obtained

$$\dot{\sigma}(X, t) = Gf_1(X, t) \quad (3-17)$$

If the derivative of sliding function is a constant positive definitive value, the system RP can definitely cross the sliding surface and the crossing time is decided by the derivative value of the sliding function.

3.2.3 Equivalent Control and Stability

When the system is in the sliding mode, it should satisfy

$$\begin{aligned}\sigma(X, t) &= 0 \dots\dots\dots (a) \\ \dot{\sigma}(X, t) &= 0 \dots\dots\dots (b)\end{aligned}\tag{3-18}$$

According to Fillipov average method [69], an equivalent control input u_{eq} can be obtained by solving the differential equation of the sliding function. See Figure 3-5 for details. The equivalent control input shall satisfy (3-19).

$$\dot{\sigma} = u_{eq} \frac{\partial \sigma}{\partial X} f_1 + (1 - u_{eq}) \frac{\partial \sigma}{\partial X} f_0, \quad 0 < u_{eq} < 1 \tag{3-19}$$

Figure 3-5 Fillipov's construction of the equivalent dynamics in sliding mode

The equivalent control law u_{eq} is also a function of X . In control of dc-dc converters, it should equal to the desired duty cycle. It is also found that this equivalent control input is a variable continuous in time domain. The system motion on the sliding surface can therefore be replaced by a continuous system as

$$\begin{aligned}\dot{X} &= u_{eq} f_1(X) + (1 - u_{eq}) f_0(X) \\ \sigma(X, t) &= 0; \quad \dot{\sigma}(X, t) = 0\end{aligned}\tag{3-20}$$

Equation (3-20) forms the basis for examining the system local stability on the sliding surface. However in most cases, this equation is a nonlinear one. Small-signal linearization must be applied to (3-20) in the vicinity of the operating point. Once the system Jacobian matrix is derived using the small signal analysis, the system stability can be easily examined through analyzing the pole location of the characteristic equation of Jacobian matrix. Other system properties such as the input audio-susceptibility and output impedance can also be examined based on the linearized state-space equations.

3.3 The Proposed Sliding Surface

There are two types of widely used sliding surfaces given in (3-21) [75, 83-84]

$$\begin{aligned}\sigma_2(X, t) &= g_{2i}(i - I_r) + g_{2v}(v_o - V_r) = 0 \dots\dots\dots (a) \\ \sigma_m(X, t) &= i + g_{mv}(v_o - V_r) + g_{mit} \int_0^t (v_o - V_r) dt = 0 \dots\dots\dots (b)\end{aligned}\tag{3-21}$$

V_r is the reference for the output voltage. It is named reference voltage in this thesis to distinguish it from the output voltage. The current i can be the inductor current for second-order converters or input inductor current of higher-order ones. The first equation is normally known as the two-variable sliding surface. The other one is known as the current mode control with PI compensator in the voltage loop, which is named as multi-loop controller in this thesis.

For (3-21a), at the starting point, $i(0)$ and $v_o(0)$ are equal to 0. The initial value of the sliding function $\sigma_2(X, t)$ is negative. To reach the sliding surface, the switch shall be turned on for some period so that $\sigma_2(X, t)$ can reach a positive value. Since generally for dc-dc converter control, current dynamic response is much faster than the output voltage response, which means in (3-21a) v_o can be assumed as 0 during start up to study the current response. Therefore, (3-21a) can be rewritten as

$$i = \frac{g_{2i}I_r + g_{2v}V_r}{g_{2i}}\tag{3-22}$$

It is found that the peak inductor current is decided by sum of reference value $g_{2i}I_r + g_{2v}V_r$. As reference part $g_{2i}I_r + g_{2v}V_r$ is larger than the desired current $g_{2i}I_r$, larger overshoot in both inductor current and output voltage will occur. To reduce the inductor current overshoot, g_{2i} should be set to large value and g_{2v} should be small. But

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smaller g_{2v} leads to larger steady state error. A PI compensator is often used to overcome this issue, which will further deteriorate the dynamic performance of the system.

For the second sliding surface, its reaching time is not only decided by the current response but also the voltage response. Voltage response is normally slow. It therefore takes longer time for the output voltage to exceed the reference voltage. So the integration part of the second equation is also a negative value, which will increase the required current value by the reference voltage itself. In practical, the integral gain g_{mit} is set to a small value to avoid large overshoot current. As g_{mit} is small, the dynamic response of this controller is also slow in case of input voltage variations and load variations.

Above analysis clearly shows that one disadvantage of above two SM controllers is that there is high current overshoot during start up. The ultimate reason is that for above two controllers the start up point is not on the sliding surface. It will take long time for system RP to reach the sliding surface. During this period, the switch is kept on and leads to large current and voltage overshoot. A typical inductor current overshoot can be as high as 300 to 400 percent of its nominal value. One possible way to reduce the start up current overshoot is to set the initial value of sliding function to be zero at start up. This can essentially decrease the reaching time. This is also the basic design principle of the proposed new sliding mode controller in this section.

The new proposed sliding surface is defined as

$$\sigma(X, t) = g_i i_L + v_o + g_v \int_0^t (v_o - V_r) dt \quad (3-23)$$

where

g_i , current coefficient, Ω

g_v , voltage time coefficient, s^{-1}

The proposed sliding surface is actually a modified version of the multi-loop controller. The difference is that the error of the output voltage in (3-21b) is changed to output voltage itself in (3-23). The switching law is the same as that shown in (3-15). In state space, this sliding surface is a straight line in the state space. During start-up, the line is crossing the origin and the system RP is just on the origin. Therefore, the reaching time is zero. As current i_L and voltage v_o increasing, the system RP can stay on the sliding

surface until it reaches the operating point. This is achieved by appropriate parameter selection. Another distinct advantage of this sliding function is that no current reference is needed. In addition, since integration part is already included in the proposed sliding surface, there is no steady state error in regulation of the output voltage. In the following section, controller design based this proposed sliding surface will be introduced.

3.4 Design Criteria for the Proposed SM Controller

The POSLL Model 1 derived in section 3.1 will be used for the new SM controller design, as it is more accurate in both transient and steady state. According to Model 1, if the switch is kept on all the time, or $d = 1$, the capacitor voltage v_{C2} is V_{in} . The system will reach an equilibrium point as

$$X|_{d=1} = \begin{bmatrix} \infty & 0 & \frac{V_{in}}{R} & V_{in} \end{bmatrix}^T \quad (3-24)$$

When the switch is kept off all the time, or $d = 0$, the voltage v_{C2} is zero. Another system equilibrium point is obtained as

$$X|_{d=0} = [0 \quad 0 \quad 0 \quad 0]^T \quad (3-25)$$

The proposed sliding surface for POSLL converter is represented as

$$\sigma(X, t) = g_i x_1 + x_4 + g_v \int_0^t (x_4 - V_r) dt \quad (3-26)$$

where

g_i current coefficient, Ω

g_v voltage coefficient, s^{-1}

The switching law is chosen as

$$\begin{cases} u^- = 1 \\ u^+ = 0 \end{cases} \quad (3-27)$$

Once the new controller is defined, the three conditions to ensure the system stability are then analyzed in the following sections.

3.4.1 Existence Condition

Two situations shall be considered for existence condition. Firstly when the system RP is in the negative vicinity of the sliding surface, the system shall satisfy

$$\lim_{\sigma \rightarrow 0^-} \left\{ \frac{g_i}{L_1} V_{in} + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3} \right) + g_v(x_4 - V_r) \right\} > 0 \quad (3-28)$$

Secondly when the system RP is in the positive vicinity of the sliding surface, it shall satisfy:

$$\lim_{\sigma \rightarrow 0^+} \left\{ \frac{g_i}{L_1} (v_{C2} - x_2) + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3} \right) + g_v(x_4 - V_r) \right\} < 0 \quad (3-29)$$

From the operation of POSLL circuit, it is found that maximum value of voltage v_{C2} is V_{in} . It decreases once the switch S is turned off. Therefore, the worst case for (3-29) happens at the moment when switch S is turned off. Then above equation can be rewritten as

$$\lim_{\sigma \rightarrow 0^+} \left\{ \frac{g_i}{L_1} (V_{in} - x_2) + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3} \right) + g_v(x_4 - V_r) \right\} < 0 \quad (3-30)$$

In order to analyze the system performance in the vicinity of operation point, only the small perturbations around the operation point are considered here. Then the existence condition, (3-27) and (3-30), changes to

$$\begin{aligned} \lim_{\sigma \rightarrow 0^-} \left\{ \frac{g_i}{L_1} V_{in} + \left(\frac{\delta x_3}{C_3} - \frac{\delta x_4}{RC_3} \right) + g_v \delta x_4 \right\} &> 0 \dots\dots\dots (a) \\ \lim_{\sigma \rightarrow 0^+} \left\{ \frac{g_i}{L_1} (V_{in} - V_r + \delta x_2) + \left(\frac{\delta x_3}{C_3} - \frac{\delta x_4}{RC_3} \right) + g_v \delta x_4 \right\} &< 0 \dots\dots\dots (b) \end{aligned} \quad (3-31)$$

For POSLL converter, V_{in} is always smaller than reference voltage V_r . From (3-31), it can be concluded that **a positive coefficient g_i is sufficient for the existence condition.**

3.4.2 Reaching Condition

Assuming the sliding function $\sigma(X, t)$ is negative and it stays as negative for long time, the switch input is then $u = 1$. From (3-23), it is known that the reaching condition can be represented as

$$\lim_{t \rightarrow \infty} [\dot{\sigma}(X, t)|_{d=1}] = \frac{g_i}{L_1} V_{in} - g_v (V_r - V_{in}) > 0 \quad (3-32)$$

which leads to

$$g_i > g_v L_1 \frac{V_r - V_{in}}{V_{in}} \quad (3-33)$$

From (3-32), it is also found that the derivative of $\sigma(X, t)$ is a positive constant which is not changed when X changes. Therefore, $\sigma(X, t)$ will keep increasing and the system RP can reach the sliding surface eventually.

If the sliding function $\sigma(X, t)$ is positive and remain positive for long time, according to the switching law, the switch input is then $u = 0$. Note that the voltage across C_2 is also zero under this condition. The derivative of $\sigma(X, t)$ can be derived as

$$\lim_{t \rightarrow \infty} [\dot{\sigma}(X, t)|_{d=0}] = -g_v V_r < 0 \quad (3-34)$$

Equation (3-34) shows that g_v should be a positive constant. Under this condition, $\sigma(X, t)$ will decrease to below zero eventually and the system RP can therefore reach the sliding surface in finite time.

In summary, ***the sufficient condition for the reaching condition is***

$$g_i > g_v L_1 \frac{V_r - V_{in}}{V_{in}} > 0 \quad (3-35)$$

3.4.3 Stability and System Dynamics on the Sliding Surface

For the proposed controller, the equivalent control signal is of the same meaning as duty cycle. In the following part, the equivalent control signal is then represented as d_{eq} . d_{eq} shall satisfy (3-20). From (3-6) and (3-23), it can be derived that

$$-\frac{\alpha g_i (x_1 + x_3)}{L_1} (1 - d_{eq})^2 - \frac{g_i x_2}{L_1} (1 - d_{eq}) + \frac{g_i V_{in}}{L_1} + \frac{(R x_3 - x_4)}{R C_3} + g_v (x_4 - V_r) = 0 \quad (3-36)$$

Equation (3-36) has only one valid solution for d_{eq} , which is

$$d_{eq} = \frac{2\alpha g_i C_3 (x_1 + x_3) + g_i C_3 x_2 - \sqrt{(g_i C_3 x_2)^2 + 4\alpha g_i C_3 (x_1 + x_3) [g_i C_3 V_{in} + L_1 (x_3 - \frac{x_4}{R}) + g_v L_1 (x_4 - V_r)]}}{2\alpha g_i C_3 (x_1 + x_3)} \quad (3-37)$$

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Substituting (3-37) into (3-6), the state-space equation of the closed-loop control system can be derived and shown in (3-38). In this equation, d_{eq} is function of the state vector, reference voltage and input voltage.

$$\dot{X} = \begin{cases} -\frac{1}{g_i C_3} x_3 + \left(\frac{1}{g_i R C_3} - \frac{g_v}{g_i}\right) x_4 + \frac{g_v}{g_i} v_r \\ \frac{1}{C_1} (1 - d_{eq}) x_1 - \frac{1}{C_1} d_{eq} x_3 \\ \frac{1}{L_2} x_2 - \frac{L_1}{L_2 C_3 g_i} x_3 + \frac{L_1}{L_2 g_i} \left(\frac{1}{R C_3} - g_v\right) x_4 + \frac{L_1 g_v}{L_2 g_i} v_r \\ \frac{1}{C_3} x_3 - \frac{1}{R C_3} x_4 \end{cases} \quad (3-38)$$

$$Y = V_O = CX$$

where $C = [0 \ 0 \ 0 \ 1]$. Set the left side of first equation of (3-38) equal to zero, only one equilibrium point can be obtained as

$$X_{eq} = \begin{bmatrix} \frac{V_r (\lambda_1 V_r - V_{in})}{R V_{in}} & V_r & \frac{V_r}{R} & V_r \end{bmatrix}^T \quad (3-39)$$

The equivalent control input can be solved as

$$D_{eq} = \frac{\lambda_1 V_r - V_{in}}{\lambda_1 V_r} \quad (3-40)$$

If introducing small perturbations to the state variables around the operation point as

$$\begin{aligned} X &= X_{eq} + \delta X \\ v_r &= V_r + \delta v_r \\ v_{in} &= V_{in} + \delta v_{in} \\ i_O &= \frac{V_r}{R} + \delta i_O \end{aligned} \quad (3-41)$$

The small-signal state-space equation can be derived as

$$\delta \dot{X} = A_S \delta X + B_{SVIN} \delta v_{in} + B_{SVR} \delta v_r + B_{SZ} \delta i_O \quad (3-42)$$

where

$$A_S = \begin{bmatrix} 0 & 0 & -\frac{1}{g_i C_3} & \left(\frac{1}{g_i R C_3} - \frac{g_v}{g_i}\right) \\ A_S(2,1) & A_S(2,2) & A_S(2,3) & A_S(2,4) \\ 0 & \frac{1}{L_2} & -\frac{L_1}{L_2 C_3 g_i} & \frac{L_1}{L_2 g_i} \left(\frac{1}{R C_3} - g_v\right) \\ 0 & 0 & \frac{1}{C_3} & -\frac{1}{R C_3} \end{bmatrix}$$

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$$\begin{aligned}
A_S(2,1) &= \frac{V_{in}}{C_1 V_r \lambda_1} - \frac{\alpha V_{in}}{C_1 V_r \lambda_1 R(1 + \frac{2\alpha}{R})} \\
A_S(2,2) &= \frac{1}{C_1(R + 2\alpha)} \\
A_S(2,3) &= -\frac{V_r \lambda_1 - V_{in}}{C_1 V_r \lambda_1} + \frac{L_1 V_r \lambda_1}{g_i C_1 C_3 V_{in}(R + 2\alpha)} + \frac{\alpha V_{in}}{C_1 V_r \lambda_1(R + 2\alpha)} \\
A_S(2,4) &= \frac{V_r \lambda_1 L_1 (g_v C_3 - 1/R)}{g_i C_1 C_3 V_{in}(R + 2\alpha)} \\
B_{SVIN} &= \begin{bmatrix} 0 & \frac{V_r \lambda_1}{C_1 V_{in}(R + 2\alpha)} & 0 & 0 \end{bmatrix}^T \\
B_{SVR} &= \begin{bmatrix} \frac{g_v}{g_i} & -\frac{g_v L_1 V_r \lambda_1}{g_i C_1 V_{in}(R + 2\alpha)} & -\frac{L_1 g_v}{L_2 g_i} & 0 \end{bmatrix}^T \\
B_{SZ} &= \begin{bmatrix} \frac{1}{g_i C_3} & -\frac{L_1 V_r \lambda_1}{g_i C_1 C_3 V_{in}(R + 2\alpha)} & \frac{L_1}{L_2 g_i C_3} & \frac{1}{C_3} \end{bmatrix}^T
\end{aligned}$$

The closed-loop system steady state stability and dynamic characteristics can be examined based on (3-42).

The small signal model of output voltage can also be derived from (3-38) as

$$\delta y = C \delta X \quad (3-43)$$

Based on (3-42) and (3-43), various transfer functions between the input, the reference and the output voltage can be derived as shown in (3-44). These transfer functions would be valuable in choosing the controller parameters g_i and g_v .

$$\begin{aligned}
G_{SVR}(s) &= C * (sI - A_S)^{-1} * B_{SVR} \\
G_{SVIN}(s) &= C * (sI - A_S)^{-1} * B_{SVIN} \\
G_{SZ}(s) &= C * (sI - A_S)^{-1} * B_{SZ}
\end{aligned} \quad (3-44)$$

3.4.4 Switching Frequency

Hysteresis control is a widely accepted method to limit the switching frequency in SM controller [87]. A zoom in figure of system RP under sliding mode with hysteresis control is shown in Figure 3-6.

Figure 3-6 Magnified view of the system trajectory under sliding mode in hysteresis control

The switching law is therefore redefined as

$$u = \begin{cases} 1 & \dots\dots\dots \sigma(X, t) < -\epsilon \\ 0 & \dots\dots\dots \sigma(X, t) > \epsilon \\ \text{not changed} & \dots\dots\dots |\sigma(X, t)| < \epsilon \end{cases} \quad (3-45)$$

The ϵ is the hysteresis band. It has been derived in [74] that

$$\begin{aligned} \Delta t_1 &= \frac{2\epsilon}{\frac{\partial \sigma}{\partial X} \cdot f_1(X, t)} \\ \Delta t_2 &= \frac{2\epsilon}{\frac{\partial \sigma}{\partial X} \cdot f_0(X, t)} \end{aligned} \quad (3-46)$$

where Δt_1 is the time duration for vector f_1 moving from position X_1 to X_2 ; Δt_2 is the time duration for vector f_0 moving from position X_2 to X_3 . Substituting state-space equation into (3-46), it is derived

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$$\begin{aligned}\Delta t_1 &= \frac{2\varepsilon}{\frac{g_i}{L_1}V_{in} + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3}\right) + g_v(x_4 - V_r)} \\ \Delta t_2 &= \frac{2\varepsilon}{\frac{g_i}{L_1}(V_{in} - x_2) + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3}\right) + g_v(x_4 - V_r)}\end{aligned}\quad (3-47)$$

Then the duration of one switch cycle can be obtained by combing the above two sub-periods:

$$T = \frac{2\varepsilon \left[2 \left(\frac{g_i}{L_1}V_{in} + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3}\right) + g_v(x_4 - V_r) \right) - \frac{g_i}{L_1}x_2 \right]}{\left[\frac{g_i}{L_1}V_{in} + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3}\right) + g_v(x_4 - V_r) \right] \left[\frac{g_i}{L_1}(V_{in} - x_2) + \left(\frac{x_3}{C_3} - \frac{x_4}{RC_3}\right) + g_v(x_4 - V_r) \right]} \quad (3-48)$$

Since only nominal steady-state operation condition is considered in the design, (3-48) can be simplified by ignoring the small variations as

$$T = \frac{2\varepsilon L_1 V_r}{g_i V_{in} (V_r - V_{in})} \quad (3-49)$$

$$f = \frac{g_i V_{in} (V_r - V_{in})}{2\varepsilon L_1 V_r} \quad (3-50)$$

It is found from (3-50) that the nominal switching frequency changes when the input voltage or the reference voltage change. It may be possible to achieve a constant switching frequency by varying the hysteresis band according to the input and reference voltage changes. However, a lot of calculation circuits have to be added in the controller. In addition, as long as the input voltage and reference voltage does not change too much, using constant hysteresis band can also be accepted as a low cost solution. Therefore, in this thesis, the hysteresis band is chosen according to the nominal operation point as

$$\varepsilon = \frac{g_i V_{in} (V_r - V_{in})}{2f L_1 V_r} \quad (3-51)$$

The proposed closed-loop control scheme is then developed in Figure 3-7. It shows that the whole control scheme includes four parts: the POSLL converter, current and voltage sensors, calculation circuit of the sliding function, hysteresis and driving circuit. Based on this proposed control scheme, some design examples will be given in the following section to demonstrate the performance of this controller.

Figure 3-7 Closed-loop control scheme for POSLL converter

3.5 Simulations

3.5.1 Small-Signal Analysis

The circuit parameters of the POSLL converter used for simulations and experiments are given in Table 3-1. The switch and diodes can be chosen according to the converter ratings. The details are ignored here.

According to the parameters given in Table 3-1, g_i and g_v can be selected to satisfy the existence and reaching condition in worst case. It is known that the worst case is to achieve the maximum output voltage (28V) in the condition of minimum input voltage (10V). From (3-33), it is then obtained

$$g_i > 0.0018g_v \quad (3-52)$$

After satisfying the reaching and existence conditions, it is also necessary to optimize the system performance under nominal work conditions. This can be done through examining the system closed-loop characteristic on the sliding surface using small signal state space equations. As the converter model is a fourth order one, it is better to separate its four poles into two groups of conjugate poles, which are far away from each other. The conjugate poles which are closed to the imaginary axes are named as the dominant poles and the other group is the non-dominant poles. The system performance optimization is

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then achieved by adjusting the position of the dominant closed-loop poles. In order to achieve a rapid dynamic response and small overshoot. The damping ratio of the dominant poles should be in the range of 0.4 to 0.7. The detailed calculation is ignored here. Finally, the controller parameters are chosen as

$$\begin{aligned} g_i &= 5\Omega \\ g_v &= 1700 \text{ s}^{-1} \end{aligned} \quad (3-53)$$

The corresponding four poles are $-2304.2 \pm 9875j$ and $-1150.2 \pm 1345j$. The damping ratio calculated from the dominant poles is 0.45. In this example, the switching frequency is chosen as 50 kHz and the hysteresis band is chosen as 0.3 according to (3-51).

Based on the above parameters, Bode plot of $G_{vref}(s)$ is obtained and shown in Figure 3-8. It is seen that the crossover frequency f_c of $G_{vref}(s)$ is 304 Hz. The phase margin is 98° .

Figure 3-8 Bode plot of $G_{SVR}(s)$

Figure 3-9 shows the audio-susceptibility of POSLL converter in both open-loop and closed-loop. It is found that the amplitude of $G_{SVIN}(s)$ is maintained at a low level over a wide frequency range. Its maximum value decreases from 25.6dB in open-loop system to -6.7dB in closed-loop system, which means the output voltage is less influenced by the input variations.

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Figure 3-9 Audio-susceptibility of POSLL converter

The output impedances $Z_{out}(s)$ under both closed-loop system and open-loop system are also calculated at the nominal operation conditions. The impedances versus the frequency are shown in Figure 3-10. Similar as the traditional current-programmed control [33], the output impedance of the proposed system is increased in the low frequency range. However, the proposed control scheme can decrease the maximum output impedance from 30.9 dB Ω in open-loop to 12.6 dB Ω in closed-loop, which can improve the system dynamic response under load variations.

Figure 3-10 Output impedance of POSLL converter

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All above examples show the controller performance under the nominal operation point. The controller performance under different input voltages is also analyzed here. In this example, input voltage is changed from 10 V to 14 V. The loci of closed-loop poles are plotted in Figure 3-11 and the damping ratio calculated from the dominant poles is shown in Figure 3-12.

Figure 3-11 Pole locus of the $G_{SVR}(s)$ under variations of input voltage

Figure 3-12 Damping ratio versus the input voltage

It is seen that the poles moves closer to the imaginative axis as the input voltage increases. However during the movement, system natural frequency is almost not changed because the imaginary parts of the poles are almost not changed. This is reasonable as the circuit

energy storage components determine the natural frequency. Also from Figure 3-12, it is found the system damping factor does not change much during the movement, which means the system overshoot is not changed much as well. Above analysis therefore shows that the controller performance is quite consistent against the input voltage changes, which is in agreement with the property of sliding mode control.

3.5.2 Circuit Simulations

To simplify the analysis, all above analysis and circuit state-space equations are based on ideal conditions, which means the circuit components such as MOSFET, inductor are assumed as ideal one and their losses are all ignored. In actual situation, the un-ideal circuit parameters will slow down the system response however it will not influence the system stability. To obtain a more representative result which is more comparable to the experiment result which will be shown later, the circuit simulations are done while considering the un-ideal components such as MOSFET, diodes and inductors. The practical POSLL converter used for circuit simulation and experiment is shown in Figure 3-13. In the circuit, the dc resistance of L_1 is combined with the current sense resistor as $R_{L1}+R_{cs}$. R_{cs2} is the resistor for sensing the current i_{C3} . The on-resistance of switch SPA80N10L [129] is 0.06Ω . Forward voltage drop of MBR10100 [130] is $0.4V$.

Figure 3-13 POSLL converter for simulation and experiment

3.5.2.1 Influence of g_i and g_v on system performance

Firstly, the influence of g_i and g_v on system performance is examined. Three different simulations are conducted here: increase g_i only; increase g_v only; increase g_i and g_v simultaneously. The results are shown as below.

Figure 3-14 shows the result when keeping g_v constant and increasing g_i . It is seen that when g_i increases, voltage response speed is improved slightly a little but its overshoot also increases, which leads to a longer settling time. It is also found that the overshoot of inductor current is decreased when g_i increases. In addition, g_i will influence mainly on the current response instead of output voltage response.

Figure 3-14 Simulated waveforms of output voltage and inductor current of POSLL converter under SM control with various g_i

Figure 3-15 shows the simulation result when keeping g_i constant while increasing g_v . It is seen that increasing g_v will achieve a more rapid transient response but more oscillations and higher overshoot at the output voltage. Settling time is also prolonged. It is also interesting to observe that the system response changes to first order type when g_v is further decreased to 900 as shown in Figure 3-15a. If comparing waveforms in Figure 3-14 and Figure 3-15, it is found that the output voltage response is more sensitive to the change of g_v than to the change of g_i .

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Figure 3-15 Simulated waveforms of output voltage and inductor current of POSLL converter under SM control with various g_v

Figure 3-16 gives the result when increasing g_i and g_v simultaneously and keeping g_i/g_v constant. Similarly, increasing g_i and g_v gives faster system dynamic response but more oscillations. In fact, the increased overshoot in inductor current is due to the increase of g_v . This can be explained based on the results shown in Figures 3-14 and 3-15.

Figure 3-16 Simulated waveforms of output voltage and inductor current of POSLL converter under SM control with various g_v and g_i but constant g_i/g_v

In accordance to the theoretical and simulation analysis, the principle for choosing g_i and g_v is to first choose the ratio of g_i/g_v according to (3-35). Then, having the converter operated at nominal conditions, both g_i and g_v are adjusted simultaneously to achieve a satisfying output voltage response. At last, g_i is adjusted to gain suitable current response.

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During this phase, the small-signal analysis can be used to determine whether a suitable damping factor and bandwidth are achieved at the operation point. Unlike traditional linear control, the SM control has similar dynamic performance over a wide range of operation conditions. In most cases, there is no need to tune the control parameters further at other input voltages.

3.5.2.2 Comparison between the proposed controller with multi-loop controller

Since the proposed control scheme is developed based on the traditional multi-loop controller, the control performances of these two controllers are compared in this section. The control scheme for multi-loop controller is shown in Figure 3-17.

In order to achieve the same crossover frequency for two controllers, it is obtained that

$$\begin{aligned} g_{mv} &= 1/g_i \\ g_{mit} &= g_v/g_i \end{aligned} \quad (3-54)$$

The multi-loop controller is also implemented with a hysteresis control and the hysteresis band is the same as the proposed controller. To avoid saturation effect from integrator, a hard limit is applied to the multi-loop controller for anti-windup purpose. The limitation value is chosen based on the worst condition, which means the output of the integrator is limited between -2.8 and 0 in this example.

Figure 3-17 Control scheme of multi-loop controller for POSLL converter

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Firstly the simulation results of controller performance under difference input voltage are given in Figures 3-18 and 3-19. Figure 3-18 shows the start-up performance of proposed controller. Figure 3-19 is the results of multi-loop controller.

Figure 3-18 Proposed controller's performance during start up at full load

Figure 3-19 Multi-loop controller's performance during start up at full load

In order to achieve a clear view, the circuit simulation is designed to let the system start switch at 0.5 ms. It is seen that multi-loop controller shows larger overshoot in both output voltage and inductor current. The current overshoot is about 300% of the nominal value for multi-loop control system, while it is less than 100% in the proposed control system. In addition, the multi-loop controller shows much different overshoot values in output voltage under different input voltages.

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The sliding function and gate signal of two controllers are also plotted in Figure 3-20 under nominal input voltage (12V) and maximum load (24Ω). As explained in Section 3.3, $\sigma(X,t)$ of the multi-loop control system remains negative for a long time during startup, which causes large overshoot. While this situation is different for the proposed controller, the system RP is well maintained on the sliding surface during the whole start up phase.

Figure 3-20 Sliding function and control output during start-up

Above example well demonstrates that the proposed control can improve the system performance during the startup. It shows less overshoot and shorter settling time comparing with the traditional multi-loop controller. The similar comparison result can be obtained on the system performance in tracking changes of reference voltages. Since both controllers have the same small signal state-space equations which result in same dynamic performance, there is no need to compare the dynamic performance of two controlled systems.

3.5.2.3 Comparison between the proposed control scheme with the high-pass sliding mode controller

The proposed controller is also compared with high-pass SM controller. The details of the high-pass SM controller can be found in [84-86], which are ignored here. Since in those references, high-pass SM controller is well implemented in Cúk converter, shown in Figure 3-21, this Cúk converter is therefore chosen as the control objective in this section.

Figure 3-21 Cúk converter with parasitic effects

All the circuit parameters and control parameters of two controllers are given in Table 3-2. Simulation results are given in Figure 3-22. Since the simulation is done at minimum load ($R = 150 \, \Omega$), both controllers show high overshoot in inductor current. It is seen that the settling time of the output voltage for two controllers are similar. However the high-pass SM controller shows larger output voltage and current overshoots, even though a current limiter has been applied to the high-pass filter controller. More oscillations and longer settling time is found in the current response of high-pass SM controller, this is because the bandwidth is relative high for the high-pass SM controller. This example clearly shows that the proposed controller has better performance over the high-pass SM controller in reducing the current and voltage overshoot during startup.

Table 3-2 Parameters of Cúk converter and the controllers

Circuit parameters for Cúk converter		Control parameters for high-pass SM controller	Control parameters for proposed SM controller
$V_{in} = 24 \, \text{V}$	$L_2 = 1.9 \, \text{mH}$	$g_I = 2.1$	$g_i = 3 \, \Omega$
$C_1 = 100 \, \mu\text{F}$	$R_2 = 0.5 \, \Omega$	$g_2 = 1$	$g_v = 550 \, \text{s}^{-1}$
$C_2 = 47 \, \mu\text{F}$	$V_r = 15 \, \text{V}$	$\tau_{HPF} = 0.22 \, \text{ms}$	$\varepsilon_{smc} = 0.1$
$L_1 = 3.3 \, \text{mH}$	$f = 50 \, \text{kHz}$	$I_{LIM} = 1.5 \, \text{A}$	$E_{hp} = 0.07$
$R_1 = 1 \, \Omega$	$R = 15 \sim 150 \, \Omega$

Figure 3-22 Output voltage and input inductor current waveforms during start-up

3.5.2.4 Dynamic performance of the proposed controller

In the previous section, the proposed SM controller shows better performance over the two existing control schemes. To obtain a more deep understanding of the proposed controller, its dynamic performance applied with POSLL converter is further studied using circuit simulation in this section. Figure 3-23 shows the system start-up performance under nominal input voltage and maximum load.

Figure 3-23 Output voltage and input inductor current during start-up

Figure 3-24 shows the closed-loop system response under step changes of reference voltage. In the simulation, the reference voltage is changed from 20 V to 28 V and then recovers under nominal input voltage and load resistance. The waveform during the first

step change is similar to the startup response. It is then proven that the proposed controller has similar performance under various reference voltages.

Figure 3-24 Output voltage and input inductor current under reference variations

However when the reference voltage is changed from 28V to 20V, the sliding function will temporally leave the sliding surface and maintain positive over a short period. During this period, the switch is off and there is a resonance between inductors L_1 and L_2 and capacitors C_1 and C_3 . This period stops when sliding function reaches the sliding surface again and the switch is turned on. During this period, system is operated in DCM. Zoomed waveforms during this period are shown in Figure 3-25. The period, when system RP is not on the sliding surface, is dependent on system status. It is better to be estimated through simulations or experiments.

Figure 3-25 Sliding function and inductor current during decrease of reference voltage

Figure 3-26 shows the closed-loop system response under step changes of input voltage at nominal load resistance and nominal output voltage. The input voltage is changed from

10V to 14V and then recovers. The overshoot and undershoot in output voltage are less than 8% of the nominal value.

Figure 3-26 Output voltage and input inductor current under input voltage variations

Figure 3-27 is the closed-loop system response under step changes of load resistance at nominal input voltage and nominal output voltage. The load resistance is changed from 147 Ω to 36 Ω and then recovers. When the load resistance is changed from 36 Ω to 147 Ω , the circuit enters DCM for a short period. Similar oscillations of inductor current i_{LI} , as shown in Figure 3-25, can also be seen in Figure 3-27. The overshoot and undershoot in output voltage are less than 8% of the nominal value.

Figure 3-27 Output voltage and input inductor current under load resistance variations

From above simulation results, it is seen that the proposed controller shows outstanding performance in term of reducing current and voltage overshoot, which decreases the required current rating of circuit components. Another advantage of this controller is no steady state error existing in the output voltage as the integrator is already included in the control equation. The proposed controller can also provide consistent dynamic performance under various input voltages. This is inherited from SM control. To further verify the performance of the proposed controller, actual circuit experiments have been done and the results are given in the next section.

3.6 Experimental Results

In this section, experimental results of the proposed SM controllers are provided to verify both the theoretical analysis and circuit simulations. The hardware prototype is developed based on the parameters given in Table 3-1. The experiment circuit is shown in Figure 3-28.

Figure 3-28 Experiment setup of POSLL converter and proposed controller

To decrease the components' voltage and current rating in the control circuit, the sliding function implemented is changed to (3-55).

$$\sigma(X, t) = i_{L1} + 0.2v_o + 354 \int_0^t (v_o - V_r) dt \quad (3-55)$$

The hysteresis band is chosen as 40 mV in this application, which gives about 50 kHz switching frequency. Reference voltage is 4.8V, which means for an output voltage of 24V.

The switch S is using Infineon MOSFET SPA80N10L. Diodes are low voltage drop diodes MBR10100CT. Inductors series resistances are measured and given in Figure 3-13. The inductor current i_{L1} is measured through a 0.1Ω shunt resistor. The hysteresis control is implemented using comparator IC LM319 [131] and RS Flip-flop IC 74LS74 [132]. The photos of the hardware circuits for the POSLL converter and the proposed SM controller are shown in Appendix F.

3.6.1 Start Up Performance

Figure 3-29 shows the experiment waveforms of output voltage v_o and inductor current i_{L1} during start up with a load resistance of 24Ω at nominal input voltage and output voltage. During start-up, the reference voltage is increased from 0V to 4.8V at time zero. In the figure, time scale is 2 ms/div.

Figure 3-29 Output voltage and inductor current during soft start with R=24Ω

Compared with simulation results given in Figure 3-23, it is found that both waveforms are quite similar. The slight difference is the steady state value of inductor current, which

is higher in the experiment results. This is reasonable as the switching losses, magnetic losses, and diode reverse recovery losses are not modeled in the simulation circuit. This will decrease the efficiency of converter and therefore a higher inductor current is required in order to achieve the same output power.

3.6.2 Dynamic Response

Figure 3-30 shows the experiment waveforms under reference voltage changes. Time scale is 2 ms/div. Output voltage scale in the figure is 5V/div with -10V offset and current scale is 0.5A/div with -1.5A offset. The reference voltage is increased from 20V to 28V in Figure 3-30a and is decreased from 28V to 20V in Figure 3-30b. This is achieved by changing the reference voltage between 4V and 5.6V in the hardware circuit. The experiment results are almost the same as the simulation results shown in Figure 3-24.

Figure 3-30 Output voltage and inductor current during step changes of reference voltage

Figure 3-31 is the experiment waveforms under input voltage changes. Time scale is 2 ms/div. In the experiment, output voltage was captured using AC coupling with 2V/div with 4V offset. Input voltage scale is 5V/div with -10V offset and inductor current scale is 0.5A/div with -1.5A offset. In Figure 3-31a, input voltage is decreased from 14V to 10V and it is increased from 10V to 14V in Figure 3-31b. This is achieved by using the step function of electronic DC source. The output voltage overshoots are smaller compared to the simulation results given in Figure 3-26. The reason is the slower change of input voltage during the experiment as shown in Figure 3-31. The change speed of input voltage is actually limited by the test equipment.

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Figure 3-31 Output voltage and inductor current during step changes of input voltage with $R=36\Omega$

Figure 3-32 is the experiment waveforms under load resistance changes. Time scale is 2 ms/div. The output voltage was captured using AC coupling with 2V/div with 4V offset and inductor current scale is 0.5A/div with -1.5A offset. In Figure 3-32a, load resistance is increased from 36Ω to 147Ω and it is decreased from 147Ω to 36Ω in Figure 3-32b. This is achieved by using the step change function of the electronic load. The experiment waveforms are also similar to the simulation results given in Figure 3-27.

Figure 3-32 Output voltage and input inductor current during step changes of load resistance

All above experiment examples confirm the previous theoretical analysis and simulation results of the proposed SM controller. It is also demonstrated that the proposed controller can be implemented in actual application without much trouble compared to the traditional SM controllers, which normally need additional current limit circuit.

3.7 Application on DC Motor Drives

Dc-dc converters are widely used in dc motor drives [1, 4, 6]. The dc motor is not similar as a resistive load. Its terminal voltage is varying when the motor speed changes. Therefore, to the best of the author's knowledge, control of the load as a dc motor is more difficult compared with control of a normal resistive load. In this section, the proposed SM controller with a POEL converter is applied to control a permanent magnet (PM) dc motor [133, 134]. POEL converter is a buck-boost type converter, which makes it desirable for dc motor application.

A typical open-loop DC motor system [135-138] with dc-dc converters is shown in Figure 3-33. The electric model of a dc motor is shown in Figure 3-34.

Figure 3-33 DC motor drive system

Figure 3-34 Electric model of a PM DC motor

The typical PM dc motor model is described as [133, 134]

$$J\dot{\omega}_m(t) = T_d(t) - T_L(t) - B_m\omega_m(t) - T_f(t) \dots\dots\dots (a) \quad (3-56)$$

$$L_a\dot{i}_a(t) = v_m(t) - R_a I_a(t) - v_{emf}(t) \dots\dots\dots (b)$$

$$v_{emf}(t) = K_E\omega_m(t) \dots\dots\dots (c)$$

$$T_d(t) = K_T i_a(t) \dots\dots\dots (d)$$

where

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v_{emf}	motor electromotive force
v_m	terminal voltage of the motor, V
i_a	armature current, A
R_a	armature resistance, Ω
L_a	armature inductance, H
J	motor and load inertia, $kg \cdot ms^{-2}$
ω_m	motor angular speed, $rad \cdot s^{-1}$
B_m	viscous friction coefficient, $N \cdot m \cdot s$
T_d	Developed torque
T_f	coulomb friction coefficient, $N \cdot m$
T_L	load torque, $N \cdot m$
K_T	motor torque constant, $N \cdot m \cdot A^{-1}$
K_E	motor EMF constant, $V \cdot rad^{-1} \cdot s$

Figure 3-34 shows that a dc motor can not be treated as a resistive load. For dc motor applications, the dynamic response of dc-dc converter is much faster than the mechanical part, which means a two-loop controller for dc motor is applicable: the inner loop can be used to control the motor current or voltage, the outer loop is used to control the motor speed. Normally current response of a fourth-order converter is much slower compared to a second-order Buck converter. In such a situation, current mode control is not desirable. Therefore, in this application the controller inner loop will be used to control the motor terminal voltage instead of current. Figure 3-35 shows the dc-dc converter with a motor load.

Figure 3-35 POEL converter with DC motor as load

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The state vector of above system can be chosen as

$$X = [i_{L1} \quad v_{C1} \quad i_{L2} \quad v_o \quad i_o]^T \quad (3-57)$$

When the switch is on, the state-space equation can be written as

$$\dot{X} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2} \\ 0 & 0 & 0 & \frac{1}{L_a} & -\frac{R_a}{L_a} \end{bmatrix} X + \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ \frac{V_{in}}{L_2} \\ 0 \\ -\frac{V_{emf}}{L_a} \end{bmatrix} \quad (3-58)$$

When the switch is off, the state-space equation is

$$\dot{X} = \begin{bmatrix} 0 & -\frac{1}{L_1} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2} \\ 0 & 0 & 0 & \frac{1}{L_a} & -\frac{R_a}{L_a} \end{bmatrix} X + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ -\frac{V_{emf}}{L_a} \end{bmatrix} \quad (3-59)$$

Define the duty cycle as d , the state-space averaged model can be derived from (3-58) and (3-59) as

$$\dot{X} = \begin{bmatrix} 0 & -\frac{1-d}{L_1} & 0 & 0 & 0 \\ \frac{1-d}{C_1} & 0 & \frac{-d}{C_1} & 0 & 0 \\ \frac{d}{L_2} & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2} \\ 0 & 0 & 0 & \frac{1}{L_a} & -\frac{R_a}{L_a} \end{bmatrix} X + \begin{bmatrix} \frac{dV_{in}}{L_1} \\ 0 \\ \frac{dV_{in}}{L_2} \\ 0 \\ -\frac{V_{emf}}{L_a} \end{bmatrix} \quad (3-60)$$

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The sliding surface for output voltage control is chosen as

$$\sigma_{mt}(x, t) = \kappa_1 x_1 + \kappa_4 x_4 + \int_0^t (x_4 - V_r) dt \quad (3-61)$$

where

κ_1 input current coefficient, $\Omega \cdot s$

κ_4 output voltage coefficient, s

The switch law is the same as the one given in (3-27). Using the same method as Section 3.4, it is found that the coefficients of (3-61) should satisfy below equation according to the existence and reaching conditions of SM control.

$$\begin{aligned} \kappa_1 &\geq \frac{L_1}{V_{in}} V_r \\ \kappa_4 &> 0 \end{aligned} \quad (3-62)$$

Since the current reference and V_{emf} are varying according to different velocity of the motor, the coefficients k_1 and k_4 are then chosen based on the maximum possible V_{emf} .

The equivalent control input can be derived from (3-19), (3-60) and (3-61), which is

$$d_{eq} = \frac{\kappa_1 x_2 - \frac{\kappa_4 L_1}{C_2} (x_3 - x_5) - L_1 (x_4 - V_r)}{\kappa_1 (x_2 + V_{in})} \quad (3-63)$$

Substituting above equation into (3-60), the closed-loop system state-space equation is obtained as

$$\dot{X} = \begin{cases} -\frac{\kappa_4}{\kappa_1 C_2} (x_3 - x_5) - \frac{1}{\kappa_1} x_4 + \frac{1}{\kappa_1} V_r \\ \frac{1}{C_1} x_1 - \frac{(x_1 + x_3)(\kappa_1 x_2 - \frac{\kappa_4 L_1}{C_2} (x_3 - x_5) - L_1 (x_4 - V_r))}{\kappa_1 C_1 (V_{in} + x_2)} \\ \frac{1}{L_2} x_2 - \frac{1}{L_2} x_4 - \frac{\frac{\kappa_4 L_1}{C_2} (x_3 - x_5) - L_1 (x_4 - V_r)}{\kappa_1 L_2} \\ \frac{1}{C_2} x_3 - \frac{1}{C_2} x_5 \\ \frac{1}{L_a} (x_4 - R_a x_5 - V_{emf}) \end{cases} \quad (3-64)$$

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It can be obtained from (3-64) that the closed-loop system has only one equilibrium point as

$$X_{eq} = \begin{bmatrix} \frac{V_r(V_r - V_{emf})}{V_{in}R_a} & V_r & \frac{V_r - V_{emf}}{R_a} & V_r & \frac{V_r - V_{emf}}{R_a} \end{bmatrix}^T \quad (3-65)$$

The closed-loop system can be linearized in the vicinity of the operating point by introducing small perturbations. The linearization leads to

$$\begin{aligned} \delta \dot{X} &= A_{mt} \delta X + B_{mt} \delta v_r \\ \delta v_o &= C_{mt} \delta X \end{aligned} \quad (3-66)$$

$$A_{mt} = \begin{bmatrix} 0 & 0 & 0 & -\frac{\kappa_5}{\kappa_1 L_a} & \frac{\kappa_5 R_a}{\kappa_1 L_a} - \frac{1}{\kappa_1} \\ \frac{V_{in}}{C_1(V_{in} + V_r)} & -\frac{V_r - V_{emf}}{C_1 R_a(V_{in} + V_r)} & \frac{\kappa_4 L_1(V_{in} + V_r)(V_r - V_{emf}) - \kappa_1 C_2 V_r}{\kappa_1 C_1 C_2 V_{in} R_a(V_{in} + V_r)} & \frac{L_1(V_r - V_{emf})}{V_{in} \kappa_1 R_a C_1} & -\frac{\kappa_4 L_1(V_r - V_{emf})}{\kappa_1 C_1 C_2 V_{in} R_a} \\ 0 & \frac{1}{L_2} & -\frac{\kappa_4 L_1}{\kappa_1 L_2 C_2} & \frac{L_1 - \kappa_1}{\kappa_1 L_2} & \frac{\kappa_4 L_1}{\kappa_1 L_2 C_2} \\ 0 & 0 & \frac{1}{C_3} & 0 & -\frac{1}{C_2} \\ 0 & 0 & 0 & \frac{1}{L_a} & -\frac{R_a}{L_a} \end{bmatrix}$$

$$B_{mt} = \begin{bmatrix} \frac{1}{\kappa_1} & -\frac{L_1(V_r - V_{emf})}{V_{in} \kappa_1 R_a C_1} & -\frac{L_1}{\kappa_1 L_2} & 0 & 0 \end{bmatrix}^T$$

$$C_{mt} = [0 \quad 0 \quad 0 \quad 1 \quad 0]$$

Equation (3-66) describes the dynamic performance of the inner voltage control loop. The transfer function between the reference voltage and the converter output voltage can be obtained from (3-66) as

$$G_{dc}(s) = \frac{V_o(s)}{V_r(s)} = C_{mt} \bullet (sI - A_{mt})^{-1} \bullet B_{mt} \quad (3-67)$$

The sliding coefficients k_1 and k_4 can be chosen to achieve an acceptable system performance. The procedure is the same as described in Section 3.4 and it is ignored here.

The transfer function between the armature current and the angular speed can be obtained from (3-56) as

$$G_{\omega o}(s) = \frac{\omega(s)}{V_o(s)} = \frac{\omega(s)}{I_o(s)} \bullet \frac{I_o(s)}{V_o(s)} = \frac{K_T}{Js + B_m} \bullet \frac{1}{L_a s + R_a} \quad (3-68)$$

Since the dc-dc converter has a relatively higher bandwidth than the outer speed regulation loop, it is then reasonable to assume the inner loop as a unit-gain block when designing the outer loop regulator $G_{wc}(s)$ of the motor control system. The block diagram for the design the speed regulator is given in Figure 3-36.

Figure 3-36 Speed control loop

For motor applications, a first order dynamic response with no overshoot is desirable. Therefore, the speed regulator is chosen as follow

$$G_{wc}(s) = \frac{sL_a + R_a}{K_T} \quad (3-69)$$

The resulted open loop transfer function is derived as

$$\frac{\varpi(s)}{\varpi_r(s)} = \frac{1}{Js + B_m} \quad (3-70)$$

Since the maximum terminal voltage and armature current of the motor are limited, modifications on the control system is therefore necessary for practical applications. The overall control scheme of a PM DC motor with a dc-dc converter as power supply is then proposed and shown in Figure 3-37.

Figure 3-37 The control scheme for PM DC motor

In the above control scheme, the limit of current is set directly. The limitation of terminal voltage is achieved through controlling the limit of current, which is

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$$V_{\lim} = I_{\lim} R_a + K_E \varpi_{rate}(t) \quad (3-71)$$

The proposed control scheme is then verified through circuit simulation using PSim. A 60 W PM DC motor is built in the simulation and its parameters are shown in Table 3-3. The parameters of POEL converter and control parameters are also shown in Table 3-3.

Table 3-3 Parameters of PM DC motor and POEL converter

PM DC motor parameters			
$V_{m-rated} = 48 \text{ V}$	$I_{a-rated} = 1.4 \text{ A}$	$B_m = 0.00007 \text{ N}\cdot\text{m}\cdot\text{s}$	$K_E = 0.136 \text{ V}\cdot\text{s}$
$V_{m-max} = 60 \text{ V}$	$I_{a-max} = 2.1 \text{ A}$	$J = 0.00032 \text{ kg}\cdot\text{m}\cdot\text{s}^{-2}$	$\varpi_m = 0 \sim 377 \text{ rad}\cdot\text{s}^{-1}$
$T_f = 0.01 \text{ N}\cdot\text{m}$	$R_a = 3.6 \Omega$	$T_L = 0 \sim 0.26 \text{ N}\cdot\text{m}$	$K_T = 0.136 \text{ N}\cdot\text{m}\cdot\text{A}^{-1}$
$L_a = 1 \text{ mH}$			
POEL converter parameters			
$V_{in} = 24 \text{ V}$	$L_I = 0.5 \text{ mH}$	$L_2 = 0.47 \text{ mH}$	$C_I = 100 \mu\text{F}$
$C_2 = 47 \mu\text{F}$	$f = 50 \text{ kHz}$	$\kappa_1 = 0.01 \Omega \cdot \text{s}$	$\kappa_4 = 0.001 \text{ s}$

Firstly, the controller performance during motor startup is simulated. In this example, the load is $0.16 \text{ N}\cdot\text{m}$ and motor speed is started from zero to $314 \text{ rad}\cdot\text{s}^{-1}$. The motor speed response is shown in Figure 3-38 and the waveform of converter output voltage is shown in Figure 3-39. The torque generated by the motor is shown in Figure 3-40. The waveforms show that the proposed controller gives satisfied performance in term of motor start up speed and converter output voltage response.

The closed-loop control system performance is also examined under load disturbance. In this case, load is increased to $0.24 \text{ N}\cdot\text{m}$ at time 1 s with the motor speed of $314 \text{ rad}\cdot\text{s}^{-1}$ and $T_L = 0.16 \text{ N}\cdot\text{m}$. The speed and voltage responses of the motor are shown in Figure 3-41 and Figure 3-42. The torque generated by the motor is shown in Figure 3-43. From the waveforms, it can be found that the proposed controller is capable of handling such load disturbance.

Figure 3-38 Motor speed response during start-up

Figure 3-39 Converter output voltage during start-up of the motor

Figure 3-40 Motor torque during start-up

Figure 3-41 Motor speed response under load increase

Figure 3-42 Converter output voltage under increase of motor load

Figure 3-43 Motor torque during increase of motor load

The above simulation results and theoretical analysis show that the proposed SM controller can provide satisfied performance when applied on DC motor drives. However, further study on the controller performance under various system conditions is needed, especially considering the influence of motor EMF voltage.

3.8 Summary

In this Chapter, the sliding-mode control for high-order dc-dc Luo converters has been addressed. A new sliding surface has been proposed. It has the same complexity as the traditional multi-loop control scheme. Only two state variables need to be sensed: output voltage and one input inductor current (present in almost all dc-dc converters). It is therefore suitable for almost all dc-dc converters, especially for high-order converters because the control system complexity does not increase when the converter order increases.

By using a reduced order approximation, the POSLL converter is modeled as a fourth-order system. The design procedure for the proposed SM control is shown with this model as an example. The closed-loop system properties such as the reference-to-output transfer function, audio-susceptibility, and output impedance are derived using traditional small-signal method around its operating point. The analysis shows that the proposed controller has several advantages:

- The proposed SM controller can effectively reduce the overshoot in current and voltage during system start up. It also improves the system performance when tracking changes of reference voltage.
- Operating in large signal mode, the controller maintains stability in a large range of operating points. In addition, the theoretical prediction of the closed-loop control system performance is almost not influenced by input variations.
- By changing the proportional part in the sliding surface, the controller can lessen the contradiction between transient and steady state performance for traditional multi-loop controller.
- By using a large integral gain, the system exhibits good performance under various condition changes such as load resistance and input voltage.

Chapter 4 Sliding-Mode Control with Constant Switching Frequency

In Chapter 3, SM controller for dc-dc converters has been studied. A new sliding surface has been proposed. The main feature of the new sliding surface is using an integrator part instead of the conventional reference part. By doing so, the system RP can start from the sliding surface initially and no reaching time is needed. Therefore system dynamic performance during startup is highly improved. Smaller overshoots and shorter settling time in output voltage response during start up are achieved in the proposed new controller. Simulations and experiments of the proposed new SM controller applied with POSLL converter have also been given in Chapter 3 to verify the theoretical analysis.

It is well known that SM control requires infinite switching frequency to maintain the tracking capability and system RP stays ideally on the sliding surface. However in practical, it is not possible to achieve infinite switching frequency. Hence, many frequency limitation methods have been proposed in the last decades [84][84, 87]. Trade-off is the robustness of the system. Although the switching frequency can be limited in certain extent, these methods are normally difficult to be implemented in practical as additional control circuits are needed and they are also sensitive to noise.

Equivalent control has been widely used for theoretical analysis of system dynamics under sliding mode control [67, 68]. The further research in references [75, 77-79, 90-92] has provided the theoretical basis for use of equivalent control as a duty cycle control. However, less attention has been paid on the actual implementation of equivalent SM controller and other related issues. For example, the equivalent control input is obtained when system RP is on the sliding surface. In practical, the system RP may leave sliding surface temporarily and the equivalent control equation is no longer valid. The system response under equivalent control during dynamics has not been addressed in existing publications.

Chapter 4 Sliding-Mode Control with Constant Switching Frequency

In this chapter a lot of efforts are therefore given to address these issues. A practical feasible equivalent SM controller is proposed in this chapter. The main idea is to apply the traditional pulse-width-modulation method to implement the proposed SM controller. In the proposed controller, the switching frequency is fixed using external clock source. As this controller is developed from conventional SM control equations, it is also entitled the many advantages of SM control, such as large-signal stability and rapid dynamic response. Simulation and experiment are also done and shown in this chapter to verify the performance of the proposed method.

4.1 The Proposed Equivalent SM Control

Dc-dc converter bilinear state-space model is shown as [77, 78]

$$\dot{X} = F_1(X, t) + F_2(X, t)u \quad (4-1)$$

The traditional sliding surface is the combination of state variables

$$\sigma(X, t) = GX + \varphi = 0 \quad (4-2)$$

G is a vector expressed as $G = [g_1, g_2, \dots, g_N]$. $g_1, g_2, \dots$ and g_n are positive constants. φ is the reference value derived from system state-space equation and operating point. Under sliding mode, it should satisfy

$$\dot{\sigma} = 0 \Rightarrow G\dot{X} + \dot{\varphi} = 0 \quad (4-3)$$

Since φ is constant, (4-3) leads to

$$G(F_1(X, t) + u_{eq}F_2(X, t)) = 0 \quad (4-4)$$

Assumed that $[GF_2]^{-1}$ exists, the equivalent control is obtained as

$$u_{eq} = -(GF_2(X, t))^{-1}GF_1(X, t) \quad (4-5)$$

The dynamics of the closed-loop system can be described as

$$\dot{X} = [I - F_2(X, t)(GF_2(X, t))^{-1}G]F_1(X, t) \quad (4-6)$$

The equivalent control input given in (4-5) contains no information of the reference. Therefore the equivalent control can not be directly applied. In this thesis, it is proposed

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that the reference part is replaced by a function of reference voltage. The order of the function over the reference voltage should be higher than 1, which ensures that the derivative of this sliding function still contains the reference information. In addition, the derivative of φ should be zero in steady state, which ensures the system dynamic characteristics are maintained almost the same as the original equivalent SM controller.

Considering above requirements, using the integration of the error between the output voltage and the reference voltage is recommended in this thesis. Therefore, the proposed sliding surface can be described as

$$\begin{aligned}\sigma(x, t) &= GX + \int_0^t (v_o - V_r) dt \\ \varphi &= \int_0^t (v_o - V_r) dt\end{aligned}\tag{4-7}$$

It is found in above equation that the derivative of φ contains the information of reference voltage and it equals to zero under steady state. Under steady state, this controller operates exactly the same as the one shown in (4-2). Appropriate selection of G_X is critical for the realization of proposed controller. It has been proven in Chapter 3 that part of the state information is enough to achieve satisfactory performance. It is therefore not necessary to set all components of matrix G to be none-zero values. The equation to calculate the equivalent control changes to (4-8).

$$u_{eq} = -[GF_2]^{-1}[GF_1(X, t) + (v_o - V_r)]\tag{4-8}$$

The general diagram of this proposed approach is shown in Figure 4-1. To avoid the influence of ripple components, low-pass filter is needed in the closed-loop control. The cross-over frequency of the low-pass filter should be much higher than the bandwidth of the controller and much lower than the switching frequency. There are many choices of cross-over frequency and each will give similar response if the above two conditions are satisfied.

Figure 4-1 Control scheme of the equivalent SM control

4.2 Design of the Equivalent SM Control for POSLL Converter

4.2.1 State-space Equations

Since the sliding surface proposed in Chapter 3 satisfies the requirements of equivalent control application, it is therefore re-used by setting $G = [g_i \ 0 \ 0 \ 1]$. Equation (4-7) changes to (4-9).

$$\sigma(X, t) = g_i i + v + g_v \int_0^t (v - V_r) dt \quad (4-9)$$

$$d_{eq} = \frac{2\alpha g_i C_3 (x_1 + x_3) + g_i C_3 x_2 - \sqrt{(g_i C_3 x_2)^2 + 4\alpha g_i C_3 (x_1 + x_3) [g_i C_3 v_{in} + L_1 (x_3 - \frac{x_4}{R}) + g_v L_1 (x_4 - V_r)]}}{2\alpha g_i C_3 (x_1 + x_3)} \quad (4-10)$$

Unfortunately, the equivalent control input shown in (4-10) is extremely complicated. This is because the comprehensive POSLL converter model (Model 1 in Chapter 3) is used here, in which the second order of duty cycle is involved. As above model is not practically applicable, the simplified state-space model of POSLL converter (Model 2 in Chapter 3) is then employed to derive the equivalent control. The new equivalent controller is obtained as

$$d_{eq} = \frac{g_i (x_2 + (\lambda_1 - 1)x_4 - v_{in}) - \frac{L_1}{C_3} (x_3 - \frac{x_4}{R}) - g_v L_1 (x_4 - V_r)}{g_i (x_2 + (\lambda_1 - 1)x_4)} \quad (4-11)$$

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To simplify the analysis, all the circuit components are assumed to be lossless. The closed-loop control system state-space equation is then obtained by combining the control law, which is shown in (4-11), with the converter equations. POSLL Model 1 is used here to derive the state-space equation as it is more accurate under both transient and steady state. The state-space equation of closed loop system is:

$$\dot{X} = \begin{bmatrix} \frac{-\alpha(1-d_{eq})^2}{L_1} & \frac{-(1-d_{eq})}{L_1} & \frac{-\alpha(1-d_{eq})^2}{L_1} & 0 \\ \frac{1-d_{eq}}{C_1} & 0 & \frac{d_{eq}}{C_1} & 0 \\ -\frac{\alpha(1-d_{eq})^2}{L_2} & \frac{d}{L_2} & \frac{-\alpha(1-d_{eq})^2}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & \frac{1}{C_3} & \frac{-1}{RC_3} \end{bmatrix} X + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 1 \\ \frac{L_2}{0} \end{bmatrix} v_{in} \quad (4-12)$$

Equation (4-12) has only one equilibrium point. It can be derived by setting the left side of (4-12) equal to zero. The equilibrium point is

$$X_{eq} = \begin{bmatrix} \frac{V_r(\lambda_1 V_r - V_{in})}{RV_{in}} & V_r & \frac{V_r}{R} & V_r \end{bmatrix}^T$$

$$D_{eq} = \frac{\lambda_1 V_r - V_{in}}{\lambda_1 V_r} \quad (4-13)$$

Applying small signal variations in the vicinity of the operation point, system linearization model is obtained as

$$\delta \dot{X} = A_{ES} \delta X + B_{ESVIN} \delta v_{in} + B_{ESVR} \delta v_r + B_{ESZ} \delta i_O \quad (4-14)$$

where

$$A_{ES} = \begin{bmatrix} -\frac{\alpha V_{in}^2}{L_1 \lambda_1^2 V_r^2} & \frac{(\lambda_1 - 1)V_{in}}{L_1 \lambda_1^2 V_r} \\ \frac{V_{in}}{V_r C_1 \lambda_1} & -\frac{1}{RC_1 \lambda_1} \\ -\frac{\alpha V_{in}^2}{L_2 \lambda_1^2 V_r^2} & \frac{\lambda_1^2 V_r + (\lambda_1 - 1)V_{in}}{L_2 \lambda_1^2 V_r} \\ 0 & 0 \end{bmatrix}$$

$$\begin{aligned}
 & \left[\begin{array}{c} \frac{2\lambda_1 - 1}{g_i C_3 \lambda_1} - \frac{\alpha V_{in}^2}{L_1 \lambda_1^2 V_r^2} \\ \frac{V_{in} - V_r \lambda_1}{V_r C_1 \lambda_1} \\ -\frac{\alpha V_{in}^2}{L_2 \lambda_1^2 V_r^2} - \frac{L_1 (2\lambda_1 - 1)}{g_i L_2 C_3 \lambda_1} \\ \frac{1}{C_3} \end{array} \quad \begin{array}{c} \frac{(2\lambda_1 - 1)(L_1 \lambda_1 V_r \frac{1 - g_v RC_3}{RC_3} + g_i (\lambda_1 - 1) V_{in})}{L_1 g_i \lambda_1^2 V_r} \\ \frac{-L_1 \lambda_1 V_r \frac{1 - g_v RC_3}{RC_3} - g_i (\lambda_1 - 1) V_{in}}{g_i C_1 \lambda_1 R V_{in}} \\ \frac{(2\lambda_1 - 1)(L_1 \lambda_1 V_r \frac{1 - g_v RC_3}{RC_3} + g_i (\lambda_1 - 1) V_{in})}{L_2 g_i \lambda_1^2 V_r} \\ -\frac{1}{RC_3} \end{array} \right] \\
 & B_{ESVR} = \begin{bmatrix} \frac{(2\lambda_1 - 1)g_v}{g_i \lambda_1} & -\frac{g_v L_1 V_r}{g_i C_1 R V_{in}} & -\frac{(2\lambda_1 - 1)g_v L_1}{g_i \lambda_1 L_2} & 0 \end{bmatrix}^T \\
 & B_{ESVIN} = \begin{bmatrix} \frac{1 - \lambda_1}{\lambda_1 L_1} & \frac{V_r}{V_{in} RC_1} & \frac{1 - \lambda_1}{\lambda_1 L_2} & 0 \end{bmatrix}^T \\
 & B_{ESZ} = \begin{bmatrix} \frac{2\lambda_1 - 1}{g_i C_3 \lambda_1} + \frac{\alpha V_{in} (2\lambda_1 - 1)}{L_1 \lambda_1^2 V_r} & -\frac{L_1 V_r}{g_i C_3 C_1 R V_{in}} - \frac{\alpha}{C_1 R \lambda_1} \\ \frac{L_1}{L_2} \left(\frac{2\lambda_1 - 1}{g_i C_3 \lambda_1} + \frac{\alpha V_{in} (2\lambda_1 - 1)}{L_1 \lambda_1^2 V_r} \right) & -\frac{1}{C_3} \end{bmatrix}^T
 \end{aligned}$$

To differentiate this equation from the one given in (3-42), all the subscripts of system matrices in this chapter will begin with character “E”.

4.2.2 Implementation Considerations

Before employing (4-14) for system dynamic performance analysis, several points shall be clarified regarding the selection of control parameters and practical implementations.

Firstly, before the switch is turned on, all system parameters are zero. The equivalent control d_{eq} at time zero can be obtained as

$$d_{eq} \Big|_{X=0} = \frac{g_v L_1 V_r - g_i V_{in}}{0} \quad (4-15)$$

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It is seen that the denominator of the above equation is 0. This is no problem for practical implementation as the output of the divider can be saturated. However, in practical d_{eq} shall be larger than 0, which means the numerator of (4-15) shall be positive. This should be satisfied when choosing g_v and g_i .

Secondly, since POSLL converter is a boost type converter, the system will not function properly if the switch is kept on all the switching period, or $d_{eq} = 1$. Therefore the limitation on maximum duty cycle d_{max} , which is less than 1, shall be implemented in the controller.

Thirdly, the circuit operation during start up needs special attention. As shown in Figure 4-2, during start up, as the output voltage is low or zero, there is a path from input voltage through diodes D_1 , D_2 and inductor L_2 to the output terminal. As a result, v_{C1} can be clamped at $-2V_D$ and i_{C3} can increase to a high value due to the resonance between L_2 and C_3 . The duty cycle d_{eq} should be at its maximum or minimum during this period. If the duty cycle d_{eq} is at maximum, the circuit is operated under maximum duty cycle d_{max} . If the duty cycle d_{eq} is at minimum, the switch is remained off and the circuit work in DCM. This period will stop once the output voltage increases to a value which is high enough to stop the resonance. Normally, high overshoot in inductor current and output voltage are observed during this period. This is not acceptable for practical applications. To avoid this, a current limit is required to stop the resonance as fast as possible.

Figure 4-2 POSLL converter during start up

Figure 4-3 Equivalent SM control scheme of POSLL converter

4.3 Simulations

The parameters of POSLL converter is the same as those shown in Table 3-1. From the above analysis, it is known that the worst case happens when the system start up at minimum input voltage, maximum output voltage and power. Therefore, the control parameters for equivalent controller are chosen so that the controlled POSLL converter can start up at worst case. The resulting control parameters are shown as

$$\begin{aligned} g_i &= 5 \Omega \\ g_v &= 3670 \text{ s}^{-1} \end{aligned} \quad (4-16)$$

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To ensure the converter can operate at minimum input voltage and maximum load, the current limit level is chosen at 2.8A. From the control equation, it is known that λ_1 can change when load resistance changes. However it is not economical to vary λ_1 with load resistance as additional circuit is needed. Therefore in this example, λ_1 is fixed at its nominal value, which is $\lambda_1 = 1.028$. The switching frequency of the converter is 50 kHz. Maximum duty cycle is chosen to be 0.95.

4.3.1 Small-Signal Analysis

The performance of the equivalent SM controller is then compared with the controller proposed in Chapter 3 with the same g_i and g_v . The two state-space equations are analyzed using Matlab. Figure 4-4 shows the bode plot of control-to-output transfer functions. Figures 4-5 and 4-6 are the system audio-susceptibility and output impedance at the nominal operation point.

Figure 4-4 Bode plots of $G_{SVR}(s)$ and $G_{ESVR}(s)$

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Figure 4-5 Audio-susceptibility of POSLL converter under SM control and equivalent SM control

Figure 4-6 Output Impedances of POSLL converter under SM control and equivalent SM control

From Figures 4-4 to 4-6, it can be observed that both controllers show similar frequency characteristics although tiny differences exist. This is reasonable as the equivalent control d_{eq} used in two controllers are different. For Chapter 3 controller, Model 1 is used to derive d_{eq} but in this Chapter 4, Model 2 is used. However since the difference between Model 1 and Model 2 under transient state are very small, above two controllers show similar dynamic characteristics.

4.3.2 Circuit Simulations

Circuit simulation is also done using PSim. The simulation step is 100 ns to achieve high accuracy. The simulation circuit of equivalent SM controlled POSLL converter is shown in Figure 4-7.

Figure 4-7 Simulation circuit for POSLL converter under equivalent SM control

In the simulation circuit, control gains K1 to K5 are calculated based on (4-11) and (4-16). There are six step voltage sources, VSTEP1 to VSTEP6, in the simulation. These will be used for simulating the system response under circuit condition changes or reference voltage changes. COMP1 is the PWM comparator and comparator COMP2 is for current limitation. The peak voltage of the ramp signal is set to 5V to improve PWM noise immunity and therefore, the denominator of the controller is multiplied by a factor of 0.2 (K6) before it is input to the divider. The cross-over frequency of two low-pass filters is set to 5.5 kHz to remove the ripple components and achieve rapid dynamic response. The current limitation is implemented by comparing the current sense voltage with a constant voltage source VCL. Later, the effects of current limitation and low-pass filters will be shown in the simulation results.

4.3.2.1 Start up

In this first example, the current limitation is removed when studying the start up performance of equivalent SM controller. The simulation waveforms are shown in Figure 4-8. In the simulation, reference voltage is 24 V, input voltage is 12 V and load resistance is 24 Ω .

Figure 4-8 Simulated waveforms of equivalent SM controlled POSLL converter without current limitation during start up with full load at nominal input voltage

In Figure 4-8, it is clearly shown that resonance occurs just after start up. During resonance period, v_{C1} is clamped at small negative value and duty cycle d_{eq} is at its maximum value. It is seen that this period stops when the capacitor current i_{C3} becomes negative. However, since a large current overshoot is developed on inductor current i_{L1} , this extra energy therefore causes a large overshoot on the output voltage before the resonance stops.

Figure 4-9 is the simulation results during startup when the current limitation is included, which is set to 2.8A. It can be seen that when current i_{L1} reaches the limit, switch S is turned off. v_{C1} then rise up and the duty cycle is decreased. Compared with the results shown in Figure 4-8, the resonance period is much shorter and less energy is stored in inductor L_1 during the resonance. The overshoot of output voltage is therefore greatly

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reduced as shown in the figure. This confirms that an auxiliary current limitation is necessary for the proposed equivalent SM controller on POSLL converter.

Figure 4-9 Simulated waveforms of equivalent SM controlled POSLL converter with 2.8A current limitation during start up with full load at nominal input voltage

The above simulations are conducted under maximum load condition. Another simulation is done when load resistance is $147\ \Omega$. In this condition, the steady state inductor current I_{L1} is quite small compared to the current limit level. The simulation waveforms are shown in Figure 4-10. It is seen that the overshoot of output voltage is almost the same as the one shown in Figure 4-9. The reason is that the energy stored in the inductor during resonance is fixed by the current limitation, which is same for any load condition.

Figure 4-10 Simulated waveforms of equivalent SM controlled POSLL converter during start up with $147\ \Omega$ load at nominal input voltage

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4.3.2.2 Steady state error and selection of low-pass filter

It is known that (4-11) is derived without considering the component loss, such as the series resistance of the inductor, forward voltage drops of diodes. In the actual implementation, steady state error may occur at the output voltage due to these losses. Of course the steady state error can be minimized by using detailed circuit model. But the theoretical analysis would become difficult and it causes trouble when studying influences of various control parameters. In addition, the steady state error can not be totally removed even using detailed models. The reason is that the equivalent controller is of type 0, which inherently develops steady state error when tracking a constant reference.

There are also another two factors which may affect the steady state error of the proposed equivalent controller. The first one is ripple components on circuit variables. To derive the equivalent control, state-space averaging method is used. The assumption of state-space averaging method is that the ripple components for any variable is very small compared to its dc components and can be ignored. Therefore, the variables used in (4-11) are only their dc parts. Unfortunately if comparing Figure 4-11 and Figure 4-12, it is found that the influence of ripple components cannot be ignored in the proposed controller. Figure 4-12 is the controller performance with a low pass filter, which removes the effect of ripple components. Such a filter is not included in the simulation for Figure 4-11. In Figure 4-11, it is seen that the reference voltage is 24V while the actual output voltage is 21.96V. The steady state error is 2.04V. The ripple component of the voltage v_{CI} is more than 0.8V, or around 3.5% of its dc value. For capacitor current i_{C3} , its dc component is zero at steady state. However, its ripple current is 0.2A! These ripple components then develop ripple component in the calculated equivalent duty cycle d_{eq} , which leads to the steady state error. However in Figure 4-12, the steady state error in output voltage is 1.68V and it is 15% less than the results given in Figure 4-11.

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Figure 4-11 Simulated waveforms of equivalent SM controlled POSLL converter without low-pass filters under full load and nominal input voltage

Figure 4-12 Simulated waveforms of equivalent SM controlled POSLL converter with low-pass filters under full load and nominal input voltage

The second factor influencing the steady state error is the VLC coefficient λ_1 . It is a fixed value in the proposed controller based on the nominal load condition. When the load condition changes, it can also develop some steady state error. This is verified in Figure 4-13. It is seen that the output voltage increases when the load resistance increases.

Figure 4-13 Output voltage of equivalent SM controlled POSLL converter at different load resistance

4.3.2.3 Dynamic response

In this section, the dynamic responses of the equivalent SM controlled POSLL converter under various system condition changes are examined. In the following examples, only one system condition is changed in each simulation and other circuit parameters are maintained at nominal values.

Figure 4-14 shows the simulation waveforms during reference voltage changes. In the simulation, reference voltage is increased from 20 V to 28 V at 20 ms and then recovered at 40 ms.

Figure 4-14 Simulated waveforms of equivalent SM controlled POSLL converter during reference variations

The figure shows that the duty cycle is well constrained between its maximum value (5) and its minimum value (0) during all the transients. This means the switching frequency is only controlled by the ramp signal. It can therefore be concluded that the switching frequency is kept at constant.

Figure 4-15 shows waveforms under input voltage variations. The input voltage is increased from 10V to 14V at 20 ms and recovered at 40 ms. Figure 4-16 is the results under load resistance changes. In the simulation, load resistance is decreased from 147 Ω to 36 Ω at 20 ms and recovered at 40 ms.

Similar results as shown in Figure 4-14 are seen in these two examples. The equivalent duty cycle is maintained within its max and min values. Therefore, constant switching frequency is achieved during transient states.

Figure 4-15 Simulated waveforms of equivalent SM controlled POSLL converter during input voltage changes

Figure 4-16 Simulated waveforms of equivalent SM controlled POSLL converter during load changes

Through the comparison between Figures 3-24 and 4-14, differences between the equivalent SM controller and the SM controller given in Chapter 3 can be found as

- Equivalent SM controller shows larger current overshoot during step up of reference voltage. This is because the voltage coefficient in equivalent SM controller is 3670, which is larger than the value used for Chapter 3 simulation.
- Equivalent SM controlled system has shorter settling time than SM controlled system. The settling times captured in two systems are shown in Table 4-1. It shows that equivalent SM controller shows better reference tracking performance than SM controller. This is also partly caused by the fact that equivalent SM controller has no effect of integration and has steady state error in the output voltage.

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- SM controlled system will enter into DCM operation in case of reference voltage decreasing. For equivalent SM controlled system, this problem no longer exists as the duty cycle is kept within 0 and 5 and the converter is always under control.

Table 4-1 Comparison of settling times for equivalent SM and SM controllers

		Equivalent SM controller	SM controller
reference	Steady state value and range	$26.7 \pm 0.53 \text{ V}$	$28 \pm 0.56 \text{ V}$
step up	Settling time	2.25 ms	3.47 ms
reference	Steady state value and range	$18.62 \pm 0.37 \text{ V}$	$20 \pm 0.40 \text{ V}$
step down	Settling time	2.02 ms	3.20 ms

In this section, circuit simulations have been conducted to verify the theoretical analysis of the proposed equivalent SM controlled POSLL converter. Compared to SM controller given in Chapter 3, equivalent SM controller is more convenient for practical application as no hysteresis control is needed and its switching frequency is fixed. Equivalent SM controller also shows shorter settling time than the SM controller. Disadvantage of the equivalent controller is the current overshoot problem during start up. However, this issue can be mitigated by applying a current limitation. To further verify the proposed controller performance, experiments on the equivalent controller are conducted in the next section.

4.4 Experiments on Equivalent SM Controlled POSLL Converter

Experiments are done in this section to verify the performance of equivalent SM controlled POSLL converter. To decrease energy consumption in the calculation circuit, voltage variables are sensed with a ratio of 0.2. Current variables are sensed with $0.1 \text{ } \Omega$ shunt resistors. Nominal reference voltage is 4.8V. POSLL converter used for experiment is the same as the one used in the previous chapter. The hardware circuit of the equivalent SM controlled POSLL converter is shown in Figure 4-17.

The experiment waveforms of the ramp signal and other variables are shown in Figure 4-18. In the experiment, scales and offset for each channel are: CH1 is output voltage (v_O) with 5V/div and -10V offset; CH2 is ramp voltage (V_{ramp}) with 1V/div and -3V offset;

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CH3 is inductor current (i_{L1}) with 0.2A/div and -0.5A offset; CH4 is 5 times of duty cycle ($5d_{eq}$) with 1V/div and -3V offset. In the example, output voltage is 22V, load resistance is $36\ \Omega$ and input voltage is 12V. It can be seen that the ripple of equivalent control is quite small as it has been reduced using the low-pass filters. As d_{eq} is between its maximum and minimum limits, the switching frequency is fixed by the ramp signal.

Figure 4-18 Experimental waveforms of equivalent SM controlled POSLL converter

With above hardware circuit, the performance of the closed-loop system is studied. The experiment waveforms during system start up under light load ($R = 147\ \Omega$) and full load ($R = 24\ \Omega$) are shown in Figure 4-19. In these figures, output voltage scale is 10V/div with 0V offset and current scale is 1 A/div with -3A offset. The scale of d_{eq} is 5 V/div with 10V offset. Time scale is 2 ms/div. The waveforms are quite similar to the simulation results given in Figure 4-9 and Figure 4-10, which then verify the performance of the proposed controller. Of course slight differences can be observed. Output voltage response is also found to be slower in the experiment results. This is possible due to the losses which are not include in the simulation

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(a) $R = 24 \Omega$

(b) $R = 147 \Omega$

Figure 4-19 Experimental waveforms of equivalent SM controlled POSLL converter during start up

Experiments are also conducted to verify the system response under condition changes, which include reference voltage changes, input voltage changes and load resistance changes. These experimental waveforms are shown in Figures 4-20 to 4-22. In all the three figures, time scale is 2 ms/div.

Figure 4-20 shows the results under step changes of reference, which is increased from 20V to 28V in Figure 4-20a and decreased from 28V to 20V in Figure 4-20b. In the figures, output voltage scale is 5 V/div with -10V offset, inductor current scale is 1 A/div with -1A offset and equivalent duty cycle scale is 2 V/div with -6V offset. It is found that the experiment waveforms are similar to the simulation waveforms shown in Figure 4-14.

(a) V_r : 20 V to 28 V

(b) V_r : 28 V to 20 V

Figure 4-20 Experimental waveforms of equivalent SM controlled POSLL converter under reference voltage variations

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Figure 4-21 shows the experiment waveforms under input voltage changes. In the experiment, input voltage is decreased from 14 V to 10 V in Figure 4-21a and is increased from 10V to 14V in Figure 4-21b. In Figure 4-21a, output voltage scale is 2 V/div with -18V offset, inductor current scale is 1 A/div with -1A offset and equivalent duty cycle scale is 2 V/div with -6V offset. In Figure 4-21b, output voltage scale is 5 V/div with -10V offset, inductor current scale is 0.5 A/div with -0.5A offset, and equivalent duty cycle scale is 2 V/div with -6V offset. The output voltage overshoots are smaller compared to the simulation results. This is because the changes of input voltage are not as fast as a step change.

Figure 4-21 Experimental waveforms of equivalent SM controlled POSLL converter under input voltage variations

Figure 4-22 shows the experiment waveforms under load resistance changes, which is decreased from 147 Ω to 36 Ω in Figure 4-22a and increased from 36 Ω to 147 Ω in Figure 4-22b. In the figures, output voltage scale is 5 V/div with -5V offset, inductor current scale is 0.2 A/div with -0.6A offset, and equivalent duty cycle scale is 1 V/div with zero offset. Also the waveforms are quite similar to the simulation results shown in Figure 4-16. There is less oscillations on the output voltage response in this experiment due to the switching losses.

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Figure 4-22 Experimental waveforms of equivalent SM controlled POSLL converter under load variations

All the above experiment results confirm the previous theoretical analysis and simulation results. Compare to the SM control given in Chapter 3, the switching frequency is well fixed in all operation conditions. The main disadvantage of equivalent SM controlled POSLL converter is the unsatisfied start up performance. An auxiliary current limitation has to be applied to limit the inductor current during start up.

4.5 Equivalent SM Control for Other Converters

The equivalent SM controlled POSLL converter shows unsatisfied performance during startup and additional current limiter is required. However, analysis shows that this is not common for all equivalent SM controlled converters. This is actually dependent on the converter to be controlled. In this section, the performance of an equivalent SM controlled POEL converter is analyzed, which will demonstrate that the current limiter is not required in this application. Comparison of SM control and equivalent control based on POEL converters will also be discussed in this section. Derivations of the close-loop system equations and small signal analysis for the equivalent SM controlled POEL converter are ignored as the procedure is similar to that given for POSLL converter. Circuit diagram of POEL converter is shown in Figure 4-23.

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Figure 4-23 POEL converter

The state-space equation of the POEL converter can be derived as

$$\dot{X} = \begin{bmatrix} 0 & \frac{(1-d)}{L_1} & 0 & 0 \\ \frac{(1-d)}{C_1} & 0 & \frac{d}{C_1} & 0 \\ 0 & \frac{d}{L_2} & 0 & \frac{-1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{RC_2} \end{bmatrix} X + \begin{bmatrix} \frac{d}{L_1} \\ 0 \\ \frac{d}{L_2} \\ 0 \end{bmatrix} v_{in} \quad (4-17)$$

where the state vector X is $[i_{L1} \quad v_{C1} \quad i_{L2} \quad v_{C2}]^T$.

The same sliding surface is used for POEL converter and it is rewritten here as

$$\sigma(X, t) = g_i i_{L1} + v_O + g_v \int_0^t (v_O - V_r) dt \quad (4-18)$$

The equivalent control d_{eq} can be obtained as

$$d_{eq} = \frac{g_i v_{C1} - \frac{L_1}{C_2} i_{C2} - g_v L_1 (v_O - V_r)}{g_i (V_{in} + v_{C1})} \quad (4-19)$$

From (4-19), it can be seen that denominator of d_{eq} is not zero at the beginning of start up. There is no chance for d_{eq} to go to maximum value. This confirms that there is no excessive large current overshoot for POEL converter. Therefore the additional current limiter is not required for this converter.

Simulation results are then given to compare the performance of SM controlled and equivalent SM controlled system. Simulation setup is similar as those used for POSLL

converters. The desired output voltage for POEL converter is 24 V. The control parameters for both controllers are chosen as

$$\begin{aligned} g_i &= 5 \, \Omega \\ g_v &= 1700 \, \text{s}^{-1} \end{aligned} \quad (4-20)$$

Figure 4-24 shows waveforms of POEL converter during start up. In the simulation, input voltage of the converter is 12V and load resistance is $24 \, \Omega$. Figure 4-24a shows the performance of SM controller and Figure 4-24b is the waveforms from equivalent SM controller. As there is steady state error for equivalent SM control, the reference voltage in Figure 4-24b is 25.8 V in order to achieve an actual output voltage of 24V.

Figure 4-24 Simulated waveforms of POEL converter controlled by both controllers during start up at $24 \, \Omega$

From Figure 4-24, it can be seen that equivalent SM control show better performance in terms of oscillation on and settling time of the output voltage. Under system condition changes, simulations will show similar results. Those simulation waveforms are ignored in this thesis.

4.6 Summary

In this Chapter, an equivalent SM control has been proposed for dc-dc converters. In the proposed method, traditional sliding surface has been modified so that equivalent SM control can be applied. The proposed control method has been applied to both POSLL

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converter and POEL converter. Based on these two application examples, the advantages and disadvantages of equivalent SM control can be summarized as follows.

With the proposed controller, the switching frequency can be fixed under all circuit conditions. Much design work on the input/output EMI filter can therefore be avoided.

Advantages of equivalent SM control include:

- Fixed switching frequency operation with PWM based control under all operation conditions. Much design work on the input/output EMI filter can be avoided.
- The practical implementation of the controller is simplified. Only one PWM comparator is required for equivalent SM control. However for SM controller, two comparators with Set-Reset flip-flop are required.
- Good dynamic response under load resistance, input voltage and reference voltage variations

Disadvantages of equivalent SM control include:

- It has steady state error inherently. It is also necessary to note that the occurrence of steady state error depends on the sliding surface used and the converter to be controlled.
- For some converters, this controller may show large overshoots in both output voltage and inductor current during start up. An auxiliary comparator for current limit is required.
- A divider circuit is required in the control circuit. Such a circuit is normally not easy to be implemented and cost can be high.

Chapter 5 Improvements on Equivalent Sliding-Mode Control

The equivalent SM control scheme has been proposed in Chapter 4. In the proposed control scheme, the equivalent duty cycle of a sliding mode controller is calculated and applied as the control signal. From this point of view, the proposed equivalent control can be considered as a PWM based controller with nonlinear feedback. The main advantage of the proposed control is that its switching frequency is fixed by the ramp signal. As it is still one kind of SM controller, the advantages of SM control are also retained, which include large signal stability and fast dynamic response during condition changes.

In Chapter 4, it has been discussed that one of the disadvantages of equivalent SM control is the non-zero steady state error in output voltage. In this chapter, an adaptive type equivalent SM controller is therefore proposed to overcome this issue. The basic principle of adaptive control is to estimate the loss items in the dc-dc converter and adjust the equivalent duty cycle accordingly. In this chapter, a detailed converter model is derived firstly. Conduction losses of inductors, diodes, and switches are considered in this model. The model forms the basis for theoretical analysis of converter power losses. Based on the analysis results, a reasonable simplified converter model is derived and then incorporated with adaptive algorithm for estimation of the power losses. Once the loss items have been taken into consideration, the steady state error can be thoroughly removed using the adaptive scheme. Stability and dynamic response of the closed-loop system are studied. Simulations and experiments result are given to verify the analysis.

In the equivalent SM controller proposed in Chapter 4, a divider circuit has been used to derive the equivalent duty cycle. However in practical controllers for dc-dc converters, divider function involves complicated circuit design and the cost is normally high. Therefore in Chapter 5, the concept of OCC is introduced to remove the divider. Such an

improvement can achieve same control performance but the practical implementation is much more simplified. Simulations and experiments results will also be given.

5.1 Steady State Error

In this section, an adaptive type equivalent SM controller is proposed to remove the steady state error on the output voltage.

5.1.1 Dc-dc Converter Model with Power Losses

Power losses in dc-dc converters are mainly contributed by three parts including conduction loss, switching loss and magnetic loss. The switching losses mainly comes from: power dissipations on the switches, which can be modeled as a switch-on drain-source resistor r_S ; power dissipation due to the parasitic effect of inductor, which can be modeled as a series resistor r_L ; the diode forward voltage drop, which can be modeled as an anti-series voltage source V_D in diode's on-state. The equivalent series resistance of a capacitor is very small and is ignored in the present analysis.

To examine the effect of power losses, a Buck converter is chosen for theoretical analysis due to its simple but representative configuration. A Buck converter with above-mentioned power losses is shown in Figure 5-1. The equivalent circuits of this converter are shown in Figure 5-2.

Figure 5-1 Buck converter with power losses

Figure 5-2 Equivalent circuits of Buck converter in different switch states

The inductor current and capacitor voltage are chosen as state variables,

$$X = [i_L, v_O]^T \quad (5-1)$$

When switch S is turned on, the state-space equation of the Buck converter is obtained as

$$\dot{X} = A_1 X + B_1 \quad (5-2)$$

$$A_1 = \begin{bmatrix} -\frac{(r_S + r_L)}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{V_{in}}{L} & 0 \end{bmatrix}^T$$

When switch S is turned off, the state-space equation of Buck converter is derived as

$$\dot{X} = A_2 X + B_2 \quad (5-3)$$

$$A_2 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} -\frac{V_D}{L} & 0 \end{bmatrix}^T$$

Assuming the duty cycle is d . Combining (5-2) and (5-3) leads to the state-space averaged model of Buck converter, which is shown as

$$\dot{X} = A_3 X + B_3 \quad (5-4)$$

$$A_3 = \begin{bmatrix} -\frac{r_S d + r_L}{L} & \frac{-1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$B_3 = \begin{bmatrix} \frac{V_{in} d - V_D(1-d)}{L} & 0 \end{bmatrix}^T$$

The VTG can be obtained by solving (5-4) in the steady state as

$$M_1 = \frac{V_O}{V_{in}} = \frac{d - \frac{V_D}{V_{in}}(1-d)}{1 + \frac{r_S d + r_L}{R}} \quad (5-5)$$

Equation (5-5) shows how the VTG is influenced by different circuit parameters.

However in above model, three loss parameters are included. These cause great trouble in applying adaptive control method. Therefore a simplified circuit model is proposed. The main idea is to use only one parameter R_L to represent the original three loss parameters. See the simple circuit model in Figure 5-3. The switch and diode are now considered as ideal ones.

Figure 5-3 Simplified Buck converter with one power loss item R_L

By replacing the power loss items in (5-4) with R_L , the revised state-space averaged equation is derived.

$$\dot{X} = AX + Bd \quad (5-6)$$

$$A = \begin{bmatrix} -\frac{R_L}{L} & \frac{-1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{V_{in}}{L} & 0 \end{bmatrix}^T$$

The modified VTG is obtained from (5-6)

$$M_2 = \frac{V_O}{V_{in}} = \frac{R}{R + R_L} d \quad (5-7)$$

In order to achieve $M_1 = M_2$, it is derived from (5-5) and (5-7) that

$$R_L = \frac{V_{in}d(r_L + r_S d) + RV_D(1-d)}{V_{in}d - V_D(1-d)} \quad (5-8)$$

5.1.2 The Proposed Controller

5.1.2.1 The equivalent sliding-mode controller

The same sliding surface is used for Buck converter as:

$$\sigma(x, t) = GX + \int_0^t (x_2 - V_r) dt = \alpha x_1 + \beta x_2 + \int_0^t (x_2 - V_r) dt \quad (5-9)$$

The measuring unit for α is $\Omega \cdot s$ and the measuring unit for β is s.

The equivalent control is given as

$$d_{eq} = -[GB]^{-1}[GA(X, t) + (x_2 - V_r)] \quad (5-10)$$

or

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$$d_{eq} = \frac{\frac{\alpha}{L}(R_{LOSS}x_1 + x_2) - \frac{\beta}{C}(x_1 - \frac{x_2}{R}) + (V_r - x_2)}{(\alpha V_{in})/L} \quad (5-11)$$

The resulting close-loop system is obtained by substituting (5-11) into (5-6)

$$\dot{X} = \begin{bmatrix} -\frac{\beta}{\alpha C} & \frac{\beta - RC}{\alpha RC} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} X + \begin{bmatrix} \frac{1}{\alpha} \\ 0 \end{bmatrix} V_r \quad (5-12)$$

The large-signal closed-loop state-space equation is a linear one. The characteristic equation of (5-12) is

$$\alpha RCs^2 + (\beta R + \alpha)s + R = 0 \quad (5-13)$$

It shows that the two poles of (5-13) are located in the LHP as long as α and β are positive constants. Thus, this system is stable if the existence and reaching condition for the sliding mode controller are satisfied. The existence and reaching condition can be proven following the same method given in Chapter 3 and 4, which are ignored here. In the following parts, the system described by (5-13) is referred to the non-adaptive system.

The control-to-output transfer function is obtained from (5-12) as

$$G_{ref}(s) = \frac{R}{\alpha RCs^2 + (\beta R + \alpha)s + R} \quad (5-14)$$

The output impedance is also obtained

$$Z_{out}(s) = \frac{\alpha Rs}{\alpha RCs^2 + (\beta R + \alpha)s + R} \quad (5-15)$$

In practice, the second item in the numerator of (5-11), $(x_1 - \frac{x_2}{R})$ is actually the capacitor current i_C . Thus, the controller can be simplified as

$$d_{eq} = \frac{\frac{\alpha}{L}(R_L x_1 + x_2) - \frac{\beta}{C}i_C + (V_r - x_2)}{\alpha V_{in}/L} \quad (5-16)$$

5.1.2.2 The adaptive equivalent sliding-mode controller

The non-adaptive controller can only operate properly under the assumption that R_L is known. Adaptive control is therefore employed. Its main principle is to estimate the unknown system parameters via mathematic algorithms. An adaptive controller to estimate the output load resistance has been given in [67]. In this thesis, using the same adaptive control to estimate the loss resistance R_L is proposed. To achieve easier and clearer theoretical analysis, another state variable x_3 is introduced, which is the estimation of R_L . The adaptive law is described as

$$\dot{x}_3 = \gamma V_r (V_r - x_2) \quad (5-17)$$

γ is the adaptive coefficient and its measuring unit is $\Omega \cdot s^{-1} \cdot V^{-2}$. γ determines the converging speed of x_3 .

Replace the R_L in (5-16) with x_3 , the controller in (5-16) becomes

$$deq = \frac{\frac{\alpha}{L}(x_3 x_1 + x_2) - \frac{\beta}{C} i_C + (V_r - x_2)}{\alpha V_{in} / L} \quad (5-18)$$

Consequently, the closed-loop state-space averaged equation is obtained by substituting (5-18) into (5-6), and the system equation changes to a third-order one.

$$\begin{cases} \dot{x}_1 = \frac{1}{L}(x_3 - R_L)x_1 - \frac{\beta}{\alpha C}(x_1 - \frac{x_2}{R}) + \frac{1}{\alpha}(V_r - x_2) \\ \dot{x}_2 = \frac{x_1}{C} - \frac{x_2}{RC} \\ \dot{x}_3 = \gamma V_r (V_r - x_2) \end{cases} \quad (5-19)$$

Let the left side of (5-19) to zero. It shows that there is only one equilibrium point for this nonlinear system. The equilibrium is

$$x_{1eq} = \frac{V_r}{R}; \quad x_{2eq} = V_r; \quad x_{3eq} = R_L \quad (5-20)$$

The small perturbations of the state variables around the operating point are defined as

$$Z = \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} = \begin{bmatrix} x_1 - x_{1eq} \\ x_2 - x_{2eq} \\ x_3 - x_{3eq} \end{bmatrix} \quad (5-21)$$

Therefore, the linearized model around operating point is obtained as

$$\dot{Z} = \begin{bmatrix} -\frac{\beta}{\alpha C} & \frac{\beta - RC}{\alpha RC} & \frac{V_r}{RL} \\ \frac{1}{C} & -\frac{1}{RC} & 0 \\ 0 & -\gamma \mathcal{W}_r & 0 \end{bmatrix} Z + \begin{bmatrix} \frac{1}{\alpha} \\ 0 \\ \gamma \mathcal{W}_r \end{bmatrix} \Delta V_r \quad (5-22)$$

The controller described in (5-18) is named as adaptive controller in the following sections of this Chapter. A generalized representation of the closed-loop control scheme for Buck converter is shown in Figure 5-4.

Figure 5-4 The closed-loop control scheme for proposed adaptive controller

To study the stability of the closed-loop system, the system characteristic equation can be derived as

$$s^3 + \left(\frac{\beta}{\alpha C} + \frac{1}{RC}\right)s^2 + \frac{1}{\alpha C}s + \frac{V_r^2 \gamma}{RLC} = 0 \quad (5-23)$$

Based on the Routh's stability criterion [128], it is known that the sufficient condition for (5-23) to have all poles with negative real part is

$$\frac{1}{\alpha C} \left(\frac{\beta}{\alpha C} + \frac{1}{RC}\right) - \frac{\gamma \mathcal{W}_r^2}{RLC} > 0 \quad (5-24)$$

γ shall be selected to satisfy (5-24) and it should not influence the system response very much. The detailed selection method is given in the design examples.

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The design procedure of the adaptive controller can be summarized as three steps. At first, α and β are chosen to satisfy the stability and performance requirements for a traditional sliding mode control. The second step is to select γ to achieve proper convergence speed. Finally, the closed-loop system characteristics such as dynamic response should be examined. A design example for Buck converter is given in next section.

Based on the results from Chapter 4, it is recommended that the low pass filter should be used for sensing state variables such as i_C , x_1 and x_2 . The cross-over frequency of the filters can be selected using the same method as in Chapter 4.

5.1.3 A Design Example of the Adaptive Controller for Buck Converter

The parameters of the Buck converter are shown in Table 5-1. It is obtained from (5-5) that the desired duty cycle is $d = 0.56$. From (5-8), the corresponding loss resistance R_L is 1.36Ω .

Table 5-1 Circuit and controller parameters

$V_{in} = 20 \text{ V}$	$\alpha = 0.001 \text{ } \Omega \cdot \text{s}$	$f_C = 4 \text{ kHz}$
$R = 11 \text{ } \Omega$	$\beta = 0.0005 \text{ s}$	$r_S = 0.008 \text{ } \Omega$
$C = 100 \text{ } \mu\text{F}$	$\gamma = 20 \text{ } \Omega \cdot \text{s}^{-1} \cdot \text{V}^{-2}$	$V_D = 0.73 \text{ V}$
$L = 1 \text{ mH}$	$V_r = 10 \text{ V}$	$r_L = 1 \text{ } \Omega$
$f = 20 \text{ kHz}$		

5.1.3.1 Design procedure

The system existence condition and reaching condition can be derived to be satisfied with all positive constants of α and β . Then the closed-loop system's performance in terms of control-to-output transfer function and output-impedance is examined. It is also found that the input-to-output transfer function of the proposed control system is zero because of the input voltage feed-forward used in the controller. f_C is the cross-over frequency of the low pass filter, it is chosen to be 4 kHz.

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Based on the above considerations, the parameters are chosen as $\alpha = 0.001 \text{ } \Omega \cdot \text{s}$ and $\beta = 0.0005 \text{ s}$. Bode plot of the transfer function $G_{ref}(s)$ is shown in Figure 5-5. And the bode plot of the transfer function $Z_{out}(s)$ is shown in Figure 5-6. The two poles of the non-adaptive system are $-2955 \pm 1127j$.

Figure 5-5 Reference-to-output transfer function $G_{ref}(s)$

Figure 5-6 Output impedance $Z_{out}(s)$

The adaptive part is added to mitigate the steady state error. γ can be chosen according to the time response of the virtual system shown in (5-19). The principle is to let x_3 rise quickly during the rising period of output voltage. When output voltage reaches its steady state value, x_3 should be closed to its desired value obtained from (5-8). It is seen from

Figure 5-5 that the bandwidth of $G_{ref}(s)$ is about 350 Hz. The rise time of the closed-loop system to track a step change of the reference voltage is thus approximately $T_r = 3$ ms. Then, the integrator's final output can be approximated as

$$\int_0^{T_r} V_r(V_r - x_2)dt \approx 0.5V_r^2T_r \quad (5-25)$$

Thus, based on experiences the adaptive coefficient γ during system start up is chosen as three to six times of the critical value calculated from (5-26).

$$\gamma_c \approx \frac{R_L}{0.5V_r^2T_r} \quad (5-26)$$

In this design example, the adaptive coefficient during system start up is chosen as $\gamma = 20$. When the system RP is on the operating point, reference voltage is kept constant. The adaptive coefficient can be chosen larger to achieve better anti-perturbation performance. Under such a case, $\gamma = 60$ is used when the system operates around the operating point.

The poles of this adaptive system can be calculated as $-2851 \pm 833j$ and -206 from (5-22). The real pole -206 is introduced due to the adaptive control part. It is quite close to the imaginative axis and therefore has slower response than the two conjugate poles. However, another system zero is also introduced, which can be calculated to be -182 . Because this zero is closed to the real pole, the residue of the real pole is small and the influence of this pole on the system response is also small [128]. Therefore the dominant poles of the adaptive system are the two conjugate poles. It is then proven that the system response will not change much although the system order is increased.

5.1.3.2 Simulation results

The step response of the system is simulated when the reference voltage is changed from 0 V to 10 V. The simulation results are shown in Figure 5-7. The rising time of the output voltage is less than 4 ms, which is quite fast compared with the natural oscillation period (about 2 ms) of the Buck converter output filter. In Figure 5-7c, x_3 converges to its steady state value (1.36). It is noted that when the output voltage is closed to the reference, the converging speed of x_3 becomes slow. This is the reason why larger γ should be used when the reference voltage is constant. The duty cycle is well constrained in its limitation range during the transient process. This ensures a constant switching frequency.

Furthermore, the inductor current shown in Figure 5-7b has an acceptable overshoot of about 60%, which is relatively small compared to the traditional SM controller.

Figure 5-7 Step responses

Simulation waveforms of closed-loop controlled Buck converter under step changes of input voltage are shown in Figure 5-8. In the simulation, the input voltage is decreased from 20V to 15V and increased to 20V again. Theoretically, no disturbance shall be seen at the output because the input-to-output transfer function is 0. The duty cycle shall quickly reach its desired value when the input voltage changes. However, in practice short duration is still needed for the output voltage to follow the duty cycle changes. Therefore in Figure 5-8a, the output voltage changes a little. The adaptive part x_3 is also changed to its new value to eliminate the steady state error.

Figure 5-8 Simulated waveforms of system response under input variations

The simulation waveforms of the closed-loop system under load resistance changes are shown in Figure 5-9. In the simulation, the load resistance is changed from 11 Ω to 22 Ω and then recovered. The overshoot of the output voltage is about 5% of nominal value. The recover time is about 5 ms. The inductor current also changes quickly under load variations. When the load and the equivalent duty cycle changes, R_L changes as well. It is shown in Figure 5-9c that x_3 reaches a new value which removes the steady state error. System capability to track the reference voltage changes is also simulated and the results are shown in Figure 5-10.

Figure 5-9 System response under load variations

Figure 5-10 System response under step change of reference voltage

5.1.3.3 Experimental results

Experiments are done in this section to verify the performance of the adaptive controller with Buck converter. The hardware circuit is shown in Figure 5-11. Current variables are captured using active current probe. To reduce energy consumption in the calculation circuit, reference voltage is chosen to be 5V for a 10V output voltage.

Figure 5-11 Hardware circuit of Buck converter with adaptive control

System response under a reference voltage change is shown in Figures 5-12 and 5-13. The experiment results are quite similar as the simulation results. In Figure 5-12, CH1 is the output voltage and CH2 is the inductor current. The current waveform shown in Figure 5-12 is the output of the low-pass filter, where most of the ripple component has been removed. The adaptive part x_3 (CH1) and the control output $5d_{eq}$ (CH2) are shown in Figure 5-13.

Figure 5-12 Output voltage and inductor current in step response

Figure 5-13 Adaptive variable and duty cycle in step response

Figures 5-14 and 5-15 show the system response under input voltage variations. The input voltage is changed from 20 V to 15 V and then recovers. Due to the practical limitation, the theoretical zero change in the output voltage can not be achieved. The practical overshoot of the output voltage is about 1 V, which is about 10% of its nominal value. It can also be seen from Figure 5-14 that the current variations are also small, which is about 10% of its nominal value.

Figure 5-16 and Figure 5-17 show the system response under step changes of load resistance. The load resistance is changed from 11 Ω to 22 Ω and recovers. The scale of duty cycle in Figure 5-17 is 5. It is seen that almost no overshoot is found in the inductor current. The system response under step changes of reference voltage is shown in Figure 5-18 and Figure 5-19. Reference voltage is under step changes from 10 V to 8 V and

recovers. It is seen that the system response is not influenced by the operating point, which is desirable for dc-dc converters.

Figure 5-14 Output voltage and inductor current under step changes of input voltage

Figure 5-15 Adaptive variable and duty cycle under step changes of input voltage

Figure 5-16 Output voltage and inductor current under step changes of load resistance

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Figure 5-17 Adaptive variable and duty cycle under step changes of load resistance

Figure 5-18 Output voltage and inductor current under step changes of reference voltage

Figure 5-19 Adaptive part and duty cycle under step changes of reference voltage

5.2 The Combination of the Equivalent SM Control with OCC

In the equivalent SM controller proposed in Chapter 4, a divider circuit has been used to generate the desired duty cycle signal. However in practical applications, divider circuit is normally complicated and expensive. In this section, the OCC concept with a voltage-controlled saw tooth waveform generator is used to replace the divider circuit.

5.2.1 One-Cycle Control Concept

The general idea of OCC has been briefly introduced in Chapter 1. In this section, a more detailed analysis is given. In the OCC, the duty cycle in each cycle is modulated so that the integration of the switched variables is exactly equal to or proportional to the reference

$$f \int_0^{T_{ON}} v_{in}(t) dt = v_{ref}(t) \quad (5-27)$$

$$v_O(t) = f \int_0^{T_{ON}} v_{in}(t) dt = v_{ref}(t) \quad (5-28)$$

A common OCC scheme is shown in Figure 5-20. V_{int} is a saw tooth signal. Its frequency is determined by the clock signal and the slew rate is determined by the diode voltage. If the reference and input are kept constant, the duty cycle can be obtained as

$$D = \frac{V_{ref}}{V_{in}} \quad (5-29)$$

With such a scheme, the original divider used for calculation of the duty cycle can be saved.

Figure 5-20 The one-cycle controlled constant-frequency switch

The desired duty cycle equation of the controller can be written as

$$d_{eq} = \frac{V_{num}}{V_{den}} \quad (5-30)$$

Comparison between (5-30) and (5-29) shows that both equations have the similar structure. To derive duty cycle with OCC, V_{den} can be used as input signal of the integrator in Figure 5-20. In such a way, the divider circuit is no longer needed. The implementation of voltage controlled saw tooth waveform can be realized using the circuit shown in Figure 5-21.

Figure 5-21 Voltage controlled saw tooth waveform generator

As shown in Figure 5-21, the current used to charge capacitor C_s is the same as the current across resistor R_s , which is determined by the input voltage V_{saw} . The clock signal, with switching frequency f is used to control the charging time of capacitor C_s . By ignoring the turn off time of the transistor and assuming the duty cycle is near zero, the charging time of C_s is $1/f$. Therefore, the peak voltage on C_s can be obtained as

$$V_{cs-pk} = \frac{V_{saw}}{R_s C_s f} \quad (5-31)$$

It is desired to let the peak value of V_{CS} equal to V_{saw} . Then the resistor R_s and capacitor C_s can be chosen according to (5-32).

$$R_s C_s f = 1 \quad (5-32)$$

5.2.2 The Combined OCC and Equivalent SM Control for Buck Converter

The adaptive controller of buck converter in (5-18) is rewritten here. Both numerator and denominator of the fraction are increased so that denominator is equal to V_{in} .

$$u_{eq} = \frac{x_2 + R_{LOSS}x_1 - \frac{\beta L}{\alpha C}i_C + \frac{L}{\alpha}(V_r - x_2)}{V_{in}} \quad (5-33)$$

The control scheme of the combined OCC and adaptive controller for Buck converter is shown in Figure 5-22.

Figure 5-22 Combined OCC and equivalent SM control

As the control equation of the combined controller is not changed, the system performance is not changed. The parameters of Buck converter used for simulation is the same as in Table 5-1. The switching frequency is 20 kHz. The step response of the closed-loop system is shown in Figure 5-23.

Comparing with Figure 5-7, it is shown that the use of one-cycle concept does not change the system response and the practical implementation is much easier because the divider circuit is no longer needed.

Figure 5-23 Step response of the combined OCC and equivalent SM controller for Buck converter

5.3 The Combined OCC and Adaptive equivalent SM Control of POSLL Converter

In the previous two sections, two improvements have been proposed for the equivalent SM controller. In order to compare the controller performance with those proposed in Chapter 3 and Chapter 4, these two improvements are also implemented for control of the POSLL converter. The converter parameters are the same as those used in Chapter 3 and Chapter 4.

5.3.1 Selection of Adaptive Part

In Section 5.1, the system power loss items have been modeled as R_L . It is also found that the system response is not significantly influenced by introducing the adaptive part. For the equivalent SM controller of POSLL converter, the coefficient $(\lambda_1 - 1)$ is chosen as the adaptive part. The reason is that the steady state value of this coefficient is quite small, which is not the dominant factor influencing the system response. Therefore, an additional system variable, λ_e , is introduced and expressed as

$$\dot{\lambda}_e = \gamma_p (V_r - v_o) \quad (5-34)$$

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By substituting (5-34) to (4-11), the adaptive equivalent SM controller for POSLL converter is derived as

$$d_{eq} = \frac{g_i(x_2 + \lambda_e x_4 - v_{in}) - \frac{L_1}{C_3}(x_3 - \frac{x_4}{R}) - g_v L_1(x_4 - V_r)}{g_i(x_2 + \lambda_e x_4)} \quad (5-35)$$

The steady state value of λ_e can be estimated using the similar method in Section 5.1. It is also possible to use circuit simulation to get the solution as follows: (1) In the circuit simulation, two converter models can be built up, one with practical circuit components and the other one using ideal components; (2) Tune the capacitance value of C_2 in the ideal model until the two converters give the same output voltage with same duty cycle and switching frequency; (3) Naming the value of C_2 under this condition as C_{2e} . The estimation of λ_e can be obtained as

$$\lambda_e = \frac{1}{2RC_{2e}f} \quad (5-36)$$

As switching losses and magnetic losses are not considered in the circuit model, estimation value obtained from (5-36) can be increased 2 to 3 times to account these effects for practical applications. With the estimated λ_e , the converging coefficient γ_p can be chosen about 3 to 6 times of the critical value shown below

$$\gamma_{pc} = \frac{2\lambda_e}{T_r V_r} \quad (5-37)$$

The final value of γ_p can be fine tuned based on the experiment results.

After choosing the adaptive part, the same method for analyzing the system performance with the adaptive part shown in Section 5.1 can be applied on POSLL converter. Since the adding adaptive part only removes the steady-state error and does not change the system dynamic performance very much, and also because the detailed derivation of system equations are really very complex, the derivation is ignored here and only simulation and experiment results are given in following section.

5.3.2 Simulation and Experimental Results

In this section, simulation and experiment results is given to the closed-loop controlled POSLL converter with adaptive controller. The circuit parameters of POSLL converter are the same as those used in Chapter 3 and Chapter 4. As the adaptive controller is based on the equivalent SM controller, the sliding surface coefficients g_i and g_v are the same as those used in Chapter 4. With the given circuit parameters, C_e and λ_e are estimated minimum input voltage and load resistance values. It can be derived that C_e is about $3.7\mu\text{F}$ for ideal converter, which leads to the VLC coefficient $\lambda_e = 0.11$. Considering the un-modeled losses λ_e is increased by 4 times. As a result, the critical converging coefficient is obtained to be $\gamma_{pc} = 12$ and the converging coefficient is chosen to be $\gamma_p = 32$. The switching frequency of the converter is 50 kHz, R_s and C_s are chosen as $20\text{ k}\Omega$ and 1 nF respectively.

It is known that $x_3 - \frac{x_4}{R} = i_{C3}$. Therefore, the final controller for simulations and experiments is shown as

$$d_{eq} = \frac{0.2(x_2 + \lambda_e x_4 - v_{in}) - 0.4i_{C3} - 0.147(x_4 - V_r)}{0.2(x_2 + \lambda_e x_4)} \quad (5-38)$$

$$\lambda_e = \int_0^t 32(V_r - v_o)dt$$

5.3.2.1 Simulation results

Circuit simulations are done using PSim. The simulation step is 100 ns to achieve high accuracy. The simulation circuit of equivalent SM controlled POSLL converter is shown in Figure 5-24.

Figure 5-24 Simulation circuit for POSLL converter using the adaptive controller

The simulation waveforms of POSLL converter during start up are shown in Figure 5-25. The voltage controlled ramp signal and the numerator of the equivalent duty cycle are also included in the same figure. It is seen that the output voltage reaches its steady state value in around 5 ms, which is similar to the results shown in chapters 3 and 4 for the SM and equivalent SM controllers. Compared to the simulated waveforms shown in Figure 4-9, it is shown that the adaptive controller effectively remove the steady state error. However, it also leads to a larger overshoot in the output voltage during start up.

Figure 5-25 Simulated waveforms of POSLL converter using adaptive controller

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To obtain more deep understanding of the adaptive controller, its dynamic performance applied with POSLL converter is further studied in this section. Figure 5-26 shows the simulation waveforms during reference variations. In the simulation, reference voltage is increased from 20V to 28V at 20 ms and then recovered at 40 ms. Compared to equivalent SM controlled POSLL converter, the adaptive controller eliminates the steady state error while leads to more oscillations in the output voltage. It is also seen that V_{num} never reaches 0. According to (5-30), it can be derived that the duty cycle of the controller also never reaches 0. Therefore, the converter switching frequency is maintained constant during transient state.

Figure 5-26 Simulated waveforms of POSLL converter during reference voltage changes

Figure 5-27 shows the simulation waveforms of POSLL converter using the adaptive control under load resistance changes. In the simulation, the load resistance is increased from 36Ω to 147Ω at 20 ms and decreased to 36Ω at 40 ms. It can be seen that steady state error on output voltage has been removed. The figures also show that the numerator of the desired duty cycle V_{num} never reaches its maximum value ($V_{ramp-pk}$) or minimum value (0) during the transient. The switching frequency is therefore constant.

Figure 5-27 Simulated waveforms of POSLL converter during load resistance changes

Figure 5-28 shows the simulation waveforms during input voltage variations. The input voltage is increased from 10V to 14 V at 20 ms and it is decreased to 10V at 40 ms. The simulation shows that there is no steady state error on the output voltage and the switching frequency is also constant during transients.

Figure 5-28 Simulated waveforms of POSLL converter during input voltage variations

5.3.2.2 Experimental results

In this section, experiment results of the proposed equivalent and adaptive SM controller are given to verify both the theoretical analysis and circuit simulations. As it is desired to reduce energy consumption in the calculation circuit in the experiment, then the voltage variables are sensed with a ratio of 0.2 and current variables are sensed with 0.1Ω current resistors. Nominal reference voltage is 4.8V. The hardware circuit is shown in Figure 5-29. Photos of the hardware circuit are given in Appendix F.

The hardware circuit for implementing the adaptive parameter λ_e includes two operational amplifiers. One is for integration and the other one is for proportion purpose. Although the divider IC AD734 using to generate duty circle in Chapter 4 is not necessary in this model, it still needs one divider IC to realize the multiplier in the adaptive part.

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smaller in the experiment. This is reasonable as there are switching losses and magnetic losses which are not modeled in the simulation. These stray components slow down the output voltage response. This also explains why less oscillation on v_{num} is observed in the experiment. As the output voltage increases slower, the controller can achieve higher duty cycle and therefore longer duration of current saturation can be observed in the experiment.

Figure 5-30 Experiment waveforms of POSLL converter using adaptive control during start up

(a) Vr: 20V to 28V

(b) Vr: 28V to 20V

Figure 5-31 Experiment waveforms of POSLL converter using adaptive control under reference voltage changes

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Figure 5-32 Experimental waveforms of POSLL converter using adaptive control under input voltage variations

System response during input voltage variations is also different for simulation and experiment results. The reason is that in the experiment, the step input voltage can not be so fast due to the input filter capacitor (100 μ F) used. Therefore the output variations in the experiment are less than those observed in the simulation.

Figure 5-33 Experimental waveforms of POSLL converter using adaptive control under load resistance changes

5.3.2.3 Comparison between SM control and adaptive equivalent SM control on POSLL converter

In this section, comparison between the SM controller used in Chapter 3 and the adaptive controller proposed in this chapter is given. Based on the simulation results of two

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controlled systems, the settling time and overshoot of output voltage under various operation conditions have been examined and the results are shown in the Table 5-2. All the settling times are measured as the time between the instant when the output voltage error is always less than 2% of desired output voltage and the instant when circuit condition changes

Table 5-2 Comparison of settling times for equivalent SM and SM controllers

	SM controller		Adaptive controller	
	Settling time	Overshoot	Settling time	overshoot
reference step up	3.46 ms	0.75 V	3.43 ms	3.30 V
reference step down	3.10 ms	0.76 V	5.70 ms	2.46 V
Load resistance up	1.71 ms	1.51 V	1.91 ms	1.40 V
Load resistance down	1.90 ms	1.42 V	1.46 ms	1.29 V
Input voltage up	1.61 ms	1.50 V	1.07 ms	1.30 V
Input voltage down	2.00 ms	1.15 V	1.32 ms	0.88 V

It can be seen that SM controller shows faster dynamic response in tracking reference voltage changes. However, under load or input voltage variations, the equivalent and adaptive SM controller has better performance in maintaining the output voltage.

5.4 Summary

In this Chapter, two improvements to the equivalent SM controller have been proposed.

An adaptive part has been proposed to be added into the equivalent SM controller. The main purpose is to remove the steady state error. A simple Buck converter has been chosen to demonstrate the basic principle of the adaptive controller. A simplified Buck converter model has been derived firstly. The adaptive algorithm is then proposed based on the simplified model to estimate the power losses in the converter. By properly modifying the control output, zero steady state error on output voltage can be achieved. The main advantages of the resulted closed-loop system include: nearly first-order dynamic response, constant switching frequency and zero steady state error.

Chapter 5 Improvements on Equivalent Sliding-Mode Control

The equivalent control given in Chapter 4 requires much calculation, which is one of the disadvantages of this kind of controller: the control scheme is complicated and the cost is high. The OCC concept is therefore introduced to remove the divider which is used in the equivalent SM controller. A voltage controlled ramp signal generator is used to realize the OCC concept and the divider is therefore no longer needed.

In the last part of this chapter, both the adaptive method and the OCC concept are included to the equivalent SM controller for POSLL converter. The simulations and experiments have been given to confirm the performance of the closed loop system. Based on the experiment results on POSLL converter, the general comments on system cost and performance of three types of SM or equivalent SM controllers are compared and summarized in Appendix G. In practice, which type of controller used is really determined by the trade-off between the cost and performance.

Chapter 6 Conclusions and Recommendations

6.1 Conclusions

The main objectives of this thesis are to examine the advanced control and modeling methodologies for dc-dc converters, to provide better understanding of dc-dc converter operations and to develop improved control schemes which can overcome some of the existing problems such as large current overshoot during start up, variable switching frequency for sliding mode control.

Based on the basic circuit principle and ripple-approximation theorem, the detailed steady state properties of Luo converters with VLCs have been studied in Chapter 2. By including the voltage variations on the voltage lift capacitor, a more accurate formula to predict the converter VTG has been obtained. In addition, a method for determining the boundary condition between CCM and DCM, and the filling efficiency of Luo converters in DCM has been developed. The influences of switching frequency and load conditions are also considered in the generalized formulas. The results are valuable for the application of Luo converters as they provide the basis for the analysis and implementation of such converters.

Based on the steady state properties of Luo converters, the steady state-space equations and small signal equations are developed for POSLL converter in Chapter 3. In the equations, the VLC capacitor is modeled as a constant voltage source during switch on period. During switch off period, the voltage drop on VLC capacitor is represented by inductor current and switching period. As a result, the derived state-space model is only fourth-order although the POSLL converter is of fifth-order. The derived model is proven to be accurate through circuit simulations.

Control of dc-dc converters is always critical as the dc-dc converters are always operated in presence of large variations of input voltage and output load resistance. Accordingly in later part of Chapter 3, the control of POSLL converter with one VLC is studied. As POSLL converter is of high order one, sliding mode control is then chosen for study as it does not require full state information. A new integral type SM controller has been developed for POSLL converters. The main advantage of the proposed controller is that it can effectively reduce the current overshoot during converter start up. This issue has not been addressed in the published control methods. The new SM controller uses integration of output voltage error as the reference signal. At system starting point, the integration value is zero, which means the system RP is right on the sliding surface (line). Therefore the reaching time is zero. By doing so, both the output voltage and inductor current overshoots during start up are greatly reduced. Small signal linearization method has been used to examine the closed-loop system performance of the proposed SM controlled POSLL converter. The design procedure of the new controller is given to POSLL converter as an example. Simulation and experiment are also given to verify the theoretical analysis.

It is well-known that traditional SM control has variable switching frequency. Although some frequency limiting methods have been proposed, the results are still unsatisfied. The implementation of frequency limitation methods is not easy in practice as well. The research of Chapter 4 is then focused on developing a controller which can achieve constant switching frequency and at the same time, can retain the advantages of SM control. The design objective has been achieved by a novel equivalent SM control method. The proposed scheme is based on the equivalent control concept. An integral item is added to the traditional sliding surface so that the equivalent control concept can be applied. To overcome the application issues of the equivalent SM control on POSLL converters, maximum switching on time and current limitations are introduced. Small-signal models have been developed for the design of such controllers. Simulations and experiments have been conducted to verify the results. The proposed equivalent SM control is also extended to other dc-dc converters in Chapter 4.

However, the proposed equivalent SM control also shows two disadvantages, which are the non-zero steady state error and high cost due to the divider used in the control circuit. Improvements on these two points are therefore given in Chapter 5. It is known that the

steady state error is mainly caused by the power loss items in the dc-dc converters. In Chapter 5, the non-zero steady state error is removed by adding an adaptive part in the equivalent controller. The adaptive part can estimate the power losses under various operation conditions. The design procedure of the adaptive controller is explained with a simple but representative Buck converter. The theoretical analysis, simulation, and experiments results all prove the effectiveness of the adaptive scheme.

In the later part of Chapter 5, the OCC has been introduced into the equivalent SM controller to reduce the computation task in the duty cycle calculation. This is achieved by using a voltage controlled saw-tooth signal generator to replace the original divider IC. The new system shows same operation performance as the original one. Finally, both the adaptive algorithm and OCC concept are applied to the equivalent SM controller of POSLL converter. The simulations and experiments show that the equivalent SM control can give satisfied performance.

The comparison of the three type controllers proposed in the thesis based on POSLL converter is list in the Appendix G.

6.2 Recommendations for Further Research

In view of the research work described in the thesis, the following directions are suggested as possible areas for further investigation.

The steady state analysis for Luo converters covers both the CCM and DCM. However, for dynamic modeling of Luo converters, the analysis has been constrained on CCM as CCM is more widely used than DCM. As a result, the three control methods derived in this thesis are only valid for converters operated in CCM. However in practical the application of DCM is also available. Studying of Luo converters operated in DCM is therefore recommended. The research work can start with derivation of the state-space equations of Luo converters under DCM. Based on the state-space equation, the closed loop controller which can achieve similar performance as in the thesis can be developed for converters under DCM.

Chapter 6 Conclusions and Recommendations

In Chapter 3, a dc-dc converter with traditional SM controller has been used as the power supply of a PM DC motor. Only simple functions are available for the designed drive system, which include limiting the terminal voltage and armature current during motor start-up, constant-torque and constant power control during motor speed increasing and closed-loop control of motor speed in case of load variations. As the research work is very limited in this thesis, more research work can be conducted in the future in order to achieve a satisfied performance in driving DC motors. The influence of motor EMF on the converter controllers also needs further investigation. How to control the converter in case of motor brake and decrease of load torque is also of interest as the performance of the proposed controller in this thesis are unsatisfied.

In the equivalent SM controllers, the computation task in the control circuit is large as for higher order converters, many state variables need to be sensed and processed. For example, 12 operational amplifiers are used in the equivalent SM controller for POSLL converter. In the future, the digital control can be applied as DSP can fulfill all the calculation tasks using only one chip. The controller implementation can be greatly simplified. As an alternative to DSP, integrated circuit (IC) solution for the whole controller is also a possible direction for future study.

Finally not last, all the controllers proposed in this thesis are only prototypes. The built converters and controllers are only the simple laboratorial version for scientific research. The protection and reliability are critical and need further considerations if the proposed converters and controllers are intended for practical applications. In addition, electromagnetic interference and electromagnetic compatibility are another two factors shall be investigated in the future.

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APPENDIX A DC-DC Converter Family Tree

Figure A-1 Dc-dc converter family tree

APPENDIX B Basic Operation of DC-DC Converters

In this appendix, the basic operation and modeling of dc-dc converters are given.

The configuration of Buck converter is given in Figure B-1. Using Buck converter as an example, the basic operation of dc-dc converters is explained as follows. A periodical square waveform with appropriate voltage level is applied to the switch S, which is the gate signal V_g .

Figure B-1 Basic operation of dc-dc converters

See Figure B-1. The duty cycle D is defined as

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \quad (\text{B-1})$$

The switching period is

$$T = T_{ON} + T_{OFF} \quad (B-2)$$

The switching frequency is $f = 1/T$.

With the repeated on and off of the switch, a non-zero dc component is produced. This component is then extracted by the low-pass LC filter to achieve a dc output. The waveform of output voltage is also given in Figure B-1. The average value of the output voltage is represented as V_o , which is

$$V_o = DV_{in} \quad (B-3)$$

It is found from (B-3) that various voltage level lower than the input voltage can be achieved by regulating the duty cycle. There are three types of techniques to adjust the duty cycle [18]:

- Pulse width modulation (PWM):** the pulse width T_{ON} changes in proportion to the input value while the switching period T is kept constant.
- Pulse frequency modulation (PFM):** T_{ON} or T_{OFF} is kept constant, the switching period T is varied as a function of control input.
- Current hysteresis control.** Utilizing the delay of current in the inductive load, the current can be controlled between the upper limit and the lower limit as shown in Figure B-2. The duty cycle is regulated by adjusting the average value of the current.

Figure B-2 Current hysteresis control

Both PWM and current hysteresis control techniques can achieve nearly constant switching frequency. As it is easier to design filter to remove the ripple contained in the output voltage with the constant frequency operation [87], the applications of PWM and current hysteresis control techniques are much wider than PFM technique.

APPENDIX C State-Space Averaging Method

Single switch dc-dc converters typically have at least two switch states corresponding to the switch status, on or off. A set of state space equations can be written according to each switch state. Taking a Boost converter as an example, its configuration under different switch positions is shown in Figure C-1. The state variables are chosen as the inductor current and the output voltage.

When the switch is turned on, the equivalent circuit is shown in Figure C-1a. The state-space equation can be derived as

$$\dot{X} = A_1 X + B_1 \quad (\text{C-1})$$

where

$$X = \begin{bmatrix} i_L \\ v_O \end{bmatrix} \text{ and } A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \text{ and } B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in}$$

When the switch is turned off, the equivalent circuit is shown in Figure C-1a. The state-space equation for this circuit can be written as well

$$\dot{X} = A_2 X + B_2 \quad (\text{C-2})$$

where

$$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \text{ and } B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in}$$

(a) Equivalent circuit in switch on

(b) Equivalent circuit in switch off

Figure C-1 Equivalent circuits of Boost converter

Equations (C-1) and (C-2) are normally called the bi-linear state-space equations for Boost converter and both are linear. Boost converter operates continuously by switching from one condition to another in CCM.

To eliminate the time-varying parameters in above two equations, the averaging method [18] developed by Middlebrook and Cúk, can be applied. Essentially, the averaged method ignores the switching details and focuses only on the average of the system dynamic motion. It is suitable for characterizing switching converters in low-frequency domain up to half the switching frequency. The derived model is called the state-space averaged model.

Suppose the system is stable and the duty cycle equals to D under steady state. If the switching period is defined as T , the time duration when the switch is turned on is DT . The time duration when the switch is turned off is $(1-D)T$. According to the averaging method, the state-space matrices can be obtained as

$$\dot{X} = A(D)X + B(D)v_{in} \quad (C-3)$$

and the state matrices are obtained from the averaging method as

$$A = A_1 * D + A_2 * (1 - D) = \begin{bmatrix} 0 & -\frac{D}{L} \\ \frac{D}{C} & -\frac{1}{RC} \end{bmatrix} \quad (C-4)$$

$$B = B_1 * D + B_2 * (1 - D) = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

Then the steady state vector of X , which is called the equilibrium point, can be derived. Since $\dot{X} = 0$ in the steady state, the equilibrium point X_{eq} , can be found as

$$X_{eq} = \begin{bmatrix} \frac{V_{in}}{R(1-D)^2} & \frac{V_{in}}{1-D} \end{bmatrix}^T \quad (C-5)$$

It shows that it is simple to obtain the steady state value of the equilibrium point with the state-space averaging method.

The equivalent averaged circuit model in large signal for the Boost converter is shown in Figure C-2. Current controlled current source and voltage controlled voltage source are used in the averaged circuit model.

Figure C-2 Averaged circuit model for Boost converter

The state-space averaged model actually removes the ripple components of state-variables. If necessary, the ripple of voltage and current variables can still be approximated [2]

$$\Delta X = [A_1 X_{eq} + B_1]DT = [A_2 X_{eq} + B_2](1-D)T \quad (C-6)$$

Almost all the state-space averaged models for dc-dc converters are nonlinear. The dynamics of such models are not easy to be predicted with the traditional linear control

theory. Then, the small-signal linearizing method is always applied to the state-space averaging model. The small-signal AC terms can be specified as

$$\begin{aligned}\delta X &= X - X_{eq} \\ \delta d &= D - D_{eq} \\ \delta v_{in} &= v_{in} - V_{in-eq}\end{aligned}\tag{C-7}$$

where, D_{eq} and V_{in-eq} are the constant values corresponding to the operating point. The small-signal terms are identified by the δ notation. It is assumed that the small-signal terms are small enough such that the product of any two small-signal terms is negligible. This assumption is not always valid in the whole state-space, but it is reasonable for the linearization system near the operating point.

Substituting (C-7) into (C-3) results in a DC equation

$$0 = AX_{eq} + BV_{in-eq}\tag{C-8}$$

and a small-signal equation

$$\delta \dot{X} = A\delta X + B\delta V_{in} + [(A_1 - A_2)X_{eq} + (B_1 - B_2)V_{in-eq}]\delta D\tag{C-9}$$

Defining

$$B_D = (A_1 - A_2)X_{eq} + (B_1 - B_2)V_{in-eq}\tag{C-10}$$

Equation (C-9) becomes

$$\delta \dot{X} = A\delta X + B\delta V_{in} + B_D\delta D\tag{C-11}$$

This is the small-signal linearized state-space equation for Boost converters. It is only valid in a small region around the operating point.

APPENDIX D Ripple Approximation Theorem

In some cases, the state-space equation of dc-dc converters is not easily obtained. If only the ripple components and the steady state value are of interest, ripple-approximation method [2] can be applied. The principles of inductor volt-second balance and capacitor charge balance will be used in this method.

Although an inductor or a capacitor is used to function as a low-pass filter, there is also small ripple remaining in a typical output voltage waveform in dc-dc converters as shown in Figure D-1.

Figure D-1 Output voltage waveform including dc and ripple components

Hence, the output voltage can be expressed as

$$v_O(t) = V_O + v_{ripple}(t) \quad (D-1)$$

The magnitude of $v_{ripple}(t)$ has been exaggerated in Figure D-1. The switching ripple should be small in any well-designed converter. It is reasonable to assume that

$$v_O(t) \approx V_O \quad (D-2)$$

This approximation is known as the small-ripple approximation or the linear-ripple approximation [2].

The inductor current can be derived by integrating the inductor voltage. When the switch is turned on in Figure C-1a, the inductor voltage is equal to the input voltage. Therefore, the derivation of the inductor current is

$$\dot{i}_L(t) = \frac{V_{in}}{L} \quad (D-3)$$

Similarly, the derivation of the inductor current is approximated during the switch-off interval as

$$\dot{i}_L(t) = \frac{V_{in} - V_O}{L} \quad (D-4)$$

The output voltage is generally larger than the input voltage. Hence, during the switch-off interval, the inductor current changes along a negative but constant slope. The inductor current during one switch period is drawn in Figure D-2.

Figure D-2 Boost converter inductor current in steady state

As illustrated in Figure D-2, the peak current through the inductor is equal to the dc component I_L plus the peak-to-average ripple Δi_L . Since DT and the slope of inductor current are known, the ripple magnitude can be obtained as

$$\Delta i_L = \frac{V_{in}}{2L} DT \quad (D-5)$$

For the Boost converter operating in steady state, the net change of the inductor current over one switching period is zero. It is applicable to derive the steady-state conditions using the principle of inductor volt-second balance. Combining (D-4) and (D-5) leads to the integration of inductor voltage over one switching period. The integration shall equal to zero and is shown as

$$\begin{aligned}
 i_L(T) - i_L(0) &= 0 = \int_0^T v_L(t) dt \\
 &= \frac{V_{in}}{L} DT + \frac{V_{in} - V_O}{L} (1-D)T
 \end{aligned} \tag{D-6}$$

Solution for (D-6) gives

$$V_O = \frac{1}{1-D} V_{in} \tag{D-7}$$

The result is the same as that obtained from the state-space averaged model.

Similar method can be applied on the capacitor to find the current components. The integration of the capacitor current should equal to zero during one switch period in steady state. The result of ripple-approximation for capacitor current in Boost converter is given as

$$I_L = \frac{V_{in}}{(1-D)^2 R} \tag{D-8}$$

The result is the same as that obtained from the state-space averaging method. The capacitor voltage ripple can be approximated as

$$\Delta v_C = \frac{V_{in}}{2RC(1-D)} DT \tag{D-9}$$

Above analysis clearly shows that the principle of inductor volt-second balance and the capacitor charge balance theory [2] is useful in deriving the steady state and ripple information of dc-dc converters, especially for higher-order ones.

APPENDIX E Discontinuous Conduction Mode

The inductor current and its ripple component have been derived for Boost converter in Appendix D. If the inductance L is too small, or the duty cycle D is too small, the circuit will go into another operating state, normally known as the DCM. Under such a case, the current flowing through the diode decreases to zero during switch off period and the diode is therefore turned off. The equivalent circuit of Boost converter working in DCM is shown in Figure E-1. The inductor current in DCM is shown in Figure E-2.

Figure E-1 Equivalent circuit for Boost converter during switch off with inductor current in DCM

Figure E-2 Boost converter inductor current waveform in DCM

It is seen from Figure E-2 that the boundary conditions for Boost converter operating in CCM or DCM are

$$\begin{aligned} I_L &\geq \Delta i_L && \text{for CCM} \\ I_L &< \Delta i_L && \text{for DCM} \end{aligned} \quad (\text{E-1})$$

Combining (D-5) and (D-8) and substituting it into (D-10), it is found that the CCM condition becomes

$$\frac{2L}{RT} \geq D(1-D)^2 \quad (\text{E-2})$$

To analyze the steady state variables of Boost converter working in DCM, the time intervals are defined as shown in Figure E-2, where D equals to D_1 .

During the interval $0 < t < D_1T$, the inductor voltage and capacitor current are

$$\begin{aligned} v_L(t) &= V_{in} \\ i_C(t) &= -\frac{V_O}{R} \end{aligned} \quad (\text{E-3})$$

During $D_1T < t < (D_1+D_2)T$, the inductor voltage and capacitor current are

$$\begin{aligned} v_L(t) &= V_{in} - V_O \\ i_C(t) &= i_L(t) - \frac{V_O}{R} \end{aligned} \quad (\text{E-4})$$

The inductor current ripple can not be neglected since it is comparable to its average value in DCM.

During $(1-D_3)T < t < T$, both the switch and diode are turned off. The inductor voltage and capacitor current are

$$\begin{aligned} v_L(t) &= 0 \\ i_C(t) &= -\frac{V_O}{R} \end{aligned} \quad (\text{E-5})$$

According to inductor volt-second balance, the inductor voltage must have a zero dc component over one switching cycle in steady state. It is therefore obtained

$$D_1V_{in} + D_2(V_{in} - V_O) + D_30 = 0 \quad (\text{E-6})$$

Since D_2 is unknown, another equation should be derived in order to solve the VTG. According to the capacitor charge balance, the capacitor current should also have zero integration over one switching cycle in steady state. Therefore,

$$-\frac{V_O}{R}D_1T + \int_{D_1T}^{(D_1+D_2)T} [i_L(t) - \frac{V_O}{R}]dt - \frac{V_O}{R}D_3T = 0 \quad (\text{E-7})$$

As illustrated in Figure E-2, the integration of the inductor current during the interval D_2T is

$$\int_{D_1 T}^{(D_1+D_2)T} i_L(t)dt = \frac{V_{in} D_1 D_2 T}{2L} \quad (E-8)$$

Substituting (E-8) into (E-7) yields

$$\frac{V_{in} D_1 D_2 T}{2L} = \frac{V_O}{R} \quad (E-9)$$

The left side of (E-9) is also the average diode current in one switching period and its right side is the average output current. (E-6) is equivalent to

$$D_2 = \frac{V_{in} D_1}{V_O - V_{in}} \quad (E-10)$$

Substituting (E-10) into (E-9) leads to

$$V_O^2 - V_O V_{in} - \frac{V_{in}^2 D^2 R T}{2L} = 0 \quad (E-11)$$

(E-11) is a second-order equation regarding to the unknown V_O . The positive root of this equation is valid since the negative one has no physical meaning. The VTG of Boost converter operating in DCM is therefore obtained

$$\frac{V_{out}}{V_{in}} = \frac{1 + \sqrt{1 + \frac{2D^2 R T}{L}}}{2} \quad (E-12)$$

The VTG of a Boost converter operating in DCM is different from the one in CCM. It is a function of the load resistance, the switching period and the duty cycle.

APPENDIX F Photos of Hardware Circuits

Figure F-1 Hardware circuit of the POSLL converter

Figure F-2 Hardware circuit of SM controller for the POSLL converter

Figure F-3 The equivalent and adaptive SM controller

Figure F-4 POSLL converter with equivalent and adaptive SM controller

Figure F-5 Experiment setup

Figure F-6 Experiment setup

APPENDIX G Comparisons of Three Controllers

		SM controller	Equivalent SM controller	Adaptive equivalent SM controller
Sensed variables	voltage	1	3	3
	current	1	2	2
Computation task		Simple 4 operational amplifiers	Complicate 12 operational amplifiers	Complicate 13 operational amplifiers 1 multiplier IC
Gate signal generations		Complicate 2 comparators 1 RS flip-flop	Simple 1 Comparator 1 voltage controlled ramp generator	Simple 1 Comparator 1 voltage controlled ramp generator
Start up performance		Best in three controllers	Worse than SM controller	Worse than SM controller
Dynamic performance		Good	Better than SM controller	Better than SM controller
Switching frequency		Varying	Fixed	Fixed
Steady state error		No	Yes	No
Extra protection circuit		No	Yes Maximum on time Maximum current	Yes Maximum on time Maximum current

Vita

He Yi was born in P. R. China, in 1978. He received his B. Eng degree from Xi'an Jiaotong University, China, in 1999 and his M. Eng degree from Xi'an Jiaotong University, China in 2002, both in Electrical Engineering. Since July 2002, he is studying for his Ph. D degree in Nanyang Technological University. His research areas include dc-dc converters, modeling, and operation, control of dc-dc converters, adaptive control, and sliding-mode control.

Research related to this dissertation has resulted in the following publications:

- [1] Yi He and Fang Lin Luo, "Analysis of Luo Converters with Voltage Lift Circuit", IEE proceedings on Electric Power Application, Vol. 152, No. 5, September 2005, pp. 1239 – 1252.
- [2] Yi He and Fang Lin Luo, "Sliding-mode Control for dc-dc Converters with Constant Switching Frequency", IEE proceedings on Control Theory Application, Vol. 153, No. 1, January 2006, pp. 37 – 45.
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Publications not related to this research project:

- [1] He Yi, Liu Weiguo and etc, “Algorithm Study on Extracting the Step Response parameters of HV Impulse Measuring System by Computer”, Journal of High Voltage Apparatus, 2001, Vol. 37, No. 1: p1 – 4. in Chinese.
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