Stress migration study of Cu/Low-k interconnect system

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Stress Migration Study of Cu/Low-k Interconnect System

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in fulfillment of the requirement for the degree of
Doctorate in Engineering

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ABSTRACT

The demand for high performance, high packing density and low power dissipation integrated circuits (IC) has caused downward scaling of feature sizes in very large-scale integration (VLSI) fabrication. However with the scaling of interconnect feature size; the interconnect delay, which is one of the key factors determining the overall performance of devices is severely penalized [1]. Therefore copper (Cu), which is well known for its lower resistivity and excellent resistance to electromigration (EM) and stress-induced voiding as compared to aluminum (Al) and its alloy, was introduced as the material for nanoscale interconnects [2-9]. However, when the efforts to develop an effective Cu etch process failed, dual damascene which is an elegant technique of inlaying metal for interconnects throughout the back-end-of-line (BEOL) becomes the preferred choice. Even though Cu dual damascene has already been proven to be process-friendly and costs effective, its reliability robustness is strongly process and structural dependent.

Starting from 0.13 μm process, yield and reliability have become critical issues for the integration of Cu and low-k dielectrics. Poor yield is observed at wafer sort and even for those apparent good chips; the failure rates are unacceptable during accelerated life testing. Physical analysis has shown the formation of stress-induced voids to be either within or beneath vias [10-35]. As such, understanding on the phenomena of stress-induced voiding in Cu interconnects must be established so as to resolve these issues.

This research emphasizes on five areas which aim to study the phenomena of different types of stress-induced voiding, to evaluate the process and geometrical dependency of stress-induced voiding, to provide an in-depth understanding of stress-induced voiding mechanisms and process, to propose approaches to improve stress migration (SM) reliability and to discuss the extendibility and impacts of the approaches to future nanoscale technologies employing porous ultra low-k dielectrics.

Systematic studies on the phenomena of the stress-induced voiding within and beneath the via of multi-level Cu interconnects are presented in Chapter 4. Physical analysis such as passive voltage contrast (PVC), transmission electron microscope (TEM) and scanning electron microscope (SEM) was employed to locate and study the stress-induced voids. It was experimentally determined that stress-induced voiding within via was more pronounced with increasing metallization layers and when Cu was integrated with low-k dielectric. In addition, the geometrical dependency of stress-induced voiding beneath via was studied and the impact of via gouging on the SM reliability was discussed. Using a three-dimensional (3D) finite element analysis (FEA) simulation model, the mechanisms responsible for stress-induced voiding were identified and several approaches such as re-sputtering step during the physical vapor deposition (PVD) process of the diffusion barrier layer and redundant via were recommended and proven to be effective in improving the SM reliability of Cu interconnects.

Design of experiments (DOE) on Cu annealing and Cu diffusion barrier layer deposition were employed in Chapter 5 to study the dominant mechanism responsible for

stress-induced voiding in Cu interconnects. It was found that the presence of any intrinsic weaknesses around a via is the dominant mechanism in determining the SM reliability. These intrinsic weaknesses are fatal and could result in an open circuit even in the case when Cu metallization is well annealed and the vacancies are minimal. Also, the process of stress-induced voiding was described and explained using a 3D FEA simulation model.

The effect of redundant via on stress-induced voiding were studied and are presented in Chapter 6. Redundant via in Cu interconnects was proven to be effective in enhancing the SM resistance than those with single via. The main cause of this improvement was found to be the tensile stress reduction effect beneath dual-damascene vias designed along wide Cu metallization. This finding correlates well with the FEA simulation result, which always shows higher stress beneath an inner via, leading to the formation of stress-induced void beneath the inner via only.

In Chapter 7, small dielectric blocks that are commonly used in wide Cu metallization to prevent dishing during chemical mechanical planarization (CMP) process were redesigned as another alternative to manage stress-induced voiding in Cu interconnects. The novel dielectric slot was successfully fabricated in Cu interconnects without additional masking steps. Electrical and physical analysis results showed that a well-designed dielectric slot had minimal impact on the interconnect resistance and was effective in controlling stress-induced voiding. The corresponding mechanisms responsible for the SM improvement were supported using a 3D FEA simulation model.

Challenges to the SM reliability of Cu interconnects in future nanoscale technologies are discussed in Chapter 8. Furthermore, another failure mode in Cu/Low-k interconnects where the via was deformed was highlighted and was reported to worsen in the case of porous ultra low-k dielectrics. Also, 3D FEA stress simulation was discussed as a good approach to provide an in-depth understanding of various SM failures seen in today's state-of-the-art CMOS technologies since it is no longer cost effective to study SM failures through the standard DOE approach. Thus early implementation of simulation model for reliability physics study and the subsequent DFM are strongly recommended for device reliability community to study SM in sub-45nm CMOS devices.

In summary, the fundamental mechanisms responsible for the SM failures in nanoscale devices were studied. The corresponding SM reliability enhancement for future nanoscale technologies in which BEOL reliability is of great concern, particularly those employing ultra low-k dielectrics, was discussed. The 3D simulation results showed that with the introduction of lower k-value dielectrics in sub-45 nm technology, innovative structural redesigns such as redundant via and/or dielectric slot in Cu interconnects would become critical to make Cu interconnects more resilient to SM degradation. As such, SM enhancement requires not only process improvements but also structural redesigns. For future development, a closer interaction among designers, process and reliability engineers is even more important to ensure that the SM reliability of interconnects is not degraded while other important parameters such as interconnect resistance and on-chip device packaging density are not severely compromised.

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CHAPTER 1

INTRODUCTION

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- 1.1 Background**
 - 1.2 Motivation**
 - 1.3 Objectives**
 - 1.4 Major Contribution of the Thesis**
 - 1.5 Organization of the Thesis**
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1.1 Background

For the past thirty years, Al-alloy was the preferred choice in the semiconductor industry for the fabrication of IC interconnects because of its low resistivity and amenability to low cost and high throughput fabrication processes. Also, its ability to form a passivating oxide film enabled it to be easily patterned and etched. Furthermore, it adhered well to most dielectrics used in the industry. While early devices were made with an Al-alloy metallization scheme, much of the industry migrated to Tungsten (W) plugs for contact and via fill for the 0.5 μm technology node and Al-alloy served only as interconnects. When Al-alloy was used in conjunction with refractory cladding materials such as Titanium (Ti) and Titanium Nitride (TiN), it exhibited enhanced reliability such as resistance to EM and stress-induced voiding. Therefore, the industry opted to stay with Al-alloy metallization and extended its usage to the 0.18 μm technology node.

Demands for better performance and higher packing density has resulted in the need to shrink the dimensions of microelectronic devices. However, interconnect scaling has limited advances in high performance IC. Resistance and capacitance (also known as RC-product) of interconnects thus become important parameters in determining IC design, design rules, packaging density and device performance. For sub-0.25 μm technology, instead of intrinsic gate delay, RC-product of interconnects becomes dominant in determining the overall device performance [36]. As such, interconnect delay must be minimized to achieve faster devices with low power consumption [37].

The pursuit for high-end devices prompted a flurry of activities in the design and process communities. In order to lower both the resistance and capacitance of interconnects; the industry gradually migrated to materials of lower resistivity, namely Cu and new insulators that have lower dielectric constants (also known as k value) [38,39]. In the 0.13 μm technology node, the delay of Cu interconnects and dielectrics with low-k values is approximately half that of Al and silicon dioxide (SiO_2) dielectric. In addition, the higher conductivity of Cu helps to reduce the number of metal layers required for optimal device performance, which remove significant process steps and has a direct impact on device yield. IC with Cu interconnects operates with approximately 30% less power at a given frequency than IC with Al interconnects, enabling higher performance devices for mobile application. Furthermore, the reduction in the critical process steps with the dual-damascene Cu process reduces the overall cost by 30% per interconnect level. Cu is also well known for its excellent resistance to EM and stress-induced voiding as compared to Al-alloy [2-9].

Owing to the great benefits of Cu, an announcement was made on its use as an alternative to Al-alloy metallization in the fabrication of IC in 1997 [4,5]. Al-based metals are normally sputtered at high temperatures on SiO₂ dielectric, which generally result in large as-deposited grain size. However, in the case of Cu, it cannot be easily patterned like Al-alloy. The lack of volatile by-products does not allow easy etching of Cu using the conventional reactive ion etch technique. Therefore, the adoption of the damascene and dual-damascene process flow has made the fabrication of devices with Cu interconnects feasible.

This new approach to create “in-laid” structures of Cu requires the use of electrolytic Cu-plating and chemical mechanical polishing techniques. Owing to the different process conditions associated with Al-based and Cu-based interconnects, traditional wear-out mechanisms such as EM and stress-induced voiding must be re-evaluated for Cu.

1.2 Motivation

Since the introduction of Cu-based interconnects, a good understanding on EM reliability differences between Al and Cu has been of paramount importance and has received much attention in many areas [40-59]. However, stress-induced voiding in Cu interconnects has received less attention because of its favorable properties such as lower mobility and similar stress levels as compared to Al. Based on this understanding, Cu is theoretically expected to have better stress-induced voiding resistance than Al. However, numerous recent reports have shown that the assumption of stress-induced robustness for Cu is overly optimistic [10-35]. In fact, the comparison of stress-induced voiding between Al and Cu is

complicated by several factors. For example, the stress-free temperature for Al-based and Cu-based interconnects may be different. Moreover, Cu metallization process and dielectric materials are also very different from those traditionally used for Al [60-69].

Cu diffuses more rapidly in Silicon (Si) and conventional dielectrics than Al. Therefore, it can cause severe threshold-voltage shifts, junction leakage, and inter- and intra-level shorts between metal leads unless it is properly encapsulated on all sides with diffusion barrier layers. Furthermore, Al-based metals are normally sputtered at high temperatures on SiO₂ dielectric, which generally result in large as-deposited grain size. On the other hand, for Cu, electrochemical plating (ECP) in a dual-damascene process flow results in small as-deposited grain size. In the case of the blanket film, the initial stress level for ECP Cu deposited at room temperature is low. However, the stress level will change significantly upon subsequent thermal treatments [40]. These new processes if not carefully managed can deteriorate the stress-induced voiding resistance of Cu interconnects.

Despite many extensive studies, the mechanisms of stress-induced voiding are still not well understood. Contradictory results and discussions have been reported in the literature. Moreover, there is no study to describe and explain the process of stress-induced voiding. Process and structural dependency of stress-induced voiding is also of great interest. So far, the effectiveness of redundant via structure in improving the SM reliability of Cu interconnects is purely demonstrated by the measurements of resistance change after a SM test. No physical analysis has been performed to support this finding and the associated mechanism responsible for the improvement remains unclear. Also, the extendibility of this approach to future nanoscale technologies employing porous ultra low-k dielectrics has not

been discussed. Hence, these areas are of great interests to yield better understanding of stress-induced voiding phenomena and to enhance the SM reliability of Cu interconnects.

1.3 Objectives

The objectives of this work are summarized as follows:

- (i) To study the phenomena of stress-induced voiding in Cu interconnects;
- (ii) To explore different methods of physical analysis to investigate and understand the mechanisms of stress-induced voiding;
- (iii) To evaluate process and geometrical dependency of stress-induced voiding;
- (iv) To model and analyze the stress distribution in Cu interconnects;
- (v) To propose approaches to improve SM reliability; and
- (vi) To discuss the extendibility and impact of the approaches to future nanoscale technologies employing porous ultra low-k dielectrics.

1.4 Major Contribution of the Thesis

The phenomena of stress-induced voiding in Cu interconnects were studied in greater details in this work. In addition to the discussion on the inter- and intra-level SM reliability of Cu interconnects on a wafer; the interaction of different mechanisms leading to stress-induced failures within vias was illustrated for the first time using TEM analysis. Also, SEM

was conducted at a high tilted angle on a selectively delayered SM damaged sample to examine the extent of void growth that caused an open circuit beneath vias. These findings are important because they led to a deeper understanding on the mechanisms that resulted in the formation of stress-induced voids within and beneath via during a SM test.

In this work, stress modeling of gouging via was performed in an attempt to achieve a more accurate stress simulation of via with wide Cu metal lead. It helped to clarify the contradictory stress simulation results in recent reports and led to the finding that appropriate control of the via gouging depth during selective process enhanced the SM reliability of Cu interconnects. In addition, DOE on Cu annealing and Cu diffusion barrier layer deposition showed that the presence of any intrinsic weak point around a via was the dominant mechanism in determining the SM reliability. These intrinsic weak points were fatal and could result in an open circuit even in the case when Cu metallization was well annealed and the vacancies were minimal. Hence, these weak points had to be managed through process improvement for robust SM reliability. Also, using a 3D FEA stress simulation model, the process of stress-induced voiding was described and explained.

Furthermore, the effectiveness of dual-via structure in suppressing the formation of stress-induced void beneath via was confirmed for the first time via physical analysis. It revealed that stress-induced void was consistently found to form beneath one via only. The 3D FEA stress simulation results showed that the inner via consistently suffered a higher stress distribution than that of the outer via which was closer to the end of underlying metal. This clearly explained why the inner via was much weaker and was more prone to stress-induced voiding. This work led to a better understanding on the sacrificial role of redundant

via which caused minimal degradation in the SM reliability. In addition, with an in-depth understanding on stress-induced voiding, an innovative structural design, i.e. dielectric slot, was proposed and patented. The effectiveness of this new design in SM reliability enhancement was subsequently evaluated and proven.

Due to increasing SM reliability challenges with the introduction of porous ultra low-k dielectrics, early utilization of simulation model for physics study and the subsequent design for manufacturability (DFM) were recommended for improved cost and time effectiveness. In addition, the application of FEA simulation was employed on several key structural designs to illustrate their extendibility to future nanoscale technologies.

1.5 Organization of the Thesis

This thesis is organized into 9 chapters. Chapter 1 introduces the motivations and objectives; including the major contribution of this work to the advanced interconnects reliability community. It also explains the plan and organization of this thesis. Chapter 2 provides a summary of the literature review, which includes the basic understanding, test methodology, lifetime models, and mechanisms of stress-induced voiding in Cu interconnects. In addition, it provides an overview of the key SM reliability issues and challenges encountered by the reliability community with the integration of Cu and low-k dielectrics. Chapter 3 describes the fabrication process steps, test structure designs, test methodology, failure criterion and physical analysis methods employed. The details of a 3D FEA simulation model developed for physic studies are also provided.

Chapter 4 studies the different mechanisms of stress-induced voiding. The chapter examines the inter- and intra-levels, and geometrical dependency of SM reliability. Different methods of physical analysis and FEA simulation were explored to study and analyze the stress-induced voiding mechanisms. Several coping strategies such as process and structural approaches were also provided. In Chapter 5, the work dwells deeper to identify the dominant mechanism, and also describes and explains the process of stress-induced voiding. In Chapter 6, the attention shifted to study the effect of structural design on SM reliability. The application of FEA simulation was shown by providing detailed information to identify the main mechanism of redundant via structure responsible for the SM reliability improvement. After understanding the physics of the stress-induced voiding and the importance of the structural design for robust SM reliability, an innovative structural design was proven in Chapter 7 to suppress the stress-induced void failure in Cu interconnects. Chapter 8 discusses the future challenges and analyzes the extendibility of several key approaches to future CMOS technologies so as to make porous ultra low-k Cu interconnects more resilient to SM degradation. Chapter 9 concludes the thesis by providing an overall summary and recommendations of this work.

CHAPTER 2

LITERATURE REVIEW

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- 2.1 Hydrostatic and von Mises Stresses**
 - 2.2 Active Diffusion Volume**
 - 2.3 Stress Gradient**
 - 2.4 Vacancy Sources**
 - 2.5 Test Methodology**
 - 2.6 Models for Stress-induced Voiding Time-to-failure**
 - 2.7 Stress-induced Voiding**
 - 2.8 Effect of Dimensional Scaling**
 - 2.9 Recent Works**
 - 2.10 Summary**
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2.1 Hydrostatic and von Mises Stresses

As a consequence of the IC processing procedure, thin film conductors are under considerable tensile stress. This is due to the difference in the thermal coefficient of expansion of metal conductor, Si and passivation, and the thermal excursions experienced by the chip during its manufacture and operation. In an encapsulated metallization, the stress levels are quite high and primarily hydrostatic. Strain of a few tenths of percent and stress approaching 10% of the elastic modulus are common. The only way to relieve a hydrostatic stress is to effect a change in volume, which requires either the formation of a void or an

extrusion depending upon the type of the stress i.e., tensile or compressive. Therefore, hydrostatic stress release will be accompanied by damages [70]. It has been experimentally observed that lowering the deposition temperature of the passivation and the tensile stress in metal film will apparently reduce the problem [24,71]. However, if tensile stress is sufficiently high, a void will form and stress gradient is the driving force of vacancy flux leading to the subsequent void growth [72-73]. This phenomenon is called stress-induced voiding in the advanced interconnect reliability community and has become a topic of considerable concern.

Unlike hydrostatic stress components, von Mises stress on the other hand may take the form of octahedral shear stress and not necessarily result in the volumetric changes of the material [30-31]. Generally, it is used as a criterion for evaluating plastic deformation. Hence, if a large von Mises stress is present within a system, failure by plastic deformation could occur. In Chapter 4 of the thesis, von Mises stress is used to verify the interpretation of an open circuit via with a portion of its diffusion barrier layer ripped off from the underlying metal lead.

2.2 Active Diffusion Volume

As discussed, vacancy motion causes stress-induced voiding and is controlled by the diffusional mechanisms, which are active within a given material. From a mass transport perspective, three major volumetric scales can be used to define the diffusional problem [10]. The first is the interconnect volume given by the product of length, height, and width within

the formation of the damage. The second is the diffusion volume available to supply vacancies that will coalesce to form void during a given SM test. The third is the stress gradient region where a significant driving force exists to compel vacancies to migrate towards a specific voiding site.

The interconnect volume is much simpler to define compared to the diffusion volume and the stress gradient region. The diffusion volume will depend on the active diffusion mechanisms present, the stress temperature and the stress time. The diffusion pathways that define the diffusion volume may be able to extend for long distances depending on the stress temperature and time; however, a diffusion pathway is usable only when a sufficient driving force exists. Recent study in the literature estimated the magnitude of the driving force to be 6.2 MPa/ μm [10].

The stress gradient region will depend on the geometrical factors that define the interconnect system, material properties of metal, barrier, dielectrics, and local stress levels developed at the stress temperature. The stress level within the stress gradient region is time-dependent since the voiding process would presumably evolve and eventually relax the local stress levels originally present at the start of the SM test. Only those vacancies within the active diffusion volume are able to participate in the voiding process. This active diffusion volume cannot exist without the interconnect volume, the diffusion volume, and the stress gradient region being simultaneously present at a specific site within an interconnect. Hence, the active diffusion volume is defined by the smallest of the three volumes surrounding the vulnerable stress-induced voiding site in a so-called coexistence region.

2.3 Stress Gradient

Empirically, the time-averaged vacancy flux is given by:

$$J = \frac{N_{\text{vac}}}{A_{\text{flux}} \cdot t_F} \quad \text{Eq. (2.1)}$$

where N_{vac} is the total number of vacancies having passed through to cause voiding,

A_{flux} is the area of the diffusion path and

t_F is the failure time.

The role of stress gradient is shown as follows [75]. The vacancy flux under a driving force can be expressed as:

$$\begin{aligned} J &= C(x, t) \cdot M \cdot F \\ &= C(x, t) \cdot \frac{D_{\text{0eff}} \exp(-Q_{\text{eff}}/k_B T)}{k_B T} \cdot \Omega \left(-\frac{\Delta\sigma}{\Delta x} \right) \end{aligned} \quad \text{Eq. (2.2)}$$

where J is the vacancy flux due to a stress gradient,

$C(x, t)$ is the local concentration,

M is the diffusional mobility,

F is the driving force,

D_{0eff} is a effective diffusional prefactor,

Q_{eff} is an activation energy,

k_B is the Boltzmann constant,

T is the test temperature,

Ω is the local atomic volume and

$\Delta\sigma/\Delta x$ is the local stress gradient.

The term Δx is meant to specify a generic linear dimension in the stress gradient and is not meant to define a specific coordinate system. The term $F = \Omega(-\Delta\sigma/\Delta x)$ is the force per vacancy that is derived from a stress gradient. Note that for simplicity, a diffusional counter flux ($\approx -D \cdot \partial C(x,t)/\partial x$) due to chemical potential differences is ignored. Also, in this study, since the lengths of the wide metal leads, 70 μm and 140 μm , are much longer than the diffusion length, 10 μm [10], involved in the void formation, it is assumed that any vacancy that is removed due to stress-induced voiding should be replaced from the nearly infinite source of vacancies within the entirety of the metal lead outside the active diffusion volume boundary. Hence, the diffusion counter flux across this boundary should be small. This means that the vacancy concentration within the active diffusion volume should remain relatively constant throughout any finite bake test.

For simplicity, if the amount of vacancies within a metal lead is assumed to be infinite and is represented by a constant, f , the local vacancy concentration would be a constant which is approximately proportional to the inverse of the atomic volume, $f\Omega^{-1}$, where f is a number that can range between 0 and 1, Eq. (2.2) is simplified to:

$$J = f \cdot \frac{D_{\text{eff}} \exp(-Q_{\text{eff}}/k_B T)}{k_B T} \cdot \left(-\frac{\Delta\sigma}{\Delta x} \right) \quad \text{Eq. (2.3)}$$

Eq. (2.3) can be used to estimate the level of stress gradients i.e. $\Delta\sigma/\Delta x$, required to cause a void.

2.4 Vacancy Sources

Cu deposited by ECP at room temperature is a rather rapid process and defects are effectively trapped during the deposition process. As such, the formation of vacancies during ECP is undoubtedly a major source of a high non-equilibrium vacancy concentration in Cu. These vacancies will presumably migrate and nucleate into voids as a multi-level interconnect system is fabricated. If such voids are small enough, their impact on resistance will be negligible prior to SM test and will establish large initial stress gradients that other vacancies can migrate towards to during thermal stress. Thus a significant resistance change during SM test would be observable.

Another possible contributor to excess vacancies is post-ECP process. Since the equilibrium vacancy concentration in bulk Cu at 423K is negligible, another thermally related process must contribute more vacancies. It was reported that vacancies generated exclusively through thermal expansion cannot sufficiently account for the observed voids size, assuming all the extra volume from the thermal expansion goes into forming excess vacancies [10]. Thus, heat treatment in static Cu after ECP will not generate sufficient vacancies.

Realistically, Cu that is fabricated in a manufacturing environment using fast deposition rate by ECP method is far from static. Cu is known to undergo room temperature recrystallization after ECP where the median grain size can change by an order of magnitude over several days [76-78]. Cu is also known to have significant grain growth during thermal annealing, even at relatively modest temperatures in comparison to its melting point [25]. Grain growth essentially eliminates excess free space within the volume of the Cu caused by an excess density of small grains. When the surface of a Cu film is free, the excess vacancies generated through the elimination of grain boundaries should be annihilated upon reaching the free surface.

In the case of Cu interconnects that are confined, any vacancies generated through significant amounts of grain growth will be unable to leave the Cu material. As a consequence, the remaining boundaries, interfaces, and even the bulk grains will become necessarily supersaturated with vacancies. Since grain growth would be expected to sweep outwards in a direction normal to the boundary surface, the grain boundaries appear to be the most likely region for vacancy storage. An additional contributor to constrained grain growth at lower metal levels would be the additional thermal treatments that occur during processing of metal layers at higher levels.

2.5 Test Methodology

As discussed in the previous sections, SM is predominantly impacted by thermally induced stress in metal interconnects and diffusion of vacancies. As shown in Fig. 2.1, at low

temperatures, metal is under high tensile stress due to thermal expansion mismatch between different materials. As temperature is increased, the stress relaxation rate from diffusion increases but the absolute stress decreases.

Fig. 2.1: Schematic illustration of the temperature dependence of thermal misfit strain in an interconnect and vacancy diffusivity, which leads to a peak in the rate of stress-induced voiding at an intermediate bake temperature between the two mechanisms [79-81].

A SM model was developed by J. W. McPherson and C. F. Dunn to quantify the voiding mechanism according to a standard reliability analysis [79-81]:

$$R = C(T_0 - T)^N \exp\left(-\frac{Q}{k_B T}\right) \quad \text{Eq. (2.4)}$$

where R is the creep rate,

C is a proportionality constant,

T_0 is the stress-free temperature and the temperature at which the thermomechanical stress transitions from tensile to compressive,

T is the test temperature,

N is the creep exponent,

Q is the diffusional activation energy and

k_B is the Boltzman constant.

The creep rate is a strong function of the test temperature and T_0 . The parameter T_0 is dependent on the thermal history and the initial stress state of the metal. Therefore, the choice of an appropriate test temperature is critical to quantify SM reliability. As reported in the literature, SM test conditions are typically in the range from 168 to 1000 hours at a fixed temperature of 150°C to 300°C [15]. The test usually involves the measurements of the change in interconnect resistance with the failure criterion in the range from 10% to 20%.

2.6 Models for Stress-induced Voiding Time-to-failure

The coefficient of the thermal expansion of SiO_2 (α_{oxide}) is much smaller than that of metal (α_M), and therefore the interconnect is in a state of higher tensile stress when it is cooled down from high deposition temperature of the encapsulating oxide (T_{dep}) to a lower storage temperature (T_{str}). The initial thermally-induced stress in the metal lead can be expressed by [26]:

$$\sigma_0 = E_{\text{eff}} (\alpha_M - \alpha_{\text{oxide}}) (T_{\text{dep}} - T_{\text{str}}) \quad \text{Eq. (2.5)}$$

where E_{eff} is an appropriate elastic modulus.

Immediately after the deposition, stress relaxation processes start in the metal lead, for example diffusional creep, dislocation climb, and/or glide. In a simplified scenario we assume diffusional creep as the dominant relaxation mechanism within the considered temperature and stress range [82-83]. The plastic strain rate under the influence of an external stress (σ) at the temperature T_{str} is given by Gibbs equation [84]:

$$\dot{\epsilon}_{\text{pl}} = a \frac{D}{k_B T_{\text{str}}} \sigma \quad \text{Eq. (2.6)}$$

where $D = D_{0\text{eff}} \exp(-Q/k_B T)$ is the diffusivity with an activation energy (Q) of the respective diffusion mechanisms. The constant (a) contains microstructural and geometrical parameters. It differs for grain boundary and bulk diffusion. In a (quasi) steady state, at a constant storage temperature, the total strain rate $\dot{\epsilon} = \dot{\epsilon}_{\text{pl}} + \dot{\epsilon}_{\text{elastic}}$ is zero and using Hooke's Law, we have:

$$\dot{\epsilon}_{\text{pl}} = -\dot{\epsilon}_{\text{elastic}} = -\dot{\sigma}/E_{\text{eff}} \quad \text{Eq. (2.7)}$$

Hence with Eq. (2.6), Eq. (2.7) becomes:

$$\dot{\sigma}(t) + a E_{\text{eff}} \frac{D}{k_B T_{\text{str}}} \sigma(t) = 0 \quad \text{Eq. (2.8)}$$

and it gives a solution of:

$$\sigma(t) = \sigma_0 \exp(-t/\tau) \quad \text{Eq. (2.9)}$$

with a time constant:

$$\tau = k_B T_{\text{str}} / a E_{\text{eff}} D \quad \text{Eq. (2.10)}$$

It is assumed that a change in the plastic strain leads to an increase in the void volume. This implies an increase of the interconnect resistance whose absolute value depends on its geometry, void size and void shape. The failure of an interconnect is defined by a certain amount of resistance increase at a given storage temperature and the time taken for the failure to occur is defined as time-to-failure (TTF). The change in the plastic strain ($\Delta \epsilon_{\text{pl}}$) which is necessary to produce the failure can be expressed by:

$$\Delta \epsilon_{\text{pl}} = \epsilon_{\text{pl}}(\text{TTF}) - \epsilon_{\text{pl}}(t=0) = \int_0^{\text{TTF}} \dot{\epsilon}_{\text{pl}}(t) dt \quad \text{Eq. (2.11)}$$

and with Eq. (2.6) and Eq. (2.9):

$$\Delta\epsilon_{pl} = \frac{aD}{k_B T_{str}} \sigma_0 \tau \left(1 - \exp\left(-\frac{TTF}{\tau}\right) \right) \quad \text{Eq. (2.12)}$$

Based on the reported experimental results [26], we assume further that $TTF \ll \tau$ and this approximation follows:

$$TTF \approx \frac{\Delta\epsilon_{pl}}{a} \frac{k_B T_{str}}{D \sigma_0} = \frac{\Delta\epsilon_{pl}}{a} \frac{k_B T_{str}}{D_{0eff} \sigma_0} \exp\left(\frac{Q}{k_B T_{str}}\right) \quad \text{Eq. (2.13)}$$

Within process qualification, it is important to take into account that a certain amount of the initial stress has already been relaxed in the period between the deposition process and the start of the SM test. Therefore a reduced initial stress (σ_0^*) can be considered instead of σ_0 by introducing a “reduced” or “effective” deposition temperature (T_{dep}^*) in Eq. (2.5), which is lower than the temperature T_{dep} . Finally, we find an equation for the TTF due to the growth of the stress-induced voids as:

$$TTF \approx C \frac{T_{str}}{T_{dep}^* - T_{str}} \exp\left(\frac{Q}{k_B T_{str}}\right) \quad \text{Eq. (2.14)}$$

where

$$C = \frac{k_B \cdot \Delta\epsilon_{pl}}{a \cdot D_{0eff} \cdot E_{eff} \cdot (\alpha_M - \alpha_{oxide})} \quad \text{Eq. (2.15)}$$

Eq. (2.15) contains constants and parameters, which are assumed to be independent on the temperature within the considered temperature range. For a given set of identical test structures, C represents a specific constant.

Similar to the Black's equation, Eq. (2.14) allows the transformation of the TTF from the high storage temperature to the operation temperature. Similar equations have been reported in [79,85], which differ from Eq. (2.14) only in the pre-exponential temperature dependence. For example, JEDEC [85] is proposing the following equation for the MTF in SM in analogy to the Black's Law:

$$\text{TTF} = C^* \frac{1}{(\Delta T)^2} \exp\left(\frac{Q}{k_B T_{\text{str}}}\right) \quad \text{Eq. (2.16)}$$

where C^* is a constant and

ΔT is the difference between the (effective) passivation deposition temperature and the storage temperature.

As a consequence, slight differences in the values of the activation energy (and hence of the extrapolated lifetime) are determined when using Eq. (2.16) instead of Eq. (2.14).

2.7 Stress-induced Voiding

Failures in microelectronics devices can be categorized as intrinsic or extrinsic. Generally, intrinsic failures are inherent in the designs and materials used. They are typically caused by wear out and is managed rather than eliminated, such as ensuring that the wear out occurs beyond the useful life of a product. On the other hand, extrinsic failures are due to process defects. They are dependent on defectivity associated with the semiconductor and packaging processes, and the complexity of the design and manufacturing processes. Extrinsic failures are managed through the application of best practices used to improve process quality and yield.

Fig. 2.2: Void was observed within a SM tested via.

Fig. 2.3: Void was observed beneath a SM tested via [10].

SM is an intrinsic wear out failure that causes an open circuit in metal interconnects, especially in via since it is the weakest link in the chain of interconnects that make up a working IC. Two types of stress-induced voiding were reported in the literature. One was found to form within a via which was connected to a wide top metal lead (see Fig. 2.2). The other was found to form beneath a via which was connected to a wide bottom metal lead (see Fig. 2.3). The mechanisms that result in the formation of the stress-induced voids will be discussed in Sections 4.1 and 4.2.

2.8 Effect of Dimensional Scaling

If the stress levels are preserved in an interconnect system with the size of the via varied, then the associated stress gradient might be expected to increase inversely proportionate with via size. The total number of required vacancies ($N_{\text{vac}} = V_{\text{void}}/\Omega$) can be assumed to equal to a volume that is some fractions of a sphere defined by the dimension of

the via width. A convenient representation of this volume could be the volume of a half-sphere or $2\pi w_{\text{via}}^3/3$, where the half sphere radius is chosen to be the via diameter (w_{via}). In some time interval, a flux of vacancies from within the active diffusion volume will need to move this volume to cause the via to open. The flux area is proportional to the via width for an interface or grain boundary diffusion mechanism and can be represented by via perimeter times the pathway width or $\pi w_{\text{via}}\delta$, where δ is the width of the diffusion pathway. Thus, the diffusional flux will show a w_{via}^2 dependence. If one solves for the failure time (t_F) in Eq. (2.1) using Eq. (2.3), t_F can be expressed as:

$$t_F = \frac{2W_{\text{via}}^2}{3\delta} / f \cdot \left(\frac{D_{\text{eff}} \exp(-Q_{\text{eff}}/k_B T_{\text{str}})}{k_B T_{\text{str}}} \right) \cdot \Omega \cdot \frac{\Delta\sigma}{\Delta x} \quad \text{Eq. (2.17)}$$

The above equation supports that halving the via dimension will decrease the lifetime by a factor of 4 if the stress gradient is assumed to be roughly constant [10]. This explanation is mainly for illustration, since great uncertainty lies with how the stress gradient evolves with time.

2.9 Recent Works

Fig. 2.4: Schematic diagrams of SM in dual damascene Cu interconnects reported by T. Oshima *et al.* [27].

As reported in Section 2.7, voiding within and beneath via typically causes stress-induced failures. Several different failure mechanisms associated to the stress-induced voiding within via were reported. As shown in Fig. 2.4, T. Oshima *et al.* [27] explained that Cu atoms in via were squeezed out with thermal stress caused by the surrounding dielectric, which has large Young's modulus and Cu expansion. The migration of Cu atoms in the via resulted in the voiding since the movement was irreversible.

Fig. 2.5: Schematic diagrams of voids and stress migration within via reported by G. B. Alers *et al.* [25].

On the other hand, G. B. Alers *et al.* [25,28] reported two other possible failure mechanisms. Figure 2.5 shows a failure mechanism initiated from one or more etch-related or fill-related voids in the metallic Cu that forms the via. Through high thermal stress, the voids coalesced and migrated to the via bottom, resulting in an open connection between the via and the diffusion barrier layer at its bottom. The other failure mechanism was related to the high level of tensile stress in Cu after a thermal cycle. At high temperature, Cu will expand more than the oxide trench enclosure thus inducing a compressive stress in Cu. Cu will recrystallize and relax through dislocation motion at these high temperatures. Upon cooling, Cu will contract and tensile stress builds up, resulting in an ambient temperature

tensile stress that is greater than the deposited stress. This internal tension if sufficiently large can simply rip the via off the diffusion barrier layer on the underlying metal lead.

Fig. 2.6: Schematic diagrams of stress-induced voiding beneath via reported by E. T. Ogawa *et al.* [10]. Vacancy generation through grain growth in constrained metal leads. Constrained small grains that underwent grain growth could not eliminate trapped vacancies at a free surface. Stress gradient developed beneath the via attracted vacancies to coalesce into voids.

In the case of the stress-induced voiding beneath via, two different failure mechanisms were reported. E. T. Ogawa *et al.* [10] explained that for a confined Cu, which did not undergo any prior annealing, the vacancies generated through significant grain growth

subsequently will be unable to leave the Cu material. As a consequence, the remaining boundaries, interfaces and even bulk grains will become supersaturated with vacancies. Since grain growth is expected to sweep outwards in a direction normal to the boundary surface, the grain boundaries is the most likely region for vacancy storage. The subsequent via placement over the interconnect would generate a stress concentration that attracts vacancies within a given active diffusion volume. The general scenario of constrained grain growth leading to vacancy supersaturation is shown in Fig. 2.6.

Fig. 2.7: Schematic diagram of the model of voiding beneath via reported by T. Oshima *et al.* [14].

On the other hand, T. Oshima *et al.* [14] explained that the driving force of the void formation is the volume contraction of Cu, which is the stress. The voiding proceeds through the thermal diffusion of vacancies through grain boundary as the main diffusion path. In addition, the vacancies concentrate under the via bottom because the stress concentration caused by structural discontinuity occurs at the via bottom. The schematic diagram of his

model on the voiding beneath via is shown in Fig. 2.7. The above discussions clearly illustrate that despite many extensive studies, the mechanisms responsible for the stress-induced voiding are still not well understood.

Fig. 2.8: FEA of dual-damascene via placed over a wide metal lead with the associated hydrostatic stress contours reported by E. T. Ogawa *et al.* [10].

Contradictory results and discussions are also reported. For example, both E. T. Ogawa *et al.* [10] and C. J. Zhai *et al.* [22] used a stress modeling to study and explain the stress distribution beneath via that connects to a wide Cu metal lead. However, the simulation results obtained were significantly different. E. T. Ogawa *et al.* reported that a local region of higher tensile stress was situated directly underneath a via center, whereas a

local region of lower tensile stress was located near the edge of the via (see Fig. 2.8). These two regions of stress concentration led to a prominent stress gradient under the via that drives vacancies under the via towards its bottom perimeter. On the other hand, as shown in Fig. 2.9, C. J. Zhai *et al.* reported that the maximum tensile stress occurs at the edge of the via and the via/line interface, leading to a valley-like stress profile at the via bottom which has a local low-tensile stress region. Therefore the atoms tend to migrate into the surrounding higher tensile stress region from the via bottom, where the tensile stress is relatively lower.

Fig. 2.9: Contour plot of hydrostatic stress of via placed over a wide metallization reported by C. J. Zhai *et al.* [22].

Studies on the structural dependency of stress-induced voiding are also of great interest. Though several reports reported the effectiveness of redundant via structure in improving SM reliability of Cu interconnects, the mechanism responsible for its improvement remains unclear. K. Yoshida *et al.* [13] explained that when void nucleated and grew beneath one via, the local stress beneath the adjacent via in the same effective diffusion area would be

reduced. The tensile stress became smaller than the critical value for void nucleation thus the adjacent via survived from stress-induced failure (see fig. 2.10). On the other hand, T. C. Huang *et al.* [29] reported that stress profile from FEA simulation showed minimal change for the bulk of the structure other than minor variation close to the via area. The stress at the via bottom was found to be lower than that at the center of wide metal lead, implying that the stress reduction effect was minor compared to the stress distributions in the wide metal area from which the vast vacancy supply. Thus, it was concluded that the dummy via provided another destination for the migrating of vacancies, which led to improved SM reliability.

Fig. 2.10: Illustration of stress change with duration as reported by K. Yoshida *et al.* [13]. In the case when the stress beneath one via became lower, other via in the same effective diffusion area could survive from stress-induced voiding.

2.10 Summary

This chapter summarizes the learning gained through the literature review. The basic understandings on stress-induced voiding such as the driving force of void nucleation and

various factors affecting its growth such as active diffusive volume, stress gradient, and the various sources of vacancy are reviewed. The SM test methodology, the models for stress-induced voiding time-to-failure and types of the stress-induced voiding are also presented. As technology advances, downward interconnect scaling was reported to degrade the SM lifetime. In addition, recent studies on the mechanisms of the stress-induced voiding, stress simulation and structural dependency of SM reliability are reviewed. Despite the extensive studies, the mechanisms of the stress-induced voiding remain unclear. Contradictory stress simulation results are found and the mechanism of redundant via in improving the SM reliability of Cu interconnects is uncertain. These doubts will be addressed via the subsequent chapters in this thesis.

CHAPTER 3

EXPERIMENTAL DETAILS

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- 3.1 Fabrication Process**
 - 3.2 Test Structures**
 - 3.2.1 Via Chain Structures with Nominal Width Metal Leads**
 - 3.2.2 Via Chain Structures with Wide Top Metal Leads**
 - 3.2.3 Via Chain Structures with Wide Bottom Metal Leads**
 - 3.2.4 Via Chain Structures with Dielectric Slots**
 - 3.3 Test Methodology and Failure Criterion**
 - 3.4 Physical Analysis Methods**
 - 3.5 Stress Measurement Techniques**
 - 3.6 Three-dimensional FEA Stress Simulation Model**
 - 3.7 Summary**
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3.1 Fabrication Process

The interconnect fabrication process used in this work was based on a standard 0.13 μm , 6-layer metallization technology with single damascene Cu on metal 1 (M1) and dual damascene Cu on the subsequent via (Vx) and metal lead (Mx), where x denotes the metallization layer. Chemical vapor deposition (CVD) dielectrics with dielectric constant values in the range from 3.5 to 3.7 and 2.7 to 3.0 were used in this work. Owing to over etch

during the via bottom opening and physical Argon (Ar) sputtering, which was employed to clean the via bottom prior to PVD of a Ta-based diffusion barrier layer, a via gouging of around 300Å to 400Å into the underlying Cu metal lead was formed. During the Cu process, Cu was ECP on a seed layer and was annealed at an elevated temperature. The Cu surface was passivated with a layer of Si₃N₄ after the redundant Cu was removed by a CMP process. Finally, the 6-layer metallization was capped with a thick passivation layer and was subjected to a short duration of forming gas anneal for defect curing before the completion of the fabrication process.

3.2 Test Structures

As discussed in Chapter 2, two different types of stress-induced voiding in Cu interconnects, namely void within and beneath via, were reported. Also, stress-induced voiding is commonly known to be process and structural dependent. As such, several test structures were designed in this work to study the phenomena of stress-induced voiding and to achieve a good and in-depth understanding of the associated failure mechanisms.

3.2.1 Via Chain Structures with Nominal Width Metal Leads

Figure 3.1 shows via chain structures with nominal width metal leads used to study the phenomenon of stress-induced voiding within via at different metallization layers. In order to achieve accurate readings consistently in each measurement and the resemblance of

large volume of interconnects in IC chips under operating conditions, all via chain structures were designed with a large number of links. Isolated via structures were not recommended and employed in this work because high current is required to achieve an accurate reading.

Fig. 3.1: Typical via chain structures used in the experiment.

- (a) Cross-section along metal lead.
- (b) Schematic of the cross-section across metal lead.
- (c) Summary table of via chain structures with nominal width metal leads.
 V_x and M_x denote via and metal interconnects respectively; where x denotes the metallization layer.

Table 3.1 shows the voltage specifications of the Keithley K4200 equipment employed to measure the resistance of the SM test structures. As shown in Table 3.2, due to the low resistance of isolated via structure, a current of 10 times higher than that of the via chain structure is needed to achieve a better accuracy for the voltage measurement. Hence, the isolated via structure is subjected to a high current density of $277 \text{ mA}/\mu\text{m}^2$ which could lead to electrical overstress.

Table 3.1: Voltage specifications of Keithley K4200 equipment.

Voltage Range (V)	Measurement	
	Resolution	Accuracy $\pm (\% \text{ rdg} + \text{volts})$
200	0.00002	0.015% + 0.003
0.2	0.000001	0.012% + 0.0001

Table 3.2: Test condition setting for via resistance measurement.

Via	Resistance (Ω)	Current (A)	Voltage (V)	Accuracy ($\pm V$)	Current Density ($\text{mA}/\mu\text{m}^2$)
Chain	100000	0.001	100	0.018	27.7
Isolated	1	0.001	0.001	0.0001	27.7
	1	0.01	0.01	0.000101	277

3.2.2 Via Chain Structures with Wide Top Metal Leads

With the understanding that a wider interconnect will have a larger total supply of vacancies than a narrow one, hence stress voiding in wider interconnect is more predominant in a given bake time interval. As such, via chain structures with wide top metal leads as

shown in Fig. 3.2, were used to further study and enhance the understanding on the phenomenon of the stress-induced voiding within via. In general, for metal lead width that is greater than 3 times the minimum design rule is considered as wide. In this case, the width of the top metal lead (i.e. M2) is much wider as compared to that of the bottom metal lead (i.e. M1). In addition, dual-via structure was designed to study the effect of redundant via on the stress-induced voiding within via.

Fig. 3.2: Via chain structures with wide top metal leads.

- (a) Layout of a single-via structure.
- (b) Layout of a dual-via structure.
- (c) Schematic of the cross-section of AA' in (a) and (b).
- (d) Summary table of via chain structures with wide top metal leads and number of vias per link.

3.2.3 Via Chain Structures with Wide Bottom Metal Leads

Fig. 3.3: Via chain structures with wide bottom metal leads.

- (a) Layout of a single-via structure.
- (b) Layout of a dual-via structure.
- (c) Schematic of the cross-section of AA' in (a) and (b).
- (d) Summary table of via chain structures with bottom metal leads of different widths, lengths and number of vias per link.

As discussed in Section 3.2.2, the total supply of vacancies is larger for wider interconnect hence stress-voiding is more predominant. Via chain structures with wide bottom metal leads as shown in Fig. 3.3 were used to study the phenomenon of the stress-induced voiding beneath via. The width of the bottom metal lead (i.e. M1) is much wider than that of the top metal lead (i.e. M2). Also, bottom metal leads of different widths and

lengths, and dual-via structure was designed to evaluate the geometrical dependency and effect of redundant via on the stress-induced voiding beneath via, respectively.

3.2.4 Via Chain Structures with Dielectric Slots

Small dielectric blocks that are commonly used in wide Cu metal leads to prevent dishing during CMP process were specially redesigned as another alternative to manage stress-induced voiding in Cu interconnects. As shown in Fig. 3.4, the design focused on incorporating a horseshoe-like dielectric slot into the wide top and wide bottom metal leads using a damascene process without additional masking steps. The SM robustness of the corresponding via chain structures with dielectric slot and dual-via was compared and reported in Chapter 7.

Fig. 3.4: Via chain structures with dielectric slots.

- (a) Layout of a wide top metal lead structure with dielectric slot.
- (b) Schematic of the cross-section of AA' in (a).
- (c) Layout of a wide bottom metal lead structure with dielectric slot.
- (d) Schematic of the cross-section of AA' in (c).
- (e) Summary table of via chain structures with dielectric slot in wide top and wide bottom metal leads.

3.3 Test Methodology and Failure Criterion

The via chain structures were subjected to high temperature stress from 150°C to 300°C using Despatch LCD1-51N ovens. A wafer was kept at room temperature as a control to ensure that the resistance change of the via chain structures at every read-out of the SM test was attributable to the stress. The resistance of the via chain structures was measured at intervals of 250, 500 and 1000-hour. As shown in Eq. (3.1), the resistance measured at each read-out (R_{readout}) was compared to the initial resistance (R_{initial}) to determine the percentage change in the via chain resistance (ΔR). In this work, the failure criterion was defined as a 20% increase in the via chain resistance.

$$\Delta R = |R_{\text{initial}} - R_{\text{readout}}| / R_{\text{initial}} \times 100\% \quad \text{Eq. (3.1)}$$

3.4 Physical Analysis Methods

Owing to the large number of vias in the via chain structures used, passive voltage contrast (PVC) technique in SEM with a resolution in the range of pA was employed to isolate and locate the failure site when the via chain structure showed high resistance after a SM test. Reactive ion etching (RIE) and mechanical polishing were employed using a NE860 system and Allied polisher, respectively; to selectively delayer the dielectric layers and Cu metal leads until the top metal of the stress-induced damaged via chain was physically revealed. During PVC analysis using a LEO 1530 SEM, an Al pad of the via

chain structure was grounded and the electron beam accelerating voltage was adjusted to maximize the secondary electron yield. This caused a positive potential on the surface of the sample.

Fig. 3.5: A typical PVC image of a via chain structure after a SM test. Areas with discontinuity appeared dark (as shown by D), whereas areas with good connectivity appeared bright (as shown by B). Thus, the stress-induced void could be easily detected.

As shown in Fig. 3.5, areas where there was a discontinuity, the secondary electrons generated were attracted by the positive potential surface thus it appeared dark (as shown by D). On the other hand, areas with good connectivity, the surface of the sample would be grounded and the secondary electrons generated could be detected by the electron beam detector thus it appeared bright (as shown by B). The difference in the contrast helped to locate the failed via easily. Subsequently, TEM analysis was performed using a Philips Tecnai F20 S-Twin to study the associated failure mechanisms. In addition, further RIE was conducted to reveal the stress-induced damaged via(s) totally and the extent of the void

growth was examined using SEM. Figure 3.6 shows an example of the SEM micrograph of a stress-induced damaged via taken at a high tilted angle.

Fig. 3.6: SEM micrograph of a stress-induced damaged via taken at a high tilted angle.

The dotted line indicates the extent of the void growth that caused an open circuit beneath the gouging via.

3.5 Stress Measurement Techniques

Over the last decade, various quantitative and qualitative techniques have been developed for residual stress measurement. In general, they are either classified under destructive or non-destructive methods. The first category of methods is based on the destruction of the state of equilibrium in the mechanical component. The residual stress is then evaluated from its relaxation. However, it is only possible to measure the consequences of the stress relaxation such as displacement, fracture and strain, and not the relaxation itself. In most cases, the strain change is selected as the parameter to be studied. The second

category of methods is based on the relationship between a physical parameter measured by different non-destructive techniques such as x-ray, ultrasound and magnetic.

x-ray is one of the more popular non-destructive techniques employed for residual stress measurement. It is based on the measurement of lattice strains by studying the variations in the interplanar spacing of the polycrystalline material. Also, it is often used to measure residual stress values in thin film layers but several precautions have to be taken. The main challenges in analysing films with thicknesses varying from a few nanometers to a few micrometers deposition on a substrate are the weakness of the diffracted intensity and the superposition of the substrate peaks as regards the analysed peaks. In order to overcome these challenges, the principle is to reduce the x-ray penetration thickness inside the material by decreasing the incident angle of the x-ray to a few degrees. In this case, the position of the sample is very important to the accuracy of the measurement. Furthermore, x-ray technique measures only the average stress in the line structures. It does not determine stress distribution in the metal line or local stress field because of the concentration at small geometries. Therefore, finite element analysis method is used to evaluate the local stress/strain fields.

3.6 Three-dimensional FEA Stress Simulation Model

Despite many studies in the literature, the SM reliability of Cu interconnects with gouging via is seldom reported. However, as discussed in Section 3.1, via gouges into the underlying metal lead during the conventional Cu interconnect fabrication process is

inevitable due to the over etch and cleaning at the via bottom. Also, future Cu interconnects technology is expected to have a more robust PVD diffusion barrier layer achieved by the barrier first method, therefore via gouging is unavoidable. As shown in Fig. 3.7, a 3D finite element mesh description of a two-level via-metal lead structure was developed using a commercial FEA software, ANSYS. The model was designed with a gouging via to achieve a more accurate stress simulation and was used to study the stress distribution around the via of the structures discussed in Section 3.2 during a SM test.

Fig. 3.7: A 3D finite element mesh description of a two-level via-metal lead structure used to study the stress distribution around a gouging via during a SM test.

In the simulation, complexity arose as the via was modeled using a circular surface while the metal leads and surrounding dielectrics were modeled using a rectangular surface. Such connection required both the cylindrical and rectangular co-ordinate systems to be considered in the model, and a proper connection between the two co-ordinate systems was

necessary. Hence in our simulation model, every node in the meshing was created by defining its co-ordinates, and the associated brick element was formed connecting to the 8 adjacent nodes with a set of well-defined material properties. In order to obtain a precise model and convergences in the modeling solution, a total of approximately 125,000 elements were employed for discretization.

In this model, the thickness of the metal leads was chosen to be in the range of 2500-3700Å, and the diffusion barrier layer coverage at the sidewall and bottom of the metal leads was approximately 60Å and 200Å, respectively. The height of the via was in the range of 3500-4000Å with a gouging of approximately 300-500Å into the underlying wide Cu metal lead. The diffusion barrier layer coverage at the sidewall and bottom of the via was approximately 20Å and 120Å respectively, and the thickness of the etch stop and capping layers was 500Å.

The bottom plane of the structure was assumed to be rigidly clamped onto the substrate, thus no displacement was allowed in the z-direction. In addition, the structure was considered to be arrayed periodically along the x- and y-directions, and mirror symmetry normal to each surface was employed on the other four surfaces [30]. The stress free temperature was chosen to be 300°C [10,30] and the hydrostatic stress distribution was plotted for the case at 200°C for all the simulations represented in this work. The simulation results represent the “initial state” of the interconnect prior to any stress-induced voiding. The thermo-mechanical properties of the materials employed in the simulation are summarized in Table 3.3 as per the literature [86-90].

Table 3.3: Thermo-mechanical properties of the materials employed in the 3D FEA stress simulation model [30-31,86-90].

Materials	Modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
Cu	129.8	0.339	16.5
Ta	186.2	0.35	6.48
Si ₃ N ₄	221	0.27	3.2
SiC	103.7	0.27	11
FSG	48	0.16	0.5
SiCOH	15	0.21	9
pSiCOH	3.85	0.28	16
SiLK	3.5	0.35	62

The stress simulation model developed in this work was verified using the stress simulation and experimental stress measurement data reported by Paik *et al.* [34]. Using the material thermo-mechanical properties, boundary conditions, stress free and stress temperatures provided in his paper, the thermal stress simulation is repeated using our model. As shown in Fig. 3.8 (a), the thermal stress data obtained from the simulation model developed in this work match well with the data, Fig. 3.8 (b), reported by Paik *et al.* Figure 3.9 shows that the sum of the thermal stress and the grain growth induced stress correlate well with the experimentally x-ray diffraction (XRD) measured stress. Hence, our model is verified to be good/ reasonable for stress simulation studies.

Fig. 3.8: (a) The thermal stress data obtained from the simulation model developed in this work. (b) The thermal stress data reported by Paik *et al.* [34]. Both data match well.

Fig. 3.9: The sum of the thermal stress and the grain growth induced stress correlates well with the experimentally XRD measured stress [34].

3.7 Summary

The fabrication process and experimental details employed in this work are summarized in this chapter. Several test structures were designed to study the phenomena of stress-induced voiding and to achieve a good and in-depth understanding of the associated failure mechanisms and its structural dependency. The details of the test methodology and failure criterion employed are provided. Also, the details of the physical analysis methods employed to examine the extent of the stress-induced voiding and damaged vias are reported. Last but not least, a 3D finite element mesh description of a two-level via-metal lead structure was developed to study the stress distribution around the gouging via during a SM test. The thermo-mechanical properties of the materials employed in the model are summarized.

CHAPTER 4

STRESS-INDUCED VOIDING IN CU INTERCONNECTS

- 4.1 Stress-induced Voiding within Via**
 - 4.1.1 Inter-level SM Reliability**
 - 4.1.2 Intra-level SM Reliability**
 - 4.1.3 Failure Analysis of Stress-induced Damaged Via**
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4.1 Stress-induced Voiding within Via

As discussed in Section 2.7, two different types of stress-induced voiding were reported. One was found to form within a via and the other was found to form beneath a via. These failures are typically caused by inherent weaknesses in the structural designs, materials (including interfacial adhesion) and/or processes used, which are unavoidable and are managed by ensuring that the wear out occurs beyond the useful life of a product.

This section presents a systematic study of the stress-induced voiding phenomenon within via. Different methods of physical analysis such as PVC and TEM were performed to examine the stress-induced damaged vias. The stress-induced voiding mechanism, which caused an open circuit in Cu interconnect was explained and stress distribution in the Cu interconnect were modeled using FEA for a detailed understanding. Such stress-induced voiding phenomenon was more pronounced when Cu was integrated with dielectric of lower constant values. The details of the findings are presented in the subsequent sub-sections.

4.1.1 Inter-level SM Reliability

As illustrated in Fig. 3.1 of Chapter 3, various via chain structures (i.e. via 1 to via 4) were used to study the phenomenon of stress-induced voiding at different metallization layers. Figure 4.1 shows the percentage change in the resistance (ΔR) of via 1 to via 4 (V1 to V4) chain structures of a same design rule for various stress temperatures (T_s) after a 1000-hour SM test. Since no bias was applied during the thermal stress, the observed percentage change

in the resistance was the direct consequence of stress-induced voiding. Such interpretation was confirmed by the different degrees of the percentage change in the resistance of V1 to V4 chain structures at different stress temperatures, which may be attributed to partial voiding.

Fig. 4.1: Percentage change in the resistance of the V1 to V4 chain structures shown in Fig. 3.1 at different stress temperatures. The results show that critical temperatures occurred between 150°C and 200°C and stress-induced voiding worsened with increasing metallization layers.

Figure 4.1 shows wider spread in the percentage change in the resistance occurred between 150°C and 200°C for all vias. In addition, it was shown that the difference in the percentage change in the resistance was less pronounced at the lower level vias (i.e. V1 and V2). However, a sharper increase was observed at the higher level vias (i.e. V3 and V4). This observation suggested that higher-level vias are more prone to stress-induced voiding. This was against the expectation because in this work, V1 to V4 have the same dimension and was fabricated using the same process conditions. Hence, the lowest level via, V1, was expected to be the weakest structure since it had undergone more thermal cycles.

Fig. 4.2: The linear-like response of the radius of the curvature to the metallization layer indicated that the radius of the curvature decreased with increasing metallization layer.

The above observation could be explained by Fig. 4.2, which shows the radius of the curvature of a 200 mm patterned wafer measured at different metallization layers after the respective Cu CMP process. This wafer had a similar processing conditions as the via chain structures shown in Fig. 4.1. Figure 4.2 shows that the radius of the curvature decreased with increasing metallization layers. Based on Park *et al.* paper, the effect of wafer bowing on stress-induced voiding was reported [12]. Smaller wafer bowing was found to have smaller stress change during the cooling of Cu anneal process. Hence, stress-induced voiding was improved. In this work, as wafer bowing increases with increasing metallization layers, larger stress change is expected at the upper metallization layers during the annealing process, leading to greater via damage and SM reliability degradation. This is believed to be the main mechanism to explain the difference of the resistance change in different metallization layers after the SM test.

This finding is important because it leads to the understanding that for any meaningful comparison of the SM reliability, the study has to be performed at the same metallization layer. In addition, it is believed that stress-induced voiding in Cu interconnects will become more challenging with the implementation of more metallization layers in the near future.

4.1.2 Intra-level SM Reliability

As shown in Fig. 4.3 (a), at a 1000-hour SM test of 200°C, the percentage change in the resistance of V4 chain structures was highest at the edge and gradually decreased towards the centre of the wafer. This observation is attributed to the nature of the PVD process, which generally gives rise to a higher deposition rate at the centre of the wafer. As it is difficult to accurately quantify the thickness of the diffusion barrier layer at the via bottom sidewall from center-to-edge of the wafer using cross-sectional TEM, blanket film wafer was used instead in this work. The thickness at the center of the wafer was observed to be approximately 15-20% thicker than that at the edge of the wafer. Therefore, the via chain structures at the centre of the wafer have better and thicker diffusion barrier layer coverage at the via bottom sidewall than those at the edge of the wafer. In addition, Figure 4.3 (b) shows that the decreasing trend of the normalized via chain resistance (R) from the centre to the edge of the wafer prior to the SM test which matched well with the deposition thickness profile of the diffusion barrier layer. This supports the understanding that due to intrinsic weakness, the via chain structures at the edge of the wafer are weaker and more susceptible to stress-induced voiding. Such observation is expected to be more severe for 300 mm wafers.

Fig. 4.3: Results of a SM test at 200°C of V4 chain structures across a 200 mm wafer.

- (a) At a 1000-hour SM test, the percentage change in resistance was highest at the edge of the wafer.
- (b) Normalized resistance prior to the SM test was used for comparison. Non-uniform diffusion barrier layer thickness was the root cause of decreasing trend in R from the centre to the edge of the wafer. The notch of the wafer is indicated by the Δ on the map.

4.1.3 Failure Analysis of Stress-induced Damaged Via

Fig. 4.4: Failure analysis of stress-induced failure within via.

- (a) TEM showed a portion of the diffusion barrier layer, as indicated by the dotted circle, was ripped off from the bottom metal lead for a stress-induced damaged via reported in Fig. 4.3 (a).
- (b) EDX performed on the material indicated by the dotted circle in (a) showed Tatanium (Ta) peak.

Failure analysis was performed on some of the stress-induced damaged V4 chain structures and the results are shown in Figs. 4.4 (a) and (b). Figure 4.4 (a), an open circuit via with a portion of its diffusion barrier layer ripped off from the underlying metal lead was

found using TEM analysis. Figure 4.4 (b), Ta peak was detected using energy dispersive x-ray (EDX) analysis. The study on the stress distribution within a gouging via and the proposed failure mechanism are presented in the next two sub-sections.

4.1.4 Stress Distribution within Gouging Via

Fig. 4.5: 3D FEA hydrostatic stress modeling within via.

- (a) Schematic of a two-level via-metal lead structure with a gouging via.
- (b) The corresponding hydrostatic stress distribution within the via during a SM test. The unit of stress distribution is in Mega Pascal (MPa).

Hydrostatic stress as formulated in Eq. (4.2) with respect to principal stresses (σ_x , σ_y and σ_z) is well known to be the driving force for void nucleation [30,31]. However, when identifying the most probable void nucleation site, besides hydrostatic stress concentration, inherent weaknesses in the structural designs, materials (including interfacial adhesion) and/or processes have to be considered. These intrinsic weaknesses would lower the energy barrier, which needs to be overcome for void nucleation thus favoring the formation of void.

$$\sigma_H = \frac{\sigma_x + \sigma_y + \sigma_z}{3} \quad \text{Eq. (4.2)}$$

As discussed in Chapter 3, in today's Cu technology, a certain degree of via gouging in the Cu interconnects fabrication is inevitable. Therefore, in this work, 3D FEA stress modeling of gouging via was performed for a more accurate stress simulation. Figure 4.5 (a) shows the schematic of a gouging via. The corresponding hydrostatic stress distribution within the via during a SM test simulated by the FEA model developed in this work is shown in Fig. 4.5 (b). Due to the via position, it was observed that the hydrostatic stress distribution within the via was not symmetric. As shown in the contour plot, the right portion within the via, A, which was positioned nearer to the edge of the underlying wide metallization had a lower stress tensile stress as compared to that of the left portion within the via, B. Furthermore, high tensile stress was found to concentrate in the via around the Cu cap layer as indicated in Fig. 4.5 (b); i.e. ranging from 300 to 350 MPa. In the literature, the σ_{crit} value for void nucleation was reported to be greater than 100 MPa for Cu/SiO₂-based interconnects [91]. Hence, stress-level reported above is believed to be sufficient for void nucleation. In addition to the high tensile stress around the Cu cap layer, the intrinsic weakness resulted

from the nature of the PVD process, which gives a poorer diffusion barrier layer coverage at the via bottom sidewall, especially at the edge of the wafer, favored the nucleation of stress-induced void within the via. This was because the critical stress (σ_{crit}) for void nucleation was lowered at the edge of the wafer as compared to that at the center of the wafer.

The small void grew in size with increasing time at high temperature stressing. Figures 4.4 (a) and (b) show that during the subsequent cooling after stressing, a portion of the diffusion barrier layer underwent plastic deformation and was eventually ripped off from the underlying metal lead, resulting in an open circuit. Von Mises stress as shown in Eq. (4.3) with respect to the principal stresses is commonly used as a criterion for evaluating plastic deformation [22,30,31]. As such, simulation of the von Mises stress was performed to verify the interpretation of the physical results obtained in Figs. 4.4 (a) and (b).

$$\sigma_v = \frac{1}{\sqrt{2}} \left[(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2 \right]^{\frac{1}{2}} \quad \text{Eq. (4.3)}$$

Figure 4.6 (a) shows a schematic of a gouging via with stress-induced void formed around the via bottom sidewall. The corresponding von Mises stress distribution in the diffusion barrier layer during a SM test simulated by the FEA model developed in this work with plastic effect included is shown in Fig. 4.6 (b). As shown by the contour plot, highest von Mises stress was found to concentrate around the perimeter of a small portion of the diffusion barrier layer, which was still connected to the underlying metal lead when the stress-induced void had grown to a considerable size. Also, the deformed shape of the diffusion barrier layer was found to coincide with the detached portion of the materials

indicated by the dotted circle in Fig. 4.4 (a). Therefore, large tensile stress built up due to Cu volume contraction during cooling coupled with high von Mises stress is attributed to cause the diffusion barrier layer to undergo plastic deformation and a portion of it been detached from the underlying metal lead.

Fig. 4.6: 3D FEA von Mises stress modeling within via.

- (a) Schematic of a gouging via with stress-induced voids around the via bottom sidewall.
- (b) The corresponding von Mises stress distribution in the diffusion barrier layer during a SM test. The unit of stress distribution is in MPa.

4.1.5 Proposed Stress-induced Voiding Mechanism

Based on the understandings gained from the TEM images, EDX analysis and stress simulation results, a model as shown in Fig. 4.7 was developed to explain the stress-induced voiding mechanism within via. The corresponding schematic diagrams of the stress-induced voiding mechanism proposed in Fig. 4.7 are emphasized in Fig. 4.8 schematically for better understanding.

Fig. 4.7: Flow chart illustrating the proposed failure mechanism of stress-induced voiding that caused an open circuit within the via seen in Fig. 4.4 (a).

In Fig. 4.8 (a), the poorer diffusion barrier layer coverage at the via bottom sidewall, especially at the edge of the wafer was due to the nature of the PVD process. Owing to the

presence of the intrinsic weakness and coupled with the high tensile stress in the via around the perimeter of the Cu cap layer, void nucleated. In Fig. 4.8 (b), the small void grew in size with increasing time at high temperature stressing. During the subsequent cooling after the stressing, the largely grown void and the tensile stress built up due to a Cu volume contraction [18,25] ripped the via off the diffusion barrier layer from the underlying metal lead, as shown in Figs. 4.8 (c) and (d), leading to an eventual open failure in Fig. 4.4 (a).

Fig. 4.8: Schematics illustrating the formation sequence ((a) to (d)) of stress-induced void within the via described in Fig. 4.7.

4.1.6 Integration with Low-k Dielectric

As shown in Fig. 3.2 of Chapter 3, Via chain structure I with a wider top metal lead of a width $2.0\ \mu\text{m}$ was used to further study the phenomenon of stress-induced voiding within

via. Fig. 4.9 shows that after a 1000-hour SM test at 200°C, the SM reliability of the Cu interconnections with diffusion barrier layer deposited by the conventional method degraded when the dielectric constant (k value) was lowered to a range of between 2.7 and 3.0. This finding is against the general understanding that, as the biaxial modulus of higher porosity dielectric film decreases, the intrinsic stress decreases correspondingly. As such, the SM reliability of Cu interconnects is expected to improve [86,92]. Zhai *et al.* reported that this discrepancy could be explained by the σ_{crit} for void nucleation, which varies with inter-layer dielectric (ILD) stacks.

Fig. 4.9: The SM reliability of V1 chain structures degraded when the dielectric k value was lowered from about 3.7 to a range of between 2.7 and 3.0. Lower effective modulus and lower fracture toughness to resist interfacial delamination of higher porosity dielectric are the main contributors to the decrease of σ_{crit} needed for void nucleation thus favoring the formation of void. The data points indicated by the dotted circle correspond to the stress-induced damaged structures.

Low-k dielectrics are noted to possess lower effective modulus and lower fracture toughness to resist interfacial delamination in the damascene structure. Hence, low-k dielectrics yield lower σ_{crit} value for void nucleation. In Christine S. Hau-Riege *et al.* paper, σ_{crit} values of greater than 100 MPa and smaller than 25 MPa were reported for Cu/SiO₂-based and Cu/low-k interconnects, respectively [91]. Therefore the integration of Cu with low-k dielectric proved to be more challenging.

4.2 Stress-induced Voiding beneath Via

This section presents a detailed study of the stress-induced voiding phenomenon beneath a via. Besides TEM, physical analysis such as SEM was employed to examine the stress-induced damaged vias. Also, a possible stress-induced voiding mechanism was proposed. Similar to the previous section, a 3D FEA model was developed to study the stress distribution beneath the gouging via during a SM test for improved understanding. In addition, the geometrical dependency of the stress-induced voiding was evaluated. The details of the findings are presented in the subsequent sub-sections.

4.2.1 SM Reliability of Via Chain Structure with Wide Bottom Metal Lead

Via chain structures I to III shown in Fig. 3.3 were used to study the phenomenon of stress-induced voiding beneath via. As shown in the previous study, a maximum stress-induced voiding rate was found to occur between 150°C and 200°C. As such, Via chain

structure I was thermally stressed at this temperature range with the percentage change in the resistance monitored at the end of a 1000-hour SM test. As shown in Fig. 4.10, the maximum stress-induced voiding was observed to occur at 200°C. Furthermore, similar to the previous case, Fig. 4.11 shows that the via chain structures with the stress-induced failures were mainly observed at the edge of the wafer. This observation is again attributed to the nature of the PVD process, which results in a poorer diffusion barrier layer coverage at the via bottom sidewall, especially at the edge of the wafer [18,33]. An approximately 15-20% thicker diffusion barrier layer is observed at the center of the wafer as compared to that at the edge of the wafer by the blank film study reported in Section 4.1.2.

Fig. 4.10: Percentage change in the resistance of Via chain structure I at various stress temperatures. The points indicated by the dotted circle correspond to the stress-induced damaged structures and the small negative change in the resistance was due to statistical fluctuation of the experimental data.

Fig. 4.11: ΔR of a Via chain structure I after a 1000-hour SM test at 200°C. Stress-induced failures shown by the dotted circles were mainly observed at the edge of the wafer. This observation is attributed to the nature of the PVD process, which has lower deposition rate at the edge of the wafer. The notch of the wafer is indicated by the Δ on the map.

4.2.2 Failure Analysis of Stress-induced Damaged Via

Extensive TEM analysis was performed on the stress-induced damaged via chain structures in order to understand the physical mechanism responsible for the stress-induced voids and the associated root cause. The stress-induced void evolution corresponding to the different stages of void growth is shown in Fig. 4.12 (a) to (c). It was found that the stress-induced void nucleated at the Cu cap/via interface around the perimeter of the via. The stress-induced voiding mechanism was further studied using SEM analysis. Mechanical polishing and reactive ion etching were employed to selectively delayer the top metal and dielectric layers until SEM physically revealed the failed vias. As compared to the results

revealed by the TEM analysis, in this approach, many failed vias can be inspected in a single SEM analysis.

Fig. 4.12: Stress-induced void indicated by the dotted circle was formed at the Cu cap/via interface around the perimeter of the via. (a) to (c) correspond to the different stages of void growth.

In Fig. 4.13, a stress-induced void that resulted in an open circuit between the via and the underlying wide M1 metallization was observed after a 1000-hour of SM test at 200°C. The SEM micrograph clearly demonstrated that the void had extended significantly away from the via into the wide Cu metal lead.

Fig. 4.13: SEM micrograph of a stress-induced damaged via taken at a high-tilted angle.

The dotted line indicates the extend of the void growth that caused an open circuit beneath the via after a 1000-hr SM test at 200°C.

4.2.3 Stress Distribution beneath Gouging Via

Both Ogawa *et al.* [10] and Zhai *et al.* [22] used a stress simulation model to study and explain the stress-induced voiding mechanism beneath via with wide Cu metal lead. In both cases, the 3D FEA models did not take into account of any via gouging, and the simulation results obtained by both studies were significantly different. Ogawa *et al.* reported that a local region of higher tensile stress was situated directly underneath a via center, whereas a local region of lower tensile stress was located near the edge of the via. As a result, a prominent stress gradient under the via drove vacancies in the vicinity of the via bottom towards its bottom perimeter [10]. On the other hand, Zhai *et al.* reported that the maximum tensile stress occurred at the edge of the via, leading to a valley-like stress profile at the via bottom which indicated a local low-tensile stress region. However, based on the results reported by Zhai *et al.*, the mechanism responsible for the stress-induced voiding is

still unclear. On one hand, since void nucleation is expected when the tensile stress exceeds a critical value (i.e. the critical stress), the via/line interface was found to be more prone to void nucleation due to the high local stress concentration. On the other hand, it was explained that atoms tend to migrate into the surrounding higher tensile stress regions from the via bottom region, where the tensile stress is relatively lower [22].

Similar to the previous case, stress modeling of gouging via was performed to achieve a more accurate stress simulation. Also, as discussed earlier, besides the hydrostatic stress concentration, inherent weaknesses in the structural designs, materials (including interfacial adhesion) and processes have to be considered when identifying the most probable void nucleation site. Figure 4.14 (a) shows the schematic of a wide M1 metallization near a gouging via. The corresponding hydrostatic stress distribution around the gouging hole in the wide M1 metallization during a SM test simulated by the FEA model developed in this work is shown in Fig. 4.14 (b).

Due to the via position relatively close to the end of M1 metallization, it was observed that the hydrostatic stress around the via bottom is not symmetric. As shown in the contour plot, the right portion of the via bottom (i.e. A in Fig. 4.14 (a)) which was positioned nearer to the end of M1 metallization had a lower tensile stress as compared to that at the left portion of the via bottom, B. In addition, the highest tensile stress was found to concentrate around the bottom portion of the gouging hole, B. These findings agree well with the stress simulation results reported by Zhai *et al.* [22]. Comparing the stress simulation results of a gouging via in Fig. 4.14 (b) with that of a non-gouging via in Fig. 4.14 (c), it was found that sufficient via gouging could enhance the SM reliability. Figure 4.14 (b) shows that the

highest tensile stress region was shifted down into the underlying metal lead, away from the Cu cap/via interface, which is considered to be one of the dominant nucleation sites since it has the weakest interfacial adhesion in the interconnect system. In this work, the tensile stress around the Cu cap/via interface between the gouging and non-gouging vias were extracted to be 240 MPa and 278 MPa, respectively. The reduction in the tensile stress was estimated to be 38 MP; i.e. approximately 14%. Hence, the driving force for void nucleation was reduced.

Despite the reduction in the driving force for void nucleation, Figs. 4.12 (a) to (c) show that the stress-induced void was found to nucleate at the Cu cap/via interface around the top perimeter of the gouging hole, C, where the tensile stress was one of the highest. Such observation is attributed to poorer diffusion barrier layer coverage at the via bottom sidewall, especially at the edge of the wafer, that was due to the nature of the PVD process. More importantly, the triple point where Cu, Cu cap and barrier layers meet has the weakest interfacial adhesion. As such, it is not surprising to find that the stress-induced void first nucleate along the interface near location C [33] as the tensile stress needed to overcome the energy barrier for the void nucleation has been significantly lowered thus favoring the formation of void. Due to this understanding, the focus is placed on the Cu cap/via interface for all subsequent stress simulations presented.

Fig. 4.14: 3D FEA hydrostatic stress modeling beneath via.

- (a) Schematic of a wide M1 metallization near a gouging via. Hydrostatic stress distribution in the wide M1 metallization around the gouging hole with depth of (b) 400 Å and (c) 62 Å during a SM test. The unit of stress distribution is in MPa.

4.2.4 Proposed Stress-induced Voiding Mechanism

Fig. 4.15: Flow chart illustrating the proposed failure mechanism of stress-induced voiding that caused an open circuit beneath the via seen in Fig. 4.13.

In this work, the Cu metallization leads of interest were annealed at an elevated temperature prior to a Cu CMP such that excess vacancies generated through the elimination of grain boundaries during grain growth were annihilated through the free surface of the Cu metallization. As shown in Figs. 4.10 to 4.13, it was observed that even with reduced vacancies in the annealed wide M1 metallization, stress-induced void could still be formed beneath the via after the SM test. As previously discussed, poorer diffusion barrier layer coverage at the via bottom sidewall, especially at the edge of the wafer was due to the nature

of the PVD process is believed to be one of the dominant causes for the experimentally observed failures. In addition, the FEA simulation results showed high tensile stress at the Cu cap/via interface around the perimeter of the gouging via. The proposed stress-induced voiding mechanism described above is summarized in Fig. 4.15. The corresponding schematics of the proposed stress-induced failure mechanism are shown in Fig. 4.16.

Fig. 4.16: Schematics illustrating the formation sequence ((a) to (d)) of stress-induced void beneath the via described in Fig. 4.15.

In Fig. 4.16 (a), the poorer diffusion barrier layer coverage at the via bottom sidewall, especially at the edge of the wafer, was due to the nature of the PVD process. As shown in Fig. 4.16 (b), owing to the presence of the intrinsic weakness and coupled with the high tensile stress, void nucleated. Though void nucleation resulted in stress relaxation, the initial FEA simulation result on the void formation indicated that the stress gradient around the via bottom was the dominant driving force for vacancy accumulation as shown in Fig. 4.16 (c).

Figure 4.16 (d) shows that eventually, the void extended significantly away from the via into the wide Cu metal lead. In brief, the presence of the intrinsic weakness coupled with the high tensile stress and the stress gradient around the via bottom are proposed to be the mechanism for the formation of the stress-induced void observed in this work.

4.2.5 Geometrical Dependency

Fig. 4.17: Percentage change in the resistance of Via chain structures I and II after a 1000-hour of SM test at 200°C. As indicated by the dotted circle, the number of stress-induced damaged via chain structures at the edge of the wafer increased when M1 leads were widened (i.e. 4% versus 10% failures). The small negative change in the resistance was due to statistical fluctuation of the experimental data.

As shown in Fig. 4.17, the number of failed via chain structures at the edge of the wafer increased for the wider M1 leads of 2.0 μm as compared to that with 1.4 μm (i.e. Via chain structures II and I, respectively in Fig. 3.3). This finding is attributed to an increase in

the in-plane stress components resulting from greater substrate constraint [22,34] and a larger amount of vacancies available in the wider M1 leads [10,13,14,17,18,22]. Interestingly, the SM reliability showed no significant difference for both Via chain structures I and II at the centre of the wafer where the diffusion barrier layer coverage at the via bottom sidewall was better. This indicates that the geometrical dependency of stress-induced voiding beneath via can possibly be managed by increasing the σ_{crit} for void nucleation with a more robust process. Improvement in the diffusion barrier layer coverage on the via bottom sidewall is one of the examples to provide more margins for the SM reliability of interest. However, it is worth noting that the effect of the metal width on the SM reliability with width larger than 2.0 μm has yet to be verified.

Fig. 4.18: Percentage change in the resistance of Via chain structures I and III after a 1000-hour of SM test at 175°C. Stress-induced voiding beneath via did not degrade when the length of Cu metal leads (i.e. M1) was increased because of the saturation effect of the stress-induced voiding. The small negative change in the resistance was due to statistical fluctuation of the experimental data.

Figure 4.18 shows that the stress-induced voiding beneath via did not degrade when the length of the M1 leads was increased from 70 μm to 140 μm (i.e. Via chain structures I and III respectively in Fig. 3.3). This finding is attributed to the saturation effect of the stress-induced voiding at an effective diffusion length of approximately 10 μm [13,14,17], which was much shorter than the two lengths used in this work.

4.3 Coping Strategies

4.3.1 Re-sputtering Step During PVD Process of Diffusion Barrier Layer

The nature of PVD process gives a lower deposition rate at the edge of the wafer leading to intrinsic weakness that needs lower energy to overcome the barrier for void nucleation, thus favoring the formation of void. Strategies such as process and/or the structural design modification of Cu interconnects proved to be effective in improving the SM reliability. One possible way is to improve the PVD process of the diffusion barrier layer [15,16,18,33]. In this approach, during the PVD process, the diffusion barrier layer was first deposited, followed by a re-sputtering step with the bias power turned on. This re-sputtering step enabled part of the diffusion barrier layer which was deposited earlier to be re-distributed at the bottom sidewall of the via, thus improving the coverage.

Fig. 4.19: As indicated by the arrows, vias showing diffusion barrier layer deposited with:

- (a) Re-sputtering step gave better and thicker diffusion barrier layer coverage on the via bottom sidewall.
- (b) Conventional method showed thinning of the diffusion barrier layer at the via bottom sidewall.

As shown in Figs. 4.19 (a) and (b), the diffusion barrier layer deposited with re-sputtering step gave better and thicker coverage on the bottom sidewall of the via than that deposited by a conventional method; approximately 2 times increase in thickness was observed. Furthermore, re-sputtering thinned the diffusion barrier layer at the via bottom thus leading to a lower via chain resistance. This technique is excellent because besides thickening the diffusion barrier layer at those areas where its coverage is the most critical but yet poorest, the re-sputtered diffusion barrier from the bottom of the via could fill any small voids at the via bottom sidewall [15,21]. Therefore, better and thicker diffusion barrier layer coverage is achieved on the via bottom sidewall.

Fig. 4.20: Results of stress-induced voiding within via after a 1000-hour of SM test at 175°C. Stress-induced voiding within via was improved with the implementation of re-sputtering step during the PVD process of diffusion barrier layer. The points indicated by the dotted circle correspond to the stress-induced damaged structures and the small negative change in the resistance was due to statistical fluctuation of the experimental data.

Figures 4.20 and 4.21 show that stress-induced voiding within and beneath via was improved with the implementation of re-sputtering step during the PVD process of the diffusion barrier layer. A 3D FEA stress simulation model of a via structure with wide bottom metal lead was developed to identify the mechanism responsible for the SM improvement seen in Fig. 4.21. Two diffusion barrier layers, with a thickness difference of about 10Å to 20Å, representing various degrees of coverage at the via bottom sidewall for a conventional and re-sputtering PVD process were studied.

Fig. 4.21: Results of stress-induced voiding beneath via after a 1000-hour of SM test at 200°C. Similar stress-induced voiding improvement was observed beneath via with the implementation of re-sputtering step during the PVD process of diffusion barrier layer. The points indicated by the dotted circle correspond to the stress-induced damaged structures and the small negative change in the resistance was due to statistical fluctuation of the experimental data.

The hydrostatic stress distributions are shown in Figs. 4.22 (a) and (b). The difference in the stress distribution at the Cu cap/via interface around the perimeter of the gouging hole, where stress-induced voids are commonly found, was insignificant. The results suggest that higher σ_{crit} for void nucleation is a more probable mechanism responsible for the better SM reliability in the re-sputtered coverage. The thicker diffusion barrier layer has higher adhesion strength thus void nucleation is not favored. On the other hand, in cases where the adhesion energy is reduced, the tensile stress needed to overcome the energy barrier for void nucleation is lowered hence resulting in a lower σ_{crit} . Also, with a reduced adhesion strength between Cu and diffusion barrier layer, vacancy diffusion through the barrier is enhanced leading to more rapid void growth. This is supported in Ishikawa *et al.*

paper, which the simulation result on the dependency of void growth rate on the adhesion strength of Cu/diffusion barrier layer interface was reported. It clearly shows the void growth rate increases as the adhesion strength of Cu/diffusion barrier layer interface reduces [15].

Fig. 4.22: Hydrostatic stress distribution in a wide M1 metallization around the gouging hole with a (a) thin and (b) thick diffusion barrier layer thickness, with an approximate difference of $10\text{\AA}$ to $20\text{\AA}$, at the via bottom sidewall during a SM test. Insignificant tensile stress difference at the Cu cap/via interface was observed. The unit of stress distribution is in MPa.

In addition, in his study, ionized metal bias sputtering (IMBS) i.e. re-sputtering method is reported to control the step coverage of the diffusion barrier layer and the adhesion strength of various interfaces. The adhesion strength of diffusion barrier layer deposited by long throw sputtering (LTS) i.e. conventional, and IMBS methods to Cu was measured by scratched test method. As shown in Fig. 4.23, the adhesion strength of Cu/diffusion barrier layer interface was reported to increase with increasing wafer bias during the diffusion barrier layer deposition. As shown, about 1.5 times higher adhesion strength in LTS method was observed.

Fig. 4.23: The adhesion strength of Cu/diffusion barrier layer interface. LTS and IMBS mean long-throw-sputtering method and ionized metal bias sputtering method respectively [15].

4.3.2 Redundant Via Structure

Dual-via structures with wide top and wide bottom metal leads (i.e. Via chain structures II and IV in Figs. 3.2 and 3.3 respectively) were used to compare with single-via structure with wide top and bottom metal leads (i.e. Via chain structure I in Figs. 3.2 and 3.3

respectively) to study the effectiveness of redundant via in improving the SM reliability of Cu interconnects. As shown in Fig. 4.23, the stress-induced voiding within via was improved with the dual-via structure. Similar improvement was seen beneath via for the via chain structures with wide bottom metal leads in Fig. 4.24. The following hypothesis was proposed as a possible cause of the improvement. Due to the formation and growth of void within or beneath a via, the local stress around the adjacent via is changed. The tensile stress thus becomes smaller than the critical value needed for the formation and growth of voids, thereby surviving the stress-induced voiding failure. Further studies are performed using via chain structures with the wide bottom metal leads to validate this hypothesis in Chapter 6.

Fig. 4.23: Percentage change in the resistance of Via chain structures I and II (i.e. single-via and dual-via structures with wide top metal leads respectively) after a 1000-hour of SM test at 175°C. Stress-induced voiding in via was improved with the dual-via structure. The points indicated by the dotted circle correspond to the stress-induced damaged structures and the small negative change in resistance was due to statistical fluctuation of the experimental data.

Fig. 4.24: Percentage change in the resistance of Via chain structures I and IV (i.e. single-via and dual-via structures with wide bottom metal leads respectively) after a 1000-hour of SM test at 200°C. Via chain structures with dual-via were proven again to enhance the SM reliability. The points indicated by the dotted circle correspond to the stress-induced damaged structures and the small negative change in the resistance was due to statistical fluctuation of the experimental data.

4.4 Summary

This chapter provides a detailed overview on the phenomenon of stress-induced voiding within via at different metallization layers. It was observed that stress-induced voiding worsened with increasing metallization layers. This finding is important as it leads to the understanding that for any meaningful comparison of SM reliability, the study has to be performed at the same metallization layer. Moreover, it is believed that stress-induced voiding in Cu interconnects would become more challenging with the implementation of more metallization layers in the near future. This urges that the SM problem has to be

addressed even as early as at the design stage so that one could adopt a more relaxed design rules for vias drawn at different increasing metallization layers rather than the conventional design which employs a standard design rule (i.e. 0.2 μm for this work) across vias at all lower layers. Also, stress-induced voiding within via was found to be more pronounced when Cu was integrated with low-k dielectric. This is explained by the σ_{crit} for void nucleation, which is a function of the effective modulus of the surrounding ILD and interface energy. Lower effective modulus and lower fracture toughness to resist interfacial delamination of higher porosity dielectric are the main contributors to the decrease in σ_{crit} . Hence the integration of Cu with low-k dielectric is more challenging.

A detailed study on the phenomenon of stress-induced voiding beneath via was presented. It was found that appropriate control of the via gouging depth could reduce the effect of stress-induced voiding beneath via. In addition, the geometrical dependency of the stress-induced voiding beneath via was studied and discussed. In both types of stress-induced voiding (i.e. within and beneath via), it was observed that the via chain structures at the edge of the wafer were weaker due to the nature of PVD process, which gives a poorer diffusion barrier layer coverage at the via bottom sidewall. Hence, they were more susceptible to stress-induced voiding. Coupled with the high tensile stress around the perimeter of the gouging via, as supported by the FEA simulation results, void nucleation during the SM test could occur. This is expected to be more severe for 300mm wafers.

Several strategies were recommended in this work to improve the SM reliability of Cu interconnects. Re-sputtering step during the PVD process of the diffusion barrier layer to improve its coverage on the via bottom sidewall is one of the examples to provide more

margins for the SM reliability of interest. However, it is worth to take note that its effect on the SM reliability of metal leads with width larger than 2.0 μm and lower k value dielectrics has yet to be verified. Redundant via is another example that was proven to be effective in managing the SM reliability of Cu interconnects. Furthermore, the mechanisms responsible for the improvement in each strategy were proposed and discussed.

CHAPTER 5

DOMINANT FAILURE MECHANISM AND PROCESS OF STRESS- INDUCED VOIDING

5.1 Design of Experiments

5.2 Dominant Failure Mechanism of Stress-induced Voiding

5.3 Process of Stress-induced Voiding

5.4 Summary

5.1 Design of Experiments

As discussed in Chapter 2, for the case of stress-induced voiding beneath via, Ogawa *et al.* reported that it was resulted from the super saturation of vacancies that developed due to grain growth when Cu was not properly annealed prior to being fully constrained. Coupled with the stress gradient developed beneath via, the vacancies were attracted to coalesce into voids [10]. On the other hand, in this work, all the Cu metallization were annealed at an elevated temperature prior to a Cu CMP process such that excess vacancies generated through the elimination of grain boundaries during grain growth were annihilated through the free surface of Cu. However, it was observed that even with reduced vacancies in the annealed wide metal lead, stress-induced void was formed beneath the gouging via after the SM test as shown in Fig. 4.10. Intrinsic weakness resulted from the nature of PVD process,

which gives a poorer diffusion barrier layer coverage at the via bottom sidewall, especially at the edge of the wafer, was proposed to be the dominant cause of the stress-induced failures.

In view of the above, DOEs on the Cu annealing and Cu diffusion barrier layer deposition as shown in Table 5.1 were designed to study and understand the dominant mechanism(s) responsible for stress-induced voiding in Cu interconnects. Processes A and D were designed to receive good Cu anneal and diffusion barrier layer coverage, and no Cu anneal and poor diffusion barrier layer coverage respectively, to further confirm the effect of the vacancies in Cu leads and the diffusion barrier layer coverage on the stress-induced voiding. Processes B and C were designed to determine whether the super saturation of the vacancies or the poor diffusion barrier layer coverage has a greater effect on the stress-induced voiding.

Similar PVD process approaches as discussed in Chapter 4 were used to design the poor and good diffusion barrier layer coverage experiment. The conventional PVD process gives poorer diffusion barrier layer step coverage. As a result, the Cu/diffusion barrier layer interface needs lower energy to overcome the barrier for void nucleation thus favoring the formation of void. On the other hand, the implementation of the re-sputtering step during the PVD process gives better diffusion barrier layer step coverage and adhesion of the Cu/diffusion barrier layer interface at the via bottom sidewall, leading to improved SM reliability.

Process	No Cu anneal	Good Cu anneal	Poor diffusion barrier layer coverage	Good diffusion barrier layer coverage
A	-	X	-	X
B	X	-	-	X
C	-	X	X	-
D	X	-	X	-

Table 5.1 DOEs of the Cu annealing and Cu diffusion barrier layer deposition to study and understand the dominant mechanism(s) responsible for stress-induced voiding in Cu interconnects.

5.2 Dominant Failure Mechanism of Stress-induced Voiding

As shown in Fig. 5.1, after a 1000-hr SM test at 200°C, Process A gave the best SM reliability whereas Process D gave the worst SM reliability. Firstly, this finding supports the understanding that super saturation of vacancies developed from grain growth when Cu was not annealed prior to being fully constrained, has an impact on the SM reliability. Secondly, the SM reliability was also impacted by the intrinsic weakness resulted from the nature of PVD process, which gives a poorer diffusion barrier layer coverage at the via bottom sidewall especially at the edge of the wafer. However, Process B was found to give better SM reliability than Process C. This indicates that the intrinsic weakness at the via bottom

sidewall has more significant impact on the SM reliability as compared to the super saturation of vacancies.

Fig. 5.1: The percentage change in the resistance of a via chain structure with wide bottom metal leads (i.e. Via chain structure I in Fig. 3.3) after a SM test for the four different processes illustrated in Table 5.1. The points indicated by the dotted circle correspond to the stress-induced damaged structures. The percentages of failed via chain structures of Process A to D are 1%, 5%, 10% and 20% respectively.

Physical analysis was performed to better understand the SM reliability results shown in Fig. 5.1. As illustrated in Fig. 5.2, for Process B, due to no Cu annealing, super saturation of vacancies were generated during grain growth when subjected to the subsequent thermal cycles after the deposition of Cu capping layer. As explained in Fig. 2.6, these vacancies accumulated at the grain boundaries to form voids since they were unable to be annihilated through the free surface of Cu. Such voids were randomly distributed and would grow in size at high temperature stressing with increasing time. In such situation, stress-induced damaged

via would result if the via was landed on or near grain boundaries of the voids. The latter would take a longer time to have a significant increase in the via resistance.

Fig. 5.2: Due to no Cu annealing, super saturation of vacancies were developed during grain growth in the subsequent thermal cycles after the deposition of Cu capping layer. These vacancies accumulated at the grain boundaries to form voids as indicated by the dotted circles. A general scenario of constrained grain growth leading to vacancy super saturation was shown earlier in Fig. 2.6.

Figure 5.3 shows a TEM image of a stress-induced damaged via due to a void formed at a Cu grain boundary. According to this mechanism, the stress-induced failure is strongly dependent on the probability of void generation at or near the via landing area. On the other hand, for Process C, intrinsic weakness was formed around the via bottom sidewall due to a poorer diffusion barrier layer coverage, especially at the edge of the wafer, thus stress-induced failure was inevitable. This clearly explains why Process C, which yield a more systematic weakness, had a more significant effect on the SM reliability than Process B,

which led to random voids along the Cu grain boundaries, as shown by the results in Fig. 5.1. As such, the presence of any intrinsic weaknesses around a via was concluded to be the most dominant mechanism in determining the SM reliability of Cu interconnects.

Fig. 5.3: A TEM image showing a stress-induced damaged via due to a void formed at a Cu grain boundary.

5.3 Process of Stress-induced Voiding

Hydrostatic stress is the driving force for void nucleation. However, as illustrated in Chapter 4, when identifying the most probable void nucleation site, besides the hydrostatic stress concentration, inherent weaknesses in the structural designs, materials (including interfacial adhesion) and/or processes used have to be considered. These intrinsic weaknesses would lower the threshold energy barrier, which needs to be overcome for void nucleation. Coupled with high tensile stress, void nucleates at the weak site. Void growth at

high temperature stressing with increasing time is controlled by the diffusional mechanism defined by the interconnect volume, diffusion volume and stress gradient region. The interconnect volume is given by the product of the geometrical length, height, and width of the Cu metallization of interest. The diffusion volume contributes the vacancies that will coalesce to form void during a given SM test and is defined by the diffusion pathways when a sufficient driving force such as stress gradient exists. As shown in this work, even with reduced vacancies in a well-annealed wide metallization, in the presence of any intrinsic weaknesses, the stress-induced void could still be formed after a SM test. This proves that the complete elimination of the vacancies from Cu grain boundaries is difficult and stress gradient is the dominant driving force for vacancy accumulation.

Stress gradient is the driving force of vacancy flux that leads to void growth. It is dependent on geometrical factors that define the interconnect system, material properties of metal, barrier, dielectrics, and local dynamic stress levels developed at the stress temperature. A 3D FEA hydrostatic stress modeling of a M1 metallization with plastic effect included was conducted to study the stress gradient distribution after a void nucleation. Figure 5.4 (a) shows the decreasing stress profiles during void growth [93]. Though void nucleation results in stress relaxation, stress gradient that is still present is the dominant driving force for vacancy accumulation. It is believed that the stress gradient leads to void growth at high temperature stressing with increasing time.

Fig. 5.4: Stress profiles and stress gradient distribution in a M1 metallization after a void nucleation.

- (a) Stress profile decreases with increasing void size [93].
- (b) Stress gradient around the void vicinity. The unit of stress gradient is in MPa/ μm .

As void grows, it results in further stress relaxation and stress gradient reduction. Eventually, when the stress gradient becomes minimal, it could not support further grain boundary diffusion and stress-induced void growth is thus inhibited. A study in the literature has indicated that the rate of the void growth and the size of the void are dependent on the stress temperature [93]. The void will reach its final size more rapidly with increasing stress temperature. This effect is caused by the temperature dependence of the grain boundary diffusion coefficient and the thermal stress. In addition, the final void size will reduce with increasing stress temperature since the thermal stress imparted by the passivation layer is lowered. Figure 5.5 summarizes the process of the stress-induced voiding.

Fig. 5.5: Flow chart illustrating the proposed mechanism of stress-induced voiding and possible mechanism of void saturation.

5.4 Summary

In this work, DOEs on the Cu annealing and Cu diffusion barrier layer deposition were employed to study and understand the dominant mechanism(s) responsible for stress-induced voiding in Cu interconnects. The presence of any intrinsic weaknesses around a via was found to be the dominant mechanism in determining the SM reliability. These intrinsic weaknesses are fatal and could cause SM failures even in the case when Cu metallization is well annealed and the vacancies are minimal. Also, using a 3D FEA simulation model, the process of stress-induced voiding was described and explained. Though void nucleation results in stress relaxation, stress gradient that is still present is the dominant driving force for vacancy accumulation. This leads to void growth at high temperature stressing with increasing time and further stress relaxation, which reduces the stress gradient. Eventually, stress gradient becomes minimal and could not support further grain boundary diffusion. Hence, stress-induced void growth is inhibited.

CHAPTER 6

EFFECT OF REDUNDANT VIA ON STRESS-INDUCED VOIDING

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- 6.1 Electrical Performance and SM Reliability of Single and Dual-via Chain Structures**
 - 6.2 Numerical Models of Redundant Via Roles**
 - 6.2.1 Sharing of Vacancy Accumulation**
 - 6.2.2 Tensile Stress Reduction Effect**
 - 6.3 Physical Analysis of Stress-induced Damaged Dual-via**
 - 6.4 Stress Distribution beneath Redundant Via**
 - 6.5 Metal Lead Width Dependency**
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6.1 Electrical Performance and SM Reliability of Single and Dual-via Chain Structures

As demonstrated in Chapter 4, redundant via in Cu interconnects was proven to be effective in enhancing the SM resistance than those with single via. The main cause of the improvement and the electrical performance of redundant via are reported in this chapter. Figure 6.1 compares the electrical performance of wide bottom Cu interconnects with single and dual-via (i.e. Via chain structures I and IV in Fig. 3.3 respectively). A lower resistance was observed for the dual-via chain structure; approximately a 25% reduction was observed.

This is attributed to the increase in the contact area of the addition of a redundant via. More importantly, as discussed in Section 4.3.2, Fig. 4.23 shows that very small change of less than 1% in the resistance of the dual-via chain structure was observed after a 1000-hour SM test at 200°C. As compared to the single-via chain structure, a remarkable SM improvement was observed. The possible mechanisms responsible for the improvement are discussed in the next sections.

Fig. 6.1: Comparing to Via chain structure I, Via chain structure IV gave a lower resistance (i.e. single-via and dual-via structures with wide bottom metal leads respectively). Approximately, a 25% reduction was observed.

6.2 Numerical Models of Redundant Via Roles

In view of the SM robustness of dual-via Cu interconnects, it is of great interest to study and understand the role of the redundant via during a SM test. Two different mechanisms of stress-induced voiding beneath via with wide metal lead were proposed. One

possible role of the redundant via is that a vacancy collector that shares the vacancy accumulation during a SM test [29]. The other possible role is attributable to the tensile stress reduction effect, which results in the formation and growth of void beneath one of the vias only (i.e., “weaker” via) [13]. To clarify this situation, two numerical models, one based on vacancy collector while the other based on tensile stress reduction, were developed to calculate the percentage change in the resistance of a dual-via chain structure as a function of the void-to-via size ratio and the population of stress-induced damaged via (i.e. the percentage of vias that are affected by stress-induced voiding within a test structure). The developed models were used to compare with the experimental results to determine the likely role of the redundant via during a SM test.

6.2.1 Sharing of Vacancy Accumulation

Figure 6.2 (a) shows the schematic of a dual-via structure with both vias sharing the vacancy accumulation equally during a SM test. As the dual-via chain structure employed in this work contains 25,000 pairs of vias, its resistance is dependent on both the size of the void and the population of vias affected by stress-induced voiding. The corresponding percentage change in the resistance of a dual-via chain structure as a function of the void-to-via size ratio and the population of the stress-induced damaged via (from 5% to 100%) was calculated as shown in Fig. 6.2 (b). It was observed that for a less than 1% change in the resistance of the dual-via chain structure, the void-to-via ratio was about 15% to 50% for a corresponding change of the population of the stress-induced damaged via from 5% to 100% respectively.

In most cases, as shown in Fig. 6.2 (b), the change in the resistance of the dual-via chain structure was more than 1%. Fig. 4.13 shows that the stress-induced void formed beneath via after a 1000-hr SM test at 200°C typically had a void-to-via size ratio significantly greater than 50%. Thus the results shown in Fig. 6.2 (b) did not correlate well with the physical analysis and experimental results shown in Figs. 4.13 and 4.24 respectively.

Fig. 6.2: Role of the redundant via as a vacancy collector.

- (a) Schematic of a dual-via structure with both vias sharing the vacancy accumulation equally.
- (b) The corresponding percentage change in the resistance of a dual-via chain structure as a function of the void-to-via size ratio and the population of the stress-induced damaged via (from 5% to 100%).

6.2.2 Tensile Stress Reduction Effect

Fig. 6.3: Tensile stress reduction effect beneath the vias.

- (a) Schematic of a dual-via structure when tensile stress reduction effect is dominant and void forms only beneath the weaker via (i.e. Via A).
- (b) The corresponding percentage change in the resistance of a dual-via chain structure as a function of the void-to-via size ratio and the population of the stress-induced damaged via (from 5% to 100%).

As shown in Fig. 6.3 (a), assuming the tensile stress reduction effect beneath the vias is dominant, this leads to the formation and growth of stress-induced void beneath the weaker via. As a result, the stress in the vicinity of the adjacent via (i.e. “stronger” via) becomes

lower than the critical stress for void nucleation. Thus the stress-induced voiding beneath the stronger via is suppressed [13].

Similar to the previous case, as the dual-via chain structure employed in this work contains 25,000 pairs of vias, its resistance is dependent on both the size of the void and the population of vias affected by stress-induced voiding. The corresponding percentage change in the resistance of a dual-via chain structure as a function of the void-to-via size ratio and the population of the stress-induced damaged via (from 5% to 100%) was calculated as shown in Fig. 6.3 (b) using the model above. The results show that the change in the resistance of the dual-via chain structure was minimally affected, from approximately 0.02% to 7% even for the worst-case scenario when both void-to-via size ratio and population of the stress-induced damaged via were 100%. Hence, the tensile stress reduction effect beneath the vias was more likely to be the mechanism responsible for the SM improvement observed.

6.3 Failure Analysis of a Stress-induced Damaged Dual-via

Figures 6.4 (a) and (b) show the SEM micrographs of a void-free dual-via structure and a similar dual-via structure with a wide bottom metal lead, prior to and after a SM test respectively. A stress-induced void was found to form beneath Via A only (i.e. inner via) that was further away from the end of the M1 metallization. This physical analysis result was consistently observed for 900 over pairs of vias analyzed, i.e. approximately 5% of the 25,000 pairs of vias in the via chain structure employed in this work. It was observed that despite the formation of the stress-induced void beneath Via A, Fig. 4.24 shows that the

electrical resistance was not significantly affected after a SM test. As such the results shown in Fig. 4.24 reinforce the conclusion drawn from Fig. 6.3 (b).

Fig. 6.4: Failure analysis of a dual-via structure.

- (a) SEM micrograph of a void-free dual-via structure prior to a SM test.
- (b) SEM micrograph of A via after 1000-hr SM test at 200°C. As shown by the dotted lines, the formation of stress-induced void beneath one of the vias was clearly seen.

6.4 Stress Distribution beneath Redundant Via

Fig. 6.5: FEA simulated hydrostatic stress distribution around the gouging holes in a wide M1 metallization during a SM test. The unit of stress is in MPa.

Figure 6.5 shows the FEA simulated hydrostatic stress distribution around the gouging holes in a wide M1 metallization during a SM test. As illustrated in the stress contour plot, Via A consistently suffered a higher hydrostatic stress distribution (i.e. 200 MPa) than that of Via B or the outer via (i.e. 171 MPa) that was closer to the end of the M1 metallization. The difference in the tensile stress at the Cu cap/via interface of the two vias was estimated to be 29 MPa, i.e. approximately 15% lower in tensile stress for Via B as compared to Via A, indicating a larger driving force for void nucleation for Via A. In addition, since Via A was further away from the end of M1 metallization, it encountered a higher effective diffusive volume of vacancies than that of Via B (see Fig. 6.6). This clearly explains why Via A was a much “weaker” via that was more prone to stress-induced voiding. The sacrificial role of Via A led to minimal degradation in the SM reliability.

Fig. 6.6: Via A encountered a higher effective diffusive volume of vacancies than that of Via B because it was further away from the end of the M1 metallization. The dashed and dotted circles indicate the approximate active diffusion volume seen by Via A and B respectively.

6.5 Metal Lead Width Dependency

As discussed in Section 4.2.5, the stress-induced voiding beneath via was found to degrade when the bottom metal lead width was increased. This is attributed to an increase in the in-plane stress components resulting from greater substrate constraint [22,30] and a larger amount of vacancies available in the wide metal lead. Thus the SM robustness of the dual-via chain structure with a wider bottom metal lead was evaluated. Similar to the single via structure, Fig. 6.7 shows the SM reliability of the dual-via structure degraded with a wider M1 metallization. In addition, the failure analysis performed on a stress-induced damaged dual-via as shown in Fig. 6.8 revealed the formation of a stress-induced void beneath both vias.

Fig. 6.7: SM reliability of dual-via structure degraded when the width of underlying metal lead was increased. The points indicated by the dotted circle correspond to the stress-induced damaged structures.

A 3D FEA stress simulation model was developed to explain the SM reliability degradation seen in Fig. 6.7. The hydrostatic stress at the Cu cap/via interface around the perimeter of the gouging via with different M1 metallization widths is shown in Fig. 6.9 (a). As discussed in the previous section, Via A, which was the inner via of the M1 metallization, always suffered a higher hydrostatic stress than that of Via B (i.e. the outer via) that was closer to the end of the M1 metallization.

As shown in Fig. 6.9 (b), the difference in the hydrostatic stress at the Cu cap/via interface of Via A and B increases with increasing M1 metallization width and seems to saturate when the M1 metallization width is greater than 2.5 μm . As such, the weaker via is believed to be distinct and void forms more readily beneath it especially when the M1 metallization width is smaller than 2.5 μm . After the void formation, due to stress reduction effect, the stress in the vicinity of the adjacent via becomes lower than the critical value for

void nucleation and survives the stress-induced voiding. In addition, the hydrostatic stress at the Cu cap/via interface of Via A and B was found to increase with increasing M1 metallization width (see Fig. 6.9 (a)). This is unfavorable for SM reliability because σ_{crit} for void nucleation is independent of metal width. In a situation when the hydrostatic stress at Via A and Via B exceeds the σ_{crit} for void nucleation, void would nucleate beneath both vias leading to an open circuit seen in Fig. 6.8. Hence, more redundant vias are recommended in wider metallization and interconnects with low σ_{crit} for void nucleation so as to achieve a more robust SM reliability.

Fig. 6.8: SEM micrograph of a stress-induced damaged dual-via taken at a high tilted angle. The dotted line indicates the extend of the void growth that caused an open circuit beneath the gouging vias after a 1000-hr SM test at 200°C.

Fig. 6.9: 3D FEA hydrostatic stress modeling beneath dual-via.

- (a) FEA simulated hydrostatic stress at the Cu cap/via interface around the perimeter of gouging vias with different M1 metallization widths during a SM test.
- (b) FEA simulated hydrostatic stress difference at the Cu cap/via interface of Via A and Via B.

6.6 Summary

This chapter analyzes the effect of redundant via on stress-induced voiding in greater details. Redundant via in Cu interconnects was proven to be effective in enhancing the SM reliability than those with single via. Tensile stress reduction effect beneath vias that were designed along the wide metal lead was the dominant mechanism responsible for the improvement. This understanding was supported by physical analysis and FEA simulation results, which always showed higher stress beneath inner via. The higher tensile stress and the higher effective diffusive volume of vacancies, lead to the formation of the stress-induced void beneath the inner via only. In addition, the study of the effect of metallization width on the design of redundant via shows the hydrostatic stress around vias increases with increasing metallization width. Thus, more vias are recommended in wider metallization for more robust SM reliability.

CHAPTER 7

NOVEL DIELECTRIC SLOT IN CU INTERCONNECTS

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- 7.1 Principle and Impact of Dielectric Slot**
 - 7.2 Design and Process Integration Challenges**
 - 7.3 Wide Top and Bottom Cu Interconnects**
 - 7.3.1 Dielectric Slot Fabrication Steps**
 - 7.3.2 Electrical Performance and SM Reliability**
 - 7.3.3 Physical Analysis and Comparison to Redundant Via Interconnects**
 - 7.3.4 Stress Distribution Around Via Without and With Dielectric Slot**
 - 7.3.5 Mechanisms Responsible for SM Reliability Improvement**
 - 7.4 Summary**
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7.1 Principle and Impact of Dielectric Slot

As explained in Chapter 5, hydrostatic stress is the driving force for stress-induced void nucleation, and void growth is dependent on vacancy flux, which is defined by vacancy concentration, diffusional mobility and stress gradient. Hence, hydrostatic stress, vacancy concentration and stress gradient are to be minimized to effectively manage the stress-induced void failure in Cu interconnects. In accordance to these understandings, small dielectric blocks that are commonly used in wide Cu metal leads to prevent dishing during

CMP process are redesigned as another alternative to manage stress-induced voiding in Cu interconnects [35]. Several examples of the dielectric slot designs are proposed in Fig. 7.1 with the aims to reduce the hydrostatic stress and increase its coverage around the via so as to reduce the effective diffusion volume of the vacancies. In addition, the impacts of the dielectric slot designs on the interconnect resistance and the process integration have to be considered. Further discussion is provided in the next section.

Fig. 7.1: Several examples of dielectric slot designs.

- (a) Rectangular slot,
- (b) Semi-circular slot,
- (c) Horseshoe-like slot and
- (d) Combination of a few smaller slots.

7.2 Design and Process Integration Challenges

Fig. 7.2: Impact on interconnects resistance with different dielectric slot dimensions.

- (a) Slot length (L) varied with fixed width of 0.3 μm.
- (b) Slot width (W) varied with fixed length of 1.2 μm. The insert shows the location of a 0.19 μm via in a 2 μm x 10 μm Cu metal lead.

The location and shape of such dielectric slot were found to be very crucial in determining its effectiveness in SM reliability improvement. After several via design optimizations, the dielectric slot was incorporated near via to reduce the hydrostatic stress surrounding it, thus lowering its tendency of void nucleation. In addition, the dielectric slot

must be sufficiently long to effectively impede vacancies coalescence in Cu interconnects for SM reliability improvement.

As shown in Fig. 7.2 (a), the interconnect resistance changes exponentially with the dielectric slot length (L) and its resistance could increase by more than 25% if an inappropriate choice of the slot length is made. Thus, an optimum length has to be chosen to prevent any significant increase in the interconnect resistance and simultaneously, it should still serve as a good vacancies coalescence impedance. Fig. 7.2 (b) shows that an inappropriate choice of the dielectric slot width (W) could also cause a significant increase in the interconnect resistance. For example, a $1\text{ }\mu\text{m}$ wide dielectric slot in a $2\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ Cu metal lead could change the resistance by 15%. As such, narrow dielectric slot is preferred. On the other hand, narrow slot poses difficulty in process integration. During the mask and etch processes, narrow photo-resist tends to topple easily and causes distorted or missing patterns. Hence, a balance between good reliability and electrical performances, and process integration could be achieved through appropriate DOEs and optimization.

7.3 Wide Top and Bottom Cu Interconnects with Dielectric Slot

In this work, horseshoe-like dielectric slot design was chosen because of its good coverage around the via which can effectively impede vacancies coalescence. In addition, its wider base as compared to a simple dielectric slot gives more margins during the mask and etch processes. For example, the narrow photo-resist will not topple easily thus not resulting

in distorted or missing patterns. The dielectric slot fabrication steps for wide top and bottom Cu interconnects are discussed in Sections 7.3.1 and 7.3.2, respectively.

7.3.1 Dielectric Slot Fabrication Steps

Fig. 7.3: Schematics illustrating the processing steps for the fabrication of dielectric slot in wide top Cu metal lead. (a)-(c) are the critical steps for the fabrication of horseshoe-like dielectric slot in M2.

The horseshoe-like slot in wide top and wide bottom metal leads (i.e. Via chain structures I and II in Fig. 3.4 respectively) are fabricated using a 0.13 μm Cu metallization

technology on 300 mm wafer. The main steps of the process flow are shown in Figs. 7.3 and 7.4, respectively.

Fig. 7.4: Schematics illustrating the processing steps for the fabrication of dielectric slot in wide bottom Cu metal lead. (a)-(c) are the critical steps for the fabrication of horseshoe-like dielectric slot in M1.

Figure 7.3 (a) shows that M2 and a horseshoe-like dielectric slot were masked together during the lithography process. The horseshoe-like dielectric slot was patterned within the wide M2 during the etch process shown in Fig. 7.3 (b). As shown in Fig. 7.3 (c), a Si_3N_4 breakthrough was performed at the via bottom after a photo-resist (PR) strip process. After which, a two-level via-metal lead structure with a horseshoe-like dielectric slot in the

wide M2 metallization was formed as shown in Fig. 7.3 (d) using the conventional Cu process.

In Fig. 7.4 (a), M1 and a horseshoe-like dielectric slot were masked together after the inter-layer dielectric (ILD) CVD process. Figure 7.4 (b) shows that during the etch process, the horseshoe-like dielectric slot was patterned within the wide M1. During the Cu process, Cu was ECP on a seed layer and was annealed at an elevated temperature. The Cu surface was passivated with a layer of Si_3N_4 after the redundant Cu was removed by a CMP process. Thereafter, a wide M1 with a horseshoe-like dielectric slot was formed as shown in Fig. 7.4 (c). Using the via-first dual-damascene patterning process (see Fig. 7.3 (d)), a two-level via-metal lead structure was developed (see Fig. 7.4 (e)).

Fig. 7.5: (a) Layout and (b) SEM micrograph of wide top Cu interconnects with a horseshoe shaped dielectric slot.

Figures 7.5 and 7.6 show a few examples of the designs and the corresponding physical structures of the horseshoe-like slots in the wide top and wide bottom metal leads,

respectively. Excellent results were obtained in the first attempt and novel dielectric slot was successfully fabricated in Cu interconnects without additional masking steps.

Fig. 7.6: (a) Layout and (b) SEM micrograph of wide bottom Cu interconnects with a horseshoe shaped dielectric slot.

7.3.2 Electrical Performance and SM Reliability

Fig. 7.7: Dielectric slot in wide top Cu metal lead gave rise to minimal effect on its resistance. Roughly a 1.5% increment was observed before a SM test.

Figure 7.7 compares the electrical performance of a wide top Cu interconnects with and without dielectric slot. It was observed that the impact of the dielectric slot on the Cu interconnect resistance was minimal; approximately a 1.5% increment was observed. More importantly, as shown in Fig. 7.8, after a 1000-hour SM test at 200°C, the SM reliability of the wide top Cu interconnects with the dielectric slot was more superior to that without the dielectric slot.

Fig. 7.8: SM reliability improved drastically for wide top Cu interconnects with dielectric slot. The points indicated by the dotted circle correspond to the stress-induced damaged structures.

The electrical performance of the wide bottom Cu interconnects with and without dielectric slot is shown in Fig. 7.9. Similar to the previous case, the impact of the dielectric slot on the Cu interconnect resistance was minimal; approximately a 1.7% increment was observed. As illustrated in Fig. 7.10, a robust SM reliability was observed after a 1000-hour test at 200°C.

Fig. 7.9: Similar resistance trend had been observed in wide bottom Cu metal lead. Dielectric slot gave rise to minimal effect on its resistance. Roughly a 1.7% increment was observed before a SM test.

Fig. 7.10: Improved SM robustness of wide bottom Cu interconnects with dielectric slot was seen. The points indicated by the dotted circle correspond to the stress-induced damaged structures.

7.3.3 Physical Analysis and Comparison to Redundant Via Interconnects

Fig. 7.11: Wide top Cu interconnects with dielectric slot showed a similar SM robustness as compared to those with dual-via structures.

Fig. 7.12: Physical analysis of SM tested via without and with dielectric slot in the wide top Cu metal lead.

- (a) Stress-induced void was formed within via when dielectric slot was absent.
- (b) No stress-induced void was found when dielectric slot was incorporated.

As illustrated in Fig. 7.11, the SM reliability of the interconnects with the dielectric slot in a wide M2 lead and dual-via interconnects, known to improve SM robustness [13,18,29], was comparable. The transmission electron microscopy micrographs shown in Fig. 7.12 clearly demonstrated the formation of stress-induced void within a via when there was no dielectric slot in the wide top Cu metal lead, whereas no void was observed when the dielectric slot was incorporated. This physical analysis result was consistently observed for a few hundred of vias analyzed.

Fig. 7.13: Similar SM robustness was demonstrated for wide bottom Cu interconnects with dielectric slot as compared to that with dual-via structures.

As shown in Fig. 7.13, a comparable SM reliability was seen between the dielectric slot in a wide M1 lead and dual-via interconnects after a 1000-hour test at 200°C. This observation was further supported by a physical analysis performed on the stressed via chain structures. Fig. 7.14 (a) shows that in the absence of the dielectric slot, the stress-induced void was formed beneath a failing via and had extended significantly into the wide bottom Cu metal lead. On the other hand, as shown in Fig. 7.14 (b), when dielectric slot was

incorporated, no stress-induced void was formed beneath via. Similar to the previous case, this physical analysis result was consistently observed for a few hundred of vias analyzed.

Fig. 7.14: Physical analysis of SM tested via without and with dielectric slot in the wide bottom Cu metal lead.

- (a) Example of stress-induced void beneath via indicated by the dotted line for the case of an absence of dielectric slot.
- (b) No stress-induced void was found when dielectric slot was incorporated. This conclusion was derived after inspecting all the vias in the via chains.

7.3.4 Stress Distribution Around Via Without and With Dielectric Slot

In this stress simulation, the focus was placed on the via around the Cu cap layer where stress-induced void was commonly found to nucleate. As shown in Fig. 7.15, in the case where a dielectric slot in a wide M2 metallization was employed, the FEA simulated hydrostatic stress in the via (i.e. 254 MPa) was lowered as compared to that without a

dielectric slot (i.e. 287 MPa). The reduction in the tensile stress was estimated to be 33 MPa, i.e. approximately 12% lower for the case with dielectric slot as compared to that without dielectric slot. Thus the driving force for void nucleation was correspondingly reduced.

Fig. 7.15: Hydrostatic stress distribution in the via (a) without and (b) with dielectric slot in a wide M2 metallization during a SM test. Via without dielectric slot consistently suffered a higher hydrostatic stress than via with dielectric slot. This was particularly so in the via around the Cu cap layer as shown in (a). The unit of stress distribution is in MPa. The insert in (b) shows the schematic of a wide M2 metallization with a dielectric slot.

Fig. 7.16: Hydrostatic stress distribution in a wide M1 metallization around the gouging hole (a) without and (b) with dielectric slot during a SM test. Via without dielectric slot consistently suffered a higher hydrostatic stress at the Cu cap/via interface than via with dielectric slot. The unit of stress distribution is in MPa. The insert in (b) shows the schematic of a wide M1 metallization with a gouging hole and dielectric slot.

In the case where a dielectric slot in a wide M1 metallization was employed, the FEA simulated hydrostatic stress around the gouging hole shown in Fig. 7.16 confirms that the via suffered a lower hydrostatic stress at the Cu cap/via interface (i.e. 211 MPa) as compared to that without a dielectric slot (i.e. 238 MPa). The reduction in the tensile stress was estimated

to be 27 MPa, i.e. approximately 12% lower for the case with dielectric slot as compared to that without dielectric slot. Again, the driving force for void nucleation was reduced.

7.3.5 Mechanisms Responsible for SM Reliability Improvement

Based on the understandings gained from the TEM and SEM images, and stress simulation results, the flow chart shown in Fig. 7.17 was developed to explain the mechanisms that resulted in the improved SM reliability observed.

Fig. 7.17: Flow chart illustrating the mechanisms that resulted in improved SM reliability due to dielectric slot in Cu interconnects.

Fig. 7.18: Mechanisms responsible for the improved SM reliability. (a) and (b) are the plan-views of a wide metal lead, M1 or M2, without and with dielectric slot respectively. The dotted circles show a reduction in the effective diffusive volume of vacancies by the dielectric slot. (c) and (d) are the cross-sectional views of a wide M2 lead without and with dielectric slot respectively. This shows an additional mechanism for the wide top Cu interconnects - a reduction in the Cu volume contraction during the cooling phase of the SM test. Thus tendency of via pull out was reduced as shown in (d).

The corresponding schematics of the mechanisms responsible for the SM reliability improvement are emphasized in Fig. 7.18. The hydrostatic stress responsible for stress-induced failures was reduced due to the dielectric slot designed near the via (see Figs. 7.15 and 7.16), hence lowering the driving force for void nucleation. In addition, as explained in Figs. 7.18 (a) and (b), void growth was inhibited due to a reduction in the effective diffusive volume of the vacancies by the dielectric slot. Figures 7.18 (c) and (d) show an additional mechanism for the wide top Cu interconnects. In this case, there is a reduction in the Cu

volume contraction during the cooling phase of the SM test, leading to a reduced tendency of via pull out as shown in Fig. 7.18 (d).

7.4 Summary

In this work, novel dielectric slot was proposed and successfully fabricated in Cu interconnects without additional masking steps. It has been proven that a well-designed dielectric slot would have minimal impact on the interconnects resistance and is effective in managing stress-induced void failure in Cu interconnects. The corresponding mechanisms responsible for the SM improvement were identified using a 3D FEA stress simulation model. Also, the proposed dielectric slot is strongly recommended for future technology in which the reliability of Cu interconnects is of great concern, especially those employing porous ultra low-k dielectric. Its extendibility is further discussed in the next chapter.

CHAPTER 8

FUTURE CHALLENGES AND THE EXTENDIBILITY OF DESIGN FOR MANUFACTURABILITY

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- 8.1 Future Challenges**
 - 8.2 Extendibility of Design for Manufacturability**
 - 8.2.1 Void Nucleation**
 - 8.2.2 Via Deformation**
 - 8.3 Summary**
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8.1 Future Challenges

As technology advances, lower k value dielectrics need to be integrated with Cu interconnects for faster devices. Previous studies have shown that dielectric materials with k value lower than 2.7 are only achievable with the introduction of pores [94]. Moreover as the biaxial modulus of higher porosity dielectric film decreases, the intrinsic stress decreases correspondingly thus it is expected that the SM reliability of Cu interconnects would improve [86,92]. However, as discussed in Section 4.1.6, dielectrics with higher porosity have lower effective modulus and lower fracture toughness to resist interfacial delamination in the damascene structure, hence yield lower σ_{crit} value for void nucleation and degrade the SM reliability of Cu interconnects. This finding is supported by several studies in the literature

[18,22,91]. Christine S. Hau-Riege *et al.* reported that the σ_{crit} for void nucleation in Cu/FTEOS is higher than in Cu/Low-k by a factor of 4 times [91]. In addition, Zhai *et al.* proposed a SM risk index by considering both stress state and σ_{crit} for void nucleation of a given Cu/ILD interconnect system to determine the probability of stress induced voiding from the stress perspective. As shown in Fig. 8.1, the SM risk index of Cu/Low-k was reported to be approximately 3 times higher than that of Cu/FTEOS [22].

Fig. 8.1: Hydrostatic stress, σ_{crit} for void nucleation and SM risk index of Cu/FTEOS and Cu/Low-k interconnects [22].

In addition to the void nucleation at hydrostatic stress concentrated region and the subsequent void growth, another failure mode in Cu/Low-k interconnects was reported by Paik *et al.* [30,31]. Due to the smaller dimension of a via, its mechanical restriction by the substrate is lesser than that of a metal lead which have a larger dimension. Therefore, the thermo-mechanical properties of a via is dominated by the mechanical properties of the

dielectric materials. Low elastic modulus and substantially high thermal expansion coefficient of the low-k dielectrics lead to high compressive stress in the via. Also, the von Mises stress in the via of Cu/Low-k interconnects was reported to be much higher than that of Cu/FTEOS interconnects. These findings were supported by physical failure analysis showed in Fig. 8.2. The via was deformed with its lower segment rose up with respect to the slip plane. Such phenomenon will be worsened in the case of porous ultra low-k dielectrics, resulting in a more challenging reliability issue for future nanoscale technologies.

Fig. 8.2: Another failure mode in Cu/Low-k interconnects where the via was deformed with its lower segment rose up with respect to the slip plane. This indicates that the deformation is due to the compressive stress in the via [30,31].

8.2 Extendibility of Design for Manufacturability

Owing to a more challenging SM reliability in low-k Cu interconnects, additional efforts are needed in process improvement to manage stress-induced voiding. Also, design for manufacturability (DFM), such as redundant via and dielectric slot, which were demonstrated in Chapters 6 and 7 to be an effective solution for the SM reliability enhancement of Cu interconnects, are strongly recommended. In the subsequent subsections, 3D FEA simulation models were employed to analyze the extendibility and impact of DFM to future nanoscale technologies in which the backend reliability is particularly important due to its integration with porous ultra low-k dielectrics.

8.2.1 Void Nucleation

A study reported in the literature is used to assess the possible cause of void initiation discussed in this work. In Alers *et al.* paper, a correlation between the yield property of Cu and stress migration performance is reported [11]. A 0.1 μm thick layer of Cu was found to have a yield stress of approximately 920 MPa and an elastic energy release rate of 10 mJ/m^2 but a plastic energy release rate of smaller than 0.1 mJ/m^2 for a 30 nm crack initiation. In contrast, a 0.5 μm thick layer of copper with a yield stress of 410 MPa was found to have an elastic energy release rate of smaller than 0.1 mJ/m^2 but a plastic energy release rate of 7 mJ/m^2 for a similar size crack initiation. The FEA calculations show that an increase in the thickness and/or a decrease in the yield stress of Cu allow strain energy to be dissipated in the

Cu without forming a crack. On the other hand, if the yield stress of Cu is high, then the stress energy in the Cu will go into the formation of a crack at the Cu cap/via interface. Once the crack is initiated, it can grow into a void through vacancy diffusion. In addition, a strong dependence of stress migration performance on metal/dielectric adhesion is reported. If the local adhesion energy between the Cu and the diffusion barrier layer and the dielectric are lower at some locations than the yield stress of Cu, voids can nucleate due to poor adhesion.

The thicknesses of the metal leads used in this work are in the range of 0.25 to 0.37 μm , which the strain energy can be dissipated in the Cu without forming a crack. Also, the stress migration results reported demonstrate a strong dependence of stress migration performance on the diffusion barrier layer process. This is consistent with the critical dependence of metal/dielectric adhesion on the stress migration performance. Therefore, the initiation of voids reported in this work is attributed to adhesion failure at the Cu cap/via interface.

With a better understanding on the cause of void initiation, 3D FEA stress simulation models of 2-level Cu interconnects with a redundant via and a dielectric slot, similar to those illustrated in Figs. 6.5 and 7.16 (b) respectively, were developed to study the extendibility of DFM in enhancing the SM reliability of porous ultra low-k Cu interconnects. The difference in hydrostatic stress at the Cu cap/via interface between Via A and B (i.e. the via which is further away from and closer to the end of M1 metallization respectively, of a redundant via structure) and between the conventional and slot designs with different surrounding dielectrics are shown in Figs. 8.3 and 8.4, respectively.

Fig. 8.3: Difference in hydrostatic stress at the Cu cap/via interface between Via A and B increases with increasing dielectric porosity.

In Fig. 8.3, the difference in the hydrostatic stress at the Cu cap/via interface of Via A and B was found to increase with increasing dielectric porosity and was most significant, approximately 40 MPa, for the porous ultra low-k Cu interconnects. As the difference in the hydrostatic stress between the vias increases, the “weaker” via is believed to be distinct and void forms more readily beneath it resulting in stress reduction effect at the adjacent via which suppresses the stress-induced voiding. In addition, the hydrostatic stress around the vias was found to decrease with increasing dielectric porosity. However, a more significant reduction in σ_{crit} for void nucleation due to lower fracture toughness to resist interfacial delamination in the damascene structure was reported in several studies [18,22,33]. In a situation when the σ_{crit} for void nucleation is lower than the hydrostatic stress of Via A and B, more redundant vias are recommended so as to effectively manage the stress-induced voiding.

Fig. 8.4: Difference in hydrostatic stress at the Cu cap/via interface between conventional and slot design increases with increasing dielectric porosity (i.e. lower k value).

Similar to the previous study, Fig. 8.4 shows that the difference in the hydrostatic stress at the Cu cap/via interface between the conventional and slot design was found to be most significant, approximately 40 MPa, for the porous ultra low-k Cu interconnects. This indicates that the dielectric slot plays a more distinct role in enhancing the SM reliability of Cu interconnects employing the porous ultra low-k dielectrics. These learning are important because they show that DFM, which is commonly used for process optimization with designs, can be employed to study the probability of the stress-induced voiding failure in future nanoscale technologies employing the porous ultra low-k dielectrics.

8.2.2 Via Deformation

Fig. 8.5: Hydrostatic stress from the top of M2 metallization to the bottom of the via during a SM test. Via without dielectric slot suffered a higher compressive stress than via with dielectric slot.

Fig. 8.6: Von Mises stress from the top of M2 metallization to the bottom of the via during a SM test. Similar stress trend shown in Fig. 8.5 was observed. Again, via without dielectric slot suffered a higher von Mises stress than via with dielectric slot.

In this study, the focus was placed on the via where high compressive stress was found to concentrate. Stresses in the via, i.e. a distance between 0.4 to 0.8 μm from the top of the M2 metallization, were used to study the effectiveness of the different designs in reducing the compressive and von Mises stresses. As illustrated in Figs. 8.5 and 8.6, when a dielectric slot was incorporated into the M2 metallization, the FEA simulated compressive and von Mises stresses in the via were correspondingly lowered. Approximately 30 MPa and 60 MPa reductions were observed, respectively. However, as the compressive and von Mises stresses in the via were still high, the stress reductions may not be effective in preventing via deformation.

In addition to the incorporation of a dielectric slot, the effectiveness of short via in preventing via deformation was studied. As shown in Fig. 8.8, though the reduction in the von Mises stress in the via was larger than the previous case, i.e. greater than 100 MPa, but the compressive (see Fig. 8.7) and von Mises stresses in the via were still high. Hence, the von Mises stress reduction may not play a significant role in preventing via deformation. Though both cases do not show promising stress reduction results, the latter is recommended because with a smaller Cu volume, the occurrence of twins in the via would be reduced correspondingly. It is believed that with the reduction of the slip planes in Cu, it may help to better manage via deformation.

Fig. 8.7: Hydrostatic stress from the top of M2 metallization to the bottom of the via during a SM test. Both conventional and shorter vias will suffer similar compressive stress.

Fig. 8.8: Von Mises stress from the top of M2 metallization to the bottom of the via during a SM test. Conventional via will suffer higher von Mises stress than shorter via.

8.3 Summary

Fig. 8.9: Early implementation of simulation model for reliability physics study and the subsequent DFM would be important considerations for device reliability community to study sub-45nm CMOS devices.

As illustrated in this work, DFM can be developed to make robust Cu interconnects more resilient to SM degradation in future nanoscale technologies where the SM reliability is highly challenging due to the introduction of porous ultra low-k dielectrics. However, in order to make DFM more useful and applicable, a thorough understanding of the dominant failure mechanisms affecting SM is necessary. 3D FEA stress simulation is one approach to provide an in-depth understanding of various stress-induced failures seen in today's state-of-the-art CMOS technologies since it is no longer cost effective to study stress-induced failures through the standard DOE approach. This implies that early implementation of simulation model for reliability physics study and the subsequent DFM shown in the flow chart in Fig.

8.9 are important considerations for device reliability community to study sub-45nm CMOS devices.

CHAPTER 9

CONCLUSION AND RECOMMENDATIONS

9.1 Conclusion

9.2 Recommendations

9.1 Conclusion

The phenomena of stress-induced voiding in Cu interconnects are studied in greater details in this work. Several physical analysis methods were explored and a 3D FEA stress simulation model was developed to achieve an in-depth understanding on the mechanisms that are responsible for the formation of stress-induced void within and beneath via during a SM test. A clear description and explanation on the process of the stress-induced voiding was provided. Furthermore, the study shows that the geometries and structural designs of Cu interconnects would continue to have substantial impact on the stress-induced voiding. As via dimension shrinks, it means that a corresponding smaller void size is needed to cause stress-induced failure, hence posing more challenges for the SM reliability. It is also discussed that inherent weaknesses in the materials (including interfacial adhesion) and processes are found to be inevitable and would continue to drive the need for improvement in metallization and processes for better management of the stress-induced voiding. This is especially the case for future nanoscale technologies employing porous ultra low-k dielectrics since lower effective modulus and lower fracture toughness to resist interfacial delamination

of the higher porosity dielectrics are the main contributors to increasing stress-induced failures.

9.2 Recommendations

As discussed in Section 2.7, SM is an intrinsic failure that causes an open circuit in metal interconnects. They are typically caused by wear out and is managed rather than eliminated, such as ensuring that the wear out occurs beyond the useful life of a product. As technology advances, the pursuit for high-end devices has prompted a flurry of activities in the design and process communities. New insulators that have lower k value are employed to integrate with Cu. These low- k dielectrics have low hardness and modulus, poor adhesion with other films and low thermal conductivity, leading to cracking, delamination, and reliability failures, thus posing significant challenges to process integration and reliability.

Owing to a more challenging reliability in low- k Cu interconnects, additional efforts are needed in process improvement to manage stress-induced voiding. As demonstrated in this work, diffusion barrier layer deposited with re-sputtering step is one possible way to improve the SM reliability. Other promising alternatives such as hybrid ILD, Cu surface cladding, alloying, etc. are reported and recommended in the literature for effective SM reliability enhancement.

Early implementation of simulation model for physics and mechanical studies and the subsequent DFM (i.e. structural improvement) such as redundant via(s), dielectric slot(s) and

short via are also recommended for an effective management of stress-induced voiding. Owing to more complex structures and advanced materials such as porous ultra low-k dielectrics being used for future nanoscale technologies and the need for faster and successful semiconductor product introduction, it is no longer cost effective to study reliability failures through the standard DOE approach. 3D FEA simulation is one of the approaches to provide in-depth understanding of various SM failures seen in today's state-of-the-art CMOS technologies. In this work, the application of the 3D FEA simulation has proven to provide the required insight for effective implementation of DFM to achieve robust SM reliability. This implies that in future nanoscale technologies, a closer interaction among designers, process and reliability engineers is required to ensure that the SM reliability of Cu interconnects is not significantly degraded while other important parameters such as the resistance of the Cu interconnects and on-chip device packaging density are not severely compromised.

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