Development of statistical model for baseband MOSFETs

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DEVELOPMENT OF STATISTICAL MODEL FOR BASEBAND MOSFETS

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TABLE OF CONTENT

ACKNOWLEDGEMENTS	i
TABLE OF CONTENT	ii
LIST OF FIGURES	iii
LIST OF TABLES	viii
LIST OF SYMBOLS & ABBREVIATIONS	x
ABSTRACT	xiii
CHAPTER 1	1
INTRODUCTION.....	1
1.1 Motivation	1
1.2 Objectives	5
1.3 Organization of the Thesis	8
CHAPTER 2	10
BACKGROUND & LITERATURE REVIEW	10
2.1 Process Variation in IC Manufacturing	10
2.2 Circuit Simulation and Compact Models	13
2.3 Statistical MOSFET Modelling	17
CHAPTER 3	27
STATISTICAL MOSFET MODELING FOR GLOBAL PROCESS VARIATION USING BPV METHODOLOGY	27
3.1 0.35 μ m CMOS Technology	27
3.2 MOSFET Characterization For Global Process Variation.....	29
3.3 Statistical MOSFET Model For Global Variation.....	30
CHAPTER 4	45
MOSFET MISMATCH TEST STRUCTURE.....	45
4.1 IC Test Structures	45
4.2 MOSFET Mismatch Test Structure Design	47
4.2.1 MOSFET mismatch test structure considerations.....	47
4.2.2 MOSFET matched pair test structure design.....	53
4.2.3 MOSFET Mismatch Characterization	58
4.3 Factors Affecting MOSFET Mismatch.....	60
CHAPTER 5	72
MOSFET MISMATCH MODELING USING BPV METHODOLOGY	72
5.1 Developments of MOSFET Mismatch Modelling.....	72
5.2 MOSFET Mismatch Characterization	74
5.2.1 CSM 0.13 μ m process technology.....	74
5.2.2 MOSFET mismatch test structure and measurement setup	77
5.2.3 Statistical MOSFET mismatch data extraction.....	81
5.3 Modelling MOSFET Mismatch Using BPV methodology.....	83
5.3.1 Electrical characteristics targets for BPV	83
5.3.2 MOSFET Mismatch BPV model parameter sensitivity matrix.....	85
5.3.3 Acquiring BSIM3v3 parameter variances using BPV	94
CHAPTER 6	115
CONCLUSIONS & FUTURE WORKS	115
6.1 Conclusions	115
6.2 Future Works.....	117
AUTHOR'S PUBLICATIONS	120
REFERENCES.....	122

LIST OF FIGURES

Figure 2.1: Two groups of process variation: inter-die and intra-die variability [3].	11
Figure 2.2: Probability density distribution of device parameter as result of intra-die and inter-die process variation [19].	12
Figure 2.3: A schematic for a circuit to be simulated using SPICE, the nodes are labelled Vin, n1, n2, Vdd, GND and Vut.	14
Figure 2.4: Process variation map for Idsat of n-MOSFET and p-MOSFET [3].	19
Figure 3.1: Different types of process control module (PCM).	29
Figure 3.2: Monte Carlo simulation of Idsat for n-MOSFET and p-MOSFET showing simulated data mc1, mc2 and mc3 at 1, 2 and 3 sigma of global process variation respectively.	36
Figure 3.3: Verification plot for Idsat of thin gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=0.35 μ m.	39
Figure 3.4: Verification plot for Vtsat of thin gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=0.35 μ m.	39
Figure 3.5: Verification plot for Idsat of thin gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=20 μ m.	40
Figure 3.6: Verification plot for Vtsat of thin gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=20 μ m.	40
Figure 3.7: Verification plot for Idsat of thin gate n-/p-MOSFET with MOSFET channel width=4 μ m and length=20 μ m.	41
Figure 3.8: Verification plot for Vtsat of thin gate n-/p-MOSFET with MOSFET channel width=4 μ m and length=20 μ m.	41
Figure 3.9: Verification plot for Idsat of thick gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=0.50 μ m.	43
Figure 3.10: Verification plot for Vtsat of thick gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=0.50 μ m.	43
Figure 3.11: Verification plot for Idsat of thick gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=20 μ m.	44
Figure 3.12: Verification plot for Vtsat of thick gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=20 μ m.	44
Figure 4.1: PCM and PEM test structures [34].	46
Figure 4.2: Different possible mismatch test structure designs. (a) Array design. (b) & (c) Simple matched pair design using 2xN and 1xM pad module respectively.	47
Figure 4.3: CS&CG configuration for MOSFET matched pair test structure [34].	49
Figure 4.4: Recommend MOSFET mismatch test structure with common source (CS) and individual gate and drain pads for each MOSFET, especially for advanced technology with thinner gate oxide [34].	50
Figure 4.5: Poor contact between probe card and module's pads [34].	50
Figure 4.6: Conditions of probe pad under repeat or multiple characterisations [34].	51
Figure 4.7: Details of the MOSFET mismatch test structures for the CSM 0.18 μ m and 0.13 μ m technologies. (a) Pad Assignments. (b) Probe pad dimensions. (c) Module layout for 10 similar MOSFET pairs. (d) MOSFET matched pair layout design (zoom-in of c.).	53

Figure 4.8: Keys details of the MOSFET mismatch test structure for CSM 90nm LP technology. (a) Pad Assignments. (b) Probe Pad Dimensions. (c) MOSFET mismatch test structure layout design using 1x25 pad module containing four matched pairs. (d) Standard MOSFET pair layout design (zoom-in of c.).....	56
Figure 4.9: Pelgrom plot to study impact of BEOL on V_{tlin} mismatch for n and p-MOSFET.....	61
Figure 4.10: Layout design of 0.13 μ m MOSFET pair that is used to study the effect of non-interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch. Total channel width: 10.4 μ m. No. of fingers: 8.	64
Figure 4.11: Layout design of 0.13 μ m MOSFET pair that is used to study the effect of interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch. Total channel width: 10.4 μ m. No. of fingers: 8.....	64
Figure 4.12: Layout design of 90nm (LP) MOSFET pair that is used to study the effect of non-interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch. Total channel width: 7.2 μ m. No. of fingers: 2.	65
Figure 4.13: Layout design of 90nm (LP) MOSFET matched pair that is used to study the effect of interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch. Total channel width: 7.2 μ m. No. of fingers: 2.	65
Figure 4.14: $\sigma_{\Delta V_{tlin}}$ vs. no. of fingers, for both n- and p-MOSFETs using 0.13- μ m technology to study the impact of multi-fingered layout on MOSFET threshold voltage mismatch characterisation. The length and width of finger size is indicated below the data point as L/W (μ m / μ m).....	66
Figure 4.15: $\text{abs}(\mu_{V_{tlin}})$ vs. no. of fingers, for both n- and p-MOSFETs using 0.13- μ m technology to study the impact of multi-fingered layout on MOSFET threshold voltage mismatch characterisation. The length and width of finger size is indicated below the data point as L/W (μ m / μ m).....	66
Figure 4.16: $\sigma_{\Delta nV_{tlin}}$ & $\mu_{nV_{tlin}}$ vs. No. of fingers for n-MOSFETs using 90-nm technology to study the impact of multi-fingered layout on MOSFET threshold voltage mismatch characterisation. The length and width of finger size is indicated below the data point as L/W (μ m/ μ m).....	68
Figure 4.17: Layout design of MOSFET pair that is used to study the impact of gate protection diode on intrinsic MOSFET mismatch.	69
Figure 4.18: Pelgrom plot of n-MOSFETs V_{tlin} using 90-nm technology. This is to study the impact of gate protection diode on MOSFET threshold voltage mismatch. Filled symbols represent data ‘without GDP’ while unfilled symbols represent data ‘with GDP’. Length (L) and width (W) in the legend are in μ m.....	70
Figure 5.1: Different MOSFET variants offer by CSM 0.13 μ m process technology.	74
Figure 5.2: Schematic of the semi-auto measurement setup.....	77
Figure 5.3: CASCADE Microchamber 8” probe station.	78
Figure 5.4: Probe card interfaced with the probe station.	79
Figure 5.5: Agilent B2201A switching matrix	80
Figure 5.6: HP 4156B Semiconductor parametric analyzer	80
Figure 5.7: Pelgrom plot for comparing $\sigma_{\Delta nI_{doff}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.	98
Figure 5.8: Pelgrom plot for comparing $\sigma_{\Delta nI_{dweak}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.	98

Figure 5.9: Pelgrom plot for comparing $\sigma_{\Delta n_{Idmod}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement for 4 corner n-MOSFET sizes.	99
Figure 5.10: Pelgrom plot for comparing $\sigma_{\Delta n_{Idstr}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.	99
Figure 5.11: Pelgrom plot for comparing $\sigma_{\Delta p_{Idoff}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.	100
Figure 5.12: Pelgrom plot for comparing $\sigma_{\Delta p_{Idweak}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.	100
Figure 5.13: Pelgrom plot for comparing $\sigma_{\Delta p_{Idoff}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.	101
Figure 5.14: Pelgrom plot for comparing $\sigma_{\Delta p_{Idstr}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.	101
Figure 5.15: Pelgrom plot for comparing $\sigma_{\Delta n_{Idoff}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	103
Figure 5.16: Pelgrom plot for comparing $\sigma_{\Delta n_{Idoff}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	103
Figure 5.17: Pelgrom plot for comparing $\sigma_{\Delta n_{Idweak}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	104
Figure 5.18: Pelgrom plot for comparing $\sigma_{\Delta n_{Idweak}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	104
Figure 5.19: Pelgrom plot for comparing $\sigma_{\Delta n_{Idmod}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	105
Figure 5.20: Pelgrom plot for comparing $\sigma_{\Delta n_{Idmod}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	105
Figure 5.21: Pelgrom plot for comparing $\sigma_{\Delta n_{Idstr}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	106
Figure 5.22: Pelgrom plot for comparing $\sigma_{\Delta n_{Idstr}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	106

Figure 5.23: Pelgrom plot for comparing $\sigma_{\Delta pIdoff}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	107
Figure 5.24: Pelgrom plot for comparing $\sigma_{\Delta pIdoff}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	107
Figure 5.25: Pelgrom plot for comparing $\sigma_{\Delta pIdweak}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	108
Figure 5.26: Pelgrom plot for comparing $\sigma_{\Delta pIdweak}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	108
Figure 5.27: Pelgrom plot for comparing $\sigma_{\Delta pIdmod}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	109
Figure 5.28: Pelgrom plot for comparing $\sigma_{\Delta pIdmod}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	109
Figure 5.29: Pelgrom plot for comparing $\sigma_{\Delta pIdstr}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	110
Figure 5.30: Pelgrom plot for comparing $\sigma_{\Delta pIdstr}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	110
Figure 5.31: Pelgrom plot for comparing $\sigma_{\Delta nvt}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.	112
Figure 5.32: Pelgrom plot for comparing $\sigma_{\Delta nvt}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	112
Figure 5.33: Pelgrom plot for comparing $\sigma_{\Delta nvt}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	113
Figure 5.34: Pelgrom plot for comparing $\sigma_{\Delta pvt}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.	113
Figure 5.35: Pelgrom plot for comparing $\sigma_{\Delta pvt}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design.	114

Figure 5.36: Pelgrom plot for comparing $\sigma_{\Delta_{pvt}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure design. 114

LIST OF TABLES

Table 2-1: Four possible corner MOSFET models for CMOS technology to reflect extreme process variation.	18
Table 3-1: Summary of CSM 0.35 μ m typical MOSFET key parameters.....	28
Table 3-2: Statistical BSIM3v3 model parameters chosen.....	30
Table 3-3: Electrical biasing conditions of the thin gate n/p-MOSFET for electrical parameter measurements for statistical MOSFET modelling of global process variation. $V_s=0V$ & $V_b=0V$	37
Table 3-4: Device dimensions of thin gate n/p-MOSFET used for statistical MOSFET modelling of global process variation	37
Table 3-5: Electrical biasing conditions of the thick gate n/p-MOSFET electrical parameter measurement for statistical MOSFET modelling of global process variation. $V_s=0V$ & $V_b=0V$	42
Table 3-6: Device dimensions of thick gate n/p-MOSFET used for statistical MOSFET modelling of global process variation	42
Table 4-1: Geometry matrix for MOSFET mismatch test structure design [34]....	51
Table 4-2: Reasons for the choice of MOSFET sizes in the geometry matrix [34].	52
Table 4-3: Geometry matrix for MOSFET mismatch test structure using CSM 0.18 μ m CMOS technology.	55
Table 4-4: Geometry matrix for MOSFET mismatch test structure using CSM 0.13 μ m CMOS technology.	55
Table 4-5: Geometry matrix for MOSFET mismatch test structure using CSM 90nm CMOS technology	57
Table 4-6: Details of MOSFET mismatch characterisation for CSM 0.18 μ m, 0.13 μ m and 90nm (LP) technologies. *: $V_{DD}=1.8, 1.2$ & $1.2V$ respectively for the three technologies.	59
Table 4-7: No. of fingers and the corresponding finger widths that were used in the design of multi-fingered layout MOSFET using 0.13 μ m and 90nm CMOS technology, with fixed channel length of 0.13 μ m and 0.1 μ m respectively..	63
Table 5-1: Electrical characteristics of CSM 0.13 μ m MOSFET variants.	75
Table 5-2: Electrical and process characteristics of CSM 0.13 μ m MOSFET.	76
Table 5-3: Details of the MOSFET terminal biases for the three I_d measurements. V_s and V_b are fixed at 0V for all three cases.	81
Table 5-4: Definitions of statistical MOSFET mismatch data extracted from MOSFET operation at saturation region. For all cases, $V_d=1.2V$ and both V_s and $V_b=0$	82
Table 5-5: Definitions of statistical MOSFET mismatch data extracted from MOSFET operation at linear region. For all cases, $V_d=0.1V$ and both V_s and $V_b=0$	82
Table 5-6: Critical MOSFET sizes chosen from the geometry matrix of the CSM 0.13 μ m MOSFET mismatch test structure for mismatch characterisation.....	84
Table 5-7: I_d variances for the saturation region for the 4 corner n/p-MOSFETs .	84
Table 5-8: I_d variances for the linear region for the 4 corner n/p-MOSFETs	85
Table 5-9: BSIM3v3 MOSFET parameters used in the MOSFET mismatch model developed using BPV methodology.....	86
Table 5-10: Step sizes of various BSIM3v3 MOSFET parameters used for finding the sensitivity matrix for the BPV methodology.	87

Table 5-11: Details of the numerical differential method used to derive the sensitivity matrix for BPV methodology.	88
Table 5-12: Sensitivity Matrix of n-MOSFET of W=10.4 μ m L=0.13 μ m	90
Table 5-13: Sensitivity Matrix of n-MOSFET of W=10.4 μ m L=10.4 μ m	90
Table 5-14: Sensitivity Matrix of n-MOSFET of W=0.15 μ m L=10.4 μ m	91
Table 5-15: Sensitivity Matrix of n-MOSFET of W=0.15 μ m L=0.15 μ m	91
Table 5-16: Sensitivity Matrix p-MOSFET W=10.4 μ m L=0.13 μ m	92
Table 5-17: Sensitivity Matrix p-MOSFET W=10.4 μ m L=10.4 μ m	92
Table 5-18: Sensitivity Matrix of p-MOSFET W=0.15 μ m L=10.4 μ m.....	93
Table 5-19: Sensitivity Matrix of p-MOSFET W=0.15 μ m L=0.15 μ m.....	93
Table 5-20: Ap and variances of various n-MOSFET BSIM3v3 parameters acquired by the BPV methodology. The MOSFET size is presented in L/W (μ m/ μ m) format.	96
Table 5-21: Ap and variances of various p-MOSFET BSIM3v3 parameters acquired by the BPV methodology. The MOSFET size is presented in L/W (μ m/ μ m) format.	96

LIST OF SYMBOLS & ABBREVIATIONS

(HP)	High Performance
(LP)	Low Power
δE_i	Small Change in Device Electrical Performance
δP_i	Small Change in Device Parameter
$\mu_{V_{tlin}}$	Mean Value of V_{tlin}
A_{ch}	Channel area
A_g	Fitting constant for global variation
A_{gL}	Fitting constant for global variation of gate length variance
A_{gW}	Fitting constant for global variation of gate width variance
A_l	Fitting constant for local variation
A_{lL}	Fitting constant for local variation of gate length variance
A_{lW}	Fitting constant for local variation of gate width variance
A_{ox}	Fitting constant for oxide variance
a_p	Fitting Constant Relating the Parameter Variance to Device Area
A_{VT}	Fitting constant for threshold voltage variance
A_{μ}	Fitting constant for mobility variance
BEOL	Back End of Line
BPV	Backward Propagation of Variance
CANCER	Computer Analysis of Nonlinear Circuits, Excluding Radiation
CMC	Compact Model Council
CMP	Chemical Mechanical Polish
CS&CG	Common Source and Common Gate
CSM	Chartered Semiconductor Manufacturing
DFM	Design For Manufacturing
DFY	Design For Yield
DIBL	Drain Induced Barrier Lowering
DUT	Device Under Test
FEOL	Front End of Line
FPV	Forward Propagation of Variance
gm	Transconductance
GPD	Gate Protection Diode
HDP	High Density Plasma
HPTEOS	High Pressure Tetraethyl Orthosilicate
IC	Integrated Circuit
I_{doff}	Drain Current with $V_g=0V$ and $V_d=V_{DD}$
I_{dsat}	Saturation Drain Current with V_g and V_d at V_{DD}
IMD	Inter-metal Dielectric
ITRS	International Roadmap for Semiconductor
K1	First order Body Effect Coefficient Parameter of BSIM3v3
LDD	Lightly Doped Drain

LER	Line Edge Roughness
lint	Length Offset Fitting Parameter from I-V without Bias Parameter of BSIM3v3
LOCOS	
LWR	Line Width Roughness
MPW	Multi-Project Wafer
Nch	Channel Doping Conc. Parameter of BSIM3v3
OPC	Optical Proximity Correction
P ₀	Mean Value of the Device Parameter
PCD	Plasma Charging Damage
PCM	Process Control Module
PDA	Personal Digital Assistant
PEM	Process Evaluation Module
RDF	Random Dopant Fluctuation
rsh	Source Drain Sheet Resistance (in ohms per sq.) Parameter of BSIM3v3
SLM	Scribe Line Module
SMU	Source/Monitor Unit
SoC	System on Chip
s _p	Fitting Constant Relating the Parameter Variance to Device Separation Distance
SPICE	Simulation Program with Integrated Circuit Emphasis
Tox	Gate Oxide Thickness Parameter of BSIM3v3
U ₀	Mobility at Temp = T _{nom} Parameter of BSIM3v3
UV	Ultra-violet
V _b	Substrate Voltage
VDD	Supply Voltage
V _{fb}	Flat-band Voltage Parameter of BSIM3v3
VMU	Voltage Measurement Unit
V _s	Source Voltage
VSU	Voltage Source Unit
V _T	Threshold Voltage
V _{th0}	Threshold voltage @ V _{bs} =0 for Large L parameter of BSIM3v3
V _{thlin}	Threshold Voltage with V _d =0.1V
V _{tsat}	Threshold Voltage with V _d =VDD
wint	Width Offset Fitting Parameter from I-V without Bias Parameter of BSIM3v3
X _j	Junction Depth Parameter of BSIM3v3
β	Current Factor
ΔI _{dmod_lin}	Mismatch in I _{dmod} of n/p-MOSFET, with V _g =0.6V and V _d =0.1V
ΔI _{dmod_sat}	Mismatch in I _{dmod} of n/p-MOSFET, with V _g =0.6V and V _d =1.2V
ΔI _{doff_lin}	Mismatch in I _{doff} of n/p-MOSFET, with V _g =0V and V _d =0.1V
ΔI _{doff_sat}	Mismatch in I _{doff} of n/p-MOSFET, with V _g =0V and V _d =1.2V
ΔI _{dstr_lin}	Mismatch in I _{dstr} of n/p-MOSFET, with V _g =1.2V and V _d =0.1V
ΔI _{dstr_sat}	Mismatch in I _{dstr} of n/p-MOSFET, with V _g =1.2V and V _d =1.2V
ΔI _{dweak_lin}	Mismatch in I _{dweak} of n/p-MOSFET, with V _g =0.1V and V _d =0.1V
ΔI _{dweak_sat}	Mismatch in I _{dweak} of n/p-MOSFET, with V _g =0.1V and V _d =1.2V

δP_G	Small Change in Device Parameter Due to Global Variation
$\delta P_L(g)$	Small Change in Device Parameter Due to Local Variation with g refers to device attributes, including geometry, orientation, etc.
$\mu_{process}$	Mean Device Parameter Value Under No Influence of Process Variation
$\mu_{simulation}$	Mean Device Parameter Value Under Influence of Both Inter- and Intra-die Process Variation
$\sigma_{(var,n-cov,np)}$	Standard Deviation in n-MOSFET Parameter without the n- and p-MOSFET Covariance
$\sigma_{(var,p-cov,np)}$	Standard Deviation in p-MOSFET Parameter without the n- and p-MOSFET Covariance
σ_{Ei}^2	Variance in Device Electrical Performance Due to Process Variation
σ_{Idsat}^2	Idsat Variance Due to Process Variation
σ_{Pi}^2	Variance in Device Parameter Due to Process Variation
σ_{Vtsat}^2	Vtsat Variance Due to Process Variation
$\sigma_{cov,np}$	Standard Deviation from Covariance of n- and p-MOSFET Parameter
σ_{inter}	Standard Deviation of Device Parameter Under Influence of Inter-die Process Variation
σ_{intra}	Standard Deviation of Device Parameter under Influence of Intra-die Process Variation
σP_G	Device Parameter Variance Due to Global Variation
$\sigma_{Pi,n}$	Standard Deviation in n-MOSFET Parameter
$\sigma_{Pi,p}$	Standard Deviation in p-MOSFET Parameter
$\sigma P_L(g)$	Device Parameter Variance Due to Local Variation with g refers to device attributes, including geometry, orientation, etc.
$\sigma_{\Delta Vtlin}$	Standard Deviation in Vtlin Mismatch

ABSTRACT

In this work, backward propagation of variance (BPV) methodology is used to develop a statistical MOSFET model for 0.35 μ m technology to account for global process variations based on electrical data from measurements of MOSFET test structures in scribe line module (SLM) of production wafers. BPV, coupled with Pelgrom model for MOSFET mismatch, is also used to develop a statistical MOSFET mismatch model for 0.13 μ m technology to account for local process variations such as random dopant fluctuation (RDF) in channel and line edge/line width roughness (LER/LWR) of gate based on MOSFET test structures that were specially designed and fabricated on multi-project wafer (MPW) for this study. The statistical MOSFET models developed in this work enable the designer to perform Monte Carlo circuit simulation using circuit simulator such as HPSICE so that better and accurate assessment can be made on the potential circuit performance and functional yield of the circuit at the design stage. MOSFET mismatch test structures were also specially designed, fabricated and characterised for 0.18 μ m, 0.13 μ m, and 90nm technologies to study the impact of backend-of-line (BEOL) metals, multi-fingered MOSFET layout design and gate protection diode against plasma charging damage (PCD) on MOSFET mismatch characteristics.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Process variation and technology advancement

As MOSFET scaling is projected by the 2005 International Roadmap for Semiconductors (ITRS) to reach 32nm in the near term and beyond for the long term, one of the grand challenges that will be faced is process variation [1, 2]. Process variation in integrated circuit (IC) manufacturing is inevitable, even it has not been scaled with MOSFET size [3]. Impact of random dopant fluctuation (RDF) [4] and line-edge/line-width roughness [5] on nanoscale MOSFET performance variability would deteriorate. Ultimately, this problem sets the bound for the IC designers on their aggressiveness in pushing IC design to its frontier.

The problem of process variability is made more challenging as advanced IC process technology becomes more complex with use of stress engineering techniques, high-k dielectric gate oxide and metal gate to enhance MOSFET performance. Furthermore, in order to allow smaller device to be printed, currently, complex optical proximity correction (OPC) [6] and resolution enhancement techniques (RET) have already been used to push the limit of lithography, and this complexity trend worsens with the imminent advent of immersion lithography [3]. In the long term, novel transistor structures such as double-gate MOSFETs and

FinFETs are emerging as the next generation of FET devices would have to counter the issues of process variability [7, 8].

As a result, variability of IC performance has widened and becomes more sensitive to process variation. Hence, in recent years, issues relevant to design for manufacturing (DFM) and design for yield (DFY) has been brought up very often in conferences, journals and articles for discussion. Solutions to counter process variations from process, device to design engineering perspective have been widely suggested [9].

Impact of process variation on circuit

MOSFET, which has been the unassailable transistor in digital circuits, has seen its share of the analog and RF circuit manufacturing pie becoming bigger and bigger in recent years. This is partly attributed to cost saving, enhanced performance and smaller chip size by employing system-on-chip (SoC) concept. At the same time, lower power consumption, which CMOS can provide, is very important in today's consumer market that is strongly driven by mobile applications such as personal digital assistants (PDAs), laptops and cell phones.

Analog and RF circuits are very sensitive to process variations and thus it is imperative that effects of process variation are taken into account during circuit design and simulation [10-14]. MOSFET matching is critical in the design of high-performance analog and RF CMOS circuits because matched devices are necessary in order to ensure proper operation with low distortion.

Digital circuits, which are known to be robust, have changed as technology scales. They have become sensitive to process variation as well and this may prove to be more serious as the power supply and threshold voltage of MOSFET scale down with newer technology [15-18]. Identical MOSFETs, which are designed purposely to be the same by IC designers in digital circuits, may be fabricated with undesirable varying electrical parametric performances due to process variations. This mismatch of MOSFET performance may cause the designed digital circuit to fail to function due to instability or to meet the required timing delay or power specifications.

Typically, for circuit simulators such as SPICE, a single SPICE model deck is used to characterize all transistors in a given circuit. This approach yields an identical MOSFET performance for every identical MOSFET layout design in a circuit with no simulation information concerning the effects of process variations. For example, simulation of an operational amplifier obtains a value for the quiescent output voltage. However, since this value is highly sensitive to the drain conductance of the output stage transistors, a slight deviation from the expected transistor channel length in the output stage can cause a considerable change in quiescent output voltage. A more useful and informative simulation result for this, or any, circuit characteristic includes a measure of drain conductance variance.

Role of statistical MOSFET model in statistical circuit simulation for circuit yield and functional prediction

An accurate device model is important for the IC designers to be able to predict the performance of their circuit prior to prototyping or full production. As the device size scales to sub-100nm regime, the cost of IC fabrication has become very high.

First-time silicon success of circuits is imperative to save any iterative cost in prototyping a circuit design as well as to meet time-to-market. Due to process variations, not every IC chip can meet the predicted performance, thus having a device model that can predict the effects of process variation on the parametric and functional yield of the IC becomes appealing. Hence, statistical analysis in IC design becomes very important and increasingly adopted for high IC yield.

For digital circuits, performance can typically be characterized by the signal propagation delay or the power dissipation [19]. Uncertainty in these characteristics is mainly due to variances in the raw value of drain current caused by variability in the IC fabrication process. Therefore, simple statistical parameter models, which only account for inter-die parameter variances, can be employed to describe performance variability in digital circuits.

On the other hand, analog circuits have greater dependence on second-order device effects such as channel length modulation and, thus, require more accurate device models to describe both the mean and second moment of operation. As mentioned earlier briefly, analog circuits or analog properties of digital circuits, e.g., noise margin, depend greatly on matched devices, an accurate statistical device model for circuit simulation must account for intra-die parameter variances. Because of this dependence on matched devices, analog circuits exhibit greater performance variability than digital circuits for a given fabrication process.

1.2 Objectives

The primary goal of this research is to create a statistical MOSFET model which is capable of simulating the effect of IC fabrication process variations on MOSFET during circuit simulation. As such, this statistical model must encapsulate the effects of device and circuit characteristics, such as device size, bias, and circuit layout, which are under the control of the circuit designer, on the variability of circuit performance. Additionally, to be useful to both analog and digital circuit designers, the statistical model must include the effects of both intra- and inter-die process variations. Standard MOSFET device models, while capable of determining the effects of width/length (W/L) ratio and bias conditions on the mean circuit performance, are unable to simulate circuit variances.

There are many MOSFET device models being developed and updated constantly, with BSIM being the de facto industry standard and PSP (a surface-potential-based compact model from joint development of the Pennsylvania State University and Philips Research) being the one for next generation technologies. The development of this statistical MOSFET model would not be in competition with them on modelling the MOSFET device physics but should leverage on the advantages of their availability. Favourably, the statistical MOSFET modelling methodology should be applicable to any process technology and MOSFET device model. Another important consideration is the compatibility of the developed model with existing circuit simulators such as HSPICE and SPECTRE. Thus this research involves a generic methodology that can transform any MOSFET device model

into one with statistical information of process variation mapped into its parameters and then perform statistical simulation on existing circuit simulators.

Being able to perform statistical circuit simulation, which accounts for variances in device characteristics, allows a circuit designer to estimate the functional or parametric yield of a designed circuit without fabricating the chip. It would also be useful in determining the sensitivity to the scaling of existing circuits as well as to predict performance variations in new designs. Likewise, comparison of different contending IC fabrication processes could be done not only on IC performance but also on IC yield via simulating the same circuit using statistical simulation. Furthermore, statistical simulation provides circuit designers a tool which aids in optimizing circuits given a set of process variances.

Currently, circuit simulators such as HSPICE are capable of performing Monte Carlo simulations by allowing different devices' model parameters to be randomly and independently varied. Using these simulations, statistical design centering can be carried out to determine values for circuit components and aspect ratios which maximize circuit yield. This optimization method furnishes accurate results provided that the varied circuit components are, indeed, independent. While this may be true for discrete components, components in integrated circuits exhibit significant correlations which can not be modelled during standard Monte Carlo simulations. In addition, these Monte Carlo simulations are not capable of accounting for the dependence of device size and circuit layout on parameter mismatch variances.

Therefore, the developed statistical MOSFET model should account for intra- and inter-die parameter variances as well as parameter correlations in order to optimize circuits. Once the dependence of circuit performance on device size and circuit layout can be simulated, an optimization procedure similar to design centering can be developed to realize circuits which meet required circuit yield while minimizing the total area of the circuit. In this respect, the model developed in this research can actually be used in the circuit optimization.

1.3 Organization of the Thesis

In Chapter 1, the motivation of having a statistical MOSFET model for statistical circuit simulation that can encapsulate the effects of process variation information is established. The goals that are to be fulfilled by the developed statistical MOSFET model are also laid down.

In Chapter 2, a thorough background and literature review on solutions to tackle process variation in IC manufacturing and circuit simulation will be given. This would allow comprehension of the significance of this work as well as better understanding of the technical terms and approaches that are to be discussed.

In Chapter 3, the development of statistical MOSFET model for global process variation will be presented and discussed in details. The BPV methodology used in the development will be elaborated and plots on Monte Carlo simulation of the n/p-MOSFET under global process variation will be discussed.

In Chapter 4, the design of MOSFET mismatch test structure will be presented and discussed. Measurement setup for MOSFET mismatch characterization will be discussed and the procedure of characterizing the MOSFET mismatch will be gone through. Extrinsic factors that might influence intrinsic MOSFET mismatch characterization will be studied.

In Chapter 5, the development of a MOSFET mismatch model using the BPV methodology coupled with Pelgrom model will be presented and discussed in

details. The scalability of the MOSFET mismatch model for different MOSFET sizes, different terminal biases and different MOSFET electrical characteristics will be studied with the use of Pelgrom plots.

In Chapter 6, summaries and conclusions on the works that contributed to chapters 3, 4 and 5 were made. Next, improvements that can be made to the thesis work were also suggested. Lastly, recommendations for future work that have significant impact and are relevant to process variation and MOSFET performance will be made.

CHAPTER 2

BACKGROUND & LITERATURE REVIEW

2.1 Process Variation in IC Manufacturing

In IC manufacturing, process variations can be classified into two groups and they are inter-die and intra-die process variations [20]. Figure 2.1 shows that inter-die process variation is used to characterize process variation observed from die-to-die, wafer-to-wafer and lot-to-lot. As a result, inter-die process variation is also commonly known as global process variation. Sources for inter-die process variation can be attributed to the drift of process control in fabrication equipment, the process control difference in different production lines of a fab and the different process controls for different fabs. Variations in electrical performance of components such as resistors, capacitors and transistors induced by inter-die process variation are termed global device variations. From a statistical modeling perspective, global device variation is easy to model, since it affects all components in a given circuit equally. Thus, in a statistical MOSFET model to address inter-die process variation, every relevant MOSFET parameter can be represented by a deviation in the mean.

Figure 2.1: Two groups of process variation: inter-die and intra-die variability [3].

Intra-die process variation refers to process variation that causes identically designed components in an IC to behave differently in electrical performance. Intra-die process variation is also commonly known as local process variation and the sources are confined to wafer-level process variations. Examples are the uniformity of deposited film thickness or quality, degree of lithography misalignment, difference in lithography exposure strength and depth of focus, concentration and profile of implant doping, etching profile of structure. The component's variation in electrical performance induced by intra-die process variation is termed local device variation or device mismatch, an example is the MOSFET mismatch. MOSFET mismatch may cause an IC to fail or perform badly. Device mismatch is much more difficult to model accurately than global device variation as it is dependent on the matching devices' dimensions, spatial separation and layout of matched devices.

Figure 2.2 shows the combination impact of inter-die and intra-die process variations on the standard deviation of a device parameter. In Figure 2.2, μ_{process} is the value of a device parameter under no influence of inter-die and intra-die process variation. Inter-die process variation alone would cause the device parameter to vary with a Gaussian distribution of mean, μ_{process} , and standard deviation, σ_{inter} . Intra-die process variation, alone, would cause the device parameter to vary with a Gaussian distribution of mean, μ_{process} , and standard deviation, σ_{intra} . In reality, both inter- and intra-die process variations would occur together and it would cause device parameter to vary with a Gaussian distribution of mean, $\mu_{\text{simulation}}$, and standard deviation, σ_{intra} . Though as shown in Figure 2.2, σ_{inter} is generally much larger than σ_{intra} , in many ICs, σ_{intra} is the deciding factor of the IC performance. For example, MOSFET mismatch would be more important than inter-die MOSFET variation on the performance of a current mirror with a constant current bias as the former can result in a systematic offset in the mirrored current.

Figure 2.2: Probability density distribution of device parameter as result of intra-die and inter-die process variation [19].

2.2 Circuit Simulation and Compact Models

Circuit simulation

Traditionally electronic circuits had been designed by building a prototype on a ‘breadboard’. This prototype could easily be evaluated and fine-tuned. But when the circuits grew larger and more complex, it became desirable to simulate their behaviours on computers. This was particularly true for ICs with hundreds and thousands of components. The task of setting up and testing such a circuit on a breadboard was becoming impossible. At the same time, computing power was increasing and it was finally possible to write a circuit simulation program that could provide accurate results. This made it possible for a circuit to be designed, evaluated and redesigned using only computer simulations. The first attempt to make a computer-aided circuit simulator was CANCER (Computer Analysis of Nonlinear Circuits, Excluding Radiation). CANCER was the predecessor of the SPICE (Simulation Program with Integrated Circuit Emphasis) program. SPICE and CANCER were developed at the University of California at Berkeley. Today SPICE is the standard circuit simulation tool for the IC industry and there exists different versions of the original SPICE, such as HSPICE from Synopsys and SPECTRE from Cadence.

A SPICE-type simulator treats a circuit in a node/element fashion as shown in Figure 2.3. The circuit is described as a collection of various electronic components (resistors, capacitors, diodes etc.) that are connected to one another at numbered nodes. This means that a circuit is completely defined in terms of the nodes and by the components connected to the nodes. A circuit with n nodes will be described by an $n \times n$ matrix. By defining state variables at each node (voltages)

and fixing the external nodes (such as ground, supply voltage etc) the matrix can be solved to determine the values of the state variables. In order to reach a solution, a model for each component is needed. The component models that are used within a circuit simulator are also known as compact models. SPICE has built-in models for resistors, capacitors, inductors, diode and transistors. For simulation of more complex semiconductor devices such as transistors, special models such as MEXTRAM for BJT and BSIM for MOSFET are needed. As IC processing technology advances, many different compact models, especially for MOSFETs, have been developed and used over the years.

Figure 2.3: A schematic for a circuit to be simulated using SPICE, the nodes are labelled V_{in} , $n1$, $n2$, V_{dd} , GND and V_{ut} .

MOSFET compact models [21, 22]

The MOSFET compact models that are commonly employed can be divided into three historical generations. The first generation of MOSFET models treats the device as almost ideal, describing the MOSFET from very simple physically based parameters. This generation of models consists of the Level 1, Level 2 and Level 3 models. The second generation of models is markedly different; here the focus of the model is for circuit simulation usage. In this generation the parameters in the model are empirical in their characters as they are usually used as fitting constants without any physical basis. This generation of models encompasses BSIM1, BSIM2 and HSPICE Level 28. The basic intent of the third generation of models is to return to a simpler model structure with a reduced number of parameters. The parameters should also be physically based. This generation also includes more advanced smoothing functions; with these functions the device equations are smooth and continuous, and a single equation is used for all regions of operation (sub- threshold, linear and saturation). Typical models from this generation are BSIM4, BSIM3, BSIM3v3 and MOS Model 9 (MM9) and MOS Model 11 (MM11) from Philips. This generation of compact models, for example MM11 is intended for digital, analog and RF circuit simulation in modern CMOS technologies and was developed to give accurate descriptions of the current and charges, especially the first-order derivatives (trans-conductance, conductance, capacitances, etc.). The main feature of the MM11 is that it is surface-potential based, thus resulting in equations that are valid in all regions (accumulation, depletion and weak-moderate- and strong inversion). The most recent addition to the MOSFET compact model family is the PSP model [23], which is intended for the same applications as MM11. The PSP model has its origin in the MM11 and is jointly

developed by Philips and Pennsylvania State University. The PSP model is also a surface-potential based MOSFET model that contains all important physical effects (mobility reduction, velocity saturation, Drain Induced Barrier Lowering (DIBL), gate current etc.). The PSP model was recently selected to be the industry-wide standard for future nanometre chip design by the Compact Model Council (CMC). CMC is the world's foremost authority on standardization, implementation and use of device compact models. It comprises of leading semiconductor companies and circuit simulator makers.

2.3 Statistical MOSFET Modelling

Statistical circuit simulation[24, 25]

Circuit simulation, with the use of various device compact models, predicts the behaviour of a circuit. Statistical circuit simulation can also be performed to predict the effects of variations in device performances on circuit performance. The sources of variations in device performances could typically be due to IC manufacturing process variation or IC operation ambient temperature distribution. In this work, the attention would be focused on the former so as to facilitate accurate statistical circuit simulation that is critical to ensure fabricated IC with desirable performance yield under all manufacturing process variations.

Corner models [24]

Traditionally, circuit simulation uses device corner models to study the effects of process variation on worst/best-case circuit performance. There are usually four possible corner MOSFET models as shown in Table 2-1 to account for the four combinations of fast and slow n/p-MOSFETs. These corner device models' parameters would usually be extracted from device test structures in wafer lots that are fabricated with purposely skewed process recipes so as to reflect the worst/best-case of devices that can be fabricated from the production line. For MOSFET, the corner models' parameters would correspond to the worst and best-case MOSFET model parameters that give the worst and best-case MOSFET performance in saturation drain current, I_{dsat} . I_{dsat} is the MOSFET drain current that flows when both the gate and drain are held at the specified supply voltage, V_{DD} . Performing worst/best-case simulation is similar to typical circuit simulation

except that the number of circuit simulations depends on the number of corner models.

For CMOS technology, there are a minimum of four possible combinations of corner n-MOSFET and p-MOSFET models. Each of them is defined by a two-letter acronym describing the relative performance characteristics of the n-MOSFET and p-MOSFET with respect to the typical device. The letters describe the n/p-MOSFET operation as being fast (F), or slow (S), with relatively higher and lower I_{dsat} respectively. They are summarized in Table 2-1. As for the nominal or typical (TT) MOSFET model, its model parameters reflect the process target and give the nominal MOSFET electrical performance. An example of I_{dsat} plot for corner models of p-MOSFET against n-MOSFET is shown in Figure 2.4.

Table 2-1: Four possible corner MOSFET models for CMOS technology to reflect extreme process variation.

Corner Model	Definition
SS	slow p-MOSFET & slow n-MOSFET
FF	fast p-MOSFET & fast n-MOSFET
FS	fast p-MOSFET & slow n-MOSFET
SF	slow p-MOSFET & fast n-MOSFET

Ideally, the corner model files should be based on parameters extracted from an extensive data base that represents the statistical variation of the process. However, usually there is either no real data or not enough statistically meaningful data on which the worst/best model parameters are extracted. Sometimes, this is due to the fact that the IC design has to take place while technology development is still on-

going and so the process variation is still not statistically stable. Furthermore, the time taken for parameter extraction of a large number of MOSFETs is lengthy for a MOSFET model such as BSIM3v3 with hundreds of model parameters.

Despite the circumstances and justification of corner models usage, there are serious problems for these corner models to be continually used for IC simulation on the impact of process variation. Firstly, these corner models represent the worst/best-case scenario for digital IC well but not for analog or mixed-signal IC. Secondly, they are overly pessimistic in the prediction of the impact of process variation on MOSFET performance. This is because the development of the corner models does not take into consideration the correlation of model parameters between n-MOSFET and p-MOSFET as well as within themselves for a MOSFET type. Thirdly, there is no differentiation of inter-die and intra-die device variations.

Figure 2.4: Process variation map for ID_{sat} of n-MOSFET and p-MOSFET [3].

Statistical MOSFET modeling for global process variation

To answer the shortcomings of using corner models, Monte Carlo based statistical circuit simulation is more commonly used to address the impact of process variation on IC. This approach not only provides a more realistic and accurate representation of device performance variations by addressing device performance correlation but also includes the effect of process variations as illustrated in Figure 2.4, by the rings of eclipses that circumvent the square data points. The statistical device models for Monte-Carlo based statistical circuit simulation usually consists of two components: the inter-die device variation and intra-die device variation. Though only a statistical MOSFET model would be touched on here, the concept applies to other devices.

Statistical MOSFET model for inter-die device variation

There are generally two approaches to develop statistical device model for inter-die device variation. They are the forward propagation of variance (FPV) [19, 26-29] and the backward propagation of variances (BPV) [25, 30]. For FPV, the variances in device parameters are derived from the electrical test (E-Test) measurement data of process control module (PCM), for instance, the E-Test data on oxide thickness, line-width, doping concentration, etc. In the case of MOSFETs, they can be used to obtain the variation of gate oxide thickness, gate length and width, channel doping concentration, respectively. These device parameter variances are then mapped into the typical MOSFET model so that Monte-Carlo circuit simulation can be performed. While for BPV, the variances in device parameters are extracted from the measurement of device desired electrical performances at different terminal biases. For example, in the case of MOSFET,

measurement of threshold voltage, V_t , and saturation drain current, I_{dsat} , for many MOSFETs are used to solve for the variances in the gate oxide thickness, gate length and width, and channel doping concentration, etc.

Statistical MOSFET model for intra-die device variation

For a statistical MOSFET model for intra-die variation, there are two approaches: analytical model and BPV. The analytical approach will be discussed by a brief description of the key results determined by three research works by Shyu, Lakshmikumar, and Pelgrom in chronicle order.

Shyu et al. [31, 32] studied the dependence of the standard deviation of current sources and capacitors on their sizes. They divided the causes of device mismatch into local variations, characterized by mismatch-causing phenomena with short correlation distances, and global variations, characterized by long correlation distances. The correlation distance refers to the distance for which a process disturbance affects transistor operation. If this distance is much smaller than the normal distance between transistors, the disturbance falls into the category of a local variation and affects, at most, one transistor. An example of a local variation is trapped charge in the gate oxide layer, which affects only one transistor. Conversely, global variations, caused by process disturbances with long correlation distances, affect all transistors in a given region. An example of a global process disturbance is the distribution of gate oxide thickness across the wafer, which generally exhibits a radial pattern from wafer center to edge. Thus, the relative device location determines the extent of the global variation effect on the

mismatch. Devices in close proximity are affected by global variations to a lesser extent than those at great separation distances.

Shyu derived transistor variances in terms of their effect on current matching in a current mirror. However, a basic form for the mismatch variance of parameters, $\sigma^2(\Delta P)$, such as the threshold voltage, oxide thickness, and mobility can be given by (2.1)

$$\sigma^2(P_1 - P_2) = \sigma^2(\Delta P) = A_g + \frac{A_l}{WL} \quad (2.1)$$

where A_g and A_l are fitting constants representing global and local variations, respectively, P_1 and P_2 can be any device parameter of interest for adjacent matched devices, and W refers to the channel width while L refers to the channel length. Local variation can be modeled by a spatial white noise mismatch-causing phenomenon. Thus, the area dependence in (2.1) is analogous to a spatial filtering of the random, local variations: the larger the device, the greater probability that local variations being "averaged out".

Additionally, Shyu examined edge effects, which partially explain the variance of channel length and width. The forms for channel length and width mismatch variances are, respectively:

$$\sigma^2(\Delta L) = A_{gL} + \frac{A_{lL}}{W^2} \quad (2.2)$$

$$\sigma^2(\Delta W) = A_{gW} + \frac{A_{lW}}{L^2} \quad (2.3)$$

In eq. (2.2), A_{gL} and A_{lL} represent the fitting constants of global and local variation of channel length, respectively, while in eq. (2.3), A_{gW} and A_{lW} represent the

fitting constants of global and local variation of channel width, respectively. Once again, the geometry dependent terms can be considered as a spatial filtering of local process disturbances in one dimension.

Lakshmikumar et al. [33] furthered Shyu's work by separating the area dependence of transistor mismatch into variance models for two parameters: the threshold voltage, V_T , and the current factor, β .

$$\sigma^2(\Delta V_T) = \frac{A_{VT}}{WL} \quad (2.4)$$

$$\frac{\sigma^2(\Delta\beta)}{\beta^2} = \frac{A_\mu + A_{ox}}{WL} + \frac{\sigma_L^2}{L^2} + \frac{\sigma_W^2}{W^2} \quad (2.5)$$

where A_{VT} , A_μ , A_{ox} are fitting constants relating the threshold voltage, mobility, and oxide capacitance to their normalized variance (variance/mean²), respectively. Unlike Shyu, Lakshmikumar used constant values for the standard deviation of the channel length and width, σ_L and σ_W . Additionally, the effect of global variations is not included in the Lakshmikumar's parameter variance model.

Pelgrom et al. further parameterized device mismatch by including a term for the substrate factor variance. Additionally, the effect of global variations was altered from a constant in Shyu's parameter variance model to a spacing dependent term. Pelgrom's general parameter variance model follows:

$$\sigma^2(\Delta P) = \frac{a_p}{WL_g} + s_p^2 D_{12}^2 \quad (2.6)$$

where a_p and s_p are the fitting constants relating the parameter variance to the device area (WL) and separation distance (D_{12}), respectively. Thus, the contribution to the parameter mismatch variance of another circuit characteristic,

the circuit layout, is addressed by Pelgrom's model. Using device data extracted from several batches, Pelgrom determined that edge effects have a negligible contribution to the overall variance of the current factor. This assumption will also be applied during the derivation of a general statistical parameter model in the research described in this thesis. However, it is expected that for very short or very narrow devices, edge effects will contribute heavily to the parameter variance.

For the BPV approach to statistical modeling for intra-die device variation, work by McAndrew [10] will be used for discussion and it includes BPV approach for statistical modeling for inter-die device variation.

For a particular device parameter P , its value can be modeled as

$$P = P_0 + \delta P_G + \delta P_L(g) \quad (2.7)$$

where P_0 is the mean value of the parameter, δP_G its global variation, and $\delta P_L(g)$ is its local variation. g refers to device attributes, including geometry, orientation, etc.

Thus, P can be statistically modeled as

$$\sigma P = \sigma P_0 + \sigma P_G + \sigma P_L(g) \quad (2.8)$$

The global variation, also known as inter-die variation, is correlated across a die and is generally independent of geometry. The local variation, also known as intra-die variation or mismatch, is uncorrelated across a die and strongly depends on geometry. It increases with the decrease in device size.

The goal of the BPV modeling approach is to represent component electrical behavior E accurately. Because of model differences, values of P best for one model need not be the best values for another model. So instead of relying on direct measurements of P , electrical behaviours that are most important for circuits are chosen as they can be measured easily and directly. Examples in the case of a MOSFET include transconductance g_m , drain current at different drain and gate biases, and output resistance.

The relationship between small changes in device electrical performances ∂E_i , device parameters ∂P_j and their partial derivatives $\partial E_i / \partial P_j$ can be approximated to first order as:

$$\delta E_i = \sum_j \frac{\partial E_i}{\partial P_j} \delta P_j \quad (2.9)$$

Thus, their relationship in term of their variances is:

$$\sigma_{E_i}^2 = \sum_j \left(\frac{\partial E_i}{\partial P_j} \right)^2 \sigma_{P_j}^2 \quad (2.10)$$

So by computing $\sigma_{E_i}^2$ from measurement data and calculating the sensitivities $(\partial E_i / \partial P_j)^2$ from numerical simulation of the typical model with circuit simulator, $\sigma_{P_i}^2$ can be calculated. The calculation in eq. (2.10) requires the matrix of squared sensitivities to be well conditioned. Testing the condition number of this matrix allows verification of the suitability of the tests E to make the P mathematically observable. The variances in eq. (2.10) can be from device measurement of intra-die and inter-die process variation such that $\sigma_{PL}^2(g)$ and σ_{PG}^2 can be derived respectively. If σ_{PL} is significant with respect to σ_{PG} , then calculation of σ_{PG} is done based on $\sigma_{PG}^2 = \sigma_P^2 - \sigma_{PL}^2(g)$, with the mismatch variance removed from the

ET data variance. McAndrew called it the “unified” approach for statistical modeling as not only is it simple and physically correct, but it is valid for modeling both global and local variation.

CHAPTER 3

STATISTICAL MOSFET MODELING FOR GLOBAL PROCESS VARIATION USING BPV METHODOLOGY

In this chapter, the development of a statistical MOSFET model for global process variation based on BPV methodology will be discussed. The process technology used is from Chartered Semiconductor Manufacturing (CSM) 0.35 μ m CMOS process technology.

3.1 0.35 μ m CMOS Technology

CSM 0.35 μ m technology uses LOCOS (Local Oxidation of Silicon) technology for isolation with retrograde n-well in p-substrate to counter punch-through effect. It uses LDD (lightly doped drain) implants for both n- and p-MOSFET to alleviate hot carrier effects and drain induced barrier lowering (DIBL) issues. Ti silicidation is used on source, drain and n/p-poly gate for both n- and p-MOSFETs, respectively, to reduce the parasitic resistance.

Up to four aluminum/copper alloy (Al-Cu) metal layers and two polysilicon(poly) layers can be used for routing. Titanium nitride (TiN) is used as barrier to prevent diffusion of metal layer via the inter-metal dielectric (IMD) layers. The IMD uses HDP (High Density Plasma) and HPTEOS (High Pressure Tetraethyl Orthosilicate) with chemical mechanical polish (CMP) for local and global planarization.

There are two types of MOSFET with different gate oxide thickness in the CSM 0.35 μ m technology. The thin gate MOSFET, which is also known as the core

MOSFET, has the gate oxide thickness of $75\text{\AA}$ for both n- and p-MOSFETs. The thick-gate MOSFET, which is also known as I/O MOSFET, has gate oxide thickness of $120\text{\AA}$ for both n- and p-MOSFETs. The maximum operating voltage (V_{DD}) used by the core MOSFET is 3.3V while that of I/O MOSFET is 5V . The typical MOSFET key parameters for the CSM $0.35\mu\text{m}$ technology are summarized in Table 3-1. V_{th} refers to the gate voltage applied when a critical current of $0.1\mu\text{A} \times (W/L)$ flows under a drain bias of 0.1V . I_{Dsat} is the drain current normalized by channel width when both gate and drain voltage are biased at V_{DD} ($3.3/5\text{V}$). BV_{dss} is the drain voltage that will cause breakdown to occur when gate voltage is at V_{DD} . I_{off} is the drain current when gate voltage is at 0V while drain voltage is at V_{DD} . Elec. Tox is the gate oxide thickness obtained using CV measurement.

Table 3-1: Summary of CSM $0.35\mu\text{m}$ typical MOSFET key parameters.

TYPICAL TRANSISTOR PARAMETERS					
	3.3v Thin Gate $w/L = 20/0.35$		5v Thick Gate $w/L = 20/0.5$		
	N Channel	P Channel	N Channel	P Channel	
V_{th}	0.60	-0.75	0.75	-0.77	V
I_{Dsat}	540	-250	535	-280	$\mu\text{A}/\mu\text{m}$
BV_{dss}	>6.6	<-6.6	>8.5	<-7.7	V
I_{off}	<30	>-30	<30	>-30	$\text{pA}/\mu\text{m}$
Elec. Tox	75	75	120	120	$\text{\AA}$

3.2 MOSFET Characterization For Global Process Variation

The measurement data for the development of the statistical MOSFET model were available from the electrical test of MOSFETs on the scribe line module (SLM) of CSM production wafer as shown in Figure 3.1. Measurement of MOSFET electrical parameters such as saturation drain current (I_{dsat}), off drain current (I_{doff}), linear threshold voltage (V_{tlin}) and saturation threshold voltage (V_{tsat}), is performed on the SLM MOSFET of production wafers. Besides MOSFET, there are other device test structures in the SLM to facilitate the verification of correct process recipe being executed and also to ensure the electrical performance specifications of devices being met. Thus, SLM is also known as PCM (process control module). Only after this qualification step will the finished production wafer be sent to the customer, or be sent for electrical sorting and then dicing. The SLM device test structures are located along the scribe line between dice on a wafer as shown in Figure 3.1b.

Figure 3.1: Different types of process control module (PCM).

3.3 Statistical MOSFET Model For Global Variation

In this section, the details of developing the statistical MOSFET model for global process variation using BPV methodology will be discussed.

Statistical MOSFET model parameters

In order to develop a statistical MOSFET model using BPV methodology, the typical MOSFET model parameters must be properly extracted. For this work, the BSIM3v3 MOSFET device model, which is the de facto industry standard, was used for developing the statistical MOSFET model for global process variation. The typical BSIM3v3 MOSFET model parameters were extracted. The key BSIM3v3 MOSFET parameters that were picked for developing the statistical MOSFET model are shown in Table 3-2.

Table 3-2: Statistical BSIM3v3 model parameters chosen.

BSIM3v3 Parameters	Parameters Definition
Vth0	Zero substrate bias threshold voltage
Tox	Gate oxide thickness
xl	Channel length offset
xw	Channel width offset
xj	Source/Drain junction depth

These parameters are selected because they are physically-based and they address the main sources of global variation that can affect the MOSFET electrical performance greatly. The next step would be to determine the critical MOSFET electrical parameters to be statistically modeled.

MOSFET Electrical Characteristics for BPV Targets

The electrical characteristics that were used as BPV targets for the development of the statistical MOSFET model are V_{tsat} and I_{dsat} . The obvious reason for picking these MOSFET electrical characteristics as targets is because they are the key drivers of MOSFET performance. So it is important to study how global process variation would affect these key drivers. For a foundry such as CSM, these values are being monitored for every production wafer's SLM MOSFET and thus there is a large amount of readily available useful data to be used for developing a statistical MOSFET model with high degree of statistical significance.

In order to derive the BPV targets from the SLM MOSFET data, their variances have to be computed and organized in a vector form as (3.1).

$$\begin{bmatrix} \sigma_{I_{dsat}}^2 \\ \sigma_{V_{tsat}}^2 \end{bmatrix} \quad (3.1)$$

This has to be done for both n- and p-MOSFETs of different sizes so that the developed statistical MOSFET model is scalable for different MOSFET geometries. Thus statistical circuit simulation for global process variation can be performed on circuit built with different MOSFET sizes and types realistically and accurately. This can be done only if measurement data is available for various MOSFET sizes of both n and p types.

Sensitivity Matrix

After identifying the key MOSFET electrical characteristics as well as MOSFET model for statistical MOSFET model development, the next thing would be to derive the sensitivity matrix with respect to global process parameters (V_{th0} , T_{ox} , x_l , x_w and x_j). The sensitivity matrix for a single MOSFET dimension is shown below.

$$\begin{bmatrix} \left(\frac{dI_{dsat}}{dV_{th0}}\right)^2 & \left(\frac{dI_{dsat}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dsat}}{dx_l}\right)^2 & \left(\frac{dI_{dsat}}{dx_w}\right)^2 & \left(\frac{dI_{dsat}}{dx_j}\right)^2 \\ \left(\frac{dV_{tsat}}{dV_{th0}}\right)^2 & \left(\frac{dV_{tsat}}{dT_{ox}}\right)^2 & \left(\frac{dV_{tsat}}{dx_l}\right)^2 & \left(\frac{dV_{tsat}}{dx_w}\right)^2 & \left(\frac{dV_{tsat}}{dx_j}\right)^2 \end{bmatrix} \quad (3.2)$$

The values of each partial differentiation in the sensitivity matrix would be found by numerical differentiation of the simulated data obtained from HSPICE circuit simulator and typical MOSFET model, with the various corresponding MOSFET parameter (V_{th0} , T_{ox} , x_l , x_w and x_j) set at different small step sizes from the nominal value.

The complete BPV methodology for the statistical MOSFET model development for a single MOSFET size is as follows:

$$\begin{bmatrix} \sigma_{I_{dsat}}^2 \\ \sigma_{V_{tsat}}^2 \end{bmatrix} = \begin{bmatrix} \left(\frac{dI_{dsat}}{dV_{th0}}\right)^2 & \left(\frac{dI_{dsat}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dsat}}{dx_l}\right)^2 & \left(\frac{dI_{dsat}}{dx_w}\right)^2 & \left(\frac{dI_{dsat}}{dx_j}\right)^2 \\ \left(\frac{dV_{tsat}}{dV_{th0}}\right)^2 & \left(\frac{dV_{tsat}}{dT_{ox}}\right)^2 & \left(\frac{dV_{tsat}}{dx_l}\right)^2 & \left(\frac{dV_{tsat}}{dx_w}\right)^2 & \left(\frac{dV_{tsat}}{dx_j}\right)^2 \end{bmatrix} \begin{bmatrix} \sigma_{V_{th0}}^2 \\ \sigma_{T_{ox}}^2 \\ \sigma_{x_l}^2 \\ \sigma_{x_w}^2 \\ \sigma_{x_j}^2 \end{bmatrix} \quad (3.3)$$

The BPV methodology was performed for every MOSFET size with available measurement data to derive the matrix equation in (3.3). This was done to increase the scalability of the statistical MOSFET model. Thus for a single type of statistical MOSFET model, the complete matrix equation to be solved for the MOSFET parameter variances is given by (3.4) and the subscripts n1 and n2 represent n-MOSFET of different sizes. Optimisation technique is used to solve for vector of device parameter variances ($\sigma_{V_{th0}}^2, \sigma_{T_{ox}}^2, \sigma_{x_l}^2, \sigma_{x_w}^2$ and $\sigma_{x_j}^2$). The same was done for p-MOSFET as well even though only n-MOSFET was shown as an example in (3.4).

$$\begin{bmatrix} \sigma_{I_{dsat},n1}^2 \\ \sigma_{V_{tsat},n1}^2 \\ \sigma_{I_{dsat},n2}^2 \\ \sigma_{V_{tsat},n2}^2 \\ \vdots \end{bmatrix} = \begin{bmatrix} \left(\frac{dI_{dsat},n1}{dV_{th0}}\right)^2 & \left(\frac{dI_{dsat},n1}{dT_{ox}}\right)^2 & \dots \\ \left(\frac{dV_{tsat},n1}{dV_{th0}}\right)^2 & \left(\frac{dV_{tsat},n1}{dT_{ox}}\right)^2 & \dots \\ \left(\frac{dI_{dsat},n2}{dV_{th0}}\right)^2 & \left(\frac{dI_{dsat},n2}{dT_{ox}}\right)^2 & \dots \\ \left(\frac{dV_{tsat},n2}{dV_{th0}}\right)^2 & \left(\frac{dV_{tsat},n2}{dT_{ox}}\right)^2 & \dots \\ \vdots & & \end{bmatrix} \begin{bmatrix} \sigma_{V_{th0}}^2 \\ \sigma_{T_{ox}}^2 \\ \sigma_{x_l}^2 \\ \sigma_{x_w}^2 \\ \sigma_{x_j}^2 \end{bmatrix} \quad (3.4)$$

After finding the n-MOSFET and p-MOSFET device parameter variances, the next step is to find the device parameter covariances. This is important to ensure that the correlations between the device parameter variances of n-MOSFET and p-MOSFET are taken care of so as to allow an accurate and realistic statistical MOSFET model for circuit simulation of global process variation. To achieve this,

the same approach to acquire the matrix to solve the n-MOSFET and p-MOSFET parameter variances using BPV approach was repeated.

First the n-MOSFET and p-MOSFET electrical parameter covariances of similar sizes have to be computed from the SLM MOSFET characterization data and organized in a vector form as (3.5).

$$\begin{bmatrix} \sigma_{Idsat,np}^2 \\ \sigma_{Vtsat,np}^2 \end{bmatrix} = \begin{bmatrix} \sigma_{Idsat,n} & X & \sigma_{Idsat,p} \\ \sigma_{Vtsat,n} & X & \sigma_{Vtsat,p} \end{bmatrix} \quad (3.5)$$

The sensitivity matrix in (3.6) for solving the covariance of n/p-MOSFET was derived by multiplying the partial derivative of the n-MOSFET with p-MOSFET for every MOSFET parameter.

$$\begin{bmatrix} \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) \\ \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) \\ \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) \\ \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right) \\ \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right) \end{bmatrix} \quad (3.6)$$

The complete matrix for solving the n/p-MOSFET parameter covariances is given by (3.7).

$$\begin{bmatrix} \sigma_{Idsat,np1}^2 \\ \sigma_{Vtsat,np1}^2 \\ \sigma_{Idsat,np2}^2 \\ \sigma_{Vtsat,np2}^2 \\ \vdots \end{bmatrix} = \begin{bmatrix} \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right)_{np1} & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right)_{np1} & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right)_{np1} & \dots \\ \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right)_{np1} & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right)_{np1} & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right)_{np1} & \dots \\ \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right)_{np2} & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right)_{np2} & \left(\frac{dI_{dsat}}{dV_{th0}} \frac{dI_{dsat}}{dV_{th0}} \right)_{np2} & \dots \\ \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right)_{np2} & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right)_{np2} & \left(\frac{dV_{tsat}}{dV_{th0}} \frac{dV_{tsat}}{dV_{th0}} \right)_{np2} & \dots \\ \vdots & \vdots & \vdots & \dots \end{bmatrix} \begin{bmatrix} \sigma_{Vth0,np}^2 \\ \sigma_{Tox,np}^2 \\ \sigma_{xl,np}^2 \\ \sigma_{xw,np}^2 \\ \sigma_{xj,np}^2 \end{bmatrix} \quad (3.7)$$

For any arbitrary n-MOSFET and p-MOSFET device parameter P_i , it would have two standard deviation values, (3.8) and (3.9), for n-MOSFET and p-MOSFET, respectively. Each of them is made up of two parts. One part is coming from the standard deviation of P_i for the corresponding MOSFET type without any contribution from the n-MOSFET or p-MOSFET, $\sigma_{(\text{var},n\text{-cov},np)}$ or $\sigma_{(\text{var},p\text{-cov},np)}$, while the other part is the covariance $\sigma_{\text{cov},np}$ common for n/p-MOSFET.

$$\sigma_{P_{i,n}} = \sigma_{(\text{var},n\text{-cov},np)} + \sigma_{\text{cov},np} \quad (3.8)$$

$$\sigma_{P_{i,p}} = \sigma_{(\text{var},p\text{-cov},np)} + \sigma_{\text{cov},np} \quad (3.9)$$

These two parts for every statistical MOSFET parameter would be input into the typical MOSFET model to perform Monte-Carlo simulation of the chosen n/p-MOSFET electrical performances. The generated Monte-Carlo simulation data can be used to compare against measurement data for verification and calibration of the statistical MOSFET model for global process variation.

Verification plots for statistical MOSFET model for global process variation

To verify the developed statistical MOSFET global variation model, Monte Carlo simulations were run on HSPICE circuit simulator to generate simulated data points for comparison against the measurement data. The simulations were run under the condition of 3 sigma global process variation. The verification plots compare the p-MOSFET data against that of n-MOSFET data. These plots capture 3 pieces of information; the variance of the n-MOSFET data, the variance of the p-MOSFET data, and the covariance of the n-MOSFET data vs. the p-MOSFET data. Both the results for thin gate MOSFET and thick MOSFET would be shown.

Monte Carlo simulation at different sigma process variation

The developed statistical MOSFET model also allows circuit simulation at different sigma process variation for the device parameters (V_{th0} , T_{ox} , x_l , x_w and x_j) so as to predict the circuit performance and functional yield at different sigma of process control for global process variation. Figure 3.2 shows how the developed statistical MOSFET model can simulate a n-MOSFET I_{dsat} behavior at different sigma of process variation.

Figure 3.2: Monte Carlo simulation of I_{dsat} for n-MOSFET and p-MOSFET showing simulated data mc1, mc2 and mc3 at 1, 2 and 3 sigma of global process variation respectively.

Thin gate 3.3V n/p-MOSFET

The representations of different data in the thin gate 3.3V n-MOSFET and p-MOSFET verification plots are as follow:

- 'x' – Measured data (150 data points)
- 'o' – Monte Carlo simulation for 3 sigma of process variation (1000 data points)
- '◇' – Monte Carlo simulation for 2 sigma of process variation (1000 data points)
- 'Δ' – Monte Carlo simulation for 1 sigma of process variation (1000 data points)
- '■' – Process corners (center = typical/nominal, ss=slow-slow, sf=slow-fast, ff=fast-fast and fs=fast-slow)

MOSFET electrical parameters (I_{dsat} , V_{tsat}) were measured or simulated using biasing conditions as in Table 3-3 with both source voltage (V_s) and substrate voltage (V_b) at 0V. The dimensions of the thin gate n-/p-MOSFET that were used are given in Table 3-4.

Table 3-3: Electrical biasing conditions of the thin gate n/p-MOSFET for electrical parameter measurements for statistical MOSFET modelling of global process variation. $V_s=0V$ & $V_b=0V$.

Data	Description
I_{dsat}	Value of drain current, I_d , when: Drain voltage, $V_d=3.3V$ Gate voltage, $V_g=3.3V$.
V_{tsat}	Value of gate voltage, V_g , when: Drain current, $I_d=0.1\mu A * W/L$, Drain voltage, $V_d=3.3V$.

Table 3-4: Device dimensions of thin gate n/p-MOSFET used for statistical MOSFET modelling of global process variation

Width/ μm	Length/ μm
20	0.35
20	20
4	20

Figures 3.3 to 3.8 show the plots of I_{dsat} and V_{tsat} for p-MOSFET against n-MOSFET. Generally, it was observed that the simulated data did reflect the

measurement variation better than the 4 corner values even in cases whereby the center of the data cluster, probably due to process drift, had skewed from the typical value,. This problem of skewed data can be tackled quickly by applying an offset value to the process corner so as to shift the center of the typical/nominal value into the center of measurement data. Nevertheless, the important thing here is that the simulated data was falling within the process corners and it gave a tighter process variation that matched the data variation more realistically. Furthermore, it showed a realistic correlation of the p-MOSFET electrical performance with that of n-MOSFET.

Figure 3.3: Verification plot for I_{dsat} of thin gate n-/p-MOSFET with MOSFET channel width= $20\mu\text{m}$ and length= $0.35\mu\text{m}$.

Figure 3.4: Verification plot for V_{tsat} of thin gate n-/p-MOSFET with MOSFET channel width= $20\mu\text{m}$ and length= $0.35\mu\text{m}$.

Figure 3.5: Verification plot for I_{dsat} of thin gate n-/p-MOSFET with MOSFET channel width= $20\mu\text{m}$ and length= $20\mu\text{m}$.

Figure 3.6: Verification plot for V_{tsat} of thin gate n-/p-MOSFET with MOSFET channel width= $20\mu\text{m}$ and length= $20\mu\text{m}$.

Figure 3.7: Verification plot for I_{dsat} of thin gate n-/p-MOSFET with MOSFET channel width= $4\mu\text{m}$ and length= $20\mu\text{m}$.

Figure 3.8: Verification plot for V_{tsat} of thin gate n-/p-MOSFET with MOSFET channel width= $4\mu\text{m}$ and length= $20\mu\text{m}$.

Thick gate 5.0V n/p-MOSFET

The representations of different data in the thick gate 3.3V n-MOSFET and p-MOSFET verification plots are as follow:

- 'x' – Measured data (600+ data points)
- 'o' – Monte Carlo simulation of 3 sigma process variation (1000 data points)
- '◇' – Monte Carlo simulation of 2 sigma process variation (1000 data points)
- 'Δ' – Monte Carlo simulation of 1 sigma process variation (1000 data points)
- '■' – Process corners (center = typical/nominal, ss=slow-slow, sf=slow-fast, ff=fast-fast and fs=fast-slow)

MOSFET electrical parameters (I_{dsat} , V_{tsat}) were measured or simulated using the biasing conditions as in Table 3-5 with both source voltage (V_s) and substrate voltage (V_b) at 0V. The dimensions of the thick gate n/p-MOSFET that were used are given in Table 3-6.

Table 3-5: Electrical biasing conditions of the thick gate n/p-MOSFET electrical parameter measurement for statistical MOSFET modelling of global process variation. $V_s=0V$ & $V_b=0V$.

Data	Description
I_{dsat}	Value of drain current, I_d , when: Drain voltage, $V_d=5.5V$ Gate voltage, $V_g=5.5V$.
V_{tsat}	Value of gate voltage, V_g , when: Drain current, $I_d=0.1\mu A * W/L$, Drain voltage, $V_d=5.5V$.

Table 3-6: Device dimensions of thick gate n/p-MOSFET used for statistical MOSFET modelling of global process variation

Width/ μm	Length/ μm
20	0.35
20	20
4	20

Figures 3.9 to 3.12 show the plots of I_{dsat} and V_{tsat} for thick gate p-MOSFET against n-MOSFET. Similar behaviours as those for the thin-gate have been observed.

Figure 3.9: Verification plot for I_{dsat} of thick gate n-/p-MOSFET with MOSFET channel width= $20\mu\text{m}$ and length= $0.50\mu\text{m}$.

Figure 3.10: Verification plot for V_{tsat} of thick gate n-/p-MOSFET with MOSFET channel width= $20\mu\text{m}$ and length= $0.50\mu\text{m}$.

Figure 3.11: Verification plot for Idsat of thick gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=20 μ m.

Figure 3.12: Verification plot for Vtsat of thick gate n-/p-MOSFET with MOSFET channel width=20 μ m and length=20 μ m.

CHAPTER 4

MOSFET MISMATCH TEST STRUCTURE

MOSFET mismatch refers to the random variation in the electrical characteristics of identically designed MOSFETs with same device dimensions due to intra-die or local process variation. For MOSFET mismatch characterization and model, well-designed test structures are very important. This is in contrast to the SLM MOSFET test structures that were used for the MOSFET characterization for global process variation across the wafers as given in Chapter 3. The MOSFET mismatch test structures for this work would be discussed. Results were based on MOSFET devices fabricated using multi-wafer project (MPW) services of CSM 0.18 μ m, 0.13 μ m and 90nm (LP) CMOS process technologies.

4.1 IC Test Structures

There are generally two types of the electrical test structures for IC manufacturing [34]. The first one is the process control module (PCM), which refers to groups of electrical test structures that are used to ensure correct process recipes were run in the production line and to determine whether the fabricated devices of a production wafer are within performance specifications. In the old times, PCM was called drop-in PCM (Figure 4.1a) as it would replace product die and occupy the space. In recent times, PCM is placed along the SLM, which was discussed in chapter 3, and Figure 1b gives an example of SLM PCM [35]. This solves the problem of taking valuable wafer real estate with drop-in PCM.

The other type of test structure group is the process evaluation module (PEM), which is used during the development of process flow for new technology. PEM is used for optimization of process recipes and devices' architectures, determining the layout design rules as well as for device model parameter extraction for devices. Figure 4.1c shows an example of what PEM looks like.

However, for this work, the designed MOSFET mismatch test structure is not placed in PCM nor PEM but in MPW of CSM. For CSM, MPW is tape-out service that is being carried out regularly for CSM's potential customers to test out their IC prototypes before any decision on ramping IC production can be made. For this work, MPW is a good choice as it is usually processed very fast and compared to PCM and PEM, there is more space to prototype test structure designs.

Figure 4.1: PCM and PEM test structures [34].

4.2 MOSFET Mismatch Test Structure Design

4.2.1 MOSFET mismatch test structure considerations

Simple Pair or array design

For MOSFET mismatch test structure, there are generally two types of designs [34, 36]. The first design is the simple MOSFET matched pair design using traditional 2xN or 1xM pad module as shown in Figure 4.2b and 4.2c, respectively. The other design, which is of growing interest, is the more complicated array design with rows and columns of individually accessible MOSFET matched pair [37-40]. There are also test structures that are designed to negate the impact of the spatial parametric gradient [41]. These designs could arguably be ignored since the MOSFET in matched pair are very close together and intrinsic MOSFET mismatch should be largely unaffected unless the MOSFET concerned is very big.

Figure 4.2: Different possible mismatch test structure designs. (a) Array design. (b) & (c) Simple matched pair design using 2xN and 1xM pad module respectively.

For this work, the design would be based on Figure 4.2b and 4.2c. One main reason for the choice is that it is simple to layout. In addition, it facilitates MOSFET mismatch characterisation by using standard module that can be used with a commonly available probe card for automated device characterisation. By having the MOSFET matched pair to be designed very closely with simple layout, it allows the proper study of the random nature of intrinsic MOSFET mismatch behaviour, without any significant extrinsic influences due to spatial parametric gradient and adjacent layout effects. However, compared to the array design, the simple pair design using 2xN or 1xM pad module takes up too much wasteful space for the pad alone. Furthermore, it can be argued that array design is more realistic as a test structure to study mismatch since it can emulate the dense packing and adjacent layout of an IC chip.

CS&CG configurations

After deciding on the simple matched pair design, the next step is to decide on how to layout the MOSFET matched pair and how to utilize the module's pads. In order to fully maximize the space provided by the pad module, the common source and common gate (CS&CG) configuration is used for the 2xN pad module [34]. Figure 4.3 shows a schematic of the CS&CG layout design for the MOSFET mismatch test structure using 2xN pad module. The MOSFET matched pairs in the module are all orientated in such a way so that the drain currents all flow in the same direction. In this way, any doubt on how the drain current direction flow along the Si crystalline plane that may affect MOSFET mismatch is dispelled. The layout is also designed to have symmetrical surrounding for both MOSFETs in the MOSFET matched pair. The obvious reason for doing so is to prevent the

difference in routing that can contribute to the intrinsic MOSFET mismatch. Another reason is to eliminate any subtle effect due to adjacent layout that can affect MOSFET mismatch.

Nevertheless, problems exist with CS&CG and one is the leakage current from gate to source that anyone of the MOSFETs in the test structure may affect the MOSFET mismatch characterization accuracy of other devices in the same module since probe card is used. Because of this, CSCG was not used to design MOSFET mismatch test structure for CSM 90nm LP technologies that have very thin gate oxide. Furthermore, the MOSFET mismatch in gate current cannot be characterized for this configuration if there is the need.

Figure 4.3: CS&CG configuration for MOSFET matched pair test structure [34].

To tackle the shortcomings of CS&CG configuration, MOSFET mismatch test structure based on Figure 4.4 is strongly recommended. This is because only the source is shared while the gate and drain are independent for the two MOSFETs in the MOSFET matched pair. MOSFET mismatch characterization for both the drain and gate current, especially for advanced technologies with thinner gate oxide, can be done. Furthermore, by using 1xM module, the test structure can be inserted into

the SLM not only for saving space but also future MOSFET mismatch monitoring through SLM PCM of production wafer.

Figure 4.4: Recommend MOSFET mismatch test structure with common source (CS) and individual gate and drain pads for each MOSFET, especially for advanced technology with thinner gate oxide [34].

Probe pad & probe card

Great attention has to be paid on the probe pad for designing of the test structures for any statistical characterization. This is because automated device characterization would very likely be carried out and hence, there must be excellent compatibility between the chosen or available probe card and the probe pad design specifications in the 2xN or 1xM module. Inaccurate MOSFET mismatch characterization data would result if there is any compatibility discrepancy between probe card and module. Figure 4.5 shows an example of poor contact of the probe card on the module's pads of the 2XN module.

Figure 4.5: Poor contact between probe card and module's pads [34].

Hence, it is advisable to design the probe pads as big as possible so as to increase the tolerance for any misalignment due to the cumulative stepping error as the automated measurement setup probe from one module to another across the whole

wafer. Furthermore, repeat or multiple characterizations may be required and this would deteriorate the condition of the probe pad as shown in Figure 6. Thus if probe pad is too small, there may not be any available good ‘spot’ left for probing if verification is needed in future.

Figure 4.6: Conditions of probe pad under repeat or multiple characterisations [34].

MOSFET mismatch test structure geometry matrix

For this work, besides MOSFET mismatch characterization, the MOSFET mismatch test structure is to be used for the extraction of statistical model parameters for MOSFET mismatch modelling. Thus, in order for the MOSFET mismatch model to be scalable for all MOSFET sizes, the geometry matrix for the MOSFET mismatch test structure becomes very important.

Table 4-1: Geometry matrix for MOSFET mismatch test structure design [34].

	W=40	W=10	W=4	W=2	W=1	W=0.5	W=0.25
L=40	$X^{1,3,4,7}$						
L=10		$X^{1,2,3,4,5,7,8a}$		$X^{3,4,5,8a}$	$X^{3,5}$	X^5	$X^{5,6,8b}$
L=4		$X^{1,3,4,5,8a}$	$X^{3,7,8a}$				X^6
L=2		$X^{3,5,8a}$		$X^{3,7,8a}$			
L=1		$X^{1,3,5}$			$X^{7,9}$		
L=0.5		$X^{1,3,5}$				X^7	
L=0.25		$X^{3,6,8b}$	X^6	$X^{1,9}$	X^1	X^1	$X^{1,2,7,8b,9}$
L=0.2		X^3					

Table 4-1 shows an example of a geometry matrix for a 0.25 μ m technology MOSFET mismatch test structure. Each 'X' in the table represents the inclusion of that MOSFET size with length and width, in microns, indicated by left column and top row, respectively. The superscripts for each 'X' in Table 4-1 are justifications for its inclusion and they are given in Table 4-2.

Table 4-2: Reasons for the choice of MOSFET sizes in the geometry matrix [34].

subscript	explanation
1	to spread out the MOSFET geometries based on the $1/\sqrt{(W*L)}$ scale
2	to cover both extreme of the MOSFET geometry so that the local variation fitting constant, A_1 can be extracted
3	to cater for analog circuits that typically use MOSFET more than 2x the minimum MOSFET size for higher output resistance and less mismatch
4	to cater for high precision analog circuits that use very big MOSFET for good matching
5	to study the dependence of mismatch on length and width
6	to study the impact of W/L ratio on the mismatch of MOSFET with same area
7	to allow accurate MOSFET mismatch characterisation that is less susceptible to the different offset levels and noise contributions of meters and sources
8	to provide critical MOSFET sizes to be characterised when time is limited for lengthy mismatch (8a) and to cater for high performance digital circuit that uses minimum channel length MOSFET
9	to provide MOSFET sizes for PCM recommendation on MOSFET mismatch monitoring

4.2.2 MOSFET matched pair test structure design

CSM 0.18 μm & 0.13 μm

The MOSFET mismatch test structures for both CSM 0.18 μm and 0.13 μm technologies are very similar. Figure 4.7 summaries the keys details of their MOSFET mismatch test structures. Figure 4.7a shows the pad number in bracket for each pad and the corresponding MOSFET terminal connection by a single letter acronyms, bulk (substrate) by 'B', well by 'W', gate by 'G', source by 'S' and drain by 'D' with subscript to indicate matched pair number and location left (L) or right (R) MOSFET.

Figure 4.7: Details of the MOSFET mismatch test structures for the CSM 0.18 μm and 0.13 μm technologies. (a) Pad Assignments. (b) Probe pad dimensions. (c) Module layout for 10 similar MOSFET pairs. (d) MOSFET matched pair layout design (zoom-in of c.).

Figure 4.7b shows the dimensions of the 2x12 module and its pads. The pad size is shown to be $100\mu\text{m}$ and can be considered very big. It provides better assurance for good contact between the pads and the probe card, the tradeoff is the space consumed. The lateral separation is fixed at $140\mu\text{m}$ so as to fit in a large range of MOSFET sizes that is dictated by the geometry matrix. This also depends on the availability of the compatible probe card. Figure 4.7c shows the complete layout design of the MOSFET mismatch test structure in a 2x25 module with 10 matched pairs for a single MOSFET size. Figure 4.7d, is the zoom-in on one matched pair layout of Figure 4.7c, with the emphasis on the symmetry of the design around the MOSFET matched pair.

The geometry matrices for the MOSFET mismatch test structures of CSM $0.18\mu\text{m}$ and $0.13\mu\text{m}$ technologies are shown in Table 4-3 and Table 4-4, respectively. For CSM $0.18\mu\text{m}$ and $0.13\mu\text{m}$ technology, a total of 26 and 22 different MOSFET sizes were designed respectively for the reasons discussed in Table 4-2. Nevertheless, the range of MOSFET sizes for each technology is different as it is largely determined by the layout design rule of that particular technology.

Table 4-3: Geometry matrix for MOSFET mismatch test structure using CSM 0.18 μ m CMOS technology.

		W	W	W	W	W	W	W	W
		57.6	14.4	5.76	2.88	1.44	0.72	0.36	0.22
L	57.6	26							
L	14.4		25	18	15	12	9	6	3
L	5.76		24	17					2
L	2.88		23		14				
L	1.44		22			11			
L	0.72		21				8		
L	0.36		20					5	
L	0.22								1
L	0.18		19	16	13	10	7	4	

Table 4-4: Geometry matrix for MOSFET mismatch test structure using CSM 0.13 μ m CMOS technology.

		W	W	W	W	W	W	W	W
		41.60	10.40	4.16	2.08	1.04	0.52	0.26	0.15
L	41.60	22							
L	10.40		21	14		10			4
L	4.16		20	13					3
L	2.08		19		11				
L	1.04		18			9			2
L	0.52		17				7		
L	0.26		16					6	
L	0.15								1
L	0.13		15	12		8		5	

CSM 90nm LP technology

For CSM 90nm LP technology, the MOSFET mismatch test structure design is very much different from that of the CSM 0.18 μ m and 0.13 μ m technologies. The most obvious difference is the module used, 1x25 module is used instead of the 2x12 module. Furthermore, the CS&CG configuration for the MOSFET matched pair design is not used but instead the design is based on Figure 4.4.

D1L	W1	G1L	G1R	S1	D1R	D2L	W2	G2L	G2R	S2	D2R	D3L	W3	G3L	G3R	S3	D3R	D4L	W4	G4L	G4R	S4	D4R	(25)
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	(22)	(23)	(24)	(25)

a. Pad Assignments

b. Probe Pad Dimensions

c. MOSFET mismatch test structure layout design using 1x25 pad module containing four matched pairs.

d. Standard MOSFET pair layout design (zoom-in of c.)

Figure 4.8: Keys details of the MOSFET mismatch test structure for CSM 90nm LP technology. (a) Pad Assignments. (b) Probe Pad Dimensions. (c) MOSFET mismatch test structure layout design using 1x25 pad module containing four matched pairs. (d) Standard MOSFET pair layout design (zoom-in of c.)

Figure 4.8a shows the pad numbers in brackets as well as the labels of MOSFET terminals to which the pads are attached. The first letter in the label stands for the acronym of the MOSFET terminal, with ‘D’ for drain, ‘W’ for well/bulk/substrate, ‘G’ for gate, and ‘S’ for source. The rest of the label is on the information of the MOSFET matched pair number as well as the left or right MOSFET terminal. Pad

number 25 is unused as only 24 pads are needed. Figure 4.8b provides the module dimension specifications, it can be observed that the pad is much smaller in size as compared to that used for CSM 0.18/0.13 μm technologies. This allows great saving in space but special care was needed during the alignment of probe card to the module for MOSFET mismatch characterization. For each 1x25 module, there are 4 MOSFET matched pairs as shown in Figure 8c and thus this number is much less than the 10 matched pairs for CSM 0.18/0.13 μm wafers. Figure 4.8d is a zoom-in of a matched pair in Figure 4.8c and it shows the layout design being symmetrical.

In the geometry matrix for CSM 90nm LP MOSFET mismatch test structure, which is shown in Table 4-5, there are 22 different MOSFET sizes. Again, they were chosen based on the guidelines given in Table 4-2 as well as the layout design rules. The number is less than that of 0.18/0.13 μm and is largely determined by the available space on the MPW mask.

Table 4-5: Geometry matrix for MOSFET mismatch test structure using CSM 90nm CMOS technology

		W	W	W	W	W	W	W	W
		12.50	7.20	2.88	1.44	0.72	0.36	0.18	0.12
L	12.50	22							
L	7.20		21	14		10			4
L	2.88		20	13					3
L	1.44		19		11				
L	0.72		18			9			2
L	0.36		17				7		
L	0.18		16					6	
L	0.12								
L	0.10		15	12		8		5	1

4.2.3 MOSFET Mismatch Characterization

In order to negate the impact of drift in ambient temperature [42] and equipment accuracy, special care was needed during the characterization of the MOSFET mismatch test structure [34]. Furthermore, the time taken for MOSFET mismatch characterization would also be a big consideration as it would be a challenge to achieve enough statistical data efficiently and effectively in a limited time period.

For CSM 0.18/0.13 μ m technologies, the MOSFET mismatch test structure characterization was carried out first on the left MOSFET before moving on to the right MOSFET of a MOSFET matched pair. The same would be done for the other matched pairs of the same MOSFET size before moving on to the next MOSFET of different size.

Table 4-6 gives the details of the three electrical tests that were measured for each MOSFET, with two of them being drain current vs. gate voltage (I_d - V_g) sweeps with drain voltage (V_d) fixed at 0.1V (lin) & V_{DD} (sat). The other being drain current vs. drain voltage (I_d - V_d) sweep with V_g fixed at 0.1V. The time taken to complete mismatch characterization for one MOSFET is given as well for different technologies. Thus to finish all the 26/22 modules per die for 0.18/0.13 μ m CMOS technologies, a total time of ~ 1.7 and ~ 1.2 hours were needed, respectively. Similar MOSFET mismatch characterization is carried out for CSM 90nm (LP) except that there are only 4 matched pairs per module. The time needed to finish all the 22 modules per die was ~ 0.5 hours, which is much faster. However, there would be more dice per wafer on 300mm wafer is used as compared to 200mm for wafer for the 0.18/0.13 μ m CMOS technologies.

Table 4-6: Details of MOSFET mismatch charactersaition for CSM 0.18 μ m, 0.13 μ m and 90nm (LP) technologies. *: VDD=1.8, 1.2 & 1.2V respectively for the three technologies.

sweep	bias	time taken (s) per device		
		0.18 μ m	0.13 μ m	90nm (LP)
Id-V _g (lin)	V _d =0.1V V _g =0.1 to VDD* @ 0.05V step V _s & V _b =0V	~12	~10	~10
Id-V _g (sat)	V _d =1.2V V _g =0.1 to VDD* @ 0.05V step V _s & V _b =0V			
Id-V _d	V _g =0.1V V _d =1/2VDD* @ 0.1V step V _s & V _b =0V			

4.3 Factors Affecting MOSFET Mismatch

As MOSFET mismatch characteristic is believed to be easily affected by its adjacent layout [39, 43] and various subtle process details [44-46]. The focus of this section would be on the study of various factors that may affect the MOSFET mismatch in electrical performance. Threshold voltage mismatch would be used as the Figure-Of-Merit (FOM) to characterize and quantify the MOSFET mismatch characteristics and the simplified Pelgrom model [54] is applied. Equation 4.1 establishes a linear relationship between the standard deviation in threshold voltage and the inverse of the square root of channel area. The threshold voltage mismatch constant (A_{vt}) of the model provides a measure of mismatch performance.

$$\sigma_{\Delta V_t} = \frac{A_{vt}}{\sqrt{WL}} \quad (4.1)$$

The threshold voltage, extracted based on constant-current criterion defined as $0.1\mu\text{A} \times W/L$, is acquired from I_d - V_g curve with drain-source voltage (V_{ds}) fixed at 0.1V. This threshold voltage is referred to as V_{tlin} here. The mismatch in V_{tlin} for the neighbouring MOSFETs in the symmetrical MOSFET matched pair test structure is the difference of their extracted V_{tlin} values.

Effect of BEOL

Typically, the effect of backend of line (BEOL) processing and routing on MOSFET mismatch characteristics is assumed to be negligible and the mismatch test structure would usually go through the full BEOL processing of the particular technology. It is possible that BEOL processing and routing can aggravate the

MOSFET mismatch characteristics. Furthermore, MOSFETs that require good matching would not be exposed for full BEOL processing since only local interconnects, such as polysilicon and the first layer metal only would be used for routing.

In order to study the impact of multilevel metallization BEOL processing on MOSFET mismatch, two split run were processed during the fabrication of the CSM 0.18 μm MOSFET mismatch test structure. One split allowed the full process flow CSM 0.18 μm technology to be run, which meant that the finished wafer would have the 6 complete Al metal layers. The other split would be stopped after the first metal layer. The MOSFET geometries that were being characterized include: L/W ($\mu\text{m}/\mu\text{m}$) = 0.22/0.22, 0.18/14.4, 14.4/0.22, 14.4/14.4, and 57.6/57.6. Both n and p-MOSFET mismatch test structures were characterised for this study and the results are shown in Fig. 4.9.

Figure 4.9: Pelgrom plot to study impact of BEOL on V_{tlin} mismatch for n and p-MOSFET.

From the Pelgrom plots in Figure 4.9, it is observed that BEOL introduced a difference of ~ 0.04 and ~ 0.25 in the mismatch constant, A_{vt} , for n and p-

MOSFET's V_{th} mismatch, respectively. In the case of n-MOSFET, BEOL caused a slight improvement in V_{th} mismatch by reduction of $\sim 0.6\%$ in A_{vt} , while for p-MOSFET, BEOL caused a significant worse V_{th} mismatch by increment of $\sim 5.6\%$ in A_{vt} . These results suggested that BEOL may have an effect on the MOSFET mismatch characteristics. It appears to have a negative effect especially for p-MOSFET. For n-MOSFET, the effect is negligible and the small difference ($\sim 0.6\%$) may be due to unaccounted measurement setup drift.

Effect of multi-fingered layout on MOSFET mismatch [39, 47]

The use of large MOSFETs with wide channel length is very common in analog/RF circuits. In order to minimize the impact of parasitic gate resistance and capacitance, multi-fingered layout is commonly used. It would be useful to study the mismatch characteristics in these multi-fingered MOSFETs.

In the study of multi-fingered layout effect on MOSFET threshold voltage mismatch, CSM 0.13 μm and 90nm CMOS (LP) technologies were employed. The basis of symmetrical layout of MOSFET matched pair discussed earlier was strictly adopted and the designs for 0.13 μm and 90nm devices are shown in Figures 4-10/11 and Figures 4-11/12, respectively. For 0.13 μm CMOS technology, 2 $\times$ 12 probe pad module was used with CG&CS configuration was employed, allowing 10 pairs of matched MOSFET devices in a single module. Both n- and p-MOSFETs were fabricated for this study. For 90-nm CMOS technology, 1 $\times$ 25 probe pad modules with CS configuration was employed for n-MOSFET devices only. This allows 4 MOSFET matched pairs in a single module.

Each finger in the multi-fingered MOSFETs was fixed in channel width and the total channel width was determined by the number of fingers (2, 4 or 8). Single or non-fingered large MOSFET was used as a control device. Both interleaving and non-interleaving multi-finger MOSFET pairs were designed and characterized. Shared source and drain terminals were used for multi-fingered MOSFET layout and dummy poly-gates were included at the outermost of the layout to prevent poly-gate length variation for isolation structures at gate polishing steps. As shown in Table 4-7, the dimensions for the single-, 2-, 4-, and 8-finger that were being characterized include: L/W ($\mu\text{m}/\mu\text{m}$) = 0.13/10.4 ($n=1$), 0.13/5.2 ($n=2$), 0.13/2.6 ($n=4$), and 0.13/1.3 ($n=8$) for 0.13- μm technology while for 90-nm technology, L/W ($\mu\text{m}/\mu\text{m}$) = 0.1/7.2 ($n=1$), 0.1/3.6 ($n=2$), 0.1/1.8 ($n=4$), and 0.1/0.9 ($n=8$). The total channel area, A_{ch} , is fixed for all the MOSFETs in the study.

$$A_{ch} = LW = L \times nW_f .$$

Table 4-7: No. of fingers and the corresponding finger widths that were used in the design of multi-fingered layout MOSFET using 0.13 μm and 90nm CMOS technology, with fixed channel length of 0.13 μm and 0.1 μm respectively..

No. of fingers, n.	Finger width, W_f (μm)	
	0.13 μm	90nm
1	10.4	7.2
2	5.2	3.6
4	2.6	1.8
8	1.3	0.9

Figure 4.10: Layout design of 0.13μm MOSFET pair that is used to study the effect of non-interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch.
Total channel width: 10.4μm. No. of fingers: 8.

Figure 4.11: Layout design of 0.13μm MOSFET pair that is used to study the effect of interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch.
Total channel width: 10.4μm. No. of fingers: 8.

Figure 4.12: Layout design of 90nm (LP) MOSFET pair that is used to study the effect of non-interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch.
Total channel width: $7.2\mu\text{m}$. No. of fingers: 2.

Figure 4.13: Layout design of 90nm (LP) MOSFET matched pair that is used to study the effect of interleaving multi-fingered MOSFET on intrinsic MOSFET mismatch.
Total channel width: $7.2\mu\text{m}$. No. of fingers: 2.

Plots of $\sigma_{\Delta V_{tlin}}$ (standard deviation of V_{tlin}) and $\mu_{V_{tlin}}$ (mean value of V_{tlin}) vs. number of fingers for characterisation results of test structures with non-fingered, interleaved and non-interleaved layout design for both 0.13 μ m n- and p-MOSFETs are plotted in Figure 4.14 and 4.15. For each device type and finger number, 864 devices were characterized.

Figure 4.14: $\sigma_{\Delta V_{tlin}}$ vs. no. of fingers, for both n- and p-MOSFETs using 0.13- μ m technology to study the impact of multi-fingered layout on MOSFET threshold voltage mismatch characterisation. The length and width of finger size is indicated below the data point as L/W (μ m / μ m).

Figure 4.15: $\text{abs}(\mu_{V_{tlin}})$ vs. no. of fingers, for both n- and p-MOSFETs using 0.13- μ m technology to study the impact of multi-fingered layout on MOSFET threshold voltage mismatch characterisation. The length and width of finger size is indicated below the data point as L/W (μ m / μ m).

For n-MOSFETs using 0.13- μm technology, it is observed that multi-fingered MOSFET layouts, both interleaved and non-interleaved, had better the threshold voltage mismatch than non-fingered n-MOSFETs of equivalent channel area, except for MOSFET size of 0.13/5.2 ($n=2$), where the threshold voltage mismatch for multi-fingered layout relative to non-fingered layout is larger by ~ 1 mV. At the same time, $\sigma_{\Delta V_{\text{tlin}}}$ for non-interleaved of different finger sizes always performs better than its interleaved counterparts.

For p-MOSFETs using 0.13- μm technology, it is observed that multi-fingered MOSFET layouts, both interleaved and non-interleaved, had better threshold voltage mismatch than non-fingered p-MOSFETs of equivalent channel area. Multi-fingered MOSFET layouts of sizes of 0.13/5.2 ($n=2$) and 0.13/2.6 ($n=4$), both interleaved and non-interleaved, had the best threshold voltage mismatch than the MOSFET with more fingers having size of 0.13/1.3 ($n=8$). The $\sigma_{\Delta V_{\text{tlin}}}$ values for both interleaved and non-interleaved matched one another quite closely, though it was observed the former was always slightly better than the latter. For both n/p-MOSFET using 0.13- μm CMOS technology, the effect of reverse narrow width effect on the $\mu_{V_{\text{tlin}}}$ can be observed in Figure 4.15, for MOSFETs with decreasing channel width or more fingers. On the other hand, the opposite trend was observed for $\sigma_{\Delta V_{\text{tlin}}}$ for both MOSFET types. There seemed to be two competing effects, the narrow channel width effect and the STI stress effect influencing the $\sigma_{\Delta V_{\text{tlin}}}$ values for multi-fingered MOSFETs.

Figure 4.16: $\sigma_{\Delta nV_{tlin}}$ & $\mu_{nV_{tlin}}$ vs. No. of fingers for n-MOSFETs using 90-nm technology to study the impact of multi-fingered layout on MOSFET threshold voltage mismatch characterisation. The length and width of finger size is indicated below the data point as L/W ($\mu\text{m}/\mu\text{m}$).

For n-MOSFETs using 90-nm technology, totally 680 devices having the same channel area ($A_{ch} = L \times nW_f$) were characterized for different finger types and channel widths. Figure 4.16 shows the variations of $\sigma_{\Delta nV_{tlin}}$ and $\mu_{nV_{tlin}}$ with number of fingers for characterisation results of test structures with single, interleaved and non-interleaved multi-fingered layout designs. It is observed that in multi-fingered layouts, both interleaved and non-interleaved, had better threshold voltage mismatch than non-fingered (single channel) n-MOSFETs of equivalent channel area. Multi-fingered layouts of $0.1\mu\text{m}/1.8\mu\text{m}$ ($n=4$), both interleaved and non-interleaved, have the smallest $\sigma_{\Delta nV_{tlin}}$ values. The $\sigma_{\Delta nV_{tlin}}$ value for interleaved multi-fingered layout of $0.1\mu\text{m}/3.6\mu\text{m}$ ($n=2$) was better than that of its non-interleaved counterpart while for other finger numbers, it was the opposite. Similar to $0.13\mu\text{m}$ CMOS technology, the reverse narrow width effect on $\mu_{nV_{tlin}}$ was observed though it seemed to become less dominant as finger size increased towards $0.1\mu\text{m}/0.9\mu\text{m}$.

($n=8$). This could probably be due to the STI stress effect becoming dominant at lower $\mu_{V_{th}}$ with narrower channel width.

Effect of gate protection diode

As MOSFET scales towards the deep-submicron size, the gate oxide becomes thinner and thinner. This thinner gate oxide arguably makes it susceptible to plasma charging damage (PCD) during some plasma processing steps and thus degradation of gate oxide integrity may occur [48, 49]. PCD can be considered as a random event and it may affect the MOSFET mismatch characteristics for advanced process technology using very thin gate oxide.

Figure 4.17: Layout design of MOSFET pair that is used to study the impact of gate protection diode on intrinsic MOSFET mismatch.

In order to study the potential effect of PCD on MOSFET mismatch, n-MOSFET pairs are designed with and without gate protection diode (GPD). Figure 4.17 shows an example of the n-MOSFET matched pair with PCD. The CSM 90-nm

(LP) technology with gate oxide thickness of 21Å was used for this study. Modules of 1×25 pads were used and common-source (CS) configuration was employed. There were 4 MOSFET matched pairs in a single module. The MOSFET dimensions that were being characterized in this study were: L/W (μm/μm) = 0.1/0.12, 0.1/7.2, 0.72/7.2, 7.2/0.12, 7.2/7.2 and 12.5/12.5.

In the study of GPD effect on MOSFET mismatch, Pelgrom plots for the standard deviation of MOSFET device test structures with and without gate protection diode are plotted against the channel area for n-MOSFETs as shown in in Figure 4.18. It is observed n-MOSFET threshold voltage mismatch performance is better for test structures without GPD. The threshold voltage mismatch constant A_{vt} was found to have a difference of ~1 mV-μm for these two types of MOSFETs with or without PCD. This result contradicts the purpose of including GPD for protecting the thin gate oxide if match devices should be used [48, 49].

Figure 4.18: Pelgrom plot of n-MOSFETs V_{tlin} using 90-nm technology. This is to study the impact of gate protection diode on MOSFET threshold voltage mismatch. Filled symbols represent data 'without GDP' while unfilled symbols represent data 'with GPD'. Length (L) and width (W) in the legend are in μm.

A straight forward explanation would be that GPD does not enhance MOSFET threshold voltage mismatch but worsens it. It is also possible that the GPD was effective in plasma charging damage (PCD) protection for only one of the MOSFETs in the MOSFET-pair test structure. Hence, it results in a worse threshold voltage mismatch characteristics. Further studies are required to investigate the effectiveness of GPD with respect to its size and the distance from the MOSFET to be protected from PCD. Last but not least, PCD may not be as serious as initially thought for gate oxide thickness of 21Å [48].

CHAPTER 5

MOSFET MISMATCH MODELING USING BPV METHODOLOGY

In this chapter, the development of a MOSFET mismatch model for CSM 0.13 μ m technology using BPV methodology will be discussed. The MOSFET characterization data obtained in Chapter 4 would be used to extract the MOSFET mismatch targets by the BPV methodology. The developed MOSFET mismatch model will then be used to perform Monte Carlo based statistical circuit simulation.

5.1 Developments of MOSFET Mismatch Modelling

MOSFET mismatch has become an increasing concern as scaling of MOSFET continues. Effects such as random dopant fluctuation (RDF) [50-52], line edge and width roughness (LER/LWR), surface roughness of channel-oxide interface, and random oxide trapped charges start to play a significant role in affecting intrinsic MOSFET mismatch performance [53].

In 1989, Pelgrom et al [54] addressed the MOSFET mismatch issues by deriving an analytical MOSFET mismatch model that established the relationship between the MOSFET geometry and its mismatch in threshold voltage and current factor. Since then this work had been the most referenced work on MOSFET mismatch modeling and a lot of relevant works had been published [40, 55-57]. However, all these models suffer from the same problem of being derived based on a simple MOSFET current expression that cannot address second order electrical characteristics of deep sub-micron MOSFET using advanced process technology.

Furthermore, mismatch in threshold voltage and current factor are not appropriate independent physical parameters to model MOSFET mismatch [58, 59]. Drennan et al [30, 59] tackled this problem by using BPV methodology coupled with Pelgrom model's basis to develop a MOSFET mismatch model that was based on advanced MOSFET compact model with physical parameters for electrical characteristics of deep submicron MOSFET. This approach is practical and useful as the developed MOSFET mismatch model can be used seamlessly with circuit simulator to perform statistical circuit simulation. Furthermore, it can be much more accurate in MOSFET mismatch simulation because BPV methodology uses mismatch characterization data to solve for the random variation in physical MOSFET model parameters. Thus, in this work, the BPV approach would be the basis of developing a MOSFET mismatch model.

As BSIM3v3 is the industry standard MOSFET compact model for circuit simulation and in this work, BSIM3v3 will be used as the advanced compact MOSFET model to develop the MOSFET mismatch model using BPV approach. HSPICE, a circuit simulator widely used in industry, will then be used with the developed MOSFET mismatch model to perform Monte Carlo MOSFET matched pair simulation so as to generate simulated MOSFET mismatch data for verification against that of the MOSFET mismatch test structure characterization done in chapter 4.

5.2 MOSFET Mismatch Characterization

5.2.1 CSM 0.13 μ m process technology

The MOSFET to be discussed in this section was manufactured using CSM 0.13 μ m technology. CSM offers three different MOSFET variants for its 0.13 μ m technology. They are the nominal, high performance (HP) and low power (LP) MOSFET as shown in Figure 5.1. For this work, only the nominal MOSFET would be studied but the same approach can be applied to the HP and LP MOSFETs.

Figure 5.1: Different MOSFET variants offer by CSM 0.13 μ m process technology.

Electrical specifications

For the CSM 0.13 μ m nominal MOSFET, there are two classifications. They are the core and the I/O MOSFET. For the core MOSFET, it has gate oxide thickness of 20Å and the nominal supply voltage (VDD) is 1.2V. As for the I/O MOSFET, there are three different possibilities and possible gate oxide thicknesses are 32Å, 45Å and 65Å for VDD of 1.8V, 2.5V and 3.3V, respectively. The physical gate length of the core MOSFET is 0.12 μ m. The threshold voltage (V_t) of the core n- and p-MOSFET are 0.34V and 0.36V, respectively. The drive current (I_{dsat})

would be $535\mu\text{A}/\mu\text{m}$ and $236\mu\text{A}/\mu\text{m}$, while the off current (I_{doff}) would be $0.35\text{nA}/\mu\text{m}$ and $1.0\text{nA}/\mu\text{m}$ for the n- and p-MOSFET, respectively. The key electrical characteristics for all of CSM $0.13\mu\text{m}$ MOSFET variants are shown in Table 5-1.

Table 5-1: Electrical characteristics of CSM $0.13\mu\text{m}$ MOSFET variants.

TRANSISTOR VERSION	NOMINAL	LOW VOLTAGE	HIGH PERFORMANCE	LOW POWER
VDD (V) CORE/IO	1.2/3.3, 2.5, 1.8	1.0/3.3, 2.5	1.2/3.3, 2.5	1.5/3.3, 2.5
PHY LGATE (μm) CORE	0.12	0.08	0.08	0.12
PHY TOX (Å) CORE/IO	20/65, 45, 32	17/65, 45	17/65, 45	26/65, 45
VT_N/P (V) CORE	0.34/0.36	0.23/0.26	0.23/0.26	0.53/0.56
IDSAT_N/P ($\mu\text{A}/\mu\text{m}$) CORE	535/236	580/270	850/380	520/220
IOFF_N/P (nA/ μm TYP, MAX) CORE	0.35, 1.0	10, 100	15, 150	0.005/0.002, 0.01

FEOL and BEOL process details

The CSM $0.13\mu\text{m}$ technology uses shallow trench isolation (STI) technology for device isolation. Cobalt salicidation is used to reduce the source, drain and gate resistance of the MOSFET. Poly half-pitch size of $0.155\mu\text{m}$ is achieved by using deep ultra-violet (DUV) lithography of 193nm wavelength with attenuated phase shift mask. For the MOSFET channel, lightly doped drain (LDD) and pocket/halo implants are used to alleviate reliability issue due to hot carrier injections and threshold voltage roll-off (V_t roll-off) due to short channel effects.

For BEOL, the metallization step uses copper (Cu) metal as the interconnect and processed by dual damascene technology. The number of metal layers possible is 8. The inter-metal dielectric (IMD) used is F-TEOS. Additional process details and electrical specifications of CSM $0.13\mu\text{m}$ technology are shown in Table 5-2.

Table 5-2: Electrical and process characteristics of CSM 0.13um MOSFET.

0.13um PROCESS FEATURE	KEY CHARACTERISTICS	GATE DIELECTRIC	
CORE VOLTAGE	1.0V, 1.2V, 1.5V	1.0V THIN GATE OXIDE	17Å
IO VOLTAGE	2.5V (3.3V TOLERANT)	1.2V THIN GATE OXIDE	20Å
3.3V (5.0V TOLERANT)		1.5V THIN GATE OXIDE	26Å
RING OSCILLATOR DELAY		1.8V THICK GATE OXIDE	32Å
NOMINAL	19 ps/STAGE	2.5V THICK GATE OXIDE	45Å
HIGH PERFORMANCE	11 ps/STAGE	3.3V THICK GATE OXIDE	65Å
LOW VOLTAGE	14 ps/STAGE	LITHOGRAPHY	DUV for all layers (except Dual Voltage Mask), with 10 Attenuated phase shift masks and 12 OPC layers
LOW POWER	25 ps/STAGE	ISOLATION	Shallow Trench
TRANSISTOR PHYSICAL GATE LENGTH		GATE	Surface-Channel N & PMOS Source/Drain Extensions with Pocket-Implant
NOMINAL	0.12um	SALICIDATION	Cobalt Silicide with Salicide-Block Available
LOW VOLTAGE & HIGH PERFORMANCE	0.08um	METAL INTERCONNECT	8 Layers Dual-Damascene CU
LOW POWER	0.12um	METAL PITCHES (CONTACTED)	M1: 0.34um, M2 - 7: 0.41um, TOP METAL: 0.90um
POLY HALF PITCH		CONTACT SIZE, VIA SIZE	Contact: 0.16um, VIA: 0.19um, TOP VIA: 0.96um
NOMINAL LOW VOLTAGE	0.155um	INTERMETAL DIELECTRIC	F-TEOS
HIGH PERFORMANCE & LOW POWER		MASKING LAYERS	33
6T SRAM CELL SIZE	2.43um ² , 2.28um ² 2.14um ² , 2.57um ²	QUALIFIED PLUG-IN MODULES	High-Q Spiral Inductors, MIM Capacitors, MOS & PN Varactors, Resistors, Deep N-Well, Metal Fuse
GATE DENSITY	220 K GATES PER mm ² (Application Dependent)		

5.2.2 MOSFET mismatch test structure and measurement setup

MOSFET mismatch test structure

As discussed in chapter 4, CSM 0.13 μ m MOSFET mismatch test structure was designed with CS&CG configuration. The pad module used is made up of 2x12 pads and it has 10 MOSFET matched pairs to be measured by the probe card automatically. This is an important consideration to maximize the usage of valuable wafer real estate and enhance efficiency of MOSFET mismatch characterization. 22 different MOSFET sizes were designed for the geometry matrix.

Measurement setup

The MOSFET mismatch characterization setup used in this work is semi-automatic and it is made up of an 8" wafer probe station, a switching matrix, a semiconductor parametric analyzer and a PC that operates the entire setup. Figure 5-2 shows a schematic of the setup.

Figure 5.2: Schematic of the semi-auto measurement setup

Software

Two programs, which are installed in the PC of the measurement setup in Figure 5.2, are required to run the MOSFET mismatch characterization automatically. They are NUCLEUS and SAGITTARIUS. The NUCLEUS software is used mainly to control the probe station movement. It allows the alignment of the wafer that has already been loaded manually on the probe station and also allows the configuring of the actual wafer map. Thus NUCLEUS provides the ease of maneuvering around the wafer to reach the desired spot via a user-friendly interface. The SAGITTARIUS software is used to integrate the probe station, switching matrix as well as the semiconductor parametric analyzer to form seamless automatic system for probing the devices under test (DUTs). This is very important when the amount of DUTs is very large as in the case of statistical MOSFET mismatch study. Otherwise, it would be too tedious, inefficient and unproductive to perform numerous measurements manually.

Figure 5.3: CASCADE Microchamber 8" probe station.

Hardware

The probe station used in the setup is from Cascade and it allows measurement of wafer with maximum size of 8". It can support 4 basic source/monitor units (SMUs) so that 4 different probed pads can be measured simultaneously. A picture of the probe station is shown in Figure 5.3.

Besides having an automatic measurement setup to facilitate a large amount of measurement, a probe card can also be a useful addition. This is because it cuts down the amount of time the setup has to move from one DUT to other. This stepping time can be substantial when many DUTs are to be characterized. The probe card used for CSM 0.13 μ m MOSFET mismatch characterization has 2x12 probes to match the 2x12 pads of the MOSFET mismatch test structure. A picture of the probe card is shown in Figure 5.4. It is already interfaced with the probe station and ready for MOSFET mismatch characterization.

Figure 5.4: Probe card interfaced with the probe station.

A switching matrix is needed with the use of probe card as the semiconductor parameter analyzer would not be able to support probes as many as 24 in this case for a 2x12 probe card. The switching matrix used for this work is Agilent B2201A, as shown in Figure 5.5, which supports 4 SMUs and full-Kelvin configuration. B2201A is important for an automatic measurement setup that uses a probe card to cut down MOSFET mismatch characterization time. At any time, B2201A only allows 4 of the 24 probes in the probe card to be performing MOSFET characterization.

Figure 5.5: Agilent B2201A switching matrix

HP/Agilent 4156B shown in Figure 5.6 is the semiconductor parameter analyzer used in the setup for semiconductor electrical characterization. HP 4156B has four highly accurate SMUs, two voltage source units (VSUs), and two voltage measurement units (VMUs). It is designed for Kelvin connections and has high-resolution SMUs and so it is suited for MOSFET mismatch characterization.

Figure 5.6: HP 4156B Semiconductor parametric analyzer

5.2.3 Statistical MOSFET mismatch data extraction

Algorithms of MOSFET mismatch characterization

As discussed in chapter 4, each module of MOSFET mismatch test structures would only contain MOSFETs of a single size. One module can hold 10 MOSFET matched pairs and hence there is a total of 20 MOSFETs. In each MOSFET pair, there would be the left and right MOSFET. During MOSFET mismatch characterization, the current MOSFET mismatch pair would have all the required measurements for the left MOSFET to be measured before the right MOSFET being measured. After both the left and right MOSFETs having their measurements taken, the next MOSFET mismatch pair would be measured till all the 10 MOSFET mismatch pairs have completed their measurements.

Details of MOSFET drain current mismatch

For every MOSFET in the designed MOSFET mismatch pair test structure, three drain current (I_d) measurements were taken for MOSFET mismatch characterization as discussed in chapter 4. Details for the biases at the MOSFET terminals during the I_d measurement are shown in Table 5-3.

Table 5-3: Details of the MOSFET terminal biases for the three I_d measurements.
 V_s and V_b are fixed at 0V for all three cases.

	Id1		Id2		Id3	
	Vd (V)	Vg (V)	Vd (V)	Vg (V)	Vd (V)	Vg (V)
start	1.2	0	0.1	0	0	0.6
end	1.2	1.2	0.1	1.2	1.2	0.6
step	0	0.05	0	0.05	0.1	0.0

The first I_d measurement (I_{d1}), characterized the MOSFET electrical behaviour at the saturation region of operation. The second I_d measurement (I_{d2}) characterized the MOSFET at the linear region of operation. Hence the obtained data from I_{d1}

and I_{d2} would allow the study cum modeling of MOSFET mismatch at the saturation and linear region of MOSFET operation. The purpose of the third I_d measurement (I_{d3}) is to provide statistical data to facilitate verification of the developed MOSFET mismatch model scalability across different terminal biases.

Extraction of statistical MOSFET mismatch data

For I_{d1} , five data points were extracted and they were called V_{tsat} , I_{doff_sat} , I_{dweak_sat} , I_{dmod_sat} and I_{dstr_sat} . The definitions of these data points are shown in the table below.

Table 5-4: Definitions of statistical MOSFET mismatch data extracted from MOSFET operation at saturation region. For all cases, $V_d=1.2V$ and both V_s and $V_b=0$.

I_{d1}	definition	Remark
V_{tsat}	$V_g@I_d = 0.1\mu A/W/L$	Sat. threshold voltage
I_{doff_sat}	$I_d@V_g = 0.0V$	Off-state leakage current (sat.)
I_{dweak_sat}	$I_d@V_g = 0.1V$	Weak inversion current (sat.)
I_{dmod_sat}	$I_d@V_g = 0.6V$	Moderate inversion current (sat.)
I_{dstr_sat}	$I_d@V_g = 1.2V$	Strong inversion current (sat.)

For I_{d2} , five data points were extracted and they are V_{tlin} , I_{doff_lin} , I_{dweak_lin} , I_{dmod_lin} and I_{dstr_lin} . The definitions of this data points are shown in the table below.

Table 5-5: Definitions of statistical MOSFET mismatch data extracted from MOSFET operation at linear region. For all cases, $V_d=0.1V$ and both V_s and $V_b=0$.

I_{d2}	definition	Remark
V_{tlin}	$V_g@I_d = 0.1\mu A/W/L$	Lin. threshold voltage
I_{doff_lin}	$I_d@V_g = 0.0V$	Off-state leakage current (lin.)
I_{dweak_lin}	$I_d@V_g = 0.1V$	Weak inversion current (lin.)
I_{dmod_lin}	$I_d@V_g = 0.6V$	Moderate inversion current (lin.)
I_{dstr_lin}	$I_d@V_g = 1.2V$	Strong inversion current (lin.)

These were done for both mismatch characterization of CSM $0.13\mu m$ n and p-MOSFETs.

5.3 Modelling MOSFET Mismatch Using BPV methodology

5.3.1 Electrical characteristics targets for BPV

The first step to develop the statistical MOSFET mismatch model using BPV methodology is to tabulate the variances of MOSFET mismatch in desired and selected electrical measurements. For this work, these measurements would refer to the different I_d values defined in Tables 4 and 5 of section 5.2. Their variances would be used as targets for the BPV methodology.

MOSFET mismatch in any electrical characteristics, E_p , is simply acquired by the equation (5.1).

$$\Delta E_p = E_{p, \text{left MOSFET}} - E_{p, \text{right MOSFET}} \quad (5.1)$$

Thus from the various extracted key I_d s data in section 5.2, a single MOSFET mismatch data in any particular I_d is computed by subtracting the I_d of the left MOSFET from that of the right MOSFET within a MOSFET matched pair test structure as in (5.2).

$$\Delta I_d = I_{d, \text{left MOSFET}} - I_{d, \text{right MOSFET}} \quad (5.2)$$

After computing the various MOSFET I_d mismatch data from the key I_d data of every characterized MOSFET matched pair of different MOSFET sizes, any outlier was removed and variances of MOSFET I_d s mismatch, $\sigma_{\Delta I_d}^2$, were computed.

The procedure described above for obtaining the variance of MOSFET I_d mismatch, $\sigma^2_{\Delta I_d}$, was done for all the n/p-MOSFET sizes that were deemed critical for the MOSFET mismatch model development to cut down time taken. Though 13 critical MOSFET sizes were chosen as highlighted in Table 5-6, only the 4 MOSFET sizes (numbered) at the corner of the geometry matrix of the MOSFET mismatch test structure design would be used for the MOSFET mismatch model using BPV methodology. The purpose is to study whether the MOSFET mismatch model based on these 4 corner MOSFET sizes can be scalable to different MOSFET sizes. The 4 corner n/p-MOSFET sizes are: (L/W, $\mu\text{m}/\mu\text{m}$) 0.13/10.4, 10.4/10.4, 10.4/0.15 and 0.15/0.15. Tables 5-6 and 5-7 show the variances of various I_d mismatch for the 4 corner n/p-MOSFET sizes.

Table 5-6: Critical MOSFET sizes chosen from the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure for mismatch characterisation.

		W	W	W	W	W	W	W	W
		41.6	10.4	4.16	2.08	1.04	0.52	0.26	0.15
L	41.6								
L	10.4		4						2
L	4.16								
L	2.08								
L	1.04								
L	0.52								
L	0.26								
L	0.15								1
L	0.13		3						

Table 5-7: I_d variances for the saturation region for the 4 corner n/p-MOSFETs

MOSFET		variance, σ^2				
type	size		drain current measurement at saturation region			
	W/ μm	L/ μm	$I_{doff}/(\text{nA}/\mu\text{m})$	$I_{dweak}/(\mu\text{A}/\mu\text{m})$	$I_{dmod}/(\mu\text{A}/\mu\text{m})$	$I_{dstr}/(\mu\text{A}/\mu\text{m})$
n	10.4	0.13	2.90025E+13	4.54172E-04	4.04647E+01	1.85971E+02
n	10.4	10.4	7.25238E-01	3.22831E-12	1.32258E-05	2.30634E-04
n	0.15	10.4	1.87499E+02	1.15534E-07	2.10357E-03	2.02689E-02
n	0.15	0.15	7.22237E+07	2.61515E-03	4.05915E+02	1.01992E+03
p	10.4	0.13	7.81175E+06	3.34096E-04	2.69370E+00	2.21181E+01
p	10.4	10.4	6.61433E-01	1.09850E-12	4.63397E-07	6.25099E-06
p	0.15	10.4	8.63233E+01	1.38434E-10	8.06408E-05	1.13085E-03
p	0.15	0.15	7.22742E+11	3.15750E-05	5.25590E+01	2.71324E+02

Table 5-8: Id variances for the linear region for the 4 corner n/p-MOSFETs

MOSFET		variance, σ^2				
type	size		drain current measurement at linear region			
	W/ μm	L/ μm	Idoff/(nA/ μm)	Idweak/($\mu\text{A}/\mu\text{m}$)	Idmod/($\mu\text{A}/\mu\text{m}$)	Idstr/($\mu\text{A}/\mu\text{m}$)
n	10.4	0.13	1.81799E+03	5.12102E-07	8.05623E+00	6.92490E+00
n	10.4	10.4	4.80531E-03	2.93799E-12	5.62351E-04	1.27787E-03
n	0.15	10.4	1.86631E+02	1.26448E-07	1.24715E-04	2.18415E-04
n	0.15	0.15	1.27598E+06	1.73466E-04	5.62851E+01	8.60122E+01
p	10.4	0.13	5.94571E+02	7.29147E-07	1.06260E+00	1.01043E+00
p	10.4	10.4	2.86756E-04	2.07318E-13	1.62698E-07	3.86276E-06
p	0.15	10.4	1.55439E-01	8.99369E-11	8.47111E-06	2.01334E-05
p	0.15	0.15	9.02477E+03	3.88269E-06	6.03692E+00	1.25813E+01

5.3.2 MOSFET Mismatch BPV model parameter sensitivity matrix

MOSFET mismatch parameters for BPV sensitivity matrix

The typical MOSFET model used for development of the BPV based MOSFET mismatch model is BSIM3v3, which is the third generation of BSIM MOSFET model developed by the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. It is developed upon a physical basis and aims to be scalable across different MOSFET terminal biases and geometries so as to attain accuracy and robustness.

In BSIM3v3 MOSFET model, some model parameters have a physical basis while others are just fitting parameters to enhance simulation accuracy, efficiency and robustness. It is important that only physical model parameters should be picked during the development of statistical MOSFET mismatch model so as to ensure that MOSFET mismatch is modeled as physically as possible and not empirically.

Ideally, the chosen MOSFET mismatch model parameters should address the sources of intrinsic MOSFET variation such as RDP, LER/LWR and surface

roughness. Furthermore, they must be able to capture the impact of different sources of variation in the operation region of MOSFET from linear to saturation, and from weak to strong inversion. Ultimately, the chosen MOSFET mismatch parameter set must be independent of one another so as to prevent ‘double-counting’ or over compensating of the MOSFET mismatch. With guidelines given, the chosen BSIM3v3 MOSFET parameters for mismatch modeling using the BPV approach are shown in Table 5-9.

Table 5-9: BSIM3v3 MOSFET parameters used in the MOSFET mismatch model developed using BPV methodology.

BSIM3v3 Model Parameter	Definition
Tox	Gate oxide thickness
Xj	Junction Depth
lint	length offset fitting parameter from I-V without substrate bias
wint	width offset fitting parameter from I-V without substrate bias
Nch	channel doping conc.
rsh	source drain sheet resistance in ohms per sq.
Vth0	Threshold voltage @ Vbs=0 for large L
Vfb	Flat-band voltage
U0	Mobility at Temp = Tnom
K1	First order body effect coefficient

Generation of sensitivity matrix using HSPICE

The step size for each model parameter to use for finding the numerical difference of the various key interested electrical parameters is determined by finding the smallest step size so as to result in an observable difference in the simulated electrical parameter using HSPICE circuit simulator. The process of finding the smallest step size thus involves iterative work of trying out different possible step sizes to achieve the smallest difference in the simulated value of the various key electrical parameters of interest. Table 5-10 shows the step sizes of different BSIM3v3 parameters used to derive the sensitivity matrix. They are important

because they determine the accuracy of the sensitivity matrix obtained by numerical differentiation.

Table 5-10: Step sizes of various BSIM3v3 MOSFET parameters used for finding the sensitivity matrix for the BPV methodology.

BSIM3v3 Parameter	Unit	Step size
Tox	m	1e-4(nm)
Xj	m	1e-2(um)
lint	m	1e-2(um)
wint	m	1e-1(um)
Nch	cm ⁻³	1e-3(1e18*cm ⁻³)
rsh	Ω/sq.	1(Ω/sq.)
Vth0	V	1e-3(V)
Vfb	V	1e-3(V)
U0	cm ² /Vs	1e-2(1e-3*cm ² /Vs)
K1	V ^{1/2}	1e-3(V ^{1/2})

Numerical differentiation method

In this part, the numerical differentiation algorithm used to derive the sensitivity matrix for BPV would be discussed. The gate oxide Tox would use as an example of for illustrating the computation of the partial differentiation of drain current i_d with respect to Tox. First, a column of different tox values at certain step sizes from the nominal Tox are tabulated. As an example, 5 different Tox values are tabulated in Table 5-11. Next, each of the Tox value would be replacing the nominal Tox parameter in the BSIM3v3 MOSFET model that was already extracted beforehand and run by HSPICE circuit simulator to obtain the simulated n- or p-MOSFET I_d of interest. Then the gradient for each Tox value is computed as shown the in the third column of the Table 5-11.

Table 5-11: Details of the numerical differential method used to derive the sensitivity matrix for BPV methodology.

Tox step size = $t_x - t_{x+1}$	simulated Id	Gradient with respect to nominal value
t_1	Id_1	$= \frac{Id_1 - Id_{nom}}{t_1 - t_{nom}}$
t_2	Id_2	$= \frac{Id_2 - Id_{nom}}{t_2 - t_{nom}}$
t_{nom}	Id_{nom}	0
t_3	Id_3	$= \frac{Id_3 - Id_{nom}}{t_3 - t_{nom}}$
t_4	Id_4	$= \frac{Id_4 - Id_{nom}}{t_4 - t_{nom}}$

In order to obtain the numerical differentiation of Id with respect to nominal gate oxide thickness t_{nom} , the average of gradient in column 3 of Table 5-11 is computed as in (5.3).

$$\frac{d(Id)}{d(Tox)} = \left(\frac{\frac{Id_1 - Id_{nom}}{t_1 - t_{nom}} + \frac{Id_2 - Id_{nom}}{t_2 - t_{nom}} + \frac{Id_3 - Id_{nom}}{t_3 - t_{nom}} + \frac{Id_4 - Id_{nom}}{t_4 - t_{nom}}}{4} \right) \quad (5.3)$$

The same numerical differentiation procedure is repeated for all the selected Id values in Tables 5-4 and 5-5, with respect to all the chosen BSIM3v3 MOSFET parameters for MOSFET mismatch model in Table 5-9.

BPV Sensitivity matrix

After the partial differentiation of every I_d against every MOSFET mismatch parameter is acquired, they were inserted into a matrix as shown in (5.4).

$$(5.4) \quad \begin{bmatrix} \left(\frac{dI_{doff_sat}}{dTox} \right) & \left(\frac{dI_{doff_sat}}{dXj} \right) & \left(\frac{dI_{doff_sat}}{dlint} \right) & \dots & \left(\frac{dI_{doff_sat}}{dVfb} \right) & \left(\frac{dI_{doff_sat}}{dU0} \right) & \left(\frac{dI_{doff_sat}}{dK1} \right) \\ \left(\frac{dI_{dweak_sat}}{dTox} \right) & \left(\frac{dI_{dweak_sat}}{dXj} \right) & \left(\frac{dI_{dweak_sat}}{dlint} \right) & \dots & \left(\frac{dI_{dweak_sat}}{dVfb} \right) & \left(\frac{dI_{dweak_sat}}{dU0} \right) & \left(\frac{dI_{dweak_sat}}{dK1} \right) \\ \dots & & & & & & \\ \left(\frac{dI_{dmod_lin}}{dTox} \right) & \left(\frac{dI_{dmod_lin}}{dXj} \right) & \left(\frac{dI_{dmod_lin}}{dlint} \right) & \dots & \left(\frac{dI_{dmod_lin}}{dVfb} \right) & \left(\frac{dI_{dmod_lin}}{dU0} \right) & \left(\frac{dI_{dmod_lin}}{dK1} \right) \\ \left(\frac{dI_{dstr_lin}}{dTox} \right) & \left(\frac{dI_{dstr_lin}}{dXj} \right) & \left(\frac{dI_{dstr_lin}}{dlint} \right) & \dots & \left(\frac{dI_{dstr_lin}}{dVfb} \right) & \left(\frac{dI_{dstr_lin}}{dU0} \right) & \left(\frac{dI_{dstr_lin}}{dK1} \right) \end{bmatrix}$$

The BPV sensitivity matrix in (5.5) was then simply found by squaring every term in (5.4).

$$(5.5) \quad \begin{bmatrix} \left(\frac{dI_{doff_sat}}{dTox} \right)^2 & \left(\frac{dI_{doff_sat}}{dXj} \right)^2 & \left(\frac{dI_{doff_sat}}{dlint} \right)^2 & \dots & \left(\frac{dI_{doff_sat}}{dVfb} \right)^2 & \left(\frac{dI_{doff_sat}}{dU0} \right)^2 & \left(\frac{dI_{doff_sat}}{dK1} \right)^2 \\ \left(\frac{dI_{dweak_sat}}{dTox} \right)^2 & \left(\frac{dI_{dweak_sat}}{dXj} \right)^2 & \left(\frac{dI_{dweak_sat}}{dlint} \right)^2 & \dots & \left(\frac{dI_{dweak_sat}}{dVfb} \right)^2 & \left(\frac{dI_{dweak_sat}}{dU0} \right)^2 & \left(\frac{dI_{dweak_sat}}{dK1} \right)^2 \\ \dots & & & & & & \\ \left(\frac{dI_{dmod_lin}}{dTox} \right)^2 & \left(\frac{dI_{dmod_lin}}{dXj} \right)^2 & \left(\frac{dI_{dmod_lin}}{dlint} \right)^2 & \dots & \left(\frac{dI_{dmod_lin}}{dVfb} \right)^2 & \left(\frac{dI_{dmod_lin}}{dU0} \right)^2 & \left(\frac{dI_{dmod_lin}}{dK1} \right)^2 \\ \left(\frac{dI_{dstr_lin}}{dTox} \right)^2 & \left(\frac{dI_{dstr_lin}}{dXj} \right)^2 & \left(\frac{dI_{dstr_lin}}{dlint} \right)^2 & \dots & \left(\frac{dI_{dstr_lin}}{dVfb} \right)^2 & \left(\frac{dI_{dstr_lin}}{dU0} \right)^2 & \left(\frac{dI_{dstr_lin}}{dK1} \right)^2 \end{bmatrix}$$

Using (5.5), the sensitivity matrices of the 4 corner n-MOSFET were obtained and shown in Tables 5-11 to 5-14, while those of p-MOSFET are shown in Tables 5-15 to 5-18.

Table 5-12: Sensitivity Matrix of n-MOSFET of W=10.4um L=0.13um

BSIM3v3 parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	1.22500E+07	4.94584E-03	4.41000E+04	1.97728E+05	2.54688E+05	1.28293E-04	1.02583E+04	1.82700E+04
Xj	2.55025E+03	1.03381E-06	5.85225E+01	7.14404E+02	3.25622E+00	1.62678E-09	1.87200E-01	2.07025E-01
lint	2.35225E+03	8.84603E-07	1.35375E+01	7.82045E+01	5.90814E+00	2.83734E-09	1.06468E+00	1.05517E+01
wint	1.37671E-02	5.78403E-12	3.69280E-04	1.00000E-02	2.71700E-04	1.38136E-13	5.95469E-05	1.48225E-03
Nch	4.63110E+04	1.93600E-05	1.69000E+02	4.26423E+02	7.84000E+02	4.22500E-07	3.65420E+01	4.20336E+01
rsh	0.00000E+00	0.00000E+00	2.27847E-05	1.74167E-03	0.00000E+00	0.00000E+00	4.18202E-06	2.42228E-03
Vth0	1.65241E+08	6.27662E-02	4.00689E+05	1.07533E+06	3.32563E+06	1.58646E-03	9.30575E+04	1.08900E+05
Vfb	2.00175E+04	1.34493E-05	3.83311E+02	2.16535E+03	4.04345E+02	3.44765E-07	8.74537E+01	1.50880E+02
U0	8.36920E+01	3.42250E-08	1.89705E+00	2.80547E+01	1.66969E+00	8.24647E-10	5.76840E-01	1.33103E+01
K1	1.19283E+08	4.53406E-02	3.00304E+05	1.00000E+06	2.39630E+06	1.13681E-03	6.73402E+04	1.01336E+05

Table 5-13: Sensitivity Matrix of n-MOSFET of W=10.4um L=10.4um

BSIM3v3 Parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	1.70583E+03	7.69421E-07	7.04018E+00	1.00000E+02	1.59640E+03	7.35306E-07	1.48190E+00	2.25000E+00
Xj	1.50471E-04	1.01336E-13	1.60000E-07	1.77803E-03	1.45604E-04	8.60444E-14	3.00444E-08	0.00000E+00
lint	4.00000E-08	2.02500E-15	0.00000E+00	0.00000E+00	2.02500E-07	6.13611E-15	2.20028E-08	0.00000E+00
wint	3.84160E-06	1.64025E-15	6.58778E-08	3.00444E-06	3.33671E-06	1.48225E-15	3.33671E-08	3.06178E-07
Nch	5.85735E-01	1.50880E-10	0.00000E+00	0.00000E+00	5.40470E-01	1.50880E-10	0.00000E+00	0.00000E+00
rsh	2.28803E-09	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	2.02500E-13	1.64694E-10
Vth0	4.11474E+04	1.75268E-05	9.41773E+01	1.30851E+03	3.84184E+04	1.63705E-05	1.97764E+01	2.20900E+01
Vfb	2.20572E+00	2.11140E-09	7.17347E-02	2.02114E+00	2.03823E+00	1.94040E-09	1.35218E-02	1.68134E-02
U0	3.04386E-02	1.37394E-11	1.22500E-03	1.00700E-01	2.74841E-02	1.27806E-11	5.15593E-04	5.70528E-03
K1	5.23211E+01	5.21361E-08	0.00000E+00	0.00000E+00	4.53378E+01	5.21361E-08	3.00444E-02	0.00000E+00

Table 5-14: Sensitivity Matrix of n-MOSFET of W=0.15um L=10.4um

BSIM3v3 Parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	2.71426E+06	4.84000E-04	1.18795E+01	1.16280E+02	2.53499E+06	4.53406E-04	1.09202E+00	2.25000E+00
Xj	1.23669E-01	3.02500E-11	4.00000E-08	1.17878E-03	1.23669E-01	3.02500E-11	0.00000E+00	0.00000E+00
lint	2.02500E-03	2.02500E-13	0.00000E+00	0.00000E+00	0.00000E+00	5.21361E-12	0.00000E+00	4.00000E-08
wint	4.57246E+01	9.60400E-09	7.68544E-07	8.63660E-03	4.27738E+01	8.88338E-09	3.02500E-05	7.09068E-04
Nch	1.62138E+02	3.94803E-09	4.00000E-06	0.00000E+00	1.37671E+02	3.78225E-09	0.00000E+00	0.00000E+00
rsh	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	2.02500E-11
Vth0	6.19272E+07	1.02603E-02	1.43740E+02	1.06080E+03	5.80489E+07	9.56262E-03	1.15600E+01	1.23541E+01
Vfb	8.59947E+03	2.41026E-06	1.43894E-01	2.25000E+00	8.06404E+03	2.23503E-06	1.00000E-02	1.88147E-02
U0	1.00000E+02	2.22656E-08	7.31595E-03	2.50000E-01	9.02500E+01	2.04299E-08	1.58404E-03	1.00000E-02
K1	8.60444E+04	1.77803E-05	4.22500E-01	0.00000E+00	1.06711E+05	1.48225E-05	0.00000E+00	0.00000E+00

Table 5-15: Sensitivity Matrix of n-MOSFET of W=0.15um L=0.15um

BSIM3v3 Parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	3.30242E+09	9.42194E-01	6.35040E+04	2.19180E+05	4.40160E+08	1.49975E-01	1.07571E+04	1.67271E+04
Xj	2.19883E+05	7.34449E-05	8.97756E+01	7.27381E+02	1.78647E+03	6.89453E-07	7.59803E-03	6.13611E-03
lint	4.91657E+04	1.61604E-05	8.41967E+00	4.58555E+01	5.53034E+02	2.23414E-07	1.02583E+00	6.73403E+00
wint	1.43863E+05	4.06959E-05	1.53795E-01	2.35662E+01	2.06837E+04	6.89579E-06	2.50000E-03	2.51910E+00
Nch	9.00000E+06	2.83734E-03	1.45604E+02	2.98138E+02	1.10250E+06	4.11008E-04	2.37331E+01	2.50000E+01
rsh	0.00000E+00	0.00000E+00	1.00000E-04	2.93945E-03	0.00000E+00	0.00000E+00	5.62500E-05	3.50661E-03
Vth0	4.94775E+10	1.34243E+01	5.80542E+05	1.18810E+06	6.54484E+09	2.12141E+00	8.90555E+04	8.41000E+04
Vfb	1.07103E+07	4.46447E-03	6.64780E+02	2.75450E+03	1.43520E+06	7.11911E-04	9.74498E+01	1.27314E+02
U0	3.01080E+04	9.78647E-06	6.25000E+00	5.22488E+01	3.69461E+03	1.40936E-06	2.33886E+00	1.84327E+01
K1	2.78000E+10	7.32604E+00	3.06178E+05	5.95469E+05	3.62404E+09	1.20012E+00	5.25938E+04	7.47111E+04

Table 5-16: Sensitivity Matrix p-MOSFET W=10.4um L=0.13um

BSIM3v3 parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	1.15600E+05	1.00000E-04	3.19037E+03	2.09284E+04	1.76181E+04	1.67731E-05	5.39014E+02	7.01367E+02
Xj	1.97551E+01	1.72222E-08	5.27621E+00	1.19025E+01	6.96112E-01	6.55104E-10	3.14471E-02	7.25336E-03
lint	2.25000E+00	1.43894E-09	1.49898E-01	1.07365E+01	1.64694E-04	2.09284E-12	1.00000E-02	8.10000E-01
wint	1.00000E-04	5.13778E-14	3.94803E-05	1.99511E-03	1.64025E-05	1.45604E-14	7.65444E-06	1.16280E-04
Nch	4.50571E+02	4.99142E-07	3.44765E+01	1.20634E+02	2.57895E+01	3.99200E-08	4.00000E+00	3.69280E+00
rsh	4.00000E-08	0.00000E+00	6.50711E-07	1.00000E-04	0.00000E+00	0.00000E+00	1.77803E-07	2.52004E-05
Vth0	3.68088E+06	3.00567E-03	6.92707E+04	3.31143E+05	5.22382E+05	4.79245E-04	1.09722E+04	1.09677E+04
Vfb	5.01028E+01	1.80767E-07	4.58555E+01	4.40300E+02	7.19134E+00	2.97620E-08	7.30801E+00	8.88040E+00
U0	3.09729E+01	2.72250E-08	8.33573E+00	3.04386E+02	3.74487E+00	3.64172E-09	1.90256E+00	2.65225E+01
K1	3.41445E+05	2.81680E-04	5.95469E+03	3.00444E+04	4.96547E+04	4.29462E-05	8.80111E+02	1.23669E+03

Table 5-17: Sensitivity Matrix p-MOSFET W=10.4um L=10.4um

BSIM3v3 parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	3.33121E+01	3.03514E-08	2.45520E-01	2.82800E+00	3.11178E+01	2.81345E-08	4.40300E-02	6.83822E-02
Xj	1.01336E-05	7.59803E-15	1.23669E-07	5.95469E-05	3.12111E-06	8.13003E-15	0.00000E+00	7.74694E-08
lint	2.02500E-07	2.02500E-17	6.13611E-09	5.21361E-06	0.00000E+00	4.00000E-18	0.00000E+00	5.21361E-08
wint	7.20028E-08	4.20336E-17	4.20336E-09	3.30625E-07	3.00444E-08	3.94803E-17	1.99511E-09	1.60867E-08
Nch	2.19180E-01	1.21000E-10	1.23669E-05	5.21361E-04	2.04304E-01	1.10670E-10	2.02500E-07	5.21361E-06
rsh	1.08900E-09	6.25000E-20	0.00000E+00	0.00000E+00	2.50000E-11	0.00000E+00	0.00000E+00	0.00000E+00
Vth0	1.62589E+03	1.37127E-06	6.38211E+00	6.37150E+01	1.50042E+03	1.26539E-06	1.08563E+00	1.12721E+00
Vfb	1.62138E-02	7.30170E-11	4.16670E-03	1.04221E-01	1.31867E-02	6.73494E-11	6.35040E-04	9.27202E-04
U0	1.28860E-02	1.20224E-11	1.28678E-03	7.60381E-02	1.17217E-02	1.09881E-11	4.49723E-04	4.12528E-03
K1	5.21361E+00	1.06711E-09	7.47111E-02	5.21361E+00	2.02500E-01	5.13778E-10	0.00000E+00	1.64694E-02

Table 5-18: Sensitivity Matrix of p-MOSFET W=0.15um L=10.4um

BSIM3v3 parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	3.93547E+03	1.88559E-06	5.35580E-01	5.88062E+00	3.60000E+03	1.75518E-06	7.19134E-02	1.42380E-01
Xj	1.38136E-03	5.20803E-13	1.01336E-07	2.48062E-04	6.08444E-04	5.95469E-13	5.21361E-08	3.12111E-08
lint	0.00000E+00	5.21361E-14	5.21361E-08	5.21361E-06	0.00000E+00	1.64694E-14	5.21361E-08	3.00444E-08
wint	6.00250E-02	2.33708E-11	5.17032E-06	3.89141E-04	5.47560E-02	2.12321E-11	2.69124E-06	2.26528E-05
Nch	3.02500E+01	7.09806E-09	2.50000E-05	8.60444E-04	2.71094E+01	6.52595E-09	5.21361E-06	6.13611E-07
rsh	1.00000E-08	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	0.00000E+00	6.13611E-13
Vth0	2.78170E+05	1.23871E-04	1.61759E+01	1.36578E+02	2.55486E+05	1.13432E-04	1.78686E+00	1.86268E+00
Vfb	1.81351E+00	5.65504E-09	1.05028E-02	2.19180E-01	1.50471E+00	5.29014E-09	1.06820E-03	1.87200E-03
U0	1.61968E+00	9.41365E-10	3.20073E-03	1.31539E-01	1.46975E+00	8.55465E-10	8.22638E-04	5.86424E-03
K1	1.64694E+02	1.48225E-07	2.50000E-01	5.21361E+00	8.10000E+01	1.23669E-07	5.21361E-02	0.00000E+00

Table 5-19: Sensitivity Matrix of p-MOSFET W=0.15um L=0.15um

BSIM3v3 parameter	Idoff_sat	Idweak_sat	Idmod_sat	Idstr_sat	Idoff_lin	Idweak_lin	Idmod_lin	Idstr_lin
Tox	1.44000E+06	9.95613E-04	1.46434E+03	1.00000E+04	3.02500E+05	2.35674E-04	1.88147E+02	2.60822E+02
Xj	2.23403E+02	1.67690E-07	2.97025E-01	2.50483E+02	4.16670E+01	3.42250E-08	2.02500E-03	1.46689E-01
lint	2.02114E+00	1.56420E-09	2.16070E-01	7.57167E+00	2.11703E+00	1.17306E-09	3.69280E-02	4.10240E-01
wint	3.17077E+00	1.74947E-09	5.31072E-02	3.47015E+00	4.45334E-01	2.89000E-10	1.24843E-02	1.63095E-01
Nch	4.83720E+03	5.01611E-06	1.22500E+01	1.23669E+01	2.38703E+02	4.42003E-07	9.60400E-01	5.65003E-01
rsh	0.00000E+00	0.00000E+00	2.50000E-07	5.60003E-05	0.00000E+00	0.00000E+00	3.73778E-08	5.16047E-06
Vth0	7.54530E+07	4.85038E-02	3.90649E+04	2.16535E+05	1.46523E+07	1.07727E-02	4.34171E+03	4.18954E+03
Vfb	8.88040E+02	2.78000E-06	2.50000E+01	3.06834E+02	1.82700E+02	6.00883E-07	2.65147E+00	3.13880E+00
U0	1.68469E+03	1.27588E-06	1.89225E+01	5.39555E+02	2.35674E+02	1.98025E-07	3.48693E+00	2.99008E+01
K1	4.86938E+06	3.33314E-03	3.34469E+03	1.64694E+04	1.00000E+06	7.01367E-04	2.20028E+02	5.21361E+02

5.3.3 Acquiring BSIM3v3 parameter variances using BPV

As MOSFET mismatch is dependent on its dimension, the basis of the Pelgrom model has to be incorporated into the BPV methodology so as to address the dependence of the MOSFET mismatch with respect to the MOSFET channel area and gate length and width. The equations in (5.6) depict the relationships between the variances of the MOSFET parameters against the MOSFET geometry parameters that were derived from Pelgrom's work [54]. The various constant parameters "A_p"s appearing in (5.6) would be the Figure-Of-Merit (FOM) on the amount of variation due to local process variation in the corresponding physical BSIM3v3 parameters. The smaller the value, the lesser is the impact of the corresponding BSIM3v3 parameter on MOSFET mismatch.

$$\begin{array}{ll}
 \sigma_{T_{ox}}^2 \propto \frac{1}{WL} & \sigma_{T_{ox}}^2 = \frac{A_{T_{ox}}}{WL} \\
 \sigma_{X_j}^2 \propto \frac{1}{W} & \sigma_{X_j}^2 = \frac{A_{X_j}}{W} \\
 \sigma_{I_{int}}^2 \propto \frac{1}{W} & \sigma_{I_{int}}^2 = \frac{A_{I_{int}}}{W} \\
 \sigma_{w_{int}}^2 \propto \frac{1}{L} & \sigma_{w_{int}}^2 = \frac{A_{w_{int}}}{L} \\
 \sigma_{N_{ch}}^2 \propto \frac{1}{WL} \Rightarrow \sigma_{N_{ch}}^2 = \frac{A_{N_{ch}}}{WL} \\
 \sigma_{V_{th0}}^2 \propto \frac{1}{WL} & \sigma_{V_{th0}}^2 = \frac{A_{V_{th0}}}{WL} \\
 \sigma_{V_{fb}}^2 \propto \frac{1}{WL} & \sigma_{V_{fb}}^2 = \frac{A_{V_{fb}}}{WL} \\
 \sigma_{U_0}^2 \propto \frac{1}{WL} & \sigma_{U_0}^2 = \frac{A_{U_0}}{WL} \\
 \sigma_{K_1}^2 \propto \frac{1}{WL} & \sigma_{K_1}^2 = \frac{A_{K_1}}{WL} \quad (5.6)
 \end{array}$$

To acquire the variances in the chosen BSIM3v3 MOSFET mismatch parameters due to local process variation by the BPV methodology, the original matrix equation in (5.7) had to be solved as in the case for statistical MOSFET modeling for global process variation in chapter 3.

$$\begin{bmatrix} \sigma_{I_{doff_sat}}^2 \\ \sigma_{I_{dweak_sat}}^2 \\ \vdots \\ \sigma_{I_{dmod_lin}}^2 \\ \sigma_{I_{dstr_lin}}^2 \end{bmatrix} = \begin{bmatrix} \left(\frac{dI_{doff_sat}}{dT_{ox}}\right)^2 & \left(\frac{dI_{doff_sat}}{dX_j}\right)^2 & \left(\frac{dI_{doff_sat}}{dl_{int}}\right)^2 & \dots \\ \left(\frac{dI_{dweak_sat}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dweak_sat}}{dX_j}\right)^2 & \left(\frac{dI_{dweak_sat}}{dl_{int}}\right)^2 & \dots \\ \vdots & \vdots & \vdots & \vdots \\ \left(\frac{dI_{dmod_lin}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dmod_lin}}{dX_j}\right)^2 & \left(\frac{dI_{dmod_lin}}{dl_{int}}\right)^2 & \dots \\ \left(\frac{dI_{dstr_lin}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dstr_lin}}{dX_j}\right)^2 & \left(\frac{dI_{dstr_lin}}{dl_{int}}\right)^2 & \dots \end{bmatrix} \begin{bmatrix} \sigma_{T_{ox}}^2(WL) \\ \sigma_{X_j}^2(W) \\ \sigma_{l_{int}}^2(W) \\ \sigma_{wint}^2(L) \\ \sigma_{Nch}^2(WL) \\ \sigma_{rsh}^2(W) \\ \sigma_{V_{th}}^2(WL) \\ \sigma_{V_{fb}}^2(WL) \\ \sigma_{U_0}^2(WL) \\ \sigma_{K_1}^2(WL) \end{bmatrix} \quad (5.7)$$

But with the coupling of the matrix in (5.7) with the basis of Pelgrom model in (5.6), the new matrix to solve for variances in the chosen BSIM3v3 MOSFET mismatch parameters by BPV methodology would look something like (5.8) for a single MOSFET size. This was repeated for all the 4 corner n/p-MOSFET sizes.

$$\begin{bmatrix} \sigma_{I_{doff_sat}}^2 \\ \sigma_{I_{dweak_sat}}^2 \\ \vdots \\ \sigma_{I_{dmod_lin}}^2 \\ \sigma_{I_{dstr_lin}}^2 \end{bmatrix} = \begin{bmatrix} \left(\frac{dI_{doff_sat}}{dT_{ox}}\right)^2 & \left(\frac{dI_{doff_sat}}{dX_j}\right)^2 & \left(\frac{dI_{doff_sat}}{dl_{int}}\right)^2 & \dots \\ \left(\frac{dI_{dweak_sat}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dweak_sat}}{dX_j}\right)^2 & \left(\frac{dI_{dweak_sat}}{dl_{int}}\right)^2 & \dots \\ \vdots & \vdots & \vdots & \vdots \\ \left(\frac{dI_{dmod_lin}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dmod_lin}}{dX_j}\right)^2 & \left(\frac{dI_{dmod_lin}}{dl_{int}}\right)^2 & \dots \\ \left(\frac{dI_{dstr_lin}}{dT_{ox}}\right)^2 & \left(\frac{dI_{dstr_lin}}{dX_j}\right)^2 & \left(\frac{dI_{dstr_lin}}{dl_{int}}\right)^2 & \dots \end{bmatrix} \begin{bmatrix} A_{T_{ox}}/WL \\ A_{X_j}/WL \\ A_{l_{int}}/W \\ A_{wint}/L \\ A_{Nch}/WL \\ A_{rsh}/W \\ A_{V_{th}}/WL \\ A_{V_{fb}}/WL \\ A_{U_0}/WL \\ A_{K_1}/WL \end{bmatrix} \quad (5.8)$$

Using optimization technique on the (5.8) for all the 4 corner MOSFET sizes, the various values of the parameter mismatch constant A_p for the MOSFET mismatch parameter variances were obtained. Tables 5-20/21 show the various constant parameter A_p values for both n- and p-MOSFET BSIM3v3 parameters as well as their corresponding variances due to local process variation for different MOSFET sizes.

Table 5-20: A_p and variances of various n-MOSFET BSIM3v3 parameters acquired by the BPV methodology. The MOSFET size is presented in L/W ($\mu\text{m}/\mu\text{m}$) format.

BSIM3v3 Parameter	n-MOSFET				
	A_p	σ^2			
		0.13/10.4	10.4/10.4	10.4/0.15	0.15/0.15
Tox	7.36E-03	5.42E-05	5.01E-07	3.47E-05	2.41E-03
Xj	7.59E-05	5.76E-09	5.54E-10	3.84E-08	3.84E-08
lint	2.10E-05	4.42E-10	4.25E-11	2.94E-09	2.94E-09
wint	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Nch	1.53E-04	2.33E-08	2.16E-10	1.50E-08	1.04E-06
rsh	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vfb	4.14E-04	1.71E-07	1.58E-09	1.10E-07	7.60E-06
U0	6.09E-05	3.71E-09	3.43E-11	2.38E-09	1.65E-07
K1	4.31E-03	1.85E-05	1.71E-07	1.19E-05	8.24E-04

Table 5-21: A_p and variances of various p-MOSFET BSIM3v3 parameters acquired by the BPV methodology. The MOSFET size is presented in L/W ($\mu\text{m}/\mu\text{m}$) format.

BSIM3v3 Parameter	p-MOSFET				
	A_p	σ^2			
		0.13/10.4	10.4/10.4	10.4/0.15	0.15/0.15
Tox	1.37E-04	1.01E-04	1.27E-06	8.79E-05	6.09E-03
Xj	5.64E-07	5.42E-08	5.42E-08	3.76E-06	3.76E-06
lint	1.89E-08	1.81E-09	1.81E-09	1.26E-07	1.26E-07
wint	8.31E-09	6.39E-08	7.99E-10	7.99E-10	5.54E-08
Nch	4.32E-07	3.19E-07	3.99E-09	2.77E-07	1.92E-05
rsh	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vfb	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
U0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
K1	2.87E-04	2.13E-04	2.66E-06	1.84E-04	1.28E-02

Verification of MOSFET mismatch model

In order to verify the various A_p values for both n- and p-MOSFET of the developed MOSFET mismatch model using BPV approach, Monte Carlo simulation of MOSFET mismatch using the acquired variances in MOSFET mismatch parameters was run. The variances of chosen I_d values for the 4 corner MOSFET sizes were extracted from Monte Carlo simulated data and compare with that extracted from the measurement data. The comparisons for various I_d and MOSFET sizes were done on the Pelgrom plot, which is plot of the standard deviation of the MOSFET electrical characteristics mismatch against the square root of the inverse MOSFET channel area. Figures 5-7 to 5-10 show the Pelgrom plots for the n-MOSFET while Figures 5-11 to 5-14 show that of the p-MOSFET.

Generally, good matching between the simulated data and the measurement were observed for both n and p-MOSFET. The only notable problem was found for the Pelgrom plots of $\sigma_{\Delta n I_{doff}}$ and $\sigma_{\Delta p I_{doff}}$ in Figures 5-7 and 5-11, especially during MOSFET operation at saturation region. The discrepancies were believed to be due to the poor accuracy of the measurement setup for I_{doff} characterisation of both n and p-MOSFET as they are very sensitive to the leakage current of the setup.

Figure 5.7: Pelgrom plot for comparing $\sigma_{\Delta Id_{off}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.

Figure 5.8: Pelgrom plot for comparing $\sigma_{\Delta Id_{weak}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.

Figure 5.9: Pelgrom plot for comparing $\sigma_{\Delta Id_{mod}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement for 4 corner n-MOSFET sizes.

Figure 5.10: Pelgrom plot for comparing $\sigma_{\Delta Id_{str}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.

Figure 5.11: Pelgrom plot for comparing $\sigma_{\Delta Id_{off}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.

Figure 5.12: Pelgrom plot for comparing $\sigma_{\Delta Id_{weak}}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.

Figure 5.13: Pelgrom plot for comparing $\sigma_{\Delta pidoff}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.

Figure 5.14: Pelgrom plot for comparing $\sigma_{\Delta pidstr}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.

MOSFET mismatch model geometry scalability

The MOSFET mismatch model were developed using the BPV methodology using only the I_d mismatch data from the 4 corner MOSFET sizes. In this sub-section, the Pelgrom plots for the comparison of the standard deviation in the mismatch of all I_d measurements in Table 5-4 and 5-5, to results using Monte Carlo simulation were generated, for all the 13 critical MOSFET sizes in the geometry matrix of the MOSFET mismatch test structure.

These Pelgrom plots allow the study on the feasibility of using only the 4 corner MOSFET sizes to predict the MOSFET I_d mismatch for the other MOSFET sizes. By being feasible, the BPV methodology discussed in this work would cut down a lot of time for MOSFET mismatch characterisation and optimisation of BPV solution and valuable wafer real estate for MOSFET mismatch test structure in the future for MOSFET mismatch model development and monitoring. From Figures 5-15 to 5-20, the Pelgrom plots are for the n-MOSFET while those of p-MOSFET are shown in Figures 5-23 to 5-30.

Overall, the matching between the simulated data and measurement data were good as the general trend of the simulated data for every Pelgrom plot was tracking that of the measurement data. The results for n-MOSFET are better than p-MOSFET. Again, problem was found for the Pelgrom plots of $\sigma_{\Delta I_{doff}}$ and $\sigma_{\Delta p_{doff}}$, especially for p-MOSFET operation in saturation region. The discrepancies were believed to be due to the poor accuracy of the measurement setup for I_{doff} characterisation of both n and p-MOSFET as they are very sensitive to the leakage current of the setup which is close to the picoampere regime of I_{doff} measurement.

Thus, the MOSFET mismatch model shows acceptable geometry scalability, which can be further optimised during BPV for p-MOSFET.

Figure 5.15: Pelgrom plot for comparing $\sigma_{\Delta I_{doff}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.16: Pelgrom plot for comparing $\sigma_{\Delta I_{doff}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.17: Pelgrom plot for comparing $\sigma_{\Delta \text{Idweak}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.18: Pelgrom plot for comparing $\sigma_{\Delta \text{Idweak}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.19: Pelgrom plot for comparing $\sigma_{\Delta I_{dmod}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.20: Pelgrom plot for comparing $\sigma_{\Delta I_{dmod}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.21: Pelgrom plot for comparing $\sigma_{\Delta Idstr}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.22: Pelgrom plot for comparing $\sigma_{\Delta Idstr}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.23: Pelgrom plot for comparing $\sigma_{\Delta I_{Doff}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.24: Pelgrom plot for comparing $\sigma_{\Delta I_{Doff}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.25: Pelgrom plot for comparing $\sigma_{\Delta Id_{weak}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.26: Pelgrom plot for comparing $\sigma_{\Delta Id_{weak}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.27: Pelgrom plot for comparing $\sigma_{\Delta I_{Dmod}}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.28: Pelgrom plot for comparing $\sigma_{\Delta I_{Dmod}}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.29: Pelgrom plot for comparing $\sigma_{\Delta Idstr}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.30: Pelgrom plot for comparing $\sigma_{\Delta Idstr}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Prediction of MOSFET threshold voltage mismatch based on MOSFET mismatch model developed using MOSFET Id mismatch with BPV methodology

During the development of the MOSFET mismatch model, only the Id data were used during the BPV methodology. If the developed MOSFET mismatch model is physical rather than empirical, then it should be able to predict the MOSFET mismatch in other electrical behaviour. In this sub-section, the Pelgrom plots for the comparison of the standard deviation in the mismatch of V_{tlin} and V_{tsat} , defined in Tables 5-4 and 5-5, of simulated results using Monte Carlo simulation from measurement were generated, for the 4 corner n/p-MOSFET sizes and all the critical n/p-MOSFET sizes in the geometry matrix of the n/p-MOSFET mismatch test structure.

The Pelgrom plots of n-MOSFET are presented first from Figures 5.31 to 5.33. These are followed by that of p-MOSFET from Figure 5.34 to Figure 5.36. Good matching of simulated data and measurement data were observed for $\sigma_{\Delta V_t}$ at linear and saturation region for both n and p-MOSFET. The trend of the simulated data also tracked the measurement data very well for all the MOSFET sizes.

Figure 5.31: Pelgrom plot for comparing $\sigma_{\Delta nvt}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner n-MOSFET sizes.

Figure 5.32: Pelgrom plot for comparing $\sigma_{\Delta nvt}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.33: Pelgrom plot for comparing $\sigma_{\Delta nvt}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical n-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.34: Pelgrom plot for comparing $\sigma_{\Delta pvt}$ of both linear and saturation regions generated from Monte Carlo (MC) simulation against that from measurement data of the 4 corner p-MOSFET sizes.

Figure 5.35: Pelgrom plot for comparing $\sigma_{\Delta pvt}$ of linear region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

Figure 5.36: Pelgrom plot for comparing $\sigma_{\Delta pvt}$ of saturation region generated from Monte Carlo (MC) simulation against that from measurement data of all the critical p-MOSFET sizes in the geometry matrix of the CSM 0.13 μm MOSFET mismatch test structure design.

CHAPTER 6

CONCLUSIONS & FUTURE WORKS

6.1 Conclusions

In this work, statistical MOSFET models were developed to address the effects of global as well as local process variations. Different CMOS technologies were investigated during these developments, ranging from CSM 0.35 μ m technology for global process variation to CSM 90nm (LP) technology for local process variation. These statistical models are capable of performing accurate and realistic statistical circuit simulation for circuit functional and performance yield analysis under real process variation conditions. The conclusions for the work done will be summarized in the chronicle order of the thesis chapters.

In Chapter 3, a statistical MOSFET model for global process variation was developed using the BPV approach. The developed statistical MOSFET model was more realistic than the traditional corner models, which were too pessimistic in setting the design margin for MOSFET under global process variation. Using BPV methodology, not only was the developed statistical MOSFET model able to tackle the problem of correlation between MOSFET parameters but also to account the correlation of n and p-MOSFET performance variation due to global process variation. The developed statistical MOSFET model also allows the study of MOSFET performance variation under different process control limits (one to three sigma) of global process variation.

In Chapter 4, MOSFET mismatch test structures were designed using a simple MOSFET matched pair on 2xN and 1xN pad modules to improve the efficiency and accuracy of intrinsic MOSFET mismatch characterization. The geometry matrix of the MOSFET mismatch test structure was also planned carefully to cater for MOSFET mismatch characterization. This is very important because the accuracy of the MOSFET mismatch characterization data obtained here would affect the legitimacy of the MOSFET mismatch model developed in Chapter 5. The effect of processing or layout factors on MOSFET mismatch characterization, such as BEOL metal layers, multi-finger MOSFET layout and gate protection diode were studied for CSM 0.18 μ m, 0.13 μ m and 90nm (LP) technologies. It was found that BEOL worsened the p-MOSFET mismatch in threshold voltage while n-MOSFET mismatch remained relatively unaffected. Multi-fingered MOSFET layout was observed to be beneficial for wide-sized MOSFET mismatch in threshold voltage if the optimum number of fingers were used. As for gate protection diode, it did not achieve the expected improvement in MOSFET mismatch performance. In fact, GPD might even worsen the MOSFET mismatch in threshold voltage.

In Chapter 5, a MOSFET mismatch model was developed using the BPV approach coupled with the basis of Pelgrom model. MOSFET mismatch data in drain current at different gate bias and in both linear and saturation regions of MOSFET operation were used as the BPV targets. By using only 4 corner MOSFET sizes, the developed MOSFET mismatch model was able to scale acceptably for different MOSFET sizes of both n and p-MOSFET. The MOSFET mismatch model was able to predict the MOSFET mismatch in threshold voltage in both linear and

saturation regions very well even though only MOSFET mismatch data in drain current were used as the BPV targets. Improvements can be made with better optimization during the BPV methodology.

6.2 Future Works

There are two recommendations for the improvement of the research work discussed in this thesis. The first recommendation is on MOSFET mismatch characterization. Currently, the two MOSFETs in a MOSFET matched pair test structure are characterized one after another. However, matching MOSFETs in a real circuit are biased at the same time. So in order to perform a realistic MOSFET mismatch characterization, the two MOSFETs in a MOSFET matched pair must be characterized at the same time to emulate the real MOSFET mismatch in a circuit. In addition, MOSFET mismatch in tunneling gate current would be interesting to study with current scaling of gate oxide to a few nm and the use of high-k gate dielectrics oxide in the future. According to a paper [60] by Intel in IEDM 2007, it was presented that high-k gate dielectrics can reduce MOSFET performance variation due to process variation.

The second recommendation is on the development of statistical MOSFET models using the BPV approach. It can be further improved with the use of TCAD (technology computer aided design) such as T-Suprem and Medici to study the sensitivity of the MOSFET electrical behaviour with respect to various process and MOSFET parameters. In this way, TCAD can help in identifying the important process and MOSFET parameters that are critical to the MOSFET performance under process variation. Furthermore, use of TCAD can isolate the sources of

process variation and study sole effect of individual source of process variation on MOSFET electrical performance. Thus with this enhanced understanding of the effect of process variation impact on MOSFET, a consistent approach merging the use of TCAD and BPV based statistical MOSFET model can result in the extraction of reasonable and physical MOSFET parameter variances during BPV methodology. This undoubtedly ensures the scalability of the developed statistical MOSFET model under all conditions.

Recommendations for future work

Future works are recommended in the area of process variation and MOSFET performance, the immediate one would be to study how the use of high-k gate dielectric and metal gate in the near future for planar MOSFET would affect the MOSFET performance variation. In addition, SOI MOSFET could also be studied other than bulk MOSFET. These could be carried out with this work as a basis and further improvement through the adoption of the recommended TCAD plus BPV methodology. Last but not least, the study of large geometry dependent variations due to the adoption of strained Si technology to boost performance will also be vital.

As scaling continues, the impact of local process variation, which has always been a concern for analog circuit, is becoming a great concern for digital circuit that makes up the biggest IC market. Thus, current study of process variation has put a lot of focus on MOSFET mismatch and there are numerous important issues worth to working on. One of them is intrinsic asymmetric MOSFET channel current due to random dopant concentration at the source and drain side. This is in contrast to

the common known asymmetric MOSFET drain current due to different source and drain size or doping. This intrinsic asymmetry MOSFET channel current can be adverse for SRAM, a very important memory component for microprocessor, as the source and drain terminals are switched during read and write operation.

Another interesting and important work would be the increasing impact of LER/LWR as gate length and width have reached 32nm and continue to scale down. Currently, LER/LWR is assumed not to be as significant as random dopant fluctuation and thus MOSFET mismatch is always associated with channel area and not the gate length and width. It is strongly believed that this would be changed in the near future and thus LER/LWR must be properly modeled by advanced MOSFET compact models so that BPV based MOSFET mismatch model is legitimate.

Besides MOSFET mismatch that is capturing the attention as MOSFET scaling continues, the impact of NBTI (negative bias temperature instability) is also an important concern. NBTI has known to be affecting p-MOSFET only by causing a shift in threshold voltage. It would be interesting to study the contribution of NBTI on p-MOSFET mismatch and to account for it properly in the MOSFET mismatch model. Lastly, novel MOSFET structures have been proposed to replace the planar MOSFET when bulk MOSFET scaling ends at the end of roadmap. Thus it would be interesting to study the mismatch behaviours of double-gate MOSFET, FinFET and nanowire MOSFET (GAA MOSFET).

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