Novel transistor structures for future deep submicron MOS applications

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Novel Transistor Structures for Future Deep Submicron MOS Applications

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SUMMARY

Bulk silicon CMOS processing is reaching the limits in device scaling and fabrication. Silicon-On-Insulator (SOI) technology provides an alternative. It not only allows better scalability but also a solution to low power and high performance applications for next generation CMOS devices. Fully depleted SOI transistors have emerged as one of the leading candidate for CMOS scaling. The possibility of using the back gate has sparked research activities in the field of novel non-classical SOI devices. In recent years, non-classical SOI devices such as double, triple and quadruple multi-gate MOSFET have attracted vast interests in various research bodies and researchers. Among the multiple gate designs, the triple gate and the gate-all-around (GAA) designs present attractive properties for high performance applications. This thesis aims to provide electrical data of two novel non-classical SOI devices, the n-gate and gate-all-around structures, both manufactured using the Chartered Semiconductor Manufacturing 0.13 μm process. The results obtained have indicated that both devices are able to achieve high drive current and outstanding subthreshold characteristics.

The project extends further to develop silicon nanowire multiple gate MOSFET devices, which utilizes the stress limited oxidation technique at Institute of Microelectronics (IME). The oxidation conditions are varied and both SOI and polysilicon wafers are used. We are able to achieve both single and double (top and bottom) silicon nanowires through this technique. Dual nanowire MOSFETs are fabricated with the incorporation of high-k gate dielectric and metal gate. Single metal (Ta₂N₅) is used as gate material for both n- and p-dual nanowire MOSFETs. Both n- and p-

type devices achieved high I_{ON}/I_{OFF} current ratio of more than 10^5 with a higher threshold voltage (V_T) compared to polysilicon devices. Metal gate workfunction shifts the I_d vs V_g characteristics devices to attain low leakage while maintaining high drive current. Fabrication processes and electrical characterization will also be covered in this thesis.

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CHAPTER 1: INTRODUCTION

1.1 MOTIVATION

The physical gate length of MOSFET has been scaled by 70% at every generation node as illustrated in Figure 1.1. This trend upholds the Moore's Law [1], which states that the number of transistors packed per unit area doubles at every eighteen month cycle. When the gate length of the device is scaled, the drain will gain more influence over the channel. The drain depletion layer will overlap the source depletion region and lowers the source-substrate potential. As scaling continues, it will be more difficult to produce devices without compromising on the performance, especially on the degrading of the subthreshold slope and drain induced barrier lowering (DIBL) effect. These effects cause variation within devices and reduce the on-off current ratio. Bulk silicon CMOS processing will therefore be reaching the limits for scaling in the next few years.

Figure 1.1 Trend of transistor gate length scaling.

Research efforts seeking for developments and solutions to sustain the growth of the silicon semiconductor industry has been ongoing. Researchers are looking for resolutions that are compatible with existing silicon processes, while providing superior device performance. The Silicon-On-Insulator (SOI) technology offers such capability. As indicated in Figure 1.2, the SOI technology delivers a leap in performance when compare to bulk silicon processing. It allows the CMOS processing technology to keep up with Moore's Law while maintaining high performance device characteristics.

Figure 1.2 Comparison of SOI and Bulk device performance at different technology nodes.

1.1.1 SUBSTRATE ENHANCEMENT

Partially depleted SOI MOSFET (PD-SOI) device have been found to be an attractive replacement for bulk MOSFETs. It provides full dielectric isolation and a reduction in junction capacitance as compare to bulk silicon transistors [2]. However the floating body in PD-SOI causing a drop in the threshold voltage (V_t) and noise overshoot

[3]. The Ultra Thin Body (UTB) fully depleted SOI (FD-SOI) MOSFET and non-classical SOI MOSFET are developed in recent years to improve on the SOI devices. All of the mentioned structures will be elaborated in Chapter 2.

1.1.2 GATE ENHANCEMENT

Non-classical SOI devices have sparked large volume of research work due to their delivery of higher performance with lower off state leakage than other SOI approaches. In today's context, several promising non-classical SOI device architectures have been explored. These include double gate FinFET, tri-gate and gate-all-around (GAA) transistors. All the above devices utilize a fully depleted substrate and multiple gate structure to improve the short channel performance, while maintaining high current drives. Figure 1.3 is taken from the International Technology Roadmap for Semiconductor (ITRS) 2005 edition where it provides a timeline on the development of SOI technology. It truly indicates that multi-gate non-classical SOI devices can be the solution for sub-20 nm devices.

Figure 1.3 Projected development of SOI technology.

1.1.3 NANOWIRES

The aspect ratio of the fin thickness and gate length is an important consideration for nano-scale SOI devices [4]. The fin thickness is usually restricted by the gate length (L_g), and this poses a significant issue on lithography. The evolution of nanowire devices successively relaxes the gate length concern, from which $2L_g/3$ for double gate structure and L_g for triple gate structure to $2L_g$ for nanowire devices [5]. Nanowires are also reported of having improved transport properties [6] for current enhancement. Owing to small diameter and good electrical characteristics, the nanowire multi-gate structure is therefore a promising candidate for sub-10 nm technology node.

1.2 OBJECTIVES

The objectives of this thesis are:

- To study and understand various SOI architectures.
- To carry out electrically characterization on novel non-classical SOI MOSFET transistors that are developed using Chartered Semiconductor Manufacturing Limited's 0.13 μm process.
- To design and develop silicon nanowire GAA MOSFET device on SOI platform based on the Institution of Microelectronics (IME) process.
- To explore metal gate and Hi-k dielectric to enhance the performance of nanowire MOSFET.

1.3 MAJOR CONTRIBUTIONS

The novel SOI MOSFET n-gate structure developed is an improvement from the tri-gate architecture proposed by Intel [7] (see Figure 2.4). The tri-gate although permits attractive electrical characteristics, suffers from early turn-on effect due to the high current density at the edges [8]. The n-gate design developed in this work, as depicted in Figure 3.1, includes an additional etching procedure to round the corners of the tri-gate device, thus eliminating the early turn-on effect. The sidewall gate electrode extension presented in the pi-gate architecture [9] is also embraced in the n-gate design. The extension of the gate electrode into the buried oxide (BOX) helps to shield the back of the channel from the electric field directed from the drain.

Various literature reviews have indicated that GAA architecture demonstrates the most attractive electrical performances among the SOI non-classical architectures. GAA architecture is able to effectively suppress the short channel effect, while maintaining high current drive. This is because of the increased in gate coverage which allows volume inversion. In this work, GAA is fabricated using the gate replacement development technique, saving a masking step for polysilicon gate etch. Such saving can eliminate possible top and bottom gate misalignment [10] issues in some GAA designs and also making the GAA more manufacturable.

The gate coverage over the channel of the device has also been investigated. The increase in gate coverage is able to improve on the drive current as well as suppressing short channel effect. On top of that, GAA MOSFET is reported to provide the best

possible electrostatic control. The reduction in both the thickness and width of the channel further enhances on the effectiveness of the overall gate control. Therefore suppression of the short channel effect can be achieved through using GAA structure.

The combination of nanowire and GAA architecture is a favorable option for future CMOS scaling [11]. Polysilicon gate nanowire MOSFETs are reported to provide great electrical performances. However, their low threshold voltage (V_t) causes high leakage current [12]. The deployment of metal gate is able to improve on the workfunction of polysilicon gate and hence providing a higher V_t and lower leakage current. With that, TaN gate has been explored in this research.

1.4 ORGANIZATION OF REPORT

Chapter 1 has presented the motivation of this research thesis; defining the objectives of this thesis and highlights on the major contributions. In Chapter 2 a comprehensive literature review of the various SOI MOSFET structures is produced. The PD-SOI and the FD-SOI devices will also be briefly touched on in Chapter 2. Non-classical SOI structures and nanowire MOSFET will be the focus of this work and will be discussed in depth.

The fabrications of a novel non-classical SOI MOSFET (termed n-gate) and the GAA structures are detailed in Chapter 3. Chapter 4 discusses on the electrical characterization of both the n-gate and GAA structures. Simulations data will also be

provided to determine the scalability of the devices. The influences of the amount of gate coverage on the drive current and short-channel performances are examined.

The nanowire MOSFET device fabrication will be illustrated in Chapter 5. The formation of nanowire via stress-limited oxidation and fabrication of the TaN gate dual nanowire MOSFET will be highlighted. In Chapter 6, the electrical performances of the nanowire MOSFETs are discussed. Finally, Chapter 7 summarizes the results of the work done. The proposal for future work, which is the investigation of the metal gate induced stress on the nanowire channel and the optimization of the threshold voltage of n-type dual nanowire MOSFET device will also be briefly described.

CHAPTER 2: LITERATURE REVIEW

2.1 MOSFET BASICS

2.1.1 DRAIN INDUCED BARRIER LOWERING

Drain induced barrier lowering (DIBL) is a short channel effect in which high drain bias cause barrier lowering and result in high leakage current. The gate voltage modulates the potential barrier at the source and substrate region. In the event of inversion, the source-substrate barrier is sufficiently lowered to allow carriers to flow. The change in energy barrier at different bias is illustrated in Figure 2.1. Figure 2.1 (a) shows the depletion layer and energy band diagram prior application of drain voltage. With the increase in drain voltage, the depletion region of the drain gradually moves closer to the source region, as depicted in Figure 2.1 (b). When the drain depletion region overlaps the source depletion region [see Figure 2.1 (c)], the potential barrier at source-substrate will be lowered. This barrier lowering process is termed DIBL.

2.1.2 SUBTHRESHOLD SLOPE

Subthreshold slope is a measure of change in drain current due to change in gate voltage in the subthreshold region and can be evaluated using Equation (2.1).

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \left(\frac{mkT}{q} \right) = 2.3 \left(\frac{kT}{q} \right) \left(1 + \frac{C_{dm}}{C_{ox}} \right) \quad \text{Equation (2.1)}$$

where C_{dm} is the depletion capacitance and C_{ox} is the gate oxide capacitance.

Figure 2.1 Energy band diagrams of a device undergoing DIBL.

For circuits to attain fast switching, a steep subthreshold slope is desired. In this case, minimum gate voltage change is desired for attaining a decade increase in the drain current. The most direct means of obtaining steep subthreshold slope is by reducing the depletion capacitance and increasing the gate oxide capacitance. The subthreshold current is independent of the drain voltage once V_{ds} is larger than a few kT/q , as diffusion-dominated current transport is expected. It has an exponential relationship with gate voltage. Hence subthreshold slope Eqn 2.1 is derived. From the equation, it is made

known that the only variables are depletion-layer capacitance (C_{dm}) and gate-oxide capacitance (C_{ox}) as kT/q is fixed. The depletion capacitance is usually associated with interface traps. Gate oxide capacitance is associated with electrical oxide thickness (EOT). Minimum S can be gained through gate oxide scaling or using Hi-k dielectric materials, such as HfO_2 , which are popular in recently reported advanced MOSFET devices.

2.2 PARTIALLY DEPLETED AND FULLY DEPLETED SOI

The thickness of the top silicon layer on the buried oxide is the key factor for determining if the SOI device is partially depleted (PD) or fully depleted (FD). A criterion has been established to differentiate between them. Shown below in Equation (2.2) is the formula for determine the depletion width.

$$W_{depl} = \sqrt{\frac{4\epsilon_{si}\phi_f}{qN_A}} \quad \text{Equation (2.2)}$$

where ϕ_f is the Fermi potential and N_A is the doping concentration of the silicon.

When the thickness of the top silicon (T_{SOI}) is more than two times the depletion width ($T_{SOI} > 2W_{depl}$), the device will be considered partially depleted. If top silicon thickness is smaller than the depletion width ($T_{SOI} < W_{depl}$), the device will be deemed a fully depleted SOI device. The criteria are illustrated in Figure 2.2. In partially depleted structure, a neutral region will be formed with the thick silicon, and hence the name partially depleted. The partially depleted transistor will be similar to bulk transistor with the neutral region as body. If the body is left floating, the transistor will be subjected to

parasitic effects [13], as such the kink-effect and single bipolar transistor latch up. These effects will be explained in the following sub-sections.

Figure 2.2 (a) Partially depleted (PDSOI) and (b) fully depleted (FD-SOI) MOSFET transistors.

2.2.1 KINK EFFECT

The kink-effect is observed in the DC IV characteristic of the PDSOI MOSFET. This effect is due to the secondary electrons and holes generated that are generated by impact ionization. The electrons get attracted to the drain across the channel, while the holes are trapped within the floating body. The accumulations of holes cause a forward bias between the source and body, hereby reducing the threshold voltage of the MOSFET. The lowering of the threshold voltage results in an increase in the drain current, to be seen as a kink effect. Figure 2.3 shows the kink effect of a PDSOI MOSFET.

Figure 2.3 DC IV characteristic of a PD-SOI MOSFET

2.2.2 LATCHUP

In a PDSOI MOSFET, the floating body acts as the base for the parasitic bipolar with the source and drain acting as the emitter and collector respectively. When the parasitic bipolar is turned on, a positive feedback path is established, resulting in an increase in the drain current. A hysteretic behavior can be observed while scanning the gate voltage. Once the bipolar is triggered, the drain current of the MOSFET cannot be cutoff. Such single transistor latch up effect will result in a loss of gate control [14].

To avoid the parasitic bipolar effects in PDSOI MOSFET, a substrate contact is added to the design. This however makes the PDSOI MOSFET design larger than the FD-SOI MOSFET design.

2.3 MULTIPLE GATE FULLY DEPLETED SOI MOSFET

The silicon film thickness of SOI is directly related to device scaling of planar FD-SOI. When the gate length is scaled down, a thinner silicon film is required. This is to maintain a full-depletion device. But a significant degradation in mobility is observed in device fabricated using silicon film thickness that is below 10 nm [15]. The mobility degradation is a result of an increased in the doping concentration in the channel that is needed to minimize the short channel effects. Multiple gate SOI structures are therefore developed to suppress the short channel effects, without compromising the mobility. The multiple gates can be realized through increased gate coverage, to achieve greater gate control over the channel.

Various multiple gate SOI structures such as double-gate [16], triple-gate [7], pi-gate and quadruple gate [11] have been proposed. Some of these structures are illustrated in Figure 2.4. They will be discussed in greater details in the section to follow.

Figure 2.4 Different configurations of SOI structures: a) double-gate; b) triple-gate; and c) quadruple gate.

2.3.1 DOUBLE-GATE SOI MOSFET

There are three types of double-gate SOI MOSFET structures, namely planar channel, vertical channel, and fin channel. They can be easily differentiated by the direction of the current flow as shown in Figure 2.5.

Figure 2.5 Different configurations of double-gate structures: a) planar channel; b) vertical channel, and c) fin channel.

The planar channel double gate MOSFET can be identified by the top and bottom gates with horizontal current flow direction. A major drawback of this design is the process complexity. Inserting the bottom gate is difficult, and aligning the bottom and top gates can also pose challenges. Misalignment between the top and bottom gates will result in a reduction in the drive current and also an increase in the overlapping capacitance.

In the case of the vertical double gate MOSFET, as the name implies, the current flows in the vertical axis. This design also suffers from high process complexity. Difficulty in defining the source and drain regions makes the device unsuitable for conventional CMOS process.

Among the three designs, the fin channel double gate MOSFET, also known as FinFET, offers the lowest process complexity. The gate length of the transistor can be defined through lithography, making the design very scalable. The Fin thickness (width), T_{si} is a critical factor for deriving a fully depleted device. The fin thickness is confined by the following equation, achieved from experiments and simulations [16]:

$$\text{Max Fin Thickness, } T_{si} = 0.7 * L_g \quad \text{Equation (2.3)}$$

where L_g is the gate length of the transistor.

Hence, the scalability of the double gate MOSFET is highly dependent on the lithography technology. Note that T_{si} and L_g of the FinFET are labeled in Figure 2.5.

2.3.2 TRIPLE-GATE SOI MOSFET

The increase in gate coverage on the channel has been proven to derive better performance devices. This sparks the exploration of triple-gate SOI MOSFETs. The increase in gate coverage improves the drive current and short channel performance. Three types of triple-gate MOSFET structures, namely the tri-gate, pi-gate, and omega gate had been developed to-date. Figure 2.6 presents the three triple-gate MOSFET designs.

The tri-gate is the basic type of triple-gate MOSFET design. It has an additional conducting top gate as compared to the fin channel double gate design. The additional gate allows the relaxation of fin thickness; hence the tri-gate is less taxing on the

lithography process as the device scales down to the sub-30 nm regime. The reduction in fin thickness is to increase the control of the channel and achieve full depleted body for double-gate to suppress short-channel effects. With additional gate added in triple-gate as compared to double-gate, there will be more control of the channel. Hence for triple-gate a larger fin thickness can be used in comparison to double-gate with the same gate length. The tri-gate design can attain full depletion up to a fin thickness that is equivalent to its gate length (L_g) [7].

Figure 2.6 Different configurations of triple-gate MOSFET structures: tri-gate; pi-gate; and omega gate, and their cross-sections.

The pi-gate design is a modification of the tri-gate type. The gate electrode takes the shape of the uppercase Greek letter Pi (Π), and hence its name. The design further improves the DIBL performance of the device through extending the gate electrode into the buried oxide (BOX). The extension helps to shield the back of the channel from the electric field lines coming from the drain end. The design is also manufacturable, by

simply adding an additional masking and reactive ion etching (RIE) step to the conventional SOI CMOS process [8].

The omega (Ω) gate MOSFET is an improvement from the pi-gate design. It adds a wet oxide etch step to undercut the gate for DIBL improvement. The undercutting also increases the gate coverage over the channel, to yield an increase in the drive current [17].

The triple gate MOSFETs exhibits coupling effects due to their three-dimensional (3D) configurations [18]. Due to the electrostatic influence of the top and side gates, the surface potential and threshold voltage varies along the gate electrode. It is found that the threshold voltage decreases in the region near the top gate (corner effect) as depicted in Figure 2.7. The corner effect cause early turn on and increases the leakage current. A hump normally can be notice from the second derivative of $I_d(V_g)$ plot (see Figure 2.8). The corner effect can be effectively suppressed by rounding the corners of the triple gate designs. Figure 2.9 describes the percentage of current contributed by the corner regions at subthreshold.

Figure 2.7 Cross-section of a triple gate device indicating the corner regions.

Figure 2.8 Second derivative of $I_d(V_g)$ plot for a triple gate device with square corners (hump) and round corners (no hump) [19].

Figure 2.9 Percentage of current contribution by the corners and non-corner regions of a triple gate device.

2.3.3 QUADRUPLE-GATE SOI MOSFET

Quadruple-gate SOI MOSFET structure is developed to allow maximum gate coverage over the channel. Quadruple-gate designs are also known as gate-all-round (GAA). This design offers the best electrical performances as compared to the triple-gate and double-gate designs. However, process complexity is the show-stopper [20] [21].

Additional processes are required to undercut the silicon channel to form cavity for the bottom gate. The GAA structure and its cross-section view are given in Figure 2.10.

Figure 2.10 (a) Three dimensional and (b) cross-sectioned view of the GAA MOSFET structure.

2.4 MULTIPLE GATE SILICON NANOWIRE MOSFET

Continual transistor scaling has led to development of nanowire multiple gate structures for sub-10 nm regime. For transistors with nano-scale gate length (L_g), it is vital that the channel conductance is controlled by the gate electrode instead of the drain. From previous review, both the double-gate and triple-gate MOSFET designs attain good short channel performance provided the fin thickness, T_{si} is equal or smaller than L_g . The nanowire multiple gate design is able to achieve a breakthrough, by allowing fin thickness, up to a maximum fin thickness of $2L_g$ [5]. This evolution is illustrated in Figure 2.11.

Figure 2.11 Evolution of nanowire multiple-gate MOSFET from double-gate and triple-gate MOSFET.

From the performance point of view, nanowire MOSFET is more superior as compared to other structures [5]. In Table 2.1, an electrical performance comparison of several sub-10 nm MOSFETs is tabulated. The nanowire FinFET is able to deliver the highest Ion/Ioff ratio and superior short-channel effect suppression. Double gate FinFET [46], is able to achieve a high Ion 10 nm gate length, in the expense of high subthreshold current. High subthreshold slope and DIBL are also expected with short-channel effect sets in. Ultra thin body planar SOI structures [47] [48] using high-k dielectric and metal gate, realize an EOT of 12 Å, which proves a effective alternative to suppress short-channel effects without increasing the gate coverage of the device. The current is enhanced with raised source/drain epitaxial silicon technique, with less concern on overlapping capacitance, due to ultra-thin silicon body. The conventional bulk transistor [49] shows high leakages even at low Vdd of 0.4 V and small EOT of 12 Å. This implies that conventional bulk transistors will likely to reach its limits at the sub-10 nm regime.

Table 2.1 Comparison of sub-10 nm MOSFET devices [5].

Structure	Double Gate FinFET	Planar SOI	Conventional Bulk	Nanowire FinFET
<i>L_g</i> (nm)	10	8	5	5 (PMOS) 10 (NMOS)
<i>V_{dd}</i> (V)	1.2	1.2	0.4	1
Electrical Oxide Thickness (EOT) (Å)	17	12	12	19
	NMOS/PMOS	NMOS/PMOS	NMOS/PMOS	NMOS/PMOS
<i>I_{on}</i> (μA/μm)	446 / 356	260 / 240	37 / 17	522 / 115
<i>I_{off}</i> (nA/μm)	150,000 / 200,000	300 / 300	5700 / 3100	10 / 0.5
<i>I_{on}/I_{off}</i>	3 / 1.8	867 / 800	6.4 / 5	52,200 / 230,000
Subthreshold Swing (mV/dec)	125 / 101	90 / 80		75 / 63
DIBL (mV/V)	71 / 120			80 / 14
CV/I (ps)		0.62 / 0.61		0.22 / 0.48

2.5 METHODS OF SILICON NANOWIRE FABRICATION

Nanowires can be fabricated using two major methods: 1) Non-lithography and 2) Lithography. Each of these methods will be discussed in details.

2.5.1 NON-LITHOGRAPHY METHOD

(I) Metal-catalyzed chemical vapor deposition technique:

The nanowires are grown using metal-catalyzed chemical vapor deposition (CVD) technique without any fine-scale lithography [22]. Gold (Au) or Titanium (Ti) nanoparticles are used as catalyst for the nanowire synthesis. A very thin layer of catalyst is deposited on the walls of the electrodes and annealed to form isolated nanoparticles of the catalyst material. The nanowires are grown using process gas such as SiH₄ or SiH₂Cl₂ as the precursor in a CVD system. To grow silicon nanowires, a small metal nanoparticle is required to accelerate the decomposition of a silicon containing gas (SiH₄ or SiH₂Cl₂). The isolated nanoparticle is obtained through annealing of the thin layered catalyst metal.

The silicon atoms precipitate at the interface between the nanoparticle and the substrate, forming a column of silicon, which the nanowire with the desired high surface-to volume ratio. Figure 2.12 illustrates the process of the nanowire growth using the metal-catalyzed CVD technique.

Figure 2.12 Metal-catalyst chemical vapor deposition nanowire growth process.

2.5.2 LITHOGRAPHY METHOD

(I) Inorganic electron-beam resist process:

The inorganic electron-beam (EB) resist process inherits the capabilities of the conventional EB lithography process that uses organic resist. Since inorganic SiO_2 resist is engaged, secondary electrons resulting from primary EB scattering are very much suppressed. This yields a higher resolution than the conventional organic EB resist process [23]. Inorganic EB resist process has high scalability with small deviations in critical dimension (CD). Therefore, the inorganic EB resist process is suitable for fabricating silicon nanostructure device where the design of shape, size, and position demand for precision lithography. Figure 2.13 shows the inorganic EB resist process used for nanowire fabrication.

Figure 2.13 Nanowire fabrications using inorganic EB resist process [23].

(II) Conventional lithography with hydrogen anneal

Silicon fins can be rounded at the corners and sides by annealing in hydrogen. This is due to the migration of silicon atoms on the surface of the substrate or silicon film [24]. With the rounding property of hydrogen anneal, silicon nanowires can be easily formed. Fin patterning can be done by conventional lithography process and trimming to achieve a small dimension of the fin. Finally, the nanowire formation is completed with a hydrogen annealing step at around 900 °C [5]. Nanowire fabrication is usually performed on SOI platform. It can also be carried out on bulk silicon using the damascene-gate process [12]. With the damascene-gate process, lateral twin wires can be fabricated, and hence enhancing the performance of the device. A series of processes are used to define the fins, and the wires are then formed by hydrogen annealing. The SiGe layer beneath the silicon channel is a critical layer in the process. SiGe has bigger grain size than Si and

hence, Si growth on SiGe will provide extra strain to boost the current drive. The SiGe layer also serves to provide the buffer layer necessary for creating the undercut in forming the GAA structure. After the development of the fins through damascene-gate process, a high SiGe to Si selectivity wet etch step is used to undercut the fins, to allow the wrapped around gate deposition. The damascene-gate process sequence is listed as follows, with Figure 2.14 enhancing the description:

- 1) SiGe / Si Growth and SiN deposition
- 2) Hardmask Silicon Nitride (SiN) trimming
- 3) Oxide fill in STI and chemical mechanical planarization (CMP)
- 4) Damascene gate stack deposition (Oxide and Nitride)
- 5) 1st damascene gate etch (Etch Nitride and Oxide)
- 6) 2nd damascene gate etch (Etch Nitride and Epi Silicon)
- 7) Field oxide recess (Etch oxide to exposed silicon and SiGe)
- 8) SiGe removal and H₂ anneal

Figure 2.14 Damascene-gate process for twin silicon nanowire formation [12].

(III) Conventional lithography with stress limited oxidation

The silicon fins is patterned using conventional lithography and etch processes. The fin is sent for oxidation using oxygen gas (DryOx) at 875 °C. Stress generated during oxidation prevents the nanowires to be oxidized completely. Figure 2.15 shows the oxide stress fields in an oxidation process. SiO₂ occupies a larger volume as compared to Si. As oxidation progress, newly formed oxide tends to push the older oxide outwards. At low temperature, high viscosity of the SiO₂ makes deformation of outer oxide layer difficult. This results in the stress been generated back to the Si and SiO₂ interface. This stress slows down the oxidation rate by making the transition of Si to SiO₂ less favorable. As a result of stress limited oxidation, small diameter silicon nanowires are formed [25]. With top silicon thickness of 200 nm, two nanowires – one at the bottom and other at the top can be formed on SOI platform. This is due to the different oxidation rates of the various silicon planes. The side of the fin that are at 110 plane oxidized two times faster than the top of the fin (at 100 plane).

- Stress from older oxide been pushed outward by newly formed oxide
- Stress at oxide-silicon interface
- Stress from the viscosity of the oxide

Figure 2.15 Illustration of oxide stress fields during oxidation process.

Annealing in hydrogen and at high temperature can be dangerous. Hence stress limited oxidation provides an alternative to the nanowire fabrication. From published results [5], [27], hydrogen anneal and stress limited oxidation have produced high performance devices at sub-10 nm gate length. Incorporation of high-k gate dielectric and metal gate are also feasible. These grounds have aroused research interest in further development of nanowire devices and will be elaborated in the next section.

2.6 NANOWIRE AND METAL GATE

Poly depletion effect has become an issue to transistor scaling in 45-nm technology node and beyond. The poly effect is the addition of electrical oxide thickness (EOT) contributed by the polysilicon gate electrode. The thinning down of gate dielectric is therefore essential as the devices scale down to suppress short channel effects. Metal gate therefore presents a solution to the poly depletion as it has low sheet resistance, and is able to solve the depletion effect.

To achieve a suitable threshold voltage for polysilicon device, channel doping is required. However, this leads to dopant fluctuation effects and low channel mobility due to scattering. In the case of metal gate, the workfunction of the metal can be engaged as a tuning parameter for threshold voltage adjustment. Various metals, for example element metals [28], [29], metal nitrides [30], metal oxides [31] and metal alloys [32], [33], and schemes such as metal silicides (FUSI) [34], [35], have been researched in recent years.

The polysilicon gate nanowire MOSFET has been reported to offer excellent electrical performances [5], [27]. Although high I_{on}/I_{off} ratio is achieved, polysilicon nanowire MOSFET suffers from high leakage current due to low threshold voltages. The solution proposed by Samsung researchers [12] employed a single metal gate for both the n- and p- nanowire MOSFETs in their CMOS process. Figures 2.16 to 2.17 illustrate the improvements of the devices when TiN gate is used to replace the polysilicon gate in nanowire MOSFETs. The improvement in the workfunction for the case of TiN gate is evident in Figure 2.16. Such improvement is attributed to the TiN gate, which is able to attain a higher threshold voltage for the n-type nanowire MOSFET, from -0.2 V to 0.24 V and at the same time keeps the leakage current low.

Figure 2.16 (a) $I_d - V_g$ characteristics of polysilicon gate nanowire NMOSFET and (b) $I_d - V_g$ characteristics of TiN metal gate nanowire NMOSFET.

Figure 2.17 provides the distribution plot of the shift in threshold voltage for NMOSFETs, which proves that TiN as a suitable gate material. The plot indicates that the shift in threshold voltage allows a two-order reduction in the leakage current.

Figure 2.17 Increase of threshold voltage and the reduction in leakage current with the introduction of TiN metal gate (for NMOSFET).

2.6.1 METAL GATE WORKFUNCTION

Gate workfunction is a crucial parameter in achieving a desirable threshold voltage as shown in Equation 2.4.

$$V_t = (\Phi_M - \Phi_S) + 2\phi_b + (Q_{dep} / C_{ox}) \quad (\text{Equation 2.4})$$

where, Φ_M and Φ_S are workfunctions of the metal gate and silicon respectively

$2\phi_b$ is potential required for inversion

(Q_{dep} / C_{ox}) is the potential drop across gate oxide

Figure 2.18 shows the energy band diagram of a typical NMOSFET to help in explaining the impact of gate workfunction and channel doping on threshold voltage of a device.

Note: E_f = Fermi energy level

Figure 2.18 Energy band diagram of a typical NMOSFET.

In planar devices, the dual metal gate process is necessary as NMOSFET needs a workfunction of 4.05 eV while PMOSFET requires 5.17 eV. This is due to the high channel doping used to suppress short channel effects; therefore band-edge metals are required.

For advanced transistor device such as FinFETs and nanowires, it is possible to use a single or dual mid-gap metal gate process. These advanced structures do not depend on high channel doping to suppress the short channel effects. In addition, the low doping concentration can improve carrier mobility, and reduces the dopant fluctuation effect. The effect of channel doping on threshold voltage with different gate workfunction is explained in Figure 2.19.

Figure 2.19 Impact of channel doping and gate workfunction on threshold voltages [36].

As indicated in Figure 2.19, in the case of low channel doping, to achieve a threshold voltage of 0.3 V, a mid-gap workfunction metal gate is required (Point A in Figure 2.19). On the other hand, if high channel doping is used to suppress short channel effects, the band-edge workfunction metal gate should be used (see Point B). Band-edge metals are metal with workfunction near the valance (E_v) and conduction (E_c) band, while mid-gap metals are those having workfunction of around 4.65 eV. Figure 2.20 explains and provides a list of band-edge and mid-gap metals.

Figure 2.20 Workfunctions of various gate electrode materials with reference to vacuum level.

2.6.2 FERMI-LEVEL PINNING

The effective workfunction of metal usually different from their vacuum workfunction. This is because the gate workfunction on high-k dielectric is “pinned” at an energy that is different from the vacuum workfunction [37]. When metal comes in contact with high-k dielectric, charge is exchanged between the surface states of the dielectric and the metal gate electrode. This interaction causes a formation of an interface dipole and the metal workfunction is pinned towards mid-gap [38]. This effect is called Fermi-level pinning. A higher threshold voltage usually is the result of this effect.

Recently studies [39] have shown that Fermi-level pinning effect increases with processing temperatures. For gate first approach, where gate electrode is defined before implantation and anneal steps, Fermi-level pinning effect will be more significant since

anneal steps are usually done at high temperatures. From Figure 2.21 it is evident that the metal workfunctions will be pinned towards mid-gap as the annealing temperature increases.

Figure 2.21 Increase of Fermi-level pinning effect on the metal workfunction with the annealing temperature.

2.7 SUMMARY

In this chapter, MOSFET basics like DIBL and subthreshold slope have been briefly covered. The advantages of fully depleted SOI with no kink effect and less prompt to latch-up in-comparison to partially depleted SOI devices. Various multi-gate fully depleted SOI structures, namely double-gate, triple-gate and quadruple-gate have been introduced. Nanowire MOSFET displays excellent electrical performances proves that it maybe alternative for sub-10 nm regime for planar transistors, with compatibility to high-k and metal gate. The next chapter shall present the fabrication of n-gate and gate-all-round SOI MOSFETs.

CHAPTER 3: FABRICATION OF N-GATE AND GATE-ALL-AREOUND (GAA) SOI MOSFET

In this project, device characterization is carried out on two proposed multiple-gate MOSFET devices: the n-gate and Gate-All-Around (GAA) devices. The former device is named n-gate due to the shape of the polysilicon gate, which reassembles the letter 'n'. Both device types are fabricated using Chartered Semiconductor Manufacturing Limited's 0.13- μm process. To better appreciate the device physics from the electrical data obtained, an in-depth understanding of the fabrication process is crucial.

3.1 FABRICATION OF N-GATE SOI MOSFET

The proposed n-gate MOSFET is an enhanced design of the basic tri-gate structure. Similar to other improved tri-gate designs, the sidewall gate electrodes are deliberately extended further, into some depths of the buried oxide, at both sides of the device channel. This will act as an actual back-gate to shield the electric field lines that are directed from the drain, to attain an enhanced gate-to-channel controllability [8]. The top surface of the silicon channel is made rounder to reduce the inevitable undesirable effects of the corner devices between the proximity of the two adjacent gates that are turn on together [7]. Figure 3.1 shows (a) sharp corner gate with coupling effect interaction of the corner two adjacent gate increasing the inversion layer density, causing a early turn on, (b) a rounded channel with a reduced inversion density eliminating corner effects.

Figure 3.1 Inversion layer densities for a square (a) and a rounded (b) corner.

3.1.1 ACTIVE AREA DEFINITION

The starting material is a SOI wafer with 1000 Å top silicon film and a 2000 Å BOX layer. Pre-pad oxidation clean with dilute hydrofluoric (HF), standard clean 1 (SC1) and standard clean 2 (SC2) are carried out at the start to remove unwanted particles or impurities. A 100 Å of pad oxide is grown to cushion the stress between the silicon and a thick layer of 1600 Å of nitride that is subsequently deposited. Positive deep ultraviolet (DUV) resist is coated to define the mask for the nitride and the pad oxide stack. The resist is exposed and developed to define the active area hard mask for the subsequent etch of underlying silicon. The etching of the top silicon film requires end point detection that allow stopping at the oxide, and a time based over-etch step. Figure 3.2 summaries the steps involved in the active area definition, while Figure 3.3 is the XSEM picture of the wafer after the silicon film etch.

Figure 3.2 Summary of active area definition flow: (a) Start wafer with wet clean; (b) pad oxide and nitride deposition; (c) Resist coating, developing and exposure; (d) Nitride hardmask etch, resist strip and active silicon etch.

Figure 3.3 XSEM picture of the wafer after active silicon definition.

3.1.2 CHANNEL ROUNDING PROCESS

A thermal oxidation step to grow a 150 Å sacrificial oxide layer over the exposed silicon body is used to round the sharp corners. A 1600-Å thick nitride layer is then deposited using the low pressure chemical vapor deposition (LPCVD). This nitride layer serves as the hardmask preceeding the two-stage n-gate shaping process. The channel rounding process is depicted in Figure 3.4. The main etch of Figure 3.4 (a) is first carried out to clear most of the nitride hardmask until it reaches the buried oxide etch-stop layer. A directional overetch step [see Figure 3.4 (b)] is then used to clear the nitride spacers at the sidewalls of the silicon body leaving the stubborn surface nitride intact. The surface removal actually helps to round off the silicon surface. The rounded shape of the initially formed hardmask after the main etch has been transferred onto the silicon channel. The final rounded Si profile is shown in Figure 3.4 (c). The shaped of the final Si is controlled by the main etch; hence the curvature of the channel is unlikely to be altered.

Figure 3.4 Two stage channel rounding process for the n-gate MOSFET.

To create gate extension into the buried oxide layer, a self-aligned RIE buried oxide etch step is engaged. The thermal oxidation process is employed to smooth the rough surface. This is followed by a rapid thermal annealing (RTA) step to heal the silicon lattice damages incurred during the nitride-etch bombardment. Once the channel is ready, the gate oxide is grown. This is followed by the deposition of a pre-doped polysilicon layer. Gate patterning that defines the gate electrode, spacer formation, source/drain implants and finally a salicidation step completes the n-gate device formation process.

In Figure 3.5, a cross-section scanning electron microscopy (XSEM) picture of an n-shaped structure is presented. It is evident that the structure has a smooth and rounded top surface. The thickness of the body is about 960 Å and the gate extension depth is ~550 Å into the buried oxide. The top-SEM micrograph of Figure 3.6 is an n-gate single-channel transistor structure with a 0.13- μm gate electrode and extended source/drain.

Figure 3.5 Rounded silicon channel with buried oxide extension etch.

Figure 3.6 Top view SEM of n-gate MOSFET structure.

3.2 FABRICATION OF GATE-ALL-AROUND (GAA) SOI MOSFET

A novel fabrication process of achieving the Gate-All-Around (GAA) SOI MOSFET device using the replacement gate mask method is discussed in this section. The main features of the fabrication process are the development of the replacement gate hardmask and the formation of the bottom gate electrode using an isotropic etch. The concept involves eliminating the masking step required for the provision of the cavity etch using a hardmask. With the removal of an additional masking step, the process becomes compatible with the conventional bulk process [26]. The penalty for removing the masking step is however the addition of other process steps. Then again, these added processes do not entail critical dimensions considerations and hence, the process complexity remains manufacturable. Having single masking step for gate patterning and cavity etch is the best approach for suppressing gate misalignment.

3.2.1 REPLACEMENT GATE PROCESS

The concept of replacement gate process uses the original gate mask to perform a reversal definition of the gate. In other words, the area that is supposed to form the gate electrode will create a gate trench instead.

The active region is first defined using the conventional bulk CMOS processing steps similar to the n-gate active area definition process discussed in section 3.1.1. Upon removing the first nitride layer from the active device region, a stack layer of 1600 Å nitride / 150 Å oxide / 1600 Å nitride is deposited. The replacement gate mask is implemented next to create a hardmask for cavity etching at later steps. The gate hardmask is patterned, etched and stopped selectively at the sacrificial oxide layer as shown in Figure 3.7.

Figure 3.7 Nitride profile after reverse gate mask exposure and nitride etch.

High density plasma (HDP) oxide of 3000 Å thick is then deposited to cover the patterned nitride. HDP oxide is used due to its good gap-fill properties. The oxide is required to be uniformly deposited and filled over the brink of the nitride strips to provide tolerance for the following chemical mechanical polishing (CMP). The HDP oxide deposition profile is captured in Figure 3.8. A capping layer is laid on top of the sample to prevent surface oxide removal during buffered oxide etch, for achieving better contrast for viewing.

Figure 3.8 HDP oxide deposition profile with over-fill of ~1400 Å for CMP tolerance.

A time-based oxide CMP step planarizes the surface and the polishing terminates upon detecting the nitride strip. The nitride strip is removed via wet chemical etch using hot phosphoric acid. Figure 3.9 presents the XSEM of the wafer after nitride stripe removal. It is noticed that the CMP process has etch away ~400 Å of oxide.

Figure 3.9 XSEM profile after CMP and hit phosphoric acid dip.

The 150 Å thin oxide layer beneath the nitride strip is then etched away. Thereafter, a nitride etch is carried out to exposed the gate region. This step creates the hardmask for cavity etching in subsequent step. The HDP oxide hardmask is removed together with the nitride during the nitride etch. The exposed silicon channel is subjected to thermal oxidation to produce 200 Å of oxide to round the channel edges. The oxide produced also serves as a protective layer for the subsequent cavity etch. Diluted hydrofluoric (HF) etch is used for undercutting the oxide beneath the silicon channel. The sacrificial oxide covering the silicon channel will also be removed by the diluted HF solution. A XSEM picture in Figure 3.10 displays the structure profile after 125 seconds of diluted HF dip.

Figure 3.10 XSEM profile after 125 seconds of diluted HF undercut.

A conformal 20 Å gate oxide is grown prior to depositing the polysilicon gate. The polysilicon is pre-doped to minimize poly depletion effect. After CMP and nitride hardmask removal, transistor fabrication can be completed with spacer formation and cobalt silicidation. A summarized fabrication flow is presented in Figure 3.11.

Figure 3.11 Fabrication flow of GAA devices using replacement gate mask.

In Figure 3.12, a GAA SOI structure (cross-sectional view) that has a 750 Å thick silicon channel that is surrounded completely by a polysilicon gate is shown. The top-view-SEM micrograph of Figure 3.13 is a GAA single-channel transistor structure with a 0.13-μm gate electrode and a source/drain overhang of around 3 μm long.

Figure 3.12 XSEM of a 0.15 μm channel width GAA structure with silicon channel bounded by polysilicon gate.

Figure 3.13 Tilted SEM profile of a 0.12 μm gate length GAA structure at a magnification of 50000×.

3.3 SUMMARY

In Chapter 3, detailed fabrication processes of both n-gate and GAA have been discussed. Novel channel rounding technique is introduced and integrated in the standard 0.13 μm process successfully. The gate replacement process for GAA fabrication is also added in the standard flow. Working devices of both n-gate and GAA are extracted and the electrical characterizations will be presented in the following chapter.

CHAPTER 4: DEVICE CHARACTERIZATION (N-GATE AND GATE-ALL-AROUND)

The electrical performances of both the n-gate and GAA SOI MOSFET will be presented in this chapter. The relationship between the gate coverage and the device performances have been investigated and will be discussed in detail. Some simulation data will also be included to evaluate the device performances at smaller dimensions. All nominalization are done through averaging using the channel width. Before presenting the results, there are several key electrical parameters to be defined. These key parameters include:

1) Threshold voltage (V_t)

For physical measurements, V_t is defined as the value of gate voltage (V_{gs}) required to achieve a drain current (I_{ds}) of $0.1 \cdot (W/L)$ μA , where W is the channel width and L is the channel length.

Two threshold voltages are used, namely the linear V_t (VT_LIN) and saturated V_t (VT_SAT). VT_LIN is threshold voltage measured at small drain voltage (V_{ds}), while VT_SAT is threshold voltage obtained at high drain voltage. By taking the difference between the two threshold voltages, short channel effect performance can be determined. Further details in the calculations to determine the short channel effect performance is explained in the next paragraph. The difference in the two threshold voltages are due to increase in drain voltage and shorter channel length as explained in Chapter 2, Section 2.1.1.

2) Drain induced barrier lowering (DIBL)

DIBL is a short channel effect performance indicator. In electrical perspective, it is the normalized shift of V_{T_LIN} and V_{T_SAT} , measured in mV/V. Shown below is the equation used to calculate DIBL:

$$DIBL \text{ (mV/V)} = 1000 * (V_{T_LIN} - V_{T_SAT}) / (\text{Difference in } V_{ds}) \quad \text{Equation (4.1)}$$

3) Subthreshold slope (SUBSLP)

SUBSLP (mV/dec) is the difference in V_{gs} required to cause a decade increment in I_{ds} within the subthreshold region. There are two subthreshold slopes to be determined: one in linear mode (SUBSLP1), while the other in saturation mode (SUBSLP2).

4.1 CHARACTERISTICS OF N-GATE MOSFET

4.1.1 ELECTRICAL PERFORMANCE OF N-GATE

In Figure 4.1, the drive current is plotted as a function of the drain voltage for different gate overdrives. The narrow-width 0.12- μm n-gate NMOS transistor displays a drive current capability of 597 $\mu\text{A}/\mu\text{m}$ (normalized with the widths of the transistors) at V_{gs} of 1.2 V. Conventional boron implantation is used to achieve an acceptable threshold voltage. The used of a lower channel doping concentration is desirable for maximizing the carrier mobility and hence the drain current. The extracted threshold voltage, V_t , which is noted to be of 0.227 V with a corresponding I_d of 125 nA. The device transconductance, G_m , which is the slope of I_d versus V_d curve in the linear region, is observed to be steep (refer to Figure 4.2). This implies that a low parasitic resistance has been achieved through the used of cobalt silicides in the source/drain regions.

Figure 4.1 I_d - V_d characteristics of a narrow width 0.12- μm n-gate NMOSFET.

Figure 4.2 I_d - V_g characteristics of a narrow width 0.12- μm n-gate NMOSFET.

On ultra thin films, silicidation is not effective as the entire silicon thickness will have to be consumed and this leads to high resistances. The optimum silicide thickness should be trimmed to approximately 80% of the total silicon film thickness [40]. The use of a selective epitaxial growth to increase the thickness of the source/drain regions (elevated source and drain region) [41] is a possible alternative, but this technique is not used in this work.

The proposed n-gate device managed to attain excellent short-channel characteristics (See Figure 4.3) with a near ideal subthreshold slope of 65 mV/dec for the linear region and 66 mV/dec at the saturation region. The excellent subthreshold slope achieved by the n-gate SOI device therefore allows the use of smaller threshold voltages when compared to the bulk devices, without having to increase the leakage current at zero gate bias. As a result better speed performance can be obtained, especially at low operating voltages.

The drain induced barrier lowering (DIBL) of the proposed n-gate device is 79.09 mV/V and the off-state leakage current, I_{off} , is only 5.28 nA/ μm at V_{ds} of 1.2 V (refer to Figure 4.3). The low leakage current can be attributed to the gate-extension beneath the buried oxide, which plays an important role to shield-off the strong electric field induced at the bottom of the silicon channel directed from the drain. This shield helps to lower the standby current. The complete absence of the “hump” effect [19], that is illustrated in Figure 2.3 is denoted in the transistor subthreshold characteristics. This indicates that the n-gate design with rounded corners helps to eliminate corner effects that can lead to a

related increase in the off-state leakage current. The experimental results have proved that the short-channel effects are attenuated in the narrow-width n-gate device. However it should be noted that the DIBL reading is slightly higher than expected. By examining the gradient of the curves at the subthreshold region in Figure 4.3, a slight deviation in parallelism is observed. We can conclude from the difference in gradient that the device is not fully depleted, due to high channel width to channel length ratio.

Figure 4.3 Subthreshold slope and off-state leakage current characteristic of a narrow width 0.12- μm n-gate NMOSFET.

4.1.2 N-GATE SIMULATIONS

In order to investigate the scalability of the n-gate SOI structure, having small gate lengths and fin-widths, simulation study is carried out. Using realistic doping

profiles imported from a 2D process simulator, TSUPREM4 taken from Chartered's 0.13 μm process, a pseudo 3D simulation is performed mainly on just two veritable device parameters: channel length and fin-width. The structure is created using MESH3D and device simulations are done using DESSIS (Device Simulation for Smart Integrated Systems) [42]. In this simulation, the gate oxide thickness is assumed to be uniform, and there are no gate oxide thinning at the edges of the silicon island. 3D device simulations allow the short channel effects of the structure to be explored. For this study, the channel length and fin-width are varied. Their dimensions are chosen to be smaller than those fabricated, ranging from 20 nm to 60 nm. The channel dose is set to $1 \times 10^{18} / \text{cm}^3$ and the gate oxide thickness is 30 Å. The buried oxide thickness is chosen to be 200 nm, which is the same thickness used in the proposed SOI devices.

The threshold variation using different channel lengths, for two samples that are of different fin-widths, have been simulated and the results are presented in Figure 4.4. From the figure, it is noted that the threshold voltage decreases with channel length. The gate potential that is required to invert the channel region is observed to reduce with the distance between the drain and the source regions. The drop in threshold voltage is more drastic for devices that have longer fin-width. This indicates that short channel effect improves with narrower fin-width. The increase in fin-width results in an increased dependent on the floating body effect, whereby the potential is able to rise as the drain charge leaks through the drain-body junction diode. The threshold voltage of the device is then lowered, which complements the natural barrier lowering of normal CMOS devices at short channel lengths. The body voltage will rise, and this will initiate a drop in the

threshold voltage to cause degradation in the short-channel performance. On the other hand, as the channel length increases, the ratio of the channel length to the fin-width escalates, and this helps to improve the short-channel performance, stabilizing the threshold voltage.

Figures 4.5 and 4.6 depict the subthreshold slope and the drain-induced barrier lowering (DIBL), and the results derived for various ratios of channel length/fin-width respectively. It is clear that those with higher channel length/fin-width ratio can deliver better short channel performances, but at the expense of a lower drive current. Hence it is essential to strike a balance between the drive current and the short channel performances. The criterion of DIBL = 100 mV and subthreshold slope = 100 mV/decade for acceptable short channel behavior that is established by [43][44] is adopted in our study. Based on Figures 4.5 and 4.6, an optimum ratio (channel length/fin-width) for achieving an acceptable short channel behavior can be expressed as follows:

$$\frac{\text{channel_length}}{\text{fin_width}} > 1.3 \quad (\text{Equation 4.2})$$

In other words, the fin-width must be smaller than 3/4 of the channel length for good control of short channel effect.

Figure 4.4 Simulation data of threshold voltage variation as function of channel length.

Figure 4.5 Simulated DIBL characteristics showing acceptable DIBL value achieved at minimum channel length / fin-width ratio of 1.3.

Figure 4.6 Simulated subthreshold characteristics whereby acceptable subthreshold slope is obtained at minimum channel length / fin-width ratio of 0.78.

4.2 CHARACTERISTICS OF GATE-ALL-AROUND (GAA) MOSFET

4.2.1 ELECTRICAL PERFORMANCE OF GATE-ALL-AROUND (GAA)

Figure 4.7 shows the I-V plots of the GAA transistor. The narrow-width 0.12- μm GAA SOI NMOS transistor presents a drive current capability of 800 $\mu\text{A}/\mu\text{m}$ at $V_g = 1.2$ V, with off-state current of 230 nA/ μm . The high drive current achieved is credited to the multiple surface inversions throughout the entire surface of the thin silicon body. The low V_t of 0.075 V has led to a high leakage current. This low V_t is due to the low work function of the poly gate as discussed in Chapter 2 Section 2.6.1. Hence, the leakage current recorded does not reflect the actual off state current of the GAA device. A metal gate can be used to achieve a proper V_t , to access the true performance.

Figure 4.7 I_d - V_d characteristics of a narrow width 0.12- μm GAA NMOSFET.

The GAA SOI device attains excellent short-channel characteristics. A near-ideal subthreshold slope of 65 mV/dec and 69 mV/dec at the linear and saturation operating regions are respectively observed. A low DIBL reading of 31.82 mV/V is obtained (refer to Figure 4.8). The bottom gate extended into the buried oxide underneath the active silicon channel; effectively shielded the back of the channel region from the electric field lines directed from the drain. Slight increase in leakage current is noticed at high negative gate voltage. This is slightly due to the lightly doped channel forming a p-type accumulated channel allowing minority carriers to flow. This current is a small current that will saturates with the limited minority carrier from the source.

Figure 4.8 Subthreshold slope and off-state leakage current characteristic of a narrow width 0.12- μm GAA NMOSFET.

4.2.2 GATE-ALL-AROUND (GAA) SIMULATIONS

Simulations have also been performed on GAA structure to determine its scalability. Figure 4.9 demonstrates that even at small dimensions, GAA devices are able to display good short channel effect performances. The maximum fin-width / channel ratio of GAA is approximately two times of n-gate. This implies that the design will be less taxing on lithography. Wide-width transistors are not characterized in this project as it is irrelevant in concluding the performances of the devices and as mention in the literature review Chapter 2 (Section 2.3.4), increasing the width will degrade the short channel effect performances of multiple gate SOI devices. An indirect way of increasing the channel width is the implementation of multiple finger devices. As multiple finger

layouts are not available, the electrical performance of wide-width MOSFET cannot be carried out.

Figure 4.9 Simulation results: DIBL and subthreshold characteristics of GAA as a function of different width.

4.3 GATE COVERAGE AND DEVICE PERFORMANCE RELATIONSHIP

Figures 4.10 (a) to (d) depict different gate configurations that are fabricated to explore the effect of gate electrode extension undercut on the GAA NMOS transistor electrically. Figure 4.10 (a) is a basic triple gate design with the poly gate electrode extending into the buried oxide, without any undercut beneath the silicon channel. Figures 4.10 (b) to (d) represent designs that have different undercut configurations, created using the replacement gate mask process. The structure in Figure 4 (b) is an omega-gate structure that is in fact an improved design of the triple-gate with additional

undercut. The improved omega-gate structure differentiates with the omega-gate structure with increase gate coverage. GAA structure shown in Figure 4 (d) is designed to have the most gate coverage, with the whole silicon channel surrounded by the gate electrode. These designs are subjected to different etch timings at: b) 100 seconds; c) 125 seconds and d) 150 seconds respectively.

Figure 4.10 Different gate configurations base on various degree of undercuttings beneath the silicon channel: (a) Triple-gate [no etch], (b) Omega-gate [100 sec], (c) Improved Omega-gate [125 sec] and (d) Gate-all-around [150 sec].

In Figure 4.11, a comparable drive current of approximately $600 \mu\text{A}/\mu\text{m}$ is noted for device structure with an undercut timing of 100 seconds as well as for the triple gate structure that has no undercut. The highest drive current of approximately $800 \mu\text{A}/\mu\text{m}$ is attained in the optimized GAA device that has an undercut of 150 seconds. Generally, the results indicate a rising trend of drive current with longer etch timings. GAA device displays an improvement of 33.3% in drive current over the triple-gate device.

Figure 4.11 Drive current characteristics for different gate configurations.

Figure 4.12, shows the subthreshold slope and the DIBL of the device structures. The subthreshold slopes for the four device structures are quite consistent and are close to the ideal theoretical value of 60 mV/dec. The small variations in the threshold slope readings between different gate configurations maybe due to measurement variations. The improvements of subthreshold slope with more gate coverage are expected, but due to the use of the 0.13 μm process, the improvements cannot be determined physically. It is likely to observe improvements if the gate length of the devices are reduced significantly.

Figure 4.12 DIBL and subthreshold slope characteristics for different gate configurations.

The simulation results in Figure 4.13 taken from a researched paper [20], indicates that at small dimensions, the GAA device has a better subthreshold performance as compared to the triple gate design. This implies that increment in gate coverage does improve subthreshold slopes. The gate coverage experiment should be carried out on smaller device dimensions to yield more significant results.

Figure 4.13 Simulated data of subthreshold slopes in SOI devices with different gate structures and gate lengths.

The DIBL of all devices are kept at below 100 mV/V, with the GAA device structure leading in DIBL suppression. The improvement in drive current and short channel effect characteristics can be due to the increase in gate controllability over the channel as the amount of undercut beneath the silicon channel increased. The increment in drive current is attributed to the increase in surface inversion. The effective suppression of the short-channel effects are due to the gate electrode shielding that surrounds the channel, with electric field directed from the drain at high drain bias.

CHAPTER 5: NANOWIRE MOSFET FABRICATION

Silicon nanowires have recently been explored as a potential structure for sub-10 nm MOSFET applications [5]. This structure is proven to yield devices that have better subthreshold performances. Larger fin width/ fin length ratio is allowed while maintaining full depletion of the body relaxes the strain on lithography. The fabrication of the proposed nanowire MOSFET structures are carried out in the Institute of Microelectronics (IME) in Singapore. The focus of this research is on nanowire formation on thin SOI platform. Thin SOI allows the exploration of dual wire devices, which are devices having two thin wires that collectively serve as the channels. The dual wires are fabricated using the stress-limited oxidation technique, which has yet to be examined. The implementation of metal gate will be another focus of the project. The mid gap metal, TaN is utilized in the proposed dual nanowire MOSFET to adjust the threshold voltages thereby reducing the leakage currents.

5.1 LITHOGRAPHY AND RESIST TRIMMING

Before nanowire formation can be performed, a silicon fin structure is required. This is achieved with double exposure lithography technique. The fin structure is the result of a combination of two lithography exposures with two different masks (See Figure 5.1). In other words, the fin pattern is produced by a second pattern superimposed on the first pattern. This allows recycling of masks, without a need to create new mask sets.

The fin width is a critical parameter in determining the oxidation time for nanowire formation. A smaller fin width will require a shorter oxidation time while a larger one a longer oxidation time to form nanowires. The fin width is kept at a range of 40 nm – 50 nm, due to the limitation of thin top silicon. Fin width that are larger than 50 nm will require longer oxidation time, which may result in the breaking of the top nanowire channel. This issue is further elaborated in section 5.3.2.

Figure 5.1 Double exposure lithography and resist trimming process

5.2 FIN ETCH

The patterned fin structure is etched using dry etch process. The buried oxide layer (BOX) act as a etch stop layer for this step. Etching stops when the oxide is reached. As an oxide layer of 1500 Å thick is seen as cyan while silicon appears silvery, visual inspections can be used to ensure all unwanted silicon areas are completely removed. Etching is completed when the wafer turns cyan in color. A vertical etch profile is also required in this step. A sloped etch profile will alter the plane of the silicon fin at the sidewalls and this will cause the formation of dual nanowire channel impossible. The active area silicon which is the left over is a fin structure shown in Figure 5.2.

Figure 5.2 SEM pictures of 500 nm and 300 nm fin structures after etch.

5.3 NANOWIRE FORMATION

Several rounds of stress-limiting oxidation are carried out to evaluate the nanowire formations using different oxidation timings and SOI thickness. This allows a better understanding of the limitations and issues involve in nanowire formation using thin SOI thickness.

5.3.1 500 Å SOI AND 400 Å POI SUBSTRATE

500 Å top silicon film SOI substrate is used. In this experiment, to form the nanowires using stress-limiting oxidation technique while preventing the source/drain silicon pad from been oxidized, plasma enhanced chemical vapor deposition (PECVD) silicon nitride is deposited to provide a protective layer. Lithography is done to expose the channel area (removing of nitride) for oxidation; it is unfortunate that the nitride spacer is formed at the sidewall of the silicon channel after nitride etch [see Figure 5.3 (a)]. Removing the nitride spacer is crucial as oxidation will be hindered. An over-etch step is hence required to remove the nitride spacer. But the etch process leads to the

etching of the silicon channel, reducing the silicon thickness to 200 Å as shown in Figure 5.3 (b). After 5 hours of oxidation at 875°C, the channel is completely oxidized.

Figure 5.3 (a) Fin structure after nitride etch with sidewall spacer; (b) after over-etch step to remove the spacer.

To overcome the nitride spacer issue, the nitride hardmask for fin etch is proposed [see Figure 5.4 (a)]. A layer of silicon oxide and nitride are deposited prior to fin lithography. This experiment is done using polysilicon-on-insulator (POI) substrates since SOI wafers are expensive. For trial purposes, the POI substrates are engaged for all later part of the nanowire work. After fin lithography, the polysilicon fin with the nitride hardmask sheltering the source/drain pad and the top portion of the channel is sent for oxidation. The wafers under went 4 to 5 hours of oxidation. The nitride hardmask is stripped using hot phosphoric acid and the wire is released after 4 to 6 minutes of HF dip.

Wafer that has undergo 5 hours of oxidation can attain single nanowire that ranges from 42 nm to 48 nm [see Figure 5.4 (b)] diameter, while 4 hours oxidation yield nanowire with diameter of 16.5 nm to 20 nm [see Figure 5.4 (c)] . For this experiment, polysilicon are oxidized from the sidewall as the top is sheltered by nitride. Wafers that

have shorter oxidation time have smaller fin width as compared to those that are given longer oxidation duration. The difference in fin widths is caused by the variation in the fin etch process. From this experiment, it can be certain that the fin width is an important parameter determining the final nanowire diameter as well as the oxidation time required. The rough surface of the polysilicon noted in Figure 5.4 (b) and (c), is developed during the polysilicon deposition step. The surface condition is worsening through the use of HF, as HF etches and further deteriorates the surface roughness. Due to the surface roughness, it is concluded that polysilicon is not capable of producing fine nanowires of less than 10 nm, as fine nanowires will be too fragile to survive after the HF dip.

Figure 5.4 (a) device structure after fin etch; (b) polysilicon nanowire release after 5 hours oxidation; (c) polysilicon nanowire after 4 hours oxidation.

5.3.2 700 Å SOI SUBSTRATE FOR DUAL NANOWIRE

Dual nanowires can be achieved using self-limiting oxidation with 700 Å and above SOI substrate. Since the sidewalls of the fin oxidizes faster as compared to the top of the fin, increasing the surface area of the fin which is the thickness of the top silicon film of the SOI substrate will be able to yield dual nanowires.

The two conditions listed below are critical for the dual nanowire formation for 700 Å SOI substrate:

- 1) fin width of an average of 50 nm after the fin etch and
- 2) oxidation time of 5 hours at 875°C.

Fin width is a critical parameter in determining the oxidation time for nanowire formation. Smaller fin width will require a shorter oxidation time while a larger one require a longer oxidation time. The fin width is kept at a range of 40 nm – 50 nm, due to the limitation of the thin top silicon. Fin widths that are larger than 50 nm will require a longer oxidation time, but this may result in the breaking of the top nanowire channel. Figure 5.5 shows the nanowires that are formed under various oxidation timings.

Figure 5.5 (a) silicon fin which is under oxidized; (b) nanowire formation with proper oxidation timing; (c) nanowire been over oxidized.

The various stress-limiting oxidation process carried out in the project, have allowed some observations to be noted. The silicon fin is oxidized more at the sidewall compared to the top and bottom region of the fin. This oxidation profile allows the formation of dual nanowires. It is also noticed that the top silicon thickness will

determine the in different nanowire that are to be formed. In Figure 5.6, different nanowire structures formed using varying top silicon thickness and oxidation timings are illustrated. Typically three zones are drawn; the ultra thin top silicon substrates of 30 nm to 50 nm are named in Zone 1, where single nanowire structures are formed. Substrates with top silicon thicknesses of around 60 nm to 90 nm, that will lead to dual nanowire with a thin silicon bridge connecting the two nanowires are grouped in Zone 2. Any top silicon thicknesses above 90 nm will result in dual nanowire without the silicon bridge (Zone 3). The oxidation timings are varied with different top silicon thickness to prevent over oxidation, damaging the nanowires and also ensuring formation of small diameter nanowires.

Figure 5.6 Formation of different with varying SOI thickness and oxidation time.

5.4 METAL GATE DEPOSITION

Unlike planar devices that require two metal gate processes, single material metal gate process is suitable for nanowire MOSFETs. Nanowire channel is not doped or lowly doped; hence using a single mid-gap metal is sufficient to achieve a suitable threshold voltage. The threshold voltage equation shown in Equation 2.3 indicates that a balance of gate workfunction and channel doping is required to obtain a reasonable threshold voltage. A higher gate workfunction will entail a lower channel doping.

A brief study on two types of metal gate; TaN and TiN are conducted. It is found that after deposition of the metal gate, the nanowires started to deform as shown in Figure 5.7. TiN produces higher stress on the nanowires as compared to TaN hence TaN is further examined. The explanation of TiN being higher stress than TaN is not known, but it may be possibly due to the difference in the mechanical properties of the two materials. Different recipes of TaN are used to locate the best procedure in depositing the metal gate. The thickness of TaN is altered and both high stress and low stress recipes (warpage test on different recipes are done to determine the stress level of the recipes) are used. The nanowires started to deform with 500 Å and 700 Å of TaN and deformation is worsening in the case of high stress recipe. Transmission Electron Microscopy (TEM) is also done to inspect the uniformity of the deposition. The TEM picture as seen in Figure 5.8, confirmed that the deformation is not caused by non-uniform deposition. It is likely that the stress causing the deformation is induced by the metal itself. It is also noticed that stress and deformation on the silicon nanowire channel increases with the thickness of

metal gate deposited. This limits the thickness of metal gate to be deposited as highly stressed long nanowire channel are likely to snap after metal deposition.

Figure 5.7 (a) nanowire before metal deposition; (b) TiN deposition; (c) low stress TaN deposition; (d) high stress TaN deposition; (e) 300Å low stress TaN deposition; (f) 500Å low stress TaN deposition; (g) 700Å low stress TaN deposition.

Figure 5.8 TEM of the structure after 700Å low stress TaN deposition.

5.3 NANOWIRE MOSFET PROCESS FLOW

With the oxidation parameters and metal gate material finalized, the nanowire MOSFET process flow can be drafted. SOI wafers with 70-nm p-type ($\sim 10^{15}/\text{cm}^3$) top silicon and 150-nm buried oxide (BOX) are used as starting materials. The use of thin SOI layer allows thinner metal gate layer to be deposited, preventing nanowire channels to be over-stressed and snap in the process. In other words, the distance between the top and bottom nanowire channel is reduced with thin top silicon, and this allows thinner metal gate to be deposited. In this case, the overlapping metal gate can be replaced with non-overlapping gate configuration as the gate of both nanowire channels are readily connected. The high overlapping capacitance induced by the overlapping gate configuration can also be eliminated. Figure 5.9 shows both the overlapping and non-overlapping gate configuration.

Figure 5.9 (a) Overlapping gate configuration; (b) Non-overlapping gate configuration.

Double exposure lithography technique and resist trimming are performed to achieve a fin width of 50 nm. After each trimming process, the fin structures are measured randomly using critical dimension surface electron microscopy (CD-SEM) to ensure the fin widths are within specifications. The wafers are etched using the reactive ion etch (RIE) to form the three-dimensional fin structure presented in Figure 5.10 (a). The fin structure is sent for dry oxidation at 875°C for 4 to 5 hours depending on the fin width [See Figure 5.10 (b)]. With well controlled self-limiting oxidation process, dual nanowire channels that are connected by a thin silicon bridge can be established. The oxidation process made use of the different oxidation rates of the various silicon planes to form the two nanowires. The sides of the fin that are at 110 plane oxidized two times faster than the top of the fin (at 100 plane). With the close proximity of the two nanowires, and the precisely controlled oxidation parameters and timings, a thin silicon bridge can be formed. The oxidized structure is later released with a DHF dip. The HF dip also undercuts the BOX layer to facilitate the development of the wrap around gate. Figure 5.10 (c) shows the dual nanowire upon oxide removal.

Figure 5.10 (a) Fin structure after RIE etch; (b) 5 hours self-limiting dry oxidation; (c) Dual nanowire channel after DHF dip.

A high quality gate oxide of 20 Å is then grown, followed by a 30-Å HfO_2 deposition to complete the gate dielectric stack. Oxide is grown before HfO_2 deposition to eliminate fermi-pinning effect and preventing mobility degradation caused by poor HfO_2 and silicon interface. 800 Å of TaN that wraps around the nanowire channel is then deposited using Physical Vapor Deposition (PVD), for improving the electrostatic control of the device [See Figure 5.11 (a)]. The TaN gate electrode is patterned with a triple-layered hardmask (Oxide-Nitride-Oxide) process. Two hardmask etching steps with additional wet processes in between are required to provide a clean TaN etch [see Figure 5.11 (b) and Figure 5.12 (a)]. Short wet etch processes are added to remove unwanted spacers, to allow a clean etch with a minimum TaN gate over-etch time. A long TaN over-etch time will cause a “gate disconnection”, which discontinue the gate as shown in Figure 5.12 (b).

(a)

(b)

Figure 5.11 (a) 800-Å TaN metal gate deposition; (b) Triple-layered hardmask and TaN etch.

Figure 5.12 (a) Clean TaN gate etch; (b) Discontinued TaN gate after metal gate etch.

BF₂ and As of dose $4 \times 10^{15} \text{ cm}^{-2}$ with 10 keV and 20 keV energies for the p- and n-dual nanowire MOSFETs respectively are engaged for the implantation step. To form the source and drain, the device is given a short 10 sec S/D activation anneal using the rapid thermal anneal (RTA) system. A 4000-Å plasma enhanced chemical vapor deposition (PECVD) oxide is deposited prior to contact patterning. The 4000-Å oxide is etched to form contact holes followed by a short nitride etch. The nitride etch is used to remove the nitride hardmask left over at the gate pad after the metal gate etch. Since the silicon source and drain pads are not protected by resist or nitride layer, they are also being etched during the nitride etch step. This results in thinning of the source and drain pads, which translates to higher source and drain resistances. Typically, after the two contact etch steps, 300 to 400 Å of source and drain silicon pads are left. Figure 5.13 (a) presents the SEM picture of the structure after the contact etch steps.

Single layer metal is used in the process, where aluminum is utilized to fill the contact holes and patterned. SEM inspection system is used to verify no short circuit of

gate, source and drain contacts [See Figure 5.13 (b)], before ending the process with a metal sintering at 430°C. A summary of the process flow is given in Figure 5.14.

Figure 5.13 (a) SEM of the structure after 4000 Å oxide deposition and contact etch; (b) SEM inspection after aluminum etch ensuring no short circuit of contacts.

- Fin patterning and trimming
- Fin etch
- Self-limiting oxidation
- Oxide removal and undercut
- Gate oxide deposition
- TaN gate and hardmask deposition
- 1st and 2nd hardmask etch (with additional wet etch steps)
- TaN etch
- S/D Implantation and anneal
- Contact formation
- Metallization and sintering

Figure 5.14 Dual nanowire MOSFET process flow.

CHAPTER 6: DEVICE CHARACTERIZATION (NANOWIRE MOSFET)

In this chapter the electrical performance of the dual nanowire MOSFET device is presented and discussed. The benefits on the use of the metal gate will also be emphasized. A comparison of the polysilicon gate and metal gate nanowire MOSFETs explicates the performance enhancement. Various MOSFET current-voltage (I-V) characteristics extracted from the nanowire devices are detailed.

6.1 DUAL NANOWIRE MOSFET STRUCTURE

The dual nanowire metal gate MOSFET structure fabricated in this project consists of two 5-nm diameter nanowire bridged by a narrow 1-nm silicon bridge as depicted in the TEM picture and schematic diagram of Figure 6.1.

Figure 6.1 (a) TEM image, and (b) the schematic representation of dual 5-nm diameter nanowire with 1-nm silicon bridge wrapped around by TaN gate.

This structure is constructed from a thin 70-nm SOI wafer using a well controlled self-limiting oxidation technique. The thin silicon bridge apparently is able to achieve an additional boost of drive current. Figure 6.2 presents the schematic and various cross-sectional plane views of the structure to give a better understanding of the structure.

Figure 6.2 Several views of the dual nanowire device: (a) 3-D view, (b) x-y top plane view, and (c) cross-sectional view on y-z plane.

6.2 CHARACTERISTICS OF DUAL NANOWIRE MOSFET

The I_d vs V_d characteristics of the 350-nm long nanowire MOSFET devices are given in Figure 6.3. At an operating voltage of 1.5 V, the p-dual nanowire device exhibits a drive current of 2.04 mA/ μm , while the n-dual nanowire device achieving 1.22 mA/ μm . The p- and n-dual nanowire devices exhibit comparable leakage currents of 2 nA/ μm and 4 nA/ μm respectively, both taken at zero gate voltage. All currents are normalized to the nanowire diameter. This gives a spread of $I_{\text{ON}}/I_{\text{OFF}}$ ratio of between $10^5 \sim 10^6$. The high drive current is attributed to the volume inversions of the two silicon nanowires and the stress in the nanowire channel, which is the deformation observed previously in Figure 5.11 (a).

Figure 6.3 I_d vs V_d plot of 350-nm dual nanowire MOSFET devices. Note that the currents have each been normalized to the diameter of the nanowire.

The thin 1-nm silicon bridge is likely to contribute only a small amount of current boost, and this is due to the high quantum confinement effects acting on the narrow silicon. This quantum confinement effect increases the threshold voltage of the silicon bridge, resulting in low drive current contribution for the device.

The higher on-current observed in p-dual nanowire device as compared to n-dual nanowire device is mainly attributed to the difference in V_T , and the change in the effective mass of the carriers. The last observation is also reported in [45]. Note that for the dual nanowire devices, this difference in the on-current is made more severe by the large difference in the two V_T . Measurement results showed that the p-dual nanowire device is able to achieve a V_T of -0.29 V, while the n-dual nanowire device has a high V_T of 0.56 V. By fixing at an operating voltage of 1.5 V, a lower overdrive ($V_g - V_T$) is attained for the n-dual nanowire device, and this will result in a lower drive current. Taking Fermi-level pinning into consideration, the workfunction of TaN is estimated to be around 4.6 eV after undergoing the 950 °C annealing step. From Figure 6.4, the threshold voltage for NMOSFET and PMOSFET should be 0.3 V (Point A in graph of Figure 6.4) and -0.55 V (Point B in graph of Figure 6.4) respectively.

Figure 6.4 Expected gate workfunction and threshold voltage plot for thin-body lowly doped MOSFETs [16].

The difference in the measured V_T (0.56 V and -0.29 V) and expected V_T (0.3 V and -0.55 V) for the NMOSFET and PMOSFET denoted may be explained as follows. The increased in V_T for NMOSFET is likely a result from the used of thick gate dielectric (20 Å SiO_2 and 30 Å HfO_2) and the quantum confinement effect. The deployment of p-type SOI wafers for both the p- and n-dual nanowire device may has led to a reduced in V_T for the p-dual nanowire device.

The change in the effective mass of the carriers contributes to the high performance of the p-dual nanowire device. It is reported that the effective mass of electron increases while effective mass of hole decreases at small dimensions (< 5nm) [45].

The stress induced in the nanowire channel also results in higher on-current for the dual nanowire devices. From the fabrication process of the dual nanowire devices, it is noticed that the nanowire channels are deformed after TaN metal is deposited, as discussed in previous chapter. This observation is not notice in polysilicon devices. Figure 6.5 shows the enhancement in mobility of the TaN gate device over the polysilicon device, with a higher and steeper transconductance (G_m) plot.

Figure 6.5 G_m plot of 500-nm nanowire devices, with TaN gate device having higher transconductance in comparison to polysilicon device.

The wrap-around gate electrode serves as a shield to block the drain field, providing good immunity to the short channel effects (SCE). The immunity is reflected in the 65 mV/dec SS and the 25 mV/V DIBL achieved by the PMOS. The NMOS also

shows low SS of 66 mV/dec and DIBL of 28 mV/dec. Both the I_d versus V_g characteristics of the n- and p-dual nanowire devices are presented in Figure 6.6.

Figure 6.6 I_d vs V_g plot of 350-nm dual nanowire MOSFET devices.

The mid-gap TaN gate elevates the V_T to solve the low V_T and high off-state leakage issues seen in polysilicon gate nanowire devices. The V_T for the PMOS is improved from 0 V to -0.29V, while the NMOS is increased from 0.2 V to 0.56 V. The elevation of the V_T shifts the PMOS I_d vs V_g curve to the left and NMOS curve to the right as indicate in Figures 6.7 (a) and (b). This shift allows the TaN gate device to realize lower leakage for as much as one order of magnitude as compare to the polysilicon gate device, while maintaining high drive current. Although the use of TaN metal gate further increases the V_T of the n-dual nanowire device, this issue can be moderated with a small dosage of V_T adjustment implant.

(a)

(b)

Figure 6.7 I_d vs V_g graph of polysilicon and TaN gate devices for both (a) NMOS and (b) PMOS. The implementation of TaN gate shift the plot to the right for NMOS and to the left for PMOS, therefore reducing the off-state leakage current, measure at $V_g = 0$.

The G_m vs V_g plot of Figure 6.3 illustrates the fast response of the transconductance to gate voltage. The transconductance saturates after peaking and this indicates that these devices are enjoying low field mobility even at high gate voltages. This is attributed to the cylindrical channel morphology and the undoped channel.

The dual nanowire devices are also immune to substrate bias, whereby the V_T remains constant with substrate bias swept from -6 V to 6 V for both the n- and p-DNWFET. This immunity is further verified with a reference planar SOI devices built on the same wafer. V_T of the reference device changes with substrate bias swept from positive to negative for PMOS and vice versa for NMOS. The substrate bias immunity is a result of the wrapped around gate shielding the channel from unwanted signals. This is illustrated in Figure 6.8.

Figure 6.8 Substrate bias (V_{BS}) sweep illustrating the immunity of substrate bias effect on both nanowire and reference devices fabricated on the same wafer.

Table 6.1 displays a summary of the dual nanowire devices performance and also a comparison of the dual nanowire electrical characteristics with the Samsung's twin-nanowire devices [12].

Structure	TSNWFET (Samsung)		DWNFET (this work)	
	P-type	N-type	P-type	N-type
Lg (nm)	15	15	350	350
Vdd (V)	1	1	1.5	1.5
I _{on} (mA/um)	1.94	1.44	2.04	1.22
I _{off} (nA/um)	2	1	2	4
I _{on} /I _{off}	10 ⁶	10 ⁶	10 ⁶	10 ⁵
Subthreshold Swing (mV/dec)	71	72	65	66
DIBL (mV/V)	43	50	25	28

Table 6.1: Comparison of twin-nanowire and dual nanowire devices.

CHAPTER 7: CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

7.1 CONCLUSION

The project explores novel advanced SOI MOSFETs for continuous scaling into the deep submicron regime. Various three dimensional (3D) multi-gate SOI MOSFET structures are examined. In consideration of the electrical characteristics and process complexity, the n-gate and Gate-All-Around (GAA) structure are proposed in this project to demonstrate their ability to provide enhanced electrical properties as well as to provide greater process compatibility with comparison to existing conventional triple-gate and the quadruple-gate designs. In brief, the n-gate NMOSFET is introduced to eliminate the early turn on effect due to the corners that are inherent to the transistors, which appear in the triple-gate structure. On the other hand, the GAA structure is proposed to offer an optimum electrical performance for deep-submicron SOI transistors that has compatible process steps with that of the conventional CMOS process. The fabrication process of the proposed multiple-gates SOI device structures has been clearly described in the thesis in Chapter 3. A novel surface rounding technique for the n-gate and the replacement gate mask process for the GAA are also demonstrated.

The experimental results obtained from the fabricated n-gate and the GAA NMOS devices have been presented in Chapter 4. The proposed n-gate device is able to eliminate the “early turn-on” effect. The GAA device exhibits both high drive current and excellent short channel performance. However, the high leakage current denoted at zero gate voltage due to the low threshold voltage suggests that metal gate should be implemented

instead of the polysilicon, to achieve an optimum threshold voltage for the GAA device. Device simulations on both n-gate and GAA are also performed to project the scalability of these devices. Base on the study carried out to investigate the effect of gate electrode extension beneath the silicon channel, it is evident that the increase in gate coverage is able to improve the current drive and more effectively suppress the short channel effects.

To take the project to another level, the focus is diverted to the nanowire MOSFET structures, which is a growing research interests among the key players in the semiconductor industry. A brief introduction on the evolution and the advantages of nanowire MOSFET structures is given in Chapter 2. By examining various published nanowire MOSFET structures, the dual nanowire MOSFET structure is proposed. The structure is equipped with two nanowire cores (top and bottom) for high current drive and minimum silicon area. The use of thin SOI substrate allows formation of thin silicon bridge joining the two nanowires with the deployment of metal gate and non-overlapping gate configuration. These changes are targeted to achieve higher threshold voltages and lower overlapping capacitances.

Both the n- and p-type dual nanowire MOSFET devices are successfully fabricated using the stress-limiting oxidation technique and conventional CMOS processes. It is found that stress-limiting oxidation is able to produce different nanowire structures (single nanowire, dual nanowire with silicon bridge and dual nanowire without silicon bridge) as depicted in Figure 5.6 with different thicknesses of SOI substrate and controlled oxidation time. Both n- and p-type devices display high I_{ON}/I_{OFF} ratios and

excellent subthreshold performances. The use of TaN metal gate increases the threshold voltages of the devices and results in a reduction in leakage current that is observed from polysilicon gate nanowire devices. It is also noted that the p-type nanowire devices outperform its n-type counterpart. The compressive stress caused by the TaN metal gate as observed in Figure 5.11 (a) and the change in effective mass of the carriers maybe the explanation for the large enhancement in the p-type nanowire devices.

In summary, three new types of advance SOI structures have been demonstrated. They offer excellent electrical properties and are conventional CMOS process compatible. These devices structures could make contributions in the sustaining of the pace-quicken trend in the submicron silicon technology and beyond.

7.2 SUGGESTIONS FOR FUTURE WORK

7.2.1 GATE-ALL-AROUND (GAA)

The GAA NMOS devices suffer from high leakage current due to low threshold voltage. An appropriate threshold voltage can be achieved with the implementation of metal. Similar to the case of dual nanowire MOSFET structure presented, mid-gap metal gates such as TaN, TiN, FUSI gate, can also be used to derive a desirable threshold voltage. Furthermore, metal gate also gives the advantages of lower gate sheet resistance, elimination of boron penetration and poly depletion in deep submicron MOSFET. The high-k gate oxide can be used to replace the conventional oxide, so as to provide low leakage current while maintaining good gate controllability over the silicon channel.

7.2.2 DUAL NANOWIRE MOSFET

High source/drain resistance is experienced in the dual nanowire devices due to thin source/drain pad. After various processes, on average 300 Å silicon is left, resulting in higher source/drain resistance. The formation in thin silicided source/drain region is capable of resolving this issue. However with the thin silicon left, silicidation process becomes difficult. The technique of raised source/drain to support silicide formation shall be considered. Prior using the raised source/drain and silicidation process, a spacer development process is required. A well defined spacer must be formed to segregate the raised source/drain from the metal gate before silicide formation.

High and asymmetry threshold voltages are observed in the nanowire devices. It is likely due to quantum confinement effect that is acting on the nanowire silicon core and the thick gate dielectric used. More in-depth workfunction studies of the TaN/HfO₂/SiO₂ gate stack should be conducted. This will help in threshold voltage adjustment especially for n-type nanowire device. Alternatively, SiGe or Ge nanowire can be fabricated. SiGe and Ge having lower band-gap provides not only lower threshold voltages, but also high mobility. TaN/HfO₂ gate stack without SiO₂ can be achieved with lower fermi-level pinning effect. The use of Mo metal gate with nitrogen implantation allows Mo workfunction adjustment (4.5 eV to 5.0 eV) using different nitrogen concentration. It is estimated that 4.52 eV and 4.95 eV are required to attain threshold voltage of ± 0.2 V for n- and p-type advance MOSFET devices respectively.

Studies on the strain/stress induced by the TaN gate can also be conducted. This can be accomplished by varying the diameter of the nanowire channels and thickness of TaN. The observations of the device performances from these experiments will allow us to deduce the type and amount of strain/stress induced on different diameter nanowires electrically. The experiments can be extended to other metal gate materials, such as TiN.

Lastly, the justification for investing in a new CMOS device technology such as the proposed advanced SOI must be found not only on its present attributes but also on its ability to favourably scale device features through future generations of lithograph and voltage.

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