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High Speed Low Voltage Low Power Embedded Analog-to-Digital Converters for Wideband Transceivers

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Abstract

The analog-to-digital converter (ADC) is one of the key building blocks in digital communication systems. In modern receiver designs, ADCs are usually fabricated on the same die with the digital baseband signal processing block for the dual-chip solution. This implementation takes into considerations of cost, flexibility and packaging. The combination of analog circuits and digital circuits in one die poses numerous challenges in ADC design due to the coupling of digital noise to analog circuits.

Currently, the fast growing demands for high data rate applications in multimedia services are calling for faster baseband circuits. With the advancement of the CMOS process, both the transistor channel length and supply voltage are shrinking, making faster digital circuits possible. However, unlike their digital counterparts, the analog circuits do not always benefit from the technology evolution in terms of accuracy, speed and power consumption. Although process advancement improves the transistor's unity gain frequency f_t , device scaling decreases the transistor intrinsic gain, making the design of high accuracy analog circuits difficult in the deep sub-micron process. Obviously the decrease of supply voltage lowers the signal-to-noise ratio since the signal amplitude has to be decreased accordingly while the noise level remains the same. The dropping in signal-to-noise ratio is another major challenge in ADC design as the technology heading toward the nanometer.

Two types of receiver architectures showing the great potential in modern wideband communication systems are the direct conversion receiver and low intermediate frequency (low-IF) receivers. Usually the direct conversion and the low-IF receivers are used at portable terminal where high speed and low power operation are the major concerns. This project focuses on dealing with speed, power, and noise issues in high speed CMOS ADC design for direct conversion and low-IF receivers. The resolution and sampling rate requirements of the ADC are considered for direct conversion receivers following the IEEE 802.11 standards. The system level studies show that the pipelined ADC architecture, based on switched capacitor (SC) techniques, is the best candidate to meet the above mentioned specifications.

The building block performance requirements in pipelined ADCs are derived based on the ADC resolution and sampling rate. At the circuit level, new techniques are proposed to relax the requirements of the operational amplifier (op amp), which is the most crucial and difficult-to-design component in pipelined ADCs. A mixed-mode sample-and-hold (S/H) circuit is designed and verified in this project. The proposed S/H circuit reduces the signal swing in pipelined ADCs, relaxes the op amp gain, bandwidth, output swing and slew-rate requirements. The mixed-mode S/H technique also reduces the capacitor matching requirement in pipelined ADCs, leading to a low power consumption. A pipelined ADC is designed based on the mixed-mode S/H technique. Implemented in a $0.18\text{-}\mu\text{m}$ CMOS process, the 8-bit pipelined ADC achieves a sampling rate up to 200-MSample/s with 54-dB spurious free dynamic range (SFDR) and 45-dB signal-to-noise and distortion ratio (SNDR). The measured integral nonlinearity (INL) and differential nonlinearity (DNL) are

0.34 LSB and 0.3 LSB, respectively. The power consumption of the prototype ADC is 22-mW at the supply voltage of 1.8-V. The techniques proposed in this project promise feasible solutions for future high-speed pipelined ADCs in even lower supply voltage environments.

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Chapter 1

Introduction

1.1 Research Background and Motivation

The fast growing demands on high data rate applications such as multimedia service in portable devices have been driving the bandwidth of wireless communication standards upward. Table 1.1 summarizes the evolution roadmap of the IEEE 802.11 wideband wireless communication standards. The data throughput of the coming 802.11n standard is expected to reach 540 Mbit/s, which will be up to 50 times faster than the 802.11b and well over 10 times faster than the 802.11a and 802.11g standards. The physical layer may require an even higher raw data rate. Besides using more advanced modulation techniques and multi-antenna spatial multiplexing such as multiple-input multiple-output (MIMO) to increase data throughput, the channel bandwidth is expected to extend to 40-MHz. All of the digital and analog circuits in such a transceiver must have a higher speed and a wider bandwidth to cater for the data rate bursting. In addition, there is another trend to include

different standards into the same wireless device to maximize device functionality and make the most use of RF and analog building blocks in a transceiver as well as to reduce cost and complexity. The multi-standard transceiver requires all the building blocks to have the ability to process all the signals from different standards of various modulation schemes [1]. This implementation imposes challenges on circuit design, especially on analog circuit design since analog circuits get much less benefit from process evolution compared to digital circuits.

Table 1.1: IEEE 802.11 wideband wireless communication standards summary.

Protocol	Release Date	Operating Frequency	Data Rate (Typ)	Data Rate (Max)	Range
802.11b	1999	2.4-2.5 GHz	6.5 Mbit/s	11 Mbit/s	50 meters
802.11a	1999	5.15-5.35/5.47-5.725/5.725-5.875 GHz	25 Mbit/s	54 Mbit/s	30 meters
802.11g	2003	2.4-2.5 GHz	25 Mbit/s	54 Mbit/s	30 meters
802.11n	2007 (projected)	2.4 GHz or 5 GHz	200 Mbit/s	540 Mbit/s	50 meters

A direct conversion receiver architecture, which is commonly used in wideband communication systems of such standards as the IEEE 802.11 and Wideband Code Division Multiple Access (WCDMA) is illustrated in Figure 1.1. The RF signal from the antenna is first band-selected by the bandpass filter. The filtered signal is then amplified by the low noise amplifier (LNA). After that, the mixer down converts the RF signal directly to the baseband signal. This implementation eliminates the need of an image reject filter which requires high quality factor (Q) components to implement. The baseband signal is amplified by the variable gain amplifier (VGA) and then digitalized by the analog-to-digital

converters (ADCs) [2]. The lowpass filters in front of the ADCs prevent the out of band signal from aliasing back to the baseband.

Figure 1.1: The direct conversion receiver.

Since signals are increasingly processed in digital domain, the ADCs become essential building blocks in digital receivers. To handle higher data rates, the sampling rate of ADCs has to be increased accordingly to cater for the wider signal bandwidth demanded by the Nyquist sampling theorem. Meanwhile, the accuracy of ADCs has to be maintained, if not improved, to guarantee an adequate signal-to-noise ratio (SNR) required by the communication standards. At the same time, the power consumption of ADCs must remain as low as possible specially in battery powered portable devices. There are four major challenges in ADC design for wideband communication systems: the noise performance, accuracy, speed and power consumption.

The first challenge is the noise performance. In analog signal processing circuits, thermal noise is the fundamental noise and sets a limit for the smallest distinguishable signal.

In switched-capacitor (SC) circuits, the integrated thermal noise power is given by

$$\overline{V_n^2} = \frac{kT}{C} \quad (1.1)$$

where k is Boltzmann's constant, T is the absolute temperature, and C is the sampling capacitance. Therefore, for a signal with *rms* value of $V_{sig,rms}$, the SNR is determined by

$$SNR = \frac{V_{sig,rms}^2}{kT/C} \quad (1.2)$$

One straightforward method for minimizing the impact of noise is to increase the signal level. Unfortunately, as the device size is scaled down in deep sub-micron technologies, the supply voltage also decreases. Hence, the signal level has to be reduced accordingly, which would lead to a decreasing of SNR unless the noise level is scaled down simultaneously. The only way to reduce the thermal noise is to increase the sampling capacitance. As will be discussed later, increasing the sampling capacitance increases the power consumption and lowers the SC circuit speed.

In a modern receiver design, ADCs are fabricated on the same die with digital baseband signal processing blocks in both single-chip and dual-chip solutions for the considerations of cost, flexibility and packaging. The system-on-chip (SoC) solution has, however, been facing difficulties with the implementation of on-chip ADCs because of the coupling of digital noise into analog circuits. This is another major source of errors and becomes worse as the speed of digital circuits and the number of gates increase.

The continuous advancement of the semiconductor technology and scaling of device size has improved the performance of digital circuits in terms of higher speed and lower power dissipation. For analog circuits, however, numerous design challenges emerge in the

deep sub-micron technology. One of the challenges is the design of highly accurated analog circuits as device scaling lowers the transistor intrinsic DC gain $g_m \cdot r_o$. The operational amplifier (op amp) is the basic and crucial block in most ADC architectures. The design of high gain op amps becomes increasingly difficult in deep sub-micron CMOS process and usually the device size has to be increased for a higher gain. The op amp gain boosting, however, comes with the price of a slower speed due to the parasitic capacitance load. Therefore, usually the speed and accuracy have to be compromised against each other in ADC design.

The sampling rate of the ADC in most applications is at least twice of the maximum analog signal bandwidth according to the Nyquist theory. In practice, the employed sampling rate is usually much higher than the Nyquist requirement in order to ease the design of the anti-aliasing filter. Although the device's unity gain frequency f_t has been increased with the advancement of technology, the speed of ADCs lags to that pace due to the thermal noise. With the supply voltage decreasing, in order to keep the SNR constant, the sampling capacitance has to be larger to reduce thermal noise. However, the speed of SC circuits is determined by op amp bandwidth and slew rate. For a single stage op amp the unity gain bandwidth is given by [77]

$$GBW = \frac{g_m}{C} \quad (1.3)$$

where g_m is the transconductance of the op amp input transistor and C is the load capacitance, which can be approximated to the sampling capacitance. Meanwhile, the slew rate of a single stage op amp can be expressed by

$$SR = \frac{I_{BIAS}}{C} \quad (1.4)$$

where I_{BIAS} is the op amp quiescent current and C is the capacitance load. It can be seen from equations (1.1) to (1.4), for a given op amp current consumption, the speed of SC circuits decreases with the supply voltage if the constant SNR has to be maintained.

The fourth challenge of ADC design in wireless communications is the power consumption. Supplied by a battery, a portable device requires low power consumption in every building block. However, the power consumption of analog circuits in deep sub-micron technology is often increased in order to meet the speed and accuracy requirements.

Based on the above discussion, the design of ADC entails many trade-offs between speed, accuracy, and power dissipation, presenting difficult challenges in both circuit design and implementation. This project will focus on the design of a deep sub-micron high speed ADC and develop techniques and circuit structures suitable for future low voltage technologies.

1.2 Objectives

In this project, the analog-to-digital converters will be designed and optimized for wireless applications according to the IEEE 802.11 broadband standards using a 0.18- μm CMOS process. Depending on the standards and considering the design margin for imperfections, the 8-bit resolution would be adequate while the sampling rate is preferred to be more than 160-MSample/s to meet the upcoming 802.11 standard which requires a much higher bandwidth. The challenges would be to obtain 8-bit accuracy at the speed of 160-MSample/s for a low supply voltage in a noisy environment. The specification target for the ADC are

listed in Table 1.2.

Table 1.2: The ADC design target

Parameter	Design Target
Resolution	8-Bit
Sampling Rate	160-MSample/s
Power Supply	1.8-V
Power Consumption	30-mW

1.3 Research Contribution

This research is concentrated on high-speed ADCs, in general, and specifically for the IEEE 802.11 wideband direct conversion and low intermediate frequency (low-IF) receivers. Requirements and optimizations of the pipelined ADCs, both at system and circuit levels, have been addressed to meet the specifications of the targeted applications. The requirements for the resolution and sampling rate of an ADC in a direct conversion receiver are studied based on the system specifications of the IEEE 802.11 standards. Following that, the requirements for the building blocks in pipelined ADCs are derived based on the ADC specifications.

In a switched-capacitor (SC) pipelined ADC, the op amp is the most design challenging block because it determines the overall ADC performance therefore has stringent performance requirements. This project proposes a mixed-mode sampling technique that relaxes the op amp requirements in the sample-and-hold circuit and in the pipelined stages.

The mixed-mode sampling technique also reduces the capacitor matching requirement in pipelined ADCs. The reduction of op amp and capacitor matching requirements leads to a lower power consumption in pipelined ADCs. The technique provides feasible solutions for the high speed pipelined ADCs design in even lower supply voltage environments.

An 8-bit 200MSample/s pipelined ADC is designed and optimized for the IEEE 802.11 standards based on the techniques proposed in this research. The new ideas and circuits in this project have been reported in related publications.

1.4 Organization of the Dissertation

This dissertation is organized into eight chapters, of which this introduction is the first. Chapter 2 reviews the basic ADC characteristics and ADC performance requirements in a wideband receiver. In Chapter 3, several high speed ADC architectures are reviewed and compared. This chapter also summarizes the latest published high speed ADCs with 8 to 10 bits resolution.

Chapter 4 highlights the design challenges facing high speed pipelined ADC design. Noise, speed, and accuracy requirements of building blocks in pipelined ADCs are derived. This chapter serves as a guideline for the design.

A mixed-mode sample-and-hold circuit is proposed in Chapter 5. The mixed-mode sampling technique reduces the requirements of the op amp in gain, bandwidth, slew rate and output swing. This technique enables the use of the single-stage cascode op amp in the low voltage environment while maintain the dynamic performance.

Based on the mixed-mode sampling technique, Chapter 6 and Chapter 7 describe the design and implementation of an 8-bit 200-MSample/s pipelined ADC. Implemented in a 0.18- μm CMOS process, the prototype chip achieves dynamic performance of 54-dB SFDR and 45-dB SNDR. The measured INL and DNL are 0.34 LSB and 0.3 LSB, respectively. The pipelined ADC has a power consumption of 22-mW in 1.8-V supply voltage.

Chapter 8 contains concluding remarks and suggestions for future work.

Chapter 2

ADC in Wideband Wireless

Communication Receivers

2.1 ADC Characteristics

An analog-to-digital converter is a device that translates continuous signals in analog format into discrete digital codes. Its characteristics can be measured by linearity and dynamic performances. Which parameter of ADC is more outstanding than others depends on the application in which the ADC is going to be used. For instance, in image processing applications, the DNL is important for sharp-edge detection, while in wideband digital receivers, the SFDR is critical for detection of low-level signals in a strong interference environment [3]. In this chapter we summarize the ADC characteristics with emphasis on wideband digital receiver applications.

2.1.1 Resolution

The resolution of an ADC is defined as the number of digital codes that represent the analog input signals. Resolution is usually presented in binary format, i.e., an N-bit resolution implies that the ADC can resolve 2^N distinct analog levels.

2.1.2 Sampling Rate

The sampling rate indicates the rate at which the input signal is sampled in a second. The ADC sampling rate is determined by the signal bandwidth and system requirements.

2.1.3 Offset and Gain Errors

The ADC offset error is defined as the difference between the ideal and actual digital outputs corresponding to the zero analog input.

The ADC gain errors include linear and nonlinear gain errors as illustrated in Figure

2.1. The linear gain error does not introduce distortion as long as the output signal does not clip. The nonlinear gain error introduces distortion and has to be minimized.

The offset and linear gain errors can be eliminated in back-end digital signal processing circuits as long as the offset and gain drifts over temperature variation are small.

Figure 2.1: Linear and nonlinear gain errors.

2.1.4 Quantization Noise

Since ADCs use finite discrete digital codes to represent infinite continuous analog inputs, there exists an inherent error called "quantization error" even in ideal converters as illustrated by the transfer curve of a 3-bit ADC in Figure 2.2 where FS is the full-scale range of the input signal from $-FS/2$ to $+FS/2$. The quantization error as a function of the input signal in a 3-bit ADC is shown in Figure 2.3. The amplitude of this error is $LSB/2$, where LSB is the least significant bit. If the input signals don't exceed the full-scale range and are uncorrelated from sample to sample, the quantization error is approximately white noise and spread uniformly over the Nyquist bandwidth from DC to $f_s/2$, where f_s denotes the sampling frequency [4]. In this case we assume that the quantization noise has a uniform

Figure 2.2: Transfer curve of a 3-bit ADC.

Figure 2.3: Quantization error in a 3-bit ADC.

probability lying anywhere in the range of $\pm LSB/2$, i.e.,

$$p(e, t) = \frac{1}{LSB}, \quad -LSB/2 < e < LSB/2 \quad (2.1)$$

Therefore, the mean square value of the quantization noise is given by [3]

$$P_n(t) = e_{rms}^2 = \int_{-\omega}^{\omega} e^2 \cdot p(e, t) \cdot de = \frac{1}{LSB} \int_{-LSB/2}^{LSB/2} e^2 \cdot de = \frac{LSB^2}{12} \quad (2.2)$$

The quantization noise is a fundamental limitation of an ADC that represents a noise floor. Although the *rms* value of the quantization noise is accurately approximated by

$e_{rms} = LSB/\sqrt{12}$, its frequency domain content may be highly correlated to the AC input signal and appears concentrated at the various harmonics of the input signal. In order to accurately measure the harmonic distortions of an ADC, the input signal frequency must be carefully chosen or a window weighting function must be used to reduce spectral leakage effects [5]. In practical ADC applications, the quantization error generally appears as random noise because of the random nature of the input signals [3].

2.1.5 Differential and Integral Nonlinearity

Differential nonlinearity (DNL) measures how far each of the actual step size deviates from the value of the one LSB ideal step size. Integral nonlinearity (INL) is the measure of the total deviation of the actual transfer characteristic from the ideal straight line transfer curve. The DNL and INL errors are illustrated in Figure 2.4. In practice, DNL and INL are described by the maximum errors measured.

Most ADCs are designed so that the DNL is spread across the entire ADC input range because the DNL increases the noise floor of the ADC in the frequency domain. The INL of the ADC transfer function produces distortion products. The distortion amplitude varies as a function of the input signal amplitude. In order to achieve a better dynamic range performance in wireless communication systems, the INL needs to be minimized. For input signals that are within a few dB of full-scale, the overall INL of the transfer function determines the distortion products. For lower level input signals, however, the harmonic contents are dominated by the DNL and do not generally decrease proportionally with decreases in input signal amplitude [3].

Figure 2.4: Actual transfer function with DNL and INL errors.

2.1.6 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio of signal power to noise power at the output of the ADC, excluding harmonics and DC components. In an ideal ADC, the only noise source is the quantization error, whose power equals to $LSB^2/12$. If the input is a sinusoidal signal, the SNR of an ideal ADC can be expressed as [6]

$$SNR = \frac{Power_{Signal}}{Power_{Noise}} = \frac{(FS/2)^2/2}{LSB^2/12} = 1.5 \times 2^{2N} \quad (2.3)$$

$$SNR_{dB} = 10 \log\left(\frac{Power_{Signal}}{Power_{Noise}}\right) = 6.02N + 1.76 \text{ dB} \quad (2.4)$$

It is important to emphasize that the quantization noise is uncorrelated and spread over the entire Nyquist bandwidth, i.e., DC to $f_s/2$. In many applications, however, the actual signal of interest occupies a bandwidth BW which is smaller than half of the sampling frequency. If digital filtering is used to remove noise components outside the bandwidth

BW , then the resulting SNR is increased due to the process gain. Taking into account the process gain, the SNR is given by

$$SNR_{dB} = 6.02N + 1.76 + 10\log_{10}\frac{f_s}{2 \times BW} \quad dB \quad (2.5)$$

where $10\log_{10}f_s/(2 \times BW)$ is the process gain.

2.1.7 Spurious Free Dynamic Range

The spurious free dynamic range (SFDR) is the ratio of the signal power to the power of the largest spurious component [6].

$$SFDR_{dB} = 10\log\left(\frac{\text{Signal Power}}{\text{Largest Spurious Power}}\right) \quad dB \quad (2.6)$$

The SFDR is the most critical measurement in communication applications. Although the largest spur is usually buried in the noise floor in a single-tone test, the spurs due to intermodulation stand out from the noise floor and become the dominant noise in a multi-tone test. Unlike the SNR, the SFDR couldn't be improved by a digital filter which removes the out-of-band quantization noise.

2.1.8 Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the total power of harmonic components to the power of signal [6], i.e.,

$$THD_{dB} = 10\log\left(\frac{\text{Total Harmonic Distortion Power}}{\text{Signal Power}}\right) \quad dB \quad (2.7)$$

2.1.9 Signal-to-Noise-and Distortion Ratio

The signal-to-noise-and distortion ratio (SNDR) is the ratio of the signal power to the total noise and distortion power within a certain frequency band, i.e.

$$SNDR_{dB} = 10\log\left(\frac{\text{Signal Power}}{\text{Noise and Distortion Power}}\right) \text{ dB} \quad (2.8)$$

Since it includes all the components of noise and distortions, SNDR is a good measurement of the overall ADC dynamic performance as a function of input frequency and amplitude. At low input amplitude the ADC performance is usually limited by the quantization error while the distortion will limit the performance at higher signal levels.

2.1.10 Effective Number of Bits

The effective number of bits (ENOB) is the ADC effective resolution based on the SNDR with a full-scale sinusoidal input signal. The ENOB is given by [6]

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \text{ bit} \quad (2.9)$$

For example, if an 8-bit ADC has a measured SNDR of 48dB, the ENOB of this ADC is $ENOB = (48 - 1.76)/6.02 = 7.68$ bits.

2.1.11 Input Bandwidth

ADC resolution is not only a function of the signal amplitude but also of the input signal frequency. At high input frequencies, the SNDR of an ADC can be reduced significantly. The input bandwidth of the ADC is defined as the input frequency at which the SNDR is 3 dB (corresponds to a decrease in the ENOB of 0.5 bits) below the maximum value.

2.1.12 ADC Dynamic Performance Illustration

Most ADC dynamic performances can be directly observed from a Fast Fourier Transform (FFT) plot. Figure 2.5 is the FFT spectrum of an ADC that illustrates the SNR, SFDR, and SNDR. The noise floor is well below the SNR due to the FFT process gain. When testing ADCs using an FFT, it is important to ensure that the FFT size is large enough that the distortion products can be distinguished from the FFT noise floor itself [3].

Figure 2.5: FFT spectrum of ADC.

2.2 ADC in Wideband Wireless Communication Receivers

When an ADC is used in a digital communication receiver, its specifications are determined by the communication protocol and receiver architecture. The continuously growing

complexity of the modulation schemes and the desire for more flexible receivers push the boundary of the baseband and digital signal processing blocks closer to the antenna, thus bringing out the idea of software defined radio. The optimistic goal is to directly sample the RF signal at the output of LNA, and move all the filtering, mixing, and channel selection functions into fast and robust digital processing circuits. However, RF sampling requires an ADC with a sampling rate in the order of up to several giga hertz, and a dynamic range capable of handling signals with micro-volt amplitudes in the presence of strong interferers. Because of the technical limitations, direct RF sampling is not feasible at present. To move as many functions as possible into the digital domain and increase receiver flexibility, two realistic receiver architectures are widely adopted: the direct conversion receiver and the low-IF receiver, which are illustrated in Figure 2.6 and Figure 2.7, respectively. The direct conversion receiver consists of an LNA, down-conversion mixers, channel selection filters, and VGAs preceding the ADCs. Since the signal is converted to the baseband in a direct conversion receiver, no image rejection filter is needed but quadrature down conversion is required. Therefore, two ADCs are necessary in a direct conversion receiver. The low-IF receiver has an LNA, image reject mixer, IF filter, and VGA before the signal is sampled by the ADC. In low-IF receiver, the signal is not converted to the baseband but at a low frequency. This implementation eliminates the DC offset error and flicker noise presented in direct conversion receivers. However, low-IF receivers require a image rejection architecture. The image rejection architecture uses the same quadrature down conversion as in the direct conversion receiver but with the BPFs instead of LPFs after the down conversion. The subtraction of the image can be done by either analog circuits or by the DSP.

Figure 2.6: Block diagram of the direct conversion receiver.

Figure 2.7: Block diagram of the low-IF receiver.

The performance requirements of ADCs in these two receiver architectures depend on the location of channel filtering function. In the direct conversion receiver and low-IF receiver, if analog channel selection filtering and variable gain amplifiers are preceding the ADC, the dynamic range requirement and the ADC resolution are relaxed. While if there is no channel selection filtering before the ADC, the whole signal band is digitized directly, a very high linearity and sampling rate are required in addition to high resolution.

As most of the circuits presented in this research are intended to be used in portable

devices for the IEEE 802.11 standards, the specifications below are proposed for the direct conversion receiver with sufficient gain and channel filtering before ADCs. Extensions to low-IF receiver with sufficient gain and channel filtering before ADCs are similar except the sampling rate of ADCs needs increase.

2.2.1 ADC Sampling Rate

In order to illustrate the ADC sampling rate requirement in IEEE 802.11 direct conversion receiver, we use the IEEE 802.11a standard as an example. The IEEE 802.11a wireless LAN standard operates over three frequency bands from 5.15 GHz to 5.85 GHz as shown in Figure 2.8. The physical layer of the 802.11a is based on orthogonal frequency-division multiplexing (OFDM) [9]. The basic concept of OFDM is to split a high-rate data stream into a number of lower rate streams that are transmitted simultaneously over several subcarriers. With lower data rates in the parallel subcarriers there is an increased symbol duration, which decreases the relative amount of dispersion in time (delay spread) caused by multipath propagation. Intersymbol interference (ISI) is almost completely eliminated because an adequate guard interval can be inserted between successive OFDM symbols. OFDM uses multiple overlapped carriers to mitigate the effects of multipath. As indicated in Figure 2.8, the IEEE 802.11a standard supports multiple 20MHz channels. Each channel is an OFDM modulated signal consisting of 52 carriers, among which 48 carry data and 4 carry pilot signals used for tracking. Each carrier has a 312.5-kHz bandwidth, giving raw data rates from 125-kB/s to 1.125-MB/s per carrier depending on the modulation type employed - binary phase shift keying (BPSK), quaternary PSK (QPSK), 16-quadrature

amplitude modulation (QAM), or 64-QAM - and the amount of error-correcting code overhead (1/2 or 3/4 rate code). The composite signal therefore has a data rate selectable from 6 MB/s up to 54 MB/s in a 20-MHz channel. When converted from the RF to the baseband signal, since the local oscillator frequency is the same as the RF carrier frequency, the upper sideband and the lower sideband are overlapped; therefore the signal bandwidth is reduced to 10-MHz.

Figure 2.8: Channel allocation of the 802.11a standard.

According to the Nyquist theory, the sampling rate must be at least twice of the signal bandwidth in order to avoid the out-of-band signals alias into the desired band. In practice, a much higher sampling rate has to be chosen to relax the requirements of the anti-alias filter. Four to eight times of the signal bandwidth was usually chosen as the sampling rate. In the IEEE 802.11a standard with a 10-MHz baseband bandwidth, a sampling rate up to 80-MSample/s is typically required [37]. In the coming IEEE 802.11n standard, the channel bandwidth is expected to be 40-MHz, which means a 20-MHz bandwidth at baseband. This demands a typical ADC sampling rate of 160-MSample/s.

2.2.2 ADC Dynamic Range

The SFDR requirement of the ADC in a communication system is determined by its dynamic range specifications, which can, in turn, be derived from the sensitivity, maximal input power, blocker level, and carrier-to-interferer ratio for a given protocol and receiver architecture. The simplified IEEE 802.11a direct conversion receiver analysis for ADC spurious requirements is shown in Figure 2.9.

Figure 2.9: ADC SFDR requirement.

In the IEEE 802.11a direct conversion receivers, with sufficient channel selection filtering, the maximum blocker level applied to ADC is about -30 dBm. The minimum detectable signal (sensitivity) is specified as -65 dBm when the data rate is 54-MBps. Approximately 6 dB carrier-to-interferer ratio (C/I) is required to prevent the interferer from

overtaking the desired signal. In practice, a design margin of 4 to 10 dB is commonly applied in the design of ADCs for wireless receivers to accommodate sudden variations in the received signal strength and to handle DC offset and VGA gain errors [3]. As a result, the ADC dynamic performance requirement can be expressed as

$$\begin{aligned}
 SFDR_{ADC} &= \text{Blocker Level} - \text{Sensitivity} + C/I + \text{Headroom} \\
 &= -30\text{dBm} - (-65\text{dBm}) + 6\text{dB} + 10\text{dB} = 51\text{dB}
 \end{aligned} \quad (2.10)$$

The simplified IEEE 802.11a direct conversion requirement for sensitivity relating to the ADC SNR is shown in Figure 2.10.

Figure 2.10: ADC SNR requirement.

We can assume that the overall noise figure (NF) and gain in front of the ADC are 6 dB and 54 dB respectively, as in a good design [47]. The thermal noise at the antenna input is

-174 dBm/Hz. The noise required to the ADC input is therefore

$$\begin{aligned} ADC_{InputNoise} &= -174dBm + Gain + NF \\ &= -174dBm/Hz + 54dB + 6dB = -114dBm/Hz \end{aligned} \quad (2.11)$$

In IEEE 802.11a standard, when the data rate is 54-MBps, the channel bandwidth is 20-MHz. When integrated over the channel bandwidth, this noise at ADC input becomes

$$\begin{aligned} ADC_{Channel Input Noise} &= -174dBm + Gain + NF + 10\log(BW) \\ &= -114dBm/Hz + 10\log(20 \times 10^6) \\ &= -114dBm + 73dB = -41dBm \end{aligned} \quad (2.12)$$

Since the 20-MHz channel is sampled at 80-MS/s, there is a process gain of

$$\begin{aligned} Process Gain &= 10\log\left(\frac{f_s}{2 \times BW}\right) \\ &= 10\log\left(\frac{80 \times 10^6}{2 \times 20 \times 10^6}\right) \\ &= 3dB \end{aligned} \quad (2.13)$$

Therefore, the ADC noise across the Nyquist band is

$$\begin{aligned} ADC_{Noise Nyquist} &= ADC_{Channel Input Noise} + Process Gain \\ &= -41dBm + 3dB \\ &= -38dBm \end{aligned} \quad (2.14)$$

Assume the full-scale input of the ADC is 2 dBm ($800-mV_{pp}$). the minimum SNR requirement for ADC is

$$SNR_{ADC} = FS - (-38dBm) = 40dBm \quad (2.15)$$

In a real design, some margin has to take into consideration. Equations (2.11) to (2.15) show that the SNR requirement of an ADC in direct conversion receiver can be expressed as:

$$SNR_{ADC} = FS - (-174dBm + 10\log(BW)) - Gain - Process\ Gain \quad (2.16)$$

For the IEEE 802.11 a/g wireless LAN protocols, ADCs with conversion rates of the order of 80-MSample/s are required [9] [10]. The modulation schemes used in the 802.11 standards also demands an 8 to 10 bits resolution for these converters in order to avoid an increased bit-error rate due to ADC's quantization noise [37] [38] [39] [40] [41] [42] [43] [44] [45]. For the next generation IEEE 802.11n wideband communication protocol with 40-MHz channel, the desired specifications are estimated to include a resolution of 8 to 10 bits and a sampling rate of over 160-MSample/s.

2.3 Conclusion

The definition of ADC performance characteristic terminology is described in this chapter. This terminology is key to understanding of the specifications of ADCs and the measurement of ADCs performance. ADC performance can be measured by static performance and dynamic performance. The static performance includes DNL and INL. The dynamic performance includes SNR, SFDR, SNDR, and THD. Which characteristic is more outstanding than others is determined by the application in which the ADC is used.

When an ADC is used in a digital communication system, its performance requirements are determined by the communication standard and receiver architecture. This chapter

derives the ADC performance requirements in a direct conversion receiver for the IEEE 802.11a standard. With the channel bandwidth increases, an 8-bit ADC with the sampling rate larger than 160-MS/s is required for the coming IEEE 802.11n standard.

Chapter 3

High-Speed ADC Architectures

In this chapter, state-of-the-art high speed ADC architectures are described and compared. Each architecture has its advantages and disadvantages, and each has a set of applications to which it is the best choice. Among these architectures, the pipelined ADC has the most successful potential for high speed low power applications such as wideband wireless communication.

3.1 Flash ADC

The flash ADC architecture is the most straightforward method to perform an analog-to-digital conversion function. A flash ADC consists of an array of comparators and encoding circuits as shown in Figure 3.1. In a flash ADC, the analog input signal applies at the inputs of all the comparators simultaneously. This input signal is compared to a set of reference voltages generated from a resistor string. The comparators generate thermometer code according to the input and references. The thermometer code is subsequently converted

Figure 3.1: Flash ADC.

to binary code by the encoding logic. The primary advantage of the flash ADC is its high conversion speed. Because of the parallel architecture of flash ADC, the conversion of each sample takes only one single clock period which is usually only limited by comparator speed.

The most prominent drawback of this architecture is that the number of comparators and resistors grows exponentially with the required resolution. An N -bit flash ADC needs $2^N - 1$ comparators. The consequence of increasing the number of comparators is the dramatically increasing of the die size and power consumption. Another problem of the flash ADC is the large input capacitance caused by the large number of comparators. Thus the circuit driving the ADC must have the ability to handle a large capacitive load. The flash

ADC requires the full resolution accuracy from every comparator; otherwise the comparator offsets will bring "bubbles" in the thermometer code. To manage the offset, the comparators in a flash ADC usually utilize the auto-zero technique. Likewise, the resistor ladder has to generate threshold voltages with the accuracy of the ADC resolution. Furthermore, the feedthrough of the analog input to the resistor ladder and the slew-dependent comparator delay degrade the static and dynamic performance of the flash ADC substantially.

Because of the large die size and high power consumption, the resolution of the flash ADC is usually limited to 6-bit. Reported performance with conversion rate of gigahertz have been achieved [11] [12] [13] [14], while the power consumption is in the order of hundreds of mW. The main application of flash ADCs is in modest resolution and extremely high speed is required, such as disk drive read channel circuits, local area network interface and ultra wideband receivers.

3.2 Two-Step ADC

To reduce the number of comparators in flash ADCs, the quantization of the input signal can be performed in two steps. The principle of the two-step ADC is illustrated in Figure 3.2. In this architecture, a coarse ADC generates the most significant bits (MSBs). The digital-to-analog converter (DAC) converts the coarse ADC output back to the analog format and subtracts it from the input signal. The residue is then converted by a fine ADC to generate the LSBs. The final digital output is the combination of the coarse ADC output and the fine ADC output. The residue signal as a function of the input voltage in a 4-bit two-step

Figure 3.2: Two-Step ADC.

ADC is shown in Figure 3.3 as an example. Since the DAC output needs to be subtracted from the input signal, a sample-and-hold is usually used at the front-end to avoid aperture error when a high frequency input signal is applied. Because the quantization is performed in two steps which require two clock cycles, the conversion speed of the two-step ADC is less than half of the speed of the flash architecture. However the number of comparators is reduced significantly. For an N -bit two-step ADC only $(2^{N_C} + 2^{N_F} - 2)$ comparators are required in which $N = N_C + N_F$. N_C and N_F are the resolutions of the coarse ADC and fine ADC, respectively. The reduction of the number of comparators results in less power consumption, lower capacitive load and smaller die size.

Although the number of comparators is reduced, the comparator accuracy requirement remains the same in a typical two-step ADC. Digital error correction techniques can be deployed to relax comparator offset error requirements. In these techniques, the number of comparators employed in the coarse ADC is larger than $2^{N_C} - 1$ therefore extra bits are generated. The extra bits are used to remove comparator offset errors in back-end digital error correction circuit. However, the accuracy requirement of the comparators in the fine

Figure 3.3: Residue as a function of input signal.

ADC is still $N_C + N_F$ unless an amplifier is inserted between the coarse and fine ADCs. To minimize the number of comparators in a two-step ADC, the resolution of the coarse ADC and fine ADC are chosen to be about the same. As a result, the interstage amplifier needs a high gain and has a small feedback factor which make it difficult to design and limits the overall performance of two-step ADCs.

The two-step ADC architecture allows for higher resolution than the flash architecture due to the reduction of number of comparators. The applications of two-step ADCs are most often found in video applications where medium resolution high speed are required. For the CMOS technology a sampling rate as high as 160 MS/s with a 10-bit resolution has been reported in [15], while a 12-bit resolution at 54MS/s has been achieved in [16]. However, both designs have large power dissipation and the application of two-step ADC in low-voltage environment is limited by the drawbacks mentioned above.

3.3 Folding and Interpolating ADC

The large number of comparators in Flash ADC can also be significantly reduced by the folding technique. A diagram of a folding ADC is shown in 3.4. The principle behind the folding technique is to perform the conversion in two steps just as the two-step ADC, but the coarse and fine converters operate in parallel. The folding circuit in front of the fine ADC generates the same signal as the subtraction circuit in the two-step ADC. Since the output from the coarse converter is not used in the fine converter, the coarse ADC and fine ADC work in parallel. Due to the parallel operation, the conversion rate of the folding ADC is approximately the same as the flash ADC while the number of comparators is only $2^{N_C} + 2^{N_F} - 2$, where N_C and N_F are the resolution of the coarse and fine ADCs respectively. The folded signal for $N_C = 2$ is shown in Figure 3.5.

Figure 3.4: Folding ADC.

In practice, the sawtooth waveform shown in Figure 3.5 is difficult to generate and a triangular waveform is preferred but it is still difficult to obtain a sharp corner in the waveform. Therefore the linearity for large output signals of the folding circuit is poor. This problem can be circumvented by using several folding circuits with different offsets

Figure 3.5: Transfer function of folding circuits.

and thus only utilizing a small linear portion of the input range. Unfortunately, with the number of folding circuits increasing, the complexity of the converter may be in the same order as the flash ADC. Therefore some of the folding signals are generated by resistive interpolation.

In Figure 3.6, an interpolation using resistors is shown. The signal $V1i$ and $V2i$ are interpolated between $V1$ to ground and $V2$ to $V1$, respectively. The relationship between $V1$, $V1i$ and $V2$ is illustrated in Figure 3.7. Only the linear region between the two dashed-line in Figure 3.7 will be used. A block diagram of a folding-and-interpolating ADC is shown in Figure 3.8. In this ADC, four folding circuits are followed by an interpolation network, and then the comparators. With the supply voltage decreasing, the linear range of the folding amplifier also decrease. Therefore, more and more interpolations are needed in low supply voltage environment. However, these multiple interpolations will increase the chip complexity and power consumption.

Figure 3.6: The resistor interpolation.

Figure 3.7: Illustration of voltage interpolation.

Figure 3.8: Folding and interpolating ADC.

The folding-and-interpolating architecture was originally developed for the bipolar technology, which is ideal for realizing accurate open-loop circuits because of good V_{be} matching and high transconductance of the bipolar transistor. On the contrast, the offset voltages in MOS transistors are the main obstacles to increasing accuracy. The resolution of CMOS folding-and-interpolation ADCs are limited to be around 8-bit by the following factors: tail current mismatch in the folding circuits, offset of preamplifiers, interpolation errors, offset of comparators and mismatch in the resistor ladder [18] [19] [20] [21]. Techniques such as averaging [22] [23] and self-calibration [24] are used to reduce offset sensitivity with the price of increasing of power consumption.

3.4 Pipelined ADC

Pipelined ADC is one of the most popular architectures for high speed, medium-to-high resolution, and low power applications. Figure 3.9 shows the structure of a typical pipelined ADC. A pipelined ADC consists of several cascaded stages, each resolving a few bits.

Figure 3.9: Pipelined ADC.

Each stage has a sub-ADC, a sub-DAC, a subtractor and an interstage gain amplifier. Usually the sub-DAC, the subtractor and the interstage gain functions are realized together by a switched-capacitor circuit, which is commonly called multiplying DAC (MDAC). The MDAC also functions as sample-and-hold for the next stage.

The operation of each stage is as follows. The sampled input signal is first quantized by the sub-ADC to produce the digital output code of this stage. Then this code is converted back to an analog signal by the sub-DAC. This analog signal is subtracted from the input signal to produce the residue. To relax the accuracy requirement of comparators in following stages, the residue is amplified by the interstage amplifier and then passed to the next stage for further quantization. Due to the sample-and-hold function in each stage (except the last stage), all stages work concurrently on the successive input signals to achieve a high throughput rate. Because of the pipelining, the first digital output is delayed by several clock cycles but in most applications this is not a severe limitation.

The pipelined ADC offers a number of advantages. First, the internal sample-and-hold function in the MDAC enables all the stages to work concurrently thus a high conversion rate is allowed. The speed of the pipelined ADC is only determined by the front-end S/H and the first stage that have the highest accuracy requirement. Second, the utilization of interstage amplifier relaxes the precision requirement of subsequent stages. For an N -bit pipelined ADC, if the first stage resolves M bits, then the following stages need only $N - M$ bits resolution. Thus, the currents in the later stages can be scaled down, leading to a lower power consumption. Third, the power and hardware of pipelined ADCs grow almost linearly with the number of bits compared to the exponential growth of power and hardware with the number of bits in the flash ADCs. Also, redundant bits and digital error correction can be used to remove large comparator offsets, making the use of high speed low power dynamic comparators possible in pipelined ADCs. Another key attribute of pipelined ADCs is that the interstage amplifier is only active during one phase of the clock cycle. In order to reuse the amplifier during the other clock phase, the op amp can be shared between two adjacent stages to further reduce power consumption [25] [26].

Because of its good linearity, the switched-capacitor (SC) technique has been widely employed in CMOS pipelined ADCs. Although current mode approaches have also been attempted [27], they have not been able to achieve the same performance as that of SC circuits. Nowadays, pipelined ADCs are successfully implemented in CMOS using switched-capacitor technique [25] [28] [29] [30] [31] [32]. The main errors in pipelined ADC come from capacitor mismatch, finite op amp gain, uncompleted op amp settling, MOS switch nonlinear on-resistance, charge injection, and clock jitter. Calibration techniques usually

involved in high-resolution pipelined ADCs eliminate these errors. In low voltage high speed pipelined ADCs, the primary trade-off lies between the precision and speed of the interstage amplifier. Much efforts have been attempted to design high gain high speed op amps, or improve system architecture to relax op amp requirements [33] [34]. More details of pipelined ADCs will be described in Chapter 4.

3.5 Time-interleaved ADC

If speed is the primary concern of an ADC, interleaving technique can be used to further improve the conversion rate. A time-interleaved ADC uses several paralleled ADCs operate on different clock phases to increase the overall speed. The concept of the time-interleaved ADC is shown in Figure 3.10. The sub-ADCs can be of any kind and operate at f_s/M .

Figure 3.10: Time-interleaved ADC.

The parallel operation also introduces new problems which are mainly caused by mismatch between the channels. These errors include the different channel offsets, different channel gains, and skew in the clock signals. Because of the channel mismatch, time-interleaved ADCs usually use additional calibration circuits to suppress these errors. The

offset can be rather easily calibrated using a mixed signal or all-digital circuitry [35]. Gain mismatch calibration is also possible, but requires more complex circuits than offset calibration [36]. The clock skew may rise due to the different propagation delays of the sample-and-hold circuits. This problem can be avoided by using a full-speed front-end sample-and-hold circuit instead of distributed channel sample-and-hold. However, the problem is that the S/H circuit has to be very fast, since it operates at full speed.

The need of several paralleled ADCs results in the large chip size and high power dissipation. The speed and power of time-interleaved ADC are determined by that of the sub-ADCs. Therefore, the researches on improving non-interleaved ADC performance can also benefit the time-interleaved ADC in speed and power consumption.

3.6 State-of-the-Art High Speed ADCs

A commonly used figure of merit (FOM) [52][59][90] based on the measured values of the sampling rate f_s , ENOB, and power consumption P is calculated according to:

$$FOM = \frac{P}{2^{ENOB} \cdot f_s} \quad (3.1)$$

In this equation, the unit of power is mW and the unit of sampling rate is in MHz . Therefore, the FOM has a dimension of pico-Joule (pJ), i.e., the energy used per conversion. Table 3-1 summaries the state-of-art high speed ADCs with 8 to 10 bits resolution.

3.7 Conclusion

This chapter describes the high speed ADC architectures. Each architecture has its own characteristics that makes it fit in certain applications. For high speed and low resolution (less than or equal to 6-bit) applications, the flash ADC is the best choice. For higher resolution, although two-step and folding and interpolating architectures can achieve fast speed, they are not suitable in low voltage applications for the reasons in foregoing discussion. Based on the comparison, it can be concluded that the pipelined ADC are the most suitable for high speed low power applications in low voltage environment. For the last six years, most research in high speed ADC with moderate resolution were in pipelined ADCs.

Table 3.1: 8-10 bits high-speed ADCs summary

Ref.	Arch.	Res.	Samp. Rate	Tech.	Supply	DNL	INL	SFDR	SNDR	ENOB	Power Diss.	Die Size	FoM
[48]	Pipelined	10b	50MS/s	0.13 μm	1.2V	0.17	0.16	70.4dB	56.6dB	9.1b	15mW	0.2mm ²	0.55
[49]	Pipelined	10b	50MS/s	0.18 μm	1.8V	0.2	0.4	69dB	54.6dB	8.8b	18mW	1.43mm ²	0.81
[50]	Pipelined	10b	125MS/s	90nm	1.2V	<1.0	<1.0	N.A	58.5dB	9.4b	37.5mW	0.3mm ²	0.44
[51]	Time-Inter.	10b	400MS/s	0.13 μm	1.2V	0.4	0.3	N.A	53.7dB	8.6b	160mW	4.2mm ²	1.03
[52]	Pipelined	10b	200MS/s	90nm	1.2V	0.66	1	66.5dB	53.6dB	8.6b	55mW	2.52mm ²	0.71
[82]	Pipelined	8b	200MS/s	0.18 μm	1.8V	0.44	0.44	57.5dB	48dB	7.7b	30mW	0.15mm ²	0.72
[54]	Time-Inter.	10b	44MS/s	0.25 μm	2.5V	1.34	1.14	N.A	60dB	9.7b	20mW	10.92mm ²	0.55
[55]	Pipelined	10b	50MS/s	0.18 μm	1.8V	0.91	1.2	67dB	55dB	8.8b	35mW	1.2mm ²	1.57
[56]	Pipelined	10b	125MS/s	0.18 μm	1.8V	0.5	0.7	N.A	53.7dB	8.6b	40mW	0.66mm ²	0.82
[57]	Pipelined	10b	12MS/s	90nm	1.2V	1	1.3	60.8dB	52.6dB	8.4b	3mW	0.3mm ²	0.8
[58]	Time-Inter	8b	150MS/s	0.18 μm	1.8V	0.43	0.64	52.5dB	46.8dB	7.5b	71mW	1.8mm ²	2.61
[59]	Two-Step	8b	125MS/s	0.13 μm	1.2/2.5V	0.15	0.25	N.A	N.A	7.7b	21mW	0.09mm ²	0.81
[60]	Folding	8b	1.6GS/s	0.18 μm	1.8V	0.15	0.35	56dB	46dB	7.3b	744mW	3.6mm ²	2.95
[61]	Pipelined	10b	80MS/s	0.13 μm	1.5V	N.A	<1	N.A	N.A	9b	33mW	N.A	0.81
[62]	Pipelined	10b	220MS/s	0.13 μm	1.2V	0.5	1	62.1dB	54.3dB	8.7b	135mW	1.3mm ²	1.62
[63]	Pipelined	10b	100MS/s	0.18 μm	1.8V	0.8	1.6	65dB	54dB	8.7b	67mW	2.53mm ²	1.61
[64]	Pipelined	10b	40MS/s	0.25 μm	2.5V	0.77	1.15	N.A.	59dB	9.5b	11.7mW	0.696mm ²	0.4
[65]	Pipelined	10b	150MS/s	0.18 μm	1.8V	0.69	1.5	64.8dB	52dB	8.3b	123mW	2.2mm ²	2.6
[66]	Pipelined	10b	120MS/s	0.25 μm	2.5V	0.4	0.48	68.4dB	54.1dB	8.7b	208mW	3.6mm ²	4.17
[67]	Pipelined	10b	80MS/s	0.18 μm	3V	0.25	0.5	72.8dB	57.9dB	9.3b	69mW	1.85mm ²	1.37
[68]	Pipelined	10b	25MS/s	0.35 μm	1.4V	0.9	3.3	55dB	48dB	7.7b	21mW	2.24mm ²	4.04
[69]	Pipelined	10b	30MS/s	0.3 μm	2V	0.4	0.5	64dB	54.2dB	8.7b	16mW	3.12mm ²	1.28
[70]	Time-Inter	10b	120MS/s	0.35 μm	3.3V	0.44	0.88	70.2dB	56.8dB	9.1b	234mW	5.2mm ²	4.18
[71]	Pipelined	8b	80MS/s	0.5 μm	3V	0.32	0.51	56.9dB	43.8dB	7b	268mW	10.3mm ²	26.18
[72]	Time-Inter	10b	200MS/s	0.5 μm	3V	0.8	0.9	55dB	43dB	6.9b	280mW	7.4mm ²	11.72
[73]	Pipelined	10b	100MS/s	0.18 μm	1.8V	0.66	0.76	63.95dB	57.1dB	9.2b	80mW	2.55mm ²	1.36
[74]	Pipelined	9b	14MS/s	0.5 μm	1.5V	0.6	0.9	55.3dB	50dB	8b	8.2mW	1.3mm ²	2.28
[75]	Pipelined	10b	40MS/s	0.35 μm	3V	0.3	0.75	72dB	59dB	9.5b	55mW	2.6mm ²	1.9

Chapter 4

Pipelined ADC Design Considerations

In section 3.4 the fundamentals of pipelined ADCs were reviewed. It is evident that the pipelined ADC architecture is well-suited for the IEEE 802.11 wideband communication receiver applications where high speed and low power are required. In practice, pipelined ADCs can be implemented using either switched-capacitor or switched-current techniques. Although switched-current techniques are good for high speed and low voltage operation, switched-current implemented pipelined ADCs have not been able to achieve the same performance as that of switched-capacitor pipelined ADCs due to the mismatch between current mirrors and charge injections caused by MOS switches [87][88]. On the other hand, switched-capacitor circuits can archive high accuracy by employing high gain op amps, making switched-capacitor implementation prevailing in pipelined ADCs. This chapter focuses on the discussion of switched-capacitor pipelined ADCs and emphasize the design challenges in low voltage with deep sub-micron process.

4.1 Building Blocks in Pipelined ADC

A pipelined ADC distributes the quantization to several low-resolution stages and combines their outputs as the final output. Because of the distribution and pipelining, high speed and high resolution are expected. A detailed block diagram of a typical pipelined ADC is drawn in Figure 4.1. It consists of a sample-and-hold, k pipelined stages, delay cells, and digital error correction circuits. Each pipelined stage has a resolution of $(M_i + 1)$ bits. The extra one bit overlaps with the first bit of next stage digital output as a redundant bit. The last pipeline stage does not need the redundant bit and is usually implemented by a flash ADC with M_k bit resolution. The total number of digital output bits from pipeline stages is therefore given by:

$$N_{total} = \sum_{i=1}^{k-1} (M_i + 1) + M_k \quad (4.1)$$

Figure 4.1: Block diagram of a pipelined ADC.

The N_{total} -bit data are fed into the digital error correction circuit which generates the

final N -bit output. The resolution N of the ADC is given by

$$N = \sum_{i=1}^k M_i \quad (4.2)$$

In practice, the number of possible output codes of stage i can be less than 2^{M_i+1} as the redundant bit does not need to be a full bit. A good example of this is the 1.5-bit stage which has 3 different output codes.

The timing diagram of a 7-stage pipelined ADC is shown in Figure 4.2 as an example. Due to the build-in S/H function in pipelined stages, consecutive stages operate in opposite clock phases. Hence, when the odd stages are in the holding mode, the even stages are in the sampling mode, and vice versa. As a result, one sample passes two stages in one clock cycle and the latency of the output to the input is typically half the number of the stages. Since different bits of an input signal is generated at different times, digital delay lines are needed for data alignment.

4.1.1 Sample-and-Hold

To eliminate the errors at high frequency, an input sample-and-hold circuit is needed in front of the first pipelined stage. Typically the noise and distortion performance of the S/H circuit determines the dynamic performance of the pipelined ADC. A conventional switched-capacitor implementation of S/H circuit is shown in Figure 4.3.

In this S/H circuit, during the sampling mode, switches controlled by ϕ_1 are turned on and the input signal is sampled in C_S and the feedback capacitor C_F is reset. During the holding mode, ϕ_2 connects the input plate of C_S to ground, the charges in C_S are transferred

Figure 4.2: Timing diagram of a 7 stages pipelined ADC.

Figure 4.3: SC implementation of sample-and-hold circuit.

to the feedback capacitor C_F . Assuming the op amp is ideal, the sampled output is given by

$$V_{out} = V_{in} \frac{C_S}{C_F} \quad (4.3)$$

4.1.2 Pipelined Stage

A detailed pipelined stage is illustrated in Figure 4.4. The stage resolution is $M_i + 1$ bit including one redundant bit. The S/H function is embedded in the SC amplifier. The input signal of each stage is the output of the previous stage, i.e., $V_{in,i} = V_{out,i-1}$. The input signal is quantized by the sub-ADC, which generates the digital output D_i . The sub-DAC then converts D_i back to analog form with the value of $D_i \cdot V_{ref}$. This value is subsequently subtracted from the input signal and their residue is amplified by the stage gain G_i , which is usually equal to 2^{m_i} , yielding the output voltage as

$$V_{out,i} = G_i \cdot (V_{out,i-1} - D_i \cdot V_{ref}) \quad (4.4)$$

Figure 4.4: A pipeline stage.

In practical implementation, the functions of sample-and-hold, digital-to-analog conversion, subtraction, and amplification are usually realized by a switched-capacitor circuit which is called MDAC. The sub-ADC is usually a flash ADC consisting of a few comparators and digital gates.

A switched-capacitor implementation of a 1.5-bit stage is shown in Figure 4.5. During clock phase ϕ_1 , the input signal is sampled by the capacitors C_S and C_F , which are equal

in size. At the end of phase ϕ_1 , the sub-ADC compares the input signal with the threshold voltages $+V_{ref}/4$ and $-V_{ref}/4$, generating the stage digital output D_i . In the second phase, ϕ_2 , the capacitor C_F is flipped around and connected between the input and output of the op amp thus forming a feedback loop [80]. During this phase, depending on the value of the sub-ADC output, the capacitor C_S is connected to one of the three reference voltages, $+V_{ref}$, 0, and $-V_{ref}$. The resulting analog output is given by

$$V_{out} = V_{in} \cdot \frac{C_S + C_F}{C_F} - D_i \cdot V_{ref} \cdot \frac{C_S}{C_F} \quad (4.5)$$

where D_i has the possible value of -1, 0, and +1.

Figure 4.5: Switched-capacitor implementation of 1.5-bit stage.

The relation between V_{in} , D_i , and connection of C_S is shown in Table 6.1. The transfer function of the 1.5-bit stage is shown in Figure 4.6.

4.1.3 Digital Error Correction

In a pipelined ADC where the interstage amplifier gain equals to the resolution of this stage, e.g. amplifier gain =4 for resolution = 2-bit, the comparators in sub-ADC must be very accurate. An offset error of the comparator can saturate the input of next stage. As an

Table 4.1: Relation between V_{in} , D_i , and connection of C_S

V_{in}	D_i	Connection of C_S
$< -V_{ref}/4$	-1	$-V_{ref}$
$-V_{ref}/4 \leq V_{in} \leq +V_{ref}/4$	0	0
$> +V_{ref}/4$	+1	$+V_{ref}$

Figure 4.6: Transfer function of 1.5-bit stage.

example, the transfer function of a 2-bit stage is shown in Figure 4.7. Because of the signal saturation, there is a large conversion error and the effective resolution of ADC is reduced. To relax the requirements on comparators, digital error correction can be use [6].

One significant advantage of pipelined ADC is the possible applications of the digital error correction technique which significantly relaxes the accuracy requirement of the comparators in the sub-ADC. Therefore the sub-ADC needs only to be accurate enough to

Figure 4.7: Comparator offset causes signal saturation.

prevent the saturation of residue voltage after amplification. If this is satisfied, the accuracy of the comparator does not affect the ADC's final accuracy. In a pipelined ADC with digital error correction, the interstage amplifier gain is reduced to introduce redundancy. This is illustrated in Figure 4.8 for the transfer function of a 2-bit stage in a pipelined ADC. The interstage gain has been reduced from 4 to 2. The output signal swing of the first stage is now only half the input range of the following stage. Hence the shifting of the comparator decision level in the first stage will not cause saturation in the following stage.

Figure 4.8: Transfer function of a 2-bit stage with reduced residue gain.

One advantage of 1.5-bit stage is that it can tolerate large comparator offset errors because of its low stage resolution and reduced interstage amplifier gain. To explain how digital error correction works, consider a 1.5-bit stage followed by a full 2-bit stage to form a 3-bit pipelined ADC. The transfer function of the first stage and the outputs of both stages are shown in Figure 4.9.

Figure 4.9: Comparator offset tolerance in 1.5-bit stage.

When an input signal slightly larger than $-V_{ref}/4$ is applied to the first stage, if the comparators are ideal, the digital output of the first stage should be 01. From the transfer curve of the 1.5-bit stage, the analog output of the first stage should be within $-V_{ref}/2$ to 0. The analog output of the first stage is the input of the second stage, and the second stage is a full 2-bit ADC. Thus the digital output of the second stage should be 01. Then the total

output is obtained from:

$$\begin{array}{rcl}
 \text{Stage1} & & 0 \ 1 \\
 \text{Stage2} & + & 0 \ 1 \\
 \hline
 \text{Output} & & 0 \ 1 \ 1
 \end{array}$$

If the comparator is not ideal and has a threshold voltage larger than both $-V_{ref}/4$ and the input signal (as shown in Figure 4.9), then the digital output of the first stage will be 00 and the analog output of the first stage becomes within the range $V_{ref}/2$ to V_{ref} . Therefore the digital output of the second stage becomes 11. In this case the total output is:

$$\begin{array}{rcl}
 \text{Stage1} & & 0 \ 0 \\
 \text{Stage2} & + & 1 \ 1 \\
 \hline
 \text{Output} & & 0 \ 1 \ 1
 \end{array}$$

which is the same as in the ideal condition.

With digital error correction, the comparator offset errors can be removed as long as the residue stays in the input range of the following stage. In the 1.5-bit stage architecture, an offset error as large as $\pm V_{ref}/4$ can be tolerated, which enables the use of fast low power dynamic comparators in sub-ADCs. However, the comparators in the last stage must be accurate because no following stage to compensate their offset errors.

Since some of the digital output codes are used as the redundant bits, more stages are needed to generate extra bits when digital error correction is used in a pipelined ADC. For this reason, usually six 1.5-bit stages and one 2-bit stage are used in an 8-bit pipelined ADC.

4.1.4 Stage Resolution and Power Consumption

In pipelined ADCs the stage resolution can be arbitrary. However, the number of bits each stage resolves has a large impact on the overall speed, accuracy, and power dissipation. Therefore the best choice of the stage resolution depends on the overall ADC specifications.

For a stage with low resolution, i.e. 1.5-bit, the comparator requirements in the sub-ADC are more relaxed. In this structure, a large comparator offset error will not saturate the following stages and this error can be removed by a digital error correction circuit. The interstage amplifier of low resolution stage requires a lower close-loop gain than that required by high resolution stage. Consequently, a low resolution stage has larger feedback factor and a higher speed. However, more stages are required if there are fewer bits per stage. Furthermore, the noise and gain errors of the later stages contribute more to the overall converter inaccuracy because of the low interstage gain [76].

For a higher resolution stage, the accuracy requirement of its interstage amplifier is relaxed since the following stages have few resolution bits to resolve. For example, in a 12-bit pipelined ADC, if the first stage resolves 2 bits, then the amplifier in this stage needs at least 10 bits accuracy which is equal to the remaining resolution for the following stages. If the first stage has a 4 bits resolution, the amplifier needs only 8-bit accuracy. The decrease of accuracy requirement lowers the open-loop gain requirement of the op amp, making it attractive in high resolution applications. However, in higher per stage resolution architecture, the op amp has a smaller feedback factor and the comparator has a smaller offset margin.

With pipelining, the maximum conversion rate becomes almost independent of the

number of stages but limited by the speed of single stage. Thus, for high-speed applications, it is desirable to minimize the number of bit per stage to maximize its speed. It has been proved for a pipelined ADC with resolution less than 10-bit, a single stage resolution of 1.5-bit is the optimized implementation [76].

4.1.5 Stage Scaling

In pipelined ADCs, the stage accuracy requirement decrease along the pipeline. The noise contribution of later stages are attenuated by the gain of previous stages. The total noise referred to the ADC input can be expressed as

$$\overline{V}_{e,total}^2 = \overline{V}_{e,1}^2 + \frac{\overline{V}_{e,2}^2}{G_1^2} + \frac{\overline{V}_{e,3}^2}{G_1^2 \cdot G_2^2} + \dots \quad (4.6)$$

where $\overline{V}_e$ is stage noise and G is stage gain. Along with the pipeline, the accuracy requirements are less and lesser stringent. Therefore the stages need not to be identical. Hence the op amp current and the sampling capacitor size can be scaled down along the pipeline to save power and die size.

4.2 Error Sources and Design Considerations of Pipelined ADCs

In a switched-capacitor implemented pipelined ADC, the major error sources include finite op amp DC gain, incomplete op amp settling, capacitor mismatch, MOS switch linearity, and clock jitter. As the device size scales down and supply voltage decreases, most of the

errors become severe. This section discusses these error sources and design consideration to minimize these errors.

4.2.1 Op Amp Gain

The transfer function of the 1.5-bit stage described by equation 4.5 is the ideal function. The assumption in this equation is that the op amp has infinite gain. Op amp is the most crucial block in a pipelined ADC and its DC gain determines the ADC accuracy. In practice, because of the finite op amp DC gain, errors are introduced in the residue transfer function of MDAC. The switched-capacitor residue amplifier in a 1.5-bit stage is shown in Figure 4.10. During the sampling phase ϕ_1 , the charge reserved in the sampling capacitors is

Figure 4.10: Switched-Capacitor implementation of 1.5-bit ADC stage.

$$Q_1 = V_{in} \cdot (C_S + C_F) \quad (4.7)$$

In the holding phase ϕ_2 , due to the finite op amp DC gain, the op amp input, node X, is not grounded but has a value of $V_X = -V_{out}/A_0$, where A_0 is the op amp DC gain. Therefore, the charge reservation at this phase can be expressed as

$$Q_2 = (V_{out} - V_x) \cdot C_F + (D_i \cdot V_{ref} - V_x) \cdot C_S - V_x \cdot C_{in} \quad (4.8)$$

where D_i is the sub-ADC output and C_{in} is the op amp gate input capacitance. Based on the charge conservation, $Q_1 = -Q_2$, the transfer function of the op amp gain can be expressed as:

$$V_{out} = \frac{1}{1 + \frac{1}{A_0 \cdot \beta}} \left(V_{in} \cdot \frac{C_S + C_F}{C_F} - D_i \cdot V_{ref} \cdot \frac{C_S}{C_F} \right) \quad (4.9)$$

where $\beta = C_F / (C_F + C_S + C_{in})$ is the feedback factor in the holding mode. If $A_0 \cdot \beta \gg 1$, the transfer function can be written as:

$$V_{out} = \left(1 - \frac{1}{A_0 \cdot \beta} \right) \left(V_{in} \cdot \frac{C_S + C_F}{C_F} - D_i \cdot V_{ref} \cdot \frac{C_S}{C_F} \right) \quad (4.10)$$

Therefore, the finite op amp DC gain introduces an error equal to $1/(A_0 \cdot \beta)$ which lowers the residue amplifier gain. The transfer function of the 1.5-bit stage with gain error is shown by the dash-line in Figure 4.11. This gain error depends on the input and reaches its maximum when the output voltage reaches its maximum value.

To prevent the gain error flowing to the following stage, the error $1/(A_0 \cdot \beta)$ must be less than half the LSB of following stages, thus the stages in the front must have higher op amp DC gain requirements. In a pipelined ADC, the op amp of first stage requires the highest DC gain. For an N -bit pipelined ADC, if the first stage is 1.5-bit stage, its following stages have a resolution of $N - 1$, therefore gain error requirement is

$$\frac{1}{A_0 \cdot \beta} < \frac{1}{2 \times 2^{N-1}} \quad (4.11)$$

which requires the op amp DC gain to be

$$A_0 > \frac{1}{\beta} \cdot 2^N \quad (4.12)$$

In practice, a few dB gain margin is needed to overcome process variation. The design of high gain op amp is the most crucial challenge in deep sub-micron analog circuit design.

Figure 4.11: Transfer curve of 1.5-bit stage with gain error.

4.2.2 Op Amp Offset

The effect of op amp offset in a MDAC is illustrated in Figure 4.12, where the voltage source V_{os} represents the op amp offset. Using the same method for deriving the gain error, the 1.5-bit stage transfer function with op amp offset can be expressed as

Figure 4.12: 1.5-bit stage with op amp offset.

$$V_{out} = V_{in} \cdot \frac{C_S + C_F}{C_F} - D_i \cdot V_{ref} \cdot \frac{C_S}{C_F} + V_{os} \frac{C_F + C_S}{C_F} \quad (4.13)$$

The op amp offset introduces a constant error in the output voltage as depicted in Figure 4.13. This error of V_{out} causes the saturate on the following stages. The op amp offset error can be minimized by using techniques such as auto-zero and chopper. Alternatively, the error can be compensated by analog or digital calibration circuits as long as the error is constant.

Figure 4.13: Transfer curve of 1.5-bit stage with op amp offset.

4.2.3 Op Amp Slew Rate and Bandwidth

When the MDAC enters the holding mode, the op amp output takes some time to settle to its final value as shown in Figure 4.14. The speed of a pipelined ADC is mostly constrained by op amp settling time. The op amp settling time consists of two parts, the nonlinear slewing

Figure 4.14: Settling of op amp output.

and the quasi-linear settling, $t = t_{slew} + t_{settle}$. At the beginning of the holding mode, the op amp enters to the slewing phase first. In this phase, the op amp uses its maximum output current I_{max} to charge the load capacitance C_L until it goes into the linear settling phase. The slew time is determined by the slew rate (SR) of op amp, which is

$$SR = \frac{I_{max}}{C_L} \quad (4.14)$$

In pipelined ADC design, t_{slew} needs to be minimized for two reasons. Firstly, the smaller the slew time t_{slew} , the faster the op amp settling, leading to an improvement of ADC speed. Secondly, if t_{slew} is small, then the op amp is in the linear settling phase at the end of holding phase. Since the settling is linear, the error of the op amp output is approximately constant and can be treated as an ADC gain error which is not harmful in most applications. A good practice is to limit t_{slew} within one-quarter of the half sampling clock cycle.

In the settling phase, the op amp output settles exponentially towards its final value. If

the op amp has a dominant pole and a second pole at a much higher frequency than that of the dominant pole, the output in this phase can be expressed as

$$V_{out}(t) = (1 - e^{-\frac{t}{\tau}})(V_{in} \cdot \frac{C_S + C_F}{C_F} - D_i \cdot V_{ref} \cdot \frac{C_S}{C_F}) \quad (4.15)$$

where τ is the settling time constant for settling.

Obviously from equation 4.15, there is an error introduced by the incomplete settling of the op amp. For an N-bit pipelined ADC, if the first state is a 1.5-bit state, the following stages have a resolution of $N - 1$, therefore incomplete settling error should satisfy

$$e^{-\frac{t}{\tau}} < \frac{1}{2 \times 2^{N-1}} \quad (4.16)$$

For pipelined ADCs, the maximum allowed settling time, t , is half of the sampling clock period. Then the minimum value for τ should be

$$\tau < \frac{1}{2 \cdot F_S \cdot N \cdot \ln 2} \quad (4.17)$$

The time constant τ can be further related to the unity gain bandwidth, ω_u , of the op amp as

$$\tau \approx \frac{1}{\beta \cdot \omega_u} \quad (4.18)$$

As a result, the op amp bandwidth requirement for a incomplete settling error smaller than half LSB of following stages is

$$\omega_u > \frac{2 \cdot N \cdot F_S \cdot \ln 2}{\beta} \quad (4.19)$$

Most typical amplifiers have multiple poles and has to be characterized by more complex functions. In practice, a much larger bandwidth is required. Furthermore, the timing must also be allocated for rising and falling edges of the clock as well as the non-overlap interval.

4.2.4 Charge Injection

In switched-capacitor circuits, MOS transistors are used as switches. A conducting MOS switch has a finite amount of mobile charge in its channel. The total charge stored in channel is [77]

$$Q_{ch} = C_{ox} \cdot (V_{gs} - V_{th}) \cdot W \cdot L \quad (4.20)$$

When the transistor is turned off, this charge is distributed between the source and drain of the device as shown in Figure 4.15

Figure 4.15: Charge injection in MOS switch.

Although the percentage of the total charge that is dumped to the source or drain is not exactly determined, but it has been assumed as fifty percent to each terminal. The charge dumped to V_{in} is not problematic, since V_{in} is a source-driven node. But the charge injected to the sampling capacitor will cause a voltage change on the capacitor. Assume that fifty percent of the total charge stored in the channel will be dumped to the sampling capacitor. Then, the change in voltage on the capacitor due to charge injection is

$$\Delta v = \frac{Q_{ch}}{2C_S} = \frac{C_{ox} \cdot (V_{gs} - V_{th}) \cdot W \cdot L}{2C_S} \quad (4.21)$$

Equation (4.21) shows that the voltage change depends on the input signal which results in signal-dependent distortion. Several techniques have been used to overcome this problem. The first method uses a dummy transistor whose size is the half of the MOS switch to absorb the channel charge as illustrated in Figure 4.16.

Figure 4.16: Canceling the charge injection with a dummy transistor.

Although the dummy transistor can reduce the effect of charge injection, the cancellation of charge inject is not complete as the two transistors are not ideally matched. Therefore this technique is sensitive to parasitics. Another technique to eliminate charge injection problem is called bottom plate sampling as shown in Figure 4.17.

Figure 4.17: A S/H circuit with bottom-plate sampling.

This sampling circuit is controlled by two clock phases ϕ_1 and ϕ_{1a} . These two clocks are in phase but ϕ_{1a} has a falling edge slightly earlier than ϕ_1 . In the sampling mode,

switches M_1 and M_2 are turned on and the input signal is sampled in C_S . At the end of the sampling mode, M_2 turns off first, leaving the top plate of C_S floating. Because there is no other DC path from the capacitor top plate, the charges from M_1 could not feed into the bottom plate of C_S . The charges from the other side of M_1 are absorbed by the signal source. Thus the signal-dependent charge-injection caused by M_1 is eliminated.

4.2.5 CMOS Switches

The on-resistance of a conducting MOS switch can be written as:

$$R_{on} \approx \frac{1}{\mu C_{ox}(W/L)(V_{gs} - V_{th})} \quad (4.22)$$

The R_{on} is inversely proportional to the overdrive voltage $V_{ov} = V_{gs} - V_{th}$ as shown in Figure 4.18 for NMOS and PMOS respectively.

Figure 4.18: On-resistance of MOS switches.

At high supply voltage, a MOS transistor has been a reasonably good approximation of

an ideal switch. At lower supply voltage, because of the insufficient overdrive voltage, R_{on} increases dramatically. The increase of R_{on} increases the RC time constant and slow down the speed of sampling. In addition, the signal-dependent R_{on} introduce nonlinearity in the ADC performance. Although the size of MOS switch can be enlarged to decrease R_{on} , a large device increases the capacitive load which in turn slows down the circuit speed.

The insufficient overdrive voltage prevents the use of MOS switches for low-voltage applications in their standard form. There are three approaches to overcome this problem.

The first method is to use low threshold voltage transistors as switches. Although most process support low V_{th} device, this method requires special mask layers and may suffer from leakage of the stored charge.

The second method is based on the switched-opamp (SO) technique [78] [79]. It is observed that in the conventional SC circuits, the switches suffering from insufficient overdrive voltage are those connected to the input or output of an op amp. In Figure 4.5, these switches are the ones connect C_S and C_F to the input during the sampling mode and the one connects the C_F to the output during the amplifying mode. Other switches operating around a constant voltage level can be adjusted to provide an adequate overdrive voltage. In the SO circuits, the problematic switches are removed and their function is realized by switching the op amp on and off. The resulting circuits are capable of low voltage operation. One example of a fully differential SO MDAC is shown in Figure 4.19 [78]. In contrast to the SC circuit, the feedback capacitors of the SO circuit are permanently connected from the output to the input of the amplifier and the input capacitors to the output of the preceding stage. The function of the switches connecting the input signal and op

amp output are replaced by switching the op amp output to ground during the amplifying mode. Therefore, no switch is suffering from the signal dependent on-resistance in the SO implementation. However, the maximum achievable feedback factor of the SO MDAC in a 1.5-bit stage is $1/4$ instead of $1/2$ as in the SC implementation, therefore the SO circuit is inherently slower than the SC circuit. Moreover, the speed is further reduced by turning the op amp on and off. Thus the switched-opamp technique is not suitable for high-speed applications.

Figure 4.19: Fully differential switched-opamp 1.5-bit MDAC.

The third method is to use a bootstrapping circuit to make the gate voltage of the switch follows the input signal. The conceptual bootstrapped MOS switch and its output are shown in Figure 4.20 [80]. In the OFF state, the gate is grounded and the switch is cutoff. In the ON state, a constant voltage is connected between the gate and source of the MOS switch to guarantee a sufficient overdrive voltage. At the same time, the linearity of this switch is improved because of the constant gate-source voltage.

Figure 4.20: Concept of the bootstrapped MOS switch.

4.2.6 Capacitor Size

The capacitor size in pipelined ADCs directly relates to the ADC speed and power consumption. For a higher speed and lower power consumption, the capacitor size should be as small as possible. The minimum capacitor size is limited by two factors, i.e., thermal noise and capacitor matching.

Thermal noise is caused by the random motion of electrons. It is the most fundamental noise in a pipelined ADC. There are two sources of thermal noise in the pipelined ADC. One is the thermal noise due to the non-zero resistance switches; the other is the noise from the active transistors of the op amps. The noise in the sampling switch is usually referred to as kT/C noise because the noise power is equals to kT/C where k is the boltsman's constant, T is the temperature in Kelvin, and C is the size of the sampling capacitors.

In the switched-capacitor 1.5-bit ADC stage as shown in Figure 4.5, when the input signal is sampled into the capacitors C_S and C_F , the thermal noise is also sampled into these capacitors connected to the op amp input with the magnitude of

$$\overline{V_n^2} = \frac{kT}{C_S + C_F + C_{in}} \quad (4.23)$$

where C_{in} is the op amp input capacitance. The total thermal noise charges are

$$\overline{Q_n^2} = (C \cdot \overline{V_n})^2 = kT(C_S + C_F + C_{in}) \quad (4.24)$$

In the holding mode, when the feedback capacitor C_F is connected from the output to the input of the op amp, the thermal noise charges are transferred to C_F , generating the output noise whose magnitude is

$$\overline{V_{out}^2} = \frac{\overline{Q_n^2}}{C_F^2} = kT \cdot \frac{(C_S + C_F + C_{in})}{C_F^2} = \frac{kT}{C_F \cdot \beta} \quad (4.25)$$

where $\beta = (C_S + C_F + C_{in})/C_F$ is the feedback factor.

To prevent the thermal noise from degrading the ADC performance, the output thermal noise power should be smaller than the quantization noise power which is $LSB^2/12$ as given in equation (2.2). This sets the lowest limit for the total sampling capacitor size as

$$C_F \cdot \beta > \frac{kT \cdot 12}{LSB^2} \quad (4.26)$$

In addition to the thermal noise, the op amp noise also contributes to the nonidealities. The op amp noise is dependent on the circuit topology and can be superimposed on the thermal noise once the op amp circuit is decided.

Capacitance mismatch is another major error source in pipelined ADCs, which can affect the linearity directly. In the transfer function of 1.5-bit stage as shown in Figure 4.5, If the capacitors C_S and C_F are not equal, then an error proportional to the mismatch is generated in the residue output as shown in Figure 4.21 with the transfer function of

$$V_{out} = V_{in} \cdot \frac{\Delta C + C_S + C_F}{C_F} - D_i \cdot V_{ref} \cdot \frac{\Delta C + C_S}{C_F} \quad (4.27)$$

For an N-bit ADC, for this error should be less than half LSB of the following stage, the capacitance mismatch should satisfies:

$$\Delta C/C < 1/2^N \quad (4.28)$$

In most low-to-medium resolution ADCs, capacitor sizes are not limited by thermal noise but by matching. Like the finite gain effect, the requirement on capacitance matching is also scaled down with the pipeline and both errors can be compensated by calibration techniques.

Figure 4.21: 1.5-bit stage transfer function with capacitor mismatch.

4.2.7 Clock Jitter

In sampling systems such as pipelined ADC, any clock jitter will produce noise at the output. Because of its random nature, the clock jitter does not introduce harmonic tones

in the output spectrum but increasing the noise floor of the system. For a sine wave input signal of $V_{in}(t) = (V_{FS}/2)\sin(2\pi f_{in}t)$, the maximum sampling error occurs at the signal zero-crossing. The maximum slope of the signal can be presented as

$$\left. \frac{dV_{in}}{dt} \right|_{max} = \pi f_{in} V_{FS} \quad (4.29)$$

Assuming the sampling clock jitter is Δt , the aperture error voltage, V_e , can be calculated as

$$V_e = \pi f_{in} V_{FS} \Delta t \quad (4.30)$$

Therefore, the SNR including the sampling clock jitter is

$$SNR = \frac{(FS/2)^2/2}{(LSB^2/12 + \pi^2 f_{in}^2 V_{FS}^2 \Delta t^2/2)} \quad (4.31)$$

4.3 Conclusion

The pipelined ADC in detail and design challenge were discussed in this chapter. It also presents the sources of errors that exist in a pipelined ADC. The accuracy and speed of a pipelined ADC are limited by numerous factors including op amp performance, MOS switch linearity, device mismatch, and clock jitter. Solutions to minimize these error source are reviewed in this chapter. Among these affecting factors, the op amp is the crucial one and becomes more and more significant in deep sub-micron low voltage pipelined ADC design. The major problems facing op amp design in deep sub-micron technology is the reduced SNR and op amp gain. This project will focus on searching new techniques to relax the op amp requirements, reduce ADC power consumption and increase ADC speed as well.

Chapter 5

The Mixed-Mode Sample-and-Hold Circuit

5.1 Overview

Most pipelined ADCs include a sample-and-hold circuit at the front-end to minimize the high frequency errors and to improve system performance. The performance of the S/H circuit dominates the overall ADC dynamic characteristics and plays a major role in determining the SFDR and SNDR of the system.

The stringent performance requirements of the S/H circuit make it the most design-challenging and power-hungry block in a pipelined ADC. It has been shown that a dedicated front-end S/H circuit can be removed and the sampling function is performed in the first stage of a pipelined ADC [81]. However, in this implementation, the resolution of the first stage needs to be larger than 2-bit to reduce the signal swing so that the aperture

errors can be removed in the digital error correction circuit. The multi-bit first stage configuration requires several input capacitors to fulfill the multi-bit function [6]. This approach increases the input capacitance of the pipelined ADC. A large input capacitance stresses the driving circuit of the ADC, which usually is a VGA in digital receiver applications. In some solutions, the full-scale input range of the ADC is reduced and so is the achievable dynamic range [82]. The time constant matching is another concern in a pipelined ADC without a front-end S/H circuit. Although the aperture error due to the time constant mismatch can be treated as a comparator offset and removed by the digital error correction logic, due to the high gain of the multi-bit first stage, it is easy for the aperture error to saturate the S/H circuit output swing. This sets a limit on the highest working frequency of the pipelined ADC without a front-end S/H circuit. Therefore, a dedicated front-end S/H is necessary for this consideration.

This chapter proposes a mixed-mode S/H circuit that reduces the requirements of op amp DC gain, bandwidth, slew rate and output swing. The relaxation on performance requirements enables the use of single-stage cascode op amp in low-voltage environment without degrading the system performances. The mixed-mode sampling technique also reduces the capacitor matching requirement in pipelined ADCs. The reduced requirements are accomplished through a built-in comparator in the S/H circuit. The aperture errors are minimized by time constant matching and digital error correction logic.

5.2 The Op Amp and Capacitors in the S/H Circuit

The performances of a S/H circuit are usually determined by an op amp in a switched-capacitor implementation. In a S/H circuit, the op amp must have enough DC gain to guarantee the accuracy requirement; and a fast slew rate and large bandwidth to meet the speed demand. The op amp performance also has an effect on the linearity of the S/H circuit, and consequently affects the overall ADC dynamic performance. Beyond these, in order to achieve a desirable SNR, a large signal swing is required at the output of op amp even in the low-voltage environment.

The schematic of a conventional switched-capacitor S/H circuit is shown in Figure 5.1. If the mismatch between C_S and C_F is ΔC as shown in Fig. 5.1, the S/H output can be expressed as

$$V_{out} = \left(1 - \frac{1}{\beta \cdot A_0} - \frac{\Delta C}{C}\right) \cdot V_{in} \quad (5.1)$$

$\beta = C/(2C + \Delta C + C_{in})$ denotes the feedback factor in the holding mode and A_0 is the op amp DC gain. C_{in} is the input capacitance of the op amp. Equation (5.1) shows that the S/H output has a error of $[(\Delta C/C) + (1/\beta \cdot A_0)] \cdot V_{in}$ due to the finite op amp DC gain and

Figure 5.1: SC implementation of sample-and-hold circuit.

capacitor mismatch. This error is signal dependent and is aggravated as the input signal V_{in} increases.

If this S/H circuit is used in an N -bit ADC, for a full-scale step input, the error due to the finite op amp DC gain and capacitor mismatch must be less than half of the LSB in order to avoid introducing any error to the following pipelined stages. Thus the op amp gain and capacitor matching requirements have to satisfy the following condition:

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C}\right) < \frac{1}{2^{N+1}} \quad (5.2)$$

Although a S/H gain error can be tolerated in some applications, the gain error drift must be minimized, which requires a high op amp DC gain across temperature and process corners.

The speed of an S/H circuit is determined by the settling time of the op amp that can be categorized into the nonlinear slewing time and the quasi-linear settling time as shown in Figure 4.14. The requirement of the op amp unity gain bandwidth, ω_u , in an N -bit S/H circuit ignoring the slew time is given by

$$\omega_u > \frac{2 \cdot (N + 1) \cdot f_s \cdot \ln 2}{\beta} \quad (5.3)$$

where f_s is the ADC sampling frequency and β is the feedback factor. The op amp unity gain bandwidth is directly related to the capacitive load. The larger the load capacitance, the higher the power consumption is required to achieve a given bandwidth.

In practice, the op amp bandwidth need to be larger than the value given by equation (5.3) to take into account the slewing time and nonoverlapping clock phases. For speed consideration, the slewing time should be minimized, which requires a high op amp slew

rate. The op amp with a high slew rate settles to the final value in the linear settling phase. Therefore even if the op amp is not fully settled at the end of the hold mode, there is only a linear error and an improvement of the dynamic performance can be expected. Since the slew rate of the op amp is determined by the output swing, the capacitive load, and the sampling frequency, a reduced output swing and smaller capacitive load can improve the S/H speed and accuracy.

5.3 Variation of Op Amp DC Gain with Respect to Output Swing

The op amp DC gain depends on input and output signal swing, which can be illustrated by the differential amplifier shown in Figure 5.2. In this amplifier, the current difference $\Delta I = I^+ - I^-$ can be expressed as [77]

$$\begin{aligned}
 \Delta I &= \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} V_{in} \sqrt{\frac{I}{\mu_n C_{ox} \frac{W_1}{L_1}} - V_{in}^2} \\
 &= \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} V_{in} \sqrt{4(V_{GS} - V_{TH})_1^2 - V_{in}^2} \\
 &= \mu_n C_{ox} \frac{W_1}{L_1} (V_{GS} - V_{TH})_1 V_{in} \\
 &\quad \times \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})_1^2}} \\
 &= g_{m1} V_{in} \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})_1^2}} \tag{5.4}
 \end{aligned}$$

where L_1 , W_1 and g_{m1} are the channel length, width and transconductance of M_1 , respectively, provided the M_1 and M_2 have the same size. The output impedance of the amplifier is $r_{o1} || r_{o3}$. Assume $r_{o1} = r_{o3}$ and M_3 and M_4 have the same size, the gain of the amplifier

equals to

$$\begin{aligned}
 A &= \Delta I \frac{r_{o1}}{2} / V_{in} \\
 &= g_m \frac{r_{o1}}{2} \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})_1^2}} \\
 &\approx A_0 \left(1 - \frac{V_{in}^2}{8V_{eff1}^2}\right)
 \end{aligned} \tag{5.5}$$

where $A_0 = g_m r_{o1}/2$ is the amplifier DC gain when the output is zero. $V_{eff1} = (V_{GS} - V_{TH})_1$ is the input transistor overdrive voltage.

Figure 5.2: A differential amplifier.

The discussion so far about the dependence of the op amp DC gain on the input and output signals has been based on the assumption that the output impedance r_o of the MOS transistor in the saturation region is constant during the signal swing. This is true for long channel device working in a high voltage environment. However, for a short channel device, r_o varies significantly with the drain-source voltage V_{DS} . In the saturation region, this dependence can be approximated as

$$r_o = \frac{2L}{1 - \frac{\Delta L}{L}} \frac{1}{I} \sqrt{\frac{qN_B}{2\epsilon_{si}} (V_{DS} - V_{dsat})} \quad (5.6)$$

The variation of r_o gives rise to nonlinearity in an op amp. The amount of nonlinearity is heavily depends on how much the output signal swings, i.e., how much the V_{DS} changes. In addition, the transistor tranconductance g_m also varies with V_{DS} , which further exacerbates the op amp nonlinearity since the voltage gain is determined by $g_m \cdot r_o$. This phenomenon becomes significant in cascoded op amps as V_{DS} of the cascoded devices changes greatly during operation. The voltage gain of an op amp varies with the output voltage is illustrated in Figure 5.5.

Figure 5.3: g_m variation with V_{DS} .

Because the voltage gain varies during operation, the gain requirement in equation (5.2) should be the gain when a largest output swing was applied. At this condition, the required

Figure 5.4: r_o variation with V_{DS} .

Figure 5.5: Op amp DC gain variation with output.

zero output op amp DC gain is usually much larger than the value given by equation (5.2).

5.4 S/H Nonlinearity Due to Op Amp Gain Variation

The nonlinear op amp DC gain is an important source of nonlinearity error in a S/H circuit.

This harmonic distortion can be analyzed via charge conservation in a switched-capacitor circuit. Replace A_0 in (5.1) with A in (5.5) and ignore the capacitor mismatch, the transfer function of the S/H circuit in Figure 5.1 can be rewritten as

$$\begin{aligned} V_{out} &\approx V_{in} \frac{C_S}{C_F} \left(1 - \frac{1}{\beta \cdot A}\right) \\ &\approx V_{in} \frac{C_S}{C_F} \left(1 - \frac{1}{\beta \cdot A_0} \cdot \frac{1}{1 - \frac{V'^2}{8V_{eff1}^2}}\right) \end{aligned} \quad (5.7)$$

where V' is the voltage at the op amp input, which can be approximated as

$$V' \approx -\frac{V_{out}}{A_0} \approx -\frac{V_{in} \cdot \frac{C_S}{C_F}}{A_0} \quad (5.8)$$

Therefore

$$\begin{aligned} V_{out} &\approx V_{in} \frac{C_S}{C_F} \left[1 - \frac{1}{\beta \cdot A_0} \cdot \frac{1}{1 + \frac{V_{in}^2 \cdot (C_S/C_F)^2}{A_0^2}}\right] \\ &\approx V_{in} \frac{C_S}{C_F} \left[1 - \frac{1}{\beta \cdot A_0} \cdot \left(1 - \frac{V_{in}^2 \cdot (C_S/C_F)^2}{A_0^2}\right)\right] \\ &= V_{in} \frac{C_S}{C_F} \left(1 - \frac{1}{\beta \cdot A_0}\right) + \frac{(C_S + C_F)^3}{\beta \cdot A_0^3} V_{in}^3 \end{aligned} \quad (5.9)$$

Equation (5.9) indicates the nonlinearity of the S/H circuit with respect to the input signal. The above analysis doesn't take into account the nonlinearity due to device transconductance g_m and output impedance r_o variations with the output swing, which contributes greatly to the overall nonlinearity but is much more complex to be derived in a close form.

5.5 Op Amp Architectures Comparison

In a pipelined ADC, the op amp is the most crucial block which determines the overall ADC performance. As discussed above, the op amp open-loop DC gain determines the ADC accuracy. The op amp slew rate and bandwidth have a large impact on the ADC speed. To maximize the signal-to-noise ratio, the op amp requires a large output swing. This section summarizes op amp architectures and compares their performance.

5.5.1 Telescopic Op Amp

A telescopic op amp is shown in Figure 5.6. The cascode devices in the telescopic op amp dramatically increase the output impedance, giving the telescopic op amp the highest gain for the single-stage implementation [77]. The DC gain of the op amp in Figure 5.6 can be expressed as

$$A_0 \approx g_{m1} \cdot [(g_{m3} \cdot r_{o3} \cdot r_{o1}) || (g_{m5} \cdot r_{o5} \cdot r_{o7})] \quad (5.10)$$

where g_m is transistor transconductance and r_o is transistor output impedance. The slew rate of the telescopic op amp is given by

$$SR = \frac{I_{M9}}{C_L} \quad (5.11)$$

where I_{M9} is the quiescent bias current in transistor M_9 and C_L is the capacitive load.

The dominant pole of the telescopic op amp is at the op amp output. The unity gain bandwidth of the op amp is given by

$$\omega_u \approx \frac{g_{m1}}{C_L} \quad (5.12)$$

Figure 5.6: Telescopic op amp.

The first non-dominant pole is located at the source of the cascode transistor M_3 , and is given by

$$\omega_n \approx \frac{1}{\left(\frac{1}{g_{m3}} + \frac{g_{m5}r_{o5}r_{o7}}{g_{m3}r_{o3}}\right)(C_{gs3} + C_{gd1})} \quad (5.13)$$

where C_{gs3} is the gate-source parasitic capacitance of transistor M_3 , and C_{gd1} is the gate-drain parasitic capacitance of transistor M_1 .

The input referred noise of the telescopic op amp is given by

$$\overline{V_n^2} \approx \frac{16}{3}kT\left(\frac{1}{g_{m1,2}} + \frac{g_{m7,8}}{g_{m1,2}^2}\right) \quad (5.14)$$

The maximum possible output swing of the telescopic op amp is $V_{DD} - 5V_{dsat}$. The limited output swing is the most prominent drawback of the telescopic op amp. However, the telescopic op amp is usually fast due to the high slew rate and high non-dominant pole frequency. The noise of the telescopic op amp is the lowest among the popular op amp

architectures. For a given load and speed, the telescopic op amp consumes less power than other architectures do.

5.5.2 Folded Cascode Op Amp

The folded cascode op amp, shown in Figure 5.7, has a larger output swing than the telescopic op amp. The output swing of the folded cascode is $V_{DD} - 4V_{dsat}$. The DC gain of the op amp in Figure 5.7 can be expressed as [77]

$$A_0 \approx g_{m1} \cdot \{ [g_{m5} \cdot r_{o5} \cdot (r_{o1} || r_{o3})] || [g_{m7} \cdot r_{o7} \cdot r_{o9}] \} \quad (5.15)$$

Due to the parallel output impedances of M_1 and M_3 , the folded cascode op amp has a lower gain than telescopic op amp.

Figure 5.7: Folded cascod op amp.

The slew rate of the folded cascode op amp is given by

$$SR = \frac{I_{M11}}{C_L} \quad (5.16)$$

where I_{M11} is the quiescent bias current in transistor M_{11} and C_L is the capacitive load.

The dominant pole of the folded cascode op amp is at the op amp output. The unity-gain bandwidth of the op amp is given by

$$\omega_u \approx \frac{g_{m1}}{C_L} \quad (5.17)$$

The first non-dominant pole is located at the source of the cascode transistor M_5 , and is given by

$$\omega_n \approx \frac{1}{\left(\frac{1}{g_{m5}} + \frac{g_{m7}r_{o7}r_{o9}}{g_{m5}r_{o5}}\right)(C_{gs5} + C_{gd3} + C_{gd1})} \quad (5.18)$$

Compare the equations 5.13 and 5.18, the non-dominant pole frequency of folded cascode op amp is lower than that of telescopic op amp due to the extra load of C_{gd3} . Therefore the speed of folded cascode op amp is usually slower than telescopic op amp.

The input referred noise of the folded cascode op amp is given by

$$\overline{V_n^2} \approx \frac{16}{3}kT\left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}^2} + \frac{g_{m9,10}}{g_{m1,2}^2}\right) \quad (5.19)$$

The input referred noise of the folded cascode op amp is larger than telescopic op amp due to the contribution of transistors M_3 and M_4 .

5.5.3 Two-stage Op Amp

Although employed cascode transistors, the gain of telescopic and folded cascode op amps is not enough in some applications. If higher gain and larger output swing are required, the

two-stage op amp shown in Figure 5.8 can be used. This two-stage op amp has a high gain telescopic first stage and a common-source amplifier as the second stage. Its DC gain is given by [77]

$$A_0 \approx g_{m1} \cdot [(g_{m3} \cdot r_{o3} \cdot r_{o1}) || (g_{m5} \cdot r_{o5} \cdot r_{o7})] \cdot g_{m9} \cdot (r_{o9} || r_{o11}) \quad (5.20)$$

The output swing of the two-stage op amp is $V_{DD} - 2V_{dsat}$, which is much larger than that of telescopic and folded cascode op amp.

Figure 5.8: Two-stage op amp.

For stability reason, a compensation capacitor C_C is used to move the dominant pole closer to original. The unity gain bandwidth of this two-stage op amp is given by

$$\omega_n \approx \frac{g_{m1}}{C_C} \quad (5.21)$$

Usually, the second stage has a lower gain compared to the first stage. Therefore the

non-dominant pole is located at the op amp output, can be expressed as

$$\omega_u \approx \frac{g_{m9}}{C_C + C_L} \quad (5.22)$$

It is clear that the non-dominant pole frequency of the two-stage op amp is much lower than that of single-stage op amp due to the compensation capacitor. This makes two-stage op amp not attractive in high-speed applications. In addition, the input referred noise of the two-stage op amp can be express as

$$\overline{V_n^2} \approx \frac{16}{3}kT\left(\frac{1}{g_{m1,2}} + \frac{g_{m7,8}}{g_{m1,2}^2} + \frac{g_{m9} + g_{m11}}{A_{S1}^2}\right) \quad (5.23)$$

where A_{S1} is the first stage gain at a certain frequency.

5.5.4 Selection of op amp for the S/H circuit

In high-speed low-power applications, it is always desirable to use the single-stage op amp architecture with the minimum transistor size whenever possible. This is due to the high-speed, low-noise, low-power and stability characteristics of single-stage op amp. In practice, one of the challenges is that the DC gain of the one-stage op amp is limited unless it involves larger transistor size to increase the output impedance. However, a larger transistor size transfers into a lower speed because of the parasitic capacitance load. Another problem associated with single-stage op amp is the limited output signal swing due to cascode operation, which leads to a limitation on the SNR and linearity. These problems become more and more significant as the supply voltage and device size scale down.

From the above discussions, the telescopic op amp will be selected for the design as it has the fastest speed, lowest power consumption and lowest noise among the op amp

architectures. The prominent drawbacks of the telescopic op amp are the limited output swing and insufficient DC gain in low-voltage environment. The following proposal is made to remedy these short-comings.

5.6 The Proposed Mixed-Mode S/H Circuit

Previous discussions show that the signal swing has a significant influence on the whole ADC performance. The larger the signal swing, the larger the gain error for a given op amp gain and capacitor mismatching. The variation of the op amp DC gain with respect to the output swing also introduces nonlinearity in a S/H circuit. These errors become severe as the headroom left for cascode device operation decreases in low voltage environment. Although the single-stage op amp is preferred in high speed applications, the error and nonlinearity often deprive its practicability in low voltage environment.

Figure 5.9: The proposed mixed-mode S/H circuit.

In order to reduce the required signal swing, we proposed a mixed-mode S/H circuit as

shown in Figure 5.9, in which $C_S = C + \Delta C$ and $C_F = C$. ΔC denotes the capacitor mismatch. One comparator was added to the conventional S/H circuit. The S/H operation is controlled by two non-overlapped clock phases, namely sampling phase ϕ_1 and holding phase ϕ_2 . ϕ_{1a} is a copy of ϕ_1 but with an earlier falling edge. During the sampling mode, switches controlled by ϕ_1 and ϕ_{1a} are on, the sampling capacitor C_S is charged to $V_{in} - V_{os}$ with the aid of the virtual ground formed by the op amp in unity-gain configuration. V_{os} is the offset voltage of op amp. Meanwhile, the feedback capacitor C_F is charged to V_{os} . The sampling mode ends at the falling edge of ϕ_{1a} . At the same clock edge, the comparator quantizes the input signal and generates the digital output D_{OUT} . Subsequently, ϕ_1 turns off the input switches and ϕ_2 connects C_F to the op amp output. The bottom plate of C_S was connected to either $+V_{ref}/2$ or $-V_{ref}/2$, determined by the value of D_{OUT} . The S/H circuit is in the holding mode and the op amp offset was eliminated by the correlated double sampling [83]. As a result, for $C_S = C_F$, the transfer function of the S/H circuit is given as:

$$V_{out} = (1 - \frac{1}{\beta \cdot A_0} - \frac{\Delta C}{C})[V_{in} + (-1)^{D_{out}} \times V_{ref}/2] \quad (5.24)$$

where

$$D_{OUT} = \begin{cases} 1 & \text{for } V_{in} \geq 0 \\ 0 & \text{for } V_{in} < 0 \end{cases} \quad (5.25)$$

$$\beta = C/(2C + \Delta C + C_{in}) \quad (5.26)$$

The relationship between V_{in} , D_i , and the connection of C_S to the reference voltage is shown in Table 5.1.

The sampled data is represented both in analog and digital forms. The transfer curve of

Table 5.1: Relation between V_{in} , D_i , and connection of C_S in mixed-mode S/H.

V_{in}	D_i	Connection of C_S
< 0	-1	$-V_{ref}$
≥ 0	$+1$	$+V_{ref}$

this mixed-mode S/H circuit is illustrated in Figure 5.10. Also shown is the one bit digital output send to the digital error correction logic. The dashed line shows the transfer curve of the conventional S/H circuit in Figure 5.1. As expected, the output swing of the proposed S/H circuit is reduced and doesn't exceed the range from $-3V_{ref}/4$ to $+3V_{ref}/4$ as long as the comparator offset error is smaller than $\pm V_{ref}/4$. The reduced analog signal swing do neither degrade the SNR nor stress the following pipelined stage since now the information is stored both in analog and digital forms and the full scale range is maintained.

Figure 5.10: The transfer curve of S/H circuit.

Although the full scale input is unchanged, the effective input signal to the op amp is reduced by $V_{ref}/2$ as can be seen in equation (5.24). Therefore, the maximum error introduced by finite op amp DC gain and capacitor mismatch is $[(\Delta C/C) + (1/\beta \cdot A_0)] \cdot FS/2$ in the mixed-mode S/H circuit. If this S/H circuit is used in an N-bit ADC, for the error to be less than LSB/2, the op amp gain and capacitor matching requirements become

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C}\right) < \frac{1}{2^N} \quad (5.27)$$

which is 6 dB lower than the requirement for the conventional S/H circuit as expressed in equation (5.2). Although this configuration increases the gain error when the input is in the vicinity of zero as shown in Figure 5.10, this error is still within the range of LSB/2 of the full scale. Due to the reduced signal swing, small capacitance of C_S and C_F can be used. In addition, since the output swing is reduced, the op amp DC gain is more stable, therefore an improvement of the S/H circuit linearity is expected.

Since the output swing is reduced, the mixed-mode S/H technique also relaxed the op amp bandwidth requirement. Using the same derivation in Chapter 4, the op amp unity gain bandwidth requirement in the mixed-mode S/H for an N-bit ADC is

$$\omega_u > \frac{2 \cdot N \cdot f_s \cdot \ln 2}{\beta} \quad (5.28)$$

The op amp and capacitor matching requirements of the conventional S/H circuit and the mixed-mode S/H circuit are summarized in Table 5.2

The analog output of the S/H circuit will be processed by the following pipelined ADC stages. The 1-bit digit output will be combined with ADC outputs to generate the final output. Figure 5.11 shows an example of the mixed-mode S/H used in a 3-bit pipelined

Table 5.2: Comparison of requirements on gain, bandwidth and capacitor matching

	Min. op amp gain	Min. op amp bandwidth	Max. capacitor mismatching
Conventional S/H	$A > \frac{1}{\beta} \cdot 2^{N+1}$	$\omega_u > \frac{1}{\beta} \cdot 2 \cdot (N+1) \cdot f_s \cdot \ln 2$	$\Delta C < \frac{1}{2^{N+1}}$
Mixed-mode S/H	$A > \frac{1}{\beta} \cdot 2^N$	$\omega_u > \frac{1}{\beta} \cdot 2 \cdot N \cdot f_s \cdot \ln 2$	$\Delta C < \frac{1}{2^N}$

ADC. The S/H circuit has a 1-bit output F_1 . The final ADC digital output $D_2D_1D_0$ is the combination of the S/H output F_1 and pipeline stages' output $F_2F_3F_4F_5$.

Figure 5.11: The proposed S/H circuit used in a 3-bit pipelined ADC.

Due to the additional comparator, in the sampling mode there are two signal paths in this S/H circuit as shown in Figure 5.12. One consists of the sampling switch, the sampling capacitor C_S and the op amp. The other includes only the comparator. Because of the time constant difference between these two paths, there exists a voltage error, i.e. the sampling capacitor C_S and the comparator see different input signals. The voltage difference is known as aperture error and will be increased as a function of input frequency. For an input signal of $V_{in} = V_{ref} \sin(2\pi f_{in}t)$, the maximum slope of this signal can be presented as

$$\left. \frac{dV_{in}}{dt} \right|_{max} = 2\pi f_{in} V_{ref} \quad (5.29)$$

Figure 5.12: The two signal paths in the sampling mode.

Assuming the unmatched time constant between the two signal paths is $\Delta\tau$, the aperture error voltage, V_e , can be calculated as

$$V_e = 2\pi f_{in} V_{ref} \Delta\tau \quad (5.30)$$

Despite the existence of the aperture error, particularly at high frequency input, it is possible to minimize this error by matching the two signal paths in terms of topology and time constant. Instead of connecting the comparator directly to the input signal, it is connected to the output of the sampling switch (shown by the dashed line in Figure 5.12), i.e., the two paths see the same delay caused by the sampling switch. In addition, the op amp and comparator both use the falling edge of ϕ_{1a} to sample and quantize the input signal.

Moreover, based on the characteristic of pipelined ADCs, the aperture error due to time constant mismatch can be treated as the comparator offset error which can be eliminated by the digital error correction.

5.7 Building Blocks

5.7.1 Op Amp

Because the mixed-mode sampling technique reduces the signal swing and relaxes the op amp gain and slew-rate requirements, a gain-boosted single-stage telescopic op amp was used in the proposed S/H circuit as shown in Figure 5.13. Transistors $M_{B1} \sim M_{B7}$ provide the biasing voltages for the op amp. Transistors $M_1 \sim M_9$ form the main telescopic op amp. To improve the gain, transistors M_{10} , M_{12} and M_{11} , M_{13} form two common-source amplifiers and negative feedback loops that make the source voltage of the common gate transistor M_3 and M_4 less sensitive to the output signal. The gain boosting circuit increases the output impedance without adding more cascode devices. The concept of the gain boosting is illustrated in Figure 5.14. A_m is the gain of the main telescopic amplifier. A_g is the gain of the boosting amplifier. A_0 is the final gain of the gain boosted op amp. In this implementation, A_m and A_g can be respectively expressed as

$$A_m = g_{m1} \{ [g_{m3} r_{o3} r_{o1}] || (g_{m5} r_{o5} r_{o7}) \} \quad (5.31)$$

$$A_g = g_{m10} (r_{o10} || r_{o12}) \quad (5.32)$$

The gain boosting is only applied to the NMOS cascode transistors. The output impedances of the PMOS active loads are increased by increasing the channel length of M_7 and M_8 since the size of these two devices have less effect on the op amp frequency response. The overall DC gain of the gain-boosted telescopic amplifier can be shown as

$$A_0 = g_{m1} \{ [g_{m3} r_{o3} r_{o1} g_{m10} (r_{o10} || r_{o12})] || (g_{m5} r_{o5} r_{o7}) \} \quad (5.33)$$

Figure 5.13: The telescopic op amp with gain boosting.

Figure 5.14: Illustration of the gain boosting.

It is clearly shown in equation (5.33) that the op amp DC gain depends on the transconductances of transistors M_1 M_3 M_5 and output impedances of M_1 M_3 M_5 M_7 . In short channel devices, both g_m and r_o increase with V_{DS} before the device reaches the drain-induced barrier lowering (DIBL) level [77]. In the mixed-mode S/H circuit, since the op amp output swing was reduced, the gate voltage of NOMS M_3 and M_4 can be made high enough to increase the V_{DS} of M_1 and M_2 . Meanwhile, the gate voltage of POMS M_5 and M_6 can also be made low enough to increase the V_{DS} of M_7 and M_8 . The increasing of the V_{DS} leads to a higher DC gain.

Figure 5.15: The pole relations of gain-boosting amplifier.

For stability and settling considerations, the gain-boosting circuit doesn't have to be very fast and its unity gain frequency should satisfy:

$$\beta\omega_{um} < \omega_{ug} < \omega_{np} \quad (5.34)$$

where β is the close-loop feedback factor, ω_{um} is the unity-gain bandwidth of the main amplifier, ω_{ug} is the unity-gain bandwidth of the gain-boosting amplifier and ω_{np} is the

second-pole frequency of the main amplifier [84]. Special attention should be paid to the position of the pole-zero doublet introduced by the gain-boosting amplifier. Although this does not deteriorate the op amp stability, this doublet does affect the op amp closed-loop settling time [85].

Since the ADC uses a fully-differential operation to maximize signal-to-noise ratio, a common-mode feedback loop is required for the op amp. The switched-capacitor common-mode feedback circuit used for the S/H and pipeline stages described in the next chapter is shown in Figure 5.16. During phase ϕ_1 , the desired common-mode voltage is stored in capacitors C_1 and C_2 . During phase ϕ_2 , the desired common-mode voltage is compared to the actual value stored in capacitors C_3 and C_4 , generating the bias voltage V_{CMFB} to control transistors M_7 and M_8 in Figure 5.13. By control the currents through M_7 and M_8 , the common-mode voltage is set to desired value during phase ϕ_2 .

Figure 5.16: The common-mode feedback circuit.

The sizes of the devices in the op amp and the biasing current are listed in Table 5.3. The simulated DC gain of the designed op amp is 64 dB while the phase margin is 74 degree. The unity gain bandwidth for the 600-fF capacitive load is 1.1-GHz. The simulated power consumption is 3.4-mW with 1.8-V power supply. Figure 5.18 shows the dependence of

Table 5.3: Device size and biasing current of the S/H op amp

Device	Width (μm)	Length (μm)	Current (μA)
M_1, M_2	64	0.2	640
M_3, M_4	64	0.2	640
M_5, M_6	64	0.2	640
M_7, M_8	240	1.0	640
M_9	192	0.3	1280
M_{10}, M_{11}	24	0.6	160
M_{12}, M_{13}	60	1.0	160
M_{B1}, M_{B2}, M_{B3}	24	0.3	160
M_{B4}, M_{B5}	16	0.2	160
M_{B6}, M_{B7}	60	1.0	160

DC gain on output swing simulated with slow MOS model. The simulation with slow model gives the lowest available output swing which is the worst-case for accuracy and linearity.

5.7.2 Comparator

The comparator used in the mixed-mode S/H circuit is shown in Figure 5.19. The differential pair M_1 and M_2 amplify the input signal and transistors $M_4 \sim M_7$ form a regeneration latch. When ϕ_{1a} is high, V_{out+} and V_{out-} are reset to V_{DD} via M_8 and M_9 . When ϕ_{1a} goes low, the differential pair M_1 and M_2 compare the input V_{in+} and V_{in-} and generate

Figure 5.17: Gain and phase plot of the S/H op amp.

Figure 5.18: Gain versus output swing plot of the S/H op amp.

voltage difference at the drain of transistor M_4 and M_5 . This voltage difference is then amplified by the positive feedback of the latch therefore V_{out+} and V_{out-} go to V_{DD} or ground according to the input voltages.

Figure 5.19: The comparator used in the S/H circuit.

The offset of this comparator can be expressed as

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2} \left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R} \right) \quad (5.35)$$

where $V_{TH1,2}$ is the threshold voltage mismatch of transistors M_1 and M_2 . $\Delta S_{1,2}$ is the physical dimension mismatch between M_1 and M_2 . ΔR is the load resistance mismatch, which is contributed by transistors $M_4 \sim M_7$. The offset voltage in this comparator is dominated by the mismatch between transistor M_1 and M_2 . Mismatches caused by other transistors are reduced by the gain of M_1 and M_2 . The offset can be reduced by decreasing

$(V_{GS} - V_{TH})_{1,2}$, which is controlled by the tail current of the differential pair. In this design, the gate of transistor M_3 is connected to V_{BIAS} instead of ϕ_1 to reduce the current in regeneration phase. The gate of M_3 is connected to ground via M_{10} in the reset phase.

The sizes of the devices in the comparator are listed in Table 5.4.

Table 5.4: Device size of the S/H comparator

Device	Width (μm)	Length (μm)
M_1, M_2	6	0.3
M_3	6	0.3
M_4, M_5	1	0.18
M_6, M_7	4	0.18
M_8, M_9	1	0.18
M_{10}	1	0.18

With manually introduced 20% device dimension mismatch, this comparator has an offset voltage less than 7.5-mV in worst-case simulation as shown in Figure 5.20. The curves listed in Figure 5.20 from the top to bottom is the comparator input voltage V_{in} , comparator output V_{out-} and V_{out+} , and the clock CLK . It can be observed that with 20% device dimension mismatch, V_{out-} and V_{out+} change their stage when $V_{in} > 7.5\text{mV}$. This comparator achieves less than 300-ps regeneration time for a 1-mV differential input signal in the worst-case corner simulation. The power consumption is 0.4-mW at 1.8-V power supply. The offset of the comparator without switching bias is shown in Figure 5.21 which is 22.6-mV with 20% device mismatch. The comparator offset error is significantly reduced

by the switching bias.

Figure 5.20: Offset error simulation of the comparator in proposed S/H circuit.

5.7.3 Bootstrapped MOS switch

Besides the op amp, the input sampling switches also introduce nonlinearity due to the signal-dependent on-resistance. In order to minimize the errors introduced by the op amp, bootstrapped MOS switches are used in the proposed S/H circuit. Figure 5.22 illustrates the bootstrapped switch circuit [86]. The bootstrapped voltage is realized with the capacitor C_1 , which is pre-charged to V_{DD} during the switch off period. At the switch-on period, C_1 is connected between the gate and source terminals of the switch M_S via the switches M_1 and M_4 . As a result, a constant gate-source voltage of V_{DD} applies to M_S , making its on-resistance independent of input signal. Except the transistors M_1 and M_S , all the body

Figure 5.21: Offset voltage simulation of the comparator without switching bias.

of NMOS are connected to ground. M_1 and M_S are implemented in deep N-well, with their bodies connect to the source of M_1 . All the body of PMOS are connected to V_{DD} except M_4 , whose body connects to its source.

The sizes of the devices in the bootstrapped switch are listed in Table 5.5.

5.8 Simulation Results

The proposed mixed-mode S/H circuit has been designed using a 0.18- μm CMOS process and simulated at worst-case corners with manually introduced 7-mV comparator offset. The simulation is performed at 200-MHz sampling frequency and 1.8-V supply. Under these conditions, the S/H circuit consumes 4-mW.

Figure 5.22: The bootstrapped switch.

Table 5.5: Device size of the bootstrapped MOS switch

Device	Width (μm)	Length (μm)
M_S	8	0.18
M_1	1	0.18
M_2	1	0.18
M_3	1	0.18
M_4	4	0.18
M_5, M_6	1	0.18
M_7	1	0.18
M_8, M_9	1	0.18
C_1	440-fF	

Figure 5.23 illustrates the digital and analog outputs of the mixed-mode S/H circuit at 200MSample/s with a $1-V_{PP}$ input sine-wave of 190-MHz (sub-sampling). It can be seen

that the output swing is less than 540-mV with the aperture error and 7-mV comparator offset presented.

Plotting in Figure 5.24 is the simulated SNDR, SFDR and THD as a function of the input signal frequency while the S/H samples at 200-MHz. The mixed-mode S/H circuit exhibits a THD lower than -60 dB and SNDR larger than 59 dB, i.e. better than 9-bit accuracy. The SNDR is larger than the theoretical analysis from equation (5.28) because of the linear settling behavior of op amp. Figure 5.25 shows the FFT plot of a 90-MHz input with 200-MSample/s, where about -61.2 dB THD and 59.5 dB SNDR are observed.

Table 5.6 summaries the simulated performance of the mixed-mode S/H circuit and compared it with the conventional S/H circuit in Figure 5.1. Both the gain error and non-linearity of the proposed mixed-mode S/H circuit are less than that of the conventional S/H circuit using the same op amp and switches.

5.9 Conclusion

In this chapter, the design of a high-speed sample-and-hold circuit has been demonstrated by simulation results at 200-MHz sampling. The mixed-mode sampling technique reduces the signal swings in a pipelined ADC, therefore the op amp gain, bandwidth, slew rate and capacitor matching requirements are relaxed. The proposed S/H circuits exhibits better linearity and lower power characteristic due to the mixed-mode sampling technique. This technique enables the use of single-state cascode amplifier in the low-voltage environment without degrading the dynamic performances and linearity.

Figure 5.23: Output waveform at 200-MHz sampling rate with 190-MHz input.

Figure 5.24: Dynamic performance of the proposed S/H circuit at 200-MS/s.

Figure 5.25: Output spectrum with 200-MHz sampling and 90-MHz input of the S/H.

Table 5.6: S/H circuit performance summary and comparison

Design	Mixed-Mode S/H	Conventional S/H
Technology	0.18- μ m CMOS	0.18- μ m CMOS
Power Supply	1.8-V	1.8-V
Sampling Frequency	200-MHz	200-MHz
SFDR	62.5 dB @ 90-MHz input	55.2 dB @ 90-MHz input
THD	-61.2 dB @ 90-MHz input	-53.2 dB @ 90-MHz input
SNDR	59.5 dB @ 90-MHz input	49.4 dB @ 90-MHz input
Power Consumption	4-mW	3.6-mW

Chapter 6

Design of an 8-Bit 200MSample/s

Pipelined ADC

The mixed-mode sample-and-hold technique proposed in Chapter 5 not only relaxes the op amp and capacitor matching requirements in the S/H circuit, but also in the pipelined stages. Base on mixed-mode sample-and-hold technique, we design and implement an 8-bit 200MSample/s pipelined ADC with dynamic performance of 55 dB SFDR and 45 dB SNDR. This chapter describes the building blocks design of the prototype ADC.

6.1 ADC Architecture

The proposed pipelined ADC with a mixed-mode S/H circuit at the front-end is shown in Figure 6.1. The mixed-mode S/H circuit reduces the input signal swing and has 1-bit digital output. The S/H circuit is followed by six modified 1.5-bit stage. The S/H reduces the input

signal swing and maintain it within the range of $-3V_{ref}/4$ to $+3V_{ref}/4$. Hence the input of the 1.5-bit stage is limited within the same range. Therefore, all the pipelined stage outputs don't need the full-scale swing and the op amp and capacitor matching requirements are relaxed. The last stage is implemented with a 2-bit flash ADC. The digital outputs of the pipeline stages and the 1-bit output from the S/H circuit are sent to the digital error correction logic to remove the comparator offset errors and generate the 8-bit digital output. Since the prototype ADC is going to be tested on wafer, to reduce the number of probing pins, a decimation circuit decimates the output data by eight, and the 8-bit converted data are output through a serialization circuit. The biasing block supplies the biasing currents to the S/H and pipeline stages. The non-overlapping clocks are generated by the clock generator.

Figure 6.1: The proposed 8-bit pipelined ADC.

6.1.1 Sample-and-hold

The front-end S/H is based in the mixed-mode sampling technique described in Chapter 5. Based on the equation (4.28), for an 8-bit ADC, the capacitor mismatch in a conventional S/H circuit should be less than 0.2%. According to the design guide of the foundry, the Chartered Semiconductor Manufacturing, to satisfy 3-sigma 0.2% mismatching for MIM capacitors, the capacitor size must be larger than 400-fF. Due to the mixed-mode S/H circuit reduces the signal swing by half, the capacitors C_S and C_F have a small size. In the S/H design, MIM capacitors of 200-fF are chosen, which have 0.4% 3-sigma percentage mismatching.

6.1.2 The pipelined stages

The first stage of the pipeline has the most stringent performance requirement. The simplified schematic of the conventional MDAC in a 1.5-bit stage is shown in Figure 6.2. During the clock phase ϕ_1 , the input signal is sampled in capacitors C_F and C_S . During the clock phase ϕ_2 , capacitor C_F is connected between the input and output of the op amp. Capacitor C_S is connected to $+V_{ref}$, 0, or $-V_{ref}$ according to the sub-ADC output in this stage. In an N-bit ADC, for the output error to be less than half of the LSB of the remaining stage's resolution, the op amp gain and capacitor matching requirement is

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C}\right) < \frac{1}{2^N} \quad (6.1)$$

And the op amp bandwidth requirement is

$$\omega_u > \frac{2 \cdot N \cdot f_s \cdot \ln 2}{\beta} \quad (6.2)$$

Figure 6.2: The MDAC in a 1.5-bit stage.

Similar to the S/H circuit discussed in Chapter 5, the signal swing also has significant effects on the performance of the first stage as shown in (6.1) and (6.2). Since the mixed-mode S/H circuit reduces the signal swing, the op amp and capacitor matching requirements are also relaxed in the pipeline stages based on the same analysis.

In the mixed-mode S/H circuit, the sampling capacitor C_S is connected to either $+V_{ref}/2$ or $-V_{ref}/2$ during the holding mode. Although two additional reference voltages, $+V_{ref}$ and $-V_{ref}$ can be used to implement conventional 1.5-bit pipeline stages, the implementation of additional reference voltage circuits will increase the overall circuit complexity, power consumption and die size. Therefore, in this design, all the pipelined stages will use the same reference $\pm V_{ref}/2$ employed in the mixed-mode S/H circuit.

The pipelined stages 1 to 6 in this ADC are implemented according to the modified 1.5-bit stage as illustrated in Figure 6.3. It has a similar configuration as that of the mixed-mode S/H circuit. Because the half reference is used, the capacitor C_S is twice the size of C_F as shown in Figure 6.3. In the sampling phase ϕ_1 , the input signal is sampled by capacitor C_S . At the end of ϕ_1 , the two comparators, which have threshold voltages set at $-V_{ref}/4$ and

Figure 6.3: The modified 1.5-bit stage.

$+V_{ref}/4$ respectively, quantize the input signal and generate the digital output 00, 01 or 10. During the amplifying phase ϕ_2 , C_S is connected to $+V_{ref}/2$, 0, or $-V_{ref}/2$ according to the comparator outputs. The feedback capacitor C_F , reset at the sampling phase, is connected around the op amp during the amplifying phases. During the sampling phase, the op amp input and output are connected, forming an unity-gain configuration which is also known as auto-zero in switch-capacitor circuits. The auto-zero implementation eliminates the op amp offset error. The transfer function of the modified 1.5-bit stage is the same as that of conventional 1.5-bit stage which is

$$V_{out} = \left(1 - \frac{1}{A_0 \cdot \beta} - \frac{\Delta C}{C}\right)(2 \cdot V_{in} - D \cdot V_{ref}) \quad (6.3)$$

where $\beta = C/(3C + \Delta C + C_{in})$ is the feedback factor. C_{in} denotes the op amp parasitic input capacitance. D has the value of -1, 0, or 1.

The relation between V_{in} , D_i , and connection of C_S is shown in Table 6.1.

Table 6.1: Relation between V_{in} , D_i , and connection of C_S

V_{in}	D_i	Connection of C_S
$< -V_{ref}/4$	-1	$-V_{ref}$
$-V_{ref}/4 \leq V_{in} \leq +V_{ref}/4$	0	0
$> +V_{ref}/4$	$+1$	$+V_{ref}$

Ignoring the op amp finite gain and capacitor mismatch, the transfer curve of the modified 1.5-bit stage is shown in Figure 6.4. Since the mixed-mode S/H circuit limits its output within $-3V_{ref}/4$ to $+3V_{ref}/4$, the output of the 1.5-bit stage will not exceed $\pm V_{ref}/2$ theoretically. To guarantee all the pipeline stages work in half signal swing, the maximum comparator offset error in the modified 1.5-bit stage should be smaller than $V_{ref}/8$.

With the output swing reduced, the op amp gain and capacitor matching requirements in pipelined stages is also relaxed for the same reasons discussed on the mixed-mode S/H circuit. As the first 1.5-bit stage has a 1-bit effective resolution, the remaining resolution for the following stages is $N - 1$ bits. The op amp gain and capacitor matching requirements are relaxed to

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C}\right) < \frac{1}{2^{N-1}} \quad (6.4)$$

which is 6 dB higher, i.e. the tolerance is higher, than the requirement for the conventional 1.5-bit stage as expressed in (6.1).

Assume that the op amp parasitic input capacitance is half of C_F , the feedback factor of the modified 1.5-bit stage is $\beta = C_F/(C_F + 2C_F + C_F/2) = 2/7$. The feedback

Figure 6.4: Transfer curve of the 1.5-bit stage.

factor of the modified 1.5-stage is smaller than that of conventional 1.5-bit stage, which is $\beta = C_F / (C_F + C_F + C_F/2) = 2/5$. However, due to the reduction of output swing by half, the op amp gain requirement in the modified 1.5-bit stage is reduced by

$$\Delta A_0 = 20 \log\left(\frac{5}{2} \times 2^N\right) - 20 \log\left(\frac{7}{2} \times 2^{N-1}\right) = 3 \text{ dB} \quad (6.5)$$

Since in the medium-resolution pipelined ADC, the op amp can be designed at a relatively low gain, a smaller capacitance can be chosen to take the advantage of signal swing reduce. In this design, C_F was chosen to be 100-fF which is the minimum capacitor size supported by the process chosen (0.18- μm , Chartered Semiconductor Manufacturing). The foundry design guide shows that the 100-fF capacitance has a 3σ mismatch smaller than

0.8%. For an 8-bit pipelined ADC in a conventional implementation, the mismatch should be less than 0.4%.

Since the output amplitude is less than half of the full-scale, the op amp unity gain bandwidth requirement in the modified first 1.5-bit stage is

$$\omega_u > \frac{2 \cdot (N - 1) \cdot f_s \cdot \ln 2}{\beta} \quad (6.6)$$

Assume the capacitive load of the modified 1.5-bit stage is C_L , the input transistor transconductance of the op amp can be express as

$$\begin{aligned} g_m &= \omega_u \cdot C_L \\ &= \frac{2 \cdot (N - 1) \cdot f_s \cdot \ln 2}{\beta} \cdot C_L \\ &= 7(N - 1) \cdot f_s \cdot \ln 2 \cdot C_L \end{aligned} \quad (6.7)$$

In the conventional 1.5-bit stage, the maximum signal swing equals to the full-scale voltage, $2V_{ref}$. Therefore a better capacitor matching is required, and consequently a larger capacitor is needed. For the conventional 1.5-bit stage to achieve the same accuracy as the modified 1.5-bit stage which has a capacitive load of C_L and signal swing of $FS/2$, the capacitive load of the conventional 1.5-bit stage needs to be $2C_L$ because of capacitor matching requirement. Hence, the input transistor transconductance of the op amp in the conventional 1.5-bit stage is

$$\begin{aligned} g_m &= \omega_u \cdot 2C_L \\ &= \frac{2 \cdot N \cdot f_s \cdot \ln 2}{\beta} \cdot 2C_L \\ &= 10N \cdot f_s \cdot \ln 2 \cdot C_L \end{aligned} \quad (6.8)$$

The op amp power consumption is proportional to the g_m of the input transistor. Therefore, although the modified 1.5-bit stage has a smaller feedback factor compared to that of the conventional design, the power consumption of the modified stage is lower due to the smaller capacitive load. Moreover, the reduced signal swing and capacitor size reduce the op amp slew rate requirement as well, thus, an improved speed is expected.

Since the feedback capacitor C_F is connected around the input and output of the op amp during both the sampling mode and amplifying mode, no switch is needed for this capacitor. Therefore eliminated the nonlinearity caused by the switches connecting C_F for op amp output.

The op amp and capacitor matching requirements of the conventional 1.5-bit stage and the modified 1.5-bit stage are summarized in Table 6.2

Table 6.2: Requirements comparison

	Min. op amp gain	Min. op amp bandwidth	Max. capacitor mismatching
Conventional 1.5-bit Stage	$A > \frac{1}{\beta} \cdot 2^N$	$\omega_u > \frac{1}{\beta} \cdot 2 \cdot N \cdot f_s \cdot \ln 2$	$\Delta C < \frac{1}{2^N}$
Modified 1.5-bit Stage	$A > \frac{1}{\beta} \cdot 2^{N-1}$	$\omega_u > \frac{1}{\beta} \cdot 2 \cdot (N - 1) \cdot f_s \cdot \ln 2$	$\Delta C < \frac{1}{2^{N-1}}$

6.1.3 Op Amp

The first pipelined stage uses the same op amp as that used in the mixed-mode S/H circuit due to the high gain and large bandwidth requirements in the first stage.

Since the op amp performance requirements are gradually relaxed along with the pipeline, begin from the second pipelined stage, the single-stage telescopic op amp without gain

boosting is used. The schematic of the telescopic op amp including the biasing circuit is shown in Figure 6.5. The bodies of NMOS are connected to ground and that of PMOS are connected to V_{DD} . The sizes of the devices in the op amp and the biasing current are listed in Table 6.3.

Table 6.3: Device size and biasing current of the second stage op amp

Device	Width (μm)	Length (μm)	Current (μA)
M_1, M_2	48	0.2	480
M_3, M_4	48	0.2	480
M_5, M_6	48	0.2	480
M_7, M_8	180	1.0	480
M_9	144	0.3	960
M_{B1}, M_{B2}, M_{B3}	12	0.3	80
M_{B4}, M_{B5}	8	0.2	80
M_{B6}, M_{B7}	30	1.0	80
M_{B8}	30	1.0	80
M_{B9}, M_{B10}	8	0.2	80

The simulation results show that the second stage op amp has a dc gain of 56 dB, a unity gain bandwidth of 1.2-GHz and a phase margin of 65 degree as shown in Figure 6.6. The gain variation with respect to the output voltage of the second stage op amp is shown in Figure 6.7. The power consumption of the second stage op amp is 2.3-mW.

Figure 6.5: Telescopic op amp in the second stage.

Figure 6.6: Gain and phase plot of the second stage op amp.

Figure 6.7: Gain variation of the second op amp.

6.1.4 Comparator

The sub-ADC in pipelined stages consists of two differential comparators with threshold voltage at $+V_{ref}/4$ and $-V_{ref}/4$ respectively. The differential input comparator, shown in Figure 6.8, has the similar switching current source implementation as that of the comparator used in the mixed-mode S/H circuit for reducing offset errors. In this circuit the bodies of NMOS are connected to ground and that of PMOS are connected to V_{DD} . The two threshold voltages $+V_{ref}/4$ and $-V_{ref}/4$ are generated by the dimension ratio between M_1 M_2 and M_{1a} M_{2a} . The threshold voltage of the comparator is determined by the balanced currents at the source of M_4 and M_5 . Since the external provided reference voltage is $V_{ref}/2$ and the required comparator threshold voltage is $V_{ref}/4$, the relation of the currents of M_3 and M_{3a} is $I_{M3} = 2I_{M3a}$. Therefore, the transistor size relation is given by

$(W/L)_{M1,M2,M3} = 2(W/L)_{M1a,M2a,M3a}$. The comparator is simulated at the worst-case which is with fast MOS model and manually increased the transistor size of M_1 , M_4 and M_7 by 20%. The simulated offset voltage of the switching current source comparator is 35-mV as shown in Figure 6.9. The offset voltage is much larger than that of the comparator in the S/H circuit due to the differential implementation. Two more input transistors are used in the differential comparator therefore the mismatch is doubled and the offset voltage is approximately four times. The comparator without switching biasing is also simulated in the same worst-case condition to compare offset voltages. The simulated offset error of the comparator without switching current source is 62.5-mV as shown in Figure 6.10.

Figure 6.8: The differential comparator.

The sizes of the devices in the comparator are listed in Table 6.4.

The output of the comparator are stored by true single phase clock (TSPC) DFFs to control the switches in next clock phase. The schematic of the TSPC DFF is shown in

Figure 6.9: Offset error simulation of the comparator in modified 1.5-bit stages.

Figure 6.10: Offset voltage simulation of the comparator without switching bias.

Table 6.4: Device size of the pipelined stage comparator

Device	Width (μm)	Length (μm)
M_1, M_2	12	0.3
M_{1a}, M_{2a}	6	0.3
M_3	12	0.3
M_{3a}	6	0.3
M_4, M_5	1	0.18
M_6, M_7	4	0.18
M_8, M_9	1	0.18
M_{10}	1	0.18

Figure 6.11. The encoder converts the thermometer code into binary code. The function of encoding is implemented inside the TSPC DFFs. The TSPC DFFs also serves as the delay line to propagate the digital output codes.

Figure 6.11: The TSPC DFF.

6.1.5 Biasing Circuit

Since transistor transconductances are important parameters in op amps, the g_m constant biasing circuit is used in this design to stabilize transistor transconductances across temperature and supply voltage variations to a first order effect [89].

The bias circuit is shown in Figure 6.12. Around the loop consisting of M_2 , M_1 , and R_B , we have

$$V_{GS2} = V_{GS1} + I_1 R_B \quad (6.9)$$

where I_1 is the current of M_1 . Due to the current mirror pair M_7 and M_8 , we have $I_1 = I_2$, where I_2 is the current of M_2 . From these conditions, we can derive

$$g_{m2} = \frac{2[1 - \sqrt{\frac{(W/L)_{M2}}{(W/L)_{M1}}}]}{R_B} \quad (6.10)$$

where (W/L) is transistor channel width and length ratio. Thus, the transconductance of M_2 is determined by geometric ratios only, and independent of power-supply voltages, process parameters, and temperature. Since all transistor currents are derived from the same biasing network, all other transconductances are also stabilized. Thus, we have, for NMOS

$$g_{mi} = \sqrt{\frac{(W/L)_{M1} I_i}{(W/L)_{M2} I_2}} \times g_{m2} \quad (6.11)$$

and for PMOS

$$g_{mi} = \sqrt{\frac{\mu_p (W/L)_{M1} I_i}{\mu_n (W/L)_{M2} I_2}} \times g_{m2} \quad (6.12)$$

The transistors M_9 to M_{14} provide the bias for the PMOS cascode devices and the NMOS cascode devices, respectively. Transistors M_{15} to M_{18} form the start-up circuit that only affects the operation if all the currents are zero at start up.

The transistor sizes and branch currents are listed in Table 6.5.

Figure 6.12: The biasing circuit.

6.1.6 MOS Switches

The size of the MOS switch has impacted both on the sampling time and linearity. With the sampling capacitor equals 200-fF, and sampling time of 2.5-ns, for the RC time constant smaller than one tenth of the sampling time, the on-resistance of the MOS switch should be less than 1250-ohm.

Figure 6.13 illustrates the test bench setup for the simulation of the MOS switch linearity. The amplitude of the 100-MHz input sinewave signal is 300-mV, which is 3/4 of a 800-mV full scale input. The simulation result of $8\mu/0.18\mu$ CMOS switch sampling a 100-MHz signal is shown in Figure 6.14. The SFDR is 68.8-dB, which is enough for 8-bit ADC application.

Table 6.5: Device size and biasing current of the biasing circuit

Device	Width (μm)	Length (μm)	Current (μA)
M_1	80	1.0	16
M_2	16	1.0	16
M_3, M_4	16	1.0	16
M_5, M_6	32	1.0	16
M_7, M_8	32	1.0	16
M_9, M_{10}	16	1.0	16
M_{11}	2	1.0	16
M_{12}	6	1.0	16
M_{13}, M_{14}	16	1.0	16
M_{15}, M_{16}	16	1.0	0
M_{17}	1	20	0
M_{18}	16	1.0	0
M_{19}, M_{20}	32	1.0	16
R_B	2.2-kohm		

The worst-case (slow model at 125C) simulation of the CMOS switch shows an on-resistance of 488-ohm as shown in Figure 6.15. This value is much less than the 1250-ohm requirement.

Therefore, except for the input switches of the S/H circuit, all the switches in this pipelined ADC are implemented by CMOS transmission gate with the transistors size of

Figure 6.13: Switch linearity setup.

Figure 6.14: Simulated linearity of CMOS switch.

$8\mu/0.18\mu$. The input switches of the S/H circuit are implemented in the bootstrapped configuration as described in Chapter 5.

Figure 6.15: Worst case simulation of on-resistance.

6.1.7 Capacitor Size

The full-scale input range of the 8-bit ADC is $800\text{-}mV_{pp}$. Based on equation (2.2), for the thermal noise less than quantization noise of 8-bit ADC, the sampling capacitance should satisfy

$$C_F \cdot \beta > \frac{kT \cdot 12}{LSB^2} = 5 \text{ fF} \quad (6.13)$$

which is quite small compared to the selected value. Therefore, in this design, the capacitor size is limited by the matching requirement, which is 0.6%. Small capacitance can be chosen to take the advantage of the reduced signal swing. In this design, as mentioned before, C_F is selected to be 100-fF which is the minimum capacitance size supported by the process chosen.

From the SC circuit noise analysis given by equation (4.25) in Chapter 4, it is desirable

to maximize the feedback factor β to minimize the thermal noise. Although the mixed-mode S/H technique decreases the feedback factor slightly, its effect on the thermal noise is not significant. In a medium-resolution pipelined ADC, the capacitor size is determined by the matching requirement instead of the thermal noise.

6.1.8 Clock Generator

In a pipelined ADC, non-overlapping multi-phase clocks are required for charge injection cancellation. The clock generation circuit used in this pipelined ADC is shown in Figure 6.16. The phase delay and non-overlapped intervals are controlled by the propagation delays of inverters and NAND gates.

Figure 6.16: The clock generator.

The simulated output of the clock generator is shown in Figure 6.17. The non-overlapping time of $CLK1$ and $CLK2$ is 400-ps.

Figure 6.17: Output of the clock generator.

6.1.9 Digital error correction

The schematic of the digital error correction logic is shown in Figure 6.18. It consists of eight full adders. Digital signal F0 to F14 are from the S/H and pipeline stages output. The final 8-bit out are latched in eight DFFs.

Figure 6.18: Diagram of the digital error correction logic.

6.1.10 Decimation Circuitry

In order to make the prototype ADC testable on wafer, the 8-bit digital output are decimated by 8 and converted into serial outputs. Therefore only one output pad is needed to test the prototype ADC. The decimation and serialization blocks are shown in Figure 6.19. Also shown is the timing diagram of the decimation and serialization blocks. The sampling clock is first divided by 8. The CLK/8 triggers eight D flip-flops to store the output every eight sampling clock cycles. The serialize block outputs 1-bit output every sampling clock cycle and it takes eight clock cycles to output the whole 8-bit output.

Figure 6.19: Decimation and serialization blocks and timing.

6.2 Conclusion

Based on the mixed-mode sampling technique, this chapter describes the design of an 8-bit pipelined ADC. A modified 1.5-bit pipeline stage architecture is also proposed. The modified 1.5-bit stages use the same reference $\pm V_{ref}/2$ employed in the mixed-mode S/H circuit. Compare to conventional implementation, op amp performance and capacitor matching requirements are relaxed in the modified 1.5-bit stage due to the mixed-mode sampling technique. The MOS switch requirements are also relaxed due to the reduction of the signal swing. In order to test the prototype chip on wafer, decimation and serialization circuits are added at the back-end of the ADC.

Chapter 7

Layout Implementation and Measurement Results

In the implementation of high speed and high frequency ADC, the circuit design, layout and measurement setup play an important role in the performance of the final product. Many considerations are required to minimize noise coupling, signal cross talking, mismatching, and nonlinearities. A careful and comprehensive measurement setup is necessary to guarantee the ADC performance is accurately measured. This chapter describes the layout of the prototype chip and the test setup used to characterize the performance as well as the measurement results.

7.1 Layout Implementation

7.1.1 Floor Plan

In high speed ADCs, careful floor planning is crucial to minimize the noise coupling between the analog circuit and the digital circuit. The layout floor plan of the prototype chip is shown in Figure 7.1. The analog area and digital area are allocated at top and bottom side of the chip, respectively. One N-well trench and one P+ substrate contact are laid between these two areas to isolate and prevent the digital noise circuitries from coupling to the sensitive analog circuit. The S/H circuit and the seven pipelined stages are laid out in one straight row to minimize the signal path and to share the same clock bus. The clock bus is next to the N-well trench and used by both analog circuits and digital circuits in the analog-to-digital conversion. The clock generator is placed close to the S/H circuit to reduce the clock skew errors. Although the later pipelined stages are far away from the clock generator, their resolution is low and larger clock skew errors can be tolerated. The clock generator is encircled by the N-well trench and P+ substrate contacts for noise isolation propose. The supply and ground lines of analog circuit and digital circuit are separated in chip also for noise isolation propose. These two supply lines and two ground lines will be connected outside the chip respectively. By using separate supply and ground lines for the analog and digital circuits, the sensitive analog circuits are decoupled from the digital switching noise introduced by large transient currents flowing in the digital supply and ground lines. Hence, the analog supply and ground lines are used for the op amps, switches, and bias circuits, while the clock generator, the comparator and digital circuits are connected to the digital supply and

Figure 7.1: The layout floor plan.

ground lines. The comparators are placed at digital area although their inputs are analog signals. This is necessary as the dynamic comparators generate a large amount of noise during switching. The comparator offset tolerance characteristic of the pipelined ADC allows the comparators to be placed in the noisy digital area. Wide top metal lines are used as the supply lines from the pads to the interior of the chip to lower the series resistance and reduce voltage drops. Multiple pins are allocated to analog supply and ground lines to reduce the parasitic inductance and the series resistance. Furthermore, on-chip decoupling capacitor formed by transistors have been used to minimize the transient disturbance of the supply voltage. All substrate contacts are tied to analog ground so that no digital switching noise gets coupled to the signal path through the substrate. All the supply and ground lines of analog blocks are connected in a star configuration to minimize interference. The layout of the prototype chip is shown in Figure 7.2. Whenever possible, differential signals are routed together and shielded to minimize the coupling noise. The prototype pipelined ADC

was fabricated using the Chartered 0.18- μm 2P6M CMOS process. The microphotograph of the die, with the location of the S/H circuit, pipelined stages, biasing circuits, and clock circuits indicated, is shown in Figure 7.3. This chip occupies $0.8 \times 1.2 \text{ mm}^2$ but the active area is only $0.4 \times 0.8 \text{ mm}^2$.

Figure 7.2: Layout of the prototype chip.

7.1.2 Op Amp Layout

The simulation shows that the op amp settling time is 2-ns which is very close to the calculated requirement. Therefore, it is very important to reduce the external parasitics of the op amp and to reduce sources of errors such as op amp offset in layout. Figure 7.4 shows the layout of the op amp in the S/H circuit. The interdigitized layout technique are

Figure 7.3: The microphotograph of the pipelined ADC.

applied to MOS transistors to have better matching. Dummy transistors are added at each end also for better matching also. Metal overlapping is avoid as much as possible in order to reduce the parasitic capacitances.

7.1.3 Capacitor Layout

Since small capacitor sizes (100-fF and 200-fF) are used in this prototype ADC, the parasitic capacitances, such as the interconnect parasitics, become significant. It is important to match the parasitic capacitances to improve capacitor matching. The layout of the capacitor C_S and C_F in the modified 1.5-bit stage is shown in Figure 7.5. C_F has a value of 100-fF and is placed at the middle. C_S consists of two 100-fF capacitors which are placed at two sides. This minimizes the mismatch caused by the gradient effects across the wafer. Dummy metal connections are routed in C_F to match the parasitic capacitance of C_S due to metal connections. All the capacitors are surrounded by a dummy ring to allow for edge

Figure 7.4: The layout of op amp in the S/H circuit.

matching.

7.1.4 Clock Phases Arrangement

The prototype pipelined ADC uses eight clock phases for signal processing. In order to minimize the cross talk between these clock phases, the clock bus is arranged as illustrated in Figure 7.6. In this arrangement, two neighboring clocks don't transit in different directions, therefore the effect of the signal cross talk becomes minimum and the rising and

Figure 7.5: The capacitors layout.

falling time of the clocks are minimized. The clock bus is shielded from the substrate by a N-well layer to reduce the clock noise coupling through the substrate. Top metal lines are used to distribute clock signals throughout the chip because of their lower resistances and lower parasitic capacitance to the substrate. Wherever the clock lines cross a sensitive analog signal, shielding is provided by a metal ground layer between the clock lines and the analog path.

7.2 Test Setup

Since the prototype is going to be tested on wafer, a 10-pin probe is used and an interface PCB board is made for the interface between the signal generators and the probe. Figure 7.7 shows the schematic of the interface board. The transformer is a Mini-Circuits RF transformer, model ADT4-1WT which has an impedance ratio of 4 (turns ratio of 2). The 3 dB bandwidth of this transformer is from 2-MHz to 775-MHz. The signal generator source

Figure 7.6: Clock bus arrangement and clock phases.

impedance is 50-ohm, therefore the 1:4 impedance ratio requires the 200-ohm secondary termination for optimum power transfer. The center tap of the transformer secondary winding connects to the common mode voltage, shifting the input signal to the optimum $V_{DD}/2$ common-mode voltage of the ADC. The R_S resistors serve to isolate the transformer secondary winding from the switching transients, and the chosen value is to be 25-ohm. The C_1 capacitors serve as common-mode charge reservoirs for the switching transients and also provide noise filtering (in conjunction with the R_S resistors). C_2 is added for additional differential filtering. The same single-end to differential conversion circuit is used

to generate the differential clock signals. For a robust mount of the wires on the 10-pin probe, the reference voltages also input to the device through the PCB. The common-mode voltage is obtained by taking the midpoint of the reference voltages. All the supplies and references are decoupled with 0.01- μF , 1- μF , and 10- μF capacitors located as close to the device as possible. The picture of the PCB board is shown in Figure 7.8 which is a two sided copper clad board

Figure 7.7: Schematic of the interface board.

The ADC is on wafer tested using the Cascade Summit 15751 8-inch probing system

Figure 7.8: The interface board.

which is shown in Figure 7.9. The test setup is shown in Figure 7.10. The Hewlett Packard 8648D signal generator are used as signal and clock inputs. The single-end signal is filtered by Mini-Circuit low pass filter to attenuate harmonics and out-of-band noise. The clock signal from the Hewlett Packard 8648D signal generator is directly differentiated by a Mini-Circuit ADT4-1WT transformer and DC biased to the CMOS trigger levels. The ADC is tested on wafer. The differential input signals, the reference voltages, and analog supply and ground are applied to the ADC through a Cascade multi-contact Eye-Pass 10-pin probe which is shown in Figure 7.11. This probe also has a 450-nF built-in decoupling capacitor, between power line and ground. The differential clock signals are injected through a Cascade Infinity GSSG probe. The digital supply and ground are brought in by a Cascade DC probe. The analog supply and digital supply are connected together off-chip.

The output data are collected by a Cascade Infinity GSG probe and a storage oscilloscope, Lecory 8600A, and analyzed using Matlab.

Figure 7.9: The probing station.

7.3 Measurement Results

The measured power consumption is 22-mW excluding the decimation, serialization and output buffer with 1.8-V supply voltage.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.3

Figure 7.10: The test setup.

Figure 7.11: The 10-pin probe.

LSB and 0.34 LSB when sampling at 200-MSample/s as plotted in Figure 7.12 and Figure 7.13, respectively. The INL plot is based on the best-straight-line linearity definition. The INL curve has three jumps and is similar to the INL of a pipelined ADC with 2-bit first

Figure 7.12: Measured DNL plot.

Figure 7.13: Measured INL plot.

stage. This is due to the combination of the 1-bit S/H digital output and the 1.5-bit first stage output, which makes this ADC has a similar INL plot as that of a 2-bit first stage.

Figure 7.14 shows the measured fast Fourier transform (FFT) plot of a 90.723-MHz sinuswave input at the sampling rate of 200-MSample/s, where the SFDR and SNDR are 54.5 dB and 44.8 dB respectively. the input signal frequency is chosen to be coherent with respect to the sampling frequency; therefore a window function is not required. The

distortion is dominated by the 3rd harmonic. Plotting in Figure 7.15 are the measured SNDR and SFDR as function of the input signal frequency while the ADC operates at 200-MSample/s. The SFDR drops at high input frequencies due to the increasing aperture error in the mixed-mode S/H circuit and the limited settling time of the op amp. Another reason for the reduction in dynamic range at high sampling rates is believed to be board-level disturbances on the input and reference voltage lines. The measured SNDR and SFDR as functions of sampling frequency are plotted in Figure 7.16 for a 40-MHz input signal. The SNDR and SFDR are approximately constant for low sampling rate and starting to drop as the sampling rate larger than 180-MHz. The effective number of bits (ENOB) for a 40-MHz signal sampled at 200-MSample/s is 7.2-bit, drops to 7-bit at 220-MSample/s and further down to 6.5-bit at 250-MSample/s.

The measured ADC results are summarized in Table 7.1. The reported performance of 8-bit high speed pipelined ADCs are compared in Table 7.2 in which the figure of merit (FOM) is defined as

$$FOM = \frac{P}{2^{ENOB} \cdot f_s} \quad (7.1)$$

where P is power consumption and f_s is sampling frequency. The figure of merit of this work is 0.74 pJ/conversion, which is comparable with other reports in similar technologies.

Figure 7.14: FFT plot of 90-MHz input at 200-MSample/s.

7.4 Conclusion

This chapter describes the layout implementation and measurement results of the prototype ADC. Careful floor plan and layout techniques are chosen to minimize noise coupling, signal cross talking and mismatching. The on-wafer test setup are describe also in this chapter. Implemented in a 0.18- μm CMOS process, the 8-bit pipelined ADC achieves a sampling rate up to 200-MSample/s with 54-dB SFDR and 45-dB SNDR. The measured INL and DNL are 0.34 LSB and 0.3 LSB, respectively. The power consumption of the prototype ADC is 22-mW at the supply voltage of 1.8-V.

Figure 7.15: SNDR and SFDR versus input frequency at 200-MSample/s.

Figure 7.16: SNDR and SFDR versus sampling frequency with 40-MHz input.

Table 7.1: Performance Summary

Technology	0.18 μ m 2P6M CMOS
Resolution	8-bit
Sampling Rate	200 MS/s
Supply Voltage	1.8 V
Input Range	0.8 V _{pp}
DNL / INL	0.3 LSB / 0.34 LSB
SNDR (f_{in} =40 MHz)	45.2 dB
SNDR (f_{in} =99 MHz)	44.2 dB
SFDR (f_{in} =40 MHz)	60.4 dB
SFDR (f_{in} =99 MHz)	53.4 dB
Active Area	0.8mm $\times$ 0.4mm
Power Consumption	22 mW

Table 7.2: Performance Comparison

8-b ADC	Tech.(μ m)	ENOB	f_s (MHz)	Power(mW)	FOM
[58]	0.18	7.25	150	71	3.1
[59]	0.13	7.6	125	21	0.87
[82]	0.18	7.68	200	30	0.73
This work	0.18	7.2	200	22	0.74

Chapter 8

Conclusion and Future Works

8.1 Conclusion

Analog-to-digital converters are key components in digital communication receivers. For wideband applications following IEEE 802.11 standards, an ADC resolution of 8 or 9 bits is sufficient to meet the system SNR requirement. However, a sampling rate of hundreds Msample/s is required to support the increasing signal bandwidth and to relax the anti-alias filter design. In addition, the power consumption of the ADC has to be minimized for the portable operation powered by battery.

The pipelined ADC architecture is a popular candidate for wideband receivers due to its high speed and power efficiency. Most of the pipelined ADCs are implemented in switched-capacitor circuits. The performance of an SC implemented pipelined ADCs is determined by the op amp and the capacitor size. The op amp must have high DC gain, high slew-rate and wide bandwidth to meet the accuracy and speed requirements. The op

amp performance also has effects on the linearity of the S/H circuit and pipeline stages, thus consequently the overall ADC dynamic performance. The capacitor size is another factor that limits the pipelined ADC performance. In a medium resolution pipelined ADC, the capacitor size is limited by matching instead of thermal noise. A large capacitor size translates to higher power consumption and lower speed.

In order to achieve a desirable SNR, a large signal swing is required in pipelined ADCs. However, a large signal swing has significant effects on the SC circuit performance. It increases the op amp gain and capacitor matching requirements, leading to high power consumption and slow conversion speed. A large signal swing also deteriorates the pipelined ADC's dynamic performance. As the device size and supply voltage decrease, the effects of signal swing on op amp gain and linearity become significant. A detailed analysis of these effects is described. Thus, although single stage cascode op amps are fast and consume less power, they are not commonly used in pipelined ADCs due to the poor gain and linearity performance at the large signal swing.

This project focuses on the design and implementation of high-speed low power CMOS analog-to-digital converter for wideband communication applications. ADC system level performance requirements are derived for direct conversion and low-IF receivers. Pipelined ADC architecture is chosen because it is very suitable for high speed low power applications. The building block performance requirements in pipelined ADCs are derived based on the ADC resolution and sampling rate. The sources of error in pipelined ADCs are also discussed and the solutions to eliminate these errors are also presented.

This project studies the effect of signal swing on the performance of SC pipelined

ADC. In order to reduce the signal swing while maintain the SNR, a mixed-mode sampling technique is proposed. The mixed-mode S/H circuit reduces the op amp gain, bandwidth, slew rate as well as the capacitor matching requirements in pipelined ADC, which leads to high speed and low power consumption. A modified 1.5-bit stage is proposed to co-operate with the mixed-mode S/H circuit. Small capacitor sizes are used in the prototype ADC to verify the mixed-mode sampling technique. Fabricated in a 0.18- μm CMOS process, the proposed pipelined ADC shows 7.2 ENOB at 200-MSample/s with only 22-mW power consumption.

8.2 Future Works

Potential future improvements include increasing the sampling rate and the precision of the ADC. With input frequency increasing, the aperture error in the mixed-mode S/H circuit becomes significant and reduces the effect of the mixed-mode sampling in terms of signal swing. How to reduce the aperture error in the mixed-mode S/H circuit at high frequency is a challenging topic for future work. One possible solution is to investigate new sampling architectures to improve the time constant matching in the mixed-mode S/H.

The future work could also focus on even lower supply voltage operation. The mixed-mode sampling technique proposed in this project reduce the signal swing and op amp gain requirements, making it attractive to the more advanced technology and lower supply voltage, such as 0.13- μm process working at 1-V supply. Normally the device matching characteristic is better in the more advanced technology. Therefore, smaller capacitors can

be used and the op amp gain requirement can be lower.

Another application of the mixed-mode sampling technique is in the high resolution low speed pipelined ADCs. In this kind of ADCs, the aperture error in the S/H circuit is small due to the low sampling rate. Therefore, the op amp can take full advantages of the mixed-mode sampling technique since the op amp gain requirement in this kind of ADC is quite high in conventional implementation.

The precision of the ADC can be improved by chip packaging and generating the reference voltages on chip to reduce the voltage fluctuations that result from the switching.

Publications

1. S. Jiang, M. A. Do, J. G. Ma and K. S. Yeo, "A Modified First Stage of Pipelined Analog-to-Digital Converters," *IEEE International Symposium on Integrated Circuits, ISIC-2004*, Singapore, Sep. 2004.
2. S. Jiang, M. A. Do, J. G. Ma and K. S. Yeo, "A 1.8-V 8-bit 200-MS/s Pipelined A/D Converter Using a Doubled Reference Voltage," *IFIP International Conference on Very Large Scale Integration, VLSI-SoC 2005*, Perth, Australia, Oct. 2005.
3. S. Jiang, M. A. Do and K. S. Yeo, "A 200-MHz CMOS Mixed-Mode Sample-and-Hold Circuit for Pipelined ADCs," *IFIP International Conference on Very Large Scale Integration, VLSI-SoC 2006*, Nice, France, Oct. 2006.
4. S. Jiang, M. A. Do and K. S. Yeo, "A CMOS Mixed-Mode Sample-and-Hold Circuit for Pipelined ADCs," *Selected chapter in the book "VLSI-SoC: Research Trends in VLSI and Systems on Chip" published by Springer in Dec. 2007.*
5. S. Jiang, M. A. Do and K. S. Yeo, "An 8-bit 200MSample/s Pipelined ADC with Mixed-Mode Front-End S/H Circuit," *Accepted by IEEE Trans. Circuits and Systems I.*

Bibliography

- [1] F. Agnelli, G. Albasini, I. Bietti, A. Gnudi, S. Vitali, and R. Castello, “Wireless Multi-Standard Terminals: System Analysis and Design of a Reconfigurable RF Front-End,” *IEEE Circuits and Systems Magazine*, pp. 38-59, First Quarter 2006.
- [2] A. A. Abidi, “Direct-Conversion Radio Transceivers for Digital Communications,” *IEEE J. Solid-State Circuits*, vol 30, no. 12, pp. 1399-1410, December 1995.
- [3] W. Kester, *Data Conversion Handbook*, Elsevier, 2005.
- [4] W. R. Bennett, “Spectra of Quantized Signals,” *Bell System Technical Journal*, Vol 27, July 1948, pp. 446-471.
- [5] “IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters,” *IEEE Standard 1241-2000*, Approved 7 December 2000.
- [6] Mikael Gustavsson and J. Jacob Wikner, “CMOS Data Converters for Communications,” Kluwer Academic Publisher, 2000.

- [7] J. Huang and R. R. Spencer, "The Design of Analog Front Ends for 1000BASE-T Receivers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 10, pp. 675-684, Oct. 2003
- [8] A Tutorial Presentation for 1000BASE-T, Online available at:
- [9] Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications High-Speed Physical Layer in the 5 GHz Band, Sept. 1999
- [10] Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, Jun. 2003.
- [11] Michael Choi and Asad A. Abidi, "A 6-b 1.3-Gsample/s A/D Converter in 0.35- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1847-1858, December 2001.
- [12] Peter C. S. Scholtens and Maarten Vertregt, "A 6-b 1.6-Gsample/s Flash ADC in 0.18- μm CMOS Using Averaging Termination," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1599-1609, December 2002.
- [13] Koen Uyttenhove and Michiel S. J. Steyaert, "A 1.8-V 6-Bit 1.3-GHz Flash ADC in 0.25- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1115-1122, July 2003.

- [14] Christoph Sandner, Martin Clara, Andreas Santner, Thomas Hartig, and Franz Kuttner, "A 6-bit 1.2-GS/s Low-Power Flash-ADC in 0.13- μm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1499-1504, July 2005.
- [15] Martin Clara, Andreas Wiesbauer, and Franz Kuttner, "A 1.8V Fully Embedded 10b 160MS/s Two-Step ADC in 0.18- μm CMOS," *IEEE Custom Integrated Circuits Conference*, 2002.
- [16] Hendrik Van Der Ploeg, Gian Hoogzaad, and Raf L. J. Roovers, "A 2.5v 12b 54MSample/s 0.25- μm CMOS ADC," *ISSCC* 2001.
- [17] Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design," Second Edition, 2001.
- [18] Yunchu Li and Edgar Sanchez-Sinencia, "A Wide Input Bandwidth 7-bit 300MSample/s Folding and Current-Mode Interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 8 August 2003.
- [19] Myung-Jun Choe, Bang-Sup Song, and Kantilal Bacrania, "An 8-b 100-MSample/s CMOS Pipelined Folding ADC," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, February 2001.
- [20] Yun-Ti Wang and Behzad Razavi, "An 8-Bit 150-MHz CMOS A/D Converter," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, March 2000.
- [21] Robert C. Taft, Chris A. Menkus, Maria Rosaria Tursi, Ols Hidri, and Valerie Pons, "A 1.8-V 1.6-GSample/s 8-b Self-Calibrating Folding ADC With 7.26 ENOB at Nyquist

- Frequency,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2107-2115, December 2004.
- [22] Klaas Bult and Aaron Buchwald, “An Embedded 240-mW 10-b 50-MS/s CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, December 1997.
- [23] Perter Vorenkamp and Raf Roovers, “A 12-b 60-MSample/s Cascaded Folding and Interpolating ADC,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, December 1997.
- [24] Myung-Jun Choe, Bang-Sup Song, and Kantilal Bacrania, “A 13-b 40-MSample/s CMOS Pipelined Folding ADC with Background Offset Trimming,” *IEEE J. Solid-State Circuits*, vol. 35, no. 12, December 2000.
- [25] Pual C. Yu and Hae-Seung Lee, “A 2.5-V 12-b 5-MSample/s Pipelined CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 31, no. 2, December 1996.
- [26] Byung-Moo Min, Peter Kim, and Ario Aude, “A 69mW 10b 80Ms/s Pipelined CMOS ADC,” *ISSCC* 2003.
- [27] John B. Hughes, Martin Mee, and William Donaldson, “A Low Voltage 8-Bit 40-MS/s Switched-Current Pipelined Analog-to-Digital Converter,” *IEEE International Symposium on Circuits and Systems*, vol. 1, May 2001.
- [28] Thomas Byunghak Cho and Paul R. Gray, “A 10b 20Msample/s 35mW Pipeline A/D Converter,” *IEEE J. Solid-State Circuits*, vol. 30, no. 3, March 1995.

- [29] Dong-Young Chang and Un-Ku Moon, "A 1.4-V 10-bit 25-MS/s Pipelined ADC Using Opamp-Reset Switching Technique," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, August 2003.
- [30] Daisuke Miyazake and Shoji Kawahito, "A 10-b 30-MS/s Low-Power Pipelined CMOS A/D Converter Using a Psudodifferential Architecture," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, February 2003.
- [31] Iuri Mehr and Larry Singer, "A 55-mW 10-bit 40-Msample/s Nyquist-Rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, March 2000.
- [32] Hsin-Shu Chen, Bang-Sup Song, and Kantilal Bacrania, "A 14-b 20-MSample/s CMOS Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, June 2001.
- [33] Boris Murmann and Bernhard E. Boser, "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, December 2003.
- [34] Eric B. Blecker, Thomas M. McDonald, and Stephen H. Lewis, "Digital Background Calibration of an Algorithmic Analog-to-Digital Converter Using a Simplified Queue," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, June 2003.
- [35] Lauri Sumanen, Mikko Waltari and Kari A. I. Halonen, "A 10-bit 200-MS/s CMOS Parallel Pipelined A/D Converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 37, July 2001.

- [36] Shafiq M. Jamal, Daihong Fu, and Stephen H. Lewis, "A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, December 2002.
- [37] Teresa H. Meng, Bill McFarland, David Su, and John Thomson, "Design and Implementation of an All-CMOS 802.11a Wireless LAN Chipset," *IEEE Communication Magazine*, pp. 160-168, August 2003.
- [38] Markus Zannoth, Thomas Ruhlicke, and Bernd-Ulrich Klepser, "A Highly Integrated Dual-Band Multimode Wireless LAN Transceiver," *IEEE J. Solid-State Circuit*, vol. 39, No. 7, pp. 1191-1195, July 2004.
- [39] Thomas Byunghak Cho, Daid Kang, Chun-Huat Heng, and Bang Sup Song, "A 2.4-GHz Dual-Mode 0.18- μm CMOS Transceiver for Bluetooth and 802.11b," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1916-1926, November 2004.
- [40] Laurent Perraud, Marc Recouly, Christophe Pinatel, Nicolas Sornin, Jean-Louis Bonnot, Frederic Benoist, Myriam Massei, and Olivier Gibrat, "A Direct-Conversion CMOS Transceiver for the 802.11 a/b/g WLAN Standard Utilizing a Cartesian Feedback Transmitter," *IEEE J. Solid-State Circuit*, vol. 39, no. 12, pp. 2226-2238, December 2004.
- [41] Masoud Zargari, Manolis Terrovitis, Steve Huang-Min Jen, Brian J. Kaczynski, David K. Su, Bruce A. Wooley, "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11 a/b/g Wireless LAN," *IEEE J. Solid-State Circuits*, vol. 39, no 12, pp. 2239-2249, December 2004.

- [42] Tadashi Maeda, Noriaki Matsuno, Shinichi Hori, Tomoyuki Yamase, Takashi Tokairin, and Hikaru Hida, "A Low-Power Dual-Band Triple-Mode WLAN CMOS Transceiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2481-2490, November 2006.
- [43] Tadashi Maeda, Hitoshi Yano, Shinichi Hori, Noriaki Matsuno, Tomoyuki Yamase, and Hikaru Hida, "Low-Power-Consumption Direct-Conversion CMOS Transceiver for Multi-Standard 5-GHz Wireless LAN Systems With Channel Bandwidth of 5-20 MHz," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 375-383, February 2006.
- [44] Shahla Khorram, Hooman Darabi, Zhimin Zhou, Qiang Li, Bojko Marholev, and Ahmadreza Rofougaran, "A Fully Integrated SOC of 802.11b in 0.18- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2492-2501, December 2005.
- [45] Srenik S. Mehta, David Weber, Manolis Terrovitis, Keith Onodera, Michael P. Mack, and Bruce A. Wooley, "A 802.11g WLAN Soc," *IEEE J. Solid-State Circuit*, vol. 40, no. 12, pp. 2482-2491, December 2005.
- [46] D. W. Cline, P. R. Gray, "A power Optimized 13-b 5-Msamples/s Pipelined Analog-to-Digital Converter in 1.2- μm CMOS," *IEEE J. Solid-Stage Circuits*, vol. 31, pp. 294-303, March 1996.
- [47] Okjune Jeon, Robert M. Fox, and Brent A. Myers, "Analog AGC Circuitry for a CMOS WLAN Receiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp.2291-2300, October 2006.

- [48] Hee-Cheol Chol, Ju-Hwa Kim, Sang-Min Yoo, Kang-Jin Lee, Tae-Hwan Oh, Mi-Jung Seo, Jae-Whui Kim, "A 15mW 0.2mm² 10b 50MS/s ADC with Wide Input Range," *ISSCC* 2006.
- [49] Seung-Tak Ryu, Bang-Sup Song, Kanti Bacrania, "A 10b 50MS/s Pipelined ADC with Opamp Current Reuse," *ISSCC* 2006.
- [50] Govert Geelen, Edward Paulus, Dobson Simanjuntak, Hein Pastoor, Rene Verlinden, "A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pj/Conversion-Step," *ISSCC* 2006.
- [51] Seung-Chul Lee, Kwi-Dong Kim, Jong-Kee Kwon, Jongdae Kim, Seung-Hong Lee, "A 10-bit 400-MS/s 160-mW 0.13- μ m CMOS Dual-Channel Pipeline ADC Without Channel Mismatch Calibration," *IEEE J. Solid-State Circuit*, vol. 41, no. 7, pp. 1596-1605, July 2006.
- [52] Daisuke Kurose, Tomohiko Ito, Takeshi Ueno, Takafumi Yamaji, and Tetsuro Itakura, "55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receivers," *IEEE J. Solid-State Circuit*, vol. 41, no. 7, pp. 1589-1595, July 2006.
- [53] Hwi-Cheol Kim, Deog-Kyoon Jeong, and Wonchan Kim, "A Partially Switched-Opamp Technique for High-Speed Low-Power Pipelined Analog-to-Digital Converters," *IEEE Tran. Circuit and Systems-I*, vol. 53, no. 4, pp. 795-801, April 2006.
- [54] Bo Xia, Alberto Valdes-Garcia, and Edgar Sanchez-Sinencia, "A 10-bit 44-MS/s 20-mW Configurable Time-Interleaved Pipeline ADC for a Dual-Mode

- 802.11b/Bluetooth Receiver,” *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 530-539, March 2006.
- [55] Imran Ahmed, and David A. Johns, “A 50-MS/s (35 mW) to 1-kS/s (15 μ W) Power Scaleable 10-bit Pipelined ADC Using Rapid Power-On Opamps and Minimal Bias Current Variation,” *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2446-2455, December 2005.
- [56] Masato Yoshioka, Mashiro Kudo, Kunihiko Gotoh, Yuu Watanabe, “A 10b 125MS/s 40mW Pipelined ADC in 0.18 μ m CMOS,” *ISSCC* 2005.
- [57] Robert Wang, Ken Martin, David Johns, Gangadhar Burra, “A 3.3mW 12MS/s 10b Pipelined ADC in 90nm Digital CMOS,” *ISSCC* 2005.
- [58] Sotirios Limotyrakis, Scott D. Kulchycki, David K. Su, and Bruce A. Wooley, “A 150-MS/s 8-b 71-mW CMOS Time-Interleaved ADC,” *IEEE J. Solid-State Circuit*, vol. 40, no. 5, pp. 1057-1067, May 2005.
- [59] Jan Mulder, Christopher M. Ward, Chi-Hung Lin, David Kruse, Jan R. Westra, Marcel Lugthart, and Frank M. L., “A 21-mW 8-b 125-MSample/s ADC in 0.09- μ m² 0.13- μ m CMOS,” *IEEE J. Solid-State Circuit*, vol. 39, no. 12, pp. 2116-2125, December 2004.
- [60] Robert C. Taft, Chris A. Menkus, Maria Rosaria Tursi, Ols Hidri, and Velerie Pons, “A 1.8-V 1.6-GSample/s 8-b Self-Calibrating Folding ADC With 7.26 ENOB at Nyquist

- Frequency,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2107-2115, December 2004.
- [61] Olaf Stroeble, Victor Dias, Christoph Schwoerer, “An 80MHz 10b Pipeline ADC with Dynamic Range Doubling and Dynamic Reference Selection,” *ISSCC* 2004.
- [62] Bjornar Hernes, Atle Briskemyr, Terje N. Andersen, Frode Telsto, Thomas E. bonnerud, Oystein Moldsvor, “A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13 μ m Digital CMOS,” *ISSCC* 2004.
- [63] Jipeng Li, Un-Ku Moon, “A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique,” *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1468-1476, September 2004.
- [64] J. Arias, V. Boccuzzi, L. Quintanilla, L. Enriquez, D. Bisbal, M. Banu, and J. Barbolla, “Low-Power Pipeline ADC for Wireless LANs,” *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1338-1340, August 2004.
- [65] Jong-Bum Park, Sang-Min Yoo, Se-Won Kim, Young-Jae Cho, and Seung-Hoon Lee, “A 10-b 150-MSample/s 1.8-V 123-mW CMOS A/D Converter With 400-MHz Input Bandwidth,” *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1335-1337, August 2004.
- [66] Sang-Min Yoo, Jong-Bum Park, Seung-Hoon Lee, and Un-Ku Moon, “A 2.5-V 10-b 120-MSample/s CMOS Pipelined ADC Based on Merged-Capacitor Switching,” *IEEE Tran. Circuits and Systems-II*, vol. 51, no. 5, pp. 269-275, May 2004.

- [67] Byung-Moo Min, Pter Kim, Frederick W. Bowman, David M. Boisvert, and Arlo J. Aude, "A 69-mW 10-bit 80-MSample/s Pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2031-2039, December 2003.
- [68] Dong-Young Chang and Un-Ku Moon, "A 1.4-V 10-bit 25-MS/s Pipelined ADC Using Opamp-Reset Switching Technique," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1401-1404, August 2003.
- [69] Daisuke Miyazaki, Shoji Kawahito, and Masanori Furuta, "A 10-b 30-MS/s Low-Power Pipelined CMOS A/D Converter Using a Pseudodifferential Architecture," *IEEE J. Solid-State Circuit*, vol. 38, no. 2, pp. 369-373, February 2003.
- [70] Shafiq M. Jamal, Daihong Fu, Nick C.-J. Chang, Paul J. Hurst, and Stephen H. Lewis, "A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1618-1627, December 2002.
- [71] Jun Ming, Stephen H. Lewis, "An 8-bit 80-Msample/s Pipelined Analog-to-Digital Converter With Backgournd Calibration," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1489-1497, October 2001.
- [72] Lauri Sumanen, Mikko Waltari, and Kari A. I. Halonen, "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1048-1055, July 2001.

- [73] Yong-In Park, S. Karthikeyan, Frank Tsay, Eduardo Bartolome, "A 10b 100MSample/s CMOS Pipelined ADC with 1.8V Power Supply," *ISSCC* 2001.
- [74] Mikko Waltari, and Kari A. I. Halonen, "1-V 9-Bit Pipelined Switched-Opamp ADC," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 129-134, January 2001.
- [75] Iuri Mehr and Larry Singer, "A 55-mW 10-bit 40-Msample/s Nyquist-Rate CMOS ADC," *IEEE J. Solid-State Circuit*, vol. 35, no. 3, pp. 318-325, March 2000.
- [76] Stephen H. Lewis, "Optimizing the Stage Resolution in Pipelined, Multistage Analog-to-Digital Converter for Video-Rate Applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, August 1992.
- [77] Behzad Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2001.
- [78] Mikko Waltari and Kari A. I. Halonen, "1-V 9-bit Pipelined Switched-Opamp ADC," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, January 2001.
- [79] Dong-Young Chang and Un-Ku Moon, "A 1.4-V 10-bit 25-MS/s Pipelined ADC Using Opamp-Reset Switching Technique," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, August 2003.
- [80] Andrew M. Abo and Paul R. Gray, "A 1.5-V 10-bit 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, May 1999.
- [81] Dong-Young Chang, "Design Techniques for a Pipelined ADC Without Using a Front-End Sample-and-Hold Amplifier," *IEEE Trans. Circuits and Systems I*, vol. 51, pp. 2123-2132, November 2004.

- [82] Hwi-Cheol Kim, Deog-Kyoon Jeong, and Wonchan Kim, "A Partially Switched-Opamp Technique for High-Speed Low-Power Pipelined Analog-to-Digital Converters," *IEEE Trans. Circuits and Systems I*, vol. 53, pp. 795-801, April 2006.
- [83] Christian C. Enz and Gabor C. Temes, "Circuit Techniques for Reducting the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE*, vol. 84, pp. 1584-1614, November 1996.
- [84] Klaas Bult and Govert J. G M. Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1379-1384, December 1990.
- [85] B. Yeshwant Kamath, Robert G. Meyer, and Paul. R. Gray, "Relationship Between Frequency Response and Settling Time of Operational Aplifiers," *IEEE J. Solid-State Circuits*, vol. sc-9, pp. 347-352, December 1974.
- [86] M. Dessouky, A. Kaiser, "Input Switch Configuration for Rail-to-Rail Operation of Switched Opamp Circuits," *Electronics Letter*, vol 35, pp. 8-10, January 1999.
- [87] D. Macq, P. G. A. Jesper, "A 10-bit pipelined switched-current A/D converter," *IEEE J. Solid-State Circuits*, vol. 29, pp. 967-971, August 1994.
- [88] C.-Y. Wu, C.-C. Chen, J.-J. Cho, "A CMOS transistor-only 8-bit 4.5-Ms/s pipelined analog-to-digital converter using fully-differential current-mode circuit techniques," *IEEE J. Solid-State Circuits*, vol. 30, pp. 552-532, May 1995.

- [89] David A. John and Ken Margin, "Analog Integrated Circuit Design," John Wiley & Sons Inc., 1997.
- [90] A. Varzaghani and C. K. Yang, "A 600-MS/s 5-Bit Pipeline A/D Converter Using Digital Reference Calibration," *IEEE J. Solid-State Circuits*, vol. 41, pp. 310-19, February 2006.