Characterization and modeling of silicon devices for RF applications

Teo, Tee Hui

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CHARACTERIZATION AND MODELING OF SILICON DEVICES FOR RF APPLICATIONS

TEO TEE HUI

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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Abstract

The objective of this research is to carry out a thorough study of the characterization and modeling of silicon devices for RFIC applications. This work will be beneficial to both Integrated Circuit (IC) design and device development. The present study investigates both passive and active devices in two widely used silicon technologies, namely CMOS and Silicon (Si)/SiGe HBT. For these devices, new direct extraction techniques are discussed, and physically meaningful and unique parameters are obtained.

Due to the lack of comprehensive analysis and experimental data in the literature for differential symmetrical spiral inductors, one main focus of this work is the design and characterization of a full set of such inductors. In addition, the conventional equivalent circuit for asymmetrical on-chip spiral inductor is extracted using a new direct extraction technique. This technique is verified to be effective for a library of spiral inductors with a wide range of device geometries. Moreover, the direct extraction technique is also extended to more advanced equivalent circuits for on-chip spiral inductors.

Although on-chip baluns are widely used in advanced RFIC design, the direct extraction of their equivalent circuits has not been reported. A new test structure and a new direct extraction technique are proposed to extract the equivalent circuit of on-chip balun. Besides being direct, this technique eliminates the use of a $50\ \Omega$ load. For a varactor's capacitance which is bias-dependent, a direct extraction technique is also proposed to extract the parameters. This technique is generic to both pn-junctions and MOS varactors. The extracted equivalent circuit is also made scalable

according to the size of the varactor.

SiGe HBTs are fabricated on lossy silicon substrates. Their substrate parasitic effects cannot be neglected, and should be accurately incorporated in the HBT equivalent circuits. A new test structure in conjunction with a new direct extraction technique are proposed to accomplish this task. Using this technique, both small-signal equivalent circuit and substrate network of Si/ SiGe HBT can be accurately extracted.

In summary, modeling and characterization of various silicon RF devices have been successfully implemented. The main contribution includes new direct extraction techniques which are proposed and developed for on-chip spiral inductor, balun and varactor along with appropriate test structures. Other contribution includes design and characterization of differential symmetrical spiral inductors, and their implementation and optimization in RFIC design. For active devices, a direct extraction technique and new test structures for the small-signal equivalent circuit of Si/ SiGe HBT are also developed.

The techniques developed here have been employed in RFIC design and optimization. The emphasis is on Inductor Capacitor Voltage Controlled Oscillator (LC-VCO), where a 2.4 GHz CMOS VCO and a 10 GHz Si/SiGe HBT quadrature oscillator have been designed, fabricated, and tested.

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List of Acronyms

A-MOS Accumulation-MOS

BiCMOS Bipolar Complementary Metal Oxide Silicon

BSIM Berkeley Short-Channel IGFET Model

CMOS Complementary Metal Oxide Silicon

DUT Device Under Test

EM Electromagnetic

GaAs Gallium Arsenide

GSG Ground-Signal-Ground

HBT Heterojunction Bipolar Transistor

IC Integrated Circuit

InP Indium Phosphide

ISM Industry, Scientific and Medical

ISS Impedance Standard Substrates

LNA Low Noise Amplifier

LC Inductor-Capacitor

LC-VCO Inductor Capacitor Voltage Controlled Oscillator

MIM Metal-Insulator-Metal

MEMS Micro Electro Mechanical Systems

MMIC Microwave Integrated Circuit

MOS Metal Oxide Silicon

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NMOS N-type Metal Oxide Silicon

PMOS P-type Metal Oxide Silicon

RF Radio Frequency

RF-CMOS Radio Frequency Complementary Metal Oxide Silicon

RF-MEMS Radio Frequency Micro Electro Mechanical Systems

RFIC Radio Frequency Integrated Circuit

Si Silicon

SiO₂ Silicon Dioxide

SiGe Silicon Germanium

SOC System On Chip

SOLT Short-Open-Load-Through

VCO Voltage Controlled Oscillator

VCVS Voltage Controlled Voltage Source

VNA Vector Network Analyzer

List of Symbols

δ	skin depth
ϵ_0	vacuum permitivity, $(8.85 \times 10^{-12} F/m)$
ϵ_{SiO_2}	relative permitivity of Silicon Dioxide (SiO_2), (3.9)
$\mu_{0,Al}$	permeability of aluminum, $(4 \cdot \pi \times 10^{-7} H/m)$
$\mu_{r,Al}$	relative permeability of aluminum, (1)
ρ_{Al}	resistivity of aluminum, $(2.65 \mu\Omega - cm)$
ω	frequency radian
ϕ_{jpn}	junction built-in voltage
C_{jpn0}	junction capacitance at zero bias for pn-junction capacitor
C_m	A-MOS capacitance
C_{m0}	capacitance at applied voltages, V_{m0}
C_{m1}	capacitance at applied voltages, V_{m1}
C_{pn}	pn-junction capacitance in its reverse biased condition
d_a	average diameter of the spiral inductor
d_i	outer diameter of the spiral inductor
d_r	fill ratio of the spiral inductor

d_o	outer diameter of the spiral inductor
f_{osc}	oscillation frequency
gm	transconductance
g_{LC}	transconductance of the Inductor-Capacitor (LC) tank
I_c	common mode current
I_d	differential current
L_{se}	single-ended mode inductance
L_{diff}	differential mode inductance
Q_{se}	single-ended mode quality factor
Q_{diff}	differential mode quality factors
Q_o	quality factor due to conductance loses only
R_{sq}	sheet resistivity
V_c	common mode voltage
V_d	differential voltage
V_{sw}	voltage swing of the VCO
$S_{11,12,21,22}$	S-parameters for two-port network
$S_{cc,cd,dc,dd}$	S-parameters for mixed-mode two-port network
S_O	S-parameters for open dummy
S_S	S-parameters for short dummy
S_{TS}	S-parameters for test structure

V_{jpn}	applied reverse voltage for pn-junction capacitor
V_{jm}	applied voltage for A-MOS capacitor
w	metal width
$Y_{11,12,21,22}$	Y-parameters for two-port network
Y_{active}	Y-parameters of the HBT active network
Y_{DUT}	Y-parameters for Device Under Test (DUT)
Y_{ext}	extrinsic two-port Y-parameters
Y_{hbt}	Y-parameters of the HBT network
Y_{OS}	Y-parameters for open-dummy after subtraction of parasitic in series
$Y_{pad-sub}$	Y-parameters of the HBT substrate and pad parasitics network
Y_{sub}	Y-parameters of the HBT substrate network
Y_{TSS}	Y-parameters for test structure after subtraction of parasitic in series
$Z_{11,12,21,22}$	Z-parameters for two-port network
Z_{cal}	calculated two-port Z-parameters
$Z_{cc,cd,dc,dd}$	Z-parameters for mixed-mode two-port network
Z_{diff}	differential input impedance
Z_{hbt}	Z-parameters of the HBT network
Z_{OS}	Z-parameters for open-dummy after subtraction of parasitic in series

Z_{mea}	measured two-port Z-parameters
Z_{se}	single-ended input impedance
Z_{sub}	Z-parameters of the HBT substrate network
Z_{TSS}	Z-parameters for test structure after subtraction of parasitic in series

Chapter 1

Introduction

This chapter briefly surveys the general background, motivation, major contribution and objective of this research project. In addition, the basic organization of this thesis is outlined at the end of the chapter.

1.1 Motivation

Advances in silicon devices have led to significantly higher demand for low-cost applications in various areas, such as wireless or wired communications. At the system level, attempts are routinely made to provide and establish new standards that match the capability of these devices. A famous exemplary case is Bluetooth, which is dedicated for CMOS implementation. Often system level development requires feedback from the device level to fully optimize the system performance.

At the same time, the device development should also be aligned with the system specifications. Thus, it is clearly wise to recognize that the study of RFIC is important in providing a fuller understanding of the devices, circuits and capabilities of a low-cost silicon process in high performance wireless communication applications. Both system and device developments finally converge at the circuit level, which implements the system using an appropriate device. A few iterations are thus required to bring the system and device developments together to fully optimize the circuit design. Fig. 1.1 depicts the link between system and device developments. On another level, it is clear that circuit design and realization depend largely on the accuracy and

knowledge of the device model and characteristics.

In general, the gap between device and circuit developments needs to be filled. The market-driven industry in this case requires highly accurate, low-cost, and fast model extraction methods. These are the fundamental issues that have motivated the research and analysis reported below. In short, this research acts as a bridge between device modeling and characterization with RFIC design.

Figure 1.1: Convergence of system to device development in RFIC design

This thesis focuses on the modeling and characterization of silicon devices for RF applications. To investigate these devices more efficiently, they are divided into two basic classes – those that are active, such as Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and SiGe HBT, and those that are passive, such as inductors, baluns and varactors. In this broad view, this work will encompass main RF devices in the silicon process and provide the extraction techniques that are generally suitable for concrete and upcoming silicon devices. A variety of related issues in device modeling of silicon devices are also studied and exploited in RFIC design. In this research, device modeling and characterization, as well as RFIC design techniques, are central.

This research is based on the available resources, and targets the new extraction and characterization techniques that can be easily adopted by IC designers during their circuit design process. At the same time, the extracted parameters provide design information to the device engineers. The implementation of the characterized

and extracted devices in RFIC design is also investigated as part of the model validation. This research should be able to draw a more complete picture of a particular silicon device in the RFIC design, as well as contribute to the wider domain of device development.

1.2 Objectives

The objective of this work is to carry out a thorough study of the characterization and modeling of silicon devices for RF applications. This study aims to overcome the limitations inherent in current characterization approaches, and to present and exploit a more effective way to accomplish the modeling of passive and active devices. The work suggests alternative methodologies that are more comprehensive and systematic in modeling and characterizing the silicon devices for RF applications.

The research will concentrate on the following:

1. Device modeling and characterization
 - Passive device: spiral inductor, balun, varactor
 - Active device: SiGe HBT
2. RFIC implementation
 - VCO

1.3 Major Contribution of the Thesis

In line with the objective of this research work, the contributions of the thesis lie mainly in the characterization and modeling of silicon devices for RF applications. These contributions are summarized below and will be further described in detail in the subsequent chapters.

The main contribution of this work includes new direct extraction techniques which are proposed and developed for on-chip spiral inductor, balun and varactor

along with appropriate test structures. Other contribution includes design and characterization of differential symmetrical spiral inductors, and their implementation and optimization in RFIC design. For active devices, a direct extraction technique and new test structures for the small-signal equivalent circuit of Si/SiGe HBT are developed. The techniques developed here have been employed in RFIC design and optimization. The emphasis is on LC-VCO design and optimization. A 2.4 GHz CMOS VCO and a 10 GHz SiGe HBT quadrature oscillator have been designed, fabricated and tested. Their implementations using the extracted equivalent circuits have verified the proposed extraction techniques and test structures.

1.4 Organization of the Thesis

This thesis is organized as follows. A synopsis of basic research issues and a literature survey are presented in Chapter 2. Chapter 3, Chapter 4 and Chapter 5 report on device characterization and modeling for passive and active devices. In Chapter 3, the analysis, design and characterization of symmetrical spiral inductors in single-ended mode and differential mode are discussed. In Chapter 4, the equivalent circuits for modeling on-chip asymmetrical spiral inductor, balun and varactor are presented. Direct extraction techniques to extract the equivalent circuits for a library of passive devices are also described in detail. Parameter extraction for an active device is then presented in Chapter 5. A small signal equivalent circuit with a substrate network for Si/SiGe HBT is discussed. A new test structure with a dedicated direct extraction technique is proposed for Si/SiGe HBT. Finally, Chapter 6 focuses on RFIC implementation. Fully on-chip LC-VCO design and implementation are discussed in this chapter. Chapter 7 presents the conclusions and points to the future work that could be pursued further.

Chapter 2

Research Issues and Literature Survey

A few important research issues in device characterization and modeling in RFIC are brought out and discussed here. As highlighted in Chapter 1, we focus our attention on the spiral inductor, balun, varactor, Si/SiGe HBT, and MOSFET in device modeling and characterization. For RFIC applications, LC-VCO is studied. To keep the thesis brief and concise, fundamental knowledge of these topics is not described in detail and references are made only to the directly related literature.

2.1 Overview

Silicon devices have the advantages of low cost and high integration when compared with other technologies, such as Gallium Arsenide (GaAs), [1, 2, 3, 4, 5, 6]. This technology has dominated in digital, analog and mixed-signal IC applications. Microprocessors using CMOS, for example, are one of the most widely used electronic devices. The recent trend has been to push silicon devices into RF and even microwave applications. Improvements in both communication systems and device levels have contributed to this development.

Unlike board-level implementation using discrete components, direct conversion transceivers are more frequently adopted for full chip realization. A higher integration level is desired in order to reduce the size and cost, but its greater functionality is equally significant. The ultimate goal is to produce a fully integrated IC combin-

ing digital, analog, mixed-signals, and RF circuits on a single chip, which is also regarded as System On Chip (SOC). This approach, however, still needs to maintain low manufacturing cost and high yield, and it should be compatible with existing technology. In other words, it may set certain limitations in the RFIC design using silicon devices.

One of the main drawbacks of silicon devices is their lossy substrate, which limits the quality factor of passive devices [7]. In this case, silicon-compatible processes are proposed to achieve high quality. For instance, Micro Electro Mechanical Systems (MEMS) is aggressively adopted into RFIC, which is always referred to as Radio Frequency Micro Electro Mechanical Systems (RF-MEMS). RF-MEMS technology is used to make passive devices, such as spiral inductors [8] or capacitors [9], with high quality [4]. However, it should be noted that RF-MEMS is limited by its relatively high manufacturing cost and low yield in comparison to standard CMOS and Si/SiGe.

In the improvement of the active device performance in RFIC applications, Bipolar Complementary Metal Oxide Silicon (BiCMOS) is preferred in comparison to CMOS in RF and analog IC design. In this approach, the BiCMOS circuit technique, which is already well established, can be adopted in RFIC design. That is the main reason why the Si/SiGe HBT is becoming popular. More importantly, Si/SiGe HBT can be integrated with the standard digital CMOS baseline process without affecting the CMOS circuit performance. The performance of CMOS is also improved drastically by the advancement of scaling technology. The current process has already moved into 90 nm CMOS, and both 65 nm and 45 nm are expected to be in production soon.

This work is constrained by using only the standard silicon process. Hence, we focus on CMOS and Si/SiGe HBT. RF-MEMS, which requires extra processes, will not be considered in our research.

There are three main issues that will be considered in the study of RF device

modeling and characterization;

- device model development: the discussion mainly focuses on new and physically related equivalent circuits, which are proposed and implemented for circuit analysis and simulation as well as device performance optimization.
- device performance improvement: this concerns various techniques that are employed to improve device performance, either using standard processes or proposing new processes and technology.
- device characterization technique: this mainly concentrates on parameter extraction, where extracted data are used for device performance evaluation.

The device model development and its performance improvement are first reviewed to get a thorough understanding of the device characteristics. This information is important in device modeling and characterization, which is the focus of this project. Based on these studies, the issues that have not been given sufficient attention by prior works are highlighted, and possible research works are then proposed.

2.2 Spiral Inductor

Most proposed equivalent circuits of the spiral inductor are variants of the basic nine elements π -model, [10, 11, 12] as shown in Fig. 2.1. C_{Acp} , L_{Adc} and R_{Adc} illustrate the core elements of the spiral inductor, while $C_{Box}(C_{Cox})$, $C_{Bsub}(C_{Csub})$ and $R_{Bsub}(R_{Csub})$ illustrate the lossy substrate network of the spiral inductor. Secondary effects, such as the skin effect, [13, 14, 15], substrate effect, [16, 17], and mutual coupling, [18, 19], are added to fit the simulated characteristics to the measured characteristics. In some cases, a spiral inductor is configured as an on-chip transformer, and its model is also developed, [20, 21].

Extraction of the circuit elements relies on the parameter fitting process. The fitting process is relaxed if there are more circuit elements in the equivalent circuit.

Figure 2.1: General equivalent circuit for spiral inductor

This is similar to adding more parameters in the numerical fitting process. Complicated equivalent circuits not only increase simulation time, but also may lead to non-physical and non-unique parameter extraction. The fitting process is simpler if a frequency-dependent element is used, but it cannot be adopted in transient simulation. Hence, frequency-independent elements and simple equivalent circuits are always favored.

There are a few popular parameter extraction techniques for the spiral inductor. These are similar to most of the other devices employing analytical solutions [22, 23] or numerical optimization [24, 25, 26, 27]. In [23, 27], only limited shapes of spiral inductor were covered. The use of these approaches is limited, as there are a few known shapes of the spiral inductor, such as square, circular, or polygon. In some of the works, parameter fitting is inevitable to obtain most of the parameters. However, no direct extraction technique has been reported for extraction of the equivalent circuit for spiral inductor. Although the equivalent circuit of the spiral inductor is rather simple compared with active devices, the extraction can be misleading if only a numerical optimization algorithm is used. This is because non-physical and non-unique values are often produced. Hence, direct extraction techniques for equivalent circuits of spiral inductors are worthwhile to pursue. Direct extraction is also important when characterization of many spiral inductors is needed. A simple and effective direct extraction technique should be developed to facilitate the extraction of a group

of spiral inductors with a wide range of device geometries. A technique that has not yet been developed becomes one of the research focuses in this work.

Many techniques and designs have been proposed to improve the performance of the spiral inductor in terms of the quality factor and inductance value, [28]. These techniques aim to reduce the series resistance and environment losses, including substrate loss, for quality factor improvement. By increasing the length or number of turns of a spiral inductor, the inductance value can be increased. Ground shielding is one of the techniques that can be used to reduce the substrate effect, [29, 30, 31]. It is believed that by using a ground shield, the eddy current on the substrate is reduced, thus improving the quality of the spiral inductor.

To reduce the series resistance, multi-layer metals are used to construct the spiral inductor in parallel, [32, 33, 34, 35]. In [33] for instance, the top metal and the underneath metal are connected to form a thicker conductor by shorting both metals using a via array. They implemented this technique for an asymmetrical spiral inductor. By adding the underneath metal, the conductor loss is believed to be reduced, but this increases the coupling effect to the substrate. The effects of the via array between the metals are also uncertain. The symmetrical spiral inductor driven in differential mode can theoretically reduce the substrate effect. This topic, however, has not been studied extensively, and is worth investigating. Multi-layer metals are also connected in series to get a higher inductance value [36, 37, 38]. In [36, 38], the top metal is connected to the lower metal to create a longer conductor, which is a different approach from [33]. Inductance is optimized in [36, 38], while quality factor is optimized in [33].

In practice, spiral inductors with inductance values greater than ten nanoHenrys are rarely reported. Due to the limitations of the standard silicon process, the quality factor improvement of the spiral inductor is actually very small. Some special processes are thus proposed, including RF-MEMS [8, 39], using low resistivity material as the metal layer [40], etching away the substrate [41, 42], increasing the

substrate resistivity [43], and increasing the metal layer thickness [44]. However, special processes are not always compatible with the standard silicon process or still have reliability problems. In [44], manipulation of the metal thickness of a spiral inductor can improve the quality factor by more than 25% to 50%. This is mainly due to the increase of the effective thickness. Another way of increasing the metal thickness in a standard process is to use multi-layer metals. Thus, multi-layer spiral inductor characterization is important, and will be included in this work.

The quality factor improvement of a spiral inductor using these techniques is summarized in Table 2.1. It should be noted that ground shields provide greater improvement than the multi-layer approach when only the standard process is considered. This is mainly because the vias that are used to connect different layers of metal introduce non-negligible resistance.

Table 2.1: Reported performance improvement of various design technique of spiral inductor

Technique	Quality Factor	Improvement
Ground Shield, [29]	7	33%
Multi-layer, [34]	6	10%
RF-MEMS, [8]	20	500%
Special Process, [43]	10	60%

These techniques, however, ignore the spiral inductor's operation when it is adopted in circuits. A spiral inductor that is used in a differential circuit is one example. In this case, the characteristics of the spiral inductor driven in differential mode are worth more attention, as there is no sufficient analysis, nor measured data, to verify these characteristics. At the same time, performance improvement of the spiral inductor using double metals must be investigated to verify the effect of the via array connecting the metals. Both of these verifications should be done on a set of spiral inductors with a wide range of device geometries. This is because single device performance cannot sufficiently represent the overall effects. Large amount of measured data is required to arrive at a more general and robust deduction.

Characterization and parameter extraction for on-chip baluns [20, 21] are always complicated and involved three-port measurement. A simple and efficient parameter extraction technique for the on-chip balun is worth exploring. Three-port measurement can be reduced to two-port measurement by exploiting the symmetrical characteristics of the on-chip balun. Using this method, a two-port measurement is required without an on-chip 50Ω load.

2.3 Varactor

In RFIC applications, a tunable capacitor is required for programmability and tunability. For example, varactor is widely used in VCO design. Varactor is a device whose capacitance can be varied by changing its bias. In other words, a varactor can function as a tunable capacitor. There are two types of varactors available in a standard silicon process, pn-junction varactor and Metal Oxide Silicon (MOS) varactor [45]. Unlike a spiral inductor, a varactor is bias dependent. The capacitance varies with the applied dc bias. This complicates the parameter extraction, since relevant parameters need to be extracted for different bias points.

A pn-junction varactor can be modeled with a standard diode model. For normal utility, the pn-junction varactor is reverse biased. Depletion capacitance is the main component when the pn-junction is reversed biased.

A MOS varactor can be used in either accumulation-mode or inversion-mode, [46, 47, 48, 49, 45, 50, 51]. It has the same structure as the MOS transistor, where the gate is assigned as one terminal and the shorted drain-source-bulk is assigned as another terminal. Modeling a MOS varactor is not as clear-cut as the pn-junction varactor, since its operation involves inversion, depletion and accumulation, while the pn-junction only involves depletion. To model the MOS varactor more easily, a CMOS sub-circuit that uses conventional model, such as Berkeley Short-Channel IGFET Model (BSIM), is proposed as the core of MOS varactor [52, 53, 54]. It is only suitable for standard P-type Metal Oxide Silicon (PMOS) or N-type Metal

Oxide Silicon (NMOS) that are configured as MOS capacitors. It is, however, not suitable for an accumulation-mode varactor that is constructed by inserting NMOS in a n-well. In this configuration, it does not function as either an NMOS or PMOS. A MOS varactor model that employs diode sub-circuit is also implemented with some standard circuit element, such as a Voltage Controlled Voltage Source (VCVS), [55, 56]. This model normally involves many circuit elements and its operation is limited to a narrow range.

The most straightforward implementation of the MOS varactor model is to use an empirical fitting expression [47, 57, 58, 59]. This approach is gaining wider acceptance, and many simulators support this feature. One of the examples is Verilog-A. The fitting process becomes very time consuming if one set of varactors with wide range of device geometries must be modeled because the parameter value ranges are very wide. Thus, direct parameter extraction must be adopted into the MOS varactor equivalent circuit extraction.

In most of the literature, only a single device with specified dimensions is presented with regard to the issues of varactors modeling and characterization. One set of varactors with wide range of device geometries has to be used for characterizing a scalable model for the varactors. Unlike the spiral inductor, where the selection is limited by its area and fixed inductance, the varactor has to be flexible in its capacitance selection. Thus, an accurate and scalable model is inevitable. Direct extraction is preferred in this context in order to provide a reliable library.

2.4 SiGe HBT

There are various techniques and procedures that have been proposed to extract the circuit elements in a Si/SiGe HBT equivalent circuit. The information that is collected from the equivalent circuit is useful for the device engineer to analyze, design and optimize the device. For a device-modeling engineer, these extracted parameters are used for scalable or empirical model development of the device. The equivalent

circuit is then used in the circuit design for simulation or analysis. Thus, parameter extraction for the HBT device has drawn a lot of attention due to its broad implications.

Small signal π -model and T -model equivalent circuits are normally used for HBT device modeling [60]. Various extractions and characterization techniques can be grouped into different categories,

- analytical solution: [61, 62, 63, 64, 65, 66, 60];
- numerical optimization: [67];
- direct extraction: [68, 69, 70, 71, 72, 73, 74, 75, 76];

There are very few extraction techniques with purely numerical optimization for HBT that are reported in the literature. However, most analytical solutions or direct extraction techniques employ numerical optimization algorithm. More often mixed techniques combine three ingredients – the analysis (providing the basic physical equation), direct extraction (extracting parameters from the measured data), and application of numerical optimization to get the best fit. Compared with the numerical optimization algorithm, which is widely available, analytical and direct extraction provide a set of physically meaningful and unique parameters. An analytical solution normally requires geometrical and physical information about the devices, which is usually not available. In this case, direct extraction that requires only measured data is preferred. However, different devices have different equivalent circuits. Thus, they have different sets of circuit equations, and different extraction procedures are required in the extraction procedure. In other words, there is no general solution and these techniques remain a popular research topic.

Substrate effects at the collector of common HBT devices, such as GaAs/ Indium Phosphide (InP) HBT, have not been considered. This is primarily a result of their relatively lossless substrate. This, however, is not the case in the Si/SiGe HBT device, where the substrate is lossy. Inclusion of the substrate network complicates the

parameter extraction process. The pn-junction at the collector is bias dependent, and this makes the extraction of the extrinsic network very complicated. Accurate extraction of this extrinsic network is very important to ensure the accuracy of the intrinsic parameter extraction. A dedicated test structure is thus required for the substrate network extraction. With this new proposed test structure and its relevant extraction procedure, the small signal equivalent circuit for Si/SiGe HBT with substrate network can be extracted accurately. This forms one of the main research topics in this work.

2.5 MOSFET

Any comprehensive study of the modeling and characterization of CMOS active device should include a discussion of MOSFET. It has the advantage of a scaling capability. When the device dimension is scaled down, the performance of the MOSFET transistor is improved in terms of speed, power consumption and area. These performance factors push the researchers to make Radio Frequency Complementary Metal Oxide Silicon (RF-CMOS) device. To properly use the MOSFET in RFIC design, an accurate characterization of the MOSFET transistor is required.

The recent focus of the MOSFET model development is based on generic RF model development [77, 78, 79, 80]. Since MOSFET is fabricated on a lossy substrate, modeling its substrate network is important [81, 82, 83, 84, 85] because it involves the substrate effect on the circuit performance, especially at RF frequency.

MOSFET equivalent circuit extraction approaches include:

- analytical solutions: [86, 87, 88, 89, 90],
- direct extraction: [91, 80].

2.6 LC-VCO

In RFIC, there are actually very few circuit blocks operating at RF frequency, particularly in a transceiver. They are the Low Noise Amplifier (LNA), up/down-converter (mixer), power amplifier, and VCO. We use the VCO as our device test vehicle, since it covers both active and passive devices studied in this work [92].

LC-VCO can be implemented in both CMOS [93, 48, 94, 50, 95, 96, 58, 97, 98] and Si/SiGe HBT [99, 100]. MOSFET has very high input impedance and is thus preferred in oscillator design. However, MOSFET at high frequency normally has larger parasitics. It is in this context that the oscillating frequency tolerance becomes an issue. Si/SiGe HBT, on the other hand, has larger transconductance and is much less parasitic. It can be considered at a frequency higher than 10 GHz.

Some of the observed performance of the on-chip VCO is reported in Table 2.2. History shows that the oscillating frequency increases with the advancement of technology. LC-VCO is widely accepted for RF communication applications since it has better phase-noise performance [101, 102]. It is interesting to note that all the on-chip VCO are fully differential. However, the spiral inductors normally are characterized in single-ended mode, where one of the terminals is terminated. The characteristics of the spiral inductors in differential mode are important and deserve more consideration.

2.7 Chapter Summary

We have looked at the *ad hoc* research work in device modeling and characterization for RF applications, particularly in silicon processes such as CMOS and Si/SiGe HBT. This research work is highly resource dependent, and it is therefore necessary to focus on certain selected topics that could make significant contribution while filling the technology gaps.

Several key issues that should be taken into account in the modeling and charac-

Table 2.2: Reported performance of various VCO design

Reference	Technology	Frequency (GHz)	Phase-noise (dBc/Hz)	Tuning Range
[93]	CMOS, 1.00 μ m	0.90	85@100kHz	–
[48]	CMOS, 0.80 μ m	2.40	118@1MHz	15.0%
[96]	CMOS, 0.25 μ m	10.00	113@600kHz	29.7%
[100]	BiCMOS, SiGe(50GHz, f_T)	2.40	97@100kHz	12.5%
[99]	BiCMOS, SiGe(55GHz, f_T)	12.00	113@10MHz	37.0%

terization of the silicon devices are:

- discrepancies in device characterization and circuit design, [3]
- direct extraction of device equivalent circuit
- less flexibility of device values selection
- lossy silicon substrate modeling and characterization

These issues are investigated in this research and will be discussed. A direct extraction technique is developed as a tool in seeking solutions to the problems in the modeling and characterization of RF devices. Chapter 3 discusses in detail the differential characteristics of the symmetrical spiral inductor with a focus on the common discrepancies in using spiral inductors in differential RF circuits. In Chapter 4, direct extractions of the equivalent circuits for on-chip spiral inductor, balun and varactor are discussed. Active device Si/SiGe HBT and its substrate network extraction are presented in Chapter 5.

Chapter 3

Passive Device Characterization: Spiral Inductor

In standard silicon processes, commonly used passive devices are resistors, inductors, and capacitors. For RF applications, the on-chip spiral inductors and varactors are considered to be the most frequently used devices. We will examine in this chapter¹ the characterization of the on-chip spiral inductor. The work investigates the characteristics and optimization of the symmetrical spiral inductor in both single-ended and differential mode excitation. The characteristics of interest include inductor value, quality factor, peak frequency, and self-resonance frequency. Peak frequency is commonly referred to as the frequency where the quality factor is maximum. Both the single-layer and double-layer inductors were characterized. Spiral inductors that are excited in differential mode and single-ended mode were also characterized for comparison. Optimized symmetrical spiral inductors were fabricated in a standard digital 0.35 μm CMOS process. Experimental results show a 60% to 100% improvement of the quality factor and peak frequency, and simultaneously a 10% to 20% improvement of the self-resonance frequency by exciting the symmetrical spiral inductors in the differential mode, in contrast to the single-ended mode. To further validate the characterized symmetrical spiral inductors, differential spiral inductors were adopted in optimizing a low power and low phase noise fully integrated 2.4 GHz VCO. The

¹Part of the material in this chapter has been published in the journals, [34, 103] and conference proceedings, [104, 105]

VCO achieved a phase noise of -105 dBc/Hz at 100 kHz offset frequency with approximately 4.5 mA. The supply voltage was 3.0 V.

Characterization of the symmetrical spiral inductor is described in this chapter. The 2.4 GHz CMOS VCO design is given subsequently in Chapter 6.

3.1 Introduction

Unlike a RF circuit on the board level, RFIC frequently employs circuits with differential topology. Some examples are differential LNA [106], differential mixer [107], differential LC-VCO [94], etc. In this case, characterization of the spiral inductor in differential mode becomes important. However, there is still a lack of extensive work on this topic that could provide comprehensive analysis of the differential mode spiral inductor involving experimental verification. We employ a mixed-mode S-parameter [108, 109] in the analysis and characterization of the differential mode spiral inductor. It is often insufficient to study the characteristics of only a single spiral inductor in differential mode [110, 111]. Thus, spiral inductors optimized at different inductance values need to be investigated.

A low-cost CMOS process, such as 0.35 μm technology, is attractive for RFIC applications up to 2.4 GHz. One of the limitations of this process is its low quality on-chip spiral inductor. In order to extend the use of 0.35 μm in this frequency range, the quality factor of the on-chip inductor should be improved. The multi-layer inductor is one method commonly adopted for this purpose [33, 36, 38]. The differential mode on-chip inductors were also proposed [110] to improve the quality factor. However, there is still a lack of extensive study on these two methods with sufficient experimental data.

Differential circuits such as VCO excite the symmetrical spiral inductor in differential mode. In such cases, the characteristics of the spiral are different from the single-ended mode and need to be considered for circuit optimization. In this work, we have designed two sets of symmetrical spiral inductors in single-layer metal and

double-layer metal. Their characteristics in both the differential and single-ended mode were verified and compared. The dc inductance of these inductors is in the range of 2 nH to 8 nH with 0.4 nH per step, which covers practical implementation in the gigahertz range. Dc inductance here denotes low frequency inductance. The experimental results imply the optimal use of the symmetrical spiral inductor in this process. High performance VCO can be designed and optimized using these characterized results, as will be discussed in Chapter 6.

3.2 Analysis

As mentioned in Section 2.2, a general spiral inductor equivalent circuit can be represented in Fig. 3.1. The figure is shown here again to illustrate the analytical expression of the equivalent circuit model parameters. For the symmetrical spiral inductor, one can assume that $C_{Box} = C_{Cox}$, $C_{Bsub} = C_{Csub}$, and $R_{Bsub} = R_{Csub}$.

Figure 3.1: General equivalent circuit for spiral inductor

The most important parameter in an equivalent circuit for a spiral inductor is low frequency inductance, which is represented by L_{Adc} in Fig. 3.1. There are a few ways of obtaining the inductance value based on the physical construction of the spiral inductor. One of the solutions is to use an EM simulator. However, computing resources and simulation time increase with the complexity of the EM simulation. At the same time, the EM simulation focuses more on verification of the performance

of the spiral inductor rather than design of the spiral inductor.

The Greenhouse algorithm is popular for inductance calculation [11], but it cannot provide the ease of spiral inductor design by considering the spiral inductor design parameters, such as number of turns n , outer diameter d_o , and inner diameter d_i . In this case, the initial design of the spiral inductor in this work requires a closed form expression for the inductance that includes only the spiral inductor design parameters. The modified Wheeler formula turns out to be the best way of designing the spiral inductor, as it is simple and moderately accurate. It requires only a very few design parameters,

$$L_{Adc} = K_1 \cdot \mu_0 \cdot \frac{n^2 \cdot d_a}{1 + K_2 \cdot d_r}, \quad (3.1)$$

$$d_a = \frac{1}{2} \cdot (d_o + d_i), \quad (3.2)$$

$$d_r = \frac{d_o - d_i}{d_o + d_i}, \quad (3.3)$$

where K_1 and K_2 are spiral inductor layout dependent parameters. There is no prior work indicating the values of K_1 and K_2 for the symmetrical spiral inductors, [112]. Hence, these values must be extracted in this work. For the symmetrical spiral inductors discussed in this section, $K_1 = 2.21$ and $K_2 = 3.55$ were found to be reasonable values for design of the symmetrical spiral inductors. The calculated dc inductance L_{Adc} using (3.1) and the measured dc inductance of the single-layer symmetrical spiral inductor are shown in Fig. 3.2. Only a single-ended excitation mode was applied for this initial guess. Note that even with this simple expression, the maximum error of the calculated values is approximately 10%, which is sufficient for any initial design of the spiral inductor.

The rest of the circuit elements in the equivalent circuit in Fig. 3.1 can also be expressed in the spiral inductor design parameters. The detail design equations are given as below,

$$R_{Adc} = \frac{l_t}{w} \cdot R_{sq}, \quad (3.4)$$

$$C_{Acp} = n_{ov} \cdot w^2 \cdot \frac{\epsilon_{SiO_2} \cdot \epsilon_0}{t_{m4-m3}}, \quad (3.5)$$

Figure 3.2: Measured and calculated (using (3.1)) single-layer symmetrical spiral inductors' dc inductance

where R_{sq} denotes the sheet resistance of the metal, n_{ov} denotes the number of the overlapped sections with metal width w , and t_{m4-m3} denotes the SiO_2 thickness between the overlapped metals. The dielectric is SiO_2 with vacuum permittivity $\epsilon_0 = 8.85 \times 10^{-12} F/m$ and relative permittivity $\epsilon_{SiO_2} = 3.9$.

$$C_{ox} = \frac{1}{2} \cdot l_t \cdot w \cdot \frac{\epsilon_{SiO_2} \cdot \epsilon_0}{t_{m4-sub}}, \quad (3.6)$$

$$C_{sub} = \frac{1}{2} \cdot l_t \cdot w \cdot C_{subu}, \quad (3.7)$$

$$R_{sub} = \frac{2}{l_t \cdot w \cdot G_{subu}} \quad (3.8)$$

where t_{m4-sub} denotes the SiO_2 thickness between the metal and the substrate, C_{subu} denotes the substrate capacitance per unit area, G_{subu} denotes the substrate conductance per unit area, and l_t denotes the total length of the metal strip constructing the spiral inductor.

For a symmetrical spiral inductor with circular shape, one can assume that the

total length is the sum of each turn's perimeter and each crossover segments,

$$\begin{aligned} l_t &= n \cdot \pi \cdot d_a + l_s, \\ l_t &= n \cdot \pi \cdot d_a \end{aligned} \quad (3.9)$$

where l_s is the total crossover segments length. If the crossover segment length is small, the quality factor due to the conductance loss, which serves the minimum quality factor before the maximum quality factor, can be estimated by substituting (3.1) and (3.9) into Q_o),

$$\begin{aligned} Q_o &= \frac{\omega \cdot L_{Adc}}{R_{Adc}}, \\ &= \omega \cdot K_1 \cdot \mu_0 \cdot \frac{n}{1 + K_2 \cdot d_r} \cdot \frac{w}{\pi \cdot R_{sq}} \end{aligned} \quad (3.10)$$

(3.10) was used as an initial guideline for optimizing the quality factor based on the designed dc inductance (3.1). From this simple design equation, one can concluded that the quality factor due to the conductance loss depends on the number of turns n , the fill ratio d_r , the metal width w , and the metal sheet resistance R_{sq} . For a more precise estimation of the quality factor, a more detailed derivation of the quality factor is required, and is described in the next subsection.

3.3 Quality Factor

The quality factor of the spiral inductor is defined as the ratio of the energy stored in the inductor to the energy dissipated in the parasitic components. It can be estimated by dividing the imaginary part with the real part of the input impedance polar equation of the two-port network of the spiral inductor. A physical model of the spiral inductor in Fig. 3.3 [29] was employed for this discussion. It is a simplified equivalent circuit of the nine elements *pi*-model Fig. 3.1. Fig. 3.3 which also represents a simplified equivalent circuit for the single-ended symmetrical spiral inductor.

The relationships between the circuit elements in Fig. 3.1 and Fig. 3.3 are sum-

marized here,

$$\begin{aligned} C_s &= C_{Adc}, \\ L_s &= L_{Adc}, \\ R_s &= R_{Adc} \end{aligned} \quad (3.11)$$

$$R_p = \frac{1}{\omega^2 \cdot C_{ox}^2 \cdot R_{sub}} + \frac{R_{sub} \cdot (C_{ox} + C_{sub})^2}{C_{ox}^2}, \quad (3.12)$$

$$C_p = C_{ox} \cdot \frac{1 + \omega^2 \cdot (C_{ox} + C_{sub}) \cdot C_{sub} \cdot R_{sub}^2}{1 + \omega^2 \cdot (C_{ox} + C_{sub})^2 \cdot R_{sub}^2} \quad (3.13)$$

The main purpose of the equivalent circuit transformation is to reduce the complexity of the following derivations to obtain a direct analysis of the spiral inductor performance measures, such as the quality factor, specifically.

Figure 3.3: Simplified equivalent circuit for spiral inductor

For the circuit network in Fig. 3.3, L_s , R_s , C_s , C_p , and R_p represent the desired inductance, series resistance, feed-forward capacitance, substrate capacitance, and substrate resistance of the symmetrical spiral inductor, respectively. The symmetrical spiral inductor is a fully symmetrical network. Hence, the single-ended² Z_{se} and the differential³ Z_{diff} input impedance can be estimated by,

$$Z_{se} = \frac{1}{Y_{11}}, \quad (3.14)$$

$$Z_{diff} = \frac{2}{Y_{11} - Y_{21}}, \quad (3.15)$$

²The input impedance which is estimated by looking into the network from either port-1 or port-2 and short circuiting the other port.

³The input impedance which is estimated by applying differential signals at port-1 and port-2.

where $Y_{11} = Y_{22}$, $Y_{12} = Y_{21}$, Y_{11} , Y_{12} , Y_{21} and Y_{22} are the Y-parameters of the two-port network. From (3.14) and (3.15), it is clear that it is equivalent to reducing the substrate capacitance by half but increasing the substrate resistance by a factor of two in the differential mode input impedance. The equivalent circuit of the differential symmetrical spiral inductor is depicted in Fig. 3.4. In other words, the substrate losses are greatly reduced.

Figure 3.4: Simplified equivalent circuit for differential symmetrical spiral inductor

The differential mode input impedance, Z_{diff} , can be derived by applying the differential signals at port-1 and port-2, which is illustrated in Fig. 3.4. Let,

$$\begin{aligned} V_d &= V_1 - V_2 \\ I_d &= \frac{I_1 - I_2}{2} \end{aligned} \quad (3.16)$$

$$\begin{aligned} V_c &= \frac{V_1 + V_2}{2} \\ I_c &= I_1 + I_2 \end{aligned} \quad (3.17)$$

$$\begin{aligned} V_1 &= Z_{11} \cdot I_1 + Z_{12} \cdot I_2 \\ V_2 &= Z_{21} \cdot I_1 + Z_{22} \cdot I_2 \end{aligned} \quad (3.18)$$

$$\begin{aligned} V_c &= Z_{cc} \cdot I_c + Z_{cd} \cdot I_d \\ V_d &= Z_{dc} \cdot I_c + Z_{dd} \cdot I_d \end{aligned} \quad (3.19)$$

$$Z_{dd} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \quad (3.20)$$

$$\begin{aligned} Z_{diff} &= Z_{dd} \\ Z_{diff} &= \frac{Y_{22} + Y_{12} + Y_{21} + Y_{11}}{Y_{11} \cdot Y_{22} - Y_{12} \cdot Y_{21}} \end{aligned} \quad (3.21)$$

with, $Y_{11} = Y_{22}$, $Y_{12} = Y_{21}$,

$$Z_{diff} = \frac{2}{Y_{11} - Y_{21}}$$

Similarly, the results can also be obtained from the mixed-mode S-parameters.

For a two-port network, the S-parameters are,

$$\begin{aligned} b_1 &= S_{11} \cdot a_1 + S_{12} \cdot a_2 \\ b_2 &= S_{21} \cdot a_1 + S_{22} \cdot a_2 \end{aligned} \quad (3.22)$$

Based on the two-port S-parameters, the mixed-mode S-parameters are,

$$\begin{aligned} b_d &= S_{dd} \cdot a_d + S_{dc} \cdot a_c \\ b_c &= S_{dc} \cdot a_d + S_{cc} \cdot a_c \end{aligned} \quad (3.23)$$

with subscripts d and c indicating the differential and the common mode term, respectively. The two-port mixed-mode S-parameters in terms of the two-port S-parameters are thus defined as,

$$\begin{aligned}
 S_{dd} &= \frac{1}{2} \cdot (S_{11} - S_{21} - S_{12} + S_{22}) \\
 S_{dc} &= \frac{1}{2} \cdot (S_{11} - S_{21} + S_{12} - S_{22}) \\
 S_{cd} &= \frac{1}{2} \cdot (S_{11} + S_{21} - S_{12} - S_{22}) \\
 S_{cc} &= \frac{1}{2} \cdot (S_{11} + S_{21} + S_{12} + S_{22})
 \end{aligned} \tag{3.24}$$

Since only the differential characteristics are of interest, the differential input impedance can be derived as,

$$Z_{diff} = 2 \cdot Z_0 \cdot \left(\frac{1 + S_{dd}}{1 - S_{dd}} \right) \tag{3.25}$$

Similarly,

$$Z_{diff} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \tag{3.26}$$

The quality factor for both of the cases can be simplified as,

$$Q_o = \frac{\omega \cdot L_s}{R_s}, \tag{3.27}$$

$$Q_{se} = Q_o \cdot \frac{1 - \left(\frac{R_s^2}{L_s} - \omega^2 \cdot L_s \right) \cdot (C_p + C_s)}{1 + \frac{R_s}{R_p} \cdot \left[1 + \left(\frac{\omega \cdot L_s}{R_s} \right)^2 \right]}, \tag{3.28}$$

$$Q_{diff} = Q_o \cdot \frac{1 - \left(\frac{R_s^2}{L_s} - \omega^2 \cdot L_s \right) \cdot \left(\frac{C_p}{2} + C_s \right)}{1 + \frac{R_s}{2 \cdot R_p} \cdot \left[1 + \left(\frac{\omega \cdot L_s}{R_s} \right)^2 \right]}, \tag{3.29}$$

where ω is the radian frequency, and L_s , R_s , C_s , R_p , and C_p represent the components as shown in Fig. 3.3 and Fig. 3.4. Q_o is the quality factor due to the conductance losses only. Q_{se} and Q_{diff} are the single-ended and the differential mode quality factors, respectively, which also take the substrate losses into consideration. In the extreme case, C_s and R_p can be ignored in both Fig. 3.3 and Fig. 3.4. The quality factor can be further simplified as (3.30) and (3.31), which only includes the low-frequency effects,

$$Q_{se} = Q_o \cdot (1 - \omega^2 \cdot L_s \cdot C_p), \tag{3.30}$$

$$Q_{diff} = Q_o \cdot \left(1 - \omega^2 \cdot L_s \cdot \frac{C_p}{2} \right). \tag{3.31}$$

By inspecting (3.30) and (3.31), we expect an improvement in the maximum quality factor and the peak frequency of the differential mode spiral inductor of at least 40%. For a spiral inductor with small inductance, the peak frequency happens to be at high frequency. At these frequencies, the second term of the numerator in (3.28) and (3.29) is much larger than one and cannot be neglected. Hence, a factor of two is expected in the improvement of the maximum quality factor and the peak frequency.

At low frequency, the series resistance is the main parasitic component. Hence, a parallel metal layer was added to the symmetrical spiral inductor to reduce the series resistance, R_s . In other words, the symmetrical spiral inductor conductor thickness is increased. However, this also increases the other parasitic effects, such as feed-forward capacitance, C_s , and oxide capacitance, C_p . The finite resistance of the via is also non-negligible. This trade-off was verified in Section 3.5.

3.4 EM Simulation

In routine practical design, the silicon area is always determined first. In a confined area, the inductor value is first specified and then its quality factor is optimized. The outer diameter is determined by the given area, and the inductance value depends on the number of turns. Analytical closed-form expressions, which have been described in the previous subsection (3.1), (3.4), (3.5) and (3.10) for the equivalent circuit parameters, were employed as a general guidelines. For small values of inductance, a wide metal is preferred in order to reduce R_s , while the C_p is negligible. However, for a large value of inductance, C_p becomes significant and the metal width should be kept minimal. In general, for differential inductors, C_s should always be minimized by maximizing the metal spacing. By adhering to these general design rules, the spiral inductors were designed and optimized. EM simulators such as ASITIC, [10] and Momentum [113] were used for fine tuning and providing the general layout of the spiral inductor.

Figure 3.5: Snapshot of symmetrical spiral inductor layout in ASITIC

The simulated performances in comparison with the measured performance of the symmetrical spiral inductors based on ASITIC were included here for references. EM simulation procedure using ASITIC is summarized here,

1. Technology information is prepared as technology parameters in ASITIC. The technology file contains specific parameters such as layer thickness, sheet resistance, and dielectric constant for various layers. The details of the parameters are shown in Fig. 3.11.
2. Spiral inductor dimensions, such as spiral radius, metal width, metals spacing, number of turns, and metal layers used, which are specified in Table 3.1, are used as the design parameters in ASITIC to design the inductors. One of the snapshots of the spiral inductor in ASITIC is shown in Fig. 3.5.
3. EM simulation is performed to estimate spiral inductor performances, such as low frequency inductance, quality factor, peak frequency, and self-resonant frequency. A specific command is used to calculate the two-port parameters of the spiral inductor using EM analysis.

The EM simulations of the spiral inductors were performed before fabrication of the spiral inductor. These simulated results were used as a general guideline for the spiral inductor design. After fabrication and measurement, the EM simulated performance of the spiral inductors were compared to the measured performance. The discrepancies between the EM simulated and measured characteristics were used to modify the EM simulation tool input parameters to further reduce these discrepancies. The input parameters can be modified to get a closer match between the EM simulated and measured characteristic for a particular spiral inductor. However, it was found that the EM simulators cannot provide a good match to the measured characteristic of the entire library of spiral inductors. An example of simulated EM and measured dc inductances are shown in Fig. 3.6 to show these discrepancies increase with the sample indices. This shows the limitation of the EM simulators. Thus, this thesis has chosen the measured characteristics as a reference in comparison with the simulated characteristics from the extracted equivalent circuit. In addition to the dc inductance, the maximum quality factor, and the peak frequency as well as the self resonant frequency are also shown in Fig. 3.7, Fig. 3.8, and Fig. 3.9, respectively.

Figure 3.6: Measured and EM simulated symmetrical spiral inductor dc inductance

One of the reasons for the discrepancies between simulated and measured per-

Figure 3.7: Measured and EM simulated symmetrical spiral inductor quality factor

Figure 3.8: Measured and EM simulated symmetrical spiral inductor peak frequency

Figure 3.9: Measured and EM simulated symmetrical spiral inductor self resonant frequency

formance of the symmetrical spiral inductors is that the via array characteristic is **simplified in the EM simulation**. The vias that connect the top and underneath metals were not able to be simulated accurately in this case. In ASITIC, "Vias are supported in a limited fashion. The capacitance and magnetic coupling between vias is ignored. Only the resistance and inductance of vias is included in the analysis" (Quoted from the ASITIC manual). Momentum, which is a 2.5D EM simulator, was also used to simulate the symmetrical spiral inductors. However, the number of via ranges from a few hundred to a thousand depending on the number of turns of the symmetrical spiral inductor, and the EM simulation for them in the spiral inductor cannot be done in this case due to limited computing resources. For instance, the number of via for the symmetrical spiral inductor with Sample Index-17 is 12,288. A snapshot of the symmetrical spiral inductor with Sample Index-17 is shown in Fig. 3.10.

These discrepancies may be caused by a different ground location in the simulation and the measurement setup. In the EM simulation, the ground is just below the spiral inductor, but the location of the ground in the measurement depends on the test structure layout.

However, ASITIC can still give a general guideline for symmetrical spiral induc-

tor design. There are no stringent requirements for computing resources and simulation time using ASITIC, as compared with other EM simulation tools. Hence, only ASITIC is used and its simulated results were presented in this work.

Figure 3.10: Snapshot of double-layer symmetrical spiral inductor layout

3.5 Characterization

The symmetrical spiral inductors were optimized by referring to (3.29) and (3.31). In differential mode, the dielectric losses, represented by C_p and R_p , are greatly reduced compared to the single-ended mode. Thus, we have a larger margin in which to optimize the symmetrical spiral inductor by minimizing the conductance losses represented by R_s , which could maximize the Q_o (3.10), (3.27).

The characteristics of the spiral inductor largely depend on the technology used. The symmetrical spiral inductor is depicted in a cross-sectional view (Fig. 3.11) that summarizes essential technology information such as thickness, resistivity, and relative permittivity for each metal and insulator layer. Only the top metals (Metal-4, and Metal-3) were used to minimize the substrate loss. Hence, only Metal-4 and Metal-3

Figure 3.11: Cross-sectional view of the symmetrical spiral inductor

were shown. In this $0.35\mu\text{m}$ CMOS process, there are four metal layers.

There are at least two major limiting factors for optimizing the performance of these symmetrical spiral inductors, (i) metal thickness and (ii) substrate resistance. The metal thicknesses are only $1.00\mu\text{m}$ and $0.70\mu\text{m}$. This limits the Q_o as the dc resistance cannot be reduced. The substrate resistance is only $10\Omega\text{-cm}$, and a large substrate loss is expected. We cannot change these two design values in the design of the spiral inductor with a standard process.

Only the top metals were used to minimize the substrate parasitic. Double-layer spiral inductors were created by adding a parallel metal under the top metal with similar geometry and dimension. This was intended to reduce the conductor resistance. Fig. 3.12 and Fig. 3.13 illustrate the three-dimensional views for both the single-layer and double-layer symmetrical spiral inductors. It is shown that both metal layers are connected with a large number of via arrays.

The dimensions of the symmetrical spiral inductor are listed in Table 3.1, where each of the sample indices represents one single-layer and its duplicated double-

Figure 3.12: Simplified three-dimensional view of a single-layer symmetrical spiral inductor

Figure 3.13: Simplified three-dimensional view of a double-layer symmetrical spiral inductor

layer symmetrical spiral inductor. A microphotograph of the test structures is shown in Fig. 3.14. The symmetrical spiral inductors were fabricated in standard digital CMOS $0.35\mu\text{m}$ process with 4-metal layers.

Table 3.1: Dimension of symmetry spiral inductors

Sample Index	Outer Diameter (μm)	Metal Width (μm)	Metals Spacing (μm)	No. of Turns
1	265	20.0	4.6	3
2	265	16.7	2.0	3
3	285	20.0	3.8	4
4	285	19.0	2.0	4
5	285	19.2	2.0	5
6	285	17.5	2.0	5
7	285	16.0	2.0	5
8	285	14.6	2.1	5
9	285	13.6	2.0	5
10	285	12.4	2.1	5
11	285	11.5	2.0	5
12	285	10.5	2.1	5
13	285	9.8	2.1	5
14	277	11.0	2.4	6
15	280	11.0	2.2	6
16	280	10.0	2.4	6
17	280	10.0	2.1	6

3.6 Measurement Setup

The S-parameter measurements were performed to characterize the symmetrical spiral inductors, and test structures were prepared for this purpose. The pads of the test structures were configured in a Ground-Signal-Ground (GSG) configuration of each port for two-port S-parameter measurements. The S-parameter measurements were carried out using a two-port network analyzer. The network analyzer performed Short-Open-Load-Through (SOLT) calibration using Cascade Microtech's Impedance Standard Substrates (ISS) before the S-parameter measurement to bring the measurement plane to the test structure (to the pads). The silicon wafer was made of backside metal. The inductor characteristics extracted from the S-parameter mea-

Figure 3.14: Microphotograph of symmetrical spiral inductor test structures (physical size: 1000 μm $\times$ 1200 μm)

measurements were de-embedded by using the open and short dummies de-embedding procedure before extraction. Fig. 3.15 shows an illustration of the circuit network for the DUT test structure, the open dummy, and the short dummy.

The measurement procedure is summarized here:

1. Calibration of the network analyzer with SOLT
2. Measurement of test structure (S_{TS}), open dummy (S_O), and short dummy (S_S)
3. Conversion of the measured S-parameters of the test structure to Z-parameters

$$S_{TS} \text{ to } Z_{TS}, \quad (3.32)$$

$$S_O \text{ to } Z_O, \quad (3.33)$$

$$S_S \text{ to } Z_S, \quad (3.34)$$

4. Subtract the known parasitic (in series) of the short dummy

$$Z_{TSS} = Z_{TS} - Z_S, \quad (3.35)$$

$$Z_{OS} = Z_O - Z_S, \quad (3.36)$$

5. Convert the above Z-parameters to Y-parameters

$$Z_{TSS} \text{ to } Y_{TSS}, \quad (3.37)$$

$$Z_{OS} \text{ to } Y_{OS}, \quad (3.38)$$

6. Subtraction of the known parasitic (in parallel) of the open dummy (which itself is de-embedded from the parasitic of the short dummy)

$$Y_{DUT} = Y_{TSS} - Y_{OS}, \quad (3.39)$$

The above mentioned procedure also explains how the spiral inductor Y-parameters are de-embedded from the measured S-parameters.

Figure 3.15: Two-port S-parameters test structure with open dummy and short dummy.

3.7 Measurement

Microphotographs of two test structures of the symmetrical spiral inductor are shown in Fig. 3.14. Open-dummy and short-dummy were both employed for the de-embedding procedure. The details of the measurement procedure have been described in Subsection 3.6. The characteristics of the symmetrical spiral inductor were estimated from a measured two-port S-parameter. However, to take into consideration the mismatch as well as the measurement error between port-1 and port-2, (3.14) and (3.15), are re-defined as

$$Z_{se} = \frac{1}{2} \cdot \left(\frac{1}{Y_{11}} + \frac{1}{Y_{22}} \right), \quad (3.40)$$

$$Z_{diff} = \frac{(Y_{11} + Y_{22} + Y_{12} + Y_{21})}{(Y_{11} \cdot Y_{22} - Y_{12} \cdot Y_{21})}. \quad (3.41)$$

These reformulations take into account the average values of port-1 and port-2. Consequently, a standard conventional estimation method of spiral inductor values

and quality factors can then be employed:

$$Q_{se} = \frac{\text{imag}(Z_{se})}{\text{real}(Z_{se})}, \quad (3.42)$$

$$Q_{diff} = \frac{\text{imag}(Z_{diff})}{\text{real}(Z_{diff})}, \quad (3.43)$$

$$L_{se} = \frac{\text{imag}(Z_{se})}{\omega}, \quad (3.44)$$

$$L_{diff} = \frac{\text{imag}(Z_{diff})}{\omega}, \quad (3.45)$$

where Z_{se} and Z_{diff} are defined as in (3.40) and (3.41), L_{se} , and L_{diff} are respective measurements of the single-ended mode and differential mode inductance.

Measurements were carried out to check if the asymmetry of the symmetrical spiral inductor at port-1 and port-2 is negligible. One of the S-parameters of the symmetrical spiral inductor is plotted in Fig. 3.16. It can be seen that the asymmetry is indeed negligible as $S_{12} = S_{21}$, and $S_{11} = S_{22}$.

3.8 Discussion

The measured dc inductances of the symmetrical spiral inductors are in the range of 2.0 nH to 8.0 nH with 0.4 nH per step. Fig. 3.17 shows the plot of the dc inductor value versus the sample index. The single-layer and the double-layer spiral inductors have almost the same dc inductor value. Fig. 3.17, Fig. 3.18, Fig. 3.19 and Fig. 3.20 show the measured spiral inductor characteristics, dc inductance, maximum quality factor, peak frequency, and self resonant frequency, versus the sample indexes.

Table 3.1 shows the metal widths, which are in the range of $10\mu m$ to $20\mu m$. The double-layer spiral inductors show less than 10% improvement in quality factor when the metal width is about $10\mu m$. Fig. 3.21, Fig. 3.22, and Fig. 3.23 show the respective measured series inductance, series resistance, and oxide capacitance (in single-ended excitation mode). For the sake of discussion, only three samples were depicted, but these have been selected from and represent the range of the larger universe of samples. Although the series resistance is reduced by using double-layer

(a) Forward Gain: S_{21}

(b) Reflection Coefficient: S_{11}, S_{22}

Figure 3.16: S-parameters for symmetrical spiral inductor (Index-17) (50MHz - 20GHz)

Figure 3.17: Dc inductance

Figure 3.18: Maximum quality factor

Figure 3.19: Peak frequency

Figure 3.20: Self-resonance frequency

metal, the oxide capacitance is increased. This drawback is illustrated in Fig. 3.22 and Fig. 3.21. In other words, if the single-layer spirals were already optimized for the quality factor, adding a parallel metal underneath introduces mainly parasitic effects. Consequently, the peak frequency and the self-resonance frequency of the double-layer spiral inductors are degraded, as evident in Fig. 3.19 and Fig. 3.20.

Figure 3.21: Measured low frequency series inductance for single-ended symmetrical spiral inductor

For the symmetrical spiral inductors with a sample index higher than 4, we noticed an improvement of about 60% in the maximum quality factor and the peak frequency when the symmetrical spiral inductors are used in differential mode. This is shown in Fig. 3.18 and Fig. 3.19. The improvement is about 100% for symmetrical spiral inductors with a sample index below 5. These values are reasonable compared with the predicted values reported in Subsection 3.2, where the improvement in the substrate resistance is totally neglected. Hence, the symmetrical spiral inductor can be used in a higher frequency range with a clearly higher quality factor. As depicted in Fig. 3.19, the peak frequency of the symmetrical spiral inductors with inductance more than 4 nH improves from 2.0 GHz to more than 3.0 GHz.

This observation leads to a further important implication, namely that a larger

Figure 3.22: Measured low frequency series resistance for single-ended symmetrical spiral inductor

Figure 3.23: Measured low frequency oxide capacitance for single-ended symmetrical spiral inductor

value of inductance can be chosen for circuit optimization. If we normally only consider the single-ended mode characteristics, the smaller value of inductance (<4 nH) is routinely preferred as its quality factor and peak frequency are higher. However, the design is not optimum if we are only considering single-ended mode characteristics. In the design of on-chip VCO, for example, the phase-noise and the power consumption can be better optimized by using a spiral inductor with a larger inductance value.

The quality factor and the peak frequency are improved dramatically in differential mode. However, there is only a 10% to 20% improvement in the self-resonance frequency for both of the single-layer and double-layer spiral inductors, as shown in Fig. 3.20. The feed-forward capacitance C_s is larger when the excitation signals are in anti-phase. These effects limit the self-resonance frequency in the differential mode.

This experiment leads us to draw two significant deductions. First, it is apparent that the performance of the single-layer and double-layer symmetrical spiral inductor is compatible due to substrate loss. Second, the symmetrical spiral inductor in differential mode has much better characteristics than in single-ended mode. We can thus presuppose these experimental results as a general guideline in symmetrical spiral inductor design and its application using this process. An on-chip VCO was designed to validate the characterized symmetrical spiral inductor and its equivalent circuit. The VCO achieves low power and low phase noise at the specified oscillation frequency by properly optimizing the spiral inductor. The relevant VCO design will be described in detail in Chapter 6.

3.9 Chapter Summary

In this chapter, the characterization of symmetrical spiral inductor has been covered in detail. Comprehensive analysis and comparison of the symmetrical spiral inductor characteristics are given for single-layer and double-layer inductors in single-ended

mode and differential mode. A complete library characterization of a differential mode symmetrical spiral inductor has been reported with a large number of experimental results. This work has been referred to as one of the major works on the symmetrical spiral inductor in [114, 115, 116, 117, 118]. It is worthwhile to mention here that the library of symmetrical spiral inductors was designed and optimized at their respective dc inductance values. The results and conclusions from these characterizations were adopted in the design of various RFIC [34, 105, 119, 120] and spiral inductors [114]. One kind of RFIC design, VCO, will be described in Chapter 6.

Chapter 4

Passive Device Modeling: Direct Parameter Extraction

We will examine in this chapter¹ the modeling of the on-chip spiral inductor and the on-chip balun (transformer), as well as the varactors (pn-junction, A-MOS).

4.1 Conventional Equivalent Circuit for On-chip Spiral Inductor

The spiral inductor has been used for a long time in Microwave Integrated Circuit (MMIC) and RFIC. In recent years, this passive device has been widely implemented in a low-cost silicon substrate such as CMOS and Si/SiGe. Various techniques have been proposed to enhance the performance of the spiral inductor, [29], [110], as well as its modeling, [10]. A frequency-independent equivalent circuit, [11], is the most widely adopted model for both circuit and device design as well as circuit simulation.

There is not yet any extraction method that can fully extract the spiral inductor equivalent circuit without using numerical optimization, [32, 25, 42, 26]. However, the numerical optimization may lead to non-physical parameter values or is only limited to certain device geometries. One of the most important steps in numerical optimization is setting the initial value of the parameter. This technique could be time consuming since a few iterations are needed to achieve reasonable results in the

¹Part of the material in this chapter has been published in the journals, [34, 103] and conference proceedings, [104, 105]

fitting process. This is mainly because normally a wide range of initial values are set to relax the convergence. Failure in setting the proper initial value for the numerical optimization may cause non-convergence. By introducing more circuit elements, it can also help in fitting the parameters, [18]. However, unnecessary computation time in circuit simulation may be required for this kind of equivalent circuit, which involves more circuit elements and electrical nodes. Thus, a simple equivalent circuit is often more attractive in circuit simulation. On the other hand, direct extraction gives unique parameter values for different devices. Thus, direct extraction is very efficient in characterizing a device library.

In this work, we show that by using simple extraction technique and simple equivalent circuit, the spiral inductor with wide range of device geometry can be accurately characterized.

4.1.1 Direct Extraction Technique

Fig. 4.1 depicts the conventional equivalent circuit (single π -model) for the spiral inductor [11]. The equivalent circuit consists of only frequency-independent elements. This equivalent circuit is attractive for circuit simulation as it involves only nine circuit elements and only three internal nodes.

Figure 4.1: Conventional equivalent circuit for spiral inductor

To characterize the spiral inductor at RF frequency, its S-parameter was first measured. The measured two-port S-parameter was then converted to Y-parameters. Us-

ing the Y-parameters, the circuit elements in Fig. 4.1 can be extracted. The measurement setup and the measurement procedure described in Subsection 3.6 were also implemented here for the equivalent circuit extraction. The Y-parameters can be grouped into,

$$Y_A = \frac{1}{2}(-Y_{12} - Y_{21}) \quad (4.1)$$

$$Y_B = Y_{11} + Y_{12} \quad (4.2)$$

$$Y_C = Y_{22} + Y_{21} \quad (4.3)$$

where Y_{11} , Y_{12} , Y_{21} , and Y_{22} are the measured Y-parameters after de-embedding.

Figure 4.2: Test structure of spiral inductor (Inner diameter, $D_I=100\mu\text{m}$, Metal width, $W_M=10\mu\text{m}$, Metals spacing, $S_M=2\mu\text{m}$, No. of turns, $n=4$).

The Y-parameters were grouped in such a way to simplify the extraction process. The entire two-port network can be divided into the core spiral inductor network and the substrate network. The core spiral inductor network is represented by Y_A (L_{Adc} , R_{Adc} , and C_{Acp}). The substrate networks are represented by Y_B (C_{Box} , C_{Bsub} , R_{Bsub}), and Y_C (C_{Cox} , C_{Csub} , R_{Csub}), at port-1 and port-2, respectively. For the symmetrical spiral inductor, [34], the substrate networks at port-1 and port-2 are simplified to be the same. However, for the circular spiral inductor that is not symmetrical in this work, both of the substrate networks at port-1 and port-2 need to be extracted

separately to include the non-symmetrical effects. One of the layouts of the circular spiral inductor is depicted in Fig. 4.2.

The substrate network can be represented in both Z- and Y-parameters [76],

$$Z_{B,C} = \frac{R_{sub}}{1 + \omega^2 R_{sub}^2 C_{sub}^2} - j \frac{1 + \omega^2 R_{sub}^2 (C_{ox} + C_{sub}) C_{sub}}{\omega C_{ox} (1 + \omega^2 R_{sub}^2 C_{sub}^2)}, \quad (4.4)$$

$$Y_{B,C} = \frac{\omega^2 R_{sub} C_{ox}^2}{1 + \omega^2 R_{sub}^2 (C_{ox} + C_{sub})^2} + j \omega C_{ox} \frac{1 + \omega^2 R_{sub}^2 (C_{ox} + C_{sub}) C_{sub}}{1 + \omega^2 R_{sub}^2 (C_{ox} + C_{sub})^2}. \quad (4.5)$$

It is clear that the (reciprocal) real parts of (4.4) and (4.5) are linear functions of ω^2 or $1/\omega^2$, where ω is the operating frequency in radians. In this case, the circuit elements can be extracted from the plots that are described by these linear equations,

$$\frac{1}{\text{real}(Z_B)} = (R_{Bsub} C_{Bsub}^2) \omega^2 + \frac{1}{R_{Bsub}}, \quad (4.6)$$

$$\frac{1}{\text{real}(Z_B)} \frac{1}{\omega^2} = \frac{1}{R_{Bsub}} \frac{1}{\omega^2} + (R_{Bsub} C_{Bsub}^2), \quad (4.7)$$

$$\frac{1}{\text{real}(Y_B)} = \frac{1}{R_{Bsub} C_{Box}^2} \frac{1}{\omega^2} + \frac{R_{Bsub} (C_{Box} + C_{Bsub})^2}{C_{Box}^2}, \quad (4.8)$$

C_{Box} , C_{Bsub} , R_{Bsub} are the circuit elements at port-1 as represented in Fig. 4.1. The same expressions are applied to the substrate network at port-2.

The core spiral inductor network can be expressed in Y-parameters as,

$$Y_A = \frac{R_{Adc}}{R_{Adc}^2 + \omega^2 L_{Adc}^2} + j \omega \left(C_{Acp} - \frac{L_{Adc}}{R_{Adc}^2 + \omega^2 L_{Adc}^2} \right). \quad (4.9)$$

Based on (4.9), direct extraction of the feed-forward capacitance is also possible if the measured frequency is high enough. This is because, $\omega^2 L_{Adc}^2 \gg R_{Adc}^2$, at high frequency, the expression of Y_A , can be reduced to,

$$\text{imag}(Y_A) \omega = (C_{Acp}) \omega^2 - \frac{1}{L_{Adc}}. \quad (4.10)$$

By plotting (4.10), the gradient at high frequency gives the approximated value of C_{Acp} .

In this work, conventional definitions are employed to characterize the spiral inductor, [11]. There are three main characteristics to be measured, effective inductance, L_{se} , effective resistance, R_{se} , and effective quality factor, Q_{se} . These definitions were adopted in the previous Subsection 3.7 using Z_{se} as in (3.44), (3.42). These values are estimated from,

$$R = \text{real} \left(\frac{1}{Y_{11}} \right), \quad (4.11)$$

$$L = \frac{\text{imag} \left(\frac{1}{Y_{11}} \right)}{\omega}, \quad (4.12)$$

$$Q = \frac{\text{imag} \left(\frac{1}{Y_{11}} \right)}{\text{real} \left(\frac{1}{Y_{11}} \right)}. \quad (4.13)$$

We can make an accurate estimation of R_{Adc} and L_{Adc} using (4.11) and (4.12) at low frequency, when the other circuit parameters effects are negligible. This is possible at about one hundred megahertz range when the capacitors are effectively open.

In summary, all nine circuit elements in the equivalent circuit can be accurately extracted, and most were extracted independently of each other. These reduce the extraction errors.

4.1.2 Results and Discussion

The extraction technique was validated with fabricated devices in $0.18\mu\text{m}$ CMOS. There are six metal layers in this process. Two of the uppermost layers, metal-6 and metal-5, were used to construct the spiral inductors. Use of the multi-layer metal is intended to reduce the series resistance and skin effect. It is important to reduce all of these second order effects in order to build a high performance spiral inductor library. Ten different spiral inductors were characterized. The device dimension is listed in Table 4.1.

The open-dummy structure was applied to de-embed the parasitic of the probe pads. Fig. 4.2 shows the test structure of the spiral inductor. The devices were mea-

Table 4.1: Extracted equivalent circuit parameters of different spiral inductors

Dimension	n	L_{Adc} nH	R_{Adc} Ω	C_{Acp} fF	C_{Box} fF	C_{Bsub} fF	R_{Bsub} Ω	C_{Coax} fF	C_{sub} fF	R_{Csub} Ω
$D_I=75\text{ }\mu\text{m}$ $W_M=6\text{ }\mu\text{m}$ $W_S=2\text{ }\mu\text{m}$	3	1.64	3.89	4.43	41.50	21.13	505.90	39.22	15.08	526.00
	4	2.62	5.42	7.41	50.28	26.01	398.20	51.54	16.10	460.70
	5	4.10	6.40	10.66	61.21	29.05	334.00	62.25	20.62	398.50
	6	5.49	7.10	14.31	72.50	37.24	283.20	72.15	22.62	357.40
	7	7.70	8.78	17.13	85.18	41.53	249.60	84.14	24.04	331.10
	3	1.63	3.74	6.88	60.07	21.07	405.00	45.35	23.59	436.30
	4	2.62	4.40	10.90	75.05	24.20	350.90	65.49	34.53	363.00
$D_I=100\text{ }\mu\text{m}$ $W_M=10\text{ }\mu\text{m}$ $W_S=2\text{ }\mu\text{m}$	5	4.10	5.90	16.62	88.42	25.22	297.60	78.15	38.94	270.30
	6	6.05	7.20	20.24	103.40	28.18	262.10	94.65	44.57	229.20
	7	8.65	8.80	26.23	123.70	28.88	237.40	111.00	52.53	202.70

sured from 50 MHz up-to 10 GHz using a Hewlett Packard test set and Cascade Microtech probe system.

As described in Section 4.1.1, all of the parameters in the equivalent circuit can be extracted based on the frequency-dependent characteristics of the circuit elements. With respect to this, the accuracy of the extraction largely depends on the frequency points and the frequency range of the measurement. However, this is not a constraint in the modern RF characterization system, where the accuracy is much improved by adopting computer-aided software, such as IC-CAP [121], Wincal [122].

Fig. 4.3, Fig. 4.4, and Fig. 4.5 illustrate the substrate network extraction of the spiral inductor. The substrate network elements, C_{ox} , C_{sub} , and R_{sub} are extracted from these plots. It is also interesting to note that when the substrate resistance is sufficiently large, [43], the substrate network cannot be extracted with these plots at this frequency range. A linear curve was only observed when these substrate effects are significant. For this series of extraction steps, C_{sub} and R_{sub} can be extracted from both Fig. 4.4 and Fig. 4.3 by measuring their gradient and intercept points. Only values that fulfill both of the plots were used to improve the accuracy. These two values were used to validate the value of C_{ox} that was obtained from Fig. 4.5.

The feed-forward capacitance can also be extracted using the same approach, and can be calculated from the resonant frequency, [32, 42]. Fig. 4.6 illustrates its extraction. However, for spiral inductors having a number of turns below four, as in this work, the resonant frequency is higher than the measured frequency, and thus it cannot be estimated merely by looking for its resonant frequency. In this case, the approach proposed in this work should be applied to extract the feed-forward capacitance. Note that the intercept point of the y-axis in Fig. 4.10 also gives the dc spiral inductor value. L_{Adc} , which was obtained here, can be used to verify the C_{Acp} value.

All extracted circuit elements are listed in Table 4.1 with respect to their geometrical dimensions. The measured characteristics of the spiral inductors were fit

Figure 4.3: Illustration of substrate network extraction (Inner diameter, $D_I=100\mu\text{m}$, metal width, $W_M=10\mu\text{m}$, metals spacing, $S_M=2\mu\text{m}$, No. of turns, $n=4$) with respect to (4.6)

Figure 4.4: Illustration of substrate network extraction (Inner diameter, $D_I=100\mu\text{m}$, metal width, $W_M=10\mu\text{m}$, metals spacing, $S_M=2\mu\text{m}$, No. of turns, $n=4$) with respect to (4.7)

Figure 4.5: Illustration of substrate network extraction (Inner diameter, $D_I=100\mu\text{m}$, metal width, $W_M=10\mu\text{m}$, metals spacing, $S_M=2\mu\text{m}$, No. of turns, $n=4$) with respect to (4.8)

Figure 4.6: Illustration of feed-forward capacitance extraction (Inner diameter, $D_I=100\mu\text{m}$, metal width, $W_M=10\mu\text{m}$, metals spacing, $S_M=2\mu\text{m}$, No. of turns, $n=4$) with respect to (4.10)

very well using the extracted circuit elements. These results are shown in Fig. 4.7, Fig. 4.8, Fig. 4.9, Fig. 4.10, Fig. 4.11 and Fig. 4.12.

Similarly, the extractions were also carried out at port-2, where Y_{22} was used to characterize the spiral inductor. However, it is more common to use these spiral inductors for single-ended applications, [34]. Hence, only single port characterization is shown.

Figure 4.7: Inductor characteristics: effective inductances (Inner diameter, $D_I=75\mu\text{m}$, metal width, $W_M=6\mu\text{m}$, and metals spacing, $W_S=2\mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Analytical expressions for the equivalent circuit element for the spiral inductor were derived and discussed in Subsection 3.2. From (3.1), it is clear that the low frequency inductance is proportional to n^2 . Fig. 4.13 and Fig. 4.14 further verify this approximation. On the other hand, the low frequency resistance of the spiral inductors is shown to be linearly proportional to n in Fig. 4.15 and Fig. 4.16. This was also supported by (3.4). Note that there are a few discrepancies in Fig. 4.15 and Fig. 4.16; these could be a result of the large process variation of via resistance.

Figure 4.8: Inductor characteristics: effective resistances (Inner diameter, $D_I=75\mu\text{m}$, metal width, $W_M= 6\mu\text{m}$, and metals spacing, $W_S=2\mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.9: Inductor characteristics: effective quality factor (Inner diameter, $D_I=75\mu\text{m}$, metal width, $W_M= 6\mu\text{m}$, and metals spacing, $W_S=2\mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.10: Inductor characteristics: effective inductances (Inner diameter, $D_I=100\mu\text{m}$, metal width, $W_M=10\mu\text{m}$, and metals spacing, $W_S=2\mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.11: Inductor characteristics: effective resistances (Inner diameter, $D_I=100\mu\text{m}$, metal width, $W_M=10\mu\text{m}$, and metals spacing, $W_S=2\mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.12: Inductor characteristic: effective quality factor (Inner diameter, $D_I=100\mu\text{m}$, metal width, $W_M=10\mu\text{m}$, and metals spacing, $W_S=2\mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.13: Low frequency inductances versus n^2 (Inner diameter, $D_I=75\mu\text{m}$, metal width, $W_M=6\mu\text{m}$, and metals spacing, $W_S=2\mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.14: Low frequency inductances versus n^2 (Inner diameter, $D_I=100\ \mu\text{m}$, metal width, $W_M=10\ \mu\text{m}$, and metals spacing, $W_S=2\ \mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.15: Low frequency resistances versus n (Inner diameter, $D_I=75\ \mu\text{m}$, metal width, $W_M=6\ \mu\text{m}$, and metals spacing, $W_S=2\ \mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

Figure 4.16: Low frequency resistances versus n (Inner diameter, $D_I=100 \mu\text{m}$, metal width, $W_M=10 \mu\text{m}$, and metals spacing, $W_S=2 \mu\text{m}$ for number of turns, $n=3,4,5,6,7$)

4.1.3 Comparison with Other Techniques

In this subsection, comparisons between our direct extraction technique and other extraction techniques will be discussed to highlight the distinctions.

4.1.3.1 Analytical Technique

It is interesting to find that very recently (during the final thesis revision after examiners' review), a conference paper has been published which presents the analytical expressions for fitting the simulated or measured S-parameter data of spiral inductors [123]. The derived expressions provide optimal values of conventional equivalent circuit in a non-iterative manner. For subsequent discussion, some of the relevant expressions are listed in the following.

Referring to Fig. 4.1, the analytical expressions for the shunt branch at port 1 are

$$R_{Bsub} = \frac{N \sum \omega^4 - (\sum \omega^2)^2}{(\sum \frac{1}{\text{real}(Z_B)}) (\sum \omega^4) - (\sum \frac{\omega^2}{\text{real}(Z_B)}) (\sum \omega^2)} \quad (4.14)$$

$$C_{Bsub} = \sqrt{\frac{R_{Bsub} \sum \frac{\omega^2}{\text{real}(Z_B)} - \sum \omega^2}{R_{Bsub}^2 \sum \omega^4}} \quad (4.15)$$

$$C_{Box} = \frac{-\sum \frac{1}{\omega^2}}{\sum \frac{R_{Bsub}^2 C_{Bsub}}{1 + \omega^2 R_{Bsub}^2 C_{Bsub}^2} + \sum \frac{\text{imag}(Z_B)}{\omega^2}}. \quad (4.16)$$

Similar expressions apply for the shunt branch at port 2. For the series branch, the analytical expressions are

$$R_{Adc} = \frac{(\sum \frac{1}{\text{real}(Y_A)})(\sum \omega^4) - (\sum \frac{\omega^2}{\text{real}(Y_A)})(\sum \omega^2)}{N \sum \omega^4 - (\sum \omega^2)^2} \quad (4.17)$$

$$L_{Adc} = \sqrt{\frac{\sum \frac{1}{\text{real}(Y_A)} - N R_{Adc}}{\sum \omega^2}} R_{Adc} \quad (4.18)$$

$$C_{Acp} = \frac{\sum \frac{\omega^2 L_{Adc}}{R_{Adc}^2 + \omega^2 L_{Adc}^2} + \sum \omega \text{imag}(Y_A)}{\sum \omega^2}. \quad (4.19)$$

In these equations, the summations are performed over N data samples.

Like our direct extraction technique, the above formulas also provide a direct method for estimating the parameter values of conventional equivalent circuit for spiral inductor. However, one should caution that relying heavily on the analytical expressions may simply lead to erroneous results. In our experience with the above formulas, it is found that some of the element values may become non-physical, e.g. negative or complex.

Since data samples often may contain certain errors or outliers, it is advisable to first plot our direct extraction curves and apply linear regression wisely on the plot. Moreover, our direct extraction technique may be extended readily to more advanced equivalent circuits as to be shown in the next section. However, it is impractical or too complicated to derive the corresponding analytical expressions for those circuits.

4.1.3.2 Numerical Optimization Techniques

From the (purely) analytical technique, we proceed to compare with (purely) numerical optimization techniques. There are many general-purpose optimization algorithms available to date, which by themselves constitute another hot area of research. With the aid of Advanced Design System (ADS) simulation software, we have attempted the extractions of circuit parameters using the optimization engines provided therein. Various optimizers have been attempted, including random, gradient, genetic and hybrid optimizers. These optimizers are differentiated by their error

function formulations and search methods. The error function formulation measures the difference between the computed and desired responses. The smaller the value of the error function, the more closely the responses coincide. The search method determines how the optimizers arrive at new parameter values, i.e. how they substitute new parameter values to effect a reduction in the error function value. One may refer to ADS manuals for more details about the optimizers.

Our experience finds that there is no satisfactory optimization methodology yet for direct parameter extraction. Quite often the optimizations may simply fail to provide physical or accurate parameter values, especially when the initial values or their ranges have not been set properly. In some cases, the number of iterations is simply too high and may even exceed more than 2000 or 4000 (especially when using random optimizer). Due to the time-consuming iterations required with no guarantee of closeness in results, we recommend that they should not be adopted from the outset. Instead, they could be exploited at the latter stage to improve the parameter values estimated using our direct extraction technique.

4.1.4 Section Summary

A fully direct extraction technique for the conventional spiral inductor equivalent circuit has been developed and demonstrated in this work. The technique is simple, comprehensive, and accurate. It is easy to incorporate into the extraction routine in characterizing large number of devices, especially in device library development. Since this technique only gives the most basic equivalent circuit for the spiral inductor, a more advanced equivalent circuit and fitting routine can also be added to account for process variation as well as measurement error. Analytical and numerical optimization techniques for parameter extraction have also been discussed. Their shortcomings are highlighted in comparison with the direct extraction technique in this work.

4.2 Advanced Equivalent Circuits for On-chip Spiral Inductor

In this section, more advanced equivalent circuits for on-chip spiral inductors will be discussed. The direct extraction technique will also be extended to extract their circuit parameters.

4.2.1 Limitations of Conventional Equivalent Circuit

The conventional equivalent circuit of the previous section is the most popular model adopted for on-chip spiral inductors to date. However, using this simple 9-element circuit, it is not accurate to model the behavior at frequencies close to the self-resonance frequency or higher. There are several limitations of this circuit which has omitted certain secondary effects (mentioned in Section 2.2) that may become important. In particular, due to the simplistic series loss representation, the skin and the proximity effects are not accounted for. These effects lead to the increase of effective series resistance as the operating frequency increases. Furthermore, losses due to eddy currents induced by the magnetic field in the silicon substrate are not included in the conventional model. Also due to the coupling through the substrate, the effective series resistance starts to decrease rapidly at around the frequency for the maximum Q . Since this frequency is generally chosen as the circuit operation frequency (to exploit the highest performance of inductor), such behavior should be modeled accurately.

To improve the modeling of on-chip spiral inductors that incorporates the aforementioned effects, many variants of the equivalent circuit have been proposed. Although one simple remedy is to use frequency-dependent circuit elements, they are difficult to implement in time-domain simulators such as SPICE. In the following, we shall investigate some advanced equivalent circuits which comprise only frequency independent elements in their models such that they can be easily integrated in SPICE-compatible simulators. Moreover, we shall apply and extend our direct ex-

traction technique above to extract the circuit parameter values in a simple and direct manner.

4.2.2 Transformer-based Equivalent Circuit and Parameter Extraction

Fig. 4.17 shows the equivalent circuit for spiral inductor based on transformer loops [124]. The inductance L_{dc} and resistance R_{dc} in the series branch represent the spiral inductor's series resistance and inductance at dc. The inductance L_{si} and resistance R_{si} simulate the i th transformer loop to account for the frequency-dependent losses. The mutual inductances M_{si} between L_{si} and L_{dc} can be thought of representing the inductive coupling between the spiral metalizations. With only a single loop, the series branch comprises effectively a simple transformer with a resistive load. Each additional transformer loop adds two extra degrees of freedom, which allow for more variability in the frequency response.

Figure 4.17: Transformer-based equivalent circuit for spiral inductor

4.2.2.1 Direct Extraction Technique

For simplicity, let us consider the single transformer loop for the equivalent circuit of Fig. 4.17. We shall extend the direct extraction technique above to deduce the circuit model parameters easily. The extraction of the two substrate networks follows the same procedure as before, whereas the extraction of the series branch with more parameters now calls for further treatment. In particular, we note that the impedance

of the series branch is given by

$$Z_A = R_{dc} + j\omega L_{dc} + \frac{\omega^2 M_{s1}}{R_{s1} + j\omega L_{s1}}. \quad (4.20)$$

At low frequencies, R_{dc} and L_{dc} dominate the impedance of the series branch in the transformer loop model. These dc values can be found by separating the measured impedance data [from the reciprocal of (4.1)] into real and imaginary parts, and extracting the low-frequency asymptotes of both curves.

After obtaining R_{dc} and L_{dc} , the remaining unknowns are extracted by rearranging (4.20) as

$$U \equiv \frac{-\omega^2}{R_{dc} + j\omega L_{dc} - Z_A} = \frac{R_{s1}}{M_{s1}^2} + j\frac{\omega L_{s1}}{M_{s1}^2}. \quad (4.21)$$

By referring to the real and imaginary parts of U at high frequencies, the circuit elements M_{s1} and R_{s1} can be extracted readily. Note that to uniquely determine (4.21), the element L_{s1} can be set arbitrarily as a constant. In our case, it has been chosen as a scaling factor of 1 μH .

4.2.2.2 Comparison and Distinction

The extraction technique described above is a simple and direct method applicable for single transformer model of spiral inductor. In [26], the authors have presented an alternative extraction procedure which is rigorous but more involved. In particular, they first define a rational polynomial T in $j\omega$ which can be written as [26, (20)]

$$T = \frac{1}{U} = \frac{a_0}{b_0 + j\omega b_1} \quad (4.22)$$

$$T[b_0 + j\omega b_1] - a_0 = 0. \quad (4.23)$$

Applying (4.23) to N frequency points results in a set of N complex equations. The resulting overdetermined system is then solved using a matrix eigenvalue equation approach. The components of the resulting eigenvalue vector provide the coefficients of the rational polynomial set forth in (4.22). The rational polynomial is

rewritten in terms of pole p_0 and residue r_0 , which are used to map to the elements [26, (22)]

$$\frac{r_0}{j\omega - p_0} = \frac{\frac{M_{si}^2}{L_{si}}}{j\omega - \frac{R_{si}}{L_{si}}}. \quad (4.24)$$

From the comparison here, one can see that the extraction procedure of [26] calls for many more algebraic operations for involving matrix eigenvalue equation. In contrast, our extraction technique is more direct and simple with no need for solving eigenvalue.

4.2.3 Wideband Equivalent Circuit and Parameter Extraction

Fig. 4.18 shows the wideband equivalent circuit of spiral inductor presented in [125]. The circuit model is different from the conventional model shown in Fig. 4.1 in two main aspects. Firstly, a parallel combination of R_{sub} and C_{sub} has been introduced to account for lateral coupling of the silicon substrate. Secondly, the LR ladder circuit formed by L_{s1} and R_{s1} in parallel to R_{s0} has been used to capture the increase in the series resistance due to both skin and proximity effects at high frequency.

Other circuit elements follow the same as conventional model, i.e. C_{ox} represents the oxide capacitance between the inductor and the substrate; R_{si} and C_{si} are the substrate resistance and capacitance to ground. Note that the original series capacitance C_s that models the capacitive coupling between input and output ports of the inductor has been omitted. This is because there is already another capacitive coupling through the oxide capacitance and moreover, through the substrate capacitance. Thus, the effect of C_s is somewhat redundant and can be neglected.

4.2.3.1 Direct Extraction Technique

With the addition of substrate lateral coupling and LR ladder elements, the wideband equivalent circuit is more difficult to extract as compared to the conventional one. We shall extend the previous direct extraction technique to deduce the circuit model parameters. Assume that one has already obtained the conventional model

Figure 4.18: Wideband equivalent circuit for spiral inductor

of inductor, which is still valid and applicable for frequencies that are not too high. Often some of the parameters remain to be accurate and useful even in the present wideband equivalent circuit.

The series branch comprising inductance and LR ladder can be extracted first from the conventional model using low frequency data. In particular, L_{s0} and $R_{||} = R_{s0} || R_{s1}$ are directly extracted from the real and imaginary parts of Z_A at low frequency limit, when the impedance of L_{s1} is negligible [126]. The LR ladder circuit is described by

$$Z_{LR} = Z_A - j\omega L_{s0} \quad (4.25)$$

$$Y_{LR} = \frac{1}{R_{s0}} + \frac{R_{s1}}{R_{s1}^2 + \omega^2 L_{s1}^2} - j \frac{\omega L_{s1}}{R_{s1}^2 + \omega^2 L_{s1}^2}. \quad (4.26)$$

By plotting the relation

$$\frac{-1}{\text{imag}(Y_{LR})} \frac{1}{\omega} = \frac{R_{s1}^2}{L_{s1}} \frac{1}{\omega^2} + L_{s1}, \quad (4.27)$$

the elements L_{s1} and R_{s1} can be obtained readily. Then R_{s0} is also deduced easily from

$$R_{s0} = \frac{R_{||} R_{s1}}{R_{s1} - R_{||}}. \quad (4.28)$$

Having deduced the series branch represented by y_{series} , we proceed to extract the remaining circuit elements. To that end, C_{ox1} and C_{ox2} may be approximated well by C_{Bsub} and C_{Csub} of conventional model at low frequencies, when the effects of other capacitances are negligible. The oxide together with laterally-coupled substrate network is characterized by

$$[Y_{ox-lat-sub}] = [Y_{inductor}] - y_{series} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (4.29)$$

$$[Z_{ox-lat-sub}] = [Y_{ox-lat-sub}]^{-1}. \quad (4.30)$$

The substrate network itself is characterized by

$$[Z_{lat-sub}] = [Z_{ox-lat-sub}] - \begin{bmatrix} \frac{-j}{\omega C_{ox1}} & 0 \\ 0 & \frac{-j}{\omega C_{ox2}} \end{bmatrix} \quad (4.31)$$

$$[Y_{lat-sub}] = [Z_{lat-sub}]^{-1}. \quad (4.32)$$

Using the parameters of $[Y_{lat-sub}]$, the elements of RC circuits in laterally-coupled substrate network can be estimated as

$$\frac{1}{R_{sub}} + j\omega C_{sub} = \frac{1}{2}(-Y_{lat-sub,12} - Y_{lat-sub,21}) \quad (4.33)$$

$$\frac{1}{R_{si1}} + j\omega C_{si1} = Y_{lat-sub,11} + Y_{lat-sub,12} \quad (4.34)$$

$$\frac{1}{R_{si2}} + j\omega C_{si2} = Y_{lat-sub,22} + Y_{lat-sub,21}. \quad (4.35)$$

Therefore, all parameters of the wideband equivalent circuit for spiral inductor have been extracted directly.

4.2.3.2 Comparison and Distinction

For comparison, we refer to an alternative extraction procedure presented in [126]. Therein, the authors have resorted to a set of analytical formulas for their direct extraction method. Some of the formulas are listed below for discussion. For instance, the elements R_{s0} and R_{s1} are obtained using (4.28) and [126, (3)] in our notations:

$$R_{s0} = R_{||} \frac{(\text{imag}(Z_A) - \omega L_{s0})^2 - R_{||} \text{real}(Z_A) + (\text{real}(Z_A))^2}{(\text{imag}(Z_A - \omega L_{s0}))^2 + (R_{||} - \text{real}(Z_A))^2}. \quad (4.36)$$

In turn, L_{s1} is obtained by solving a quadratic equation [126, (4)]:

$$\begin{aligned} & \left(\text{imag}(Z_A)\omega^2 - \omega^3 L_{s0} \right) L_{s1}^2 - R_{s0}^2 \omega L_{s1} \\ & + \left(\text{imag}(Z_A) - \omega L_{s0} \right) \times (R_{s0} + R_{s1})^2 = 0. \end{aligned} \quad (4.37)$$

Comparing (4.36)-(4.37) and (4.27), it is clear that our direct extraction technique is simpler than their method. There is no need to rely on lengthy analytical formula or quadratic solution for extracting the parameters.

For the remaining circuit elements, the authors of [126] have approximated the impedance of substrate body part at low frequency by neglecting C_{sub} , C_{si1} and C_{si2} as [126, (7)]

$$\frac{1}{\text{real}\left(\frac{1}{Y_{body}}\right)} = \frac{(R_{si1} + R_{sub} + R_{si2})^2 + \omega^2 R_{si1}^2 (R_{sub} + R_{si2})^2 C_{ox1}^2}{\left[R_{si2}(R_{si1} + R_{sub})(R_{si1} + R_{sub} + R_{si2}) + \omega^2 R_{si1}^2 R_{si2} R_{sub}(R_{sub} + R_{si2}) C_{ox1}^2 \right]}. \quad (4.38)$$

Since this formula is somewhat complicated, it is expanded into power series and truncated as

$$\frac{1}{\text{real}\left(\frac{1}{Y_{body}}\right)} \approx \frac{(R_{si1} + R_{sub} + R_{si2})}{R_{si2}(R_{si1} + R_{sub})} + \omega^2 \frac{R_{si1}^3 (R_{sub} + R_{si2}) C_{ox1}^2}{(R_{si1} + R_{sub})^2 (R_{si1} + R_{sub} + R_{si2})}. \quad (4.39)$$

The element R_{si1} is extracted from certain y-intercept under the assumption of $R_{si1} = R_{si2}$, after which it is used to obtain R_{sub} . For the capacitances, similar assumption is made as $C_{si1} = C_{si2}$ for their extraction from the complicated impedance of substrate body part at high frequency, while C_{sub} is obtained based on self-resonance frequency data [126].

From the above discussion, we see that the extraction of laterally-coupled substrate network involves more complicated manipulations and introduces additional approximations and assumptions. Indeed, the assumption of R_{si} and C_{si} being the same for both sides means that the extraction method of [126] is not applicable for cases with asymmetric spiral inductors. In contrast, our direct extraction technique is considerably simpler without involving complicated formulas. It is also applicable to more general inductors with no need for any symmetry assumption.

4.2.4 Section Summary

Thus far, we have described the conventional and some advanced equivalent circuits commonly adopted for on-chip spiral inductors. Our direct extraction technique provides a fast, simple and direct way to estimate their circuit parameters. In the literature, there are other equivalent circuits that are more exotic and comprise many more circuit elements. Some examples include the equivalent circuits that have many transformer loops or are distributed, as well as those that introduce mutual couplings among various inductances [26], [18]. For these circuits, the complete direct extraction of their parameters is not trivial or not possible. However, it is still quite often that the direct extraction technique can be applied partially or in hybrid with other approaches. In particular, it can be exploited together with general-purpose optimization routines for comprehensive equivalent circuits. As mentioned above, general-purpose optimization may sometimes fail to provide physical or accurate parameter values, especially when the initial values or their ranges have not been set properly. In this case, the direct extraction of the conventional or advanced circuits of previous subsections allows one to quickly estimate the initial values and ranges.

4.3 Equivalent Circuit for On-chip Balun

The symmetrical spiral inductor with center tap is also regarded as a balun. It is used as an on-chip transformer for either single-ended to differential or differential to single-ended conversion. In the following text, “balun” is used for discussion.

A direct extraction technique of the equivalent circuit parameters for a three-port balun on a silicon substrate was proposed and developed. The extraction is based on a two-port measurement rather than a three-port measurement by grounding the third port. The use of the on-chip $50\ \Omega$ load is also avoided. Hence, this technique greatly simplifies the measurement and the extraction process. One set of balun that was fabricated in a $0.18\ \mu\text{m}$ standard CMOS process with a single-poly-6-metal was used for the verification. The extracted results were in excellent agreement with the

measured results up to 10 GHz.

4.3.1 Introduction

The balun, one of the RF passive components, is a key component in an LC-VCO, double-balanced mixer, push-pull amplifier, and other RFIC designs. An accurate physical model is essential in the circuit design, circuit simulation, evaluation of the process technology, and optimization of the balun design. Efficient modeling methods for calculating and fitting the model from the balun geometry and process parameters have been recently addressed, [13, 20, 21, 127]. Unfortunately, these process parameters are often not always well-known for the particular modeling situation at hand. Thus, it is useful to directly determine the parameters of a balun equivalent circuit from the measured S-parameters.

In this work, a direct extraction method for the balun was proposed and implemented. Based on the ratio of the self-inductance to its series resistance, it is possible to extract the resistance, inductance, and mutual inductance between two main spirals from the Z-parameters.

Conventionally, a three-port measurement is required to fully characterize this three-port device. In this measurement, the third port must be connected with specified load (normally $50\ \Omega$) when a standard two-port Vector Network Analyzer (VNA) is used. In the standard CMOS process, the quality of on-chip load is very susceptible to parasitic effects. At the same time, its resistance can vary significantly due to the process variations and the temperature change, which have an impact upon the measurement accuracy. To avoid the non-standard three-port calibration procedure as well as the on-chip load, the selected third port was shorted to ground. Hence, the standard two-port measurement can be employed using this new test structure. Together with the direct extraction technique, this measurement setup offers an effective and accurate characterization of the three-port on-chip balun.

Figure 4.19: Microphotograph of balun test structures in 0.18 μm CMOS (physical size: 1300 μm $\times$ 800 μm)

Figure 4.20: Balun equivalent circuit for three-port model

Figure 4.21: Balun equivalent circuit for low frequency model

Figure 4.22: Balun equivalent circuit for high frequency extrinsic model

4.3.2 Theory

The balun microphotograph is shown in Fig. 4.19. The balun equivalent circuit used in the present extraction method is shown in Fig. 4.20, which has three terminals: terminal-1, terminal-2, and terminal-3. The notations of the equivalent circuit elements were labeled based on the terminals and consist of three parts: (i) resistance/inductance, (ii) coupling capacitance, and (iii) substrate effect parasitic. The center tap port is represented by inductance L_1 and resistance R_1 . The main strip is expressed by resistances R_2 , R_3 and inductances L_2 , L_3 , respectively. The mutual inductance between the main strips is described by parameter K . The lumped couplings between ports are represented by capacitances C_{12} , C_{13} , and C_{23} , respectively. The substrate effect parasitics are denoted by oxide capacitances C_{s1} , C_{s2} , and C_{s3} ; substrate capacitance C_{s11} , C_{s22} , and C_{s33} ; and substrate resistances R_{s1} , R_{s2} , and R_{s3} , respectively. The extrinsic pad and the test connection capacitances were de-embedded from the measured S-parameters. In the measurement setup, the center tap port was assigned as port-1 and one of the main spiral output ports was assigned as port-2, while the other port was shorted to ground.

Therefore, the equivalent circuit contains nineteen parameters. The seven parameters, namely, R_1 , R_2 , R_3 , L_1 , L_2 , L_3 , and K were assumed to be frequency independent. Hence, they can be extracted from the measured S-parameters because the capacitances can be neglected in this frequency region.

The seven parameters can be reduced to six unknowns as the ratio $\frac{L_1}{R_1}$ is proportional to the ratio $\frac{L_3}{R_3}$. This ratio can be obtained from low frequency Z-parameters. Once the ratio is known, these seven parameters can easily be extracted from the measured Z-parameters. The mutual inductance ratios of L_1 to L_2 or L_3 were legitimately ignored as they are weakly coupled.

The equivalent circuit of Fig. 4.20 at low frequency can be seen in Fig. 4.21. With

terminal-3 shorted to ground, the Z-parameters were expressed as follows,

$$Z_{11} = R_1 + R_3 + j\omega(L_1 + L_3) \quad (4.40)$$

$$Z_{12} = Z_{21} = R_3 + j\omega(L_3 + M) \quad (4.41)$$

$$Z_{22} = R_2 + R_3 + j\omega(L_2 + L_3 + 2M) \quad (4.42)$$

where, the mutual inductance $M = K \cdot \sqrt{L_2 L_3}$.

The resistances R_1 , R_2 , and R_3 can be extracted by solving the below equations,

$$R_1 = \text{real}(Z_{11} - Z_{12}) \quad (4.43)$$

$$R_2 = \text{real}(Z_{22} - Z_{12}) \quad (4.44)$$

$$R_3 = \text{real}(Z_{12}). \quad (4.45)$$

With the resistances determined, we proceed to focus on solving for the inductances. The ratio as in (4.46) was to be used as an additional condition [18].

$$\frac{L_1}{L_3} = \gamma \cdot \frac{R_1}{R_3} \quad (4.46)$$

The γ depends on the metal sheet resistance, the width of the metal strip, the space between the two strips, and the number of turns of the strip. Here, once the ratio γ was determined based on the above ratio equation, the self-inductances and the mutual inductance were evaluated as follows,

$$L_3 = \frac{\text{imag}(Z_{11})}{\omega} \cdot \frac{\text{real}(Z_{12})}{\gamma \cdot \text{real}(Z_{11}) + (1 - \gamma) \cdot \text{real}(Z_{12})} \quad (4.47)$$

$$M = \frac{\text{imag}(Z_{12})}{\omega} - L_3 \quad (4.48)$$

$$L_1 = \frac{\text{imag}(Z_{11})}{\omega} - L_3 \quad (4.49)$$

$$L_2 = \frac{\text{imag}(Z_{22})}{\omega} - L_3 - 2M \quad (4.50)$$

$$K = \frac{M}{\sqrt{L_2 L_3}}. \quad (4.51)$$

Insofar as the factor K is less than one and the inductance L_1 should be greater than zero, we can obtain the range of γ as

$$0 < \gamma \leq \frac{R_3}{R_1} \left[\frac{\text{imag}(Z_{22}) \cdot \text{imag}(Z_{11})}{\text{imag}(Z_{12})^2} - 1 \right]. \quad (4.52)$$

Based on the extracted resistances and inductances, we can easily calculate the two-port Z-parameters using the equations from (4.40) to (4.42), while terminal-3 was shorted to ground. Its equivalent circuit is shown in Fig. 4.21. In the meantime, the measured two-port balun S-parameters can also be converted into either two-port Y-parameters or Z-parameters. The extrinsic two-port Y-parameters consist of all the couplings between the strips and the substrate parasitic that were obtained by using the measured two-port Y-parameters that subtract the calculated two-port parameters,

$$[Y_{ext}] = [Z_{mea}]^{-1} - [Z_{cal}]^{-1} \quad (4.53)$$

where Y_{ext} is denoted as the extrinsic two-port Y-parameters; Z_{mea} and Z_{cal} are the measured and calculated two-port Z-parameters, respectively.

The extrinsic equivalent circuit is shown in Fig. 4.22. From the above calculation equations, it follows that this equivalent circuit should consist of the coupling between the strips and the substrate parasitic. The coupling capacitances between the two ports can be extracted easily from external Y-parameters, Y_{ext} ,

$$C_{12} = \frac{\text{imag}(Y_{ext12})}{\omega} \quad (4.54)$$

$$C_{13} \approx C_{12}. \quad (4.55)$$

Once the coupling capacitances between the strips were extracted, the coupling capacitances and the resistances between the substrate and the balun, Y_{ext13} and Y_{ext23} , can be extracted by using the substrate extraction technique, which will be discussed in Chapter 5. Y_{ext13} and Y_{ext23} are substrate networks at port-1 and port-2 respectively.

4.3.3 Measurement and Discussion

The extraction algorithm was validated with the fabricated devices. The baluns were fabricated by a conventional commercial foundry 0.18 μm CMOS process that had six metal interconnects on a silicon substrate with a resistance of 10 $\Omega\text{-cm}$. The inductor strip was formed by a top metal layer 6 (M6) with 2 μm thickness, and

metal layer 5 (M5) and metal layer 4 (M4) stacked together with a dense via array to form the underpass. The metal width is $10\text{ }\mu\text{m}$ with $2\text{ }\mu\text{m}$ metal-to-metal spacing. The inner diameter of the balun is $100\text{ }\mu\text{m}$. Three baluns, which have 3, 5, and 7 turns respectively, were measured.

The two-port S-parameters were measured and used for the circuit element extraction. One of the symmetrical ports of the test structure was connected to the GSG test pads and the other was connected to ground. The center tap port was connected to another GSG test pad. The test structure is documented in Fig. 4.19.

Figure 4.23: Measured low frequency resistances for 3-turn balun

The measured S-parameters after de-embedding of open and short test structures were converted into Z-parameters for the resistance extraction. Using (4.43), (4.44), and (4.45), the resistances R_1 , R_2 , and R_3 can be extracted from the real part of Z-parameters. Fig. 4.23, Fig. 4.24, and Fig. 4.25 show the measured resistance values at low frequency for 3-turn, 5-turn, and 7-turn baluns respectively. The resistance is constant over the frequency range. Here, the ratio of R_3 to R_1 can be estimated and these values were used to estimate the ratio of L_3 to L_1 , (4.46). For a fixed value of γ , the self-inductance and the mutual inductances can be extracted, and then the

Figure 4.24: Measured low frequency resistances for 5-turn balun

Figure 4.25: Measured low frequency resistances for 7-turn balun

coupling capacitances and the substrate resistances can be extracted with (4.47) to (4.51).

At these frequency ranges, the skin effect is negligible. Using the resistivity of aluminum, ρ_{Al} , relative permeability, $\mu_{r,Al}$, permeability, $\mu_{0,Al}$, with skin depth, δ , one can approximate the skin depth at 500 MHz,

$$\begin{aligned}\rho_{Al} &= 2.65 \mu\Omega - cm, \\ \mu_{r,Al} &= 1, \\ \mu_{0,Al} &= 4 \cdot \pi \times 10^{-7} H/m, \\ \delta &= \sqrt{\frac{2 \cdot \rho_{Al}}{2 \cdot \pi \cdot f \cdot \mu_{r,Al} \cdot \mu_{0,Al}}} \\ \delta_{500MHz} &= 3.66 \mu m\end{aligned}\tag{4.56}$$

The metal thickness in this case is $2.0 \mu m$, (width more than $10.0 \mu m$), which is nearly half of the skin depth at 500 MHz ($3.66 \mu m$), and thus the resistances are not affected by the skin effect. These resistances were used to extract the dc resistances (low frequency) of the equivalent circuits; thus, only 100 to 500 MHz was required.

If the measured frequency is increased, the skin effect becomes significant and the resistance is increased. Normally, spiral inductors are constructed by the top layer metals in order to reduce conductor loss (because the larger metal cross-section is possible), and to minimize coupling to the substrate. The metal thickness and width are typically on the order of a few microns in each dimension. At a frequency of a few giga-hertz, these dimensions are on the order of skin depth for Aluminum in this technology. For example, $\delta_{1.65GHz} = 2.00 \mu m$, $\delta_{6.75GHz} = 1.00 \mu m$, $\delta_{10.00GHz} = 0.82 \mu m$. This means the current distribution in the conductors will start to change by crowding toward the surface of the line. This current crowding increases the resistance in the inductor.

Fig. 4.26, Fig. 4.27, and Fig. 4.28 show the low frequency inductances, self-inductances, and mutual-inductances for this extraction process. The inductances in this frequency range are also constant. Hence, the relationship in (4.46) was assumed

Figure 4.26: Measured low frequency inductances for 3-turn balun

Figure 4.27: Measured low frequency inductances for 5-turn balun

Figure 4.28: Measured low frequency inductances for 7-turn balun

to be valid at low-frequency.

Fig. 4.29, Fig. 4.30, and Fig. 4.31 show a comparison of the reflection coefficient and the transmission gain between the measured and the simulated S-parameters of the baluns. Note that the equivalent circuit fits the measured data very well up-to 10 GHz. For completeness, the measured and the simulated S-parameters are also plotted in Fig. 4.32, Fig. 4.33, and Fig. 4.34. Both the measured and the extracted results appear to fit very well over the whole frequency range. The main extracted circuit element values of the baluns with different turns are summarized in Table 4.2. Both resistances and inductances increase proportionally with the increase in the number of turns.

In general, for sufficiently small L_1 , γ was approximated as zero, and thus the values of the elements of the equivalent circuit can be directly determined. For other cases where L_1 is significant, γ can be estimated from the specific balun's geometry, [18], since $\gamma = \frac{L_1 R_3}{L_3 R_1}$ can be simplified to only dimensional ratios. With this appropriate initial value of γ , the extraction process converges in a few iterations. In short, the basic process elaborated here is very time efficient. The three-port equiv-

Figure 4.29: Input/output reflection coefficient (S_{11} , S_{22}) and forward/reverse transmission (S_{21}) gain for 3-turn balun

Figure 4.30: Input/output reflection coefficient (S_{11} , S_{22}) and forward/reverse transmission (S_{21}) gain for 5-turn balun

Figure 4.31: Input/output reflection coefficient (S11, S22) and forward/reverse transmission (S21) gain for 7-turn balun

Table 4.2: Extracted circuit elements for different turns of baluns (Metal width=10μm, Metal spacing=2μm, Inner diameter=100μm)

Circuit Elements	Balun		
	3-turns	5-turns	7-turns
$R_1 (\Omega)$	0.845	0.862	0.859
$R_2 (\Omega)$	1.725	2.917	4.370
$R_3 (\Omega)$	1.725	2.917	4.370
$L_1 (nH)$	0.049	0.048	0.043
$L_2 (nH)$	0.727	1.296	2.180
$L_3 (nH)$	0.727	1.296	2.180
K	0.060	0.393	0.596

(a) Forward Gain: S_{12} , S_{21}

(b) Reflection Coefficient: S_{11} , S_{22}

Figure 4.32: S-parameters for 3-turns balun (100MHz - 10GHz)

(a) Forward Gain: S_{21}

(b) Reflection Coefficient: S_{11} , S_{22}

Figure 4.33: S-parameters for 5-turns balun (100MHz - 10GHz)

(a) Forward Gain: S_{21}

(b) Reflection Coefficient: S_{11} , S_{22}

Figure 4.34: S-parameters for 7-turns balun (100MHz - 10GHz)

alent circuit of the balun that is shown in Fig. 4.20, can be obtained by assuming, $C_{s3} = C_{s2}$, $C_{s33} = C_{s22}$ and $R_{s3} = R_{s2}$. This is clearly reasonable since the balun is fully symmetric.

Instead of defining just the absolute and relative errors, the mixed relative and absolute errors can be used to obtain the best fit between measurement and simulation. The optimization error is defined by,

$$\Delta E = \frac{1}{4N} \sum_{i=1}^N \left[\left(\frac{S_{11}^{mea} - S_{11}^{sim}}{S_{11}^{mea}} \right)^2 + \left(\frac{S_{12}^{mea} - S_{12}^{sim}}{S_{12}^{mea}} \right)^2 + \left(\frac{S_{21}^{mea} - S_{21}^{sim}}{S_{21}^{mea}} \right)^2 + \left(\frac{S_{22}^{mea} - S_{22}^{sim}}{S_{22}^{mea}} \right)^2 \right] \quad (4.57)$$

where N is the number of frequency points. The initial value of γ is set to half of the range as in (4.52) and then folds down until a minimum of error was found.

4.3.4 Validation

Validation of the three-port equivalent circuit from the two-port measurement can be done through two two-port S-parameter measurements on two test structures (the terminals described in above are referred to the equivalent circuit shown in Fig. 4.20):

1. Test Structure-1: terminal-1 and terminal-2 were assigned to port-1 and port-2, while terminal-3 was shorted to ground (this validation was described in Section 4.3.3)
2. Test Structure-2: terminal-2 and terminal-3 were assigned to port-1n and port-2n, while terminal-1 was left open

By shorting terminal-3 to ground, a two-port S-parameter measurement and extraction can be easily performed in comparison with a three-port S-parameter measurement. No information is lost in this case as terminal-2 and terminal-3 are in symmetry. The symmetry has been proven and details are given in the next paragraph. Fig. 4.20 shows the equivalent circuit of the three-port balun. The substrate network at terminal-3 (C_{s3} , C_{s33} , R_{s3}) can be replaced with the substrate network

extracted at terminal-2 (C_{s2} , C_{s22} , R_{s2}) due to the fact that terminal-2 and terminal-3 are symmetric. Table 4.2 also shows that $R_2 = R_3$, and $L_2 = L_3$, **which confirmed** that terminal-2 and terminal-3 are symmetric. The validations have been shown in Fig. 4.32, Fig. 4.33 and Fig. 4.34, where the comparisons between the extracted equivalent circuits with the measured results were carried out.

To further validate the extracted three-port equivalent circuit, two-port S-parameter measurements were carried out on a second test structures with terminal-2 and terminal-3 in Fig. 4.20 reassigned to port-1n and port-2n, while terminal-1 was left opened. The two-port S-parameters of the equivalent circuit with terminal-2 and terminal-3 in Fig. 4.20 reassigned to port-1n and port-2n while port-1 was left open and were also simulated and compared with the measured two-port S-parameters. The results are shown in Fig. 4.35, Fig. 4.36 and Fig. 4.37. As expected, port-1n and port-2n are symmetric, as $S_{11n} = S_{22n}$, $S_{12n} = S_{21n}$. At the same time, the simulated equivalent circuit S-parameters match well with the measured test structure S-parameters. With these measurements and comparisons, the results of the extracted three-port equivalent circuit using two-port measurement were validated.

4.3.5 Section Summary

A direct extraction technique of the equivalent circuit for baluns on a silicon substrate was described and validated. In this measurement setup, the three-port measurement was **simplified to two-port without sacrificing accuracy**. Meanwhile, characterization error was improved by avoiding the use of on-chip load. Through the iteration process, the elements of the equivalent circuit can be directly extracted and optimized. The simulated S-parameters fit the measured S-parameters up to 10 GHz for the entire balun under test. In addition to reflecting an efficient computation result, i.e., a unique and accurate solution, this method is clearly both generic and physically based. Moreover, the fact that the extraction technique has been adopted in the design of an on-chip transformer-based feedback oscillator, [128] further verifies the

(a) Forward Gain: S_{12}, S_{21}

(b) Reflection Coefficient: S_{11}, S_{22}

Figure 4.35: S-parameters for 3-turn balun (terminal-2 $\rightarrow$ port-1n, terminal-3 $\rightarrow$ port-2n, terminal-3 $\rightarrow$ open) (100MHz - 10GHz)

(a) Forward Gain: S_{21}

(b) Reflection Coefficient: S_{11}, S_{22}

Figure 4.36: S-parameters for 5-turn balun (terminal-2 $\rightarrow$ port-1n, terminal-3 $\rightarrow$ port-2n, terminal-3 $\rightarrow$ open) (100MHz - 10GHz)

(a) Forward Gain: S_{21}

(b) Reflection Coefficient: S_{11} , S_{22}

Figure 4.37: S-parameters for 7-turn balun (terminal-2 – > port-1n, terminal-3 – > port-2n, terminal-3 – > open) (100MHz - 10GHz)

usefulness of the technique. [129] also employed this extraction technique in their spiral inductor characterization.

4.4 Equivalent Circuit for On-chip Varactor

The capacitor is another important passive device for RFIC applications, and a capacitor with variable capacitance is used for tuning purposes. It is also referred to as a varactor. The varactor is widely used in RFIC where tuning is required, such as in tunable filters, VCO, etc.

Direct parameter extraction of the equivalent circuit for an on-chip varactor was proposed and implemented in this work. Two types of varactor were concentrated upon – the pn-junction varactor and A-MOS varactor. They were implemented in a 0.18 μm CMOS process. Varactors with different numbers of fingers were characterized and used to validate this extraction technique.

Parameter extraction and modeling of the varactor are described in this chapter. The extracted parameters are utilized in Si/SiGe HBT VCO design, which is taken up in detail in Chapter 6.

4.4.1 Capacitance Scaling

There are three types of RF capacitors available in this process: Metal-Insulator-Metal (MIM), pn-junction, and A-MOS. A generic equivalent circuit for an RF capacitor consists of a series of capacitors, resistors, and inductors, as well as the substrate network, Fig. 4.38, [45]. The capacitances of these capacitors are fundamentally different functions of the applied voltage. Port-1 and port-2 represent the top plate and bottom plate of the capacitor, respectively. The design of the capacitor should minimize the substrate effect at the bottom plate. Thus, a simple substrate network is adequate to represent the substrate effect in this equivalent circuit.

The MIM capacitor is independent of the voltage variation, and is therefore not tunable. The pn-junction capacitor in its reverse biased condition is described by the

depletion capacitance as,

$$C_{pn} = \frac{C_{jpn0}}{\left(1 - \frac{V_{jpn}}{\phi_{jpn}}\right)^{m_{jpn}}} \quad (4.58)$$

where C_{jpn0} is the junction capacitance at zero bias, V_{jpn} is the applied reverse voltage, ϕ_{jpn} is the junction built-in voltage, and m_{jpn} is the exponent.

The A-MOS capacitor has two modes of operation: accumulation mode and depletion mode. Its capacitance can be described empirically as [58],

$$C_m = C_{m0} + C_{m1} \cdot \tanh\left(\frac{V_{jm} - V_{m0}}{V_{m1}}\right) \quad (4.59)$$

where C_{m0} , C_{m1} are the capacitance at the applied voltages, V_{m0} , V_{m1} , respectively, and V_{jm} is the applied voltage. These parameters are directly extracted from the measured data. It is scalable and related to its physical characteristics. The expression can be implemented with Verilog-A for circuit simulation, since it is widely supported by circuit simulators such as SPECTRE by Cadence and Advanced Design System by Agilent. Verilog-A also has the advantage of fast and easy implementation compared with other models [52, 53, 51, 59].

Figure 4.38: General equivalent circuit for RF capacitor

4.4.2 Extraction of Varactor Equivalent Circuit

The circuit element values are extracted directly from the measured S-parameters. At different bias voltages, the voltage-dependent circuit element values are different as well. A direct extraction technique should be employed to accurately estimate the

voltage dependent values. Higher accuracy of the extracted values will ease the fitting process to obtain the transfer functions given in (4.58) and (4.59). The extraction technique is described here, and the impedance of the series components in Fig. 4.38 can be described by,

$$Z_a = R_a + j(\omega L_a - \frac{1}{\omega C_a}) \quad (4.60)$$

$$Z_c = R_c - j(\frac{1}{\omega C_c}) \quad (4.61)$$

where all the variables, R_a , R_c , C_a , and C_c are the resistances and capacitances that are delineated in Fig. 4.38.

The imaginary part of (4.60) is rearranged as,

$$\text{imag}(Z_a)\omega = \omega^2 L_a - \frac{1}{C_a} \quad (4.62)$$

$$\text{imag}(Z_a)\frac{1}{\omega} = -\frac{1}{C_a}\frac{1}{\omega^2} + L_a \quad (4.63)$$

where the variables, L_a , and C_a are the inductance and capacitance that are described in Fig. 4.38.

Figure 4.39: Illustration of varactor network extraction, L_a , using A-MOS capacitor with number of fingers, $N_f=104$

Figure 4.40: Illustration of varactor network extraction, C_a , using A-MOS capacitor with number of fingers, $N_f=104$

By plotting $\text{imag}(Z_a)\omega$ versus ω^2 , L_a can be estimated from its gradient. The same approach applies to obtain C_a by plotting $\text{imag}(Z_a)\frac{1}{\omega}$ versus $\frac{1}{\omega^2}$. R_a was simply estimated from the real part of (4.60). This technique is more accurate and of wider-band than the extraction method described in [59], where L_a is calculated at only a single frequency point. R_c and C_c can also be extracted from the real and imaginary parts of (4.61). Fig. 4.39 and Fig. 4.40 illustrate the extraction techniques described here. The gradients in Fig. 4.39 indicate the inductance variations, and the gradients in Fig. 4.40 indicate the capacitance variations. These gradients were extracted and plotted against their applied voltages. The results are shown in Fig. 4.41 and Fig. 4.42 for the pn-junction varactor and the A-MOS varactor.

Fig. 4.41 and Fig. 4.42 show the measured capacitances as a function of the applied voltages. It is worth stressing that the measured data closely fits the simulated transfer functions. These transfer functions can be described in terms of the number of fingers, n , and are thus scalable. What is noteworthy here is that the transfer function can fit very well for both measured and simulated parameters for various numbers of fingers. This shows the results of using the direct extraction technique

Figure 4.41: Pn-junction varactor transfer function for different number of fingers, C_{pn} .

Figure 4.42: A-MOS varactor transfer function for different number of fingers, C_m .

at the initial stage of modeling. The transfer functions were obtained empirically by substituting (4.64), (4.65) into (4.58), (4.59) respectively,

$$C_{pn} = \frac{C_{jpn0}}{\left(1 - \frac{V_{jpn}}{\phi_{jpn}}\right)^{m_{jpn}}} \quad (4.64)$$

$$C_{jpn0} = (5.642n - 2.705) \times 10^{-14}$$

$$m_{jpn} = 0.242$$

$$\phi_{jpn} = 0.663$$

$$C_m = C_{m0} + C_{m1} \cdot \tanh\left(\frac{V_{jm} - V_{m0}}{V_{m1}}\right) \quad (4.65)$$

$$C_{m0} = (2.924n + 6.413) \times 10^{-14}$$

$$C_{m1} = (1.759n + 3.340) \times 10^{-14}$$

$$V_{m0} = -0.110$$

$$V_{m1} = 0.350$$

where the meanings of the variables are already given in (4.58) and (4.59).

The transfer function is practically useful if a varactor with a smaller number of fingers is required, such as $n < 26$ in this case. This is because characterization of a varactor with a small number of fingers cannot be done due to process limitation, large parasitic effects, and basic inaccuracy of measurement. In the design of the Si/SiGe HBT VCO at 10 GHz, for example, the capacitance is about 0.50 pF, with the number of fingers equals to ten.

4.4.3 Section Summary

A direct parameter extraction of the equivalent circuit for the on-chip varactor was proposed, described, and implemented. It has been validated with two types of varactor with a wide range of finger numbers, and the varactors were used in the design of the oscillator. This direct extraction technique can be helpful to the design engineer seeking to build a scalable varactor library. At the same time, this technique is also practically useful in the situation where the given data do not include the desired values.

4.5 Chapter Summary

In this chapter, direct parameter extractions have been covered for passive device modeling including:

1. conventional equivalent circuit for on-chip spiral inductor
2. advanced equivalent circuits for on-chip spiral inductor
3. equivalent circuit for on-chip balun
4. equivalent circuit for on-chip varactor.

For direct parameter extraction of the equivalent circuit for on-chip spiral inductor, a new extraction technique has been proposed which extends the substrate network extraction technique that was developed for Si/SiGe, [76]. The equivalent circuit for the asymmetric spiral inductor with a wide range of device geometries has been extracted to verify this simple and efficient technique. The direct extraction technique has also been extended to more advanced equivalent circuits for spiral inductor. The extraction technique of the substrate network will be further described in Chapter 5.

For direct parameter extraction of the equivalent circuit for on-chip balun, a new test structure and a new extraction technique have been proposed. The results of this work have been adopted in the design of an on-chip power oscillator, [128]. In a recently published work, [129], this extraction technique was also adopted in characterizing the on-chip transformer.

For direct parameter extraction of the equivalent circuit for on-chip varactor, a new extraction technique has also been proposed. It is a generic direct extraction technique for both the pn-junction varactor and the A-MOS varactor. Scalable models have been obtained for both types of varactors. The results of this work have been adopted in the design of an on-chip 10 GHz oscillator, [105].

Chapter 5

Active Device Modeling and Characterization

Active device Si/SiGe HBT is investigated here. We focus on the substrate network extraction and small-signal equivalent circuit extraction in this chapter¹.

A systematic approach to directly extract the equivalent circuit of the HBT, including the substrate network, was proposed, developed, and implemented. All parameters were extracted from the measured S-parameters. The substrate network was accurately extracted by measuring the collector port. Equivalent circuits without the substrate effects can be extracted by systematically analyzing and solving the two-port network equations. This technique was validated with fabricated devices in Si/SiGe HBT technology from 50 MHz to 26.05 GHz. The extracted results are in excellent agreement with the measured results.

5.1 Introduction

Si/SiGe HBT is extremely popular in the ever-growing realm of wireless communication devices. This appeal derives from the simple fact that in the competitive marketplace, their implementation requires low-cost, high performance, and high integration with digital base-band. Accurate device modeling is necessary to fully characterize the designed circuit, especially at high frequency. HBT parameter extraction has been widely discussed in recent literature, [73, 74, 66, 60, 75, 65]. The

¹Part of the material in this chapter has been published in the conference proceeding, [76, 105]

substrate effect at the collector has not been considered in GaAs/ InP HBT. However, due to the lossy substrate, the substrate effect for Si/ SiGe HBT cannot be ignored [130]. It should be accurately extracted and included in the equivalent circuit.

The extraction procedure involves either direct extraction [73, 69], analytical solution [62], or optimization [63], and culminates with solving the equations by reducing the unknowns. In all cases, the package interconnect parasitic has to be removed before the extraction of the core device. To minimize the parasitic effects, especially the substrate parasitic at the collector, the parasitic network should be removed first. Nevertheless, even when this sequence is followed, it must be acknowledged that due to measurement tolerance, measurement conditions, and process variation, only an estimate of the parasitic values can be obtained. Hence, the extraction of the active device should best be started with the parameters having the lowest sensitivity to the parasitic. The technique that is described in this work provides a very comprehensive and systematic way to determine which unknowns should be solved prior to others.

5.2 Analysis

For a Si/SiGe HBT npn device, the substrate must be connected to the most negative potential, which is the ground in the general case. Fig. 5.2 shows the small-signal equivalent circuit of the Si/SiGe HBT npn device including the substrate network. Since it is a common emitter, the emitter is also connected to the substrate. In this case, a three-port test structure with access to the substrate terminal cannot be used for modeling and characterization of the substrate effects. This is because the substrate network and collector-to-emitter network cannot be separated, as shown in Fig. 5.2. Bear in mind that the junction capacitances, C_{jbc} , C_{jbe} , and C_{jcsb} , are bias-dependent; separation of them may not be possible. The substrate network is only important at the collector terminal in a Si/SiGe HBT device as its emitter and base are shielded from substrate by the collector, thus the substrate network at the collector is required to be extracted. In such case, a two-port measurement is sufficient for

Figure 5.1: Simplified cross-sectional view of SiGe HBT (DT:deep trench)

modeling and characterization of the substrate network.

In the measurement setup, a two-port characterization for the collector with an open-base and open-emitter was employed to investigate the substrate effect. This test structure also provides the parameters for substrate parasitic de-embedding. The active device elements can then be accurately extracted without the parasitic effect. Unlike the conventional HBT test structure, an open-base and open-emitter Si/SiGe HBT test structure was proposed to extract the Si/SiGe HBT substrate network at its collector. The interconnects between the pad to the emitter and the pad to the base were disconnected in this test structure. These eliminate the effects of the networks between the collector to the emitter and the collector to the base in the process of extracting the collector substrate network. The simplified cross-sectional view of the Si/SiGe HBT is depicted in Fig. 5.1. In this setup, the connections of base and emitter to port-1 and ground were eliminated to extract the substrate network at port-2, which is connected to the collector.

Fig. 5.2 shows the small-signal equivalent circuit of the Si/ SiGe HBT, including the substrate network. Referring to Fig. 5.2, the base was assigned to port-1 and the collector was assigned to port-2, while the emitter was shorted to ground in this test structure. The HBT network can thus be obtained through de-embedding of the substrate network and the pad parasitic, as follows,

$$[Y_{hbt}] = [Y_{active}] - [Y_{pad-sub}] \quad (5.1)$$

where Y_{active} , $Y_{pad-sub}$ are the respective Y-parameters of the active network, substrate, and pad parasitic, and Y_{hbt} is the Y-parameters of the HBT network. $Y_{pad-sub}$ consists of C_{pbc} , C_{pbe} , and the substrate network.

5.2.1 Substrate Network Extraction

With access to the collector terminal only and the base and emitter open, two-port characterization is possible as port-1 and port-2 are connected to the open-base open-emitter test structure as shown in Fig. 5.4. Port-1 is not open.

Figure 5.2: Small-signal equivalent circuit of Si/SiGe HBT including substrate network

Figure 5.3: Simplified schematic of SiGe HBT for substrate network extraction

First of all, the substrate network is found at the collector only. As shown in Fig. 5.1 only the collector has direct contact with the p-substrate through the buried N+, while the base and the emitter are shielded from the p-substrate by the collector. Thus, the extraction at the collector is sufficient to capture the substrate effect. For the substrate network extraction, a two-port measurement was first performed on the open-base open-emitter test structure, Fig. 5.4, but only the network at the collector port was extracted. The networks between the base-collector and the emitter-collector were examined to ensure they are also open. The equivalent circuit of the open-base open-emitter after the short and the open dummy de-embedding is shown in Fig. 5.5. It is clear that it is a *pi*-network. Thus, the substrate network can be extracted as,

$$Y_{sub} = Y_{pad-sub,22} + Y_{pad-sub,21} \quad (5.2)$$

Figure 5.4: Test structure layouts of Si/SiGe HBT in common-emitter and open-base open-emitter configuration

The equivalent circuit of the substrate network is illustrated in Fig. 5.2. R_{sub} and C_{sub} are bias-independent; meanwhile, C_{jcsb} (the junction capacitance between collector and substrate) is a function of the applied junction voltage (V_{js}). A direct extraction technique was developed to accurately extract this network, and in this case only, port-2 connected to the collector was considered. The substrate network

Figure 5.5: Equivalent circuit of open-base open-emitter test structure

was extracted with a test structure where the base and emitter are opened. The test structure is illustrated in Fig. 5.1. The simplified schematic for the substrate network extraction is also shown in Fig. 5.3. The real part of the substrate network can be represented in terms of impedance and admittance networks respectively, as,

$$\text{real}(Z_{sub}) = \frac{R_{sub}}{(1 + \omega^2 R_{sub}^2 C_{sub}^2)} \quad (5.3)$$

$$\text{real}(Y_{sub}) = \frac{\omega^2 C_{jcsb}^2 R_{sub}}{(1 + \omega^2 (C_{jcsb} + C_{sub})^2 R_{sub}^2)} \quad (5.4)$$

where ω is the radian frequency. By plotting $\frac{1}{\text{real}(Z_{sub})}$ versus ω^2 and $\frac{1}{\text{real}(Y_{sub})}$ versus $\frac{1}{\omega^2}$, R_{sub} , C_{sub} , and C_{js} can be estimated from the intercept point at the y-axis and the gradient of the plots. The substrate resistance can be estimated with $R_{Si} = \frac{C_{sub} \cdot R_{sub}}{(e_r \cdot e_0)}$, where e_r and e_0 are the relative substrate and absolute free space permittivity.

5.2.2 Pad Parasitic Extraction

The pad parasitics, C_{pbc} , C_{pbe} were first extracted in cut-off mode [64]. In this extraction, the junction capacitance characteristics C_{jbe} , C_{jbc} , in reverse bias, were used. The total capacitance is given by,

$$C_{tot} = \frac{C_{j0}}{(1 - \frac{V_j}{\phi_j})^{m_j}} + C_p, V_j < \frac{\phi_j}{2} \quad (5.5)$$

where C_{j0} is the junction capacitance at zero bias, C_p is the parasitic capacitance, V_j is the applied reverse voltage, ϕ_j is the junction built-in voltage, and m_j is the exponent. In this process, the junction built-in voltage drops to between 0.70 V to

Figure 5.6: Substrate network extraction at $V_{js} = -3.00V$

Figure 5.7: Substrate network extraction for capacitances and resistance as a function of V_{js}

0.80 V, and the exponent is typically $\frac{1}{3}$ to $\frac{1}{2}$. By fitting C_{tot} to the measured junction capacitance with constrained values of ϕ_j and m_j , C_{pbe} and C_{pbc} can be estimated. $Y_{pad-sub}$ can be constructed with the extracted values of C_{pbc} , C_{pbe} , and the substrate network.

Figure 5.8: Parasitic capacitances extraction

5.2.3 HBT Extraction

The active device is referred to the Si/SiGe HBT equivalent circuit, as illustrated in Fig. 5.2. The entire network after de-embedding of the pads and substrate parasitic, can be described as,

$$[Z_{hbt}] = [Z_{int}] + \begin{bmatrix} z_b & 0 \\ 0 & z_c \end{bmatrix} + \left(\frac{1}{y_{jbe}} + z_e \right) \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \quad (5.6)$$

$$[Y_{int}] = [Y_{inti}] + y_{jbcx} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (5.7)$$

$$[Z_{inti}] = \begin{bmatrix} R_{bi} & 0 \\ -\alpha & (1-\alpha) \\ y_{jbci} & y_{jbci} \end{bmatrix} \quad (5.8)$$

$$\begin{aligned}
 z_b &= R_{bx} + j\omega L_b & y_{jbe} &= \frac{1}{R_{jbe}} + j\omega C_{jbe} \\
 z_c &= R_c + j\omega L_c & y_{jbc i} &= \frac{1}{R_{jbc i}} + j\omega C_{jbc i} \\
 z_e &= R_e + j\omega L_e & y_{jbcx} &= \frac{1}{R_{jbcx}} + j\omega C_{jbcx}
 \end{aligned} \tag{5.9}$$

$$\alpha = \frac{\alpha_0 e^{-j\omega\tau_d}}{1 + j\omega\tau_b}$$

where α , α_0 , τ_d , and τ_b , approximate the transport factor, dc current gain, phase-delay time, and time constant related to the first pole respectively, and R , L , C with subscripts are the components corresponding to Fig. 5.2. Y and Z , with the same subscripts, refer to the same network represented in Y - and Z -parameters.

By directly inspecting (5.6), z_b and z_c should be eliminated first, which is the most common practice in the literature for HBT network extraction. The subsequent step is either extraction of y_{jbe} or y_{jbcx} , which should normally reduce the HBT network to a simple T-network or π -network. In recently reported techniques [66, 75], y_{jbcx} , and R_{bi} were assumed to be purely capacitive and resistive. However, this solution is susceptible to parasitic effects and R_{jbcx} is ignored. In the present work, we solved y_{jbe} first by exploiting the physical relationship of the base transport factor to the junction characteristic [63]. Extraction of the α is insensitive to the parasitic effect, and thus can be extracted accurately in this way. Details of the extraction are given below.

The bias-independent networks, z_b , z_c , and z_e were determined using an open-collector technique [69, 72]. These elements constitute the extrinsic network of the active device. The intrinsic network, which consists of mostly bias-dependent elements, was obtained by subtracting the HBT network with the extrinsic network, as follows,

$$[Z_{intx}] = [Z_{int}] + \left(\frac{1}{y_{jbe}}\right) \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \tag{5.10}$$

At this state, y_{jbcx} and y_{jbe} will be the common terms in the equations (5.7) and (5.10), and hence the transport factor, α , can be extracted independently from (5.10). α_0 , τ_d , and τ_b were extracted from the transport factor magnitude and phase responses

Figure 5.9: Extrinsic parasitic resistance extraction at high-base currents

Figure 5.10: Extrinsic parasitic inductance extraction at high-base currents

Figure 5.11: R_{jbe} extraction at active forward operation region with high collector currents

by plotting $\frac{1}{|\alpha|^2}$ versus ω^2 , and φ versus ω .

$$\alpha = \frac{Z_{intx,12} - Z_{intx,21}}{Z_{intx,22} - Z_{intx,21}} \quad (5.11)$$

$$|\alpha|^2 = \frac{\alpha_0^2}{(1 + \omega^2 \tau_b^2)} \quad (5.12)$$

$$\begin{aligned} \varphi &= \angle(\alpha(1 + j\omega\tau_b)) \\ &= \angle(\alpha_0 e^{-j\omega\tau_d}) \\ &= -\omega\tau_d \end{aligned} \quad (5.13)$$

The extracted τ_b was then used to estimate the y_{jbe} [63, 64]. Since the R_{jbe} can be accurately extracted [61], C_{jbe} can be calculated from $\tau_b = R_{jbe} \cdot C_{jbe}$. Once the y_{jbe} was determined, the HBT network was further reduced to (5.7). Thus y_{jbex} can be estimated from,

$$Y_{int,12} = -y_{jbex} \quad (5.14)$$

Figure 5.12: Transport factor extraction at $I_b=40\mu A$, $V_{ce}=2.10V$

Finally, the rest of the elements can be estimated from (5.8)

$$Z_{inti,11} = R_{bi} \quad (5.15)$$

$$Z_{inti,22} - Z_{inti,21} = \frac{1}{y_{jbc i}}. \quad (5.16)$$

5.3 Experimental Results

The extraction technique is validated with fabricated SiGe HBT with a deep trench for isolation. An n-p-n device with six emitters was measured. Each emitter has an area of $0.30 \times 20.00 \mu m^2$.

Fig. 5.6, Fig. 5.7, Fig. 5.8, Fig. 5.9, and Fig. 5.10 show the substrate network and the bias-independent element extraction. The substrate resistivity, $R_{Si} = 7.476 \Omega - cm$, is consistent with the data provided by the foundry, which ranges approximately from 5.0 to $10.0 \Omega - cm$. The extraction of the base transport factor is illustrated in Fig. 5.11 and Fig. 5.12. The measured and the simulated S-parameters of the Si/SiGe HBT npn device at the forward-active operation region biased at $I_b=40 \mu A$, $V_{ce}=2.00 V$ were also depicted in Fig. 5.13. It is significant that the measured and simulated results fit closely in all the desired frequency ranges.

Figure 5.13: Measured and simulated S-parameter results (50MHz-26.05GHz)

5.4 Conclusion

In this research, a new direct extraction technique for a small-signal Si/SiGe HBT equivalent circuit with a substrate network was proposed, together with a new test structure for substrate network extraction. A new direct extraction technique for the substrate network was also described. This general technique can be applied to the same network in other equivalent circuits such as for a spiral inductor.

The substrate network can be modeled with R_{sub} , C_{sub} , and C_{jsub} , where C_{jsub} was modeled as the pn-junction diode capacitance. Hence, large-signal modeling and characterization were not required in this work to extract the small-signal equivalent circuit for Si/SiGe HBT with substrate network.

The Si/SiGe HBT direct extraction technique has been regarded as one of the major works in HBT extraction in [131, 132]. The substrate network extraction technique was also adopted in HBT extraction, as reported in [131, 132]. The extraction technique and test structure have also been adopted into CMOS device characterization with similar test structure (open-gate open-source) [133]. This further verifies

the extraction technique that has been developed here. The HBT substrate network extracted in this work was also used in the design of the 10 GHz Si/SiGe oscillators [105, 134], which will be described in detail in Chapter 6.

Chapter 6

RFIC Design: On Chip Oscillator

Design and implementation of RFIC, using the models and characterized devices from Chapter 3, Chapter 4 and Chapter 5, are further investigated here. We focus on the VCO design in this chapter¹.

This chapter serves to extend the validation of the modeling and characterization work that has been proposed and implemented in the previous chapters. First, the design of the LC-VCO in 0.35 μm CMOS, where the results of the symmetrical spiral inductor characterization were utilized, is described. In the second part, the oscillator design at 10 GHz using Si/ SiGe HBT is presented. The characterized varactor and Si/ SiGe HBT substrate network were adopted in this design.

6.1 CMOS VCO Design

In practice, there are a few design specifications that constrain the fully integrated LC type VCO design. The first design specification is the oscillation frequency, which requires proper inductance and capacitance value selection for the LC tank. The capacitor type and value determine the tuning range and tuning profile of the VCO. This is a prime requirement for the synthesizer design. Based on the initial capacitor value, the inductor value is then decided. There are at least two design specifications that limit the inductor value selection, namely phase noise and current consumption.

¹Part of the material in this chapter has been published in the journal, [34] and conference proceeding, [105]

The design procedure combines these interactively until the design specification is met. A few useful design consideration are listed here,

$$f_{osc} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}, \quad (6.1)$$

$$g_{LC} \approx \frac{1}{Q_L \cdot \omega \cdot L}, \quad (6.2)$$

$$gm \geq n_s \cdot g_{LC}, \quad (6.3)$$

$$V_{sw} = I \cdot \left(\frac{1}{g_{LC}} \right), \quad (6.4)$$

where, f_{osc} is the oscillation frequency, C and L are the lumped capacitor and inductor values in the LC tank, g_{LC} is the transconductance of the LC tank, Q_L is the quality factor of the spiral inductor, gm is the transconductance of the active device, n_s is a factor greater than one to ensure start-up oscillation over design variation, and V_{sw} and I are the voltage swing and the current consumption of the VCO.

Larger voltage swing contributes to the lower phase noise, and hence it is limited by g_{LC} for specified current consumption [92]. By inspecting the design equations (6.1) to (6.4), the quality factor Q_L and the inductor value L must be maximized to optimize the phase noise and the current consumption.

The trade-off between tuning range and phase noise for the LC-VCO must be optimized for a particular application. In this work, the tuning range was first determined and then the phase-noise was optimized. The tuning range required is from 2.40 to 2.50 GHz, centered at 2.45 GHz, which has been fulfilled by this design. Since the required tuning range is not very wide, a spiral inductor with a high quality factor at these frequency ranges was adopted to obtain good phase-noise. The quality factor of the inductor (≈ 10) is nominal to the phase noise performance of the LC-VCO based on Leeson's phase-noise equation (6.5). This is because the quality factors of other components, such as the varactor (≈ 40), are much higher.

The effective quality factors in single-ended and differential modes are depicted in Fig. 6.1. Empirical study indicates that VCO phase noise is inversely proportional

Figure 6.1: Effective quality factor for symmetrical spiral inductors, (with referred to Chapter 3)

Figure 6.2: Effective inductance for symmetrical spiral inductors, (with referred to Chapter 3)

to Q_L^2 [101].²

By employing symmetrical spiral inductors in differential mode, Fig. 6.1 shows that the effective quality factor can be improved by approximately 60% to 100% in comparison with their single-ended mode counterpart. The quality improvement amounts to a 4 to 6 dB phase noise reduction. In summary, it is clear a differential symmetrical spiral inductor is preferred for low phase noise LC-VCO design.

6.1.1 Measurement Results

A schematic of the differential LC-VCO is depicted in Fig. 6.3. The LC-VCO was implemented in 0.35 μm CMOS. Fig. 6.4 shows the microphotograph of the LC-VCO.

There is a trade-off between the LC-VCO tuning range and both phase noise and power consumption. In this demonstration, a differential A-MOS varactor with a small nominal capacitance was adopted to cover the required 2.4 GHz Industry, Scientific and Medical (ISM) band. The corresponding symmetrical spiral inductor was taken from sample index ten (referred to Chapter 3). A single-layer symmetrical spi-

²Lesson's phase noise equation,

$$\begin{aligned}\mathcal{L}(\Delta\omega) &= 10 \cdot \log \left\{ \frac{F \cdot k \cdot T}{2 \cdot P_0} \cdot \left[1 + \frac{\omega_c}{\Delta\omega} + \left(\frac{\omega_0}{2 \cdot Q \cdot \Delta\omega} \right)^2 \cdot \left(1 + \frac{\omega_c}{\Delta\omega} \right) \right] \right\} \\ &\approx 10 \cdot \log \left\{ \frac{F \cdot k \cdot T}{2 \cdot P_0} \cdot \left(\frac{\omega_0}{2 \cdot Q \cdot \Delta\omega} \right)^2 \right\},\end{aligned}\quad (6.5)$$

where

- $\mathcal{L}(\Delta\omega)$ is the single-sideband phase noise density (dBc/Hz) at frequency offset $\Delta\omega$,
- ω is the oscillation frequency,
- $\Delta\omega$ is the offset from the carrier frequency,
- ω_c is the flicker corner frequency of the active device,
- P_0 is the carrier power (W), T is the temperature in Kelvin (K),
- F is a noise factor unique for each oscillator circuit, which depends on the device sizes, current, and other circuit parameters,
- k is the Boltzman's constant (1.38×10^{-23} J/K),
- Q is the quality factor of the inductors

ral inductor was used to reduce the substrate noise coupling [135]. A LC-VCO using a double-layer symmetrical spiral inductor was also designed and implemented for comparison. Both LC-VCOs use the same devices and biasing, except that the single-layer symmetrical spiral inductor was replaced by a double-layer symmetrical spiral inductor. The biasing current, I_d , in this LC-VCO core, was set to approximately 4.5 mA. Both the $M_{p1,p2}$ and $M_{n1,n2}$ have an aspect ratio of 50 and 25 for phase noise optimization. The LC tank was constructed by a symmetrical spiral inductor and a A-MOS varactor with approximately 5 nH and 0.80 pF nominal values.

The simulated and the measured results match well. The simulated results have a higher oscillation frequency as the parasitic of the interconnects were not fully included in the simulation phase.

Figure 6.3: Differential LC-VCO schematic

The tuning characteristic, output spectrum, and phase noise performance of the LC-VCO are depicted in Fig. 6.5, Fig. 6.6, and Fig. 6.7, respectively. Only the measured results for VCO with single-layer inductors are shown, since both VCO's give identical performance. Note that the phase noise performance for both LC-VCO's shows no significant difference. These results further verify the conclusion that a

Figure 6.4: Microphotograph of the LC-VCO (physical size: $800\text{ }\mu\text{m} \times 1000\text{ }\mu\text{m}$)

Figure 6.5: Buffered VCO output tuning characteristic

Figure 6.6: Measured buffered VCO output spectrum, control voltage=1.5V

Figure 6.7: Buffered VCO output phase noise, control voltage=1.5V

single-layer symmetrical spiral inductor and a double-layer symmetrical spiral inductor have similar performance.

The entire LC-VCO, including the test circuit, draws about 14.0 mA from a 3.0 V supply. The core LC-VCO draws only approximately 4.5 mA. Table 6.1 tabulated the performance of a few 2.4 GHz VCOs. It can be observed that the LC-VCO examined in this research had demonstrably better performance in terms of power and phase noise. This is due to proper selection of the spiral inductor, and further, by closely considering the differential characteristic of the symmetrical spiral inductor.

Table 6.1: 2.4GHz VCO’s performance summary

	This work	Bunch <i>et al.</i> [50]	Andreani <i>et al.</i> [48]	Rogers <i>et al.</i> [100]
Technology	0.35 μ m CMOS	0.35 μ m CMOS	0.80 μ m CMOS	BiCMOS
Supply Voltage	3.0V	3.3V	2.5V	3.3V
Drain Current	4.5mA	12.0mA	9.0mA	4.0mA
Phase noise (dBc/Hz, at 100kHz offset)	-105	-97	-95	-97
Tuning Range	10%	16%	15%	27%

6.1.2 Section Summary

By employing a symmetrical spiral inductor in differential mode operation, the quality factor and peak frequency are improved significantly over its single-end counterpart. With proper selection of a spiral inductor, a fully differential CMOS LC-VCO can achieve superior phase noise performance at minimum power. This work has also been listed as one of the state of the art CMOS LC-VCO designs in [136].

6.2 SiGe HBT Quadrature Oscillator Design

Design of quadrature oscillators at 10 GHz was demonstrated, which involved development of the direct parameter extraction technique of the scalable varactors in

Chapter 4. The varactor was used in the tank circuit. The effects of the substrate parasitic of the Si/ SiGe in the quadrature LC oscillator design was also investigated in Chapter 5. Exploiting the substrate effect and accurate device characterization, a quadrature oscillator with -106 dB phase noise at 1 MHz offset, using 2.50 V single supply, was designed and implemented in Si/ SiGe HBT. The core oscillator consumes only 1.6 mA at 10 GHz.

6.2.1 Introduction

The quadrature oscillator is one of the most important components in clock recovery circuits in the optical devices [95, 96, 97, 98, 99, 137]. In this application, the oscillator does not require as wide a tuning range as VCO in frequency synthesizers. However, due to process variation and parasitic effects, designing an oscillator to oscillate at the desired frequency becomes a challenge in both process control and device modeling. To minimize design error, devices that contribute to the oscillation should be carefully characterized and included in the design phase.

At 10 GHz, a device with less parasitic effects is preferred. Hence, Si/ SiGe is widely adopted in these frequency ranges due to its high frequency capability. The substrate parasitic at the collector, which is the output port, becomes important at these frequencies. Accurate extraction of the substrate network has been reported in [76], and the result was adopted here in the design of a 10 GHz LC oscillator. In the design of the oscillator, a varactor value of less than 0.50 pF was required. However, characterization of a varactor with such a low value is problematic and easily affected by the measurement setup, and the model is not always available. In this work, we need to estimate the varactor value from the measured data. A direct extraction technique for the scalable varactors was developed and demonstrated in Chapter 4.

Figure 6.8: Block diagram of SiGe HBT quadrature oscillator

Figure 6.9: Oscillator core schematic of SiGe HBT quadrature oscillator

6.2.2 Analysis

Fig. 6.8 shows the block diagram of the quadrature oscillator [93]. V_{oI} and V_{oQ} are the quadrature oscillation signals. The corresponding schematic of the oscillator core is depicted in Fig. 6.9. Two oscillator cores are required to generate a $\frac{\pi}{2}$ phase difference. Similarly, n_o oscillators are used to generate the $\frac{\pi}{n_o}$ phase difference. Hence, circuitries of the quadrature oscillator are at least doubled as compared to the single oscillator. In this case, the power consumption of the oscillator core should be minimized.

Based on the LC oscillator design considerations proposed in [92], [34], a larger inductance is required to minimize power consumption. This, however, reduces the tuning range. The symmetrical spiral inductor was selected for its higher quality factor and area efficiency [34]. Its center tap is connected to V_s , which is the supply voltage, as seen in Fig. 6.9. V_s dc couples to the collector of the npn devices and the cathode of the pn-junction varactors. In this case, the substrate parasitic at the collector should be carefully considered. This is because the parasitic capacitances are part of the tank circuit, as follows,

$$f_{vco}(V) = \frac{1}{2 \cdot \pi \sqrt{L \cdot (C_{pn}(V) + C_p)}} \quad (6.6)$$

where L and $C_{pn}(V)$ are the inductance of the spiral inductor and the pn-junction capacitance, respectively. C_p simply represents the parasitic capacitances. The bias currents for the oscillator core and input devices $I_{1,2}$ were optimized for phase noise, [137]. Although the bias currents can also be used to tune the oscillation frequency, it was fixed in this work to validate the substrate effect. Si/ SiGe HBT with width=0.30 μm and length=20.0 μm was used for $n_{pn1,2,3,4}$ in Fig. 6.9. The biasing currents $I_{1,2}$ are approximately 1 mA. The symmetrical spiral inductor with center tapped, L_s , has a dc inductance of approximately 0.40 nH, and the pn-varactors, $D_{1,2}$ have a nominal capacitance of 0.25 pF. The dc coupled and ac coupled devices, $R_{1,2}$ and $C_{1,2}$ are 5 k Ω and 0.40 pF respectively. ,

Figure 6.10: Microphotograph of the quadrature oscillator (physical size: $1900\ \mu\text{m} \times 1400\ \mu\text{m}$)

In this section, the symmetrical spiral inductor model was extracted with the technique described in Section 4.3, in which it is center tapped. There are two conditions that allow both the spiral inductor without center tap and with center tapped to have the same characteristics;

1. Both spiral inductors are symmetric
2. The center tap is connected to the ac ground of the symmetrical spiral inductor.

In other words, both the input signals at terminal-1 and terminal-2 have to be differential signals.

The LC oscillator in this section is fully differential, and the symmetrical spiral inductor input terminals were connected to the differential signals. Hence, we can use the findings in Chapter 3 as a guideline in designing this LC oscillator.

6.2.3 Experimental Results

The LC quadrature oscillator was designed and fabricated using Si/ SiGe HBT with $0.18\ \mu\text{m}$ CMOS baseline. The schematic is depicted in Fig. 6.8 and Fig. 6.9. Fig. 6.10 shows the microphotograph of the quadrature LC oscillator, including the on-chip

buffer. For the core circuit, each npn device has an emitter area of $0.30 \times 20.00 \mu\text{m}^2$. A pn-junction varactor with eight fingers was used. For each finger, the area of the anode is $2 \times 15 \mu\text{m}^2$. The characteristics of the pn-junction varactor were estimated from the extraction results in Chapter 4.

The performance of the quadrature LC oscillator was measured with a Rohde & Schwarz signal analyzer (FSQ26) equipped with phase noise measurement capability. The output spectrum of the oscillator at 2.50 V and 3.00 V supply voltages are shown in Fig. 6.11 and Fig. 6.12 respectively. As expected, the oscillator with higher supply voltage has better phase noise performance. It shows about a 6 dB improvement with 3.00 V compared to a 2.50 V supply voltage at 1 MHz offset frequency.

Figure 6.11: Buffered output spectrum at supply voltage, $V_s=2.50\text{V}$

The tuning profile of the oscillator at different supply voltages was also measured, as seen in Fig. 6.13. The supply voltage can be incorporated in the oscillator design for tuning purposes. In this case, a locally regulated supply voltage to the oscillator should be employed. This is a common practice used to suppress the pulling/pushing effect. In this work, a 2.50 V supply voltage has been found suitable for the 10 GHz

Figure 6.12: Buffered output spectrum at supply voltage, $V_s=3.00\text{V}$

application. The oscillation frequency of the oscillator as a function of the supply voltage was also measured, as seen in Fig. 6.14. In this measurement, the voltage across the pn-junction varactor was fixed. Thus, the variation is merely due to the substrate capacitance at the collector.

The extracted equivalent circuits were used for simulation of the oscillations. As expected, the simulated and measured results matched well. The simulated circuit performances have slightly higher oscillation frequencies. This is mainly because of the under-estimation of the parasitic of interconnect.

6.2.4 Section Summary

The substrate effect of the npn SiGe device was investigated and incorporated into the 10 GHz LC oscillator design. In the design of the oscillator, a direct extraction technique was also developed to assist the design engineer in building a scalable varactor library. Using these design techniques, a low phase noise and low power oscillator at 10 GHz was implemented.

Figure 6.13: VCO tuning profile as a function of control voltage, V_t at different supply voltages, V_s (dotted line with symbol: measured performance, dotted line without symbol: simulated performance)

Figure 6.14: VCO tuning profile as a function of supply voltages, V_s , by fixing $V_d=2.00V$ ($V_d=V_s - V_t$) (dotted line with symbol: measured performance, dotted line without symbol: simulated performance)

6.3 Chapter Summary

In this chapter, two types of oscillators were designed and implemented in two different technologies;

1. LC-VCO at 2.45 GHz using 0.35 μ m CMOS
2. quadrature LC oscillator at 10 GHz using Si/ SiGe HBT with 0.18 μ m CMOS baseline

The results from the device modeling and characterization work, which were described in the previous chapters, were adopted in these RFIC designs. The devices used were a symmetrical spiral inductor, A-MOS varactor, pn-junction varactor, and substrate network of Si/ SiGe HBT. Based on the complex and multi-level design experience reported here, we can argue that the results of the modeling and characterization were sufficiently tested and confirmed. By properly characterizing the devices according to specific design requirements, such as the differential symmetrical spiral inductor, an optimum workable design can be achieved. At the same time, the direct extraction technique can contribute to the development of the scalable models and physical meaningful equivalent circuits. The equivalent circuit is very important in the simulation of the RFIC for performance optimization. All of these features have been demonstrated in this chapter.

Chapter 7

Conclusions and Recommendations

In this chapter, a summary of the achievements of this work is first given. This is followed by some suggestions for future work.

7.1 Conclusion

A study of the modeling and characterization of various silicon devices was carried out in this work. Both passive and active devices that are available in silicon processes were considered. Some selective research issues were addressed and efforts were made to propose their solutions. The research includes characterization of differential spiral inductor, extraction techniques for on-chip spiral inductor, transformer and varactor, as well as silicon device substrate network extraction and Si/SiGe HBT small-signal equivalent circuit extraction. Several innovations and significant results were made in each of the topics. Fig. 7.1 summarizes the overall contributions in this work.

A lack of comprehensive analysis and experimental data for differential symmetrical spiral inductor is the impetus for the design and characterization of a library of symmetrical spiral inductor. Both single-layer and double-layer symmetrical spiral inductors were implemented. To facilitate the design and characterization of the symmetrical spiral inductor, a few analytical expressions consisting of the design parameters were developed to serve as initial design equations. Subsequently, EM simulations were carried out to assist in fine tuning the desired performance of sym-

Figure 7.1: Summary of research work

metrical spiral inductor. Finally, symmetrical spiral inductors were fabricated and measured for characterization. From the results of the characterization, it is found that the performance of a double-layer symmetrical spiral inductor has no significant improvement over a single-layer symmetrical spiral inductor. However, the symmetrical spiral inductor in differential mode has much better characteristics than in single-ended mode. This was discussed in Chapter 3. These results are important to the IC designer during spiral inductor selection for circuit design in order to get an optimum trade-off. One example is the design of fully on-chip LC-VCO, which was also discussed in Chapter 6.

A simple but effective direct extraction technique for the equivalent circuit of spiral inductor with substrate network was proposed. A library of spiral inductors with wide range of device geometries was demonstrated. Characteristics of the extracted spiral inductor equivalent circuit match the measured characteristics up to 10 GHz for all the spiral inductors in the library. This is possible because a fully direct extraction technique was implemented as in Section 4.1. The direct extraction technique was

also extended to more advanced equivalent circuits for spiral inductors in Section 4.2.

The importance of the on-chip balun in advanced RFIC design also stimulates the development of new test structure and its relevant equivalent circuit extraction technique. This was reported in Section 4.3, where a new test structure and a new extraction technique were proposed and implemented. The test structure eliminates the requirement of three-port measurement and on-chip 50Ω load. The extraction technique was based on the two-port measurement by grounding one of the balun ports. The measurement was performed on the center tap and the other balun port. Both the test structure and the extraction technique were verified through comparison between measured and extracted characteristics. The results are in excellent agreement up to the frequency of interest, 10 GHz.

The equivalent circuit of varactor is bias-dependent and its extraction is complicated and time consuming using conventional fitting technique. A direct extraction technique was proposed to solve this problem. The details were described in Section 4.4. The extraction technique is also simple, effective, and applicable to both A-MOS and pn-junction varactors. This extraction technique was verified with a set of these varactors with a wide range of device geometries. The extracted varactor models are scalable with the number of fingers.

One point worth mentioning here is that all the extraction techniques proposed in this work are direct extraction. Unlike most of the reported extraction techniques, which merely focus on single device, these extraction techniques were verified with a library of devices, which covers a large variation of device geometries. This shows the usefulness of the direct extraction techniques proposed in this work.

One of the most critical problems of using Si/ SiGe HBT in comparison with other types of HBT is that its substrate network effect cannot be neglected. Thus, the Si/ SiGe HBT substrate network must be accurately modeled, characterized, and extracted. It should be included in the IC design phase for accurate simulation and estimation of the substrate effect. In this case, a test structure and a direct extrac-

tion technique were developed and implemented for the Si/ SiGe HBT small-signal equivalent circuit as well as its substrate network. This was discussed in Chapter 5. Unlike the conventional test structure, this work proposes a new test structure that is open-base and open-emitter for the Si/ SiGe HBT substrate network extraction. A new extraction technique was also proposed along with this new test structure.

The modeling and characterization of various devices here have been adopted in RFIC design. One of the best test vehicles is LC-VCO. The design, implementation, and optimization of the VCO were described in detail in Chapter 6. A high performance 2.45 GHz fully integrated LC-VCO was designed and optimized by considering the characteristics of the symmetrical spiral inductor in differential mode. A good trade-off between phase-noise and power was achieved.

A 10 GHz Si/ SiGe HBT quadrature oscillator was also designed and implemented. The extracted substrate network from Chapter 5 was utilized in this oscillator design. Low phase noise of -106 dBc/Hz at 1 MHz offset and low power of 1.6 mW at 2.50 V supply were achieved. Considering the oscillation frequency of 10 GHz, this oscillator achieved good trade-off between the phase noise and power consumption. The simulated and measured results were in good agreement. This has further verified the extracted equivalent circuits from the previous chapters.

In conclusion, the characterization and modeling of various silicon devices presented in this work will be useful for both the device and IC designs. Based on the results from this work, the device scientist can better optimize the characteristics of the device, while the IC designer can be more flexible in device selection and optimization of the circuit.

7.2 Recommendations for Future Research

This research work has involved a large number of resources, time, and painstaking experimental work. The topics covered are heterogeneous and cut across various disciplines, including device, process, modeling, characterization, and IC design.

Due to the finite resources available, it is not possible to include every aspect in detail, but only those relevant issues for which the proposed solutions seek to contribute and add value to future work.

7.2.1 Process And Device Development

Perhaps the most interesting future work is the design and development of new dedicated devices, and the characterization of them for RFIC design. As can be seen in Section 2.2, increasing the thickness of metalization is one of the best techniques for improving quality factor. Therefore, the thickness of the metal that will be used for those new devices should no doubt be a design variable for designer’s careful consideration.

Recently, 3-D devices are also attracting immense interest. Incorporating MEMS into a standard process to provide high quality and high isolation device should also be given greater attention. Improvement in process development and integration of MEMS and CMOS will definitely drive the adoption of new applications using new devices.

Figure 7.2: Measured and EM simulated dc inductance for single-layer symmetrical spiral inductor

7.2.2 EM Simulation

EM simulation of spiral inductor can be performed before fabrication as a general guideline for spiral inductor design. An example of the EM simulated and measured dc inductance is shown in Fig. 7.2. Note that there are some discrepancies for some samples showing the limitations of EM simulators. Meanwhile, full wave EM simulation of a large array of vias is not quite feasible due to simulation complexity and limited computing resources. In this context, research into effective EM simulation technique for the design and simulation of a library of spiral inductors can be explored for future work. The EM simulation should be time effective and accurate to estimate the characteristics of spiral inductors with a wide range of device geometries.

Author's Publications

Recent publication from this research work.

Journal papers;

1. T.H. Teo, Y.-B. Choi, H. Liao, Y.-Z. Xiong, and J.S. Fu, "Characterization of symmetrical spiral inductor in 0.35 μm CMOS technology for RF application," *Solid-State Electronics*, vol. 48, no. 9, pp. 1643–1650, September 2004.
2. Y.-Z. Xiong, T.H. Teo, and J.S. Fu, "Direct extraction of equivalent circuit parameters for balun on silicon substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 8, pp. 1915–1917, August 2005.
3. Jeffrey Shiang Fu, T. Hui Teo, and Eng Leong Tan, "Fully integrated frequency synthesizer design for wireless network application with digital programmability," *Microwave and Optical Technology Letters*, John Wiley & Sons, vol. 49, no. 10 pp. 2579–2582, October 2007.

Conference papers;

1. T.H. Teo, Y.-Z. Xiong, J.S. Fu, H. Liao, J. Shi, M. Yu, and W. Li, "Systematic direct parameter extraction with substrate network of SiGe HBT," *2004 IEEE Digest of Papers for Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 603–606, June 2004.
2. Y.-Z. Xiong, T.H. Teo, and J.S. Fu, "Characterization and modeling of balun on silicon substrate," *Proceedings of the 10th International Conference on Integrated Circuits, Devices, and Systems 2004 (ISIC 2004)*, September 2004.

3. T. H. Teo, Y. Z. Xiong, J. S. Fu, and E. L. Tan, “LC oscillator design at 10-GHz using substrate capacitance with scalable varactor parameters extraction technique,” *Proceedings of the 35th European Microwave Conference*, pp. 665–668, October 2005.

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Author's Vita

T.Hui Teo received the Bachelor of Engineering with honor from the Science University of Malaysia, Malaysia, in 1999 and Master of Engineering from the National University of Singapore, Singapore, in 2001, both in electrical and electronic engineering.

He was with Intelligent Micro-Device Pte. Ltd. as senior integrated circuit (IC) design engineer, where he worked on high precision sensor ASIC. In prior of this, he served ST Microelectronics. Currently, he is employed as a senior research engineer at Institute of Microelectronics, Singapore. His research interests are in analog & RF integrated circuit design and device modeling. He has involved in research projects and products development in WLAN, RF-link (low power RF transceiver), RFID, UWB (OFDM), automotive sensor ASIC, biomedical sensor ASIC, nano-structure bio-sensor IC and etc. He is the project investigators of a few research and industrial projects. He is currently an IEEE Senior Member.