On the design and applications of power buffer systems

Wang, Xiaoyu

2008

Wang, X. (2008). On the design and applications of power buffer systems. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/41755>

<https://doi.org/10.32657/10356/41755>

ON THE DESIGN AND APPLICATIONS OF POWER BUFFER SYSTEMS

WANG XIAOYU

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2008

Acknowledgements

First and foremost, I would like to express my sincere appreciation to my supervisor, Associate Professor, Dr. Mahinda Vilathgamuwa, for his invaluable instructions, directions, and consistent encouragement throughout my Ph.D. candidature. I am also deeply thankful to Prof. Choi San Shing, for his knowledge, guidance, fruitful discussions. I am greatly indebted to their broad interests, high enthusiasms for research and exemplary academic standards. Without them, completion of this thesis would have been much more difficult, if not impossible.

I am grateful to Nanyang Technological University for providing me research scholarship to carry out this research project. In particular, I would like to acknowledge my gratitude to Mr. Yeoh Tiow Koon, Ms Chew-Sim Annie, and Mr. Lee Ting Yeng for the technical support they have given me in the course of my research.

I greatly appreciate Professor, Lalit Kumar Goel, for his concerns and his secretary Koh-Chua Mei Fong, Alice for her continuous consideration.

I would also like to thank my friends for their supports in research and personal life.

Special thanks to my parents, uncles and aunties for their love, patience and support over these three years or so of my graduate program. Peace soul to my beloved sister.

Last but not least, I would like to express my gratitude to my wife, Zhang Jing, for her love, encouragement and understanding.

Summary

With advanced development of power electronic technologies, power electronic based devices have been found increasingly penetrating the power system. Such devices are normally highly regulated and draw constant power from the utility regardless of upstream conditions. From the system operation point of view, such constant power loads (CPL) show nonlinear dynamic features to the mains grid and may destabilize the system. In worst situations, voltage collapse could occur. Taking these factors into consideration, the negative influence of the power electronic based devices on the power system stability, especially on the voltage stability cannot be ignored any longer. It has attracted interests from researchers in finding solutions to mitigate such unfavorable characteristics in recent years.

Power quality issues on the load side have attracted much more attention from customers and utilities over the last few decades. The main reason for that is computerized and power electronic based equipment are increasingly used and these have been critical to successful manufacturing and business applications, such as those in hospitals, air traffic control, financial institutions and other automated processes. These equipment are sensitive to power disturbances since excessive deviations of the supply frequency and voltage, even for a short duration, will lead to unscheduled shutdown of industrial processes or equipment failure, causing substantial financial losses for the end-users. Therefore, power supply quality has to be improved especially under the deregulated conditions.

On the generation side, due to the deregulation of the power supply industry and increasing concern on the environment, distributed generation (DG) technologies have gained considerable interest from utilities in recent years. Compared with conventional electricity generations, DGs can supply electricity to customers with higher reliability and efficiency and more cost-effective and environmentally friendly way. With wide-spread

application of DGs, however, they also induce technology challenges to the traditional power systems. For example, due to the intermittent nature of wind speed, fluctuation output from wind farms may cause frequency deviations. These unfavorable impacts of DGs have to be tackled properly before they are integrated with existing power systems.

Taking these issues into consideration, a power buffer system is proposed in this thesis. The main focus of this project is to investigate the energy storage system (ESS) design for buffer system in voltage stability enhancement, load ride-through and wind power fluctuation attenuation.

The power buffer consists of front end three-phase boost converter and input R - L filter. Investigation begins with the mathematical model of the buffer system which is attained based on the voltage drop on the filter and the load-supply power balance. The controller applied for the power buffer during normal condition is proposed. This constant power control method consists of the inner current and outer voltage control loops. With PI constants appropriately selected, the power buffer is operated at unity power factor (UPF) condition and the dc-link voltage is maintained at its nominal level. During a disturbance, the power buffer is switched into constant impedance operation mode, under which the buffer-load combination is controlled to be a constant impedance thus the undesirable dynamic feature of the downstream CPLs is decoupled from the upstream utilities. Thereby, system stability is enhanced.

Performance of power buffer with Battery Energy Storage System is also examined. During voltage sag, the equivalent impedance of the buffer-load combination is just kept at constant at pre-fault level. This reduces the amount of power drawn from upstream systems and lessens the stress of CPLs on the utility. The load-supply power imbalance under such constant impedance control mode is compensated by the BESS connected to the dc-link. The model of the power buffer with BESS is derived, based on which the steady state and dynamic state performances of the buffer system are analyzed. In the steady state study, universal BESS model is applied. The relationship between the steady state dc-link voltage and the voltage sag depth is derived. In dynamic state analysis, the

impact of battery discharge current on the dynamic performance of power buffer is examined. To guarantee the proper operation of the buffer system and downstream connected sensitive loads, the BESS has to be suitably designed based on the information from these steady state and dynamic state analysis.

Integration of power buffers into power system for purpose of transient stability enhancement and load ride-through is also investigated. Two power buffer systems are connected to the sending- and receiving-ends respectively. When a fault occurs in the transmission link, voltage depression occurs in the network. From the instant of the fault inception and during the post-fault transient period, the CPLs connected to bus bars degrade the system transient stability. With power buffer incorporated, by detecting the generator speed acceleration or deceleration, the buffer system is switched into constant power mode or constant impedance mode accordingly, thus reducing the acceleration and deceleration at both ends and improving the transient stability of the system. The BESS capacities within the buffer systems are sized sufficiently large enough to guarantee the supply quality of downstream sensitive loads not to be disturbed.

As extension of its application in power system, power buffer is utilized in wind farms to attenuate the generated power fluctuation. An objective function is formulated in terms of the dispatch level and amortized BESS capital cost. From the planning point of view, the output power from the wind farm is assumed constant. By optimizing the objective function, the dispatch level is optimized and the BESS capacity in power- and energy-specifications is appropriately sized. Such a BESS can accommodate the power imbalance during fluctuation of wind but keep the output of the wind farm stable. Afterwards, based on the long term battery model, an iterative approach is proposed to calculate the dc-link voltage from the BESS power profile over the designed time interval. To guarantee the proper operation of the power electronics devices, the dc-link voltage has to be kept within the specific limits. Should there be unacceptable short-term violations in the dc-link a super-capacitor can be suitably designed to accommodate such short term violations.

Table of Contents

Acknowledgements.....	i
Summary.....	ii
Table of Contents.....	v
List of Figures.....	x
List of Tables	xiii
List of Abbreviations	xiv
List of Symbols.....	xvi
Chapter 1 Introduction.....	1
1.1 Motivation.....	1
1.2 Objectives	3
1.2.1 Decouple Dynamics of CPLs from Upstream Systems	3
1.2.2 Power Quality Improvement of Downstream Loads	4
1.2.3 Fluctuation Attenuation of Wind Farms Using Power Buffer	4
1.3 Major Contributions.....	5
1.3.1 Modeling and Development of Controller for Power Buffer System	5
1.3.2 Steady State and Dynamic Analysis of Power Buffer System with BESS..	6
1.3.3 Power Buffer in Transient Stability Enhancement and Load Ride-through	6
1.3.4 Attenuation of Wind Power Fluctuation via Power Buffer	7
1.4 Thesis Organization	8

Table of Contents

Chapter 2	A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems	10
2.1	Introduction	10
2.2	Voltage Stability	12
2.2.1	Load Characteristic Impact on Voltage Instability	13
2.2.2	Constant Power Loads	17
2.2.3	Countermeasures for Voltage Instability	18
2.3	Power Quality	20
2.3.1	Power Quality Terms and Definitions	21
2.3.2	CBEMA and ITIC Curves	23
2.4	Energy Storage System	25
2.4.1	Batteries	26
2.4.2	Super-capacitors	27
2.4.3	Flywheels	29
2.4.4	Superconducting Magnetic Energy Storage (SMES)	30
2.5	Lead-acid Battery Fundamentals and Models	32
2.5.1	Electrochemical: fundamentals of lead-acid batteries [89, 94-98]	32
2.5.2	Battery Capacity	34
2.5.3	Internal Resistance	36
2.6	Battery Models	37
2.6.1	Electrochemical Models	38
2.6.2	Equivalent Circuit Models	42
2.7	Distributed Generation	48
2.7.1	Micro-turbines [33]	49
2.7.2	Photovoltaics [33]	50
2.7.3	Fuel Cells [40, 42]	50
2.7.4	Wind Turbines [40, 42]	51
2.8	Conclusions	54
Chapter 3	Power Buffer Design for Load Dynamic Decoupling	55

Table of Contents

3.1	Introduction.....	55
3.2	Modeling and Control of Three-phase Active Power Buffer.....	58
3.2.1	Power System under Healthy Conditions	58
3.2.2	Power System under Upstream Fault Conditions	63
3.3	Simulation Results	69
3.3.1	Voltage Sag with 90% Positive Phase Sequence and 20% Negative Phase Sequence Components	69
3.3.2	Voltage Sag with 80% Positive Phase Sequence and 20% Negative Phase Sequence Components	72
3.4	Conclusions.....	73
Chapter 4	Power Buffer System Incorporated with BESS	75
4.1	Introduction.....	75
4.2	The New Power Buffer Scheme and its Principle of Operation	76
4.3	Analysis of the Power Buffer System	79
4.3.1	Circuit Model of Buffer with the Battery Storage	80
4.3.2	Steady-State Analysis of Power Buffer Operation	82
4.3.3	Transient Performance of Power Buffer	86
4.4	Simulation Results	90
4.5	Conclusions.....	94
Chapter 5	Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through	96
5.1	Introduction.....	96
5.2	Description of the Buffer Scheme.....	97
5.2.1	Buffer Scheme to Achieve Stability Enhancement.....	98
5.2.2	Buffer Scheme to Achieve Improved Load Ride-through	101
5.3	BESS Model Description	103
5.4	DC-link Voltage Determination.....	107

Table of Contents

5.5	BESS Capacity Determination.....	113
5.6	Illustrative Examples	114
5.6.1	A Temporary Mid-line Three-phase Fault	116
5.6.2	A Temporary Three-phase Fault at 1/3 Line Length from Bus 2	118
5.6.3	Further Discussion of the Results	119
5.7	Conclusions.....	121
Chapter 6	Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm	122
6.1	Introduction.....	122
6.2	System Configuration	124
6.3	Analysis of the BESS Sizing Scheme	126
6.3.1	BESS Power and Energy Specifications.....	126
6.3.2	Determination of BESS Power and Energy Capacities	127
6.3.3	Determination of P_d	128
6.4	DC-link Voltage Constraints.....	129
6.4.1	Battery Model	130
6.4.2	Determination of v_{dc}	131
6.4.3	Numerical Procedure to Determine v_{dc}	135
6.5	Illustrative Example	139
6.6	Conclusions.....	145
Chapter 7	Conclusions and Recommendations	147
7.1	Conclusions.....	147
7.2	Recommendations.....	149
References.....		152
Appendices.....		166

Table of Contents

VITA 169

List of Figures

Fig. 2-1 The temperature profiles of thermostat at different voltage level [9]. 16

Fig. 2-2 General power buffer structure. 19

Fig. 2-3 CBEMA curve [31]. 24

Fig. 2-4 ITIC curve [31]. 25

Fig. 2-5 Energy storage technologies: power ratings, discharge times and their applications [92]. 31

Fig. 2-6 Illustration of electrochemical cell and the electrode reactions [94, 95]. 32

Fig. 2-7 Low-rate and high-rate discharge curves of a lead-acid battery [95]. 35

Fig. 2-8 The current/voltage curve of lead-acid battery [95]. 37

Fig. 2-9 Typical three-segment model of open circuit voltage characteristic. 40

Fig. 2-10 Equivalent circuit of the universal model of battery. 41

Fig. 2-11 Simple linear battery model. 43

Fig. 2-12 Thevenin battery model. 44

Fig. 2-13 Fourth order battery model. 45

Fig. 2-14 Third order battery dynamic model. 46

Fig. 2-15 Schematic diagram of dual shaft MT [33]. 49

Fig. 2-16 Typical variable speed wind turbine integration topology with the use of a synchronous generator [70]. 53

Fig. 2-17 Typical variable speed wind turbine integration topology with the use of DFIG [70]. 53

Fig. 3-1 A load supplied through a buffer. 57

Fig. 3-2 Control system under healthy conditions [116, 117]. 60

Fig. 3-3 Inner current control loop. 61

Fig. 3-4 Outer voltage control loop. 63

Fig. 3-5 Parallel equivalent circuit of power buffer. 64

Fig. 3-6 Phasor diagram to describe the buffer-load combination under fault condition. 64

Fig. 3-7 An equivalent circuit of power buffer with the external filter included. 65

List of Figures

Fig. 3-8 Power buffer control system under faulty conditions.	67
Fig. 3-9 Bode-plots of (a) $\frac{I_d}{I_d^*}$ and (b) $\frac{V_{dc}}{V_{dc}^*}$	70
Fig. 3-10 Simulation results of power buffer with resistor load, (a) PCC voltage, (b) DC-Link voltage, (c) input current at time of sag initiation, (d) input current at time of sag removal.	71
Fig. 3-11 Simulation results of power buffer with resistor load, (a) PCC voltage, (b) DC-Link voltage, (c) input current at time of sag initiation, (d) input current at time of sag removal.	73
Fig. 4-1 Schematic diagram of a new BESS based power buffer-load scheme.....	76
Fig. 4-2 Equivalent circuit of power buffer-load combination in parallel representation.	77
Fig. 4-3 Phasor diagram describing the power buffer at (a) non-unity power factor and (b) unity power factor conditions at the PCC.	79
Fig. 4-4 Circuit model of lead-acid battery bank.	81
Fig. 4-5 Steady-state DC-link voltage ($V_{dc,ss}$) as a function of battery state of discharge (f) and power mismatch.	84
Fig. 4-6 Steady-state DC-link voltage ($V_{dc,ss}$) as function of battery state of discharge (f) and sag/swell level.	85
Fig. 4-7 Variations of damping ratio and dominant pole with battery discharge current.	90
Fig. 4-8 Buffer-load response under an unbalanced voltage sag of 40% positive phase sequence and 20% negative phase sequence (a) PCC voltage, (b) DC-Link voltages, with and without the battery, (c) input current, (d) input real and reactive power at PCC, (e) real power supplied by battery bank, (f) DC-Link voltage performance at different discharge current values.	93
Fig. 5-1 Schematic diagram of a two-generator network system with power buffers.	98
Fig. 5-2 Rotor angle difference ($\theta_1 - \theta_2$) between G_1 and G_2 : with and without power buffers.	101
Fig. 5-3 (a) Schematic showing the interconnection of lead-acid battery cells in the BESS, and (b) Typical response of battery cell terminal voltage $v_{b,i,j}$ to a step change in cell discharge current $i_{b,i,j}$	104
Fig. 5-4 Equivalent circuit of BESS.	106
Fig. 5-5 Approximate $P_b(t)$ by individual power pulses $\bar{P}_{b(k)}$	107

Fig. 5-6 Estimation of dc-link voltage at the end of 1 st time interval.	109
Fig. 5-7 Estimation of DC-link voltage at the end of 2 nd time interval.	111
Fig. 5-8 BESS ₂ response following a temporary 10-cycle three-phase mid-line fault: (a) P_{b2} , and (b) v_{dc2}	116
Fig. 5-9 BESS ₂ response following a temporary 10-cycle fault at 1/3 line length from Bus 2: (a) P_{b2} and (b) v_{dc2}	118
Fig. 5-10 A solid 3-phase fault at 0.3 line length distance from Bus 2: (a) P_{b2} , (b) v_{dc2} and (c) rotor angle difference.	120
Fig. 6-1 Variable speed wind turbine with inter-connection to the mains grid through power buffer system.	124
Fig. 6-2 A typical wind power profile based on data taken from [12]: constant P_d is shown.	125
Fig. 6-3 Profiles of (a) battery power for $P_d = 0.6$ p.u., and (b) battery energy corresponding to $P_d = 0.55, 0.6$ and 0.65 p.u. for the typical wind profile given in Fig. 6-2.	128
Fig. 6-4 DC-link (a) equivalent circuit, (b) simplified equivalent circuit, with BESS parasitic branch neglected.	131
Fig. 6-5 Approximation of $P_b(t)$ by individual power pulse $\bar{P}_{b(k)}$	132
Fig. 6-6 (a) Generic power pulse $\bar{P}_{b(k)}$ and the overall time-response in dc-link voltage constituting of (b) positive $\bar{P}_{b(k)}$ step and the corresponding dc-link voltage deviation and (c) negative $\bar{P}_{b(k)}$ step and the corresponding dc-link voltage deviation.	136
Fig. 6-7 (a) Wind power output, (b) benefit B vs dispatched level, (c) battery power profile at the selected dispatch level, (d) battery energy profile at the selected dispatch level, (e) dc-link voltage with a 19-branches BESS, (f) dc-link voltage with the 19-branch BESS paralleled with a 220F capacitor, (g) power stored/supplied by the capacitor, and (h) the re-calculated battery power with the capacitor implemented.	142
Fig. 6-8 (a) Wind power profile on Aug 29, 2006, and (b) corresponding dc-link voltage with the 19-branch BESS paralleled with the 220F capacitor.	145

List of Tables

Table 2-1 Comparison of different FC technologies [40]..... 51

Table 3-1 Parameters used for power buffer simulations [119] 69

Table 4-1 Parameters for Constant Power Load Simulations [69, 75] 91

Table 5-1 Battery Parameters Used in the Simulations [75]..... 105

Table 5-2 Transmission Line Parameters [121]..... 115

Table 5-3 Machine, Exciter and Governor Parameters [84] 115

Table 6-1 Battery Parameters [76]..... 140

List of Abbreviations

AC	Alternating Current
ASD	Adjustable Speed Drive
BESS	Battery Energy Storage System
CAES	Compressed Air Energy Storage
CBEMA	Computer Business Equipment Manufacturer Association
CPL	Constant Power Load
DC	Direct Current
DFIG	Doubly-Fed Induction Generator
DG	Distributed Generation
DOC	Depth of Charge
DStatCom	Distribution Static Compensator
DVR	Dynamic Voltage Restorer
EMF	Electromotive Force
ESS	Energy Storage System
FACTS	Flexible AC Transmission Systems
FC	Fuel Cell
ITIC	Information Technology Industry Council
MHC	Mechanical Hydraulic Controlled
MT	Wind Turbine
PCC	Point of Common Coupling
PMSG	Permanent Magnet Synchronous Machine
PQCC	Power Quality Control Center
PV	Photovoltaic
PWM	Pulse Width Modulation
SMES	Superconducting Magnetic Energy Storage
SOC	State of Charge
SOD	State of Discharge

List of Abbreviations

T&D	Transmission and Distribution
ULTC	Under Load Tap Changing
UPF	Unity Power Factor
VLRA	Valve Regulated Lead Acid
WT	Wind Turbine

List of Symbols

A	Area of the battery plates
C	Capacitance
$C(I, \theta)$	Battery capacity after a constant discharge current under constant temperature condition
C_{0*}	Nominal battery capacity at 0 °C
C_a	Battery capacity at 20 °C
d	Separation between the two charged cell plates
E_0	Equilibrium voltage of battery cell under open circuit
$E_{0,s}$	Equilibrium voltage of battery cell under standard conditions
$E_b, E_{b,\max}$	BESS energy and its maximum value
f	Battery SOD
I	Current
i_a, i_b, i_c	Three-phase input currents in a-b-c reference frame
$\bar{I}_{b(k)}$	Average current applied over k^{th} time interval
I_d^*, I_q^*	Reference d- and q-axis currents in positive sequence system
I_d^{-*}, I_q^{-*}	Reference d- and q-axis currents in negative sequence system
I_d, I_q	Input currents in d-q-0 reference frame
$\dot{I}_{in}$	Phase vector of input current
I_R, I_X	Real- and reactive-parts of $\dot{I}_{in}$
J	Moment of inertia
k_p, k_i	PI controller constants
L	Inductance
P	Real power
P_{12}	Power transferred through the transmission link
$\bar{P}_{b(k)}$	Power pulse applied over k^{th} time interval
P_b^*	Optimal value of P_b

List of Symbols

$P_b, P_{b,\max}$	BESS power and its maximum value
P_{b1}, P_{b2}	Power supplied by the BESS at sending- and receiving-end
P_d	Dispatched power from wind farm to the utility
P_{D1}, P_{D2}	Power consumed by the constant impedance loads at sending- and receiving-end
P_{G1}, P_{G2}	Power generated by the generator at sending- and receiving-end
P_l	Power consumed by the load
P_s	Power supplied by the source
P_{S1}, P_{S2}	Power consumed by the constant power loads at sending- and receiving-end
P_w	Wind power
$Q = CV$	Quantity of charge stored between the battery cell plates
$Q = \omega L/R$	Quality factor
Q_0	Reference charge capacity of battery cell
R	Equivalent battery resistance
R_0	Battery internal resistance at fully charged condition
R_{in}, X_{in}	Equivalent resistance and reactance of power buffer
R_θ	Battery thermal resistance between battery and environment
V	Voltage
V_{dc}	DC-link voltage
$v_{dc}(k)$	Calculated DC-link voltage at k^{th} time interval
$v_{dc,\text{lower}}, v_{dc,\text{upper}}$	Lower and upper limits for the proper operation range of v_{dc}
v_{ga}, v_{gb}, v_{gc}	Three-phase voltages at PCC
v_{gd}, v_{gq}	Three-phase voltages at PCC in d-q-0 reference frame
$\dot{V}_s, \dot{V}_g, \dot{V}_w$	Phasors of source voltage, PCC voltage and buffer terminal voltage
v_{wa}, v_{wb}, v_{wc}	Three-phase voltages at power buffer terminal
v_{wd}, v_{wq}	Three-phase voltages at power buffer terminal in d-q-0 reference frame
W	Energy stored in the capacitor
δ	Temperature coefficient
ϵ	Dielectric constant
θ	Temperature

List of Symbols

θ_a	Ambient temperature
θ_f	Freezing temperature
ξ	Damping ratio
τ	Time constant
ω	Rotor angular velocity

Chapter 1

Introduction

1.1 Motivation

With wide-spread proliferation of modern electronic equipment in present-day power systems, their negative influences on the voltage stability have drawn attention from many researchers. One of the main characteristics of power electronic based devices is that they are highly regulated and hence they are inclined to draw constant amount of power from the utility. Therefore, such loads are generally referred as constant power loads (CPL). From the upstream point of view, the CPLs show negative incremental impedance. This feature is undesirable for stable operation of the upstream systems, in particular during faulty conditions. For example, under some disturbances, the above mentioned negative incremental impedance of CPL will cause voltage instability or even voltage collapse of the whole system [1-21]. Recent survey results have revealed that there were many factors that contributed to the August 14th, 2003 blackout. However, it is very interesting to note that the city of Cleveland, where the blackout originated, has been experiencing industrial growth and new factories using large electric drives were set up. These CPLs would have contributed to the voltage collapse, due to the fact that the upstream system cannot supply as much power as demanded by the downstream constant power loads over the transient intervals [22].

On the load side, power quality issues have been attracting a significant attention in the last few decades. One of the main reasons is that, as mentioned above, the increase in penetration of power electronic equipment in the power system, such as motor drives, micro-computers and automation devices. Such loads are sensitive to disturbances induced in the upstream sources. Undesirable power quality may cause malfunction of

these sensitive devices and result in economic loss to the customers. Nowadays, utility customers are better informed about power quality. Especially, in case of deregulated power systems, meeting power quality standards is an important motivation for the utility operators, because loss of a disgruntled customer to a rival electricity supplier will have a significant economical impact. Therefore, both customers and utilities are more acutely aware of the need of quality power supplies than ever before [23-31].

On the generation side, due to the deregulation of the power supply industry and increasing concern on environment, distributed generation (DG) technologies have gained great interest from utilities in recent years. DGs are generally small scale electricity generations located close to end customers, in form of micro-turbine, photovoltaic, fuel cell, and wind turbine etc [32-43]. By introducing these DGs, customers can be supplied electricity with more reliable, higher-efficiency and cost-effective manner by avoiding transmission and distribution through long distance from traditional generation centers located far away. Furthermore, DGs possess the most appealing merits that they are environmentally friendly and use renewable resources, such as sunlight and wind.

However, with wide-spread application of DGs, they also induce technological challenges to the traditional power systems. For example, due to the intermittent characteristic of the sun shine and wind speed, output fluctuation of DGs may cause frequency oscillations. These unfavorable impacts of DGs have to be tackled properly before they are integrated with the existing power systems and fully play their roles [32, 33, 44-56].

Energy storage system (ESS) is one of the solutions adopted in power systems to improve the system performance. With advanced development of ESS technologies, large capacity ESSs have become cost-effective to be applied in high voltage power systems. With the assistance of power electronic based interfaces, the extra electricity energy during low load demand intervals can be stored in form of electrochemical, electromagnetic, kinetic or potential storage medium. When a disturbance occurs in the power systems, energy stored in ESS can be released to play the functions of guaranteeing system stability and power quality [57-64].

1.2 Objectives

Taking all the factors mentioned in last section into consideration, ESS based power buffer systems have been proposed in [22, 65-69]. By properly controlling the power buffer during the disturbance occurring in the upstream system, the undesirable dynamic characteristics of CPLs are decoupled and this in turn prevents the probable occurrence of voltage collapse. ESS within the buffer system plays a central role in determining the overall ride-through capability. With application of power buffer in high voltage power systems, attempts to size the ESS capacity have to be made to maintain the power quality of the downstream sensitive loads.

The research work to be addressed in this thesis is focused on the design of power buffer systems to be applied into high voltage power systems. The detailed objectives can be addressed as follows:

1.2.1 Decouple Dynamics of CPLs from Upstream Systems

As mentioned above, the negative incremental impedance of CPL is the main factor contributing to voltage instability problem. One possible solution for this is to alter the load characteristic shown to source side after a disturbance is detected. Apparently, if the equivalent impedance of the load can be controlled to be constant or the input current can be kept constant, the power flowing into downstream loads will be reduced and the voltage drop along the line will be decreased or at least kept at a constant value. All these will reduce the power drawn from the upstream systems and hence release the stress of CPLs on the utility. Thereby voltage stability of the system can be enhanced during disturbances. Fortunately, this objective can be realized by adjusting power electronic devices connected to loads. Based on the commonly used three phase boost converter, a power buffer configuration is proposed to improve voltage stability. The mathematical model and constant impedance control scheme applied for the power buffer under fault conditions are also presented in Chapter 3.

1.2.2 Power Quality Improvement of Downstream Loads

The power quality of the downstream loads is another factor taken into consideration in power buffer system design. Especially, with wide-spread use of highly regulated power electronic based devices, they are more sensitive to supply side disturbances than that of traditional loads. Therefore, the power buffer has to be designed carefully to meet power quality requirements of the connected loads. This function is fulfilled by the ESS connected to the dc-link. To guarantee the proper operation of downstream loads, the ESS performance, including its steady state and dynamic performance needs to be carefully examined. These ESS related issues will be addressed in Chapters 3 and 4.

1.2.3 Fluctuation Attenuation of Wind Farms Using Power Buffer

As one of the most promising renewable energy sources, the trend of wind power generation is changing from isolated usage to wide spread utilization. In the last decade, the global wind energy capacity has increased rapidly. The installed wind power capacity all over the world has grown to 47.317 GW from about 3.5 GW in 1994. In year 2004, 7976 MW of wind power capacity installed, an increase in the total installed wind power generating capacity of 20% [70]. Though wind technologies have improved significantly during the past 20 years, to incorporate large amount of wind energy into the existing power systems is still under active research and development. As discussed before, one of the big challenges of wind power integration with mains grid is that the large amount of fluctuated power induces frequency variation in the power systems. As an extension of power buffer applications, the buffer can be applied to achieve the goal of wind power fluctuation attenuation. This part of work will be presented in Chapter 6.

1.3 Major Contributions

Original contributions achieved thus far can be summarized as follows:

1.3.1 Modeling and Development of Controller for Power Buffer System

There are numerous power converter topologies used to feed electronically-controlled loads. Some of them have been used for power buffer applications [22, 66-69]. Among such converters, those of which could shape the line currents to be sinusoidal and control the dc-link voltage have been gaining popularity. For high power applications, the three-phase boost converter adopted in this thesis is able to take in almost sinusoidal input currents with a near unity power factor and to work in both rectifying and regenerating modes. The power circuit of power buffer mainly consists of a three-phase converter and its front end R - L filter.

Based on such a buffer scheme, the mathematical model for the further system design is proposed in this thesis. After small signal analysis applied, a conventional PI controller for the buffer system is presented. This controller is referred as constant power mode since the dc-link voltage is regulated to be at nominal level. During fault intervals, however, the power buffer is switched into so called constant impedance mode under which the buffer-load combination is adjusted to be a constant impedance. In the latter controller design, the unbalance fault situation has also been taken into account. Method to select the PI controller parameters and to determine the constant impedance value are discussed in detail. In this analysis, the equivalent impedance during the disturbance is kept at pre-fault value. Therefore, the power flow from the upstream source to the downstream loads will be reduced, which decouples the negative influence of the CPL dynamics on the source side and hence enhances the system voltage stability. Indeed the dc-link voltage depresses with the lack of power, under conditions that a passive load is connected. Under deep sag conditions, the dc-link voltage may drop below the acceptable level only above which can the back-to-back converters work properly.

1.3.2 Steady State and Dynamic Analysis of Power Buffer System with BESS

To satisfy the power quality of the downstream connected loads, ESS is included into the power buffer system. Under fault situations, the front end rectifier is adjusted so that equivalent impedance of the buffer-load combination is kept constant at its pre-fault level. The mismatch power between that supplied from upstream and that demanded by the constant power load is compensated or absorbed by the ESS connected to dc-link. In this study, BESS is selected due to its cost-effectiveness and mature technology. Combining the universal battery model [71] with the mathematical model of the front-end converter, the circuit model of power buffer with BESS is proposed. Again, small signal method is applied to reduce the nonlinear system from second-order to first-order and based on that the steady state- and dynamic-performances of the power buffer are analyzed. In both analyses, the power quality of the downstream load is considered, i.e., to guarantee proper operation of the power electronic converter based loads, the dc-link voltage is kept within an acceptable range, say $[0.9, 1.1]$ p.u. [72-74]. From steady state analysis, the relationship between voltage sag depth with dc-link voltage level for different BESS state of discharge (SOD) can be found. The dynamic analysis is focused on the impact of BESS parameters on the transient performance of the power buffer. Such information can be used for the design of BESS based on the power buffer ride-through ability.

1.3.3 Power Buffer in Transient Stability Enhancement and Load Ride-through

A two-generator system is examined to investigate the effect of proposed power buffer system on transient stability enhancement and load ride-through. With the assumption that the input mechanical power to the machines un-changed, when a fault occurs in the system, the surplus power at the sending end will accelerate the machine but the receiving end machine will be decelerated, due to the disruption of power transfer from sending end

to receiving end. With the use of proposed power buffer systems and through detection of the rotor speed, the power buffer is operated in constant power mode or constant impedance mode depending on whether the machine accelerates or decelerates respectively. When power buffer is operated in constant power mode, the buffer-load combination will maintain constant power drawn from the utility, which in turn reduces the acceleration of the sending end machine. From the design principle of power buffer, one knows that the amount of power drawn by the buffer-load combination will be reduced by square of the voltage magnitude with the constant impedance operation during a fault induced voltage sag condition. Therefore, the operation of power buffer in constant impedance mode in the receiving end will reduce the deceleration of the receiving end machine.

During the fault and post-fault intervals, the mismatch power between the CPLs and that supplied by the upstream network is taken by the BESS within buffers. The BESS capacity has to be sized sufficiently large that the dc-link voltage is well within its pre-set limits to guarantee the appropriate operation of the downstream loads and power electronic devices as well. For this transient study, the short term battery model presented in [75] is adopted. An iterative method is derived to calculate the dc-link voltage based on the readily obtained BESS power profile and BESS parameters, from which the BESS capacity can be sized.

1.3.4 Attenuation of Wind Power Fluctuation via Power Buffer

With rapid development of wind energy, penetration of wind power in power systems tends to increase. Due to the intermittent feature of wind speed, the output of wind power is unsteady. Significant amount of such fluctuated power injected to the power system will have negative effects, such as frequency deviation and voltage fluctuation. Therefore, a scheme incorporating power buffer with wind farms to attenuate the wind power fluctuation is proposed in this thesis. Though, the generated wind power fluctuates, the output power from the wind farm in this scheme is scheduled to be kept constant. The

power difference between these two quantities is proposed to be absorbed or supplied by BESS in power buffer. Therefore, the capacity of the BESS is a key factor in determining whether the power buffer can work properly. A cost function in terms of dispatched power level, BESS power capacity and energy capacity is formulated. Through optimization of this formulation at the maximum profit point, the dispatch level of the wind farm and the BESS size in power and energy specifications will be determined.

Since this scheme is for system planning purpose, the long term battery model given in [76, 77] is used to investigate whether aforementioned BESS capacity is large enough, so that the dc-link voltage variation is kept within the specified limits. If the limits are violated, a suitably designed capacitor is connected to accommodate the short-term violations.

1.4 Thesis Organization

The focus of the thesis is on design of power buffer systems to enhance system stability, improve power quality and attenuate wind power fluctuation. Chapter 1 provides a brief summary of the motivation and lists the major contributions made in this project. A review of voltage stability issues, power quality problems, ESS technologies and DG technologies are given in Chapter 2. A literature review pertaining to the research area is also included.

Original contributions of this research are described in detail from Chapter 3 to Chapter 6. In Chapter 3, the mathematical model of the power buffer is derived. Constant power and constant impedance control schemes are designed for the power buffer applicable for normal and fault conditions respectively. Under normal conditions, the power buffer is operated at UPF and dc-link voltage is regulated at its nominal value. When a fault occurs, the equivalent impedance of buffer-load combination is regulated to decouple the dynamic of constant power loads from the source side to prevent system collapse.

The ESS part of the power buffer is examined in Chapter 4. With the incorporation of the universal battery model, the steady state and dynamic performance of the buffer system is

investigated. The steady state model relates voltage sag depth with the steady state dc-link voltage value for different BESS SOD and the dynamic model describes the buffer dynamic features in terms of BESS internal parameters. This information is useful for the designers and operators in BESS design and maintenance.

In Chapter 5, power buffer systems are applied to a two-machine system to enhance the system transient stability and load ride-through during fault and post-fault intervals. After a fault occurs, the buffer-load combination is properly regulated to be in either constant power or constant impedance modes so that the transient of the system is improved. Power quality of the downstream constant power loads is guaranteed by the suitably sized BESSs.

Application of power buffer in attenuating wind power fluctuation is presented in Chapter 6. From planning point of view, an objective function in terms of dispatch level and BESS specifications is proposed. Subsequently, the dispatch level and BESS capacity are simultaneously determined through optimization of the above mentioned cost function. For BESS, if dc-link voltage violates the specified limits, capacitor is an option selected to accommodate such violations.

Conclusions and recommendations for future works are given in Chapter 7.

Chapter 2

A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

2.1 Introduction

As discussed in Chapter 1, with the advancement of power electronic technologies, power electronic converter based loads have been increasingly penetrating power system. Since such devices are normally highly regulated, they tend to draw constant power from the utility regardless of upstream conditions. From the system operation point of view, these constant power loads exhibit nonlinear dynamic feature to the mains grid and may deteriorate the system stability after a small perturbation. In worst situations, voltage collapse will be resulted. Taking these factors into consideration, the negative influence of the power electronic converter based loads on the power system stability, especially on the voltage stability are attracting increasing attention in recent years [1-21]. In this Chapter, a general review of the load characteristic and their impacts on the voltage stability are given. As one of the countermeasures to mitigate the negative influence of constant power loads on the upstream source, the power buffer is introduced, which decouples load dynamics from the source to ride-through the disturbance.

On the load side, however, computerized and power electronic equipment are used increasingly and are critical to successful manufacturing and business applications, such as those in hospitals, air traffic control, financial institutions and other automated processes. These equipment are sensitive to power supply disturbances since excessive deviations of supply frequency and voltage, even for a short duration, will lead to unscheduled shutdown of industrial processes or equipment failure, causing substantial

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

financial losses for the end-users [22-31, 65-69, 72-74, 78, 79]. Therefore, power quality is also essential in the proper operation of sensitive loads and it will be discussed briefly in this Chapter.

To enhance voltage stability and power quality, energy storage system (ESS) is one of the common devices utilized in power systems [57-64]. The electrical energy can be stored in forms such as electromagnetic, kinetic or potential. With the assistance of advanced power electronic technologies, electrical energy in the ac system can be converted into one of aforementioned forms and stored in the ESS. When a disturbance happens in the power system, controllers including exciters and governors of the synchronous generators may not always respond rapid enough to maintain the system stability. Consequently, energy stored in ESS can be released so that it would improve the system stability and power quality. The general forms of the ESS are summarized in this Chapter and especially the battery energy storage system (BESS) based on lead-acid battery is addressed in detail for its cost-effectiveness and technological maturity.

The last part of this Chapter presents issues related to the distributed generation (DG). With ever-increasing electricity demand in the power system and great concern on the environment, the traditional electrical generation methods cannot be used to meet such requirements. In traditional systems, the power plant is typically located near the fuel source but is far from the load center. The generated electricity is transmitted over long distance transmission and distribution (T&D) networks before delivered to the costumers. The T&D networks should be reconstructed to improve the transmission capacity, which needs large capital investment and normally takes a long time to finish the reconstruction. If the new development on the network lags increase in load demand, the supply reliability will be degraded. Therefore, it is necessary to find a new approach to meet the load demand. Moreover, the traditional electricity generators emit gaseous emissions from fossil-fuelled plants and are not environmental friendly. With increasing concerns on the environmental pollution, the researchers and governments all-over the world are driven to find clean and abundant sources of energy [32-43]. Among possible energy sources, the wind energy has been becoming more attractive and gaining popularity due

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

to its low cost and abundance in nature. Its penetration in the power system has rapidly increased during the last decade and this trend will tend to continue in near future [32, 70, 80-82]. With the inherent intermittent nature of wind energy, integration of such sources of power will have significant effects on the conventional power systems [44-54]. A power fluctuation attenuation scheme, based on the BESS incorporated power buffer system, and applicable for wind energy integration, is therefore proposed in this thesis.

In this Chapter, impacts of load characteristic on voltage stability will be addressed in the following section. Power quality issues and commonly used power quality improvement methods will be given in Section 2.3. The various ESS forms are introduced in Section 2.4 and particularly the BESS models are presented in Section 2.5. DG technologies and their impacts on the mains grid will be reviewed in Section 2.6.

2.2 Voltage Stability

Voltage stability is a subset of overall power system stability. In literature voltage stability covers quite a wide variety of phenomena. In this thesis, the following definition suggested by CIGRE [83] is adopted.

A power system at a given operating state is *small-disturbance voltage stable* if, following any small disturbance, voltages near loads are identical or close to the pre-disturbance values. A power system at a given operating state and subject to a given disturbance is *voltage stable* if voltages near load approach post-disturbance equilibrium values. The disturbed state is within the region of attracting of the stable post-disturbance equilibrium.

In short, voltage stability is the ability of a power system to maintain steady acceptable voltages at all buses in the system under original operating condition and after being subjected to a disturbance. It relies on the ability to maintain/restore equilibrium between load demand and load supply from the power source. The absence of voltage stability in power system leads to voltage instability and that results in occurrences in form of

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

progressive fall or rise of voltages at some buses. If voltage instability occurs, it may cause loss of load in an area, tripping of transmission lines and other elements by their protective systems and leads to cascading outages. Such outages or other operating conditions that violate field current limit may even result in loss of synchronism of some generators. The progressive drop in bus voltages can also be associated with rotor angle instability [1, 83-85]. All these are un-favorable for operation of the overall system.

The worst case effect of the voltage instability is voltage collapse. This is a process by which the sequence of events accompanying voltage instability leads to a blackout or abnormally low voltages in total or a significant part of the power system [83, 84, 86]. In the later case, though stable operation at low voltage may continue after some loads are tripped intentionally or unintentionally, the remaining loads tend to be voltage sensitive and the demanded normal voltage cannot be met. Especially after the disasters happened in northeastern USA and central Canada on August 14, 2003, the term ‘voltage instability’ and ‘voltage collapse’ are drawing more interest from engineers and researchers. This topic appears more frequently in open literature and in discussions among system planners and operators [1, 2, 4, 6, 7, 85-87].

2.2.1 Load Characteristic Impact on Voltage Instability

As pointed out in [84], voltage instability is strongly affected by system conditions and characteristics. Among those the followings are the main factors that contribute to voltage instability or collapse:

- Unfavorable load characteristics
- Large distances between generation and load
- Poor coordination between various control and protective systems
- Under-load tap changing (ULTC) action during low voltage conditions

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

Among the above listed reasons, load characteristics is the one influences most on voltage stability [1-9]. From this point of view, voltage stability has been called load stability, since voltage instability is usually originated in load. Note that “load” here is the load seen from transmission system high voltage buses and includes the effects of sub-transmission and distribution systems. Responding to a disturbance, power consumed by the loads tends to be restored by the action of motor slip adjustment, distribution voltage regulators, tap-changing transformers or thermostats. Restored loads will increase the stress on the high voltage network by increasing the reactive power consumption and causing further voltage reduction. This negative loop continues to cause voltage instability when load dynamics try to restore power consumption beyond the capacity of the transmission network and the connected generation.

The following specific load characteristics are paid special attention in the voltage stability studies [9, 83, 84]:

Discharge Lighting

Such loads include mercury vapor, sodium vapor, fluorescent or similar types of lighting widely utilized in industry for car-park and traffic. In commercial area, discharge lightings may occupy up to 20% of the system loads. These loads extinguish at about 80% of nominal voltage and will drop to zero during a fault or when voltage swings down during a power-angle swing. Generally speaking, a momentary drop in load near the electrical center of a system will usually improve the first-swing. However, lighting near the sending-end generators extinguishes and takes one to two seconds to restart after the fault. This will increase generator acceleration deteriorating stability.

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

Induction Motors

The inertia and rotor flux time constant of a motor mainly determine the motor real and reactive power response to voltage and frequency swing characteristics following a fault. Reaccelerating motors near accelerated generators tend to slow generators and improve stability. However, if the reaccelerating motors are in weak areas, voltage will be pulled down, synchronizing power reduced and the stability degraded. Motor starter contactors may drop at 65-75% in the case of 2300 V and 4000 V motors and 55-65% in the case of motors at 460 V and below. Motors may drop during the fault event or during a voltage sag/swell following a fault. This will deteriorate stability since the lost load power adds to transfers if this is near sending-end generators. Near the receiving-end or in weak areas, such loss of motor load may enhance stability.

Thermostat-controlled Loads

In short term studies, many loads, for example space heaters, molding and packaging machines, soldering machines, and water heaters, can be seen having constant resistance characteristic. Such loads are operated in a temperature range where the effect of changes in power input doesn't change temperature enough to significantly affect resistance. However, during just the beginning seconds after a decrement in voltage, the reduction in heat product from such devices will be sensed by thermostats and the 'on' part of the thermostat cycle will be extended. Thermostats that are in the 'off' duration of their cycle when the voltage change occurs will not respond to the voltage drop until they enter the 'on' part of their cycle.

Fig. 2-1 The temperature profiles of thermostat at different voltage level [9].

A temperature profile of a thermostat-controlled load with 100% and 90% voltage has been shown in Fig. 2-1. As can be seen, temperature rises more slowly than normal during the 'on' interval of the cycle when voltage is low. But temperature drops at the same rate during the 'off' period of the cycle. However, the average temperature, and thus the average power input, is the same for both cases. From the long term point of view, therefore, the thermostat-controlled loads are equivalent to constant power loads. There are many industrial, commercial and residential loads possessing such characteristic in the power system.

Electronic Devices (Regulated Power Supplies)

Many electronic devices, such as computers, microwave ovens, TVs, and other switch-mode or regulated power supplies always demand a constant dc output for input voltage down to 90% of normal. Therefore, they are effectively constant power loads down to this voltage. Below this voltage, some of these loads will malfunction or cannot be operated

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

properly. The power drawn thus will drop when voltage depresses below this 90% level of the rated voltage.

Adjustable Speed Drives

Motors using power electronics for variable speed control have been commonly used in power systems. Since controlled rectifiers are used, power factor is improved for low voltage as the firing angle is reduced to maintain the dc voltage. Therefore, they will shut down typically when voltage depresses below the lowest point, normally of 90% of the rated value [83]. Like above mentioned electronic devices, such loads respond fast to voltage relative to rotor angle oscillations. These loads effectively show constant power characteristic to the power system.

2.2.2 Constant Power Loads

Present power systems have been equipped with advanced power electronic devices extensively [21]. Compared to conventional power systems, these new systems have unique features, including dynamics and stability problems, which have been studied, researched and understood only recently. One of the key characteristics shown by such devices is that under highly regulated conditions, they will draw constant power from the upstream. For a given disturbance, the input current increases when the input voltage depresses and vice versa, which makes the constant power loads (CPL) to behave like having a negative impedance feature looking from the input terminals. This characteristic deteriorates the voltage drop/swell situation further and in worst case, voltage instability will be resulted. This destabilizing effect is the negative impedance instability [10, 12, 13, 17, 19].

2.2.3 Countermeasures for Voltage Instability

To improve voltage stability, the planners and researchers have proposed several solutions from generation systems and transmission systems point of view [83]. Fundamentally, however, voltage stability is caused by load stability. Therefore, effective countermeasures for voltage instability can be found with the investigation of the root of problem.

Planning by Reducing Feeder Impedances

Upgrading sub-transmission and distribution circuits will help voltage stability by reducing feeder impedances. Utilization of higher voltage distribution circuits may also be beneficial. Correct representation of sub-transmission systems is desirable for voltage stability studies. Such representations should include equivalents of feeder impedances, non-utility generations and dynamic loads.

Voltage Reduction

Voltage reduction under critical conditions is frequently used to obtain load relief. For voltage stability, the reduction in reactive power loads may be particularly important. It is because distribution transformers are commonly operated in saturation. A 1% reduction in voltage may cause a sustained reduction in reactive power load by 4-7%.

Under-voltage Load Shedding

Under-voltage load shedding is a cost-effective, decentralized voltage stability solution only for the infrequent disturbances. This is an important backup for primary solutions to

voltage stability problems. Under-voltage load shedding removes a burden from system operators who otherwise might be required to rapidly shed load manually during emergencies. It allows operators to take more risk in achieving economic system operation. The time delay must be short of 1-1.5 seconds to avoid stalling of induction motors during the final phase of voltage instability. If most of the loads are static and highly voltage sensitive, the time delays may be longer.

Power Buffer

To mitigate the negative influence of the CPLs on voltage stability, much work has been carried out to find solutions [11, 14, 15, 20]. However, the common approaches are to add resistance to the input filter to lower the quality factor and cancel the negative resistance supplied by the constant load. This can be implemented by either adding resistance or by adding a large input shunt capacitor. Unfortunately, the adding capacitor not only changes the frequency characteristics of the system, but also increases the positive resistance by the accompanied resistor of the capacitor.

Power buffer is an interface device between a source and load that is used to alter the effective load characteristic presented to the source and to shield the load from source transient [65-67, 69]. This is accomplished by using an energy storage system (ESS) such as capacitor or battery. Generally speaking, the power buffer is used to dynamically decouple the load from the source and vice versa. The general structure of the power buffer is shown in Fig. 2-2 [68], where V_{in} is the source voltage and P_{load} is the power drawn by CPL.

Fig. 2-2 General power buffer structure.

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

The power buffer presents a variable impedance to the source. The real power mismatch between P_{load} and that absorbed by the buffer P_e is supplied by ESS. Note that the source can be AC or DC and the power buffer circuit can be built up based on AC/DC or DC/DC converters.

2.3 Power Quality

For reasons mentioned below, power quality has been drawing attention increasingly from both electric utilities and industry end-users of electricity [23-30, 79];

- With new loads and devices containing microprocessor-based controls and power electronic devices that are particularly sensitive to many kinds of disturbances, an increasing proportion of loads have become very sensitive to power quality variations than ever before.
- To reduce losses, much effort has been put on overall power system efficiency by application of devices such as adjustable-speed motor drives and shunt capacitors for power factor correction. This results in higher harmonic level and has increased impact of harmonics on the system.
- Utility customers have been well informed about issues such as interruptions, sags etc. and are in a better position in demanding the utility to improve the quality of power delivered.
- Most utilities have been committed to deliver a high quality power supply for many decades. Designing a system with high supply reliability, at reasonable cost, is always a technical challenge.
- Power quality has become so reliable that long interruptions are rare in most industrialized countries. This means that the consumers are very sensitive on phenomena such as voltage sags and harmonic distortions.

Though power quality has been under research since late 1980s, there is no exact meaning of the term ‘power quality’. However, the following set of definitions are widely used in the recent literature [28],

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

- **Voltage quality** is concerned with deviations of the voltage from the ideal. In an AC system, the ideal voltage is a single-frequency sine wave of constant frequency and constant magnitude.
- **Current quality** is concerned with deviations of the current from the ideal. The ideal current is again a single-frequency sine wave of constant frequency and magnitude. An additional requirement is that the sine wave is in phase with the supply voltage.
- **Power quality** is the combination of voltage quality and current quality.

In most practical situations, however, power supply systems can only control the quality of the voltage; it has no control over the currents that particular loads might draw. Therefore, the standards in the power quality fields are devoted to maintain the supply voltage within certain limits. From this perspective, power quality is also voltage quality.

2.3.1 Power Quality Terms and Definitions

Power quality standards may differ from country to country. It is therefore important to provide a clear understanding of the terms and definitions that are used in the literature before one can proceed to consider detailed analysis work. The following items are attracting interest and are briefly introduced [28-30],

Voltage sags: Voltage sag is a decrease in voltage to between 0.1 and 0.9 p.u. in *rms* value at power frequency for duration of 0.5 cycles to 1 minute. It is considered as the most frequent power quality problem in practice. Generally, voltage sags are caused by faults on adjacent feeders or the switching of heavy loads. Many load devices are quite sensitive to voltage sags, they could be tripped when the *rms* voltage depresses below 90% for longer than one or two cycles. This will cause economic loss to the customers.

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

Voltage swells: As the opposite of voltage sag, a voltage swell is defined as a voltage increase to between 1.1 and 1.8 p.u. in *rms* value at the power frequency for durations from 0.5 cycles to 1 minute. Similar to sags, swells occur when unbalanced faults happen in the adjacent area. Swells can also be caused by switching off a large load or energizing a large capacitor bank.

Voltage interruptions: Voltage interruptions mean complete loss of voltage of below 0.1 p.u. on one or more phase. Momentary interruptions are defined as those incidents lasting between 0.5 cycles and 3 s, temporary interruptions have time span between 3 s and 60 s, and sustained interruptions are those last for a period longer than 60 s.

Transients: Transient is a sudden, non-power frequency change between two consecutive steady states of voltage, current or both. It can be *impulsive*, which is unidirectional in polarity (primarily either positive or negative), or *oscillatory*, which includes both positive and negative polarity values. Though most transients are usually generated near the user due to the operation of other equipment, switching operations on the utility network can pose a more serious problem. For example, capacitor switching can lead to transients with magnitude of 2~3 p.u. and the high energy levels can considerably shorten the life of surge protection devices.

Harmonics: Harmonic is defined as sinusoidal voltages or currents having frequencies that are multiples of the fundamental power frequency. Generally harmonics are caused by nonlinear characteristics of power system devices and loads. For example, the switches of power electronics devices in the adjustable-speed drives could inject high order harmonics components into the power system and leads to the distorted waveforms in the current. In recent years, in particular with the growth of non-linear loads such as personal computers and power electronic devices, the combined effects of many such devices can result in harmonic distortion of voltage/current greater than 5~10% levels and exceed the normal industry regulation standards.

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

Notches: Notching is a periodic voltage disturbance lasting less than 0.5 cycles. Mainly power electronics devices cause notching when the current is commutated from one phase to another during the momentary short-circuit between the two participating phases.

Voltage fluctuations/flickers: Voltage fluctuations are systematic variations in the envelope or a series of random voltage changes with magnitudes that do not normally exceed the range of 0.9 to 1.1 pu. Typical cause of flickers includes the operations of power converters on electrical devices.

2.3.2 CBEMA and ITIC Curves

The so-called Computer Business Equipment Manufacturer Association (CBEMA) curve given in Fig. 2-3 is nominally used to describe the voltage quality of a power system regarding voltage interruptions, sags or swells. This curve is originally produced as a guideline to help CBEMA members in the design of the power supply for their computers and electronic devices. This curve relates the magnitude and duration of voltage variations which can be tolerated by such devices connected to a power system. The region between the two uppermost and lower boundaries define the tolerance envelop within which the electronic devices are expected to operate reliably. Operated outside this region, the device may be shut down for lack of energy or damage due to insulation failure or over-voltage.

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

The CBEMA Curve from FIPS No. 94.

Fig. 2-3 CBEMA curve [31].

With replacement of CBEMA by Information Technology Industry Council (ITIC), the ITIC curve is developed by the new council as shown in Fig. 2-4. From this figure one can find that the tolerance limits at different durations given in ITIC curve are very similar with that in CBEMA curve. The main difference between them is that the ITIC version is piecewise and hence easier to digitize than the CBEMA one. And due to the prominence of the CBEMA curve among the computer and electronic industries, the ITIC curve is being considered as the subsequent CBMEA curve within the high technology circle.

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

Fig. 2-4 ITIC curve [31].

2.4 Energy Storage System

From previous discussions, one can find that, with experience of ever-increasing load demand in the power systems, the utility could not develop generation and transmission facilities as fast as possible due to economic, environmental and technical constraints. Especially with the emergence of computer-based systems, power quality has become one of the important factors to be improved for the system operators. It is because that most disturbances will cause malfunctioning of such sensitive devices and lead to economic losses.

To cater for aforementioned challenges and with advanced development of power electronic technologies, researchers have adopted power electronic converter based devices, such as Flexible AC Transmission Systems (FACTS) in transmission level or Distribution Static Compensator (DStatCom) and Dynamic Voltage Restorer (DVR) in distribution level. In most of these devices, however, the energy storage system (ESS) plays a very important role. High advances in energy storage technologies make various

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

solutions in power system applications possible. Though the energy storage technologies are initially developed for large-scale load-level purposes, they are frequently considered as useful tools in improving system stability, power transfer ability and power quality in power systems [57-64, 71, 88-93].

Energy storage technologies developed presently such as batteries, ultra-capacitors, flywheels and superconducting magnetic energy storage (SMES) are commonly used in power system utilizations [57, 60-62, 64]. In the following sections, these four technologies will be introduced briefly. The energy storage systems should preferably be capable of the following properties:

- High power ratings (tens of MW)
- High energy storage capacity (tens of MWh)
- Separable power and energy ratings
- Fast response times (ms)
- Low self-discharge
- Low investment and operating costs

2.4.1 Batteries

As one of the most cost-effective energy storage medium, batteries store energy in electrochemical form. Under a potential applied to the terminals, an internal chemical reaction takes place in the batteries and they are charged to store electrical energy. Reversely, during the discharging process, the stored energy in batteries is removed by undertaking the reverse chemical reaction. Due to the chemical kinetics involved during the internal reaction, heat will be generated during the charging/discharging procedure. Therefore, batteries cannot be operated at high power level for long time intervals. Otherwise, heat generated in rapid charge/discharge process will damage or shorten the lifetime of batteries. Generally speaking, a battery system consists of a group of low-

voltage battery cells connected in parallel and series to obtain a desirable electrical characteristic [94, 95].

The battery technologies considered for large-scale energy storage presently include lead-acid batteries, nickel-metal hydride batteries, nickel-cadmium batteries and lithium-ion batteries. Compared with the lead-acid type, Ni-Cd and Li-ion types are more advanced and possess higher energy density capabilities. However, they are not cost effective and technologies are not matured enough for higher power applications. Therefore, lead-acid batteries are the most widely used medium designed for bulk energy storage for rapid charge and discharge. Among lead-acid batteries, valve regulated lead-acid (VRLA) batteries have better cost and performance characteristic for stationary applications [89]. It is for this reason that VRLA batteries are adopted in this thesis as the energy storage medium in the power buffer system design. The details of their fundamental electrochemical reactions, equivalent electrical circuits will be addressed in next section.

Among available energy storage technologies, batteries are the most versatile because of their high energy capability, acceptable power density, and relative low cost and mature technologies. Therefore, they have gained wide spectrum of applications.

2.4.2 Super-capacitors

Capacitors store energy in electrical form by accumulating positive and negative charges between two conducting plates that are separated by an insulating or dielectric material. The quantity of charge stored between the plates, Q , is determined by the capacitance, C , and the voltage over the two plates, V . The relationship is given by the following equation,

$$Q = CV \quad (2.1)$$

The capacitance is in turn varies proportionally with the area of the plates and inversely with the distance between the plates, as shown in (2.2),

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

$$C = \frac{\epsilon A}{d} \quad (2.2)$$

where ϵ is the dielectric constant of the material between the oppositely charged electrodes. A is the area of the plates and d is the separation between the two charged plates. From (2.2), it can be found that the capacitance can be increased by increasing the area of the plates, increasing the dielectric constant or decreasing the distance between the plates.

The energy stored in the capacitor, W , depends on the capacitance and square of the voltage as given in the following equation,

$$W = \frac{1}{2} CV^2 \quad (2.3)$$

It is readily seen from (2.3) that the energy storing capability of a capacitor can be increased by either increasing the capacitance or the voltage. The stored voltage, however, is constrained by the voltage-tolerance-strength of the dielectric.

Super-capacitors differ from the conventional capacitors in that they are ‘electrolytic’ rather than ‘electrostatic’ elements. They store energy at the interface between the ionic conducting electrolyte and the electronic conducting electrode (typically carbon), which build up an electrochemical double-layer. The carbon materials used have a very high surface area (up to 2000 m²/g) and the electrode distance is in order of several angstroms. The voltage ratings of the super-capacitors are normally low, typically about 1.5 V for systems with aqueous electrolytes and about 3 V for systems with non-aqueous electrolytes. The energy capacity of these capacitors, however, can be thousands of time larger than that of the conventional ones.

Compared with lead-acid batteries, the energy densities of super-capacitors are relatively low (up to 10 Wh/kg). The power densities, nevertheless, are much higher because the capacitors can be charged and discharged at very high rates.

2.4.3 Flywheels

Flywheels store energy in kinetic form by rotating mass of their rotors. The capability of energy stored is proportional to the moment inertia of the flywheels rotors and the square of their rotational speed, as given in the following equation,

$$W = \frac{1}{2} J \omega^2 \quad (2.4)$$

where J is the moment inertia of the flywheel and is determined by the radius, mass, and height (length) of the rotor, as shown in (2.5). ω is the rotor angular velocity and is limited by the tensile strength of the rotor material.

$$J = \frac{r^2 m h}{2} \quad (2.5)$$

From (2.4) and (2.5) one can find that to achieve the same amount of energy stored, lightweight materials allow higher speeds than heavy materials of the same tensile strength. In these cases, the lighter materials can store more energy per unit weight and per unit volume. In practical development of flywheels for power applications, currently there are two schemes being utilized. One is to increase the flywheel moment of inertia by applying a rotor made of steel with high tensile strength and large radius. The speed of this type of flywheels is typically up to 10,000 revolutions per minute (rpm). The second scheme is to develop flywheels with high speed. The rotors of this type are made of lightweight materials, such as plastic reinforced with fibers with high tensile strength which can sustain speeds up to 100,000 rpm.

The response time of a flywheel energy-storage system is in order of several milliseconds. Therefore, flywheels can deliver very high power, which is usually limited by the interfacing power electronics. The largest commercially available flywheel system is about 5 MJ/1.6 MW weighing roughly 10,000 kg. Flywheels are much less costlier than

super-capacitors and SMES and are competing with batteries in high-power, low energy applications.

2.4.4 Superconducting Magnetic Energy Storage (SMES)

SMES systems store energy in the magnetic field produced by the DC current circulating through a superconducting coil. The inductive energy stored, W , and the rated power, P , are expressed in (2.6) and (2.7) respectively,

$$W = \frac{1}{2} LI^2 \quad (2.6)$$

$$P = \frac{dW}{dt} = LI \frac{dI}{dt} = VI \quad (2.7)$$

where L is the inductance of the coil. I is the DC current flowing through the coil and V is the voltage across the coil.

When cooled below its critical temperature (typically of -269°C), the resistance of the superconducting coil drops to zero and therefore, the coil can conduct very high currents without electrical losses. The only losses in the SMES system are caused by refrigeration that is necessary to maintain the coil temperature below the critical value and the non-superconducting components like power condition circuitry. Therefore, SMES systems have high efficiency and fast response capability. The peak power available from SMES is limited only by the ratings of the interfacing power electronics.

As with flywheels, the energy capacity of SMES systems is quite low, typically a few kWh, which is independent of the power density. Compared with other energy storage technologies, SMES systems are still costly so far. However, the integration of an SMES coil into existing FACTS devices reduces the cost for the inverter unit, which is the

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

normally the largest part of the cost of the whole SMES system. Currently, SMES systems are applicable where fast response, high power and low energy are needed.

Except for the above mentioned four energy storage technologies, there are several others that have been considered and utilized in the power systems, such as pumped-hydro energy storage, compressed-air energy storage (CAES) and fuel cells. Among those, pumped-hydro and CAES are both capable of high power, high energy applications. But they generally take multiple seconds to minutes to come on line from a standby or spinning reserve status. Therefore, they are not suitable for power quality application where a rapid response is required. They are better for assignment as an energy resource for load leveling. From this point of view, these technologies are only mentioned peripherally in this review.

Summarily, Fig. 2-5 shows the above mentioned energy storage technologies arrayed across three types of applications and plotted in terms of typical system sizes and maximum discharge times.

Fig. 2-5 Energy storage technologies: power ratings, discharge times and their applications [92].

2.5 Lead-acid Battery Fundamentals and Models

The history of lead-acid battery can be tracked back to over 100 years ago. The first practical fundamental element of lead-acid battery was reported in 1859 by Gaston Planté who detected that discharging current could be drawn from a pair of lead plates that had been immersed in sulfuric acid and subjected to a charging current. Based on this concept, Camille Fauré introduced the pasted plate in 1881, which has been mainly implemented to date. During the past hundred years, the basic elements of the battery have not been further radically changed.

2.5.1 Electrochemical: fundamentals of lead-acid batteries [89, 94-98]

The electrochemical cells constitute basic elements of a battery. The scheme of battery cell and the reactions taking place inside of the cell are shown in Fig. 2-6. The positive and negative electrodes are immersed in the electrolyte. The so-called active materials or reacting substances are stored in the electrodes.

Fig. 2-6 Illustration of electrochemical cell and the electrode reactions [94, 95].

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

The electrochemical reaction is made possible by the changeover from ionic current to electronic current at the electrolyte/electrode interface. This is a reaction which involves the taking up or giving off of electrons. In this reaction either a reduced substance is oxidized, yielding electrons or an oxidized substance is reduced, consuming the corresponding amount of electrons. The reactions take place at positive- and negative-plates are described as in the following equation [95],

where P, N indicate positive and negative electrodes respectively. S_{ox} and S_{red} are the oxidized and reduced states of the chemical compounds that react.

For lead-acid batteries, lead is the active material. Corresponding to (2.8), the following equation is applicable,

Taking into consideration of reactions that occur with the sulfuric acid, (2.9) has to be completed to (during discharge process),

By carrying out the above reaction, cell equilibrium voltage across the two electrodes is resulted and can be calculated based on Nernst Equation as given below [95],

$$E_0 = E_{0,s} + \frac{RT}{nF} \ln \frac{a_{\text{H}^+} \cdot a_{\text{HSO}_4^-}}{a_{\text{H}_2\text{O}}} \quad (2.11)$$

where E_0 is the equilibrium voltage of the cell. $E_{0,s}$ is the equilibrium potential under standard conditions. T is the temperature in K and R is the molar gas constant for an ideal gas ($R = 8.3413 \text{ J/K} \cdot \text{mole}$). F is the Faraday constant, equivalent to 96 485 As. nF gives

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

the amount of electrical charge connected with the reaction. a_{H^+} , $a_{HSO_4^-}$ and a_{H_2O} are the activities, approximately the concentrations, of H^+ , HSO_4^- and H_2O respectively.

Once split up the cell reaction into two separate electrode reactions and connect consumer circuits to the two electrodes, the electrons are collected as a current flowing through the outside devices. The inside chemical energy stored in battery will be converted into electric energy. During the charge process, reactions reverse of (2.10) take place and the battery is restored.

2.5.2 Battery Capacity

Battery capacity describes the energy amount that can be removed out from a battery during discharge process. It is very important to define the capacity precisely. Generally speaking, the battery capacity is defined by the following equation [98],

$$C = \int_0^t I(t) \cdot dt \quad (2.12)$$

where C is the battery capacity in Ah. I is the discharge current in A. t is the discharge duration in hours. It is to be noted that if the battery is discharged in constant current, (2.12) is simplified to the product of current times discharge period, $I \cdot \Delta t$.

Though (2.12) defines the capacity in an unambiguous way, battery capacity is not a fixed quantity, but depends on the conditions under which it is operated. In general, the followings are considered to be the main factors that influence battery capacity in practice.

- Discharge current
- Voltage limit
- Temperature
- State of discharge (SOD)

- History of the battery

The impact of the last two factors on battery capacity is straightforward. The deeper the battery is discharged, i.e., the higher SOD, the less quantity of charges is stored in the battery and less energy can be supported by the battery any more. In turn, the longer time the battery has been utilized or more cycles being charged and discharged, more or less the battery capacity is reduced. Finally, once its capacity goes below the acceptable level, it will be discarded. The relationship between the first two factors and battery capacity is depicted in Fig. 2-7.

Fig. 2-7 Low-rate and high-rate discharge curves of a lead-acid battery [95].

Physically, increased current reduces the potential of the positive electrode because of increased polarization. On the other hand, the potential of the negative electrode increases simultaneously. As a result, the terminal voltage across the battery will reduce more under larger discharge current. This point can be readily seen from Fig. 2-7. The top curve depicts a low rate discharge case, in which the discharge duration is more than 5 hours when the terminal voltage depresses to 1.7 V from its initial value. In the high rate discharge case as shown in lower curve, however, even the initial voltage is already reduced for the increased polarization. The slope of the latter case becomes much stiffer than that of the low rate discharge case. The above mentioned end of discharge voltage of 1.7 V is reached immediately.

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

Voltage limit is the final voltage or end of discharge voltage, which is defined by the battery manufacturer, adopted cell design and the application of the battery. Its influence on battery capacity can also be seen from Fig. 2-7. One can examine the top curve first, if the end of discharge voltage is shifted from the above mentioned 1.7 V to 1.9 V as shown by the slash line, the discharge duration is reduced to less than 4 hours and the capacity of the battery is only 80% of the lower rate discharge case. The influence of voltage limit is more apparent in the low curve. As can be seen, if the same voltage limit is selected, the discharge reaches the limit at the very beginning and battery capacity is much reduced. Therefore, for high rate discharge case, the voltage limit has to be changed.

Due to the change of temperature dependent kinetic parameters, the battery capacity decreases 0.5-1% with increment of per degree Celsius. The change of the battery capacity can be calculated based on that under standard reference temperature using the following equation,

$$C_a = \frac{C}{1 + \delta(\theta - 20)} \quad (2.13)$$

where C is the battery capacity at temperature θ . C_a is the actual capacity at 20 °C. θ is temperature in degrees Celsius. δ is the temperature coefficient and it equals to 0.006 for most lead-acid batteries [95].

2.5.3 Internal Resistance

Internal resistance is one of the important characteristic parameters of battery. However, unlike a simple ohmic resistance, which describes the linear relationship between the voltage and the current flowing through the component, the battery internal resistance is a highly nonlinear quantity. It is because that the battery current and voltage are determined by the complex electrochemical reactions taking place inside the battery and $v-i$ relationship is shown in Fig. 2-8.

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

Fig. 2-8 The current/voltage curve of lead-acid battery [95].

From the above figure, it can be seen that the battery voltage and current are not in a proportional relationship and thus the battery internal resistance is not linear but depends on the current. The current/voltage curve is not symmetrical for the charging and discharging reactions. Therefore, the internal resistance is different during these two processes.

As with battery capacity, the battery internal resistance is also influenced by its SOD and temperature. This point depends on the different manufactures and can be obtained by the experimental method. But the internal resistance normally increases with decrement of temperature due to the reduced conductivity and retarded kinetic parameters.

2.6 Battery Models

As mentioned in the above contents, the battery electrochemical reaction is a complex process and many factors influence battery characteristics. From analysis point of view, however, it is easier to describe the battery performances by using electrical parameters. Therefore, there exist several equivalent electrical circuit models of battery developed in battery applications. Though none of them is completely accurate and includes all necessary performance effecting factors, the following ones introduced in this section are

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

commonly used in the practical utilizations [71, 75-77, 99-103]. It is to be noted that the factors list below are generally considered in the battery modeling,

- SOD
- Rated capacity
- Battery Temperature
- Rate of charge or discharge
- Usage history
- Electrolyte concentration and
- Sulfate formation

2.6.1 Electrochemical Models

As the simplest battery models, the electrochemical models are only based on electrochemistry but ignore the thermodynamic and quantum effects. Therefore, though these models can be used for energy predictions, they are unable to model such phenomena as time with rate of change of voltage under load. These models do not include temperature and age information.

2.6.1.1 Peukert's Equation [98]

The Peukert's equation is one of the widely accepted relationships between battery capacity, discharge current and time. It is an empirical equation as given in the follows,

$$I^n t = C \quad (2.14)$$

where I is the constant discharge current in A. t is the time to discharge at current I in seconds. C and n are the battery constants which are determined from constant current test. n approaches 1.0 for very low currents and 2.0 for very high currents. For lead-acid batteries, typical value of n is of 1.35.

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

Based on Peukert's equation, the term *C-rate* is usually used to determine battery capacity, which is actually a current but is expressed as a time in hours. C-rate refers to the time required to fully discharge the rated capacity of a lead-acid battery at given constant current. For example, C/20 rate is the current required to discharge a battery in 20 h, C/3 is the current to discharge in 3 h.

2.6.1.2 Shepherd's Equation

The Shepherd model is perhaps the best known and most often used battery model in electric vehicle analysis. It was developed to describe the electrochemical behavior of the battery directly in terms of voltage and current. This model represents the terminal voltage by the well known Shepherd's equation as following,

$$E = E_0 - Li - Ki \left(\frac{1}{1-f} \right) \quad (2.15)$$

where E is battery terminal voltage of a cell. E_0 is the open circuit voltage of the battery cell when fully charged. i is the instantaneous current. $f = it/Q_0$ is SOD of the battery. Q_0 is the battery reference charge capacity in Ah. L and K are constants related to the internal resistance.

It is to be noted that Shepherd's equation is normally used to describe the general battery terminal characteristics because it is very difficult to find uniform constants in (2.15) applicable for all batteries to describe their internal electrochemical phenomena. The constants are usually found through curve fitting techniques using specific measured terminal characteristics, which is a complicate process especially under the large and widely varying current loading condition. Therefore, most of Shepherd's research in developing (2.15) was based on constant discharge current at rather low current levels. He tried to find the cut-off point beyond which the terminal voltage decreases very rapidly.

2.6.1.3 Unnewehr Universal Model [71]

To simply Shepherd's equation, Unnewehr proposed the universal model to approximate the terminal voltage in terms of f above the knee of voltage discharge curve,

$$E = E_0 - Kf - Ri \quad (2.16)$$

where R is the equivalent battery resistance in Ω and other symbols have the same meaning with that in (2.15).

Equation (2.16) is useful in modeling segments of the voltage discharge curve where a single straight line function as defined in this equation is inadequate over the desired range of f , as given in the following figure,

Fig. 2-9 Typical three-segment model of open circuit voltage characteristic.

In Fig. 2-9, E_v is the open circuit battery terminal voltage under no-load situation. It is defined by the first two terms of (2.16) as,

$$E_v = E_0 - Kf \quad (2.17)$$

By further examining equations (2.15) and (2.16), the universal battery model shown in Fig. 2-10 can be readily formed.

Fig. 2-10 Equivalent circuit of the universal model of battery.

In the above figure, the equivalent internal resistance of each battery is very complex function, which has been normalized and termed as an ‘ R -function’ and is expressed in the following equation,

$$R = R_0 - K_R f \quad (2.18)$$

where R is the total internal resistance. R_0 is the total internal resistance at fully charged condition. K_R is the experimental constant.

The symbol P in Fig. 2-10 represents exchanged power during charge or discharge process. It is related with current and voltage by the following equation,

$$\begin{aligned} \text{Discharge:} \quad I &= \frac{E_v - \sqrt{E_v^2 - 4RP}}{2R} \\ \text{Charge:} \quad I &= \frac{-E_v + \sqrt{E_v^2 + 4RP}}{2R} \end{aligned} \quad (2.19)$$

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

From basic electrical circuit theory, one can also obtain the maximum amount of power, $P_{\max}$, from Fig. 2-10 when external load resistance equals to the battery internal resistance R ,

$$P_{\max} = \frac{E_v^2}{4R} \quad (2.20)$$

2.6.2 Equivalent Circuit Models

Engineers have developed many equivalent circuit models for batteries for power system applications. Normally, the charge storing capacity of the battery is represented by a capacitor or by a capacitor in parallel with the ‘steady state battery’ which consists of a voltage source in series with a resistor. In the later case, the rate of change of voltage can be limited which cannot be achieved with a steady state model. The following sections describe several models which are commonly adopted in the analysis.

2.6.2.1 Simple Linear Battery Model [103]

The most commonly used battery model is shown in Fig. 2-11. In this model, the battery consists of open circuit voltage E_0 and a constant equivalent internal series resistance R . The terminal voltage is represented by V_0 . The value of V_0 can be obtained from the open circuit measurement. R can be measured from both the open circuit measurement and one extra measurement with load connected at the terminal when the battery is fully charged.

Though this model is widely adopted, it does not take the varying characteristic of the internal impedance of the battery with varying state of charge, electrolyte concentration and sulfate formation into consideration. This model is only applicable in some circuit simulation where the energy drawn out of the battery is assumed to be unlimited or where the state of charge is of little importance.

Fig. 2-11 Simple linear battery model.

2.6.2.2 Thevenin Battery Model [75, 103]

Thevenin model is another widely used battery equivalent circuit, which consists of an ideal open circuit voltage, internal resistance, capacitance and over-voltage resistance, denoted by E_0 , R , C_0 and R_0 respectively. The model is shown in Fig. 2-12. In this model, E_0 represents the equivalent EMF of the battery under no load. R represents the ohmic polarization. The over-voltage capacitance C_0 describes the double layer dynamics and the over-voltage resistance R_0 depicts the charge transfer losses. V_0 is the battery terminal voltage and I is the discharge current.

Thevenin model provides a high degree of accuracy while maintaining simplicity. But the major disadvantage of this model is that all circuit parameters are modeled as constants whereas they are functions of various battery conditions in fact.

Fig. 2-12 Thevenin battery model.

Based on Thevenin model, an improved discharge model applicable for short term has been proposed by Zhan *et al.* in [75]. The parameters have been modified to ensure higher accuracy with a parameter identification method.

In this short term model, the temperature is assumed to be constant and the SOD is about 100%. The parameters are highly nonlinear and mainly dependent on the discharge rate. They could be obtained from the measured battery output voltage during a series of step load tests. A typical lead-acid battery dynamic response to a step load can be described by,

$$V_0 = E_0 - RI - R_0 I \left(1 - e^{-\frac{t}{R_0 C_0}} \right) \quad (2.21)$$

2.6.2.3 Fourth Order Dynamic Model [102]

Giglioi *et al.* propose the fourth order dynamic model as shown in Fig. 2-13. The model is comprised of two parts: 1) current I_p flowing through R_p (electrolyte reaction), R_d and C_d (ohmic effect) and R_w and C_w (waste of energy); 2) current I_s flowing through R_s (self discharge).

Fig. 2-13 Fourth order battery model.

Though this model is sophisticated and accurate for simulation purpose, it still has some disadvantages in that: 1) a longer time is required for computation due to the high order of model and 2) modeling procedure is too complicated because it involves a lot of empirical parameters.

2.6.2.4 Improved Dynamic Model [76, 77]

As refinement of the dynamic model in the above sub-section, Ceraolo propose the reduced battery model with series connection of R - L - C networks. The third order model is shown in Fig. 2-14.

The battery terminal voltage is denoted by v_b . The model consists of linear reversible branch and nonlinear parasitic branch. The linear part is constituted by one R - C circuit, R_1 and C_1 , serially connected with the internal EMF, E_m , and two separated internal resistors, R_2 and R_0 . Note that all of these parameters are functions of the battery temperature, θ , and its state of charge (SOC) and/or depth of charge (DOC). The SOC and DOC of the battery model are defined by the following two formulations:

Fig. 2-14 Third order battery dynamic model.

$$SOC = 1 - Q_e / (K_c C_{0*}) \quad (2.22)$$

$$DOC = 1 - Q_e / C(I_{avg}, \theta) \quad (2.23)$$

where Q_e is the discharged charge from the battery and determined by $Q_e(t) = \int_0^t -I_m(\tau) d\tau$ (under the assumption that at $t = 0$, the battery is fully charged). K_c is an empirical coefficient. I_{avg} is the average discharge current. The battery capacity $C(I, \theta)$ after a constant discharge current under constant temperature condition could be calculated by,

$$C(I, \theta) = \frac{K_c C_{0*} \left(1 + \frac{\theta}{-\theta_f} \right)^\epsilon}{1 + (K_c - 1)(I / I^*)^\delta} \quad (2.24)$$

where C_{0*} is the nominal capacity of the battery at 0 °C, ϵ is also an empirical coefficient and θ_f indicates the freezing temperature, which can be typically selected to be -40 °C.

Note that the above capacity, SOC and DOC calculations are based on discharge procedure in [76, 77]. It is assumed in this thesis that they are also applicable for the charge procedure. The only difference is that the current direction reverses and the

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

positive sign of the current changed to negative but keeping the magnitude the same in the calculations.

The dynamic electrolyte temperature, θ , is determined by the following differential equation,

$$C_{\theta} \frac{d\theta}{dt} = P_s - \frac{\theta - \theta_a}{R_{\theta}} \quad (2.25)$$

where C_{θ} is the battery capacitance, R_{θ} is the thermal resistance between the battery and the environment, θ_a is the ambient temperature and P_s is the internally generated heat in the battery.

After SOC, DOC, and θ are determined by (2.22), (2.23) and (2.25) respectively, the battery parameters, E_m , R_0 , R_1 and R_2 can be determined by,

$$\left. \begin{aligned} E_m &= E_{m0} - K_E(273 + \theta)(1 - SOC) \\ R_0 &= R_{00} [1 + A_0(1 - SOC)] \\ R_1 &= -R_{10} \ln(DOC) \\ R_2 &= -R_{20} \frac{\exp[A_{21}(1 - SOC)]}{1 + \exp(A_{22}I_m / I^*)} \end{aligned} \right\} \quad (2.26)$$

where E_{m0} , K_E , R_{00} , A_0 , R_{10} , R_{20} , A_{21} and A_{22} are constants for the specific battery and could be obtained by experimental methods.

i_b in Fig. 2-14 is the battery input current. But only part of i_b , i.e. i_m , contributes to the energy storage charged into the battery. From Fig. 2-14 one can also achieve the following equation which relates the resistive current in the R - C circuit, i_1 , with i_m in terms of the battery parameters,

$$\tau_1 \frac{di_1}{dt} = i_m - i_1 \quad (2.27)$$

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage System and Distributed Generation Systems

where $\tau_1 = R_1 C_1$ is the time constant and could be assumed to be constant for a particular battery.

In summary, the reversible part of the battery model is determined by the following three dynamic equations,

$$\left. \begin{aligned} \frac{di_1}{dt} &= \frac{1}{\tau_1} (i_m - i_1) \\ \frac{dQ_e}{dt} &= -i_m \\ \frac{d\theta}{dt} &= \frac{1}{C_\theta} \left(P_s - \frac{\theta - \theta_a}{R_\theta} \right) \end{aligned} \right\} \quad (2.28)$$

The parasitic circuit built in this model is highly nonlinear and irreversible. The voltage across this branch, V_{PN} , is slightly differentiated with the battery terminal voltage by the resistance R_0 . And the current flowing through this branch, also the balance between i_b and i_m , could be approximated by the following expression,

$$I_p = V_{PN} G_{p0} \exp \left[V_{PN} / V_{p0} + A_p (1 - \theta / \theta_f) \right] \quad (2.29)$$

where G_{p0} , V_{p0} and A_p are also constants for a particular battery and could be obtained from battery manufacturing brochures.

2.7 Distributed Generation

As stated in Section 2.1, with constrains of environment and deregulation of the traditional power system, the existing T&D system cannot always satisfy costumer demands. To solve the conflict between the ever-increasing load demand and the limited transfer capability of the existing systems, DGs have gained popularity during the past decade due to their low cost and easy installation [32-43, 55, 56]. Commonly used DG technologies are introduced in this section. Among them wind energy generation has been rapidly developed for its abundance in the nature.

2.7.1 Micro-turbines [33]

A micro-turbine (MT) is a Brayton cycle engine with small capacity. It can operate using natural gas, propane and fuel oil to produce shaft power. The essential components of a MT consist of a compressor, combustor, recuperator, small turbine and generator, as shown in Fig. 2-15.

Fig. 2-15 Schematic diagram of dual shaft MT [33].

A dual shaft scheme is given in Fig. 2-15, and a single shaft design is also available in which the power produced in the expander is supplied to both the compressor and the load by a single shaft. Between these two schemes, however, the dual shaft design can be better controlled but with the cost of another rotating part and two more high speed bearings. Electricity is generated by a permanent magnet generator connected to the output shaft or by way of a synchronous generator driven by a gear box.

Unlike traditional combustion turbines, MTs operate at low temperature and pressure and faster speed (100,000 rpm). Therefore, they are under active development also due to the following attractive features: low capital cost, good efficiency (30-33%, LHV basis), modest emissions, possibility of thermal or electrical cogeneration in industry and in buildings and excellent modularity. The ratings of MT are generally of 0.4-1m³ in volume and 20-500 kW in size.

2.7.2 Photovoltaics [33]

Photovoltaic (PV) cells directly convert sufficiently energetic photons in sunlight to electricity. To generate sufficient power, large array areas are required since sunlight is a diffuse resource. Fortunately, this can be offset by zero cost of the fuel itself. With increasing development of semiconductor technology in the past 30 years, the prices of PV arrays have dropped by at least two orders of magnitude. But PV cells are still too expensive for widespread applications. However, in the mountainous areas where grid power does not exist or in developing countries where electricity infrastructure investments are lacking, PVs can provide power more efficiently than other alternatives.

The merits of PV systems include environment friendly operation without fossil fuel consumption, low temperature thermal cogeneration for space heating, excellent modularity, maintenance free except for incorporated energy storage system, and excellent part load efficiency. With different amount of cell arrangement, application range of PV systems varies from 1+ kW for household and small commercial applications to more than 20 kW for off-grid purposes. In developing countries, however, larger scale PV system can be achieved by installing more arrays.

Except for the above mentioned high price, the main barrier to PV usage is, among others, that its output electricity density is highly dependent on the environmental conditions. For example, with the change of sunlight within a single day, the generation of PV would fluctuate. This intermittent feature of power could be problematic when supplied to a load. Therefore, ESS such as battery is generally incorporated in a PV system.

2.7.3 Fuel Cells [40, 42]

A fuel cell (FC) is a device in which hydrogen and oxygen combined without combustion to generate electricity and provide thermal energy through electrochemical process. FC can be considered as a battery supplying electricity as long as its fuels are continued to supply. Unlike batteries, however, FC does not need to be charged for the consumed

Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems

materials during the electrochemical process because there materials are continuously supplied.

A wide variety of hydrogen-rich fuels can be used in FCs, such as natural gas, gasoline, biogas and propane. The most attractive property of FC is that it only provides true clean solution to electricity production outside the renewable sector. FC operates at different pressures and temperatures varying from atmospheric to hundreds of atmospheric pressure and from 20 to 200 °C respectively. The power ratings of different FC technologies are listed in Table 2-1.

Table 2-1 Comparison of different FC technologies [40]

Type	Power Range	Temperature	Application
Proton Exchange Membrane	2 to 250 kW	70 - 100 °C	Residential and automotive
Phosphoric Acid	~ 250 kW	~ 200 °C	Commercial, low temperature steam co-generation
Molten Carbonate	250 kW to 2 MW	~ 600 °C	Large commercial, small industrial
Solid Oxide	kW to ~ 20 MW	700 – 1000 °C	Utility, industrial

2.7.4 Wind Turbines [40, 42]

Wind energy is not a new form; it has been used for decades. But with the development of power electronic technologies and increasing concern on environment all over the world, wind generation has been increasingly developed during the past 10 years. This trend will continue in the next few decades, since wind energy is the only economically viable alternative energy source so far. A wind turbine (WT) consists of a rotor, turbine blades, generator, drive or coupling devices, shaft and the nacelle that contains the gearbox and

*Chapter 2 A Review of Works on Voltage Stability, Power Quality, Energy Storage
System and Distributed Generation Systems*

the generator drive. The ratings of state of the art wind turbines today range from 1 to 3.5 MW, with 4-5 MW turbines under development for offshore applications. WT(s) can be installed individually or combined together to form wind farms.

Among many advantages of wind energy, the followings are the most important ones that are of interest,

- Unlike the traditional electricity generation by using fuels such as coal and oil, the wind energy contributes to clean air, without contributing to acid rain and global warming.
- The wind source is abundant in nature.
- Cost of the traditional electricity generation will increase with the increment of fuel sources, but that of wind energy will decrease with development of WT technologies.

Similar with the output of PV arrays, the wind power also fluctuates due to the intermittent characteristic of wind speed [44-46, 48-50, 52, 53]. Therefore, to integrate such a variable amount of power with the utility, power electronic based inverters are commonly utilized to decouple the frequency difference between the wind power and mains grid. At current stage, variable speed wind turbines are gaining popularity due to their high transfer efficiency, especially at low wind speed conditions [70, 81, 82, 104, 105]. The following two variable speed topologies shown in Fig. 2-16 and Fig. 2-17 respectively are generally adopted [70, 82],

- Synchronous generator followed by a rectifier providing a regulated dc-link. The dc-link feeds a full power converter that produce AC power.
- Doubly-fed induction generator (DFIG) with a back-to-back power converter controlling the rotor power flow. The converter processes up to 0.3 p.u. power. To accommodate various transient grid interconnection and stability requirements in a robust and reliable way, converter ratings are typically approaching 0.5 p.u. power.

Fig. 2-16 Typical variable speed wind turbine integration topology with the use of a synchronous generator [70].

Fig. 2-17 Typical variable speed wind turbine integration topology with the use of DFIG [70].

With rapid development of wind technologies, wind power generation undergoes a change from small area to widespread integration with existing power systems. There are still a lot of technical challenges faced by researchers in generating reliable and stable wind power. As mentioned above, power fluctuation is a big challenge to be tackled [44-54, 80-82]. To attenuate the power fluctuation, a BESS based power buffer circuit is proposed in this thesis.

2.8 Conclusions

With increasing penetration of power electronic based devices in power systems, their negative influence on the voltage stability cannot be neglected any longer, because these devices are normally highly regulated and appear as constant power loads to the utility. Impacts of different types of load characteristics on voltage stability are briefly introduced in this Chapter. On the load side, the power electronic loads are also sensitive to the disturbances occurring in the upstream systems. The commonly considered issues pertaining to power quality have also been included in this part. As one of the countermeasures for voltage instability, power buffer is proposed as an effective solution. To guarantee the power quality of downstream constant power load, ESS must be connected with the power buffer. The commonly used ESS forms are reviewed in this Chapter. Focused on the cost-effective BESS, its basic electrochemical theory and electrical equivalent circuit are highlighted.

DGs are under active development to cater for ever-increasing load demand and environmental constraints. Some of promising technologies are introduced in this Chapter. The proposed power buffer system can play its role in the integration of DGs with the mains grid.

As shown in the following chapters, the BESS based power buffer circuit can decouple the load dynamics during upstream disturbances and hence voltage instability is enhanced. With the assistance of BESS, the power quality of the downstream loads is guaranteed as well. Furthermore, the function of proposed power buffer is extended for the integration of wind energy with mains grid. This present work will attempt to explore power buffer and BESS sizing issues in the voltage stability improvement, power quality enhancement and wind power fluctuation attenuation.

Chapter 3

Power Buffer Design for Load Dynamic Decoupling

3.1 Introduction

As mentioned in Chapter 2, with the increased installation of power electronic converter based loads, there would be a possibility that large number of loads would draw constant power from the utility regardless of the network conditions. These loads include computer power supplies and adjustable speed drive (ASD) etc. Such loads possess a common feature that the supply voltage needs to be regulated at a desired value. Therefore, such power electronic converter based loads frequently present constant power sink and they intend to draw constant power from the utility regardless of the utility conditions.

The above described constant power loads offer negative incremental impedance to the utility as derived in the following contents. At the original situation, the load drawn power, P , could be written in terms of terminal voltage, V , and current, I ,

$$P = VI \quad (3.1)$$

After a small disturbance in the voltage, ΔV , and resulting current variation, ΔI , the power relationship of the disturbed condition is,

$$P = (V + \Delta V)(I + \Delta I) \quad (3.2)$$

Based on the relationship given in (3.1) and assume that the second order item ($\Delta V \Delta I$) is negligible, one could obtain the equivalent impedance of the constant power load, R_e , from (3.2) as,

$$R_e = \frac{\Delta V}{\Delta I} = -\frac{V}{I} \quad (3.3)$$

Due to the negative incremental impedance presenting to the utility, these constant power loads are not desirable for the system operation. In the worst condition, when a voltage depression occurs in the source, the input current to the loads needs to be increased, which will depress the terminal voltage further. If such vicious circle continues and could not be stopped, voltage collapse in the system can happen at the end [14, 20].

From the point of view of the connected load, they are also adversely affected by the dynamic behavior in the utility. As mentioned before, the constant power loads are normally voltage regulated. If the source voltage deviates significantly from its nominal level, the protection circuit of power electronic devices will trip and power supply to downstream loads is interrupted, which is detrimental and should be avoided. One could find from the open literature that there are some topologies which have been proposed to mitigate the negative impact of voltage sags on the power electronic devices [17, 72-74].

From the above discussion, one can conclude that transient disturbances originated either in utility side or in load side will impact negatively on system dynamics, especially in weak power systems. Consequent instabilities and complete system collapse could happen during a transient due to the negative incremental impedance characteristic shown by the power electronic converter based, constant power loads.

One method to mitigate the effects of the disturbances is through the use of active dynamic power buffers [22, 66, 69]. A power buffer is an interface device between the load and the power system so that load dynamics seen by the system and source transients seen by the load are altered. The main idea originated from altering the impedance characteristic of buffer-load combination during the transient period through control of power electronic devices. From references [1-6, 8, 9], one finds that linear loads are much more ideal than their nonlinear counterparts from system stability point of view. Consequently, the buffer could be controlled to be of constant current or constant

impedance during the disturbance intervals. In either scenario, however, it is apparent that the amount of power supplied by the utility could not meet that demanded by the downstream loads in fault durations. The balance of power should be supplied by the energy storage system (ESS) connected to the power buffer. By doing so, input energy is absorbed and used in such a manner that system stabilities are not jeopardized. Only constant impedance scenario is focused in this study.

As for the power buffer topology, power buffer system could be built based on DC/AC or AC/DC voltage source inverter configuration, as described in [68]. The power section of the buffer in this study is built using a full-bridge pulse width modulated rectifier connected to the utility via a series R - L filter, as shown in Fig. 3-1.

Fig. 3-1 A load supplied through a buffer.

For schematic topology shown in Fig. 3-1, a new control scheme combining traditional control techniques and constant impedance control method [22] to effectively control the power flowing into the power buffer is proposed. In this Chapter, the control scheme will be elaborated and analyzed, followed by an introduction of input impedance determination method under fault conditions. The controller is designed to cater for both balanced and unbalanced fault situations. The simulation results to verify the validity of the proposed control scheme are also given in this Chapter. The design of the ESS will be discussed in the next chapter and only the controller design is focused in the following sections.

3.2 Modeling and Control of Three-phase Active Power Buffer

Presently, many power converter topologies [106-114] are used to supply electronically-controlled loads. Among such converters, those of which could shape the line currents to be sinusoidal form and control the dc-link voltage have been gaining popularity. The 3-phase boost converter topology shown in Fig. 3-1 would draw almost sinusoidal input currents with near unity power factor and would work in both rectifying and regenerating modes [115]. This converter topology is the preferred solution in many industry applications such as cranes, elevators and centrifuges. In this study, this converter topology is proposed to be used as an active buffer whereby it can act as an interface between the supply and load. It functions to decouple the load dynamics from the power system. Under healthy conditions, the converter transfers power while maintaining the dc-link voltage constant. However, after fault conditions are detected, the operating status of the buffer can be regulated such that the converter-load combination acts as a constant impedance device seen from the upstream power system. In this way, the converter decouples the negative impact of the downstream constant power loads on the upstream system. In order for it to be effective, it is necessary to deal with the power unbalance that would occur between the load and the supply, through an appropriate energy storage scheme. As mentioned in the above, only the controller design will be elaborated in this Chapter and the ESS will be dealt with in the next chapter. Therefore, the ESS part has not been shown in Fig. 3-1.

3.2.1 Power System under Healthy Conditions

3.2.1.1 Analysis

From Fig. 3-1, the following equations can be derived using the basic circuit laws.

Chapter 3 Power Buffer Design for Load Dynamic Decoupling

$$\left. \begin{aligned} v_{ga} - Ri_a - L \frac{di_a}{dt} &= v_{wa} \\ v_{gb} - Ri_b - L \frac{di_b}{dt} &= v_{wb} \\ v_{gc} - Ri_c - L \frac{di_c}{dt} &= v_{wc} \\ \frac{d}{dt} \left(\frac{1}{2} CV_{dc}^2 \right) + \frac{V_{dc}^2}{R_{eq}} &= v_{wa}i_a + v_{wb}i_b + v_{wc}i_c \end{aligned} \right\} \quad (3.4)$$

where, v_{ga} , v_{gb} , v_{gc} are the three-phase voltages at the point of common coupling (PCC) and v_{wa} , v_{wb} , v_{wc} denote the fundamental frequency components of the buffer terminal voltages. V_{dc} represents the dc-link voltage. The input currents are denoted by i_a , i_b and i_c in a-b-c reference frame. R and L are the filter resistance and inductance respectively. R_{eq} depicts the equivalent resistance of the load connected. C is the capacitance of the dc-link capacitor, which is used here as a filter but not as a medium for energy storage [22, 66, 69] to supply the mismatch power between the source and load. The first three equations in (3.4) are obtained based on the Kirchhoff's voltage law across the filter impedance and the fourth is using power balance.

In the positive phase sequence system, the conventional a-b-c to d-q-0 transformation as given in the following form is adopted,

$$\begin{bmatrix} S_d \\ S_q \\ S_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin \omega t & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \quad (3.5)$$

where, S_a , S_b and S_c in the right hand side are electrical quantities, such as voltage or current in the a-b-c reference frame and S_d , S_q and S_0 are the transformed quantities in d-q-0 frame. ω is the supply angular frequency in rad/s.

Chapter 3 Power Buffer Design for Load Dynamic Decoupling

Based on the above transformation, equation (3.4) can be transformed from a-b-c reference frame to d-q-0 synchronous frame as follows,

$$\left. \begin{aligned} L \frac{di_d}{dt} &= v_{gd} - Ri_d + \omega Li_q - v_{wd} \\ L \frac{di_q}{dt} &= v_{gq} - Ri_q - \omega Li_d - v_{wq} \\ \frac{1}{2} C \frac{dV_{dc}^2}{dt} &= \frac{3}{2} v_{wd} i_d + \frac{3}{2} v_{wq} i_q - \frac{V_{dc}^2}{R_{eq}} \end{aligned} \right\} \quad (3.6)$$

Based on (3.6) the control scheme under normal condition is proposed as shown in Fig. 3-2. In this control system, the d-axis current regulates the transferred real power and hence is used to maintain the dc-link voltage. The q-axis current is used to achieve variable reactive-power transfer.

Fig. 3-2 Control system under healthy conditions [116, 117].

The control structure can be seen as a ‘cascaded’ one. $C_1(s)$ and $C_2(s)$ are the inner current loop controllers and $C_3(s)$ is the outer voltage loop controller. These controllers are proportional-integral type, details of which will be elaborated in the following two sub-

sections. Note that the couplings of i_d , i_q in (3.6) have been considered in the PI controller design.

3.2.1.2 Inner Current Control Loop Design

The inner current control system, $C_1(s)$, is shown in Fig. 3-3. It is a traditional PI controller where suitable PI constants (k_{p1} and k_{i1}) can be obtained using Bode plots and pole-zero maps to guarantee stable performance [118]. Note that the PI constants are system dependent thus their effects will be illustrated in simulations for a given system.

Fig. 3-3 Inner current control loop.

The controller $C_2(s)$ is designed in the similar manner as of $C_1(s)$.

3.2.1.3 Outer Voltage Control Loop Design

For the outer control loop, in order to reduce the non-linear second-order control system to a linear first-order one, small signal linearization is carried out for (3.6) around the steady state point determined by V_{gd} , V_{gq} , I_d , I_q , V_{wd} , V_{wq} and V_{dc} . The variable quantities corresponding to the above ones are denoted by the prefix δ . Substituting the new state quantities, $V_{gd} + \delta V_{gd}$, $I_d + \delta I_d$ etc. into (3.6) and separating the steady state equation from the small signal parts, one could obtain the small signal model and the steady state model as given in the following two equations respectively,

Chapter 3 Power Buffer Design for Load Dynamic Decoupling

$$\left. \begin{aligned} \frac{d\delta i_d}{dt} &= \frac{1}{L} \delta v_{gd} - \frac{\omega}{Q} \delta i_d + \omega \delta i_q - \frac{1}{L} \delta v_{wd} \\ \frac{d\delta i_q}{dt} &= \frac{1}{L} \delta v_{gq} - \omega \delta i_d - \frac{\omega}{Q} \delta i_q - \frac{1}{L} \delta v_{wq} \\ \frac{d\delta v_{dc}}{dt} &= \frac{3V_{wd}}{2CV_{dc}} \delta i_d - \frac{2}{R_{eq}C} \delta v_{dc} + \frac{3I_d}{2CV_{dc}} \delta v_{wd} \end{aligned} \right\} \quad (3.7)$$

and

$$\left. \begin{aligned} V_{gd} - RI_d + \omega LI_q - V_{wd} &= 0 \\ V_{gq} - RI_q - \omega LI_d - V_{wq} &= 0 \\ \frac{3}{2} V_{wd} I_d - \frac{V_{dc}^2}{R_{eq}} &= 0 \end{aligned} \right\} \quad (3.8)$$

where, Q is the filter quality factor given by $Q = \frac{\omega L}{R}$. It is to be noted that the steady state quantities in (3.7) are determined by (3.8).

In s -domain and based on the small signal system equation (3.7), the transfer function from the PWM terminal voltage to the dc-link voltage could be derived as,

$$\delta v_{dc} = \frac{\left(3LI_d \left(\left(s + \frac{\omega}{Q} \right)^2 + \omega^2 \right) - 3V_{wd} \left(s + \frac{\omega}{Q} \right) \right) \delta v_{wd} - 3\omega V_{wd} \delta v_{wq}}{LCV_{dc} \left(\left(s + \frac{\omega}{Q} \right)^2 + \omega^2 \right) \left(s + \frac{2}{R_{eq}C} \right)} \quad (3.9)$$

Assuming fast dynamics and unity gain in the inner loop, the outer voltage control loop could be designed based on (3.7) and (3.9), as given in Fig. 3-4. Again the suitable PI constants for $C_3(s)$, k_{p3} and k_{i3} , are selected using the classical techniques similar to those applicable in $C_1(s)$ and $C_2(s)$ design. Besides maintaining the stability of the outer control loop, the PI constants for $C_3(s)$ have to be selected to keep V_{dc} at nominal level in healthy conditions.

Fig. 3-4 Outer voltage control loop.

As the last part of this sub-section, after d- and q-components of the PWM converter terminal voltage obtained from the discussion above, they will be transformed back to a-b-c frame and PWM switching signals are formed from v_{wa} , v_{wb} and v_{wc} by dividing v_{dc}^* to control the front-end converter. The reverse transformation from d-q-0 to a-b-c used in this study is given as,

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} \cos \omega t & -\sin \omega t & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & -\sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} S_d \\ S_q \\ S_0 \end{bmatrix} \quad (3.10)$$

3.2.2 Power System under Upstream Fault Conditions

3.2.2.1 Analysis

In this part, a control method that decouples the load and system dynamics during the fault conditions will be proposed, which will mitigate the adverse effects of the constant power load on the system. In case of a general unbalanced fault, it is also necessary to avoid the influence of negative sequence current on the power system. Hence the

proposed scheme needs to control the positive and negative sequence systems separately. The controller applicable for the positive sequence system will be elaborated in the following part and followed by that for the negative sequence system given in the last part of this sub-section. For the positive sequence system, the constant impedance control method is described as follows.

Fig. 3-5 Parallel equivalent circuit of power buffer.

Suppose the equivalent circuit of the power buffer-load combination, seen from the AC terminal, is as shown in Fig. 3-5. The model is used to analyze the control of the power buffer under fault conditions. The terminal voltage $\dot{V}_g$ and input current $\dot{I}_{in}$ are related through the equivalent circuit parameters R_{in} and X_{in} .

As shown in Fig. 3-5, $\dot{I}_{in}$ can be separated into real and reactive parts as I_R and I_X , the phasor diagram of which with reference to $\dot{V}_g$ is shown in Fig. 3-6.

Fig. 3-6 Phasor diagram to describe the buffer-load combination under fault condition.

The real- and reactive-parts of $\dot{I}_{in}$ determine the real and reactive power flowing into the buffer terminal respectively, where,

$$\left. \begin{aligned} P_{in} &= \frac{V_g^2}{R_{in}} \\ Q_{in} &= \frac{V_g^2}{X_{in}} \end{aligned} \right\} \quad (3.11)$$

If the filter resistance, R , and inductance, X , are included in the controller design and under assumption that the filter resistance is negligible, the equivalent circuit can also be represented in series form as given in the following figure,

Fig. 3-7 An equivalent circuit of power buffer with the external filter included.

The parametric values in Fig. 3-7 are related with those in Fig. 3-5 by the following two equations,

$$\left. \begin{aligned} R_1 &= \frac{R_{in} X_{in}^2}{R_{in}^2 + X_{in}^2} \\ X_1 &= \frac{R_{in}^2 X_{in}}{R_{in}^2 + X_{in}^2} - X \end{aligned} \right\} \quad (3.12)$$

Based on Fig. 3-7 one could calculate the buffer terminal voltage $\dot{V}_w$ based on the following equation,

$$\dot{V}_w = \frac{R_1 + jX_1}{R_1 + j(X + X_1)} \dot{V}_g \quad (3.13)$$

Chapter 3 Power Buffer Design for Load Dynamic Decoupling

Taking $\dot{V}_g$ as the reference vector and after some rearrangement, the d- and q-components of $\dot{V}_w$ can be derived,

$$\left. \begin{aligned} v_{wd} &= \frac{R_1^2 + X_1(X + X_1)}{R_1^2 + (X + X_1)^2} v_{gd} \\ v_{wq} &= -\frac{R_1 X}{R_1^2 + (X + X_1)^2} v_{gd} \end{aligned} \right\} \quad (3.14)$$

As described in (3.11), the real- and reactive-powers flowing into the power buffer can be regulated by the equivalent impedance of R_{in} and X_{in} . On the other hand, the adjustment of R_{in} and X_{in} and hence that of R_1 and X_1 , will impact the PWM voltage, $\dot{V}_w$. Based on such intrinsic relationships, one could regulate the power drawn by the buffer through adjusting the PWM converter terminal voltage $\dot{V}_w$ based on R_{in} and X_{in} values, so that the power flow is regulated but is not determined by the power absorbed by the load.

It is suffice to say that in this way the power buffer-load combination is seen as constant impedance from the source. Transient mismatch in power can be compensated using an energy storage system such as capacitor bank or other ESS connected to the dc-link, thus creating a favorable situation in terms of system stability. Note that the additional power source connected to the load has not been included in the present analysis, but it is assumed that it would be there to provide the power, should it be needed. The determination of R_{in} and X_{in} will be described in the next sub-section.

Usually power system faults are unsymmetrical and they would cause voltage- and current-unbalances in the load side. Without adequate measures taken, such unbalances will impact negatively on the downstream load and upstream utility as well [25]. To mitigate the negative influence of the unbalance, the power buffer could be controlled to draw zero negative sequence current. In the negative sequence system, a PI controller is used to reduce the negative sequence current drawn by the buffer-load combination.

Combining the control schemes for positive- and negative-sequence frames described above, the overall control system under fault situations is depicted in Fig. 3-8. The negative sequence current control loop is also shown in the bottom part of Fig. 3-8.

Fig. 3-8 Power buffer control system under faulty conditions.

The current references in the negative sequence system, i_d^{-*} and i_q^{-*} are set to zero and suitable PI constants selected to control the negative sequence current to zero and hence mitigate the negative influence of unbalanced current on the load side. The superscripts '+' and '-' in Fig. 3-8 denote the quantities in positive- and negative-sequence systems respectively.

Once d- and q-components of the power buffer terminal voltages in positive- and negative-sequence systems are obtained, one could form v_{wd} and v_{wq} using the superposition law as shown in Fig. 3-8. Finally, the reverse transformation from d-q-0 to a-b-c reference frame as given in (3.10) is applied. The PWM control signals are obtained from v_{wa} , v_{wb} and v_{wc} by dividing v_{dc}^* .

3.2.2.2 R_{in} and X_{in} Selection

As addressed above, R_{in} and X_{in} determine the power flow into the buffer-load combination during a fault.

One can start from the determination of R_{in} . From the real power point of view, the power supplied by the source, P_s , and consumed by the load, P_l , could be expressed in the following two equations respectively,

$$P_s = 3 * \frac{V_{g0}^2}{R_{in}}$$

$$P_l = \frac{V_{dc0}^2}{R_{eq}}$$

based on the power balance between source and load sides, one could equate P_s and P_l to obtain R_{in} as

$$R_{in} = \frac{3 * V_{g0}^2 * R_{eq}}{V_{dc0}^2} \quad (3.15)$$

where, R_{eq} is the equivalent load resistance. V_{g0} is the nominal voltage magnitude at PCC and V_{dc0} is the nominal dc-link voltage.

As for X_{in} , to operate the power buffer-load combination in UPF seen from PCC, X_{in} value should theoretically be selected at infinity. In practice, one can select it to be a much larger value, say, 10 times of R_{in} .

Based on the equivalent circuit in Fig. 3-5, the input current during the fault disturbance can be derived as,

$$I_{in} = V_g \sqrt{\frac{1}{R_{in}^2} + \frac{1}{X_{in}^2}} \tag{3.16}$$

From (3.16) one can readily find that the input current will decrease proportionally with PCC voltage, V_g during the fault interval, which reduces the voltage drop across the front-end filter and it prevents the negative incremental impedance effect shown by CPLs, as described in Section 3.1. In this manner, voltage stability of the system is enhanced.

3.3 Simulation Results

3.3.1 Voltage Sag with 90% Positive Phase Sequence and 20% Negative Phase Sequence Components

To illustrate the effectiveness of the scheme, a power system model based on Fig. 3-1 was constructed using Matlab/Simulink programming language. The parameters used in the simulation are given in the following table,

Table 3-1 Parameters used for power buffer simulations [119]

Supply Voltage (line-line)	150 V (1.0 p.u.)
Resistance of The Filter	0.314 Ω (0.00503 p.u.)
Inductance of The Filter	1 mH (0.00503 p.u.)
Resistance of Load	62.4 Ω (1.0 p.u.)
DC-Link Capacitor	10 mF (0.00510 p.u.)

Using a control tool-box in Matlab, PI constants were determined as $k_{p1} = -1$ and $k_{i1} = -50$ for the inner control loop and $k_{p3} = 0.076$ and $k_{i3} = 0.25$ for the outer control loop respectively. The corresponding Bode plots of the inner loop, $\frac{I_d}{I_d^*}$, and the outer loop,

$\frac{V_{dc}}{V_{dc}^*}$, are shown in Fig. 3-9 (a) and (b) respectively. From these two figures, one can see that, 1) both inner and outer loops are low pass systems, 2) the gain and phase margins of the inner loop are infinity dB and 100 degrees respectively. Such large gains guarantee

Chapter 3 Power Buffer Design for Load Dynamic Decoupling

the stability of the inner closed-loop, 3) the gain and phase margins of the outer loop are 60 dB and 22.5 degrees, which reveals that the outer voltage loop is also stable, and 4) the cut-off frequencies of the inner loop and the outer loop are 250 rad/sec and 50 rad/sec respectively, which means that the response of the inner current loop is 5 times faster than that of the outer voltage loop. This is in accordance with the assumption of fast dynamic and unity gain of inner loop in the outer loop design.

Fig. 3-9 Bode-plots of (a) $\frac{I_d}{I_d^*}$ and (b) $\frac{V_{dc}}{V_{dc}^*}$.

Under normal conditions, the dc-link voltage is maintained at 380 V. At $t = 4.0$ s, suppose an unbalanced sag with 90% of positive phase sequence and 20% of negative phase sequence voltage occurs at the utility side. To mitigate the negative effect of the load to the source, the control system of the power buffer is switched from constant power mode to the constant impedance mode. The equivalent impedance is obtained from (3.15) based on the recorded voltages, V_{g0} , and power, P_l at normal conditions. At $t = 5.0$ s, the sag is removed and the system is restored to the normal situation. The simulation results are given in Fig. 3-10. It is to be noted that only the fundamental frequency components are presented in this these figures and this statement also applies to Fig. 3-11.

Fig. 3-10 Simulation results of power buffer with resistor load, (a) PCC voltage, (b) DC-Link voltage, (c) input current at time of sag initiation, (d) input current at time of sag removal.

The PCC voltage waveform is shown in Fig. 3-10 (a). It can be seen from Fig. 3-10 (b) that the dc-link voltage indeed drops during the fault interval by using the constant impedance control method. Fortunately, for that PCC voltage is above 0.9 p.u., the dc-link voltage is kept above the pre-set lower limit, $v_{dc,lower} = 342$ V or 0.9 p.u., under which the power electronic based converter can work properly [72-74]. Fig. 3-10 (c) and (d) show the input current waveforms at the initial period of the sag and subsequent to the removal

of the sag respectively. From the plots, it could be readily found that the input current is controlled balanced and that I_{in} drops to 90% of its nominal value, which corresponds to the analysis based on (3.16). Note that in this simulation, R_{in} is always kept at its pre-fault value of $14.58\ \Omega$ during the fault condition and X_{in} value is $145.8\ \Omega$ to operate the system in near UPF. The results shown in Fig. 3-10 verify the effectiveness of the constant impedance control method in mitigating voltage collapse by reducing the input current during the fault period.

3.3.2 Voltage Sag with 80% Positive Phase Sequence and 20% Negative Phase Sequence Components

To further verify the effectiveness of the constant impedance control method under a more severe disturbance, suppose the disturbance has resulted in the PCC voltage of 80% in positive sequence and 20% in negative sequence respectively. Subsequent simulations produce results which are shown in Fig. 3-11.

Fig. 3-11 Simulation results of power buffer with resistor load, (a) PCC voltage, (b) DC-Link voltage, (c) input current at time of sag initiation, (d) input current at time of sag removal.

The dc link voltage waveform is given in Fig. 3-11 (b) which shows that in this severe sag situation, the dc-link voltage cannot be maintained above the pre-set limit. This is not acceptable for the proper operation of the power electronic based converters [72-74]. To overcome this situation, ESS needs to be connected and this aspect is described in the next chapter. I_{in} profiles at the beginning and end of the sag incident are shown in Fig. 3-11 (c) and (d) respectively, from which one can find that even at such severe unbalanced sag situation, I_{in} can still be controlled to be balanced with its amplitude depressing to 80% of its original level. Note that in this simulation, R_{in} is kept at the nominal value of $14.58 \, \Omega$ and X_{in} is $145.8 \, \Omega$ to operate the power buffer in UPF during the sag interval.

3.4 Conclusions

The power buffer concept provides a means by which the negative influence of CPLs on the utility side can be mitigated. At healthy conditions, the power buffer adjusts the power factor of the buffer-load combination and maintains the dc-link voltage at its original level. During utility disturbances, by using the constant impedance control method to control the real and reactive power flow into the power buffer, the buffer would be able to

Chapter 3 Power Buffer Design for Load Dynamic Decoupling

decouple the dynamics of CPLs from upstream sources, avoiding the negative incremental impedance feature shown by the CPLs where no countermeasures are taken. The controller is also designed to mitigate the negative influence of the unbalanced current on the load side, should it be an unbalanced disturbance. Effectiveness of the proposed controllers has been verified by simulation results presented in this Chapter. Power difference between the load demand and that supplied by the utility can be compensated by a suitable ESS connected to the power buffer, which will be elaborated in the Chapter 4.

Chapter 4

Power Buffer System Incorporated with BESS

4.1 Introduction

In Chapter 3, three phase active power buffer concept has been introduced. A constant impedance control method applicable for the power buffer in mitigating the negative impact of constant power load on the utility is proposed, which decouples the load dynamics from the upstream source and prevents the voltage instability or voltage collapse in the worst situation.

However, energy storage system (ESS) has not been taken into consideration in the previous design. With depth of voltage sag increasing, the previous scheme may not be valid because the dc-link would not be maintained within the preset limits.

To cater for the deep sag conditions and improve the power buffer ride-through ability, a new power buffer scheme with ESS is proposed and examined in this Chapter. Though the power buffer controller concept is similar with that presented in the previous scheme, the impedance is kept constant over the sag intervals. Under this condition, the power supplied by the source will be reduced by square of the voltage magnitude assuming that the buffer system is always operated in UPF mode. The power shortfall between the load demand and that supplied by source is compensated by the ESS connected to the dc-link.

In [22, 66, 69], the authors assume that the capacitor is of sufficient capacity to meet the power shortfall and analyzed the depth of voltage sag with relationship to the sustaining time of the power buffer. If used in high power systems, however, the energy capacity of

the capacitor can be limited and it should be augmented by a high energy density alternative [69]. In this study, a battery energy storage system (BESS) is implemented to function as ESS in the buffer system.

In next section, the power circuit of the buffer system is elaborated and its operation principle is presented. Following that the load ride-through capability is analyzed as it relates to the battery state of discharge. Simulation results based on Matlab/Simulink are given in Section 4.4 to verify the effectiveness of the proposed scheme.

4.2 The New Power Buffer Scheme and its Operation Principle

The power buffer scheme to be studied in this Chapter is as shown in Fig. 4-1,

Fig. 4-1 Schematic diagram of a new BESS based power buffer-load scheme.

From Fig. 4-1 one finds that the power circuit of the buffer system is similar to that given in last Chapter, except that a battery bank is connected to the dc-link and the upstream source has been included. In this figure, v_{sa} , v_{sb} and v_{sc} are the upstream source voltage and the source inductance is L_s . Note that L_s depends on the fault level at the point of common coupling (PCC). On the load side, the regulated power electronic loads are modeled as a single constant power sink as shown in Fig. 4-1. Other symbols have the same meaning with those in Fig. 3-1.

Chapter4 Power Buffer System Incorporated with BESS

The control system of the new power buffer follows the method that has been proposed in last Chapter. Only a brief introduction of the buffer operation principle and controller design will be given in this Chapter.

Under normal conditions, the power buffer is operated in constant power mode. The front-end rectifier is controlled to maintain the dc-link voltage at nominal level to supply the downstream load.

When a voltage sag occurs, the power buffer is designed such that the buffer-load combination is switched from the constant power mode to constant impedance mode. Under latter mode, the buffer-load combination could be represented by a parallel connection of R_{in} and X_{in} , as shown in the following figure. In this figure, $\dot{V}_s$ is the upstream voltage and $X_s = \omega L_s$ is the source impedance which depends on the fault level at the PCC.

Fig. 4-2 Equivalent circuit of power buffer-load combination in parallel representation.

Similar to Chapter 3, R_{in} and X_{in} in this Chapter are determined through the following equation,

Chapter4 Power Buffer System Incorporated with BESS

$$\left. \begin{aligned} R_{in} &= \frac{V_{g0}^2}{P_l} \\ X_{in} &= \frac{V_{g0}^2}{Q_l} \end{aligned} \right\} \quad (4.1)$$

where P_l and Q_l are the constant real- and reactive-power seen from PCC respectively. V_{g0} is the nominal PCC voltage under healthy condition. Note that under UPF operation, X_{in} value is very much larger than R_{in} . At steady-state, R_{in} and X_{in} can be readily determined using (4.1) because V_{g0} , P_l and Q_l are readily measurable. The determined values would be the equivalent impedance of the load-buffer combination prior to (say) voltage sag.

After R_{in} and X_{in} values are obtained, one can substitute them into equations (3.12) - (3.14) to derive d- and q-components of front-end rectifier terminal voltage v_{wd} and v_{wq} .

Consequently, the real and reactive power flows into the power buffer can be regulated through control of $\dot{V}_w$ in the following way. Under fault conditions, the input impedance at the buffer-load terminal is maintained constant at the known pre-sag value $R_{in} + jX_{in}$. This is achieved through controlling the buffer PWM to produce necessary $\dot{V}_w$ as given in (3.14). In this way, the power drawn by the buffer is governed by R_{in} and X_{in} and is not determined by the power absorbed by the load. In this way, the buffer-load combination behaves as a constant impedance seen from the source.

The present approach achieves the power flow control by ensuring the input impedance of the buffer-load combination to be exactly the same as that pre-fault. In this approach, the power flowing into the PCC will be proportional to the square of the PCC voltage magnitude, V_g . Therefore, the input power drawn by the buffer-load combination will decrease during the sag event. Any mismatch in power between that from the PCC and the load demand can be compensated by energy storage system connected to the dc-link, thus creating a favorable situation in terms of system stability.

The control system structure of the power buffer during sag event based on the above approach concept is similar to that given in last Chapter of Fig. 3-8.

The above control scheme will be extended in this chapter to include the battery energy storage system to provide load ride-through.

4.3 Analysis of the Power Buffer System

From Fig. 4-2, one obtains the phasor diagram depicted in Fig. 4-3 (a),

Fig. 4-3 Phasor diagram describing the power buffer at (a) non-unity power factor and (b) unity power factor conditions at the PCC.

$\dot{V}_s$ represents the upstream voltage and X_s is the source impedance. As the input impedance of the buffer-load combination remains constant at the pre-sag value when an upstream fault occurs, I_{in} would decrease in proportion with the sag depth. As explained earlier, this constant impedance mode prevents V_g from depressing as much as that under the constant power case. The power supplied by the upstream source, however, will be reduced to a level corresponding to the square of the sag voltage magnitude. From Fig. 4-3 (a) and for a given sag, maximum real power drawn from V_s occurs when the power flow from source at the PCC is at unity power factor, i.e., $\dot{I}_{in}$ is in phase with $\dot{V}_g$. The

Chapter4 Power Buffer System Incorporated with BESS

phasor diagram depicting such maximum power transfer condition is shown in Fig. 4-3 (b) and the maximum power level P_{max} is

$$P_{max} = \frac{V_g^2}{R_{in}} \quad (4.2)$$

Hence, in the proposed scheme, once a sag is detected, i.e. $V_g < V_{g,min}$, where $V_{g,min}$ is typically 0.95 p.u., the power buffer is switched from constant power mode to constant impedance mode.

The next focus of this Chapter is to examine the requirement of the energy storage system when the buffer operates in the constant impedance mode.

4.3.1 Circuit Model of Buffer with the Battery Storage

Unlike work carried out in [22, 66, 69] where capacitor has been proposed as the media of energy storage, battery has been considered for incorporation in the buffer scheme in this Chapter. With its competitive price, lead-acid battery has become a widely used energy storage device in power systems [57, 59-62, 64]. Furthermore, with its higher energy storage capacity than a capacitor, battery is deemed to be more suitable for high power applications required in buffer.

The proposed buffer scheme will now be described. There are several electrical models pertaining to lead-acid battery described in the literature [71, 75-77, 99-101]. The most commonly used model is the Thevenin equivalent representation shown in Fig. 4-4. In the model, E is the no-load battery voltage and R_s is the internal resistance. R_p represents the non-linear contact resistance of the plate to electrolyte and C_p , the capacitance of the parallel plates of the electrolyte and electrode. In practical battery operation, these battery parameters are dependent not only on the state of discharge (f) of the battery, but also on the discharge current and the temperature at which the battery operates. In the present

Chapter4 Power Buffer System Incorporated with BESS

analysis, however, since it is expected that the battery is to function over a very short duration, one may assume E , R_s , R_p and C_p are constant over the operational period in order to simplify the analysis. The battery model would be suitable for use in analyzing the behavior of the buffer.

Fig. 4-4 Circuit model of lead-acid battery bank.

From load side of Fig. 4-1 and Fig. 4-4, one can obtain the following equations based on basic circuit laws,

$$\left. \begin{aligned} i_{cp} &= C_p \frac{dv_{cp}}{dt} \\ i_{cap} &= C \frac{dv_{dc}}{dt} \\ i_{btr} &= \frac{1}{R_s} (E - v_{dc} - v_{cp}) \\ i_{btr} &= i_{cp} + \frac{v_{cp}}{R_p} \\ i_{btr} - i_{cap} &= \frac{\Delta p}{v_{dc}} \end{aligned} \right\} \quad (4.3)$$

where v_{cp} , v_{dc} are the voltages across the dc-link and that across the capacitor C_p of the battery respectively. i_{btr} , i_{cp} and i_{cap} are the currents in the battery branch, in the capacitor sub-branch and in the dc-link capacitor respectively. Let Δp be the mismatch power

Chapter 4 Power Buffer System Incorporated with BESS

between the power buffer and the constant power load. Under the UPF operating condition at the buffer terminals,

$$\Delta p(t) = P_l - P_{\max} \quad (4.4)$$

where P_l represents the load power demand and $P_{\max}$ is the maximum power defined in (4.2).

After some re-arrangements of the above set of equations, one can obtain the following equations to describe the dynamic behavior of the power buffer during the transient period,

$$\left. \begin{aligned} \frac{1}{2} C \frac{dv_{dc}^2}{dt} &= -\Delta p + \frac{E}{R_s} v_{dc} - \frac{1}{R_s} v_{dc}^2 - \frac{v_{dc}}{R_s} v_{cp} \\ C_p \frac{dv_{cp}}{dt} &= \frac{1}{R_s} E - \left(\frac{1}{R_s} + \frac{1}{R_p} \right) v_{cp} - \frac{1}{R_s} v_{dc} \end{aligned} \right\} \quad (4.5)$$

4.3.2 Steady-State Analysis of Power Buffer Operation

From (4.5), the equations describing the steady state of the buffer are

$$\left. \begin{aligned} \Delta P - \frac{E}{R_s} V_{dc,ss} + \frac{1}{R_s} V_{dc,ss}^2 + \frac{V_{dc,ss} V_{cp,ss}}{R_s} &= 0 \\ \frac{1}{R_s} E - \left(\frac{1}{R_s} + \frac{1}{R_p} \right) V_{cp,ss} - \frac{1}{R_s} V_{dc,ss} &= 0 \end{aligned} \right\} \quad (4.6)$$

where ΔP , $V_{dc,ss}$ and $V_{cp,ss}$ represent steady state values of Δp , v_{dc} and v_{cp} of (4.5) respectively.

From (4.6), one can derive the relationship between the steady state voltages across C_p , the dc-link voltage ($V_{dc,ss}$) and the mismatch power ΔP in terms of the battery parameters as

Chapter 4 Power Buffer System Incorporated with BESS

$$V_{cp,ss} = \frac{R_p(E - V_{dc,ss})}{R_s + R_p} \quad (4.7)$$

$$\Delta P = \frac{V_{dc,ss}(E - V_{dc,ss})}{R_s + R_p} \quad (4.8)$$

Equation (4.8) relates ΔP and the steady state value of the dc-link voltage $V_{dc,ss}$ through the battery parameters, E , R_s and R_p . In carrying out this analysis, it is assumed that the transient process following the switching in battery bank has ceased. This means that only the battery resistance needs to be considered. The universal battery model given in [71] is then applicable:

$$\left. \begin{aligned} E &= E_0 - Kf \\ R_b &= R_0 - K_R f \end{aligned} \right\} \quad (4.9)$$

In this model, E_0 and R_0 are the open circuit terminal battery voltage and the total equivalent battery resistance at full charge respectively. R_b is the total internal resistance which depends on the state of discharge (SOD) or f . K and K_R are experimentally obtained constants. When the battery is fully charged, $f = 0$. $f > 0$ indicates that the battery is in the discharged state. Conversely, $f < 0$ shows the battery is over-charged.

Substituting (4.9) into (4.8), the relationship between $V_{dc,ss}$, f and ΔP can be obtained,

$$V_{dc,ss} = \frac{E_0 - Kf + \sqrt{(E_0 - Kf)^2 - 4(R_0 - K_R f)\Delta P}}{2} \quad (4.10)$$

Equation (4.10) allows one to determine $V_{dc,ss}$ for given battery f and ΔP . A typical family of curves based on (4.10) is shown in Fig. 4-5. The base value of power is selected as the nominal power demand of the load. The base value of the dc voltage is based on the fact that the modulation index of the rectifier under pre-sag condition is at typical value of 0.8.

Fig. 4-5 Steady-state DC-link voltage ($V_{dc,ss}$) as a function of battery state of discharge (f) and power mismatch.

From Fig. 4-5 one notes that for a given battery state of discharge f , $V_{dc,ss}$ decreases with ΔP . On the other hand, for a given ΔP , $V_{dc,ss}$ reduces with increment of f .

Furthermore, by substituting (4.2) and (4.4) into (4.10), one obtains

$$V_{dc,ss} = \frac{E_0 - Kf + \sqrt{(E_0 - Kf)^2 - 4(R_0 - K_R f)(P_l - V_g^2 / R_{in})}}{2} \quad (4.11)$$

Equation (4.11) relates the variations in $V_{dc,ss}$ with the voltage sag magnitude V_g , the battery discharge state f and the constant impedance (R_{in}) considered in Section 4.2. Again typical curves describing (4.11) is shown on Fig. 4-6. In this figure, it is seen that for a given sag (V_g), $V_{dc,ss}$ increases with the decrease of f . This means that the battery which has a lower f will have a higher internal EMF, lower internal resistance and can therefore supply more power than a battery with higher f for given E_0 and R_0 .

Fig. 4-6 Steady-state DC-link voltage ($V_{dc,ss}$) as function of battery state of discharge (f) and sag/swell level.

In practice, to guarantee satisfactory operation of power buffer, it is also necessary to ensure that $V_{dc,ss}$ should be kept within a range (say $\pm 10\%$) around its nominal value [72-74]. This condition must be satisfied for the given battery f . These limits are shown on Fig. 4-6 as curves AB and CD. These two boundaries define the operation range of the power buffer for different battery SOD. Hence the feasible operating region of the buffer-load combination is within the area ABCD. One could use the information given in this figure to readily estimate the most severe sag or swell the buffer-load combination would ride-through under steady-state conditions. For example, if the battery SOD $f = 0.4$, from Fig. 4-6, one notes that any voltage disturbance which causes V_g to lie within the range 0.82 p.u. (sag) to well beyond 1.4 p.u. (swell) can be readily dealt with by the buffer, and the load demand can be met with $V_{dc,ss}$ within the acceptable limit. As the battery SOD can be continuously monitored, a possible implementation scheme would entail the on-line measurement of f , and subsequently use it to predict the load-ride through level. As the buffer is used to provide the short-fall in power during the load ride-through, f will increase over time. The ride-through capacity of the buffer would be updated

continuously so that one could determine the instant that the battery bank needs to be re-charged, in order to meet some pre-specified load ride-through criteria.

In fact, one should also consider the inevitable delay from the instance of the detection of the voltage disturbance until the sag is confirmed. Based on ITIC/CBEMA curve [24], typical satisfactory operation of sensitive loads can still be maintained if the delay is less than a quarter cycle of the power frequency and the dc-link voltage is quickly restored soon after. Over this initial sag interval of a quarter cycle, the load-buffer will be allowed to operate under constant power mode. This is because voltage instability is unlikely to be very much affected over this relatively short interval. Once the sag event is confirmed and its severity identified, the buffer-load combination is then switched into constant impedance mode. By doing so, not only the utility voltage stability is enhanced, the constant power load demand is also met by the use of battery energy compensation.

While the above is concerned with voltage sag incident, similar analysis can be carried out for voltage swell, i.e. $V_g > 1$ p.u. as shown in Fig. 4-6.

4.3.3 Transient Performance of Power Buffer

As mentioned in the last sub-section, one expects the variation of dc-link voltage (V_{dc}) is within a narrow range around its nominal value; consequently, it is reasonable to analyze the transient performance of (4.5) in its small-signal form as,

$$\left. \begin{aligned} \frac{d\delta v_{dc}}{dt} &= -\frac{2V_{dc,ss} + V_{cp,ss} - E}{R_s C V_{dc,ss}} \delta v_{dc} - \frac{1}{R_s C} \delta v_{cp} - \frac{1}{C V_{dc,ss}} \delta \Delta p \\ \frac{d\delta v_{cp}}{dt} &= -\frac{1}{R_s C_p} \delta v_{dc} - \frac{1}{C_p} \left(\frac{1}{R_s} + \frac{1}{R_p} \right) \delta v_{cp} \end{aligned} \right\} \quad (4.12)$$

From this result, stability and transient performance of the system following the battery switch-in can be analyzed. From (4.12), one can obtain the transfer function

Chapter4 Power Buffer System Incorporated with BESS

$$\frac{\delta v_{dc}}{\delta \Delta p} = -\frac{1}{CV_{dc,ss}} \frac{s + \alpha}{s^2 + (\alpha - \beta)s - \gamma - \alpha\beta} \quad (4.13)$$

where,

$$\alpha = \frac{R_s + R_p}{R_s R_p C_p}, \beta = \frac{E - 2V_{dc,ss} - V_{cp,ss}}{R_s C V_{dc,ss}}, \gamma = \frac{1}{R_s^2 C C_p} \quad (4.14)$$

From the characteristic equation of (4.13) and using the Routh criterion [120], stability of the buffer-battery system would be guaranteed if and only if

$$\alpha - \beta > 0 \quad (4.15)$$

$$-\alpha\beta - \gamma > 0 \quad (4.16)$$

From (4.15), one obtains the necessary condition for stability as

$$V_{dc,ss} > \frac{R_s R_p C_p}{(R_s + R_p)^2 C + R_p C_p (2R_s + R_p)} E \quad (4.17)$$

Substituting (4.7) into (4.16), $V_{dc,ss}$ must also satisfy the condition

$$V_{dc,ss} > 0.5E \quad (4.18)$$

However, upon closer examination it is noted that the following in-equality relationship is always valid,

$$(R_s + R_p)^2 C + R_p C_p (2R_s + R_p) > 2R_s R_p C_p \quad (4.19)$$

Hence, one can conclude once (4.18) is satisfied, (4.17) would be satisfied automatically.

Under battery discharge mode, $\Delta P > 0$. From (4.8), it can be determined that indeed, $V_{dc,ss} > 0.5E$. Hence, (4.18) is always satisfied. Thus the buffer system is always stable and v_{dc} will settle to a constant value following a step change Δp .

Chapter4 Power Buffer System Incorporated with BESS

Furthermore, one can also examine the characteristic equation of (4.13) to obtain the damping ratio ζ where

$$\zeta = \frac{\alpha - \beta}{2\sqrt{-\alpha\beta - \gamma}}$$

Substituting (4.14) into the above expression and since $E \approx V_{dc,ss}$, one can derive the following equation for ζ in terms of the battery parameters, R_s , R_p and C_p .

$$\zeta = \frac{R_s C + R_p C + R_p C_p}{2\sqrt{R_s R_p C C_p}} \quad (4.20)$$

From (4.19), the following in-equality is obtained

$$(R_s C - R_p C_p)^2 + R_p^2 C^2 + 2R_p^2 C C_p > 0 \quad (4.21)$$

One can readily show that $\zeta > 1$. Hence it can be concluded that the system is always over-damped. It is also possible to quantify how each of the battery parameters affects ζ . For example, by partial differentiating (4.20) with respect to R_s , one obtains

$$\frac{\partial \zeta}{\partial R_s} = \frac{R_s C - R_p C - R_p C_p}{4R_s \sqrt{R_s R_p C C_p}} \quad (4.22)$$

Since C_p is of the order of F but C is of the order of mF, the term $R_p C$ can be ignored. Thus $R_p C_p \gg R_s C$ can be assumed in the numerator of (4.22). Therefore (4.22) can be simplified as

$$\frac{\partial \zeta}{\partial R_s} = \frac{-R_p C_p}{4R_s \sqrt{R_s R_p C C_p}} \quad (4.23)$$

The sensitivity function in (4.23) has a negative value indicating that with an increase in R_s there would be a decrease in the damping ratio of the system.

Similarly, the same approach can be applied to study the sensitivity of ζ to R_p and C_p as follows,

Chapter4 Power Buffer System Incorporated with BESS

$$\frac{\partial \zeta}{\partial R_p} = \frac{R_p C + R_p C_p - R_s C}{4 R_p \sqrt{R_s R_p C C_p}} \quad (4.24)$$

$$\frac{\partial \zeta}{\partial C_p} = \frac{R_p C_p - R_s C - R_p C}{4 C_p \sqrt{R_s R_p C C_p}} \quad (4.25)$$

Both sensitivity functions have positive values. It indicates that ζ increases with R_p or C_p .

Finally, the characteristic equation shows that there are two real negative roots

$$\left. \begin{aligned} s_1 &= \frac{\beta - \alpha - \sqrt{(\alpha + \beta)^2 + 4\gamma}}{2} \\ s_2 &= \frac{\beta - \alpha + \sqrt{(\alpha + \beta)^2 + 4\gamma}}{2} \end{aligned} \right\} \quad (4.26)$$

On closer examination, it is noted that $\alpha > 0$, $\beta < 0$ and $\gamma > 0$. Hence it can be concluded from (4.26) that $s_1 \ll s_2$ and the dynamic performance of the system is primarily dominated by the pole s_1 .

From [75, 100], it is shown that R_s , R_p and C_p vary with the discharge current. The parametric variations are expressed in terms of the battery discharge current. From the data shown in [75] for example, one can obtain the values of R_s , R_p and C_p and from which the damping ratio and dominant pole variations with the discharge current can be determined. Typical results are shown in Fig. 4-7.

Fig. 4-7 Variations of damping ratio and dominant pole with battery discharge current.

From the figure, one finds that ζ reaches its maximum value at a discharge current of some 153 A in this example before it progressively decreases as the current increases. The dominant pole changes little as the discharge current increases to 153 A and decreases greatly with further increment of the current.

4.4 Simulation Results

To verify the validity of the operation scheme proposed, a power buffer model based on Fig. 4-1 is built using Matlab/Simulink software. The parameters used in the simulations are shown in Table 4-1.

Table 4-1 Parameters for Constant Power Load Simulations [69, 75]

Supply voltage (line-line)	415 V (0.480 p.u.)
Resistance of buffer filter	61.33 mΩ (0.00821 p.u.)
Inductance of buffer filter	0.97 mH (0.04 p.u.)
DC-Link capacitor	10 mF (0.043 p.u.)
Battery EMF (E_0)	864 V (1.0 p.u.)
Internal resistance $R_{s(1000A)}$	0.216 Ω (0.0289 p.u.)
Over-Voltage resistance $R_{p(1000A)}$	0.072 Ω (0.00965 p.u.)
Over-Voltage capacitance $C_{p(1000A)}$	1.39 F (0.000307 p.u.)
Internal resistance $R_{s(153A)}$	0.461 Ω (0.0618 p.u.)
Over-Voltage resistance $R_{p(153A)}$	0.288 Ω (0.0386 p.u.)
Over-Voltage capacitance $C_{p(153A)}$	6.94 F (0.0000614 p.u.)
Capacity of constant power load	100 kW (1.0 p.u.)
Proportional factor for $C_1(s)$ and $C_2(s)$	- 0.1 (V/A)
Integral factor for $C_1(s)$ and $C_2(s)$	- 10 (V/A)
Proportional factor for $C_3(s)$	0.05 (A/V)
Integral factor for $C_3(s)$	25 (A/V)
Proportional factor for $C_4(s)$ and $C_5(s)$	- 0.1 (V/A)
Integral factor for $C_4(s)$ and $C_5(s)$	- 1 (V/A)

Under pre-sag condition, the dc-link voltage is maintained at 859 V and the modulation index is 0.79. A constant power load of 100 kW is connected to the buffer. Incidents of 10-cycle upstream unbalanced faults are used to study the performance of the buffer system. The data of the buffer system is taken from [69] while that of the battery is from [75].

The case shown is pertaining to a severe unbalanced voltage sag which has resulted in 40% positive phase sequence plus 20% negative phase sequence components. The control method of the power buffer is switched from constant power mode to constant impedance

Chapter4 Power Buffer System Incorporated with BESS

mode after the sag is confirmed, one quarter cycle from sag initiation. The simulation results are shown in Fig. 4-8.

Fig. 4-8 Buffer-load response under an unbalanced voltage sag of 40% positive phase sequence and 20% negative phase sequence (a) PCC voltage, (b) DC-Link voltages, with and without the battery, (c) input current, (d) input real and reactive power at PCC, (e) real power supplied by battery bank, (f) DC-Link voltage performance at different discharge current values.

The PCC voltage waveform in Fig. 4-8 (a) shows the occurrence of the unbalance voltage sag. Fig. 4-8 (b) shows that the dc-link voltage (solid line) decreases soon after the sag initiation but the battery connected to the dc-link subsequently boosts the voltage and supplies the mismatch power. V_{dc} is kept within the desirable range despite the constant impedance control method used during the sag period. Additionally, for comparison reason, the dc-link voltage without the battery switch-in is shown in Fig. 4-8 (b). One notes that under a severe sag, the dc-link voltage decreases to zero almost instantaneously following the sag occurrence. If this occurs, the load would be disturbed. To prevent such an occurrence, the battery bank has to be switched in once sag is confirmed in order to maintain the dc-link voltage at the desirable level. The input current waveform of Fig. 4-8 (c) shows that under the unbalanced source voltage condition, through the negative frequency sequence controller in the control system, the input current drawn from the supply is controlled to be essentially balanced. Since the buffer control method is under constant impedance mode over the sag period, the input current drops to 40% or some 80 A, which is proportional to the magnitude of the sag voltage. The large buffer current

overshoot observed in Fig. 4-8 (c) is caused by the controller mode change and the switching in of the battery following the sag occurrence. The quarter cycle delay assumed between the instant of the detection of fault and the buffer control mode change with the subsequent battery switch-in has contributed to the large transient. In the present study, the transient current reaches some 90% above its pre-sag value for a very short duration. Therefore, the switching device within the buffer has to be rated to carry this large current for a momentary period.

Fig. 4-8 (d) and (e) show the variations of input real and reactive power from the upstream system into the buffer and the real power supplied by the battery, respectively. It can be seen from Fig. 4-8 (d) that the real power supplied by the upstream is reduced to 16 kW or 16% of the nominal value over the sag period, and that the input reactive power at the PCC is controlled to be zero in pre- and post-sag periods in order to satisfy the UPF operation. From Fig. 4-8 (d) and (e) one also finds that the real power supplied by the upstream system during pre-fault duration meets the load demand of 100 kW and the combined power supplied by the utility and the battery during sag is maintained at 100 kW, the mismatch power being supplied by the battery energy storage system.

Finally, to verify the influence of the state of discharge and thus the battery parameters on the transient performance of buffer system, two sets of battery parameters corresponding to different discharge current conditions are analyzed in the simulation. The results are shown in Fig. 4-8 (f). Comparing the V_{dc} response curve under discharge current of 1000 A with that of 153 A, one notes that the response of the buffer-battery with 153 A case is less well-damped than that of 1000 A discharge current. This verifies the finding described in Sub-section 4.3.3.

4.5 Conclusions

A new scheme for the design and operation of power buffer is proposed. Under normal network condition, the buffer operates under constant power control mode. When a fault occurs, the buffer is switched into constant impedance control mode, so that the upstream

Chapter4 Power Buffer System Incorporated with BESS

is decoupled from the constant power load in order to mitigate the negative impact of the constant load on the system voltage stability. The mismatch power between the upstream source and that demanded by the load during the sag is supplied by the battery bank connected to dc-link. By doing so, the input current is allowed to decrease with the decrease of PCC voltage so that voltage stability of the power system can be enhanced. Furthermore, analytical expressions governing the load ride-through capability and the battery state-of-discharge have been derived. Through an analysis of the buffer-battery transient response characteristic, the most onerous condition under which the load-ride through can be achieved has been identified. The steady state and transient performances of the proposed buffer system are verified through simulations. The results have shown the effectiveness of the proposed scheme in mitigating voltage instability induced by fault disturbances occurring in the upstream supply system.

Chapter 5

Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

5.1 Introduction

Stability of power systems has always been an important consideration, especially when it involves the transmission of power over long distances. The problem is compounded somewhat in recent years when a significant proportion of present-day industrial loads are equipped with power-conditioning capabilities. As discussed in the last two chapters, these loads usually draw constant power regardless of their terminal voltage level. In the event of a fault in the system, the depressed voltage will result in an increase in the load current. This would lead to an increase in the voltage drop across the source impedance, which in turn causes a further decrease in load terminal voltage. Load voltage stability would be impacted negatively if no counter-measures are taken. Furthermore, constant power loads also affect rotor-angle stability of power systems, in a manner very much different from that if the loads were to behave like a constant-impedance type. Hence it is not surprising to note that the impacts of loads on power system are attracting the interest of many researchers [1-9].

In an attempt to address the above-mentioned stability problem due to the presence of constant power loads, the use of a power buffer system through which the loads are supplied has been proposed in [22, 66, 69]. The buffer consists of two back-to-back connected converters which are interconnected by a DC-link.

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

The success of such a buffer system must include a suitable energy storage system to compensate for any of the mismatch in power between the constant power load and that supplied by the upstream system, during and after a fault.

The conceptual buffer scheme and its operational principle are described in the next section. A method to determine the capacity of the storage system necessary to ensure the success of the scheme is given in Sections 5.3-5.5. Numerical examples are used in Section 5.6 to illustrate the applicability of the proposed scheme.

5.2 Description of the Buffer Scheme

While recognizing practical power systems are highly complex, the generic two-generator power system network shown in Fig. 5-1 is nevertheless convenient for use in illustrating the operating principle of the buffer scheme. The two generators, G_1 and G_2 , are interconnected by the transmission link between Buses 1 and 2. Power generated by G_1 and G_2 are denoted as P_{G1} and P_{G2} respectively. Losses in the transmission system are assumed negligible. As the focus of this work is on the buffer scheme, details of the generators and their control systems will not be described here except in Section 5.6, where detailed generator model representations have been included in the illustrative examples.

In the present problem formulation, one recognizes there would be load demands that are considered essential. The nature of these demands would be such that supply to them must not be disturbed under specified momentary voltage disturbance conditions, which are typically caused by faults or large load switchings. Indeed, consideration for supplying such loads has given rise to the idea of Custom Power and the concept of Power Quality Control Center (PQCC) [78, 79]. In whatever form, provisions would have to be made in the networks so that these loads, denoted as S_1 and S_2 in Fig. 5-1, can ride-through such voltage sag/swell disturbances. Hence, S_1 and S_2 would draw constant real powers P_{S1} and P_{S2} respectively, regardless of the status of the power system. The provision considered in this work to ensure S_1 and S_2 real power demands are met is through the arrangement of the buffers, also shown in the figure. The remaining loads D_1

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

and D_2 at Buses 1 and 2 have no such stringent power requirement. The steady-state powers drawn by these loads are denoted as P_{D1} and P_{D2} . D_1 and D_2 could be assumed to be of constant impedance type in this network model.

Fig. 5-1 Schematic diagram of a two-generator network system with power buffers.

Having met the demands P_{S1} and P_{D1} , suppose Bus 1 has surplus generation from G_1 while Bus 2 has insufficient in-feed from G_2 to meet the demands P_{S2} and P_{D2} . The deficiency is imported from G_1 , via the link, by the amount P_{12} . The steady-state power flow pattern is therefore as shown in Fig. 5-1.

5.2.1 Buffer Scheme to Achieve Stability Enhancement

Next consider the function of the buffers. In the proposed scheme, the power buffers are based on pulse width modulation (PWM) controlled converters. Under healthy system conditions, the buffers operate under constant power mode to meet the demands P_{S1} and P_{S2} , through control of the respective front-end converter while maintaining the DC-link

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

voltages, v_{dc1} and v_{dc2} , at their nominal levels. This will ensure proper operations of the downstream converter-loads S_1 and S_2 . It is through the control actions of the converters that S_1 and S_2 will enjoy excellent supply quality, an attribute similar to that described in [78] for the so-called super-premium loads.

When a fault occurs in the transmission link, the voltage in the network would be depressed. From the instant of the fault incipient and the initial transient period of (say) a few seconds, the governor control systems of G_1 and G_2 will generally be too slow to respond appreciably. Thus the input mechanical powers to the generators can be considered constant. On the other hand, the excitation systems of the generators would usually be able to adjust the respective generator internal EMF, since the control systems are designed to maintain the generators' terminal voltage constant. Even with the actions of the excitation systems, however, a severe fault would cause the power P_{12} transmitted through the link to be greatly reduced. If both S_1 and D_1 were to behave like constant impedance type, Bus 1 load demand would also reduce as the load terminal voltage is depressed during fault. Therefore, the surplus energy resulting from the constant input mechanical power and the reduced output electrical power P_{G1} will accelerate the rotor of G_1 . To reduce the power imbalance at Bus 1 and since S_1 is of constant power type, it is proposed that Power Buffer 1 is to operate in the following way. When G_1 rotor accelerates during fault, Power Buffer 1 will be designed to operate under constant power mode. In this way, the load demand at Bus 1 will be higher compared to that without the buffer. This will reduce the acceleration of G_1 .

At Bus 2, the situation is the reverse to that of Bus 1 which is, for the same fault and without Buffer 2, the net effect would be for G_2 to decelerate with respect to G_1 . This is the classical 2-machine transient stability situation. Depending on the pre-fault power transfer level, fault clearing time (among other factors), there is a danger G_1 and G_2 may go into first-swing instability condition. Hence, in order to mitigate the possibility of instability, Power Buffer 2 will be designed to operate under constant impedance mode during fault so that Bus 2 total load demand will be reduced. The constant impedance mode means that viewed from the source into the Buffer 2 input terminals, it will have the

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

same load impedance value as that before fault [65]. In this way, the deceleration in G_2 would be less compared to the case without Buffer 2, when the constant power demand P_{S2} has to be met by an increase in P_{G2} since P_{12} is reduced. Thus by forcing Buffer 1 into constant power mode and Buffer 2 into constant impedance mode during fault, the rotor speed difference, and the rotor angle difference, between G_1 and G_2 can be reduced in comparison to the case when the buffers are not used.

The buffers can also be designed to operate on the same principle following fault clearance when the network re-adjusts its bus voltages and power flows. When there is accelerating power acting on G_1 and the generator speed increases, Power Buffer 1 is to operate under constant power mode. Conversely, when the generator decelerates, the buffer is switched to constant impedance mode. The role of Buffer 2 is to regulate the speed of G_2 in a similar manner. Repeated switchings between the two buffer modes continue until the network settles into a new steady-state operating condition.

The consequence of the proposed buffer operation is illustrated in Fig. 5-2. Based on the two-machine example of Fig. 5-1, the figure shows the generator rotor angle difference between G_1 and G_2 caused by a temporary fault on the transmission link, with and without the buffer scheme. The parameters of the power system and buffers are given in the numerical sample part. In this example, a 10-cycle 3-phase fault on the link has resulted in the loss of synchronism in the generators when the buffers are not used. The instability is avoided once the buffer scheme has been incorporated. It clearly demonstrates that the buffer systems do function as effective network system dampers or stabilizers.

Fig. 5-2 Rotor angle difference ($\theta_1 - \theta_2$) between G_1 and G_2 : with and without power buffers.

5.2.2 Buffer Scheme to Achieve Improved Load Ride-through

Accompanying the above network stabilization function, one should also consider the impacts of the constant demands, P_{S1} and P_{S2} of loads S_1 and S_2 , on the buffers. As stated earlier, during fault or post-fault, there would be instances when the buffer(s) have to operate under constant impedance mode. Over these instances, since P_{S1} (or P_{S2}) has to be catered for, the shortfall between P_{S1} (or P_{S2}) and the power supplied by the upstream utility has to be met. This is achieved by drawing power from the energy storage system (ESS) mentioned earlier. There are several possible storage mediums which could be used, such as super-capacitors and flywheels. In this investigation, only lead-acid battery energy storage system (BESS) has been considered. The reason is BESS is one of the most cost-effective and well-established technology for large-scale energy storage

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

applications [57, 59-62, 64]. The BESS is shown connected across the DC-link of the buffers in Fig. 5-1.

In the scheme, the buffers function to guarantee constant power supply to S_1 and S_2 . When Buffer 1 operates under constant impedance mode for example, BESS₁ supplies any shortfall in power for S_1 when the network voltage is depressed. This will decrease the DC-link voltage, v_{dc1} . However, in order to ensure S_1 supply quality is not affected, v_{dc1} has to be kept within certain limit, denoted by the range $[v_{dc,lower}, v_{dc,upper}]$, or the inverter associated with S_1 will operate outside its control range. If the latter case occurs, the inverter protection system will be triggered and supply to S_1 will be disrupted. This occurrence must be avoided. It should be noted that the extent v_{dc1} will deviate from its nominal value depends very much on the capacity of BESS₁. Hence, it remains to determine the respective BESS capacity so that the buffers are able to help S_1 and S_2 loads ride through the worst fault conditions the scheme is to cater for. In this way, the power buffers will ensure both stability enhancements while the supply quality to the loads will be guaranteed. A method to determine the BESS capacity will be described in the next sections.

A point worth mentioning is when a buffer is operating under the constant impedance mode during upstream fault condition, the control system for the buffer is designed in such a way that viewing from the source, the buffer-load combination has a positive effective resistive value [65] as described in last two chapters. This means that real power flow is from the source to the buffer: there is no danger of reverse power flow from the buffer into the upstream fault.

In the following three sections, the BESS model used in this investigation will be given first, followed by a proposed method to determine the BESS capacity which is based on the needs of the protected load.

5.3 BESS Model Description

There are several models proposed by researchers which can be used to describe the behavior of a battery cell [71, 75-77, 99-101]. The model proposed in [75] pertaining to lead-acid battery cell is chosen for incorporation in the present buffer scheme. The reason for the selection is since the focus is on transient stability enhancement; the time-scale of interest is well within the so-called short-term response characteristics of the battery cell model given in [75]. The adopted cell circuit model is reproduced in Fig. 5-3 (a). As shown, $E_{b,i,j}$ is the cell open circuit EMF, internal resistance $R_{s,i,j}$ represents the ohmic resistance due to polarization in the battery cell, $R_{p,i,j}$ and $C_{p,i,j}$ are used to describe the discharge transfer loss and dynamics between parallel plates of electrodes and electrolyte respectively.

In Fig. 5-3 (b), typical response of the cell terminal voltage $v_{b,i,j}$ to a step battery cell current change $i_{b,i,j}$ is shown. One notes that a step increase in $i_{b,i,j}$ would result in the cell terminal voltage $v_{b,i,j}$ to decrease almost instantaneously, before it approaches its steady state value in an exponential manner. In describing this behavior, the battery cell terminal voltage change due to the step current has been described in [75] in the following way:

$$v_{b,i,j} = E_{b,i,j} - R_{s,i,j}i_{b,i,j} - R_{p,i,j}i_{b,i,j}(1 - e^{-\frac{t}{\tau_{i,j}}}) \quad (5.1)$$

where $\tau_{i,j}$ is the time constant of battery cell and

$$\tau_{i,j} = R_{p,i,j}C_{p,i,j} \quad (5.2)$$

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

(a)

(b)

Fig. 5-3 (a) Schematic showing the interconnection of lead-acid battery cells in the BESS, and (b) Typical response of battery cell terminal voltage $v_{b,i,j}$ to a step change in cell discharge current $i_{b,i,j}$.

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

Typically, $\tau_{i,j}$ is of the order of 0.2 s to a few seconds, depending on the step current change magnitude. Table 5-1 shows the typical parametric values of the cell resistances and capacitance [75] and the corresponding $\tau_{i,j}$.

Table 5-1 Battery Parameters Used in the Simulations [75]

ΔI (A)	R_s (Ω)	R_p (Ω)	C_p (F)	τ (s)
25	0.005	0.015	20	0.3
50	0.008	0.003	900	2.7
100	0.0052	0.003	1000	3
200	0.0032	0.002	1000	2
400	0.0022	0.001	750	0.75
600	0.002	0.0008	600	0.48
800	0.0018	0.00075	400	0.3
1000	0.0015	0.0007	200	0.14

The BESS would be constructed from series-parallel connection of the individual battery cells. The connection diagram is given in Fig. 5-3 (a). Consider the i^{th} series cell on the j^{th} parallel branch of the BESS. Each cell model consists of its EMF, $E_{b,i,j}$, resistances $R_{s,i,j}$ and $R_{p,i,j}$, and capacitance $C_{p,i,j}$, as explained earlier.

Suppose the BESS has m cells connected in series in each branch, and a total of n parallel branches, as shown in Fig. 5-3 (a). The BESS terminal voltage is denoted by v_{dc} since the BESS is assumed connected directly across the DC-link of the buffer system. The BESS equivalent circuit, based on Fig. 5-3 (a), is given in Fig. 5-4. Assume all the mn cell units are identical, and one obtains the BESS internal parameters denoted by E_b , R_s , R_p and C_p , expressed in terms of the cell parameters, as follows,

$$\left. \begin{aligned} E_b &= mE_{b,i,j} / n \\ R_s &= mR_{s,i,j} / n \\ R_p &= mR_{p,i,j} / n \\ C_p &= nC_{p,i,j} / m \end{aligned} \right\} \quad (5.3)$$

Fig. 5-4 Equivalent circuit of BESS.

In the manner similar to (5.1), the BESS terminal voltage $v_{dc}(t)$ can be described in terms of the BESS parameters and step change in the BESS current i_b as

$$v_{dc} = E_b - R_s i_b - R_p i_b (1 - e^{-\frac{t}{\tau}}) \tag{5.4}$$

where τ is the time constant of the BESS and

$$\tau = R_p C_p \tag{5.5}$$

The circuit model of the BESS is amenable for analysis, except for one complication. In adopting the equivalent circuit model, it has been stated earlier that the cell resistance and capacitance values are not constant but are functions of the current step magnitude. In fact, the state of discharge of the cell and temperature at which the cells operate also affect the parametric values. Fortunately, the latter two factors could be considered constant over a fault disturbance event because the duration of the fault plus its clearance is usually too short for the battery temperature and discharge state to vary appreciably. In this way, the values of the parameters would only depend on the discharge current step magnitude. In what follows, it will be assumed that the parametric values of R_s , R_p and C_p would be known for given current step magnitude. The information can be obtained either from the cell manufacturer or obtained through experimental measurements.

5.4 DC-link Voltage Determination

As explained in section 5.2, it is important the DC-link voltage must be maintained within limits. Using the equivalent circuit model developed earlier, the BESS terminal voltage can be determined as follows. In transient stability study and in a step-by-step manner, the quantities $P_{12}(t)$, $P_{G1}(t)$ and $P_{G2}(t)$ are readily calculated. At Buses 1 and 2, P_{S1} and P_{S2} are known constants whereas P_{D1} and P_{D2} vary with the respective bus voltage magnitude squared. One can therefore calculate $P_{b1}(t)$ and $P_{b2}(t)$ as follows,

$$\left. \begin{aligned} P_{b1}(t) &= P_{S1} - P_{G1} + P_{12} + P_{D1} \\ P_{b2}(t) &= P_{S2} - P_{G2} - P_{12} + P_{D2} \end{aligned} \right\} \quad (5.6)$$

Consider one of the buffers and omit the subscript 1 or 2 to simplify expressions to follow. Approximate the continuous function $P_b(t)$ over the interval of interest T by a series of $N+1$ values: $P_{b(0)}, P_{b(1)}, \dots, P_{b(k)}, \dots, P_{b(N)}$ at times $t_{(0)}, t_{(1)}, \dots, t_{(k)}, \dots, t_{(N)}$. Fig. 5-5 shows the $(k-1)^{\text{th}}$, k^{th} and $(k+1)^{\text{th}}$ intervals. Assume equal time interval so that each segment is of duration

Fig. 5-5 Approximate $P_b(t)$ by individual power pulses $\bar{P}_{b(k)}$.

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

$$\Delta t = \frac{T}{N}$$

In this way, $P_b(t)$ may then be approximated by N pulses, each of duration Δt and the magnitude of each pulse is given by

$$\bar{P}_{b(k)} = \frac{P_{b(k-1)} + P_{b(k)}}{2} \quad k = 1, 2, \dots, N \quad (5.7)$$

Hence $\bar{P}_{b(k)}$ will be the power pulse applied over the k^{th} time interval. Accordingly, the battery current step change due to $\bar{P}_{b(k)}$ is

$$\bar{I}_{b(k)} = \frac{\bar{P}_{b(k)}}{v_{dc(k-1)}} \quad k = 1, 2, \dots, N \quad (5.8)$$

where $v_{dc(k-1)}$ is the BESS terminal voltage at the end of the $(k-1)^{\text{th}}$ time interval.

Next, $v_{dc(k)}$ can be generated through the following step-by-step and iterative method. Consider v_{dc} at the end of the first time step, i.e., $k = 1$. The initial BESS terminal voltage is given by $v_{dc(0)} = E_b$, assuming the battery current is zero initially and the BESS open-circuit voltage is known. As shown in Fig. 5-6, suppose the first power pulse, $\bar{P}_{b(1)}$, is positive. From (5.8) the corresponding battery current step change is given by

$$\bar{I}_{b(1)} = \frac{\bar{P}_{b(1)}}{v_{dc(0)}} \quad (5.9)$$

With the known step current, one can utilize the corresponding BESS parametric values, denoted as $R_{s(1)}$, $R_{p(1)}$ and $C_{p(1)}$, to determine the DC-link voltage at the end of first time interval using (5.4), i.e.

$$v_{dc(1)} = v_{dc(0)} - R_{s(1)} \bar{I}_{b(1)} - R_{p(1)} \bar{I}_{b(1)} (1 - e^{-\frac{\Delta t}{\tau_{(1)}}}) \quad (5.10)$$

where $\tau_{(1)} = R_{p(1)} C_{p(1)}$.

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

Fig. 5-6 Estimation of dc-link voltage at the end of 1st time interval.

The net v_{dc} variation $\Delta v_{dc(1)}$ at the end of the 1st time step is derived from (5.10),

$$\Delta v_{dc(1)} = v_{dc(1)} - v_{dc(0)} = \Delta v_{dc(1,1)}^+ = - \left(R_{s(1)} \bar{I}_{b(1)} + R_{p(1)} \bar{I}_{b(1)} (1 - e^{-\frac{\Delta t}{\tau(1)}}) \right) \quad (5.11)$$

where $\Delta v_{dc(1,1)}^+$ denotes the voltage variation caused by the first positive current pulse at the end of first time interval $t(1)$.

Fig. 5-6 shows that the v_{dc} varies over the first time interval. Since $\bar{P}_{b(1)}$ is assumed constant over the interval Δt , the battery current will in turn vary with v_{dc} . Taking this factor into consideration, an inner-loop calculation step is suggested in the numerical solution method, so as to improve the accuracy of the DC-link voltage calculation. The inner-loop calculation is described as follows.

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

Use $v_{dc(1)}$ obtained from (5.10) as an intermediate variable, one can derive the corresponding battery current as,

$$\bar{I}'_{b(1)} = \frac{\bar{P}_{b(1)}}{v_{dc(1)}} \quad (5.12)$$

Then update $\bar{I}_{b(1)}$ by taking the average value of $\bar{I}_{b(1)}$ from (5.9) and $\bar{I}'_{b(1)}$ from (5.12). One then re-calculates $\Delta v_{dc(1)}$ using (5.11) and $v_{dc(1)}$ through (5.10) with the new $\bar{I}_{b(1)}$. The above improved battery current and terminal voltage calculation procedure is repeated until $v_{dc(1)}$ converges. Since it has been known that the battery time-constant τ is much larger than the step-size Δt , therefore it is envisaged that this inner-loop calculation will only result in relatively minor corrections in $\bar{I}_b$ during the iterative process. Hence convergence can be attained rather quickly.

From the start of 2nd time interval, i.e. $t > t_{(1)}$, $\bar{P}_{b(2)}$ is introduced as shown in Fig. 5-7 (b). A new battery current step change $\bar{I}_{b(2)}$ is introduced where

$$\bar{I}_{b(2)} = \frac{\bar{P}_{b(2)}}{v_{dc(1)}}$$

$v_{dc(1)}$ is obtained from (5.10). However, in order to completely simulate the net effect of the first pulse, it is necessary to combine the effects shown in Fig. 5-7 (a) with that of Fig. 5-7 (c), i.e. to introduce a negative current step of magnitude $\bar{I}_{b(1)}$ at the start of the 2nd time interval, as shown in top of Fig. 5-7 (c). This negative step current produces a voltage response at the end of 2nd time interval thus

$$\Delta v_{dc(1,2)}^- = R_{s(1)} \bar{I}_{b(1)} + R_{p(1)} \bar{I}_{b(1)} (1 - e^{-\frac{\Delta t}{\tau(1)}}) \quad (5.13)$$

where $\Delta v_{dc(1,2)}^-$ denotes the voltage variation caused by the negative step current at the end of second time interval $t_{(2)}$. In the last equation, it is assumed the negative step

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

current has the same BESS parametric values as that of positive step current of the same magnitude.

Fig. 5-7 Estimation of DC-link voltage at the end of 2nd time interval.

Hence, at the end of the 2nd time step, the BESS voltage variations caused by the positive step currents $\bar{I}_{b(1)}$ and $\bar{I}_{b(2)}$ are

$$\Delta v_{dc(1,2)}^+ = - \left(R_{s(1)} \bar{I}_{b(1)} + R_{p(1)} \bar{I}_{b(1)} (1 - e^{-\frac{2\Delta t}{\tau(w)}}) \right)$$

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

$$\Delta v_{dc(2,2)}^+ = - \left(R_{s(2)} \bar{I}_{b(2)} + R_{p(2)} \bar{I}_{b(2)} (1 - e^{-\frac{\Delta t}{\tau_{(2)}}}) \right)$$

where $R_{s(2)}$, $R_{p(2)}$ and $C_{p(2)}$ are the BESS parameters corresponding to the current step change of magnitude $\bar{I}_{b(2)}$ and $\tau_{(2)} = R_{p(2)} C_{p(2)}$. At the same time, the negative step current produces the voltage change $\Delta v_{dc(1,2)}^-$ as shown in (5.13). Hence, the battery terminal voltage variation at the end of the 2nd time step is

$$\Delta v_{dc(2)} = \Delta v_{dc(1,2)}^+ + \Delta v_{dc(2,2)}^+ + \Delta v_{dc(1,2)}^-$$

and v_{dc} at $t_{(2)}$ is

$$v_{dc(2)} = v_{dc(0)} + \Delta v_{dc(2)} \quad (5.14)$$

Having obtained $v_{dc(2)}$ from (5.14), the same inner-loop updating procedure described earlier for $\bar{I}_b$ to calculate Δv_{dc} over the first time interval can also be applied until $v_{dc(2)}$ converges.

The above v_{dc} calculation procedure is repeated over the interval T . In general, at the k^{th} interval, $v_{dc(k)}$ is determined by the following equations,

$$v_{dc(k)} = v_{dc(0)} + \sum_{M=1}^k \Delta v_{dc(M,k)}^+ + \sum_{M=1}^{k-1} \Delta v_{dc(M,k)}^- \quad (5.15)$$

where

$$\Delta v_{dc(M,k)}^+ = - \left(R_{s(M)} \bar{I}_{b(M)} + R_{p(M)} \bar{I}_{b(M)} (1 - e^{-\frac{(k-M+1)\Delta t}{\tau_{(M)}}}) \right) \quad (5.16)$$

$$\Delta v_{dc(M,k)}^- = R_{s(M)} \bar{I}_{b(M)} + R_{p(M)} \bar{I}_{b(M)} (1 - e^{-\frac{(k-M)\Delta t}{\tau_{(M)}}}) \quad (5.17)$$

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

$R_{s(M)}$, $R_{p(M)}$ and $C_{p(M)}$ are the BESS parameters corresponding to current step $\bar{I}_{b(M)}$ and $\tau_{(M)} = R_{p(M)}C_{p(M)}$, $k = 2, 3 \dots N$.

Combining (5.10) and (5.15) one can obtain the general expressions for determining v_{dc} at the end of k^{th} time step as

$$v_{dc(k)} = \begin{cases} v_{dc(0)} + \Delta v_{dc(1)} & k = 1 \\ v_{dc(0)} + \sum_{M=1}^k \Delta v_{dc(M,k)}^+ + \sum_{M=1}^{k-1} \Delta v_{dc(M,k)}^- & k = 2, 3 \dots N \end{cases} \quad (5.18)$$

where $\Delta v_{dc(1)}$, $\Delta v_{dc(M,k)}^+$ and $\Delta v_{dc(M,k)}^-$ are calculated using (5.11), (5.16) and (5.17) respectively.

5.5 BESS Capacity Determination

It is now clear the BESS not only compensates for the balance of the power between the constant power load demand and that supplied by the upstream utility system, but also ensures that supply quality to the load does not deteriorate.

Also as explained in sub-section 5.2.2, when a fault occurs and the buffer is switched to the constant impedance control mode, power has to be extracted from the buffer BESS to meet the balance of the power demanded by the downstream constant power load. Discharging power from the BESS will consequently depress the BESS terminal voltage v_{dc} . If the BESS capacity is insufficient, v_{dc} may be forced to drop below its set lower limit $v_{dc,lower}$. This is not acceptable because v_{dc} must not deviate to such an extent that the inverter to the downstream constant power load is unable to maintain its terminal voltage to desirable level. One could increase the BESS capacity to prevent v_{dc} from falling below $v_{dc,lower}$ by adding additional branches of the battery cells. From section 5.3, by increasing the number of branches n , the internal resistances R_s and R_p will be correspondingly reduced while the capacitance C_p will be increased. For a given P_b , the discharge current will be reduced and hence, the terminal voltage deviations will be less.

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

Over the transient interval when the power system re-adjusts its power flows and network voltages, it is also likely that the amount of power supplied by the upstream source can be greater than that demanded by the downstream constant power load. Under such a circumstance, the surplus power will be absorbed by the BESS and v_{dc} increases. Hence, the capacity of BESS should also be sufficiently large to guarantee v_{dc} does not exceed the pre-set upper limit $v_{dc,upper}$. Again this can be achieved by increasing the number of parallel branches of the cells. The capacity of the BESS may therefore be determined based on the worst fault disturbance condition the buffer scheme is designed to cater for.

5.6 Illustrative Examples

To illustrate the design procedure of the previous section, the simple power system depicted in Fig. 5-1 is simulated using the well-known package PSCAD. In this example, a single-circuit radial link between Buses 1 and 2 is assumed. The line and generator parameters used for the simulations are listed in Table 5-2 and Table 5-3 [84, 121]. The AC1A type excitation and mechanical-hydraulic controlled (MHC) governor systems [84] are also included in the generator systems and the parameters used in the simulations have also been listed. The power flow pattern at nominal condition is such that G_1 has a generation of 320 MW and G_2 is of 80 MW. The load levels at Buses 1 and 2 are 250 MW and 150 MW respectively. Hence 70 MW is imported from Bus 1 into Bus 2 through the transmission link.

Suppose all the loads at both ends are essential and are to be protected by the power buffers. By assuming different line fault conditions, the responses of the power system were studied. From the original power flow conditions and (5.6), P_b profile of the BESS can be obtained for both buffers. v_{dc} of the respective buffer is calculated using the computational method described in section 5.5. Note that the power flow quantities are obtained using the multi-meter blocks in PSCAD. The electromagnetic transient phenomenon associated with the fault event is essentially over and transient stability of the network is of concern.

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

Table 5-2 Transmission Line Parameters [121]

$V_{l,rms}$ (kV)	f (Hz)	L (km)	r (Ω /km)	x (Ω /km)	b (S/km)
132 kV	50	150	0.068	0.404	7.59E-6

Table 5-3 Machine, Exciter and Governor Parameters [84]

Equivalent Machine Parameters Used in the Simulations							
Items	S_N (MVA)	H (s)	X_d (p.u.)	X_d' (p.u.)	X_d'' (p.u.)	X_q (p.u.)	
G_1	360	4.0	1.00	0.30	0.20	0.60	
G_2	150	4.0	2.00	0.25	0.20	0.50	
Items	X_q'' (p.u.)	X_a (p.u.)	T_{d0}' (s)	T_{d0}'' (s)	T_{q0}' (s)	T_{q0}'' (s)	
G_1	0.20	0.12	5.00	0.08	-	0.12	
G_2	0.20	0.15	6.00	0.03	0.60	0.06	
AC1A Type Exciter and Regulator Parameters Used in the Simulations (p.u.)							
T_R	K_A	T_A	T_B	T_C	K_F	T_F	K_E
0.0	400.0	0.02	0.0	0.0	0.03	1.0	1.0
T_E	K_D	K_C	V_{RMAX}	V_{RMIN}	V_{AMAX}	V_{AMIN}	
0.8	0.38	0.2	6.03	-5.43	14.5	-14.5	
MHC Governor Parameters Used in the Simulations							
G_1	T_P (s)	K_S	T_G (s)	R_P		R_T	
	0.05	5.0	0.2	0.04		0.4	
	T_R (s)	G_{MAX} (p.u./s)	G_{MIN}	$R_{max\ open}$ (p.u./s)		$R_{max\ close}$ (p.u./s)	
	5.0	1.0	0.0	0.16		0.16	
G_2	K_G	T_{SR} (s)	T_{SM} (s)	T_{SI} (s)		L_{C1}	
	20	0.1	0.2	0.2		0.2	
	L_{C2}	L_{I1}	L_{I2}				
	-0.5	0.2	-0.5				

Note: G_1 : Hydro type and G_2 : Thermal type

5.6.1 A Temporary Mid-line Three-phase Fault

A temporary 10-cycle three-phase-to-ground fault event at the mid-point of the transmission line is examined first. By varying the buffer switching pattern to realize either constant impedance or constant power modes on the basis of the respective generator speed, it is intended that stability of the power system is improved. Consider Buffer 2 and as stated in Section 5.2, Power Buffer 2 is switched into constant impedance mode during the fault occurrence. BESS₂ discharges to compensate for the mismatched power between the constant power S_2 demanded and that supplied by the upstream sources. The power profile of BESS₂ is calculated using (5.6) and is given in Fig. 5-8 (a). Positive values in the figure denote power discharging from BESS₂ while negative ones indicate BESS₂ is being charged. At Buffer 1, there is negligible amount of power exchange between BESS₁ and the external system. This is because the constant mechanical power generated by G_1 is greater than that demanded by the load connected to Bus 1. Hence, Buffer 1 is operating under the constant power mode during the fault to reduce the acceleration of G_1 rotor. Therefore, only the performance and simulation results of Buffer 2 are addressed in the following.

Fig. 5-8 BESS₂ response following a temporary 10-cycle three-phase mid-line fault: (a) P_{b2} , and (b) v_{dc2} .

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

The BESS cells have the parametric values given in Table 5-1. Assume the modulation indices of the power buffers are at the typical value of 0.8, the initial DC-link voltage of Power Buffer 2 is 269.44 kV. Therefore, each BESS branch will compose of 40825 cells since each cell is rated 6.6 V. Using the computational procedure described in Section 5.4 and based on P_{b2} shown on Fig. 5-8 (a), v_{dc} is calculated. The time step used is half cycle of the power frequency. v_{dc} so obtained is shown in Fig. 5-8 (b). In these plots, the base power and dc-link voltage values used are 360 MW and 269.44 kV respectively.

For satisfactory operations of the downstream protected loads, assume the DC-link voltage is constrained to operate within the range [0.9, 1.05] p.u. This is a reasonable assumption: for example, adjustable speed drive systems would only operate satisfactorily within this range [72-74]. Suppose BESS₂ has only one branch of the cells. From Fig. 5-8 (b) one notices that in supporting the load demand S_2 , v_{dc2} is depressed below the set lower limit over the initial stage of the fault disturbance. Moreover, v_{dc2} subsequently rises momentarily beyond its upper limit during the system recovery period. In this case, S_2 will not be supplied at a voltage level acceptable for satisfactory continuous operation.

One can attempt to increase BESS₂ capacity by adding one more branch of the cells. The corresponding v_{dc2} profile for the 2-branch BESS₂ is also shown in Fig. 5-8 (b). The 2-branch BESS₂ is seen able to maintain v_{dc2} well within the limits. Therefore, the capacity of BESS₂ is determined to consist of 2 branches as only in this instance, the DC-link voltage is improved and the voltage quality of S_2 is of acceptable level. Although not shown here, the power system is observed to be transiently stable with such a load buffer scheme.

An interesting observation can be made from Fig. 5-8 (b). It is seen that v_{dc} post-fault steady-state level remains the same as that of the pre-fault level, although it is clear from Fig. 5-8 (a) that there is a net export of energy from BESS₂ to the load over the study period. With the net discharge of energy from the BESS, the battery terminal voltage is expected to decrease in the longer term because its internal EMF (E_b) decreases as the BESS state-of-discharge (SOD) increases [75]. In the present work, it has been assumed

that E_b remains constant over the fault incident. For longer term study of (say) several tens of seconds, it is necessary to include the SOD effect into the analysis.

5.6.2 A Temporary Three-phase Fault at 1/3 Line Length from Bus 2

The capacity of the BESS₂ determined for the mid-point fault condition is evaluated for its suitability for the same temporary three-phase 10-cycle fault event, but now located at a distance corresponding to 1/3 of the line length from Bus 2. P_{b2} for this case is given in Fig. 5-9 (a) while v_{dc} computed is shown in Fig. 5-9 (b).

Fig. 5-9 BESS₂ response following a temporary 10-cycle fault at 1/3 line length from Bus 2: (a) P_{b2} and (b) v_{dc2} .

Comparing P_{b2} shown in Fig. 5-9 (a) with that in Fig. 5-8 (a), one observes that with the fault occurring closer to Bus 2, BESS₂ has to increase its discharged power. Indeed, as shown in Fig. 5-9 (b) and under such a fault condition, BESS₂ with 2 cell branches would only result in v_{dc2} just marginally above the lower limit during this fault. The estimated v_{dc2} when BESS₂ consists of 3 cell branches is also given in Fig. 5-9 (b) and is seen to produce satisfactory performance. Again although not shown here, the power system is transiently stable with such a load buffer scheme.

5.6.3 Further Discussion of the Results

From the results of the numerical examples, it is not surprising to note that as the fault event is moved electrically closer to the load-buffer, it is necessary to increase the BESS capacity in order to cater for the constant power demand of the load. Hence, in the extreme case of the fault occurring at the load terminals, the BESS capacity would have to be equal to the load capacity, in order to maintain the supply to the load. However, stability of the power system is not necessarily guaranteed. This is because rotor-angle stability of the power system depends on, among many other factors, the generator inertia. The control action taken to adjust the load demand is just one way to alleviate the rotor angle difference between the generators. Hence, when a fault event is so severe that even with the BESS absorbing/injecting the maximum power, the buffers may still be unable to prevent the generators from losing synchronism.

Taking the above transmission system as an example, stability study for the same temporary three-phase 10-cycle fault introduced at a location 0.3 line length from G_2 has also been carried out. The results are given in Fig. 5-10. Even having the respective BESS capacity increased to meet the demands of S_1 and S_2 completely, instability cannot be avoided in this fault incident. This is because during this fault, voltage at Bus 2 is so low that P_{G2} and P_{12} are negligible. Hence, the mechanical input power to G_2 is used almost completely to accelerate its rotor. While G_1 would also accelerate at the same time, it is observed from the simulation results that it is at a lesser rate than that of G_2 . Eventually this leads to the loss of synchronism. The instability problem can only be solved using other measures. Coordination of the measures and the buffer actions can be a fruitful area for future work.

Chapter5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

Fig. 5-10 A solid 3-phase fault at 0.3 line length distance from Bus 2: (a) P_{b2} , (b) v_{dc2} and (c) rotor angle difference.

Another interesting issue concerns the proportion of the super premium loads. Instead of assuming all the loads are protected by the buffers, additional studies have been carried out when the load connected to each bus is assumed to consist of equal amount of constant power premium load protected by the power buffer systems, and constant impedance load. Hence, the pre-fault load capacities of S_1 and D_1 are both equal to 125 MW and that of S_2 and D_2 are 75 MW each. For space limit reason, the results are not given here but base on the simulation of the temporary 10-cycle three-phase fault

Chapter 5 Design of a Buffer Scheme to Enhance Network Transient Stability and Load Ride-through

considered earlier, one observes that the stability zone of such a load mix condition has resulted in a larger stability zone, compared to that when all the loads are of constant power type: the corresponding stability zone approaches to some 0.87 of the line length. The main reason for the increase is because during fault, the 50% Bus 2 constant impedance load has alleviated the power demand on G_2 . The deceleration of G_2 rotor is less compared to the previous cases with 100% constant power load. In this way, the rotor angle difference between the two generators is lessened. The implementation of the buffer scheme has obviously enhanced further the transient stability margin of the power system.

5.7 Conclusions

From the basic function of power buffers for voltage quality improvement for downstream protected constant power load, an extension of their application to include load damping to enhance power system stability has been explored. Specifically, the focus is on the battery energy storage system (BESS) of the buffers. An equivalent circuit BESS model is constructed based on the battery cell model given in [75]. When a buffer operates under constant impedance mode, the BESS discharges or absorbs power from the external system. This will cause its terminal voltage to deviate. A computational technique to determine the terminal voltage has been derived based on the battery power discharged or absorbed. As the BESS is connected across the buffer DC-link, the voltage deviations will impact on the voltage quality of the downstream protected load. Provided the DC-link voltage stays within set limits, supply quality to the protected load will be assured. When the DC voltage violates the limit, the capacity of the BESS has to be increased. The proposed method allows suitable capacity of the BESS to be determined. Through the implementation of proposed power buffer scheme, not only the stability of the network can be enhanced but also the supply quality of the protected loads can be assured under system disturbance conditions.

Chapter 6

Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm

6.1 Introduction

With the concern on energy supply security and the environment, the search for sustainable energy resources has become very important. Among renewable sources, wind energy has gained rapid development and has made significant in-road into present power systems. Its advantages are low operational cost, and its abundance in nature. Nowadays, the trend of wind energy has been directed from small area utilization to large wind farm which could generate and transmit significant amount of energy to loads [70, 81, 82].

Wind generation, much like renewable sources such as solar, is unsteady. Wind speed is influenced by the natural and meteorological conditions that depend on the location of the wind farm. This random feature of wind makes the output power of the wind farm to fluctuate continuously. This will result in network frequency deviation and voltage fluctuation. In [52] for example, the impact of wind on network frequency is examined and a method to mitigate the frequency excursion is proposed through the control actions of speed-governor of generators. Reference [53] proposes solving an observed instability problem in an isolated power system through the re-tuning of the wind energy converters.

Using the governor action as described in [52] would result in the wear and tear of the speed-control system. As alternative to the above techniques to attenuate the variability of wind power, the use of energy storage system (ESS) has been considered in e.g. [44, 46,

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm

49]. In [49], the use of superconducting magnetic coils incorporated into the DC link of the wind farm converter station is proposed. The authors provide a conceptual design but unfortunately, the paper does not include numerical results to validate the effectiveness of the proposed scheme. The superconducting coil could be replaced with a shunt capacitor which forms part of a filtering scheme, as proposed by Li et al in [44], such that short-term DC-bus voltage deviations due to the fluctuating wind power can be effectively controlled. If the ESS is intended for use in conjunction with the wind farm for tracking daily load cycle, or for peak load lopping purposes, then other means of energy storage such as that based on battery would be more suitable [46]. Indeed, the authors in [46] concluded that energy management incorporating battery energy storage over 24 hours could be attractive in allowing higher wind energy penetration level than what is currently seen in practice. What the authors in [46] have not addressed is the impact of the storage capacity on the performance of the renewable energy system.

The purpose of the investigation to be described in this Chapter is intended to fill in the gap by addressing the design of a battery energy storage system, incorporated into a power buffer for the wind farm. Battery energy storage system (BESS) not only possesses higher energy capacity and hence is suitable for the long term running [46], it is also shown to be cost-effective for use in power system [57-59]. For wind farm application for example, a flow battery system has been described in [45] although the authors have not provided any method by which the battery capacity can be determined. Specifically, in this Chapter, a methodology is proposed to determine the required BESS capacity. The method is based on given wind power profile and the optimization of an objective function through which the optimal dispatched power level from the wind farm will be obtained. The corresponding BESS power and energy capacity which allow such a dispatch will be determined while the accompanying DC voltage will be controlled to within specified limits through the application of a suitably designed capacitor. The design procedure allows the BESS capacity determination for the purpose of daily load tracking or load leveling.

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

This Chapter is organized as follows: the energy buffer-storage scheme is described in the next section. In Section 6.3, a method to determine the BESS capacity is presented. With the BESS in place and the power input from the wind farm, their impact on the converter DC-link voltage is examined in Section 6.4. Validity and illustration of the application of the methodology are illustrated in Section 6.5. Simulation results based on PSCAD/EMPDC and Matlab are given there.

6.2 System Configuration

Reference [82] describes various topologies of wind turbine-mains grid connection. With the decrease in cost of permanent magnet material and its lighter weight, permanent magnet synchronous generators (PMSG) are becoming more economical and attractive, especially with the increase of turbine ratings [82]. PMSG is integrated with the mains grid through a fully-rated power converter so as to decouple the frequency difference between the generator output and the grid. The power buffer scheme considered in this paper is based on such a PMSG-turbine connection, as depicted in Fig. 6-1.

Fig. 6-1 Variable speed wind turbine with inter-connection to the mains grid through power buffer system.

Fig. 6-1 shows that the wind energy captured by the turbine blades is converted through the PMSG into electrical power, denoted by P_w . From previous references, it is clear that P_w tends to be highly stochastic and an effective way to describe P_w is through statistical means. Alternatively, as part of wind farm planning, site selection and design process,

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

wind data is often collected at site if such data of (say) past few years is available. As the main focus of this work is on the design of the BESS, it is now assume that sufficient wind data is available and the profile of P_w is known over a period of T hours. Fig. 6-2 shows a typical profile of P_w , derived from the wind speed data taken from a site described in [122]. In the figure, P_w has been normalized and hence is within the range $[0, 1]$ p.u. The profile has been obtained by averaging the wind speed data over 10-minutes interval.

Fig. 6-2 A typical wind power profile based on data taken from [12]: constant P_d is shown.

To cater for grid integration, the back-to-back converters (CON1 and CON2 in Fig. 6-1) are utilized to inter-connect the generator and grid transformer through a DC-link. One can assume that the power loss in the two converters is negligible. The DC-link capacitor C functions as harmonics filter and in some designs, it can also take the role of the energy-storage system [44]. However, typical energy storage capacity of capacitor tends to be small compared to the BESS considered in the study. Hence, in terms of initial

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm

power flow analysis, the capacitor power may be neglected. It is further assumed that the dispatched power P_d from CON2 to the mains grid is to be kept constant over the interval T . Although this assumption tends to facilitate analysis, it also has a desirable effect from a practical viewpoint: it prevents the fluctuating P_w from impacting negatively on the grid, in terms of network voltage and frequency profiles. To realize the constant power feature, the mismatch power between P_w and P_d has to be compensated for by the BESS, which has the output $P_b(t)$ shown in Fig. 6-1.

The front-end boost converter (CON1) and the BESS constitute the power buffer system. The power buffer smoothes the fluctuations in P_w in the following way: to achieve a given P_d , CON1, is controlled to adjust the DC-link voltage v_{dc} through controlling its modulation index so that the nett power supplied from CON1 and BESS is exactly P_d . CON2 converts the DC power into ac form at grid frequency and also controls the reactive power flow. Details of such converter control for wind turbines are not described here but interested readers may refer to [70].

To ensure the success of the above scheme, the determination of the P_d level and BESS capacity specification have to be addressed. This is elaborated in the next Section.

6.3 Analysis of the BESS Sizing Scheme

6.3.1 BESS Power and Energy Specifications

Battery capacity is normally specified in terms of power- and energy-capacity [64]. The energy capacity describes the energy that can be drawn from or stored into the battery. The power rating determines the power that can be supplied or stored by the battery under rated discharge/charge time interval. The capital cost of the battery could also be determined, based on the power and energy capacities [91]. Consequently, the design problem in hand is to determine the BESS capacity based on a cost-benefit consideration, as shown below.

6.3.2 Determination of BESS Power and Energy Capacities

In the buffer system, the BESS power, $P_b(t)$, can be written in terms of P_w and P_d as,

$$P_b(t) = P_w - P_d \quad (6.1)$$

From (6.1), for a given constant dispatched level P_d , the battery power $P_b(t)$ will vary in the same manner as P_w . By setting P_d to another constant value will only result in $P_b(t)$ curve being shifted up or down, but $P_b(t)$ will remain of the same shape as P_w . For example, for the P_w profile given in Fig. 6-2, the $P_b(t)$ profile given in Fig. 6-3 (a) corresponding to a constant $P_d = 0.6$ p.u. From Fig. 6-3(a) one finds that the maximum battery power, $P_{b,\max}$, occurs at T_1 when $P_{b,\max} = -0.5$ p.u. over the interval T . The negative sign indicates that at this precise moment, the BESS is discharging. It is quite conceivable for a different value of P_d , the corresponding $P_{b,\max}$ may be positive. It then indicates that the BESS is being charged at the maximum value at that instance.

Integration of $P_b(t)$ with respect to time yields the nett energy (E_b) injected into or discharged from the BESS, up to time t . Correspond to changes in $P_b(t)$, the $E_b(t)$ profile will also vary for different P_d . For instance, $E_b(t)$ profiles corresponding to $P_d = 0.55, 0.6$ and 0.65 p.u. respectively have been given in Fig. 6-3(b). Positive values in Fig. 6-3(b) show nett gain/loss in stored energy in the BESS, as compared to the battery initial stored energy level.

For specific value of P_d , the corresponding value of $P_{b,\max}$ determines the BESS power capacity. To achieve the goal of dispatching the constant P_d over the designed period T , the BESS capacity has to be specified to be at least as large as the corresponding $P_{b,\max}$. Take the profile shown in Fig. 6-3(a) for example, once the BESS capacity is designed to be at least as large as $P_{b,\max}$, the BESS could absorb/supply the surplus/shortfall in power for the corresponding constant dispatched level P_d .

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm

Fig. 6-3 Profiles of (a) battery power for $P_d = 0.6$ p.u., and (b) battery energy corresponding to $P_d = 0.55, 0.6$ and 0.65 p.u. for the typical wind profile given in Fig. 6-2.

As described earlier, besides power capacity, battery energy capacity should also be considered. For the study undertaken in this paper, the BESS energy capacity is specified in similar manner as in the case of BESS power capacity: the energy capacity of the BESS has to be as large as that it could absorb/supply the maximum amount of the charged/discharged energy. Hence, the BESS energy capacity should be at least as large as $E_{b,max}$ for the corresponding P_d value.

6.3.3 Determination of P_d

From the last sub-section, it is noted that with different P_d , $P_{b,max}$ and $E_{b,max}$ will change accordingly. Since the focus of this work is on the design of the BESS, one can assume the capital cost of the wind turbine and power converters are constant. Therefore, the benefit (per hour) for dispatching P_d into the grid over period T could be calculated from

$$B = \alpha P_d - \beta P_{b,max} - \gamma E_{b,max} \quad (6.2)$$

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm

where α is the unit price of the wind energy (\$/kWh) sold to the grid. β (\$/kW) and γ (\$/kWh) are the amortized BESS capital costs per hour over T . The costs include the operating expenditure in its power- and energy-rates respectively and could be obtained from the battery manufacturers. Note that in the p.u. system, α , β and γ could also be considered as three coefficients or weights pertaining to P_d , $P_{b,\max}$ and $E_{b,\max}$ respectively. The physical meaning of (6.2) is evident: the first term denotes the obtainable benefit or income of the wind farm from selling P_d per hour at price of α . The second and third terms determine the amortized capital cost of the BESS sized by $P_{b,\max}$ and $E_{b,\max}$ over the designed period T . Therefore, the net benefit obtained by the wind farm, B , from incorporating such a BESS could be calculated.

With the design problem so formulated, the objective is therefore to design the BESS to maximize B . From the discussion in Sub-section 6.3.2, one notes that the BESS ratings are intrinsically determined by the dispatch-able level P_d . Therefore, with known α , β and γ , one can search for the optimal P_d to maximize B in an iterative manner by first setting $P_d = 0$ and increasing P_d progressively until the optimal P_d , denoted as P_d^* , which maximizes B is obtained. The optimal P_d^* therefore provides the power- and energy-capacities of the BESS, $P_{b,\max}$ and $E_{b,\max}$.

6.4 DC-link Voltage Constraints

Having the BESS capacity determined by following the procedure described in Sub-section 6.3.3, another design consideration is to ascertain whether the DC-link voltage v_{dc} is within pre-set limit $[v_{dc,\text{lower}}, v_{dc,\text{upper}}]$, i.e., one has to verify the BESS capacity is sufficiently large that v_{dc} will remain within the pre-set limit as P_w varies. In order to carry out the analysis, the battery model used will be introduced next. It is then followed by a method to calculate v_{dc} .

6.4.1 Battery Model

Several equivalent battery circuit models have been reported in the literature. The models are applicable to study the battery behavior over the short or long-term interval during its charge/discharge process [75-77]. For the present study, the consideration is for the charging/discharging processes of the battery for relatively long-term operations, e.g., over hours/days. The lead-acid battery model proposed by Ceraolo in [76] is suitable for such an application. The battery model has been reproduced in Fig. 6-4 (a), where E_m denotes the battery internal EMF, the linear internal resistances by R_0 , R_1 and R_2 respectively and C_1 the internal capacitance. The PN branch describes the parasitic effect of the battery and the effect of this branch is only noticeable at the end of the charging process. The battery terminal current, the charging/discharging current and the parasitic current are depicted by i_b , i_m and I_p respectively. Detailed description of the battery equivalent circuit and parametric determinations are given in Chapter 2. Definition and specification of the battery capacity, $C(I, \theta)$, the battery state of charge (SOC) and depth of charge (DOC), and the battery temperature, θ are given there.

Based on the BESS model given in [76] and taking into consideration the dc-link capacitor, one can obtain the equivalent circuit as shown in Fig. 6-4(a). Comparing the circuit given in Fig. 6-4(a) with that given in [76], it is observed that the differences between these two are: 1) the added capacitor branch consists of the capacitance, C , and the capacitor parasitic resistance, R_c . The current flowing into this branch is denoted with i_c , and 2) the input current, i , is the terminal current which includes the battery current, i_b . Another point which should be noted is the parasitic branch PN . Since in this study, the BESS is continuously operated in charging or discharging process, the parasitic current i_p is very small compared with that of the charging/discharging current and thus, i_p could be ignored [77]. The reduced equivalent circuit is given in Fig. 6-4(b), in which the current flowing into or out of the BESS is used entirely in the charging or discharging of the BESS, i.e., $i_b = i_m$,

Fig. 6-4 DC-link (a) equivalent circuit, (b) simplified equivalent circuit, with BESS parasitic branch neglected.

6.4.2 Determination of v_{dc}

In Fig. 6-4(b), one finds that the DC-link voltage, v_{dc} , is influenced not only by the battery EMF, E_m , but also by the terminal input current i . To account for the effects of these two sources on v_{dc} , the theory of superposition can apply, as follows. When the P_d level has

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

been determined following the procedure described in Sub-section 6.3.3, the corresponding battery power (P_b) profile can be readily obtained using (6.1) since P_w is assumed known. Next, over the interval T , $P_b(t)$ can be subdivided into N equal sections, with each section occupying a duration of T/N hours. Fig. 6-5 shows an example of such sub-division. As long as the time interval of each section is short enough, within such an interval, the amount of power and current injected into or flown out from the battery could be assumed constant and equal to the average values $\bar{P}_{b(k)}$ and $I_{(k)}$,

Fig. 6-5 Approximation of $P_b(t)$ by individual power pulse $\bar{P}_{b(k)}$.

$$\bar{P}_{b(k)} = \frac{P_{b(k-1)} + P_{b(k)}}{2} \tag{6.3}$$

$$I_{(k)} = \frac{\bar{P}_{b(k)}}{v_{dc(k-1)}} \tag{6.4}$$

*Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm*

where $k = 1, 2, \dots, N$. $v_{dc(k-1)}$ is the battery voltage at time $t_{(k-1)}$. The battery SOC, DOC and θ , and hence the parametric values accompanying the equivalent circuit would also be constant. This is because the battery model is applicable to long-term interval implementation and over such a short interval T/N hours, the parametric values would stay constant. Positive $\bar{P}_{b(k)}$ in Fig. 6-5 represents a charging event for the battery and conversely, negative values of $\bar{P}_{b(k)}$ will depict cases of battery discharging.

With P_b represented by the pulse train, the corresponding current pulse train is also given in (6.4). The current, of amplitude I , can therefore be modeled as one current source. Therefore from Fig. 6-4(b), v_{dc} can be calculated in the s -domain through the application of superposition principle, as follows,

$$v_{dc}(s) = \frac{(1 + sR_c C)(1 + sR_1 C_1)E_m + (1 + sR_c C)[R_0 + R_1 + R_2 + sR_1 C_1(R_0 + R_2)]I}{s \{ (1 + sR_1 C_1)[1 + sC(R_0 + R_2 + R_c)] + sR_1 C \}} \quad (6.5)$$

Battery time constant is normally of the order of few thousand of seconds while the parallel resistance is in milliohm range [76, 77]. Thus, the battery internal capacitance, C_1 , is much larger than the typical value of the DC-link capacitor, C . Therefore, in the denominator of (6.5), one notes that $R_1 C_1 \gg R_1 C$. Hence (6.5) could be reduced to

$$v_{dc}(s) = \frac{(1 + sR_c C)(1 + sR_1 C_1)E_m + (1 + sR_c C)[R_0 + R_1 + R_2 + sR_1 C_1(R_0 + R_2)]I}{s(1 + sR_1 C_1)[1 + sC(R_0 + R_2 + R_c)]} \quad (6.6)$$

With partial fraction expansion applied, (6.6) can be re-written in the form

$$v_{dc}(s) = \left(\frac{1}{s} - \frac{\lambda_1 \tau_2}{1 + s\tau_2} \right) E_m + \left(\frac{\lambda_2}{s} - \frac{\lambda_3 \tau_1}{1 + s\tau_1} + \frac{\lambda_4 \tau_2}{1 + s\tau_2} \right) I \quad (6.7)$$

From the inverse Laplace transformation of (6.7), one can obtain the time function of v_{dc} as,

$$v_{dc} = E_m - \lambda_1 E_m e^{-\frac{t}{\tau_2}} + \lambda_2 I - \lambda_3 I e^{-\frac{t}{\tau_1}} + \lambda_4 I e^{-\frac{t}{\tau_2}} \quad (6.8)$$

*Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm*

where $\lambda_1 - \lambda_4$, τ_1 and τ_2 in (6.7) and (6.8) are circuit dependent items. The exact expressions of these parameters are given as following,

$$\left. \begin{aligned} \lambda_1 &= \frac{R_0 + R_2}{R_0 + R_2 + R_c} \\ \lambda_2 &= R_0 + R_1 + R_2 \\ \lambda_3 &= \frac{R_1(R_1 C_1 - R_c C)}{R_1 C_1 - C(R_0 + R_2 + R_c)} \\ \lambda_4 &= \frac{R_0 C(R_0 + R_1 + R_2)}{R_1 C_1 - C(R_0 + R_2 + R_c)} \\ \tau_1 &= R_1 C_1 \\ \tau_2 &= C(R_0 + R_2 + R_c) \end{aligned} \right\} \quad (6.9)$$

v_{dc} will be further examined based on (6.8). Firstly, it is readily seen that the steady state value of the v_{dc} is,

$$V_{dc,ss} = E_m + \lambda_2 I = E_m + (R_0 + R_1 + R_2)I$$

Not surprisingly, $V_{dc,ss}$ is only governed by the battery and is unaffected by the selection of the DC-link capacitor C .

From (6.8) one also observes that the transient response of v_{dc} is governed by the two time constants, $\tau_1 = R_1 C_1$ and $\tau_2 = C(R_0 + R_2 + R_c)$. From the above discussion, one notes that typically C_1 is more than a few thousand times larger than C , and that $R_0 + R_2 \gg R_c$ while R_1 , R_0 and R_2 are comparable. Hence, $\tau_1 \gg \tau_2$, with τ_2 typically in the range of several seconds. Therefore, the dynamic exponential performance of v_{dc} at the initial period of every step input is primarily dominated by τ_2 which in turn is directly proportional to the capacitance C .

From further examination of the expressions relating to λ_1 , λ_3 , and λ_4 in (6.9), one also observes that: 1) λ_1 and λ_3 are relatively insensitive to C and R_c since $R_0 + R_2 \gg R_c$ and $R_1 C_1 \gg R_c C$, and 2) λ_4 increases with C . Whence, it again shows that C governs the transient behavior of v_{dc} .

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm

This above analysis provides some useful directions with regard to effect changes in the dynamic performance of v_{dc} through adjusting C . Indeed, it shows that the BESS can be designed based on the longer term performance of the power system, while C can be determined to meet transient or short-term v_{dc} performance requirement. This point will be elaborated further in the following sub-section and verified in the illustrative example.

6.4.3 Numerical Procedure to Determine v_{dc}

Based on the derivation shown in the previous sub-section, a numerical method will now be given to determine v_{dc} under fluctuating wind power condition.

The k^{th} power pulse $\bar{P}_{b(k)}$ taken from Fig. 6-5 is reproduced in Fig. 6-6(a). Its amplitude is determined from (6.3). To emulate the power pulse function, one could treat it as the superposition of a positive step power of amplitude $\bar{P}_{b(k)}$ starting from $t_{(k-1)}$, and another negative step power of the same magnitude but starting from $t_{(k)}$, as shown in Fig. 6-6(b) and (c) respectively. v_{dc} at $t_{(k-1)}$ is known. Hence from (6.4) one can readily obtain the corresponding battery current, $I_{(k)}$. Also, from Sub-section 6.4.2, the BESS parameters at $t_{(k-1)}$ are also known. Hence following (6.8), for the positive step, one can calculate v_{dc} for $t_{(k-1)} < t < t_{(k)}$ due to the contributions of the two inputs, $E_{m(k)}$ and $I_{(k)}$, as

$$v_{dc}(t) = E_{m(k)} - \lambda_{1(k)} E_{m(k)} e^{-\frac{t-t_{(k-1)}}{\tau_{2(k)}}} + \lambda_{2(k)} I_{(k)} - \lambda_{3(k)} I_{(k)} e^{-\frac{t-t_{(k-1)}}{\tau_{1(k)}}} + \lambda_{4(k)} I_{(k)} e^{-\frac{t-t_{(k-1)}}{\tau_{2(k)}}} \quad (6.10)$$

where the circuit parameters constants, $\lambda_{1(k)}$, $\lambda_{2(k)}$, $\lambda_{3(k)}$, $\lambda_{4(k)}$, $\tau_{1(k)}$ and $\tau_{2(k)}$ are given in the following equation (6.11). This is the time-response $v_{dc}(t)$ shown in the right-hand side trace of Fig. 6-6(b).

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

Fig. 6-6 (a) Generic power pulse $\bar{P}_{b(k)}$ and the overall time-response in dc-link voltage constituting of (b) positive $\bar{P}_{b(k)}$ step and the corresponding dc-link voltage deviation and (c) negative $\bar{P}_{b(k)}$ step and the corresponding dc-link voltage deviation.

*Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm*

$$\left. \begin{aligned} \lambda_{1(k)} &= \frac{R_{0(k)} + R_{2(k)}}{R_{0(k)} + R_{2(k)} + R_c} \\ \lambda_{2(k)} &= R_{0(k)} + R_{1(k)} + R_{2(k)} \\ \lambda_{3(k)} &= \frac{R_{1(k)}(R_{1(k)}C_{1(k)} - R_c C)}{R_{1(k)}C_{1(k)} - C(R_{0(k)} + R_{2(k)} + R_c)} \\ \lambda_{4(k)} &= \frac{R_{0(k)}C(R_{0(k)} + R_{1(k)} + R_{2(k)})}{R_{1(k)}C_{1(k)} - C(R_{0(k)} + R_{2(k)} + R_c)} \\ \tau_{1(k)} &= R_{1(k)}C_{1(k)} \\ \tau_{2(k)} &= C(R_{0(k)} + R_{2(k)} + R_c) \end{aligned} \right\} \quad (6.11)$$

From $t > t_{(k)}$, v_{dc} is determined not only by $E_{m(k)}$ and $I_{(k)}$ but also by the inputs $-E_{m(k)}$ and $-I_{(k)}$. These two inputs are introduced to nullify the positive step inputs $E_{m(k)}$ and $I_{(k)}$ introduced at $t_{(k-1)}$. The corresponding response due to the negative step is shown in the right-hand side trace of Fig. 6-6(c). By combining the responses to the positive and negative step inputs and again through application of (6.8), v_{dc} for $t > t_{(k)}$ can be calculated as

$$\begin{aligned} v_{dc}(t) = & E_{m(k)} - \lambda_{1(k)} E_{m(k)} e^{-\frac{t-t_{(k-1)}}{\tau_{2(k)}}} + \lambda_{2(k)} I_{(k)} - \lambda_{3(k)} I_{(k)} e^{-\frac{t-t_{(k-1)}}{\tau_{1(k)}}} + \lambda_{4(k)} I_{(k)} e^{-\frac{t-t_{(k-1)}}{\tau_{2(k)}}} \\ & - E_{m(k)} + \lambda_{1(k)} E_{m(k)} e^{-\frac{t-t_{(k)}}{\tau_{2(k)}}} - \lambda_{2(k)} I_{(k)} + \lambda_{3(k)} I_{(k)} e^{-\frac{t-t_{(k)}}{\tau_{1(k)}}} - \lambda_{4(k)} I_{(k)} e^{-\frac{t-t_{(k)}}{\tau_{2(k)}}} \end{aligned} \quad (6.12)$$

where the circuit parameters constants are the same as that in (6.10). The overall response in $v_{dc}(t)$ is shown in the bottom trace of Fig. 6-6(a).

Based on the same reasoning as above, a general numerical procedure to determine the dc-link voltage is through the following iterative approach:

$$v_{dc(n)} = \begin{cases} v_{dc(1,1)}^+ & n = 1 \\ \sum_{l=1}^n v_{dc(l,n)}^+ + \sum_{l=1}^{n-1} v_{dc(l,n)}^- & n = 2, 3 \dots N \end{cases} \quad (6.13)$$

*Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm*

where $v_{dc(l,n)}^+$, caused by the l^{th} positive inputs $E_{m(n)}$ and $I_{(n)}$, is that appeared at the end of the n^{th} time interval and $v_{dc(l,n)}^-$, is that due to the negative inputs $-E_{m(n)}$ and $-I_{(n)}$, appears at the end of $(n+1)^{\text{th}}$ time interval. $v_{dc(l,n)}^+$ and $v_{dc(l,n)}^-$ are given by the following equations

$$v_{dc(l,n)}^+ = E_{m(l)} - \lambda_{1(l)} E_{m(l)} e^{-\frac{(l-n+1)\Delta t}{\tau_{2(l)}}} + \lambda_{2(l)} I_{(l)} - \lambda_{3(l)} I_{(l)} e^{-\frac{(l-n+1)\Delta t}{\tau_{1(l)}}} + \lambda_{4(l)} I_{(l)} e^{-\frac{(l-n+1)\Delta t}{\tau_{2(l)}}}$$

$$v_{dc(l,n)}^- = -E_{m(l)} + \lambda_{1(l)} E_{m(l)} e^{-\frac{(l-n)\Delta t}{\tau_{2(l)}}} - \lambda_{2(l)} I_{(l)} + \lambda_{3(l)} I_{(l)} e^{-\frac{(l-n)\Delta t}{\tau_{1(l)}}} - \lambda_{4(l)} I_{(l)} e^{-\frac{(l-n)\Delta t}{\tau_{2(l)}}}$$

The circuit parameter dependent constants, $\lambda_{1(l)}$, $\lambda_{2(l)}$, $\lambda_{3(l)}$, $\lambda_{4(l)}$, $\tau_{1(l)}$ and $\tau_{2(l)}$, can be obtained by replacing k with l in (6.12).

The application of (6.13) can be described as follows. At the start time $t_{(0)}$, one can assume that v_{dc} is at its nominal level, i.e. $v_{dc(0)} = 1$ p.u. and the BESS status is at its fully charged condition. This means $\text{SOC}_{(0)} = 1$, $\text{DOC}_{(0)} = 1$, and $\theta_{(0)}$ is the ambient temperature. With known BESS status, the power circuit parameters of the BESS within the first time step, i.e. $E_{m(1)}$, $R_{0(1)}$, $R_{1(1)}$, $C_{1(1)}$ and $R_{2(1)}$, can be determined using (2.26) in Chapter 2. Also, since $v_{dc(0)}$ is known and the charging/discharging power during the first time interval, $\bar{P}_{b(1)}$ is given, one could readily obtain the corresponding battery current, $I_{(1)}$, using (6.4).

With the known $E_{m(1)}$ and $I_{(1)}$ and circuit parameters, v_{dc} at the end of the 1st time interval, $t_{(1)}$, can be calculated using (6.13). Meanwhile, the BESS status parameters, $\text{SOC}_{(1)}$, $\text{DOC}_{(1)}$ and $\theta_{(1)}$, can also be updated using (2.22), (2.23) and (2.28). Accordingly, the BESS parameters, $E_{m(2)}$, $R_{0(2)}$, $R_{1(2)}$, $C_{1(2)}$ and $R_{2(2)}$ can be calculated based on (2.26). Again from (6.3) and (6.4), the battery power and current during the second time interval, $P_{b(2)}$ and $I_{(2)}$, can be readily obtained. The above procedure can be repeated until $t = T$.

Once v_{dc} profile has been determined through the above proposed method, one can then examine whether the BESS can maintain v_{dc} to within its specified limits. If v_{dc} cannot be

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer Applicable for Wind Farm

kept within the limits, one solution is to increase the BESS capacity but this will increase the cost of the power buffer. Often v_{dc} violates the limits only over short time interval(s) and increasing the battery capacity may not be a cost-effective solution. Instead, from the analysis on the dynamic response of v_{dc} shown in Section 6.4.2, increasing the shunt capacitor C could be a better alternative. This is because capacitor possesses the characteristic of higher power density but lower energy density, as compared to BESS [93]. It is ideal for use to alleviate short duration v_{dc} voltage violations. This point will be demonstrated in the next Section.

6.5 Illustrative Example

The wind data obtained from an existing wind farm is used to illustrate the BESS design procedure proposed in Sections 6.3 and 6.4. In the study, wind speed profile of an autumn day (November 29, 2006) was obtained from the wind farm at Audubon, USA [122]. The wind speed was then averaged over 10-minute intervals, to form the input to the wind turbine and synchronous generator modeled in PSCAD/EMTDC software package to produce the wind power P_w shown in Fig. 6-7(a). The choice of the 10-minute interval is suitable as this time-scale is short compared to the time constant of the BESS selected for this example. In this instance, maximum P_w is 2.83 MW. Hence, 2.83 MW has been chosen to be the base power used in the study and one readily observes that P_w varies within the range 0.2 to 1 p.u.

In this study, the weight coefficients in (6.2) are selected in the following way. Suppose the electricity generated by the wind farm is sold to the grid at $\alpha = 0.065$ \$/kWh [92]. Also taken from [92], the battery cost is assumed to be \$116/kWh and its maintenance cost is \$29/kWh/year. Based on a conservative assumption that battery life is 2 years [90], one can calculate the amortized capital cost of the battery in terms of energy to yield $\gamma = (116/2+29)/8760 = 0.0099$ \$/kWh/h. From the battery kWh/kW cost ratio reported in [88], the power related battery cost is estimated to be $\beta = 0.0116$ \$/kW/h. Furthermore, the BESS model established in Sub-section 6.4.1 is utilized and the corresponding parameters are given in Table 6-1. The data is taken from [76].

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

In the initial stage of the study, the shunt capacitor C has been omitted. With the substitution of the above mentioned price coefficients into (6.2) and following the BESS capacity determination procedure described in Sub-section 6.3.3, the obtainable benefit B is as shown in Fig. 6-7(b) for various values of the dispatched wind power P_d . Fig. 6-7(b) shows that maximum B occurs when $P_d = 0.7$ p.u. Therefore, based on the design criterion described in Sub-section 6.3.3, one can conclude that the optimal economic dispatch level for the wind farm is when $P_d^* = 0.7$ p.u.

Table 6-1 Battery Parameters [76]

Parameters pertaining to battery capacity	$I^* = 49 \text{ A}$ $K_c = 1.18$ $\epsilon = 1.29$	$C_{0*} = 261.9 \text{ Ah}$ $\theta_f = -40 \text{ }^\circ\text{C}$, $\delta = 1.40$
Parameters pertaining to the main branch	$\tau_1 = 5000 \text{ s}$ $K_E = 0.58\text{e-}3 \text{ V/}^\circ\text{C}$, $R_{00} = 2.0 \text{ m}\Omega$ $R_{20} = 15 \text{ m}\Omega$ $A_{21} = -8.0$	$E_{m0} = 2.135 \text{ V}$ $R_{10} = 0.7 \text{ m}\Omega$, $A_0 = -0.3$, $A_{22} = -8.45$
Parameters pertaining to the parasitic branch	$E_p = 1.95 \text{ V}$ $G_{p0} = 2 \text{ pS}$	$V_{p0} = 0.1 \text{ V}$, $A_p = 2.0$
Parameters pertaining to the thermal model	$C_\theta = 15 \text{ Wh/}^\circ\text{C}$	$R_\theta = 0.2 \text{ }^\circ\text{C/W}$

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

(a)

(b)

(c)

(d)

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

Fig. 6-7 (a) Wind power output, (b) benefit B vs dispatched level, (c) battery power profile at the selected dispatch level, (d) battery energy profile at the selected dispatch level, (e) dc-link voltage with a 19-branches BESS, (f) dc-link voltage with the 19-branch BESS paralleled with a 220F capacitor, (g) power stored/supplied by the capacitor, and (h) the re-calculated battery power with the capacitor implemented.

With the P_d level so determined, the BESS power- and energy-capacities can be readily calculated based on the battery power (P_b) and battery energy (E_b) profiles given in Figs. 6-7 (c) and (d) respectively. Note that the battery power profile is obtained by deducting

*Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm*

P_d from the wind power output given in Fig. 6-7(a) and the battery energy profile is obtained by integrating P_b with respect to time. In this example, the BESS is designed to have the power capacity $P_{b,max} = 0.47$ p.u. or 1.33 MW and energy capacity $E_{b,max} = 0.24$ p.u. or 0.68 MWh, as can be seen from Figs. 6-7 (c) and (d) respectively.

One should then also verify whether the above determined BESS is sufficiently large to meet the power quality requirement, i.e., whether v_{dc} is within the pre-set limit of (say) $[0.9, 1.1]$ p.u., to ensure proper operation of CON2.

Under normal condition and in this example, the PMSG terminal voltage, $V_{l-l,rms}$, is assumed to be 690 V. Under the assumption that the modulation index of CON1 is at the typical value of 0.8, nominal v_{dc} is kept at 1408 V. As the battery cell rated voltage is 2.135 V and capacity $C_{10} = 500$ Ah, one BESS branch is to consist of $1408/2.135 \approx 660$ cells, connected in series. Each branch will then have the energy capacity of $660 \times 500 \times 2.135 \approx 704$ kWh. Since the battery has the rated capacity of 500Ah for 10 hours, hence each branch will then have the power capacity of $704/10$ kW or 70.4 kW. Therefore, to meet the specified power requirement, the BESS has to be designed to have at least $1.33 \text{ MW}/70.4 \text{ kW}$ or 19 parallel branches of cells. It can be readily verified that the specified energy requirement is also met with this design. With such a battery bank installed, Fig. 6-7(e) shows the calculated v_{dc} based on the computational procedure of Section 6.4. From Fig. 6-7(e), one notes that v_{dc} violates the pre-set limit at a few instances of the day: the designed BESS cannot ensure v_{dc} stays within its stipulated range. However, upon closer examination of Fig. 6-7(e), one finds that v_{dc} violates the pre-set limit only over short time intervals. Therefore, a capacitor bank C is utilized here to alleviate those violations in the following way.

Fig. 6-7(e) shows that the peak value of v_{dc} is almost 1.14 p.u. or 1607.9 V at around 0410 hours. To attenuate v_{dc} to within the pre-set upper limit of 1.1 p.u. or 1550.67 V, the capacitor should absorb the extra energy when v_{dc} is above 1.1 p.u. From the same figure, one also observes that v_{dc} reaches the 1.1 p.u. level at around 0407 hours. Hence, one could readily estimate the energy that should be absorbed by the capacitor. In this

*Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm*

example, this energy is 15.456 MJ. Assume the capacitor is of C F, hence,

$$15.456 \text{ MJ} = \frac{1}{2} C (1607.9^2 - 1550.67^2) \text{ or } C = 171 \text{ F.}$$

One then repeats the above computational procedure to re-evaluate v_{dc} with C sets to this value. In this case C was eventually found to be slightly higher at 220 F in order to maintain v_{dc} to the pre-set limit. The result with the 220 F capacitor implemented has been given in Fig. 6-7(f), from which one observes that v_{dc} is then well within the pre-set limit.

Indeed, one should examine whether the added capacitor would affect the capacity of the BESS determined earlier. As the capacitor energy capacity is much smaller than that of the battery, it is reasonable to expect the BESS energy capacity will not be much impacted by the addition of the capacitor. This aspect of the design has been checked as follows.

From the estimated v_{dc} shown in Fig. 6-7(f) and based on the equivalent circuit in Fig. 6-4(b), one can readily obtain the capacitor current i_c and the power flow through the capacitor can be calculated. This calculation has been carried out and the capacitor power over the day has been given in Fig. 6-7(g). One can conclude that the scales of the capacitor power variations are small compared with that of the battery power shown in Fig. 6-7(c) where C has not been incorporated. In other word, the previously determined BESS power capacity will not be significantly influenced by the utilization of the capacitor. This is confirmed by the net BESS power profile shown in Fig. 6-7(h) in this battery-capacitor combination.

In the event the capacitor changes the BESS capacity during the above checking procedure, one has to repeat the BESS sizing procedure described in Sub-sections 6.4.2 and 6.4.3. This iterative method should be undertaken until the result of the BESS capacity with the capacitor converges.

Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm

To further verify the effectiveness of the specified BESS in attenuating P_w fluctuations, the wind speed profile for a summer day (Aug 29, 2006) was also downloaded from [122]. The same BESS and 220 F capacitor used earlier were then applied. For such a different wind power profile, as given in Fig. 6-8(a), the resulted dc-link voltage profile is shown in Fig. 6-8(b). It is observed that the dc-link voltage is well within the pre-set limits.

Fig. 6-8 (a) Wind power profile on Aug 29, 2006, and (b) corresponding dc-link voltage with the 19-branch BESS paralleled with the 220F capacitor.

In practice, the above design procedure has to be carried out over the entire interval T to ensure that v_{dc} is well within the pre-set limits.

6.6 Conclusions

With the rapid increase of wind generated power in power systems, the inherent intermittent feature of wind could impact utility operation negatively. One solution to tackle this problem is to utilize power buffer devices with BESS incorporated, as proposed in this Chapter. A BESS capacity determination scheme is proposed with the view of not only keeping the injected power from the wind generator constant, but also to

*Chapter 6 Determination of Battery Energy Storage Capacity Required in a Buffer
Applicable for Wind Farm*

achieve maximum economic operation in terms of the power abstracted from the renewable source as against the cost of the BESS installation. By the implementation of such a BESS design approach, the BESS power and energy capacity will be determined and the dispatch level from the wind farm could also be guaranteed to be constant. Additionally, the effectiveness of the BESS capacity should also be checked against the perspective of proper operation of the power electronics devices, i.e. the BESS capacity has to be sized to ensure that the dc-link voltage is maintained well within pre-set limit. The proposed BESS sizing scheme has been demonstrated using the wind data obtained from a practical wind farm and the simulation results have been presented in this Chapter.

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

The main theme of this research is to investigate the design of power buffer system for voltage stability enhancement, load ride-through and wind power fluctuation attenuation. By adjusting the PWM controlled power electronic devices, dynamic of constant power loads (CPL) can be decoupled from mains grid to mitigate the voltage instability. To guarantee the power quality of downstream sensitive loads, ESS needs to be incorporated into the buffer. The ride-through ability of power buffer is highly dependent on the capacity of ESS. Presently, battery energy storage systems (BESS) are commercially available due to their cost-effectiveness and technological maturity and are suitable for applications in high power systems. Therefore, BESS are adopted in this thesis and its capacity sizing schemes are determined based on the corresponding power buffer ride-through abilities and BESS electrical equivalent models.

Based on commonly used three-phase boost converter, the topology of power buffer consisting of front end converter and input R - L filter is built up. The mathematical model of the buffer system is derived based on the voltage drop on the filter and the load-supply power balance relationship. After a-b-c to d-q-0 transformation and small signal analysis applied, the second-order nonlinear system is simplified to a linear first-order system. From this system, the controller applied for the power buffer during normal condition is proposed. This so-called constant power control method consists of the inner current and outer voltage control loop. With PI constants appropriately selected, the power buffer is operated at unity power factor (UPF) condition and the dc-link voltage is maintained at its nominal level. During disturbances, the power buffer is switched into constant impedance

Chapter 7 Conclusions and Recommendations

operation mode, under which the buffer-load combination is controlled to be as a constant impedance so that the undesirable dynamic feature of the downstream CPLs is decoupled from the upstream utilities. The detailed impedance determination approach for constant impedance control method is also addressed in Chapter 3.

The overall BESS incorporated power buffer system is examined in Chapter 4, where the input impedance during the voltage sag is just kept at constant with pre-fault level over the fault interval. This reduces the amount of power flowing into the buffer-load combination from upstream systems and lessens the stress of CPLs on the utility. The load-supply power imbalance under such constant impedance control mode is compensated by the BESS connected to dc-link. The model of the power buffer with BESS is derived based on which the steady-state and dynamic-performances of the buffer system are analyzed. In the steady state study, universal BESS model is applied. The relationship between steady state dc-link voltage and voltage sag depth is derived. In the dynamic state study, however, it is found that the dc-link voltage profile is dependent on the BESS internal parameters, which are nonlinearly related with BESS discharge current. Therefore, the impact of discharge current on the dynamic performance of power buffer is examined. To guarantee the proper operation of the buffer system and downstream connected sensitive loads, the BESS has to be suitably designed based on the information from these steady state and dynamic state analysis.

Integration of power buffers into power system for purpose of transient stability enhancement and load ride-through is investigated in Chapter 5. Two power buffer systems are connected to the sending- and receiving-end respectively. When a fault occurs in the transmission link, the voltage is depressed in the network. From the instant of the fault inception and until the end of post-fault transient period, the CPLs connected to bus bars deteriorate the system transient stability. With the assumption that mechanical power fed to generators being constant at pre-fault value due to slow response of the governor systems, the surplus power at the sending end will accelerate the machine speed if no countermeasures are taken. Similarly, the generator at the receiving end would decelerate because of deficiency power imported from the sending end. This may lead to

Chapter 7 Conclusions and Recommendations

instability in the overall system. With power buffer incorporated, depending on whether the generator speed accelerates or decelerates, the buffer system is switched into constant power mode or constant impedance mode respectively, thus improving the transient stability of the system. The BESS capacities within the buffer systems are sized sufficiently enough to guarantee the supply quality of downstream sensitive loads not disturbed.

As an extension of its application in power system, power buffer is utilized in wind farms to attenuate the generated power fluctuation. In Chapter 6, from the planning point of view, the output power from the wind farm is assumed to be kept constant. An objective function is formulated in terms of the dispatch level and amortized BESS capital cost. By optimizing this function, a dispatch level is found and the BESS capacity in power- and energy-specifications is sized as well. Such a BESS can accommodate the power fluctuations while keeping the output of the wind farm stable. Subsequently, based on the long term battery model, an iterative approach is proposed to calculate the dc-link voltage from the BESS power profile over the designed time interval. To guarantee the proper operation of power electronic devices, the dc-link voltage has to be kept within specific limits. Short-time violations of the dc-link voltage can be prevented by connecting a suitably designed super-capacitor.

7.2 Recommendations

In view of the progress described in the previous chapters, the following directions are suggested as possible areas for further investigation.

In Chapters 3 - 4, the constant impedance control method is proposed to mitigate the negative influence of CPL on voltage stability by decoupling the load dynamic from the source side. It is very critical to detect the inception of fault and confirm the sag, only then the power buffer control mode can be switched from constant power mode to the constant impedance to limit the input current. For simplification reason, the sag detection duration is assumed to be 1 electrical cycle and the operation mode switching would be

Chapter 7 Conclusions and Recommendations

finished over this time interval, as shown in Fig. 3-10 (e) and Fig. 3-11 (e). This assumption in practical may not be valid. If the performance of sag detection method is poor and the confirmation interval is longer, the downstream CPL will raise the input current level during this short time. In the worst case, especially under heavily loaded conditions, this increased current may violate the current limit, which may not be acceptable from the operation point of view. Therefore, fast and accurate sag detection method has to be investigated. Otherwise, current limit techniques have to be taken into consideration and integrated into the power buffer controller design.

In Chapter 5, the examination of the power buffer in enhancement of transient stability and ride-through is based on the assumption that CPLs would occupy 100% of the downstream load capacity for purpose of simplification. In practice, the downstream loads consist not only of such constant power type, but also of other types, such as voltage dependent loads, which are not detrimental from transient stability point of view. Though in the last part of Chapter 5, a situation of 1:1 ratio in CPL and voltage dependent loads has been examined, it indicates that ratio of CPL in the downstream would have a direct influence on the BESS capacity within the power buffers. It is interesting to determine the relationship between BESS size and the percentage of CPL for different fault conditions, such as fault locations. Thus a new BESS sizing scheme can be formulated based on the ‘protection boundary’ of the power buffer. For any fault occurs along transmission link within the above boundary, the buffer can guarantee the transient stability of the system in fault and post-fault conditions. Furthermore, one can take into account different load characteristics to investigate the power buffer performance. However, in such a hybrid system, the situation would become complex.

In Chapter 6, though the stochastic characteristic of wind speed which makes the generated wind power fluctuate has been examined, the influence of this factor on the BESS design has not been taken into consideration in this thesis. From meteorology point of view, wind speed is dependent on the natural and meteorological situation where the wind farm is located. With the assistance of highly developed computer technologies, however, the wind speed profile can be forecasted based on the historic data. Researchers

Chapter 7 Conclusions and Recommendations

in meteorology and wind energy studies have developed several methods to predict the wind speed in short and long time periods. Among them statistical methods are very promising, since it has been found that the wind speed in general follows Weibull or simplified Rayleigh distribution. This information is useful that BESS can be designed with some reliability margin, within which the BESS can help mitigating the fluctuation and can help wind farm to supply stable power. Beyond this margin, however, the statistical probability of wind power occurrence is low and to design BESS for such condition is not cost-effective. From economic considerations, this is a fruitful task worthwhile investigating.

References

- [1]
- [1] Thierry Van Cutsem, "Voltage instability: Phenomena, countermeasures, and analysis methods," *Proceedings of the IEEE*, vol. 88, pp. 208-227, 2000.
- [2] S. Z. Zhu, *et al.*, "Effect of load modeling on voltage stability," in *Proceedings of 2000 Power Engineering Society Summer Meeting*, pp. 395-400, 2000.
- [3] C. D. Vournas and N. D. Krassas, "Voltage stability as affected by static load characteristics," *IEE Proceedings C (Generation, Transmission and Distribution)*, vol. 140, pp. 221-8, 1993.
- [4] Pouyan Pourbeik, David Wang, and Khoi Hoang, "Load modeling in voltage stability studies," in *Proceedings of 2005 IEEE Power Engineering Society General Meeting*, pp. 1893-1900, 2005.
- [5] M. K. Pal, "Voltage stability conditions considering load characteristics," *IEEE Transactions on Power Systems*, vol. 7, pp. 243-9, 1992.
- [6] Kip Morison, Hamid Hamadani, and Lei Wang, "Practical Issues in Load Modeling for Voltage Stability Studies," in *Proceedings of 2003 IEEE Power Engineering Society General Meeting*, pp. 1392-1397, 2003.
- [7] Valery Knyazkin, Claudio A. Canizares, and Lennart H. Soder, "On the parameter estimation and modeling of aggregate power system loads," *IEEE Transactions on Power Systems*, vol. 19, pp. 1023-1031, 2004.
- [8] Les M. Hajagos and Behnam Danai, "Laboratory measurements and models of modern loads and their effect on voltage stability studies," *IEEE Transactions on*

Power Systems, vol. 13, pp. 584-590, 1998.

- [9] "Load representation for dynamic performance analysis [of power systems]," in *IEEE Transactions on Power Systems*, vol. 8, *IEEE Trans. Power Syst. (USA)*. IEEE Task Force on Load Representation for Dynamic Performance: IEEE Task Force on Load Representation for Dyanmic Performance, 1993, pp. 472-82.
- [10] Ali Emadi and Mehrdad Ehsani, "Negative impedance stabilizing controls for PWM DC/DC converters using feedback linearization techniques," in *Proceedings of the Intersociety Energy Conversion Engineering Conference*, pp. 613-620, 2000.
- [11] Xiaogang Feng, *et al.*, "Individual load impedance specification for a stable DC distributed power system," in *Proceedings of the IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 923-929, 1999.
- [12] V. Grigore, *et al.*, "Dynamics of a buck converter with a constant power load," in *Proceedings of 29th Annual IEEE Power Electronics Specialists Conference*, pp. 72-8, 1998.
- [13] Choi Byungcho, B. H. Cho, and Hong Sung-Soo, "Dynamics and control of DC-to-DC converters driving other converters downstream," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, pp. 1240-8, 1999.
- [14] Carl M. Wildrick, *et al.*, "A Method of defining the load impedance specification for a stable distributed power system," *IEEE Transactions on Power Electronics*, vol. 10, pp. 280-285, 1995.
- [15] M. F. Schlecht, "Distributed power architecture system stability requires compensation of DC-DC converter inputs," *PCIM Magazine*, vol. 26, pp. 52-56, Feb. 2000.
- [16] C. Rivetta, G. A. Williamson, and A. Emadi, "Constant power loads and negative

- impedance instability in sea and undersea vehicles: statement of the problem and comprehensive large-signal solution," in *Proceedings of 2005 IEEE Electric Ship Technologies Symposium*, pp. 313-20, 2005.
- [17] A. Emadi, *et al.*, "Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives," *IEEE Transactions on Vehicular Technology*, vol. 55, pp. 1112-25, 2006.
- [18] Ali Emadi, "Modeling of power electronic loads in AC distribution systems using the generalized state-space averaging method," *IEEE Transactions on Industrial Electronics*, vol. 51, pp. 992-1000, 2004.
- [19] M. Belkhat, R. Cooley, and A. Witulski, "Large signal stability criteria for distributed systems with constant power loads," in *Proceedings of 26th Annual IEEE Power Electronics Specialists Conference*, pp. 1333-8, 1995.
- [20] Xiaogang Feng and Fred C. Lee, "On-line measurement on stability margin of DC distributed power system," in *Proceedings of the IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 1190-1196, 2000.
- [21] A. Emadi, M. Ehsani, and J. M. Miller, "Advanced silicon rich automotive electrical power systems," in *Proceedings of Gateway to the New Millennium. 18th Digital Avionics Systems Conference*, pp. 1-8, 1999.
- [22] Wayne W. Weaver and Philip T. Krein, "Mitigation of voltage collapse through active dynamic buffers," *International Journal of Critical Infrastructures*, vol. 3, pp. 101-123, 2007.
- [23] J. Schlabbach, *Voltage quality in electrical power systems*. London: Institution of Electrical Engineers, 2001.
- [24] Barry W. Kennedy, *Power quality primer*. New York: McGraw Hill, 2000.
-

- [25] Arindam Ghosh and Ledwich Gerard, *Power quality enhancement using custom power devices*. Boston: Kluwer Academic Publishers, 2002.
- [26] Roger C. Dugan, *Electrical power systems quality*, 2nd ed. New York: McGraw-Hill, 2003.
- [27] Math H. J. Bollen, *Signal processing of power quality disturbances*. Piscataway, NJ: IEEE Press; Hoboken, NJ: Wiley, 2006.
- [28] Math H. J. Bollen, *Understanding power quality problems: voltage sags and interruptions*. New York: IEEE Press, 2000.
- [29] J. Arrillaga, N. R. Watson, and S. Chen, *Power system quality assessment*. New York: John Wiley & Sons, 2000.
- [30] Kusko Alexander, *Power quality in electrical systems*. New York, London: McGraw-Hill [distributor], 2007.
- [31] Lee Geun-Joon, M. M. Albu, and G. T. Heydt, "A power quality index based on equipment sensitivity, cost, and network vulnerability," *IEEE Transactions on Power Delivery*, vol. 19, pp. 1504-10, 2004.
- [32] Nicholas Jenkins, *et al.*, *Embedded generation*. London: Institution of Electrical Engineers, 2000.
- [33] Anne-Marie Borbely and Jan F. Kreider, *Distributed generation: the power paradigm for the new millennium*. Boca Raton, Fl.: CRC Press, 2001.
- [34] Hans B. Puttgen, Paul R. Macgregor, and Frank C. Lambert, "Distributed Generation: Semantic Hype or the Dawn of a New Era," *IEEE Power and Energy Magazine*, vol. 1, pp. 22-29, 2003.
- [35] G. Pepermans, *et al.*, "Distributed generation: definition, benefits and issues," *Energy Policy*, vol. 33, pp. 787-98, 2005.

- [36] Mohammad N. Marwali and Ali Keyhani, "Control of distributed generation systems - Part I: Voltages and currents control," *IEEE Transactions on Power Electronics*, vol. 19, pp. 1541-1550, 2004.
- [37] Mohammad N. Marwali, Jin-Woo Jung, and Ali Keyhani, "Control of distributed generation systems - Part II: Load sharing control," *IEEE Transactions on Power Electronics*, vol. 19, pp. 1551-1561, 2004.
- [38] M. I. Marei, E. F. El-Saadany, and M. M. A. Salama, "A novel control algorithm for the DG interface to mitigate power quality problems," *IEEE Transactions on Power Delivery*, vol. 19, pp. 1384-92, 2004.
- [39] Koen J. P. Macken, Math H. J. Bollen, and Ronnie J. M. Belmans, "Mitigation of voltage dips through distributed generation systems," *IEEE Transactions on Industry Applications*, vol. 40, pp. 1686-1693, 2004.
- [40] James P. Lyons and Vlatko Vlatkovic, "Power electronics and alternative energy generation," in *Proceedings of the IEEE Annual Power Electronics Specialists Conference*, pp. 16-21, 2004.
- [41] B. Kuri and F. Li, "Distributed generation planning in the deregulated electricity supply industry," in *Proceedings of 2004 IEEE Power Engineering Society General Meeting*, pp. 2085-9, 2004.
- [42] W. El-Khattam and M. M. A. Salama, "Distributed generation technologies, definitions and benefits," *Electric Power Systems Research*, vol. 71, pp. 119-128, 2004.
- [43] M. Begovic, *et al.*, "Impact of renewable distributed generation on power systems," in *Proceedings of the Hawaii International Conference on System Sciences*, pp. 47, 2001.
- [44] Li Wei, G. Joos, and C. Abbey, "Attenuation of wind power fluctuations in wind

- turbine generators using a DC bus capacitor based filtering control scheme," in *Proceedings of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, pp. 6, 2006.
- [45] T. Hennessy and M. Kuntz, "Flow battery storage application with wind power," in *Proceedings of the IEEE Power Engineering Society Transmission and Distribution Conference*, pp. 937-939, 2006.
- [46] John P. Barton and David G. Infield, "Energy storage and its use with intermittent renewable energy," *IEEE Transactions on Energy Conversion*, vol. 19, pp. 441-448, 2004.
- [47] Tomonobu Senjyu, *et al.*, "Output power leveling of wind turbine generator for all operating regions by pitch angle control," *IEEE Transactions on Energy Conversion*, vol. 21, pp. 467-475, 2006.
- [48] Jose Cidras Pidre, Camilo Jose Carillo, and Andres Elias Feijoo Lorenzo, "Probabilistic model for mechanical power fluctuations in asynchronous wind parks," *IEEE Transactions on Power Systems*, vol. 18, pp. 761-768, 2003.
- [49] Shinichi Nomura, *et al.*, "Wind farms linked by SMES systems," *IEEE Transactions on Applied Superconductivity*, vol. 15, pp. 1951-1954, 2005.
- [50] Changling Luo, *et al.*, "Strategies to smooth wind power fluctuations of wind turbine generator," *IEEE Transactions on Energy Conversion*, vol. 22, pp. 341-349, 2007.
- [51] Tatsuto Kinjo, *et al.*, "Output levelling of renewable energy by electric double-layer capacitor applied for energy storage system," *IEEE Transactions on Energy Conversion*, vol. 21, pp. 221-227, 2006.
- [52] Luo Changling and Ooi Boon-Teck, "Frequency deviation of thermal power plants due to wind farms," *IEEE Transactions on Energy Conversion*, vol. 21, pp. 708-16,
-

2006.

- [53] C. Carrillo, *et al.*, "Power fluctuations in an isolated wind plant," *IEEE Transactions on Energy Conversion*, vol. 19, pp. 217-21, 2004.
- [54] Mary Black and Goran Strbac, "Value of bulk energy storage for managing wind power fluctuations," *IEEE Transactions on Energy Conversion*, vol. 22, pp. 197-205, 2007.
- [55] J. G. Slootweg and W. L. Kling, "Impacts of distributed generation on power system transient stability," in *Proceedings of the IEEE Power Engineering Society Transmission and Distribution Conference*, pp. 862-867, 2002.
- [56] Ahmed M. Azmy and Istvan Erlich, "Impact of distributed generation on the stability of electrical power systems," in *Proceedings of 2005 IEEE Power Engineering Society General Meeting*, pp. 1056-1063, 2005.
- [57] P. F. Ribeiro, *et al.*, "Energy storage systems for advanced power applications," *Proceedings of the IEEE*, vol. 89, pp. 1744-56, 2001.
- [58] N. W. Miller, *et al.*, "Battery energy storage systems for electric utility, industrial and commercial applications," in *Proceedings of Eleventh Annual Battery Conference on Applications and Advances*, pp. 235-40, 1996.
- [59] Max D. Anderson and Dodd S. Carr, "Battery energy storage technologies," *Proceedings of the IEEE*, vol. 81, pp. 475-479, 1993.
- [60] A. Ter-Gazarian, *Energy storage for power systems*. Stevenage, Herts., U.K.: P. Peregrinus on behalf of the Institution of Electrical Engineers, 1994.
- [61] Birol Kikş and Sadk Kakaç, *Energy storage systems*. Dordrecht; Boston: Kluwer Academic Publishers, 1989.
- [62] W. C. Dobie, "Electrical energy storage," *Power Engineering Journal* [see also

- Power Engineer*], vol. 12, pp. 177-181, 1998.
- [63] R. M. Dell and D. A. J. Rand, "Energy storage - A key technology for global energy sustainability," *Journal of Power Sources*, vol. 100, pp. 2-17, 2001.
- [64] J. N. Baker and A. Collinson, "Electrical energy storage at the turn of the Millennium," *Power Engineering Journal*, vol. 13, pp. 107-12, 1999.
- [65] X. Y. Wang, D. M. Vilathgamuwa, and S. S. Choi, "Decoupling load dynamics to prevent power system collapse," in *Proceedings of IEEE Power Engineering Society General Meeting*, pp. 1-8 2006.
- [66] D. L. Logue and P. T. Krein, "Utility distributed reactive power control using correlation techniques," in *Proceedings of IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 1294-1300, 2001.
- [67] D. L. Logue and P. T. Krein, "Preventing instability in DC distribution systems by using power buffering," in *Proceedings of 2001 IEEE 32nd Annual Power Electronics Specialists Conference*, pp. 33-7, 2001.
- [68] Daniel Lee Logue, "*power electronic building block applications in optimization, control, and simulation*," PhD Thesis, UIUC, 2000.
- [69] Daniel Logue and Philip T. Krein, "Power buffer concept for utility load decoupling," in *Proceedings of the IEEE Annual Power Electronics Specialists Conference*, pp. 973-978, 2000.
- [70] Frede Blaabjerg and Zhe Chen, *Power electronics for modern wind turbines*. San Rafael, Calif.: Morgan & Claypool Publishers, 2006.
- [71] L. E. Unnewehr and S. A. Nasar, *Electric vehicle technology*. New York: Wiley, 1982.
- [72] A. Van Zyl, *et al.*, "Voltage sag ride-through for adjustable-speed drives with
-

- active rectifiers," *IEEE Transactions on Industry Applications*, vol. 34, pp. 1270-7, 1998.
- [73] Jose Luis Duran-Gomez, Prasad N. Enjeti, and Byeong Ok Woo, "Effect of voltage sags on adjustable-speed drives: A critical evaluation and an approach to improve performance," *IEEE Transactions on Industry Applications*, vol. 35, pp. 1440-1449, 1999.
- [74] Math H. J. Bollen, "Characterization of voltage sags experienced by three-phase adjustable speed drives," *IEEE Transactions on Power Delivery*, vol. 12, pp. 1666-1671, 1997.
- [75] C. J. Zhan, *et al.*, "Two electrical models of the lead-acid battery used in a dynamic voltage restorer," *IEE Proceedings: Generation, Transmission and Distribution*, vol. 150, pp. 175-182, 2003.
- [76] M. Ceraolo, "New dynamical models of lead-acid batteries," *IEEE Transactions on Power Systems*, vol. 15, pp. 1184-90, 2000.
- [77] Stefano Barsali and Massimo Ceraolo, "Dynamical models of lead-acid batteries: Implementation issues," *IEEE Transactions on Energy Conversion*, vol. 17, pp. 16-23, 2002.
- [78] Y. Q. Zhan, S. S. Choi, and D. M. Vilathgamuwa, "A voltage-sag compensation scheme based on the concept of power quality control center," *IEEE Transactions on Power Delivery*, vol. 21, pp. 296-304, 2006.
- [79] Narain G. Hingorani, "Introducing custom power," *IEEE Spectrum*, vol. 32, pp. 41-48, 1995.
- [80] A. Arulampalam, *et al.*, "Power quality and stability improvement of a wind farm using STATCOM supported with hybrid battery energy storage," *IEE Proceedings: Generation, Transmission and Distribution*, vol. 153, pp. 701-710, 2006.
-

- [81] Sathyajith Mathew, *Wind energy: fundamentals, resource analysis and economics*. Berlin: Springer, 2006.
 - [82] Siegfried Heier, *Grid integration of wind energy conversion systems*, 2nd ed. Chichester, England; Hoboken, NJ: Wiley, 2006.
 - [83] Carson W. Taylor, *Power system voltage stability*. New York: McGraw-Hill, 1994.
 - [84] P. Kundur, *Power system stability and control*. New York: McGraw-Hill, 1994.
 - [85] Prabha Kundur, *et al.*, "Definition and classification of power system stability," *IEEE Transactions on Power Systems*, vol. 19, pp. 1387-1401, 2004.
 - [86] in *Voltage stability of power systems: concepts, analytical tools, and industry experience*. IEEE Special Publication 90TH0358-2-PWR: IEEE Special Publication 90TH0358-2-PWR, 1990.
 - [87] P. Kundur, J. Paserba, and S. Vitet, "Overview on definition and classification of power system stability," in *Proceedings of CIGRE/IEEE PES International Symposium. Quality and Security of Electric Power Delivery Systems*, pp. 1-4, 2003.
 - [88] "Energy Storage Technologies - A Review Paper," Australian Greenhouse Office, 2005, Available at <http://www.greenhouse.gov.au/renewable/aest/>.
 - [89] D. A. J. Rand, *et al.*, *Valve-regulated lead-acid batteries*. Amsterdam; Boston: Elsevier, 2004.
 - [90] J. McDowall, "Conventional battery technologies-present and future," in *Proceedings of 2000 Power Engineering Society Summer Meeting*, pp. 1538-40, 2000.
 - [91] Tsung-Ying Lee and Nanming Chen, "Optimal capacity of the battery energy storage system in a power system," *IEEE Transactions on Energy Conversion*, vol.
-

8, pp. 667-673, 1993.

- [92] T. E. Lipman, R. Ramos, and D. M. Kammen, "*An Assessment of Battery and Hydrogen Energy Storage Systems Integrated with Wind Energy Resources in California*," California Energy Commission, PIER Energy-Related Environment Research, CEC-500-2005-136, 2005.
- [93] Rengui Lu, *et al.*, "Super-capacitor stacks management system with dynamic equalization techniques," *IEEE Transactions on Magnetics*, vol. 43, pp. 254-258, 2007.
- [94] H. A. Kiehne, *Battery technology handbook*, 2nd ed. New York: Marcel Dekker, 2003.
- [95] D. Berndt, *Maintenance-free batteries: lead-acid, nickel/cadmium, nickel/hydride: a handbook of battery technology*. New York: John Wiley, 1993.
- [96] H. A. Kiehne, *Batteries: fundamentals and theory, running techniques, outlook*. Ehningen Bei Boeblingen: expert verlag, 1989.
- [97] Magdalena Nuñez, *Electrochemical studies of batteries*. New York: Nova Science Publishers, 2005.
- [98] David Linden and Thomas B. Rdeey, *Handbook of batteries*, 3rd ed. New York: McGraw-Hill, 2002.
- [99] Alvin J. Salkind, *et al.*, "Impedance modeling of intermediate size lead-acid batteries," *Journal of Power Sources*, vol. 116, pp. 174-184, 2003.
- [100] Z. M. Salameh, M. A. Casacca, and W. A. Lynch, "A mathematical model for lead-acid batteries," *IEEE Transactions on Energy Conversion*, vol. 7, pp. 93-8, 1992.
- [101] Yoon-Ho Kim and Hoi-Doo Ha, "Design of interface circuits with electrical battery models," *IEEE Transactions on Industrial Electronics*, vol. 44, pp. 81-86,

1997.

- [102] R. Giglioli, *et al.*, "Charge and discharge fourth order dynamic model of the lead-acid battery," in *Proceedings of 10th International Electric Vehicle Symposium*, pp. 371-382, 1990.
- [103] D. Sutanto, H. L. Chan, and C. C. Fok, "Battery model for use in electric vehicles and battery energy storage systems," in *Proceedings of 8th European Conference on Power Electronics and Applications*, pp. 10, 1999.
- [104] Donald S. Zinger and Eduard Muljadi, "Annualized wind energy improvement using variable speeds," in *Proceedings of the Industrial and Commercial Power Systems Technical Conference*, pp. 80-83, 1997.
- [105] Nayeem Rahmat Ullah and Torbojorn Thiringer, "Variable speed wind turbines for power system stability enhancement," *IEEE Transactions on Energy Conversion*, vol. 22, pp. 52-60, 2007.
- [106] R. Wu, S. B. Dewan, and G. R. Slemon, "Analysis of an AC-to-DC voltage source converter using PWM with phase and amplitude control," *IEEE Transactions on Industry Applications*, vol. 27, pp. 355-64, 1991.
- [107] R. Wu, S. B. Dewan, and G. R. Slemon, "A PWM AC-to-DC converter with fixed switching frequency," *IEEE Transactions on Industry Applications*, vol. 26, pp. 880-5, 1990.
- [108] E. Wernekinck, A. Kawamura, and R. Hoft, "A high frequency AC/DC converter with unity power factor and minimum harmonic distortion," *IEEE Transactions on Power Electronics*, vol. 6, pp. 364-70, 1991.
- [109] D. R. Veas, J. W. Dixon, and Ooi Boon-Teck, "A novel load current control method for a leading power factor voltage source PWM rectifier," *IEEE Transactions on Power Electronics*, vol. 9, pp. 153-9, 1994.

-
- [110] A. V. Stankovic and T. A. Lipo, "A novel control method for input output harmonic elimination of the PWM boost type rectifier under unbalanced operating conditions," *IEEE Transactions on Power Electronics*, vol. 16, pp. 603-11, 2001.
- [111] Hur Namho, Jung Jinhwan, and Nam Kwanghee, "A fast dynamic DC-link power-balancing scheme for a PWM converter-inverter system," *IEEE Transactions on Industrial Electronics*, vol. 48, pp. 794-803, 2001.
- [112] Choi Jong-Woo and Sul Seung-Ki, "Fast current controller in three-phase AC/DC boost converter using d-q axis crosscoupling," *IEEE Transactions on Power Electronics*, vol. 13, pp. 179-85, 1998.
- [113] Simone Buso, *et al.*, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Transactions on Power Electronics*, vol. 13, pp. 814-823, 1998.
- [114] Sam Ben-Yaakov and Ilya Zeltser, "Dynamics of a PWM boost converter with resistive input," *IEEE Transactions on Industrial Electronics*, vol. 46, pp. 613-619, 1999.
- [115] Ned. Mohan, *Power electronics: converters, applications, and design*. Hoboken, NJ: John Wiley & Sons, 2003.
- [116] A. W. Green, J. T. Boys, and G. F. Gates, "3-phase voltage sourced reversible rectifier," *IEE Proceedings B Electric Power Applications [see also IEE Proceedings-Electric Power Applications]*, vol. 135, pp. 362-370, 1988.
- [117] J. W. Dixon and Boon-Teck Ooi, "Indirect current control of a unity power factor sinusoidal current boost type three-phase rectifier," *IEEE Transactions on Industrial Electronics* vol. 35, pp. 508-515, 1988.
- [118] Stanley M. Shinnars, *Modern control system theory and design*, 2nd ed. New York: J. Wiley, 1998.
-

- [119] A. W. Green, J. T. Boys, and G. F. Gates, "3-phase voltage sourced reversible rectifier," *IEE Proceedings C (Generation, Transmission and Distribution)*, vol. 135, pp. 362-370, 1988.

- [120] M. Gopal, *Modern control system theory*. New York: Wiley, 1993.

- [121] B. M. Weedy, *Electric power systems*, 4th ed. New York: Wiley, 1998.

- [122] Available at <http://mesonet.agron.iastate.edu/request/awos/1min.php>

Appendices

Appendix A

Derivation of (4.13)

From (4.12) the following state space equations can be reached,

$$\begin{pmatrix} \dot{\delta v}_{dc} \\ \dot{\delta v}_{cp} \end{pmatrix} = \begin{bmatrix} \frac{E - 2V_{dc,ss} - V_{cp,ss}}{R_s C V_{dc,ss}} & -\frac{1}{R_s C} \\ -\frac{1}{R_s C_p} & -\frac{1}{R_s C_p} - \frac{1}{R_p C_p} \end{bmatrix} \begin{pmatrix} \delta v_{dc} \\ \delta v_{cp} \end{pmatrix} + \begin{bmatrix} -\frac{1}{C V_{dc,ss}} \\ 0 \end{bmatrix} (\delta \Delta p)$$

and

$$\delta v_{dc} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{pmatrix} \delta v_{dc} \\ \delta v_{cp} \end{pmatrix}$$

Based on the state space theory, one can obtain the following transfer functions in s domain,

$$\begin{aligned} \frac{\delta v_{dc}}{\delta \Delta p} &= \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} s - \frac{E - 2V_{dc,ss} - V_{cp,ss}}{R_s C V_{dc,ss}} & \frac{1}{R_s C} \\ \frac{1}{R_s C_p} & s + \left(\frac{1}{R_s C_p} + \frac{1}{R_p C_p} \right) \end{bmatrix}^{-1} \begin{bmatrix} -\frac{1}{C V_{dc,ss}} \\ 0 \end{bmatrix} \\ &= \begin{bmatrix} 1 & 0 \end{bmatrix} \frac{1}{\left(s - \frac{E - 2V_{dc,ss} - V_{cp,ss}}{R_s C V_{dc,ss}} \right) \left[s + \left(\frac{1}{R_s C_p} + \frac{1}{R_p C_p} \right) \right] - \frac{1}{R_s^2 C C_p}} \\ &\quad \times \begin{bmatrix} s + \left(\frac{1}{R_s C_p} + \frac{1}{R_p C_p} \right) & -\frac{1}{R_s C} \\ -\frac{1}{R_s C_p} & s - \frac{E - 2V_{dc,ss} - V_{cp,ss}}{R_s C V_{dc,ss}} \end{bmatrix} \begin{bmatrix} -\frac{1}{C V_{dc,ss}} \\ 0 \end{bmatrix} \end{aligned}$$

$$= -\frac{1}{CV_{dc,ss}} \frac{\left[s + \left(\frac{1}{R_s C_p} + \frac{1}{R_p C_p} \right) \right]}{\left(s - \frac{E - 2V_{dc,ss} - V_{cp,ss}}{R_s CV_{dc,ss}} \right) \left[s + \left(\frac{1}{R_s C_p} + \frac{1}{R_p C_p} \right) \right] - \frac{1}{R_s^2 CC_p}} \quad (A.1)$$

For clarity, the constants α , β , γ are defined as follows,

$$\alpha = \frac{R_s + R_p}{R_s R_p C_p}, \quad \beta = \frac{E - 2V_{dc,ss} - V_{cp,ss}}{R_s CV_{dc,ss}}, \quad \gamma = \frac{1}{R_s^2 CC_p}$$

Substituting the above three constants into (A.1), (4.13) can be obtained readily.

Appendix B

Derivation of (6.8)

From (6.5) the following can be obtained,

$$v_{dc}(s) = \frac{(1 + sR_c C)(1 + sR_1 C_1)E_m + (1 + sR_c C)[R_0 + R_1 + R_2 + sR_1 C_1(R_0 + R_2)]I}{s[1 + sR_0 C + sR_c C + sR_1 C_1 + s^2 R_1 C_1 R_0 C + s^2 R_1 C_1 R_c C + sR_1 C]} \quad (A.2)$$

As addressed in Sub-section 6.4.2, the battery capacitance, C_1 is much larger than that of the dc-link capacitor, C . Therefore, $sR_1 C$ can be ignored in (A.2) and (6.5) is reduced to (6.6) as,

$$\begin{aligned} v_{dc}(s) &= \frac{(1 + sR_c C)(1 + sR_1 C_1)E_m + (1 + sR_c C)[R_0 + R_1 + R_2 + sR_1 C_1(R_0 + R_2)]I}{s(1 + sR_1 C_1)[1 + sC(R_0 + R_2 + R_c)]} \\ &= \frac{(1 + sR_c C)E_m}{s[1 + sC(R_0 + R_2 + R_c)]} + \frac{(1 + sR_c C)[R_0 + R_1 + R_2 + sR_1 C_1(R_0 + R_2)]I}{s(1 + sR_1 C_1)[1 + sC(R_0 + R_2 + R_c)]} \end{aligned} \quad (A.3)$$

From partial fraction expansion, the above equation could be written in the form of,

$$v_{dc}(s) = \left[\frac{x_1}{s} + \frac{x_2}{1 + sC(R_0 + R_2 + R_c)} \right] E_m + \left[\frac{x_3}{s} + \frac{x_4}{(1 + sR_1 C_1)} + \frac{x_5}{1 + sC(R_0 + R_2 + R_c)} \right] I \quad (A.4)$$

where x_1 , x_2 , x_3 , x_4 and x_5 are unknown quantities, solutions of which can be found by equating (A.3) and (A.4). They are,

$$\left. \begin{aligned} x_1 &= 1 \\ x_2 &= -(R_0 + R_2)C \\ x_3 &= R_0 + R_1 + R_2 \\ x_4 &= \frac{R_1^2 C_1 (R_1 C_1 - R_c C)}{(R_0 + R_2)C + R_c C - R_1 C_1} \\ x_5 &= \frac{(R_0 + R_2)C^2 (R_0 + R_2 + R_c)}{R_1 C_1 - (R_0 + R_2)C - R_c C} \end{aligned} \right\} \quad (A.5)$$

Substituting these known quantities into (A.4) and applying the inverse Laplace-transformation, (6.8) can be readily found.

VITA

Xiaoyu Wang was born in 1976 in P. R. China. He received B. Eng. Degree and M. Eng. Degree from North China Electric Power University, Beijing, P. R. China in 1999 and 2004 respectively, both in Electrical Engineering.

Since July 2004, he is pursuing for his Ph.D Degree in Power Engineering in Nanyang Technological University. His research interests are in Power System Analysis, Power Electronics, Distribution Generation and Energy Storage System.

Research related to this dissertation has resulted in the following publications:

- [2] X. Y. Wang, D. M. Vilathgamuwa and S. S. Choi, "Determination of battery storage capacity in energy buffer for wind farms," accepted to be published on *IEEE Trans. on Energy Conversion*, refer to TEC-00392-2007.
 - [3] X. Y. Wang, D. M. Vilathgamuwa and S. S. Choi, "A Buffer Scheme with Battery Energy Storage Capability for the Enhancement of Network Transient Stability and Load Ride-through," accepted to be published on *Journal of Power Sources*, refer to POWER_10337.
 - [4] X. Y. Wang, D. M. Vilathgamuwa and S. S. Choi, "Decoupling load and power system dynamics to improve system stability," in *Proc. of IEEE PEDS*, K.L., Malaysia, Nov. 2005
 - [5] X. Y. Wang, D. M. Vilathgamuwa and S. S. Choi, "Decoupling load dynamics to prevent power system collapse," in *Proc. IEEE PES General Meeting*, Montreal,
-

Canada, Jun. 2006.

- [6] X. Y. Wang, D. M. Vilathgamuwa and S. S. Choi, "On the Design of Power Buffer and its Applications," accepted by DRTP 08, Nanjing, China, Apr. 2008.
- [7] X. Y. Wang, D. M. Vilathgamuwa and S. S. Choi, "Design of a power buffer system to enhance voltage stability," submitted to ICHQP 08.