Development and characterization of deep reactive ion etching technology for through silicon interconnection

Nagarajan, Ranganathan

2010

Nagarajan, R. (2010). Development and characterization of deep reactive ion etching technology for through silicon interconnection. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/41775>

<https://doi.org/10.32657/10356/41775>

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**DEVELOPMENT AND CHARACTERIZATION OF DEEP
REACTIVE ION ETCHING TECHNOLOGY FOR THROUGH
SILICON INTERCONNECTION**

RANGANATHAN NAGARAJAN

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2010

DEVELOPMENT AND CHARACTERIZATION OF DEEP REACTIVE ION
ETCHING TECHNOLOGY FOR THROUGH SILICON INTERCONNECTION

RANGANATHAN NAGARAJAN

2010

DEVELOPMENT AND CHARACTERIZATION OF DEEP REACTIVE ION ETCHING TECHNOLOGY FOR THROUGH SILICON INTERCONNECTION

RANGANATHAN NAGARAJAN

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2010

STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the result of original research work and to the best of my knowledge has not been submitted for a higher degree to any other University or Institution.

A handwritten signature in blue ink, appearing to read 'Ranganathan', with a horizontal line drawn underneath it.

Ranganathan Nagarajan

06-August 2010

ACKNOWLEDGEMENT

I wish to express my deep and sincere gratitude to my supervisors Professor Pey Kin Leong, Head of Division of Microelectronics (Nanyang Technological University) and Professor Krishnamachar Prasad, Head of Department of Electrical and Electronic Engineering (Auckland University of Technology) for their timely guidance and constant encouragement despite their busy schedule. I have greatly benefited by their invaluable suggestions and attention to the minutest details. It has been my good fortune to have them as my guide and mentors through these years of my research.

I am very much grateful to Dr. Patrick Lo Guo-Qiang, Lab Director of Semiconductor Process Technology Lab for co-supervising and provide me valuable guidance, encouragement and support. I am also thankful to Dr. N. Balasubramanian (Ex-IME), Dr. Kripesh Vaidyanathan and Dr. Subhash Chander Rustagi of IME for providing technical guidance and support in course of my research work. I am also grateful to D.Y. Lee, Zhou Qiaoer and C.S. Soh for assisting me in my experimental and simulation studies. As all my experimental work and analytical characterization studies were done at IME, I am deeply thankful to the all the support staff in Semiconductor Process Technology Lab, Analytical Services Lab and Microsystems Modules and Components Lab who have extended their help and support in my research work.

I would specially like to than Janet Hopkins of Surface Technology Systems, UK for providing me with valuable information on STS DRIE system. I would also like to thank Soo Fat Chin from Silvaco and Sergey Babin from TRAVIT for providing me access to the Topography Simulation tools.

Development and characterization of deep reactive ion etching
technology for through silicon interconnection

Finally, I am very much thankful and grateful to Agency for Science Technology and Research (ASTAR) and Institute of Microelectronics (IME) for sponsoring my PhD program in Nanyang Technological University.

Abstract

Deep reactive ion etching (DRIE) is an enabling technology for three dimensional (3D) integration of planar integrated circuits. This work focuses on various challenges associated with deep reactive ion etching technology for realizing through silicon interconnection for 3D Microsystems application. In the first part of the thesis, stress simulation studies were done on TSV structures of various via geometries and shapes to determine the regions of high stress due to CTE mismatch. It was determined that the top and bottom of the vias and the surrounding materials experience maximum mechanical stress. It was also found that the stress is concentrated in the sharp peaks and valleys of the scallops formed by Bosch etch process. A test vehicle was designed and fabricated by copper damascene process with various geometries and barrier structures to experimentally study the effect of sidewall scallops on electrical leakage between adjacent TSV structures. It was shown that the leakage current can be reduced by about nearly 3 orders of magnitude when the sidewall roughness is reduced or replaced by a smoother sidewall for the initial few microns of the depth of the via by using a non-Bosch etch process. This study has shown that the Bosch etch process can still be used, with all its merits of high etch rate and high etch selectivity, for vertical TSV etch application by tailoring a short first etch step with smooth sidewall.

In the second part of the research, tapered TSV etching technology was developed and characterized for TSV with diameters of 20-100 μm and depth of 100-300 μm for advanced 3D-Packaging application. In this study, the evolution of tapered via etch topography was modeled for various via diameters and experimentally validated within 5-

10% deviation. It was also experimentally shown that by combining Bosch, RIE and Isotropic etch processes into a multi-step etch process it is possible to achieve acceptable tapered profile of 83-87° and depth from 200-300µm. It was finally demonstrated that a void-free TSV can be formed with good electrical isolation and electrical continuity.

In the third part of the work the influence of deep silicon via profile and sidewall roughness on the electrical conduction through the TSV dielectric was studied. Based on extensive experimental characterization it was shown that the sidewall scallops due to Bosch process and curvature defects due to RIE process strongly influences the dielectric conduction in TSV. It was also shown that the scallops and curvature defects causes defect-induced PF type of leakage mechanism between TSVs. It was further shown that smoothening the sidewall defects at top results in significant reduction in leakage current by 3-5 order of magnitude.

In conclusion, this research work addressed the critical TSV etch challenges and failure mechanisms and demonstrated suitable approaches to resolve them for implementation in 3D IC and 3D-Packaging application.

TABLE OF CONTENTS

STATEMENT OF ORIGINALITY	i
ACKNOWLEDGEMENT	ii
ABSTRACT	iv
TABLE OF CONTENT	vi
LIST OF FIGURES	xi
LIST OF TABLES	xx
CHAPTER 1 INTRODUCTION	1
1.1 Overview.	1
1.2 Motivation for three dimensional integration	2
1.3 Challenges confronting silicon via etch technology	4
1.4 Motivation and research objectives	7
1.4.1 Motivation	7
1.4.2 Research Objective	7
1.5 Major Contributions of the Thesis	9
1.6 Organization of the Thesis	11
CHAPTER 2 LITERATURE REVIEW	13
2.1 Overview of TSV etch technology	13
2.2 Silicon via etch technology options	14
2.2.1 Orientation Dependent Anisotropic Wet Etching	14
2.2.2. Plasma Etching	16
2.2.3 Bosch etch Process	17

2.2.4	Reactive Ion Etch (RIE) Process	19
2.2.5	Cryogenic RIE Process	21
2.2.6	Summary	23
2.3	TSV etch process characterization	24
2.3.1	TSV etch requirements	24
2.3.2	TSV etch process characterization studies	26
2.3.3	TSV electrical characterization	27
2.4	Summary	28
CHAPTER 3 TOPOGRAPHY MODELING AND THERMO-MECHANICAL SIMULATION FOR TSV CHARACTERIZATION		29
3.1	Introduction	29
3.2	Topological simulation with Athena Elite	31
3.2.1	Athena overview	31
3.2.2	Athena features and capabilities	32
3.2.3	String Algorithm	32
3.2.4	Grid definition	34
3.2.5	Etch models	35
3.2.5.1	Isotropic Etch Model	35
3.2.5.2	RIE Model	36
3.2.6	Etch Statements	37
3.2.7	Summary	39
3.3	Simulation of Thermo-Mechanical Stresses In TSV	40
3.3.1	Overview of ANSYS	40
3.3.2	Finite Element Analysis (FEA)	40
3.3.3	Thermo-mechanical stress analysis in TSV	42

3.3.4	Summary	46
3.4	Conclusion	46
CHAPTER 4 STUDY OF THERMO-MECHANICAL STRESS AND ITS IMPACT ON THROUGH SILICON VIAS		47
4.1	Introduction	47
4.2	Experimental study	49
4.2.1	Motivation for thermo-mechanical study of TSV	49
4.2.2	Thermo-mechanical simulation study using Finite element analysis	51
4.2.3	Test vehicle design	57
4.2.4	Development of Bosch etch process with minimum sidewall roughness	59
4.2.5	Test vehicle fabrication	64
4.2.6	Electrical test vehicle Characterization	66
4.3	Results and discussion	70
4.3.1	Effect of thermo-mechanical stress on TSV interconnect structures	70
4.3.2	Effect of Bosch process (A) with rough sidewalls	71
4.3.3	Effect of non-Bosch process (B) with smooth sidewalls	74
4.3.4	Effect of non-Bosch+Bosch etch process (Hybrid or combination etch process)	76
4.3.5	Effect of thermal stress on TSV interconnect structures	79
4.4	Conclusions	79
CHAPTER 5 DEVELOPMENT OF DUAL-ETCH VIA TAPERING PROCESS FOR THROUGH-SILICON INTERCONNECTION		81
5.1	Introduction	81
5.2	Motivation for tapering deep silicon via	83
5.3	Experimental work	84
5.3.1	Experiment Setup	84

Development and Characterization of deep reactive ion etching
technology for through silicon interconnection

5.3.2	Overview of dual-etch silicon via tapering process	86
5.3.3	Characterization of 1 st etching step	88
5.3.4	Characterization of 2 nd etching step by global isotropic etch process	95
5.4	Topography simulation via tapering process	97
5.5	Results and Discussion	101
5.5.1	RIE lag mechanism in Bosch etch process	101
5.5.2	RIE lag mechanism in non-Bosch etch process	102
5.5.3	Evolution of tapered etch profile by global isotropic etch process	105
5.5.4	Impact of dual-etch tapered via etch process on Cu-via-filling Process	107
5.6	Summary	108
CHAPTER 6 INTEGRATION OF TAPERED VIA ETCH TECHNOLOGY FOR SILICON CARRIER FABRICATION		109
6.1	Introduction	109
6.2	Significance of via profile in TSV application	111
6.3	Criteria for TSV interconnect material selection	112
6.4	Experimental plan	113
6.4.1	Silicon Carrier fabrication requirement	113
6.4.2	Silicon carrier design	114
6.4.3	Silicon carrier fabrication process	116
6.4.4	Development of multi-step tapered TSV etch process	117
6.4.4.1	Approach	117
6.4.4.2	Characterization of multi-step tapered etch process	119
6.4.4.3	Multi-step etch process results	124
6.4.5	Development of Low-temperature dielectric deposition	127

Development and Characterization of deep reactive ion etching
technology for through silicon interconnection

6.4.6	Copper via-filling process	130
6.4.7	Copper CMP and wafer back-grind	131
6.5	Results and discussion	133
6.6	Conclusions	136
CHAPTER 7	STUDY OF ELECTRICAL CONDUCTION IN DEEP SILICON VIA STRUCTURES FOR TSV APPLICATION	138
7.1	Introduction	138
7.2	Conduction mechanism in dielectric	139
7.2.1	Fowler-Nordheim tunneling	139
7.2.2	Schottky Emission	140
7.2.3	Frenkel-Poole emission	141
7.2.4	Ohmic conduction	142
7.2.5	Ionic conduction	143
7.2.6	Space charge limited conduction	143
7.3	Test vehicle design and fabrication	144
7.4	Electrical Characterization	148
7.5	Results and Discussion	149
7.6	Conclusions	160
CHAPTER 8	CONCLUSIONS AND FUTURE WORK	162
8.1	Conclusions	162
8.2	Recommendations for future work	164
APPENDIX A		167
PUBLICATIONS		177
BIBLIOGRAPHY		180

LIST OF FIGURES

Figure 1.1	Trends for the smallest transistor gate length and minimum interconnect width in an integrated electronic circuit [1].	1
Figure 1.2	SEM cross-sectional micrographs of six metal level interconnection in a 0.13 μm technology showing the decrease of interconnect dimensions for the layers that are closer to the silicon devices [1].	2
Figure 1.3	Multi chip sensor module is shown with lateral placement of components. A vision of 3D hyper integration of multiple functional modules is also shown by vertical placement. The stacked modules will be interconnected by through silicon vias (TSV) which is not shown in the figure [5, 6].	3
Figure 1.4	A typical vertically stacked 3D Microsystem architecture is illustrated with 2 silicon carriers with through silicon interconnections. Also shown in the figure are some of the major technology challenges encountered during the integration of a TSV technology.	6
Figure 1.5	3D stacked package using organic substrates with through vias. Courtesy: Amkor	7
Figure 1.6	3D stacked package using organic substrate with through vias. Courtesy: STATs Chip PAC	7
Figure 2.1	Orientation dependent wet etching of $\langle 100 \rangle$ silicon [38].	15
Figure 2.2	Hymite's patented tapered through silicon via technology with hermetic sealed cap wafer with plated through silicon interconnection for MEMS packaging [8]. (b) KOH + DRIE etched TSV structure by Ångström Aerospace Corporation (ÅAC) [41].	16
Figure 2.3	Etch/Passivation gases and Bias power switching is plotted as a function of process time in a typical Bosch etch process. The SF_6 and C_4F_8 is switched at intervals corresponding to etch and passivation cycle time. The Platen bias power is also switched along with the gases. SEM micrograph shows results achieved with a typical Bosch etch process with enlarged images of top and bottom portion of the trench.	19
Figure 2.4	(a) Optical cross section images of 20 μm wide trench etched by RIE process using SF_6 , O_2 , Ar chemistry. (b) Cross section image after partial isotropic silicon etch process and (c) Cross section images of same trench etched by more isotropic etch process.	20

Development and Characterization of deep reactive ion etching
technology for through silicon interconnection

Figure 2.5	Cryogenic etch process trend as a function of wafer temperature. It can also be seen that the etch profile of <100> silicon is highly pressure dependent. It can also be seen that the process is sensitive to orientation of the silicon under higher pressure and lower ion flux [67, 68].	21
Figure 2.6	3D IC technology and TSV Roadmap [79].	25
Figure 3.1	String Model approximation to model the Etch Front [101].	34
Figure 3.2	Material cross section defined by initial triangular grid pattern [101]	35
Figure 3.3	Tony plot of isotropic etch and RIE etch. Figure-3.3(a) shows pure isotropic chemical etch while 3.3(b) shows results due to RIE model which shows the effects of chemical, physical and beam divergence.	36
Figure 3.4	Simulation of tapered deep silicon etch process using the isotropic and RIE etch models. SEM micrograph shows the experimental result. It may be noted that the scale of x-axis is different from y-axis of the simulation result.	38
Figure 3.5	2D mesh showing higher density at the area of interest. Relaxing density in non-critical areas will reduce computation time in simulation [102].	41
Figure 3.6	Cross-section illustration of through silicon and blind via structure used for evaluating the thermo-mechanical stress pattern in the structure.	42
Figure 3.7	Thermo-mechanical stress distribution map in a TSV structure that was modeled under a thermal load.	45
Figure 4.1	Face to face bonded CMOS device wafer stack with TSV interconnection	47
Figure 4.2	Face to face bonded MEMS and CMOS device wafers bonded and interconnected with TSV connections	48
Figure 4.3	3D view and cross-sectional view of a through silicon interconnect structure used to study the stress distribution on the sidewalls in a Bosch and non-Bosch etched TSV structure.	50
Figure 4.4	(a) Simulated stress pattern on SiO ₂ isolation layer: (b) Stress on tantalum barrier layer due to thermal cycling on through-wafer copper interconnect structure.(c) Stress pattern on copper at both ends of the copper vias and (d) Stress on the tantalum barrier due to copper stress on both ends of the via.	53

Figure 4.5	Thermo-mechanical stresses in TSV and silicon interface due to rough sidewalls due to Bosch etch process. It can be seen that the stress concentration is high in the sharp peaks and valleys of the scallops and decreases from top and bottom towards the middle of the TSV.	54
Figure 4.6	Thermo-mechanical stresses in TSV and silicon interface is shown due to smooth sidewalls formed by a non-Bosch etch process. It can be seen that the stress is high in top and bottom which gradually decreases towards the middle of TSV.	55
Figure 4.7	Top view and cross-section view of test structure to evaluate the performance of through-wafer interconnection.	58
Figure 4.8	SEM image showing edge roughness due to Bosch process. Roughness gradually decreases 200-100nm.	62
Figure 4.9	FIB SEM images of 6µm deep silicon vias after Cu electroplating.	62
Figure 4.10	Process data log plot of process pressure and platen power in a standard Bosch etch process which uses a static pressure and platen power setting.	62
Figure 4.11	Plot showing the dynamic ramping of pressure and platen power in the optimized Bosch etch process. It typically takes few minutes for pressure and power to stabilize and follows the ramp rate as per recipe Table 4.9.	63
Figure 4.12	(a) Tilt SEM micrograph of trenches formed by the Bosch process (A) with a sidewall roughness of ~0.05 µm. (b) Smooth trench profile formed by a non-Bosch etch process (B) with a sidewall roughness of ~0.01µm. (c) Trenches formed by a hybrid etch process combination of a non-Bosch (B) and a Bosch etch process (A) .	66
Figure 4.13	Comparison of leakage current in wafers etched by the Bosch process (A) with different barrier schemes.	67
Figure 4.14	Comparison of leakage current in wafers etched by the Bosch process (A) with different depths.	67
Figure 4.15	Comparison of leakage current in wafer etched by the non-Bosch process (B) with different barrier schemes.	68
Figure 4.16	Comparison of leakage current in wafer etched by Bosch (A), non-Bosch (B) and hybrid etch processes (B + A).	68
Figure 4.17	Leakage current trend for 5µm comb test structures with 100µm depth (Run#1) etched by Bosch process (A) when subjected to different thermal loading conditions during leakage test.	69

Figure 4.18	Copper peeling observed during chemical mechanical polishing (CMP) process at comb structures for wafers with thicker barriers due to high film stress.	69
Figure 4.19	SEM micrograph of cross-sectioned test samples etched with the Bosch process (A). The scallops can be seen which causes thinning of barrier films due to rough sidewall and shadowing effect in a physical vapor deposition (PVD) process.	72
Figure 4.20	SEM micrograph of cross-sectioned test samples etched with the non-Bosch process (B). The uniform deposition of barrier films due to smooth sidewall is quite evident at top and bottom of the test structures.	74
Figure 4.21	SEM micrographs of 5 μ m wide rectangular and circular TSV structure etched by Bosch etch process with very similar profile angle and sidewall roughness. (a) Cross-section of rectangular TSV structure. (b) Cross section of circular TSV structure	78
Figure 4.22	SEM micrographs of 5 μ m wide rectangular and circular TSV structure etched by non-Bosch etch process with very similar profile angle and sidewall roughness. (a) Cross-section of rectangular TSV structure. (b) Cross section of circular TSV structure	78
Figure 5.1	Examples of 3D-MEMS wafer level packages with TSV through thick substrates [135, 136].	82
Figure 5.2	Four different shapes typically encountered in deep silicon via micromachining processes are shown. (a)-(c) show the non-uniform deposition of dielectric and barrier/seed metallization on via sidewall due to ion shadowing effect arising from high aspect ratio and sidewall defects. (d) Shows how a tapered profile can mitigate this problem.	83
Figure 5.3	Configuration of ICP DRIE system used for development of tapered via etch process.	85
Figure 5.4	Conceptual approach of silicon via tapering process after Bosch etch and non-Bosch etch process as first step and global isotropic etch process as second step.(a) Shows cross-section view of vertical via profile after Bosch etch process. (b) Partially tapered etch profile after RIE etch process. (c) Tapered etch profile after performing the global isotropic etch process. This process removes the sidewall scallops due to Bosch process and the sharp top curvature due to RIE process.	87

Figure 5.5	SEM cross sectional micrograph of trenches with depth varying from 260-350 μm for trenches of width varying from 10-100 μm after etching with Bosch process. The measured top/bottom CD and trench depth is summarized in Table 5.2..	90
Figure 5.6	Plots of etch rate, etch depth and RIE lag with variation of trench/via width from 10-100 μm using Bosch etch process. (a) It can be seen that the RIE lag increases while the etch rate decreases with increasing aspect ratio. (b) It can be seen that the trench depth/etch rate increases while the RIE lag decreases with increasing trench/via width.	91
Figure 5.7	SEM cross-sectional micrographs of trenches with depth varying from 190-240 μm for trenches of width varying from 10-100 μm after etching by the non-Bosch process.	94
Figure 5.8	Etch characterization plot of the non-Bosch etch process is shown for different trench widths and aspect ratios. (a) It can be seen that the etch depth increases and eventually slows down while the etch profile becomes straighter (see Fig. 5.8) with increasing trench width. It can also be seen that the RIE lag decreases with increasing trench width. (b) The RIE lag increases with increasing aspect ratio while the etch rate decreases with increasing aspect ratio.	94
Figure 5.9	(a-b) SEM micrographs of TSV sidewall after first etch by Bosch process followed by via tapering isotropic etch process. (c-d) SEM micrographs of sidewall after first etch by non-Bosch etch process followed by via tapering by isotropic etch process.	96
Figure 5.10	Experimental results of first etch done by the Bosch etch process and second etch done by the global isotropic etch process.	98
Figure 5.11	Comparison is made between simulated and experimental results of dual-etch tapered via etch process. It can be seen that there is a very close match between the two results within a 10% tolerance.	99
Figure 5.12	Simulation of via tapering effect as a function of global isotropic etch process time from 0-30 minutes.	100
Figure 5.13	Simulated results plotted as a function of isotropic etch time and aspect ratio. (a) It is seen that the etch depth decreases with increasing etch time while the taper depth increases with etch time. The top width of the trench increases linearly with etch time while the bottom of the trench is unaffected due to diffusion limited etching. (b) The isotropic etch rate increases with increasing etch time till it slows down after an aspect ratio of 8. It is also seen that the taper depth increases with increasing etch time.	100

- Figure 5.14 (a) shows trench depth variations versus trench width after first etch by the Bosch process and the second etch by global isotropic etch process. It can be seen that the second etch step reduces the silicon thickness globally according to size of the via opening. (b) shows the amount of depth reduction due to different global etch condition and with increasing trench width. 105
- Figure 5.15 (a) Plot shows the depth of the tapering as a function of trench width. (b) Shows the dependence of the taper angle on the second etch process conditions (see Table 5.4). The first etch was done by the Bosch process. It can be seen that via tapering effect is higher for vias $< 50\mu\text{m}$. It is also seen that via tapering is higher when SF_6 is increased and when Argon ions are added to plasma 106
- Figure 5.16 Optical micrographs of $221\text{-}228\mu\text{m}$ tapered silicon via after copper electroplating process (a) Main etch done by a non-Bosch etch process and (b) Main etch done by a Bosch etch process 107
- Figure 6.1 (a) 3D stacked silicon carriers using conventional wire-bonding scheme [163]. (b) Vertical integration of silicon carriers with flip-chip and wire-bonded devices [165]. (c) Single level carrier-based package with several assembled 3D ICs [164]. 110
- Figure 6.2 (a) Illustration of 3-D SIP platform formed by stacking 2 silicon carriers with through-silicon copper interconnections. Carrier thickness can typically be in the range of $200\text{-}300\mu\text{m}$. (b) Layout of through silicon vias on silicon carrier-1 and 2 for evaluating the TSV and wafer stacking process. 115
- Figure 6.3 Illustration of a multi-step TSV etch process technology. (a) In the first step, a Bosch etch is used to achieve $\sim 50\%$ of full TSV depth. (b) In the second step, a tapered reactive ion etch process is used to the remaining depth of the via. (c) In the third step, the resist mask and sidewall polymers are cleared by a wet clean process. (d) In the last step the sharp corners at the top is removed by global isotropic etch process to achieve the desired taper angle and top via dimension. 119
- Figure 6.4 (a) Trend chart showing the variation of taper angle as trench/via width is varied from $10\text{-}100\mu\text{m}$. It can be seen that by adding the third etch step (Recipe-D) the slope increases by as much as $1\text{-}2$ degrees. (b) Chart shows the trend of change in angle for when trench width varies from $10\text{-}100\mu\text{m}$ for recipes A to E. 121
- Figure 6.5 (a) Trend chart due to Recipe-A (Bosch) showing the variation of etch depth as a function of etch process time for trenches from $10\text{-}100\mu\text{m}$. (b) Chart shows the trend of RIE lag as trench width varies from $10\text{-}100\mu\text{m}$ when etch time is increased. 121

Figure 6.6	(a) Chart shows variation of trench depth as trench width is varied from 10-100 μ m. The depth due to recipe-A and B is not same as A+B. (b) Chart shows the trend of RIE lag when trench width varies from 10-100 μ m for recipes A to E. The RIE lag changes significantly for trench widths below 50 μ m.	122
Figure 6.7	(a) Chart showing variation of top trench width as trench width is varied from 10-100 μ m. The trench width variation is linear for all recipes conditions. (b) Chart shows the trend of Etch rate when trench width varies from 10-100 μ m for recipes A to E. The etch rate drops significantly from recipe A to E due to drop in etch depth (Refer to Chapter 5, Section 5.5.3).	123
Figure 6.8	SEM cross-sectional results of 300 μ m deep via formed by multi-step etch process described in Fig. 6.3. (a) Cross-sectional results after first etch by the Bosch process when 50 μ m diameter vias are etched to a depth in the range of 150-160 μ m. (b) Tapered etch profile formed after second etch by a controlled isotropic etch process. (c) Final tapered via profile after the sharp corner at the top is removed by a global isotropic etch process.	125
Figure 6.9	SEM micrographs showing via at the top after performing the via tapering process on vias formed by (a) Bosch and (b) non-Bosch etch process.	125
Figure 6.10	Optical microscope images showing top-view of vias after each stage of the multi-step via tapering process.	126
Figure 6.11	SEM micrographs of 100 μ m and 200 μ m deep vias etched by dual-etch process which is part of the generic multi-step tapered via etch process described in Fig. 6.3.	126
Figure 6.12	(a) SEM micrographs of 200 μ m deep via etched by dual-etch process. (b) SEM micrograph of 200 μ m deep via etched by Multi-step etch process to achieve the same target via geometry. (c) Image of 300 μ m deep vias etched by multi-step etch process to achieve similar top and bottom geometry of the via.	127
Figure 6.13	(a) SEM cross-sectional micrograph of void-free electroplated copper via formed after the via sidewalls are isolated by low-temperature silicon dioxide. (b-d) SEM micrographs of higher magnification view of sidewall isolation oxide at top, middle and bottom of the via.	129
Figure 6.14	(a) SEM micrograph of 200 μ m deep tapered vias filled with electroplated copper after multi-step tapered via etch process described in Fig. 6.3.	131

Figure 6.15	(a) SEM micrograph of 300 μ m deep tapered via formed by multi-step tapered via etch process described in Figure 6.3. (b) Optical microscope image showing void-free electroplated copper vias.	131
Figure 6.16	Optical image of cross-sectioned silicon carrier wafer showing a void-free electroplated copper vias. The silicon carrier wafer was back grinded and polished to expose the copper vias on both sides.	132
Figure 7.1	(a) Illustration of top view of test vehicle designed to evaluate the leakage between adjacent vias of different etch profiles like (b) tapered and smooth profile, (c) straight and scalloped sidewall, (d) tapered and curved profile and (e) scalloped and reentrant profile with larger scallop size.	146
Figure 7.2	Optical images of the cross-section of five silicon via samples etched with different recipes (a) A1, (b) C1, (c) F1, (d) B1 and (e) E1 respectively as shown in Table 2 and 3.	146
Figure 7.3	SEM cross-sectional micrographs of samples etched with Recipe (a) A1, (b) C1, (c) B1 and (d) E1 respectively. The roughness measured in each samples is also shown. It can be seen that the scallops is very high for Recipe C1 (see (b)) compared to A1 (see (a)). The results shown in (d) show that the curvature formed by RIE process shown in (c) is removed after global isotropic etch process D1.	147
Figure 7.4	Leakage current in deep silicon vias etched by Recipe A1 with vertical profile and a peak to peak sidewall roughness of $\sim 0.10\mu$ m. (a) I-V plot at room temperatures (RT) and 100 °C with current expressed in log-scale, (b) Plot of $\ln(I/V)$ versus $\sqrt{V}$ and (c) Plot of $\ln(I/V^2)$ versus reciprocal of V.	150
Figure 7.5	Cross sectional measurements done at the top and bottom of a via etched by Recipe A1 with vertical profile and sidewall roughness of 0.05-0.10 μ m. (a) Shows dielectric (SiO ₂) thinning from 2.0 μ m to 1.2 μ m due to vertical profile and (b) Further thinning of dielectric from 1.2 μ m at the top to 0.27-0.30 μ m at the bottom.	151
Figure 7.6	Leakage current in deep silicon vias etched by Recipe C1 with a reentrant profile and larger peak to peak sidewall roughness of 0.2-0.3 μ m. (a) I-V plot with current expressed in log-scale, (b) Plot of I versus V ² and (c) Plot of $\ln(I/V)$ versus $\sqrt{V}$.	152
Figure 7.7	Cross-sectional measurement done at the top and bottom of deep silicon vias etched by Recipe-C1 with reentrant profile and larger peak to peak sidewall roughness of 0.2-0.3 μ m. (a) Shows dielectric (SiO ₂) thickness varying from ~ 0.86 -1.0 μ m due to scallops at the top and (b) Dielectric thinning from 1.0 μ m at the top to 0.17-0.38 μ m at the bottom.	153

- Figure 7.8 Leakage current in deep silicon vias etched by dual-etch via tapering process Recipe F1 (i.e., a Bosch etch C1+ Global isotropic etch D1) which converts the reentrant profile shown in Fig. 2(b) to a slightly tapered profile at the top. (a) Shows I-V plot with current in log-scale, (b) Plot of $\ln(I/V)$ versus $\sqrt{V}$ and (c) Plot of $\ln(I/V^2)$ versus reciprocal of V . 154
- Figure 7.9 Cross-sectional measurements done at the top and bottom of silicon vias etched by dual-etch via tapering Recipe F1. (a) Shows conformal dielectric (SiO_2) deposition at the top due to tapered profile and (b) Dielectric thickness varies from 0.38-0.48 μm at the bottom due to scallops prevailing at the bottom. 155
- Figure 7.10 Leakage current in deep silicon vias etched by tapered RIE-etch Recipe B1 which creates tapered profile but with a sharp curvature at the top as shown in Fig. 7.2(d). (a) Shows I-V plot with leakage current in log-scale. It can be seen that the leakage current at 100 °C increases at the rate of 1.0 pico-amps/volt. (b) The I-V plot in 0-15V range shows Ionic conduction behavior where the slope decreases with increase in temperature. 157
- Figure 7.11 SEM micrographs of deep silicon vias etched by tapered RIE-etch Recipe B1 which creates tapered profile with a sharp curvature at the top. The cross-section micrographs were analyzed after a dielectric and metal deposition. (a) Shows non-conformal dielectric (SiO_2) deposition at the top due to curvature and (b) Smoother sidewall profile seen at the bottom with minimum dielectric thickness variation of 0.29-0.30 μm . 157
- Figure 7.12 Leakage current in deep silicon vias etched by a dual-etch via tapering process i.e., Recipe E1 (i.e., a non-Bosch etch B1 and a Global isotropic etch D1). (a) Shows I-V plot with leakage current in log-scale. Due to reduced curvature at the top, the leakage current at 100 °C increases at a lower rate of 0.3 pico-amps/volt. (b) The I-V plot shows an Ionic conduction mechanism in the range of 0-25V where the slope decreases with increase in temperature. 158
- Figure 7.13 SEM micrographs showing deep silicon vias etched by a dual-etch via tapering process Recipe E1 which has converted the curved profile (See Fig. 7.2(d)) to a smoother tapered profile at the top (See Fig. 7.2(e)). (a) Shows a more conformal dielectric (SiO_2) deposition at the top due to reduced curvature compared to Fig-7.11(a). (b) Smoother sidewall profile seen at the bottom with minimum dielectric thickness variation of 0.41-0.44 μm . 159
- Figure 7.14 Consolidated I-V trend of leakage current due to recipe A1 to F1 at 22 and 100 °C 160

Figure A-1 Within wafer CMP dishing measured at 5 sites across 2 wafers with 167
profiler. The mean dishing is 363 nm with within wafer variation of
50 nm

LIST OF TABLES

Table 2.1	Summary of key features of the three types of DRIE processes [69, 70].	22
Table 3.1	Summary of important Athena Elite statements.	39
Table 3.2	Mechanical properties of Cu.	43
Table 3.3	Mechanical properties of SiO ₂ and Si.	43
Table 3.4	Mechanical properties of Si ₃ N ₄ .	43
Table 3.5	Mechanical properties of Ta.	43
Table 3.6	Stresses in TSV structure with TSV diameter/depth/width of 5µm.	44
Table 3.7	Stresses in TSV structure with via diameter of 50µm.	44
Table 3.8	Stresses in TSV structure with via depth of 100µm.	44
Table 4.1	Material properties @ 25 °C [121].	52
Table 4.2	Plastic model for copper.	52
Table 4.3	Summary of stresses on SiO ₂ and Cu for a 100 µm deep TSV with variation in diameter from 50-150 µm.	52
Table 4.4	Summary of stresses on SiO ₂ and Cu for 50 µm diameter vias with variation in depth from 50 to 150 µm.	52
Table 4.5	Summary of stresses in SiO ₂ and Cu due difference in sidewall condition due to Bosch (rough sidewall) and non-Bosch etch process (smooth sidewall).	52
Table 4.6	Summary of stresses in Tantalum barrier, SiO ₂ and Cu due difference in sidewall condition due to Bosch (rough sidewall) and non-Bosch etch process (smooth sidewall).	53
Table 4.7	Design table of Comb structure with 8 fingers.	58
Table 4.8	Process flow for test vehicle fabrication.	59
Table 4.9	Bosch and Non-Bosch etch process conditions used in this study.	63
Table 4.10	Summary of significant observation for various process conditions evaluated.	65
Table 4.11	Comparison of leakage current at 20V for test vehicles etched with Bosch, Non-Bosch and Hybrid etch process.	77

Development and Characterization of deep reactive ion etching technology for through silicon interconnection

Table 5.1	Process flow for silicon carrier fabrication.	86
Table 5.2	Etch rate characterization results of Bosch etch process.	90
Table 5.3	Etch rate characterization results of non-Bosch etch process.	93
Table 5.4	Summary of various Global isotropic etch processes evaluated for via tapering.	96
Table 5.5	Dual-etch via tapering process using Bosch and non-Bosch process.	96
Table 5.6	Comparison of experimental and simulation results of the dual-etch process.	98
Table 5.7	Simulation results of via tapering etch process with varying etch process time.	100
Table 6.1	TSV process flow for fabrication of silicon carrier.	117
Table 6.2	Recipe-A, B and D are three components of a 3-step tapered TSV etch process. The table also shows the effect of each etch process on taper angle formed.	120
Table 6.3	The table shows the trend of etch depth and RIE lag due to Bosch etch process as etch time is increased. It can be seen that the RIE lag increases with increase in time.	120
Table 6.4	The table also shows the effect of each etch process (A-E) on trench depth achieved and the impact on RIE lag due to each recipe condition	122
Table 6.5	Effect of each etch process step on trench width at the top.	123
Table 6.6	Summary of via etch process characterization results of each recipe in a multi-step process. Recipe-A and B are etched for 50 min each.	127
Table 6.7	Summary of low-temperature deposition process	129
Table 6.8	Process parameter for via exposure by back-grinding and polishing.	133
Table 6.9	Through silicon via continuity test results.	136
Table 7.1	Summary of electrical conduction processes in insulators [7].	144
Table 7.2	Process flow used for testing leakage current due to various via profiles.	147
Table 7.3	Recipes used for the evaluation of vias with different profiles and sidewall roughness.	148
Table 7.4	Summary of recipes used and conduction mechanism observed.	159
Table 7.5	Impact of profile and sidewall roughness on leakage current measured at 20V at room temperature	160

Development and Characterization of deep reactive ion etching
technology for through silicon interconnection

Table A-1	Within wafer variation measured in dielectric and metallization processes	167
Table A-2	Within wafer CMP dishing measured at 5 sites across 2 wafers with profiler	167
Table A-3	Variations in dielectric, barrier films and sidewall roughness within TSV test structure (See Fig 4.7) measured by SEM cross-section through the 5 μ m test structure	168
Table A-4	Variations in dielectric, barrier films and sidewall roughness within TSV test structure measured by SEM cross-section through the 35 μ m test structure	168
Table A-5	Electrical leakage current measurement results at 22 °C to study the impact of different process condition (See Table 4.10). The results are presented in Fig 4.13 to 4.16	169
Table A-6	Electrical leakage current measurement of TSV test structure with 5 μ m width and 100 μ m trench depth at different temperatures (50-200 °C) [See Fig 4.17]	173
Table A-7	Electrical leakage current measurement results at room temperature (22 °C) and 100 °C to study the impact of etch profile and sidewall defects due to silicon via etch process on dielectric conduction mechanism. The results are presented in Fig 7.4-7.13)	174
Table A-8	Measurement of variations in dielectric, Ti/Cu metallization and sidewall roughness at top and bottom of the 50 μ m diameter TSV test structure measured by SEM cross-section analysis	176

Chapter 1

1. Introduction

1.1 OVERVIEW

Last four decades have seen the computing applications driving innovations and developments in semiconductor industries to achieve improvements in electronic products. These improvements were made possible by the semiconductor industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated electronic circuits. The most frequently cited circuit integration trend is also known as the Moore's Law, *i.e.*, the number of components per chip doubles roughly every 24 months. The Moore's Law has also enabled large R&D investments in the last three decades, motivating industry and research collaborations [1]. Figures 1.1 and 1.2 show the miniaturization trend that has been driving the semiconductor industry.

Figure 1.1: Trends for the smallest transistor gate length and minimum interconnect width in an integrated electronic circuit [1].

Figure 1.2: SEM cross-sectional micrographs of six metal level interconnection in a 0.13 μm technology showing the decrease of interconnect dimensions for the layers that are closer to the silicon devices [1].

1.2 MOTIVATION FOR THREE DIMENSIONAL INTEGRATION

Due to the shrinking dimensions of interconnects and hence a reduced two dimensional (2D) real estate for placement and routing of interconnections, a need has emerged to look for alternate interconnection architectures. Researchers in Stanford University have studied the pros and cons of 2D and three dimensional (3D) architectures through stochastic modeling and have shown the limitations in 2D interconnection architecture with an increase in the number of levels of interconnects and pointed out that significant improvements can be achieved by using a 3D wiring architecture [2]. In today's technology, it is the interconnect and not the device geometry that ultimately limits the speed and performance as we move towards gigascale integration [3]. This shift from the

front-end to the back-end (interconnect) of the silicon technology started happening in the late nineties when aluminum was getting replaced with copper as interconnect material [4].

Figure 1.3: Multi chip sensor module is shown with lateral placement of components. A vision of 3D hyper integration of multiple functional modules is also shown by vertical placement. The stacked modules will be interconnected by through silicon vias (TSV) which is not shown in the figure [5, 6].

James *et al.* proposed a generic three dimensional hyper integration architecture (See Fig. 1.3) which transcends from the traditional 2D Multi-Chip Module (MCM) approach [5] to vertical integration of the various functional modules [6]. It was later successfully shown by IBM that wafer scale 3D integration can be done by using through silicon vias (TSV) using various integration schemes [7]. It has also been shown that silicon on insulator (SOI) based CMOS wafers can also be face-to-face bonded to form vertically integrated IC without having to do any TSVs. Instead, the buried oxide in SOI is used as the dielectric layer to form the interconnection [8]. 3D integration can be done by directly bonding devices at chip level [9], at wafer level [10] or by chip to wafer bonding

[11]. In yet another approach known as the interposer or carrier based 3D integration, chips are assembled on carriers and then stacked to form 3D Microsystems [12].

In all these diverse 3D stacking approaches, the wiring between the stacked chips is done by through silicon metal feed-through or TSV. Deep reactive ion etching (DRIE) by Bosch etch process [13], conventional reactive ion etching (RIE) [14], laser drilling [15], ultrasonic drilling and high resolution powder blast micromachining [16, 17] are some of the known methods for TSV fabrication. The DRIE by Bosch process or the RIE method are the most common and preferred techniques for TSV fabrication [18]. The present research work reported in this thesis therefore focuses on this enabling process. A detailed study of DRIE process development and characterization has been carried out specifically for TSV application.

1.3 CHALLENGES CONFRONTING SILICON VIA ETCH TECHNOLOGY

A typical vertically integrated 3D Microsystems package architecture is illustrated in Fig. 1.4 with two silicon carriers using TSV interconnections. It may be noted that the silicon carrier based 3D package is a variant of 3D stacked package on package (PoP) shown (See Fig 1.5 and 1.6) which uses organic substrate with through vias instead of silicon substrate. Hence, the 3D stacking is carried out in assembly and packaging facility. As the infrastructure at packaging industries are limited, the TSV geometry is typically in the range of 10-50 μ m diameter with carrier thickness of 100-300 μ m. Key focus for adoption of TSV technology would require new materials to be development for thin wafer handling, inter-level dielectric and redistribution metallization.

The main supply chain of 3D IC or 3D package is decided by the process integration scheme used. If a wafer scale TSV chip stacking approach is adopted [7, 10],

the TSV technology can be integrated as an extension of wafer fab BEOL technology. However, this imposes severe constraints on the silicon via etch technology, the materials used and its thermal budgets to minimize the thermal stress on the through silicon interconnects. Based on the 2008 ITRS high density TSV (HDTSV) draft specifications [3], the diameter of TSV for 3D IC is expected to be scaled down to 1.0 μm with via depth of 10 μm and minimum via to via spacing of 1.5 μm by the year 2015. The 3D stacked devices are formed by various wafer level bonding media [10] to eventually yield a vertically interconnected functional 3D IC. Figure 1.4 shows 3D IC assembled on 3D package. It also illustrates the critical silicon via etch technology challenges that need to be addressed (a, g, f) which is discussed further in following section.

The figure also shows some of the major silicon via etch technology challenges due to straight and tapered etch process. The aggressive DRIE chemistry used in TSV process creates several undesirable effects like the sidewall scallops and curvatures [13, 19]. The effect of the sidewall scallops (due to Bosch etch) on the uniformity of plasma deposited silicon dioxide and interconnect metallization consisting of copper diffusion barrier, copper seed metallization and electroplated copper are shown in micrographs (a), (g) and (f) respectively in Fig. 1.4 [20]. The scallops can affect the continuity of the dielectric and copper metallization layers which eventually affect the performance of the TSV interconnection. Micrograph (b) in Fig. 1.4 shows another challenge that needs to be dealt with while performing the silicon via etch and stop on the insulating under-layer. This is a typical issue in via-last silicon etch process which requires prevention of any dielectric charging at the silicon-oxide interface to avoid potential notching at the base [21]. Notch creates a discontinuity in the dielectric and the metal deposition process, which, in

turn, affects the electrical performance of a TSV interconnection. Lastly, the micrographs (c-e) in Fig. 1.4 show the adverse effects of sidewall curvature due to tapered via etch process in the Inductively Coupled Plasma (ICP) RIE system, which again affects the step coverage during the dielectric and the metal deposition process [19]. Some of these issues are addressed in the present research work.

Figure-1.4: A typical vertically stacked 3D Microsystem architecture is illustrated with 2 silicon carriers with through silicon interconnections. Also shown in the figure are some of the major technology challenges encountered during the integration of a TSV technology.

Figure 1.5: 3D stacked package using organic substrates with through vias. Courtesy: Amkor

Figure 1.6: 3D stacked package using organic substrate with through vias. Courtesy: STATs Chip PAC

1.4 MOTIVATION AND RESEARCH OBJECTIVES

1.4.1 Motivation

Though the DRIE technology was introduced for MEMS application in early nineties [13, 22], its use in wafer level packaging and 3D IC application started only in 1997 [18]. Hence, this technology is still evolving and developing. It is therefore the motivation of this research work to focus on the silicon DRIE technology and perform various fundamental characterization studies to understand the underlying mechanisms driving the formation of straight and tapered via profile and also understand some of the (undesirable) failure mechanisms and its impact on electrical isolation. It is also the motivation of this work to model the impact of thermo-mechanical stress on the deep silicon vias formed by Bosch etch process and correlate it with experimental results.

1.4.2 Research Objectives

The objective of this research is to develop and characterize extensively the deep silicon etch technology for TSV application. In the first part of the study, the failure modes and failure mechanisms due to Bosch etching process with depths smaller than $30\mu\text{m}$ having straight via profiles will be characterized. Straight via profiles are preferred for

wafer level 3D IC applications [10] where the via dimensions are smaller than $10\mu\text{m}$. While the 3D integration approach has been demonstrated by many researchers with the Bosch etch process, there is still no comprehensive study conducted on the impact of the sidewall roughness due to series of isotropic etching steps and its impact on the electrical leakage characteristics. The impact of thermo-mechanical stresses caused by the thermal loading due to post-TSV metallization processes and its effects on the electrical performance will also be studied.

The second part of the research focuses on the development and characterization of tapered silicon via etch technology for Interposer or Carrier based 3D integration application with via diameters of $20\text{-}100\mu\text{m}$ and depth of $100\text{-}300\mu\text{m}$. As no single etch process can meet all the requirements for such application, it is intended to develop and characterize a multi-step etch process which combines the best features of three different etch processes, *viz.*, the Bosch etch process, the RIE process and the isotropic etch process. Finally, the tapered silicon etch process will be integrated into the fabrication technology of silicon interposer with through silicon interconnection. It will be demonstrated that a void-free through silicon interconnect can be achieved with good electrical isolation.

In the third part of the research, the electrical conduction mechanism responsible for leakage through the sidewall isolation dielectric in deep silicon via is studied. The influence of deep silicon via profile and sidewall roughness on electrical conduction will also be studied.

1.5 MAJOR CONTRIBUTIONS OF THE THESIS

- 1.5.1** Deep silicon copper interconnection related failure mechanisms caused by the wavy sidewall roughness due Bosch etch process has been studied by developing a test vehicle to evaluate various etch processes. The sidewall roughness induced by various DRIE processes has been evaluated to determine a viable etch process for 3D IC application [23, 24].
- 1.5.2** Bosch DRIE process has been extensively investigated for eventual implementation in 3D IC. The present work focuses on thermo-mechanical stresses caused by thermal loading due to post-TSV processes and its impact on the electrical performance of TSV copper interconnect. A clear correlation between high leakage current behavior (due to non-uniform Ta barrier deposition over the rough sidewalls) and the thermo-mechanical stress induced by post-TSV metallization processes is shown [23, 25].
- 1.5.3** A novel dual etch process technology has been demonstrated, which provides opportunity to precisely and independently control the required via slope that is required to achieve conformal deposition of the dielectric, copper diffusion barrier and copper seed metallization. By partitioning the via formation process into an anisotropic etch and an isotropic etch process, it is possible to maintain high overall etch rates without compromising on the final via profile and throughput. The via profile achieved has been extensively characterized with respect to a wide range of critical process parameters and via geometries. It is demonstrated that regardless of

the choice of via formation method, it is feasible to achieve a controllable via taper to realize a void-free copper via-filling by electroplating process [26-28].

1.5.4 A deep silicon via tapering process has been evaluated as a plug-in process for tailoring with disparate etch technologies for achieving tapered via profile. It is intended to be a manufacturable solution for tapering and smoothening sidewalls of very deep silicon blind vias formed by different methods like Bosch and RIE process [29].

1.5.5 A novel three-step tapered via etching process has been developed and demonstrated as a viable process for fabricating a void-free through-silicon copper interconnection structure for TSV structures in the range of 250-350 μm . Plasma etch mechanisms responsible for the step-by-step evolution of tapered silicon via profile angle in the desirable range of 83–87° are discussed in detail. It is further shown that this multi-step etch process enables the formation of void-free copper vias for via depths close to 300 μm [30].

1.5.6 Athena Elite topography simulation study was done for TSV application. Elite predicts the topology evolution during complex multi-step RIE processes by using the string algorithm. The topology process is modeled by defining isotropic, chemical, directional and divergence parameters. The simulated topology was then validated by actual experimental data. Manuscript has been submitted to Journal of Micromechanics and Microengineering which is presently under review.

1.5.7 A detailed overview of silicon carrier based packaging for 3D system in packaging application has been reviewed. In this work, the various critical process modules that play a vital role in the integration and fabrication of silicon carrier with high

aspect ratio tapered through-silicon interconnections have been explained and discussed with experimental data. A low-temperature dielectric deposition process is also developed with good dielectric coverage on the via sidewall. The final integration of the tapered silicon RIE process with silicon carrier fabrication process technology has been demonstrated and electrically tested [31, 32].

1.6 ORGANIZATION OF THE THESIS

This thesis consists of eight chapters. Chapter 1 explains the background and motivation as well as objectives and major contribution of this thesis. Chapter 2 provides a detailed literature review of the deep reactive ion etching technology for TSV application. Chapter 3 explains about the simulation and modeling tools and techniques used in this research to characterize the straight and tapered silicon via etch process. The first part of the chapter is devoted to etch topographical simulation with Athena Elite from Silvaco. The second part of the chapter focuses on thermo-mechanical simulation work by finite element analysis with ANSYS. Chapter 4 describes the study of failure mechanisms due to Bosch etch process when it is used for TSV application. This study also addresses the challenges and potential solutions to deal with thermo-mechanical stresses as a result of thermal cycles during post-via etch integration processes. Chapter 5 describes the development and characterization of novel dual-etch tapered via etch technology for TSV application. Chapter 6 discusses the methodology to integrate the tapered silicon etch process to fabricate the silicon carrier wafer with through silicon interconnections. In this work, the TSV process is integrated with wafer thinning and assembled with test dies to form 3D stacked silicon module. Thermal cycling and Electrical continuity test results are

also presented. Chapter 7 studies the influence of sidewall roughness and deep silicon via etch profiles on electrical leakage current and its conduction mechanism based on classical dielectric conduction models. Chapter 8 discusses the overall conclusions and recommendations for further work.

Chapter 2

2. Literature Review

2.1 OVERVIEW OF ETCH TECHNOLOGIES FOR TSV APPLICATION

Silicon micromachining or bulk silicon etching technology has emerged as industry's major work-horse for silicon micro-structuring due its ubiquitous application. Bulk silicon etching or silicon micromaching refers to etching microstructures or forming deep recesses into silicon substrate to form electronic, mechanical or electro-mechanical components [33]. Silicon micromachining technology is also used to sculpt silicon to form micro-molds which is used for fabricating molded micro-parts [34]. In this chapter, various etch technology options for TSV and their pros and cons are discussed. The main reasons for selecting deep reactive ion etching technique and the motivation to choose an inductive coupled plasma (ICP) system for performing deep reactive ion etching is also discussed.

One of the most important requirement for a through silicon interconnect or through silicon via for its implementation in 3D Microsystems or 3D ICs is its performance as a reliable electrical interconnect [35]. Though copper damascene technology has been widely studied as a 2D IC interconnect [36] and as a through silicon interconnect in 3D IC applications [35], it has however been researched upon much less as through silicon interconnect structure. Figure 1.4 in Chapter 1 gives an overview of various TSV interconnect related challenges.

The scope and focus of this research is devoted to the development and characterization of deep reactive ion etching process and study its impact on electrical isolation of the through silicon interconnect structure. The first part of the research focuses

on challenges, failure mechanisms and its resolution in a vertical TSV structure fabricated by Bosch etch process. The second part of the study is on the development and characterization of deep silicon tapered etch process. Extensive electrical characterization has been done for straight and tapered via structures formed by Bosch and RIE process. Finally, the electrical leakage current mechanism through the dielectric isolation has been studied and explained. This literature review has been split into two sections. The first part explores various silicon via etch technologies available with its pros and cons. The second part reviews silicon via etch technology related issues that have been studied and characterized by Industries and Research community.

2.2 SILICON VIA ETCH TECHNOLOGY OPTIONS

2.2.1 Orientation Dependent Anisotropic Wet Etching

Silicon substrate being a monolithic material has a unique crystalline orientation which was traditionally utilized for performing orientation dependent wet etching with potassium hydroxide (KOH) and tetra methyl ammonium hydroxide (TMAH). The crystal structure of silicon is that of the diamond type with lattice constant $a = 357 \text{ \AA}$. The structure is face centered cubic (FCC) but with two atoms in the unit cell. Figure 2.1 shows the tapered etch profile achievable with silicon wafer of orientation $\langle 100 \rangle$. Following reaction is expected to take place with alkaline solution:

A major advantage of this method of micromachining is that it is low-cost technology requiring simple wet process stations and low-cost cost chemicals. However, the pattern size cannot be scaled down for deeper trenches as the depth is self-limited by

the formation of V-shape. Another major limitation of this method is that it can only result in tapered profile due to definite orientation of monolithic silicon substrate. One way to overcome this limitation is to choose silicon substrate of different orientation depending on the profile requirement. For example, to achieve a vertical profile one needs a choose silicon substrate with $\langle 110 \rangle$ orientation [33]. Though the wet anisotropic etch process is not versatile enough for all types of etching applications it nevertheless has many a niche applications like MEMS and Electro-optical sub-assembly platforms fabrication [39]. Wet anisotropic etching has also been used in through silicon via fabrication for 3D MEMS packaging application. Figure 2.2 shows the cross-section view of MEMS package with a hermetic sealing cap wafer. The cap wafer has through silicon interconnections formed by anisotropic wet etching process to facilitate conformal metallization over tapered TSV structures as demonstrated by Hymite [40] and Ångström Aerospace Corporation (ÅAC) [41].

Figure 2.1: Orientation dependent wet etching of $\langle 100 \rangle$ silicon [38].

Figure 2.2: (a) Hymite's patented tapered through silicon via technology with hermetic sealed cap wafer with plated through silicon interconnection for MEMS packaging [40]. (b) KOH + DRIE etched TSV structure by Ångström Aerospace Corporation (ÅAC) [41].

2.2.2 Plasma Etching

In contrast to wet etching technique, plasma etching does not use wet chemicals to etch patterns. It uses chemically active radicals and ions to etch materials. The etching precursors are derived from gaseous plasma. A plasma is a highly ionized gaseous medium made of reactive (but neutral) free radical, ions (which are charged), neutral gases, heat and UV light (emitted from excited states of the gas molecules, radicals and ions) [42].

Plasma etching was a mature technique to etch layers for production of integrated circuits (ICs) in seventies [43] which further developed into Reactive Ion Etching (RIE) through innovations in reactor designs. RIE is now the main technology in large volume production [44]. In the nineties, several new techniques emerged to achieve high density plasma without causing plasma damage to wafer surface. In the RIE mode one requires an RF power in the range of 300-1000 W to generate enough reactive precursors. A major limitation of RIE configuration is that it uses same RF source to produce reactive plasma which generates a fixed DC potential that accelerates the reactive ions towards the target substrate for etching. As a consequence, an increase in ionization or dissociation is always accompanied by an increase in DC potential with resultant damage to the material or

substrate being etched. Hence, such a system can only generate low-density plasma of $10^9 - 10^{10} \text{ cm}^{-3}$ with average electron energy of 1-10 eV [45].

In the nineties several new techniques emerged to achieve high density plasma without causing plasma damage to wafer surface. These techniques basically decouple the plasma generation mechanism and plasma etching mechanism. The wafer to be etched is placed on the RF powered electrode so that the reactive ions in the positively charged glow region gets attracted towards the wafer surface with the help of external bias potential to initiate a directional or anisotropic etching reaction. In this mode, the plasma is mainly created by a separate RF source while the wafer holding electrode is powered by another RF source which draws the reactive ions across the sheath to perform etch. As the RF power applied to the wafer is not required to ionize the gas, only small amount of power is needed (typically $< 100 \text{ W}$). Thus the damage to the wafer can be minimized significantly [46]. Some of these decoupled high density RIE systems are magnetically enhanced reactive ion etchers (MERIE), Inductive coupled plasma (ICP) etcher and electron cyclotron resonance (ECR) etching systems, which can produce very high plasma density in the range of $10^{10} - 10^{13} \text{ cm}^{-3}$ [47, 48]. ICP systems are commonly preferred for silicon DRIE applications due to their ability to operate in wider pressure range of 10-100 millitorr, unlike the other high density plasma sources like MERIE and ECR. Some of the ICP etch process modes like Bosch etch, ICP-RIE and Cryogenic RIE will be discussed in following sections.

2.2.3 Bosch etch Process

The Bosch etch process or time multiplexed deep etching (TMDE) process was pioneered by Laermer and Schilp of Robert Bosch GmbH in the year 1996 [49]. It consists

of series of repetitive short steps of etching and passivation (typically 4-10 seconds) until the required etch depth has been achieved. The cyclical nature of etch and passivation steps results in a waved sidewall profile as shown in Fig. 2.3(a). The etching and passivating gases and RF power are controlled independently as the plasma alternates between an etching and passivation steps as shown in Fig. 2.3(b) [50, 51]. This switched etch and passivation process results in a wavy sidewall profile as shown in Fig. 2.3(c). It may be noted that the directional ion bombardment from etch step promotes the preferential removal of the passivation film deposited from the previous passivation step on horizontal surfaces, allowing the profile to evolve in a highly anisotropic fashion (See Fig. 2.3(c)). It has now paved the way to development of bulk micromachined MEMS by using this technique [52]. Powell *et al.* of Aviza Technology Ltd, UK, has demonstrated that Bosch etch process can be used to achieve void-free copper via-filling. It has also been shown that sidewall roughness due to Bosch etch process can significantly affect dielectric and metal step coverage and via-filling [53]. Song *et al.* of Institute of Microelectronics, Beijing, China, have shown that high aspect TSV with aspect ratio of 10 and 20 μm via diameter can be formed by Bosch etch process. As the via aspect ratio is > 5 , they have overcome the limitation of via-filling by doing bottom via plating [54]. . Van Aelst *et al.* of IMEC, Belgium, have shown that it is possible to reduce or eliminate the undercuts due to Bosch etch process by using a dual mask approach to compensate for the undercut [55]. However, no detailed study has been done on the impact of the sidewall ripples or scallops on its performance as through silicon interconnect. Chapter 4 focuses on studying the effect of sidewall roughness on its electrical performance.

Figure 2.3: Etch/Passivation gases and Bias power switching is plotted as a function of process time in a typical Bosch etch process. The SF_6 and C_4F_8 is switched at intervals corresponding to etch and passivation cycle time. The Platen bias power is also switched along with the gases. SEM micrograph shows results achieved with a typical Bosch etch process with enlarged images of top and bottom portion of the trench.

2.2.4 Reactive Ion Etch Process

Commercial decoupled ICP DRIE system can be configured to operate with **switched** or **fixed** RF source and bias power mode. Under a switched mode, it can run Bosch process and under a fixed ICP coil and bias power, it operates in RIE mode. In a fixed or continuous RF power mode, it results in a smoother sidewall compare to Bosch etch process [56]. However, as the sidewall passivation is done continuously, the achievable etch rate and selectivity to mask is much lower compared to Bosch etch process. It may be noted that unlike in cryogenic DRIE process which operates at -110 to -80 °C [57], the ICP RIE process operates at close to room temperature. Fluorine based etch process (from Sulfur hexafluoride (SF_6)) is commonly preferred for MEMS and TSV applications as very high etch rates are achievable with conventional RIE tools [58].

Carbon tetrafluoride (CF_4), nitrogen trifluoride (NF_3), chlorine (Cl_2) and hydrogen bromide (HBr) chemistries are also being used for shallow silicon trenches with slower etch rates ($<1.0\mu\text{m}/\text{min}$) and better process control [59].

Figure 2.4: (a) Optical cross sectional images of $20\mu\text{m}$ wide trench etched by RIE process using SF_6 , O_2 , Ar chemistry. (b) Cross sectional image after partial isotropic silicon etch process and (c) Cross sectional images of same trench etched by more isotropic etch process.

Some of the major challenges in continuous deep silicon etching process are in achieving good control on etch profile and sidewall roughness due to chemically aggressive nature of SF_6 plasma [58]. With proper balance between isotropic etch and sidewall passivation chemistry it is possible to achieve tapered to vertical etch profile with minimum notch at the top (see Fig. 2.4(a)-(c)). Li *et al.* at Delft University of Technology have also done detailed study to reduce the sidewall curvature at the top to achieve a tapered etch profile [60]. Hence, the continuous etching DRIE process is highly suitable for tapered TSV application as in low aspect ratio applications [61]. In this research work, detailed process development and characterization studies have been done with silicon via

etch depth and aspect ratios much higher than what has been attempted in other contemporary research studies [60-63]. Chapter 5 discusses 2-step and 3-step etch process to achieve TSV depths from 200-300 μm for via dimensions in the range from 10-100 μm .

2.2.5 Cryogenic RIE Process

In cryogenic RIE process, the wafer is chilled to -110 to -80 °C using liquid nitrogen for cooling the wafer holding electrode during the silicon etch. The low temperature slows down the chemical reaction that produces isotropic etching. However, ions continue to bombard the silicon surfaces facing the plasma and etch them with vertical profile and smooth sidewalls. Cryogenic RIE process uses SF_6 and O_2 , at liquid nitrogen temperatures for deep silicon etching with extremely high etch selectivity with respect to silicon dioxide and photoresist of greater than 1000 [64, 65].

Figure 2.5: Cryogenic etch process trend as a function of wafer temperature. It can also be seen that the etch profile of $\langle 100 \rangle$ silicon is highly pressure dependent. It can also be seen that the process is sensitive to orientation of the silicon under higher pressure and lower ion flux [67, 68].

Table-2.1: Summary of key features of the three types of DRIE processes [69, 70].

Parameters	BOSCH DRIE	ICP DRIE	Cryogenic DRIE
Sidewall protection	Fluorocarbon polymer	SiO_xF_y	SiO_xF_y
Sidewall roughness	Wavy sidewalls due to F-based isotropic etch	Smooth sidewall with sharp curvature at top	Smooth sidewalls
Bias power	10-100 Watts	10-30 watts	15-20 watts
Mask selectivity (Resist)	60-70:1	25-30:1	> 100:1
Mask selectivity (SiO_2)	130-140:1	80-95:1	Upto 1000:1
Special hardware	Standard	Standard	Liquid N_2 cooled wafer holding electrode
Main advantages	<ul style="list-style-type: none"> Vertical profile with high etch rates (5-10$\mu\text{m}/\text{min}$) possible. Profile can be tapered by 1-2°. 	<ul style="list-style-type: none"> Tapered etch profile possible in the range of 70-90°. Etch rates ~3-4 $\mu\text{m}/\text{min}$ 	<ul style="list-style-type: none"> Smooth sidewalls with vertical/slight tapered etch profile possible. Etch rate < 5$\mu\text{m}/\text{min}$
Any issues	Sidewall roughness in range of 100-200nm	Tapered profile with sharp curvature at the top	Stress build-up due CTE mismatch at low temperature

Despite high selectivity and smooth sidewalls, the cryogenic etch process can potentially cause stress-induced cracking in photoresist etch masks [66] due large coefficient of thermal expansion (CTE) differences between mask and underlying silicon substrate. Another major concern with cryogenic etch process is that it highly temperature dependent and orientation dependent. It can be seen from Fig. 2.5 that as wafer temperature increases from cryogenic temperature to room temperature the undercut below the mask increases at the top. It may also be noted that as ion flux is increased to achieve higher etch rate and vertical profile, the undercut increases due to ion scattering effect at the top. However by decreasing the ion flux to control the undercut, it results in orientation dependent etch profile. Table 2.1 summarizes the key features of all the three competing DRIE process technologies.

2.2.6 Summary

Wet anisotropic etching technique has limited application in 3D integration technology as it is not scalable with increase in functional density and shrinkage in product dimensions. Combinations of wet and dry etch methods could only help in pushing the limits a little. Both the above approaches also have limitations due its inability to integrate in preprocessed CMOS wafers. Hence, wet and wet/dry etch approach has been used only in cases where via-first approach has been used. It is also used in 3D MEMS packaging and image sensing application where the aspect ratio requirements are not very demanding [71, 72].

Among the various dry etching options discussed in this section, Bosch and RIE processes have been widely used in TSV applications. Due to recent developments in ICP tools, high etch rates of 5-10 μ m/min are achievable by the Bosch process. RIE process on the other hand has the flexibility to tailor a wide range of silicon etch profile from straight to highly tapered profile. Cryogenic RIE however has several drawbacks due to the cryogenic temperature. Its heavy consumption of liquid nitrogen adds to the cost of the process. The exothermic silicon etching reaction and the liquid nitrogen substrate temperature results in severe stress on the etch mask and the underlying films [66, 69]. Further, fully processed wafers have multiple layers of metals and dielectric which have different CTE. Hence under cryogenic temperature the wafer can potentially warp under severely stress. Thus cryogenic-RIE is not preferred for TSV application. It is the focus of this research to study in greater details the ICP Bosch and RIE processes and extend its capability to TSV application.

2.3 DRIE PROCESS CHARACTERIZATION

2.3.1 Requirements for silicon via etch process:

Silicon via etch process requirements can be broadly classified for its final integration into either via-first or via-last 3D integration technology [73]. The via-first approach requires the silicon via etch to be done first and then wafer thinned to form the through wafer interconnection for chip-level or wafer-level stacking. The substrate used can be semi-processed, full-processed or un-processed silicon wafer. In case of via-last approach, the silicon via etch is done after the semi-processed or full-processed wafer thinned to required final thickness. The etch process requirements can further be classified based on its product requirements such as packing density or pitch of the TSV. The TSV top/bottom diameter, depth and taper angle are finally dictated by thickness of the silicon wafer and pitch of the I/O pads [73]. According to ITRS 2008 report, devices that could appear in production in near future would be using 3D BEOL-compatible 3D hyper-integration with $\leq 10\mu\text{m}$ silicon thickness. TSV diameter would be limited by silicon thickness and TSV aspect ratio. Similarly pitch would be limited by TSV diameter, misalignment tolerance and minimum pad spacing [74]. Wafer scale 3D integration approach looks most attractive as it allows bonded wafers to be thinned easily due to rigid support from one of the bonded wafer while the second wafer can be thinned down [75]. In case of via-first approach, popular with IDMs, the TSV diameters are generally in the range from 2-20 μm with aspect ratio of 3-10 [76]. In case of via-last integration approach, popular with packaging houses, the aspect ratios are usually in the range of 2-10:1 with via diameters in the range of 15-50 μm depending on the ability to achieve good dielectric and seed metallization [76, 77].

Figure 2.6: 3D IC technology and TSV Roadmap [79].

There is a third category of 3D integration approach which makes use of silicon carrier or interposer with TSV structures for 2D component assembly as in an organic substrate. The silicon carrier is then vertically integrated to form 3D Silicon Microsystems. The via diameters for such applications are usually 50-100 μm with a TSV depth of 100-300 μm [78]. Figure 2.6 shows the 3D IC technology roadmap which also gives an overview of the TSV diameter scenario in the Industry today according to market research firm Yole Development published in September 2008 in a webcast [79].

2.3.2 Silicon via etch process characterization studies:

To achieve optimum process performance it is necessary that the DRIE process be fully characterized for good etch rate uniformity or maintain minimum RIE lag across the wafer with minimum sidewall roughness. Franz Laermer of Robert Bosch GmbH had discussed in great detail in his review paper about characterization of RIE lag effects due to Bosch etch process [69]. Soren Jensen in his research work had studied pattern dependent and aspect ratio dependent loading effects [80]. R.A. Gottscho *et al.* from AT&T Bell Labs had shown that the RIE lags effects can be minimized by decreasing the substrate temperature [81]. These findings show that it is possible to find an operating regime for maintaining etch depth uniformity across the wafer for TSV application. In the present research work, new silicon via etch processes have been developed and characterized which combines Bosch and RIE process. Hence, similar work has not been attempted earlier.

Extensive amount of work has been done and published on improving the deep silicon etch profile by balancing etch and passivation cycles in Bosch etch process [82-83]. Janet Hopkins *et al.* from Surface Technology Systems, UK presented another way of achieving improved profile control in high aspect ratio microstructures by using process parameter ramping feature in ICP DRIE system. It has been shown that by continuously ramping the platen power and pressure, it is possible to achieve vertical profile with aspect ratios close to 20 [84]. Sidewall roughness reduction has been the main motivation in vertical mirror fabrication for Fiber-Optic Switching applications which requires sidewall roughness to be less than 50nm [85]. Lot of work had been done by optimizing the Bosch process parameters [85-87]. For the first time in this research work the sidewall roughness

has been further critically evaluated with respect to its impact on electrical leakage performance and effect on thermo-mechanical stresses due to post-TSV metallization processes which has been discussed in Chapter 4 of this thesis.

2.3.3 TSV electrical characterization

The ultimate goal of TSV is to serve as a reliable through-silicon electrical interconnect. As the packing density in a 3D IC increases, its ability to remove the heat generated by the stacked devices effectively becomes a major concern. Fortunately, if the TSV is designed appropriately, it can reduce the thermal resistance and help in better thermal management in a 3D IC [88]. J. U. Knickerbocker *et al.* of IBM have done extensive through silicon interconnection characterization by designing test vehicles with integrated passive components for studying RF signal integrity by using various 3D integration approaches [89]. P.S. Andry *et al.* went further in investigating various TSV materials like tungsten, copper, copper composite and solder and evaluated its via resistance, electrical yield, and current-carrying capacity [90]. Jun So Pak *et al.* of Terahertz Interconnection and Packaging Laboratory have done electrical characterization of TSV with different structural parameters such as via pitch, height and dielectric thickness. It was shown that as the resistivity of silicon increases, it is more effective for the DC and high frequency leakage currents to be blocked between signal and ground TSV [91].

As the TSV aspect ratio increases, it becomes very challenging to achieve good sidewall coverage with isolation dielectric, seed metal and finally achieve void-free via-fill. These factors affect the electrical performance in terms of via resistance and electrical isolation. Further, the sidewall smoothness or roughness also affects its electrical behaviors.

Based on the literature survey done, it was hard to find any published work on electrical leakage conduction between TSV structures and correlate it with process parameters and structural parameters like sidewall roughness and aspect ratio.

2.4 SUMMARY

Detailed literature review was done in two areas of the research work undertaken in this project: (a) Available silicon via etch technologies and factors driving the selection of silicon etch technology and (b) Silicon via etch process characterization studies done. Based on the literature studies done it is seen that Bosch and RIE technologies are most favored for high aspect ratio deep silicon via etch application. It was also seen that very limited studies have been done with mixed silicon etch technologies such as Bosch + RIE process. Also it is seen that there is almost no publication on multi-step DRIE technologies which offers greater opportunities than any single technology such as Bosch or RIE. It was also seen that most of the publications focused on electrical characterization of TSV structure such as electrical resistance measurement and RF characterization. There was almost no publications available on the DC characterization of TSV structures with respect to various etch process conditions. The present research work had done a detailed electrical characterization of TSV under various process conditions and eventually attempted to correlate the failure mechanisms with thermo-mechanical stresses imposed by TSV fabrication processes.

Chapter 3

Topography modeling and thermo-mechanical simulation for TSV

3.1 INTRODUCTION

As microfabrication technology becomes more complex with the increase in number of process steps, modeling surface topography becomes increasingly important for predicting the performance of the technology. Simulation also allows accurate prediction and optimization of the performance of a part or whole of the process technology with changing dimensions, materials and loads without the need to make any prototype. Surface topography affects the performance of photolithography and etching steps both of which are universal in microfabrication. As the feature size becomes smaller the surface topography variations and its impact on lithography and etch gains greater significance [92]. Whatever its physical details, the etching process can in many cases be modeled as a series of surface etching phenomena. Etching simulation starts from an initial profile that moves through a medium in which the speed of etching propagation can be a function of position and other variables that determine the final profile.

Simulation of surface topography evolution due to etch and deposition processes and the stresses thereon due to the thermal processes involved in the wafer fabrication processes is an important area of research in the semiconductor industry [93-95]. A lot of work has been done in studying and understanding the interactions of the semiconductor device fabrication processes on the reliability of two dimensional electrical interconnect

structures. A popular simulation software is “Fammos” from Synopsys which analyzes the stress evolution due semiconductor fabrication processes on 2D [96]. Similarly, a lot of work has been done in the area of electro-mechanical and electro-optical structural simulations. Electronic packaging is another area where a lots of different materials interact during the packaging process. Coefficient of thermal expansion (CTE) mismatch due to different materials like organics dielectric material, electrical interconnects materials and the silicon substrate results in various types of failures. In 3D ICs and 3D Microsystems, the stress-related issues get compounded and become severe due to stacking of several thin dies with TSV structures, various types of thin films and redistribution lines. Examples of well known failures include degradation of transistor performance and loss of standby power due to electrical leakages induced by thermo-mechanical stresses induced by adjacent shallow trench isolation (STI) structures on transistors [97] and the breakage of silicon substrates due to radial stress generated by copper filling the TSVs [98]. The sources of such stresses need to be accurately modeled to create appropriate design rules for reliability and yield of 3D ICs. Following simulation tools are commonly used for topography simulation and modeling:

- SPEEDIE: 2D simulator from Stanford University based on physical models for deposition and etching
- SAMPLE from University of California
- SHADE from IBM
- ELITE topography simulation tool from Silvaco
- VICTORY a 3D etch simulation software recently developed by Silvaco

- DIOS a two-dimensional process simulator developed initially by the Swiss company ISE.
- RECIPE a 2D and 3D DRIE etch process simulation tool developed by Intellisense
- TRAVIT an analog process simulator supplied by Abeamtech.

This chapter provides an overview of the simulation and modeling work that would be done in subsequent experimental work. The next section (Section 3.2) focuses on the topography simulation studies for modeling deep silicon via etch structures for TSV application by using Technology Computer Aided Design (TCAD) simulation software Athena Elite from Silvaco, CA (USA). The second part (Section 3.3) gives an overview of thermo-mechanical simulation with ANSYS.

3.2 TOPOGRAPHY SIMULATION WITH ATHENA ELITE

3.2.1 Athena overview

ATHENA is a high level simulation platform provided by Silvaco which integrates several process simulation modules in an interactive user-friendly environment. ATHENA provides a convenient platform for seamlessly simulating and integrating processes like ion implantation, diffusion, oxidation, lithography, plasma etching and deposition. The Athena platform is available to run on Sun, Linux and Windows platforms. ELITE is simulation module of ATHENA which allows the use of models for deposition and etch processes. Various etch process modes are modeled by defining a machine and invoking the machine to perform the required etch. ELITE can also model Monte Carlo etching process by using fluxes of atomic particles to emulate various etch modes. ELITE uses a string algorithm to describe topographical changes that occur during etching processes. This section describes

the models and techniques used in ELITE and the command language used to access model parameters.

3.2.2 Elite features and capabilities

Elite is a 2D topography simulator for modeling physical etching and deposition. It also contains Monte Carlo deposition and etch simulation capability, which provide atomistic etching and deposition models. However, as the simulation work done in this research study is based on the Elite models, the rest of this section will focus mainly on Elite. Elite offers the users the flexibility to model various types of plasma etch processes like isotropic chemical etch and directional etch. It can help in predicting complex etch topographies for various etch processes. Accurate prediction of profile evolution is extremely important to ensure good step-coverage of plasma deposited dielectric and metal films which eventually help in achieving seamless copper electroplating inside the deep silicon vias.

3.2.3 String Algorithm

The ELITE module of ATHENA platform allows the use of models for deposition and etch processes. These processes are modeled by defining a machine and invoking the machine to perform either deposit or etch. For all models except Monte Carlo Deposition and Monte Carlo Etching, ELITE uses a string algorithm to describe topographical changes that occur during deposition and etching processes. This section describes the models and techniques used in ELITE to model the topography resulting from deep silicon etching process.

Jewett *et al.* were among the pioneers who attempted to model the surface advancement by string algorithm [99, 100] wherein the surface is approximated by a series

of points joined by straight line segments forming a string. String algorithm approximates the etched surfaces as a string of joined set of points formed in response to a particular process condition. During the simulation, the segments joining adjacent points are kept roughly equal in length by adding points in regions of expansion of the front, and by deleting points in regions of contraction. Elite links the string to simulation grinds such that during etching the simulation cuts into the grid patterns as the etch advances. Elite also applies special re-gridding algorithm to the area under the etched surfaces as the etching progresses.

For the string algorithm in ELITE to be useful, the pattern to be etched needs to be uniform in one dimension, so that the problem can be solved using only two dimensions. For most microfabrication problems, the important cases involve the cross-sections of lines, so this model is directly applicable. In TSV application, the vias are always circular in shape; hence the symmetry of cross-sections is such that the algorithm is still valid. Another assumption is that the etch rate is a scalar function of position, and is independent of the direction of local etch front motion and the history of the front. In some real situations, this assumption is not valid. Another case where this assumption does not hold is in the so-called “preferential etching” where the etching proceeds more quickly along certain crystal directions, making the etch anisotropic. During each time increment, each point advances perpendicularly to the local etch front as in Fig. 3.1. The algorithms in ELITE attempt to maintain approximately equal segment lengths. This results in position errors of about one-half the segment length. The error can be reduced by decreasing the average segment length. For most cases of interest, the etch rate varies with position. This leads to some errors in the position and in the direction of each point on the string.

3.2.4 Grid definition

The segments in the string algorithm are approximated by specifying rectangular grids. The grid pattern that defines the surface is known as mesh. The correct specification of a grid is critical in process simulation. The number of nodes in the grid N_p has a direct influence on simulation accuracy and time. A finer grid should exist in those areas of the simulation structure where we would like greater accuracy as explained in Fig. 3.2.

Figure 3.1: String Model approximation to model the Etch Front [101]

The number of arithmetic operations necessary to achieve a solution for processes simulated, using the finite element analysis method could be estimated as $(N_p)^\alpha$, where α is of the order 1.5 - 2.0. Therefore, to maintain the simulation time within reasonable bounds, the fine grid should not be allowed to spill over into unnecessary regions. The maximum number of grid nodes is 20,000 for ATHENA simulations, but most practical simulations use far fewer nodes than this limit. The grid in ATHENA consists of points connected to form a number of triangles. Each point has one or more nodes associated with it. A point within a material region has one node, while a point which belongs to several regions has several nodes. A node represents the solution in a particular material region at the point.

Figure 3.2: Material cross section defined by initial triangular grid pattern [101]

3.2.5 Etch models

3.2.5.1 Isotropic Etch Model

ELITE provides a set of basic etch models corresponding to different etch mechanisms. Any one of these models can be selected to define a machine that can then be invoked to perform processing on the structure. There are two isotropic etch models in ELITE. WET.ETCH parameter in the RATE.ETCH statement specifies isotropic wet chemical etch. In wet etching the reactive precursors chemically react with the exposed surface in all directions. No physical or directional reactions take place. Due to the chemical reaction, isotropic profiles develop mask undercutting and semi-circular cross-sections. Another isotropic etch model is invoked by using parameter RIE in the RATE.ETCH statement. It may be noted that in RIE mode the isotropic etch is coupled

with physical etch. Hence, to achieve purely chemical etch the physical etch parameters should be set to zero. Figure 3.3 shows the effects of lateral etch due to Wet etch and RIE etch.

3.2.5.2 RIE Model

In the RIE model, the etching process consists of both isotropic and physical etch. The RIE etch model built in the RATE.ETCH statement defined by the RIE parameters- *isotropic, directional, chemical and divergence*. Hence, we can model ion milling (physical etching), isotropic etching (chemical etching) and beam divergence model which emulates the effect of angular incidence of reactive ion flux. Therefore, the divergence parameter can be specified only if a non-zero value of chemical etch rate is specified as the divergence of beam always results in some degree of lateral etch. Figure 3.3 shows the effects of isotropic and RIE models. The next section describes the various statements in greater detail.

Figure 3.3: Tony plot of isotropic etch and RIE etch. Figure 3.3(a) shows pure isotropic chemical etch while 3.3(b) shows results due to RIE model which shows the effects of chemical, physical and beam divergence.

3.2.6 Etch Statements

This section describes some of the critical statements. Detailed descriptions of all the statements can be found in Athena User's Manual [94]. Figure 3.4 shows a simulation example which demonstrates the usage of statements. The ETCH statement describes an etch process. Two types of etch simulation methods are possible. The first is geometrical etching (defined by the user) and the second is physical etching which is defined by the statement RATE.ETCH. The material to be etched is specified by the statement MATERIAL X. If a material X is specified, only that material is etched even if other materials lie within the etch region. If no material is specified, all materials in the etch region are removed. The material can be photoresist, silicon, silicon dioxide etc. It is also necessary to specify etch machine with statement MACHINE=Y. MACHINE specifies the machine name for the RATE.ETCH statement. MATERIAL specifies material for which parameters of the etch machine are to be applied. WET.ETCH and RIE specify a particular model for the machine definition. DIRECTIONAL specifies the directional component of the etching rate used by the RIE model. The ionic etch rate is the contribution of the ions in the RIE etching mechanisms. The ions are assumed to have an anisotropic angular distribution specified by divergence parameter. ISOTROPIC specifies the isotropic etch rate used by the WET.ETCH and RIE models. The isotropic etch rate is the contribution of thermal atoms, radicals, and molecules coming out of the plasma. These are assumed to have an isotropic angular distribution. Therefore, the isotropic etching may lead to an undercutting of the mask. CHEMICAL is the etch rate in the RIE model normal to the ion beam when the DIVERGENCE is specified as non-zero. DIVERGENCE specifies the

beam divergence used by the RIE model. The angular distribution of the ions coming down to the wafer is Gaussian. An example of a simulation program to achieve tapered silicon etch profile by a RIE process is shown in Fig. 3.4. Table 3.1 shows some additional statements whose explanation is given in Table-3.1. These are the minimum number of statements needed to perform simulation in Athena Elite.

```
go athena
# X-Y Grid definition
line x loc=0.00 spac=10.00
line x loc=10 spac=1.0
line x loc=20 spac=1.0
line x loc=30 spac=0.50
line x loc=50 spac=0.50
line x loc=60 spac=1.0
line x loc=70 spac=1.0
line x loc=80 spac=1.0
line y loc=0.00 spac=0.50
line y loc=50 spac=0.50
line y loc=300.0 spac=2.0
# Define substrate
initialize silicon orientation=100
# Photoresist mask patterning
deposit material=photoresist thick=13.0 divis=13
etch material=photoresist start x=30.0 y=-13
etch          cont x=30.0 y=0
etch          cont x=47.0 y=0
etch          done x=47.0 y=-13
structure outfile=step0.str
# DRIE etch process
rate.etch machine=STS-DRIE rie silicon u.m iso=0.36
dir=3.88 chemical=0.1 divergence=50
rate.etch machine=STS-DRIE rie material=photoresist
u.m iso=0.14 dir=0 chemical=0.1 divergence=100
etch machine=STS-DRIE time=50 minutes dx.mult=1
structure outfile=step10.str
# Print simulation results
tonyplot -st step*.str
quit
```

Simulated tapered etch profile

Experimental results of actual tapered etch profile

Figure 3.4: Simulation of tapered deep silicon etch process using the isotropic and RIE etch models. SEM micrograph shows the experimental result. It may be noted that the scale of x-axis is different from y-axis of the simulation result.

Table 3.1: Summary of important Athena Elite statements

Statements	Descriptions
Go Athena	GO ATHENA starts the simulation program
Line x	LINE specifies a mesh line during grid definition.
Line y	
Initialize	INITIALIZE specifies the initial starting material and background doping levels and crystal orientation
Deposit	DEPOSIT deposits a layer of specified material.
Etch	ETCH simulates an etch process.
Rate.etch	RATE.ETCH specifies the etch rate parameters for a machine, which is used in a subsequent ETCH statement
Structure Infile	STRUCTURE writes the mesh and solution information. INFILE specifies the name of the section file generated during simulation.
Structure Outfile	OUTFILE specifies the name of the file to be written.
Tonyplot	Tonyplot starts the graphical post-processor TONYPLOT.
Quit	QUIT terminates execution of ATHENA.

3.2.7 Summary

Elite is a topography simulation software which has the ability to model etch and deposition surface topographies based on process variables like isotropic etch rate, chemical etch rate, ion flux divergence and anisotropic etch rate as in an actual reactive ion etching process. ELITE uses string algorithm to describe topographical changes that occur during deposition and etching processes (unlike Monte Carlo method which uses atomistic etching and deposition models). Smooth and accurate surface topography can be modeled by appropriately meshing the surface to be etched. Suitable statements are used to input etch parameters, solve the etch process and finally output the post-processed results.

3.3 SIMULATION OF THERMO-MECHANICAL STRESSES IN TSV

3.3.1 Overview of ANSYS

ANSYS is engineering software which provides a wide range of mechanical and multi-physics simulation capabilities. The ANSYS Mechanical simulation products provide a full complement of nonlinear and linear elements, material laws ranging from metal to rubber. ANSYS Mechanical software can be used to study structural and thermo-mechanical stresses in semiconductor components, electronics packages and printed circuit boards. Mechanical solutions also offer coupled physics analysis capabilities to simulate wide range of physics phenomena including thermal-stress and electro-mechanical analysis for MEMS. ANSYS Mechanical software incorporates pre-processing (geometry creation, meshing), solver and post-processing modules. It also has general-purpose finite element modeling packages for numerically solving mechanical problems. ANSYS uses the finite-element method to solve the underlying governing equations and the associated problem-specific boundary conditions

3.3.2 Finite Element Analysis (FEA)

The finite element analysis is basically a numerical technique used for finding approximate solutions of partial differential equations and integral equations. FEA consists of various models of materials that is stressed and analyzed for specific results. In each modeling schemes, the programmer can insert numerous algorithms (functions) which may make the system behave linearly or non-linearly. The computation time depends on the complexity of the problem and the size and number of the mesh. FEA requires the structures to be analyzed to be defined by points called nodes which make a grid called a mesh (See Fig. 3.5) [102]. This mesh is then programmed to contain the material and

structural properties which define how the structure will react to certain loading conditions. Nodes are assigned at a certain density throughout the material depending on the anticipated stress levels of a particular area. Regions which will receive large amounts of stress usually have a higher node density than those which experience little or no stress. Points of interest may consist of: fracture point of material, fillets, corners, complex detail, and high stress areas. The mesh is like a spider web made from nodes. The following are some examples of the loading conditions that can be applied to a problem:

- Point, pressure, thermal, gravity, and centrifugal static loads
- Thermal loads from solution of heat transfer analysis
- Enforced displacements
- Stress of materials

Each FEA program also comes with an element library such as, for example:

- Rod/beam elements
- Plate/Shell/Composite elements
- Shear panel
- Rigid elements

Figure 3.5: 2D mesh showing higher density at the area of interest. Relaxing density in non-critical areas will reduce computation time in simulation [102].

3.3.3 Thermo-mechanical stress analysis in TSV

3.3.3.1 Problem definition: This section describes various critical steps followed to solve for thermo-mechanical stress in a TSV and blind-via structure filled with solid copper. Each TSV structure is made of circular and square vias of $5\mu\text{m}$ width/diameter and $5\mu\text{m}$ depth. It is the intention to identify the critical locations where mechanical stresses are concentrated due to thermal loading on the structure. It is also intended to compare the stress pattern in a through silicon and blind-via structure. Figure 3.6 describes the details of the simulation.

Figure 3.6: Cross-section illustration of a through silicon and blind via structure used for evaluating the thermo-mechanical stress pattern in the structure.

3.3.3.2 Start-up and preliminary set-up: A step by step guide to usage of ANSYS has been provided with several examples in this reference [103]. The first step is to create a folder at a convenient location to store files created during the session.

3.3.3.3 Specify element type and constants: In this step the geometry of the structure to be modeled is created. The object is specified with appropriate displacement constraints, load and mesh parameters.

3.3.3.4 Specify material properties: In the Material Models Available Frame of the Define Material Model Behavior window, double-click on Structural, Linear, Elastic, and Isotropic. Enter the Young's Modulus and Poisson's Ratio. Tables 3.2 to 3.5 show all the model parameters used.

Table 3.2: Mechanical properties of copper (Cu).

Plastic Model	Copper
CTE (-40~125°C) (ppm/K)	16.12
Young's Modulus (GPa)	127.4
Poisson's Ratio	0.36
Yield strength (MPa)	262
Hardening coefficient (MPa)	315
Hardening exponent	0.54

Table 3.3: Mechanical properties of silicon (Si) and silicon dioxide (SiO₂).

Linear elastic Model	Silicon	SiO ₂
CTE (-40~125°C) (ppm/K)	2.6	0.94
Young's Modulus (GPa)	130.91	70
Poisson's Ratio	0.28	0.17

Table 3.4: Mechanical properties of Silicon nitride (Si₃N₄).

Linear elastic Model	Si ₃ N ₄
CTE (-40~125°C) (ppm/K)	2.8
Young's Modulus (GPa)	~220
Poisson's Ratio	0.26
Yield strength (MPa)	-
Ultimate strength (MPa)	~172

Table 3.5: Mechanical properties of tantalum (Ta).

Linear elastic Model	Ta
CTE (-40~125°C) (ppm/K)	6.5
Young's Modulus (GPa)	186
Poisson's Ratio	0.35
Yield strength (MPa)	170
Ultimate strength (MPa)	450

3.3.3.5 Specify geometry of the structure and the mesh geometry: In this step, the structure geometry and the meshing parameters are defined. Next, we define the boundary conditions, namely, the displacement constraints and loads. Note that in ANSYS terminology, the displacement constraints are also "loads". We can apply the loads either to the geometry model or to the finite-element model (that is to the elements and nodes directly).

3.3.3.6 Solve: This solves the current loading conditions. The information entered is reviewed in the */STAT Command window*. This is a summary of the problem that ANSYS is about to solve.

3.3.3.7 Post-process the results: Post-processing is the step where we look at and analyze the results obtained from the ANSYS solution. This plots the thermo-mechanical stress pattern in the TSV structure in the *Graphics* window. The results obtained from FEA analysis depend on the mesh. An important step in the analysis is to make sure that the mesh resolution is adequate for the desired level of accuracy. This is done by refining the mesh and comparing results obtained with different levels of mesh resolution. As a final step, the results obtained should be compared with appropriate theoretical results whenever possible. Wherever possible, an experimental study should be done to verify the results and confirm the assumptions made are correct.

Table 3.6: Stresses in TSV structure with TSV diameter/depth/width of 5 μ m

Location of stress	Through-silicon via	Square via	Blind-via
Stress on SiO ₂ (MPa)	194.1	219.8	233.7
Stress on copper (MPa)	248.6	273.4	274.7

Table 3.7: Stresses in TSV structure with via diameter of 50 μ m

Via depth (μ m)	50	100	150
Stress on SiO ₂ (MPa)	244.2	253.7	305.7
Stress on copper (MPa)	235.1	260.9	263.0

Table 3.8: Stresses in TSV structure with via depth of 100 μ m

Via diameter (μ m)	50	70	100	150
Stress on SiO ₂ (MPa)	253.7	355.7	353.8	375.5
Stress on copper (MPa)	260.9	264.0	262.8	261.7

Chapter 3 – Topography modeling and thermo-mechanical simulation for TSV characterization

Figure 3.7: Thermo-mechanical stress distribution map in a TSV structure that was modeled under a thermal load.

The simulation results shown in Fig. 3.7 are easy to interpret based on color code shown at the bottom of each stress map. It may be seen that the red color indicates highest stress point. It is evident from summary Table-3.6-3.8 that the stress level in a dielectric is much higher than in copper in a TSV structure. This information is vital in selecting appropriate dielectric materials to cushion the stress acting on the dielectric layer due to high CTE difference between copper in TSV and the dielectric material. Paralyne is one such dielectric material which has been proposed which can buffer the large stress from being transferred to silicon [104]. It can also be seen that the stress level increases with increase in depth and diameter of TSV. Another significant observation from the simulation is that the centre of the vias are less stressed than the edges of the via that is in

contact with dielectric with which there is a significant difference in CTE (refer to Table-3.2 and 3.3). It has been shown that in certain 3D IC schemes where dielectric glue is used to bond thin wafers with TSVs, the high copper stress in ends of TSV causes delamination in bonding dielectric films at the ends of the TSVs [105].

3.3.4 Summary

An overview of ANSYS FEA software and its key features were described for performing thermo-mechanical stress simulation in TSV structures. An example of simulation was presented to evaluate the stress distribution in a TSV due to thermal load as seen in a real fabrication process condition. The stress distribution across the TSV for vias of various geometries were reviewed which provide valuable insight into potential failure points.

3.4 CONCLUSION

This chapter introduced some of the important simulation techniques used in evaluating and characterizing through silicon via technology. Athena Elite of Silvaco and ANSYS simulation tools were presented with suitable simulation examples to demonstrate the usefulness of these tools. The rest of the thesis will focus on applications of these simulation tools in developing and characterizing the through silicon via etch technology for 3D Microsystems application.

Chapter 4

Study of thermo-mechanical stresses and its impact on through silicon vias

4.1 INTRODUCTION

There exists a wide diversity of 3-D integration techniques in the literature [106, 107], but the most appealing and competitive schemes are those that can be implemented without disrupting the front-end processed device wafers. Typically, they involve aligning and stacking 2 or more functional wafers by low-temperature wafer bonding techniques. The devices in each substrate are interconnected by through-wafer interconnections, also known as through-silicon vias, which are either formed before or after stacking the wafers.

Figure 4.1: Face to face bonded CMOS device wafer stack with TSV interconnection.

Figure 4.2: Face to face bonded MEMS and CMOS device wafers bonded and interconnected with TSV connections.

Figure 4.1 illustrates one possible approach in which the wafers can be stacked by Cu-Cu thermo-compression bonding with device sides facing each other [108, 109]. Figure 4.2 illustrates another possible approach in which a cap wafer is bonded to a micro electromechanical system (MEMS) wafer wherein TSV interconnections are provided through the cap wafer [110].

Although different schemes vary significantly in their process flow, most 3D microsystems share some common features: (a) The bonding material of choice (metal or dielectric glue), (b) a method for Si substrate thinning, (c) the wafer-to-wafer alignment scheme, and (d) through silicon via (TSV) fabrication methodology. The objective of this work is to study extensively the silicon via etch process-induced failure mechanisms as it is one of the critical enabling process for 3D microsystems fabrication. Silicon vias can be fabricated by laser drilling [111] or by various DRIE methods. The present work focuses extensively on one of the most widely used DRIE processes known as the Bosch etch

process [112] and studies its impact on the electrical performance for through-silicon interconnection application. It is also the objective of this work to perform Finite Element Analysis (FEA) modeling and study the effect of thermo-mechanical stress on the TSV and its performance.

4.2. EXPERIMENTAL STUDY

4.2.1 Motivation for thermo-mechanical study of TSV

The main motivation for doing thermo-mechanical simulation is to study the impact of thermal load on through silicon interconnect structure. It is further intended to identify potential failure sites in the through silicon interconnect structures and use it in explaining some of the failure mechanisms during electrical characterization. The coefficient of thermal expansion (CTE) of copper (~ 17.5 ppm / $^{\circ}\text{C}$) is 7 times higher than that of silicon (~ 2.5 ppm/ $^{\circ}\text{C}$). Thus, when the copper TSV is subjected to a thermal load, a large local stress is induced between the copper and silicon/dielectric (e.g., SiO_2), which will create TSV interconnection reliability issue [113]. Stress-induced metal voiding and dielectric cracking due to thermo-mechanical stresses has already been reported earlier in multi-level aluminum interconnect structures [114, 115]. Thermal stress characteristics of damascene copper interconnect passivated with low-k/silicon dioxide and protected by tantalum diffusion barrier has also been widely investigated by FEA [116]. Suo has classified various 2D Semiconductor interconnect failures and its failure mechanisms [117]. These studies show that narrow encapsulated aluminum and copper interconnects can easily develop stress-induced voids or cracks when the magnitude of the stress exceeds the yield strength of the metal.

Figure 4.3: 3D view and cross-sectional view of a through silicon interconnect structure used to study the stress distribution on the sidewalls in a Bosch and non-Bosch etched TSV structure.

With the emergence of TSV as an alternate interconnection solution for resolving interconnect bottleneck, a lot of work is being done to study the impact of process-induced thermal loading on through silicon interconnects. Cu-filled TSV has been studied with different via geometries and it has been shown that post-process temperature induces highest values of stress in the silicon adjacent to the TSV due to a very high radial force after filling of the TSV [118, 119]. Cheryl *et al.* in their study on solid and hollow Cu-TSV structures have shown that due to large CTE mismatch between copper and dielectric isolation layer, a lot of radial and axial stress is received by the dielectric material which can potentially impact its performance as an insulator [113]. In most of these FEA studies, the effect of thermo-mechanical stresses on thin barrier and dielectric layer has been ignored as the focus mostly has been on the effect of the CTE mismatch on copper interconnect or on thin silicon substrates due to radial stress acting upon it due to copper

TSV and/or bonding glue used to stack-up chips [119, 120]. In the present study, the effect of TSV shape and their geometry has been evaluated. The effect of thermal load on thin barrier and dielectric layers have also been studied in this work. Further, the effect of the sidewall scallops on the barrier and dielectric isolation layer is also investigated. Figure 4.3 shows an illustration of the TSV structure under study. It is finally intended to study the impact of the corrugated or scalloped sidewalls on the TSV electrical leakage performance under electrical stress.

4.2.2 Thermo-mechanical simulation study using Finite element analysis (FEA)

The following assumptions are made in FEA using ANSYS software:

- The 3D FEA models only considers one quarter of the via structure due to symmetry. Via diameter and depth are both set at 5 μm .
- The thickness of SiO_2 is set at 1.0 μm and tantalum barrier thickness is set as 50 nm.
- 8 node solid elements are employed. All materials are considered as linear elastic and isotropic except copper. An inelastic rate dependant multi-linear isotropic Mises model is used for copper [113].
- For relative comparison purposes, boundary conditions, element type, smart mesh size, and evaluation index are fixed in view of the singularity effect.
- Since the electroplating is conducted at room temperature, the stress in the physical structure is assumed to be free at 25°C. All the material properties are listed in Tables 4.1 and 4.2 [121].
- Thermal loading: - 40 to 125°C.

Table 4.1: Material properties @ 25 °C [121].

Linear elastic Model	Silicon	SiO₂	Si₃N₄	Ti	Ta
CTE (-40~125°C) (ppm/K)	2.6	0.94	2.8	8-10	6.5
Young's Modulus (GPa)	130.91	70	~220	116	186
Poisson's Ratio	0.28	0.17	0.26	0.34	0.35
Yield strength (MPa)	120			140	170
Ultimate strength (MPa)			~172	220	450

Table 4.2: Plastic model for copper.

Plastic Model	Values
CTE (-40~125°C) (ppm/K)	16.12
Young's Modulus (GPa)	127.4
Poisson's Ratio	0.36
Yield strength (MPa)	262
Hardening coefficient (MPa)	315
Hardening exponent	0.54

Table 4.3: Summary of stresses on SiO₂ and Cu for a 100 µm deep TSV with variation in diameter from 50-150 µm.

Variation of diameter of 100µm deep vias	50 µm	100 µm	150 µm
Stress on SiO ₂ in the ends of TSV (MPa)	253.7	353.8	375.5
Stress on copper in the ends of TSV (MPa)	260.9	262.8	261.7

Table 4.4: Summary of stresses on SiO₂ and Cu for 50 µm diameter vias with variation in depth from 50 to 150 µm.

Variation of depth of 50µm diameter vias	50 µm	100 µm	150 µm
Stress on SiO ₂ (MPa) in the ends of TSV	244.2	254	305.7
Stress on copper (MPa) in the ends of TSV	235.1	260.9	263.0

Table 4.5: Summary of stresses in SiO₂ and Cu due difference in sidewall condition due to Bosch (rough sidewall) and non-Bosch etch process (smooth sidewall).

Surface condition on TSV sidewall	Thermo-mechanical stress in TSV without Ta barrier (MPa)		
	Silicon (Si)	Silicon dioxide (SiO₂)	Copper (Cu)
Smooth surface	46.1	165	193
Rough surface	76.9	243	297

Table 4.6: Summary of stresses in tantalum barrier, SiO₂ and Cu due difference in sidewall condition due to Bosch (rough sidewall) and non-Bosch etch process (smooth sidewall).

Sidewall condition	Thermo-mechanical stress in TSV with Ta barrier added (MPa)							
	Silicon (Si)		Silicon dioxide (SiO ₂)		Copper (Cu)		Tantalum (Ta)	
	Middle	Top	Middle	Top	Middle	Top	Middle	Top
Smooth	48	64	100	149	115	168	126	161
Rough	56	100	166	360	100	297	160	269

Figure 4.4: (a) Simulated stress pattern on SiO₂ isolation layer: (b) Stress on copper sidewall due to thermal cycling on through-wafer copper interconnect structure.(c) Stress pattern on copper at both ends of the copper vias and (d) Stress on the tantalum barrier due to copper stress on both ends of the via.

Stress-induced copper interconnect and dielectric cracking are potential failures in high density copper technology due to CTE mismatch between the copper metallization inside the via structure and the copper diffusion barrier (Ta or Si₃N₄) and the dielectric material (SiO₂) surrounding the copper. This mismatch generates thermal stresses when the

structure is subjected to thermal loads [122]. The simulation results are later utilized to correlate with the electrical leakage characteristics of TSV structures under thermal load. Thermal loading of -40° to 125°C has been chosen in this study as it is commonly used to study the reliability of interconnect structures. The temperature range also represents both the extreme environment temperatures and also the operating temperatures during the normal operation of electronic devices [117, 123].

Figure 4.5: Thermo-mechanical stresses in TSV and silicon interface due to rough sidewalls due to Bosch etch process. It can be seen that the stress concentration is high in the sharp peaks and valleys of the scallops and decreases from top and bottom towards the middle of the TSV.

FEA is done for different depths and diameters of the TSV structures of interest, which is tabulated in Tables 4.3 and 4.4. It is seen from the simulation results that the radial and axial stress in general increase with via diameter and with increasing depth. Figure 4.4 shows the stress patterns emerging due to a 5 μm diameter TSV with a depth of 5 μm . Tables 4.5 and 4.6 summarize the results of a study done with TSV with rough sidewalls due to Bosch process as compared with an ideal smooth or straight side walled TSV structure. Figures 4.5 and 4.6 show the stress pattern in silicon and silicon dioxide region in the TSV structure.

Figure 4.6: Thermo-mechanical stresses in TSV and silicon interface is shown due to smooth sidewalls formed by a non-Bosch etch process. It can be seen that the stress is high in top and bottom which gradually decreases towards the middle of TSV.

Some significant observations from the simulation studies are summarized as follows:

- At the top and bottom of the via fabricated by the Bosch process, the stress on copper interfacing the Ta barrier is about 297 MPa while in the middle of the via, the stress on the copper interface is about 100 MPa.
- For the smooth surface, the stress on the top and bottom of the TSV structure is about 168 MPa while the stress on the middle is about 115 MPa. In both cases, the interconnect diameter is 5 μm and the depth of the via is also 5 μm .
- 2D model with symmetry boundary condition was used. The element type is PLANE82. Smartmesh is used and the size level is 5. The material property of the silicon and silicon dioxide is linear (Elastic) while the copper material model is plastic. The barrier layer is ignored because it is so thin that it will have little effect on the other layers.
- After the Bosch etch process, the stress on SiO_2 in the middle is 166 MPa and at the top and bottom is around 360 MPa. For the smooth sidewall, the stress in SiO_2 in the middle is 107 MPa and at the top and bottom it is around 149 MPa.
- After adding a barrier layer in the model (50 nm Ta), the stresses on copper and silicon are similar as in case with no barrier layer. However the stress on SiO_2 reduces (Max: 169 MPa) because the CTE of Ta is about 6.5 ppm/ $^{\circ}\text{C}$, copper, 16 ppm/K, and USG 0.94 ppm/ $^{\circ}\text{C}$.
- The stress on Ta at the top and bottom is 269 MPa while in the middle it is 160 MPa.

The main motivation of this stress simulation study is to show the relative stress distribution in the Ta-barrier and dielectric layer (SiO_2) in the TSV structure with open space on both sides. A study of embedded TSV structure with dielectric and redistribution

metallization with actual thermal excursion as in a packaging process can be found in another related work [32,199]. However, in both open space and embedded TSV stress simulation studies, the high stress points still remain the same. In the following section (Section 4.3) the thermo-mechanical stresses are correlated with the electrical test results achieved and some of the failures are explained.

4.2.3. Test vehicle design

Figures 4.1 and 4.2 shows some typical implementations of through-silicon interconnection structures in a vertically stacked 3D microsystems package. In Section 4.2.2, the stress distribution on the rough and smooth sidewalls of a TSV structure has been studied by FEA. In this section, it is our objective to design a test vehicle to study the effects of sidewall roughness created by the deep silicon via-etch process on the electrical performance of the through-wafer copper interconnections. The main motivation of this study is to show the impact of sidewall roughness due to silicon via etch process on the electrical leakage behavior of TSV structure. As comb structures are commonly chosen for TDDB and dielectric leakage studies [128], it was decided to use similar structure for evaluating the sidewall roughness due to silicon via etch process. Though circular vias are commonly used for TSV applications due to minimum thermal stress in the TSV structure, there are few publications that have shown the usage of rectangular trenches as TSV structure [198]. The test vehicle therefore is a comb structure designed as shown in Fig. 4.7 and Table 4.7, to measure the current leakage between adjacent rectangular blind vias under various electrical and thermal stresses.

Figure 4.7: Top view and cross-section view of test structure to evaluate the performance of through-wafer interconnection.

The test device consists of four pairs of parallel trench structures with different trench widths and separations. These trench structures represent deep silicon vias with different via diameters and pitch. The comb structure shown is formed by two metal masking steps: a trench metal mask and via metal mask. The via width is varied from 5 to 50 µm to study the effects of copper stress on the silicon dioxide dielectric and tantalum barrier. It is also our intent here to study the impact of silicon via etching process on the electrical performance when various diffusion barrier schemes are used. Table 4.8 shows the process flow to fabricate the test vehicle.

Table 4.8: Process flow for test vehicle fabrication.

Step #	Process description
1	3 μm plasma enhanced chemical vapor deposition (PECVD) SiO_2
2	1 μm damascene copper interconnection trench masking and etch process
3	Deep silicon copper via masking and etch process
4	500 nm TEOS based Silicon dioxide (SiO_2) liner deposition
5	Cu-diffusion barrier + 150 nm Cu seed sputtering (Barrier films/thickness varied as per different experimental conditions shown in Table 4.5)
6	Copper electroplating
7	Copper <u>annealing</u> at 200 $^{\circ}\text{C}$ and Chemical Mechanical Polishing (CMP)
8	100 nm Si_3N_4 /300 nm SiO_2 Passivation (400 $^{\circ}\text{C}$)
9	Pad window patterning and aluminum deposition
10	Aluminum Pad masking and etching
11	Annealing (400 $^{\circ}\text{C}$)
12	Electrical measurements

4.2.4 Development of Bosch etch process with minimum sidewall roughness

The deep silicon etch was carried out using the standard Bosch process in Multiplexed inductively coupled plasma (ICP) etching system from Surface Technology Systems (STS). The main gas precursors are sulfur hexafluoride (SF_6) and oxygen (O_2) for the etch cycle and octofluorocyclobutane (C_4F_8) for the sidewall passivation cycle, which are repeated alternately until the required trench depth is achieved. Due to a strong isotropic nature of SF_6 / O_2 etch chemistry, each etch cycle results in a sidewall recess called scallop. As a consequence of the Bosch etch process, the scallops cause the dielectric deposition, tantalum and copper seed metallization to be non-uniform. Further, due to the directional nature of ion-assisted process like plasma enhanced chemical vapor

deposition (PECVD) and physical vapor deposition (PVD), the film thickness uniformity is strongly influenced by the depth, sidewall profile and aspect ratio [124].

In the plasma, SF_6 , among other things, dissociates into atomic fluorine and heavy SF_5^+ ions as follows:

Usually, 10% O_2 is added to help in liberating more fluorine radicals in the plasma reaction between SF_6 and O_2 . Silicon is then subsequently etched by the fluorine according to the reaction

During the passivation phase of the Bosch process, CF_2 is formed from C_4F_8 as follows:

The CF_2 then adsorbs on the surfaces and forms a Teflon-like polymer according to the reaction

During the etch phase, the CF_2 molecules are removed by a combination of physical ion sputtering and chemical reactions. The physical component in the Bosch process is contributed by positively charged S_xF_y^+ and the chemical etch is mainly due to F and O_2 , which are generated from the etch step. The scallops are due to isotropic etching mechanism as indicated in Eqn. (4.2). In the case of the non-Bosch etch process, the etch and passivation reactions take place simultaneously. A standard Bosch etch process with a fixed pressure and platen power and an improved version with parameter ramping feature [125] is summarized in Table 4.9. Figure 4.8 shows the SEM cross-sectional micrograph of the test structure with the improved etch recipe. Figure 4.9 shows SEM micrograph after

the copper electroplating process which shows that void-free copper via-filling has been achieved. It can also be seen that the sidewall scallop size decreases with depth of the via. Figure 4.10 shows the process data log plot of the process pressure and platen power in a standard Bosch etch process which uses a static pressure and platen power setting. After a few minutes of pressure rise, it stabilizes to a fixed value as per recipe settings shown in Table 4.9. The pressure and power oscillates due to switching between etch and passivation cycle in the Bosch process. The envelope seen above due to peak pressure and power shows the steady-state trend during etch process. Figure 4.11 shows a similar plot of the modified Bosch etch process with a gradual decrease in the pressure and gradual increase in the platen power. It can be seen that in both the standard and improved etch process, it takes a few minutes in the beginning of the process for pressure and power to stabilize and follows the ramp rate as per recipe Table 4.9. These trends can be due to initial lag in the silicon etch. Once the silicon etch begins, the pressure starts to rise and then stabilizes to a steady-state value as shown in both the plots. Recipe A shown in Table 4.9 shows an improvement over the standard Bosch recipe due to a gradual reduction in the pressure and gradual increase in the platen power which reduce ion scattering and thus scallops.

Chapter 4 - Study of thermo-mechanical stresses and its impact on through silicon vias

Figure 4.8: SEM images showing edge roughness gradually decreases from 200-100nm.

Figure 4.9: FIB SEM image of 6 μm deep silicon vias after copper electroplating.

Figure 4.10: Process data log plot of process pressure and platen power in a standard Bosch etch process which uses a static pressure and platen power setting.

Figure 4.11: Plot showing the dynamic ramping of pressure and platen power in the optimized Bosch etch process. It typically takes few minutes for pressure and power to stabilize and follows the ramp rate as per recipe Table 4.9.

Table 4.9: Bosch and non-Bosch etch process conditions used in this study.

Standard Bosch etch process:	Etch cycle: 25 <i>mTorr</i> ; SF ₆ : 100 <i>sccm</i> ; O ₂ : 10 <i>sccm</i> ; Coil Power: 600 W; Platen power: 13 W; 7.5 <i>sec</i> .
	Passivation cycle: 15 <i>mTorr</i> ; C ₄ F ₈ : 170 <i>sccm</i> ; Coil Power: 600 W; 5 <i>sec</i> .
	Platen Temperature: 10 °C
	Total process time: As per depth; Etch rate: 1-1.2 $\mu\text{m}/\text{min}$
Parameter ramped Bosch etch process (A):	Etch cycle: 25 <i>mTorr</i> with ramp rate = -0.1 <i>mtorr/min</i> ; 130 <i>sccm</i> SF ₆ ; 13 <i>sccm</i> O ₂ ; 600 W Coil power; 20 W Platen power with ramp rate = +0.1 <i>W/min</i> ; 5 <i>seconds</i>
	Passivation cycle: C ₄ F ₈ : 85 <i>sccm</i> ; 600 W Coil power; 5 <i>seconds</i> .
	Platen Temperature: 10 °C
	Total process time: As per depth; Etch rate: 2-2.5 $\mu\text{m}/\text{min}$
Non-Bosch etch process (B)	SF ₆ : 40 <i>sccm</i> ; C ₄ F ₈ : 90 <i>sccm</i> ; Coil Power: 800 W; Platen power: 20 W; Pressure: 12-12.3 <i>mtorr</i> @ 45% APC; Platen temperature: 10 °C; Etch rate: ~ 0.2-0.3 $\mu\text{m}/\text{min}$.

4.2.5 Test vehicle fabrication

As the standard non-Bosch RIE process was able to give a smooth sidewall profile, the recipe was not further optimized. The test vehicle as described in Fig. 4.7 is fabricated using the process flow shown in Table 4.8. Nine experimental wafers were fabricated with different process conditions to evaluate the impact of sidewall roughness and different copper barrier films. The experimental runs were designed to evaluate the effect of the sidewall roughness on the interconnect performance. It is also intended to study the effect of different barrier schemes in lowering the impact of sidewall roughness. As the dielectric and barrier layers were deposited by plasma processes, the uniformity of the sidewall deposition is crucial for achieving good performance for the deep-silicon copper interconnection [126]. Table 4.10 summarizes various experimental variations done to the copper diffusion barrier films. Thicker or double barrier stacks are expected to prevent any electrical leakage due to thinning down of barrier films due to sidewall scallops formed by the Bosch etch process. However, varying the barrier thickness will have its consequences which are summarized in last column of Table 4.10. All the thin films used in the test vehicle fabrication process were first characterized on test wafer before fabricating the test vehicle. Table A-1 summarizes the test wafer results. It can be seen that the maximum thickness non-uniformity is seen for tantalum (Ta) deposition process. Best uniformity is seen for TEOS oxide deposition process. Like-wise, copper CMP process was characterized for planarity and dishing on TSV wafers with vias of 5 μ m diameter. The surface planarity was measured by using a stylus profiler. The value of dishing measured on 2 wafers at 5 sites across the wafer is summarized in Table A-2. Figure A-1 shows the within wafer uniformity plot based on 5-sites measurement for the 2 wafers. It can be seen

that the average dishing is $\sim 363\text{nm}$ which is not expected to pose any problem in the TSV performance as the maximum dishing is about 10% of the dielectric thickness of $3\mu\text{m}$ on top of the silicon surface. After the test vehicle has been fabricated based on the process runs summarized in Table 4.10, the film thickness uniformity on sidewalls of the $5\mu\text{m}$ and $35\mu\text{m}$ test structures were studied in SEM. Table A-3 and A-4 summarizes the thickness of TEOS oxide, barrier layer and sidewall roughness measured at top middle and bottom region of the TSV trench structures.

Cross-sectional and 45° tilt-view SEM micrographs were taken from wafers etched with the Bosch etch process (See Fig. 4.12(a)), non-Bosch etch process or ICP-RIE process (See Fig. 4.12(b)) and a hybrid process which combines a non-Bosch (B) and a Bosch etch process (See Fig. 4.12(c)). In the next section the experimental results are discussed extensively for each process run. Further, the impact of the film thickness variations within wafer and within the TSV structures is discussed in the next section.

Table 4.10: Summary of significant observation for various process conditions evaluated.

Run#	Etch process	Isolation dielectric thickness used	Cu-barrier evaluated	Via depth	Observation after CMP
1	Bosch (A)	500 nm TEOS oxide	25 nm Ta	$100\mu\text{m}$	OK
2	Bosch (A)	500 nm TEOS oxide	25 nm Ta	$10\mu\text{m}$	OK
3	Bosch (A)	500 nm TEOS oxide	100 nm SiN +25 nm Ta	$10\mu\text{m}$	Cu Peeling
4	Non-Bosch (B)	500 nm TEOS oxide	100 nm SiN +25 nm Ta	$10\mu\text{m}$	Cu Peeling
5	Non-Bosch (B)	500 nm TEOS oxide	25 nm Ta	$10\mu\text{m}$	OK
6	Non-Bosch (B)	500 nm TEOS oxide	100 nm Ta	$10\mu\text{m}$	OK
7	Bosch (A)	500 nm TEOS oxide	100 nm Ta	$10\mu\text{m}$	OK
8	Bosch (A)	500 nm TEOS oxide	100 nm SiN +100 nm Ta	$30\mu\text{m}$	Cu Peeling
9	Non-Bosch (B)+Bosch (A)	500 nm TEOS oxide	100 nm Ta	$30\mu\text{m}$	Cu Peeling

Figure 4.12: (a) Tilt SEM micrograph of trenches formed by the Bosch process (A) with a sidewall roughness of $\sim 0.05 \mu\text{m}$. (b) Smooth trench profile formed by a non-Bosch etch process (B) with a sidewall roughness of $\sim 0.01 \mu\text{m}$. (c) Trenches formed by a hybrid etch process combination of a non-Bosch (B) and a Bosch etch process (A) .

4.2.6 Electrical test vehicle Characterization

The test vehicle with long comb structures (see Fig. 4.7) are specially designed to detect dielectric and barrier failures under high voltage stress from 0-100 V and thermal stress from 25-200 °C. Comb structure is being used due to its large surface area and its ability to magnify leakage currents due to surface defects inside the vias [127]. Leakage current between adjacent comb structures is used as a measure of the quality of dielectric isolation and copper-diffusion barrier when deposited over uneven or rough surfaces etched by different type of etch processes (See Table 4.10). Though the leakage mechanisms in low-k dielectric in copper damascene interconnect have been extensively studied [128-130], a study of similar nature for TSV interconnections have not been reported so far. The electrical leakage current measurements done on wafers belonging to run#1 to 9 is shown in Figs. 4.13 to 4.17 with the leakage current expressed in logarithmic scale. The full measurement database is appended in Appendix A for reference.

Figur-4.13: Comparison of leakage current in wafers etched by the Bosch process (A) with different barrier schemes.

Figure 4.14: Comparison of leakage current in wafers etched by the Bosch process (A) with different depths.

Figure 4.15: Comparison of leakage current in wafer etched by the non-Bosch process (B) with different barrier schemes.

Figure 4.16: Comparison of leakage current in wafer etched by Bosch (A), non-Bosch (B) and hybrid etch processes (B + A).

Figure 4.17: Leakage current trend for 5 μ m comb test structures with 100 μ m depth (Run#1) etched by Bosch process (A) when subjected to different thermal loading conditions during leakage test.

Figure 4.18: Copper peeling observed during chemical mechanical polishing (CMP) process at comb structures for wafers with thicker barriers due to high film stress.

4.3. RESULTS AND DISCUSSION

4.3.1 Effect of thermo-mechanical stress on TSV interconnect structures

Thermo-mechanical stress modeling data presented in Section 4.2.2 shows a clear trend between the applied thermal stress and mechanical stress created in the TSV structure. Tables 4.3 and 4.4 summarize the mechanical stress created in TSV of different diameters and depths. It can be seen that the stress in copper is much higher at the ends of the vias than in the middle. It can also be seen that the high stress in the copper is transferred to adjoining dielectric interface due to difference in CTE between Cu and SiO₂. Figure 4.4 shows the stress distribution in copper, SiO₂ and tantalum barrier film. It can be seen that the stress is highest in the 100 nm thick barrier film. The high stress in the dielectric and barrier layer makes them vulnerable to stress-induced cracking if the barrier becomes thinner due to sharp corners or abrupt steps in the TSV sidewalls.

It can be seen from Figs. 4.5 (a) and (d) that the SiO₂ layer and tantalum barrier layer experience much higher stress than the copper interconnect at both ends of the via structure. A summary of significant observations due to the simulation of various geometries of the TSV structures are also tabulated in Tables 4.6 and 4.7. It can be seen that the stress on the copper and dielectric layers grows with the via diameter and depth. The stress in copper seems to be grow to a lesser extent due to its ductile nature. The main reason for the stress buildup on the dielectric and barrier layer is due to a larger volume of copper and its high CTE with respect to SiO₂ and Ta (See Tables 4.1 and 4.2). The simulation results also show that when the TSV structure is subjected to a thermal load from -40 to 125 °C, a stress level of ~400 MPa and 172 MPa are produced in the Ta barrier

and SiO₂ of the TSV structure, respectively. It can also be seen from Steps 7, 8 and 11 of Table 4.8, that the TSV structure is also being subjected to higher thermal loading from 200 to 400 °C due to post-TSV processes which can cause much higher stress levels to build-up on Ta and SiO₂ films in the TSV structure which can potentially cause dielectric or barrier layer to crack at any weak site(s) on the sidewalls.

It may be noted from Table A-3 and A-4 that the thickness of barrier on the sidewalls of the trench is a function of sidewall roughness, depth and width of the trench. Though the variability of film thickness is slightly higher due to the sample preparation process, following key conclusions may still be made from the SEM cross section data:

- (a) The sidewall roughness decreases with depth for Bosch process
- (b) The barrier thickness decreases with depth of the trench
- (c) The barrier thickness is slightly thicker in the middle than at the bottom edge
- (d) The barrier/isolation thickness is thinner at the top edge of the TSV due to undercut below the hard mask and consequent shadowing effect (See Fig 4.19 and 4.20)
- (e) The Bosch process has higher sidewall roughness which decreases from 50-60nm at the top and decreases to 10-20 nm at the bottom.
- (f) The non-Bosch etch process has much lower sidewall roughness which is < 10 nm.
- (g) 30µm deep trench structures have higher undercut at the top which results in lesser deposition of dielectric and barrier at the top than for 10µm deep trenches.

4.3.2 Effect of Bosch process (A) with rough sidewalls

Figure 4.12 (a) shows the maximum peak to peak sidewall roughness is ~ 50 nm for Process A. Figure 4.12(b) shows that the non-Bosch Process B gives a smoother sidewall

with roughness of ~ 10 nm. Figure 4.12 (c) shows the results achieved by a hybrid etch process made of non-Bosch Process B first and then followed by a Bosch Process A. The main motivation for this process was to rectify the scallops within the initial 4-5 μm of the trench depth where the potential for electrical failure is higher due to high sidewall roughness.

Figure 4.19: SEM micrograph of cross-sectioned test samples etched with the Bosch process (A). The scallops can be seen which causes thinning of barrier films due to rough sidewall and shadowing effect in a physical vapor deposition (PVD) process.

Figure 4.13 shows SEM cross-sectional micrographs of copper via structure from Run #2. It shows clearly the rough sidewalls and the non-uniform deposition of tantalum barrier layer. When such an uneven thickness of the barrier layer is subjected to a thermal loading from post-metallization processes (see Steps 7, 8 and 11 in Table 4.3), it has a potential to yield at the weak sites under high thermo-mechanical stress [131]. It can be seen from the initial thermo-mechanical simulation study that there is a concentration of high film stress at the top/bottom corners of the interconnect structure. It also shows that the stress is the highest in the Ta layer of the interconnect structure. Another important observation from the stress simulation studies shown in Fig. 4.5(d) is that the stress in the

tantalum layer is much higher than its yield strength (see Table 4.1) and getting closer to its ultimate strength of ~450 MPa. Hence, if the stress level of the tantalum layer in the top corners of the TSV structure exceeds its yield strength (170 MPa), it is expected to crack the barrier film at its weakest point [132]. Weakening or cracking of the tantalum barrier is expected to result in high electrical leakage current due to copper ion diffusion through the weak barrier and dielectric layer [133]. It can also be seen from Table A-3 and A-4 appended in Appendix A that the thinning of barrier layer is also caused by the dielectric over-hang caused by silicon undercut during the etch process. The effect of barrier thinning is further aggravated by scallops which increase the shadowing effect in the sputtering process. The barrier thinning also was observed with increase in the depth of the trench. However, as the sidewalls are smoother at the bottom, the effect of barrier thinning is not expected to impact the TSV structure.

The electrical leakage current plots are shown in Figs. 4.13 to 4.16 for the test structures with comb width of 5 μm for different process conditions listed in Table 4.5. Figure 4.17 shows the electrical behavior of 5 μm wide comb structures with a 100 μm depth under various thermal loading during the leakage current measurements. It may be seen that high electrical leakage current is observed in all wafers etched with the Bosch etch process with rough sidewalls as shown in Figs. 4.13 and 4.14. Figure 4.13 and Table 4.11 show that there is a 26X reduction in the leakage current when the tantalum barrier thickness is increased to 100 nm from 25 nm for silicon vias etched by the Bosch process. However, when the barrier thickness is increased by having an additional layer of 100 nm of Si_3N_4 , the barrier fails due to high film stress resulting in high leakage current as seen in Fig. 4.13. Figure 4.18 shows the barrier layers peeling-off during the CMP

process as a result of high film stress. From this study it may be concluded that there is limited room to increasing the barrier thickness as the intrinsic stress of the deposited films also goes up causing barrier delamination issues (see Table 4.10). Hence, it may be concluded that a viable solution to this problem lies in improving the DRIE process with smoother sidewalls.

Figure 4.14 shows the effect of varying depths for comb structures etched with the Bosch process (A). It can be seen that there is a gross leak for the test vehicle samples with a depth of $30\text{ }\mu\text{m}$ and $100\text{ }\mu\text{m}$ despite using thicker or additional barrier layers. The failure mechanism contributing to high leakage current is possibly due to poor step-coverage of the deeper trench structures and due to delamination of thicker barrier layers due to the presence of a higher film stress.

4.3.3 Effect of non-Bosch process (B) with smooth sidewalls

Figure 4.20: SEM micrograph of cross-sectioned test samples etched with the non-Bosch process (B). The uniform deposition of barrier films due to smooth sidewall is quite evident at top and bottom of the test structures.

An important conclusion from the FEA study discussed in Section 4.2.2 and 4.3.1 is that the dielectric and barrier layers should be strong enough to withstand high thermo-

mechanical stress load in the top and bottom ends of the copper-plated via structures. It is therefore extremely important to ensure that the silicon dioxide and the tantalum film are conformal and defect free at the top and bottom ends of the interconnects for a good electrical performance. Figure 4.12 shows that a uniform deposition of dielectric and barrier film can be achieved at the top and bottom of the comb structures by using a non-Bosch process (B) with smooth sidewalls. It can also be seen from Table A-3 and 4 appended in Appendix A that the sidewall roughness for non-Bosch etch process is less than 10 nm at top middle and bottom region of the TSV sidewalls. It can also be seen that the undercut to the 3 μ m hard mask is much lower for process B. Thus uniform barrier thickness on sidewall is expected to help in minimizing the leakage current as shown in Fig 4.16. Another important factor that affects the barrier thickness uniformity within the trench is the width of the opening which allows more uniform sidewall deposition with increasing width of the trench (See Table A-4).

For the same via depth and barrier thickness (25 nm), the leakage current in wafers etched with non-Bosch process is atleast 32X smaller than that of the Bosch etch process when measured at 20V (See Table 4.11 and Fig. 4.16). However, despite increasing the tantalum barrier thickness from 25 nm to 100 nm in wafers etched by the Bosch process, there is only a 26X reduction in the leakage current (See Table 11 and Fig. 4.13). This shows that there is a strong effect of the sidewall scallops on the leakage performance in TSV.

A major disadvantage in using the non-Bosch etc process is that it has very low etch rates in the range of 0.2 to 0.3 μ m/min compared to the Bosch etch process which can

etch at 2.5 $\mu\text{m}/\text{min}$ for straight profile (See Table 9). Hence, for vertical TSV with depths in the range of 10-100 μm , it is not practical to etch at such a slow rate.

4.3.4 Effect of non-Bosch+Bosch etch process (Hybrid or combination etch process)

A third option of using a non-Bosch + Bosch process was evaluated and studied for deeper vias and trench structures. The motivation for this study is to develop a deep trench etch process that has high etch rate like in the Bosch process and yet be able to achieve smooth sidewall for good interconnect performance. As shown in Figs. 4.8 and 4.9, the smooth sidewall is required only for the initial 3-4 μm depth, beyond which the sidewall surface becomes smoother. Hence, it was decided to tailor the non-Bosch process (B) with a smooth sidewall with the normal Bosch etch process (A) to etch deep silicon structures to the required depth (See Fig. 4.10(c)). The sidewall roughness and barrier thickness uniformity on sidewalls of the trench is summarized in Table A3 and A-4 in Appendix A. It can be seen from the table that the sidewall roughness due to the hybrid etch process (run-9) is similar to process B (run-6) but the barrier thickness on the sidewall is slightly lower at the top (25-30nm) for run-9 compared to run-6 (30-40nm). Similarly, the dielectric thickness for run-9 at the top is lower (143-184nm) compared to run-6 (230-240nm). This can be attributed to the higher undercut below the hard-mask seen for run-9 due to additional etch time from process A in the hybrid process.

It may be seen from Fig. 4.16 that with the “non-Bosch + Bosch” combination (Hybrid etch process), the leakage current results are as good as in the non-Bosch etched wafers (See Table 4.11). The leakage current for the hybrid etch process (B+A) and Bosch etch process (A) are in the 1-10 pA range. However, it is seen that the barriers breakdown

after 60V. This is attributed to poor barrier and dielectric deposition uniformity over the sidewalls of 30 μm deep comb structures.

From section 4.3.2 and 4.3.3 it can be seen that the leakage behavior in TSV structure is mainly dominated by the silicon etch profile and sidewall roughness caused by the Bosch, non-Bosch and hybrid etch processes. It can also be seen from Fig. 4.21 that the via profile and sidewall roughness for rectangular and circular vias look quite similar in the range of 50-60 nm. Similarly, Fig. 4.22 shows the cross section of rectangular and circular via structures formed by non-Bosch etch process with similar etch profile and sidewall roughness ($< 10\text{nm}$). Due to a close similarity in profile and sidewall roughness due to both Bosch and non-Bosch etch process, it is expected that the circular and rectangular TSV structure will show similar electrical leakage behavior regardless of the etch process used. Hence, any improvement in the sidewall roughness in rectangular via structure due to silicon via etch process is also expected to show similar improvement in circular vias structures

Table 4.11: Ratio of leakage current at 20V for test vehicles etched with Bosch, non-Bosch and hybrid etch process.

Bosch (Run#2) with 25 nm Ta : Non-Bosch (Run#5) with 25 nm Ta	32 : 1
Bosch (Run#2) with 25 nm Ta : Bosch (Run#7) with 100 nm Ta	26 : 1
Bosch (Run#7) with 100 nm Ta: Hybrid (Run#9) with 100 nm Ta	1 : 1

Figure 4.21: SEM micrographs of 5μm wide rectangular and circular TSV structure etched by Bosch etch process with very similar profile angle and sidewall roughness. (a) Cross-section of rectangular TSV structure. (b) Cross section of circular TSV structure.

Figure 4.22: SEM micrographs of 5μm wide rectangular and circular TSV structure etched by non-Bosch etch process with very similar profile angle and sidewall roughness. (a) Cross-section of rectangular TSV structure. (b) Cross section of circular TSV structure.

4.3.5 Effect of thermal stress on TSV interconnect structures

Figure 4.17 shows the leakage current performance of 5 μm wide comb test structures with a 100 μm depth under different thermal stress conditions. The main motivation for this study is to accelerate the failure mechanism and identify the most dominant failure mode(s). In this study, the test wafers were subjected to different substrate temperatures from room temperature of 22°C to 200°C. It is evident from the leakage current plots that the leakage current starts to increase significantly from a picoamperes range to microamperes range as temperature is increased to 200°C. This behavior can again be attributed to non-uniform dielectric and Ta barrier deposition over rough sidewalls formed by the Bosch process (A). Also, as explained in Section 3.1, the high thermo-mechanical stress at the top and bottom of the copper plated via structures is expected to cause the non-uniform Ta barrier films to break at weak sites which results in higher leakage current with temperature.

4.4. CONCLUSIONS

Based on the thermo-mechanical stress modeling, it was predicted that the top corners of through silicon copper via structures will experience high barrier and dielectric stress due to CTE mismatch with through silicon copper vias. Thermo-mechanical stresses on the barrier and dielectric films are also expected to increase with increasing temperature in larger and deeper copper via structures. Simulation studies have also shown that the stresses in the barrier and dielectric layers are mainly concentrated in the sharp corners of the scallops formed by the Bosch etch process which decreases with increasing depth.

Experimental studies were done to reduce the effect of sidewall roughness and

improve the Ta/SiO₂ deposition uniformity by evaluating Bosch, non-Bosch and hybrid etch processes. A test vehicle was designed and fabricated with different etch processes and barrier schemes and studied under different electrical and thermal stress conditions. Results from this work show that the leakage current can be significantly reduced when the sidewall roughness produced by the Bosch etch process is reduced by using a non-Bosch etch process which produces a much smoother sidewalls. It was further observed that the non-Bosch and the hybrid etch processes showed nearly three orders of magnitude lower leakage current than the Bosch etch process. It was also observed that the leakage current increases with increase in temperature, indicating that there is a clear correlation between the leakage mechanism and the thermo-mechanical stress induced during the electrical test.

It was also shown that the main limitation of the slow etching non-Bosch etch process can be overcome by using the hybrid etch process as it only requires the non-Bosch etch process for the initial few microns before switching to the fast etching Bosch process. It was shown that there is no significant impact on leakage current due to scallops formed due to the second etch step. Hence, the hybrid etch process was shown as a viable option for fabricating deeper vias with depths greater than 10 μm which requires higher overall etch rate.

Chapter 5

Development of dual-etch via tapering process for through-silicon interconnection

5.1 INTRODUCTION

One of the greatest challenges confronting the TSV technologists is to maintain high silicon etch rate while at the same time maintaining good control on sidewall roughness and TSV profile for thick silicon substrates. Figure 2.6 shows the 3D IC technology roadmap [79] for various applications with silicon substrate thickness ranging from 20-300 μm . Chapter-4 discussed DRIE technology with straight vias profile for wafer-scale integration of thin silicon substrate (<50 μm). The focus of this work is to develop and characterize a silicon via etch technology that can be used for substrate thickness in the range of 100-300 μm for MEMS and Carrier based packaging application [12, 78, 134]. Figure 5.1 shows some examples of 3D architecture for MEMS packaging application where there is a need for realizing TSV through thick silicon substrates [135, 136]. Forming deep TSV structures through thick substrates of few hundred microns thickness with diameters in the range of 50-100 μm requires very high etch rate processes to reduce the time to process. Profile control is another major challenge when etch rates are high [83, 84, 86]. In case of Bosch etch process, high etch rate process results in severe sidewall scallops, reentrant profile and undercut below the mask [137] which would cause poor sidewall deposition uniformity of dielectric, barrier and seed layers materials (Refer to Section 4.3.2 of Chapter-4). In case of non-Bosch etch process, high etch rates would

result in mask undercut and curvature formation at the top. The focus of this work is to develop and characterize a deep silicon via tapering process by combining convention via drilling methods like Bosch etch process [49-51, 137] and Reactive ion etching process (RIE) [44-48] with an strong isotropic reactive ion etching process [138, 139].

Figure 5.1: Examples of 3D-MEMS wafer level packages with TSV through thick substrates [135, 136].

5.2 MOTIVATION FOR TAPERING DEEP SILICON VIA

The main motivation for via tapering is that it helps in improving the lateral deposition of isolation dielectric, copper diffusion barrier and copper seed metallization over the sidewalls of the deep silicon vias as illustrated in Fig. 5.2. It further enables a void-free copper via electroplating [140]. High aspect ratio vertical profile and scalloped sidewalls, as in Bosch etch process, can significantly contribute to non-uniform sidewall deposition due to profile shadowing effects [141]. The visibility of the ion flux is reduced with increase in depth due to certain points in the profile as shown in Fig. 5.2 which causes non-uniform sidewall deposition.

Figure 5.2: Four different shapes typically encountered in deep silicon via micromachining processes are shown. (a)-(c) show the non-uniform deposition of dielectric and barrier/seed metallization on via sidewall due to ion shadowing effect arising from high aspect ratio and sidewall defects. (d) Shows how a tapered profile can mitigate this problem.

Via sidewall tapering is also preferred wherever there are limited deposition capabilities due to less sophisticated tools available in MEMS foundries and Wafer level bumping/packaging facilities [142]. It is therefore desirable to add a via tapering process to the existing via formation methods like DRIE, laser drilling [143] or powder blasting [144] to achieve the required via profiles. Hence, a taper angle in the range of 83-87° has been proposed for overcoming the problem of conformal deposition of dielectric and barrier/seed metal deposition in TSV application to achieve void-free via-filling [140-143]. It can be seen from Fig. 2.6 and 5.1 that the main beneficiaries of tapered TSV process technology are the carrier based packaging, MEMS wafer level packaging and other applications using thick silicon substrates with TSV. In these applications, it is possible to accommodate the enlargement of the via opening due to tapering as their diameters are quite large in the range of 20-100 μ m.

5.3 EXPERIMENTAL WORK

5.3.1 Experimental Setup

The tapered silicon via etch process development has been done in Surface Technology System (STS) Inductive Coupled Plasma etching system. Although STS ICP etcher is mainly designed for performing Bosch deep reactive ion etch process, it can also be used in reactive ion etch mode, which is referred as non-Bosch process in this thesis. The system consists of ICP electronics, load lock and carousel wafer loading unit and a process chamber. The plasma is generated by coil assembly which is inductively coupled at 13.56 MHz via the matching unit in an alumina chamber. This provides high density plasma capable of achieving high etch rates with little substrate damage. Independent biasing of platen is made available by a separate 13.56 MHz biasing circuit at the bottom electrode, also known as platen electrode, which comes with automatic power control and impedance matching [145]. Process gas is introduced to the chamber through the upper electrode assembly. Wafers are placed on the lower electrode or platen which is powered at 13.56 MHz. The platen temperature is kept at 10°C by using re-circulating deionized water through a chiller system. Figure 5.3 shows the main configuration of the ICP tool used in the experimental work. The figure also describes the basic dissociation and recombination reactions which take place during the silicon etching process. It is necessary to ensure that there is sufficient ion flux to assist the chemical reaction between F-radicals in the plasma and the silicon substrate [146].

Figure 5.3: Configuration of ICP DRIE system used for development of tapered via etch process.

Mask patterns with circular, square and rectangular patterns with diameter/width varying from 10–100 μm are transferred onto a 10 μm thick positive photo resist mask layer coated on silicon test wafers. Boron doped test wafers with resistivity in the range of 10-100 $\Omega\text{-cm}$ has been used in this experiment. Etch time has been set to achieve a trench/via depth in the range of 200-300 μm . It may be noted that for convenience of cross-sectioning for SEM analysis, rectangular trenches have been chosen as a representation of circular vias as no significant change in profile was observed between the two. The vertical silicon vias were then tapered and characterized with different via tapering processes.

Table 5.1: Process flow for silicon carrier fabrication.

Step#	Process description
1.	Lithography of Silicon vias (10-100 μ m vias)
2.	Deep silicon via etch (Main etch step)
3.	Photo resist strip and solvent clean process
4.	Global isotropic etch (Via tapering etch)
5.	Dielectric deposition (1.0 μ m SiO ₂)
6.	1000A Titanium barrier deposition
7.	10,000A Copper seed layer deposition
8.	Copper via-fill by electroplating (40 μ m Cu)

5.3.2 Overview of dual-etch silicon via tapering process

The dual-etch via tapering technology consists of two silicon etching steps. First etch step consists of a high etch-rate process to form deep silicon vias of required depth followed by photoresist stripping and post-etch polymer removal process. The second etch step consists of a global isotropic etch process which results in widening of top of the vias/trenches more than the bottom to form a graded or tapered etch profile. The first etching step is designed to provide high anisotropic etch rate and throughput while the second etch step is designed to provide high isotropic etch rate. The main advantage of this approach is that it helps in maintaining high overall etch rates and still tailor the required via profile. Figure 5.2 shows the existing problems with deep silicon etch process by Bosch and non-Bosch process and how it can be mitigated or overcome by tapering the etch profile. Figure 5.4 shows step by step how the tapering can be achieved. It can be seen that while the isotropic etch process helps in tapering or flaring the via, it also helps in removing or rounding-off some of the surface defects like micro-cracks formed during

wafer thinning process [147, 148] which precedes the silicon etch process in via-last 3D integration technologies [149, 150].

Figure 5.4: Conceptual approach of silicon via tapering process after Bosch etch and non-Bosch etch process as first step and global isotropic etch process as second step. (a) Shows cross-section view of vertical via profile after Bosch etch process. (b) Partially tapered etch profile after RIE etch process. (c) Tapered etch profile after performing the global isotropic etch process. This process removes the sidewall scallops due to Bosch process and the sharp top curvature due to RIE process.

In this work, the existing standard Bosch and non-Bosch etch process, summarized in Table 5.5, has been used to demonstrate the via tapering technology described in Fig. 5.4. In the next section, the Bosch, non-Bosch and global isotropic etch process have been characterized in great detail for trench/via width from 10-100 μm and for different aspect ratios. The plasma etch reaction and fundamental etching mechanism responsible for these processes has also been discussed.

5.3.3 Characterization of first etching step

5.3.3.1 Characterization of first etch step by Bosch process:

The Bosch etch process is based on independent control of short isotropic etch and sidewall passivation chemistries based on $\text{SF}_6 + \text{O}_2$ and C_4F_8 plasmas. As a consequence, it is capable of very high degree of anisotropy and high etch rate. However, an increase in etch rate results in visible sidewalls scallops and reentrant profile due to isotropic nature of SF_6 based etch chemistry. The etch mechanism due to mixture of SF_6 and O_2 gases can be explained as below:

S_xF_y^* , F^* and O^* represents neutral species coming from plasma reaction.

In the etch cycle of the Bosch process, SF_6 dissociates into atomic fluorine (F) and heavy SF_5^+ ions as shown in Eqn. (5.1). Silicon is then subsequently etched by the F-radicals according to the Eqn. (5.5). During the passivation phase of the Bosch process, CF_2 is formed from C_4F_8 as shown in Eqn. (5.3) below:

The CF_2 shown above then adsorbs on the surfaces and forms a Teflon-like polymer shown in Eqn. (5.4) below:

The sidewall passivation layer is deposited as per Eqn. (5.4) during the etch cycle. During the etch phase, these two inhibiting layers are removed by combination of physical ion sputtering and chemical reactions. The physical component in the Bosch process is contributed by positively charged SF_5^+ and chemical etch is mainly due to F and O_2 which are generated from etch step. The scallops shown in Fig-5.4(a) is due to isotropic etching mechanism due to reactions shown in Eqns. (5.1) and (5.5). Figure 5.4(b) shows that after applying the second etching step or global isotropic etch step, the scallops are effectively removed to form smoother sidewalls. Hence, scallops can be tolerated in this process.

Table 5.1 and Fig. 5.5 summarizes the Bosch etch process characterization results for trench width and via diameter ranging from 10-100 μm and depth in the range of 250-350 μm . Figure 5.6 shows the plot of etch depth, etch rate and RIE lag as a function of varying trench diameter from 10-100 μm . The RIE lag has been measured as a difference in the etch depth between adjacent trenches as the trench width is varied by an increment of 10 μm .

Chapter 5 - Development of dual-etch via tapering process for through-silicon interconnection

Figure 5.5: SEM cross sectional micrograph of trenches with depth varying from 260-350 µm for trenches of width varying from 10-100µm after etching with Bosch process. The measured top/bottom CD and trench depth is summarized in Table 5.2.

Table 5.2: Etch rate characterization results of Bosch etch process.

Trench width (µm)	Top width (µm)	Bottom Width (µm)	Trench depth (µm)	Aspect Ratio (AR)	Etch rate (µm/min)	RIE lag (µm)	Bosch etch process		
							Etch parameters	Etch	Pass
10	21.6	22.0	262.0	12.0	2.2				
20	29.5	30.9	291.1	9.6	2.4	29.10	C ₄ F ₈ (sccm)	0	110
30	39.8	42.2	307.0	7.5	2.6	15.90	SF ₆ (sccm)	130	0
40	50.2	51.1	317.8	6.3	2.6	10.80	O ₂ (sccm)	13	0
50	60.9	65.2	323.4	5.1	2.7	5.60	Argon (sccm)	0	0
60	70.3	75.0	328.1	4.5	2.7	4.70	Cycle time(sec)	8	5
70	79.2	85.3	335.6	4.1	2.8	7.50	Coil power (W)	600	600
80	89.5	95.6	336.6	3.6	2.8	1.00	Platen power (W)	23	0
90	100.3	105.5	339.4	3.3	2.8	2.80	Pressure (mtorr)	27-29	16-18
100	108.8	116.7	345.5	3.1	2.9	6.10	Total process time (min.)	115

Figure 5.6: Plots of etch rate, etch depth and RIE lag with variation of trench/via width from 10-100 μm using Bosch etch process. (a) It can be seen that the RIE lag increases while the etch rate decreases with increasing aspect ratio. (b) It can be seen that the trench depth/etch rate increases while the RIE lag decreases with increasing trench/via width.

5.3.3.2 Characterization of first etch step by non-Bosch process:

In case of the first etch performed by non-Bosch process, it is possible to achieve some degree of tapered profile and higher etch rate as some degree of sidewall curvature is acceptable as shown in Fig. 5.4(c). The non-Bosch etch process uses SF_6 , O_2 and Argon in an un-switched mode in the ICP system. Instead of using C_4F_8 as the passivation precursor O_2 has been used as it leads to less accumulation of polymers and also allows more F-radicals to be available to etch silicon at a higher rate. This however results in formation of some undercut and curvature below the mask due to increased isotropic etch reaction. The ratio of SF_6 to O_2 is therefore crucial to maintain a good balance between silicon etching with F-radicals and sidewall passivation with the inhibiting layer SiO_xF_y to maintain a good via or trench profile [152, 153]. Argon has been added to give directionality to the etch process by momentum transfer to the F-radicals which pushes the etch precursors to go deep down the trenches. Also, as Argon is a heavy gas it breaks the inhibiting layer at the bottom of the trenches/vias and allows etch reactions to continue with increasing aspect

ratio. However, as the via depth or aspect ratio increases, the reaction becomes more dominated by the physical etch caused by reactive ions such as SF_5^+ rather than by the F-radical which is confined only to the top as its diffusion is limited with depth and width of the trench opening. The RIE etch mechanism can be explained based on three etch components as explained below by Volland *et al* [154]:

Etch rate (R_{Si}) = Isotropic rate (R_{iso}) + Anisotropic rate (R_{aniso}) - Passivation etch rate (R_p)

where,

$$R_{Si} = \eta_F \Phi_F + K_e \Phi_i - R_p \quad \text{----- (5.11)}$$

η_F = Reaction rate coefficient of fluorine radicals (F)

Φ_F = Fluorine radical flux or neutral flux

Φ_i = Ion flux

K_e = Reaction rate enhancement coefficient

$$\eta_F = K_0 \exp\left(\frac{-E_a}{k_B T}\right) \quad [154] \quad \text{----- (5.12)}$$

where,

E_a = Activation energy of F-Si reaction

K_0 = Constant

k_B = Boltzmann's constant

Table 5.3 summarizes the process conditions and the characterization results of the RIE or non-Bosch etch process that was evaluated for trench/via widths varying from 10-100 μm . Two significant observations can be made from the experimental characterization results. The RIE lag in the non-Bosch etch process is much lower than that in the Bosch etch process for same mask patterns. The RIE lag effect is significant only in the range of 10-20 μm trench width. Another significant observation is that the taper angle of the non-

Bosch etched trenches decreases with increasing width of the trenches as can be seen from SEM micrographs shown in Fig. 5.7. This can be attributed to the fact that the neutral flux (Φ_F) can easily diffuse into larger trenches/vias along with ion flux (Φ_i) unlike in trenches with smaller widths $< 20\mu\text{m}$ where the neutral flux are limited by narrow widths and hence are mostly confined to the top of the trenches. It can also be seen that the isotropic etch component (R_{iso}) follows an Arrhenius relationship with respect to temperature (T) and hence is sensitive to wafer surface temperature which provides the necessary activation energy for this reaction. The anisotropic etch component (R_{aniso}) increases with ion flux which follows an angular distribution function $\Phi_i(\theta)$. The ion flux can be increased by (a) increasing platen power, (b) by adding noble gases like Argon and (c) by reducing the process pressure, as shown in Table 5.3. Finally, the etch profile in the Bosch or non-Bosch process is controlled by maintaining a proper balance between the isotropic (R_{iso}) and anisotropic (R_{aniso}) etch components [152, 153].

Table 5.3: Etch rate characterization results of non-Bosch etch process.

Trench Width (μm)	Top width (μm)	Bottom width (μm)	Mean Taper angle ($^\circ$)	Mean trench depth (μm)	Aspect ratio	Etch rate ($\mu\text{m}/\text{min}$)	RIE lag (μm)	Non-Bosch etch process	
10	54.5	30.4	84.8	194.0	4.6	3.9		APC (%)	84.3
20	62.3	44.7	86.4	204.7	3.8	4.1	10.7	Pressure (mtorr)	30 mtorr
30	73.0	59.1	86.8	212.5	3.2	4.3	7.8	Coil Power (W)	600
40	82.4	72.0	87.5	217.3	2.8	4.3	4.8	Platen Power (W)	30
50	90.9	82.0	87.5	220.1	2.5	4.4	2.8	SF ₆ (sccm)	42
60	101.7	95.6	88.2	223.7	2.3	4.5	3.6	O ₂ (sccm)	33
70	112.2	108.3	88.3	226.3	2.1	4.5	2.7	Argon (sccm)	30
80	121.4	120.4	88.9	228.1	1.9	4.6	1.7	C ₄ F ₈ (sccm)	0
90	129.7	129.9	89.0	229.5	1.8	4.6	1.4	Platen temperature ($^\circ\text{C}$)	10
100	141.8	142.8	89.2	231.4	1.6	4.6	1.9	Process time (min)	50

Figure 5.7: SEM cross-sectional micrographs of trenches with depth varying from 190-240 μm for trenches of width varying from 10-100 μm after etching by the non-Bosch process.

Figure 5.8: Etch characterization plot of the non-Bosch etch process is shown for different trench widths and aspect ratios. (a) It can be seen that the etch depth increases and eventually slows down while the etch profile becomes straighter (see Fig. 5.8) with increasing trench width. It can also be seen that the RIE lag decreases with increasing trench width. (b) The RIE lag increases with increasing aspect ratio while the etch rate decreases with increasing aspect ratio.

5.3.4 Characterization of second etching step by global isotropic etch process

The objective of the second etch process is to taper the profile of the TSV structure. This is accomplished by an isotropic etch chemistry which is rich in free radicals as shown in Eqn. (5.1) in Section 5.3.3.1. A gas ratio of 10:1 for the SF_6/O_2 etch chemistry has been used as it results in high isotropic etching which is further assisted by ion bombardment. Figure 5.5 illustrates the fundamental mechanism responsible for the tapering of the silicon trenches and vias. The isotropic etch (R_{iso}) process dominates over the anisotropic etch process (R_{aniso}) (refer to Eqns. (5.11) and (5.12)). It is therefore evident that there is no passivation process required. Hence, R_p shown in Eqn. (5.11) is zero. The tapering process therefore requires (a) enhanced chemical etching with radical/neutral flux (Φ_F) and (b) sufficient ion flux (Φ_i) to increase the taper angle by ion-assisted tapered sidewall etching and by pushing radical flux further down the trench/vias through inelastic collisions.

Table 5.4 summarizes four different process conditions (E1-E4) that have been evaluated to study the evolution of tapered etch profile. Wafers etched with each of the isotropic etch process was scanned with Dimension 5000 Atomic Force Microscope (AFM) from Veeco Instruments and its average surface rough (R_a) was measured. A 5nm by 5nm square area was scanned with a scan rate of 1.507 Hz outside the silicon via in the centre and edge of the wafer. The last column in Table 5.4 summarizes the surface roughness measured for each process condition. It can be seen that condition E1 yields the best results with minimum surface roughness. Figure 5.9 (a-d) shows SEM micrographs taken after performing the global isotropic via tapering process for vias etched by Bosch and non-Bosch etch process using the recipe E1 which gives minimum surface roughness

during global silicon etch. Table 5.5 summarizes the final dual-etch via tapering process for evaluating the via-filling capability by copper electroplating process.

Table 5.4: Summary of various Global isotropic etch processes evaluated for via tapering.

2 nd etch Recipe #	SF ₆ (sccm)	O ₂ (sccm)	Ar (sccm)	Coil Power (W)	Platen power (W)	Pressure (mtorr)	Surface Roughness (nm)
E1	180	18	0	600	30	13.0	0.585
E2	250	25	30	1000	30	32.0	10.1
E3	180	18	0	600	30	35.0	0.965
E4	250	25	0	600	30	20.0	1.041

Table 5.5: Dual-etch via tapering process using the Bosch and non-Bosch process.

First etch step (Bosch etch process)	Etch cycle: Pressure=27-29mt; Coil Power=600W; Platen power= 23W; SF ₆ =130sccm; O ₂ =13 sccm; Cycle time= 8 seconds
	Passivation cycle: Pressure=16-18mt; Coil power=600W; Platen power=0 W; C ₄ F ₈ = 85sccm; Cycle time=5 seconds
	Platen Temperature: 10 °C; Total process time: 60 minutes. Etch rate: 2-3µm/min on 15-20% exposed area. Etch selectivity to resist mask = 82-100:1
First etch step (Non-Bosch etch process)	Pressure=30mT (APC: 78%); SF ₆ =42 sccm; O ₂ =33 sccm; Ar=30 sccm; Coil Power=600W; Platen power= 30W Platen Temperature: 30 °C; Process time: 60min. Etch rate: 3.9-4.6µm/min on 15-20% exposed area. Etch selectivity to resist mask = 27-30:1
Second etch step or Global isotropic etch process	Pressure=35 mTorr (APC: 82.2%); SF ₆ =180 sccm; O ₂ =18 sccm; Coil power=600W; Platen power=30W; Platen Temperature: 10 °C; Process time: 5-30 minutes depending on required slope. Etch rate: 1.2-1.5 µm/min

Figure 5.9: (a-b) SEM micrographs of TSV sidewall after first etch by Bosch process followed by via tapering isotropic etch process. (c-d) SEM micrographs of sidewall after first etch by non-Bosch etch process followed by via tapering by isotropic etch process.

5.4 TOPOGRAPHY SIMULATION OF VIA TAPERING PROCESS

Chapter-3 provided a detailed overview of 2D Topography simulation using Athena Elite from Silvaco. The RIE etch model built in the RATE.ETCH statement is defined by the RIE parameters- *isotropic, directional, chemical and divergence*. Hence, we can model ion milling (physical etching), isotropic etching (chemical etching) and beam divergence model which emulates the effect of angular incidence of reactive ion flux. The divergence parameter can be specified only if a non-zero value of chemical etch rate is specified as the divergence of beam always results in some degree of lateral/chemical etch.

The motivation of the topography simulation study is to model the dual-etch tapered via etch process with first etch step defined by geometric etch model to represent Bosch etch profile. The second etch step is modeled by using RIE model parameters- Divergence, Chemical etch, Isotropic and Directional etch. Design of experiment (DOE) was done by varying three factors - Divergence, Chemical and Isotropic etch. Directional etch has been set to zero as it is insignificant in second etch step. The optimum solution from DOE was used to set up the simulation program. Based on the optimum solution a close match was seen with the experimental results as summarized in Table 5.6. Figure 5.11 shows a comparison between the simulated and experimental etch trend of a dual-etch via tapering process. It can be seen that there is a very close correlation within a 10% deviation.

Table 5.6: Comparison of experimental and simulation results of the dual-etch process.

Trench width aft. 1 st etch (μm)	Trench depth aft. 1 st etch (μm)	Experimental Results after global isotropic etch for 30min				Athena Elite Simulated results		
		Top width (μm)	Bottom width (μm)	Trench Depth (μm)	Etch rate ($\mu\text{m}/\text{min}$)	Top Width (μm)	Bottom Width (μm)	Trench Depth (μm)
21.6	262.0	48.3	21.6	237.7	2.2	46.4	22.1	237
29.5	291.1	53	29.5	255	2.4	56	32.6	264
39.8	307.0	66.1	40.3	268.6	2.6	67.1	43.4	285
50.2	317.8	76.9	51.6	283.6	2.6	77.6	54.3	299
60.9	323.4	88.1	65.2	291.1	2.7	88.3	64.4	296
70.3	328.1	98	73.1	294.8	2.7	98.3	75.2	309
79.2	335.6	106.4	85.3	301.9	2.8	108	85.2	309
89.5	336.6	121.4	96.1	301.9	2.8	119	96.1	325
100.3	339.4	128	107.8	309.8	2.8	129	107	313
108.8	345.5	138.8	121.4	315.9	2.9	139	117	317

Figure 5.10: Experimental results of first etch done by the Bosch etch process and second etch done by the global isotropic etch process.

After establishing a dual-etch process model, it has been used in further predicting the etch profile evolution as a function of isotropic etch time. Figures 5.12 and 5.13 show the predicted results when the via tapering etch process is applied with different isotropic etch time from 5-30 minutes for a 20 μm wide trench/via structure. It can be seen that while the depth of the trench/via decreases linearly, the depth of the taper increases with increasing etch time. It is also seen that the bottom of the trench is least affected even after longer etch from 5-30 minutes. This confirms that the basic etch mechanism for the second etch step is a diffusion limited etch process.

Figure 5.11: Comparison is made between simulated and experimental results of dual-etch tapered via etch process. It can be seen that there is a very close match between the two results within a 10% tolerance.

Figure 5.12: Simulation of via tapering effect as a function of global isotropic etch process time from 0-30 minutes.

Table 5.7: Simulation results of via tapering etch process with varying etch process time.

Etch time (min)	Top width (μm)	Bottom Width (μm)	Final trench Depth (μm)	Taper depth (μm)	Aspect Ratio	Isoetch Rate (μm/min)	Depth Loss (μm)
5	26.1	20.2	258	39	11.1	0.8	4
10	29.2	20.6	254	72.2	10.2	0.8	8
15	33.9	20.9	249	122	9.1	0.87	13
20	37.7	21.4	244	147	8.3	0.9	18
25	41.6	21.7	239	191	7.6	0.92	23
30	45.6	22	235	234	7	0.9	27

Figure 5.13: Simulated results plotted as a function of isotropic etch time and aspect ratio. (a) It is seen that the etch depth decreases with increasing etch time while the taper depth increases with etch time. The top width of the trench increases linearly with etch time while the bottom of the trench is unaffected due to diffusion limited etching. (b) The isotropic etch rate increases with increasing etch time till it slows down after an aspect ratio of 8. It is also seen that the taper depth increases with increasing etch time.

5.5 RESULTS AND DISCUSSION

5.5.1 RIE lag mechanism in Bosch etch process

It can be seen from Table 5.2 and Fig. 5.7 that the RIE lag effect is gradually decreasing for dimensions greater than 50µm. It can be explained that the increase in the RIE lag with decreasing trench width or via diameter is mainly due to inability of F-radicals or the neutral flux to diffuse into smaller gaps [155-157]. Coburn and Winters showed that this reduction of the neutral flux towards the bottom of the feature can best be described by Knudsen transport model [158]. In this model, neutrals are lost either on the feature sidewall as described by the transmission probability or get reflected from the etching surface as described by the reaction probability. The remaining species contribute to the etching process based on Eqn. (5.9).

$$\Phi_{Ftop} - (1 - K)\Phi_{Ftop} - K(1 - S)\Phi_{Fbottom} = S\Phi_{Fbottom} \quad \text{----- (5.9)}$$

where,

Φ_{Ftop} = Neutral flux of reactant species at top or incident flux

$\Phi_{Fbottom}$ = Neutral flux of reactant species that has reached the bottom of trench/via

K = Neutral flux transmission probability to reach the bottom

S = Reaction probability on the bottom surface

R_{bottom} & R_{top} = Etch rate at bottom and top of the trench/via

Since the etch rate is proportional to available reactant flux at the top and bottom of the structure, the above expression can also be expressed in terms of etch rate as follows:

$$\text{Etch rate at the bottom } (R_{\text{bottom}}) = \frac{R_{\text{top}} \Phi_{F_{\text{bottom}}}}{\Phi_{F_{\text{top}}}} = \frac{KR_{\text{top}}}{[K(1-S) + S]} \text{ ----- (5.10)}$$

Typical high etch rate Bosch process is dominated by high SF_6 gas flow (100-200 sccm) and higher pressure (20-30 mtorr) to increase the K and S factor in Eqn. (5.10). However, the experimental results summarized in Fig. 5.6 confirms that only the top region of the trench has visible scallops while more than 50% of the trench sidewall in the bottom region is smooth. This effect is due to the depletion of neutral flux (Φ_F) at the bottom with increasing aspect ratio. Hence the above aspect ratio induced RIE lag is unavoidable. It is also possible to use the gas conductance model proposed by Coburn and Winters [156] to explain the difference in the etch rate between high and low aspect ratio trenches/vias. As the pumping conductance in trenches with wider width is much higher than trenches with smaller width, it can be explained that higher conductance facilitates faster replacement of reaction byproducts from the bottom of the trenches. Hence, higher pumping speed can also reduce the RIE lag effect.

5.5.2 RIE lag mechanism in non-Bosch etch process

Table 5.3 and Fig. 5.8 show a significant trend of non-Bosch etch process which is dominated by ion flux (Φ_i). the flow of SF_6 is also much lower (42 sccm) compared to 130 sccm in the Bosch etch process. The effect of neutral flux (Φ_F) is further suppressed by adding more Oxygen in the process as shown in Table 5.3. In order to breakthrough the inhibiting layer of SiO_xF_y , Argon gas has been added and higher platen power of 30W has been used. It can also be seen from Figs. 5.6 and 5.8 that there is a significant difference in the RIE lag effect between the Bosch and non-Bosch etch process. Though the etch rate

decreases with increasing aspect ratio as in the Bosch etch process, the dominance of ion flux creates less impact on the RIE lag despite an increase in the aspect ratio. The maximum lag is still less than 10μm compared to the Bosch process where the minimum lag is in the range of 5-10μm.

The difference in the RIE lag between the Bosch and non-Bosch can also be explained based on the following expression derived from ideal gas law which correlates Fluorine radical flux (Φ_F) with partial pressure of F-radical (P_F) [159]:

$$\Phi_F = \frac{P_F}{\sqrt{2\pi m_F k_B T}} \quad \text{----- (5.13)}$$

where,

m_F is atomic mass of Fluorine,

k_B is the Boltzmann's constant and

T is Plasma temperature.

Based on the Eqn. (5.13), the silicon etch rate can be determined as follows:

$$R_{Si} = \frac{\Phi_F S}{r_E \rho} = \left(\frac{P_F}{\sqrt{2\pi m_F k_B T}} \right) \left(\frac{S}{r_E \rho} \right) \quad \text{----- (5.14)}$$

From the above equation it is possible to conclude that the reaction probability of F with silicon and the partial pressure of F or higher gas flow or chamber pressure play a significant role in enhancing the silicon etch rate at the top and bottom of silicon microstructures. Alternatively, it is also possible to express R_{Si} as follows:

$$R_{Si} = (2.91 \pm 0.20) \times 10^{-12} n_f \sqrt{T} \exp\left(\frac{-E_a}{k_B T}\right) \text{ (Flamm *et al.*, 160)] ----- (5.15)}$$

$$= \eta_F \Phi_F = K_0 \Phi_F \exp\left(\frac{-E_a}{k_B T}\right) \text{ (Volland *et al.* [154]) ----- (5.16)}$$

where,

S is reaction probability of F with Si,

ρ is atomic density of silicon

r_E is between 1-4 which is the stoichiometry of the reaction product. For SiF_4 it is 4.

n_f is Fluorine atom concentration [160] which is equivalent to Φ_F (F-radical flux)

E_a is the activation energy for Si-F etch reaction

η_F = Reaction rate coefficient of fluorine radicals (F)

Equations (5.15) and (5.16) can also be combined as follows:

$$R_{Si} = (2.91 \pm 0.20) \times 10^{-12} \sqrt{T} \Phi_F \exp\left(\frac{-E_a}{k_B T}\right) \quad \text{----- (5.17)}$$

Where $K_o = (2.91 \pm 0.20) \times 10^{-12} \sqrt{T}$

It is now possible to express the reaction rate coefficient as follows:

$$\eta_F = (2.91 \pm 0.20) \times 10^{-12} \sqrt{T} \exp\left(\frac{-E_a}{k_B T}\right) \quad \text{----- (5.18)}$$

From Eqns. (5.14) and (5.18) it is possible to deduce that ion flux can play a useful role in increasing the reaction rate coefficient η_F as it provides the necessary activation energy (E_a) required for the reaction between F and Si at the top and bottom of the trenches and thus reduces the difference in the etch rate at the top and bottom of the trench. In case of the non-Bosch process it can further be explained that due to a higher platen power of 30W (compared to only 23W in case of Bosch process) and due to a suppression of F-radical due to lower SF_6 to O_2 gas ratio (see Table 5.3), the reaction is dominated by ion assisted etching in vertical direction by positively charged ions like SF_5^+ ion which have a greater tendency to reach the bottom of the trench/vias as they are accelerated towards the wafer on cathode. Hence, the depletion of F-radicals at the bottom has not produced any significant RIE lag effect.

5.5.3 Evolution of tapered etch profile by global isotropic etch process

Table 5.4 shows four process conditions that can potentially cause the neutral flux to diffuse into the trench and cause greater tapering of the microstructure. The impact of increased neutral flux on the condition of silicon surface can be seen in last column of Table 5.4. Figures 5.14 and 5.15 present the impact of the four process conditions on the geometry of trenches when its width varies from 10-100 μm .

Figure 5.14: (a) shows trench depth variations versus trench width after first etch by the Bosch process and the second etch by global isotropic etch process. It can be seen that the second etch step reduces the silicon thickness globally according to size of the via opening. (b) shows the amount of depth reduction due to different global etch condition and with increasing trench width.

Figure 5.14 (a) presents the depth variation after the global isotropic etching process with recipes E1-E4. It can be seen that as the process pressure is varied from 13 to 35 mtorr (E1 and E3), the loss of silicon increases significantly from 5-35 μm . However, both recipes gave minimum surface roughness after 30 minutes etch. It may be noted that high depth loss indicates that the neutral flux is unable to diffuse down the trench which results in greater etch in the top region. This condition results in loss of the overall depth. This result is consistent with Eqn. (5.14) which indicates that higher F radical flux (Φ_F)

and high partial pressure (P_F) allows greater reaction probability at the bottom of the trench/vias which is expected to result in lesser depth loss as in E3. Similarly, the behavior of recipes E2 and E4 can be explained better by Eqns. (5.15) and (5.16) which show that a higher SF_6 flow or higher ion-bombardment would result in higher reaction probability at the top and bottom of the trench. The taper angle is therefore much higher than for E1 and E3. However, due to an excessive reaction on the surface due to higher fluorine concentration and greater ion bombardment, the surface roughness is higher than for E1 and E3.

Figure 5.15: (a) Plot shows the depth of the tapering as a function of trench width. (b) Shows the dependence of the taper angle on the second etch process conditions (see Table 5.4). The first etch was done by the Bosch process. It can be seen that via tapering effect is higher for vias $< 50\mu m$. It is also seen that via tapering is higher when SF_6 is increased and when Argon ions are added to plasma.

Figure 5.15 shows that E2 gives the highest taper angle by pushing the neutral flux (Φ_F) down and also provides activation energy (E_a) to the bottom surface thus enabling greater spread in the taper angle from the top to bottom. This increase in taper was made possible due to Argon addition which also increases the surface roughness. From all the

four recipe conditions, only recipe E1 yields minimum surface roughness and acceptable taper angle.

Figure 5.16: Optical micrographs of 221-228μm tapered silicon via after copper electroplating process (a) Main etch done by a non-Bosch etch process and (b) Main etch done by a Bosch etch process.

5.5.4 Impact of dual-etch tapered via etch process on Cu-via-filling process

Figure 5.16 (a) and (b) shows the final tapered via profile after the dual-etch technology was implemented with Bosch and non-Bosch etch process as the first etch step. The second etch step was done using the E1 (see Table 5.4) and finally the tapered silicon vias were filled with copper by DC pulsed plating method. Figure 5.16(a) was formed by doing the first etch with a non-Bosch process and in the case of Fig. 5.16(b) it was etched by a Bosch process. Though a slight via tapering would be sufficient for getting void-free copper via filling, it should be noted that for deeper vias ($>200\mu\text{m}$) the tapering should be extended further towards the bottom to achieve void-free via filling.

5.6 SUMMARY

A dual-etch via tapering technology was introduced which offers the flexibility of combining disparate via drilling technologies like Bosch and non-Bosch etch technologies. Through this work it has been shown that the dual-etch process technology provides high degree of process flexibility to the user by independently controlling etch rate and sidewall tapering process. Though the proposed via tapering process was demonstrated for vias formed by Bosch and non-Bosch methods, it was shown that this technology can be applied to other methods of forming deep silicon vias. Detailed characterization studies were done on the Bosch, non-Bosch and Isotropic etch process to understand the aspect ratio induced RIE lag effects. From a detailed characterization of different isotropic etch processes and its impact on surface roughness, it was shown that the most desirable via tapering process should operate under low pressure for optimum performance. It was finally shown that it is possible to realize a void-free copper via-filling by the standard DC pulsed plating. The results presented thus meets a critical requirement for forming through-silicon copper interconnection for 3D Microsystems packaging application.

Chapter 6

Integration of tapered via etch technology for silicon carrier fabrication

6.1 INTRODUCTION

TSV technology enables vertical integration of multiple functions and disparate technologies within a small foot-print and form-factor. Numerous 3D architectures and integration approaches have been reviewed by J.Q. Lu and K. Roseare in [75]. Among the various 3D integration methodologies, silicon carrier based 3D integration approach had received lot of attention due to the advantage of being able to assemble known good dies and also due to better testability [161]. In early nineties, multi chip module (MCM) technology was a popular choice for high density lateral integration or 2D integration [162]. Subsequently, Massit and Nicolas proposed a vertically integrated 3D MCM architecture to improve electrical and thermal performance of densely packed electronic components [163]. Since 2000, various silicon carrier based architectures emerged [164, 165]. Figures 6.1 to 6.3 shows the trend in 3D integration approaches based on silicon carriers. It may be noted that the silicon carriers may be made of active or passive silicon substrate. Similarly, the assembled components may be MEMS or ICs.

The scope of this chapter is to develop and characterize various critical process modules that are required for final integration and fabrication of silicon carrier with high aspect ratio tapered TSV interconnections. The main motivation of this study is to demonstrate the feasibility of integrating the dual-etch tapered silicon via etching process

(discussed in Chapter 5) with all the post-processes shown in Table 6.1 to form a 200 μm thick silicon carrier by a via-first approach. The silicon carriers is eventually assembled and tested for electrical continuity of through silicon interconnection by assembling dummy chips. A generic multi-step silicon via etching methodology has also been presented that can cater to a wide range of depth requirements from 100 to greater than 300 μm TSV depth and taper angle in the range of 83-87°.

Figure 6.1: (a) 3D stacked silicon carriers using conventional wire-bonding scheme [163]. (b) Vertical integration of silicon carriers with flip-chip and wire-bonded devices [165]. (c) Single level carrier-based package with several assembled 3D ICs [164].

6.2 SIGNIFICANCE OF VIA PROFILE IN TSV APPLICATION

Silicon via etch profile plays a significant role in the realization of reliable and void-free interconnect. The choice of silicon via geometry and its profile angle largely depend on the TSV integration approach used in the fabrication technology. CMOS Wafer fab based TSV technology adopts via geometry in the range of 1-5 μm diameter with a depth of 10-50 μm and a vertical profile [73, 79]. Vertical TSV profiles can be integrated into CMOS fabrication technology due to availability of sophisticated tool set for conformal dielectric deposition, sidewall metallization and via filling. In case of via-last TSV technology [21], the via profile and aspect ratio is limited by the need to etch-stop on dielectric layer with minimum notch [21, 166]. Vertical TSV profile with high aspect ratio and scalloped sidewalls, as in the Bosch etch process, can significantly contribute to non-uniform sidewall deposition by profile shadowing effects caused by ion angular distribution (IAD) of incoming ions [141, 167-169]. The visibility of the ion flux is also reduced with increase in depth due to certain points in the profile as shown in Fig. 5.3 which causes non-uniform sidewall deposition. As the wafer level packaging facility mostly lacks expensive tool-sets needed to overcome these issues, a tapered via profile is adopted as a compromise solution to overcome these integration challenges [142].

Tapered vias, compared with vertical vias, ensure good sidewall coverage with dielectric isolation layer, copper diffusion barrier and copper seed layer. Tapered profile also greatly eases via filling [170]. It should be noted that deposition processes like plasma enhanced chemical vapor deposition (PECVD) and physical vapor deposition (PVD) are strongly dependent on via profile to achieve uniform sidewall coverage which is essential for a reliable TSV structure [142]. A taper angle in the range of 83-87° is widely reported

to ensure good dielectric and seed layer step coverage and achieve a void-free copper via plating. [171]. Though the step-coverage of plasma deposited films decreases with decreasing deposition temperature, it is nevertheless required to keep the temperature as low as possible to minimize build-up of thermal stresses around the interconnect structures [25, 113]. Thus tapered via profile greatly helps in offsetting the disadvantage due to lower temperature for dielectric deposition which can be as low as 150 °C for image sensor application [172]. The ultimate compromise to having a tapered TSV is some relaxation in the via pitch to accommodate the enlargement of the top via diameter. In the present work, a taper angle of 83-87° has been targeted for TSV depth in a range of 100-300µm with average via aspect ratios of 2-5.

6.3 CRITERIA FOR TSV INTERCONNECT MATERIAL SELECTION

Polysilicon is chosen as via filling material when pre-processed materials and structures can withstand low-pressure chemical vapor deposition (LPCVD) process temperature of 550-650 °C and high temperature polysilicon doping and annealing at 900-1000 °C [173]. The high process temperature gives polysilicon deposition process an excellent ability to deposit uniformly over the via sidewall and form void-free interconnect structures. Void-free polysilicon via-filling is suitable for applications that require very high via aspect ratio of 30-35 [174, 175]. The polysilicon interconnect also enjoys another advantage of having a coefficient of thermal expansion (CTE) very close to that of surrounding materials like silicon and silicon dioxide. Tungsten (W) CVD is another popular candidate in CMOS wafer fabs as it is commonly used in making metal contacts at 300-450 °C. W via-fill can also be used for high aspect ratio vertical TSV of 1-5µm

diameter and 30-50 μ m depth [176].

Aluminum and copper are widely used for the back-end metallization in wafer fab technology. The most commonly preferred back-end metallization technology is the copper damascene technology which was conceived and developed in early 1990s [177]. An advantage with barrier/copper seed metallization and electroplating process is that it can also be done at room temperature with minimum stress build-up. It should however be noted that during subsequent post-TSV fabrication processes, like dielectric deposition process, large thermo-mechanical stresses can build-up around the interconnect structures due to CTE mismatch between metal and dielectric. These stresses can lead to stress-induced voiding within the metal interconnections which can eventually cause an open circuit or resistance increase in interconnections [178]. The thermal budget for TSV and post-TSV processes is further decided by polymeric glue that is used to attach the thin carrier substrates with a support wafer. The polymeric glue can degrade when subjected to temperatures higher than 250 °C [179]. In the present work, copper damascene technology has been used for demonstrating void-free via filling. The dielectric deposition temperature has been kept at 250 °C.

6.4 EXPERIMENTAL PLAN

6.4.1 Silicon carrier fabrication requirement

Silicon carrier made of test wafers with resistivity of 0-100 Ω -cm is suitable for application below 5GHz. For higher frequency application which involves RF passive or active device integration, a much higher resistivity substrate of 1000-2500 Ω -cm would be required [180, 181]. In the present work, standard silicon test wafers have been chosen as

only mechanical samples are intended to be made for electrical continuity measurements of TSV structures. Following are the key process modules that need to be integrated to fabricate a silicon carrier with TSV interconnections:

- (a) Deep-silicon tapered via etch process: The tapered via is evolved in three etching steps. Each step can be independently optimized and characterized to achieve the final via process.
- (b) Via sidewall dielectric isolation process: A low-temperature (250°C) plasma enhanced chemical vapor deposition (PECVD) process is developed and characterized for providing low-stress dielectric isolation structure for the TSV.
- (c) Uniform deposition of copper diffusion barrier and copper seed metallization and final via-fill by copper electroplating process. It is intended to use the available standard metallization and electroplating process conditions.
- (d) Chemical mechanical polishing (CMP) of over-plated copper to form a damascene copper via.
- (e) Wafer back grind and polishing to form through silicon copper interconnection.

6.4.2 Silicon carrier design

The present work focuses on silicon carrier fabrication by via-first approach [73, 179]. Design of test dies and silicon carriers chips are shown in Fig. 6.2 for electrical continuity and reliability testing of vertically assembled stacked module. A 200 μm thick silicon carrier with electrical continuity test structures of 50 μm diameter via has been targeted by via-first approach. The average aspect ratio targeted for tapered silicon via in this study is ≥ 3 with bottom via diameter of 40 μm and top diameter of 100 μm . The aspect

ratio is calculated by dividing the via depth by average via diameter. The average via diameter is based on top and bottom via diameter.

The TSVs are designed as peripheral vias with redistribution metal traces to interconnect with daisy chained test chips. The continuity of the TSVs are tested by electrically probe-testing the organic substrate on which the silicon carriers are eventually assembled as shown in Fig. 6.2. The three chips shown are test dies with daisy chain structures for continuity check of the TSV interconnects after the silicon carriers are stacked. The assembled 3-D stacked modules are subjected to a thermal cycle (TC) reliability test. The condition for the TC test is -40°C to 125°C for 1000 cycles. Electrical daisy probing is done at regular intervals to detect any failures in the modules [117, 123, 181]. The details of assembly and test methodology have been explained by Navas *et al.* in their work [32, 182].

Figure 6.2: (a) Illustration of 3-D SIP platform formed by stacking 2 silicon carriers with through-silicon copper interconnections. Carrier thickness can typically be in the range of $200\text{-}300\mu\text{m}$. (b) Layout of through silicon vias on silicon carrier-1 and 2 for evaluating the TSV and wafer stacking process.

6.4.3 Silicon carrier fabrication process

The silicon carrier fabrication technology is described in some detail in this section as it is the focus of this work. The silicon carrier fabrication technologies can be broadly classified into two approaches namely - via-first and via-last approach [73]. In the via-first approach, the required numbers of TSVs are fabricated as blind vias with the dielectric isolation and barrier/seed metallization before performing copper electroplating and chemical mechanical polishing (CMP) process. After performing the copper CMP process the multi-level metallization are fabricated until the final passivation and UBM metallization. The carrier wafer is then attached to a handler wafer and back grinded and polished till the TSV structures are exposed from backside of the carrier wafer. Again multi-level metallization traces are formed similar to front-side of the carrier wafer till under-bump metallization (UBM). The handler wafer is now released and separated from the front-side [182].

In case of via-last approach, the multi-level metallization structures are first formed and then the front-side of the wafer is attached to a handler wafer and back grinded to 200 μ m thickness. Through silicon via structures are then formed to stop on front-side metal pads. The sidewalls of the through silicon vias are then deposited with dielectric isolation, barrier and copper seed metal layer. The vias are then filled by electroplated copper. The over-plated copper is removed by CMP process. The exposed TSVs are further redistributed by multi-level metallization. Finally, the backside metal pads are passivated and then patterned to form UBM metallization. The handler wafer is then separated. The process details are summarized below in Table 6.1.

Table-6.1: TSV process flow for fabrication of silicon carrier.

#	Via-first	Via-last
1	Blind via formation by DRIE	Front side multi-level metallization till Final passivation and UBM metallization
2	1 μ m PECVD SiO ₂ deposition	Handler wafer attachment on front-side
3	1KA Ti+1 μ m Cu seed metal deposition	Wafer thinning to 200 μ m
4	Cu-Electroplating & CMP process	Through silicon via formation by DRIE
5	Front side multi-level metallization till Final passivation and UBM metallization	2 μ m PECVD SiO ₂ deposition and etch back
6	Handler wafer attachment on front-side	1KA Ti+1 μ m Cu seed metal deposition
7	Wafer thinning to 200 μ m	Cu-Electroplating & CMP process
8	Backside multi-level metallization	Backside multi-level metallization
9	Passivation deposition, Pad open & UBM formation	Passivation deposition, Pad open & UBM formation
10	Handler wafer separation	Handler wafer separation

The fully fabricated silicon carriers are then used as a substrate for assembling test dies with daisy chains and then stacked as shown in Fig. 6.2. It may be noted that the handle wafer mentioned in both the approaches are attached by a temporary adhesive which is finally removed in the last step to detach the processed silicon carrier wafer [179]. A detailed study of thin wafer handling process is beyond the scope of the present work. The present work therefore focuses mainly on development and integration of TSV process for carrier fabrication by via-first approach. The various challenges in process integration are also addressed.

6.4.4 Development of multi-step tapered silicon via etch process

6.4.4.1 Approach

The deep silicon via etch process development is done in inductive coupled plasma based deep reactive ion etching system from Surface Technology System [137, 145]. The system is used in (a) switched mode for Bosch etch process, (b) in unswitched mode for RIE process and (c) in predominantly chemical etch mode. A generic multi-step via

formation process is shown with independently controlled process steps as illustrated in Fig. 6.3. In step-1, a Bosch etch process is done with vertical profile [49-52]. In step-2, a RIE etch process is done with a tapered etch profile [152, 153]. The second step usually results in some undercut and sharp curvature at the top. In step-3, the etch mask is stripped and cleaned to expose the silicon surface and via. Finally, in step-4, a global isotropic etch process is done to remove the sharp curvature at the top and further taper the via profile.

This generic silicon via etch process consisting of step-1 to 4 can be used to suit various application. Step-1 can be used whenever a vertical etch profile is preferred. Step-2 to step-4, also described as dual-etch via tapering process in Chapter 5, can be used for applications requiring tapered via depth from 100-200 μm . The dual-etch process is limited by the etch process selectivity with respect to resist mask. A typical 10 μm thick photo resist mask would be just sufficient to etch to a depth of 200-250 μm for vias of diameter from 40-50 μm due to a selectivity of only 27-30:1 (refer to Table 5.5 in Chapter 5). However, by adding Step-1 (Bosch process), it becomes feasible to extend the tapered via depth beyond 300 μm . By using a highly selective etch process like the Bosch process with selectivity of 82-100:1 (refer to table 5.5), the overall selectivity of mask improves and allows prolonged etching to depth $> 300\mu\text{m}$. An important aspect of introducing a step-1 by a Bosch process or any other approach is that it allows us to tailor a high etch rate process without worrying about sidewall roughness. The reason is that the second etching step fully removes the sidewall roughness formed by the previous etching step and at the same time creates a tapered etch profile as shown in Fig. 6.3. Process steps 2 to 4 are similar to dual-etch process described in Chapter 5.

Figure 6.3: Illustration of a multi-step silicon via etch process technology. (a) In the first step, a Bosch etch is used to achieve ~50% of full TSV depth. (b) In the second step, a tapered reactive ion etch process is used to the remaining depth of the via. (c) In the third step, the resist mask and sidewall polymers are cleared by a wet clean process. (d) In the last step the sharp corners at the top is removed by global isotropic etch process to achieve the desired taper angle and top via dimension.

6.4.4.2 Characterization of multi-step tapered etch process

Straight etch process by the Bosch etch process has already been discussed in detail in Chapter 4. Similarly, the dual-etch via tapering process consisting of a combination of (a) Bosch (Recipe-A) and global isotropic etch process (Recipe-D) and (b) non-Bosch (Recipe-B) and global isotropic etch process (Recipe-D) has also been discussed in great detail in Chapter 5. The present work is therefore focused on combination of Bosch, non-Bosch and Global isotropic etch process as described in Fig. 6.3.

Table 6.2 summarizes the process conditions of the Bosch, non-Bosch and isotropic etch process already characterized individually in Chapter 5. Table 6.2 and Fig. 6.4 also show the taper angle achieved after each process conditions. It can easily be seen that the third etch step (Recipe-D) plays a crucial role in tuning the top via dimension and taper angle. Table 6.3 summarizes the trench depth measurement results after various etch processes (A, B, C and E) have been evaluated when etch time is increased from 45 to 120 minutes. Figure 6.5 shows the trend chart of trench depth as a function of width from 10-

100 μ m when the etch time is varied from 45 to 120 minutes.

Table 6.2: Recipe-A, B and D are three components of a 3-step tapered silicon via etch process. The table also shows the effect of each etch process on taper angle formed.

Recipe-A (Bosch)	Etch: SF ₆ : 130 sccm; O ₂ : 13 sccm; Pressure: 27-29 mtorr; Coil power: 600W; Platen power: 23 W; Cycle time: 8 sec.							
	Passivation: C ₄ F ₈ : 110 sccm; Pressure: 16-18 mtorr; Coil power: 600W; Cycle time: 5 sec [Total process time: 50 minutes]							
Recipe-B	SF ₆ : 42 sccm; O ₂ : 33 sccm; Ar: 30 sccm; Pressure: 30 mtorr; Coil power: 600W; Platen power: 30W; Etch time: 50 min. [RIE process]							
Recipe-C	Recipe-A (50 min) + Recipe-B (50 min) [Bosch + RIE Process]							
Recipe-D	SF ₆ : 130 sccm; O ₂ : 10 sccm; Pressure: 30 mtorr; Coil: 600W; Platen: 30W; Etch time: 5 min. [Global Isotropic etch]							
Recipe-E	C+D: Recipe-A (50 min) + Recipe-B (50 min) + Recipe-D (5 min)							
Trench Width (μm)	Variation of taper angle and change in slope of the trench with multi-step etch process (°)							
	Angle-A	Angle-B	Angle-C	Angle-E	Δ_A	Δ_B	Δ_C	Δ_E
10	89.2	84.8	85.4	84.1	0.8	5.2	4.6	5.9
20	89.3	86.4	86.2	84.5	0.7	3.6	3.8	5.5
30	89.2	86.8	86.9	85.6	0.8	3.2	3.1	4.4
40	89.6	87.5	87.5	85.8	0.4	2.5	2.5	4.2
50	89.7	87.5	87.6	86.1	0.3	2.5	2.4	4.0
60	89.7	88.2	87.9	86.5	0.3	1.8	2.1	3.5
70	89.6	88.3	88.2	87.0	0.4	1.7	1.8	3.0
80	89.6	88.9	88.7	87.3	0.4	1.1	1.3	2.7
90	90.2	89.0	89.2	87.7	-0.2	1.0	0.8	2.3
100	90.3	89.2	89.2	87.6	-0.3	0.8	0.8	2.4

Table 6.3: The table shows the trend of etch depth and RIE lag due to Bosch etch process as etch time is increased. It can be seen that the RIE lag increases with increase in time.

Trench width (μm)	Trench depth (45min)	Trench depth (50min)	Trench depth (60min)	Trench depth (120min)	RIE lag (45min)	RIE lag (50min)	RIE lag (60min)	RIE Lag (120min)
10	131.77	136.64	183.07	260.50				
20	143.81	150.08	201.96	287.98	12.04	13.44	18.89	27.48
30	150.38	155.54	212.44	303.98	6.57	5.45	10.48	16.00
40	153.34	159.76	218.87	314.88	2.96	4.22	6.43	10.90
50	155.63	162.37	222.87	322.28	2.29	2.61	4.00	7.40
60	157.08	165.64	226.17	325.43	1.45	3.27	3.30	3.15
70	158.54	167.16	228.14	330.35	1.46	1.52	1.97	4.93
80	159.38	167.59	229.55	333.40	0.84	0.43	1.41	3.05
90	159.38	168.51	230.99	335.75	0.00	0.92	1.44	2.35
100	159.38	169.30	231.82	342.23	0.00	0.78	0.83	6.48

Figure 6.4: (a) Trend chart showing the variation of taper angle as trench/via width is varied from 10-100 μ m. It can be seen that by adding the third etch step (Recipe-D) the slope increases by as much as 1-2 degrees. (b) Chart shows the trend of change in angle for when trench width varies from 10-100 μ m for recipes A to E.

Figure 6.5: (a) Trend chart due to Recipe-A (Bosch) showing the variation of etch depth as a function of etch process time for trenches from 10-100 μ m. (b) Chart shows the trend of RIE lag as trench width varies from 10-100 μ m when etch time is increased.

In Fig. 6.6 the etch depth and RIE lag has been plotted as a function of the trench width for each combination of the multi-step etch process A-E. It can be seen that the RIE lag is matching well for an etch time of 50 minutes for both the Bosch and non-Bosch etch

process. For this condition, it is also possible to achieve etch depth from 300-350 μm for 10-100 μm wide trench/vias. An important point from Fig. 6.6(a) is that while the etch rate of recipe-B (a non-Bosch process) is 30-35% higher than recipe-A (Bosch process), its selectivity to resist is almost 3 times lower than recipe-A (See Table 6.6).

Table 6.4: Effect of each etch process recipe (A-E) on trench depth achieved and the impact on RIE lag due to each recipe condition.

Trench (μm)	Effect of multi-step etch process on trench/via depth and RIE lag							
	Depth (A)	RIE lag (A)	Depth (B)	RIE lag (B)	Depth (C)	RIE lag (C)	Depth (E)	RIE lag (E)
10	136.6		194.0		291.6		288.0	
20	150.1	13.4	204.7	10.7	312.2	20.6	309.4	21.4
30	155.5	5.5	212.5	7.8	328.5	16.4	324.5	15.1
40	159.8	4.2	217.3	4.8	340.2	11.7	335.9	11.4
50	162.4	2.6	220.1	2.8	348.8	8.6	345.6	9.7
60	165.6	3.3	223.7	3.6	356.8	7.9	352.8	7.2
70	167.2	1.5	226.3	2.7	362.1	5.4	357.7	4.9
80	167.6	0.4	228.1	1.7	365.2	3.0	361.9	4.2
90	168.5	0.9	229.5	1.4	370.1	5.0	367.5	5.6
100	169.3	0.8	231.4	1.9	373.4	3.3	371.7	4.2

Figure 6.6: (a) Chart shows variation of trench depth as trench width is varied from 10-100 μm . The depth due to recipe-A and B is not same as A+B. (b) Chart shows the trend of RIE lag when trench width varies from 10-100 μm for recipes A to E. The RIE lag changes significantly for trench widths below 50 μm .

Table 6.5: Effect of each etch process step on trench width at the top.

Trench width (μm)	Trench width at the top in μm after etch with recipes (A-E)				Etch rate (ER) of each of the recipes (A-E)			
	A	B	C	E	ER-A	ER-B	ER-C	ER-E
10	17.2	54.5	63.4	73.9	2.7	3.9	2.9	2.7
20	27.4	62.3	71.35	80.25	3.0	4.1	3.1	2.9
30	36.6	73.0	82.3	90.9	3.1	4.3	3.3	3.1
40	46.3	82.4	93.1	100.65	3.2	4.3	3.4	3.2
50	56.0	90.9	101.6	108.2	3.2	4.4	3.5	3.3
60	66.1	101.7	111.6	117.8	3.3	4.5	3.6	3.4
70	74.9	112.2	120.45	129.85	3.3	4.5	3.6	3.4
80	84.6	121.4	130.3	139.7	3.4	4.6	3.7	3.4
90	94.5	129.7	139	149.5	3.4	4.6	3.7	3.5
100	103.4	141.8	150.7	157.95	3.4	4.6	3.7	3.5

Figure 6.7: (a) Chart showing variation of top trench width as trench width is varied from 10-100 μm . The trench width variation is linear for all recipes conditions. (b) Chart shows the trend of Etch rate when trench width varies from 10-100 μm for recipes A to E. The etch rate drops significantly from recipe A to E due to drop in etch depth (Refer to Chapter 5, Section 5.5.3).

Table 6.5 and Fig. 6.7(a) shows the amount of trench/via tapering or enlargement of the top dimension is possible when etched with recipe-A to E. It may be noticed that the top width increases linearly with mask width. Figure 6.7(b) shows that the overall etch rate of recipe-C and E is lower than recipe-B. This can be due to reduction in the depth due to silicon erosion during global isotropic etch process and also due to the RIE lag

effect with increasing etch depth as observed from Table 6.3 and Fig. 6.5.

6.4.4.3 Multi-step etch process results

Figure 6.8 shows SEM cross sectional micrographs of 50 μ m diameter vias etched with the multi-step etch process to a target depth in the range of 290-310 μ m in four stages as described in Fig. 6.3. Figures 6.8 (a) to (c) also show the gradual evolution of a vertical via profile (90°) to become a tapered via profile with a taper angle of 84°.

It can be observed that the rough sidewall scallops due to the Bosch etch process and the sharp top curvature due to the non-Bosch etch process shown in Figs. 6.9(a) and (b) disappears completely after the global isotropic etch (Recipe-D) is performed as shown in Fig. 6.9(c). Based on the experimental results, the value of the curvature varies between 1-5 μ m depending on the diameter of the diameter of the via. It can also be seen from Fig. 6.10 that the rough edges of the vias due to resist residues during thick resist lithography and due to the chemically aggressive non-Bosch etch process can make the via edges very rough and irregular. But after the third etch step, the rough edges are smoothened and rounded as seen in Fig. 6.10(c).

It may be noted that there is a trade-off between the maximum resist thickness that can be used and the smallest pattern it can resolve in any lithography system. Thick resist (> 10 μ m thickness) can sometimes result in under-exposure or underdevelopment which makes the edges look rough as shown in Fig. 6.10(a). In case of the Bosch or non-Bosch etch process, usage of high flow rate of SF₆ or high process pressure, results in undercut below the mask which makes the edges irregular as shown in Fig. 6.10(b). Thus, by using a third etch step (global isotropic etch), the roughness is effectively removed as shown in Fig. 6.10(c).

Chapter 6 - Integration of tapered via technology for silicon carrier fabrication

Figure 6.8: SEM cross-sectional results of 300 μm deep via formed by multi-step etch process described in Fig. 6.3. (a) Cross-sectional results after first etch by the Bosch process when 50 μm diameter vias are etched to a depth in the range of 150-160 μm . (b) Tapered etch profile formed after second etch by a controlled isotropic etch process. (c) Final tapered via profile after the sharp corner at the top is removed by a global isotropic etch process.

Figure 6.9: SEM micrographs showing via at the top after performing the via tapering process on vias formed by (a) Bosch and (b) non-Bosch etch process.

Figure 6.10: Optical microscope images showing top-view of vias after each stage of the multi-step via tapering process.

Figure 6.11 shows SEM cross-sectional micrographs of 100 and 200 μm deep TSV by using only the non-Bosch etch process and global isotropic etch process. As the depth is below 200 μm, the first etch step by Bosch etch process is skipped. Figures 6.12 (b) and (c) shows the tapered via results achieved with 50 μm diameter vias with the multi-step etch process for a depth of 200 μm and 300 μm respectively. The top dimension of 100 μm has been achieved by using the third etch recipe (Recipe-D) by adjusting the etch time. Table 6.6 summarizes the process characterization results achieved by using 60 μm trench/via structure.

Figure 6.11: SEM micrographs of 100 μm and 200 μm deep vias etched by dual-etch process which is part of the generic multi-step tapered via etch process described in Fig. 6.3.

Figure 6.12: (a) SEM micrographs of 200µm deep via etched by dual-etch process. (b) SEM micrograph of 200µm deep via etched by Multi-step etch process to achieve the same target via geometry. (c) Image of 300µm deep vias etched by multi-step etch process to achieve similar top and bottom geometry of the via.

Table 6.6: Summary of via etch process characterization results of each recipe in a multi-step process. Recipe-A and B are etched for 50 min each.

Multi-step etch process parameters	Recipe-A	Recipe-B	Recipe-C (A+B)
Via diameter at top of 60µm via (µm)	61.87	85.63	98.6
Via diameter at bottom of via (µm)	63.48	72.5	66
Depth of via (µm)	155.09	192.5	300.8
Photo Resist Loss after etch (µm)			
Centre of wafer	1.53	6.81	8.21
Edge of wafer	1.88	6.97	8.67
Etch rate Selectivity (Si:Resist)			
Centre of wafer	108.04	33.19	43.40
Edge of wafer	88.20	31.92	41.17
Silicon Etch Rate (µm/min)			
Centre Trench	3.31	4.52	3.56
Edge Trench	3.32	4.45	3.57
Edge Via	3.10	3.85	3.01

6.4.5 Development of Low-temperature dielectric deposition

After the deep silicon vias have been formed, the vias are required to be electrically isolated by a uniform dielectric isolation layer. Normal process temperature for dielectric

deposition by plasma enhanced chemical vapor deposition (PECVD) is 350-400°C. However, to prevent stress from accumulating in the silicon carrier wafer, a low-temperature process was developed. A low-temperature PECVD deposition process is needed not only for through silicon via isolation but also for dielectric isolation between redistribution layers on both sides of the carrier substrate. The temperature for the deposition process was chosen as 250 °C as it is below the glass transition temperature of polymers glue used for thin wafer handling.

The proposed PECVD SiO₂ process was developed in Plasmatherm-790 dual chamber deposition/Etch system. The dielectric thickness used for the evaluation is 2.0µm. The recipe conditions used and the process characterization results achieved is summarized in Fig. 6.13. The sidewall deposition thickness at the top, middle and bottom of 235 µm deep tapered silicon via was measured by a Jeol SEM (JSM6700F) after completing the copper seed metallization and copper via filling by electroplating process. To enhance the resolution of the SEM image, the cross-section sample was lapped and polished in fine grain slurry and dipped in buffered oxide etchant (BOE) for 10 seconds. The short BOE etch improves the contrast between the dielectric layer and the background. It can be seen from Fig. 6.13 that there is sufficient dielectric coverage of sidewalls of the TSV structure. It can also be seen that the electroplated copper is void-free. It can be seen that the minimum thickness achieved is 0.35-0.45µm while the maximum thickness achieved at the top sidewall is 0.7 to 0.8µm which is sufficient for good electrical isolation for TSV application.

Figure 6.13: (a) SEM cross-sectional micrograph of void-free electroplated copper via formed after the via sidewalls are isolated by low-temperature silicon dioxide. (b-d) SEM micrographs of higher magnification view of sidewall isolation oxide at top, middle and bottom of the via.

Table 6.7: Summary of low-temperature deposition process.

Deposition parameters	Process settings
Temperature	250 °C
Pressure	900 mTorr
Power	20 Watts
SiH ₄	6 sccm
N ₂ O	400sccm
N ₂	150 sccm
Process characterization results	
Deposition rate	569 Å/min
Uniformity	5.6%
Oxide thickness (top)	1.9-2.1 μm
Oxide thickness (middle)	0.45-0.55 μm
Oxide thickness (bottom)	0.35-0.45 μm

6.4.6 Copper via-filling process

According to the curvature enhanced accelerator coverage (CEAC) mechanism proposed for copper damascene electroplating process [182, 183], the void-free filling of high aspect ratio vias occurs in following steps:

- a) Adsorption of additives and nucleation of electroplated copper on PVD films at a high over potential;
- b) Conformal growth of copper during initial deposition and at low current densities
- c) Bottom-up filling as result of accelerator and its by-product accumulation due to rapid decrease in the surface area, especially at the bottom corners of narrow features and suppressor replacement by accelerating species and
- d) Bump formation & planarization of surface due to replacement of accelerator with leveler and suppressor.

The copper electroplating solution for deep via-filling application can be either copper sulfate or cyanide-based. Typical composition of an electrolyte includes CuSO_4 , H_2SO_4 and Cl^- , additives including suppressor (Carrier), accelerator (Brightener) and leveler. The electroplating system used for the via filling is a research system from Rena. The standard plating solution from Atotech was used for the plating process. Figures 6.14 and 6.15 show the copper electroplating results achieved with 200 μm and 300 μm deep tapered vias. It can be seen that there is no voids in the vias. Plating was done at room temperature by using following plating conditions and process sequence:

1. Pre-wetting for 3mins with 6 volume % of Spherolyte C1, rinse in de-ionized water for 5 minutes and dip in diluted accelerator solution for 3 minutes.
2. Rena Plater rotation speed of 25 rpm at a flow rate of 20 L/min by DC plating

3. Plating is done by DC plating method with a current of 0.3 A for 30~35 hours.

Figure 6.14: (a) SEM micrograph of 200 μ m deep tapered vias filled with electroplated copper after multi-step tapered via etch process described in Fig. 6.3.

Figure 6.15: (a) SEM micrograph of 300 μ m deep tapered via formed by multi-step tapered via etch process described in Figure 6.3. (b) Optical microscope image showing void-free electroplated copper vias.

6.4.7 Copper CMP and wafer back-grind

After the copper via-filling, the over-plated copper is removed by chemical mechanical polishing. After Cu-CMP process, further metallization layers are processed

before attaching a temporary handle wafer on the front-side and then doing a back-grind and polishing to expose the through silicon copper vias. A wet polishing is a standard process after back-grinding to remove any defects generated due to back-grinding. The same tool has been used for chemical mechanical polishing (CMP) with suitable high etch rate slurry. It may be noted that an appropriate de-ionized water cleaning step is done to remove the slurry residue. A soft-bond back-grinding wheel was used for back-grinding copper and silicon together to expose the through silicon vias. A rough grind was first performed to remove major part of the silicon. Then soft grinding wheel was used to expose the copper vias. A summary of the wafer back-grinding and polishing parameters is summarized in Table 6.8. Figure 6.16 shows cross-sectional optical image of silicon carrier after Cu-CMP, wafer thinning and post-metallization.

Figure 6.16: Optical image of cross-sectioned silicon carrier wafer showing a void-free electroplated copper vias. The silicon carrier wafer was back grinded and polished to expose the copper vias on both sides.

The completed silicon carrier wafer is then assembled on board and tested for electrical continuity and via resistance [32, 182]. The carriers were tested for thermal cycle reliability condition -40 °C to 125 °C upto 1000 cycles. The via electrical resistance was monitored as part of the daisy chain connecting chip1, chip 2 & chip 3 to the PCB (see Fig-6.2). The via resistance did not change and the cross section of the via showed no failure. The through silicon via continuity test and the via reliability test results are summarized in Table-6.9.

Table 6.8: Process parameter for via exposure by back-grinding and polishing.

Process conditions	Rough grind	Via exposure
Spindle speed	3200 rpm	2800 rpm
Chuck Table Speed	250 rpm	150 rpm
Cutting depth	400 micron	100 micron
Feed rates	100 $\mu\text{m}/\text{min}$	200 $\mu\text{m}/\text{min}$
Mesh size	# 325	# 600

6.5 RESULTS AND DISCUSSION

It can be seen from trend chart in Fig. 6.4(a) that the taper angle due to Recipe A is close to 90° as expected in a Bosch etch process. The taper angle due to Recipe B and C shows that there is no significant change. This shows that the tapered profile is mainly influenced by the Recipe-B. It can also be seen that the taper angle can be further increased by 1-2 degree by adding global isotropic etch process (Recipe-D) for 5 minutes (See Fig. 6.4(b)). Similarly, it can be seen from Table 6.5 and Fig. 6.7 that the top width of trenches formed due to Recipe-A can be linearly enlarged by adding Recipe-B and Recipe-D without any impact on bottom dimension. It can be explained that this effect is mainly due to diffusion limited chemical etching mechanism in process B and D.

It may be noticed from Table 6.3 and Fig. 6.5(b) that the RIE lag effect due to

Recipe-A is significant for trench/via widths below 60 μm due to inability of the ions and neutral flux to reach the bottom due to increase in profile shadowing effects with increasing aspect ratio [141]. Similarly, it can be noticed that with increase in the etch time and etch depth, the RIE lag is increased significantly for trench widths smaller than 60 μm .

The tapered via etch results achieved with the multi-step etch process is shown in Fig. 6.12 (b) and (c) for 200 μm and 300 μm deep vias respectively. Figure 6.11 shows the results achieved for 100 μm and 200 μm deep vias respectively by using only the dual-etch process. In both these methods, it can be seen that the required taper angle within 83-87° has been achieved. An important point to be noted from the multi-step etch process characterization results summarized in Table 6.6 is that Recipe-B (a non-Bosch etch process) has only one third as much selectivity to the photo resist as compared to the Bosch etch process (Recipe-A). The main reason for this difference is that Recipe-B have higher platen power of 30W compared to only 23W used in the Bosch etch process (Recipe-A). Further, the SF₆ to O₂ ratio in Recipe-A is 10 compared to 1.3 in Recipe-B which makes it less chemically aggressive. Thus the high reactivity of Recipe-B and high power makes it less selective. It can also be seen from Table 6.6 that the resist remaining is only 1-1.5 μm which is barely sufficient to etch another 20-30 μm with Recipe-B. But by adding Recipe-A before Recipe-B, it has been shown that with the same resist thickness of 10 μm it is possible to etch 300-350 μm deep vias as shown in Fig. 6.15.

It has been shown from the chart in Fig. 6.6(b) that the RIE lag is quite close to each other when the etch time of the Bosch and non-Bosch etch process is same. It is important that the RIE lag be kept as low as possible to minimize too much variation amongst different via dimensions. It can also be seen that when both processes are

combined as in Recipe-C, the RIE lag increases further due to increase in the aspect ratio which leads to ion shadowing effect [141, 167-169].

Figures 6.9 and 6.10 show that after etching with Recipe-A, B or C, the edges are very rough. But after the third etch step with Recipe-D, the etch profile becomes more tapered and smoother. It can be seen that the sidewall roughness due to the Bosch process is $< 200\text{nm}$ whereas the sidewall curvature due to second etch step with Recipe-B is $5\text{-}6\mu\text{m}$ which is more severe. This difference is due to high chemical reactivity of Recipe-B and also due to continuous etch unlike the short isotropic etch cycles in case of Recipe-A. It can be observed from Figs. 6.11 and 6.12 that the third etch step (Recipe-D) has been used to adjust the top via diameter to achieve the required amount of slope. The third process step also removes the curvature and round-off the top corner.

Table 6.9 summarize the electrical continuity test done at time zero and after thermal cycling. It can be seen that there is no significant change in the continuity resistance after subjecting the samples to thermo-mechanical reliability test (-40 to 125°C) for 250, 500, 750 and 1000 cycles. The via resistance includes the through silicon interconnect structures in series with solder joints used for assembling the test dies and the carrier on the board. It may be noted that the UMB pads provided in the silicon carriers have been designed for assembling chip-1, 2 and 3 on to silicon carrier-1 and 2. The solder joints joining chip-1, 2 and 3 were individually tested for continuity through the TSV in the carrier on which it is assembled. The TSV continuity measurements were done from the test pads provided on the organic substrate on which the stacked carriers are assembled.

Table 6.9: Through silicon via continuity test results.

Chain resistance	At T=0 (Ω)	250 cycles (Ω)	500 cycles (Ω)	750 cycles (Ω)	1000 cycles (Ω)
Chip 1 to board	23.9	23.9	24.3	24.3	24.3
Chip 2 to board	21.3	21.5	21.9	22.3	22.3
Chip 3 to board	25.2	25.5	25.9	25.9	26.0

For measuring the TSV resistance without solder joint, the adjacent TSV structures that were interconnected on the bottom side was electrically probed from the top side. To improve the accuracy of the resistance measurement Kelvin (4-wire) resistance measurement was done. The average TSV resistance was measured to be 0.10 Ohms per via.

6.6 CONCLUSION

A generic multi-step tapered via etch technology was demonstrated in this work. It has been showed that the vertical etch profile normally achieved by the Bosch etch process can be tapered by tailoring additional reactive ion etch processes to achieve high degree of process control and flexibility by independently controlling each stage of the process. The limitations of single step and dual-etch process was studies and it has been shown that due to the limitation of selectivity to photo resist mask, the multi-step via tapering process has a significant advantage in extending the via depth beyond 300 μm .

The multi-step via etch process was subsequently integrated with a low-temperature dielectric deposition, metallization and copper electroplating process and it was shown that a void-free copper via-filling could be achieved with adequate dielectric coverage on the sidewalls and bottom of the via. Based on the tapered TSV process, a fully integrated silicon carrier was fabricated and assembled with test dies. Thermal cycling (-40

to 125°C) and electrical continuity tests showed insignificant degradation in the electrical resistance of the through silicon interconnects. The results presented thus meets a critical requirement for forming through-silicon copper interconnection for 3D system in packaging application. It can also be concluded that a high aspect ratio tapered via with aspect ratio of >3 can be achieved by a void-free copper filling.

Chapter 7

Study of electrical conduction in deep silicon via structures for TSV application

7.1 INTRODUCTION

TSV being an electrical interconnection from the front to the backside of the silicon substrate, it is essential that it provides a reliable and low-resistance interconnection with minimum leakage conduction between TSVs. Most of the published work in the area of 3D integration have investigated the performance of the TSVs as an electrical interconnect by integrating with test devices or functional ICs. Knickerbocker *et al.* have done extensive TSV characterization by designing test vehicles with integrated passive components for studying RF signal integrity using various 3D integration approaches [89]. Andry *et al.* performed further investigation with various TSV materials such as tungsten, copper, copper composite and solder and evaluated its via resistance, electrical yield, and current-carrying capacity [90]. Pak *et al.*, of Terahertz Interconnection and Packaging Laboratory have conducted electrical characterization of TSV with different structural parameters such as via pitch, height and dielectric thickness. It was shown that as the resistivity of silicon increases, it is more effective for the DC and high frequency leakage current to be blocked between signal and ground TSV [91]. Navas *et al.* have assembled test chips in silicon carriers and then vertically integrated them to check the performance of TSV and solder-joints when subjected to thermal cycles [161, 165, 182].

In the present work, extensive and detailed characterization has been done to study the influence of deep silicon via profile and sidewall roughness on the leakage current through isolation dielectric layer in deep silicon via structures. Possible conduction mechanism responsible for the leakage between deep silicon via structures of various sidewall profiles are proposed using the classical transport models [184]. Our previous experimental work presented in Chapter 4 has shown that the sidewall roughness due to Bosch etch process results in increase in the electrical leakage between deep silicon via structures under thermal stress [23, 25]. In this work, additional experiments have also been conducted to study the leakage conduction mechanisms between vias with various profiles and sidewall roughness.

7.2 CONDUCTION MECHANISMS IN DIELECTRIC

7.2.1 Fowler-Nordheim tunneling

Though insulators are poor conductors of electricity, they are capable of limited conduction under various circumstances. An understanding of various conduction mechanisms will provide insight in interpreting the behavior of the insulators in TSV structures. The most common form of current conduction in insulators is by tunneling mechanism(s). This mode of current conduction is under the influence of high electric field across the insulator and should therefore be independent of temperature [184]. This conduction mode is also known as Fowler-Nordheim (FN) tunneling mechanism expressed by following equation:

$$I = K_1 V^2 \exp\left(\frac{-b}{V}\right) \quad \text{----- (7.1)}$$

$$\ln\left(\frac{I}{V^2}\right) = -b\left(\frac{1}{V}\right) + \ln K_1 \quad \text{----- (7.2)}$$

where,

V is the voltage across the insulator (i.e., typically SiO_2),

I is the current through the insulator

T the temperature of the insulator and

K_I and b are constants.

It can be seen that this mode of conduction results in a linear plot between $\ln(I/V^2)$ and (I/V) with a negative slope ($-b$) and a y-intercept of $\ln K_I$. Fowler-Nordheim tunneling conduction in SiO_2 is reported to occur at very high electric field in the range of 7-8 MV/cm [185, 186]. This form of conduction is expected in defect-free insulators. Any defect in the SiO_2 or the silicon- SiO_2 interface can introduce traps in the dielectric which causes other forms of conduction mechanisms to creep-in as explained below. Thus, FN effect can be used to explain the conduction behavior in a TSV dielectric deposited over smooth sidewall as compared to dielectric deposited over a defective surface formed by Bosch or RIE etch process.

7.2.2 Schottky Emission

Thermionic or Schottky Emission (SE) is another form current conduction in insulators [186]. Thermal emission over the barrier lowered by a strong electric field is governed by the Richardson-Schottky (RS) relation [187]:

$$I = K_2 T^2 \exp \left[\frac{q}{kT} (a\sqrt{V} - \Phi_B) \right] \quad \text{----- (7.3)}$$

$$\ln \left(\frac{I}{T^2} \right) = \left(\frac{qa\sqrt{V}}{k} - \frac{q\Phi_B}{k} \right) \left(\frac{1}{T} \right) + \ln K_2 \quad \text{----- (7.4)}$$

where,

T the temperature of the insulator

k is Boltzmann's constant

q is elementary charge of electron.

Φ_B is the potential barrier height of the insulator which an electron has to cross to conduct through the insulator. K_2 , and a are constants.

For a fixed voltage in low to medium voltage or electric field range, a linear plot is expected between $\ln(I/T^2)$ and $(1/T)$. Similarly for a fixed temperature, the above equation can be rewritten as follows:

$$\ln(I) = \left(\frac{qa}{kT} \right) \sqrt{V} + \ln(K_2 T^2) - \left(\frac{q\Phi_B}{kT} \right) \quad \text{----- (7.5)}$$

From the above modified equation it can be seen that for a fixed temperature (T), the plot between $\ln(I)$ and square root of V will be linear if the conduction mode is by Thermionic or Schottky emission. As the temperature increases the intercept will increase or shift upwards. Thus temperature dependence in the leakage current in TSV may indicate a SE type of conduction.

7.2.3 Frenkel-Poole emission

When a dielectric layer has lot of process induced defects, it creates several charge trapping sites in the dielectric. This causes the electrons from adjoining metal or semiconductor to get trapped in these trap sites also known as states. The Poole-Frenkel effect describes how, in a large electric field, the electron gets sufficient electrical potential energy to sweep these trapped electrons into the conduction band of the dielectric.

Similarly, the trapped electrons can also be swept if sufficient thermal energy is given under a lesser electric field [188-190]. The conduction behavior can be explained by following equation:

$$I = K_3 V \exp \left[\frac{q}{kT} (2a\sqrt{V} - \Phi_B) \right] \quad \text{----- (7.6)}$$

$$\ln \left(\frac{I}{V} \right) = \left(\frac{2qa}{kT} \right) \sqrt{V} + \left(\ln K_3 - \frac{q\Phi_B}{kT} \right) \quad \text{----- (7.7)}$$

where,

K_3 and a are constants.

It can be seen from this equation that a plot of $\ln(I/V)$ versus square root of V will show a linear behavior for a given temperature when the voltage or field strength is high. When the temperature is increased, one can expect the y-intercept to increase and the slope to decrease with temperature (T). The Frenkel-Poole (FP) effect can be used to explain the impact of defective dielectric layer due to Bosch or RIE etch process.

7.2.4 Ohmic conduction

This form of conduction is similar to an ideal resistive conduction of any material through which current is passed. In case of dielectric, conduction takes place only when the potential is above the band-gap of the SiO_2 . An Ohmic behavior can be seen only in low electric field regime. When the field is increased, it can introduce other modes of conduction like PF or FN [184]. The Ohmic conduction is expressed by following equation:

$$I = K_4 V \exp\left(\frac{-c}{T}\right) \quad \text{----- (7.8)}$$

where K_4 and c are constants.

From the rewritten equation it can be seen that the plot of I versus V will show a linear behavior with a positive slope. The conductance or the slope is expected to increase with temperature. This behavior is limited to semiconductor and insulator where electrons are provided energy to jump into conduction band. In case of a metal, as electrons are already in conduction band, an increase in temperature shows an increase in collisions between the electrons which results in decrease in conductance.

7.2.5 Ionic conduction

Ionic conduction is similar to diffusion process under electric field. In case of insulator, the ionic conduction decreases with time as the carrier injection into the insulator is not sustainable due very high barrier height [184]. The ionic conduction can also be thermally activated in the dielectric. Ionic conduction can thus be due to thermally activated hopping of ions over an energy barrier under the influence of electric field or potential expressed by following equation:

$$I = K_5 \left(\frac{V}{T}\right) \exp\left(\frac{-K_6}{T}\right) \quad \text{----- (7.9)}$$

where K_5 and K_6 are constants

7.2.6 Space charge limited conduction [184, 191-193]:

This model typically applies when charge carriers have been emitted from some region of a solid under applied electric field. Space charges can occur within solid or liquid

dielectrics that are stressed by high electric fields. Space charge can result due (a) ionization of species within the dielectric, (b) charge injection from electrodes and (c) trapping sites in dielectric due to defective silicon surface or dielectric deposition process.

The current is given by the equation:

$$I = K_7 V^2 \quad \text{-----} \quad (7.10)$$

where K_7 is a constant. Table 7.1 summarizes all the conduction models discussed in this section. The second column represents the conduction mechanisms in linear form which will be used in the following sections.

Table 7.1: Summary of electrical conduction processes in insulators [7].

Process	Expression	Linear expression
Fowler-Nordheim tunneling [10, 11]	$I = K_1 V^2 \exp\left(\frac{-b}{V}\right)$	$\ln\left(\frac{I}{V^2}\right) = -b\left(\frac{1}{V}\right) + \ln K_1$
Schottky Emission (SE or RS) [11, 12]	$I = K_2 T^2 \exp\left[\frac{q}{kT}(a\sqrt{V} - \Phi_B)\right]$	$\ln(I) = \left(\frac{qa}{kT}\right)\sqrt{V} + \ln(K_2 T^2) - \left(\frac{q\Phi_B}{kT}\right)$
Poole-Frenkel emission [13-15]	$I = K_3 V \exp\left[\frac{q}{kT}(2a\sqrt{V} - \Phi_B)\right]$	$\ln\left(\frac{I}{V}\right) = \left(\frac{2qa}{kT}\right)\sqrt{V} + \left(\ln K_3 - \frac{q\Phi_B}{kT}\right)$
Ohmic [7]	$I = K_4 V \exp\left(\frac{-c}{T}\right)$	$I = K_4 V \exp\left(\frac{-c}{T}\right)$
Ionic conduction [7]	$I = K_5 \left(\frac{V}{T}\right) \exp\left(\frac{-K_6}{T}\right)$	$I = K_5 \left(\frac{V}{T}\right) \exp\left(\frac{-K_6}{T}\right)$
Space charge limited [16-18]	$I = K_7 V^2$	$\ln(I) = \ln(K_7) + 2\ln(V)$

Φ_B =barrier height, V =Voltage across the insulator, I = Leakage current flowing through the insulator, T = Temperature of the insulator, k is Boltzmann's constant, q is elementary charge of electron and a, b, c, K_1 to K_7 are constants.

7.3. TEST VEHICLE DESIGN AND FABRICATION

It has been shown in our previous work in Chapters 4 and 5 that the DRIE process plays a significant role in defining the sidewall roughness and the via profiles. The main objective of this study is to investigate the influence of the sidewall roughness and via

profile on the conduction mechanism in deep silicon via structures. A detailed overview of various types of conduction mechanisms have already been given in section 7.2. For studying the deep silicon vias with tapered via profile, a test vehicle was designed with four circular vias per chip which are separated by 250 μm from each other. The via geometry was selected carefully so that it is the typical range for silicon carrier based packaging [79].

In a silicon carrier based 3D-package, the silicon substrate is usually not grounded as both sides and the TSV are electrically isolated with an insulating layer of silicon dioxide. For this reason, in the present work, it was decided to focus mainly on leakage measurements between via to via and the various etch process related factors affecting its performance. The proposed test vehicle is shown in Table 7.2. The process flow requires only a two masking and etching processes. The first mask is for patterning and etching circular vias in STS with different recipes to achieve 4 different profiles (b) to (e) as illustrated in Fig. 7.1. This process is followed by global metallization and patterning and wet etching to form large test pads around the vias as shown in Fig. 7.1. Each wafer represents different process conditions to study the impact of profiles and sidewall roughness on the leakage current.

To study the effect of sidewall roughness and via profile, five recipes have been created with vertical, reentrant and positively tapered profiles as summarized in Table 7.3. A depth of close to 100 μm has been targeted with 50 μm via diameter in mask. A standard 10 μm thick positive photoresist mask has been used. As the proposed study does not require solid electroplated copper via, the via metallization process has been simplified in the test vehicle fabrication by using only sputtering deposition process as the aspect ratio of the via is only 2.

The experimental results after via etch and metallization are shown in Fig. 7.2. The SEM cross-sectional micrographs of the sidewall roughness due to recipes A1 to E1 are shown in Fig. 7.3. The dielectric thickness and metal thickness variation at top and bottom of the TSV structure in each of the five wafers fabricated has been summarized in Table A-8 attached in the Appendix A.

Figure 7.1: (a) Illustration of top view of test vehicle designed to evaluate the leakage between adjacent vias of different etch profiles like (b) tapered and smooth profile, (c) straight and scalloped sidewall, (d) tapered and curved profile and (e) scalloped and reentrant profile with larger scallop size.

Figure 7.2: Optical images of the cross-section of five silicon via samples etched with different recipes (a) A1, (b) C1, (c) F1, (d) B1 and (e) E1 respectively as shown in Table 2 and 3.

Figure 7.3: SEM cross-sectional micrographs of samples etched with Recipe (a) A1, (b) C1, (c) B1 and (d) E1 respectively. The roughness measured in each samples is also shown. It can be seen that the scallops is very high for Recipe C1 (see (b)) compared to A1 (see (a)). The results shown in (d) show that the curvature formed by RIE process shown in (c) is removed after global isotropic etch process D1.

Table 7.2: Process flow used for testing leakage current due to various via profiles.

Step	Stage	Step Description
1	Wafer start	Test wafers [0-100Ω-cm; <100>, 200 mm dia.]
2	Via lithography	Via formation on front side of wafer
3	DRIE	DRIE etch in STS with a target etch depth : 90-110μm
4	Wet strip of resist	Solvent clean with PRS3000 for 30 min.
5	Plasma resist strip	Photo Resist Wet strip in PRS3000 strip solution for 30 min. @ 65 °C
6	Post strip clean	Deionized water rinse and spin rinse dry
7	Via tapering	Global isotropic etch in STS DRIE etcher for 5 min.
8	Clean	Wet clean
9	Isolation Oxide deposition	2 μm isolation TEOS oxide deposition in Novellus PECVD system
10	Metallization	1000A Ti + 2μm Cu sputtering in Balzer PVD system
11	Dry resist film lamination	20μm Dupont dryfilm resist thickness; Roller temperature: 100-110 °C; 28psi ; Roller speed: 1m/min; Post lamination bake @ 100 °C, 1min
12	Dry-film lithography	Expose and develop dry film for Pad formation
13	Metal etch	Wet etch 2μm Cu + 1000A Ti
14	Dry film strip	Dry film strip with agitation in wet bench
15	Leakage current testing	Test with a voltage sweep from 0-10V

Table 7.3: Recipes used for the evaluation of vias with different profiles and sidewall roughness.

Recipe-A1 (Bosch)	Etch:SF ₆ : 130 sccm; O ₂ : 13 sccm; Pressure: 27-29 mtorr; Coil: 600W; Platen: 23W; 8 sec.	Fig 7.2 (a) & Fig 7.3 (a)
	Pass:C ₄ F ₈ : 110 sccm; Pressure: 16-18 mtorr; Coil: 600W; 5 sec. (Total Process Time: 30 min)	
Recipe-B1 (non-Bosch)	SF ₆ :42 sccm; O ₂ :33 sccm; Ar:30 sccm; Pressure: 30 mtorr; Coil: 600W; Platen:30W. (Etch time: 32 min.) [RIE process]	Fig 7.2 (d) & Fig 7.3 (c)
Recipe-C1 (Bosch)	Etch:SF ₆ : 130 sccm; O ₂ : 13 sccm; Pressure: 31-33 mtorr; Coil: 600W; Platen: 30W; 10 sec.	Fig 7.2 (b) & 7.3(b)
	Pass:C ₄ F ₈ : 110 sccm; Pressure: 25-28 mtorr; Coil: 600W; 4 sec. (Total Process Time: 25 min)	
Recipe-D1	SF ₆ : 130 sccm; O ₂ : 10 sccm; Pressure: 30 mtorr; Coil: 600W; Platen: 30W; Etch time: 5 min. [Global Isotropic etch]	Fig 7.3 (e)
Recipe-E1	B1+D1: Recipe-B1 (32 min) + Recipe-D1 (5 min) [Dual-etch via tapering process]	Fig 7.2 (e) & Fig 7.3 (d)
Recipe-F1	C1+D1: Recipe-C1 (25 min) + Recipe-D1 (5 min) [Dual-etch via tapering process]	Fig 7.2 (c)

7.4 ELECTRICAL CHARACTERIZATION

Agilent 4155C Parameter Analyzer and Signatone manual wafer prober were used to perform the electrical measurements on the finished samples. All the five processed samples were tested at 5 sites (i.e top, bottom, left, right and centre) of the wafer and average value was used for detailed analysis. The samples were tested from 0-40 Volts in steps of 0.5V. The measurements were done at room temperature of 22 °C and at 100 °C to investigate effect due to temperature. The main motivation for this study is to examine the influence of TSV profile and sidewall defects on TSV leakage behavior and correlate it with well known dielectric conduction mechanisms (See Table 7.1). It may be noted from Table 7.1 that the second column expresses various conduction mechanisms in linear form with the slope showing temperature dependence. Hence, the leakage measurements are performed at 22 °C (Room temperature) and 100 °C to look for a change in the

temperature-dependent slope. The complete measurement database has been appended in Appendix A (See Table A-7). All the measurement results shown in Figs. 7.4 to 7.13 have been plotted with respect to the parameters derived from various conduction models discussed in Section 7.2.

7.5 RESULTS AND DISCUSSIONS

7.5.1 Effect of recipe-A1:

Figure 7.4(a) shows the normal I - V plot measured at room temperature (22 °C) and at 100 °C. The plot of $\ln(I/V)$ versus square-root of V shows a linear trend in the range of 20-40V with a positive slope. It can also be seen that the slope decreases with increasing temperature. This trend clearly correlates with Poole-Frenkel (PF) conduction model which is primarily a trap-assisted conduction model due to defects in dielectric layer.

Based on the rough sidewall due to the Bosch etch process shown in Figs. 7.3(a) and 7.5, it can be explained that traps are likely to be formed in the dielectric. It can also be seen that rough sidewall prevails both in the top and the bottom of the via. Figure 7.4(c) shows that the slope of the $\ln(I/V^2)$ versus (I/V) plot is negative with a slight temperature dependence (~3%) in the high voltage regime of 30-40V. This indicates that the conduction mechanism is not a pure FN tunneling (see Eqn. 7.2). In a normal plasma deposited silicon dioxide, PF conduction has been reported to occur at > 1.4 MV/cm [194] compared to FN conduction which is known to occur at higher fields in the range of 7-8 MV/cm [185, 186]. However, due large number of sidewall scallops formed by Recipe-A1, a PF type of conduction mechanism appears to dominate in the voltage range of 20-40V as seen in Figs. 7.4(b) and (c). It can also be seen from Table A-8 that the TEOS oxide thickness decreases from ~1.2 μ m at the top to ~0.3 μ m at the bottom due to the nature of

PECVD process. Similarly, the sidewall metallization process also decreases from 1.13 μm at the top to 0.27-0.33 μm at the bottom. Though the dielectric and copper thickness reduction from top to bottom is not expected to affect the leakage performance significantly, the titanium barrier thinning (not shown in the table) is expected affect the conduction mechanism when there is not sufficient titanium to block copper ions from diffusing into the dielectric. Judging from the very low leakage current value (10^{-12} to 10^{-10} A) at both low and high temperature, it can be concluded that there is no copper diffusion into the dielectric.

Figure 7.4: Leakage current in deep silicon vias etched by Recipe A1 with vertical profile and a peak to peak sidewall roughness of $\sim 0.10\mu\text{m}$. (a) I-V plot at room temperatures (RT) and 100 °C with current expressed in log-scale, (b) Plot of $\text{Ln}(I/V)$ versus $\sqrt{V}$ and (c) Plot of $\text{Ln}(I/V^2)$ versus reciprocal of V .

Figure 7.5: Cross sectional measurements done at the top and bottom of a via etched by Recipe A1 with vertical profile and sidewall roughness of 0.05-0.10 μm. (a) Shows dielectric (SiO₂) thinning from 2.0 μm to 1.2 μm due to vertical profile and (b) Further thinning of dielectric from 1.2 μm at the top to 0.27-0.30 μm at the bottom.

7.5.2 Effect of recipe C1:

In comparison to recipe A1 which has vertical profile with minimum sidewall roughness of 0.05-0.10 μm, the Recipe C1 gives rise to a much higher degree of roughness (0.2-0.3 μm) and also a reentrant profile as shown in Figs. 7.2(b) and 7.3(b). Figure 7.6(c) shows that there is a strong PF type of conduction mechanism due to a ~ 30% drop in slope when temperature is increased from 22 to 100 °C. It can also be seen that due to an increase in the sidewall roughness, the Recipe C1 results in almost a 3 order of magnitude increase in the leakage current as compared to Recipe A1 at low voltage range of 0-10V. Due to the presence of a highly rough silicon surface, the sidewall dielectric is expected to have a lot of traps which are expected to cause thermally assisted hopping even at lower voltage range of 0-20V (See Fig 7.6(a)).

Figure 7.6: Leakage current in deep silicon vias etched by Recipe C1 with a reentrant profile and larger peak to peak sidewall roughness of 0.2-0.3 μm . (a) I - V plot with current expressed in log-scale, (b) Plot of I versus V^2 and (c) Plot of $\ln(I/V)$ versus $\sqrt{V}$.

It may be noted from Table A-8 that the the large scallops on the sidewalls due to process C1 has caused the dielectric thickness to decreases from 0.88-1.04 μm at the top to 0.13-0.17 μm at the bottom. The scallops similarly have caused the sidewall metallization thickness to decrease from 0.25-0.32 μm at the top to 0.18-0.20 μm at the bottom. The effect of significant thinning of sidewall metal (Cu/Ti) due to large sidewall scallops (0.2-

0.3 μm) is also expected to weaken the barrier (Ti) resulting in increase in the leakage current.

Figure 7.7: Cross-sectional measurement done at the top and bottom of deep silicon vias etched by Recipe-C1 with reentrant profile and larger peak to peak sidewall roughness of 0.2-0.3 μm . (a) Shows dielectric (SiO₂) thickness varying from $\sim$ 0.86-1.0 μm due to scallops at the top and (b) Dielectric thinning from 1.0 μm at the top to 0.17-0.38 μm at the bottom.

7.5.3 Effect of recipe F1:

It can be noted from Fig. 7.9 (a) that the leakage current reduces significantly by almost 3 order of magnitudes by smoothening the sidewall of the via with Recipe D1 (i.e., global isotropic etch). This observation is consistent with the results presented in Chapter 4 for hybrid etch process which is a combination of a non-Bosch and a Bosch etch process (See Fig. 4.16). It can also be seen from Figs. 7.2 (b) and (c) that the reentrant profile still remains at the bottom of the via despite slight tapering and smoothening achieved at the top. It may be observed from Table A-8 (See Appendix A) that after the top of the via has been smoothened by recipe: D1, the roughness reduced from 0.2-0.3 μm to 20-30nm. As the effect of global isotropic etch process also decreases with depth of the via, the bottom

sidewall smoothens to a lesser degree in the range of 100-138nm. This results in greater increase in dielectric and Cu/Ti thickness at the top than at the bottom of the via as shown in the Table A-8.

As a consequence of this improvement at the top of the vias, the dielectric leakage current significantly reduces as shown in Fig 7.9(a). Figure 7.9 (b) shows that despite that the slope of the plot is positive as expected in PF equation in high voltage region, it has not shown any significant drop as expected with increasing temperature. It is postulated that the traps in the dielectric due to roughness in the sidewall has been largely smoothed at the top of the vias by the global isotropic etch (See Fig. 7.8) and hence no significant trap-assisted charge hopping is dominant. From Fig. 7.9 (c), it can be observed that the slope of the $\ln(I/V^2)$ versus I/V plot is negative and not significantly affected by the temperature as expected in a defect-free FN model. It can thus be concluded that the conduction mechanism is a combination of PF and FN.

Figure 7.8: Cross-sectional measurements done at the top and bottom of silicon vias etched by dual-etch via tapering Recipe F1. (a) Shows conformal dielectric (SiO_2) deposition at the top due to tapered profile and (b) Dielectric thickness varies from 0.38-0.48 μm at the bottom due to scallops prevailing at the bottom.

Figure 7.9: Leakage current in deep silicon vias etched by dual-etch via tapering process Recipe F1 (i.e., a Bosch etch C1+ Global isotropic etch D1) which converts the reentrant profile shown in Fig. 2(b) to a slightly tapered profile at the top. (a) Shows I-V plot with current in log-scale, (b) Plot of $\ln(I/V)$ versus $\sqrt{V}$ and (c) Plot of $\ln(I/V^2)$ versus reciprocal of V.

7.5.4 Effect of recipe B1:

The electrical results of Recipe B1 are shown in Fig. 7.10(a and b). The analysis of the results shows that there is a clear correlation with PF conduction mechanism in the range of 10-40V. It can be seen from Table A-8 that there is a significant thickness variation of 0.5-1.04 μm at the top due to shadowing effect of the sharp curvature of 3-4 μm . This in turn also affects the uniformity of sidewall metallization which varies from 0.15-0.62 μm . These factors are expected to

be responsible for the PF type of leakage conduction. It may thus be seen that both the recipe A1, B1 and C1 have similar effect on the conduction behavior due to defective sidewalls. As observed in Fig 7.2 (d) the profile of via structure is tapered at the bottom. Hence, the conduction behavior is expected to be dominated by the curvature defect at the top of the via. Another significant observation is that the leakage current due to the curvature defect (shown in Fig-7.11) is almost 3 orders of magnitude lower than that due to large scallops due to C1 (shown in Fig-7.7). It is also noticed that the leakage current due to smaller scallops (see Fig-7.5) is 2 to 3 orders of magnitude lower than that due to Recipe B1 (see Fig-7.11). It is thus seen that the effect of scallop size dominates over the curvature (See Figure 7.14 and Table-7.5).

Figure 7.10: Leakage current in deep silicon vias etched by tapered RIE-etch Recipe B1 which creates tapered profile but with a sharp curvature at the top as shown in Fig. 7.2(d). (a) Shows normal I-V plot. (b) The Ln (I/V) versus $\sqrt{V}$ plot in 10-40V range shows that the slope decreases with increase in temperature as in a PF type of dielectric conduction.

Figure 7.11: SEM micrographs of deep silicon vias etched by tapered RIE-etch Recipe B1 which creates tapered profile with a sharp curvature at the top. The cross-section micrographs were analyzed after a dielectric and metal deposition. (a) Shows non-conformal dielectric (SiO_2) deposition at the top due to curvature and (b) Smoother sidewall profile seen at the bottom with minimum dielectric thickness variation of 0.29-0.30 μm .

7.5.5 Effect of recipe E1:

As shown in Fig 7.2(d) and 7.13, the sharp curvature defect due to recipe B1 has been minimized resulting in a more uniform dielectric and metal deposition on sidewalls of the TSV. Though the sharp curvature formed by B1 has been rounded at the top edge there is still a slight bowing by 0.8-1.0 μm as shown in Table A-8. An analysis of the leakage current results showed that there is no clear correlation with PF or FN conduction mechanism. The leakage current is however two order of magnitude lower than that of Recipe B1 which indicates that the dielectric is either thicker, less defective or both. From Figure 7.13, it can also be confirmed that the dielectric is thicker and more uniform from the top to the bottom with smoother surface. It is seen that by reducing the curvature at the top, the leakage current can be reduced significantly. It can be seen from Figure 12(a) that

the I-V is a linear in the 0-15 V regime and its slope increases with increasing temperature. This behavior can be expected due to the presence of thermal hopping in defect-free dielectric in low-field region of $< 1.4\text{MV/cm}$ [195].

Figure 7.12: Leakage current in deep silicon vias etched by a dual-etch via tapering process i.e., Recipe E1 (i.e., a non-Bosch etch B1 and a Global isotropic etch D1). (a) Shows I-V plot with leakage current in log-scale. (b) The I-V plot is shown in a log scale to show the reduction in order of magnitude of leakage current compared to recipe B1

Figure 7.13: SEM micrographs showing deep silicon vias etched by a dual-etch via tapering process Recipe E1 which has converted the curved profile (See Fig. 7.2(d)) to a smoother tapered profile at the top (See Fig. 7.2(e)). (a) Shows a more conformal dielectric (SiO₂) deposition at the top due to reduced curvature compared to Fig-7.11(a). (b) Smoother sidewall profile seen at the bottom with minimum dielectric thickness variation of 0.41-0.44 μm.

Figure 7.14(a & b) plots the leakage current for all the different recipes used in this study at 22 and 100 °C. The plots are shown in log-scale for better comparison and clarity. Table 7.4 provides an overall summary of various types of dielectric conduction mechanisms observed for different TSV profiles and sidewall roughness conditions. Table 7.5 summarizes the significant effects observed due to different TSV profiles and sidewall conditions. It also compares the effect of various recipes, sidewall roughness and via profiles on leakage conduction at 20V through the dielectric in TSV.

Figure 7.14: Consolidated I-V trend of leakage current due to recipe A1 to F1 at 22 and 100 °C

Table 7.4: Summary of recipes used and conduction mechanism observed.

Recipe	Profile	Sidewall roughness	Conduction mechanism
A1	Vertical	Rough sidewall (~0.05-0.10 μm)	PF and FN
B1	Tapered with curvature at top	Top curvature length of 3-5 μm with smooth surface	PF
C1	Reentrant	Rough sidewall (~0.20-0.30 μm)	PF
E1	Tapered	Top curvature length < 1.0 μm with smooth surface	No clear trend.
F1	Reentrant with tapering at top	Tapered profile at top with sidewall roughness of 0.1-0.5 μm	PF and FN

Table 7.5: Impact of profile and sidewall roughness on leakage current measured at 20V at room temperature

Recipe-id	A1	C1	F1	E1	B1
Maximum current at RT at 20V	2.1×10^{-11}	5.8×10^{-6}	4.6×10^{-11}	3.4×10^{-12}	4.1×10^{-9}
Effect of profile change from reentrant to vertical & the effect of increase in scallop size (C1 vs. A1)	C1/A1	3×10^5	Increase in leakage current by 5 orders of magnitude		
Comparison of effect of large scallops (0.2-0.3 μm) and curvature defect ($\sim 5\mu\text{m}$) on leakage current (C1 vs. B1)	C1/B1 :	1×10^3	Increase in leakage current by 3 orders of magnitude due to large scallops compared to curvature		
Comparison of effect of smaller scallops (0.05-0.1 μm) and curvature ($\sim 5\mu\text{m}$) on leakage current (A1 vs. B1)	A1/B1	5×10^{-3}	Decrease in leakage current by 2 to 3 orders of magnitude with decrease in scallop size		
Effect of smoothening sidewall scallops by dual-etch process F1 (F1 vs. C1)	F1/C1	8×10^{-6}	Decrease in leakage current by nearly 5 orders of magnitude		
Effect of smoothening of curvature by dual-etch process E1(E1 vs. B1)	E1/B1	8×10^{-4}	Decrease in leakage current by nearly 3 orders of magnitude		

7.6 CONCLUSIONS

Based on the five different silicon via surfaces and profile conditions evaluated in this work, it was seen that the sidewall roughness or scallops mainly contributed to trap-assisted conduction. It is also seen that when the sidewall roughness due to scallops formed by Bosch etch process is increased, the leakage mechanism showed a greater correlation to PF type of conduction. Another significant observation is that by changing the reentrant profile formed by Bosch process (C1) to a tapered profile with a dual etch process (F1), the leakage current can be reduced by almost five orders of magnitude. It was also observed that the conduction mechanism also changed from PF mechanism towards FN type of conduction mechanism as in a defect-free dielectric. A corollary of this result is that it may be possible to use a high etch rate process which results in large scallop size and reentrant

profile (see Figures 7.2(b) and 7.3(b)) as long as the sidewall roughness can be smoothened by a global isotropic etch process which eventually results in a slight tapered profile at the top.

In case of the non-Bosch etch process (B1) with tapered via profile and sharp curvature, it was found that the leakage current displayed a PF type of conduction mechanism as in a Bosch etch process. It was however seen that the leakage current was mainly dominated by the scallop size compared to curvature. By minimizing the curvature with dual-etch process (E1) it was shown that the effective dielectric thickness on the sidewall and its uniformity improve significantly. It was also seen that the dual-etch process (E1) resulted in a reduction in leakage current by almost three order of magnitude compared to the single-step non-Bosch etch process (B1).

Thus it may be concluded that for a reliable electrical isolation with minimum leakage current between the TSV structures, it is necessary to minimize the sidewall curvature or scallops. It was also observed that a more uniform dielectric thickness and metal deposition on the TSV sidewalls contributed to lowering leakage current.

Chapter 8

Conclusion and Future Work

8.1 CONCLUSIONS

Based on extensive literature review it was shown that deep silicon reactive ion etch technology and Bosch etch process in particular to be the most preferred etch technology for through silicon interconnection or TSV application. This research therefore focused on critical challenges pertaining to deep silicon via etch technology and demonstrated approaches to overcome them by a series of detailed experimental and characterization studies.

In the first part of the work (discussed in Chapter 4) a detailed investigation was done to study the various kinds of failure modes and failure mechanisms due to the Bosch etch process with depth $\leq 30\mu\text{m}$ and straight via profile which is commonly used for wafer level 3D IC applications. Based on the thermo-mechanical stress modeling, it was shown that the corners of through silicon copper via structures and the scallops will contribute to maximum stress on the barrier and dielectric layer. It was further shown experimentally that the leakage current in the vias can be significantly reduced when the sidewall roughness produced by the Bosch process is reduced by using a non-Bosch (RIE) process or by tailoring it with the Bosch process to produce a smooth sidewall in the initial 3-4 μm of the via. It was also shown that a correlation existed between the sidewall roughness, leakage current and the thermo-mechanical stress induced due to the post-process.

In the second part of the research work, a multi-step tapered silicon via etching technology was developed and comprehensively characterized for depths in the range of 100-300 μ m for MEMS and carrier-based wafer level packaging. The step-by-step evolution of via profile and the etch mechanism were discussed. It was shown that a 2-step or dual-etch technology provides high degree of process flexibility as it allows global isotropic etch step to be tailored with both the Bosch and non-Bosch etch process for achieving TSV depths from 100-200 μ m (discussed in Chapter 5). For achieving via depths > 200 μ m, a 3-step or triple-etch process technology was developed by tailoring Bosch, RIE and Isotropic etch process. It was finally shown that the multi-step tapered via etch process can achieve smooth sidewall with the capability to tune via depth over a wide range from 100-300 μ m with profile angle in the range of 83-87° to achieve void-free copper via-filling (discussed in Chapter 6). It was further shown that the tapered via etching process can be fully integrated in the silicon carrier fabrication technology to build a 3D stacked silicon module.

In the third and final part of the work, the influence of deep silicon via profile and sidewall roughness on the leakage current through sidewall isolation dielectric is studied extensively for TSV application. It is shown that when the sidewall roughness or scallops formed by Bosch etch process are increased, the leakage mechanism shows a greater correlation to Poole-Frenkel (PF) conduction which results in an increased leakage current under high electric field. Another significant observation is that when a sidewall tapering or smoothening process is applied to the silicon via with very rough sidewalls, the leakage current decreases by almost 3 orders of magnitude and changes the conduction mechanism from the PF to Fowler-Nordheim (FN) conduction as in a defect-free dielectric. It has also

been shown that in case of silicon vias formed by non-Bosch etch process with tapered via profile, the leakage current reduces by two orders of magnitude compared to that in the Bosch etch process. It is further shown that by reducing the top curvature defects with the dual-etch process, the effective dielectric thickness on the sidewall and its uniformity improves significantly resulting in a further reduction of the leakage current by another order of magnitude. Thus a better dielectric isolation can be achieved with a tapered via than in case of vertical vias due to more conformal dielectric thickness and metal deposition and smoother sidewalls.

8.2 RECOMMENDATIONS FOR FUTURE WORK

The present research work had focused extensively on silicon via etch technologies for use before the wafer thinning process as it is well suited for both semiconductor wafer fabs and packaging houses due to ease in implementation within the existing supply chain. Based on the 2008 ITRS high density TSV (HDTSV) draft specifications [3], the diameter of TSV is expected to be scaled down to $1.0\text{ }\mu\text{m}$ with via depth of $10\text{ }\mu\text{m}$ and minimum via to via spacing of $1.5\text{ }\mu\text{m}$ by the year 2015. A reduction in spacing between TSVs further necessitates minimizing sidewall roughness caused by silicon via etch process to minimize via to via electrical leakage [197]. Therefore, one of the focus areas for next generation silicon via etch technology for implementation in wafer-fab will be to achieve smoother sidewalls with more vertical via etch profile due to limited via to via spacing. The TSV scaling trend is thus expected to motivate development of newer silicon via etch technologies with smoother sidewalls such as non-Bosch etch process [196] and hybrid etch processes [23, 25]. Moving away from Bosch etch process is further motivated by a

need to avoid the constraints imposed by its scalloping effects which disrupt the subsequent deposition of continuous and uniform barrier and copper seed layers. While achieving smooth sidewall with high etch rates requires advanced tools with high capital cost, Chapter 4 had shown that a combination of short smooth etch followed by standard Bosch etch process (hybrid process) can accomplish the same objective as a non-Bosch process. Hence, this approach may be further evaluated for smaller diameter vias for next generation TSV application.

Another technology that is gaining attention amongst packaging industries involves formation of TSV after the back-end of the line (BEOL) processes but before the wafer thinning process. This approach requires etching vias through thick multi-layered dielectric stack of 6-9 μm and then continue to etch the silicon vias with minimum or no undercut below the dielectric. As per ITRS 2009 specification for assembly and packaging technology [197], the TSV diameter is expected to be scaled down to 2-4 μm with aspect ratio increasing to 10-20 by the year 2015. The above requirement thus poses a huge challenge to lithography technology which requires thick enough photoresist mask to be patternable with its thickness in the range of 8-10 μm while at the same time resolve finer via geometries of 2-4 μm . With the present thick resist technology this is a big challenge and hence requires lot of new material development. Present generation etch tools are dedicated for etching silicon and dielectric materials and hence are not capable of performing etching of multiple layers of disparate materials. For the next generation etch technology, it requires continuous etching of disparate films like low-k dielectric, barrier films, silicon dioxide and eventually the silicon substrate. This would further require a

good etch selectivity to resist mask, control on etch profile and maintain minimum silicon undercut and sidewall roughness.

The present work had focused on developing and characterizing vertical and tapered deep silicon via etch technologies for TSV application with standard BEOL dielectric films processed at 250 °C and 400 °C. However, in future, it is expected that much lower temperature dielectric films will be adopted due to lower thermal budget imposed by thin wafer handling adhesive material (150-200 °C) [179]. A low-temperature process is also motivated by a need to minimize the thermo-mechanical stresses imposed by TSV structure as explained in Chapter 4. With recent technology advancement in deposition tools (STS Multiplex CVD), lower temperature dielectric films can be deposited at temperatures 150-200 °C. Hence, an investigation of the low-temperature dielectric and its electrical performance would provide vital solution for next generation TSV application.

Finally, for implementing TSV in both active device substrates (for small geometry vias) and passive substrates (for large geometry vias as in interposer), it is necessary to characterize it extensively for various coupling effects between vias and via to substrate. In the present work, TSV to TSV leakage effects were fully characterized for both small and large geometry vias. However, TSV to substrate effects have not been studied. A detailed study on leakage current between the TSV to substrate can provide additional insight into the leakage behaviors of TSV structures with respect to silicon substrate. Further, the leakage current investigation can be enhanced by using a thermal oxide for dielectric isolation. Though thermal oxide is not a preferred material for TSV isolation, it can still be used to determine the ideal lower limit of TSV leakage as it is expected to have very low defect density compared to all other low temperature dielectrics.

Appendix A

Supplementary information for Chapter 4

Table A-1: Within wafer variation measured in dielectric and metallization processes

Films used in TSV	Target thickness (nm)	Sheet Rho (Ω -cm)	Within wafer thickness non-uniformity (%)
Copper seed	150	1.60E-01	4.67%
Ta-barrier	25	81.01	5.38%
Ta-barrier	100	22.688	6.98%
TEOS oxide	500	-	2%

Table A-2: Within wafer CMP dishing measured at 5 sites across 2 wafers with profiler

Die #	CMP dishing in Wafer #1	CMP dishing Wafer #2	Mean CMP dishing (nm)
1	417.0	297.8	357.4
2	406.9	438.5	422.7
3	371.1	273.1	322.1
4	268.5	345.3	306.9
5	555.7	254.9	405.3

Figure A-1: Within wafer CMP dishing measured at 5 sites across 2 wafers with profiler. The mean dishing is 363 nm with within wafer variation of 50 nm.

Table A-3: Variations in dielectric, barrier films and sidewall roughness within TSV test structure (See Fig 4.7) measured by SEM cross-section through the 5 μ m test structure:

Run #	TEOS oxide thickness (nm)			Barrier thickness (nm)			Sidewall roughness (nm)			Cu-barrier stack (nm)	Via depth	Etch process
	Top	Middle	Bottom	Top	Middle	Bottom	Top	Middle	Bottom			
2	177-210	225-250	250-260	11-17	13-16	10-16	50-59	33-40	10-20	25 nm Ta	10 μ m	Bosch (A)
3	177-210	225-250	250-260	53-74	62-76	51-60	51-65	30-36	10-15	100 nm SiN + 25 nm Ta	10 μ m	Bosch (A)
4	237-240	219-222	230-237	83-90	90-100	80-83	< 10	<10	<10	100 nm SiN + 25 nm Ta	10 μ m	Non-Bosch(B)
5	230-239	219-225	240-245	21.6	20-25	20-30	< 10	<10	<10	25 nm Ta	10 μ m	Non-Bosch(B)
6	230-240	219-230	217-242	30-40	35-36	30-36	< 10	<10	<10	100 nm Ta	10 μ m	Non-Bosch(B)
7	190-206	225-250	250-260	47-53	50-65	38-56	50-56	40-43	10-15	100 nm Ta	10 μ m	Bosch (A)
8	177-210	193-246	235-275	44-70	60-90	81-85	40-50	29-33	15-20	100 nm SiN +100 nm Ta	30 μ m	Bosch (A)
9	143-184	165-200	132-153	36-40	35-40	36-40	< 10	40-43	10-15	100 nm Ta	30 μ m	B + A

Table A-4: Variations in dielectric, barrier films and sidewall roughness within TSV test structure measured by SEM cross-section through the 35 μ m test structure:

Run #	TEOS oxide thickness (nm)			Barrier thickness (nm)			Sidewall roughness (nm)			Cu-barrier stack (nm)	Via depth	Etch process
	Top	Middle	Bottom	Top	Middle	Bottom	Top	Middle	Bottom			
2	257-353	296-351	308-325	25.4	14	10-15	63	35	22	25 nm Ta	10 μ m	Bosch (A)
3	283-366	272-386	284-348	63-93	60-86	78	77	58	22	100 nm SiN + 25 nm Ta	10 μ m	Bosch (A)
4	270-360	290-300	280-340	65-93	64-90	90-100	30	25	<10	100 nm SiN + 25 nm Ta	10 μ m	Non-Bosch(B)
5	296-300	292-300	290-300	25	25-30	20	30	22	<10	25 nm Ta	10 μ m	Non-Bosch(B)
6	289-300	300-304	300-307	42	57	51	<10	<10	<10	100 nm Ta	10 μ m	Non-Bosch(B)
7	260-300	287-300	250-300	65-75	55-73	63-66	61	45	<30	100 nm Ta	10 μ m	Bosch (A)
8	246-281	281-300	260-300	81-95	95-100	99-102	30-36	<10	<10	100 nm SiN +100 nm Ta	30 μ m	Bosch (A)
9	231-245	235-267	223-265	33-35	34-36	33	<30	27	25	100 nm Ta	30 μ m	B + A

Electrical measurement database for Chapter 4

Table A-5: Electrical leakage current measurement results at 22 °C to study the impact of different process condition (See Table 4.10). The results are presented in Fig 4.13 to 4.16

V	Run-1	Run-2	Run-3	Run-4	Run-5	Run-6	Run-7	Run-8	Run-9
0	-1.50E-13	-8.78E-12	5.98E-11	4.72E-12	2.00E-13	1.20E-12	2.66E-12	-2.92E-12	1.30E-13
0.5	2.26E-11	9.88E-11	1.48E-10	2.43E-11	6.25E-12	4.60E-12	9.70E-12	8.67E-11	3.59E-12
1	3.94E-11	1.67E-10	1.83E-10	4.08E-11	9.54E-12	6.48E-12	1.51E-11	2.92E-10	5.12E-12
1.5	5.40E-11	2.40E-10	2.07E-10	5.54E-11	1.17E-11	7.90E-12	1.98E-11	1.10E-09	6.40E-12
2	6.87E-11	3.02E-10	2.29E-10	6.84E-11	1.35E-11	9.16E-12	2.40E-11	3.51E-09	7.82E-12
2.5	8.46E-11	3.60E-10	2.72E-10	7.92E-11	1.52E-11	1.03E-11	2.78E-11	4.17E-08	9.01E-12
3	1.05E-10	4.15E-10	3.24E-10	8.75E-11	1.70E-11	1.13E-11	3.11E-11	8.49E-07	1.03E-11
3.5	1.30E-10	4.65E-10	3.75E-10	9.62E-11	1.88E-11	1.22E-11	3.42E-11	9.02E-07	1.12E-11
4	1.96E-10	5.14E-10	4.28E-10	1.04E-10	2.09E-11	1.31E-11	3.71E-11	9.50E-07	1.26E-11
4.5	1.13E-09	5.61E-10	4.80E-10	1.10E-10	2.26E-11	1.38E-11	3.97E-11	9.98E-07	1.44E-11
5	1.23E-07	6.03E-10	5.95E-10	1.14E-10	2.45E-11	1.45E-11	4.21E-11	1.05E-06	1.62E-11
5.5	1.89E-07	6.16E-10	6.02E-10	1.15E-10	2.61E-11	1.52E-11	4.43E-11	1.08E-06	1.80E-11
6	2.49E-07	6.52E-10	6.42E-10	1.13E-10	2.76E-11	1.57E-11	4.63E-11	1.10E-06	1.95E-11
6.5	2.88E-07	6.84E-10	7.41E-10	1.12E-10	2.87E-11	1.63E-11	4.81E-11	1.12E-06	2.14E-11
7	3.23E-07	7.32E-10	6.50E-10	1.12E-10	3.01E-11	1.68E-11	4.97E-11	1.14E-06	2.25E-11
7.5	3.42E-07	7.55E-10	6.29E-10	1.13E-10	3.13E-11	1.73E-11	5.12E-11	1.16E-06	2.40E-11
8	3.55E-07	7.87E-10	5.94E-10	1.14E-10	3.24E-11	1.78E-11	5.22E-11	1.19E-06	2.56E-11
8.5	3.63E-07	8.18E-10	6.11E-10	1.15E-10	3.34E-11	1.82E-11	5.35E-11	1.21E-06	2.71E-11
9	3.72E-07	8.50E-10	6.09E-10	1.16E-10	3.43E-11	1.87E-11	5.45E-11	1.22E-06	2.86E-11
9.5	3.82E-07	8.79E-10	6.32E-10	1.17E-10	3.50E-11	1.91E-11	5.53E-11	1.24E-06	2.98E-11
10	3.92E-07	9.09E-10	6.30E-10	1.19E-10	3.59E-11	1.95E-11	5.60E-11	1.25E-06	3.11E-11
10.5	3.97E-07	9.34E-10	6.40E-10	1.20E-10	3.67E-11	1.99E-11	5.64E-11	1.27E-06	3.27E-11
11	4.04E-07	9.59E-10	6.23E-10	1.21E-10	3.75E-11	2.03E-11	5.70E-11	1.28E-06	3.41E-11
11.5	4.13E-07	1.00E-09	6.49E-10	1.22E-10	3.82E-11	2.07E-11	5.74E-11	1.30E-06	3.55E-11
12	4.24E-07	1.06E-09	6.40E-10	1.23E-10	3.86E-11	2.09E-11	5.77E-11	1.32E-06	3.73E-11
12.5	4.31E-07	1.10E-09	6.43E-10	1.24E-10	3.94E-11	2.14E-11	5.78E-11	1.33E-06	3.89E-11
13	4.32E-07	1.14E-09	6.60E-10	1.25E-10	4.00E-11	2.18E-11	5.79E-11	1.35E-06	4.00E-11
13.5	4.41E-07	1.17E-09	6.76E-10	1.25E-10	4.06E-11	2.23E-11	5.83E-11	1.36E-06	4.14E-11
14	4.47E-07	1.20E-09	6.89E-10	1.26E-10	4.12E-11	2.26E-11	5.82E-11	1.39E-06	4.32E-11
14.5	4.54E-07	1.23E-09	7.22E-10	1.26E-10	4.18E-11	2.29E-11	5.85E-11	1.41E-06	4.50E-11
15	4.65E-07	1.26E-09	7.21E-10	1.26E-10	4.20E-11	2.34E-11	5.86E-11	1.42E-06	4.97E-11
15.5	4.65E-07	1.29E-09	7.29E-10	1.26E-10	4.27E-11	2.39E-11	5.88E-11	1.44E-06	4.96E-11
16	4.64E-07	1.32E-09	7.19E-10	1.25E-10	4.32E-11	2.42E-11	5.88E-11	1.45E-06	5.02E-11
16.5	4.67E-07	1.34E-09	7.29E-10	1.25E-10	4.37E-11	2.47E-11	5.87E-11	1.46E-06	5.37E-11
17	4.71E-07	1.37E-09	7.37E-10	1.24E-10	4.42E-11	2.51E-11	5.87E-11	1.48E-06	5.81E-11
17.5	4.74E-07	1.40E-09	7.47E-10	1.24E-10	4.47E-11	2.55E-11	5.86E-11	1.51E-06	7.27E-11
18	4.83E-07	1.42E-09	7.91E-10	1.23E-10	4.52E-11	2.57E-11	5.86E-11	1.58E-06	7.53E-11
18.5	5.00E-07	1.45E-09	7.99E-10	1.22E-10	4.54E-11	2.62E-11	5.88E-11	1.53E-06	8.10E-11
19	5.01E-07	1.47E-09	7.35E-10	1.21E-10	4.60E-11	2.66E-11	5.86E-11	1.53E-06	8.19E-11
19.5	4.99E-07	1.49E-09	7.45E-10	1.20E-10	4.66E-11	2.71E-11	5.87E-11	1.56E-06	8.15E-11
20	5.04E-07	1.52E-09	7.73E-10	1.19E-10	4.71E-11	2.75E-11	5.88E-11	1.57E-06	8.20E-11
20.5	5.08E-07	1.54E-09	8.09E-10	1.18E-10	4.76E-11	2.77E-11	5.88E-11	1.59E-06	8.33E-11
21	5.27E-07	1.56E-09	1.11E-09	1.17E-10	4.81E-11	2.83E-11	5.86E-11	1.60E-06	8.48E-11
21.5	5.43E-07	1.59E-09	1.14E-09	1.16E-10	4.85E-11	2.87E-11	5.86E-11	1.63E-06	8.31E-11
22	5.34E-07	1.61E-09	3.32E-09	1.15E-10	4.92E-11	2.91E-11	5.86E-11	1.64E-06	8.98E-11
22.5	5.48E-07	1.63E-09	9.44E-08	1.14E-10	4.99E-11	2.96E-11	5.86E-11	1.60E-06	8.99E-11
23	5.55E-07	1.65E-09	1.85E-09	1.13E-10	5.07E-11	2.99E-11	5.89E-11	1.61E-06	8.84E-11

Appendix A

23.5	5.67E-07	1.67E-09	2.52E-09	1.13E-10	5.15E-11	3.06E-11	5.90E-11	1.62E-06	9.04E-11
24	5.78E-07	1.69E-09	4.00E-08	1.12E-10	5.24E-11	3.12E-11	5.91E-11	1.63E-06	9.37E-11
24.5	5.83E-07	1.71E-09	3.40E-06	1.11E-10	5.34E-11	3.19E-11	5.93E-11	1.64E-06	9.47E-11
25	5.97E-07	1.74E-09	3.38E-06	1.10E-10	5.41E-11	3.25E-11	5.95E-11	1.65E-06	9.42E-11
25.5	5.76E-07	1.76E-09	3.38E-06	1.10E-10	5.55E-11	3.30E-11	5.94E-11	1.67E-06	9.63E-11
26	5.74E-07	1.78E-09	3.38E-06	1.09E-10	5.64E-11	3.40E-11	5.98E-11	1.70E-06	1.01E-10
26.5	5.74E-07	1.80E-09	3.39E-06	1.09E-10	5.76E-11	3.50E-11	5.99E-11	1.71E-06	1.04E-10
27	6.06E-07	1.82E-09	3.40E-06	1.08E-10	5.89E-11	3.61E-11	6.01E-11	1.73E-06	1.06E-10
27.5	5.98E-07	1.84E-09	3.41E-06	1.08E-10	6.03E-11	3.73E-11	6.03E-11	1.75E-06	1.08E-10
28	6.06E-07	1.85E-09	3.43E-06	1.08E-10	6.18E-11	3.82E-11	6.07E-11	1.76E-06	1.09E-10
28.5	6.14E-07	1.87E-09	3.45E-06	1.07E-10	6.31E-11	3.99E-11	6.11E-11	1.76E-06	1.26E-10
29	6.16E-07	1.89E-09	3.47E-06	1.07E-10	6.46E-11	4.14E-11	6.18E-11	1.78E-06	1.36E-10
29.5	6.23E-07	1.91E-09	3.48E-06	1.18E-10	6.60E-11	4.30E-11	6.24E-11	1.79E-06	1.46E-10
30	6.29E-07	1.93E-09	3.49E-06	1.10E-10	6.75E-11	4.46E-11	6.31E-11	1.79E-06	1.07E-10
30.5	6.31E-07	1.94E-09	3.50E-06	1.10E-10	6.84E-11	4.58E-11	6.39E-11	1.81E-06	1.02E-10
31	6.39E-07	1.96E-09	3.51E-06	1.10E-10	7.01E-11	4.79E-11	6.44E-11	1.82E-06	1.11E-10
31.5	6.39E-07	1.98E-09	3.52E-06	1.11E-10	7.14E-11	4.95E-11	6.52E-11	1.83E-06	1.11E-10
32	6.37E-07	1.99E-09	3.54E-06	1.11E-10	7.27E-11	5.12E-11	6.64E-11	1.85E-06	1.18E-10
32.5	6.53E-07	2.01E-09	3.55E-06	1.11E-10	7.34E-11	5.30E-11	6.71E-11	1.86E-06	1.20E-10
33	6.57E-07	2.02E-09	3.56E-06	1.12E-10	7.50E-11	5.38E-11	6.81E-11	1.87E-06	1.20E-10
33.5	6.58E-07	2.04E-09	3.58E-06	1.12E-10	7.62E-11	5.58E-11	6.93E-11	1.89E-06	1.33E-10
34	6.49E-07	2.05E-09	3.59E-06	1.13E-10	7.67E-11	5.74E-11	7.04E-11	1.90E-06	1.19E-10
34.5	6.53E-07	2.08E-09	3.59E-06	1.14E-10	7.81E-11	5.81E-11	7.14E-11	1.91E-06	1.21E-10
35	6.57E-07	2.09E-09	3.60E-06	1.15E-10	7.85E-11	5.91E-11	7.25E-11	1.90E-06	1.28E-10
35.5	6.67E-07	2.10E-09	3.61E-06	1.16E-10	7.87E-11	6.03E-11	7.36E-11	1.92E-06	1.38E-10
36	6.72E-07	2.12E-09	3.63E-06	1.16E-10	8.00E-11	6.15E-11	7.48E-11	1.93E-06	1.31E-10
36.5	6.81E-07	2.13E-09	3.65E-06	1.18E-10	8.01E-11	6.26E-11	7.58E-11	1.95E-06	1.18E-10
37	6.83E-07	2.15E-09	3.67E-06	1.19E-10	8.15E-11	6.37E-11	7.68E-11	1.95E-06	1.25E-10
37.5	6.89E-07	2.16E-09	3.68E-06	1.20E-10	8.48E-11	6.46E-11	7.79E-11	1.96E-06	1.35E-10
38	6.99E-07	2.17E-09	3.69E-06	1.21E-10	8.57E-11	6.56E-11	7.88E-11	1.98E-06	1.38E-10
38.5	7.28E-07	2.19E-09	3.70E-06	1.23E-10	8.77E-11	6.65E-11	7.93E-11	2.00E-06	1.37E-10
39	7.21E-07	2.20E-09	3.71E-06	1.24E-10	8.83E-11	6.75E-11	8.05E-11	2.01E-06	1.28E-10
39.5	7.18E-07	2.21E-09	3.72E-06	1.26E-10	8.95E-11	6.74E-11	8.15E-11	2.02E-06	1.37E-10
40	7.26E-07	2.23E-09	3.73E-06	1.27E-10	9.04E-11	6.88E-11	8.25E-11	2.03E-06	1.42E-10
40.5	7.53E-07	2.24E-09	3.74E-06	1.29E-10	9.12E-11	6.97E-11	8.28E-11	2.04E-06	1.49E-10
41	7.48E-07	2.25E-09	3.76E-06	1.31E-10	9.19E-11	6.97E-11	8.39E-11	2.05E-06	1.40E-10
41.5	7.58E-07	2.26E-09	3.77E-06	1.32E-10	9.26E-11	7.11E-11	8.44E-11	2.06E-06	1.29E-10
42	7.62E-07	2.28E-09	3.78E-06	1.34E-10	9.31E-11	7.21E-11	8.45E-11	2.07E-06	1.41E-10
42.5	7.74E-07	2.29E-09	3.79E-06	1.36E-10	9.38E-11	7.28E-11	8.56E-11	2.08E-06	1.47E-10
43	7.83E-07	2.30E-09	3.80E-06	1.38E-10	9.43E-11	7.27E-11	8.59E-11	2.10E-06	1.41E-10
43.5	7.95E-07	2.31E-09	3.80E-06	1.40E-10	9.48E-11	7.37E-11	8.70E-11	2.14E-06	1.36E-10
44	8.24E-07	2.32E-09	3.81E-06	1.41E-10	9.54E-11	7.36E-11	8.79E-11	2.14E-06	1.47E-10
44.5	8.04E-07	2.33E-09	3.82E-06	1.43E-10	9.59E-11	7.41E-11	8.83E-11	2.18E-06	1.48E-10
45	8.06E-07	2.34E-09	3.83E-06	1.45E-10	9.63E-11	7.55E-11	8.89E-11	2.19E-06	1.43E-10
45.5	8.24E-07	2.35E-09	3.85E-06	1.46E-10	9.69E-11	7.64E-11	9.13E-11	2.19E-06	1.50E-10
46	8.36E-07	2.36E-09	3.87E-06	1.48E-10	9.73E-11	7.71E-11	9.34E-11	2.20E-06	1.46E-10
46.5	8.73E-07	2.37E-09	3.87E-06	1.49E-10	9.77E-11	7.66E-11	9.48E-11	2.21E-06	1.53E-10
47	8.93E-07	2.38E-09	3.88E-06	1.51E-10	9.82E-11	7.80E-11	9.61E-11	2.22E-06	1.50E-10
47.5	9.57E-07	2.38E-09	3.89E-06	1.52E-10	9.86E-11	7.79E-11	9.71E-11	2.24E-06	1.51E-10
48	1.02E-06	2.39E-09	3.89E-06	1.54E-10	9.92E-11	7.74E-11	9.81E-11	2.26E-06	1.55E-10
48.5	1.21E-06	2.40E-09	3.89E-06	1.55E-10	9.96E-11	7.83E-11	9.91E-11	2.25E-06	1.56E-10
49	1.22E-06	2.41E-09	3.90E-06	1.56E-10	9.99E-11	7.81E-11	1.00E-10	2.27E-06	1.62E-10
49.5	1.33E-06	2.42E-09	3.91E-06	1.57E-10	1.00E-10	7.92E-11	1.01E-10	2.31E-06	1.66E-10
50	1.40E-06	2.43E-09	3.92E-06	1.58E-10	1.01E-10	7.91E-11	1.02E-10	2.32E-06	1.79E-10

Appendix A

50.5	1.42E-06	2.43E-09	3.93E-06	1.59E-10	1.01E-10	7.95E-11	1.03E-10	2.32E-06	1.71E-10
51	1.62E-06	2.44E-09	3.93E-06	1.60E-10	1.02E-10	8.07E-11	1.04E-10	2.34E-06	1.77E-10
51.5	1.76E-06	2.45E-09	3.94E-06	1.61E-10	1.02E-10	8.07E-11	1.05E-10	2.34E-06	1.80E-10
52	1.75E-06	2.46E-09	3.94E-06	1.62E-10	1.02E-10	8.16E-11	1.06E-10	2.37E-06	1.85E-10
52.5	1.76E-06	2.46E-09	3.95E-06	1.63E-10	1.03E-10	8.45E-11	1.08E-10	2.39E-06	1.88E-10
53	1.51E-06	2.47E-09	3.95E-06	1.64E-10	1.03E-10	8.55E-11	1.09E-10	2.41E-06	2.13E-10
53.5	1.60E-06	2.48E-09	3.97E-06	1.65E-10	1.03E-10	8.66E-11	1.10E-10	2.42E-06	2.19E-10
54	1.89E-06	2.49E-09	3.98E-06	1.66E-10	1.04E-10	8.85E-11	1.12E-10	2.43E-06	2.20E-10
54.5	2.27E-06	2.50E-09	4.00E-06	1.66E-10	1.04E-10	8.94E-11	1.13E-10	2.46E-06	2.23E-10
55	2.24E-06	2.50E-09	4.01E-06	1.67E-10	1.04E-10	9.01E-11	1.14E-10	2.46E-06	2.26E-10
55.5	2.29E-06	2.51E-09	4.01E-06	1.68E-10	1.05E-10	9.08E-11	1.16E-10	2.49E-06	2.25E-10
56	1.70E-06	2.52E-09	4.02E-06	1.69E-10	1.05E-10	9.15E-11	1.18E-10	2.53E-06	2.36E-10
56.5	2.04E-06	2.53E-09	4.02E-06	1.69E-10	1.06E-10	9.21E-11	1.19E-10	2.57E-06	2.46E-10
57	2.10E-06	2.53E-09	4.02E-06	1.70E-10	1.06E-10	9.27E-11	1.21E-10	2.59E-06	2.52E-10
57.5	2.52E-06	2.54E-09	4.03E-06	1.71E-10	1.06E-10	9.32E-11	1.23E-10	2.60E-06	2.62E-10
58	1.91E-06	2.55E-09	4.04E-06	1.72E-10	1.06E-10	9.35E-11	1.25E-10	2.61E-06	2.72E-10
58.5	2.13E-06	2.56E-09	4.05E-06	1.72E-10	1.07E-10	9.43E-11	1.27E-10	2.61E-06	2.81E-10
59	1.92E-06	2.56E-09	4.05E-06	1.73E-10	1.07E-10	9.46E-11	1.29E-10	2.64E-06	2.92E-10
59.5	1.95E-06	2.57E-09	4.05E-06	1.74E-10	1.08E-10	9.53E-11	1.31E-10	2.66E-06	2.99E-10
60	2.39E-06	2.58E-09	4.06E-06	1.74E-10	1.08E-10	9.58E-11	1.33E-10	2.68E-06	3.11E-10
60.5	2.41E-06	2.59E-09	4.06E-06	1.75E-10	1.08E-10	9.61E-11	1.36E-10	2.69E-06	3.19E-10
61	3.31E-06	2.60E-09	4.07E-06	1.76E-10	1.09E-10	9.66E-11	1.38E-10	2.70E-06	3.26E-10
61.5	3.55E-06	2.60E-09	4.08E-06	1.76E-10	1.09E-10	9.72E-11	1.40E-10	2.74E-06	3.42E-10
62	2.24E-06	2.62E-09	4.09E-06	1.77E-10	1.09E-10	9.78E-11	1.43E-10	2.74E-06	3.57E-10
62.5	3.27E-06	2.63E-09	4.11E-06	1.78E-10	1.10E-10	9.83E-11	1.46E-10	2.77E-06	3.76E-10
63	3.97E-06	2.64E-09	4.13E-06	1.78E-10	1.10E-10	9.87E-11	1.48E-10	2.81E-06	3.89E-10
63.5	5.98E-06	2.64E-09	4.15E-06	1.79E-10	1.10E-10	9.92E-11	1.51E-10	2.82E-06	4.03E-10
64	8.23E-06	2.65E-09	4.15E-06	1.79E-10	1.11E-10	9.97E-11	1.54E-10	2.82E-06	4.20E-10
64.5	9.90E-06	2.66E-09	4.15E-06	1.80E-10	1.11E-10	1.00E-10	1.57E-10	2.83E-06	4.39E-10
65	1.00E-05	2.66E-09	4.15E-06	1.81E-10	1.12E-10	1.01E-10	1.61E-10	2.84E-06	4.50E-10
65.5	1.00E-05	2.67E-09	4.15E-06	1.82E-10	1.12E-10	1.01E-10	1.64E-10	2.86E-06	4.73E-10
66	1.00E-05	2.68E-09	4.16E-06	1.82E-10	1.12E-10	1.02E-10	1.67E-10	2.88E-06	4.96E-10
66.5	1.00E-05	2.68E-09	4.17E-06	1.82E-10	1.13E-10	1.02E-10	1.70E-10	2.85E-06	5.14E-10
67	1.00E-05	2.69E-09	4.18E-06	1.83E-10	1.13E-10	1.03E-10	1.74E-10	2.86E-06	5.32E-10
67.5	1.00E-05	2.70E-09	4.18E-06	1.84E-10	1.13E-10	1.03E-10	1.77E-10	2.87E-06	5.57E-10
68	1.00E-05	2.71E-09	4.18E-06	1.84E-10	1.14E-10	1.04E-10	1.81E-10	2.93E-06	5.83E-10
68.5	1.00E-05	2.72E-09	4.19E-06	1.85E-10	1.14E-10	1.04E-10	1.84E-10	3.00E-06	6.12E-10
69	1.00E-05	2.73E-09	4.19E-06	1.86E-10	1.15E-10	1.04E-10	1.88E-10	3.03E-06	6.43E-10
69.5	1.00E-05	2.74E-09	4.19E-06	1.86E-10	1.15E-10	1.05E-10	1.91E-10	3.01E-06	6.67E-10
70	1.00E-05	2.75E-09	4.19E-06	1.87E-10	1.15E-10	1.05E-10	1.95E-10	3.01E-06	6.95E-10
70.5	1.00E-05	2.76E-09	4.19E-06	1.88E-10	1.16E-10	1.06E-10	2.00E-10	3.02E-06	7.13E-10
71	1.00E-05	2.77E-09	4.20E-06	1.89E-10	1.16E-10	1.06E-10	2.04E-10	3.05E-06	7.41E-10
71.5	1.00E-05	2.78E-09	4.22E-06	1.90E-10	1.17E-10	1.07E-10	2.08E-10	3.06E-06	7.73E-10
72	1.00E-05	2.79E-09	4.22E-06	1.90E-10	1.17E-10	1.07E-10	2.12E-10	3.07E-06	8.02E-10
72.5	1.00E-05	2.79E-09	4.22E-06	1.91E-10	1.18E-10	1.08E-10	2.16E-10	3.08E-06	8.36E-10
73	1.00E-05	2.80E-09	4.21E-06	1.92E-10	1.18E-10	1.08E-10	2.21E-10	3.10E-06	8.71E-10
73.5	1.00E-05	2.82E-09	4.21E-06	1.93E-10	1.19E-10	1.09E-10	2.25E-10	3.12E-06	1.01E-09
74	1.00E-05	2.83E-09	4.20E-06	1.94E-10	1.19E-10	1.09E-10	2.29E-10	3.14E-06	1.19E-09
74.5	1.00E-05	2.83E-09	4.20E-06	1.95E-10	1.20E-10	1.10E-10	2.34E-10	3.14E-06	1.40E-09
75	1.00E-05	2.84E-09	4.21E-06	1.96E-10	1.20E-10	1.10E-10	2.38E-10	3.15E-06	1.56E-09
75.5	1.00E-05	2.85E-09	4.21E-06	1.97E-10	1.20E-10	1.11E-10	2.43E-10	3.16E-06	1.77E-09
76	1.00E-05	2.85E-09	4.22E-06	1.98E-10	1.21E-10	1.11E-10	2.47E-10	3.19E-06	1.95E-09
76.5	1.00E-05	2.86E-09	4.22E-06	1.99E-10	1.22E-10	1.12E-10	2.52E-10	3.24E-06	2.11E-09
77	1.00E-05	2.86E-09	4.22E-06	2.01E-10	1.22E-10	1.13E-10	2.57E-10	3.29E-06	2.29E-09

Appendix A

77.5	1.00E-05	2.87E-09	4.22E-06	2.02E-10	1.23E-10	1.13E-10	2.61E-10	3.27E-06	2.48E-09
78	1.00E-05	2.87E-09	4.23E-06	2.03E-10	1.23E-10	1.14E-10	2.66E-10	3.36E-06	2.61E-09
78.5	1.00E-05	2.88E-09	4.23E-06	2.04E-10	1.24E-10	1.15E-10	2.71E-10	3.42E-06	2.75E-09
79	1.00E-05	2.88E-09	4.23E-06	2.05E-10	1.25E-10	1.15E-10	2.76E-10	3.45E-06	2.89E-09
79.5	1.00E-05	2.88E-09	4.25E-06	2.07E-10	1.25E-10	1.16E-10	2.80E-10	3.43E-06	3.03E-09
80	1.00E-05	2.89E-09	4.26E-06	2.08E-10	1.26E-10	1.17E-10	2.85E-10	3.45E-06	3.21E-09
80.5	1.00E-05	2.89E-09	4.28E-06	2.10E-10	1.27E-10	1.17E-10	2.90E-10	3.48E-06	3.31E-09
81	1.00E-05	2.90E-09	4.28E-06	2.11E-10	1.28E-10	1.18E-10	2.95E-10	3.43E-06	3.33E-09
81.5	1.00E-05	2.90E-09	4.28E-06	2.13E-10	1.29E-10	1.19E-10	3.00E-10	3.42E-06	3.45E-09
82	1.00E-05	2.90E-09	4.28E-06	2.14E-10	1.30E-10	1.20E-10	3.05E-10	3.54E-06	3.59E-09
82.5	1.00E-05	2.91E-09	4.28E-06	2.16E-10	1.31E-10	1.21E-10	3.10E-10	3.56E-06	3.77E-09
83	1.00E-05	2.91E-09	4.28E-06	2.18E-10	1.32E-10	1.22E-10	3.14E-10	3.59E-06	3.81E-09
83.5	1.00E-05	2.91E-09	4.29E-06	2.19E-10	1.33E-10	1.23E-10	3.19E-10	3.66E-06	3.92E-09
84	1.00E-05	2.92E-09	4.30E-06	2.21E-10	1.34E-10	1.24E-10	3.25E-10	3.59E-06	4.05E-09
84.5	1.00E-05	2.92E-09	4.30E-06	2.23E-10	1.35E-10	1.25E-10	3.30E-10	3.63E-06	4.16E-09
85	1.00E-05	2.92E-09	4.30E-06	2.25E-10	1.36E-10	1.26E-10	3.35E-10	3.66E-06	4.34E-09
85.5	1.00E-05	2.92E-09	4.30E-06	2.27E-10	1.38E-10	1.28E-10	3.39E-10	3.66E-06	4.40E-09
86	1.00E-05	2.93E-09	4.31E-06	2.29E-10	1.39E-10	1.29E-10	3.44E-10	3.67E-06	4.50E-09
86.5	1.00E-05	2.93E-09	4.30E-06	2.31E-10	1.40E-10	1.30E-10	3.49E-10	3.66E-06	4.62E-09
87	1.00E-05	2.93E-09	4.30E-06	2.34E-10	1.20E-10	1.31E-10	3.54E-10	3.63E-06	4.79E-09
87.5	1.00E-05	2.94E-09	4.30E-06	2.36E-10	1.43E-10	1.33E-10	3.59E-10	3.68E-06	4.84E-09
88	1.00E-05	2.94E-09	4.31E-06	2.39E-10	1.45E-10	1.35E-10	3.64E-10	3.70E-06	4.95E-09
88.5	1.00E-05	2.94E-09	4.32E-06	2.42E-10	1.47E-10	1.36E-10	3.69E-10	3.73E-06	5.05E-09
89	1.00E-05	2.95E-09	4.34E-06	2.44E-10	1.48E-10	1.37E-10	3.73E-10	3.76E-06	5.10E-09
89.5	1.00E-05	2.95E-09	4.34E-06	2.47E-10	1.50E-10	1.39E-10	3.78E-10	3.79E-06	5.24E-09
90	1.00E-05	2.95E-09	4.34E-06	2.50E-10	1.52E-10	1.41E-10	3.83E-10	3.74E-06	5.42E-09
90.5	1.00E-05	2.96E-09	4.34E-06	2.53E-10	1.54E-10	1.43E-10	3.88E-10	3.80E-06	5.61E-09
91	1.00E-05	2.96E-09	4.34E-06	2.56E-10	1.57E-10	1.45E-10	3.92E-10	3.71E-06	5.66E-09
91.5	1.00E-05	2.97E-09	4.33E-06	2.60E-10	1.59E-10	1.47E-10	3.97E-10	3.75E-06	5.72E-09
92	1.00E-05	2.98E-09	4.34E-06	2.63E-10	1.61E-10	1.49E-10	4.01E-10	3.72E-06	5.86E-09
92.5	1.00E-05	2.99E-09	4.34E-06	2.67E-10	1.64E-10	1.52E-10	4.06E-10	3.78E-06	5.94E-09
93	1.00E-05	3.00E-09	4.35E-06	2.71E-10	1.66E-10	1.54E-10	4.11E-10	3.83E-06	6.15E-09
93.5	1.00E-05	3.01E-09	4.35E-06	2.75E-10	1.69E-10	1.57E-10	4.16E-10	3.83E-06	6.22E-09
94	1.00E-05	3.02E-09	4.35E-06	2.79E-10	1.72E-10	1.60E-10	4.20E-10	3.84E-06	6.32E-09
94.5	1.00E-05	3.04E-09	4.35E-06	2.83E-10	1.75E-10	1.62E-10	4.24E-10	3.86E-06	6.35E-09
95	1.00E-05	3.06E-09	4.36E-06	2.87E-10	1.78E-10	1.65E-10	4.29E-10	3.86E-06	6.47E-09
95.5	1.00E-05	3.09E-09	4.35E-06	2.92E-10	1.81E-10	1.68E-10	4.33E-10	3.85E-06	1.19E-06
96	1.00E-05	3.11E-09	4.35E-06	2.97E-10	1.84E-10	1.71E-10	4.38E-10	3.82E-06	1.20E-06
96.5	1.00E-05	3.15E-09	4.36E-06	3.02E-10	1.88E-10	1.75E-10	4.42E-10	3.82E-06	1.21E-06
97	1.00E-05	3.18E-09	4.37E-06	3.07E-10	1.91E-10	1.78E-10	4.47E-10	3.83E-06	1.22E-06
97.5	1.00E-05	3.23E-09	4.39E-06	3.12E-10	1.95E-10	1.81E-10	4.50E-10	3.81E-06	1.24E-06
98	1.00E-05	3.27E-09	4.39E-06	3.18E-10	1.99E-10	1.85E-10	4.54E-10	3.79E-06	1.26E-06
98.5	1.00E-05	3.33E-09	4.39E-06	3.24E-10	2.02E-10	1.89E-10	4.59E-10	3.81E-06	1.27E-06
99	1.00E-05	3.38E-09	4.39E-06	3.29E-10	2.06E-10	1.92E-10	4.63E-10	3.82E-06	1.29E-06
99.5	1.00E-05	3.44E-09	4.39E-06	3.36E-10	2.11E-10	1.96E-10	4.68E-10	3.86E-06	1.30E-06
100	1.00E-05	3.49E-09	4.39E-06	3.42E-10	2.15E-10	2.01E-10	4.71E-10	3.86E-06	1.31E-06

Appendix A

Table A-6: Electrical leakage current measurement of TSV test structure with 5 μ m width and 100 μ m trench depth at different temperatures (50-200 °C) [See Fig 4.17]:

V	I _{50C}	I _{100C}	I _{150C}	I _{200C}	V	I _{50C}	I _{100C}	I _{150C}	I _{200C}
0.1	7.70E-09	4.49E-08	1.28E-07	7.59E-07	5.1	7.58E-07	3.78E-06	8.89E-06	1.00E-05
0.2	1.56E-08	9.05E-08	2.57E-07	1.51E-06	5.2	7.83E-07	3.88E-06	9.11E-06	1.00E-05
0.3	2.36E-08	1.37E-07	3.87E-07	2.28E-06	5.3	8.06E-07	3.96E-06	9.34E-06	1.00E-05
0.4	3.17E-08	1.84E-07	5.16E-07	3.03E-06	5.4	8.30E-07	4.04E-06	9.59E-06	1.00E-05
0.5	4.00E-08	2.32E-07	6.46E-07	3.80E-06	5.5	8.54E-07	4.14E-06	9.82E-06	1.00E-05
0.6	4.86E-08	2.81E-07	7.77E-07	4.57E-06	5.6	8.80E-07	4.25E-06	1.00E-05	1.00E-05
0.7	5.75E-08	3.31E-07	9.09E-07	5.34E-06	5.7	9.06E-07	4.35E-06	1.00E-05	1.00E-05
0.8	6.63E-08	3.82E-07	1.04E-06	6.13E-06	5.8	9.32E-07	4.45E-06	1.00E-05	1.00E-05
0.9	7.57E-08	4.35E-07	1.18E-06	6.91E-06	5.9	9.57E-07	4.56E-06	1.00E-05	1.00E-05
1	8.54E-08	4.89E-07	1.32E-06	7.71E-06	6	9.80E-07	4.66E-06	1.00E-05	1.00E-05
1.1	9.53E-08	5.43E-07	1.45E-06	8.52E-06	6.1	1.01E-06	4.77E-06	1.00E-05	1.00E-05
1.2	1.06E-07	5.99E-07	1.60E-06	9.35E-06	6.2	1.03E-06	4.88E-06	1.00E-05	1.00E-05
1.3	1.17E-07	6.57E-07	1.74E-06	1.00E-05	6.3	1.06E-06	4.99E-06	1.00E-05	1.00E-05
1.4	1.27E-07	7.16E-07	1.88E-06	1.00E-05	6.4	1.09E-06	5.10E-06	1.00E-05	1.00E-05
1.5	1.38E-07	7.77E-07	2.03E-06	1.00E-05	6.5	1.11E-06	5.22E-06	1.00E-05	1.00E-05
1.6	1.50E-07	8.38E-07	2.18E-06	1.00E-05	6.6	1.14E-06	5.34E-06	1.00E-05	1.00E-05
1.7	1.61E-07	9.01E-07	2.34E-06	1.00E-05	6.7	1.16E-06	5.46E-06	1.00E-05	1.00E-05
1.8	1.73E-07	9.64E-07	2.49E-06	1.00E-05	6.8	1.19E-06	5.56E-06	1.00E-05	1.00E-05
1.9	1.85E-07	1.03E-06	2.65E-06	1.00E-05	6.9	1.22E-06	5.66E-06	1.00E-05	1.00E-05
2	1.97E-07	1.10E-06	2.82E-06	1.00E-05	7	1.25E-06	5.76E-06	1.00E-05	1.00E-05
2.1	2.11E-07	1.17E-06	2.98E-06	1.00E-05	7.1	1.28E-06	5.89E-06	1.00E-05	1.00E-05
2.2	2.25E-07	1.23E-06	3.14E-06	1.00E-05	7.2	1.31E-06	6.01E-06	1.00E-05	1.00E-05
2.3	2.39E-07	1.30E-06	3.31E-06	1.00E-05	7.3	1.34E-06	6.13E-06	1.00E-05	1.00E-05
2.4	2.53E-07	1.38E-06	3.47E-06	1.00E-05	7.4	1.37E-06	6.26E-06	1.00E-05	1.00E-05
2.5	2.67E-07	1.45E-06	3.64E-06	1.00E-05	7.5	1.39E-06	6.38E-06	1.00E-05	1.00E-05
2.6	2.82E-07	1.52E-06	3.82E-06	1.00E-05	7.6	1.43E-06	6.50E-06	1.00E-05	1.00E-05
2.7	2.98E-07	1.60E-06	4.00E-06	1.00E-05	7.7	1.46E-06	6.62E-06	1.00E-05	1.00E-05
2.8	3.14E-07	1.67E-06	4.17E-06	1.00E-05	7.8	1.49E-06	6.73E-06	1.00E-05	1.00E-05
2.9	3.32E-07	1.75E-06	4.35E-06	1.00E-05	7.9	1.52E-06	6.85E-06	1.00E-05	1.00E-05
3	3.48E-07	1.83E-06	4.54E-06	1.00E-05	8	1.55E-06	6.97E-06	1.00E-05	1.00E-05
3.1	3.62E-07	1.91E-06	4.72E-06	1.00E-05	8.1	1.58E-06	7.10E-06	1.00E-05	1.00E-05
3.2	3.82E-07	2.00E-06	4.91E-06	1.00E-05	8.2	1.61E-06	7.21E-06	1.00E-05	1.00E-05
3.3	3.99E-07	2.08E-06	5.09E-06	1.00E-05	8.3	1.65E-06	7.34E-06	1.00E-05	1.00E-05
3.4	4.18E-07	2.17E-06	5.29E-06	1.00E-05	8.4	1.68E-06	7.47E-06	1.00E-05	1.00E-05
3.5	4.38E-07	2.26E-06	5.48E-06	1.00E-05	8.5	1.71E-06	7.59E-06	1.00E-05	1.00E-05
3.6	4.58E-07	2.35E-06	5.67E-06	1.00E-05	8.6	1.74E-06	7.74E-06	1.00E-05	1.00E-05
3.7	4.75E-07	2.44E-06	5.87E-06	1.00E-05	8.7	1.77E-06	7.89E-06	1.00E-05	1.00E-05
3.8	4.93E-07	2.53E-06	6.07E-06	1.00E-05	8.8	1.80E-06	8.00E-06	1.00E-05	1.00E-05
3.9	5.13E-07	2.62E-06	6.28E-06	1.00E-05	8.9	1.84E-06	8.13E-06	1.00E-05	1.00E-05
4	5.30E-07	2.72E-06	6.48E-06	1.00E-05	9	1.87E-06	8.28E-06	1.00E-05	1.00E-05
4.1	5.49E-07	2.81E-06	6.69E-06	1.00E-05	9.1	1.91E-06	8.43E-06	1.00E-05	1.00E-05
4.2	5.69E-07	2.90E-06	6.90E-06	1.00E-05	9.2	1.94E-06	8.57E-06	1.00E-05	1.00E-05
4.3	5.88E-07	3.01E-06	7.11E-06	1.00E-05	9.3	1.97E-06	8.71E-06	1.00E-05	1.00E-05
4.4	6.09E-07	3.08E-06	7.33E-06	1.00E-05	9.4	2.01E-06	8.84E-06	1.00E-05	1.00E-05
4.5	6.30E-07	3.19E-06	7.54E-06	1.00E-05	9.5	2.05E-06	8.99E-06	1.00E-05	1.00E-05
4.6	6.50E-07	3.29E-06	7.76E-06	1.00E-05	9.6	2.09E-06	9.12E-06	1.00E-05	1.00E-05
4.7	6.72E-07	3.39E-06	7.98E-06	1.00E-05	9.7	2.12E-06	9.26E-06	1.00E-05	1.00E-05
4.8	6.91E-07	3.47E-06	8.21E-06	1.00E-05	9.8	2.16E-06	9.40E-06	1.00E-05	1.00E-05
4.9	7.11E-07	3.58E-06	8.43E-06	1.00E-05	9.9	2.20E-06	9.55E-06	1.00E-05	1.00E-05
5	7.32E-07	3.68E-06	8.66E-06	1.00E-05	10	2.24E-06	9.68E-06	1.00E-05	1.00E-05

Electrical measurement database for Chapter 7

Table A-7: Electrical leakage current measurement results at room temperature (22 °C) and 100 °C to study the impact of etch profile and sidewall defects due to silicon via etch process on dielectric conduction mechanism. The results are presented in Fig 7.4-7.13)

V	Recipe-A1		Recipe-C1		Recipe-F1		Recipe-E1		Recipe-B1	
	I _{RT}	I _{100C}	I _{RT}	I _{100C}	I _{RT}	I _{100C}	I _{RT}	I _{100C}	I _{RT}	I _{100C}
0.5	2.32E-13	4.38E-13	1.96E-08	4.53E-09	1.34E-12	5.00E-14	3.84E-12	4.12E-12	1.29E-11	1.81E-10
1	6.50E-13	1.32E-12	5.61E-08	1.90E-08	2.07E-12	3.90E-12	3.88E-12	4.17E-12	2.71E-11	3.36E-10
1.5	9.45E-13	1.99E-12	7.00E-08	3.02E-08	2.48E-12	7.21E-12	3.82E-12	4.31E-12	4.60E-11	5.00E-10
2	1.21E-12	2.70E-12	8.20E-08	4.95E-08	2.68E-12	1.05E-11	3.64E-12	4.46E-12	6.39E-11	7.01E-10
2.5	1.46E-12	3.35E-12	9.50E-08	9.38E-08	3.02E-12	1.37E-11	3.55E-12	4.57E-12	8.98E-11	9.15E-10
3	1.70E-12	4.02E-12	1.11E-07	1.54E-07	3.25E-12	1.68E-11	3.53E-12	4.69E-12	1.22E-10	1.14E-09
3.5	1.89E-12	5.05E-12	1.26E-07	2.60E-07	3.35E-12	1.97E-11	3.38E-12	4.83E-12	1.63E-10	1.38E-09
4	2.10E-12	5.65E-12	1.42E-07	3.14E-07	3.70E-12	2.22E-11	3.25E-12	4.95E-12	2.04E-10	1.76E-09
4.5	2.32E-12	6.01E-12	1.61E-07	3.61E-07	3.98E-12	2.42E-11	3.16E-12	5.03E-12	2.36E-10	2.09E-09
5	2.52E-12	6.53E-12	1.82E-07	4.80E-07	4.30E-12	2.54E-11	2.98E-12	5.19E-12	2.69E-10	2.52E-09
5.5	2.76E-12	7.14E-12	2.08E-07	4.98E-07	4.70E-12	2.68E-11	3.08E-12	5.31E-12	2.98E-10	2.92E-09
6	2.97E-12	7.80E-12	2.39E-07	5.31E-07	5.06E-12	2.85E-11	3.10E-12	5.51E-12	3.56E-10	3.26E-09
6.5	3.19E-12	8.52E-12	2.71E-07	5.70E-07	5.57E-12	3.02E-11	3.06E-12	5.65E-12	4.14E-10	3.71E-09
7	3.45E-12	9.30E-12	3.11E-07	6.08E-07	6.06E-12	3.25E-11	3.09E-12	5.81E-12	4.65E-10	4.21E-09
7.5	3.74E-12	1.01E-11	3.56E-07	6.53E-07	6.78E-12	3.48E-11	2.99E-12	6.01E-12	5.29E-10	4.75E-09
8	4.00E-12	1.11E-11	4.10E-07	7.40E-07	7.32E-12	3.72E-11	3.06E-12	6.15E-12	5.79E-10	5.21E-09
8.5	4.31E-12	1.20E-11	4.66E-07	8.21E-07	7.68E-12	4.00E-11	2.99E-12	6.36E-12	6.45E-10	5.87E-09
9	4.63E-12	1.30E-11	5.24E-07	1.19E-06	8.40E-12	4.33E-11	2.93E-12	6.57E-12	6.87E-10	6.64E-09
9.5	4.93E-12	1.41E-11	5.93E-07	1.31E-06	9.07E-12	4.64E-11	2.95E-12	6.76E-12	7.28E-10	7.46E-09
10	5.32E-12	1.53E-11	6.74E-07	1.44E-06	9.58E-12	5.07E-11	2.99E-12	6.94E-12	7.96E-10	8.46E-09
10.5	5.70E-12	1.67E-11	7.53E-07	1.57E-06	1.03E-11	5.58E-11	3.13E-12	7.17E-12	7.84E-10	9.33E-09
11	6.09E-12	1.82E-11	8.51E-07	1.71E-06	1.11E-11	5.94E-11	3.02E-12	7.34E-12	7.88E-10	1.04E-08
11.5	6.54E-12	1.99E-11	9.71E-07	1.87E-06	1.22E-11	6.33E-11	3.03E-12	7.61E-12	8.84E-10	1.16E-08
12	7.07E-12	2.18E-11	1.10E-06	2.02E-06	1.35E-11	6.73E-11	3.09E-12	7.91E-12	9.03E-10	1.28E-08
12.5	7.38E-12	2.33E-11	1.24E-06	2.20E-06	1.47E-11	7.19E-11	3.09E-12	8.17E-12	9.81E-10	1.37E-08
13	7.91E-12	2.49E-11	1.42E-06	2.37E-06	1.61E-11	7.71E-11	3.02E-12	8.49E-12	1.13E-09	1.50E-08
13.5	8.43E-12	2.68E-11	1.59E-06	2.61E-06	1.77E-11	8.24E-11	3.12E-12	8.79E-12	1.22E-09	1.62E-08
14	9.00E-12	2.89E-11	1.78E-06	2.83E-06	1.98E-11	8.73E-11	3.09E-12	9.08E-12	1.36E-09	1.78E-08
14.5	9.63E-12	3.10E-11	1.97E-06	3.06E-06	2.21E-11	9.30E-11	3.09E-12	9.49E-12	1.48E-09	1.97E-08
15	1.03E-11	3.32E-11	2.22E-06	3.32E-06	2.31E-11	9.99E-11	3.12E-12	9.91E-12	1.67E-09	2.15E-08
15.5	1.11E-11	3.57E-11	2.46E-06	3.60E-06	2.75E-11	1.07E-10	3.14E-12	1.03E-11	1.83E-09	2.30E-08
16	1.19E-11	3.84E-11	2.71E-06	3.89E-06	2.79E-11	1.15E-10	3.13E-12	1.06E-11	2.08E-09	2.45E-08
16.5	1.27E-11	4.12E-11	3.00E-06	4.36E-06	3.00E-11	1.24E-10	3.29E-12	1.10E-11	2.30E-09	2.70E-08
17	1.37E-11	4.43E-11	3.32E-06	4.51E-06	3.30E-11	1.33E-10	3.20E-12	1.15E-11	2.50E-09	2.77E-08
17.5	1.48E-11	4.76E-11	3.64E-06	4.88E-06	3.54E-11	1.43E-10	3.23E-12	1.20E-11	2.68E-09	2.95E-08
18	1.59E-11	5.11E-11	4.05E-06	5.23E-06	3.62E-11	1.53E-10	3.29E-12	1.24E-11	3.02E-09	3.21E-08
18.5	1.71E-11	5.48E-11	4.46E-06	5.59E-06	4.01E-11	1.64E-10	3.35E-12	1.29E-11	3.42E-09	3.50E-08

Appendix A

19	1.83E-11	5.90E-11	4.92E-06	6.00E-06	4.11E-11	1.75E-10	3.32E-12	1.34E-11	3.85E-09	3.70E-08
19.5	1.92E-11	6.34E-11	5.37E-06	6.42E-06	4.34E-11	1.89E-10	3.40E-12	1.39E-11	4.18E-09	3.96E-08
20	2.07E-11	6.80E-11	5.83E-06	6.89E-06	4.60E-11	2.02E-10	3.44E-12	1.46E-11	4.15E-09	4.18E-08
20.5	2.30E-11	7.30E-11	6.32E-06	7.41E-06	5.05E-11	2.17E-10	3.44E-12	1.51E-11	4.49E-09	4.42E-08
21	2.45E-11	7.84E-11	7.01E-06	7.88E-06	5.26E-11	2.33E-10	3.41E-12	1.58E-11	4.94E-09	4.70E-08
21.5	2.60E-11	8.41E-11	7.65E-06	8.50E-06	5.56E-11	2.50E-10	3.47E-12	1.65E-11	5.47E-09	4.97E-08
22	2.74E-11	9.02E-11	8.34E-06	9.11E-06	5.96E-11	2.66E-10	3.30E-12	1.72E-11	5.91E-09	5.29E-08
22.5	2.90E-11	9.66E-11	9.27E-06	9.71E-06	6.30E-11	2.84E-10	3.40E-12	1.80E-11	6.32E-09	5.66E-08
23	3.15E-11	1.04E-10	1.01E-05	1.03E-05	6.55E-11	3.05E-10	3.46E-12	1.89E-11	6.90E-09	5.97E-08
23.5	3.35E-11	1.12E-10	1.09E-05	1.09E-05	7.08E-11	3.25E-10	3.49E-12	1.96E-11	7.42E-09	6.32E-08
24	3.58E-11	1.20E-10	1.19E-05	1.17E-05	7.16E-11	3.50E-10	3.56E-12	2.05E-11	7.84E-09	6.65E-08
24.5	3.80E-11	1.29E-10	1.29E-05	1.24E-05	7.50E-11	3.71E-10	3.65E-12	2.14E-11	8.51E-09	6.98E-08
25	4.07E-11	1.38E-10	1.42E-05	1.32E-05	7.88E-11	4.01E-10	3.77E-12	2.24E-11	9.08E-09	7.32E-08
25.5	4.37E-11	1.47E-10	1.51E-05	1.41E-05	8.34E-11	4.31E-10	3.89E-12	2.35E-11	9.72E-09	7.71E-08
26	4.68E-11	1.58E-10	1.65E-05	1.49E-05	8.77E-11	4.50E-10	3.89E-12	2.46E-11	1.08E-08	7.88E-08
26.5	5.03E-11	1.69E-10	1.76E-05	1.59E-05	9.21E-11	4.85E-10	3.89E-12	2.58E-11	1.21E-08	8.18E-08
27	5.45E-11	1.80E-10	1.87E-05	1.68E-05	9.74E-11	5.17E-10	3.98E-12	2.71E-11	1.28E-08	8.58E-08
27.5	5.82E-11	1.93E-10	1.99E-05	1.77E-05	1.01E-10	5.48E-10	3.86E-12	2.83E-11	1.37E-08	8.96E-08
28	6.29E-11	2.06E-10	2.13E-05	1.87E-05	1.07E-10	5.81E-10	3.84E-12	2.97E-11	1.46E-08	9.89E-08
28.5	6.65E-11	2.21E-10	2.25E-05	1.98E-05	1.12E-10	6.25E-10	3.89E-12	3.11E-11	1.56E-08	1.03E-07
29	7.14E-11	2.36E-10	2.39E-05	2.06E-05	1.16E-10	6.65E-10	4.04E-12	3.26E-11	1.65E-08	1.07E-07
29.5	7.64E-11	2.53E-10	2.57E-05	2.16E-05	1.22E-10	7.09E-10	4.15E-12	3.43E-11	1.79E-08	1.13E-07
30	8.19E-11	2.71E-10	2.69E-05	2.25E-05	1.28E-10	7.57E-10	4.14E-12	3.60E-11	1.97E-08	1.18E-07
30.5	8.81E-11	2.90E-10	2.84E-05	2.37E-05	1.33E-10	8.01E-10	4.26E-12	3.78E-11	2.13E-08	1.23E-07
31	9.54E-11	3.10E-10	2.95E-05	2.48E-05	1.42E-10	8.51E-10	4.39E-12	3.96E-11	2.25E-08	1.21E-07
31.5	1.01E-10	3.32E-10	3.08E-05	2.60E-05	1.50E-10	8.96E-10	4.42E-12	4.14E-11	2.38E-08	1.30E-07
32	1.09E-10	3.57E-10	3.29E-05	2.73E-05	1.60E-10	9.79E-10	4.39E-12	4.35E-11	2.56E-08	1.36E-07
32.5	1.17E-10	3.81E-10	3.45E-05	2.86E-05	1.65E-10	1.03E-09	4.42E-12	4.55E-11	2.79E-08	1.45E-07
33	1.26E-10	4.07E-10	3.51E-05	2.99E-05	1.72E-10	1.12E-09	4.52E-12	4.77E-11	2.87E-08	1.52E-07
33.5	1.38E-10	4.36E-10	3.64E-05	3.12E-05	1.80E-10	1.16E-09	4.43E-12	5.00E-11	3.09E-08	1.59E-07
34	1.47E-10	4.66E-10	3.80E-05	3.23E-05	1.87E-10	1.22E-09	4.48E-12	5.23E-11	3.34E-08	1.64E-07
34.5	1.56E-10	4.97E-10	3.95E-05	3.39E-05	1.94E-10	1.30E-09	4.60E-12	5.51E-11	3.51E-08	1.71E-07
35	1.67E-10	5.31E-10	4.12E-05	3.53E-05	2.02E-10	1.39E-09	4.58E-12	5.77E-11	3.77E-08	1.77E-07
35.5	1.80E-10	5.69E-10	4.34E-05	3.64E-05	2.17E-10	1.45E-09	4.57E-12	6.07E-11	3.98E-08	1.78E-07
36	1.95E-10	6.10E-10	4.53E-05	3.81E-05	2.25E-10	1.53E-09	4.68E-12	6.35E-11	4.15E-08	1.88E-07
36.5	2.04E-10	6.53E-10	4.78E-05	3.93E-05	2.28E-10	1.62E-09	4.75E-12	6.68E-11	4.39E-08	1.95E-07
37	2.16E-10	6.96E-10	5.03E-05	4.05E-05	2.61E-10	1.72E-09	4.85E-12	7.02E-11	4.57E-08	2.07E-07
37.5	2.30E-10	7.46E-10	5.31E-05	4.13E-05	3.13E-10	1.80E-09	4.97E-12	7.37E-11	4.97E-08	2.15E-07
38	2.46E-10	8.03E-10	5.58E-05	4.29E-05	2.68E-10	1.91E-09	4.95E-12	7.73E-11	5.17E-08	2.22E-07
38.5	2.64E-10	8.60E-10	5.77E-05	4.45E-05	2.72E-10	2.04E-09	4.84E-12	8.10E-11	5.45E-08	2.32E-07
39	2.81E-10	9.19E-10	5.89E-05	4.65E-05	2.82E-10	2.14E-09	4.98E-12	8.52E-11	5.65E-08	2.41E-07
39.5	3.02E-10	9.82E-10	6.11E-05	5.02E-05	2.96E-10	2.25E-09	4.96E-12	8.94E-11	5.84E-08	2.49E-07
40	3.21E-10	1.06E-09	6.39E-05	5.77E-05	3.06E-10	2.37E-09	5.09E-12	9.37E-11	6.23E-08	2.55E-07

Table A-8: Measurement of variations in dielectric, Ti/Cu metallization and sidewall roughness at top and bottom of the 50 μ m diameter TSV test structure measured by SEM cross-section analysis:

Wafer #	TEOS oxide thickness (μ m)		Cu/Ti thickness (μ m)		Sidewall roughness (nm)		Etch process
	Top	Bottom	Top	Bottom	Top	Bottom	
1	1.19-1.29	0.27-0.30	1.132	0.27-0.33	50-60	< 30	A1
2	0.88-1.04	0.13-0.17	0.25-0.32	0.18-0.20	200-226	80-100	C1
3	1.14-1.29	0.39-0.48	0.80-1.0	0.18-0.21	20-30	100-138	F1
4	1.13-1.28	0.41-0.44	0.85-0.90	0.19-0.22	0.8-1.0 μ m	< 30	E1
5	0.50-1.04	0.30-0.32	0.15-0.62	0.10-0.14	3-4 μ m	< 30	B1

PUBLICATIONS

Journal Papers

- [1] N. Ranganathan, K. Prasad, Liao Ebin and N. Balasubramanian, Development of dual-etch via tapering process for through-silicon interconnection, Sensors and Actuators, Physical A, Volume 139, Issues 1-2, 12 September 2007, pp 323-329.
- [2] N. Ranganathan, K Prasad, N Balasubramanian and K L Pey, Study of thermo-mechanical stress and its impact on through silicon vias, Journal of Micromechanics and Microengineering, 18 (2008) 075018 (13 pp)
- [3] N Ranganathan, D Y Lee, L Ebin, N Balasubramanian, K Prasad and K L Pey, Development of tapered silicon micro-micromachining process for 3-D Microsystems Packaging, Journal of Micromechanics and Microengineering, Volume 18, Number 11, November 2008 (8pp).
- [4] N.Ranganathan, Liao Ebin, Linn Linn, L.W. Sheng, O.K.Navas, V.Kripesh and N.Balasubramanian, Integration of high aspect ratio tapered silicon via for silicon carrier fabrication, IEEE Transaction on Advanced Packaging Vol. 32, No. 1, Feb. 2009, pp. 62-71.
- [5] N. Ranganathan, D.Y. Lee, Linn Linn, G.Q. Lo, K. Prasad and K.L. Pey, Impact of Bosch etch process on deep silicon copper vias, Submitted to IEEE Transaction on Advanced Packaging (Manuscript submission under review).
- [6] N. Ranganathan, A.Malar, D.Y.Lee, K. Prasad and K.L. Pey, Development and characterization of tapered silicon etch process by topography modeling. (Submitted to Journal of Microelectronics and Electronic Packaging (Manuscript accepted for publication)).

International Conference Publications

- [7] N. Ranganathan, K. Prasad, N. Balasubramanian, Zhou Qiaoer and S. C. Hwee, High aspect ratio through-wafer interconnect for three dimensional integrated circuits, Proceedings of 55th Electronic Components and Technology Conference, Orlando, USA – May/June 2005, pp 343-348.
- [8] N. Ranganathan, Jiang Ning, Liao Ebin, C.S.Premachandran, K. Prasad and N.Balasubramanian, Through-wafer interconnection by deep damascene process for MEMS and 3D wafer level packaging, 7th Electronic Packaging Technology Conference, 7-9 Dec 2005, Singapore.
- [9] N. Ranganathan¹, D.Y. Lee, C.S. Soh, Liao Ebin, K. Prasad and N. Balasubramanian, Development of tapered deep silicon via etch technology for 3-D silicon Microsystems, Asia-Pacific Conference of Transducers and Micro-Nano Technology (APCOT 2006), Marina Mandarin Hotel, Singapore, 25-28 June 2006, pp. 1-4.
- [10] N. Ranganathan, Liao Ebin, Lee Dayong, Soh Chee Seng, K. Prasad and N. Balasubramanian, Development of novel deep silicon tapered via etch process for through-silicon interconnection in 3-D integrated systems, 56th Electronic Components and Technology Conference, 30 May-2 June 2006, pp 383–387.
- [11] N. Ranganathan, Liao Ebin; N. Balasubramanian, K. Prasad, K and K.L. Pey, Development and characterization of silicon via tapering process for 3D System in Packaging application, 14th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2007), 11-13 July 2007, pp. 296 – 300.

-
- [12] N.Ranganathan, Liao Ebin, Linn Linn, Lee Wen Sheng Vincent, O.K.Navas, V.Kripesh and N.Balasubramanian, Integration of high aspect ratio tapered silicon via for through-silicon interconnection, 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, May 27-30, 2008, pp. 859-865.

International Conference Presentations

- [13]. N.Ranganathan, K. Prasad, Chin Hwee, Zhou Qiaoer and N.Balasubramanian, “Characterization of deep silicon damascene copper via for 3D integrated circuits”, ICMAT, 3-8th July 2005, Singapore.
- [14]. N.Ranganathan, “Three dimensional interconnection technology-From hype to reality”, Invited talk at Workshop on “Technology of Si - based Nanodevices”, 24th Feb. 2006, NTU Singapore.
- [15]. N. Ranganathan, K. Prasad , Lee Dayong and N.Balasubramanian, “A deep silicon tapered via etch process for through-wafer interconnects in three dimensional integrated circuits”, MRS Spring 2006, USA.

BIBLIOGRAPHY

- [1] Mauro J. Kobrinsky et al, Intel Technology Journal, Vol 8, Issue 2, 2004, pp. 129-142.
- [2] G. Chandra, P. Kapur and K. C. Saraswat, Proc. IEEE Int. Interconnect Tech. Conf., June 2002, San Francisco, pp. 164-166.
- [3] ITRS 2008 Roadmap Update(<http://www.itrs.net/Links/2008ITRS/Home2008.htm>)
- [4] J.D. Meindl, Computing in Science & Engineering Vol. 5, Issue 1, Jan.-Feb. 2003, pp. 20 – 24.
- [5] R. R. Johnson, Multichip Module: Next generation packages, IEEE Spectrum, Vol. 27(3), 1990, pp. 34 48.
- [6] Jian-Qiang Lu, Ken Rose and Susan Vitkavage, Future Fab International, July 2007, Issue 23 (<http://www.future-fab.com/>)
- [7] S. J. Koester et al, IBM J. Res. & Dev., Vol. 52(6), Nov. 2008, pp. 583-597.
- [8] Guarini, K.W et al, International Electron Devices Meeting, 8-11 Dec. 2002, pp. 943-945.
- [9] K. Takahashi, M. Hoshino, H. Yonemura, M. Tomisaka, M. Sunohara, M. Tanioka, T. Sato, K. Kojima and H. Terao, 51st Electronic Components and Technology Conference, 29 May-1 June 2001, pp.541 - 546.
- [10] R. Reif, A. Fan, Kuan-Neng Chen and S. Das, International Symposium on Quality Electronic Design, 2002, 18-21 March 2002, pp:33 – 37.
- [11] Chien-Wei Chien et al, 57th Electronic Components and Technology Conference, May 29 June 1, 2007, pp. 305 – 310.

- [12] M.J. Wolf, P. Ramm, A. Klumpp and H. Reichl, Dans Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS - DTIP 2008, Nice : France (2008).
- [13] J. Bhardwaj, H. Ashraf, and A. McQuarrie, Annual Meeting of the Electrochemical Society, Montreal, Quebec, Canada, May 4-9, 1997.
- [14] T. Wells, M.M El-Gomati, J. Wood and S. Johnson, 9th International Vacuum Microelectronics Conference, 1996. (IVMC'96), 7-12 July 1996, pp. 349–353.
- [15] Alexey M.Rodin, Joseph Callaghan and Niall Brennan, Available at: www.xsil.com/xsil/Files/xm-08-005.0_Paper_DP_Vias.pdf
- [16] B Tan, Journal of Micromechanics and Microengineering, 2006, 16, pp. 109-112.
- [17] Wensink, H, Berenschot, J.W, Jansen, H.V and Elwenspoek, M.C, The Thirteenth Annual International Conference on Micro Electro Mechanical Systems (MEMS 2000), 23-27 Jan 2000, pp.769-774.
- [18] J. Gobet, J.-P. Thiebaud, F. Crevoisier, and J.M. Moret, Proceedings of the SPIE – The International Society for Optical Engineering, 29 September 1997, Austin, TX, USA, Vol. 3223, pp. 17-25.
- [19] Ha-Duong Ngo et al, Journal of Physics: Conference Series, 2006, 34, pp. 271-276.
- [20] K. Powell, S. Burgess, T. Wilby, R. Hyndman, J. Callahan, International Interconnect Technology Conference (IITC 2008), 1-4 June, 2008, pp. 40-42.
- [21] Martin J. Walker, Proc. SPIE, Edinburgh, UK, 30 May, 2001, Vol. 4407, 89-99 2001.
- [22] Frank Engel Rasmussen, Ph.D Thesis, Technical University of Denmark, 31st October 2003.

- [23] N. Ranganathan, K. Prasad, N. Balasubramanian, Zhou Qiaoer and S. C. Hwee, Proceedings of 55th Electronic Components and Technology Conference, Orlando, USA – May/June 2005, pp 343-348.
- [24] N. Ranganathan, Jiang Ning, Liao Ebin, C.S.Premachandran, K. Prasad and N.Balasubramanian, 7th Electronic Packaging Technology Conference, 7-9 Dec 2005, Singapore.
- [25] N. Ranganathan, K Prasad, N Balasubramanian and K L Pey, J. Micromech. Microeng. 18 (2008) 075018 (13 pp)
- [26] N. Ranganathan¹, D.Y. Lee, C.S. Soh, Liao Ebin, K. Prasad and N. Balasubramanian, Asia-Pacific Conference of Transducers and Micro-Nano Technology (APCOT 2006), Marina Mandarin Hotel, Singapore, 25-28 June 2006, pp 1-4.
- [27] N. Ranganathan, Liao Ebin, Lee Dayong, Soh Chee Seng, K. Prasad and N. Balasubramanian, 56th Electronic Components and Technology Conference, 30 May-2 June 2006, pp 383 – 387.
- [28] N. Ranganathan, K. Prasad, Liao Ebin and N. Balasubramanian, Sensors and Actuators, Physical A, Volume 139, Issues 1-2, 12 September 2007, pp 323-329.
- [29] N. Ranganathan, Liao Ebin; N. Balasubramanian, K. Prasad, K and K.L. Pey, 14th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2007), 11-13 July 2007, pp. 296 – 300.
- [30] N Ranganathan, D Y Lee, L Ebin, N Balasubramanian, K Prasad and K L Pey, Journal of Micromechanics and Microengineering, Volume 18, Number 11, November 2008 (8pp).

- [31] N.Ranganathan, Liao Ebin, Linn Linn, L.W. Sheng, O.K.Navas, V.Kripesh and N.Balasubramanian, IEEE Transaction on Advanced Packaging (Accepted for publication in Feb 2009)
- [32] Navas Khan et al, 58th Electronic Components and Technology Conference (ECTC 2008), 27-30 May, 2008, pp: 550 – 555.
- [33] Petersen, K.E, Proceedings of the IEEE, May 1982, Vol. 70, Issue: 5, pp 420- 457.
- [34] T.J. Hubbard, PhD Thesis, California Institute of Technology, Pasadena, CA, 1994.
- [35] K. Sakuma et al, IBM J. Res. & Dev, Vol. 52, No. 6, November 2008, pp:611-622.
- [36] K. Ueno et al, Electron Devices Meeting, 10-13 Dec. 2000, pp:265 – 268.
- [37] Duan Xue Feng, MS Thesis, Mc Gill University, Quebec, Canada, 1999.
- [38] A.G. Andreou and J. Wang, MEMS course 520/530/580.495, John Hopkins University.
- [39] Gohji Nakagawa, Kazunori Miura, Seimi Sasaki, and Mitsuhiro Yano, Journal of Lightwave Technology, Vol. 14, No. 6, June 1996, pp 1519-1523.
- [40] Arnd Kilian et al, 19th Annual Meeting of the IEEE Lasers and Electro-Optics Society, 2006, Oct. 2006, pp102 – 103.
- [41] www.aaerospace.com/content/download/AAC_XiVIA_presentation_081015_final.pdf
- [42] G. S. Oehrlein et al, IBM J. Res and Dev, Vol. 43 (1/2) 1999.
- [43] M. Armacost et al, IBM J. Res and Dev, Vol. 43 (1/2) 1999
- [44] Introduction to Plasma Technology (<http://www.crystec.com/triplae.htm>)
- [45] <http://www.oxfordplasma.de/technols/rie.htm>
- [46] D Misra et al Semicond. Sci. Technol. Vol.5, Number 3, March 1990, 229-236.

- [47] Anthony Ricci, Dry Etch Process Application Note (ABG-106-0405), Application bulletin from Pall Microelectronics (www.pall.com/articles_MicroE_38439.asp)
- [48] www.tu-harburg.de/ht/deutsch/lehre/pdf/plasma_etching.pdf
- [49] F. Laermer, A. Schilp, German Pat.; DE 4 241 045 granted on 26 May 1994 (US Pat. 5 501 893 granted on 26 March 1996)
- [50] M. Offenbergl, F. Laermer, B. Elsner, H. Muenzel and W. Riethmueller, Transducers, Stockholm, Technical Digest of Transducers, 1995, pp. 589–592.
- [51] A. A. Ayón, R. Braff, C. C. Lin, H. H. Sawin, and M. A. Schmidt, Journal of The Electrochemical Society, 146 (1), 1999, pp.339-349
- [52] M. Lutz et al, A precision yaw rate sensor in silicon micromachining, Transducers, Chicago, IL, Technical Digest of Transducers, 1997, pp. 847–850.
- [53] Kevin Powell, Stephen Burgess, Tony Wilby, Rhonda Hyndman and John Callahan, Interconnect Technology Conference, 2008. IITC 2008. International, 1-4 June, 2008, pp. 40 – 42.
- [54] Chongshen Song, Zheyao Wang, Qianwen Chen, Jian Cai and Litian Liu, Microelectronic Engineering, Volume 85, Issue 10, October 2008, Pages 1952-1956.
- [55] J. Van Aelst, H. Struyf, W. Boullart and S. Vanhaelemeersch, Thin Solid Films, Volume 516, Issue 11, 1 April 2008, pp. 3502-3506.
- [56] R.F. Figueroa, S. Spiesshoefer, S.L. Burkett and L. Schaper, J. Vac. Sci. Technol. B 23 (5), Sep/Oct 2005, pp. 2226-2231.
- [57] R. Dussart et al, Journal of Micromechanics and Microengineering, 14(2),190-196, 2004.

- [58] R.F. Figueroa, S.Spiesshoefer, S. L. Burkett and L. Schaper, J. Vac. Sci. Technol. B 23 (5), Sep/Oct 2005.
- [59] M. Armacost et al, IBM Journal of Res. Dev., Plasma processing, Vol.43 (1/2), 1999.
- [60] R Li, Y Lamy, W F A Besling, F Roozeboom and P M Sarro, J. Micromech. Microeng. 18 (2008) (8pp).
- [61] A.A. Chambers, Silicon Micromachining as an enabling technology for advanced device packaging, Semiconductor Manufacturing Magazine, November 2004.
- [62] Dzafir Shariff, Dr Nathapong Suthiwongsunthorn, Florian Bieck and Dr Jürgen Leib, 57th Electronic Components and Technology Conference, May 29-June 1 2007, pp. 858 – 863.
- [63] Masaya Kawano, Nobuaki Takahashi, Yoichiro Kurita, Koji Soejima, Masahiro Komuro, and Satoshi Matsui, IEEE Transactions on Electron Devices, Vol. 55, Issue 7, July 2008, pp.1614-1620.
- [64] H. Jansen, Microelectronics Journal, 32(9):769{777, 2001.
- [65] Blauw. M.A, PhD Thesis, Delft University of Technology, Delft, NL (2004).
- [66] L. Sainiemi and S. Franssila, J. Vac. Sci. Technol. B Volume 25, Issue 3, pp. 801-807 (May 2007).
- [67] Felix Lu, AQT/Duke University, April 22, 2008.
- [68] H. Reichl, A. Ostmann, R. Wieland and P. Ramm, 14th European Microelectronics and Packaging Conference & Exhibition, Friedrichshafen, Germany, 23-25 June 2003, pp 1-6.

- [69] Franz Laermer, Dry Etching, Comprehensive Microsystems, 2008, Chapter 1.08, Pages 217-233.
- [70] N Ranganathan, D Y Lee, L Ebin, N Balasubramanian, K Prasad and K L Pey, Journal of Micromechanics and Microengineering, Volume 18, Number 11, November 2008 (8pp).
- [71] Guoqiang Feng, Xiao Peng, Jian Cai and Shuidi Wang, 6th International Conference on Electronic Packaging Technology, 30 Aug.-2 Sept. 2005, pp: 57- 60.
- [72] Zheyao Wang et al, IEEE Transaction on Advanced Packaging, Vol. 29, No. 3, Aug. 2006, pp.615-622.
- [73] Steve Lassig, Solid State Technology, Issue 12, Vol. 50, December, 2007.
- [74] International Technology Roadmap of Semiconductor 2008 (<http://www.itrs.net>)
- [75] Jian-Qiang Lu and Ken Rose, Future Fab Intl. Issue 23, 9 July 2007, pp 25-27.
- [76] Kathy Cook, David Butler, Paul Siblingrud, Kathy O'Donnell, Thorsten Matthias and Eric Beynes, 3D-TSVs: A 'One Size Fits All' Approach is Unlikely, I-Micronews Letter-Advanced Packaging: 3D IC, WLP & TSV, May 19th 2008.
- [77] Peter Singer, Through-Silicon Vias: Ready for Volume Manufacturing?, Semiconductor International, March-01, 2008.
- [78] K.O. Navas et al, IEEE Advanced Packaging, Vol.31, No.1, p 44-50, (2008).
- [79] Yole development Advanced packaging webcast, September 2008
- [80] Ph.D. Thesis of Soren Jensen, Department of Micro- and Nanotechnology, Technical University of Denmark, 31.03.2004.
- [81] Richard A. Gottscho, C. W. Jurgensen, and D. J. Vitkavage, J. Vac. Sci. Technol. B 10, 2133 (1992).

- [82] M. A. Blauw, T. Zijlstra, and E. van der Drift, J. Vac. Sci. Technol. B 19(6), Nov/Dec 2001 2930-2934.
- [83] A. A. Ayón, R. Braff, C. C. Lin, H. H. Sawin and M. A. Schmidt, Journal of The Electrochemical Society, 146 (1) 339-349 (1999).
- [84] J. Hopkins, H. Ashraf, J. K. Bhardwaj, A. M. Hynes, I. Johnston, J. N. Shepherd, “The Benefits of Process Parameter Ramping During the Etching of High Aspect Ratio Silicon Structures”, Proceedings of the Materials Research Society Fall Meeting, Boston, MA, USA. December 1998.
- [85] C. Marxer, C. Thio, M.A. Gretillat, N.F. de Rooij, R. Battig, O. Anthamatten, B. Valk and P. Vogel, Journal of Microelectromechanical Systems, Vol. 6, Issue 3, Sept. 1997 277-285.
- [86] N. Ranganathan and Ramana Murthy, International Conference on Solid State Devices and Materials, 12 - 15 September 2006.
- [87] H.C. Liu, Y.H. Lin and W. Hsu, Microsystem Technologies 10 (2003) 29–34.
- [88] Li Jing and Hiroshi Miyashita, IEEE Asia Pacific Conference on Circuits and Systems, APCCAS 2006, 4-7 Dec. 2006, pp: 808 – 811.
- [89] J. U. Knickerbocker et al, IBM J. Res. & Dev. Vol. 52 No. 6 Nov. 2008 553-569.
- [90] P. S. Andry, C. K. Tsang, B. C. Webb, E. J. Sprogis, S. L. Wright, B. Dang and D. G. Manzer, 3D Chip Technology Volume 52, Number 6, 2008.571-581.
- [91] Jun So Pak, Chunghyun Ryu and Joungho Kim, Electronic Materials and Packaging, 2007. EMAP 2007. International Conference on 19-22 Nov. 2007 1-6.
- [92] Barbara Abraham-Shrauner, J. Vac. Sci. Technol. B 12(4) Jul/Aug 1994, 2347-2351.

- [93] In Man Kang et al, Journal of the Korean Physical Society, Vol. 44, No. 1, January 2004, pp. 69-72.
- [94] M.S. Kim et al, Surface and Coatings Technology, Volume 202, Issues 22-23, 30-Aug. 2008, pp. 5697-5700.
- [95] M. Nandakumar et al, International Electron Devices Meeting 1998, 6-9 Dec. 1998, pp.133-136.
- [96] <http://www.synopsys.com/TOOLS/TCAD/INTERCONNECTSIMULATION/Pages/FammosTX.aspx>
- [97] In Man Kang et al, Journal of the Korean Physical Society, Vol. 44, No. 1, January 2004, pp.69-72
- [98] Alexander Polyakov, Marian Bartek and Joachim N. Burghartz, Eurosensors XVI The 16th European Conference on Solid-State Transducers, September 15-18, 2002, Prague, Czech Republic, pp. 466-469.
- [99] R.E. Jewett, P.I. Hagouel, A.R. Neureuther, and T. Van Duzer, Polymer Engineering and Science, 17:381-384, 1977.
- [100] R. Jewett, Master's thesis, University of California, Berkeley, CA, 1979.
- [101] ATHENA User's Manual for 2D process simulation software.
- [102] http://en.wikipedia.org/wiki/Finite_element_method
- [103] ANSYS Short Course at Cornell University
(<http://instruct1.cit.cornell.edu/courses/ansys/>)
- [104] Bart Vandevelde, Chukwudi Okoro, Mario Gonzalez, Bart Swinnen, Eric Beyne, 9th Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE 2008, pp. 1-7.

-
- [105] Jing Zhang 1, Max O. Bloomfield, Jian -Qiang Lu, Ronald J. Gutmann, Timothy S. Cale, *Microelectronic Engineering*, Volume 82, Issues 3-4, December 2005, pp. 534-547.
 - [106] Hyongsok et al, *Japanese. J of Appl. Phys*, **38** 1999 2393.
 - [107] H. Reichl, A. Ostmann, R. Wieland and P.Ramm, 14th European Microelectronics and Packaging Conference & Exhibition Friedrichshafen, Germany, 23-25 June 2003, pp. 1-6.
 - [108] . J. Lannon Jr., C. Gregory, M. Lueck, A. Huffman, D. Temple, 59th Electronic Components and Technology Conference, ECTC 2009, 26-29 May 2009, pp. 355-359.
 - [109] S. Gupta, M. Hilbert, S. Hong and R. Patti, VLSI Multi-Level Interconnection Conference (VMIC-2004) [<http://www.tezzaron.com/about/papers/papers.html>]
 - [110] N. Marengo, S. Warnat and W. Reinert, DTIP 2007, Stresa, Italy, 25-27 April 2007, pp. 37-39.
 - [111] Chiung-Wen Lin, Hsueh-An Yang, Wei Chung Wang and Weileun Fang, *J. Micromech. Microeng*, 2007, **17** 1200-1205
 - [112] Bhardwaj, J; Ashraf, H; McQuarrie, A, *Proceedings of Electrochemical.Society* 1997 118.
 - [113] Cheryl S.S, John H. Lau, Zhang Xiaowu and Vaidyanathan Kripesh, *Proceedings of 58th Electronic Components and Technology Conference*, May 27-30, 2008, Lake Buena Vista, FL, USA (Accepted).
 - [114] A.I. Sauter and W.D. Nix, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 15, Issue 4, Aug. 1992, pp.594 – 600.

-
- [115] P.M. Igic and P.A. Mawby, Microelectronics Reliability, Vol. 40, Issue 3, 17 March 2000, pp. 443-450
 - [116] Y.-L. Shen, Microelectronic Engineering, Volume 83, Issue 3, March 2006, pp. 446-459.
 - [117] Z. Suo, Reliability of Metal Interconnects, Comprehensive Structural Integrity, 2007, Chapter 8.08, pp. 265-324.
 - [118] M.J Wolf et al, 58th Electronic Components and Technology Conference, 2008, 27-30 May 2008, pp. 563 – 570.
 - [119] B. Vandeveld, C. Okoro, M. Gonzalez, B. Swinnen and E. Beyne, International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-Systems, 2008 (EuroSimE 2008), 20-23 April 2008, pp. 1 – 7.
 - [120] Jing Zhang, Max O. Bloomfield, Jian-Qiang Lu, Ronald J. Gutmann and Timothy S. Cale, Proceedings of the ninth European workshop on materials for advanced metallization 2005, Volume 82, Issues 3-4, December 2005, pp. 534-547.
 - [121] <http://www.matweb.com/>
 - [122] Shen, Y-L, 2005 *Journal of Electronic Materials*, **34 (5)**, 497.
 - [123] Munroe, R.A, Proceeding of 50th Electronic Components and Technology Conference, 2000, 21-24 May 2000, Las Vegas, NV, USA, pp. 1576-1581.
 - [124] E. Baër, J. Lorenz and H. Ryssel, 2002 *Microelectronic Engineering* **64** 321.
 - [125] Hopkins, J; Ashraf, H; Bhardwaj, J K; Hynes, A M; Johnston, I; Shepherd, J N, Materials science of microelectromechanical systems (MEMS) devices; Proceedings of the Symposium, Boston, MA; US; 1-2 Dec. 1998. pp. 63-68.

-
- [126] N. Ranganathan, K. Prasad, Liao Ebin and N. Balasubramanian, 2007 *Sensors and Actuators A* **139** 323.
 - [127] C.F. Tsang et al, *Microelectronics Reliability* 45 (2005) pp. 517–525.
 - [128] K. Y. Yianga, W. J. Yoo, Q. Guo and K. Ahila, *Applied Physics Letters*, Vol. 83 (3), 21 July 2003, pp. 5524-526.
 - [129] Zhen-Cheng Wu *et al*, *IEEE Electron Device Letters*, Vol. 22 (6), June 2001, pp. 263-265.
 - [130] Baozhen Li, Timothy D. Sullivan, Tom C. Lee and Dinesh Badami, *Microelectronics Reliability* 44 (2004) 365–380.
 - [131] Robert R. Keller, Reiner Mönig, Cynthia A. Volkert, Eduard Arzt, Ruth, Schwaiger, and Oliver Kraft, 2002 *Stress-Induced Phenomena in Metallization: Sixth International Workshop*, pp. 119-132.
 - [132] Glenn B. Alers, K. Jow, R. Shaviv, Gerrit Kooi, and G. W. Ray, *IEEE transactions on device and materials reliability*, 4 (2), June 2004, 148-152.
 - [133] Zs. Tökei, Y.-L. Li and G.P. Beyer, *Microelectronics and Reliability*, **45 (9-11)**, 2005, 1436-1442.
 - [134] S. W. Yoon, V.P. Ganesh, S.Y.L. Lim, and V. Kripesh, *IEEE Transactions on Advanced Packaging*, Aug. 2008, Vol. 31 (3), pp. 519-526.
 - [135] C.S. Premachandran, N. Rangnathan, S. Mohanraj, C.S. Choong, M.K. Iyer, 55th *Electronic Components and Technology Conference*, 31 May-3 June, 2005, pp. 1094 – 1098.

- [136] C.S. Premachandran, John Lau, Ling Xie, Ahmad Khairyanto, Kelvin Chen, Myo Ei Pa, M. Chew and W.K. Choi, 58th Electronic Components and Technology Conference, 27-30 May 2008, pp.314 – 318.
- [137] Bhardwaj J, Ashraf H and McQuarrie, Annual Meeting of the Electrochemical Society, Montreal, Quebec, Canada, May 4 9, 1997.
- [138] Jing Ji, Francis E H Tay, Jianmin Miao and Jianbo Sun, International MEMS Conference 2006, Journal of Physics: Conference Series 34 (2006) 1137–1142.
- [139] Vivek K Singh and E.S.G. Shaqfeh, J. Vac. Sci. Technol. B 10(3), May/June 1992, pp. 1091-1104.
- [140] Rozalia Beica, Charles Sharbono and Tom Ritzdorf, Dans Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS - DTIP 2008, 9-11 April 2008, Nice, France.
- [141] PhD dissertation of A. Sheikholeslami, Topography Simulation of Deposition and Etching Processes, Institut für Mikroelektronik, Septemebr 2006.
- [142] M.Puech, J.M.Thevenoud, J.M.Gruffat, N.Launay, N.Arnal and P.Godinat, Fabrication of 3D packaging of TSV using DRIE, Dans Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS-DTIP 2008, Nice : France (2008).
- [143] A.M. Rodin, J. Callaghan and N. Brennan, High Throughput Low CoO Industrial Laser Drilling Tool, Available at: www.xsil.com/xsil/Files/xm-08-005.0_Paper_DP_Vias.pdf

- [144] H. Wensink, J.W. Berenschot, H.V. Jansen and M.C. Elwenspoek, The 13th Annual International Conference on Micro Electro Mechanical Systems, Miyazaki, Japan, 23-27 Jan 2000, pp. 769-774.
- [145] A.M. Hynes, H. Ashraf, J.K. Bhardwaj, J. Hopkins, I. Johnston and J.N. Shepherd, Sensors and Actuators Physical A, Vol. 74, 1999, pp. 13–17.
- [146] H. M. Andreson, J.A. Merson and R.W. Light, IEEE Transactions on Plasma Science, Vol. PS-14, No. 2, April 1986, pp. 156-164.
- [147] B. Majeed, K.M. Razeed, I. Paul, J. Barton and C. O'Mathuna, J. Micromech. Microeng. Volume 16, Number 8, August 2006, pp. 1519–1529.
- [148] J. D. Wu, C. Y. Huang and C. C. Liao, Microelectronics Reliability, Vol. 43 (2), February 2003, pp. 269-277.
- [149] R. Beica, C. Sharbono and T. Ritzdorf, 58th Electronic Components and Technology Conference, 27-30 May 2008, pp.577 – 583.
- [150] S. Pozder *et al.*, International Interconnect Technology Conference, IEEE 2007, 4-6 June 2007, pp. 213 – 215.
- [151] H.M. Anderson, J.A. Merson and R.W. Light, IEEE Transactions on Plasma Science, Vol. 14, Issue 2, April 1986. pp. 156 – 164.
- [152] Henri Jansen, Meint de Boer, Johannes Burger, Rob Legtenberg, and Miko Elwenspoek, Journal of Microelectronic Engineering **27** (1995) 475-480.
- [153] H. Zou, Microsystem Technologies 10 (2004) 603–607.
- [154] B. E. Volland, H. Heerlein, I. Kostic and I. W. Rangelow, Microelectronics Engineering, Vol. 57-58, September 2001, pp. 641-650.

- [155] A.A. Ayon and X. Zhang and R. Khanna, *Sensors and Actuators A* 91 2001 381-385
- [156] J.W. Coburn and H.F. Winters, *Applied Physics Letters*, 55 (26), 25-Dec. 1989, pp. 2730-2732.
- [157] Y. Junghoon, Y. Wu, J.C. Selby, and M.A. Shannon, *J. Vac. Sci. Technol. B* 23 (6), Nov/Dec 2005, pp. 2319-2329.
- [158] D. Keila and E. Anderson, *J. Vac. Sci. Technol. B* 19 (6), Nov/Dec 2001, pp. 2082-2088.
- [159] M. A. Blauw and E. van der Drift, *Journal of Applied Physics*, Vol. 94 (10), 15 Nov 2003, pp. 6311-6318.
- [160] D.L. Flamm, V.M. Donnelly and J.A. Mucha, *J. Appl. Phys.* 1981, Vol. 52, pp. 3633.-3639.
- [161] V. Kripesh, S.W. Yoon, V.P. Ganesh, N. Khan, M.D. Rotaru, W. Fang and M.K. Iyer, *IEEE Transactions On Advanced Packaging*, Vol. 28, No. 3, August 2005, pp. 377-386.
- [162] R. R. Johnson, *Multichip Module: Next generation packages*, *IEEE Spectrum*, 27 3 (1990) 34 48.
- [163] C.G. Massit and G.C. Nicolas, 45th Electronic Components and Technology Conference, Las Vegas, NV, USA, 1995. 21-24 May 1995, pp. 641-644.
- [164] J.U. Knickerbocker *et al*, 58th Electronic Components and Technology Conf., 27-30 May 2008, Lake Buena Vista, FL, pp. 538-543.

- [165] Navas Khan *et al.*, 58th Electronic Components and Technology Conf., 27-30 May 2008, Lake Buena Vista, FL, pp. 550-555.
- [166] F. Laermer and A. Urban, *Microelectronic Engineering*, 67–68 (2003) 349–355.
- [167] R. Zhou, H. Zhang; Y. Hao; D. Zhang and Y. Wang, The 16th Annual International Conference on Micro Electro Mechanical Systems, Kyoto, Japan, 19-23 Jan., 2003, pp. 161-164.
- [168] M. A. Blauw, T. Zijlstra and E. van der Drift, *J. Vac. Sci. Technol. B*, Vol.19 (6), Nov/Dec 2001, pp. 2930-2934.
- [169] E. Ba'r, J. Lorenz and H. Ryssel, *Microelectronic Engineering*, Vol. 64 (1), 2002, pp. 321-328.
- [170] Rozalia Beica, Charles Sharbono and Tom Ritzdorf, “Copper Electrodeposition for 3D Integration”, DTIP of MEMS and MOEMS, Nice, French Riviera, France, 9-11 April 2008.
- [171] Alexey M.Rodin, Joseph Callaghan and Niall Brennan, “High Throughput Low CoO Industrial Laser Drilling Tool”, available at: www.xsil.com/xsil/Files/xm-08-005.0_Paper_DP_Vias.pdf.
- [172] Ha-Duong Ngo *et al.*, *Journal of Physics: Conference Series* 34 (2006) 271–276.
- [173] D. Shariff, N. Suthiwongsunthorn, F. Bieck and Jürgen Leib, 57th Electronic Components and Technology Conference, ECTC '07, Reno, Nevada, May 29-1 June, 2007, pp. 858-863.

- [174] M.Puech, JM Thevenoud , JM.Gruffat, N. Launay, N. Arnal and P. Godinat, “Fabrication of 3D Packaging TSV using DRIE”, DTIP of MEMS and MOEMS, Nice, French Riviera, France, 9-11 April 2008.
- [175] D. Henry, X. Baillin, V. Lapras, M.H. Vaudaine, J.M. Quemper, N. Sillon, B. Dunne, C. Hernandez and E. Vigier-Blanc, 57th Electronic Components and Technology Conference, ECTC '07, Reno, Nevada, May 29-1 June, 2007, pp. 830-835.
- [176] M.J. Wolf, P. Ramm, A. Klumpp and H. Reichl, DTIP 2008, Nice, France, 9-11 April, 2008.
- [177] P.C.Andricacos, C. Uzoh, J.O.Dukovic, J.Horkans and H. Deligianni, “Damascene copper electroplating for chip interconnections”, IBM Journal of Research and Development 42 (5), 567.
- [178] Yuejin Hou and Cher Ming Tan, “Stress-induced voiding study in integrated circuit interconnects”, Semiconductor Science Technology, 23 (2008), pp 1-9.
- [179] Rama Puligadda, Sunil Pillalamarri, Wenbin Hong, Chad Brubaker, Markus Wimplinger and Stefan Pargfrieder, Material Research Society Symposium Proceedings, 2007, Vol. 970, pp. 239-252.
- [180] Ru-Yuan Yang, Cheng-Yuan Hung, Yan-Kuin Su, Min-Hang Weng and Hung-Wei Wu, Microwave and Optical Technology Letters, Vol. 48, Issue 9, June 2006, pp. 1773-1776.
- [181] George E. Ponchak, Alan N. Downey and Linda P. B. Katehi, IEEE Radio Frequency Integrated Circuits Symposium, 1997, pp. 101-104

-
- [182] Navas Khan *et al.*, IEEE Transactions Advanced Packaging, Vol. 31, No. 1, February 2008, pp. 44-50.
 - [183] Moffat T.P, Wheeler D and Josell D, “Super filling and the Curvature Enhanced Accelerator Coverage Mechanism”, *Interface*, 2004, pp. 46-52.
 - [184] S.M. Sze, Physics of Semiconductor Devices, 2nd edition, Section 7.3.4
 - [185] W.R. Harrella and J. Frey, Thin Solid Films 352 (1999), pp. 195-204.
 - [186] J. Franclov’a, Z. Kuřcerov’a, and V. Burvřřá, WDS'05 Proceedings of contributed Papers, Part II, 2005, pp. 353–356.
 - [187] M P Hernández, C F Alonso and J L Peña, J. Phys. D: Appl. Phys. 2001 34, pp. 1157-1161.
 - [188] C. F. Tsang, C. K. Chang, A. Krishnamoorthy, K. Y. Ee, Y. J. Su, H. Y. Li, W. H. Li and L. Y. Wong, Microelectronics Reliability 45 (2005) 517–525.
 - [189] S.A. Awan, R.D. Gould and S. Gravano, Thin Solid Films 355-356 (1999) 456-460.
 - [190] Zhen-Cheng Wu *et al.*, IEEE Electron Device letters, Vol. 22, N0. 6, June 2001, 263-265.
 - [191] A.A. Grinberg, Serge Luryi, M.R. Pinto and N.L. Schryer, IEEE Transaction on Electron Devices, Vol. 36 (6), June 1989, pp. 1162-1170.
 - [192] Y.K. Sharma, Electronics Letters, Vol.16, Issue 23, Nov. 6, 1980, pp. 896 – 897.
 - [193] J Sworakowski and G F L Ferreira, J. Phys. D: Appl. Phys. 17 (1), 14 Jan. 1984, pp. 135-139.
 - [194] Yunlong Li, IEEE Transaction on Device and materials Reliability, Vol. 7 (2), June 2007, pp. 252-258.

- [195] K. Y. Yianga, W. J. Yoo, Q. Guo and A. Krishnamoorthy, Applied Physics Letters, Vol. 83 (3), 21 July 2003, pp. 524-526.
- [196] W.H. Teh, R. Caramto, S. Arkalgud, T. Saito, K. Maruyama and K. Maekawa, Interconnect Technology Conference, 2009. IITC 2009. IEEE International Volume, Issue, 1-3 June 2009, pp. 53 – 55.
- [197] ITRS Interconnect Working Group, 2009 Winter Conference, 16th December 2009 (<http://www.itrs.net/Links/2009Winter/Presentations>)
- [198] R. Hon, S.W.R Lee, S.X. Zhang and C.K. Wong, “Multi-Stack Flip Chip 3D Packaging with Copper Plated Through-Silicon Vertical Interconnection”, Electronic Packaging technology Conference 2005, Vol-2, 7-9 Dec 2008.
- [199] X. Zhang, T.C. Chai, J. H. Lau, C. S. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, G.Y. Tang, Y.Y. Ong, S.R. Vempati, E. Wai, H.Y. Li, E.B. Liao, N. Ranganathan, V. Kripesh, J. Sun., Proceeding of 59th Electronic Components and Technology Conference, Sheraton San Diego, USA, 26-29 May 2009, pp. 305-312.