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STUDY OF BREAKDOWN IN ULTRATHIN GATE DIELECTRICS IN NANOSCALE MOSFETS

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STATEMENT OF ORIGINALITY

I hereby certify that the content of this dissertation is the result of work done by me and has not been submitted for a higher degree to any other University or Institution.

16 December 2008

Date

Lo Vui Lip

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ABSTRACT

Progressive breakdown has been found to provide an extra post-breakdown reliability margin for devices with ultrathin gate oxide. It is primarily constituted by two major regions, which are digital and analog breakdown. In this project, the progressive breakdown in the ultrathin gate oxide is thoroughly characterized and studied using different novel approaches.

A K-cycle multiple-stage constant-voltage stress has been employed to study the behaviors of the gate leakage current (I_g) at different stages of the progressive breakdown under various conditions. A critical gate voltage (V_{crit}) is found to demarcate the evolution of I_g during the progressive breakdown. For a gate voltage (V_g) smaller than V_{crit} , the digital breakdown dominates for which I_g digitally fluctuates with no apparent net increase. For V_g larger than V_{crit} , I_g rapidly evolves into a stable high leakage state, indicating that the analog breakdown starts to prevail. The transition of the digital breakdown into the analog breakdown is irreversible. This transition can rarely occur if V_g does not exceed V_{crit} . This brings a significant impact on the degradation rate of I_g (dI_g/dt) at nominal operating voltages (V_{op}). We show that the extrapolation of dI_g/dt from a high V_g to V_{op} can be largely overestimated, implying that the lifetime prediction of gate oxide is overly pessimistic. Additionally, V_{crit} is found to decrease with decreasing gate oxide thickness (T_{ox}). However, it is found that V_{crit} saturates for T_{ox} smaller than 1.6 nm, meaning that the presence of the digital breakdown in prolonging the progressive breakdown is preserved. Besides V_{crit} , the magnitude of I_g acts as another important factor in determining the transition of the digital breakdown into the analog breakdown.

The $1/f$ -like noise measurements of I_g confirm that a percolation path formed within the gate oxide during the occurrence of a dielectric breakdown event could grow from an unstable physical structure in the digital breakdown into a stable physical structure in the analog breakdown. The independence of V_{crit} on breakdown location, stressing duration and device dimensions further proves that the digital fluctuation of I_g is governed by the intrinsic properties of the percolation path. A model involving oxygen-vacancy-related defects, such as E'-centers and neutral oxygen vacancies, has been developed to explain the digital fluctuation and the digital-to-analog transformation of I_g . According to our results, if a device with the digital breakdown operates at V_g lower than V_{crit} , then this will provide extra time for other "potential" percolation paths to be formed at different locations within the gate oxide, affecting the post-breakdown device reliability.

To study the behaviors of I_g in the analog breakdown, we have developed a compact but simple method to determine the effective resistance associated with a percolation path and the channel resistances (R_{ch}) at one particular instant of the progressive breakdown. This method is called the percolation resistance (R_{perc}) measurement (PRM) method. Using the PRM method, the evolution of I_g during the progressive breakdown can be understood as a process controlled by the interplay between R_{perc} and R_{ch} . It is found that R_{perc} rapidly degrades in the early stage of the progressive breakdown with a rate of 0.1-0.2 decades per second at $V_g = 1.5$ V. As the progressive breakdown continues to evolve, the degradation of R_{perc} drastically slows down, and the parasitic resistances (R_{para}) become increasingly significant. Note that R_{para} is mainly constituted by R_{ch} in this study. In the later stage of the progressive breakdown, R_{perc} degrades with a very slow rate, leading to a saturation of R_{perc} . Additionally, we

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The existence of a high local temperature in the vicinity of a percolation path during the progressive breakdown has been confirmed by the heat generation rate calculation based on R_{perc} , the infrared photoemission microscopic results and the simulation results based on the finite element analysis. This could cause the dopants at the source and the drain terminal of a device to be redistributed, leading to the occurrence of dielectric-breakdown-induced dopant redistribution. The diode current at the substrate-source and drain p - n junction of a device is found to increase significantly as the progressive breakdown evolves. The experimental measurements are in good agreement with the simulation results associated with the dopant redistribution. This confirms that the dopant redistribution is one of the dominant mechanisms responsible for a change in

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CHAPTER ONE

INTRODUCTION

1.1 BACKGROUND

Due to the inherent chemical and physical properties, silicon dioxide (SiO_2) has been the material of choice for the gate oxide of a metal-oxide-semiconductor field-effect transistor (MOSFET) for many decades. One of the major trends of the microelectronics industry is to continuously scale down the gate oxide thickness (T_{ox}) such that the performance and the density of integrated circuits can be further improved [1-3]. This trend has been accelerated by the vast improvements in silicon manufacturing technology. By reducing T_{ox} , a higher drive current and a faster speed can be achieved in a MOSFET. However, regardless of the advantages mentioned above, the continuous downward scaling of T_{ox} comes with some drawbacks [4-8]. One of the most severe drawbacks is that the reliability of gate oxide significantly degrades due to the presence of the considerably huge gate leakage current (I_g). In particular, gate dielectric breakdown will lead to partial or total device malfunctioning. This may consequently degrade the overall performance of an integrated circuit. Therefore, gate dielectric breakdown is one of the important fields in the study of device or circuit reliability, especially for nowadays nanoscale complementary metal-oxide-semiconductor (CMOS) technology.

Many high-k materials, such as lanthanum oxide (La_2O_3), zirconium oxide (ZrO_2), tantalum oxide (Ta_2O_3) and hafnium oxide (HfO_2), have been explored as the alternative

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gate dielectric materials to overcome the considerably huge I_g existing in silicon oxynitride, as mentioned above. Among the high-k materials, hafnium oxide is a very promising candidate. Beside of having good material properties ($k = \sim 25$ and energy band gap = 5.7 eV), hafnium oxide has demonstrated better device characteristics and is compatible with the polycrystalline-silicon gate process. Essentially, three major issues must be addressed in order to fabricate useful devices for CMOS circuit application using hafnium oxide as the gate dielectric materials. These are (1) the high and unstable device threshold voltage, (2) the large difference between the capacitive equivalent oxide thickness of n- and p-MOSFETs, and (3) the degradation of the carrier mobility in the channel of a device.

Gate dielectric breakdown is generally defined as the loss of insulating properties of the gate oxide. In other words, the occurrence of a dielectric breakdown event corresponds to a substantial decrease in the resistances of some local defective areas within the gate oxide. When the gate oxide is stressed with a constant voltage or current, different types of defects or electronic traps will be gradually generated within the gate oxide. A conductive percolation path [9-12], which allows the flow of a huge amount of I_g , will be formed within the gate oxide as the defect density exceeds a critical threshold, and hence, a dielectric breakdown event is said to occur. As reported in all the related studies, the occurrence of a dielectric breakdown event is often associated with a sudden, abrupt increase in I_g . The process of stressing the gate oxide with a constant voltage or current until the occurrence of a dielectric breakdown event produces characteristic time-dependent dielectric breakdown (TDDB) [13]. Note that TDDB is widely used in the microelectronics industry to assess the reliability of gate oxide.

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The gate oxide integrity tests are carried out under the accelerated stressing conditions such that the data of TDDDB can be collected within a reasonable window of time (e.g., a few hours or days). Hence, the lifetime of gate oxide measured under the accelerated stressing conditions have to be extrapolated to the nominal operating conditions. This process will be complicated by the fact that the physical mechanisms governing gate dielectric wear-out and breakdown under the accelerated stressing conditions could be different from that under the nominal operating conditions [14-16].

Gate dielectric breakdown tends to alter the electrical properties of a MOSFET. Breakdown modes describe the effects of gate dielectric breakdown on device performance. A soft and a hard breakdown are two major breakdown modes that can be observed in ultrathin gate dielectric breakdown [17-21]. A MOSFET that experiences a soft breakdown will be considered as a partially failed device as it can still operate with a degraded performance. Conversely, a MOSFET that experiences a hard breakdown will be considered as a totally failed device. Since a globally accepted physical model in explaining the process of creating damages to the gate oxide is still lacking, the criterion in determining whether a dielectric breakdown event belongs to a soft or hard breakdown still remains ambiguous. The breakdown mode of the thick gate oxide with T_{ox} above 3 nm is mostly a hard breakdown, while the breakdown mode of the thin or ultrathin gate oxide with T_{ox} below 3 nm is either a soft or hard breakdown. This implies that dielectric breakdown in the thin or ultrathin gate oxide may not be catastrophic.

Progressive breakdown is a unique phenomenon that is only discovered and observed in ultrathin gate dielectric breakdown [22-24]. After the occurrence of a dielectric breakdown event, instead of experiencing an instantaneous, huge jump, I_g will

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degrade towards the device failure criterion with a relatively gradual profile. This breakdown transient is known as progressive breakdown. In other words, the progressive breakdown can be treated as the evolution of a soft breakdown into a hard breakdown. The post-breakdown reliability margin or residual time of a MOSFET is believed to be closely dependent on the progressive breakdown. Hence, the study of progressive breakdown in the ultrathin gate oxide becomes increasingly important. Until recently, various new electrical approaches and physical characterization techniques have been developed to study the progressive breakdown. A lot of useful insights are provided to further enhance the understandings on the physical mechanisms governing the behaviors of I_g during the progressive breakdown. This in turn would make the reliability projection of nanoscale CMOS devices with ultrathin gate oxide to become more accurate and help in exploring new avenues for the enhancement of device or circuit reliability.

1.2 MOTIVATION

The reliability of gate dielectric has been an intensive research topic for more than three decades, especially when the device dimensions are continuously scaled down. According to the latest report of *International Technology Roadmap for Semiconductors* (ITRS), silicon oxynitride with the equivalent oxide thickness (EOT) of 0.8-1.2 nm will be used in standard sub-65-nm CMOS technologies. This is due to the very stringent requirements of a low I_g and a fast device speed for microprocessor applications. While there is a very high level of interest in the use of alternative high- κ materials as the gate dielectric, silicon oxynitride continues to serve as the best choice for the insulating layer of a MOSFET. The progressive breakdown is particularly important in ultrathin gate dielectric

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breakdown as it provides an extra post-breakdown reliability margin. In general, there appears to be no universal agreement on an accurate physical model in explaining the ultrathin gate dielectric reliability involving the progressive breakdown. Therefore, there is a need to study the physical mechanisms governing the progressive breakdown in details and the effects of the progressive breakdown on device performance.

1.3 OBJECTIVES

The ultimate objective of this project is to perform a comprehensive and systematic analysis on the physical mechanisms governing the progressive breakdown. Moreover, its impacts on the reliability projection of nanoscale CMOS devices with ultrathin gate oxide will be thoroughly studied. We establish theoretical models that are not only able to explain various breakdown phenomena observed in the experimental data, but are also able to predict the post-breakdown electrical properties of n-MOSFETs.

1.4 ORGANIZATION OF THESIS

This thesis is divided into six major chapters. The organization of this thesis is presented as follows:

- *Chapter Two* is a literature review of the research work that has been done and reported for ultrathin gate dielectric breakdown.
- *Chapter Three* explains the procedure and the details of experiments carried out in this study.
- *Chapter Four* covers the comprehensive study of digital breakdown, which is the early stage of the progressive breakdown.

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- *Chapter Five* covers the comprehensive study of analog breakdown, which is the later stage of the progressive breakdown.
- *Chapter Six* provides the conclusions of this project and the recommendations of future work.

1.5 CONTRIBUTIONS

This project mainly focuses on the study of digital and analog breakdown, which are two major regions that constitute the progressive breakdown in the ultrathin gate oxide. A new stressing methodology, which is known as a K-cycle multiple-stage constant-voltage stress, has been developed to study the behaviors of I_g at different stages of the progressive breakdown under various conditions. A critical gate voltage (V_{crit}) and the magnitude of I_g are found to be two major factors in determining the transition of the digital breakdown into the analog breakdown. For V_g larger than V_{crit} , the digital breakdown will rapidly evolve into the analog breakdown, in which this transition is irreversible. On the other hand, for V_g smaller than V_{crit} , the digital breakdown can hardly evolve into the analog breakdown, meaning that the progressive breakdown is prolonged during the normal device operations. Hence, this brings a significant impact on the degradation rate of I_g (dI_g/dt) at nominal operating voltages (V_{op}). According to our results, dI_g/dt extrapolated from a high V_g to V_{op} can be tremendously overestimated. For T_{ox} above 1.6 nm, V_{crit} decreases with decreasing T_{ox} . This implies that the digital breakdown will rapidly evolve into the analog breakdown when T_{ox} is scaled down to a point beyond which V_{crit} is equal to or smaller than V_{op} . However, for T_{ox} below 1.6 nm, a saturation of V_{crit} can be found, indicating that the presence of the digital breakdown in prolonging the

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progressive breakdown is preserved. In addition, the role of I_g in causing the transition of the digital breakdown into the analog breakdown has been investigated. We propose that the digital fluctuation of I_g in the digital breakdown is caused by the transformation of various types of oxygen-vacancy-related defects during electrical stressing. V_{crit} is found to be independent on breakdown location, stressing duration and device dimensions. This indicates that the digital fluctuation of I_g is governed by the intrinsic properties of a percolation path. A $1/f$ -like noise study for I_g further demonstrates that the percolation path in the digital breakdown possesses an unstable physical structure, implying that the percolation path could be randomly switched on and off. Furthermore, we found that multiple percolation paths could be created in a device with the digital breakdown at V_g smaller than V_{crit} . This will significantly affect the post-breakdown device reliability.

The percolation resistance (R_{perc}) measurement (PRM) method has been developed to study the behaviors of I_g in the analog breakdown. R_{perc} defines the effective resistance associated with a percolation path. The PRM method also allows us to monitor the channel resistances (R_{ch}) at one particular instant of the progressive breakdown. Based on the results obtained using the PRM method, the analog breakdown can be divided into two distinct regions, which are controlled by R_{perc} and the parasitic resistances (R_{para}), respectively. In this study, R_{para} is assumed to be nearly equal to R_{ch} . The dependence of R_{perc} on various key parameters, such as breakdown location, channel length, temperature and voltage, has been studied in details. The presence of the R_{para} -controlled region aids in prolonging the period of I_g reaching the device failure criterion. However, the continuous shrinkage of channel length will cause this benefit on extending the device lifetime to disappear. Our results suggest that the physical mechanism controlling the progressive

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breakdown under the accelerated stressing conditions could be quite different from that under the normal device operations. In addition, the I - V characteristics in accumulation mode in the analog breakdown have been found to exhibit a *Schottky*-like behavior. Based on this finding, we demonstrate that the behaviors of I_g in the analog breakdown could be governed by (1) a change in the structural properties in the vicinity of the percolation path, and (2) the percolation path dilation. As compared to the digital breakdown, a relatively stable silicon-like percolation path and a *Schottky* barrier are proposed to exist in the analog breakdown.

The heat generation rate calculation based on R_{perc} , the infrared photoemission microscopic results and the simulation results based on the finite element analysis show that a breakdown n-MOSFET will be associated with a high local temperature. The existence of substantial local heating effects in the vicinity of the percolation path acts as the main driving force to trigger the occurrence of dielectric-breakdown-induced dopant redistribution. The dopant redistribution can be observed through the change in the diode current at the substrate-source and drain p - n junction of a breakdown n-MOSFET. The effects of the dopant redistribution on the progressive breakdown have been thoroughly studied.

The above work has been published in premier conferences, such as *IEEE International Electron Device Meeting (IEDM)* and *International Reliability Physics Symposium (IRPS)*, as well as prestigious journals, such as *IEEE Electron Device Letters (EDL)* and *Transactions on Electron Devices (TED)*.

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LITERATURE REVIEW

2.1 INTRODUCTION

Silicon dioxide has been intensively used for more than three decades as dielectric materials to insulate the gate electrode from the channel of a MOSFET. With a large energy bandgap of 8.9 eV, silicon dioxide is considered as an excellent insulator. The nearly exclusive use of silicon dioxide in conventional CMOS applications is mainly due to the reason that silicon dioxide uniquely possesses the required combination of several chemical and physical properties. The interface between silicon dioxide and silicon (Si) is very stable. The density of the electronic states at the Si-SiO₂ interface is low. This results in good charge-carrier mobility in the channel of a MOSFET. Furthermore, silicon dioxide is associated with a relatively low electron and hole trapping rate, and consists of excellent compatibility with conventional CMOS technology. The bulk resistivity of silicon dioxide is about 10^{15} Ω -cm, and the dielectric breakdown strength of silicon dioxide is about 10^7 V/cm. The film of silicon dioxide can be grown by thermal oxidation on a clean silicon surface, and thus, they can be made with a considerably low density of the trapped charges. Note that the energy barrier between silicon and silicon dioxide for electrons and holes are about 3.1 eV and 4.5 eV, respectively. The gate oxide plays a vital role to couple the electric potential from the gate electrode to the channel of a MOSFET.

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Therefore, a better control on the channel of a MOSFET by the gate electrode can be obtained when the gate oxide is made as thin as possible.

The study of gate dielectric reliability has been a focus of attention as T_{ox} is scaled below 3 nm [4-8]. It is expected that dielectric breakdown in the thin gate oxide will become more serious than that in the thick gate oxide, because the electric field across the gate oxide (E_{ox}) increases with decreasing T_{ox} . One of the major issues in the thin gate dielectric reliability is an excessively large I_g . It creates new challenges for reliability assessment and characterization, especially in deep sub-micron CMOS technology. In addition, the detection of thin gate dielectric breakdown becomes very difficult due to the presence of a quasi- or soft breakdown [17-21], which has not been observed in thick gate dielectric breakdown. Progressive breakdown is a new dielectric breakdown feature that appears in ultrathin gate oxide [22-24]. Instead of experiencing an instantaneous, huge jump, I_g will progressively evolve into a higher conduction state. Therefore, traditional testing methodologies, experimental procedure and failure criteria used to study the reliability of thick gate oxide must be modified such that the detection of thin gate dielectric breakdown is reliable and robust.

For the thin gate oxide, the determination of an accurate E_{ox} can be difficult due to the presence of an excessively large I_g , the gate electrode depletion and the quantum confinement effects. The direct tunneling mechanism [25-30] is responsible for an excessively large I_g in the thin gate oxide at a low E_{ox} . In addition, due to a considerably huge amount of the charge carriers directly tunneling through the gate oxide, the voltage that drops across the interconnects and the gate electrode can be significant, leading to an underestimation of E_{ox} . This is a major concern for test structures with large areas, in

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which the conduction of a considerably huge I_g exists before the occurrence of a dielectric breakdown event.

The reliability of silicon dioxide in the microelectronics industry can be generally understood as the ability of silicon dioxide to retain the insulating properties as it is subjected to a nominal operating electric field for ten years. For the gate oxide with T_{ox} below 3 nm, controversies still exist over the proper extrapolation of the gate oxide lifetime from the accelerated stressing conditions to the nominal operating conditions. Undoubtedly, this has major implications on accurately projecting the reliability of nanoscale CMOS devices with thin gate oxide at V_{op} [14-16, 31, 32].

2.2 SILICON OXYNITRIDE AS EXTENSION OF SILICON DIOXIDE

Nanoscale CMOS technology requires a constant evolution with a continuous downward scaling of T_{ox} to follow Moore's Law. An excessively large I_g is one of the crucial challenges in the study of ultrathin gate dielectric reliability as T_{ox} is further scaled down to less than 3 nm. It has been predicted that 1.2 nm is the limitation of the continuous downward scaling of T_{ox} [33]. As reported in Ref. [34], T_{ox} of about 1.5 nm is associated with the I_g of about 10 A/cm². Moreover, for the thin gate oxide, the thickness of the Si-SiO₂ interface and the trap capture cross-section become non-scalable [35]. In conventional silicon dioxide, the thickness of the Si-SiO₂ interface, which appears in the form of sub-oxide, is about 5 Å. This means that when T_{ox} is less than 1.2 nm, the film of silicon dioxide will lose the original bulk properties, and the characteristics of the Si-SiO₂ interface will become dominant. To overcome these challenges, it is proposed that silicon dioxide can be replaced by silicon oxynitride (SiO_xN_y), which can be produced through

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the nitridation of silicon dioxide or deposition of silicon oxynitride on the silicon substrate [36-39]. The advantage of introducing nitrogen into the film of silicon dioxide can be briefly explained by the following formula:

$$t_{SiON} = t_{SiO2} \left(\frac{k_{SiON}}{k_{SiO2}} \right) \quad (2.1)$$

where t_{SiON} and k_{SiON} are the thickness and the dielectric constant of silicon oxynitride, respectively. Moreover, t_{SiO2} and k_{SiO2} are the thickness and the dielectric constant of silicon dioxide, respectively. Since k_{SiON} is larger than k_{SiO2} , equivalent device performance for a specific t_{SiO2} can be achieved with a higher t_{SiON} . It can be noticed that the constraint of the continuous downward scaling of T_{ox} can be relaxed by increasing the dielectric constant of gate oxide if silicon dioxide is replaced by silicon oxynitride. As compared to silicon dioxide, silicon oxynitride possesses a higher dielectric constant, a relatively lower I_g and a higher dielectric breakdown strength. Although silicon oxynitride is able to efficiently reduce I_g , the defect origins in silicon oxynitride are about three fold of those in silicon dioxide. As reported in Ref. [34], known defects in silicon oxynitride can be classified into six main groups:

- Paramagnetic defects, such as $\equiv Si^\bullet$, $\equiv Si-O-O^\bullet$ and $\equiv Si_2N^\bullet$;
- Diamagnetic defects, such as $\equiv Si-Si\equiv$, $=N-H$ and $=Si:$ with the dislocation of the Si center;
- Neutral defects, such as $\equiv Si-O^\bullet$, $=Si:$, $\equiv SiOH$ and $\equiv Si-O-O-Si\equiv$;
- Charged defects, such as $\equiv Si^\bullet + Si\equiv$ and $\equiv Si_2N:$;
- Intrinsic defects, such as $\equiv Si^\bullet$, $=N-N=$, $\equiv Si-O-O-Si\equiv$ and $=Si:$, and;
- Extrinsic defects, such as $\equiv SiH$, $\equiv Si_2NH$ and $\equiv SiOH$.

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The symbol “–”, “=” and “≡” denote one single bond, two single bonds and three single bonds, respectively. Additionally, the symbol “•” denotes one unpaired electrons, and the symbol “:” denotes one pair of electrons. The electronic quality of gate oxide is mainly governed by the neutral and the charged defects, which appear in the form of non-bridging or dangling silicon and oxygen bonds. Interstitial or bonded impurities can also serve as the electronic trapping centers within the gate oxide. From the physical point of view, the dangling silicon and oxygen bonds and the bonded impurities can modify the local potential in the gate oxide.

2.3 TUNNELING MECHANISMS

When the gate electrode is applied with a sufficiently large V_g , the charge carriers at the surface of an inversion layer can tunnel into or through the gate oxide, and this will give rise to I_g . There are two major types of tunneling mechanisms, which are quantum mechanical phenomena, in the study of gate dielectric reliability, namely, the Fowler-Nordheim (FN) tunneling [40-43] and the direct tunneling mechanism [25-30].

We are going to differentiate the dominant tunneling mechanisms in the gate oxide with T_{ox} above 3 nm from that with T_{ox} below 3 nm. It has been widely reported that there exists an important difference in the physics behind the tunneling of the charge carriers into or through the thick and the thin gate oxide. The dominant tunneling mechanism in the gate oxide with T_{ox} above 3 nm is the Fowler-Nordheim (FN) tunneling mechanism. On the other hand, the direct tunneling mechanism starts to dominate at low V_g when T_{ox} is gradually scaled down below 3 nm. Generally, the thick gate oxide is associated with T_{ox} above 3 nm, while the thin gate oxide is associated with T_{ox} below 3 nm [44]. In

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addition, the gate oxide is considered as “ultrathin” when T_{ox} is less than 2 nm. For the thick gate oxide, at a typical operating electric field of 5 MV/cm, the current density due to the FN tunneling mechanism is less than 10^{-9} A/cm² [45]. However, for the thin gate oxide, the direct tunneling current increases exponentially by about one order of magnitude for every 0.2-0.3 nm reduction in T_{ox} [5].

Figure 2.1. Energy band diagram showing the FN tunneling of the electrons into the oxide conduction band via a triangular energy barrier.

2.3.1 FOWLER-NORDHEIM TUNNELING MECHANISM

The FN tunneling mechanism [40-43] is dominant in the thick gate oxide. It takes places when the charge carriers tunnel into the oxide conduction band via a triangular energy barrier. As shown in Fig. 2.1, for an n-channel MOSFET (n-MOSFET), when V_g is positive and sufficiently large, the electrons near the surface of an inversion layer formed

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in the p-type silicon substrate will tunnel into the oxide conduction band via a triangular energy barrier. It can be noticed that the FN tunneling mechanism creates an “electrical thinning effect” (i.e., a reduction in the electrical thickness), allowing the FN tunneling of the charge carriers into the gate oxide to occur. I_g governed by the FN tunneling mechanism can be modeled as [40]

$$J_{FN} = \left(\frac{q^3 E_{ox}^2}{8\pi\hbar\phi_{ox}} \right) \exp \left(\frac{-8\pi\sqrt{2m^*}\phi_{ox}^{2/3}}{3\hbar q E_{ox}} \right). \quad (2.2)$$

Eqn. (2.2) can be obtained by applying the Wentzel-Kramers-Brillouin approximation for a triangular energy barrier. Here, $\hbar$ is the Plank constant, ϕ_{ox} denotes the Si-SiO₂ interface energy barrier for the charge carriers, and m^* is the effective mass of the charge carriers tunneling into the gate oxide.

2.3.2 DIRECT TUNNELING MECHANISM

In the early 1980s, J. Maserjian *et al.* reported that for the gate oxide with a T_{ox} of 4-5 nm, I_g at V_g below 3 V increased after the gate oxide has been stressed at a high E_{ox} [25]. Nowadays, it is well known that this phenomenon is controlled by the direct tunneling mechanism [25-30]. Generally, the direct tunneling mechanism is dominant in the thin or ultrathin gate oxide at a low V_g . It takes places when the charge carriers tunnel through the gate oxide via a trapezoid energy barrier, as shown in Fig. 2.2. Indirectly, this means that the charge carriers travel from the cathode to the anode without entering the oxide conduction band. The direct tunneling of the charge carriers through the gate oxide is ballistic or quasi-ballistic in nature. Fig. 2.2 illustrates the various components of I_g governed by the direct tunneling mechanism for a positively-biased n-MOSFET.

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- Conduction-band electron tunneling (CBET) – Direct tunneling of the electrons from the conduction band of the p-type silicon substrate into the n^+ -type polycrystalline-silicon gate.
- Valence-band electron tunneling (VBET) – Direct tunneling of the electrons from the valence band of the p-type silicon substrate into the n^+ -type polycrystalline-silicon gate.
- Valence-band hole tunneling (VBHT) – Direct tunneling of the holes from the valence band of the n^+ -type polycrystalline-silicon gate into the p-type silicon substrate.

I_g governed by the direct tunneling mechanism can be modeled in accordance with the following generic equation [26, 27, 30]

Figure 2.2. Energy band diagram showing the direct tunneling of the charge carriers through the gate oxide via a trapezoid energy barrier. CBET, VBET and VBHT represent the conduction-band electron tunneling, valence-band electron tunneling and valence-band hole tunneling respectively.

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$$J_{DT} = C \left(\frac{V_{ox}}{T_{ox}} \right)^2 \exp \left(\frac{-B \left\{ 1 - \left[1 - \left(\frac{V_{ox}}{\phi_{ox}} \right) \right]^{3/2} \right\}}{\frac{V_{ox}}{T_{ox}}} \right) \quad (2.3)$$

where B and C are the physical parameters that take into account the voltage dependence of the density of electronic states at the Si-SiO₂ interface and the effective mass of the charge carriers tunneling through the gate oxide. Additionally, V_{ox} is a voltage across the gate oxide. V_{ox} can be related to V_g as follows

$$V_{ox} = V_g - V_{fb} - \phi_s - V_{dp} \quad (2.4)$$

where V_{fb} is the flat-band voltage, ϕ_s is the surface potential, and V_{dp} is the depletion layer of the polycrystalline-silicon gate.

2.3.3 TRAP-ASSISTED TUNNELING MECHANISM

The trap-assisted tunneling mechanism is another widely accepted tunneling mechanism that can take place in the gate oxide. During the occurrence of the trap-assisted tunneling mechanism, the charge carriers can tunnel into or through the gate oxide with the assistance of the electronic trapping centers within the gate oxide (i.e., bulk traps) or at the Si-SiO₂ interface (i.e., interface states). These electronic traps normally correspond to the empty bonding states of silicon dioxide. The presence of these electronic trapping centers can cause an “electrical thinning effect” to occur. Therefore, it can be imagined that the charge carriers tunnel through the gate oxide with a reduced electrical thickness. The trap-assisted tunneling mechanism is not easily explained using a closed-form equation since the phenomenon is complex. However, it is found to be dependent on E_{ox} and the density

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of the bulk traps and the interface states. The trap-assisted tunneling of the charge carriers into or through the gate oxide via a bulk trap and an interface state is shown in Fig. 2.3. Note that both the elastic and the inelastic trap-assisted tunneling mechanism are possible to take place.

Figure 2.3. Energy band diagram showing the trap-assisted tunneling of the charge carriers into or through the gate oxide via a bulk trap and an interface state.

2.4 DEFECT GENERATION

Defect generation is an important process in causing gate dielectric wear-out and breakdown to occur [41, 42, 46-48]. The tunneling of the electrons into or through the gate oxide will trigger several destructive processes that are primarily depending on the electron energy. For the thin gate oxide, the electron energy is determined by V_g as the tunneling of the electrons through the gate oxide is ballistic or quasi-ballistic in nature [46, 49, 50]. At a high V_g , impact ionization and anode hole injection will take place, leading

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to hole trapping and the creation of hole-related defects within the gate oxide [27, 42, 45, 51, 52]. However, at a low V_g , it has been reported that trap creation attributed to the release of hydrogen from the anode dominates [46, 50, 53]. Eventually, damages to the gate oxide are built up through the accumulation of various types of defects within the gate oxide. After a critical defect density is reached, the gate oxide destructively, irreversibly breaks down. Fig. 2.4 summarizes the modes of degradation for the gate oxide at different ranges of V_g , which will eventually lead to gate dielectric wear-out and breakdown [54].

Figure 2.4. General schematic summarizing the modes of degradation for the gate oxide at different ranges of V_g , which will eventually lead to gate dielectric wear-out and breakdown [54].

2.5 STRESS-INDUCED LEAKAGE CURRENTS

It has been known that the gate oxide stressing with a constant V_g will lead to an increase in I_g , which is often called the stress-induced leakage current (SILC) [55-57]. SILC is directly proportional to the density of the electronic traps generated within the gate oxide under the accelerated stressing conditions. Moreover, I_g attributed to the formation of minuscule conductive percolation paths within the gate oxide during the occurrence of a

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dielectric breakdown event is classified as B-mode SILC [57]. According to D. J. DiMaria *et al.* [55], SILC is caused by the generation of the neutral electron traps within the gate oxide. These neutral electron traps act as “stepping stones” that assist the charge carriers to tunnel into or through the gate oxide. This phenomenon is identical to the trap-assisted tunneling mechanism [58, 59] explained in *Section 2.3.3*. As reported in Ref. [55], the generation of the neutral electron traps within the gate oxide is related to the hot-electron-induced hydrogen release mechanism [60], which will be discussed in the following section. Note that the neutral electron traps, which are the trapping centers produced through the annihilation of the trapped holes by free electrons, is demonstrated to possess very minimum contributions to SILC under the accelerated stressing conditions [54]. Atomic hydrogen from remote plasma has been shown to be highly reactive at the Si-SiO₂ interface at the room temperature, leading to the generation of the fast interface states [61-63] and the positively-charged slow interface states [64, 65]. The charge centers of the hydrogen-induced slow interface states were found to be 2-3 nm away from the Si-SiO₂ interface [65]. These defects are believed to give rise to the trap-assisted tunneling of the charge carriers into or through the gate oxide. By exposing the thin film of silicon oxide to remote plasma, it can be observed that the presence of atomic hydrogen will induce a gradual increase in the leakage current of the film. This is similar to SILC generated under the accelerated stressing conditions.

2.6 GATE DIELECTRIC INTRINSIC BREAKDOWN MODELS

The objective of a gate dielectric intrinsic breakdown model is to describe the lifetime of gate oxide as a function of various key parameters, such as electric field, voltage,

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temperature, gate oxide thickness and device area [14, 16, 50, 66-69]. The anode hole injection, the thermo-chemical, and the hydrogen release model are some of the well-known gate dielectric intrinsic breakdown models. The basis of a gate dielectric intrinsic breakdown model is a physical mechanism responsible for creating damages to the gate oxide and eventually triggering the occurrence of a dielectric breakdown event. In addition, the practical application of a gate dielectric intrinsic breakdown model is to accurately extrapolate the device lifetime from the accelerated stressing conditions to the nominal operating conditions. However, the choice of a gate dielectric intrinsic breakdown model has been a debatable subject for many years. The lifetime prediction of gate oxide based on E_{ox} , I/E_{ox} or V_g is intensively discussed, but a universally-accepted conclusion has not yet reached.

2.6.1 THERMO-CHEMICAL MODEL (*E*-MODEL)

The thermo-chemical model was proposed by J. W. McPherson *et al.* [70-73] from the mid-1980s to the late 1990s. It is developed in accordance with the reaction rate theory and the interactions among the local electric fields (E_{loc}) of dipoles associated with oxygen-vacancy-related defects within the gate oxide. Fig. 2.5 shows a general schematic that describes the non-uniform distribution of an electric field in the gate oxide due to the presence of a local electric field induced by the dipole moment of an oxygen-vacancy-related defect. The polarization vector caused by the distortion of silicon dioxide lattice and the shift of an electron cloud about each oxygen nucleus under E_{ox} is given by

$$P = \chi \epsilon_0 E_{ox} \quad (2.5)$$

where χ is the electric susceptibility.

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This model proposes that defect generation is an electric-field-driven process, and I_g flowing through the gate oxide plays the secondary role. In the thermo-chemical model, the lifetime or time-to-dielectric-breakdown of gate oxide is described as [70]

$$t_{BD} \propto \exp\left(\frac{\Delta H_0}{kT} - \gamma E_{ox}\right). \tag{2.6}$$

In Eqn. (2.6), ΔH_0 defines the activation energy for the $\text{O-Si}\equiv\text{O}_3$ covalent-bond breakage, γ defines the electric field acceleration factor, k is the Boltzmann constant, and T is the temperature. Since the logarithm of t_{BD} is directly proportional to E_{ox} , the thermo-chemical model is also commonly known as the E -model. Note that ΔH_0 will be lowered by the presence of strained Si-O bonds and hydrogen or hole capture.

Figure 2.5. Non-uniform distribution of an electric field in the gate oxide due to the presence of E_{loc} induced by the dipole moment of an oxygen-vacancy-related defect.

The thermo-chemical model has been widely accepted because the data of t_{BD} reported in Refs. [66-68, 74] exhibit an exponential relationship with E_{ox} . However, it must be

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pointed out that the exponential relationship between t_{BD} and E_{ox} is not the direct proof for the validity of a specific physical model. Probably, the strongest evidence against the thermo-chemical model comes from the experiments of substrate-hot-electron (SHE) injection [75, 76]. Using a specially-designed n-MOSFET, as shown in Ref. [77], a forward-bias n^+ -type diffusion in the p-type silicon substrate was used to inject the electrons into an inversion layer under the Si-SiO₂ interface. The amount of I_g flowing through the gate oxide could be controlled by independently adjusting the bias conditions at the gate electrode and the substrate, varying the magnitude of a forward-bias voltage across the junction of the electron injector. The substrate bias conditions controlled the energy of the incident electrons at the Si-SiO₂ interface between the gate oxide and the substrate. Conversely, the gate bias conditions controlled the energy of the incident electrons at the Si-SiO₂ interface between the gate oxide and the gate electrode. It was found that the charge-to-dielectric-breakdown (Q_{BD}) of gate oxide is strongly dependent on the substrate bias conditions, even though E_{ox} remains unchanged. Therefore, Q_{BD} correlates with the energy of the electrons tunneling into or through the gate oxide instead of E_{ox} . This was also demonstrated in the conventional gate oxide stressing in the FN tunneling regime by varying the doping concentration of the anode [78, 79].

2.6.2 ANODE HOLE INJECTION MODEL (1/ E -MODEL)

According to the anode hole injection model [27, 42, 45, 51, 52], the occurrence of a dielectric breakdown event is triggered by holes that are induced by the hot electrons and injected into the gate oxide from the anode. When the gate oxide of a n-MOSFET is stressed in the FN tunneling regime in inversion mode, the hot electrons tunneling into the

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oxide conduction band will lose energy, leading to the creation of electron-hole pairs at the anode. Due to the presence of E_{ox} , the holes at the valence band of the anode will be injected into the gate oxide. The holes trapped within the gate oxide will result in damages to the gate oxide. One of the important parameters in the anode hole injection model is the hole-fluence-to-dielectric-breakdown (Q_p) of gate oxide. For T_{ox} above 6 nm, Q_p is independent on E_{ox} and remains approximately constant at 0.1 C/cm^2 [80]. Conversely, for T_{ox} below 6 nm, Q_p decreases with increasing E_{ox} [80]. In the anode hole injection mode, Q_{BD} is given by

$$Q_{BD} = \frac{Q_p}{\alpha_p} \exp\left(\frac{B}{E_{ox}} (\phi_p V_{ox})^{3/2}\right). \quad (2.7)$$

According to Eqn. (2.7), Q_{BD} is inversely proportional to the logarithm of E_{ox} . Thus, the anode hole injection model is also known as the $1/E$ -model. According to the calculations reported in Ref. [81], for MOSFETs with the n^+ -type polycrystalline-silicon gate, the threshold of V_g for the generation of positively-charged defects by hole trapping within the gate oxide is found to be 7-8 V. This was experimentally confirmed by D. J. Maria *et al.* [52]. Hence, it is inappropriate to use the anode hole injection model to explain gate dielectric breakdown during the normal device operations. The anode hole injection model has been recently modified or improved such that it is able to explain gate dielectric breakdown at a low V_g [82]. The modified or improved version of the anode hole injection model proposes that at a low V_g , a weaker minority-carrier ionization process is responsible for the injection of holes from the anode into the gate oxide. It can successfully fit the slope of the t_{BD} versus V_g relationship at a high E_{ox} . However, one of the major discrepancies of this model is that it does not agree with the absolute magnitude of the defect generation rate.

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2.6.3 HYDROGEN RELEASE MODEL

The evidence for the involvement of hydrogen in defect generation and gate dielectric breakdown is circumstantial but strong [46, 54, 83]. For instance, this can be observed in the passivation of dopants in the substrate [84] and the hydrogen redistribution during the gate oxide stressing by the hot electrons [85-86]. The desorption rate of hydrogen from the silicon surfaces [87], which was measured as a function of the energy of the incident electrons, showed a similar trend to the voltage dependence of defect generation [46, 53]. The observation of the significant isotope effects on the stress-induced flat-band voltage shift and SILC [88] further enhance the general acceptance of the hydrogen release model.

Figure 2.6. Creation of damages to the gate oxide by the hot-electron-induced hydrogen release mechanism [60].

Fig. 2.6 shows the creation of damages to the gate oxide by the hot-electron-induced hydrogen release mechanism [60]. Hydrogen-related species, which include either protons

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or atomic hydrogen, are freed from the silicon surfaces at the anode by the energetic electrons. Due to the presence of E_{ox} , hydrogen-related species will diffuse from the anode to the cathode via the gate oxide. Eventually, they will react with the lattice of gate oxide to create electronic trapping centers.

Figure 2.7. General schematic of a percolation path formed within the gate oxide of a n-MOSFET due to the accumulation of various types of defects.

2.6.4 PERCOLATION MODEL

The application of percolation concepts and theories to gate dielectric breakdown may be traced to the observations of fractal-like electrical discharge patterns [89-91]. These patterns could be reproduced through the numerical simulations of bond percolation on a two-dimensional lattice. It was assumed that the growth probability of these patterns depends on E_{loc} . A similar approach was recently used to model t_{BD} for a thin layer of silicon dioxide situated in between two conductors [92, 93]. In this approach, silicon dioxide breaks down when the cluster of connected bonds grows from one interface to another [92, 93]. Fig. 2.7 shows the general schematic of a percolation path formed within

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the gate oxide of a n-MOSFET due to the accumulation of various types of defects. The n⁺-type polycrystalline-silicon gate and the p-type silicon substrate are electrically connected with each other via the percolation path, allowing a huge amount of the electrons to flow from the cathode to the anode.

R. Degraeve *et al.* [9, 10] first reported the simulations of a percolation approach to model gate dielectric breakdown in the thin film of silicon dioxide. In this work, spheres with a radius of a_0 , which are defects generated during electrical stressing, are randomly placed in a three-dimensional matrix that represents the covalent network of silicon dioxide. The statistical distribution of the sphere or defect density that permits the formation of a conductive channel within the gate oxide can be determined. At a given sphere or defect density, a dielectric breakdown event will occur with higher probability with decreasing T_{ox} . In addition, the spread of the dielectric breakdown distribution is larger in the thin gate oxide. Both of these behaviors are in well agreement with the experimental observations. J. H. Stathis [12] further developed the percolation model to the ultrathin gate oxide, showing that the critical defect density will eventually become independent on T_{ox} . According to J. H. Stathis [12], the percolation model with a non-uniform distribution of defective sites may be a more appropriate model for gate dielectric breakdown, because defects are preferentially generated near the substrate and the gate electrode.

The statistics of gate dielectric breakdown are usually described using the Weibull distribution [12, 94, 95], which is given by

$$F(x) = 1 - \exp\left[-\left(\frac{x}{\alpha}\right)^\beta\right] \quad (2.8)$$

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where β is known as the slope parameter. The Weibull distribution is an extreme-value distribution in $\ln(x)$ and is appropriate for problems involving a weakest link. From elementary statistics, if the probability for any one unit fails is p , then the probability for any one of N independent units fails is

$$F = 1 - (1 - p)^N. \tag{2.9}$$

Eqn. (2.9) can be reorganized as

$$W = \ln[-\ln(1 - F)] = \ln(N) + \ln(-\ln(1 - p)). \tag{2.10}$$

W is known as the Weibit. Note that β is an important parameter in the evaluation of the gate dielectric reliability.

Figure 2.8. Weibull distribution in describing the statistics of gate dielectric breakdown for various T_{ox} [95]. It can be observed that the slope, which is β , decreases with decreasing T_{ox} .

It has been reported that β decreases with decreasing T_{ox} . A typical example for the dependence of T_{ox} on β is shown in Fig. 2.8 [95]. One of the important advantages of the

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percolation model is to establish a direct correlation between β and the critical number of defects required in triggering the occurrence of a dielectric breakdown event. The percolation model predicts that the occurrence of a dielectric breakdown event is associated with a singular behavior when T_{ox} becomes less than or comparable to the defect size, that is, T_{ox}/a_0 is getting closer to 1. This suggests that in sub-90-nm CMOS technology with T_{ox} less than 1.6 nm, a single defect created near the center of the gate oxide will be sufficient to form a conductive channel within the gate oxide. However, it is reported that the number of defects required to trigger a dielectric breakdown event might be larger than one, even though β is equal to one [96, 97].

The TDDB power-law model [31, 98], which was first published by E. Wu *et al.*, mainly describes the voltage acceleration of ultrathin gate dielectric breakdown. One of the major capabilities of the TDDB power-law model is to accurately analyze the gate dielectric breakdown data with various T_{ox} [95, 98]. As compared to the TDDB exponential model, which has been applied in older CMOS technology nodes, the TDDB power-law model gives a more optimistic gate oxide lifetime prediction. J. H. Stathis reported that for 100 ppm failure rate and the gate area of $0.1 \mu\text{m}^2$, the maximum allowable supply voltage projected based on the TDDB exponential model will be unacceptably low when T_{ox} is scaled below 2 nm [44]. However, the TDDB power-law model projects that the maximum allowable supply voltage at $T_{ox} = 1 \text{ nm}$ is approximately 1 V [44]. Furthermore, the power exponent (n), which is the acceleration factor for TDDB, serves as another important parameter in the TDDB power-law model. n for n-MOSFETs varies between 41 and 44 [99]. According to Ref. [100], the hydrogen release mechanism at the Si-SiO₂ interface is most likely governed by the single electron-induced coherent

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multi-level excitation of Si-H vibration. This comes from the conclusion that $n = 41-44$ is in good agreement with the power exponent of 40-48 in the model of Si-H desorption at the silicon interface, which was proposed by McMahon *et al.* [101].

Figure 2.9. Some typical examples of the progressive breakdown reported in Ref. [23], in which ultrathin silicon oxynitride was stressed with various $V_{gstress}$.

2.7 PROGRESSIVE BREAKDOWN

Progressive breakdown is a unique phenomenon that can only be observed in the ultrathin gate dielectric breakdown [22-24]. Fig. 2.9 shows some typical examples of the progressive breakdown, in which ultrathin silicon oxynitride with $T_{ox} = 1.5\text{ nm}$ was stressed with various $V_{gstress}$ [23]. Instead of an abrupt jump, I_g evolved into a next higher leakage level with a gradual profile after a dielectric breakdown event is triggered. The progressive breakdown starts by the digital fluctuation of I_g . After a certain period of time, I_g will rapidly degrade until a point beyond which I_g gradually saturates. The occurrence

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of a thermal runaway can be identified by a sudden, abrupt increase in I_g after sometimes in the saturation of I_g , whereas a device experiences a catastrophic or hard breakdown. According to J. S. Suehle *et al.* [24], the early stage of the progressive breakdown is classified as digital breakdown, while the later stage of the progressive breakdown is classified as analog breakdown. The digital breakdown corresponds to a “digitally” fluctuated I_g , while the analog breakdown corresponds to a relatively stable I_g . A device will not fail at the onset of the progressive breakdown as I_g still remains in a reasonably low conduction state. However, the failure of a device will occur when I_g progressively evolves to a leakage level that causes the disruption of device performance. This means that the progressive breakdown provides an extra post-breakdown reliability margin. Therefore, the understandings on the physical mechanisms governing the evolution of I_g during the progressive breakdown are critical for the reliability projection of nanoscale CMOS devices with ultrathin gate oxide.

2.8 BREAKDOWN MODE

Substantial progress has been made to understand the effects of a soft and a hard breakdown [17-21] on device operations and circuit functions, even though a universally accepted criterion has yet to emerge. For instance, a soft breakdown is dominant if I_g does not exceed a certain value, the increase in I_g is less than N times of I_g upon the occurrence of a dielectric breakdown event, the degradation of device performance is within a specific percentage, etc. One of the relatively common methods in differentiating a soft and a hard breakdown is based on the behaviors of I_g - V_g curves, as shown in Fig. 2.10 [18]. Note that SBD Types 2 and 3 are not universal definitions for the soft breakdown

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types, in which different research groups may have different arguments. Generally, it is well accepted that the progressive breakdown is constituted by both the soft and the hard breakdown

Figure 2.10. Behaviors of I_g - V_g curves in differentiating a soft and a hard breakdown [18]. Note that SBD Types 2 and 3 are not universal definitions for the soft breakdown types, in which different research groups may have different arguments.

For the thick gate oxide, the occurrence of a dielectric breakdown event is immediately followed by a hard breakdown. However, many studies have reported that the ultrathin gate oxide is associated with a new type of breakdown modes, which is named as soft breakdown. In general, a soft breakdown occurs when there is an anomalous increase in SILC without the creation of severe damages to the gate oxide. As compared to a hard breakdown, a soft breakdown is still identified as a low conduction state, in which a device is still partially functioning [17-21]. Soft breakdown has been at least classified into three different types, namely [102-104]:

- Analog soft breakdown – It is characterized by random noise.

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- Digital soft breakdown – It is characterized by a telegraph-switching pattern.
- Micro-breakdown – It is characterized by a leakage current that is smaller than I_g in a typical soft breakdown. It has not yet been detected in devices with large areas.

According to S. H. Lee *et al.* [105], a soft breakdown corresponds to local physical damages at the interface of the anode caused by the electrons tunneling into the oxide conduction band. The damaged interface of the anode is then modeled as a series resistance with a trapezoidal potential barrier on reduced “electrical” thickness [105]. In addition, a soft breakdown may correspond to the initial stage of the progressive breakdown, in which defects are gradually created in the vicinity of the percolation path [9, 10, 92, 93]. Since the electrical properties of a device with a soft breakdown normally do not experience any significant variation (i.e., variation in critical device parameters is within specification); thus, for some of the applications, the occurrence of a soft breakdown does not necessarily imply device failure.

As compared to a soft breakdown, a hard breakdown is identified as a high conduction state [17-21]. A hard breakdown, which is believed due to the occurrence of a thermal runaway, normally corresponds to the creation of severe damages to the gate oxide that result in total device malfunctioning. The I - V characteristics for a device with a hard breakdown often appear in a nearly resistor-like shape, as shown in Fig. 2.10. S. Lombardo *et al.* studied a hard breakdown from the point of views of stored energy in capacitors [106]. However, some of the researchers reported that the concept or model of stored energy in capacitors could not provide convincing explanations on the occurrence of a hard breakdown [107, 108]. Basically, most of the researchers agree that the physical origins of a soft and a hard breakdown possess the same nature. It is believed that the

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major difference between a soft and a hard breakdown is the process of energy dissipation [107, 108]. During the occurrence of a hard breakdown, the local temperature in the vicinity of the percolation path may rise above the silicon melting point [109, 110]. As a result, this could lead to the formation of severe, irreversible microstructure damages [109, 111-116] within a device. S. Lombardo *et al.* suggested that if a high E_{ox} is maintained after the occurrence of a hard breakdown, then the location of a percolation path formed within the gate oxide will propagate with the sound velocity from the initial position [106]. For clarity, the general difference between a soft and a hard breakdown is summarized in Table 2.1.

Soft Breakdown	Hard Breakdown
<ul style="list-style-type: none">• Low conduction state.• Partial device malfunctioning.• No thermal runaway.• No severe microstructure damages.• I-V characteristics are difficult to quantify.	<ul style="list-style-type: none">• High conduction state.• Total device malfunctioning.• Thermal runaway.• Severe microstructure damages.• I-V characteristics behave nearly resistor-like.

Table 2.1. General difference between a soft and a hard breakdown.

2.9 DIELECTRIC-BREAKDOWN-INDUCED EPITAXY

Dielectric-breakdown-induced epitaxy (DBIE) [109, 111-116] is one type of subtle, irreversible microstructure damages that can be observed in a device with either a soft or hard breakdown. Fig. 2.11 shows a typical example for DBIE in a breakdown n- and p-MOSFET. The DBIEs were observed using the transmission electron microscopic (TEM) technique [113]. The formation of DBIE is dependent on stressing polarity, in which DBIE will be formed at the cathode and grow from the cathode to the anode [113]. As shown in Fig. 2.11, DBIE in a p-MOSFET stressed with a negative V_g is formed at the

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polycrystalline-silicon gate, but DBIE in a n-MOSFET stressed with a positive V_g is formed at the silicon substrate. It has been found that the size of DBIE in a n-MOSFET is nearly twice larger than that in a p-MOSFET [114]. The results suggest that the direction of an electron wind force during electrical stressing serves as one of the crucial factors in forming DBIE. The studies of DBIE are particularly important as it is believed that the formation and the evolution of DBIE play a critical role in affecting the conduction mechanisms during the progressive breakdown.

Figure 2.11. Typical example for DBIE in a breakdown n- and a p-MOSFET, in which these are observed using the TEM technique [113]. DBIE in a p-MOSFET stressed with a negative V_g is formed at the polycrystalline-silicon gate, but DBIE in a n-MOSFET stressed with a positive V_g is formed at the silicon substrate.

A model has been proposed to describe the formation and the evolution of DBIE during the progressive breakdown, as shown in Figure 2.12 [109]. At a constant V_g , the energetic electrons that tunnel through the gate oxide from the cathode to the anode will result in defect generation. A percolation path will be formed within the gate oxide after the defect density reaches a critical threshold, electrically connecting the polycrystalline-silicon gate and the silicon substrate with each other. A large amount of I_g will locally

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surge through the narrow percolation path. Since the Joule heating effects are proportional to the square of the current density; thus, the local temperature in the vicinity of the percolation path will be substantially high and is believed could exceed the silicon melting point [109, 110, 113, 114].

Figure 2.12. Model that describes the formation and the evolution of DBIE during the progressive breakdown [109].

The percolation path is believed to be a dynamically grown conductive channel, in which it could laterally dilate during the progressive breakdown [115]. As the local temperature in the vicinity of the percolation path rises, more defects around the percolation path will be thermally activated and created. Eventually, the enhanced local Joule heating effects will cause the percolation path to laterally dilate [115]. This model assumes that I_g flowing through the percolation path increases with increasing local temperature. According to M. Houssa *et al.* [11], the dependence of I_g flowing through a percolation

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cluster on temperature is believed due to the scattering of the electrons by a random array of dangling bonds and defects that are present in the vicinity of the percolation path [11]. Obviously, as I_g increases, the local temperature in the vicinity of the percolation path will be further enhanced. This current-temperature positive feedback loop ensures a continuous increase in I_g and the local temperature in the vicinity of the percolation path, as long as the gate oxide stressing is maintained.

When the local temperature in vicinity of the percolation path becomes comparable or higher than the silicon melting point, silicon-silicon bonds at the silicon substrate just below the vicinity of the percolation path will be broken. The formation of DBIE begins with the drift of dislodged silicon atoms from the silicon substrate to the gate oxide. The silicon flux that contributes to the formation of DBIE contains two main components [109, 113, 114]:

- The accelerated self-diffusion of the dislodged silicon atoms due to the presence of a very steep thermal gradient in the vicinity of the percolation path.
- The enhanced migration of the dislodged silicon atoms due to the presence of a very strong electron wind force from the cathode to the anode through the percolation path.

After DBIE is formed, the thermal runaway may be alleviated through the consumption of the free energy in the system as well as the reconfiguration of the percolation path. C. H. Tung *et al.* suggested that one of the following situations may occur during the progressive breakdown [109]:

- For a very low current compliance limit, the current-temperature positive feedback loop is not sufficient to trigger the formation of DBIE. Hence, a soft breakdown without DBIE takes place during the progressive breakdown.

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- For an intermediate current compliance limit, there is an energy balance between the current-temperature positive feedback loop and the evolution of DBIE. If the current-temperature positive feedback loop dominates, I_g will be high, leading to the occurrence of a thermal runaway, and hence, a hard breakdown takes place during the progressive breakdown. In contrary, if the evolution of DBIE dominates, free energy in the system will be consumed, and hence, a soft breakdown with DBIE takes place during the progressive breakdown.
- For a high current compliance limit, the current-temperature positive feedback loop is sufficient to induce the formation of DBIE. Since I_g is high, a thermal runaway will be triggered. As a result, a hard breakdown takes place during the progressive breakdown.

2.10 SUMMARY

Gate dielectric breakdown is one of the most important reliability concerns in the MOSFET miniaturization. Many studies have demonstrated that gate dielectric breakdown becomes more serious as T_{ox} is continuously scaled down in order to achieve superb device performance. Several gate oxide intrinsic breakdown models, such as the thermo-chemical, the anode hole injection, the hydrogen release and the percolation model, have been developed and proposed to understand the physical mechanisms governing the occurrence of a dielectric breakdown event. The ultimate objective of these models is to accurately predict the lifetime of gate oxide from the accelerated stressing conditions to the normal device operations. However, none of these models is able to provide a complete picture in robustly and satisfactorily explaining all the phenomena observed in gate dielectric breakdown. In addition, progressive breakdown, which is a

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unique phenomenon that can only be observed in ultrathin gate dielectric breakdown, has been intensively studied as it provides an extra post-breakdown reliability margin. Also, DBIE is reported as one type of important, irreversible microstructure damages, which could play a critical role in affecting the conduction mechanism during the progressive breakdown.

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EXPERIMENTAL PROCEDURE AND DETAILS

3.1 INTRODUCTION

The reliability of gate dielectric becomes a critical concern as T_{ox} is scaled below 3 nm in advanced CMOS technology [4-8]. The gate oxide with T_{ox} below 3 nm is considered as the thin gate oxide. I_g in the thin gate oxide is mainly attributed to the direct tunneling mechanism [25-30]. In addition, the gate oxide with T_{ox} below 2 nm is considered as the ultrathin gate oxide. Different from a sudden, abrupt increase in I_g observed in the thick gate oxide, the degradation of I_g in the thin or ultrathin gate oxide is progressive. The role of the progressive breakdown in extending the post-breakdown lifetime of nanoscale CMOS devices with thin or ultrathin gate oxide is particularly important [22-24]. For that reason, the testing algorithms and techniques of traditional reliability characterization used for the thick gate oxide must be revised and modified such that the study of ultrathin gate dielectric reliability can be more precise.

In this chapter, the procedure and the details of various types of stressing methodologies are thoroughly discussed. Furthermore, a new stressing methodology, which is known as a K-cycle multiple-stage constant-voltage stress (CVS), has been developed specifically for the study of progressive breakdown. It allows us to further understand the physical mechanisms governing the behaviors of I_g at different stages of the progressive breakdown.

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3.2 SAMPLE INFORMATION AND EQUIPMENT

Devices used in this study are isolated n-MOSFETs fabricated by standard sub-0.13- μm CMOS technology. The gate dielectrics of the n-MOSFETs, which are ultrathin silicon oxynitride, were grown on p-type (110) silicon wafers in an oxygen ambient followed by an N_2O annealing at a temperature range of 900-1000 $^{\circ}\text{C}$ in a rapid thermal oxidation system. Additionally, the gate electrodes of the n-MOSFETs are heavily-doped n-type polycrystalline silicon. Table 3.1 shows the gate oxide thickness, the channel length (L) and the channel width (W) of the n-MOSFETs investigated in this study.

Gate Oxide Thickness (T_{ox})	Channel Lengths (L)	Channel Widths (W)
12 to 22 $\text{\AA}$	0.04 to 1 μm	0.1 to 1.2 μm

Table 3.1. T_{ox} , L and W of the n-MOSFETs investigated in this study.

Figure 3.1. (a) 8-inch Cascade Microtech wafer probe station. (b) Agilent Technologies E4156/5280 precision semiconductor parameter analyzer.

The equipment used for reliability characterization includes an 8-inch Cascade Microtech wafer probe station and an Agilent Technologies E4156/5280 precision semiconductor parameter analyzer, which are shown in Figs. 3.1(a) and 3.1(b),

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respectively. The 8-inch Cascade Microtech wafer probe station serves as a platform for the gate oxide stressing and all the related electrical measurements. It consists of a 372-572-K thermo-chuck for holding an 8-inch (or 200-mm) wafer at different temperatures. The Agilent Technologies E4156/5280 precision semiconductor parameter analyzer is mainly used to perform the gate oxide stressing and all the related electrical measurements. It consists of four highly accurate source-monitor units (SMUs) with a current resolution of 1 fA and a voltage resolution of 2 μ V, as shown in Fig. 3.1(b). These SMUs are separately connected to four Cascade Microtech probe heads placed on the 8-inch Cascade Microtech wafer probe station via Kelvin tri-axial cables with low leakage currents. These probe heads are primarily used to steadily hold the tungsten needles, which are separately connected to the drain terminal, the source terminal, the gate electrode and the substrate of a MOSFET.

3.3. CALCULATION OF STRESSING GATE VOLTAGE

Before the gate oxide stressing is carried out, the breakdown voltage (V_{BD}) of the n-MOSFET must be determined. V_g represents a voltage that is applied to the gate electrode of a n-MOSFET, while V_d , V_s and V_{sub} denote the drain, the source and the substrate voltage, respectively. The I_g - V_g measurement was carried out by sweeping V_g from 0 V to a higher value with a constant voltage increment of 0.05 or 0.1 V, while the drain terminal, the source terminal and the substrate of the n-MOSFET were grounded (i.e., $V_d = V_s = V_{sub} = 0$). I_g increased with increasing V_g due to the direct tunneling of the charge carriers through the gate oxide. When I_g experienced a sudden, abrupt increase, the n-MOSFET was said to encounter a dielectric breakdown event, and the corresponding V_g was treated

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as V_{BD} . Fig. 3.2(a) shows a typical example for the I_g - V_g ramping test in determining V_{BD} for a n-MOSFET with $T_{ox} = 16 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$. This procedure was repeated for about 10-20 n-MOSFETs that possess the same dimensions and were well distributed over a wafer. Eventually, the average breakdown voltage (V_{BDA}) of a n-MOSFET could be obtained.

Figure 3.2. (a) Typical example for an I_g - V_g ramping test in determining V_{BD} for a n-MOSFET ($T_{ox} = 16 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$). With the presence of a sudden, abrupt increase in I_g , V_{BD} was found to be 3.38 V. (b) β versus V_g relationship reported in Ref. [117].

$V_{gstress}$ defines a constant V_g used to stress the gate oxide of a n-MOSFET. By knowing V_{BDA} , $V_{gstress}$ could be determined. Basically, $V_{gstress}$ must be lower than V_{BDA} such that a dielectric breakdown event will not immediately occur upon the gate oxide stressing. The formula for the calculation of $V_{gstress}$ is given by [117]

$$\ln(t_{BD}) = \ln(t_{BD}') + \beta(V_{BDA} - V_{gstress}) \quad (3.1)$$

where t_{BD} and t_{BD}' are the time-to-dielectric-breakdown of gate oxide at $V_{gstress}$ and V_{BDA} , respectively. In this study, t_{BD} was specified in the range of 100-3000 s. β is a voltage acceleration factor. β for a particular V_g was estimated from Fig. 3.2(b), which shows the

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β versus V_g relationship reported in Ref. [117]. Fig. 3.3 shows a flowchart describing the procedure of calculating $V_{gstress}$ in accordance with the estimation of V_{BDA} , Eqn. (3.1) and Fig. 3.2(b). The calculated $V_{gstress}$ for $T_{ox} = 12\text{-}22\text{ \AA}$ used in this study are summarized in Table 3.2.

Figure 3.3. Flowchart describing the procedure of calculating $V_{gstress}$ in accordance with the estimation of V_{BDA} , Eqn. (3.1) and Fig. 3.2(b).

T_{ox}	12.5 Å	16 Å	16.5 Å	20 Å	22 Å
$V_{gstress}$	2.6 to 2.7 V	3 to 3.3 V	2.9 to 3.1 V	3.7 to 4 V	3.9 to 4.2 V

Table 3.2. $V_{gstress}$ for $T_{ox} = 12.5, 16, 16.5, 20$ and $22\text{ \AA}$ calculated based on the estimation of V_{BDA} , Eqn. (3.1) and Fig. 3.2(b).

3.4 STRESSING METHODOLOGIES

3.4.1 CONSTANT-VOLTAGE STRESS

Constant-voltage stress (CVS) is one of the widely used stressing methodologies in the study of ultrathin gate dielectric reliability [118-120]. For the thin or ultrathin gate oxide, the direct tunneling of the charge carriers through the gate oxide is ballistic or quasi-ballistic in nature. This implies that the generation of defects within the gate oxide depends on the energy of the charge carriers at the anode, which is primarily controlled by V_g . Therefore, in order to more precisely study ultrathin gate dielectric breakdown, a constant-current stress, which is normally used for the thick gate oxide, has been replaced by a CVS.

In a CVS, the gate oxide of a n-MOSFET was stressed with $V_{gstress}$ based on Table 3.2 until specific dielectric breakdown criteria were met. Fig. 3.4 shows the evolution of I_g for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.3 \text{ \mu m}^2$) stressed using a CVS with $V_{gstress} = 4.1 \text{ V}$ in inversion mode at the room temperature. The inset at the upper right of Fig. 3.4 shows an enlarged view of the profile of SILC in linear scale, in which I_g increased with increasing stressing time due to the generation of electronic traps within the gate oxide during electrical stressing. The gate oxide stressing was normally terminated when a sudden, abrupt increase in I_g with the magnitude of more than two times larger than the fresh or non-breakdown I_g was detected. A sudden, abrupt increase in I_g is generally identified as the occurrence of a dielectric breakdown event. According to the percolation model proposed by R. Degraeve *et al.* [9, 10], a dielectric breakdown event occurs when a conductive percolation path is formed within the gate oxide, electrically connecting the gate electrode and the substrate of a n-MOSFET with each

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other. As shown in the inset at the lower right of Fig. 3.4, I_g gradually evolved into a higher level after the occurrence of a dielectric breakdown event, indicating the existence of the progressive breakdown.

Figure 3.4. Evolution of I_g for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.3 \text{ \mu m}^2$) stressed using a CVS with $V_{gstress} = 4.1 \text{ V}$ in inversion mode at the room temperature. The whole process involving the generation of the electronic traps within the gate oxide and the occurrence of a dielectric breakdown event is universally referred to as TDDB. The inset at the upper right shows an enlarged view of the profile of SILC in linear scale. SILC increased with increasing stressing time due to the generation of electronic traps within the gate oxide during electrical stressing. The inset at the lower right shows an enlarged view of the profile of I_g for the n-MOSFET after 430 s. It can be noticed that I_g took about 6 s to reach $100 \text{ \mu A}$ after the occurrence of a dielectric breakdown event.

When the gate oxide of a n-MOSFET is stressed using a CVS, I_g will gradually increase with time due to the generation of electronic traps within the gate oxide caused by the charge carrier tunneling, resulting in the creation of SILC [55-57]. The whole process involving the generation of the electronic traps within the gate oxide and the occurrence of a dielectric breakdown event produces TDDB [13].

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3.4.2 SUCCESSIVE OR CURRENT-LIMITED CONSTANT-VOLTAGE STRESS

Successive CVS is another stressing methodology frequently used in this study. A successive CVS was developed on the basis of a CVS. The major objective of using a successive CVS is to study the I - V characteristics at different stages of the progressive breakdown for a n-MOSFET [118, 120]. A current compliance limit (I_{gl}) is a controlling parameter mainly used to determine one particular stage of the progressive breakdown. Hence, a successive CVS is also referred to as current-limited CVS. Note that the fastest response time of I_{gl} used in this study is 0.5 s. In the beginning of a successive CVS, the gate oxide of a n-MOSFET was stressed with a high $V_{gstress}$. Note that the choice of $V_{gstress}$ was determined in accordance with Table 3.2. The amount of I_g flowing through the percolation path formed within the gate oxide during the occurrence of a dielectric breakdown event was limited by I_{gl} . The gate oxide stressing was automatically halted when I_g reached I_{gl} . This part is similar to a CVS, as discussed above. However, different from a CVS, I_g in a successive CVS is limited by I_{gl} . After collecting all the useful post-breakdown electrical data, the gate oxide stressing was continued by setting a higher I_{gl} without changing $V_{gstress}$. In summary, a successive CVS allows us to monitor the I - V characteristics at different stages of the progressive breakdown for a n-MOSFET by successively increasing I_{gl} . Fig. 3.4 shows the evolution of I_g for a n-MOSFET ($T_{ox} = 20$ Å and $L \times W = 0.5 \times 0.6 \mu m^2$) stressed using a successive CVS with $V_{gstress} = 3.9$ V in inversion mode at the room temperature. I_{gl} was initially set to 10 μA . After I_g reached 10 μA , I_{gl} was increased to 15 μA , and the gate oxide stressing was continued. The similar procedure was repeated for $I_{gl} = 20, 30, 50, 100$ and 200 μA , while $V_{gstress}$ remained unchanged at 3.9 V.

Figure 3.5. Evolution of I_g for a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ }\mu\text{m}^2$) stressed using a successive CVS with $V_{gstress} = 3.9 \text{ V}$ in inversion mode at the room temperature. I_{gl} was initially set as 10 μ A. After I_g reached 10 μ A, I_{gl} was increased to 15 μ A, and the gate oxide stressing was continued. The similar procedure was repeated for $I_{gl} = 20, 30, 50, 100$ and 200 μ A, while $V_{gstress}$ remained unchanged at 3.9 V. I_{gl} was used to determine one particular stage of the progressive breakdown.

3.4.3 TWO-STAGE CONSTANT-VOLTAGE STRESS

In order to acquire more insightful data that can improve the understandings on the physical mechanisms governing the progressive breakdown, the I - V characteristics at different stages of the progressive breakdown for a n-MOSFET must be studied in details. This can only be achieved if the progressive breakdown evolves with a relatively slower rate. However, as shown in Fig. 3.5, the progressive breakdown arrested under a successive CVS with a high $V_{gstress}$ rapidly evolved. For that reason, the major objective of using a two-stage CVS, which was developed by modifying a successive CVS, is to prolong the progressive breakdown [16, 121]. Obviously, a two-stage CVS is constituted by two main phases of implementation:

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• 1st-stage CVS:

The 1st-stage CVS is responsible for accelerating the generation of the electronic traps within the gate oxide until the occurrence of a dielectric breakdown event is triggered. In other words, the main objective of the 1st-stage CVS is to complete the TDDB of a n-MOSFET within a reasonable window of time. Similar to a successive CVS, the n-MOSFET was initially stressed under the accelerated stressing conditions with a high $V_{gstress}$ based on Table 3.2. However, a low I_{gl} of 1-10 μ A was used to limit the amount of I_g flowing through a percolation path formed within the gate oxide during the occurrence of a dielectric breakdown event. The purpose of using a low I_{gl} is to ensure that the early stage of the progressive breakdown can be successfully arrested. In general, the 1st-stage CVS was implemented as a successive CVS with a low I_{gl} .

T_{ox}	12.5 Å	16 Å	16.5 Å	20 Å	22 Å
$V_{gstress}$ used in the 2 nd -stage CVS	1.8 to 2.4 V	2.3 to 2.6 V	2.3 to 2.6 V	3 to 3.3 V	3.2 to 3.5 V

Table 3.3. $V_{gstress}$ used in the 2nd-stage CVS for T_{ox} = 12.5, 14.5, 16, 20 and 22 Å.

• 2nd-stage CVS:

After a dielectric breakdown event occurred in the 1st-stage CVS, a lower $V_{gstress}$, which is summarized in Table 3.3, was used to further stress the gate oxide of the n-MOSFET. In the 2nd-stage CVS, either the stressing time or I_{gl} served as a controlling parameter in selectively halting the progressive breakdown. This allows us to study the I - V characteristics at different stages of the progressive breakdown for the n-MOSFET in details, in which this is useful in analyzing the severity of the progressive breakdown. Some of the examples will be provided in the following section.

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Figure 3.6. Evolution of I_g for a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. **(a)**, **(b)** Evolution of I_g in the 1st- and the 2nd-stage CVS, respectively, for the n-MOSFET. In the 1st-stage CVS, $V_{gstress} = 4 \text{ V}$ and $I_{gl} = 10 \text{ \mu A}$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.2 V without setting any limit on I_{gl} . The 1st-stage CVS corresponds to the TDDB of the n-MOSFET, while the 2nd-stage CVS corresponds to the progressive breakdown for the n-MOSFET. The red arrow in (b) shows a typical evolving trend for the progressive breakdown, which is in well agreement with the results demonstrated in Fig. 2.9.

Fig. 3.6 shows the evolution of I_g for a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. Fig. 3.6(a) show the evolution of I_g in the 1st-stage CVS for the n-MOSFET, where $V_{gstress} = 4 \text{ V}$ and $I_{gl} = 10 \text{ \mu A}$ were used. On the other hand, Fig. 3.6(b) shows the evolution of I_g in the 2nd-stage CVS for the n-MOSFET, where $V_{gstress}$ was reduced to 3.2 V without setting any limit on I_{gl} . The 1st-stage CVS corresponds to the TDDB of the n-MOSFET, while the 2nd-stage CVS corresponds to the progressive breakdown for the n-MOSFET. The red arrow in (b) shows a typical evolving trend for the progressive breakdown, which is in well agreement with the results demonstrated in Fig. 2.9. Comparing to the progressive breakdown in Fig. 3.5, it can be observed that the progressive breakdown in Fig. 3.6(b) has been successfully prolonged using a two-stage CVS.

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3.4.4 K-CYCLE MULTIPLE-STAGE CONSTANT-VOLTAGE STRESS

A two-stage CVS was further developed into a K-cycle multiple-stage CVS. The main objective of a K-cycle multiple-stage CVS is to study the behaviors of I_g at different stages of the progressive breakdown under various conditions. In general, a K-cycle multiple-stage CVS is a repetitive process of stressing the gate oxide of a n-MOSFET with one particular range of V_g , which can be as low as V_{op} . Similar to the two-stage CVS, a K-cycle multiple-stage CVS started by stressing the gate oxide of a n-MOSFET with $V_{gstress}$ shown in Table 3.2, ensuring that the TDDB of the n-MOSFET could be completed within a reasonable window of time. $I_{gl} = 1-10 \mu A$ was used to limit I_g at a low level during the occurrence of a dielectric breakdown event such that the early stage of the progressive breakdown could be successfully arrested. After the TDDB of the n-MOSFET was completed with the detection of a sudden, abrupt increase in I_g , the 1st-cycle multiple-stage CVS was carried out. V_{init} and V_{final} define an initial and a final $V_{gstress}$ used in the 1st-cycle multiple-stage CVS, respectively. The n-MOSFET was stressed with $V_{gstress} = V_{init}$ for a specific constant duration, which was represented as t_{stress} . The gate oxide stressing was repeated by increasing $V_{gstress}$ with a constant voltage denoted as ΔV , until V_{final} was reached. V_{final} could be determined when $I_g = I_{gl}$ was satisfied. On the other hand, V_{final} could be set as a voltage lower than certain a threshold value to prevent the further evolution of the progressive breakdown, depending on the purpose of the experiment. In each cycle of the experiment, the gate oxide of the n-MOSFET was stressed from V_{init} to V_{final} with a constant increment of ΔV . Thus, this stressing methodology is referred to as a multiple-stage CVS. This was followed by the 2nd-, the 3rd-, and the Kth-cycle multiple-stage CVS, which was similar to the 1st-cycle multiple-stage CVS. Since the procedure of

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a multiple-stage CVS was repeated, we eventually named this stressing methodology as a K-cycle multiple-stage CVS.

Figure 3.7. Flowchart describing the procedure of implementing a K-cycle multiple-stage CVS.

Fig. 3.7 summarizes the general procedure of implementing a K-cycle multiple-stage CVS. For clarity purpose, the stressing conditions used in the K^{th} -cycle multiple-stage CVS would be defined as $V_{init}(K)$, $\Delta V(K)$, $t_{stress}(K)$ and $V_{final}(K)$. Fig. 3.8 shows the evolution of I_g for an n-MOSFET ($T_{ox} = 16 \text{ \AA}$ and $L \times W = 0.3 \times 0.3 \text{ \mu m}^2$) stressed using a two-cycle multiple-stage CVS in inversion mode at the room temperature. Fig. 3.8(a) shows the TDDb of the n-MOSFET, while Fig. 3.8(b) shows the evolution of I_g in the 1st- and the

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2nd-cycle multiple-stage CVS for the n-MOSFET. In Fig. 3.8(b), the black, the red and the blue line show I_g at $V_{gstress} = 1.7, 1.8$ and 1.9 V, respectively.

(a)

(b)

Figure 3.8. Evolution of I_g for a n-MOSFET ($T_{ox} = 16$ Å and $L \times W = 0.3 \times 0.3$ μm²) stressed using a two-cycle multiple-stage CVS in inversion mode at the room temperature. (a) Evolution of I_g before the occurrence of a dielectric breakdown event for the n-MOSFET. (b) Evolution of I_g in the 1st- and the 2nd-cycle multiple-stage CVS for the n-MOSFET. The TDDB of the n-MOSFET was carried out with $V_{gstress} = 3.1$ V and $I_{gl} = 10$ μA. The two-cycle multiple-stage CVS was performed with $V_{init}(1) = V_{init}(2) = 1.7$ V, $\Delta V(1) = \Delta V(2) = 0.1$ V and $t_{stress}(1) = t_{stress}(2) = 300$ s and $V_{final}(1) = V_{final}(2) = 1.9$ V.

The TDDB of the n-MOSFET was carried out with $V_{gstress} = 3.1$ V and $I_{gl} = 10$ μA. Note that the profile of SILC, which was the evolution of I_g before the gate dielectric breakdown was triggered, was similar to those shown in Figs. 3.4, 3.5 and 3.6(a), in which the generation of electronic traps within the gate oxide during electrical stressing leads to the gradual increase in I_g . The occurrence of a dielectric breakdown event was detected when I_g experienced an instantaneous jump to 10 μA. The stressing conditions of the 1st- and the 2nd-cycle multiple-stage CVS were $V_{init}(1) = V_{init}(2) = 1.7$ V, $\Delta V(1) = \Delta V(2) = 0.1$ V and $t_{stress}(1) = t_{stress}(2) = 300$ s and $V_{final}(1) = V_{final}(2) = 1.9$ V.

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Figure 3.9. I_d - V_d characteristics for SI at $I_{gl} =$ (a) 60 and (b) 250 μA , where $V_d = 0.6, 0.9, 1.2$ and 1.5 V. g_m - V_g characteristics for SI at $I_{gl} =$ (c) 60 and (d) 250 μA , where $V_d = 0.05$ V. (e) I_g - V_g characteristics of SI at $I_{gl} = 60$ and 250 μA . The fresh I_d - V_d , g_m - V_g and I_g - V_g characteristics for SI were plotted for comparison. At $I_{gl} = 60 \mu\text{A}$, I_g is considered to be in a soft-breakdown regime. On the other hand, at $I_{gl} = 250 \mu\text{A}$, I_g is considered to be in a severe soft-breakdown or hard-breakdown regime.

3.5 POST-BREAKDOWN ELECTRICAL MEASUREMENTS

The hardness of the progressive breakdown can be monitored and quantified using the post-breakdown electrical measurements of a n-MOSFET. Fig. 3.9 shows a typical example. *S1*, which represents a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.2 \times 0.3 \text{ \mu m}^2$) stressed using a successive CVS in inversion mode at the room temperature, will be used in the subsequent discussion. The I_d - V_d , the g_m - V_g and the I_g - V_g characteristics for a n-MOSFET are three main types of post-breakdown electrical measurements used in this study to investigate the hardness of the progressive breakdown, where I_d and g_m denote the drain current and the transconductance of the n-MOSFET, respectively.

- For the I_d - V_d measurement, I_d was measured at a given constant V_g by sweeping V_d , while the source terminal and the substrate of the n-MOSFET were grounded (i.e., $V_s = V_{sub} = 0$). Figs. 3.9(a) and 3.9(b) show the I_d - V_d characteristics for *S1* at $I_{gl} = 60$ and $250 \text{ \mu A}$, respectively, where $V_g = 0.6, 0.9, 1.2$ and 1.5 V .
- For the g_m - V_g measurement, I_d was measured at a given constant V_d by sweeping V_g , while the source terminal and the substrate of the n-MOSFET were grounded (i.e., $V_s = V_{sub} = 0$). g_m was determined by dI_d/dV_g . Figs. 3.9(c) and 3.9(d) show the g_m - V_g characteristics for *S1* at $I_{gl} = 60$ and $250 \text{ \mu A}$, respectively, where $V_d = 0.05 \text{ V}$.
- For the I_g - V_g measurement, I_g was measured by sweeping V_g , while the drain terminal, the source terminal and the substrate of the n-MOSFET were grounded (i.e., $V_d = V_s = V_{sub} = 0$). Fig. 3.9(e) show the I_g - V_g characteristics for *S1* at $I_{gl} = 60$ and $250 \text{ \mu A}$.

The I_d - V_d , the g_m - V_g and the I_g - V_g characteristics for *S1* before the occurrence of a dielectric breakdown event were also plotted for comparison. The case of $I_{gl} = 60 \text{ \mu A}$ is considered as a soft breakdown. On the other hand, the case of $I_{gl} = 250 \text{ \mu A}$ is considered

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as a severe soft breakdown or hard breakdown. It can also be observed that the post-breakdown I_d and g_m were lower and degraded. This is mainly due to the presence of an excessively large I_g flowing through the gate dielectric of SI . Similar phenomenon can be noticed in the I_s - V_s characteristics for SI , where I_s denotes the source current. Obviously, when the progressive breakdown evolved, the curve of I_g - V_g would continuously degrade.

The breakdown location, which is denoted as s_{BD} , defines the location of a percolation path along the channel of a device [122-124]. s_{BD} serves as an important parameter in the study of gate dielectric breakdown. B. Kaczer *et al.* proposed that s_{BD} can be calculated as [122-124]

$$s_{BD} = \left(\frac{\Delta I_d}{\Delta I_d + \Delta I_s} \right) \times L \quad (3.2)$$

where ΔI_d and ΔI_s are the increase in I_d and I_s after the occurrence of a dielectric breakdown event. Eqn. (3.2), which is derived in accordance with a current-separation methodology, is the location of a percolation path as a fraction of the device channel. $s_{BD} = 0$ and $1L$ represent the source and the drain terminal of a breakdown n-MOSFET, respectively. The post-breakdown electrical measurements in evaluating Eqn. (3.2) should be carried out in accumulation mode. In inversion mode, the accuracy of Eqn. (3.2) will be affected by two factors: (a) the presence of a voltage offset between the drain and the source terminal, and (b) the series resistances on the source and the drain terminal [124].

3.6 SUMMARY

In order to more thoroughly understand the physical mechanisms governing the progressive breakdown, a K-cycle multiple-stage CVS was developed. Using this new

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stressing methodology, the behaviors of I_g at different stages of the progressive breakdown under various conditions can be thoroughly studied. This provides a lot of useful insights to the study of ultrathin gate dielectric reliability involving the progressive breakdown, which will be discussed in details in *Chapter Four*.

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DIGITAL BREAKDOWN AND ITS CONSEQUENCES ON ULTRATHIN GATE DIELECTRIC RELIABILITY

4.1 INTRODUCTION

In common practice, the gate oxide integrity tests are performed under the accelerated stressing conditions. The main objective is to ensure that TDDB can be completed within a reasonable window of time (e.g., a few hours or days) [13]. The lifetime prediction of gate oxide is evaluated by extrapolating the data of TDDB from the accelerated stressing conditions to the nominal operating conditions using a specific physical model. For the past few decades, various physical models, which describe the possible physical mechanisms responsible for triggering the occurrence of a dielectric breakdown event from different aspects, have been developed. For instance, the anode hole injection model proposes that the lifetime of gate oxide is exponentially dependent on $1/E_{ox}$ [27, 42, 45, 51, 52]. In contrary, according to the thermo-chemical model, t_{BD} is exponentially scaled with E_{ox} [70-73]. None of these gate dielectric intrinsic breakdown models is completely exact. As a result, there exist disagreements, which could be significant in some of the cases, among the lifetime prediction of gate oxide performed by different research groups. It is

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obvious that the reliability of a device projected at V_{op} will be inaccurate if the physical mechanisms governing gate dielectric breakdown at the nominal operating conditions is different from that at the accelerated stressing conditions.

For the gate oxide with T_{ox} below 3 nm, the progressive breakdown is known to provide an extra post-breakdown reliability margin for a slightly malfunctioning device to continuously operate [22-24]. Therefore, the reliability projection of nanoscale CMOS devices with ultrathin gate oxide must take into account the effects of the progressive breakdown. The progressive breakdown can be divided into different stages governed by different physical mechanisms. Digital and analog breakdown are two critical regions of the progressive breakdown that has been intensively studied [24]. Once the progressive breakdown starts to evolve, I_g behaves digital-like, and this region of the progressive breakdown is known as digital breakdown [24]. This is followed by the analog breakdown after a certain period of time, which corresponds to a relatively stable evolution of I_g [24]. However, a thorough study on the behaviors of I_g at different stages of the progressive breakdown under various conditions is still lacking.

In this chapter, we focus on studying the physical mechanisms governing the digital breakdown during the normal device operations. Moreover, the impacts of the digital breakdown on ultrathin gate dielectric breakdown will be comprehensively discussed. According to our findings, the existence of the digital breakdown, which dominates in the early stage of the progressive breakdown at a low V_g , plays a critical role in post-breakdown ultrathin gate dielectric reliability assessment.

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4.2 EXPERIMENTS

To study the physical mechanisms governing the behaviors of I_g in the digital breakdown or the early stage of the progressive breakdown under various conditions, a K-cycle multiple-stage CVS described in *Chapter Three* was used. All the necessary sample information and stressing conditions can also be found in *Chapter Three*.

4.3 CHARACTERIZATION OF POST-BREAKDOWN I_g IN DIGITAL AND ANALOG BREAKDOWN

Fig. 4.1 shows a typical example for the evolution of I_g for a breakdown n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.6 \text{ \mu m}^2$) stressed using a three-cycle multiple-stage CVS in inversion mode at the room temperature. The TDDB of the n-MOSFET was carried out with $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$. The stressing conditions of the 1st-, the 2nd- and the 3rd-cycle multiple-stage CVS were $V_{init}(1) = V_{init}(2) = V_{init}(3) = 1.2 \text{ V}$, $\Delta V(1) = \Delta V(2) = \Delta V(3) = 0.2 \text{ V}$, $t_{stress}(1) = t_{stress}(2) = t_{stress}(3) = 500 \text{ s}$, $V_{final}(1) = V_{final}(2) = 3.4 \text{ V}$ and $V_{final}(3) = 3.6 \text{ V}$. Figs. 4.2(a) and 4.2(b) show an enlarged view of the 1st- and the 3rd-cycle multiple-stage CVS at $V_{gstress} = 1.6, 1.8, 2 \text{ and } 2.2 \text{ V}$ for the n-MOSFET in Fig. 4.1, respectively.

It has been reported in Ref. [24] that during the progressive breakdown, I_g will gradually evolve from the digital breakdown into the analog breakdown, indicating that there are two important regions in the progressive breakdown. Similarly, from Figs. 4.1 and 4.2, it can be observed that the behaviors of I_g at a specific $V_{gstress}$ in the 1st-cycle multiple-stage CVS are different from those in the 2nd- and the 3rd-cycle multiple-stage

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CVS. The 1st-cycle multiple-stage CVS corresponds to the digital breakdown, while the 2nd- and the 3rd-cycle multiple-stage CVS correspond to the analog breakdown.

Figure 4.1. Evolution of I_g for a breakdown n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.6 \text{ \mu m}^2$) stressed using a three-cycle multiple-stage CVS in inversion mode at the room temperature. The TDDDB of the n-MOSFET was carried out with $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$. The three-cycle multiple-stage CVS was performed with $V_{init}(1) = V_{init}(2) = V_{init}(3) = 1.2 \text{ V}$, $\Delta V(1) = \Delta V(2) = \Delta V(3) = 0.2 \text{ V}$, $t_{stress}(1) = t_{stress}(2) = t_{stress}(3) = 500 \text{ s}$, $V_{final}(1) = V_{final}(2) = 3.4 \text{ V}$ and $V_{final}(3) = 3.6 \text{ V}$. Note that $V_{final}(1) = V_{crit}$.

The digital and the analog breakdown are demarcated with each other by the V_{final} of the 1st-cycle multiple-stage CVS. This voltage is a critical gate voltage specifically denoted as V_{crit} (i.e., $V_{crit} = V_{final}(1)$). The effects of V_{crit} on the progressive breakdown will be discussed in details in the following section. Some of the specific properties associated with the digital and the analog breakdown are described as follows:

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Digital Breakdown:

The 1st-cycle multiple-stage CVS corresponds to the early stage of the progressive breakdown, in which the progressive breakdown was initially arrested at a low I_{gl} of 1 μ A. As shown in Figs. 4.1 and 4.2(a), I_g exhibited an irreproducible, random step-like profile, analogous to the results reported in Refs. [22, 24]. This region of the progressive breakdown is commonly referred to as digital breakdown.

Figure 4.2. Enlarged view of (a) the 1st- and (b) the 3rd-cycle multiple-stage CVS at $V_{gstress} = 1.6, 1.8, 2$ and 2.2 V for the n-MOSFET in Fig. 4.1. As shown in (a), the digital fluctuation of I_g can be characterized as: {1} the random oscillation at two specific values, {2} a sudden huge increase and {3} a sudden huge decrease.

The digital fluctuation of I_g can be identified by obvious, drastic switching effects. As shown in Fig. 4.2(a), I_g could instantaneously and randomly increase (or decrease) to a high (or low) level that could be more than one order of magnitude different. For instance, I_g at $V_{gstress} = 2$ V could suddenly increase from $\sim 8 \times 10^{-9}$ A to $\sim 1 \times 10^{-7}$ A (i.e., {2} in Fig. 4.2(a)), while I_g at $V_{gstress} = 2.2$ V could suddenly decrease from $\sim 1.5 \times 10^{-8}$ A to $\sim 1 \times 10^{-9}$ A (i.e., {3} in Fig. 4.2(a)). Furthermore, it can be observed that I_g

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randomly fluctuated or oscillated at two specific values for a given $V_{gstress}$ in most of the times. For instance, it can be seen that at $V_{gstress} = 1.6$ V, the random oscillation in I_g took place between $\sim 2.8 \times 10^{-8}$ A and $\sim 4 \times 10^{-8}$ A (i.e., {1} in Fig. 4.2(a)).

- Analog Breakdown:

In the 2nd- and the 3rd-cycle multiple-stage CVS, as shown in Figs. 4.1 and 4.2(b), I_g is reproducible and steadily increased with increasing $V_{gstress}$, in which no apparent digital fluctuation of I_g can be observed. This region of the progressive breakdown is named as the analog breakdown. In addition, the relationship between I_g and V_g can be modeled using power law, that is

$$I_g = K \times V_g^\alpha \quad (4.1)$$

where K and α are experimentally fitting parameters.

Fig. 4.3(a) shows the evolution of I_g for another breakdown n-MOSFET ($T_{ox} = 22$ Å and $L \times W = 1 \times 0.6 \mu m^2$) stressed using a one-cycle multiple-stage CVS in inversion mode at the room temperature. The n-MOSFET was initially stressed with $V_{gstress} = 4.1$ V and $I_{gl} = 1 \mu A$. The stressing conditions of the one-stage multiple-stage CVS were $V_{init} = 2.6$ V, $\Delta V = 0.1$ V, $t_{stress} = 500$ s and $V_{final} = 3.4$ V. Figs. 4.3(b) and 4.3(c) show the I_g - V_g characteristics of the n-MOSFET in Fig. 4.3(a), which were measured at different instants of the digital and the analog breakdown, respectively. For example, at the instant of 500 s, the experiment was halted, and the post-breakdown I_g - V_g measurement was carried out, as shown in Fig. 4.3(b). Note that Figs. 4.3(b) and 4.3(c) include the fresh and the SILC-induced I_g - V_g characteristics, indicating the degradation of I_g before the occurrence of a dielectric breakdown event. It can be observed in Fig. 4.3(b) that the I_g - V_g characteristics in the digital breakdown did not gradually degrade with the evolution of the progressive

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breakdown. Conversely, for some of the cases, the post-breakdown I_g - V_g characteristics were partially recovered.

Figure 4.3. (a) Evolution of I_g for a breakdown n-MOSFET ($T_{ox} = 22$ Å and $L \times W = 1 \times 0.6 \mu m^2$) stressed using a one-cycle multiple-stage CVS in inversion mode at the room temperature. The TDDB of the n-MOSFET was carried out with $V_{gstress} = 4.1$ V and $I_{gl} = 1 \mu A$. The one-cycle multiple-stage CVS was performed with $V_{init} = 2.6$ V, $\Delta V = 0.1$ V, $t_{stress} = 500$ s and $V_{final} = V_{crit} = 3.4$ V. (b), (c) I_g - V_g characteristics at different instants of the digital and the analog breakdown, respectively, for the n-MOSFET.

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Furthermore, during the sweeping of V_g , I_g could randomly experience a sudden, abrupt increase or decrease, leading to the degradation or partial recovery of I_g . For instance, I_g for the deep blue line (i.e., at the instant of 3500 s) experienced a sudden, abrupt increase at $V_g = 1.3$ V, while I_g for the dark cyan line (i.e., at the instant of 2000 s) experienced a sudden, abrupt decrease at $V_g = 1.5$ V. The digital fluctuation of I_g could also be observed during the sweeping of V_g , as shown in I_g for the blue line (i.e., at the instant of 1500 s) at $V_g = 0.3$ - 0.5 V.

Comparing Fig. 4.3(b) with Fig. 4.3(c), the I_g - V_g characteristics in the digital and the analog breakdown are quite different from each other. The major difference is that the I_g - V_g characteristics in the analog breakdown steadily degrade to a higher leakage state when the progressive breakdown evolves. No recovery of I_g occurred. Additionally, the digital fluctuation of I_g during the sweeping of V_g could hardly be observed in the analog breakdown. The study of the physical mechanisms governing the behaviors of I_g in the analog breakdown will be given in *Chapter Five*.

Fig. 4.1 is universal for n-MOSFETs with ultrathin silicon oxynitride fabricated by different CMOS technology nodes and different manufacturers. Similar results can be seen for $T_{ox} = 16$ and 12.5 Å, as shown in Figs. 4.4(a) and 4.4(b), respectively. It is believed that the digital fluctuation of I_g in the digital breakdown is strongly related to the change in the physical properties of a percolation path formed within the gate oxide in the early stage of the progressive breakdown. A model based on the molecular structure of the percolation has been proposed to explain the physical mechanisms governing the behaviors of I_g in the digital breakdown, and this will be thoroughly discussed in the following section.

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(a)

(b)

Figure 4.4. Evolution of I_g for two breakdown n-MOSFETs: **(a)** $T_{ox} = 16$ Å and $L \times W = 0.5 \times 0.6$ μm^2 , and **(b)** $T_{ox} = 12.5$ Å and $L \times W = 0.04 \times 1$ μm^2 . The n-MOSFET in **(a)** and **(b)** were stressed using a two- and a three-cycle multiple-stage CVS in inversion mode at the room temperature, respectively. The stressing conditions used for the n-MOSFET in **(a)** and **(b)** are described in the boxes at the right of the corresponding figure.

The digital and the analog breakdown are universal phenomena that can be observed in n-MOSFETs with ultrathin gate oxide. In general, the progressive breakdown

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is mainly constituted by the digital and the analog breakdown, which are a low and a high conduction state, respectively. Based on our results, the analog breakdown is preceded by the digital breakdown, meaning that the digital breakdown will take place before the occurrence of the analog breakdown. Since the digital breakdown is dominant in the early stage of the progressive breakdown for which a n-MOSFET is still functioning; thus, the study of the digital breakdown is particularly important.

4.4 CRITICAL GATE VOLTAGE AND ITS IMPACTS TO EVOLUTION OF POST-BREAKDOWN I_G

As shown in Figs. 4.1, 4.4(a) and 4.4(b), in the 1st-cycle multiple-stage CVS, I_g for $T_{ox} = 22, 16$ and $12.5 \text{ \AA}$ exhibited an abrupt, rapid increase at $V_{gstress} \cong 3.4, 2$ and 2.4 V , respectively. Following this abrupt, rapid increase, the profile of I_g became relatively stable. The results imply that there exists a critical gate voltage, which is denoted as V_{crit} , to govern the transition of the digital breakdown into the analog breakdown. As shown in Fig. 4.1, it can be observed that the 3rd-cycle multiple-stage CVS remained in the analog breakdown after the digital breakdown evolved into the analog breakdown from the 1st-cycle multiple-stage CVS to the 2nd-cycle multiple-stage CVS at $V_{final}(1) = V_{crit} = 3.4 \text{ V}$. This means that the transition of the digital breakdown into the analog breakdown is irreversible.

4.4.1 DEPENDENCE OF V_{CRIT} ON GATE OXIDE THICKNESS

A statistical study of V_{crit} was carried out by repeating the experiments discussed in Figs. 4.1, 4.4(a) and 4.4(b). The purpose of this statistical study is to determine V_{crit} for a

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specific T_{ox} . Five different T_{ox} , which are 12.5, 16, 16.5, 20 and 22 Å, were involved in this statistical study. The sample size for each of the T_{ox} is given in Table 4.1. Through this statistical study, we found that V_{crit} for $T_{ox} = 12.5, 16, 16.5, 20$ and 22 Å are in the range of 2-2.4, 2-2.4, 2.2-2.6, 2.5-2.9 and 2.9-3.5 V, respectively. Table 4.1 summarizes V_{crit} for various T_{ox} . Note that the samples were provided by two different manufacturers (i.e., Manufacturers A and B).

Manufacturer	A	B	A	B	B
T_{ox}	12.5 Å	16 Å	16.5 Å	20 Å	22 Å
Number of Samples	14	37	14	24	56
V_{crit}	2 to 2.4 V	2 to 2.4 V	2.2 to 2.6 V	2.5 to 2.9 V	2.9 to 3.5 V

Table 4.1. V_{crit} for various T_{ox} , which include 12.5, 16, 16.5, 20 and 22 Å. Note that the samples were provided by two different manufacturers (i.e., Manufacturers A and B).

Knowing that V_{crit} for $T_{ox} = 16$ Å is in the range of 2-2.4 V, as shown in Table 4.1, an experiment was conducted to study the behaviors of I_g for $V_{gstress}$ did not exceed V_{crit} . This means that $V_{gstress}$ was kept smaller than 1.9 V. Fig. 4.5 shows a typical example for the evolution of I_g for a breakdown n-MOSFET ($T_{ox} = 16$ Å and $L \times W = 0.3 \times 0.6 \mu m^2$) stressed using an eight-cycle multiple-stage CVS in inversion mode at the room temperature. The n-MOSFET was initially stressed with $V_{gstress} = 3.3$ V and $I_{gl} = 10 \mu A$. Except for t_{stress} , the stressing conditions of each cycle of the multiple-stage CVS remained the same: $V_{init} = 1.2$ V, $\Delta V = 0.2$ V and $V_{final} = 1.8$ V. V_{final} was chosen to be 1.8 V such that the requirement of $V_{gstress}$ smaller than 1.9 V was met. t_{stress} for the 1st- to the 8th-cycle multiple-stage CVS were set to 100, 300, 500, 600, 700, 900, 1200 and 1600 s, respectively.

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Figure 4.5. Evolution of I_g for a breakdown n-MOSFET ($T_{ox} = 16 \text{ \AA}$ and $L \times W = 0.3 \times 0.6 \text{ \mu m}^2$), showing that the transition of the digital breakdown into the analog breakdown will not take place if $V_{gstress}$ is smaller than V_{crit} . Note that V_{crit} for $T_{ox} = 1.6 \text{ nm}$ was found to be in the range of 2-2.4 V, as shown in Table 4.1. The n-MOSFET was stressed using an eight-cycle multiple-stage CVS in inversion mode at the room temperature. The TDDB of the n-MOSFET was carried out with $V_{gstress} = 3.3 \text{ V}$ and $I_{gl} = 10 \text{ \mu A}$. The initial voltage, the voltage increment and the final voltage used in the eight-cycle multiple-stage CVS were the same, which were $V_{init} = 1.2 \text{ V}$, $\Delta V = 0.2 \text{ V}$ and $V_{final} = 1.8 \text{ V}$. Furthermore, $t_{stress}(1) = 100 \text{ s}$, $t_{stress}(2) = 300 \text{ s}$, $t_{stress}(3) = 500 \text{ s}$, $t_{stress}(4) = 600 \text{ s}$, $t_{stress}(5) = 700 \text{ s}$, $t_{stress}(6) = 900 \text{ s}$, $t_{stress}(7) = 1200 \text{ s}$ and $t_{stress}(8) = 1600 \text{ s}$.

As shown in Fig. 4.5, the digital fluctuation of I_g can consistently be seen irrespective to any cycle of the multiple-stage CVS. I_g did not evolve into a relatively stable leakage state, as long as $V_{gstress}$ did not exceed V_{crit} . Similar results can also be observed in Fig. 4.4(b). In brief, the transition of the digital breakdown into the analog breakdown could rarely occur if $V_{gstress}$ is smaller than V_{crit} . Conversely, the digital breakdown will rapidly evolve into the analog breakdown when $V_{gstress}$ is equal to or larger than V_{crit} . Note that the

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transition of the digital breakdown into the analog breakdown is irreversible, as shown in Fig. 4.1.

Figure 4.6. V_{crit} versus T_{ox} relationship. A saturation of V_{crit} at 2-2.4 V implies that the extra advantage provided by the digital breakdown in extending the post-breakdown reliability margin still exists at T_{ox} below 1.6 nm. The red and the black color refer to the n-MOSFETs fabricated by Manufacturers A and B, respectively.

Based on the results in Table 4.1, the V_{crit} versus T_{ox} relationship is shown in Fig. 4.6. V_{op} with various T_{ox} , which are obtained from ITRS and some of the published data, are also plotted. The red and the black color refer to the n-MOSFETs fabricated by Manufacturers A and B, respectively. As mentioned above, if V_{crit} is much larger than V_{op} , the transition of the digital breakdown into the analog breakdown can hardly occur during the normal device operations. This means that the post-breakdown reliability margin can largely be extended. It can be noticed from Fig. 4.6 that for T_{ox} larger than 1.6 nm, V_{crit}

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steadily decreases with decreasing T_{ox} . This leads to a major post-breakdown reliability concern. It is initially predicted that at a lower T_{ox} where V_{crit} is equal to V_{op} , the digital breakdown will vanish upon the occurrence of a dielectric breakdown event, and I_g will spontaneously evolve into a stable high leakage state. If V_{op} is larger than V_{crit} , the progressive breakdown could totally vanish, and a device may immediately experience a catastrophic breakdown once a dielectric breakdown event is triggered to occur. However, as shown in Fig. 4.6, for T_{ox} smaller than 1.6 nm, a saturation of V_{crit} at 2-2.4 V can be observed. The difference between V_{op} and V_{crit} remains constant at 0.9-1.4 V. This implies that the shrinkage of the progressive breakdown due to the absence of the digital breakdown will not occur when T_{ox} is continuously scaled below 1.6 nm. In summary, the role of the digital breakdown in prolonging the progressive breakdown at a low V_g has been extended to standard sub-65-nm CMOS technology employing T_{ox} below 1.6 nm.

4.4.2 OVERESTIMATION OF POST-BREAKDOWN I_g DEGRADATION RATE AT NOMINAL OPERATING VOLTAGES

Fig. 4.7 shows the degradation rate of I_g (dI_g/dt) at various $V_{gstress}$ for about thirty n-MOSFETs ($T_{ox} = 12.5 \text{ \AA}$ and $L \times W = 0.04 \times 1 \text{ \mu m}^2$) stressed in inversion mode at the room temperature. The samples in Fig. 4.7 are categorized into three major types:

- Circles – The samples involving only the analog breakdown;
- Triangles – The samples involving the digital and the analog breakdown, and;
- Squares – The samples involving only the digital breakdown.

Six of the samples, which are denoted as A, B, C, D, E and F (i.e., the filled symbols in Fig. 4.7), will be discussed in details.

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Figure 4.7. dI_g/dt at various $V_{gstress}$ for about thirty breakdown n-MOSFETs ($T_{ox} = 12.5$ Å and $L \times W = 0.04 \times 1 \mu m^2$) stressed in inversion mode at the room temperature. The filled symbols (i.e., Samples A, B, C, D, E and F) will be discussed in details. Sample A was stressed with $V_{gstress} = 2.6$ V and $I_{gl} = 100 \mu A$. Samples B, C, D, E and F were stressed using a two-stage CVS. In the 1st-stage CVS, $V_{gstress} = 2.6$ V and $I_{gl} = 5 \mu A$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to a value smaller than 2.6 V with $I_{gl} = 100 \mu A$. For all the samples involving only the digital breakdown (i.e., the squares), the gate oxide stressing could be further continued as I_g was still in the digital breakdown and had not yet reached $I_{gl} = 100 \mu A$. Y_{ANA} is a fitting line obtained from dI_g/dt for samples that only involve the analog breakdown. Additionally, Y_{upp} and Y_{low} are the upper and the lower bound of dI_g/dt for samples that involve only the analog breakdown, respectively.

dI_g/dt , which defines the degradation rate of I_g during the progressive breakdown [125-127], can be generally described as

$$\frac{dI_g}{dt} = \frac{I_{g2} - I_{g1}}{t_2 - t_1}. \tag{4.2}$$

(t_1, I_{g1}) and (t_2, I_{g2}) are the initial and the final point of the progressive breakdown. At $V_{gstress} = 2.6$ V, the n-MOSFETs (including Sample A) were stressed until a dielectric

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breakdown event occurred and I_g reached $I_{gl} = 100 \mu\text{A}$. A typical example is shown in Fig. 4.8, which is the evolution of I_g for Sample A. It can be noticed that I_g degraded from $I_{gl} = 5 \mu\text{A}$ to $I_{g2} = 100 \mu\text{A}$ within $\sim 2.25 \text{ s}$ (i.e., $t_2 - t_1$ in Eqn. (4.2)), and hence, dI_g/dt for Sample A can be calculated as $4.22 \times 10^{-5} \text{ A/s}$.

Figure 4.8. (a) Evolution of I_g for Sample A, which was stressed with $V_{gstress} = 2.6 \text{ V}$ and $I_{gl} = 100 \mu\text{A}$. (b) Enlarged view of the profile of I_g for Sample A after 464 s. I_g degraded from $I_{gl} = 5 \mu\text{A}$ to $I_{g2} = 100 \mu\text{A}$ within $\sim 2.25 \text{ s}$, and thus, dI_g/dt for Sample A is calculated as $4.22 \times 10^{-5} \text{ A/s}$. Note that $V_{gstress}$ is larger than V_{crit} .

On the other hand, the data of dI_g/dt at $V_{gstress}$ smaller than 2.6 V (including Samples B, C, D, E and F) was collected using a two-stage CVS in inversion mode at the room temperature [127]. In the 1st-stage CVS, $V_{gstress} = 2.6 \text{ V}$ and $I_{gl} = 5 \mu\text{A}$ were used. Assume that the physical origins of defects initially created within the gate oxide by $V_{gstress} = 2.6 \text{ V}$ and $I_{gl} = 5 \mu\text{A}$ are similar for all the breakdown n-MOSFETs. In the 2nd-stage CVS, $V_{gstress}$ was reduced to a value lower than 2.6 V with $I_{gl} = 100 \mu\text{A}$. Fig. 4.9(a) shows the evolution of I_g in the 1st-stage CVS for Samples B, C and D. Moreover, Figs. 4.9(b), 4.9(c) and 4.9(d) show the evolution of I_g in the 2nd-stage CVS for Samples B, C and D, respectively, where $V_{gstress} = 2.3 \text{ V}$. I_g at the first instant of the 2nd-stage CVS is defined as

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I_{g1} . By setting $I_{g2} = 100 \mu\text{A}$, the calculation of dI_g/dt for the samples at $V_{gstress}$ below 2.6 V can be carried out.

Figure 4.9. (a) Evolution of I_g in the 1st-stage CVS for Samples B, C and D. (b), (c), (d) Evolution of I_g in the 2nd-stage CVS for Samples B, C and D, respectively. In the 1st-stage CVS, $V_{gstress} = 2.6 \text{ V}$ and $I_{gl} = 5 \mu\text{A}$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 2.3 V with $I_{gl} = 100 \mu\text{A}$. dI_g/dt for Samples B, C and D are calculated as 2.15×10^{-6} , 1.66×10^{-7} and $2.92 \times 10^{-8} \text{ A/s}$, respectively. Note that $V_{gstress}$ is larger than or nearly equal to V_{crit} .

In general, dI_g/dt in Fig. 4.7 can be divided into three distinct categories, namely, Categories I, II and III.

- Category I ($V_{gstress} > 2.4 \text{ V}$):

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This category can be found at $V_{gstress}$ larger than V_{crit} . It is constituted by the samples involving only the analog breakdown (i.e., the circles in Fig. 4.7, including Sample A). As discussed above, I_g will rapidly evolve into the analog breakdown if $V_{gstress}$ is larger than V_{crit} . According to Table 4.1, V_{crit} for $T_{ox} = 12.5 \text{ \AA}$ is in the range of 2-2.4 V. Since $V_{gstress} = 2.6 \text{ V}$ is larger than $V_{crit} = 2\text{-}2.4 \text{ V}$, no digital breakdown can be observed in Fig. 4.8. The spread of dI_g/dt at $V_{gstress} = 2.6 \text{ V}$, as shown in Fig. 4.7, is mainly controlled by s_{BD} [127]. The calculation of s_{BD} is provided in *Chapter Three*. dI_g/dt is larger for s_{BD} closer to 0 or 1L, but is smaller for s_{BD} closer to 0.5L [127]. Hence, the calculation of dI_g/dt involves only the analog breakdown. If t_{ANA} is the period of the analog breakdown, then $t_2 - t_1 = t_{ANA}$. We can rewrite Eqn. (4.2) as

$$\frac{dI_g}{dt} = \frac{I_{g2} - I_{g1}}{t_{ANA}}. \quad (4.3)$$

- Category II ($2 \text{ V} \leq V_{gstress} \leq 2.4 \text{ V}$):

This category can be found at $V_{gstress}$ nearly equal to V_{crit} . It is constituted by the samples with the different combinations of the digital and the analog breakdown. Essentially, there are three major cases in this category:

Case A: Samples involving only the analog breakdown (i.e., the circles in Fig. 4.7, including Sample B).

This case is similar to Category I. Fig. 4.9(b) shows a typical example for which I_g quickly evolved from the digital breakdown into the analog breakdown, where V_{crit} is believed smaller than $V_{gstress} = 2.3 \text{ V}$. Based on Eqn. 4.3, dI_g/dt for Sample B can be calculated as $2.15 \times 10^{-6} \text{ A/s}$. Together with the samples in Category I, a steady decreasing trend of dI_g/dt with decreasing $V_{gstress}$ can be observed. This is in well agreement with the results reported in Refs. [125-127].

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Figure 4.10. Evolution of I_g in the 2nd-stage for Samples (a) E and (b) F. In the 1st-stage CVS, $V_{gstress} = 2.6$ V and $I_{gl} = 5$ μ A were used. In the 2nd-stage CVS, Sample E was stressed with $V_{gstress} = 2.2$ V, while Sample F was stressed with $V_{gstress} = 2$ V, where $I_{gl} = 100$ μ A. The gate oxide stressing in (a) and (b) could be further continued, while I_g was still in the digital breakdown and had not yet reached $I_{gl} = 100$ A. dI_g/dt for Samples E and F are calculated as 1.14×10^{-8} and 2.45×10^{-9} A/s, respectively. It is believed that $V_{gstress}$ is slightly smaller than V_{crit} . (c), (d) Enlarged view of some of the portions in (a) and (b), respectively, indicating the digital fluctuation of I_g .

Case B: Samples involving the digital and the analog breakdown (i.e., the triangles in Fig. 4.7, including Samples C and D).

It can be noticed that dI_g/dt in this case is much lower than those in Case A. As shown in Figs. 4.9(c) and 4.9(d), the digital breakdown is very apparent. Before quickly

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evolving into the analog breakdown, I_g remained in the digital breakdown for a certain period of time. This means that $t_2 - t_1 = t_{DIG} + t_{ANA}$, where t_{DIG} is the period of the digital breakdown. Thus, we can rewrite Eqn. (4.2) as

$$\frac{dI_g}{dt} = \frac{I_{g2} - I_{g1}}{t_{DIG} + t_{ANA}}. \quad (4.4)$$

Based on Eqn. (4.4), dI_g/dt for Samples C and D can be calculated as 1.66×10^{-7} and 2.92×10^{-8} A/s, respectively. In the analog breakdown for which only t_{ANA} is included for the calculation, dI_g/dt for Samples C and D are estimated to be 2.82×10^{-6} and 2.62×10^{-7} A/s, respectively, using Eqn. (4.3). Note that 2.82×10^{-6} and 2.62×10^{-7} A/s fall within a region formed by Case A at $V_{gstress} = 2.3$ V. As a result, the presence of the digital breakdown will lead to a lowering of dI_g/dt in Case A. Obviously, the lowering of dI_g/dt in Case A will be more apparent at a lower $V_{gstress}$.

Case C: Samples involving only the digital breakdown (i.e., the squares in Fig. 4.7, including Samples E and F).

For all the samples in this case, the gate oxide stressing could be further continued as I_g was still in the digital breakdown and had not yet reached $I_{gl} = 100$ A. It is believed that the transition of the digital breakdown into the analog breakdown could eventually be triggered as $V_{gstress}$ and V_{crit} are close with each other. The evolution of I_g in the 2nd-stage CVS for Sample E is shown in Fig. 4.10(a), where $V_{gstress} = 2.2$ V. I_g digitally fluctuated with a random trend, and the transition of the digital breakdown into the analog breakdown did not take place yet. Thus, the calculation of dI_g/dt is not straightforward. The first step is to estimate t_{ANA} by constructing Y_{ANA} , which is a fitting line of dI_g/dt for the samples involving only the analog breakdown. According

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to Y_{ANA} , we can define Y_{upp} and Y_{low} , which are the upper and the lower bound of dI_g/dt for the samples involving only the analog breakdown, respectively. Y_{ANA} , Y_{upp} and Y_{low} are parallel with each other. As shown in Fig. 4.7, at $V_{gstress} = 2.2$ V, $Y_{upp} = \sim 1 \times 10^{-6}$ A/s and $Y_{low} = \sim 7 \times 10^{-8}$ A/s can be obtained. Assume that I_g for Sample E immediately enters into the analog breakdown after 8000 s. Then, we define I_g at the last instant of Sample E as I_{g1} ($\cong 9.42 \times 10^{-7}$ A), and I_{g2} is set to 100 μ A. According to Eqn. (4.3), t_{ANA} required for $Y_{upp} = \sim 1 \times 10^{-6}$ A/s and $Y_{low} = \sim 7 \times 10^{-8}$ A/s are

$$t_{upp} = \frac{I_{g2} - I_{g1}}{Y_{upp}} = \frac{1 \times 10^{-4} - 9.42 \times 10^{-7}}{1 \times 10^{-6}} \cong 100s$$

and

$$t_{low} = \frac{I_{g2} - I_{g1}}{Y_{low}} = \frac{1 \times 10^{-4} - 9.42 \times 10^{-7}}{7 \times 10^{-8}} \cong 1415s,$$

respectively. Knowing that t_{DIG} for Sample E is 8000 s and defining I_g at the initial instant of Sample E as I_{g1} ($\cong 1.09 \times 10^{-6}$ A), we can approximate dI_g/dt for Sample E based on Eqn. (4.4) as

$$\begin{aligned} \frac{dI_g}{dt} &= \frac{\left(\frac{I_{g2} - I_{g1}}{t_{DIG} + t_{upp}} \right) + \left(\frac{I_{g2} - I_{g1}}{t_{DIG} + t_{low}} \right)}{2} = \frac{\frac{1 \times 10^{-4} - 1.09 \times 10^{-6}}{8000 + 100} + \frac{1 \times 10^{-4} - 1.09 \times 10^{-6}}{8000 + 1415}}{2} \\ &\cong 1.14 \times 10^{-8} \text{ A/s}. \end{aligned}$$

For the digital breakdown has not yet evolved into the analog breakdown, this method allows a prediction on the lowering of dI_g/dt in Case A at a specific $V_{gstress}$ due to the presence of t_{DIG} . It is clear that $dI_g/dt \cong 1.14 \times 10^{-8}$ A/s is a very conservative prediction (i.e., the upper estimation of actual expected dI_g/dt), as explained in Fig. 4.11(a). We believe that Sample E is a case for which $V_{gstress}$ ($= 2.2$ V) is slightly

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smaller than V_{crit} ($= 2.3$ or 2.4 V for example). Therefore, it is expected that I_g would continuously remain in the digital breakdown for a specific period of time before entering into the analog breakdown. This leads to an extension of t_{DIG} , which in turn causes a more significant lowering of dI_g/dt in Category I. Fig. 4.10(b) shows the evolution of I_g in the 2nd-stage CVS for Sample F, where $V_{gstress} = 2$ V. Similar to Sample E, dI_g/dt for Sample F can be calculated as 2.45×10^{-9} A/s. Figs. 4.10(c) and 4.10(d) show an enlarged view of some of the portions in Figs. 4.10(a) and 4.10(b), respectively, indicating the digital fluctuation of I_g .

- Category III ($V_{gstress} < 2$ V):

This category can be found at $V_{gstress}$ smaller than V_{crit} . It is constituted by the samples involving only the digital breakdown (i.e., the squares in Fig. 4.7). Different from the Case C of Category II, the transition of the digital breakdown into the analog breakdown could hardly take place. The calculation of dI_g/dt for this case is even more complicated as I_g will only digitally fluctuated within a specific range and will not enter into the analog breakdown. We define I_{gmax} and I_{gmin} as a maximum and a minimum value for the digital fluctuation range of I_g . Assume that $I_{g2} - I_{g1} = I_{gmax} - I_{gmin}$. t_{ANA} can be discarded. Hence, dI_g/dt can be estimated as

$$\frac{dI_g}{dt} = \frac{I_{gmax} - I_{gmin}}{t_{DIG}} \quad (4.5)$$

In most of the cases, $I_{g2} - I_{g1}$ is smaller than $I_{gmax} - I_{gmin}$, as shown in Figs. 4.10(a) and 4.10(b). Moreover, t_{DIG} could be extremely large as the gate oxide could be continuously stressed, in which I_g will remain in the digital breakdown. As shown in Fig. I in Appendix A, a breakdown n-MOSFET ($T_{ox} = 12.5$ Å and $L \times W = 0.04 \times 1$

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μm^2) was stressed with $V_{gstress} = 1.8\text{ V}$ for more than 120000 s (i.e., about 1.4 days), while I_g still remained in the digital breakdown without experiencing any apparent net increase. All these factors imply that dI_g/dt based on Eqn. (4.5) is a very conservative prediction, as explained in Fig. 4.11(b). dI_g/dt could be equal to zero when I_g experiences a partial “recovery” due to the switching off of some of the defects in the vicinity of a percolation path. This will be discussed in details in the later section. As shown in Fig. 4.7, at $V_{gstress}$ below 2 V, no data falls within the decreasing trend of dI_g/dt in Category I and the Case A of Category II, which is a region between Y_{upp} and Y_{low} . A much lower dI_g/dt can be observed, implying that the digital breakdown is dominant at a low $V_{gstress}$.

Category II is a mixing mode for Categories I and III. Table 4.2 provides a summary on formulae used to calculate or estimate dI_g/dt in Categories I, II and III.

Case(s)	Formula(e)
Analog Breakdown (Category I, Case A of Category II)	$\frac{dI_g}{dt} = \frac{I_{g2} - I_{g1}}{t_{ANA}}$
Digital and Analog Breakdown (Case B of Category II)	$\frac{dI_g}{dt} = \frac{I_{g2} - I_{g1}}{t_{DIG} + t_{ANA}}$
Digital Breakdown (Case C of Category II)	$t_{upp} = \frac{I_{g2} - I_{g1}}{Y_{upp}}$ $t_{low} = \frac{I_{g2} - I_{g1}}{Y_{low}}$ $\frac{dI_g}{dt} = \frac{\left(\frac{I_{g2} - I_{g1}}{t_{DIG} + t_{upp}}\right) + \left(\frac{I_{g2} - I_{g1}}{t_{DIG} + t_{low}}\right)}{2}$
Digital Breakdown (Category III)	$\frac{dI_g}{dt} = \frac{I_{g\max} - I_{g\min}}{t_{DIG}}$

Table 4.2. Formulae used to perform the calculation or estimation of dI_g/dt in Categories I, II and III.

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According to our results, it is expected that I_g will remain in the digital breakdown and could hardly evolve into the analog breakdown at V_{op} , which is much smaller than V_{crit} , as shown in Fig. 4.6. This will result in a significant impact on the extrapolation of dI_g/dt from a high $V_{gstress}$ to V_{op} .

Figure 4.11. General schematic describing a conservative prediction of dI_g/dt in the Cases (a) A and (b) B of Category III. (c) General schematic of an overestimation of dI_g/dt at V_{op} , which is extrapolated from the accelerated stressing conditions with $V_{gstress}$ larger than V_{crit} .

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During the normal device operations, t_{DIG} can be extremely large (e.g., Fig. I in Appendix A). Therefore, dI_g/dt at V_{op} will be significantly overestimated if it is extrapolated from the accelerated stressing conditions with $V_{gstress}$ larger than V_{crit} . Consequently, this would yield an overly pessimistic lifetime prediction of gate oxide. Fig. 4.11(c) shows a general schematic of an overestimation of dI_g/dt at V_{op} , which is extrapolated from the accelerated stressing conditions with $V_{gstress}$ larger than V_{crit} . All the currently reported data [125-127] was collected in the region of $V_{gstress}$ larger than or nearly equal to V_{crit} . This means that the reliability projection of nanoscale CMOS devices with ultrathin gate oxide must be carefully revised.

By extrapolation, Y_{ANA} at $V_{op} = 1$ V can be estimated as 6.24×10^{-14} A/s. Hence, for a n-MOSFET with the analog breakdown, I_g will degrade with about 1.97×10^{-6} A per year during the normal device operations. Our prediction is in the same range with the results reported in Refs. [125, 126]. We know that a dielectric breakdown event initially created at $V_{gstress} = 2.6$ V and $I_{gl} = 5$ μ A corresponds to I_g in the digital breakdown. Since V_{op} is much smaller than V_{crit} , I_g could hardly evolve from the digital breakdown into the analog breakdown. Now, we assume that the presence of t_{DIG} can cause a lowering of Y_{ANA} for about one order of magnitude at $V_{op} = 1$ V, as shown in most of the cases at $V_{gstress}$ below V_{crit} in Fig. 4.7. During the normal device operations, I_g will degrade with about 1.97×10^{-7} A per year, which requires about 50 years to reach the device failure criterion of 10 μ A specified for conventional static random-access memory devices. Again, the prediction is very conservative. This suggests that due to the presence of an extremely long t_{DIG} at V_{op} much smaller than V_{crit} , the ultrathin gate oxide is in fact associated with an excellent post-breakdown lifetime.

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4.4.3 EFFECTS OF STRESSING DURATION, BREAKDOWN LOCATION AND
DEVICE DIMENSIONS ON V_{crit}

Fig. 4.12 shows the evolution of I_g with various t_{stress} for three breakdown n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \text{ \mu m}^2$) stressed using a one-cycle multiple-stage CVS in inversion mode at the room temperature. The n-MOSFETs were initially stressed with $V_{gstress} = 4 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$. The stressing conditions of the one-stage multiple-stage CVS were $V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 100\text{-}500 \text{ s}$ and $V_{final} = V_{crit} = 3.3\text{-}3.4 \text{ V}$.

Figure 4.12. Evolution of I_g with various t_{stress} for three breakdown n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \text{ \mu m}^2$) stressed using a one-cycle multiple-stage CVS in inversion mode at the room temperature. The TDDB of these n-MOSFETs was carried out with $V_{gstress} = 4 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$. The one-cycle multiple-stage CVS was performed with $V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 100\text{-}500 \text{ s}$ and $V_{final} = V_{crit} = 3.3\text{-}3.4 \text{ V}$. S1, S2 and S3 refer to the breakdown n-MOSFETs stressed with $t_{stress} = 100, 300$ and 500 s , respectively.

s_{BD} for the n-MOSFETs were $0.54\text{-}0.61L$, meaning that the percolation path in each n-MOSFET was located at the center of the device channel. The n-MOSFETs with nearly

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the same s_{BD} were chosen such that the effects of s_{BD} on V_{crit} can be neglected. V_{crit} was found to be 3.3-3.4 V. The results in Fig. 4.12 suggest that V_{crit} is independent on t_{stress} . This implies that t_{stress} plays an insignificant role in triggering the transition of the digital breakdown into the analog breakdown. In order to confirm that V_{crit} is independent on t_{stress} , about thirty breakdown n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \text{ \mu m}^2$) were further stressed, as shown in Fig. 4.13. The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 4.12.

Figure 4.13. Independence of V_{crit} on t_{stress} , which varied from 100 s to 2000 s. The sample size was about thirty breakdown n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \text{ \mu m}^2$). The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 4.12.

It can be observed that the independence of V_{crit} on t_{stress} is still valid even for a longer t_{stress} , such as 2000 s. V_{crit} remained nearly unchanged in the range of 2.9-3.5 V, and it did not exhibit any particular trend when t_{stress} was varied from 100 s to 2000 s, signifying that V_{crit} is independent on t_{stress} . Again, this means that assessment on the lifetime of gate oxide at V_g above V_{crit} is different from that at V_g below V_{crit} .

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Figure 4.14. Independence of V_{crit} on s_{BD} , which was controlled from 0L to 1L. The device dimensions of these n-MOSFETs are the same (i.e., $T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \mu\text{m}^2$). The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 4.12.

Similar statistical studies on the relationship between V_{crit} and other important parameters were carried out. These parameters include the breakdown location (i.e., s_{BD}), the channel length (i.e., L) and the channel width (i.e., W). Note that the stressing conditions applied to the n-MOSFETs involved in these statistical studies were similar to those in Fig. 4.12. V_{crit} associated with various s_{BD} for fifteen breakdown n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \mu\text{m}^2$) are shown in Fig. 4.14. It can be noticed that V_{crit} was irregularly scattered in the range of 2.9-3.5 V from $s_{BD} = 0L$ to $s_{BD} = 1L$, implying that the location of a percolation path along the device channel has the minimum effects on V_{crit} . Furthermore, Figs. 4.15(a) and 4.15(b) show that V_{crit} is independent on L and W , respectively. The n-MOSFETs in Fig. 4.15 have the same T_{ox} (i.e., $22 \text{ \AA}$). As shown in Fig. 4.15(a), with the fixed W of $0.3 \mu\text{m}$ but L varying from $0.3 \mu\text{m}$ to $1 \mu\text{m}$, no specific relationship between V_{crit} and L can be found. Similar results can be observed in Fig.

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4.15(b). With the fixed L of $1\text{ }\mu\text{m}$ but W varying from $0.3\text{ }\mu\text{m}$ to $1.2\text{ }\mu\text{m}$, V_{crit} and W are found to be independent with each other. Again, it can be observed that V_{crit} was consistently in the range of $2.9\text{--}3.5\text{ V}$. In summary, except for T_{ox} , the effects of external factors, which include t_{stress} , s_{BD} , L and W , on V_{crit} are very insignificant. Indirectly, this means that V_{crit} could just be governed by the physical structures and the intrinsic properties of the percolation path.

Figure 4.15. Independence of V_{crit} on (a) L and (b) W . These n-MOSFETs possess the same T_{ox} (i.e., $22\text{ }\text{\AA}$). In (a), W is fixed at $0.3\text{ }\mu\text{m}$, while L varies from $0.3\text{ }\mu\text{m}$ to $1\text{ }\mu\text{m}$. In (b), L is fixed at $1\text{ }\mu\text{m}$, while W varies from $0.3\text{ }\mu\text{m}$ to $1.2\text{ }\mu\text{m}$. The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 4.12.

4.4.4 V_{crit} AND MAGNITUDE OF POST-BREAKDOWN I_g IN GOVERNING
TRANSITION OF DIGITAL BREAKDOWN INTO ANALOG BREAKDOWN

In the previous section, it has been found that V_{crit} serves as one of the vital factors in limiting the evolution of I_g from the digital breakdown into the analog breakdown. Now, we study the relationship between the magnitude of I_g and the transition of the digital breakdown into the analog breakdown.

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Figure 4.16. Evolution of I_g from the digital breakdown into the analog breakdown for a n-MOSFET ($T_{ox} = 12.5 \text{ \AA}$ and $L \times W = 0.04 \times 1 \text{ \mu m}^2$) with increasing I_{gl} . The n-MOSFET was initially stressed with $V_{gstress} = 2.6 \text{ V}$ and $I_{gl} = 5 \text{ \mu A}$. The behaviors of I_g were investigated under a low $V_{gstress}$ of 1.6 V for $t_{stress} = 500 \text{ s}$. The gradual degradation of I_g was carried out under a higher $V_{gstress}$ of 2.6 V by progressively setting I_{gl} to a higher value.

Fig. 4.16 shows the evolution of I_g from the digital breakdown into the analog breakdown for a n-MOSFET ($T_{ox} = 12.5 \text{ \AA}$ and $L \times W = 0.04 \times 1 \text{ \mu m}^2$) with increasing I_{gl} . The increase of I_{gl} represented the growth of the progressive breakdown. This means that I_{gl} indicated one particular instant of the progressive breakdown. The n-MOSFET was initially stressed with $V_{gstress} = 2.6 \text{ V}$ and $I_{gl} = 5 \text{ \mu A}$. After the occurrence of a dielectric breakdown event, the behaviors of I_g captured at $I_{gl} = 5 \text{ \mu A}$ were investigated under a low $V_{gstress}$ of 1.6 V for $t_{stress} = 500 \text{ s}$. $V_{gstress} = 1.6 \text{ V}$, which was much lower than $V_{crit} = 2\text{-}2.4 \text{ V}$ for $T_{ox} = 12.5 \text{ \AA}$, was chosen such that the further degradation of I_g would hardly take place. Subsequently, the n-MOSFET was stressed with a higher $V_{gstress}$ of 2.6 V and a

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higher I_{gl} of 10 μA . $V_{gstress}$ higher than V_{crit} for $T_{ox} = 12.5 \text{ \AA}$ was chosen such that I_g could be further degraded from 5 μA to 10 μA . This allowed the progressive breakdown to evolve into a higher leakage state. Again, in order to investigate whether I_g captured at $I_{gl} = 10 \mu\text{A}$ exhibited digital or analog behaviors, $V_{gstress} = 1.6 \text{ V}$ and $t_{stress} = 500 \text{ s}$ were used. Similar procedure was repeated by progressively increasing I_{gl} but keeping other stressing conditions unchanged. The flowchart describing the implementation of the above experiment is shown in Fig. 4.17.

Figure 4.17. Flowchart describing the implementation of the experiment used to study the relationship between the magnitude of I_g and the transition of the digital breakdown into the analog breakdown.

As shown in Fig. 4.16, for I_{gl} lower than 45 μA , the digital fluctuation of I_g could still be observed. Conversely, I_g started to enter into the analog breakdown for I_{gl} higher than 45 μA . In general, the digital profile of I_g was gradually suppressed with increasing I_{gl} . At this level, we propose that I_g is constituted by two components, which are

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$$I_g = I_{DIG} + I_{ANA} \tag{4.6}$$

I_{DIG} defines the “digitally” fluctuated I_g flowing through a percolation path associated with the physical structure in Fig. 4.18(a). Upon the occurrence of a dielectric breakdown event, it is believed that the percolation path only involves a few effective electronic traps that are sufficient to allow the hopping of the electrons from the cathode to the anode, where some of the portions of the percolation path are still non-defective, as shown in Fig. 4.18(a). The digital fluctuation of I_g is attributed to the transformation of defects in the vicinity of the percolation path, which will be thoroughly discussed in the following section. I_{ANA} defines the relatively stable I_g flowing through a percolation path associated with the physical structure in Fig. 4.18(b).

Figure 4.18. Physical structure of a percolation path in (a) the digital and (b) the analog breakdown. In the digital breakdown, the percolation path only involves a few electronic traps that are sufficient to allow the hopping of the electrons from the cathode to the anode, where some of the portions of the percolation path are still non-defective. On the contrary, in the analog breakdown, the percolation path is proposed to possess a silicon-like conductive channel at the core.

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We propose that a percolation path will eventually become a silicon-like conductive channel in the analog breakdown, and the detailed discussion will be provided in *Chapter Five*. There are two cases:

- $V_{gstress}$ smaller than V_{crit} :

The digital breakdown prevails in the early stage of the progressive breakdown, and hence, I_g is nearly equal to I_{DIG} . As shown in Fig. 4.5, I_g can hardly evolve into a high conduction state if $V_{gstress}$ does not exceed V_{crit} . This implies that the percolation path will not be easily worn-out at a low V_g . We believe that the percolation path will be further worn-out with the creation of more defects in the vicinity of the percolation path after a long period of stressing time [109, 114, 115], leading to a gradual increase in I_g , as shown in Fig. 4.18(a). Note that I_g still remains in the digital breakdown. With the flow of a higher I_g through the percolation path, the wear out of the percolation path can be enhanced. This in turns leads to the increase in I_g . The local temperature in the vicinity of the percolation path could be high when a huge amount of I_g flows through a very narrow conductive channel [109, 110, 114]. As a result, this could transform some of the defective areas in the percolation path into a relatively stable silicon-like structure, which contributes to I_{ANA} later. Note that the defective areas in the percolation path refer to unstable broken silicon bonds left by the kicking-out of oxygen atoms during the progressive breakdown (*Section 4.6*). During the gradual growth of the percolation path from the physical structure in Fig 4.18(a) into Fig. 4.18(b), I_{ANA} starts to increase but I_{DIG} remains unchanged, and thus, I_g is the combined effects of I_{DIG} and I_{ANA} . When the percolation path possesses the physical structure in Fig. 4.18(b), I_{ANA} dominates over I_{DIG} , leading to a relatively stable I_g with

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a noisy profile. In this case, the analog breakdown prevails. However, this may take a very long period of time to occur.

Figure 4.19. $I_g @ V_g = 1 \text{ V}$ at different stages of the progressive breakdown for the n-MOSFET in Fig. 4.16. The digital breakdown is found at I_{gl} smaller than $45 \text{ } \mu\text{A}$, while the analog breakdown is found at I_{gl} larger than $45 \text{ } \mu\text{A}$. The dotted box shows a region for which the n-MOSFET in Fig. 4.16 was still functioning, where $I_g @ V_g = 1 \text{ V}$ did not exceed $1 \text{ } \mu\text{A}$ (i.e., the yellow region). Note that a n-MOSFET will be considered as a failed device if $I_g @ V_g = 1 \text{ V}$ exceeds $1 \text{ } \mu\text{A}$.

- $V_{gstress}$ larger than V_{crit} :

When the digital breakdown prevails in the early stage of the progressive breakdown, I_g is nearly equal to I_{DIG} . Based on our results, I_g will quickly evolve into a high conduction state if $V_{gstress}$ exceeds V_{crit} . The percolation path will be rapidly worn-out at a high V_g as more defects can be easily created in the vicinity of the percolation path. This will lead to the increase in I_g , while I_g still remains in the digital breakdown, as shown in Fig. 4.18(a). If I_g is limited at a low I_{gl} , the local temperature in the vicinity

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of the percolation path may be insufficient to transform the defective areas in the percolation path into a relatively stable silicon-like structure. This means that the transition of the digital breakdown into the analog breakdown is limited by I_{gl} . By setting I_{gl} to a higher value, some of the defective areas in the percolation path could be transformed into the silicon-like structure, causing I_{ANA} to increase but I_{DIG} to remain unchanged, as shown in Fig. 4.18(b). Finally, I_g will enter into the analog breakdown.

In summary, it is believed that V_{crit} serves as a factor in rapidly wearing out the percolation path such that a sufficiently huge amount of I_g can be generated. For $V_{gstress}$ smaller than V_{crit} , the percolation path could not be easily worn out. Since I_g is small, the digital breakdown could hardly evolve into the analog breakdown. For $V_{gstress}$ larger than V_{crit} , the percolation path will easily be worn out, allowing more I_g to flow through the percolation path, as shown in Fig. 4.18(b). However, if I_g is limited, the local temperature in the vicinity of the percolation path may be insufficient to transform the percolation path into a silicon-like structure. As a result, the transition of the digital breakdown into the analog breakdown will not occur.

Fig. 4.19 shows $I_g @ V_g = 1$ V at different stages of the progressive breakdown for the n-MOSFET in Fig. 4.16. Assume that the device failure criterion is $I_g = 1$ μ A at $V_g = 1$ V. The dotted box in Fig. 4.19 shows data points below 1 μ A. It can be observed that the n-MOSFET in Fig. 4.16 was still functioning for I_{gl} lower than 25 μ A. Note that $I_{gl} = 25$ μ A corresponds to the digital breakdown, which can be identified by the digital fluctuation of I_g at $V_{gstress} = 1.6$ V, as shown in Fig. 4.16. This implies that the digital breakdown plays the most important role in providing an extra post-breakdown reliability

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margin. The occurrence of a dielectric breakdown event will not directly lead to the total malfunctioning of a n-MOSFET if I_g can be limited at a low level for which the digital breakdown is dominant. Under the accelerated stressing conditions, $V_{gstress}$ is normally larger than V_{crit} , and thus, I_g will often rapidly increase to a high level. Therefore, the role of the digital breakdown in prolonging the progressive breakdown is very insignificant at a high $V_{gstress}$. On the contrary, during the normal device operations for which V_{op} is much smaller than V_{crit} , I_g will remain in the digital breakdown for a considerably long period of time, and this can significantly enhance the lifetime of gate oxide.

4.5 1/F-LIKE NOISE STUDY OF POST-BREAKDOWN I_g IN DIGITAL AND ANALOG BREAKDOWN

Figs. 4.20(a) and 4.20(b) show the $1/f$ -like noise signal spectrum ($S(f)$) for I_g in the digital and the analog breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.2 \times 0.3 \text{ } \mu\text{m}^2$), respectively, at $V_g = 0.9\text{-}2.1 \text{ V}$. A spike at $f = 50 \text{ Hz}$ can consistently be observed. It is due to the power supply noise, which will not affect our analysis. In Fig. 4.20(a), the $1/f$ -like noise for I_g in the digital breakdown does not follow any particular trend with respect to V_g . For instance, the $1/f$ -like noise for I_g at $V_g = 1.5 \text{ V}$ experienced partial recovery, as compared with that at $V_g = 1.2 \text{ V}$. This also took place on the $1/f$ -like noise for I_g at $V_g = 1.8$ and 2.1 V . However, as shown in Fig. 4.20(b), the $1/f$ -like noise for I_g in the analog breakdown increases with increasing V_g . The $1/f$ -like noise for the fresh I_g of the n-MOSFET, which is independent on V_g , is included for comparison. Furthermore, at a specific V_g , the $1/f$ -like noise for I_g in the digital breakdown is constituted by several regions with different slopes.

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(a)

(b)

Figure. 4.20. $1/f$ -like noise signal spectrum (i.e., $S(f)$) for I_g in (a) the digital and (b) the analog breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.2 \times 0.3 \text{ \mu m}^2$) at various V_g . The $1/f$ -like noise for the fresh I_g of the n-MOSFET, which is independent on V_g , is included for comparison.

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For instance, as shown in Fig. 4.20(a), three different slopes can be observed in the $1/f$ -like noise for I_g at $V_g = 2.1$ V. On the other hand, this was not seen in the $1/f$ -like for I_g in the analog breakdown. Fig. 4.21 shows the $1/f$ -like noise for I_g at different stages of the progressive breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ }\mu\text{m}^2$) at $V_g = 1.8$ V. For I_{gl} below $15 \text{ }\mu\text{A}$, the digital breakdown dominates, and this was confirmed by the digital fluctuation of I_g . On the other hand, for I_{gl} above $50 \text{ }\mu\text{A}$, the analog breakdown dominates, and this was confirmed by the relatively stable profile of I_g .

Figure 4.21. $1/f$ -like noise for I_g at different stages of the progressive breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ }\mu\text{m}^2$) at $V_g = 1.8$ V. $I_{gl} = 1, 5$ and $15 \text{ }\mu\text{A}$ correspond to the digital breakdown, while $I_{gl} = 50, 70$ and $100 \text{ }\mu\text{A}$ correspond to the analog breakdown. Additionally, $I_{gl} = 35 \text{ }\mu\text{A}$ corresponds to a stage when I_{DIG} and I_{ANA} are comparable with each other.

Additionally, $I_{gl} = 35 \text{ }\mu\text{A}$ corresponds to a stage for which I_{DIG} and I_{ANA} are comparable with each other. In summary, the $1/f$ -like noise for I_g in the digital breakdown largely fluctuates with a random trend. However, the $1/f$ -like noise for I_g in the analog breakdown

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experiences very less fluctuation and is reproducible. Furthermore, the $1/f$ -like noise for SILC behaves identical to that for the fresh I_g . The increase in the magnitude and the slopes of $S(f)$ are believed due to the formation of a percolation path within the gate oxide as this can only be noticed after the occurrence of a dielectric breakdown event.

Figure. 4.22. Typical examples for the fitting of the curves of $S(f)$ versus f based on Eqn. (4.7). The green and the blue line represent the $1/f$ -like noise for the fresh and the post-breakdown I_g . Moreover, the solid line is the measured data, while the dash line is the fitting data.

The general formula of $1/f$ -like noise signal spectrum can be described as [128-131]

$$S(f) = \frac{K}{f^\alpha} \tag{4.7}$$

where K is a constant parameter. α , which defines the slopes of $S(f)$, is mainly applied to classify the types or color of noise. Hence, the extraction of α from the curves of $S(f)$ versus f is particularly important. One of the ways in extracting α is to fit the curves of $S(f)$

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versus f using Eqn. (4.7). Typical examples for the fitting of the curves of $S(f)$ versus f based on Eqn. (4.7) are shown in Fig. 4.22. The classification of different types of noise in accordance with α is presented as follows [128-131]:

- White noise, $\alpha = 0$:

The white noise is a random signal with a flat power spectral density. One common type of white noise in electronic devices is the thermal noise, which is also known as the Johnson-Nyquist noise. The thermal noise is generated by the thermal agitation of charge carriers in an electrical conductor at equilibrium, regardless of any applied voltage.

- Pink or flicker noise, $\alpha = 1$:

The pink noise, which is also known as the flicker noise, is generated by the flow of a direct current in an electronic device. The pink noise can be observed in almost all types of electronic devices. The occurrence of pink noise could be due to various factors, such as impurities in the channel of a MOSFET, as well as the generation and the recombination of charge carriers in a MOSFET. The pink noise is considered as low- f phenomenon as it will be over-shadowed by the white or thermal noise at a higher f .

- Brown noise, $\alpha = 2$:

The brown noise, which is named after Robert Brown, is generated by the Brownian motions or random movements of particles in an irregular environment. The fractional brown noise is associated with $0 < \alpha < 2$, where α is a non-integer. The combined effects of the white, the pink and the brown noise will lead to the generation of fractional brown noise.

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- Black noise, $\alpha > 2$:

The black noise could be the mixture of the different types of noise.

Note that the $1/f$ noise is a term that strictly refers to the pink noise, where $\alpha = 1$. In this study, α varies from 0 to 5, and thus, the term “ $1/f$ -like noise” is used.

Fig. 4.23 shows the range of α in different cases. At a low f , α for the fresh I_g and SILC are in the range of 0.9-1.2, indicating that the fresh I_g and SILC are associated with the pink or flicker noise. Contrarily, it can be observed that α for the fresh I_g and SILC are nearly equal to zero at a higher f . Thus, the $1/f$ -like noise at a higher f for the fresh I_g and SILC are mainly composed by the white noise. Note that both the pink and the white noise are commonly seen in non-breakdown electronic devices [129, 130]. As shown in Fig. 4.23, α for I_g in the digital and the analog breakdown can be much larger than 1, showing that the brown noise prevails. Different from Cases C and D, the brown noise cannot be noticed in Cases A and B. Hence, the presence of the brown noise in the digital and the analog breakdown is believed due to the Brownian motions or random movements of the charge carriers through a percolation path formed within the gate oxide. α for I_g in the digital breakdown, which varies from 0.5 to 5, experiences the largest fluctuation. This signifies that the physical nature of the percolation path could be very unstable. When α is smaller than 1, the brown noise disappears, implying that the percolation path is “switched off”. Contrarily, when α is larger than 1, the brown noise appears, implying that the percolation path is “switched on”. However, α for I_g in the analog breakdown fluctuates in a relatively narrow range of 1.9-3. This signifies that the percolation path could be associated with a stable physical structure. Since α is consistently larger than 1, the brown noise permanently dominates, and the percolation path will never be “switched off”.

Figure 4.23. Range of α in different cases: Cases A and B correspond to the fresh I_g and SILC at f smaller and larger than 50 Hz, respectively. Cases C and D correspond to the digital and the analog breakdown, respectively.

4.6 DIGITAL FLUCTUATION OF POST-BREAKDOWN I_g DUE TO OXYGEN-VACANCY-RELATED DEFECT TRANSFORMATION

In this section, we establish a theoretical explanation for the digital fluctuation of I_g based on the transformation of oxygen-vacancy-related defects, which primarily include neutral oxygen vacancies and E'-centers that are typically created in silicon dioxide and silicon oxynitride during the gate oxide stressing. Therefore, we will first provide some general information about each type of oxygen-vacancy-related defects before the model is discussed.

4.6.1 SILICON DIOXIDE TETRAHEDRON

Silicon dioxide, which is formed by strong, directional covalent bonds, consists of a well-defined local tetrahedral structure: four oxygen atoms are arrayed at the corners of a

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tetrahedron around one silicon atom with the O-Si-O bond angle of 109 degrees. Fig. 4.24 shows the molecular geometry of a silicon dioxide covalent network formed by linking two silicon dioxide tetrahedrons with each other.

Figure 4.24. Molecular geometry of a silicon dioxide covalent network that is formed by linking two silicon dioxide tetrahedrons with each other.

According to Refs. [132-135], the Si-O bond length could vary from 0.1595 nm to 0.1615 nm. Thus, a covalent network of silicon dioxide will consist of a short- and a long-bond silicon atom, as shown in Fig. 4.24. The definition of each of the parameters is given as follows:

- r_{SB} defines the distance between an oxygen atom and a short-bond silicon atom, while r_{LB} defines the distance between an oxygen atom and a long-bond silicon atom.
- A_{SB-O} defines the axis along an oxygen atom and a short-bond silicon atom, while A_{LB-O} defines the axis along an oxygen atom and a long-bond silicon atom.
- A_E defines the axis parallel to an electric field.

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- γ_{SB} defines the angle between A_{SB-O} and A_E , while γ_{LB} defines the distance between A_{LB-O} and A_E .

The Si-O-Si bond angle, which is $\gamma_{SB} + \gamma_{LB}$, can vary from 100° to 170° .

Figure 4.25. Molecular geometry of an E'-center in silicon dioxide and silicon oxynitride. Spin localization concentrates at the short-bond silicon atom, while a positive charge or trapped hole is situated at the long-bond silicon atom.

4.6.2 NEUTRAL OXYGEN VACANCY AND E'-CENTER

A neutral oxygen vacancy, which is a neutrally-charged state and denoted as V_O , is equivalent to the “kick-out” of one oxygen atom from a strong covalent network of silicon dioxide [132-135]. Eventually, the short-bond silicon atom will possess one unpaired electron, and this is the same for the long-bond silicon atom. A neutral oxygen vacancy could be considered as a spin-1 defect if the unpaired electrons are either spinning-up or -down. Obviously, no spin will be detected if one of the unpaired electrons is spinning-up

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but another one is spinning-down. When an oxygen atom linking two silicon dioxide tetrahedrons is missing, the short- and the long-bond silicon atoms would symmetrically relax towards each other and interact to form a so-called strained silicon-silicon bond. Some of the studies have been proposed that the strained silicon-silicon bond plays a critical role in triggering the occurrence of a dielectric breakdown event [70-73].

The electron spin resonance (ESR) technique has been widely used to study point defects in silicon dioxide [136]. Based on the ESR technique, it is found that an E'-center possesses the spin of $\frac{1}{2}$ on the sp^3 hybrid orbital of a short-bond silicon atom. An E'-center, which is a positively-charged state and denoted as V_O^+ , is observed as one type of the most dominant oxygen-vacancy-related defects in silicon dioxide [132-135]. In general, the formation of an E'-center can be characterized as the "kick-out" of one oxygen atom and one electron in the sp^3 hybrid orbital of a long-bond silicon atom from a strong covalent network of silicon dioxide. Therefore, a neutral oxygen vacancy is believed to be the precursor of an E'-center [132-135], in which an E'-center can be formed by removing one electron from a neutral oxygen vacancy. The removal of one unpaired electron from the long-bond silicon atom means that a positive charge exists on the long-bond silicon atom. The long-bond silicon atom, which has a trapped hole, will move towards the basal plane of three oxygen atoms along A_{LB-O} . It is suggested that the long-bond silicon atom will be bonded with a back-bonding oxygen atom, and this is known as a puckered configuration. Due to the presence of a puckered configuration, an E'-center is reported as a meta-stable point defect in silicon dioxide. In addition, the short-bond silicon atom, which has one unpaired electron, will move away from the basal plane of three oxygen atoms along A_{SB-O} . However, some of the simulation results demonstrated

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that the short-bond silicon atom will move towards the basal plane of three oxygen atoms along A_{SB-O} . The molecular geometry of an E'-center is demonstrated in Fig. 4.25. r_{SB} ' defines the distance between the short-bond silicon atom and the missing oxygen atom after asymmetric atomic relaxation. Likewise, r_{LB} ' defines the distance between the long-bond silicon atom and the missing oxygen atom after asymmetric atomic relaxation.

Figure 4.26. Calculated dipole moment of an E'-center with $r_{SB} = 0.1598$ nm, $r_{LB} = 0.1612$ nm and $\gamma_{SB} + \gamma_{LB} = 140^\circ$ under different cases, in which the short-bond silicon atom moves (a) towards or (b) away from the missing oxygen atom. Note that $d_{SB} = |r_{SB}' - r_{SB}|$ and $d_{LB} = |r_{LB}' - r_{LB}|$.

4.6.3 MODEL

According to the observations of J. H. Stathis [3], the gradual evolution of SILC with increasing stressing time is associated with the generation of more paramagnetic defects within the gate oxide. Hence, it is believed that the occurrence of a dielectric breakdown event is due to the formation of a percolation path within the gate oxide with the accumulation of E'-centers, which are categorized as one common type of paramagnetic defects in silicon dioxide.

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To model the digital fluctuation of I_g in the digital breakdown, we assume that defects in a percolation path formed within silicon dioxide and silicon oxynitride are mainly constituted by E'-centers and neutral oxygen vacancies [70-73, 131-135]. An E'-center can be considered as a permanent dipole, which points from the negative charge at the short-bond silicon atom to the positive charge at the long-bond silicon atom. Then, the dipole moment of an E'-center can be calculated as

$$p = q \times r_{DIP} \quad (4.8)$$

where

$$r_{DIP} = \sqrt{r_{LB}^2 + r_{SB}^2 - 2r_{LB}r_{SB}\cos(\gamma_{LB} + \gamma_{SB})} \quad (4.9)$$

Figs. 4.26(a) and 4.26(b) shows the calculated dipole moment of an E'-center with $r_{SB} = 0.1598$ nm, $r_{LB} = 0.1612$ nm and $\gamma_{SB} + \gamma_{LB} = 140^\circ$ under different cases, in which the short-bond silicon atom moves towards or away from the missing oxygen atom. Note that $d_{SB} = |r_{SB}' - r_{SB}|$ and $d_{LB} = |r_{LB}' - r_{LB}|$. It can be noticed that the dipole moment of an E'-center varies from 5 Debye to 25 Debye, agreeing well with the simulation results reported in Refs. [133, 134]. The size and the shape of an E'-center are demonstrated as the dotted red ellipse in Fig. 4.25. d_A and d_B define the horizontal and the vertical diameter of an ellipse representing an E'-center, respectively. Our calculations show that d_A and d_B vary from 2 Å to 5.5 Å. Fig. 4.27 shows the calculated d_A and d_B of an E'-center with $r_{SB} = 0.1598$ nm and $r_{LB} = 0.1612$ nm, where $\gamma_{LB} = 40, 120, 200$ and 320° such that $\gamma_{SB} + \gamma_{LB} = 120$ and 140° . Using the similar procedure, the dipole moment and the size of a neutral oxygen vacancy and an interface state or Pb-center [137, 138] can be obtained, as summarized in Table 4.3. Since a neutral oxygen vacancy is not a permanent dipole, it is associated with a lower dipole moment.

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Figure 4.27. Calculated d_A and d_B of an E' -center with $r_{SB} = 0.1598$ nm and $r_{LB} = 0.1612$ nm, where $\gamma_{LB} = 40, 120, 200$ and 320° such that $\gamma_{SB} + \gamma_{LB} = 120$ and 140° .

	E' -center	Neutral oxygen vacancy	Pb-center
Dipole moment	5-25 Debye	1-2 Debye	5-30 Debye
d_A and d_B	2-6 Å		

Table 4.3. Dipole moment and size of an E' -center, a neutral oxygen vacancy and a Pb-center [137, 138].

Fig. 4.28 shows a simple, columnar percolation path formed within a 16-Å silicon dioxide network [96, 97]. The percolation path is mainly constituted by three defects, which are two interface states or Pb-centers and one bulk trap. One of the Pb-centers is situated at the silicon substrate/silicon dioxide interface, while another is situated at the poly-silicon gate/silicon dioxide interface. The bulk trap, which is either an E' -center or neutral oxygen vacancy, is situated in the gate oxide. The molecular geometry properties of these defects are randomly generated by Monte Carlo simulation.

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(a)

(b)

Figure 4.28. A simple, columnar percolation path formed within a 16-Å silicon dioxide network. The percolation path is mainly constituted by two interface states, which are denoted as IT₁ and IT₂, and one bulk trap, which is denoted as BT. **(a)** Local electric field distribution for which BT is V_O⁺. **(b)** Calculated ϕ_E along the line AA' in accordance with Eqn. (4.10). The black and the red solid line correspond to the case for which the bulk trap is V_O⁺ and V_O, respectively.

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The distance between two defects is 5-6 Å, which is in a range that allows the electron hopping from the cathode to the anode through defective sites to occur [96, 97]. Fig. 4.28(a) shows the local electric field distribution, assuming that the bulk trap is an E'-center. Due to the presence of different dipole moments, the local electric field around the vicinity of a percolation path has been largely disturbed. Consequently, the non-uniformity of the local electric field distribution will result in a lowering of the local electron barrier heights (ϕ_E).

Figure 4.29. An inclined percolation path, which is a variation of the percolation path shown in Fig. 4.28. The inclination angle must be smaller than 35-37°, allowing the electron hopping from the cathode to the anode through the defective sites to occur.

As shown in Fig. 4.28(b), ϕ_E along the line AA' can be calculated in accordance with [139]

$$\phi_E = q\Phi_E - \beta^{-1}E_{loc}^{1/2} \tag{4.10}$$

where

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$$\beta = \sqrt{\frac{q^3}{4\pi\epsilon_0\epsilon_{loc}}} \quad (4.11)$$

E_{loc} and ϵ_{loc} define the local electric field and the local permittivity within the gate oxide, respectively. E_{loc} will be high when an area consists of huge variation in ϵ_{loc} , which in turn depends on Eqn. (4.8). According to Eqn. (4.10), the lowering of ϕ_E will not occur if $E_{loc} = 0$ (i.e., variation in ϵ_{loc} does not exist). The black and the red solid line in Fig. 4.28(b) correspond to the case for which the bulk trap is an E'-center and a neutral oxygen vacancy, respectively. The calculation of ϕ_E is performed from the silicon substrate/silicon dioxide interface to the polycrystalline-silicon gate/silicon dioxide interface with the interval of 2 Å. Note that the ideal case of $q\Phi_E = 3.2$ eV is used. It can be observed that some of the areas within the percolation path in Fig. 4.28(a) are non-defective. Thus, the change in ϕ_E in these areas will be relatively minor.

Fig. 4.29 shows an inclined percolation path, which is a variation of the percolation path shown in Fig. 4.28. This is another possible geometry of a percolation path involving two interface states and one bulk trap. The transformation of a bulk trap from an E'-center into a neutral oxygen vacancy, or vice versa, will generate the structure of ϕ_E similar to Fig. 4.28(b). However, the non-defective regions in the structure of ϕ_E will be elongated with increasing inclination angle with respect to the axis of the applied electric field. For the case shown in Fig. 4.29, the inclination angle must be smaller than 35-37°, allowing the electron hopping from the cathode to the anode through the defective sites to occur [96, 97].

A flowchart that describes the transformation between an E'-center and a neutral oxygen vacancy with the presence of the charge carriers, which are electrons and holes,

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during the gate oxide stressing is shown in Fig. 4.30 [140]. A neutral oxygen vacancy will be transformed into an E'-center by capturing a hole, and vice versa.

Figure 4.30. Flowchart describing the transformation between an E'-center and a neutral oxygen vacancy with the presence of charge carriers during the gate oxide stressing [140].

Note that a neutral oxygen vacancy is believed to be the precursor of an E'-center. Fig. 4.31 shows the hole generation rate, which can be described as I_{sub}/I_g , in the digital and the analog breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ A}$ were used. In the 2nd-stage CVS, $V_{gstress} = V_{crit} = 3 \text{ V}$ were used without setting any limit on I_{gl} . I_{sub}/I_g in the digital breakdown is in the range of 0.1-0.9, meaning that the valence-band hole tunneling from the polycrystalline-silicon gate into the silicon substrate is substantially high. This enhances the possibility for a neutral

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oxygen vacancy captures a hole to form an E'-center. Moreover, it can be observed that I_{sub}/I_g quickly reduced to a low level of 10^{-4} - 10^{-3} when I_g evolved from the digital breakdown into the analog breakdown.

Figure 4.31. Hole generation rate, which can be described as I_{sub}/I_g , in the digital and the analog breakdown for a n-MOSFET ($T_{ox} = 22$ Å and $L \times W = 0.5 \times 0.6$ μm^2) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1$ V and $I_{gl} = 1$ A were used. In the 2nd-stage CVS, $V_{gstress} = V_{crit} = 3$ V were used without setting any limit on I_{gl} .

In the analog breakdown, a percolation path with a relatively stable core will be formed, allowing the huge amount of electrons to flow from the channel of a MOSFET to the gate electrode. As a result, I_g significantly increases, and this will in turn suppress I_{sub}/I_g . Moreover, as shown in Fig. 4.30, if an E'-center captures an electron, then the compensation of charges and the elimination of unpaired spins will lead to the formation of a neutral oxygen vacancy with a strained silicon-silicon bond.

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(a)

(b)

Figure 4.32. A simple, columnar percolation path formed within a 12-Å silicon dioxide network. The percolation path is mainly constituted by two interface states, which are denoted as IT₁ and IT₂, and three bulk traps, which are denoted as BT₁, BT₂ and BT₃. (a) Local electric field distribution for which BT₁, BT₂ and BT₃ are V_O⁺. (b) Calculated ϕ_E along the line BB' in accordance with Eqn. (4.10). The black, the red and the blue solid line correspond to the case for which (BT₁, BT₂, BT₃) = (V_O⁺, V_O⁺, V_O⁺), (BT₁, BT₂, BT₃) = (V_O, V_O, V_O) and (BT₁, BT₂, BT₃) = (V_O⁺, V_O, V_O⁺), respectively.

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For V_g smaller than V_{crit} , the likelihood of transforming an E'-center into a neutral oxygen vacancy during the gate oxide stressing, or vice versa, is higher than that of further wearing-out the percolation path by creating new defects in the vicinity of the percolation path. The transformation of defects [140] during the gate oxide stressing will cause a constant change in ϕ_E , enhancing or reducing the tunneling of charge carriers. For instance, as shown in Fig. 4.28(b), when the bulk trap is transformed from an E'-center into a neutral oxygen vacancy, ϕ_E will increase, causing the amount of tunneling electrons to reduce. Therefore, this will result in the random fluctuation of I_g at two specific values, as shown in Fig. 4.2(a).

Fig. 4.32 shows a simple, columnar percolation path formed within a 12-Å silicon dioxide network, for which the percolation path is mainly constituted two interface states and three bulk traps. Fig. 4.32(a) shows the local electric field distribution for which the bulk traps are E'-centers. Moreover, Fig. 4.32(b) shows the calculated ϕ_E along the line BB' in accordance with Eqn. (4.10) for three different combinations of the types of bulk traps. Since there are more bulk traps in a percolation path, more permutations of the bulk traps could lead to more changes in ϕ_E . As a result, this will cause I_g to increase or decrease digitally to more levels, as shown in Fig. 4.2(a). There should be at least $2^3 = 8$ possibilities for the changes in ϕ_E . The high local heat generated by the flow of I_g through the percolation path could lead to the re-bonding of unstable, broken silicon bonds in E'-centers and neutral oxygen vacancies, forming a conductive channel at the core of the percolation path, as shown in Fig. 4.18(b). This will lead to a relatively stable I_g , that is, the analog breakdown.

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4.7 MULTIPLE PERCOLATION PATHS IN DIGITAL BREAKDOWN

It has been reported that for a n-MOSFET with ultrathin gate oxide and a gate area less than $1 \mu\text{m}^2$, the progressive breakdown under the accelerated stressing conditions will most likely be governed by one single percolation path [141]. In this section, we will demonstrate the occurrence of multiple percolation paths in the digital breakdown at V_g smaller than V_{crit} .

Fig. 4.33 show the evolution of I_g (i.e., the caption “I”) and s_{BD} (i.e., the caption “II”) during the progressive breakdown for three n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \mu\text{m}^2$) stressed using one-cycle multiple-stage CVS in inversion mode at the room temperature. s_{BD} was measured in inversion mode during the gate oxide stressing and accumulation mode after the gate oxide stressing. The TDDB of these n-MOSFETs was carried out with $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \mu\text{A}$. The one-cycle multiple-stage CVS was performed with:

- $V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 100 \text{ s}$ and $V_{final} = V_{crit} = 3 \text{ V}$ for the n-MOSFET in Fig. 4.33(a)
- $V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 300 \text{ s}$ and $V_{final} = V_{crit} = 3.2 \text{ V}$ for the n-MOSFET in Fig. 4.33(b), and;
- $V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 300 \text{ s}$ and $V_{final} = V_g = 3 \text{ V}$ for the n-MOSFET in Fig. 4.33(c).

As shown in Fig. 4.33(a), s_{BD} remained nearly unchanged at $0.5\text{-}0.6L$, which is the center of the device channel, when I_g evolved from the digital breakdown into the analog breakdown. This implies that the behaviors of I_g throughout the progressive breakdown were governed by one single percolation path.

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Figure 4.33. Evolution of (I) I_g and (II) s_{BD} during the progressive breakdown for three n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) stressed using one-cycle multiple-stage CVS in inversion mode at the room temperature. The TDDDB of these n-MOSFETs was carried out with $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$. Three cases are shown here: (a) One single percolation path ($V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 100 \text{ s}$ and $V_{final} = V_{crit} = 3 \text{ V}$), (b) multiple percolation paths ($V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 300 \text{ s}$ and $V_{final} = V_{crit} = 3.2 \text{ V}$), and (c) a second percolation path at the source terminal ($V_{init} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{stress} = 300 \text{ s}$ and $V_{final} = V_g = 3 \text{ V}$).

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However, as shown in Fig. 4.33(b), s_{BD} steadily evolved at 0.6L before ~850 s and experienced a sudden change from 0.6L to 0.78L after ~850 s. Note that I_g was still in the digital breakdown. Subsequently, I_g fluctuated in between 0.6L and 0.9L, and became stable after entering into the analog breakdown at ~1750 s. It is believed that a second percolation path (or may be more) could be formed to cause the fluctuation of s_{BD} between 0.6L and 0.9L. Fig. 4.33(c) shows the worst case. s_{BD} suddenly jumped from 0.4L to 0L at V_g smaller than V_{crit} . This means that a second percolation path was formed at a distance very close to the source terminal, resulting in the occurrence of a catastrophic breakdown due to the electrical short between the gate electrode and the source terminal. Note that V_{crit} for $T_{ox} = 22 \text{ \AA}$ is in the range of 2.9-3.5 V, as shown in Table 4.1.

Under the accelerated stressing conditions, the progressive breakdown in a n-MOSFET with ultrathin gate oxide and a gate area less than $1 \mu\text{m}^2$ is most likely governed by one single percolation path [141]. However, it is believed that the gate oxide consists of other “potential” percolation paths [12] even for a small gate area. As mentioned in the previous section, the digital breakdown can hardly evolve into the analog breakdown if V_g is smaller than V_{crit} . This means that in the digital breakdown, if V_g is low, further wearing-out of the first percolation path takes a long time, and this may provide sufficient time for other “potential” percolation paths to form. In contrast, under the accelerated stressing conditions, the first percolation path will be rapidly worn-out and becomes a relatively stable conductive channel, suppressing the formation of other “potential” percolation paths. In brief, the results indicate that multiple percolation paths are most probably to occur in the digital breakdown when V_g is smaller than V_{crit} . This means that device failure will still occur if the effective I_g from all the percolation paths exceeds the

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device leakage current criterion. However, when the n^{th} percolation path is formed at the source or drain terminal during the normal device operations, the occurrence of a catastrophic breakdown will always be triggered. Fig. 4.34 summarizes the formation of multiple percolation paths in the digital breakdown at V_g smaller than V_{crit} , and its impact on the post-breakdown device reliability.

Figure 4.34. Formation of multiple percolation paths in the digital breakdown at V_g smaller than V_{crit} , and its impact on the post-breakdown device reliability.

4.8 SUMMARY

Using a K-cycle multiple-stage CVS, V_{crit} is found to demarcate the evolution of I_g during the progressive breakdown into two distinct regions, which are the digital and the analog breakdown. V_{crit} is a significant parameter in studying the behaviors of I_g at a low V_g during the progressive breakdown. In the early stage of the progressive breakdown, if V_g is smaller than V_{crit} , I_g digitally fluctuates with no apparent net increase. However, for V_g larger than V_{crit} , I_g rapidly evolves into a relatively stable high leakage state, which is the analog breakdown. The transition from the digital breakdown into the analog breakdown is irreversible. The digital breakdown can hardly evolve into the analog breakdown if V_g is

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smaller than V_{crit} , meaning that the progressive breakdown can largely be prolonged at a low V_g . As a result, this brings a significant impact on the extraction of dI_g/dt from a high V_g (i.e., $V_{gstress}$) to a low V_g (i.e., V_{op}). Moreover, a saturation of V_{crit} in the range of 1.9-2.4 V is found for T_{ox} lower than 1.6 nm. This implies that the role of the digital breakdown in extending the post-breakdown gate oxide lifetime still exists in sub-90-nm CMOS technology employing T_{ox} below 1.6 nm. The magnitude of I_g also plays a critical role in governing the transition of the digital breakdown into the analog breakdown. If the progressive breakdown is arrested at a low I_{gl} , the percolation path will not be transformed into a relatively stable silicon-like structure due to the absence of a high local temperature. As a result, the analog breakdown will not take place.

The $1/f$ -like noise measurements of I_g at different stages of the progressive breakdown confirm that a percolation path formed within the gate oxide could grow from an unstable physical structure in the digital breakdown into a stable physical structure in the analog breakdown. We show that V_{crit} is an independent function of various parameters, such as s_{BD} , L , W and t_{stress} . A model involving E'-centers and neutral oxygen vacancies is developed to explain the digital fluctuation and the digital-to-analog transformation of I_g . At a low V_g , the digital fluctuation of I_g is mainly attributed to the transformation of defects during the gate oxide stressing. The model suggests that at V_g smaller than V_{crit} , multiple percolation paths are more likely to occur in a device with the digital breakdown, affecting the post-breakdown lifetime of a device operating at V_{op} .

CHAPTER FIVE

INFLUENCE OF OXIDE BREAKDOWN PERCOLATION RESISTANCE ON MOSFETS

5.1 INTRODUCTION

According to the percolation model [9-12], the occurrence of a dielectric breakdown event is triggered by the formation of a conductive percolation path within the gate oxide. The percolation path, which is mainly constituted by oxygen-vacancy-related defects [132-136], serves as a conductive channel that electrically links the gate electrode and the substrate with each other. This is responsible for a sudden, abrupt increase in I_g , indicating that the progressive breakdown [22-24] starts to evolve. After a rapid degradation to a certain high level, I_g will gradually saturate. This region is generally classified as the analog breakdown. It is believed that the behaviors of I_g in the analog breakdown are governed by a change in the resistances of some local defective areas within the gate oxide. This implies that the effective resistance of a percolation path [23, 142, 143] acts as one of the vital parameters in controlling the evolution of I_g in the analog breakdown. The effective post-breakdown gate resistance, which is computed as $R_g = V_g / I_g$, is a total resistance that has been used to classify a soft and a hard breakdown [17-21]. As suggested by F. Crupi *et al.* [143], a n-MOSFET is said to experience a hard breakdown if it is associated with R_g smaller than $10^5 \Omega$, while a n-MOSFET is said to experience a soft

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breakdown if it is associated with R_g larger than $10^5 \Omega$. R_g may be employed as a criterion to determine the breakdown hardness of a n-MOSFET, but it does not provide any detail on the interaction among different resistances during the progressive breakdown. It has also been reported that an external resistor connected to the gate electrode can prolong the degradation of I_g to a specific high level [143].

In this chapter, a simple but compact methodology has been developed to measure the evolution of the percolation resistance and the channel resistances during the progressive breakdown. Using this method, the physical mechanisms governing the behaviors of I_g in the analog breakdown can be studied in details.

5.2 EXPERIMENTS

To study the physical mechanisms governing the behaviors of I_g in the analog breakdown or the later stage of the progressive breakdown under various conditions, a two-stage CVS described in *Chapter Three* was used. All the necessary sample information and stressing conditions can also be found in *Chapter Three*. The post-breakdown electrical measurements of the n-MOSFETs involved in this study were performed at a low V_g , which is normally less than 2 V, such that the degradation of a percolation path can be minimized.

5.3 PERCOLATION RESISTANCE MEASUREMENT METHOD

The PRM method is developed in accordance with the flow of the terminal currents in a breakdown n-MOSFET. Fig. 5.1 shows the general schematic of the PRM method, which is mainly constituted by three independent experimental steps in determining the

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percolation resistance and the channel resistances at one particular instant of the progressive breakdown. The definition of each parameter shown in Fig. 5.1 is described as follows:

- R_{perc} , which is simply known as the percolation resistance, is the effective resistance of a conductive percolation path formed within the gate oxide of the n-MOSFET during the occurrence of a dielectric breakdown event;

Figure 5.1. General schematic of the PRM method, which is developed in accordance with the flow of the terminal currents in a breakdown n-MOSFET. R_{perc} is the effective resistance of a percolation path formed within the gate oxide of the n-MOSFET during the occurrence of a dielectric breakdown event. $R_{\text{ch-d}}$ and $R_{\text{ch-s}}$ are the effective channel resistance from the percolation path to the drain and the source terminal of the n-MOSFET, respectively.

- $R_{\text{ch-d}}$ and $R_{\text{ch-s}}$ are the effective channel resistance from the percolation path to the drain and the source terminal of the n-MOSFET, respectively;
- R_{poly} is the resistance associated with the gate electrode of the n-MOSFET;

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- I_g , I_d , I_s and I_{sub} are the post-breakdown current that flows to the gate electrode, the drain terminal, the source terminal and the substrate of the n-MOSFET, respectively, and;

V_g , V_d , V_s and V_{sub} are the voltage applied to the gate electrode, the drain terminal, the source terminal and the substrate of the n-MOSFET, respectively.

Figure 5.2. (a) Configuration of the first experimental step of the PRM method. (b) Typical example for I_g - V_g characteristics at one particular instant of the progressive breakdown for an n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$), where $V_d = V_s = V_{sub} = 0$. The arrow indicates $I_g @ V_g = 1.5 \text{ V}$.

The first experimental step of the PRM method involves a post-breakdown I_g - V_g measurement, while the drain terminal, the source terminal and the substrate of the n-MOSFET are grounded (i.e., $V_d = V_s = V_{sub} = 0$). The configuration of the first experimental step of the PRM method is shown in Fig. 5.2(a). Fig. 5.2(b) shows a typical example for the I_g - V_g characteristics at one particular instant of the progressive breakdown for an n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$). Then, we can obtain

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$$I_{gl}(R_{perc} + R_{poly}) + I_{d1}R_{ch-d} = V_g \tag{5.1}$$

and

$$I_{gl}(R_{perc} + R_{poly}) + I_{s1}R_{ch-s} = V_g \tag{5.2}$$

where $V_g = 1.5$ V was commonly used in this study. Rearranging Eqns. (5.1) and (5.2), we have

$$I_{d1}R_{ch-d} = I_{s1}R_{ch-s} \tag{5.3}$$

Figure 5.3. (a) Configuration of the second experimental step of the PRM method. (b) Typical example for I_d - V_g characteristics at one particular instant of the progressive breakdown for a n-MOSFET ($T_{ox} = 22$ Å and $L \times W = 1 \times 1.2$ μm^2), where $V_s = V_{sub} = 0$. The arrows indicate $I_d = 0$ @ $V_g = 1.1$ V and $I_d = 0$ @ $V_g = 1.5$ V.

V_g is chosen to be in the range comparable to the operating voltages of a n-MOSFET such that an inversion layer is successfully created at the Si-SiO_xN_y interface underneath the gate oxide of the n-MOSFET. Additionally, V_g must be considerably lower than $V_{gstress}$, in which this can ensure that the further degradation of the percolation path is avoided or minimized.

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The second experimental step of the PRM method involves a post-breakdown I_d - V_g measurement by applying a small constant voltage in the order of 10^{-5} - 10^{-3} V to the drain terminal of the n-MOSFET, while the source terminal and the substrate of the n-MOSFET are grounded (i.e., $V_s = V_{sub} = 0$). The configuration of the second experimental step of the PRM method is shown in Fig. 5.3(a). Fig. 5.3(b) shows a typical example for the I_d - V_g characteristic at one particular instant of the progressive breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$). Due to the gradual increase in V_g and the presence of a small constant V_d , a maximum in the I_d - V_g curve can be noticed. Furthermore, the reversal of the flowing direction of I_d , which means that I_d changes from a positive value to a negative value, occurred at a specific V_g . The factors of determining V_g for $I_d = 0$ involve the hardness of the progressive breakdown and the magnitude of V_d . By adjusting V_d such that $I_d = 0 @ V_g = 1.5 \text{ V}$, we obtain

$$I_{g2}(R_{perc} + R_{poly}) + I_{s2}R_{ch-s} = V_g \quad (5.4)$$

Since $I_d = 0$, $I_{g2} = I_{s2}$. This gives

$$I_{g2}[(R_{perc} + R_{poly}) + R_{ch-s}] = V_g \quad (5.5)$$

Compared to R_{perc} , R_{poly} will be negligibly small.

The third experimental step of the PRM method is implemented by swapping the drain terminal with the source terminal in the configuration of the second experimental step of the PRM method. Hence, the third experimental step of the PRM method involves a post-breakdown I_s - V_g measurement by applying a small constant voltage to the source terminal of the n-MOSFET, while the drain terminal and the substrate of the n-MOSFET are grounded (i.e., $V_d = V_{sub} = 0$). By adjusting V_s such that $I_s = 0 @ V_g = 1.5 \text{ V}$, we obtain

$$I_{g3}(R_{perc} + R_{poly}) + I_{d3}R_{ch-d} = V_g \quad (5.6)$$

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Likewise, since $I_s = 0$, $I_{g3} = I_{d3}$. This gives

$$I_{g3} [(R_{perc} + R_{poly}) + R_{ch-d}] = V_g \quad (5.7)$$

I_{d1} , I_{s1} , I_{g2} and I_{g3} are the post-breakdown terminal currents that can be experimentally obtained. The PRM method is valid if the following assumptions are not violated:

- V_g in the first, second and third experimental step of the PRM method must remain constant such that the alteration of R_{ch-d} and R_{ch-s} is negligible.
- V_d in the second experimental step of the PRM method (or V_s in the third experimental step of the PRM method) must be much smaller than V_g .
- I_{sub} is negligibly small, as compared to I_g , I_d and I_s .

Finally, $(R_{perc} + R_{poly})$, R_{ch-d} and R_{ch-s} can be calculated by solving Eqns. (5.3), (5.5) and (5.7). Since R_{poly} is much smaller than R_{perc} , $(R_{perc} + R_{poly})$ is approximately equal to R_{perc} , that is, $R_{perc} \cong (R_{perc} + R_{poly})$.

5.4 EVOLUTION OF R_{PERC} DURING PROGRESSIVE BREAKDOWN

Fig. 5.4(a) shows the evolution of R_{perc} , R_{ch-d} , R_{ch-s} and R_g at $V_g = 1.5$ V during the progressive breakdown for a n-MOSFET ($T_{ox} = 22$ Å and $L \times W = 1 \times 0.6$ μm^2), which is denoted as *SI* for convenience. *SI* was stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1$ V and $I_{gl} = 1$ μA were used. In the 2nd-stage, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . The progressive breakdown was halted at different instants, and R_{perc} , R_{ch-d} and R_{ch-s} at each instant of the progressive breakdown were calculated using the PRM method.

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Figure 5.4. (a) Evolution of R_{perc} , R_{ch-d} , R_{ch-s} and R_g at $V_g = 1.5$ V during the progressive breakdown for SI ($T_{ox} = 22$ Å and $L \times W = 1 \times 0.6 \mu m^2$), which was stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1$ V and $I_{gl} = 1 \mu A$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . (b) Evolution of s_{BD} during the progressive breakdown for SI . Note that s_{BD} remained nearly unchanged at 0.46-0.5L. The squares and the stars represent s_{BD} calculated from Eqn. (3.1) in accumulation mode at $V_g = -1.5$ V and Eqn. (5.8), respectively.

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For a n-MOSFET with ultrathin gate oxide and a gate area less than $1 \mu\text{m}^2$, the degradation of I_g during the progressive breakdown under the accelerated stressing conditions most probably corresponds to the degradation of one single percolation path [141]. For that reason, the degradation of R_{perc} during the progressive breakdown for SI is believed to be governed by one single percolation path. Generally, R_{perc} degrades with an extremely fast rate in the early stage of the progressive breakdown, but it largely slows down in the later stage of the progressive breakdown.

- $\square$ $L \times W = 1 \times 1.2 \mu\text{m}^2$ $\blacktriangledown$ $L \times W = 0.3 \times 0.6 \mu\text{m}^2$
 $\bullet$ $L \times W = 1 \times 0.6 \mu\text{m}^2$ $\diamond$ $L \times W = 1 \times 0.3 \mu\text{m}^2$
 $\triangle$ $L \times W = 0.5 \times 0.6 \mu\text{m}^2$

Figure 5.5. Evolution of R_{perc} at $V_g = 1.5 \text{ V}$ during the progressive breakdown for five n-MOSFETs with various device dimensions ($T_{\text{ox}} = 22 \text{ \AA}$, $L = 0.3\text{-}1 \mu\text{m}$ and $W = 0.3\text{-}1.2 \mu\text{m}$). These n-MOSFETs were stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{g\text{stress}} = 4\text{-}4.1 \text{ V}$ and $I_{gl} = 1 \mu\text{A}$ were used. In the 2nd-stage CVS, $V_{g\text{stress}}$ was reduced to $3.2\text{-}3.4 \text{ V}$ without setting any limit on I_{gl} . The evolution of R_{perc} during the progressive breakdown can be divided into two distinct regions, which are the R_{perc} - and the R_{para} -controlled region.

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In contrary, throughout the progressive breakdown, the degradation of R_{ch-d} and R_{ch-s} are relatively gentle and gradual.

Fig. 5.4(b) shows the evolution of the breakdown location, which is s_{BD} , during the progressive breakdown for SI . The squares in Fig. 5.4(b) represent s_{BD} calculated from Eqn. (3.2) in accumulation mode at $V_g = -1.5$ V. It can be observed that s_{BD} remained nearly unchanged at $0.46-0.5L$, meaning that the percolation path in SI was situated at the center of the device channel. In addition, since s_{BD} evolved with a stable profile, it is believed that no second percolation path was created within the gate oxide of SI during the progressive breakdown. As shown in Fig. 5.4(a), we can notice that R_{ch-d} is nearly equal to R_{ch-s} . Hence, the percolation path in SI is expected to be situated at the center of the device channel, meaning that s_{BD} should be close to $0.5L$. This basically agrees well with s_{BD} calculated from Eqn. (3.2). By obtaining R_{ch-d} and R_{ch-s} through the PRM method, we can calculate s_{BD} based on the following equation:

$$s_{BD} = \left(\frac{R_{ch-s}}{R_{ch-d} + R_{ch-s}} \right) \times L \quad (5.8)$$

As demonstrated in Refs. [123, 124], Eqns. (3.1) and (5.8) are equivalent with each other. The stars in Fig. 5.4(b) represent s_{BD} calculated from Eqn. (5.8). It can be observed that s_{BD} calculated from Eqns. (3.1) and (5.8) are in the same range, indicating that the PRM method is dependable and robust. R_g is included in Fig. 5.4(a) for comparison. It is important to note that the interaction among R_{perc} , R_{ch-d} and R_{ch-s} cannot be observed through R_g .

Similar results, as shown in Fig. 5.5, have been observed for breakdown n-MOSFETs with various device dimensions (i.e., $T_{ox} = 22$ Å, $L = 0.3-1$ μm and $W = 0.3-1.2$ μm). Note that our experimental measurements match well with the simulation results

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proposed by T. Hosoi *et al.* [23]. As shown in Figs. 5.4(a) and 5.5, two distinct slopes can be identified in the early and the later stage of the progressive breakdown. Thus, we classify the degradation of R_{perc} during the progressive breakdown into two distinct regions, namely, the R_{perc} - and the R_{para} -controlled region. R_{para} is the parasitic resistance that involves the total channel resistance (i.e., R_{ch}), the external resistance (i.e., R_{ext}) and R_{poly} . Here, R_{ch} is equivalent to the parallel resistance of $R_{\text{ch-d}}$ and $R_{\text{ch-s}}$.

Figure 5.6. Degradation rate of R_{perc} (i.e., dR_{perc}/dt) in the R_{perc} -controlled, the transition and the R_{para} -controlled region for about twenty breakdown n-MOSFETs ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.6 \text{ \mu m}^2$). The stressing conditions used in these n-MOSFETs were similar to those in Fig. 5.4. Note that dR_{perc}/dt describes the effective degradation of a percolation path during the progressive breakdown.

The R_{perc} -controlled region (i.e., $t < 20 \text{ s}$) corresponds to a rapid degradation of R_{perc} in the early stage of the progressive breakdown. Conversely, the R_{para} -controlled region (i.e., $t > 100 \text{ s}$) corresponds to a saturation of R_{perc} in the later stage of the progressive breakdown.

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As shown in Fig. 5.5, there exists a transition region (i.e., $20 \text{ s} < t < 100 \text{ s}$) when the R_{perc} -controlled region starts to evolve into the R_{para} -controlled region. Fig. 5.6 shows the degradation rate of R_{perc} (i.e., dR_{perc}/dt) in the R_{perc} -controlled, the transition and R_{para} -controlled region for about twenty breakdown n-MOSFETs ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.6 \text{ \mu m}^2$). The stressing conditions used in these n-MOSFETs were similar to those in Fig. 5.4. Note that dR_{perc}/dt describes the effective degradation of a percolation path during the progressive breakdown. With the presence of an inversion layer at the Si-SiO_xN_y interface underneath the gate oxide and the absence of an external resistor, R_{para} is mainly constituted by R_{ch} , that is, $R_{\text{para}} \cong R_{\text{ch}}$. In the R_{perc} -controlled region, where the progressive breakdown just starts to evolve, R_{perc} is extremely large, resulting in $R_{\text{g}} \cong R_{\text{perc}}$. As shown in Fig. 5.4(a), R_{perc} in the R_{perc} -controlled region was larger than $3 \text{ M}\Omega$. Moreover, we can observe that R_{perc} was at least three orders of magnitude larger than $R_{\text{ch-d}}$ and $R_{\text{ch-s}}$ in this region. This means that during the gate oxide stressing with $V_{\text{gstress}} = 3.2\text{-}3.4 \text{ V}$, V_{perc} is nearly equal to V_{gstress} , where V_{perc} is the voltage across R_{perc} . dR_{perc}/dt in the R_{perc} -controlled region was estimated to be 10^7 ohms per second (or 0.1-0.2 decades per second), indicating that a percolation path was quickly wearing out since V_{gstress} entirely dropped across the percolation path.

As shown in Fig. 5.5, the degradation of R_{perc} during the progressive breakdown gradually slowed down when R_{perc} evolved into the transition region (i.e., $20 \text{ s} < t < 100 \text{ s}$). Compared to the dR_{perc}/dt of 10^7 ohms per second in the R_{perc} -controlled region, dR_{perc}/dt in the transition region substantially reduced to the range of $10^3\text{-}10^4 \text{ }\Omega/\text{s}$. This indicates that the percolation path in the transition region experienced a relatively much slower degradation.

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Figure 5.7. General flowchart describing the interaction among various resistances in the R_{perc} -controlled, the transition and the R_{para} -controlled region.

After the initially rapid degradation of R_{perc} , V_{perc} will start to reduce when the degradation of R_{perc} reaches a point where R_{para} is no longer negligible, as compared to R_{perc} . When R_{perc} continues to degrade, the domination of R_{perc} over R_{para} will gradually disappear. It is expected that V_{perc} in the transition region will be much lower than $V_{gstress}$ as a substantial portion of $V_{gstress}$ is now redistributed across R_{para} . As a result, the reduction in V_{perc} will partially relieve the stressing across the percolation path, leading to the decrease in dR_{perc}/dt . This generates a positive feedback loop that will cause dR_{perc}/dt to gradually reduce. Fig. 5.7 shows the general flowchart describing the interaction among various resistances in the R_{perc} -controlled, the transition and the R_{para} -controlled region.

Figure 5.8. Evolution of I_g and R_{perc} at $V_g = 1.5$ V during the progressive breakdown for a n-MOSFET ($T_{ox} = 22$ Å and $L \times W = 1 \times 0.6$ μm^2) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1$ V and $I_{gl} = 1$ μA were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} .

Eventually, R_{perc} evolved into the R_{para} -controlled region, as shown in Fig. 5.5. Note that dR_{perc}/dt in the R_{para} -controlled region remained at a very low level less than 10^3 Ω/s , causing a saturation of R_{perc} to take place. The degradation of R_{perc} in this region saturates as there could be a substantially decrease in V_{perc} , meaning that the degradation of a percolation path becomes less severe. The saturation of R_{perc} in the R_{para} -controlled region, which is believed to occur as R_{perc} becomes comparable to or may be even smaller than R_{para} , is in well agreement with the saturation of I_g in the later stage of the progressive breakdown reported in Refs. [22-24].

The evolution of I_g at $V_{gstress} = 3.3$ V and R_{perc} at $V_g = 1.5$ V during the progressive breakdown for a n-MOSFET ($T_{ox} = 22$ Å and $L \times W = 1 \times 0.6$ μm^2), which was stressed

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using a two-stage CVS in inversion mode at the room temperature, are plotted together in Fig. 5.8. In the 1st-stage CVS, $V_{gstress} = 4.1$ V and $I_{gl} = 1$ μ A were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . Since I_g in the 1st-stage CVS was captured at a low I_{gl} , the initial instant of I_g in the 2nd-stage CVS would remain in the digital breakdown, as explained in *Chapter Four*. This means that the R_{perc} -controlled region starts from the digital breakdown.

Figure 5.9. General schematic describing the physical mechanisms responsible for different stages of the progressive breakdown.

For $V_{gstress}$ larger than V_{crit} , I_g will rapidly evolve from the digital breakdown into the analog breakdown. It can be observed that the R_{perc} -controlled region corresponds to a sudden, abrupt increase in I_g , which is identical to all the results of $V_{gstress}$ larger than or equal to V_{crit} shown in *Chapter Four*. Moreover, according to the study in *Section 4.4.3*, the digital breakdown will only enter into the analog breakdown when a specific level of

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I_g is reached. Therefore, the R_{perc} -controlled region can generally be understood as a region that specifies the irreversible transition of the digital breakdown into the analog breakdown, which occurs somewhere in the R_{perc} -controlled region. It has been found that the behaviors of I_g in the digital breakdown are governed by the physical properties of a percolation path. This is in good agreement with the observation that the degradation of R_{perc} in the R_{perc} -controlled region is only governed by the degradation of a percolation path. We believe that the degradation of R_{perc} in this region is mainly attributed to the change in the physical properties of a percolation path from a less conductive channel into a more conductive channel, as shown in Fig. 4.18. In summary, the measurements of R_{perc} using the PRM method allow us to understand the physical mechanisms governing the evolution of I_g during the progressive breakdown. Fig. 5.9 shows the general schematic describing the physical mechanisms responsible for different stages of the progressive breakdown.

5.5 EFFECTS OF BREAKDOWN LOCATION AND CHANNEL LENGTH ON R_{PERC} DURING PROGRESSIVE BREAKDOWN

In this section, we will focus on studying the effects of breakdown location (i.e., s_{BD}) and channel length (i.e., L) on the evolution of R_{perc} during the progressive breakdown. Since R_{ch} is evaluated in accordance with a current-separation methodology, R_{ch} is a function of s_{BD} . This further implies that s_{BD} plays a critical role in affecting the progressive breakdown [122-124, 127]. Fig. 5.10 shows the evolution of R_{perc} at $V_g = 1.5$ V with various s_{BD} during the progressive breakdown for six n-MOSFETs ($T_{\text{ox}} = 22$ Å and $L \times W = 1 \times 0.6 \mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature.

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In the 1st-stage CVS, $V_{gstress} = 4.1$ V and $I_{gl} = 1$ μ A were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . s_{BD} for these n-MOSFETs varied from 0.44L to 0.85L.

Figure 5.10. Evolution of R_{perc} at $V_g = 1.5$ V with various s_{BD} during the progressive breakdown for six n-MOSFETs ($T_{ox} = 22$ Å and $L \times W = 1 \times 0.6$ μm^2) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1$ V and $I_{gl} = 1$ μ A were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . s_{BD} for these n-MOSFETs were 0.85, 0.66, 0.49, 0.58, 0.44 and 0.77L. The inset shows an enlarged view of the R_{perc} -controlled region with $t < 20$ s.

In the R_{perc} -controlled region, the dependence of R_{perc} on s_{BD} is negligibly small, as shown in the inset of Fig. 5.10. Since R_{perc} is much larger than R_{ch} , the role of R_{ch} in affecting the degradation of R_{perc} is very minimal. As a result, in the R_{perc} -controlled region, R_{perc} is independent on s_{BD} . This implies that the degradation of R_{perc} in the R_{perc} -controlled region is merely due to a decrease in the resistances of some local defective areas within the gate oxide.

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In the R_{para} -controlled region, it can be observed that for the cases of s_{BD} closer to $0.5L$, which is the center of the device channel, the degradation of R_{perc} saturated at a higher level. Conversely, for the cases of s_{BD} closer to 0 or $1L$, which is the edge of the device channel, the saturation of R_{perc} in the R_{para} -controlled region occurred at a lower level. Since a n-MOSFET consists of a symmetric structure, $s_{\text{BD}} = yL$ is equivalent to $s_{\text{BD}} = (1 - y)L$, where y is a value between 0 and 1. For example, R_{perc} for the cases of $s_{\text{BD}} = 0.44L$ and $s_{\text{BD}} = 0.58L = 0.42L$ saturated at nearly the same level, as shown in Fig. 5.10. In the R_{para} -controlled region, the effects of R_{ch} on the evolution of R_{perc} during the progressive breakdown are no longer negligible, and thus, R_{perc} is dependent on s_{BD} . As shown in Fig. 5.1, the distance from a percolation path to the drain or source terminal will be the largest when the percolation path is situated at the center of the device channel. Therefore, a maximum of $R_{\text{ch-d}}$ or $R_{\text{ch-s}}$ would be obtained for $s_{\text{BD}} = 0.5L$, giving rise the saturation of R_{perc} at the highest level. However, as shown in Fig. 5.1, when a percolation path is getting closer to the edge of the device channel, $R_{\text{ch-d}}$ or $R_{\text{ch-s}}$ will gradually reduce, causing R_{perc} to saturate at a lower level.

The dependence of R_{perc} on s_{BD} for breakdown n-MOSFETs that possess $L = 0.5$ and $0.3 \mu\text{m}$ are shown in Figs. 5.11(a) and 5.11(b), respectively. For comparison, these n-MOSFETs consist of the same T_{ox} (i.e., $22 \text{ \AA}$) and W (i.e., $0.6 \mu\text{m}$). The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 5.10. It can still be observed that the saturation of R_{perc} in the R_{para} -controlled region for s_{BD} closer to $0.5L$ occurred at a level higher than that closer to 0 or $1L$. However, the dependence of R_{perc} on s_{BD} in the R_{para} -controlled region becomes weaker with decreasing L . We believe that the effects of $R_{\text{ch-d}}$ or $R_{\text{ch-s}}$ at various s_{BD} on the progressive breakdown will gradually

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diminish as L is getting smaller and/or becomes comparable to the effective diameter of a percolation path. This has an important post-breakdown reliability implication that the significance of s_{BD} in controlling the progressive breakdown in a larger n-MOSFET may gradually disappear when L is largely scaled down, especially in standard sub-90-nm CMOS technology [120-122, 125].

Figure 5.11. Evolution of R_{perc} at $V_g = 1.5$ V with various s_{BD} during the progressive breakdown for n-MOSFETs that possess $L =$ (a) 0.5 and (b) $0.3 \mu m$. Other device dimensions of these n-MOSFETs are the same (i.e., $T_{ox} = 22 \text{ \AA}$ and $W = 0.6 \mu m$). The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 5.10. In (a), the n-MOSFETs were associated with $s_{BD} = 0.35, 0.24$ and $0.52L$. In (b), the n-MOSFETs were associated with $s_{BD} = 0.55, 0.42, 0.71$ and $0.27L$. The insets in (a) and (b) show the enlarged views of the R_{perc} -controlled region with $t < 20$ s.

Besides s_{BD} , R_{ch} is also a function of L , and thus, the study of the role of L in governing the progressive breakdown is necessary. Fig. 5.12 shows the evolution of R_{perc} at $V_g = 1.5$ V during the progressive breakdown for all the n-MOSFETs in Figs. 5.9, 5.10(a) and 5.10(b), which are associated with $L = 1$ (i.e., the black symbols), 0.5 (i.e., the green symbols) and $0.3 \mu m$ (i.e., the blue symbols), respectively. In general, the saturation

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of R_{perc} in the R_{para} -controlled region took place at a lower level with decreasing L . Fig. 5.13 shows the evolution of R_{perc} at $V_g = 1.5$ V during the progressive breakdown for three of the cases in Fig. 5.12, which are (1) $s_{\text{BD}} = 0.77L = 0.23L$ for $L = 1 \mu\text{m}$, (2) $s_{\text{BD}} = 0.24L$ for $L = 0.5 \mu\text{m}$, and (3) $s_{\text{BD}} = 0.27L$ for $L = 0.3 \mu\text{m}$. These cases correspond to nearly the same s_{BD} of 0.23-0.27 L . In the previous discussion, we know that s_{BD} is vital in controlling the progressive breakdown. Thus, s_{BD} is kept as a constant such that the effects of L on the progressive breakdown can be decoupled from that of s_{BD} .

Figure 5.12. Evolution of R_{perc} at $V_g = 1.5$ V during the progressive breakdown for all the n-MOSFETs in Figs. 5.9, 5.10(a) and 5.10(b), which are associated with $L = 1$ (i.e., the black symbols), 0.5 (i.e., the green symbols) and $0.3 \mu\text{m}$ (i.e., the blue symbols), respectively.

As shown in the inset of Fig. 5.13, due to the domination of R_{perc} over R_{ch} , the degradation of R_{perc} in the R_{perc} -controlled region is very weakly dependent on L . However, in the R_{para} -controlled region, R_{perc} saturated at a lower level with decreasing L . Generally, the decrease in L will lead to a decrease in $R_{\text{ch-d}}$ or $R_{\text{ch-s}}$ if s_{BD} is fixed. As a result, R_{perc} for a

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breakdown n-MOSFET with a smaller L will saturate at a lower level. Furthermore, it can be observed that the dependence of R_{perc} on L in the R_{para} -controlled region becomes weaker when L decreases. This is in well agreement with the previous observation on Fig. 5.11(b) for which the progressive breakdown for a very narrow n-MOSFET could be independent on L .

Figure 5.13. Evolution of R_{perc} at $V_g = 1.5$ V during the progressive breakdown for three of the cases in Fig. 5.12, which are (1) $s_{\text{BD}} = 0.77L = 0.23L$ for $L = 1$ μm , (2) $s_{\text{BD}} = 0.24L$ for $L = 0.5$ μm , and (3) $s_{\text{BD}} = 0.27L$ for $L = 0.3$ μm . Note that s_{BD} for these cases remained nearly the same at $0.23\text{--}0.27L$. The inset shows an enlarged view of the R_{perc} -controlled region with $t < 20$ s.

5.6 TEMPERATURE DEPENDENCE OF R_{PERC} DURING PROGRESSIVE BREAKDOWN

Fig. 5.14(a) shows the temperature dependence of R_{perc} at $V_g = 1.5$ V from the R_{perc} -controlled region to the R_{para} -controlled region for a breakdown n-MOSFET ($T_{\text{ox}} = 20$ Å

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and $L \times W = 0.5 \times 0.6 \mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \mu\text{A}$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.2 V without setting any limit on I_{gl} . At each instant of the progressive breakdown, R_{perc} at $V_g = 1.5 \text{ V}$ was measured at four different temperatures, which were 25, 60, 100 and 150 °C. In general, R_{perc} reduced with increasing temperatures, indicating that the conduction mechanism responsible for the flow of I_g through the percolation path during the progressive breakdown could be a thermally-activated process. It can be noticed that R_{perc} in the R_{perc} -controlled region decreased with a faster rate with increasing temperatures, as compared to those in the R_{para} -controlled region. Fig. 5.14(b) shows the evolution of the activation energy (i.e., E_a) associated with R_{perc} during the progressive breakdown for the n-MOSFET in Fig. 5.14(a). At each instant of the progressive breakdown, E_a can be calculated from the slope of the Arrhenius plot of R_{perc} shown in Fig. 5.14(a). In the R_{perc} -controlled region, E_a rapidly decreased from 0.23 eV to 0.12 eV. However, E_a in the R_{para} -controlled region remained nearly unchanged at 0.05 eV. This means that the dependence of R_{perc} on temperatures has been largely reduced when the progressive breakdown evolves from the R_{perc} -controlled region into the R_{para} -controlled region. The difference between E_a in the R_{perc} - and the R_{para} -controlled region may signify that the microscopic nature of a percolation path could grow from one phase into another. This implies that different physical mechanisms could be involved in governing different stages of the progressive breakdown.

Defects that are accumulated within the gate oxide and trigger the occurrence of a dielectric breakdown event are believed similar to those that are responsible for the behaviors of I_g in the early stage of the progressive breakdown [107, 108].

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(a)

(b)

Figure 5.14. (a) Temperature dependence of R_{perc} at $V_g = 1.5$ V during the progressive breakdown for a n-MOSFET ($T_{\text{ox}} = 20$ Å and $L \times W = 0.5 \times 0.6$ μm^2) stressed using a two-stage CVS in inversion mode in the room temperature. In the 1st-stage CVS, $V_{g\text{stress}} = 3.8$ V and $I_{gl} = 10$ μA were used. In the 2nd-stage CVS, $V_{g\text{stress}}$ was reduced to 3.2 V without setting any limit on I_{gl} . At each instant of the progressive breakdown, R_{perc} at $V_g = 1.5$ V was measured at 25, 60, 100 and 150 °C. (b) Evolution of E_a during the progressive breakdown for the n-MOSFET in (a).

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Our results suggest that the degradation of R_{perc} in the R_{perc} -controlled region, which corresponds to the early stage of the progressive breakdown, is independent on breakdown location and device dimensions. This implies that the degradation of R_{perc} in the R_{perc} -controlled region could be primarily governed by the molecular properties of defects in the vicinity of the percolation path, as described in *Chapter Four*. In the early stage of the progressive breakdown, the physical structure of the percolation path is believed still remaining in a very unstable initial state. This has been discussed in details in *Chapter Four*. Therefore, the degradation of R_{perc} in the early stage of the progressive breakdown may be largely attributed to the creation of more defects [115] in the vicinity of the percolation path.

We believe that a relatively stable silicon-like percolation path, which is shown in Fig. 4.18(b), will be formed in the R_{para} -controlled region, and it is responsible for the behaviors of I_g in the analog breakdown. The detailed discussion will be given in the following section. Thus, the degradation of R_{perc} in the R_{para} -controlled region is relatively less dependent on temperatures. It is believed that the conduction mechanism responsible for the flow of I_g through the percolation path in the R_{para} -controlled region could be further complicated by the presence of various physical damages, such as DBIE [109, 111-116].

5.7 VOLTAGE DEPENDENCE OF R_{PERC} DURING PROGRESSIVE BREAKDOWN

From Fig. 5.4(a), R_{perc} at $V_g = 1.5$ V is nearly identical to R_g . With the capability of monitoring R_{perc} and R_{ch} based on the PRM method, we can provide evidence that R_{perc}

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acts as a dominating resistance that contributes to R_g at a low V_g . Fig. 5.15 shows the evolution of R_{perc} at various V_g during the progressive breakdown for a n-MOSFET ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{g\text{stress}} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$ were used. In the 2nd-stage CVS, $V_{g\text{stress}}$ was reduced to 3.4 V without setting any limit on I_{gl} .

Figure 5.15. Evolution of R_{perc} at $V_g = 1.2, 1.4, 1.6$ and 1.8 V during the progressive breakdown for a n-MOSFET ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{g\text{stress}} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$ were used. In the 2nd-stage CVS, $V_{g\text{stress}}$ was reduced to 3.4 V without setting any limit on I_{gl} .

It can be observed that R_{perc} at one particular instant of the progressive breakdown decreased with increasing V_g , implying that R_{perc} is a function of V_g , and hence, the degradation of a percolation path during the progressive breakdown is voltage-dependent.

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An exponential relationship between R_{perc} and V_g can be established for one particular instant of the progressive breakdown, that is

$$R_{perc} = A \times \exp(-B \times V_g) \quad (5.9)$$

where A and B are two fitting parameters.

Assume that Eqn. (5.9) is valid for a high V_g . Fig. 5.16 shows the measured and the extrapolated ($R_{perc} + R_{poly}$) at different instants of the progressive breakdown for the n-MOSFET in Fig. 5.15. The measured ($R_{perc} + R_{poly}$) at a low V_g (i.e., 1-1.5 V) in the R_{perc} - and the R_{para} -controlled region are shown in the dotted circle. Note that the measured ($R_{perc} + R_{poly}$) were calculated using the PRM method. In addition, the extrapolated ($R_{perc} + R_{poly}$) at a high V_g (i.e., 2-3.5 V) equivalent to the range of $V_{gstress}$ in the R_{perc} - and the R_{para} -controlled region are shown in the dotted square. Note that the extracted ($R_{perc} + R_{poly}$) were obtained through the extrapolation of the measured ($R_{perc} + R_{poly}$) based on Eqn. (5.9). R_{ch} , which is assumed to be linearly dependent on V_g , is included for comparison.

It is found that at $V_g = 2-3.5$ V, the extrapolated ($R_{perc} + R_{poly}$) in the R_{para} -controlled region is in the range of $10^2-10^5 \Omega$, which is equal to or even smaller than R_{ch} . At a low V_g , R_{perc} is high, implying that V_{perc} is nearly equal to V_g . As shown in Fig. 5.16, since R_{perc} is predicted to be comparable to R_{ch} at a high V_g , $V_{gstress}$ will be redistributed across R_{perc} and R_{ch} , and hence, only a portion of $V_{gstress}$ will drop across R_{perc} . This means that V_{perc} is much smaller than $V_{gstress}$ during the gate oxide stressing with a high V_g . Hence, the extrapolated ($R_{perc} + R_{poly}$) at $V_g = 2.5-3.0$ V serves as a better estimation for R_{perc} during the gate oxide stressing with $V_{gstress} = 3-3.5$ V. As R_{perc} continues to decrease with increasing stressing time, V_{perc} will gradually decrease, leading to a further decrease

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in dR_{perc}/dt . According to Thevenin's Theorem, the equivalence of the supply resistances (i.e, output resistances) and the load resistance will lead to the maximum power transfer. Therefore, at a given V_g , when R_{perc} (which can be treated as the load resistance) becomes comparable to R_{para} (which can be treated as the supply resistance), a maximum power dissipation will take place. It is believed that this large dissipated power will trigger significant local heating effects in the vicinity of the percolation path. Consequently, this will cause catastrophic failure, which possibly involves severe, irreversible microstructure damages, such as DBIE [109, 111-116], to occur.

Figure 5.16. Measured and extracted ($R_{\text{perc}} + R_{\text{poly}}$) versus V_g in the R_{perc} - and the R_{para} -controlled region for the n-MOSFET in Fig. 5.15. The dotted circle at $V_g = 1-1.5$ V includes the measured ($R_{\text{perc}} + R_{\text{poly}}$), which were calculated using the PRM method. On the other hand, the dotted square at $V_g = 2-3.5$ V includes the extrapolated ($R_{\text{perc}} + R_{\text{poly}}$), which were obtained through the extrapolation of the measured ($R_{\text{perc}} + R_{\text{poly}}$) based on Eqn. (5.9). R_{ch} , which is assumed to be linearly dependent on V_g , is included for comparison. The black symbols refer to ($R_{\text{perc}} + R_{\text{poly}}$), while the blue symbols refer to R_{ch} . It can be noticed that ($R_{\text{perc}} + R_{\text{poly}}$) and R_{ch} become comparable with each other at a high V_g .

5.8 SCHOTTKY-LIKE BEHAVIOR RESPONSIBLE FOR CONDUCTION MECHANISMS IN ANALOG BREAKDOWN

Fig. 5.17 shows the $I_{sub}-V_g$ characteristics in the R_{perc} -controlled, the transition and the R_{para} -controlled region for a breakdown n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . Note that the $I_{sub}-V_g$ characteristics for the n-MOSFET were measured in accumulation mode.

Figure 5.17. $I_{sub}-V_g$ characteristics in the R_{perc} -controlled, the transition and the R_{para} -controlled region for a breakdown n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) stressed using a two stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . Note that the $I_{sub}-V_g$ characteristics for the n-MOSFET were measured in accumulation mode.

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Figure 5.18. (a) TEM micrograph of a breakdown n-MOSFET in the transition and the R_{para} -controlled region. DBIE can be observed at the p-type silicon substrate [109, 111-116]. It is believed that the percolation path is situated on top of DBIE. **(b)** General schematic showing the postulated field-emission (i.e., the n⁺-type polycrystalline-silicon gate/percolation path contact) and thermionic-emission barrier (i.e., the percolation path/p-type silicon substrate contact) in the vicinity of the percolation path.

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This study focuses on accumulation mode such that the effects induced by the presence of the device channel are minimized. The preliminary observations of Fig. 5.17 are summarized as follows:

- In the R_{perc} -controlled region, the $I_{\text{sub}}-V_g$ characteristics for the n-MOSFET do not follow any specific trend.
- In the transition region, a linear region starts to appear at V_g below 0.7 V in the $I_{\text{sub}}-V_g$ characteristics for the n-MOSFET.
- In the R_{para} -controlled region, the $I_{\text{sub}}-V_g$ characteristics for the n-MOSFET, which consist of a relatively apparent linear region at V_g below 0.4 V, exhibit a *Schottky*-like behavior.

Therefore, a *Schottky*-like barrier could exist and play an important part in governing the conduction mechanisms in the transition and the R_{para} -controlled region. Fig. 5.18(a) shows a typical example for the transmission-electron microscopic (TEM) image of a breakdown n-MOSFET in the transition and the R_{para} -controlled region. The presence of DBIE in the p-type silicon substrate can be observed, and it is believed that the percolation path is situated on top of DBIE [109, 111-116]. Similar TEM results are consistently seen in various T_{ox} [109, 111-116]. Due to the presence of the heavily-doped n^+ -type polycrystalline-silicon gate, the percolation path/ n^+ -type polycrystalline-silicon gate contact is postulated to be associated with a field-emission barrier. The percolation path/p-type silicon substrate contact is postulated to be associated with a thermionic-emission barrier, which is responsible for the *Schottky*-like behavior of the $I_{\text{sub}}-V_g$ characteristics for a breakdown n-MOSFET in accumulation mode. Fig. 5.18(b) is a general schematic showing these two possible barriers in the vicinity of the percolation

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path. The *Schottky*-diode equation seems to provide a good approximation on the $I_{sub}\text{-}V_g$ characteristics for a breakdown n-MOSFET in accumulation mode obtained from the experiments [144, 145]:

$$I_{sub} = A_{perc} A^{**} T^2 \exp\left(\frac{-\phi_{sub}}{kT}\right) \exp\left(\frac{qV_g}{n_{sub} kT}\right) \tag{5.10}$$

where A_{perc} is the cross-sectional area of the percolation path, $A^{**} = 32 \text{ Acm}^{-2}\text{K}^{-2}$ is the effective Richardson constant for the p-type silicon substrate, and k is the Boltzmann constant.

Figure 5.19. Evolution of n_{sub} and n_g during the progressive breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ }\mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ }\mu\text{A}$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 3.3 V without setting any limit on I_{gl} . n_{sub} and n_g are the ideality factor extracted from the $I_{sub}\text{-}V_g$ and the $I_g\text{-}V_g$ curve for the n-MOSFET in accumulation mode, respectively. As compared to n_g , n_{sub} , which varied from 1.3 to 1.7, is closer to 1, meaning that I_{sub} is governed by a more ideal *Schottky*-like barrier.

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The ideality factor and the effective barrier height at one particular instant of the progressive breakdown, which are indicated as n_{sub} and ϕ_{sub} in Eqn. (5.10), respectively, can be extracted. In the later section, we will present that the extraction of n_{sub} and ϕ_{sub} from the $I_{\text{sub}}-V_g$ characteristics for a breakdown n-MOSFET in accumulation mode provides an indirect but useful approach to study the effective “growth” of a percolation path in affecting the conduction mechanisms governing the later stage of the progressive breakdown, in which this is physically invisible in the conventional bright-field TEM images.

Fig. 5.19 shows the evolution of ideality factors (i.e., n_{sub} and n_g) during the progressive breakdown for a n-MOSFET ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ }\mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at room temperature. In the 1st-stage CVS, $V_{g\text{stress}} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ }\mu\text{A}$ were used. In the 2nd-stage CVS, $V_{g\text{stress}}$ was reduced to 3.3 V without setting any limit on I_{gl} . n_{sub} and n_g are the ideality factor extracted from the $I_{\text{sub}}-V_g$ and the I_g-V_g curve for the n-MOSFET in accumulation mode, respectively. The ideality factor, which relate to the slope of the linear region in the $I-V$ curve, strongly suggests the existence of a *Schottky*-like barrier in controlling the post-breakdown $I-V$ characteristics in the transition and the R_{para} -controlled region. As compared to n_g , n_{sub} varied from 1.3 to 1.7. For an ideal *Schottky* diode, the ideality factor is close to 1, meaning that the thermionic current is dominant at a low-voltage regime. When the ideality factor is in the range of 1 and 2, the surface generation-recombination current starts to be dominant at a high-voltage regime, and a *Schottky* diode is considered as non-ideal. The corresponding structure is no longer classified as a *Schottky* diode if the ideality factor is larger than 2. Since n_{sub} is closer to 1, I_{sub} is governed by a more ideal *Schottky*-like barrier. Note that I_g

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could be convoluted with I_s or I_d . Fig. 5.20 shows the flow of I_g , I_s , I_d and I_{sub} at one particular instant of the progressive breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) associated with $s_{BD} = 0.76L$ by sweeping V_g from 0 V to -1.1 V and setting $V_d = V_s = V_{sub} = 0$. It can be observed that I_g was mainly constituted by I_{sub} and I_d at a low V_g .

Figure 5.20. Flow of I_g , I_s , I_d and I_{sub} at one specific instant of the progressive breakdown for a n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$) associated with $s_{BD} = 0.76L$, where V_g was swept from 0 V to -1.1 V and $V_d = V_s = V_{sub} = 0$. Note that $I_g \cong I_{sub} + I_d$ at a low V_g , meaning that the linear region of I_g was affected by the presence of I_d .

Due to a smaller channel resistance, the effects of I_s or I_d on I_g will be more significant when the percolation path is located closer to the source or drain terminal of a breakdown n-MOSFET. This could happen when either the percolation path dilates and grows towards the source or drain terminal of the n-MOSFET [115], or the dopants at the source

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or drain terminal of the n-MOSFET are thermally redistributed and diffuse towards the percolation path.

At the beginning of the R_{perc} -controlled region, it is believed that the percolation path is associated with an unstable physical structure, corresponding to n_{sub} much larger than 2. The R_{perc} -controlled region will evolve into the transition region as the percolation path is rapidly worn-out and transformed from an unstable state into a relatively stable state. This results in n_{sub} of around 1.7. In the R_{para} -controlled region, n_{sub} generally remained in the range of 1.3-1.7, confirming the presence of a stable percolation path. As a whole, the results suggest that a percolation path associated with a relatively stable *Schottky*-like barrier only appears in the later stage of the progressive breakdown, that is, the saturation of I_g .

Fig. 5.21 shows the evolution of n_{sub} with various s_{BD} during the progressive breakdown for six n-MOSFETs ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$). The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 5.19. It can be observed that n_{sub} for the cases of $s_{\text{BD}} = 0.88, 0.39, 0.23$ and $0.52L$ remained in the range of 1.3-1.7. This implies that n_{sub} is independent on s_{BD} . Since n_{sub} corresponds to the *Schottky*-like behavior of the contact between the percolation path and the p-type silicon substrate, the results are in good agreement with the understanding that n_{sub} should be a very weak function of s_{BD} . However, for the cases of $s_{\text{BD}} = 0.01$ and $0.98L$, where the percolation path is situated very close to the source or drain terminal of the n-MOSFET, n_{sub} fluctuated between 1.6 and 2, indicating that the non-ideal *Schottky* characteristics are due to the influence of I_s or I_d . It is expected that the cases of $s_{\text{BD}} = \sim 0$ or $\sim 1L$ will not show any *Schottky*-like behaviors as both the n^+ -type polycrystalline-silicon gate and the

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source or drain terminal will produce contacts that are governed by the field emission. This suggests that the post-breakdown conduction mechanisms are affected by the close proximity between a percolation path and the source or drain terminal of a n-MOSFET.

Figure. 5.21. Evolution of n_{sub} with various s_{BD} during the progressive breakdown for six n-MOSFETs ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$). The stressing conditions applied to these n-MOSFETs were similar to those in Fig. 5.19. The results show that n_{sub} is generally independent on s_{BD} . The red symbols refer to the cases of s_{BD} very close to the source or drain terminal of the n-MOSFET (i.e., $s_{BD} = 0.98$ and $0.01L$).

The *Schottky*-like behavior has been further confirmed by studying the temperature effects on the I_{sub} - V_g characteristics for a breakdown n-MOSFET in accumulation mode. Rearranging Eqn. (1), the saturation current can be obtained as [144, 145]

$$I_{sat} = A_{perc} A^{**} T^2 \exp\left(\frac{-\phi_{sub}}{kT}\right) = \frac{I_{sub}}{\exp\left(\frac{qV_g}{n_{sub}kT}\right)} \quad (5.11)$$

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Fig. 5.22 shows the evolution of the effective barrier heights (i.e., ϕ_{sub}) in the R_{perc} -controlled, the transition and the R_{para} -controlled region for a breakdown n-MOSFET ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ }\mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{\text{gstress}} = 4 \text{ V}$ and $I_{\text{gl}} = 1 \text{ }\mu\text{A}$ were used. In the 2nd-stage CVS, V_{gstress} was reduced to 3.4 V without setting any limit on I_{gl} . The $I_{\text{sub}}\text{-}V_g$ characteristics at each instant of the progressive breakdown for the n-MOSFET in accumulation mode were measured at various temperatures from 298 K to 353 K, as shown in the inset of Fig. 5.22.

Figure 5.22. Evolution of ϕ_{sub} in the R_{perc} -controlled, the transition and the R_{para} -controlled region for a breakdown n-MOSFET ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ }\mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. In the 1st-stage CVS, $V_{\text{gstress}} = 4 \text{ V}$ and $I_{\text{gl}} = 1 \text{ }\mu\text{A}$ were used. In the 2nd-stage CVS, V_{gstress} was reduced to 3.4 V without setting any limit on I_{gl} . At each instant of the progressive breakdown, the $I_{\text{sub}}\text{-}V_g$ characteristics for the n-MOSFET in accumulation mode were measured at various temperatures, which are 298, 313, 333 and 353 K, as shown in the inset. ϕ_{sub} is equivalent to the slope of the (I_{sat}/T^2) versus $(1/kT)$ relationship, which can be obtained from Eqn. (5.11) for V_g below 0.6 V.

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ϕ_{sub} is equivalent to the slope of the (I_{sat} / T^2) versus $(1 / kT)$ relationship, which can be obtained from Eqn. (5.11) for V_g below 0.6 V [141, 145]. In the R_{perc} -controlled and the transition region with n_{sub} larger than 1.7, the extraction of ϕ_{sub} may be invalid. However, the results are included for comparison. On the other hand, during the evolution of the transition region into the R_{para} -controlled region with $n_{\text{sub}} = 1.3$ -1.7, ϕ_{sub} reduced from 0.6 eV to 0.4 eV. Assume that the percolation path is associated with an ideal cylindrical shape. We have $A_{\text{perc}} = \pi D_{\text{perc}}^2 / 4$, where D_{perc} defines the effective diameter of a percolation path. Based on Eqn. (5.11), D_{perc} at a specific temperature is estimated to be in the range of 9-17 nm. It has been proposed that the diameter of a percolation path formed in the early stage of the progressive breakdown is 1-4 nm [12]. When the R_{perc} -controlled region evolves into the transition and the R_{para} -controlled region, D_{perc} increases from 1-4 nm to 9-17 nm, signifying that the percolation path dilation could take place during the progressive breakdown [115]. We believe that ϕ_{sub} and D_{perc} interplay with each other to control the conduction mechanisms in the later stage of the progressive breakdown. The increase in D_{perc} could be due to the generation of more defects within the gate oxide in the vicinity of the percolation path, while the lowering of ϕ_{sub} could be due to a change in the material properties of the percolation path.

It is believed that the large energy bandgap of silicon oxynitride in the vicinity and within the percolation path has been collapsed in the transition and the R_{para} -controlled region with n_{sub} in the range of 1.3-1.7. The ϕ_{sub} of 0.4-0.6 eV could correspond to the barrier heights for holes to travel from the valence band of the p-type silicon substrate to n^+ -type polycrystalline-silicon gate. The lowering of ϕ_{sub} during the progressive breakdown, as shown in Fig. 5.22, can be approximated using the following formula:

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$$\phi_{sub} = kT \left[\ln \left(\frac{n_{poly}}{n_i} \right) + \ln \left(\frac{P_{sub}}{n_i} \right) \right] \quad (5.12)$$

where n_{poly} is the donor concentration of the polycrystalline-silicon gate, and p_{sub} is the acceptor concentration of the silicon substrate. The change in ϕ_{sub} is governed by n_{poly} and p_{sub} , that is, the adjustment of the Fermi level of the polycrystalline-silicon gate and the silicon substrate, which are defined as $E_{F(gate)}$ and $E_{F(sub)}$, respectively. Due to the presence of substantial heating effects in the vicinity of the percolation path [109, 110, 114] during the progressive breakdown, it is possible that the dopants at the silicon substrate in the vicinity of the percolation path may diffuse out from the breakdown spot. Note that the dopant concentration gradient gently reduces from the silicon surface to the silicon substrate. This will lead to a local decrease in p_{sub} . As a result, $E_{F(sub)}$ close to the interface of silicon oxynitride will be moved towards the intrinsic energy level, causing ϕ_{sub} to reduce.

5.9 EXISTENCE OF HIGH LOCAL TEMPERATURE IN VICINITY OF PERCOLATION PATH

As discussed above, it is believed that D_{perc} is dynamic during the progressive breakdown, meaning that the percolation path could dilate or grow along the device channel during the progressive breakdown [115]. Assume that the percolation path is a conductive channel associated with R_{perc} , which can be calculated based on the PRM method. Then, the relationship between R_{perc} and D_{perc} can be described as

$$R_{perc} = \frac{\rho_{perc} T_{ox}}{A_{perc}} = \frac{4\rho_{perc} T_{ox}}{\pi D_{perc}^2} \quad (5.13)$$

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where ρ_{perc} is the effective resistivity of the percolation path. For simplicity, we consider the case for which the percolation path consists of an ideal cylindrical shape. Moreover, the following assumptions are made:

- In the R_{perc} -controlled region, D_{perc} is assumed to be a constant parameter, but ρ_{perc} degrades with increasing stressing time. As discussed earlier, the degradation of R_{perc} in the R_{perc} -controlled region is merely attributed to the rapid wear out of a percolation path. Due to a material property change, a percolation path in this region is quickly transformed from a less conductive channel into a more conductive channel, implying a decrease in ρ_{perc} .
- In the R_{para} -controlled region, ρ_{perc} is assumed to be a constant parameter, but D_{perc} evolves with increasing stressing time. The possible occurrence of percolation path dilation in the R_{para} -controlled region has been discussed in details in the previous section for which D_{perc} can evolve from 1-4 nm to 9-17 nm. In addition, the lowering of ϕ_{sub} indicates that a change in the material properties of the percolation path could occur in this region. But for simplicity, we assume that ρ_{perc} remains unchanged.

Fig. 5.23(a) shows the evolution of D_{perc} during the progressive breakdown for the n-MOSFET in Fig. 5.4. For a given set of R_{perc} calculated using the PRM method at $V_g = 1.5$ V, D_{perc} can be obtained based on Eqn. (5.13). It can be noticed that in the R_{para} -controlled region, D_{perc} increased during the progressive breakdown and was larger than 8 nm after 500 s. D_{perc} estimated using Eqn. (5.13) is in the same range with that using Eqn. (5.11), which is 9-17 nm.

Knowing R_{perc} and D_{perc} , the heat generation rate at one specific instant of the progressive breakdown can be calculated as

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$$H_{gen} = \frac{P_{perc}}{v_{perc}} = \frac{4I_g^2 R_{perc}}{\pi D_{perc}^2 T_{ox}} \quad (5.14)$$

where P_{perc} defines the power dissipated from the percolation path, and v_{perc} defines the volume of the percolation path. Eqn. (5.14) is only a simplified way in demonstrating the significant local heating effects in the vicinity of the percolation path and the dilation of the percolation path during the progressive breakdown. Note that the percolation path is not an ideal resistor, and the ballistic transport of charge carriers through the percolation path is not considered. Fig. 5.23(b) shows the evolution of H_{gen} during the progressive breakdown for the n-MOSFET in Fig. 5.4, which is estimated in accordance with Eqn. (5.14) from R_{perc} and D_{perc} in Fig. 5.23(a). In the R_{para} -controlled region, which corresponds to the saturation of R_{perc} in the later stage of the progressive breakdown, the estimated H_{gen} are about one to two orders of magnitude higher than the results reported in Ref. [146], which are about 10^{19} J/s.m³. One of the possible reasons is that D_{perc} is underestimated. According to Pey *et al.* [115], the dilation of the percolation path should be strongly skewed towards the closer source or drain terminal of a breakdown n-MOSFET instead of evolving with an ideal cylindrical shape. Therefore, D_{perc} calculated using Eqn. (5.13) are possibly underestimated, leading to an overestimation of H_{gen} . In addition, the assumptions on D_{perc} and ρ_{perc} in the R_{perc} - and the R_{para} -controlled region could be overly simplified. As described in *Chapter Four*, a percolation path could be a silicon-like conductive channel due to the kicking-out of oxygen atoms from the local defective areas within the gate oxide. Thus, ρ_{perc} is assumed to be the resistivity of silicon. Despite of these simplifications, the results shown in Fig. 5.23 still give us information on the relationship between R_{perc} , D_{perc} and H_{gen} .

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Figure 5.23. Evolution of (a) D_{perc} and (b) H_{gen} during the progressive breakdown for the n-MOSFET ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.6 \text{ \mu m}^2$) in Fig. 5.4. For a given set of R_{perc} calculated using the PRM method at $V_g = 1.5 \text{ V}$, D_{perc} can be obtained based on Eqn. (5.13). Moreover, H_{gen} is estimated in accordance with Eqn. (5.14) from R_{perc} and D_{perc} in (a).

As reported in Ref. [110], the temperature profile in Kelvin for a breakdown n-MOSFET with $T_{\text{ox}} = 20 \text{ \AA}$ and $L = 0.13 \text{ \mu m}$ was simulated using ANSYS, which is a finite-element-analysis simulator. A silicon-like percolation path with the diameter of 8 nm, which served as a heat source, was placed at the center of the device channel. With $H_{\text{gen}} = 10^{19} \text{ J/s.m}^3$, a high local temperature in the vicinity of the percolation path, which

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could exceed the silicon melting point (i.e., $\sim 1410^\circ\text{C}$), can be observed after a 10-ms breakdown transient. Since the power dissipation in the ultrathin gate oxide during the progressive breakdown will experience a sudden increase and reach a steady state within the range of microseconds at a high $V_{gstress}$ [146]; thus, a breakdown transient in the order of milliseconds was used in Ref. [110].

Infrared photoemission microscopy (IRPEM) technique, which is sensitive to the heat emission, was used to demonstrate the existence of substantial local heating effects in a breakdown n-MOSFET. Figs. 5.24(b)-(e) show the IRPEM images at different stages of the progressive breakdown for a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.3 \times 0.3 \text{ }\mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \text{ }\mu\text{A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3.1 \text{ V}$ and $I_{gl} = 50, 100$ and $300 \text{ }\mu\text{A}$ were used in the 2nd-stage CVS. Additionally, Fig. 5.24(f) shows the optical image for the n-MOSFET. Fig. 5.24(a) shows the IRPEM image for the n-MOSFET before the gate oxide stressing was carried out. Note that no bright spot (i.e., infrared photoemission) was detected for a fresh n-MOSFET. Figs. 5.24(b), 5.24(c) and 5.24(d) show the IRPEM images for the n-MOSFET experiencing a soft breakdown at $I_{gl} = 10, 50$ and $100 \text{ }\mu\text{A}$, respectively. The soft breakdown was identified by the transistor-like post-breakdown I_d - V_d characteristics of the n-MOSFET. Different from Fig. 5.24(a), a bright spot can be consistently observed after the occurrence of a dielectric breakdown event. The infrared photoemission is indirectly related to the phonon-related emission. Therefore, it is believed that the presence of a bright spot created by the infrared photoemission in a breakdown n-MOSFET is mainly due to the substantial local heating effects in the vicinity of the percolation path.

Figure 5.24. IRPEM images for a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.3 \times 0.3 \text{ }\mu\text{m}^2$) at different stages of the progressive breakdown. The n-MOSFET was stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \text{ }\mu\text{A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3.1 \text{ V}$ and $I_{gl} = 50, 100$ and $300 \text{ }\mu\text{A}$ were used in the 2nd-stage CVS. (a) IRPEM image obtained before the occurrence of a dielectric breakdown event. (b), (c), (d), (e) IRPEM image obtained at $I_{gl} = 10, 50, 100$ and $300 \text{ }\mu\text{A}$, respectively. $I_{gl} = 10, 50$ and $100 \text{ }\mu\text{A}$ correspond to a soft breakdown, while $I_{gl} = 300 \text{ }\mu\text{A}$ corresponds to a hard breakdown. (f) Optical image for the n-MOSFET.

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This could be induced by the strong flow of I_g through the percolation path. Clearly, the size of the bright spot would grow when I_{gl} increased from 10 μA to 50 μA , and then to 100 μA . This implies that the local heating effects in a breakdown n-MOSFET become more significant when the progressive breakdown evolves into a higher leakage level. Furthermore, Fig. 5.24(e) shows the IRPEM image for the n-MOSFET experiencing a hard breakdown at $I_{gl} = 300 \mu\text{A}$. The hard breakdown was identified by the resistor-like post-breakdown I_d - V_d characteristics of the n-MOSFET. It can be observed that the bright spot grew to a considerably huge size, which is even much larger than the device area. For a hard breakdown, the local heating effects in a breakdown n-MOSFET could be very severe and laterally spread out, causing severe microstructure damages, such as contact burn and metal migration from the silicides at the source or drain terminal of a breakdown n-MOSFET [116], to occur. In brief, the IRPEM results suggest that a high local temperature in the vicinity of the percolation path exist, and will increase and spread out from the percolation path during the progressive breakdown.

5.10 DOPANT REDISTRIBUTION DUE TO SUBSTANTIAL LOCAL HEATING EFFECTS IN VICINITY OF PERCOLATION PATH

The existence of a high local temperature in the vicinity of a percolation path will cause the dielectric-breakdown-induced dopant redistribution to occur. As shown in Fig. 5.25, when the dopants at the source or drain terminal are redistributed, the distance between the percolation path and the source or drain terminal will decrease. As discussed in the previous section, s_{BD} serves as one of the vital parameters in controlling the later stage of the progressive breakdown. Therefore, the dopant redistribution is a physical mechanism

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that must be thoroughly studied in order to have further understandings on the progressive breakdown.

A catastrophic breakdown will occur as the distance between the percolation path and the source or drain terminal is equal to zero, implying that the gate electrode is electrically shorted with the source or drain terminal [18, 19, 141, 142]. Similar to the punch-through phenomenon, the dopant redistribution will cause the distance between the local depletion region of the source and the drain terminal to reduce, resulting in a local channel short [147]. This will completely degrade the device performance. The local channel short can be identified when both the post-breakdown I_d-V_d and I_s-V_s characteristics of a breakdown n-MOSFET behave resistor-like but the corresponding TEM images may show no physical damages or physical damages at only the source or drain terminal [116].

In general, we believe that the dielectric-breakdown-induced dopant redistribution in a n-MOSFET will more readily occur at areas that are situated close to the vicinity of the percolation path, as shown in Fig. 5.25. This is mainly due to the fact that the temperature distribution in the whole device structure is non-uniform, in which the temperature gradient will decreasingly evolve from the center of the percolation path to the surrounding areas. If the percolation path is situated at the center of the device channel, the dopant redistribution at the source or drain terminal will be more likely symmetric with each other. On the other hand, if the percolation path is situated close to the source terminal, the dopant redistribution at the source terminal will be more severely affected, as compared to that at the drain terminal. Similar effects can be seen if the percolation is situated close to the drain terminal.

Figure 5.25. (a) Dopant redistribution at the source or drain terminal will be more likely to be symmetric with each other if the percolation path is situated at the center of the device channel. (b) Dopant redistribution at the source terminal will be more severe as compared to that at the drain terminal if the percolation path is situated close to the source terminal, and vice versa.

5.10.1 DIODE CURRENT AT SUBSTRATE-SOURCE OR DRAIN P-N JUNCTION

The substrate-source or drain junction of a n-MOSFET is a *p-n* junction. The diode *I-V* characteristics at the substrate-source junction of a breakdown n-MOSFET were measured by applying a voltage to the source terminal with the substrate grounded (i.e., $V_{sub} = 0$), while the drain terminal and the gate electrode were floated. The diode current at the substrate-source junction in the forward- and the reverse-bias regime could be obtained when the source terminal was applied with a negative and a positive voltage, respectively. Similar experiments were performed at the substrate-drain junction of the n-MOSFET.

Figs. 5.26(a) and 5.26(b) show the diode *I-V* characteristics at the substrate-source and drain junction, respectively, of a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ }\mu\text{m}^2$) at different stages of the progressive breakdown. The n-MOSFET was stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \text{ }\mu\text{A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3 \text{ V}$ and $I_{gl} = 100\text{-}500 \text{ }\mu\text{A}$ were used in the

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2nd-stage CVS. Using Eqn. (3.2), $s_{BD} = 0.53L$ can be obtained. Due to the fact that the percolation path was situated almost at the center of the device channel, the change in the post-breakdown diode I - V characteristics at the substrate-source and drain junction of the n-MOSFET are expected to be similar. Figs. 5.26(c) and 5.26(d) show the details of the diode current in the low-voltage region of the forward-bias regime as well as the reverse-bias regime in Fig. 5.26(b), respectively. Moreover, Figs. 5.26(e) and 5.26(f) show the corresponding change in the post-breakdown diode current in Fig. 5.26(b) with respect to the diode current of a fresh n-MOSFET, which was calculated using

$$\Delta I_d = \frac{I_d(breakdown) - I_d(fresh)}{I_d(fresh)} \times 100\%. \quad (5.15)$$

A significant increase in the post-breakdown diode current can be observed in the low-voltage region of the forward-bias regime as well as the reverse-bias regime when I_{gl} increases from 10 μA to 500 μA . At $I_{gl} = 500 \mu A$, the change in the post-breakdown diode current in the low-voltage region of the forward-bias regime as well as the reverse-bias regime can exceed 100 and 10 times, respectively, at a particular voltage range. In the high-voltage region of the forward-bias regime, the change in the post-breakdown diode current for all I_{gl} is negligibly small as the diode series resistance start to dominate [148]. A catastrophic breakdown has not yet occurred even at $I_{gl} = 500 \mu A$ as the post-breakdown I_d - V_d and I_s - V_s characteristics of the n-MOSFET still remained transistor-like [115, 120, 121].

Refs. [149, 150] provide a detailed explanation on the dielectric-breakdown-induced dopant redistribution, which is simulated using TSUPREM and MEDICI. Our experimental observations are in well agreement with the simulation results reported in Refs. [149, 150], in which the post-breakdown diode current in the low-voltage region of

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the forward-bias regime as well as the reverse-bias regime increases during the progressive breakdown. According to Refs. [149, 150], the change in the post-breakdown diode I - V characteristics as a function of the growth of the progressive breakdown are related to the doping concentration change that is primarily due to the dopant redistribution. Under the presence of a high local temperature in the vicinity of the percolation path, arsenic at the source or drain terminal will diffuse at a faster rate, as compared to boron in the substrate. This is mainly attributed to the much higher concentration gradient of arsenic, even though the diffusion coefficient of boron is about order of magnitude higher than that of arsenic [151]. As a result, the redistribution of arsenic is more significant. Moreover, the simulation results reported in Refs [149, 150] show that the dopant redistribution may eventually lead to the occurrence of a local channel short, which is a catastrophic breakdown.

Assume that the post-breakdown substrate-source or drain junction is a linearly graded p - n junction, where the net doping concentration (n_{dop}) is proportional to the grading constant (a_g), that is, $n_{\text{dop}} = |N_d - N_a| \propto a_g$ [148, 152], where N_d and N_a represent the arsenic and the boron concentration. Based on Refs. [149, 150], n_{dop} decreases when the dopant redistribution becomes more severe, indicating that n_{dop} decreases during the progressive breakdown. As a result, a_g decreases, and hence, the depletion width, which is proportional to $a_{\text{grad}}^{-1/3}$ [148], increases, leading to an increase in the space-charge recombination current (I_{scr}). As the forward-bias voltage continues to increase, I_{scr} will gradually be dominated by the increasing diffusion current. In the high-voltage region of the forward-bias regime, the change in the post-breakdown diode current can be neglected as the diode series resistance is not much affected by the dopant redistribution.

Figure 5.26. Diode I - V characteristics at the substrate- (a) source and (b) drain junction of a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$) at different stages of the progressive breakdown. The n-MOSFET was stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \text{ \mu A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3 \text{ V}$ and $I_{gl} = 100\text{--}500 \text{ \mu A}$ were used in the 2nd-stage CVS. Diode current in (c) the low-voltage region of the forward-bias regime as well as (d) the reverse-bias regime in (b). Change in the post-breakdown diode current in (e) the forward-bias regime as well as (f) the reverse-bias regime in (b).

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In summary, the presence of substantial local heating effects in the vicinity of the percolation path will cause the properties of the substrate-source or drain p - n junction to change, leading to the change in the post-breakdown diode current.

5.10.2 LOCAL CHANNEL SHORT DUE TO DOPANT REDISTRIBUTION

During the dopant redistribution, arsenic at the source or drain terminal will be redistributed and move closer with each other, causing local channel narrowing effects to take place. A local channel short will occur when the dopants at the source or drain terminal of a breakdown n-MOSFET are in contact with each other. A typical example for a local channel short induced by the dopant redistribution is demonstrated in Fig. 5.27.

Figure 5.27. A typical example for a local channel short induced by the dielectric-breakdown-induced dopant redistribution. **(a)** TEM micrograph of a n-MOSFET suffering from a catastrophic breakdown. DBIE can only be observed at one of the edges of the device channel. **(b)** Resistor-like post-breakdown I_d - V_d and I_s - V_s characteristics of the n-MOSFET.

Fig. 5.27(a) shows the TEM image of a n-MOSFET suffering from a catastrophic breakdown, in which DBIE could only be observed at one of the edges of the device

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channel. Fig. 5.27(b) shows the post-breakdown I_d - V_d and I_s - V_s characteristics of the n-MOSFET. It can be noticed that both the post-breakdown I_d - V_d and I_s - V_s characteristics of the n-MOSFET behave resistor-like. This implies that the local channel short was triggered by the dopant redistribution rather than by microstructure damages.

Figure 5.28. $\Delta_{D/S}$ at different stages of the progressive breakdown for the n-MOSFET in Fig. 5.26. Note that $s_{BD} = 0.53L$. (a), (b) $\Delta_{D/S}$ in the low-voltage region of the forward-bias and the reverse-bias regime, respectively.

5.10.3 EFFECTS OF BREAKDOWN LOCATION AND CHANNEL LENGTH ON DOPANT REDISTRIBUTION

We let $\Delta_{D/S} = \Delta I_d / \Delta I_s$, where ΔI_s and ΔI_d define a change in the diode current at the substrate-source and drain junction of a breakdown n-MOSFET, respectively. Fig. 5.28 shows $\Delta_{D/S}$ at different stages of the progressive breakdown for the n-MOSFET in Fig. 5.26. Note that s_{BD} for the n-MOSFET in Fig. 5.26 was $0.53L$. If $\Delta_{D/S}$ approaches one, then the post-breakdown diode current change at the substrate-source or drain junction

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will be nearly identical with each other. This implies that the dopant redistribution at the source terminal is symmetric with that at the drain terminal. Conversely, one of the terminals may experience more severe dopant redistribution if $\Delta_{D/S}$ is smaller or larger than one. Figs. 5.28(a) and 5.28(b) show $\Delta_{D/S}$ in the low-voltage region of the forward-bias and the reverse-bias regime, respectively. We put our emphasis on the low-voltage region as the change in the post-breakdown diode current in this regions is more apparent and follows a consistent trend.

Figure 5.29. $\Delta_{D/S}$ at different stages of the progressive breakdown for a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \text{ \mu A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3.1 \text{ V}$ and $I_{gl} = 50\text{-}450 \text{ \mu A}$ were used in the 2nd-stage CVS. Note that $s_{BD} = 0.11L$. (a), (b) $\Delta_{D/S}$ in the low-voltage region of the forward-bias and the reverse-bias regime, respectively.

It can be observed that $\Delta_{D/S}$ for all I_{gl} are nearly equal to one (i.e., $\Delta_{D/S} = 0.9\text{-}1.2$), indicating that the extent of the dopant redistribution at the source terminal is nearly similar to that at the drain terminal. Since the percolation path acts as a heat source

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situated at the center of the device channel during the progressive breakdown, the temperature profile at the source and the drain terminal should be nearly similar with each other, leading to the observed symmetric dopant redistribution.

Figure 5.30. $\Delta_{D/S}$ at different stages of the progressive breakdown for a n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.3 \times 0.3 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \text{ \mu A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3 \text{ V}$ and $I_{gl} = 50\text{-}450 \text{ \mu A}$ were used in the 2nd-stage CVS. Note that $s_{BD} = 0.84L$. (a), (b) $\Delta_{D/S}$ in the low-voltage region of the forward-bias and the reverse-bias regime, respectively.

Fig. 5.29 show $\Delta_{D/S}$ at different stages of the progressive breakdown for another n-MOSFET ($T_{ox} = 20 \text{ \AA}$ and $L \times W = 1 \times 1.2 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \text{ \mu A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3 \text{ V}$ and $I_{gl} = 50\text{-}450 \text{ \mu A}$ were used in the 2nd-stage CVS. For comparison, the device dimensions of the n-MOSFETs in Figs. 5.28 and 5.29 are the same. However, the n-MOSFET in Fig. 5.29 was associated with $s_{BD} = 0.11L$, indicating that the percolation path was situated close to the source terminal. As shown in Fig. 5.29,

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$\Delta_{D/S}$ varied from 0.05 to 0.4 when I_{gl} increased from 50 μA to 250 μA . This means that the dopant redistribution at the source terminal was more severe. Since the heat source associated with the percolation path was located closer to the source terminal, the change in the post-breakdown diode current at the substrate-source junction will be more severe than that at the substrate-drain junction. For $I_{gl} = 10 \mu\text{A}$, $\Delta_{D/S}$ remained in the range of 0.8-1. This implies that the dopant redistribution is insignificant or has not yet occurred at a low I_{gl} , which corresponds to the early stage of the progressive breakdown. However, $\Delta_{D/S}$ was in the range of 0.6-1.6 for $I_{gl} = 350\text{-}450 \mu\text{A}$. It is believed that in the later stage of the progressive breakdown, the local temperature in the vicinity of the percolation path could reach a substantially high level that the temperature distribution in the whole device structure became nearly uniform [110, 149, 150].

Fig. 5.30 shows $\Delta_{D/S}$ at different stages of the progressive breakdown for a n-MOSFET with smaller device dimensions (i.e., $T_{ox} = 20 \text{ \AA}$ and $L \times W = 0.3 \times 0.3 \mu\text{m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. $V_{gstress} = 3.8 \text{ V}$ and $I_{gl} = 10 \mu\text{A}$ were used in the 1st-stage CVS, while $V_{gstress} = 3 \text{ V}$ and $I_{gl} = 50\text{-}450 \mu\text{A}$ were used in the 2nd-stage CVS. s_{BD} for the n-MOSFET was $0.84L$. It can be observed that $\Delta_{D/S}$ remained in the range of 0.7-1.3 for all I_{gl} . This indicates that the source and the drain terminal could have experienced symmetric dopant redistribution, even though the percolation path is situated nearer to the drain terminal. According to the simulation results reported in Ref. [110], the heat confinement effect induced by the Joule heating of a percolation path will be very substantial in breakdown n-MOSFETs that possess very narrow device geometry. The local temperature in the vicinity of the percolation path could be close to the silicon melting point, and the difference in the temperature gradient

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over the whole device structure is negligibly small, regardless the breakdown location. Therefore, the experimental measurements shown in Fig. 5.30 are consistent with the simulation results reported in Ref. [110].

5.11 SUMMARY

The PRM method, which is a new methodology used to measure the effective R_{perc} and R_{ch} at one particular instant of the progressive breakdown, has been described in details. It is found that the evolution of R_{perc} during the progressive breakdown can be classified into the R_{perc} - and the R_{para} -controlled region. The R_{perc} -controlled region corresponds to the early stage of the progressive breakdown, in which a percolation path experiences extremely rapid degradation. As the progressive breakdown continues to evolve, R_{para} becomes dominant, and the degradation of R_{perc} gradually slows down with decreasing V_{perc} . The R_{para} -controlled region corresponds to the later stage of the progressive breakdown, in which the stress across a percolation path has been partially relieved as R_{perc} is comparable to R_{para} . In addition, applying the PRM method, the effects of breakdown location and channel length on the degradation of R_{perc} during the progressive breakdown are studied in details. Furthermore, the degradation of a percolation path during progressive breakdown was found to be a thermally-activated and voltage-dependent process, implying that the progressive breakdown under the normal device operations and the accelerated stressing conditions could be governed by different physical mechanisms.

A *Schottky*-like barrier, which is situated somewhere between the percolation path and the p-type silicon substrate, could have been formed in the later stage of the

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progressive breakdown. This is strongly suggested by n_{sub} in the range of 1.3-1.7. In addition, we present that the conduction mechanism in the later stage of the progressive breakdown is governed by the interplay between the lowering of ϕ_{sub} attributed to a material property change in the vicinity of the percolation path and the percolation path dilation.

The existence of substantial local heating effects in the vicinity of the percolation path, which is confirmed by the IRPEM analysis and the ANSYS simulations, can cause the dopants at the source and the drain terminal of a breakdown n-MOSFET to be redistributed. The dielectric-breakdown-induced dopant redistribution is found to be one of the dominant physical mechanisms responsible for the degradation of the diode I - V characteristics at the substrate-source and drain junction of a breakdown n-MOSFET. In addition, the dopant redistribution in a breakdown n-MOSFET with a long channel is breakdown-location dependent, but this is not true for a breakdown n-MOSFET with a short channel. The dopant redistribution may accelerate the progressive breakdown as it could reduce the distance between the percolation path and the source or drain terminal, which in turn shrinking the post-breakdown gate oxide lifetime.

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CONCLUSION AND RECOMMENDATIONS

6.1 CONCLUSION

Digital and analog breakdown, which are two major regions of the progressive breakdown, have been studied in details using two major experimental techniques, which are a K-cycle multiple-stage CVS and the PRM method. A K-cycle multiple-stage CVS, which is a new stressing methodology, is mainly developed to study the behaviors of I_g in the digital breakdown under various conditions (i.e., the normal device operations and the accelerated stressing conditions). On the other hand, the PRM method is mainly developed to study the evolution of R_{perc} during the progressive breakdown, which in turns providing insights in understanding the physical mechanisms responsible for the behaviors of I_g in the analog breakdown.

(a) Digital Breakdown

The digital breakdown corresponds to the early stage of the progressive breakdown. It is a low conduction state for which a n-MOSFET is normally still functioning. In general, the digital breakdown can be characterized by the digital fluctuation of I_g . Our results suggest that the behaviors of I_g in the digital breakdown are mainly governed by the intrinsic properties of the percolation path within the gate oxide. The external parameters, such as breakdown locations and device dimensions, have

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minimum effects on the behaviors of I_g in the digital breakdown. Moreover, based on the $1/f$ -like noise study, we propose that the percolation path in the digital breakdown could be associated with an unstable physical structure. The digital fluctuation of I_g is believed due to a change in the local barrier heights caused by the transformation of oxygen-vacancy-related defects during the gate oxide stressing. One of the important findings is that the irreversible transition of the digital breakdown into the analog breakdown is governed by V_{crit} . If $V_{gstress}$ does not exceed V_{crit} , I_g will remain in the digital breakdown for a certain period of time. For T_{ox} smaller than 1.6 nm, a saturation of V_{crit} at 2-2.4 V is observed, meaning that the role of the digital breakdown in prolonging the progressive breakdown has been extended to standard sub-65-nm CMOS technology employing T_{ox} below 1.6 nm. For $V_{gstress}$ smaller than V_{crit} , the substantial lowering of dI_g/dt takes place as I_g will remain in the digital breakdown for a very long period of time. This implies that dI_g/dt at V_{op} will be significantly overestimated if it is extrapolated from the accelerated stressing conditions, yielding an overly pessimistic prediction on the gate oxide lifetime. In other words, the gate oxide is predicted to possess an excellent post-breakdown reliability margin at V_{op} , as compared to the prediction obtained from the conventional method that is derived from the accelerated stressing conditions. The progressive breakdown at a high V_g has been reported to be controlled by a single percolation path. However, it is found that multiple percolation paths are likely to be formed in the digital breakdown at a low V_g . The formation of the n^{th} percolation path at the source or drain terminal of a n-MOSFET, which will immediately lead to the occurrence of a catastrophic breakdown, acts as an ultimate killer for the ultrathin gate oxide.

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(b) Analog Breakdown

The analog breakdown, which is primarily constituted by the R_{perc} - and the R_{para} -controlled region, corresponds to the later stage of the progressive breakdown. It is a relatively high conduction state for which a n-MOSFET may or may not be functioning. In general, the analog breakdown can be characterized by a relatively stable I_g . At $V_{g\text{stress}}$ equal to or larger than V_{crit} , I_g will rapidly evolve from the digital breakdown into the analog breakdown. This rapid evolution of I_g is mainly due to the rapid degradation of R_{perc} , in which the percolation path is quickly wearing out as V_{perc} is nearly equal to $V_{g\text{stress}}$. This region is known as the R_{perc} -controlled region, which is found to be merely governed by the intrinsic properties of the percolation path. The digital breakdown starts to evolve into the analog breakdown somewhere in the R_{perc} -controlled region, depending on the magnitude of I_g . At a specific high I_g flowing through the percolation path, we believe that this will generate sufficient heat in transforming the percolation path from an unstable structure into a relatively stable structure with a silicon-like conductive channel at the core. After the rapid degradation of R_{perc} in the R_{perc} -controlled region, a saturation of R_{perc} will take place, and this region is known as the R_{para} -controlled region. The existence of a *Schottky*-like barrier in the R_{para} -controlled region indicates that a stable silicon-like percolation path could be formed in the R_{para} -controlled region. The voltage dependence of R_{perc} in the R_{para} -controlled region further implies that the physical structure of the percolation path in this region remains in a stable state. In the R_{para} -controlled region, the effects of the external parameters, such as breakdown location and device dimensions, on the progressive breakdown start to prevail. This plays an important role in affecting the lifetime prediction of gate oxide if the device failure criterion is in the R_{para} -controlled

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region. Undoubtedly, the intrinsic properties of a percolation path still play a role in controlling the evolution of I_g in the analog breakdown. As shown in Fig. 6.1., there are four possible physical mechanisms dominant in the R_{para} -controlled region in causing the shrinkage of the progressive breakdown: (1) the material property change in the vicinity of the percolation path, (2) the percolation path dilation, (3) the dopant redistribution, and (4) the formation and the growth of microstructural damages, such as DBIE. All of these will eventually lead to the occurrence of a catastrophic breakdown.

Figure 6.1. General schematic summarizing the possible physical mechanisms dominant in the R_{para} -controlled region in causing the shrinkage of the progressive breakdown: (a) the material property change in the vicinity of the percolation path, (b) the percolation path dilation, (c) the dopant redistribution and (d) the formation and the growth of microstructure damages, such as DBIE.

6.2 RECOMMENDATIONS

We believe that this project could be further extended. Some of the possible directions for future investigations and studies are given as follows:

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- A robust gate oxide lifetime projection model, which is able to accurately explain the gate dielectric breakdown data in statistical views by including the effects of the digital breakdown, should be fully developed.
- Approaches proposed and discussed in this study, such as the K-cycle multiple-stage CVS and the PRM method, can be applied to thoroughly analyze (1) the progressive breakdown in p-channel MOSFETs fabricated using different technology nodes, and (2) gate dielectric breakdown in advanced MOSFETs associated with high-k/metal-gate stacks. Similarities and differences are compared in details such that the device reliability can be more accurately projected.
- Although ultrathin gate dielectric breakdown has been intensively studied for more than one decade, the nature of a percolation path formed within the gate oxide during the occurrence of a dielectric breakdown event still remains unclear. The atomistic simulations based on the First Principle and various advanced physical analyzing tools, such as electron energy loss spectroscopy, are the methods of choice to uncover the physical origin of a percolation path, especially when the gate oxide is only formed by few mono-layers. This can certainly provide useful insights in enhancing or proofing the validity and the robustness of some of the gate dielectric intrinsic breakdown models.

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APPENDIX A

Figure I:

Evolution of I_g in the 2nd-stage for a breakdown n-MOSFET ($T_{ox} = 12.5 \text{ \AA}$ and $L \times W = 0.04 \times 1 \text{ \mu m}^2$) stressed using a two-stage CVS in inversion mode at the room temperature. (a) 0 s to 5000 s, (b) 30000 s to 35000 s, (c) 60000 s to 65000 s, (d) 90000 s to 95000 s, and (e) 120000 s to 125000 s. In the 1st-stage CVS, $V_{gstress} = 2.6 \text{ V}$ and $I_{gl} = 5 \text{ \mu A}$ were used. In the 2nd-stage CVS, $V_{gstress}$ was reduced to 1.8 V with $I_{gl} = 100 \text{ \mu A}$. The gate oxide stressing could be further continued, while I_g was still in the digital breakdown and had not yet reached $I_{gl} = 100 \text{ A}$. Note that $V_{gstress}$ is much smaller than V_{crit} , which is in the range of 2-2.4 V. Moreover, it can be observed that I_g at 0 s in (a) and 125000 s in (e) remained nearly unchanged at $\sim 3 \times 10^{-7} \text{ A}$, indicating that I_g did not experience any apparent net increase after the n-MOSFET was stressed for more than 120000 s. This implies that the transition of the digital breakdown into the analog breakdown could hardly occur at $V_{gstress}$ lower than V_{crit} .

(a)

(b)

(c)

(d)

(e)