Reliability modeling for ULSI interconnects

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RELIABILITY MODELING FOR ULSI INTERCONNECTS

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SUMMARY

Electromigration (EM) and stress-induced voiding (SIV) are the two major reliability concerns for metal interconnects in integrated circuits. In particular, with the dimensions of interconnect scaled into nano regime and the inclusion of low-k materials as dielectrics, the reliability aspects for on chip interconnects are becoming more challenging. In this work, both EM and SIV failure physics are investigated using finite element based modeling and verified through experiments.

The most fundamental aspect of EM is diffusion, where electron wind force (EWF) is considered as the only source of driving force for EM mass transport. As interconnect line width becomes narrow, the effects of the surrounding materials on EM can no longer be accounted for by the modification of the atomic diffusivity as in the traditional diffusion path approach. In this work, a modified EM modeling methodology is proposed to improve the EM modeling accuracy. This methodology is based on the driving force approach and its mathematical formulations are derived based on Green's theorem. Three important driving forces are considered in this work: electron wind force (EWF), temperature gradient induced driving force (TGIDF), and thermo-mechanical stress gradient induced driving force (SGIDF). The formulations are implemented through finite element analysis (FEA), and the EM void nucleation and its growth can be simulated through the developed static and dynamic simulation FEA codes. It is found that the thermo-mechanical stress gradient induced driving force is the dominant driving force for EM failure in M2 test structures. The modeling results are consistent with our experimental results on reservoir effect structures.

It is known that the interconnect geometry and surrounding materials has a strong impact on the EM performance. In the subsequent part of the thesis, the effect of interconnect design factors on EM is investigated. The effect of reservoir extension on the EM lifetime is studied both experimentally and analytically. Lifetime enhancement factor is found to decrease with increasing EM stress current experimentally. The analytical formulation for the lifetime enhancement factor is derived to reveal the dependence of lifetime enhancement factor on EM test conditions.

For SIV, we propose a lifetime model from the energy perspective. A SIV lifetime equation is derived which is similar to the Black's equation for EM failure. It is shown that SIV lifetime is strongly dependent on the passivation quality at the cap layer interface, the confinement effect by the surrounding materials to interconnects, and the available diffusion paths in interconnects.

The effects of interconnect design factors on SIV performance are explored with FEA. 3D finite element simulations are performed to simulate the void nucleation and void growing process during SIV for line-via structures with SiO₂ and low-k interconnects. With FEA, the mechanisms for poor SIV performance of low-k interconnects as well as different void growing dynamics between SiO₂ and low-k interconnects are revealed. Thermo-mechanical stresses in Cu interconnects are analyzed to investigate the effect of dielectric materials as well as line width on the stress distributions in line-via structures. The hydrostatic stress and von Mises stress distributions can be simulated and their distributions are important in assessing the stress related damages in Cu interconnects.

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LIST OF ABBREVIATIONS

AFD	- Atomic flux divergence
ARC	- Anti-reflection coating
BEOL	- Back end of line
CDF	- Cumulative distribution function
CDO	- Carbon doped oxide
CFD	- Computational fluid dynamics
CMP	- Chemical mechanical polishing
CTE	- Coefficient of thermal expansion
DOF	- Degree of freedom
ECP	- Electrochemically plated
EM	- Electromigration
EWf	- Electron wind force
FDE	- Partial differential equation
FEA	- Finite element analysis
FEM	- Finite element method
HTS	- High-temperature storage
ILD	- inter-level dielectrics
IMD	- Inter-metal dielectric
MEP	- Mean free path
MOS	- Metal-oxide-semiconductor
MTF	- Median-time-to-failure
MTTF	- Mean time to failure
PECVD	- Plasma enhanced chemical vapor deposition
RIE	- Reactive ion etching

SFT - Stress free temperature

SGIDF - thermo-mechanical stress gradient induced driving force

SIV - Stress-induced voiding

SM – Stress migration

TCR - Temperature coefficient of resistivity

TDDB - Time dependent dielectric breakdown

TEM - Transmission electron microscopy

TGIDF - Temperature gradient induced driving force

ULSI - Ultra-large scale integrated circuits

USG - Undoped silicate glass

XRD - X-ray diffraction

1. INTRODUCTION

1.1 Background

Multilevel interconnects is one of the most important technologies for ultra-large scale integrated circuits (ULSIs) such as microprocessors (MPUs), dynamic random access memories (DRAMs), and application specific integrated circuits (ASICs). Due to the advancement of microelectronic industry, the performance of integrated circuits has been continuously improved by scaling down device dimensions and increasing device density. The reduced physical gate dimension of a metal-oxide-semiconductor (MOS) transistor has decreased the gate delay and increased the signal propagation speed. On the other hand, interconnects have increased in density and decreased in size due to this miniaturization. The scaling of interconnects increases the back-end-of-line (BEOL) interconnect delay. Figure 1.1 summarizes the total signal delay, the combination of transistor gate delay and Al/oxide interconnect (RC) delay, as a function of minimum feature size [1]. The interconnect delay is determined by the line resistance (R) and the intra-line capacitance (C). For submicron device, the interconnect delay becomes the performance limiting factor of the device. This has generated an intensive effort to improve materials and processing for interconnect technology.

Figure 1.1: Interconnect and gate delay time as a function of device feature size.

There are two effective ways to reduce interconnect delay. One is to use materials with lower resistivity for interconnect lines to reduce the R component. Cu has replaced Al(Cu) alloy as the interconnect material due to its lower resistivity [2] and better electromigration (EM) resistance [3]. The other way to reduce the interconnect delay is to use a lower dielectric constant material (low- k) for interlayer dielectric (ILD) to reduce the intra-line capacitance, C . Cu and low- k dielectric, when successfully integrated, can improve the performance of the integrated circuits by reducing the interconnect delay more than 50% compared to Al(Cu)/oxide interconnects for sub-quarter micron technology [4]. These low- k materials include silicon oxyfluoride (FSG), fluorinated polyimides (FPIs), Black Diamond (SiCOH), etc. However, these low- k materials have thermal and mechanical properties inferior to those of SiO_2 , which may pose reliability issues in future narrow Cu/low- k interconnects.

With the continuing scaling of on-chip interconnects, the metal interconnect dimension scales down for about 30% at each technology node scaling, rendering interconnect reliability to become the dominant factor for the circuit reliability [5]. Among all the failure mechanisms for interconnects, EM and stress-induced voiding

(SIV) are the major failure mechanisms in modern BEOL reliabilities. They are induced by different driving forces which will be detailed below. In reality, these two driving forces are coupled together through Joule heating. Therefore, special attention is needed in the EM test structure design and test stress conditions in order to study each failure mechanism individually. Besides the above-mentioned two failure mechanisms, time dependent dielectric breakdown (TDDB) [6] and plastic deformation [7] have also been reported with the implementation of narrow Cu/low-k interconnects.

Electromigration is diffusion-controlled mass transport, driven by electron current flow in metal lines. During EM, electrons collide with metal ions, transferring momentum to metal ions. As a result of this collision process, metal ions migrate from the cathode and accumulate at the anode. In an interconnect structure, a local imbalance of EM mass flux can occur at structural discontinuities, such as a barrier interface or a grain boundary/interface junction. The flux divergence can lead to damage formation resulting in EM failure. The cathode and anode ends of the line are the divergent sites and subject to large flux divergence, which can result in mass depletion and accumulation, respectively. As a result, a void or an extrusion can be formed at the cathode or anode end, rendering the failure of interconnects. Because of these severe functional effects on interconnects, EM has been studied intensively over the last fifty years [8-16].

During the fabrication of interconnects, the process temperature can go up to 400 °C during annealing and the deposition of dielectrics, large thermo-mechanical stress is generated upon cooling down the interconnect to room temperature. Besides that, extra thermo-mechanical stress can also be caused by the non-uniform temperature distributions in interconnect, attributed by the Joule heating effect in the presence of high current density. Therefore, the encapsulated interconnect is under hydrostatic tension and

this hydrostatic stress can be relaxed in the presence of mini-void or flaw in interconnects, leading to stress-induced voiding (SIV) in the form of open circuit or substantial resistance increase [17, 18].

1.2 Motivation

It is important to predict how long the interconnect can function properly before EM or SIV failure. However, it is impractical to test the interconnect in actual operating conditions as the failure time can be in terms of years. Therefore, interconnects are usually tested at high current and high temperature to accelerate the failure and their lifetime in normal condition can be estimated by extrapolation. As the extrapolation is based on the lifetime models, a better understanding of the underlying failure mechanism is required. So far, lifetime models have been based on empirical methods, e.g. Black's equation for EM [10], phenomenological equation for SIV by Fisher *et al.* [19], etc. Thus, an evaluation of potential failure modes is very important as interconnect dimension has been scaled into nano regime.

As EM is a very complicated diffusion process which involves different driving forces and various diffusion paths, the changing dominance of the driving forces and the diffusion paths due to the design and process of an interconnect system complicates our understanding of EM physics. Fortunately, with the advancement of computing power of modern computers and sophisticated software, the understanding of underlying EM physics is enhanced through numerical modeling of EM [20-23]. Finite element analysis (FEA) is one of the most promising methods in studying EM physics. However, the value and effectiveness of FEA in reliability modeling is not fully appreciated by both the academic and industry.

With the help of multi-physics FEA software ANSYS[®], realistic 3D interconnect structures can be modeled with all the surrounding materials taken into considerations. With proper boundary conditions applied and solved, the simulation results (current density, temperature, stress, etc) and their derivatives (stress gradient, temperature gradient, etc) can be displayed in a contour format, therefore, the weak point prone to EM can be located and the dominant driving force can be identified. Similarly for SIV, thermo-mechanical stress and its gradient can be simulated for 3D interconnect structures. Further more, the effect of surrounding materials, interconnect dimensions, test conditions on EM and SIV can be analyzed with FEA. This is significant for ULSI development so that a reliable interconnect system can be built as to further advance the ULSI technology.

Reliability evaluation and improvement of new interconnects require a deep understanding of the physics of EM and SIV. However, experimental investigations can be very expensive and slow. Furthermore, not all underlying physics in EM and SIV can be captured experimentally. One motivation of this thesis work is to explore the capability of FEA in interconnects reliability modeling and new failure physics can be discovered through FEA modeling.

1.3 Contribution

Both EM and SIV are affected the physical properties of the interconnect, which include the interconnect dimensions, surrounding material properties, etc. With FEA, the failure physics for both EM and SIV can be explored and the effect of interconnect design factors on EM and SIV performance can be analyzed quantitatively. The main contribution of this thesis work covers the following aspects,

1. A comprehensive description of the finite element analysis including the basic FEA concept, FEA formulations, analysis procedures and its applications is presented. The issues of element shape, meshing density and substrate thickness in the modeling for interconnects are addressed.
2. For EM,
 - a) A detailed review of the two most popular approaches in EM studies: the diffusion path approach and the driving force approach are presented in depth. In particular, we focus on the formulations, lifetime estimation, the validity of each approach and their comparisons.
 - b) A modified EM modeling methodology is proposed to improve the EM modeling accuracy. This methodology is based on the driving force approach and its mathematical formulations are derived based on Green's theorem. The formulations are implemented in FEA codes, and the EM void nucleation and void growth can be simulated through static simulation and dynamic simulation. The results are consistent with the experimental findings on reservoir effect EM studies.
 - c) The effects of interconnect design factors on EM performance are explored with FEA:
 - i. The effect of reservoir extension on the EM lifetime is studied both experimentally and analytically. Lifetime enhancement factor is found to decrease with increasing EM stress current experimentally. The analytical formulation for the lifetime enhancement factor is derived to explain the experimental findings.
 - ii. We demonstrate the EM characteristic as a function of electron flow direction and ratio of the lengths in width transition Cu interconnects. It is

found experimentally that EM life-time significantly shorten when the electron flow direction is from narrow-to-wide segment.

- iii. Blech product in EM is compared with Cu/oxide and Cu/low-k interconnects. It is found that Blech product is lower for Cu interconnects at high temperature due to its inelastic behavior. A good passivation is needed to improve the EM lifetime for future narrow low-k interconnects.
- d) The issue in high temperature and high stress current EM test is presented. The variation of activation energy and current density exponent in Black's equation is derived analytically. This variation can be important in future EM test in low-k interconnects with severe Joule heating.

3. For SIV,

- a) We present a lifetime model for SIV from the energy perspective. A SIV lifetime equation is derived which is similar to the Black's equation for EM failure. It is shown that SIV lifetime is strongly dependent on the passivation quality at the cap layer interface, the confinement effect by the surrounding materials to interconnects, and the available diffusion paths in interconnects. The critical temperature for SIV is also derived analytically.
- b) The effects of interconnect design factors on SIV performance are explored with FEA:
 - i. 3D finite element simulations are performed to simulate the void nucleation and void growing process during SIV for line-via structures with SiO₂ and low-k dielectrics. With FEA, the mechanisms of poor SIV performance for low-k interconnects as well as different void growing dynamics between SiO₂ and low-k interconnects are revealed.

- ii. Thermo-mechanical stresses in Cu interconnects are calculated to investigate the effect of dielectric materials as well as line width on the stress distributions in line-via structures using FEA. The hydrostatic stress and von Mises stress distributions can be simulated and their distributions are important in assessing the stress related damages in Cu interconnects.

1.4 Organization of the thesis

This thesis is divided into six chapters. Chapter 1 gives an introduction of the overall thesis, including general background, motivation and the contribution of this thesis work. Chapter 2 presents a detailed literature review for the overall interconnect reliabilities, with special focus on EM and SIV. Chapter 3 is devoted to finite element analysis. This includes the FEA formulation, analysis procedures and its applications in reliability modeling. Besides, the issues of element shape, meshing density and substrate thickness in the modeling for interconnect are also covered. Chapter 4 focuses on the EM work, including the newly developed EM simulation methodology, the effect of interconnect design factors on EM and the issues in highly stressed EM test. In Chapter 5, we shall focus on the SIV studies, including the newly developed SIV lifetime model and the effect of interconnect design factors on SIV reliabilities. Finally, Chapter 6 summarizes the results of this thesis and gives recommendations for future work.

2. LITERATURE REVIEW

2.1 Overview of Interconnect Reliabilities

Interconnects are essential to any network. For electrical network, interconnects are needed to connect different electrical functional blocks so that electrical signals can flow in between the blocks for information processing. Interconnects also provide paths for energy supply to the blocks. Therefore, interconnects in electrical network are crucial and must be good electrical conductors.

When the concept of integration begin in the early 50's for electronics, interconnects remain important to connect all the transistors and passive components in a single integrated chip, and one of the first few failure mechanisms that occurred in the first integrated chip is interconnect related failure [24]. As integration technology advances, the interconnect technology also advances with a continuous shrinking in dimension, but its reliability remains a key determining factor to the reliability of an integrated system [25].

For integrated electronic chip, interconnects are mainly metal, and Al, Cu and Tin alloy solder are the most commonly used metal for interconnects. The common failure mechanisms for these metals are electromigration (EM), stress induced voiding (SIV), corrosion, whisker formation, stress induced hillock, and time dependent dielectric breakdown (TDDB).

2.1.1 Electromigration

Electromigration (EM) is a phenomenon of mass transport in metal film when the film is stressed with high electrical current density ($\sim 10^5$ A/cm²). Due to the small cross-sectional area of the interconnections (or thin films) used in microelectronic devices, the current density at normal operating condition is extremely high and as a consequence the EM induced mass transport may occur through diffusion. This significant mass transport during EM renders accumulation of vacancies or atoms, creating voids or hillocks in the interconnection. The void formation in the interconnection results in open circuit or increased line resistance that can cause circuit functional (or parametric) failure. The hillock formation in the interconnection results in short circuit between adjacent interconnects. The EM induced mass transport is accelerated when the temperature of an interconnection is increased.

2.1.2 Stress induced voiding

Stress induced voiding (SIV) is also called stress migration (SM), and it is a phenomenon of metal voiding in conductor lines that are under tension in the absence of electrical current. Large amount of thermo-mechanical stress can be developed due to the thermal expansion mismatch between interconnect material and the surrounding materials. The voids can totally sever a conductor line to cause circuit failures.

Stress induced voids can be classified into two major categories, a wedge-shaped and a slit-shaped void. The wedge-shaped voids form at the edges of conductor lines and tend to peak in lines of 2-3 μm width. Slit-like voids are not easy to observe but nearly all the open-conductor failures are caused by them. Figure 2.1 below shows examples of stress

induced voiding in ULSI interconnection with USG (undoped silicate glass) and CDO (carbon doped oxide) as inter-metal dielectric respectively.

Figure 2.1: Stress induced voiding in ULSI interconnections with (a) USG and (b) CDO as inter-metal dielectric

2.1.3 Corrosion

There are basically three different types of corrosion that can occur in metals, namely electrochemical corrosion, galvanic corrosion and gas corrosion [26, 27].

Electrochemical corrosion occurs due to the different oxidation potentials of the adjacent metal films and the presence of moisture. This difference in oxidation potential is the result of externally applied bias. If catalysts such as chlorides are present, the corrosion rate will be greatly increased, leading to corrosion through the formation of stable corrosion products, which may not contain chloride itself. An example of corrosion product is lead carbonate.

Chloride ions play a key role as a catalyst in many corrosion mechanisms occurring in the semiconductor, microelectronics and electronics industries. Only traces of chlorides are needed to promote and accelerate corrosion reaction.

In the absence of external bias, the dissimilar regions within an interconnect will also possess different oxidation potential. This dissimilar region could be the different metals,

or different amount of impurity in the metal. In this case, the anodic and cathodic processes are localized. The electron current will flow between the anode and cathode through the metal, and in the electrolyte the movement of cations is toward the cathodic region and the anions toward the anode. As a result, the anode will suffer metal loss (cations).

Even in the complete absence of moisture on metal surface, corrosion can still occur due to the presence of chemically active gases. An example is the exposure of Ag film to S_8 saturated vapors. For detail discussion of corrosion, readers are referred to [28].

2.1.4 Whisker formation

Whiskers formed on metal film surface can cause short circuit or increased leakage current. Tin whisker is commonly observed in electronic products. It was discovered in 1951 by Compton *et al.* [29], but was found to be mitigated with the addition of Pb in the solder in 1954 by Arnold *et al.* [30]. Figure 2.2 shows the whisker formation on the compressed SnPb eutectic layer as an example [31].

Figure 2.2: Tin whisker growth at ambient temperature on the compressed SnPb eutectic layer

However, the shrinkage of the size of solder today renders electromigration to occur in solder. This electromigration will activate the formation of tin whisker even in leaded solder as observed recently by Fan-Yi *et al.* [32].

Besides solders, Al interconnects can also form whisker mainly due to the results of electromigration [33]. Hinode *et al.* [34] found that Al whisker formation is preceded through the following steps:

- a) non-uniform grain growth during annealing (formation of local low stress positions),
- b) diffusion driven by stress gradients (along grain boundaries and lattices),
- c) dislocation climb from Frank—Read source,
- d) dislocation glide to extrude aluminum,
- e) step formation on the film surface by breaking through the oxide layer, and re-arrangement of side surfaces to reduce the surface energy.

After their thorough studies of whiskers on Al, they concluded the following [34]:

- a) Whiskers nucleated in a relatively narrow temperature range (230-300 °C) in the sample films, and this temperature range corresponds to the start of the plastic deformation of the overall film.
- b) Whisker formation is caused by thermal stress that results from a thermal expansion mismatch between the film and the substrate.
- c) Most whiskers were straight (though sometimes kinked at an angle of 120 °), rod-shaped and had plane side surfaces.
- d) The whiskers were mostly single crystals with their bottom part within the film, and the bottom part was a larger grain than the surrounding grains.
- e) Whiskers tend to grow 20 °—55 ° from the perpendicular direction. This may be related to the slip plane directions in the highly prefer-oriented (111) films.

- f) Growth only occurs at the bottom of a whisker.
- g) An oxidizing atmosphere suppresses nucleation of the whiskers.
- h) A higher heating rate decreases the whisker number density and length.
- i) Aluminum films contained many impurities, such as oxygen and nitrogen, can suppress grain growth, causing localization of stress relief, resulting in whisker formation.

Takatsuija *et al.* [35] also found that whisker generation is promoted as the exposure times in the temperature range of 230-300 °C becomes longer. Furthermore, most whiskers grow from (110)-oriented and (211)-oriented grains, and that no whiskers grow from (111)-oriented grains.

2.1.5 Hillock formation

Thermally induced Al hillocks cause manufacturing and reliability problems in integrated devices. These thermal hillocks interfere with the uniformity of subsequent spin-on materials such as photoresist, and can create pinholes in passivation on top metal line rendering the metal surface susceptible for corrosion or electrical breakdown. Thermal hillocks have both lateral and vertical dimensions on the order of 1 μm [36].

Iwamura *et al.* [37] found that whiskers are variants of hillocks. The formation of both hillocks and whiskers is observed at the same time during heating, and their sizes increase with increasing temperature. With further heating, the bottom of a whisker changes its form to a hillock.

In fact, it is found that interconnect materials can generally form either hillock and/or whisker after prolonged operation as a result of stress relaxation. They are highly

dependent on the microstructure of the thin film and the nature of the stress in the film. Figure 2.3 shows bimodal size distribution of conical hillocks formed on the electrodeposit surface of 16 μm thick pure Sn electrodeposit [38].

Figure 2.3: Hillocks formed on the electrodeposit surface of 16 μm thick pure Sn electrodeposit.

2.1.6 Time dependent dielectric breakdown (TDDB)

With continuous scaling and the introduction of low-k dielectrics in Cu interconnects, TDDB reliability has become important although it was not an issue for Al interconnects. This is because Cu ions can easily diffuse into dielectrics in the absence of barrier metal. The low-k materials, when integrated in Cu interconnects, have generally low breakdown strength of less than 3 MV/cm, high leakage current, poor barrier confinement. The effectiveness of the barrier metal to prevent Cu diffusion is studied through TDDB test.

2.2 Overview of Al and Cu based interconnects

The Al(Cu) alloy has been widely used as an interconnect material in the IC technology. However, it has high resistance-capacitance (RC) delay and is prone to EM

failure. As a result, Cu is receiving considerable attention as an alternative to Al(Cu) alloy in ULSI interconnects. Cu offers many intrinsic advantages over conventional Al(Cu) alloy, including lower electrical resistivity, and higher mechanical strength. Furthermore, Cu has lower atomic diffusivity than Al because of its higher melting temperature [39]. Table 2.1 compares some physical properties between Al and Cu [40]. The EM resistance for Al has been improved by the addition of alloying elements (0.5-2wt% of Cu [15]) but the resistivity of Al is also increased. As a result, Cu has replaced Al in most areas of interconnect. Its resistance is lower than that of Al and Joule heating is less for similar current densities resulting in lower increases in resistances [41].

Table 2.1: Bulk material properties of Al and Cu

Property	Aluminum	Copper
Resistivity (ρ)	2.65 $\mu\Omega\cdot\text{cm}$	1.67 $\mu\Omega\cdot\text{cm}$
Temperature Coefficient of Resistivity (α)	4.5×10^{-3}	4.3×10^{-3}
Relative ΔT at Joule Heating	1.93 $^{\circ}\text{C}$	1 $^{\circ}\text{C}$
Effective Valance (Z^* bulk)	6.5-16.4	3.7-4.3
Activation Energy (Lattice)	1.48 eV	2.19 eV
Self Diffusivity (at 100 $^{\circ}\text{C}$)	$2.1\times 10^{-20} \text{ cm}^2/\text{s}$	$2.1\times 10^{-30} \text{ cm}^2/\text{s}$
$Z^*\rho D$ (at 100 $^{\circ}\text{C}$)	$3.62\text{-}9.12\times 10^{-19} \mu\Omega\cdot\text{cm}^3/\text{s}$	$1.3\text{-}1.5\times 10^{-29} \mu\Omega\cdot\text{cm}^3/\text{s}$
Coefficient of Thermal Expansion (CTE)	$2.35\times 10^{-5}/\text{K}$	$1.7\times 10^{-5}/\text{K}$
Melting Point	660 $^{\circ}\text{C}$	1083 $^{\circ}\text{C}$
Thermal Conductivity	2.38 W/cm	3.98 W/cm

The fabrication processes are drastically different between Cu and Al interconnects due to their differences in chemical properties. As a result, the use of Cu interconnect, on the other hand, introduces several problems that did not exist in the Al (Cu) interconnects. First of all, Cu can diffuse very fast in both oxide and silicon. Further more, Cu can be easily oxidized at low temperature and does not form a self protective layer to stop further oxidation. Therefore, Cu lines and vias must be confined at all locations using some barrier material (e.g. Ta [42], Ti [43], etc). This barrier material (liner) also promotes the adhesion of Cu to Si or SiO_2 . Besides this, a lack of volatile compounds at temperatures for reactive ion etching (RIE) is another challenge for Cu interconnects, which makes it difficult for Cu to be patterned using conventional subtractive plasma etching as

employed in Al interconnects. The most practical technique for Cu patterning is the damascene process where Cu is deposited in trenches or vias etched in the dielectric layer. Excess Cu is then removed by Chemical Mechanical Polishing (CMP). After that, the Cu lines are capped with a dielectrics diffusion barrier (e.g. SiN).

The cross section schematic view for Al and Cu interconnects is shown in Figure 2.4. The Al interconnect has thick refractory metal layers (TiN, Al₃Ti), at the top and bottom of the lines serving as anti-reflection coatings (ARC) and seed layer for the via-fill process, respectively. Robust tungsten (W) filled vias are used to connect different levels of Al metallization as shown in Figure 2.4(a). The side walls and the bottom of the Cu line are encapsulated by the diffusion barrier layer (Ta) while the top surface is passivated by cap layer (SiN or Si₃N₄) as shown in Figure 2.4(b).

Figure 2.4: (a) Al interconnects with W-filled vias and conducting shunt layers at the top and bottom of a line. (b) Dual-damascene Cu interconnects, with Cu-filled vias, thin barrier layer at the side and bottom of a line, and a dielectric cap layer at the top.

The EM behaviors between Al and Cu interconnects are different due to different architecture schemes with different materials used in fabrication. Theoretically, Cu interconnects should display more superior EM performance than Al interconnects due to a much lower self diffusivity as shown in Table 2.1. Due to the presence of fast diffusion path at Cu/cap layer interface, the EM performance for Cu interconnects may be poorer than that of Al. For Al interconnect, a very thin oxide film ($\sim 60\text{\AA}$) is formed on the Al

surface which acts as an effective diffusion barrier and therefore the surface diffusion is eliminated. Grain boundaries have been identified as the dominant diffusion path for Al interconnects. For narrow Al interconnect with bamboo structures, its EM lifetime may be better than Cu interconnects due to the absence of grain boundary diffusion. In this case, the dominant diffusion pathway is the interface between the Al alloy and barrier layers.

For Cu interconnects, the fast diffusion along Cu/cap is believed to be caused by the defects generated during the Cu top surface CMP process [44]. These defects are trapped near the Cu/cap interface and provided a fast diffusion path for EM transport. In current Cu technology, the critical tensile stress for void nucleation has been estimated to be around 40 MPa [45], comparing to 500 MPa for Al technology.

2.3 Fundamentals of Electromigration

2.3.1 History of Electromigration

In principle, EM should exist whenever there is a current flowing through a metal wire. In bulk wires, such as those used for home circuitry, the maximum current density is about 10^4 A/cm² due to Joule heating [46]. Any current density even modestly exceeding this value will produce enough heat to melt the metal wire. In this case, the driving force (current density) is insufficient to induce EM process. The situation is different in the case of thin film interconnect used for connecting devices in integrated circuits. A thin film interconnect can carry a much higher current density (10^7 A/cm²), which facilitates EM [47]. This is because the Si substrates on which interconnects are built are very good heat conductors. On the other hand, in a device having a very dense integration of circuits,

heat management is a serious issue. Typically, a device is cooled by a fan or other means in order to maintain the operation temperature around 100 °C.

Investigation of EM phenomenon can be traced back about a century ago with the first observation reported by Geradin (1861) in molten alloys of lead-tin and mercury-sodium. Systematic EM studies have been carried out since 1950s. The first reported work on EM was presented by Fiks in 1959 [8]. Followed that, Huntington and his coworkers at the Rensselaer Polytechnic contributed significantly to the EM failure process through their studies on current induced motion of surface scratches on bulk metals [9]. They found two opposing forces acting on thermally activated metal ions and they are called “direct force” and “electron wind force”, which are still under study today. The direct force is the force experienced by the activated positive metal ion in the opposite direction to the electron flow due to the application of electric field. On the other hand, electron wind force is the force experienced by metal ion in the direction of electron flow due to the momentum exchange between the moving electrons with the ions. Followed that, two milestones in the EM research history established by the formulation of Black’s equation by Black in 1969 [10] and the discovery of backflow stress by Blech in 1976 [48]. Since then various theoretical models and experiments have been developed to uncover the underlying EM physics.

2.3.2 Flux equations

Electromigration is a mass transport process which can be observed in metal conductors at high current densities. This mass transport is caused by the sum of different forces acting on a metal atom: the direct force due to the Coulomb interaction of the positive metal ions with the electric field and the electron wind force resulting from the

momentum transfer between the electrons and the metal ions. The resulting force f_e due to EM is conventionally expressed as [9]

$$f_e = Z^* e \rho j \quad (2.1)$$

where e is the electric charge and ρ is the resistivity of the metal. The product ρj is the electric field in the metal line, and $e \rho j$ has the dimension of force. The dimensionless number Z^* is known as the effective charge number. Z^* is a negative number because the electron wind force is in the direction of the electron flow which is opposite to the electric current density.

In this work, we assume EM is via a vacancy exchange mechanism, i.e. the flux of metal atoms is equal and opposite to the flux of vacancies. In fact, the atomic model and vacancy model will lead to mutually consistent predictions if one assumes 1) mass transport is through substitutional vacancy mechanism and 2) the vacancies are in thermal equilibrium with the stress [49].

The Nernst-Einstein's equation related the electron wind force to the atomic flux J , which is the number of atoms crossing a unit area per unit time.

$$J_{EM} = \frac{D Z^* e \rho j}{\Omega k_B T} \quad (2.2)$$

where $D = D_0 e^{-E_A/k_B T}$ is the diffusivity, E_A is activation energy and Ω is the atomic volume of the metal. It is noted that D in Eq. (2.2) represents an effective diffusivity along the interconnect because the EM mass transport can occur through different diffusion mechanisms such as lattice diffusion, interface diffusion, grain boundary diffusion, etc.

Electromigration behavior has been investigated using edge displacement experiments which were first introduced by Blech [48, 50]. Short Al segments of different

lengths are deposited on a continuous line of a higher resistivity diffusion barrier material Ta/TiN as shown schematically in Figure 2.5. When current flows through the Al segment, atoms are depleted from the cathode and accumulated at the anode. Since the Al segment is constrained by the underlying diffusion barrier layer and the native oxide, this leads to the generation of backflow stress. When atoms accumulate at the anode, there is an increase in the number of lattice sites, leading to the generation of compressive stresses. Similarly, tensile stress is generated at the cathode end. As a result a stress gradient is developed along the segment opposite the electron wind force.

Figure 2.5: Schematic illustration of the Blech structure in edge displacement experiments

The atomic flux driven by the backflow stress gradient can be written as

$$J_{\sigma} = \frac{D}{k_B T} \frac{\delta \sigma_b}{\delta x} \quad (2.3)$$

where σ_b is the backflow stress. The backflow stress gradient drives metal atoms back towards the cathode end, resulting in mass transport opposing that of the electron wind force. This phenomenon is called the “Blech effect”. The net atomic flux due to the combined effects of the electron wind force and backflow stress gradient is the sum of Eqs. (2.2) and (2.3) as shown in Eq. (2.4)

$$J = J_{EM} - J_{\sigma} = \frac{DN}{k_B T} \left(eZ^* \rho j - \Omega \frac{\delta \sigma_b}{\delta x} \right) \quad (2.4)$$

If the net atomic flux given in Eq. (2.4) is zero, there is no mass transport or the interconnect line is immortal. Under this condition, the Blech product can be derived as

$$jL_c = \frac{\Omega \sigma_{crit}}{Z^* e \rho} \quad (2.5)$$

where L_c is the Blech length and σ_{crit} is the critical stress the metallization can sustain before void nucleation. It is noted that σ_{crit} is developed from backflow stress and it is elastic in nature [51]. Equation (2.5) reveals that with shorter lines or lower current densities, the EM induced mass transport can be suppressed entirely under the steady state. However, if the backflow stress is greater than the critical stress, extrusions or hillocks will form and EM will continue.

An important application of the Blech effect is that if all the conductors in a chip can be made shorter than the Blech length for a given current density, EM can be eliminated as a failure mechanism.

2.3.3 Black's equation

In order to evaluate EM reliability under service condition, a means of scaling accelerated test results to much less severe operating conditions is required. In 1967, Black carried out series of EM experiments on Al-based metallization systematically [10]. He formulated a semi-empirical equation by relating the test temperature and current density to the median time to failure,

$$t_{50} = Aj^{-n}e^{E_A/k_BT} \quad (2.6)$$

where A is a constant, j is the current density, n is the current density exponent, E_A is the activation energy of the failure process, k_B is Boltzmann's constant and T is the absolute temperature. n is between one and two, depending on whether the failure is growth limited or nucleation limited. Equation (2.6) is known as the Black's equation and it is used widely in the EM study of VLSI interconnects.

2.4 Fundamentals of stress-induced voiding

The interconnect structure consists of several different materials including metal (W contacts, Al or Cu), dielectric (SiO_2 or low-k), diffusion barrier (Ta or Ru), and cap layer (SiN or CoWP) on top of thick Si substrate. The fabrication of the structures involves several thermal cycles from room temperature to 350~450 °C, resulting in a large amount of thermo-mechanical stress due to the thermal expansion mismatch between interconnect material and the surrounding materials. The magnitude of thermo-mechanical stress depends on the interconnect geometry (e.g. line widths, aspect ratio) as well as the surrounding materials (e.g. SiO_2 or low-k). Other than the thermo-mechanical stress, considerable grain growth (grain boundary elimination) induced stress is also known to be developed for Cu interconnects by electroplating [52].

The developed large thermo-mechanical stress can act as a driving force for stress relaxation and lead to stress induced void formation in interconnects in the form of open circuit or substantial resistance increase [17]. Besides, the initial stress-induced voids can further deteriorate the EM lifetime of the interconnects as observed experimentally [53]. Recent studies have shown that SIV become more severe with the incorporation of low-k dielectrics [54].

At high temperature, the stress relaxation rate is depending on the initial thermal stress gradient and mass transport. Rhee *et al.* reported that Cu interconnect behave elastically due to the rigid confinement by the surrounding materials through x-ray diffraction [55]. Therefore, the thermo-mechanical stress can be assumed to be hydrostatic in the SIV studies for Cu interconnects.

SIV is tested through high-temperature storage (HTS) test. The interconnect is stress free at a temperature T_0 , close to the final annealing temperature. Samples are kept in an oven at temperature T below T_0 . The thermal mismatch increases with decreasing interconnect temperature, resulting in higher thermo-mechanical stress. The atomic diffusivity is depending on temperature as $D = D_0 e^{-E_A/k_B T}$. As interconnect temperature drops, the thermo-mechanical stress increases but the diffusivity decreases. Consequently, there is a critical temperature (T_{crit}) at which SIV lifetime is minimum. The median-time-to-failure (MTF) is fit to a semi-empirical relation [56]

$$MTF = \frac{C}{(T_0 - T)^N} e^{\frac{Q}{k_B T}} \quad (2.7)$$

where C and N are fitting parameters. The failure time approaches infinity when the test is performed at stress free temperature (SFT) T_0 or at absolute zero.

2.5 Conclusion

In this chapter, we begin with an overview of interconnect reliability issues which cover corrosion, whisker formation, hillock formation and TTDB. This is followed by the comparisons between Cu and Al interconnects from the reliability perspective. As we limit our scope to EM and SIV for interconnect reliability modeling in this thesis work, the fundamentals of EM and SIV are reviewed in Section 2.3 and Section 2.4, respectively.

Even EM and SIV are categorized under different failure mechanisms for interconnect reliability studies, the fundamental physics behind EM and SIV are the same as both are due to the mass transport under diffusion, arising from different driving force

along different diffusion paths. The two are not to be confused as EM is tested under high temperature and high current while SIV is tested only through high temperature baking. The difference is the driving force can be different in the case of EM and SIV. The detailed studies of EM and SIV can be found in Chapter 4 and Chapter 5, respectively.

3. FINITE ELEMENT ANALYSIS (FEA)

3.1 Why choose FEA for reliability modeling

The nature of EM and SIV are caused by the diffusion of interconnect material under different driving forces due to severe mechanical and electrical loading, e.g. electron wind force, thermal gradient induced driving force, stress gradient induced driving force, etc. Therefore, it is important to understand how these driving forces and the coupling effect between different driving forces are affected by the test conditions, the interconnect geometry, the interconnect composition materials, etc. Besides, the actual interconnect are 3D in nature in their physical implementation so 3D modeling is essential for the reliability study of today's interconnects.

It is often necessary to obtain the approximate numerical solutions for complex engineering problems, in which exact close-form solutions are difficult to obtain, e.g. the temperature distributions during cooling of integrated circuit chips, the current density distribution in multi-level interconnects, etc. Although it is possible to derive the governing equations and boundary conditions from first principles, it is difficult to obtain any form of analytical solution to such problem. This complexity arises due to the fact that the geometry, the boundary conditions, or the material compositions can be highly irregular or arbitrary. In these situations, numerical methods can be employed to obtain the approximate solutions. Different numerical methods have been developed to solve the differential equations in 3D coupled-field problems, e.g. finite element method, finite difference method, finite volume method, etc.

With finite difference method, the differential equation is written for each node, and the derivatives are replaced by difference equations. This approach results in a set of simultaneous linear equation. The accuracy can be improved by increasing the number of nodes. Although finite difference method is easy to understand and employ in simple problems, it becomes difficult to apply to problems with complex geometry or complex boundary conditions. Compared to the finite difference method, it is reported that finite element method can treat irregular geometry and offer improved accuracy and efficiency [57]. The finite volume method is a further refined version of the finite difference method and has become popular in computational fluid dynamics (CFD).

Finite element method is a numerical technique for finding approximate solutions of partial differential equations (FDE) as well as of integral equations. It has wide applications and enjoys extensive utilization in the structural, thermal and fluid analysis areas because of its diversity and flexibility as an analysis tool. Finite element method divided the solution region into many small elements and the characteristic of each element can be determined by the piece-wise approximations. This reduces the complex partial differential equations to either linear or nonlinear simultaneous equations. Through the finite element discretization, the continuum problem with infinite number of unknowns is simplified to one with a finite number of unknowns at specified points referred as nodes. Several approaches can be used to transform the physical formulation of the problem to its finite element discrete model. The commonly used approaches are Ritz method, Rayleigh method and weighted residual methods. For the detailed descriptions of these methods, one may refer to [58].

For interconnect reliability modeling, finite element method has been used extensively in both on chip interconnect and solder joint modeling [22, 59-63]. The commercial finite element software ANSYS[®] is employed throughout this research work.

3.2 Finite element formulations for thermal analysis

Heat analysis is very important in microelectronics devices as too much heat can accelerate electromigration, stress migration, or even lead to device melting. Heat transfer is the energy transfer process resulting from the temperature differences in devices. The simulated temperature distribution can be used to model the temperature dependent phenomena which in turn affect device reliability significantly, e.g. diffusion, thermo-mechanical stress, etc.

The three basic modes of heat transfer are conduction, convection and radiation. For heat conduction, the heat transfer rate per unit area based on *Fourier's law* for one dimension is expressed as [58]

$$q_x = -k \frac{dT}{dx} \quad (3.1)$$

where q_x is the heat flux along the x direction ($\text{pW}/(\mu\text{m})^2$), k is the thermal conductivity ($\text{pW}/(\mu\text{m}\cdot\text{K})$), and dT/dx is the temperature gradient ($\text{K}/\mu\text{m}$).

For heat transfer by convection, the flux heat flux equation is given by *Newton's law of cooling* as [58]

$$q = h(T_w - T_a) \quad (3.2)$$

where $(T_w - T_a)$ is the temperature difference between the wall and the fluid, h is the convection heat transfer coefficient ($\text{pW}/(\mu\text{m})^2 \cdot \text{K}$).

A basic equation for heat transfer can be expressed as [58]

$$-\left(\frac{\partial q_x}{\partial x} + \frac{\partial q_y}{\partial y} + \frac{\partial q_z}{\partial z}\right) + G = \rho c \frac{\partial T}{\partial t} \quad (3.3)$$

where G is the heat generation per unit volume, ρ is the density and c is the specific heat. The first term in Eq. (3.3) stands for the heat transferred to the control volume (conduction, convection or radiation), the second term represents the internally generated heat (e.g. Joule heating), and the last term is heat stored in the control volume.

Consider the case where the heat transfer is through conduction, substitute Eq. (3.1) into Eq. (3.3) and assume an isotropic thermal conductivity [64], we have

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{G}{k} = \frac{1}{\alpha} \frac{\partial T}{\partial t} \quad (3.4)$$

where $\alpha = k / \rho c$ is the thermal diffusivity, which is important in the transient heat transfer analysis. In the analysis of steady state conduction with no heat generation, Eq. (3.4) can be simplified as

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0 \quad (3.5)$$

The analysis becomes nonlinear if the material properties are dependent on temperature. There are two types of boundary conditions: *Dirichlet* condition and *Neumann* condition.

For *Dirichlet* condition, the temperature of the boundary is known:

$$T = T_0 \text{ on } \Gamma_T \quad (3.6)$$

For *Neumann* condition, heat flux is imposed on the boundary

$$q = -k \frac{\partial T}{\partial n} = C \text{ on } \Gamma_{qf} \quad (3.7)$$

In Eqs. (3.6) and (3.7), Γ is the boundary surface, n is the outward direction normal to the surface, and C is the given constant flux. It can be seen that convection heat transfer boundary condition falls into *Neumann* category.

3.3 Analysis procedures

ANSYS[®] is able to perform various types of analysis, ranging from a simple, linear, static analysis to a complex, nonlinear, transient dynamic analysis. A typical ANSYS[®] analysis comprises three steps:

- a) Pre-processing: a finite element mesh is developed to divide the geometry into sub-domains for mathematical analysis, and applies material properties and boundary conditions.
- b) Solution: the governing matrix equations are derived from the model and solved for the primary quantities.
- c) Post-processing: the validity of the solution is checked, the values of the primary quantities (such as displacement and stresses) are examined, and additional quantities (such as specialized stresses and error indicators) are derived and examined.

3.3.1 Pre-processing

In pre-processing, the analyst needs to develop an appropriate finite element mesh, assign suitable material properties, and apply boundary conditions in the form of restraints and loads. The finite element model comprises nodes and elements, which

describes the realistic model geometry. The nodes, which are point locations in space, are generally located at the element corners and sometimes at each middle point.

ANSYS[®] element library contains more than 150 different element types. The element type determines the degree of freedom (DOF) set at each node, which implies the discipline of the analysis (structural, thermal, magnetic, electrical, etc). The element shape (1D, 2D or 3D) is also determined by element type. Each element type requires material properties. Linear material properties can be constant or temperature-dependent, and isotropic or orthotropic. Nonlinear material properties are usually tabular data, such as plasticity data (stress-strain curves for different hardening laws), creep data, etc. Different 1D, 2D, 3D element are summarized in Figure 3.1.

Figure 3.1: Different 1D, 2D and 3D basic elements

There are two methods to create the finite element model: solid modeling and direct generation. With solid modeling, the analyst describes the geometric boundaries of the model, establishes control over the size and desired shape of the elements, and then instructs the ANSYS[®] program to generate all the nodes and elements automatically. In contrast, with the direct generation method, the analyst determines the location of every node and the size, shape, and connectivity of every element prior to defining these entities in the ANSYS[®] model. The direct generation can become tedious for large models, contributing to the potential modeling errors. Solid modeling is usually more powerful

and versatile than direct generation, and is commonly the preferred method for model creation.

With solid modeling, once the geometric shape of the model is described, ANSYS® can mesh the geometry with nodes and elements automatically. The geometry can be meshed with an automatic free-meshing algorithm or a mapping algorithm. Free-meshing automatically subdivides meshing regions into elements, with the advantages of fast meshing, no restrictions in terms of element shapes, and adaptive capabilities. Compared with free mesh, a mapped mesh is restricted in terms of element shape and the pattern of the mesh. With mapped mesh, the geometry can be meshed with accurate and efficient solid linear 3D element, improving solution accuracies. The smaller the element size or the higher the element order, the better the mesh will represent the real geometry. Figure 3.2 shows the finite element model for Cu interconnects by mapped mesh. Only Cu and diffusion barrier layer Ta are shown in the figure.

Figure 3.2: Finite element model for Cu interconnect by mapped mesh with surrounding materials removed.

Boundary conditions include restraints as well as other externally and internally applied loads. Examples of restraints are declaring a nodal translation or temperature.

Examples of loads in interconnect modeling are convections, voltage, electrical current, and heat flux. They can be applied either on the solid model (keypoints, lines, and areas) or the finite element model (nodes and elements). The applied boundary conditions are based on the discipline of the analysis and the boundary conditions for the typical analysis used this thesis work is summarized in Table 3.1.

Table 3.1: Boundary conditions for typical analysis types used in this thesis work

Analysis type	Restraints	Loads
Electrical-thermal	Temperature, Voltage	Heat flux, Heat generation rate, Radiation
Thermal-mechanical	Displacement	Pressure, Temperature

3.3.2 Solution

During the solution phase of an analysis, the governing equations for each element are calculated, assembled into matrix form and then solved numerically by the computer. The assembly process depends not only on the type of analysis (e.g. static or dynamic), but also on the model's element types and properties, material properties and boundary conditions. The individual element equations are assembled into the system equations, which describes the behavior of the body as a whole. They generally take the form:

$$[K]\{U\} = \{F\} \quad (3.8)$$

$$[K]\{T\} = \{f\} \quad (3.9)$$

Equations (3.8) and (3.9) are the matrix equation for structural analysis (thermo-mechanical analysis) and thermal analysis (electrical-thermal) analysis. In structural analysis, $[K]$ is a square matrix known as the stiffness matrix, $\{U\}$ is the vector of unknown nodal displacement, and $\{F\}$ is the vector of the applied nodal forces. In thermal analysis, $[K]$ is the thermal stiffness matrix, $\{T\}$ is the vector of unknown temperatures and $\{f\}$ is the thermal load. Before the equation can be inverted and solved

for $\{U\}$ or $\{T\}$, boundary conditions must be applied. In structural analysis, the body must be restrained from rigid body motion. For thermal problems, the temperature must be defined at one or more nodes.

ANSYS[®] provides different solvers in an analysis such as Sparse-Direct-Solver, PCG solver, JCG solver, etc. Each solver is optimized for different applications. For details, one can refer to the ANSYS[®] documentation [65].

3.3.3 Post-processing

The results of the analysis can be investigated in post-processing phase. Post-processing begins with a thorough check for problems that may have occurred during solution. Once the solution is verified to be free of numerical problems, the quantities of interest may be examined. For example, the displacement of a solid linear brick element's node is a 3-component spatial vector, and the model's overall displacement is often displayed by superposing the deformed shape over the undeformed shape. Stresses, being tensor quantities, currently lack a good single visualization technique, and thus derived stress quantities (von Mises stress, hydrostatic stress, etc) are extracted and displayed.

3.4 Application of FEA in interconnect modeling

3.4.1 Thermo-mechanical stress

Since process temperature can go up to 400 °C during annealing and the deposition of dielectrics, the thermal stress in the metal lines can reach a level of hundreds of MPa.

High tensile stress can cause void formation. Thermo-mechanical stress can be characterized by either beam bending technique or X-ray diffraction (XRD) [66, 67]. Beam bending technique can be used to determine the average stress of a thin layer deposited on a rigid substrate using modified Stoney's equation, while XRD gives the principle stresses in selected grains of the crystal films. However, neither of the methods can determine the local stress distribution and the stress in patterned dielectric materials. Finite element analysis can reveal the local stress not only in the metal lines, but also in patterned dielectric and other materials, providing useful insights into the stress-related reliability issues in Cu metallization [55, 68-70].

The stress simulation is through coupled field thermo-mechanical analysis. Hydrostatic stress distribution for Cu/low-k interconnects is shown in Figure 3.3. Von mises stress distribution is shown in Figure 3.4. The boundary conditions will be described in details in Chapter 5.

Figure 3.3: Hydrostatic stress distribution. Test temperature is at 300 °C and stress free temperature is at 350 °C. Unit: MPa.

Figure 3.4: Von Mises stress distribution. Test temperature is at 300 °C and stress free temperature is at 350 °C. Unit: MPa.

3.4.2 Current crowding

The current density is not uniform in via structure in interconnects. It is shown that current is crowded at the inner corner of a bend conductor. Current crowding phenomenon also appears in solder bumps. For Cu interconnects, current crowding occurs at the inner corner of via bottom. For flip chip solder bump, the current crowding region is near the intersection of the chip interconnect and the solder bump where the current density changes abruptly in the solder bump [71]. In a current crowded zone, not only the current density is non-uniform in the interconnects, the temperature distribution is also non-uniform since the current and temperature are coupled to each other in an electrical conductor [72]. The local temperature can be higher than the test temperature due to Joule heating effect. The non-uniform temperature distribution in turn produces non-uniform thermo-mechanical stress distribution in the current crowding region. To obtain quantitative understanding of the magnitudes and distributions of electrical current densities around current crowding region, FEA is employed extensively [71, 72].

Coupled field electrical-thermal analysis is used to simulate the current density distribution. Temperature distribution and its gradients can also be obtained. Current

density distribution and temperature gradient distributions for Cu/low-k interconnects are shown in Figure 3.5 and Figure 3.6, respectively. Figure 3.7 shows the current density distribution for flip chip solder bump. The boundary conditions will be described in details in Chapter 4.

Figure 3.5: Current density distribution in Cu/low-k interconnects. Unit: pA/ μm^2 .

Figure 3.6: Temperature gradient distribution in Cu/low-k interconnects. Unit: K/ μm .

Figure 3.7: Current density distribution in flip chip solder bump. Unit: $\text{pA}/\mu\text{m}^2$.

3.5 Effect of element shape and meshing density on solution accuracy

Elements are organized into groups of similar characteristics. According to element names, elements are grouped as PLANE, SOLID, SHELL, etc. The basic element shapes have been summarized in Figure 3.1. According to element order, they can be divided as linear and quadratic. Element order refers to the interpolation of an element's nodal results to the interior of the element. Linear elements do not have mid-side nodes. In general the strain can only vary linearly from one node to another. Quadratic elements have mid-side nodes. The shape function for strains is in 2rd order and is more accurate for a given numbers of nodes in the model. It is stated in the ANSYS[®] manual that, for linear elements (no mid-side nodes), it is not recommended to use the tetrahedral forms of 3D linear elements in thermo-mechanical simulations [65]. To achieve better accuracy and efficiency, hexahedral elements are preferred for 3D meshes. However, one disadvantage of using hexahedral elements is that only regularly shaped rectangular type volume can be meshed into hexahedral elements. While for tetrahedral mesh, it can be

used to mesh any volume. There is no general rule to decide which element shape should be preferred for a particular simulation. To gain a better understanding between the finite element model and solution accuracy, a group of simulations using different element shapes are performed so that the effect of element shapes on the simulation accuracy can be compared. The simulation results can provide a general guideline for our finite element simulations.

A simple Cu line via structure is chosen for illustration. Three finite element models with different meshes have been chosen to be compared with a benchmark finite element model. For the benchmark model, linear hexahedral elements are employed at an extremely high mesh density so the simulation results from this benchmark model are assumed to be ideal. The other three finite element models are meshed with linear hexahedral elements, linear tetrahedral elements, and quadratic tetrahedral elements at the same meshing density. Therefore, the effect of meshing density on the simulation results accuracy can be excluded. As the simulation is divided to coupled field electrical-thermal and coupled field thermal-mechanical analysis, the element types chosen for the simulations are summarized in Table 3.2. It is noted that other element types may also be used in Table 3.2 as long as the element shape and order are the same. For example, *solid92* can also be used to replace *solid98* for thermo-mechanical analysis. The simulation results will remain the same. The four finite element models are shown in Figure 3.8.. Therefore, the variations in the simulation results will be attributed to the element shape and element order.

Table 3.2: Selected element types for various element shapes and simulation physics.

	Linear Hexahedron	Linear Tetrahedron	Quadratic Tetrahedron
Electrical-thermal	Solid69	Solid69	Solid98
Thermo-mechanical	Solid45	Solid45	Solid98

Figure 3.8: Finite element model by different mesh method (a) Benchmark linear hexahedral mesh 283680 nodes (b) Linear hexahedral mesh 135450 nodes (c) Linear Tetrahedral mesh 131994 nodes (d) Quadratic tetrahedral mesh 132475 nodes.

Simulation results are summarized in Table 3.3. By comparing the simulation results from the benchmark model to other models, the results of linear tetrahedron model deviate most from the results of benchmark model. From the hydrostatic stress results in Table 3.3, it can be seen that the results from linear hexahedron model is the most close to the benchmark model. The results from quadratic tetrahedron model are slightly further apart. This suggest that, at the same mesh density, the simulation accuracy in descending order can be linear hexahedron mesh, quadratic tetrahedron mesh, linear tetrahedron mesh. Therefore, linear tetrahedron elements are not recommended for thermo-mechanical analysis due to their high stiff matrix in Eq. (3.8) [73]. Quadratic tetrahedral elements can be used if hexahedral mesh is difficult.

Table 3.3: Simulation results for Cu line via structures with different meshes

	Thermal (K/°C)	gradient	Hydrostatic (MPa)	stress	Stress (MPa/μm)	gradient
Benchmark	0.117×10^{-3}	~0.16714	85.728~126.323		0.726768~2201	
Linear Hexahedron	0.167×10^{-3}	~0.158901	85.891~122.476		1.054~1870	
Linear Tetrahedron	0.785×10^{-4}	~0.213673	79.321~186.265		3.153~10429	
Quadratic Tetrahedron	0.113×10^{-3}	~0.163453	85.921~139.139		2.584~2848	

3.6 Effect of substrate thickness

In the electrical-thermal analysis of interconnects, the actual substrate is 300 μm in thickness and the dimension of interconnect has been scaled down into submicron regime. In order to obtain realistic simulation results, the full substrate thickness has to be modeled in the finite element analysis, resulting in a very large finite element model and long simulation time. In fact, the substrate thickness has a strong effect on the simulation results as the heat transfer through substrate is the dominant thermal path [74]. The overall thermal resistance is found to be linearly proportional to the substrate thickness and the convection can be ignored due to the small dimension of the interconnects [75].

Based on the fact that overall thermal resistance is linearly proportional to substrate thickness and substrate is the dominant thermal path for Joule heat dissipation, the finite element model can be adjusted to reduce the finite element model size without compromise on the simulation accuracy.

A thin Si substrate is used in the modeling (e.g. 0.2 μm) and the thermal conductivity for Si substrate is downscaled in proportion to the substrate thickness down scaling. Two groups of electrical-thermal simulations were performed to verify the above proposals. One group is using the true Si substrate, from 0.2 to 20 μm. The other group is using a fixed Si substrate thickness at 0.2 μm. The thermal conductivity is downscaled

accordingly as if the substrate thickness has been increased. For example, the thermal conductivity of Si is downscaled 100 times to simulate a substrate thickness of 20 μm for a 0.2 μm substrate thickness in the finite element model. The simulation results are summarized in Figure 3.9. It can be seen that the simulated temperature through thermal conductivity downscaling (dotted curve) overlaps with the one with varying substrate thickness (solid curve) very well. Therefore, this method helps to reduce the finite element size without compromising the simulation accuracy. It can also be used in other microelectronic structure where the substrate thickness is much larger than the device under interest.

Figure 3.9: Temperature increment by Joule heating

3.7 Conclusion

In this chapter, a detailed description of the finite element analysis including the basic FEA concept, FEA formulation, analysis procedures is presented. The application of FEA in interconnect modeling is illustrated with examples. The issues of element shape, meshing density and substrate thickness in the finite element modeling for interconnects

are elaborated. The applications of FEA in EM and SIV modeling are detailed in the following two chapters.

4. ELECTROMIGRATION

4.1 Introduction

The most fundamental aspect of EM is diffusion which can occur through several different diffusion paths. The effect of surrounding materials and interconnect geometry on EM is taken into account through the modification of atomic diffusivity. This is called diffusion path approach in EM studies [15, 76]. With the continuous scaling of the interconnect dimensions, besides electron wind force, other driving forces are becoming important and each driving force needs to be considered individually in the EM modeling. This is so called driving force approach [21, 22, 59, 72]. The detailed descriptions of the two approaches and their comparisons will be shown in Section 4.2. The methodology developed for finite element modeling of EM by the driving force approach is detailed in Section 4.3.

There are several factors that can significantly affect EM reliability. The interconnect geometry and interconnect materials are the most crucial ones. For the interconnect geometry, EM reliability has been investigated for different geometries for EM test structures, e.g. reservoir effect [77, 78], gouging via [69], line width scaling [79], multiple via [16], width transitional structures [80], barrier layer scaling [81], etc. Also EM performance deteriorates with the implementation of low-k inter-level dielectrics (ILD), attributed by the poor confinement by the low-k ILD as well as the poor passivation effect for low-k materials [82-84]. The reservoir effect in EM including the experiment, the numerical analysis of lifetime enhancement factor will be described in Section 4.5.1.

Section 4.5.2 focuses on the effect of width transitional structures on EM. The Blech effect is compared between SiO₂ and low-k ILD interconnects by FEA with inelastic behavior of Cu considered in Section 4.5.3.

The EM test is usually performed with test temperature from 200 to 350 °C and current density of several mega-amp/cm². As the actual interconnect temperature plays an important role in the time to failure through Black's equation (Eq. (2.6)), accurate measurement of the interconnect temperature, including the Joule heating effect, is important in EM test [85]. In Section 4.6, we show how the variations of the interconnect temperature affects the experimentally determined activation energy E_A and current density exponent n .

4.2 Diffusion path and driving force approach in Electromigration

4.2.1 Diffusion path approach

In diffusion path approach, electron wind force (EWF) is considered as the only source of driving force for EM mass transport. All the other driving forces are accounted for by the modifications of atomic diffusivities in various diffusion paths. The total mass transport is the sum of the separate quantities of mass moving through the lattice, the grain boundaries, surfaces, and the interfaces. All the potential diffusion paths are shown schematically in Figure 4.1. The typical activation energy for different diffusion paths are listed in Table 4.1 [86].

Figure 4.1: Different diffusion paths: 1, bulk; 2, grain boundary; 3, grain/bulk; 4, defect; 5, surface.

Table 4.1: Activation energy for different diffusion paths [86]

Metallization	Activation energy (eV) for different diffusion paths			
	Bulk	Grain Boundary	Surface	Interface
Al	1.4	0.6	NA	?
Al/Cu (alloy)	1.2	0.7	NA	0.9-1.0
Cu	2.1	1.2	0.7	0.8-1.2

As shown in Table 4.1, the surface diffusion in Al and its alloys is unavailable since it is blocked by its native oxide. Hence Al and its alloys show grain boundary dominated EM failure. For Al interconnect, when the line width is less than the grain size, the microstructure of the Al line becomes bamboo and no grain boundaries are available for long range mass transport. So the primary diffusion path is eliminated due to microstructure evolutions and the dominant diffusion path migrates to the interface. Hence the mean time to failure (MTTF) is improved greatly [87].

Taking into account all the possible diffusion paths, the EM drift velocity can be obtained as

$$v_d = \frac{DZ^*}{k_B T} e \rho j \quad (4.1)$$

where effective DZ^* can be written as

$$DZ^* = D_b Z_b^* f_b + D_d Z_d^* f_d + D_i Z_i^* f_i + D_s Z_s^* f_s + D_{gb} Z_{gb}^* f_{gb} \quad (4.2)$$

The subscripts in Eq. (4.2) denote various diffusion paths as follows: b: bulk, d: dislocation, i: interface, s: surface, gb: grain boundary with f as the fraction of atoms diffusing through a given path way. Beside the diffusivity, the effective valence number is also different along different diffusion path as the electron wind force varies according to the local environment surrounding an atom [88]. In the typical EM process, the contribution from 'bulk' is significantly small compared with others. Thus in the interconnect EM reliability assessment, dislocation, interface, surface and grain boundary paths are of paramount importance.

Although the bulk activation energy of Cu interconnect is much larger than that of Al interconnect, their interface activation energy are almost the same, due to the non-protective Cu surface. Hence, the EM failure in Cu interconnects is interface dominated. The interfaces at the side walls and the bottom (Cu/Ta) or the top of lines (Cu/SiN) are the fast diffusion path as shown in Figure 4.2. Hence, the interface quality is critical to the EM reliability for Cu interconnects.

Figure 4.2: TEM cross sectional image of Cu damascene interconnect [89].

4.2.2 Driving force approach

As line width becomes narrow, the effects of the surrounding materials on EM can no longer be accounted for by the modification of the atomic diffusivity alone as was described in the above-mentioned diffusion path approach. In fact, the effects are so strong that they can counteract the electron wind force, and thus constitutes different types of driving forces during EM in interconnects. Three important driving forces are considered in this work: electron wind force (EWF), temperature gradient induced driving force (TGIDF), and thermo-mechanical stress gradient induced driving force (SGIDF).

The importance of driving force approach is illustrated through the Al based line via structure studies in the work by Tan *et al.* [21]. From their work, it is shown that, with the continuous line width scaling, the void nucleation site will migrate from the inner corner of via to the outer corner of the line-via interface for Al based metallization and this conclusion is further confirmed by their experimental results.

Atomic mass transport cannot induce failure unless there is a non-zero atomic flux divergence (AFD). Thus for a given section of interconnect, if $\nabla J=0$, the material entering into and flowing out from the section is the same. On the other hand, $\nabla J \neq 0$, mass accumulation (i.e. when $\nabla J < 0$) or depletion (i.e. when $\nabla J > 0$) occurs and this results in EM failure in the form of hillocks and voids.

In the presence of the inhomogeneity of the microstructure/texture, the atom diffusivity is altered along a diffusion path, and AFD is produced. Besides, there are many other causes for AFD to occur in interconnects. One was reported to be the non-uniform grain structure and their orientations [12]. A typical example is the void forms at the triple point of grain boundary [90]. Another cause of AFD is the local grain size

variation as shown schematically in Figure 4.3. Significant mass accumulation can occur at the grain boundary from small to large grains, whereas a corresponding mass depletion proceeds at the boundary from large to small grains. Besides the microstructure induced AFD, the structural changes in the direction of flux can also cause AFD. Such structure induced AFD are typically observed at the end of conductors where perfect blocking boundaries exists, inner corner of via where current crowding is located [72], etc.

Figure 4.3: AFD due to grain size variation.

4.2.3 EM lifetime estimation by driving force approach

In driving force approach, the diffusion time of metal atoms in interconnects is indirectly coupled with the interacting fields such as current, temperature, stress, etc. This approach is mainly manifested by Tan *et al.* [20-22, 40, 72] after the basic formulation by Dalleau *et al.* [91]. Recently, Tan *et al.* [22] proposed new AFD formulations by overcoming the weakness of preexisting ones and this will be detailed in Section 4.3.

A simple relation between EM lifetime and AFD can be derived as follows. AFD formulations by EWF, TGIDF, and SGIDF are expressed in Eqs. (4.3)-(4.5) [91]

$$\text{div}(\mathbf{J}_A) = \left(\frac{E_A}{k_B T^2} - \frac{1}{T} + \alpha \frac{\rho_0}{\rho} \right) \mathbf{J}_A \nabla T$$

$$(4.3) \text{div}(\mathbf{J}_{th}) = \left(\frac{E_A}{k_B T^2} - \frac{3}{T} + \alpha \frac{\rho_0}{\rho} \right) \mathbf{J}_{th} \nabla T + \frac{NQ^* D_0}{3k_B^3 T^3} j^2 \rho^2 e^2 \exp\left(-\frac{E_A}{k_B T}\right)$$

$$(4.4)$$

$$\begin{aligned} \text{div}(\mathbf{J}_s) = & \left(\frac{E_A}{k_B T^2} - \frac{1}{T} \right) \mathbf{J}_s \nabla T + \frac{2E\alpha_l N \Omega D_0}{3(1-\nu)k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \left(\frac{1}{T} - \alpha \frac{\rho_0}{\rho} \right) \nabla T^2 \\ & + \frac{2E\alpha_l N \Omega D_0}{3(1-\nu)k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \frac{j^2 \rho^2 e^2}{3k_B^2 T} \end{aligned} \quad (4.5)$$

where $\mathbf{J}_A$, $\mathbf{J}_{th}$ and $\mathbf{J}_s$ are referring to the atomic flux by the respective driving forces as shown in Eqs. (4.21)-(4.23). It is noteworthy that AFD and N in the above equations are referring to the instantaneous values. The physical time factor for the EM process is coupled to the driving forces by means of additional equations as shown below. By adding Eqs. (4.3)-(4.5), the total AFD can be expressed as,

$$AFD_{total} = N \cdot F(j, T, \sigma_H, E \dots) \quad (4.6)$$

Equation (4.6) shows that instantaneous total AFD is linearly proportional to instantaneous local atomic concentration N in the space domain. Besides that, the instantaneous AFD is also related to the instantaneous atom concentration in time domain. F in Eq. (4.6) is a function of various physical parameters in Eqs. (4.3)-(4.5). With the material balance equation

$$AFD_{total} + \frac{\delta N}{\delta t} - \frac{\delta C}{\delta t} = 0 \quad (4.7)$$

where N and C are the atom concentration and vacancy concentration, respectively. The vacancy contribution is at least five orders smaller than atomic contributions, thus it can be ignored [14]. Combining Eqs. (4.6) and (4.7),

$$N \cdot F + \frac{\delta N}{\delta t} = 0 \quad (4.8)$$

The theoretical solution for Eq. (4.8) is

$$N = N_0 e^{-F \cdot t} \quad (4.9)$$

N_0 is the initial atomic concentration. In order to eliminate F in Eq. (4.9), Eq. (4.9) is rewritten as

$$F = \frac{1}{t} \ln \frac{N_0}{N} \quad (4.10)$$

Substitute Eq. (4.10) into Eq. (4.6) and rearrange,

$$\left(\frac{N}{N_0} \right)^N = e^{-AFD \cdot t} \quad (4.11)$$

Equation (4.11) is a closed form equation depicting the relationship between the instantaneous atom concentration, instantaneous total AFD and time. From Eq. (4.11), it is revealed that local atom concentration is related to the product of the total AFD and time. Eq. (4.11) can be rearranged as

$$t = \frac{N}{AFD} \ln \frac{N_0}{N} \quad (4.12)$$

Eq. (4.12) shows that EM lifetime is inversely proportional to the AFD value. Hence it is highly desirable to reduce the AFD in interconnects as to improve the EM lifetime.

In practical implementation, the void is assumed to nucleate at the maximum AFD site in the static EM simulation. Through this way, the weakest point prone to EM failure in the test structure can be located through FEM simulations [21, 72].

Following static simulation, dynamic simulation is needed if one wants to estimate the EM lifetime. In dynamic simulation, the elements corresponding to the maximum AFD values are physically deleted to simulate the growth of a void. The static equilibrium condition is maintained during the element removing process [92]. The element is considered to be empty (void) when the atom concentration is reduced to 10% of the initial atom concentration by mass transport [91]. From Eq. (4.12) the time needed to delete a particular volume can be written as

$$t = \frac{N}{AFD} \ln 10 \quad (4.13)$$

The elements can be deleted one after another during the void growing process and the time needed for each element deletion can be calculated by Eq. (4.13). This element deletion process stops if the line resistance increases by 10% and the total EM lifetime can be calculated. For details on the dynamic simulation, one can refer to the work by Tan *et al.* [22].

4.2.4 EM lifetime estimation by diffusion path approach

In diffusion path approach, Alam *et al.* [93] also proposed a systematic way to evaluate the EM lifetime. The effective diffusivity DZ^* for Cu and Al lines can be shown in Eqs. (4.14) and (4.15) by assuming all other diffusion paths have negligible contributions.

$$Z^*D = Z_s^*D_s\delta_s\left(\frac{2}{h}\right) + Z_{GB}^*D_{GB}\delta_{GB}\left(1 - \frac{d}{w}\right) \quad (4.14)$$

$$Z^*D = Z_s^*D_s\delta_s\frac{1}{h} \quad (4.15)$$

where D is the diffusivity with an Arrhenius dependence on temperature, Z^* is the effective valance number, δ is the diffusion interface width, and d , h , and w , are the grain size, line thickness, and line width, respectively. Subscript S denotes the Al/refractory metal liner interfaces and the Cu/cap interface for Al and Cu interconnect systems, respectively. Here, we have assumed a polycrystalline Al line with dominant diffusion path at grain boundary and interfaces. For Cu, bamboo structure is adopted with dominant diffusion path at Cu/cap interface.

Typically there are two types of EM failure: nucleation limited failure and growth limited failure. Nucleation limited failure will be most common in processes that do not contain a redundant shunt layer. Line is considered to have failed if the buildup of stress (EM-induced stress or backflow stress) reaches a critical level (critical stress). A critical tensile stress leads to void formation or a critical compressive stress causes dielectrics cracking. This critical stress has been formulated by Hou *et al.* [94]. When the void forms, a tremendous release of strain energy occurs which promotes very rapid void growth. In the absence of the shunt layer, an open circuit developed almost immediately. In this case, the time to failure will depend on the square of the inverse of current density (j^{-2}) in Black's equation [95, 96].

On the other hand, for growth limited failure, the failure depends on reaching a critical void size. The initial rapid growth of the void will not produce an open circuit due to the presence of the shunt layer. The void nucleation time is assumed to be negligible so most of the time is spent growing a critical void at the cathode end of the line. The time to failure will depend on the inverse of the current density (j^{-1}).

For nucleation limited EM failure, the time to void nucleation can be expressed in closed form using the critical stress σ_{crit} [97],

$$t_{nucleation} = \left(\frac{\sigma_{crit}}{\rho e Z^* D j} \sqrt{\frac{\pi k_B T \Omega D}{4B}} \right)^2 \quad (4.16)$$

where Ω is the atomic volume, ρ is the resistivity of the metal, and B is the effective bulk modulus of the surrounding materials.

For growth limited EM failure, the lifetime is the time needed to transport enough material to form a critical void. The lifetime can be formulated as [98]

$$t_{growth} = \frac{V_{crit} / \Omega}{J \cdot w \cdot h} \quad (4.17)$$

where V_{crit} is the critical void volume leading to EM failure, J is the net atomic flux as defined in Eq. (2.4). It should be take note here that J is the atomic flux in the electron wind force direction so it is only referring to the atomic flux contributed by electron wind force. Back flow stress can also be included in the calculation for short lines.

In reality, the test samples seldom follow exactly the nucleation limited or growth limited failure mechanism as described above. n is usually found to be between 1 and 2 in Black's equation. Clement attribute this by a "serial" model which describes nucleation followed by void growth. Park *et al.* [99] also proved that current density exponent changes from 1 to 2 when scaling from accelerated test conditions to field conditions due to a change in the failure mechanism.

4.2.5 Comparisons between the two approaches

Both driving force and diffusion path approaches have been implemented successfully in studying EM physics. The two approaches are not contradicting with each other, instead, they are complementary. In diffusion path approach, the diffusion along a particular diffusion path can be accelerated by other driving forces besides the electron wind force. Therefore, the atoms may not necessarily move along the electron wind force direction. Future studies should consider both the driving force and diffusion path in studying the EM physics.

Compared with diffusion path approach, there are still two main problems associated with the driving force approach as follows:

1. Lack of justifications for the AFD equations by TGIDF and SGIDF.

2. SGIDF considered in driving force approach may confuse with the SIV.

For point 1, the AFD formulations in Eqs. (4.4) and (4.5) for TGIDF and SGIDF are dominated by the current density distributions. For the electric current, its distribution is mainly determined by local resistivity. The current tends to flow in a low resistivity path. For temperature gradient, its distribution is mainly determined by the thermal conductivity. While for the thermo-mechanical stress gradient, the stress will be determined by the difference of thermal expansion coefficient (CTE) between the metallic material and surrounding materials. Therefore, Eqs. (4.4) and (4.5) needs to be re-examined to reflect the true driving force for EM failure. The AFD formulations by different driving forces are re-examined in Section 4.3.

For point 2, the SGIDF considered may bring the confusion with SIV as both are due to the high thermo-mechanical stress gradients in interconnects. In fact, the two are not confusing with each other as SGIDF is within the context of EM testing while SIV is a failure mechanism during high temperature storage test. Besides the EWF, SGIDF is also a dominant driving forces for void nucleation [20, 100] and possible void growth [22] in EM failure. For SIV, the failure is solely attributed to the thermo-mechanical stress. In conclusion, SGIDF and SIV are different failure phenomenon because they are studied under different test conditions using different test structures.

4.3 Improvement in the accuracy of finite element modeling of EM

Traditional EM models are based on the solutions of diffusion equations, and the electron wind force is proposed to be the sole driving force. The atomic diffusivity of

metal atoms are altered through either interconnect material microstructure or texture inhomogeneity, resulting in Atomic Flux Divergence (AFD) and hence the formation of voids and hillocks, rendering EM failure. The effect of the surrounding ILD and the structure geometry on EM is also taken into account through the modification of the atomic diffusivity. Such an approach to EM is called the diffusion path approach.

As interconnect line width shrinks to sub-micron level, the diffusion path approach is no longer valid as other driving forces become dominant, and this prompted the development of the driving force approach for the EM study by Rzepka *et al.*[59] in 1999. Dalleau *et al.* [91] provided a pioneer work to combine all the driving forces in their EM model using finite element method (FEM) in 2001, and the driving forces considered are the electron-wind force (EWF), the temperature gradient induced driving force (TGIDF) and the thermo-mechanical stress gradient induced driving force (SGIDF).

Tan *et al.* [20] also showed that the thermo-mechanical stress is the dominant driving force for Cu narrow interconnects failure. Recently, Li *et al.* [100] proved that the thermo-mechanical stress is the critical factor for vacancy nucleation at the interface of the barrier layer and the grain boundary using the combined Monte Carlo simulation and FEM approach.

However, as interconnects continue to scale down, we found that the conventional driving force formulation is no longer accurate in predicting void nucleation site as will be shown in this work. This inaccuracy arises from the fact that as line becomes extremely narrow, the assumptions made in the derivations for the conventional driving force formulation are no longer valid as will be detailed in the next section.

In view of the problems stated above, a modified driving force formulation is proposed. Finite element software ANSYS[®] is employed to construct the FE model for copper dual damascene (DD) structures. The validity of the model is verified through the study of the reservoir effect in EM.

4.3.1 Theoretical considerations

4.3.1.1 Problems with conventional driving force formulation

In the conventional driving force formulation, the following equations are used [20, 91]

$$\text{div}(\mathbf{J}_A) = \left(\frac{E_A}{k_B T^2} - \frac{1}{T} + \alpha \frac{\rho_0}{\rho} \right) \mathbf{J}_A \nabla T \quad (4.18)$$

$$\text{div}(\mathbf{J}_{th}) = \left(\frac{E_A}{k_B T^2} - \frac{3}{T} + \alpha \frac{\rho_0}{\rho} \right) \mathbf{J}_{th} \nabla T + \frac{NQ^* D_0}{3k_B^3 T^3} j^2 \rho^2 e^2 \exp\left(-\frac{E_A}{k_B T}\right) \quad (4.19)$$

$$\begin{aligned} \text{div}(\mathbf{J}_s) = & \left(\frac{E_A}{k_B T^2} - \frac{1}{T} \right) \mathbf{J}_s \nabla T + \frac{2E\alpha_l N \Omega D_0}{3(1-\nu)k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \left(\frac{1}{T} - \alpha \frac{\rho_0}{\rho} \right) \nabla T^2 \\ & + \frac{2E\alpha_l N \Omega D_0}{3(1-\nu)k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \frac{j^2 \rho^2 e^2}{3k_B^2 T} \end{aligned} \quad (4.20)$$

Equations (4.18)-(4.20) represent the AFD due to EWF, TGIDF and SGIDF respectively. In these equations, the following symbols refer to the interconnect material:

D_0 is the pre-factor of the self-diffusion coefficient,

E_A is the activation energy for the self-diffusion,

T is the local temperature,

Q^* is the heat of transport,

N is the atomic density,

Ω is the atomic volume ($\Omega = 1/N$),

j is the local current density,

E is the Young's modulus,

ν is the Poisson ratio,

α_l is the thermal expansion coefficient (CTE) of the metallic film,

ρ is the electrical resistivity which is dependent on temperature given as

$\rho = \rho_0 (1 + \alpha (T - T_0))$, and α is the temperature coefficient of resistivity, ρ_0 is the electrical resistivity at temperature T_0 . Other symbols are k_B which is the Boltzmann constant and e is the fundamental electron charge.

The atomic fluxes J_A , J_{th} , and J_s caused by EWF, TGIDF and SGIDF respectively can be modeled by Eqs. (4.21)-(4.23) below [11, 100, 101]

$$J_A = \frac{N}{k_B T} Z^* e \rho D_0 \exp\left(-\frac{E_A}{k_B T}\right) j \quad (4.21)$$

$$J_{th} = -\frac{NQ^* D_0}{k_B T^2} \exp\left(-\frac{E_A}{k_B T}\right) \nabla T \quad (4.22)$$

$$J_s = \frac{N\Omega D_0}{k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \nabla \sigma_H \quad (4.23)$$

In the derivations of Eqs. (4.19) and (4.20), the following energy balance equation in a thin film conductor at steady state is used [102],

$$j^2 \rho + K \nabla^2 T - \frac{k(T - T_s)}{th} = 0 \quad (4.24)$$

where K and k are the thermal conductivity of the metallic film and the dielectrics respectively, T and T_s are the temperature of the metallic film and the substrate respectively, t is the metallic film thickness, and h is the dielectric film thickness. The three terms in Eq. (4.24) represent Joule heating due to electrical current, lateral heat conduction along the plane of a film, and vertical heat conduction through the dielectrics into the substrate, respectively. The contributions by the three terms in Eq. (4.24) are calculated for Cu thin film with different thicknesses as shown in Table 4.2. As the line

thickness decreases, heat conduction through the dielectrics into the substrate increases dramatically. Therefore, it is inaccurate to ignore the last term as it was done in the conventional derivations. For realistic, the full substrate thickness of 300 μm is considered and the current density is assumed to be 1 MA/cm² in the analysis.

Table 4.2 Steady state power dissipation in a thin film conductor for different line thicknesses. As the line thickness decreases, heat conduction through the dielectrics into the substrate increases dramatically.

Line thickness(μm)	$J^2\rho(\text{pW}/\mu\text{m}^3)$	$K\nabla^2T(\text{pW}/\mu\text{m}^3)$	3 rd term of Eq. (4.24) ($\text{pW}/\mu\text{m}^3$)	Contribution by 3 rd term of Eq. (4.24)
3	3.46×10^6	3.26×10^6	0.2×10^6	6.1%
1	3.46×10^6	2.84×10^6	0.62×10^6	17.9%
0.325	3.46×10^6	1.56×10^6	1.9×10^6	54.9%
0.2	3.46×10^6	0.36×10^6	3.1×10^6	89.6%

Also, in the derivations of Eq. (4.20), the coupling effect between the hydrostatic stress and the temperature is considered and formulated as follows

$$\sigma_H = \frac{1}{3}(\sigma_{11} + \sigma_{22} + \sigma_{33}) = -\frac{2E\Delta\alpha_l}{3(1-\nu)}(T - T_{SFT}) \quad (4.25)$$

where σ_H is the hydrostatic stress in the interconnect, σ_{11} , σ_{22} and σ_{33} are stresses along the principal axes, T_{SFT} is the stress free temperature (SFT) of the interconnect, and $\Delta\alpha_l$ is the difference of the CTE between the interconnect metallization and the surrounding materials. Equation (4.25) is derived based on the Eshelby's inclusion model [103] and the cross section of the metal film was assumed to be an elongated ellipsoid in their analysis.

In reality, the cross section of a typical Cu interconnect is rectangular with cap layer on the top and diffusion barrier layers on the sidewalls and bottom, so Eq. (4.25) is insufficient in describing the coupling effect between the stress and temperature. In fact, the stress distribution is highly non-uniform due to the material and the structure inhomogeneities in interconnects. Through simulations, the thermo-mechanical stress distribution is strongly dependent on the structure geometry such as the line width, the

aspect ratio, the presence of via etc. The discrepancy will be even higher for narrow interconnects due to the increased thermo-mechanical hydrostatic stress as shown in Table 4.3. The volume-averaged stress shown in Table 4.3 is calculated using Eq. (4.26) given below

$$\sigma_{volume_ave} = \frac{\int_V \sigma_H dV}{\int_V dV} \quad (4.26)$$

The volumetric domain size in computing Eq. (4.26) is chosen to be relatively large such that further increasing in the size will only alter the result by less than 1%. The difference between SFT and test temperature is taken to be 50°C in the analysis.

Table 4.3: Hydrostatic stress comparisons between Eq. (4.25) and simulations for different line widths. The hydrostatic stress distribution evaluated by Eq. (4.25) is uniform whereas simulations reveal the stress distribution is highly dependent on the geometry of the structures.

Line width (μm)	Eq. (4.25) (MPa)	Simulation (MPa)		
		Min	Max	Volume-averaged
1	94.8	61	149	112.1
0.6	94.8	65.2	151	119
0.28	94.8	74.7	159	133
0.16	94.8	78.3	168	140.3

The two assumptions stated above encroach on the accuracy of the conventional driving force formulation in its application to narrow interconnects. In the present study, a modified driving force formulation for narrow interconnects is proposed and justified using experimental results in the literature.

4.3.1.2 Proposed driving force formulation and its improvement

From the atomic flux Eqs. (4.21)-(4.23), the divergence of the respective atomic fluxes can be derived based on the Green's theorem [104]

$$\text{div}(\mathbf{J}_A) = \left(\frac{E_A}{k_B T^2} - \frac{1}{T} + \alpha \frac{\rho_0}{\rho} \right) \frac{N}{k_B T} e Z^* \rho D_0 \exp\left(-\frac{E_A}{k_B T}\right) j g \nabla T \quad (4.27)$$

$$\text{div}(\mathbf{J}_{th}) = -\left(\frac{E_A}{k_B T^2} - \frac{2}{T} \right) \frac{N Q^* D_0}{k_B T^2} \exp\left(-\frac{E_A}{k_B T}\right) \nabla T g \nabla T - \frac{N Q^* D_0}{k_B T^2} \exp\left(-\frac{E_A}{k_B T}\right) \nabla g (\nabla T) \quad (4.28)$$

$$\text{div}(\mathbf{J}_s) = \left(\frac{E_A}{k_B T^2} - \frac{1}{T} \right) \frac{N \Omega D_0}{k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \nabla \sigma_H \cdot \mathbf{g} \nabla T + \frac{N \Omega D_0}{k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \nabla \mathbf{g} (\nabla \sigma_H) \quad (4.29)$$

Compared with the conventional driving force formulation, the new derivations are without the above-mentioned assumptions. For example, in Eq. (4.28) of the AFD due to TGIDF, vertical heat conduction through the dielectrics into the substrate is considered. For AFD due to SGIDF in Eq. (4.29), the coupling effect between the hydrostatic stress and the temperature is simulated by two coupled field analysis in ANSYS[®], the electrical-thermal and the thermal-mechanical analysis, without any assumption on the geometry of the structure. Furthermore, the directions of the respective driving forces are taken into consideration such that all the driving forces are represented as vectors and their interactions are represented by the dot product in Eqs. (4.27)-(4.29).

4.3.2 Model descriptions

The geometry parameters for FE models are taken from Refs. [77, 78] as shown in Table 4.4. By virtue of the symmetry of the structure, only half of the model is simulated. The Ta diffusion barrier and SiN cap layer are also included as shown in Figure 4.4. The material properties are taken from Ref. [40] and listed in Table 4.5. Six FE models with different reservoir lengths spanning from 0 to 0.125 μm are constructed. These EM models are subjected to a current density of 1.2 MA/cm² and a test temperature of 300 °C. The SFT is assumed to be 350 °C [20].

Table 4.4: Structural dimension list

Feature	Size(μm)
Line width	0.28
Line thickness	0.35
Via diameter	0.26
Via height	0.68
Barrier layer thickness	0.025
Cap layer thickness	0.05
Reservoir length	0~0.125
Silicon substrate thickness	300

Table 4.5: Material properties list

Mat.	Young's Modulus (GPa)	Poisson ratio	Thermal conductivity (W/mK)	Co-efficient of thermal expansion ($1/^{\circ}\text{K}$)
Cu	129.8	0.339	379	16.5×10^{-6}
Ta	186.2	0.35	53.65	6.48×10^{-6}
SiN	265	0.27	0.8	1.5×10^{-6}
SiO ₂	71.4	0.16	1.75	0.68×10^{-6}
Si	130	0.28	61.9	4.4×10^{-6}

Figure 4.4: Finite element model for reservoir EM study

4.4 Comparisons between the two driving force formulations

4.4.1.1 Void nucleation (static simulation)

The FE models developed consist of two steady state analyses, namely a direct coupled analysis with the current and the temperature fields, and an analysis with indirect

coupling between the temperature and the stress fields. The flow chart for the static EM simulation is shown in Figure 4.5.

In electrical-thermal analysis, the substrate bottom surface is kept at constant EM test temperature with constant current density applied. The nodal temperatures are then retrieved from this stage for use in the thermal-mechanical analysis. In the thermal-mechanical analysis, the following boundary conditions are applied: 1) the substrate bottom is fixed with zero displacement and 2) the vertical symmetric plane is constrained to remain vertical arising from the mirror symmetrical nature of the structure under consideration.

User subroutines were developed to calculate the divergence of temperature gradient and thermo-mechanical stress gradient in ANSYS[®]. The AFD contributions due to EWF, TGIDF and SGIDF are calculated using Eqs. (4.27)-(4.29) for the proposed method, and Eqs. (4.18)-(4.20) for the conventional driving force method. The void incubation time is assumed to be negligible [76]. The location of maximum positive AFD is taken as the void nucleation site [105].

Figure 4.5: Flow chart for the static EM simulation

Figure 4.6 and Figure 4.7 show the AFD distributions of the M2 structure using the proposed and the conventional formulations respectively. For easy visualization, all the other materials are removed in the figures and only the bare Cu is shown. One can see that the predicted void nucleation sites are different between these two methods. Conventional method predicts the void nucleation site at the inner corner of the via bottom as indicated by Figure 4.7. However, via bottom failure is proven to be the early failure due to process related defects [106] and it can be eliminated by via process optimization [107]. Hence, the prediction by the conventional formulation is incorrect in our defect-free model.

Figure 4.6: AFD distributions using the proposed FEM and the maximum AFD sites are labeled as “Location 1” and “Location 2” at Cu/SiN interface.

Figure 4.7: AFD distributions using the conventional FEM. The maximum AFD site is found to be at inner corner of via bottom.

On the other hand, the intrinsic EM failure in the M2 structure is predicted by the proposed method. There are two maximum AFD sites labeled as “Location 1” and “Location 2” in Figure 4.6, and both “Location 1” and “Location 2” are at the Cu/SiN interface. “Location 1” is located at the corner of the M2 line corresponding to the site of the maximum thermo-mechanical stress [108]. “Location 2” is located directly above the via and Vairagar *et al.* proved that it is indeed the void nucleation site using qualitative Monte-Carlo simulation [109]. In fact, the two potential void nucleation sites are well reported in literatures [108, 110]. Table 4.6 summarizes the contributions by the various driving forces for the atomic flux (AF) and AFD, and SGIDF is identified as the dominant driving force which also agrees with the studies by Shen *et al.*[111] and Tan *et al.*[72].

Table 4.6: AFD contributions of different driving forces

Driving force	Atomic Flux (atoms/ $\mu\text{m}^2\cdot\text{s}$)	Atomic Flux Divergence (atoms/ $\mu\text{m}^3\cdot\text{s}$)
EWf	6.54×10^{11}	1.34×10^8
TGIDF	4.45×10^8	1.83×10^9
SGIDF	7.36×10^{13}	5.69×10^{12}

4.4.1.2 Void growth (dynamic simulation)

After void nucleation, the voids begin to grow due to the continuous removal of materials from the void nucleation sites. The AFD value represents the rate of mass transport. Figure 4.8 shows the flowchart of the dynamic simulation. Twenty elements with the highest total AFD values are selected and physically deleted in each loop to simulate the void growth. The geometry of the FE model is then modified and this process repeats itself until the interconnect resistance increases by 10%. Figure 4.9 shows the FE model after an iteration of 20 loops. It can be seen clearly that the voids grow simultaneously at “Location 1” and “Location 2” at the beginning of the void growing process, in agreement to the experimental results reported [79].

Figure 4.8: Flowchart for the dynamic EM simulation

Figure 4.9: Void growth at “Location 1” and “Location 2” simultaneously after 20 iteration loops.

4.4.1.3 Critical reservoir length estimation

It is well-known that the introduction of reservoir as shown in Figure 4.10 can enhance the EM performance. However, it is also observed that the lifetime improvement ceases when the length of the reservoir is above a critical value. Gan *et al.* [77] introduced a concept of “effective reservoir volume” where only part of the extension volume is served as the reservoir for void accumulation. Shao *et al.* [78] postulated that the critical reservoir length may be partly attributed to the statistical nature of the failures. However, the mechanism of the limited lifetime enhancement due to reservoir remains unknown.

Figure 4.10: Schematic diagram of the cross sectional view of the reservoir region

In order to explore the mechanism through FEM, we examine the lifetime from the AFD calculations. The EM lifetime is inversely proportional to the volume-averaged AFD as can be derived below. In other words, AFD can be employed to predict the EM lifetime qualitatively.

Consider a control volume equal to the size of the critical volume of the void that causes 10% resistance increase in interconnects, i.e. the void volume at EM failure. If

$\overline{AFD}_{total,V}$ is the volume-averaged total AFD within the control volume, then by virtue of the conservation of mass, we have

$$\overline{AFD}_{total,V} + \frac{\delta N}{\delta t} - \frac{\delta C}{\delta t} = 0 \quad (4.30)$$

where C is the average vacancy concentration and N is the average atomic concentration within the control volume, respectively. Since the vacancy contribution is at least five orders smaller than the atomic contributions for the void formation, it can be ignored [14].

Integrate Eq. (4.30) gives

$$\int_{N_o}^0 dN = - \int_0^{TTF} \overline{AFD}_{total,V} dt \quad (4.31)$$

$$N_o = \overline{\overline{AFD}_{total,V}} \times TTF$$

where $\overline{\overline{AFD}_{total,V}}$ is the $\overline{AFD}_{total,V}$ averaged over the duration of TTF, and it reflects the average material depletion rate in the void growing process. TTF is the time to failure, i.e. the EM lifetime. Since N_o is the initial atomic concentration of the metal and is a constant for a given metal, we have the EM lifetime inversely proportional to the $\overline{\overline{AFD}_{total,V}}$ as shown in Eq. (4.31)

To have a closer look, when a void is formed inside a metal line, partial relaxation of the thermo-mechanical stress in the vicinity of the void is observed [111]. Further relaxation of stress can be realized by either plastic deformation or diffusion. Since EM test temperature is relatively high at 300 °C in our study, the thermo-mechanical stress is assumed to be released by diffusion [103], which leads to an increased SM driving force subsequently. As a result, the total AFD increases.

Figure 4.11 shows the variation of $\overline{AFD_{total,V}}$ within the control volume after each loop of iteration, depicting the progressive AFD growth as voids are growing. The fluctuation of the AFD in Figure 4.11 is due to the finite size of the elements used for the element deletion to simulate the void growth. As was derived earlier, one will take the mean of the volume-averaged total AFD for analysis as it is related to the EM lifetime, and this mean AFD is shown in Figure 4.11.

Figure 4.11: Volume-averaged AFD, $\overline{AFD_{total,V}}$ within the control volume during void growing process.

Figure 4.12 shows the $\overline{\overline{AFD_{total,V}}}$ at different reservoir length. $\overline{\overline{AFD_{total,V}}}$ is averaged over the number of loops simulated to reach the failure condition as described in Figure 4.8. One can clearly see that the $\overline{\overline{AFD_{total,V}}}$ decreases gradually with the reservoir length until a critical point of around $0.08 \mu m$, after which the $\overline{\overline{AFD_{total,V}}}$ remains constant. In other words, the void growth rate decreases as the reservoir length increases and correspondingly the EM lifetime increases till around $0.08 \mu m$. Further increase in the reservoir length does not decrease $\overline{\overline{AFD_{total,V}}}$, making the lifetime enhancement effect of the reservoir length ceases. The result is in close agreement with Gan *et al.* [77] who found that the critical length is around $0.06 \mu m$ using the same test structure and test

conditions studied here. On the other hand, the conventional formulation predicts the voids at via bottom, and hence no reservoir effect can be predicted by the conventional method.

Figure 4.12: Variation of the mean of the volume-averaged AFD, $\overline{\overline{AFD_{total,V}}}$, within the control volume with the reservoir length. $\overline{\overline{AFD_{total,V}}}$ decreases gradually with the reservoir length until a critical length of around $0.08 \mu\text{m}$.

4.4.1.4 Mechanisms of the reservoir length effect

From the above results, it is clear that the dominant driving force for the void formation is SGIDF in the reservoir region. High thermo-mechanical stress gradient is responsible for the void nucleation and the subsequent void growth is through stress relaxation in the form of diffusion. Current crowding effect is ignored in the analysis because the reservoir is a low current density region. Besides, it is also shown numerically that the effect of current-density gradient driving force is negligible [77].

Figure 4.13 explains the mechanism of reservoir effect schematically. In the case of the test structure without any reservoir extension as shown in Figure 4.13(a), “Location 1” and “Location 2” grow simultaneously in the beginning. After some time, the two voids collapse into a bigger void and form a critical void above via finally.

Figure 4.13: Void growing process in the reservoir region. (a) For Metal-2 structure with no reservoir extension, the initial two voids collapse into a bigger void and a critical void forms above via finally. (b) For Metal-2 structure with large reservoir extension, the critical void is solely developed from the initial void at “Location 2”.

However, in case of the test structure with a reservoir extension, the contribution by the void at “Location 1” to the final critical void decreases with increasing reservoir length due to the increased distance between “Location 1” and the via, and as a result, the $\overline{AFD}_{total,v}$ decreases. When the reservoir length increases beyond a critical value as shown in Figure 4.13(b), the void at “Location 1” will not be able to collapse with the critical void above via before the line fails. In other words, the critical void grows solely from “Location 2”, hence further increase in the reservoir length will not enhance the EM lifetime.

In short, the underlying physics of the reservoir effect is the decreasing probability of the void in the reservoir extension to be part of the critical void for EM as the reservoir length increases.

4.4.2 Summary

In this study, the inaccuracies of the conventional driving force FEM model for narrow interconnects are shown, and a refined driving force FEM to study the EM in narrow interconnects is proposed. The validity of the proposed method is demonstrated by applying the method to investigate the void nucleation sites, the void growth process and the reservoir effect on EM in copper dual-damascene (DD) interconnects. From the investigation, it is found that thermo-mechanical stress induced migration is the dominant driving force for void nucleation and growth in the M2 reservoir region. The physical mechanism of the reservoir effect is hence proposed in this work.

4.5 Effect of interconnect structure and materials on EM

4.5.1 Reservoir effect studies in Cu interconnect

As line-via structures are inevitable in ULSI multi-level metallization, and the number of line-via structures is increasing tremendously, EM in line-via structures is becoming more important. It is stated in [72] that the limiting factor in interconnect reliability is increasingly dominated by the EM performance of vias with the line playing a substantially lesser role in submicron technology.

Electromigration lifetime can be enhanced by adding a reservoir around the vias for both Cu and Al interconnects [77, 78, 109, 112-114]. The lifetime improvement ceases when the length of the reservoir is above a critical value. The lifetime enhancement factor M is defined as $MTTF_{reservoir} / MTTF_{noreservoir}$. It is known that the lifetime enhancement

factor M decreases with increasing EM test current or test temperature [113]. Decreasing M with increasing current density was observed experimentally in the work by Le *et al.* for Al interconnect [113]. However, the experimental proof between lifetime enhancement factor M and EM test condition for Cu interconnects is lacking, and the reason for changing M with changing EM stress condition remains unknown. The knowledge on the changing M with stress condition is necessary when extrapolating EM lifetime to normal operating condition for reservoir structures, and it is the purpose of this work to investigate the dependence of M on the stress conditions.

In this section, we show the EM experiment on M2 reservoir effect test structures and the experiment results are compared with the experimental results from literature. Our previous modeling results in Section 4.3 revealed that the thermo-mechanical stress gradient induced driving force (SGIDF) is the dominant driving force for intrinsic EM failure in M2 test structures [22], and this is also evidenced by experimental results from this work. In comparison to the previous work on the reservoir study for Cu interconnect [77, 78], we also found that M changes with the current density. We develop a model to explain such dependence as detailed below.

4.5.1.1 Experiment

M2 test structures of length 800 μm are fabricated using 180 nm copper/oxide dual damascene technology. The schematic of the cross section view is shown in Figure 4.14. Cu line thickness, line width, the thickness of Ta barrier layer and SiN cap layers are 0.35 μm , 0.28 μm , 25 nm and 50 nm respectively. Via diameter is 0.26 μm . M1 dummy lines (connected to pads) are made very short ($\sim 10 \mu\text{m}$) so that EM failure can be avoided in these dummy lines. Details of the fabrication process can be found in Ref. [72].

Figure 4.14: Schematic of M2 test structure

Three accelerated package level EM experiments are conducted using AETRIUMTM reliability tester. To investigate the reservoir effect on M2 test structure, structures with no reservoir, reservoir length of 0.06 μm and 0.12 μm respectively were tested at 300 $^{\circ}\text{C}$ with a current density of 2 MA/cm^2 . At least 12 samples are employed in each experiment, and the failure criterion in these experiments is 10% increase in the sample resistance. Transmission electron microscopy (TEM) was used for post-EM failure analysis. High quality of the samples is confirmed by the low variations of the initial sample resistances and their temperature coefficient of resistivity (TCR) as shown in our other work [115].

Our EM test structures are identical to those in the work by Gan et al. [77]. The only difference between their experiment and the present work is the current density where a lower current density of 1.2 MA/cm^2 was employed in their experiment. The Cumulative Distribution Function (CDF) plot for both experiments is shown in Figure 4.15, and the calculated log-normal σ are around 0.46 and 0.43 for 2 and 1.2 MA/cm^2 respectively. The very close σ implies the same failure mechanisms among the samples, making it meaningful to compare the experimental results between the two experiments.

Also from Figure 4.15, there is little lifetime enhancement by extending the reservoir length from 0.06 μm to 0.12 μm , where the enhancement factors are 1.25 and 1.3 at 0.06

μm to $0.12 \mu\text{m}$ respectively for stress current of 2 MA/cm^2 , and that for 1.2 MA/cm^2 are 2.9 and 3. Thus, the optimal reservoir length is around $0.06 \mu\text{m}$ for both experiments and it seem to be not significantly dependent on the stress current.

Figure 4.15: (a) CDF plot from the present work (b) CDF plot from Gan's experiment [77]

The estimated lifetime enhancement factors at the optimal reservoir length based on Figure 4.15 are found to be 3 and 1.3 for stress current density of 1.2 and 2 MA/cm^2 , respectively. This shows that the lifetime enhancement effect decreases with increased EM stress current for Cu interconnects.

The representative failure analysis image is shown in Figure 4.16(a) and Figure 4.16(b) for structure without reservoir and with $0.12 \mu\text{m}$ reservoir structure, respectively. It can be seen clearly that EM void is nucleated along Cu/SiN interface at the edge of the reservoir and grow along both line length and line thickness directions, resulting in partially spanning void in Figure 4.16(a) and fully spanning void in Figure 4.16(b), respectively. The failure modes between Figure 4.16(a) and Figure 4.16(b) are similar, in consistent with the same slope in CDF plot as observed in Figure 4.15. For M2 test structure, via bottom is often reported as the early failure site due to process related defects [106] and it can be avoided by via process optimization [107]. Early failure at via bottom is not observed in this experiment, indicating high quality of the sample

fabrication process. It is noted that the current crowding site (inner corner between M2 and via) is also clear from EM void in Figure 4.16(a) and Figure 4.16(b), implying that the EWF is not the dominant driving force for EM failure.

Figure 4.16: FA images through TEM (a) no reservoir (b) 0.12 μm reservoir

4.5.1.2 Evolution of driving forces

From the work reported by Tan et al. [72], stress gradient and temperature gradient indeed contribute to the EM failure, and their effects on EM seem to be more than just a modification of the flux divergence. Besides, with continuous scaling of interconnects, the dominant diffusion path has changed from grain boundary to Cu/cap interface and therefore a lower value of Z^* is reported for surface migration compared with grain boundary diffusion if the size effect is neglected [88], implying a decreasing electron wind force as atoms move from bulk to grain boundary to surface. The thermo-mechanical stress is also larger for nano-interconnects [22]. Hence, it is necessary to re-evaluate the strength of various driving forces present through finite element analysis (FEA). In this section, the strength of driving forces by stress gradient and temperature gradient will be compared with the electron wind force for different line widths.

The atomic flux due to EWF is traditionally expressed as [11]

$$\vec{J}_A = \frac{N}{k_B T} Z^* e \rho D_0 \exp\left(-\frac{E_A}{k_B T}\right) \cdot j \quad (4.32)$$

Similarly, the atomic flux due to temperature gradient induced driving force (TGIDF) and stress gradient induced driving force (SGIDF) are shown in Eqs. (4.33) and (4.34), respectively [101, 116]

$$\vec{J}_{th} = -\frac{NQ^* D_0}{k_B T^2} \exp\left(-\frac{E_A}{k_B T}\right) \cdot \nabla T \quad (4.33)$$

$$\vec{J}_s = \frac{N\Omega D_0}{k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \cdot \nabla \sigma_H \quad (4.34)$$

Therefore, the ratio of atomic fluxes between TGIDF and EWF can be derived as

$$r_{21} = \frac{J_{th}}{J_A} = \frac{Q \cdot \nabla T}{Z^* e \rho j T} \quad (4.35)$$

The ratio of atomic fluxes between SGIDF and EWF can also be expressed as

$$r_{31} = \frac{J_s}{J_A} = \frac{\nabla \sigma_H}{NZ^* e \rho j} \quad (4.36)$$

In Eqs. (4.32)-(4.36), D_0 is the pre-factor of the self-diffusion coefficient, E_A is the activation energy for the self-diffusion, T is the local temperature, Q^* is the heat of transport, N is the atomic density, Ω is the atomic volume ($\Omega = 1/N$), j is the local current density, ρ is the electrical resistivity, Z^* is the effective valance number, σ_H is the hydrostatic stress, k_B is the Boltzmann constant and e is the fundamental electron charge.

We employ FEA to calculate numerically the ratios as shown in Eqs. (4.35)-(4.36) for a simple Cu line structure. The width for the structure is changing from 0.05 μm to 1 μm while the thickness is fixed at 0.35 μm . The results are also compared between different ILD: SiO_2 and carbon-doped oxide (CDO). The test structure is subjected to a

typical current density of 2 MA/cm². The simulation results for r_{21} and r_{31} are plotted in Figure 4.17(a) and Figure 4.17(b), respectively.

Figure 4.17 (a) The ratio of temperature gradient induced driving force over electron wind force (b) The ratio of stress gradient induced driving force over electron wind force.

The temperature gradient from simulation is between 0.002-0.01 K/μm. Figure 4.17(a) shows that the temperature gradient is larger for Cu/low-k interconnects compared with Cu/SiO₂ based interconnects for interconnect with the same line width, which is due to the poorer thermal conductivity of the low-k material. Besides, the temperature gradient decreases with decreasing line width, indicating smaller contribution from TGIDF for narrower interconnects. Therefore, for interconnect with narrower line width, TGIDF is smaller. EWF is 2-3 orders higher than TGIDF as shown in Figure 4.17(a), and TGIDF is unlikely to be a dominant driving force for EM failure in nano-interconnect.

Figure 4.17(b) reveals that the stress gradient increases with decreasing line width, indicating a higher thermo-mechanical stress gradient for narrower interconnects. The stress gradient is also higher for low-k interconnects which is consistent with the work reported by Gan et al. [117]. The SGIDF is 2-3 orders higher than EWF as shown in Figure 4.17(b). The importance of high thermo-mechanical stress on EM reliability was first reported by Tan et al. [20]. Later on, Li et al. [100] reported that vacancies tend to cluster at the intersections of grain boundary and the passivation layer under the thermo-

mechanical stress in Al interconnects. This experimental finding also confirms the dominance of SGIDF in narrow interconnects. The insignificance of EWF is also evidenced from the failure analysis results in Figure 4.16.

4.5.1.3 Lifetime enhancement

The nature of SGIDF dominated EM in narrow interconnect and SIV are similar as both are due to the diffusion of interconnect material under the thermo-mechanical stress gradient [22, 68]. The two are not to be confusing as EM is tested under high temperature and high current while SIV is tested only through high temperature baking. As it has been proven that SGIDF is the dominant driving force, the lifetime equation from our previous stress induced voiding (SIV) work [118] (Section 5.2) may be employed to explore the changing lifetime enhancement factor with changing stress conditions in the present work.

The SIV lifetime formulation is an analytical lifetime model based on the stress relaxation in interconnects. The generalized expression for the SIV time to failure can be expressed as [118]

$$t_f = C \frac{T}{(T_0 - T)^N} e^{\frac{E_A}{k_B T}} \quad (4.37)$$

where N is the temperature exponent which depends on the particular geometry and microstructure of the interconnect, C is the temperature independent constant, T_0 is the stress free temperature (SFT), T is the interconnect temperature, E_A is the activation energy for self-diffusion and k_B is the Boltzmann constant.

For interconnect with reservoir

$$MTTF_{reservoir} = C_1 \frac{T}{(T_0 - T)^{N_1}} e^{E_A / k_B T} \quad (4.38)$$

For interconnect without reservoir

$$MTTF_{noreservoir} = C_2 \frac{T}{(T_0 - T)^{N_2}} e^{E_A / k_B T} \quad (4.39)$$

It is noted that in Eqs. (4.38) and (4.39), temperature exponent N is different for the structures with and without reservoir since N is dependent on the geometry and microstructure of the interconnect. The additional reservoir extension can serve as a stress relaxation volume, resulting in a different temperature exponent. Interconnect temperature is the same for structures with and without reservoir for the same stress condition through finite element analysis (FEA). Therefore, the lifetime enhancement factor can be expressed as

$$M = \frac{C_1}{C_2} (T_0 - T)^{N_2 - N_1} = C_0 (T_0 - T)^{\Delta N} \quad (4.40)$$

For the interconnect structure used in this work, SFT is at 310 °C. Interconnect temperature is different at different current densities due to the Joule heating effect. The interconnect temperature is simulated through the coupled field electro-thermal analysis using finite element software ANSYS[®]. For the simulation details, one can refer to Ref. [22]. The simulated interconnect temperature increment due to Joule heating is 2.27 and 6.84 °C for test current densities of 1.2 and 2 MA/cm². The simulated Joule heating is also close to the experimental measured temperature increment through temperature coefficient of resistivity (TCR) extrapolation [119].

Using the simulated interconnect temperature and experimentally measured lifetime enhancement factor, C_0 and ΔN in Eq. (4.40) can be determined. C_0 is evaluated to be

0.443 and ΔN is 0.9356. Therefore, the lifetime enhancement equation can be expressed as

$$M = 0.443(T_0 - T)^{0.9356} \quad (4.41)$$

It is noted that T in Eq. (4.41) represents the actual interconnect temperature. For the commonly used package level EM test, interconnect temperature is the summation of oven temperature and the temperature increment by Joule heating as shown in Eq. (4.42).

$$T = T_{oven} + \Delta T_{joule} \quad (4.42)$$

A higher EM test temperature or higher EM current leads to a higher interconnect T , rendering a lower lifetime enhancement factor according to Eq. (4.41).

For the interconnect structure used in this experiment, interconnect temperature increment by Joule heating is simulated through FEA and the empirical equation is obtained through numerical fitting given below. For a given interconnect structure, Joule heating will be dependent on the square of the stress current and stress temperature. In the numerical fitting process, ΔT_{joule} is obtained at different combinations of j^2 and T_{oven} . The fitting equation derived is as follows

$$\Delta T_{joule} = \frac{1.785 \cdot T_{oven}}{573} j^2 \quad (4.43)$$

In Eq. (4.43), the units T and j are K and MA/cm², respectively. It is noteworthy that the temperature increment by Joule heating is also dependent on the oven temperature for the same EM current. For the same EM test current, temperature increment by Joule heating is higher for higher EM test temperature as indicated by Eq. (4.43).

Substitute Eqs. (4.42)-(4.43) into Eq. (4.41),

$$M = 0.443 \left(T_0 - T_{oven} - \frac{1.785 \cdot T_{oven}}{573} j^2 \right)^{0.9356} \quad (4.44)$$

Equation (4.44) is an empirical lifetime enhancement formulation as a function of the EM test temperature and EM test current. As Eq. (4.44) is based on the interconnect structure from this experiment, a more general lifetime enhancement factor equation can be written as

$$M = C_0 \left(T_0 - T_{oven} - k_0 T_{oven} j^2 \right)^{\Delta N} \quad (4.45)$$

Based on the derivation, C_0 is dependent on C_1 and C_2 in Eqs. (4.38)-(4.39), hence C_0 is dependent on the void surface area at failure, the interfacial layer thickness of the cap layer/Cu interconnect, interconnect width and thickness [68]. k_0 is a fitting parameter representing the Joule heating effect for the interconnect system. ΔN is the difference between N_1 and N_2 in Eqs. (4.38) and (4.39), hence ΔN is dependent on the diffusion paths available for the stress relaxation and/or the microstructure of the interconnect. A positive ΔN will be explained in next section.

For very small EM current at 0.1 MA/cm², the lifetime enhancement factor as a function of test temperature is computed using Eq. (4.44) as shown in Figure 4.18 by ignoring the Joule heating effect. As the interconnect temperature increases, the lifetime enhancement factor decreases. For interconnect temperature below 150 °C, the lifetime enhancement factor is above 50, showing that the reservoir extension is very effective to enhance the EM reliability under normal operating conditions. At a fixed oven temperature of 300 °C, the lifetime enhancement factor as a function of stress current is shown in Figure 4.19. With a higher current density, the interconnect temperature increases due to Joule heating effect. Therefore, the lifetime enhancement factor also decreases for a higher current density, which is also observed experimentally in this work.

Figure 4.18: Lifetime enhancement factor as a function of interconnect temperature. Current density is at 0.1 MA/cm².

Figure 4.19: Lifetime enhancement factor as a function of interconnect stress current. Oven temperature is at 300 °C.

4.5.1.4 Discussion

The calculated positive ΔN in Eq. (4.40) is expected from our previously established SIV model. As shown in Ref. [118], N in Eq. (4.37) is dependent on the particular geometry and microstructures of the interconnect. For simplicity, assuming a uniform grain structure in this work and the effect of microstructure on N can be ignored. For interconnects with and without reservoir, the diffusion path can be different due to

different geometries. The diffusion schematic is shown in Figure 4.20. The void nucleation site is commonly observed at the Cu/cap layer above via [22], and it is represented by the black spot in Figure 4.20. For interconnect with no reservoir, the stress relaxation volume can only grow to the right along M2 or down into via. For interconnect with reservoir, the reservoir extension can also served as a volume for stress relaxation as shown in Figure 4.20(b). As derived analytically in Ref. [118], temperature exponent N is larger for the cases with less diffusion paths for stress relaxation volume growth. Therefore, N_1 is smaller than N_2 in Eqs. (4.38)-(4.39), rendering a positive ΔN for the lifetime formulation in Eq. (4.40).

Figure 4.20: Diffusion path for stress relaxation in interconnect. (a) Without reservoir (b) With reservoir

With this understanding, we therefore postulate that the experimental observed dependence of lifetime enhancement factor on stress condition is due to the fact that the reservoir extension is serving as a volume for stress relaxation, leading to a different temperature exponent for different reservoir length structures.

SFT is an idealistic temperature at which the thermo-mechanical stress in interconnects becomes zero. The actual SFT is highly dependent on the manufacturing process due to many thermal process involved. However, an inaccurate SFT can lead to

inaccurate determination of C_0 and ΔN as can be seen in Eq. (4.40). To overcome the inaccuracy of SFT, SFT must be determined experimentally.

As there are three unknowns in Eq. (4.40), C_0 , ΔN and T_0 , three equations are needed to be solved to determine the three unknown parameters. If lifetime enhancement factor can be measured at three different test temperatures, the three unknowns can be solved simultaneously. Through this approach, the SFT can also be determined accurately. Further work will be done in this area.

4.5.1.5 Summary

In this section, the decreasing lifetime enhancement effect with increasing stress current for EM was observed experimentally for Cu interconnect. Based on EM void location and the increasing EM lifetime with increasing current density, EWF is not the dominant driving force for intrinsic EM failure in M2 test structure. Using the established SIV time to failure formulations, the analytical formulation for the lifetime enhancement factor is derived and the numerical analysis shows that the reservoir extension is very effective to enhance the EM reliability under normal operating conditions.

4.5.2 Width transition structure studies in Cu interconnect

Usually, the EM reliability of an interconnect system is assessed by accelerated life test of representative test structure. Commonly, M1 and M2 line-via test structures are used for EM reliability assessment of copper damascene interconnection system [85, 120]. However, real chip interconnection often contains narrow-to-wide or wide-to-narrow width transition [121]. In contrast to the constant width test structure, it is therefore required to study the EM behavior of width transition test structure to predict

EM life-time more precisely. For a given width transition interconnect, direction of electron flow (from narrow-to-wide segment and wide-to-narrow segment), ratio of segment lengths and failure location are of paramount importance for that interconnect system. Such results on EM would be useful for IC interconnect layout design.

Although attempt is made to study EM behavior in width transition test structure for Al-based interconnect system [121], little is known for the case of Cu-based interconnect system besides the work presented by Christine *et al.* [80] in IRPS 2008 for Cu/low-k interconnect system. To our knowledge, the EM behavior on the direction of electron flow in width transition structure is not addressed.

In this section, we investigate the EM behavior for submicron dual damascene Cu/oxide interconnects, with special focus on the direction of electron flow (from narrow-to-wide segment and wide-to-narrow segment) and the impact of the ratio of the lengths of narrow to wide segments in width transition test structures. Finite element model (FEM) is developed to understand the mechanisms of EM in the width transition test structures.

4.5.2.1 Experiments

A schematic diagram of the test structure employed in this study is shown in Figure 4.21. EM test structures of length $300\text{ }\mu\text{m}$ ($=L_1+L_2$) with line width of $0.28\text{ }\mu\text{m}$ ($=W_1$) and $0.56\text{ }\mu\text{m}$ ($=W_2=2W_1$) are fabricated using 180 nm copper/oxide dual damascene technology. The first inter-metal dielectric (IMD) stack consists of plasma enhanced chemical vapour deposited (PECVD) layer of 50 nm SiN and 800 nm undoped silicate glass (USG) on top of the p-Si substrate using Novellus concept two Sequel Express PECVD system. M1 trench was patterned using 248 nm lithography system and the USG

layer was etched using a fluorine-based dry-etch chemistry in TFL 85 DRM oxide etcher. Photoresist stripping and wet clean were performed to ensure polymer residue-free trenches.

Figure 4.21: Schematic of width transition test structure

Formation of Cu metallization in these trenches involved depositing a stack of 25 nm Ta barrier and 150 nm Cu seed by physical vapor deposition (PVD) in Applied materials PVD/CVD Endura HP 5500 followed by 0.6 μm electrochemically plated (ECP) Cu layer using Novellus SABRE system. A 50 nm thick SiN layer was deposited after CMP process to serve as Cu cap layer. Then layers of 800 nm USG, 50 nm SiN and 500 nm USG were deposited as IMD-2 in which 50 nm SiN serve as trench-2 stop layer. Via and M2 trench were then formed by a via-first dual damascene process. The M1 (lines connected to pads) were short so that voids would be expected to form in M2 line. The lines are of 0.35 μm thick and the via diameter (connecting M1 and M2 lines) is of 0.26 μm . As final process step, all wafers were annealed at 350°C for 30 minutes.

High precision electrical resistance measurements are conducted at room temperature (26 °C) as well as elevated temperatures (300 °C) before the actual EM test on the

samples (in these measurements, a low magnitude of test current is used to avoid Joule heating). The ratio of the standard deviation to the average resistance over large sample size is found to be less than 5% implying tight distribution of the sample resistance. This, together with the effective room temperature resistivity of $1.6 \pm 0.2 \mu\Omega\text{-cm}$ and temperature coefficient of resistivity of $(3.8 \pm 0.2) \times 10^{-3} / ^\circ\text{C}$ are the indication of the good quality of our sample integration process. These electrical measurements are conducted to ensure that the actual EM experiments are conducted on good quality samples and to gain confidence on our EM experimental results [122]. The typical sample resistance (at room temperature) data is shown in Figure 4.22.

Figure 4.22: Sample resistance data measured at room temperature.

Three accelerated package level EM experiments are conducted using AETRIUM® reliability tester. At least 13 samples are tested in each experiment. In these EM experiments, test temperature of 300 °C and current density of 2 MA/cm² (with respect to the narrow segment) are employed as stress conditions. The failure criterion in these experiments is the 10% increase of the sample resistance. The structural description, direction of electron flow and EM results are summarized in Table 4.7. Extensive physical failure analysis on failed samples is conducted by FIB-SEM system.

Table 4.7: EM test data. The symbol ‘ σ ’ represents ‘log-normal sigma’.

Expt.No.	L_1/W_1 (μm)	L_2/W_2 (μm)	e^- –flow direction	t_{50} (hrs)	σ
1	150/0.28	150/0.56	L_1 to L_2	71.40 ^a	0.2 ^a
2	150/0.28	150/0.56	L_2 to L_1	189.29 ^a 229.31 ^b	0.5 ^a 0.3 ^b
3	20/0.28	280/0.56	L_2 to L_1	117.27 ^a 176.82 ^b	0.9 ^a 0.3 ^b

Superscript ‘a’ and ‘b’: ^adata obtained from single mode analysis; ^bdata obtained after removal of early failure modes.

4.5.2.2 AFD simulation

A 3 dimensional AFD based coupled field FEM is developed to understand the EM characteristics as observed experimentally. By virtue of the symmetry of the structure, only half of the model is simulated. The finite element model is meshed with hexagonal elements as shown in Figure 4.23.

The finite element models developed here consist of two steady state analyses, namely a direct coupled analysis with the current and the temperature fields, and an analysis with indirect coupling between the temperature and the mechanical stress fields. In the electrical-thermal analysis, the substrate bottom surface is kept at constant EM test temperature (300 °C) and constant current density (2 MA/cm² with respect to narrow segment) is applied to the Cu interconnect. The nodal temperatures are then retrieved from this stage for use in the thermal-mechanical analysis. In the thermal-mechanical analysis, the following boundary conditions are applied: 1) the substrate bottom is kept fixed with zero displacement and 2) the vertical symmetric plane is constrained to remain vertical arising from the mirror symmetrical nature of the structure under consideration.

User subroutines are developed to calculate the total AFD from the coupled field electrical-thermo-mechanical analyses. A detail description of the model with formulations can be found elsewhere [123]. Commercial finite element software ANSYS[®] is employed for this work.

Figure 4.23: (a) Mesh of the entire model. Mesh of Cu width transition structure- (b): $L_1 = L_2 = 150 \mu\text{m}$, and (c): $L_1 = 20 \mu\text{m}$, $L_2 = 280 \mu\text{m}$.

4.5.2.3 Results and discussions

The mono-modal cumulative distribution functions (CDFs) of the EM failures are shown in Figure 4.24. From the failure distributions shown in Figure 4.24, one may suspect that there could be bi-modal failure mechanism particularly, in the second and third experiment (note that σ 's of these two experiments are quite high). These two failure modes could be the most commonly observed failure mode at the cathode side in M2 test line and the failure mode at the width transition location in the test line as this is the location of flux divergence caused by the structural inhomogeneity [121]. Hence, physical failure analysis is conducted at the both locations. Interestingly, width transition location is not found as a failure site in any of our experiments. Representative micrographs of failed samples are shown in Figure 4.25. Extensive physical failure analysis leads us to conclude that there exists only one failure mode similar to that is shown in Figure 4.25(a).

Figure 4.24: Mono-modal EM failure distributions for width transition test structure.

Figure 4.25: SEM micrographs of failed units (dotted arrow shows the direction of electron flow). (a) Near cathode. (b) The width transition location is shown by a circle.

Because of the existence of single mode failure mechanism, we can treat the first few failures in second and third experiments as early failures (infant mortality [45]). Although the mechanism of failure is same in all the samples in the last two experiments, statistically it is required to consider bi-modal failure distribution due to the presence of early failures, so that we can obtain the actual failure distribution related to the wear-out EM. With this consideration, the failure distributions are shown in Figure 4.26. Note that the three failure distributions in Figure 4.26 are quite parallel to each with σ 's in the range of 0.2 to 0.3, indicating that the distributions are quite tight with the attribution of a strong single mode failure.

Figure 4.26: EM failure distribution after early failure are removed. The early failure are considered as one of the failure modes in the bi-modal failure statistics. In order to obtain the CDF's, 'maximum likelihood method' is employed with 95% confidence bounds.

The AFD distribution obtained from FEM is shown in Figure 4.27. From the AFD distribution, it can be found that the maximum AFD location is the inner corner of the via near the cathode. This location is indeed found as the failure site through physical failure analysis as shown in Figure 4.25(a).

Figure 4.27: AFD (atoms/μm³-sec) distribution in width transition test structure. (a) $r = 0.5$ and (b) $r = 0.07$.

From Table 4.7, we can see that the EM life-time is significantly shorter when the electron flow direction is from narrow-to-wide segment. When the current is going from the narrow to wide line, only the narrow line portion will have the possibility of void, and hence its t_{50} will be governed by the current density computed using the narrow line width. On the other hand, when the current is going from the wide to narrow, only the wide line portion will have the possibility of void, and its t_{50} will be determined by the current density calculated using the wide line width. As the wide line width is two times larger than that of narrow line width, the current density computed using the narrow line width will be double of that computed using the wide line width. If we use the Black

equation to compute, and assume that the current density exponent is 1, then $t_{50\text{wide}}/t_{50\text{narrow}}=2$, and our experimental result is 2.65. Hence the “extra” $t_{50\text{wide}}$ is believed to be due to the larger critical void size for 10% resistance in the wide line as the Black’s equation does not take into account of the critical void size. If we use the current density exponent of 2, then $t_{50\text{wide}}/t_{50\text{narrow}}=4$, which is too high to explain our results. Although one can adjust the n to have the ratio match the experimental results, n will be 1.4. As was mentioned by Lloyd [124], n must be either 1 or 2 in order for the physics to make sense, thus we can see that the longer t_{50} as current going from wide to narrow line is attributed to the reduced current density and the larger critical void size needed for 10% resistance in the wide line. Additionally, the resistance increase behavior for the case of wide-segment cathode is found to be more gradual as compared to the case of narrow-segment cathode.

Also, from Table 4.7, it can be found that with the decrease in the ratio ($r = L_1/L_2$) of the lengths of narrow to wide segments (with $L_1+L_2 = \text{constant}$), significantly shorter EM life-time is obtained. This is because the EM mass-transport in Cu dual damascene structure is mainly governed by Cu/Cap interface and the quality of the chemical-mechanical-polishing (CMP) technique. As the defect density (generated by CMP) is uniform, it is quite obvious that total number of defects will increase when the length of the wide segment increases (or the ratio r decreases). The result of the increase in the number of defects and since the presence of defects is the governing parameter of EM transport; the EM life-time becomes shorten with the decrease in the ratio r .

4.5.2.4 Summary

We demonstrated the EM characteristics as a function of electron flow direction and ratio of the lengths in width transition Cu damascene test structure. It is found that EM

life-time significantly shorten when the electron flow direction is from narrow-to-wide segment. Therefore, such electron flow direction should be chosen for EM reliability assessment to avoid over estimation from electron flow direction dependent life-time. Apart from the electron flow direction dependence, it is also found that the EM life-time is a strong function of the ratio of the lengths of narrow and wide segments for width transition test structure. Detail EM dependences with varying r , varying test current density, and two different electron flow direction is the proposal for future work.

4.5.3 Blech effect in Cu interconnects with oxide and low-k dielectrics

The electron wind force pushes copper atoms from cathode to anode and the accumulation and depletion of Cu atoms at anode and cathode ends respectively produces a backflow stress gradient in the interconnect. This stress gradient opposes the electric wind force and reduces the impact of the electron wind force on atomic movement, and thus enhances its EM lifetime. Blech demonstrated that there existed a threshold condition, defined by $(jL)_c$, below which the interconnect becomes immortal in terms of its EM lifetime [50], where j is the current density in the interconnect and L is the length of the interconnect. This $(jL)_c$ is called the Blech Product. This phenomenon is useful and has been employed in circuit design, allowing higher current density in shorter interconnects with high reliability.

Blech product is affected by many factors such as the mechanical properties of inter-level dielectrics (ILD), temperature of the interconnect, interconnect material properties etc. Blech product for Cu/oxide interconnect was shown to be 2 to 3 times higher than the value observed in Al (Cu)/oxide interconnects. The higher value of the Blech product in

Cu may be due to the higher Young's Modulus of Cu (~ 104 GPa) as compared to that in Al (~ 69 GPa) [125].

For low-k interconnects, Blech product was shown to be lower than their oxide counterpart due to the lower mechanical strength of the low-k ILD [126]. The weak confinement by low-k materials decreases the backflow stress, resulting in an increase of the net drift velocity of atoms and a reduction of EM lifetime.

As the Blech effect affects the EM lifetime of an interconnect, and all the EM tests are conducted at higher temperature, it is important to examine the temperature dependence of the Blech product. Wang *et al.* [127-129] found experimentally that the Blech product was temperature dependent for the temperature range of 295-400 °C. They attributed this phenomenon to the temperature-dependent mechanical properties of the interconnect materials. On the other hand, Lee found that Blech product was independent of temperature within the temperature range of 340-400 °C for Cu/oxide interconnects [130].

In this section, we investigate the mechanism of the temperature dependence of the Blech product for both the Cu/oxide and Cu/low-k interconnects. Using finite element modeling (FEM), we demonstrate that Blech product should be temperature dependent at high temperature if the inelastic behavior of Cu is considered. This inelastic behavior has not been taken into consideration in the previous works. The simulated Blech product is found to be consistent with the literature reported values.

4.5.3.1 Model description

A 3D simplified finite element (FE) model is constructed using commercial FEM software ANSYS[®]. By virtue of the symmetry of the structure, only half of the model is

simulated. The test line has a thickness and a width of 0.35 and 0.28 μm , respectively. The Ta diffusion barrier and SiN cap layer are also included as shown in Figure 4.28.

Figure 4.28: Half-line finite element model

The stress and strain values of the Cu interconnect are computed using ANSYS thermo-mechanical analysis element *solid45* with the following boundary conditions: 1) the substrate bottom is fixed with zero displacement and 2) the vertical symmetric plane is constrained to remain vertical arises from the mirror symmetrical nature of the structure under consideration.

The low-k ILD considered in this work is Carbon-doped Oxide (CDO). The SiO₂, Si, Ta, SiN and CDO are all taken to be isotropic linear elastic solids. However, a commonly used bilinear model is employed for Cu with a linear dependence of the initial yield strength with temperature. At 20 °C and 350 °C, yield strengths of Cu are 676 MPa and 165 MPa, respectively [131]. The stress-strain behavior for the bilinear model is shown in Figure 4.29.

Figure 4.29: Stress-strain behavior of Cu by bilinear model.

4.5.3.2 Critical stress and Blech product evaluations

The net atomic flux as a result of electron wind force and backflow stress can be expressed as [132]

$$J = \frac{DC}{k_B T} \left(\rho j e Z^* - \Omega \frac{\delta \sigma}{\delta x} \right) \quad (4.46)$$

where D is the atomic diffusivity of Cu, C is the Cu atom concentrations, k_B is the Boltzmann's constant, T is the temperature of the interconnect, ρ is the resistivity, j is the current density, e is the fundamental electron charge, Z^* is the effective charge number, Ω is the atomic volume, and σ is the backflow stress. Under the Blech effect, the backflow stress is fully balanced by the electron wind force,

$$(j \cdot L)_c = \frac{\Omega \sigma_{crit}}{\rho e Z^*} \quad (4.47)$$

The calculation of critical stress σ_{crit} for Cu interconnect in Eq. (4.47) is formulated in the next paragraph. It is strongly dependent on the confinement on the Cu structure imposed by the surrounding ILD, the barrier metal and cap layer. This critical stress is contributed by various stress components present in Cu interconnects such as backflow stress, thermo-mechanical stress, etc. For simplicity, we only consider the backflow stress

in this work. The effect of thermo-mechanical stress will be briefly discussed in the next section. ρZ^* is an intrinsic material property of Cu, and is independent of temperature [133]. In Eq. (4.47), all the parameters are independent of temperature except the critical stress, so we can focus our study on the temperature effect of the critical stress.

For EM along a thin line, it was understood that local stress relaxes to a hydrostatic state long before diffusion along the line reaches a steady state [17], so the stress is taken to be hydrostatic in the present work. The stress can form a void in the interconnect if the associated strain energy relief W_{strain} is sufficient to supply the required interface energy for the formation of a void. The strain energy relief is given by

$$W_{strain} = \frac{1}{2} V_{relaxation} \sum_{i=1,2,3} \varepsilon_i \sigma_i = \frac{3}{2} \varepsilon_H \sigma_H V_{relaxation} \quad (4.48)$$

where ε_i and σ_i are referring to the strain and stress in the principal axes. ε_H is the hydrostatic strain with σ_H being the corresponding hydrostatic stress. $V_{relaxation}$ is the stress relaxation volume over which the stress is completely relaxed. The volumetric strain is generated due to the backflow stress by [83]

$$\frac{\sigma_H}{B} = \varepsilon_{vol} \quad (4.49)$$

where B is the effective bulk modulus which describes the confinement on the metal line by the surrounding materials. The calculation of B by FEM is detailed in Ref. [134]. ε_{vol} can be approximated as $3 \varepsilon_H$ for a rectangular cross section interconnect as can be derived easily as follows. Assume an interconnect with the dimensions of $L \times W \times H$, the volumetric strain of the interconnect is

$$\varepsilon_{vol} = \frac{LWH - LWH(1 - \varepsilon_H)^3}{LWH} = 3\varepsilon_H - 3\varepsilon_H^2 + \varepsilon_H^3 \approx 3\varepsilon_H \quad (4.50)$$

By combining Eqs. (4.48) and (4.49), we have

$$W_{strain} = \frac{\sigma_H^2}{2B} V_{relaxation} \quad (4.51)$$

On the other hand, the interface energy is given by

$$W_{int} = A_{void} \gamma \quad (4.52)$$

where A_{void} is the surface area of the initial void along the Cu/SiN interface and γ is the interface energy per unit area. Here we consider voids are formed along the Cu/SiN interface as typically observed [100]. For void to form, the minimum hydrostatic stress required can therefore be determined from Eqs. (4.51) and (4.52) as follows,

$$\sigma_{crit} = \sqrt{\frac{2A_{void} \gamma B}{V_{relaxation}}} \quad (4.53)$$

Equation (4.53) shows that the critical stress is proportional to the square root of the product of effective bulk modulus and interface energy, which is also reported by Zhai *et al.*[135]. This implies that the critical stress for void nucleation is determined by the Cu/cap interface condition and the mechanical properties of interconnect materials. The ratio $A_{void}/V_{relaxation}$ depends on the specific fabrication process and is assumed to be constant for particular interconnect as obtained experimentally [132]. Substitute Eq. (4.53) into Eq. (4.47), we have

$$j \cdot L_C = \frac{\Omega}{\rho e Z^*} \sqrt{\frac{2A_{void} \gamma B}{V_{relaxation}}} \quad (4.54)$$

In this work, B is determined through FEM simulation and the rest of the parameters in Eq. (4.54) are taken from references as listed in Table 4.8. Equation (4.54) implies that a good passivation condition will lead to a higher Blech product due to higher interface energy. It can also be seen that interconnects with higher ILD mechanical strength are associated with a higher Blech product due to higher effective bulk modulus.

Table 4.8: Simulation parameter list

Parameter	Material	Value	Ref
Atomic concentration	Cu	$8.44 \times 10^{-28}/\text{m}^3$	[72]
product of ρZ^*	Cu	$6.68 \times 10^{-9} \text{ W-m}$	[76]
Interface energy (Cu/SiO ₂)	Cu/cap	5 J/m ²	[100]
Interface energy (Cu/CDO)	Cu/cap	2 J/m ²	[100]
Young's modulus	Cu	129.8 GPa	[131]
Young's modulus	CDO	7.76 GPa	[136]
Young's modulus	SiO ₂	71.4 GPa	[72]
$A_{\text{void}}/V_{\text{relaxation}}$	Cu	0.0008/ μm	[100]
Electronic charge	-	$1.6021 \times 10^{-19} \text{ C}$	-

4.5.3.3 Results and discussions

Figure 4.30 shows the calculation results of effective bulk modulus for both Cu/oxide and Cu/CDO interconnects. The calculated B is in the range of 25~32 GPa for Cu/oxide interconnect within the temperature range 50~350 °C, close to the value reported by Hau-Riege *et al.* [134]. Further more, as temperature increases above 200 °C, B decreases gradually to account for the plastic deformation. B for Cu/CDO interconnects has the same trend with respect to temperature as their oxide counterpart. The large difference in the magnitude of B between Cu/oxide and Cu/CDO interconnects is due to the lower mechanical properties of CDO as compared to SiO₂ as shown in Table 4.8 [45].

Figure 4.30: Simulation results of effective bulk modulus for both Cu/oxide and Cu/CDO interconnects.

As depicted in Figure 4.31, the calculated Blech product of Cu/oxide interconnect is in the range of 3600~4100 A/cm within the temperature range of 50~350 °C. By taking plastic deformation at high temperature into consideration, the Blech product drops above 200 °C. Wang *et al.* [128] reported Blech product in the range 2660~3940 A/cm in the temperature range 295~400 °C, close to our simulated values.

Figure 4.31: Simulation results of Blech product for both Cu/oxide and Cu/CDO interconnects

It is noteworthy that our simulated temperature dependence is not as strong as the experimental observations. This discrepancy may arise due to some factors which are not considered in the analysis such as aspect ratio, microstructure, process specification, etc [130]. The simulated Blech product for Cu/CDO interconnect is in the range of 1600~2500 A/cm, lower than their oxide counterpart due to lower critical stress. The drop in the Blech product for Cu/low-k interconnect was also reported experimentally [83]. Besides, it is found that the temperature dependence of Blech product for Cu/CDO interconnect is much stronger than Cu/oxide interconnect as observed in Figure 4.31. This result shows that low-k interconnect is more prone to plastic deformation which is also consistent with experimental findings [137].

As indicated by Eq. (4.54), Blech product can be improved by either using a mechanically stronger ILD material or improve the interface between Cu/cap layer.

However, since all low-k materials are mechanically weak, Blech product can only be improved by a proper interface treatment of Cu/cap interface.

In practical situation, the presence of thermo-mechanical stress further complicates the study of Blech effect. Since Cu interconnects are fabricated through many thermal processes at different temperatures, it is very difficult to estimate the stress free temperature (SFT). We consider a simple case where a uniform thermo-mechanical stress is distributed along the metal line as shown in Figure 4.32. Without the thermo-mechanical stress, the steady state backflow stress is less than the critical stress, so the metal line is immortal. With the thermo-mechanical stress, the total stress at the cathode exceeds the critical stress which results in EM failure. In other words, the maximum backflow stress which can be sustained by the interconnect is lowered in the presence of the tensile thermo-mechanical stress, resulting in lower Blech product.

Figure 4.32: A tensile thermo-mechanical stress is added to the metal line. The maximum backflow stress which can be sustained by the interconnect is reduced, resulting in a lower Blech product.

4.5.3.4 Summary

In this part of study, we have demonstrated that the Blech product is lower for Cu interconnects at high temperature due to its inelastic behavior. Besides, we also prove that the effect of inelasticity is more dominant in low-k interconnects. The present findings suggest that, for future narrow low-k interconnects, the inelastic behavior of Cu at high

temperature will further degrade the EM lifetime. This is because for low-k interconnects, they are more prone to plastic deformation [132] and the interface between interconnects and dielectrics are more significant due to the larger surface to volume ratio. In such situation, a good passivation is needed to improve the EM lifetime.

4.6 Enhancement of EM Test Accuracy

The influence of the current density j and metal line temperature T on the median time to failure (MTF) t_{50} is described by the Black's equation [10],

$$t_{50} = A \cdot j^{-n} \cdot e^{E_A / K_B T} \quad (4.55)$$

where E_a is the activation energy, n is the current density exponent, A is a parameter sensitive to the fabrication process and the geometry of the interconnect, and $K_B T$ has the usual meaning. Electromigration experiments are normally conducted at higher current densities and temperatures than expected in service conditions to shorten the test time.

As the current density is increased dramatically with shrinking device dimensions, the interconnect temperature can be much higher than the oven temperature due to Joule heating effect in the packaging level EM testing. Joule heating effect is also strongly dependent on the interconnect systems. Joule heating in multi-level metallization is more significant than that in single level metallization [138]. The thickness of substrate also has a strong effect on the temperature increment by Joule heating [74]. With continuous increasing of stress current and implementation of low-k dielectrics as inter-level dielectric (ILD), Joule heating is becoming more prominent [139].

The interconnect temperature increment due to Joule heating is usually estimated by utilizing the temperature coefficient of resistivity (TCR) of the metallization in EM test [85]. Joule heated sample resistance and non-Joule heated sample resistance are measured at the test temperature and this together with the measured or given TCR, can be used to estimate the temperature rise due to Joule heating. It is important to measure the actual interconnect temperature accurately because t_{50} is in general a function of $\exp(E_a/k_B T)$ as shown in Eq. (4.55). In practice, the actual interconnect temperature can deviate from the estimated interconnect temperature due to the oven temperature variations, individual interconnect sample resistance variations, the accuracy of measured TCR, etc. With more severe Joule heating expected in future low-k interconnects, the sample resistance variations are becoming more important since Joule heating is dependent on the sample resistance, resulting in higher temperature variations in interconnects. The variations of the interconnect temperatures can lead to the variations of experimentally determined E_a and n although the actual E_a and n does not change. This implies a varying accelerating factor, which shall lead to inaccurate extrapolated EM lifetime. So far, it remains unclear how a variation in interconnect temperature affects the experimentally determined E_a and n quantitatively.

In this study, we perform quantitative investigations on how the variations of interconnect temperature affect EM activation energy E_a and current density exponent n . First we consider a typical Cu/low-k interconnect. The Joule heating effect and the associated temperature variation are estimated using FEA under typical experimental conditions. Only oven temperature variation and sample resistance variation are considered in contributing the interconnect temperature variations. The variation of E_a due to the variation of interconnect temperature is derived analytically so that the variation of E_a can be estimated once the temperature variation is known. It is found that a small variation of E_a can lead to a large fluctuation in the projected interconnect

lifetime. The variation formulation for n is also derived so that it can be estimated once the temperature deviation is known. Both formulations can provide a quick and accurate assessment on the variation of EM parameters due to interconnect temperature variation under Joule heating effect.

4.6.1 Temperature variation in interconnects

Interconnect temperature in oven EM test can be expressed as

$$T = T_{oven} + \Delta T_{joule} \quad (4.56)$$

where T_{oven} is the oven temperature and ΔT_{joule} is the temperature increment due to Joule heating. For typical high temperature oven used in EM test,

$$T_{oven} = T_{set} + \Delta T_{oven} \quad (4.57)$$

where T_{set} is the oven temperature setting and ΔT_{oven} is the temperature variation of the oven. Typical oven shows 1% uniformity in the spatial temperature distribution as in the specification for Blue MTM oven. Therefore, $\Delta T_{oven} = \pm 0.01 \cdot T_{set}$.

Temperature rise due to Joule heating is formulated as [85]

$$\Delta T_{joule} = \frac{\Delta R}{TCR \cdot R_0} \quad (4.58)$$

In Eq. (4.58), ΔR is the resistance difference between the Joule heated sample resistance R_j and non-Joule heated sample resistance R_N , R_0 is the sample resistance at 0 °C and TCR is also referenced at 0 °C. It is noted that ΔR is dependent on stress current, non-Joule heated sample resistance and TCR. Depending on the manufacturing process, the initial sample resistance can have a variation up to 10 % [122], leading to different ΔT_{joule} among different samples. Besides that, TCR is also different among the samples as it is dependent on the microstructure of the sample [140]. For Cu interconnect, constant TCR

cannot be used because Cu resistivity is no longer linearly dependent on temperature above 200 °C [119]. All the above-mentioned facts result in the fluctuations of ΔT_{joule} , especially in the presence of severe Joule heating.

To simplify the analysis, we only consider the fluctuation of resistance among the samples and temperature variation in the oven in this work. In fact, this is an optimistic assumption because the TCR variations shall further increase the interconnect temperature variations. We denote the variation of interconnect temperature T in Eq. (4.56) as ε . From Eqs. (4.56) and (4.57),

$$\varepsilon = \Delta T_{oven} + \frac{\delta \Delta T_{joule}}{\delta R_N} \times \Delta R_N = \Delta T_{oven} + \varepsilon_{joule} \quad (4.59)$$

ε_{joule} in Eq. (4.59) is the variation of the temperature increment (ΔT_{joule}) under Joule heating effect which is due to the variation of sample resistance and it is estimated by FEA as shown below.

Joule heating effect is estimated by the coupled field electrical-thermal analysis using finite element software ANSYS[®] for a typical Cu/low-k interconnect. The finite element model has been described in Section 4.3.2 and the finite element mesh is shown in Figure 4.4. Low-k material carbon-doped oxide (CDO) is chosen as the dielectrics in this work. The material properties are taken from Ref. [40]. In the analysis, the substrate bottom surface is kept at constant EM test temperature with a pre-determined current density applied to the interconnect. Current densities ranging from 0.01 to 6 MA/cm² are chosen to assess the Joule heating effect. Four different EM test temperatures are chosen to investigate the impact of EM test temperatures on Joule heating effect. The simulation results are summarized in Table 4.9.

Table 4.9: Joule heating effect at different test temperatures and current densities for Cu/CDO interconnects.

Current density (MA/cm ²)	Temperature (°C)			
	100	200	300	400
0.01	100	200	300	400
0.5	100.55	200.72	300.88	400.97
1	102.23	202.90	303.57	403.91
2	109.08	211.81	314.54	415.94
4	139.61	251.51	363.42	469.48
6	191.07	318.43	445.79	559.75

From Table 4.9, at a test temperature of 300 °C and current density of 4 MA/cm², the temperature increment is 63.42 °C, close to the 65 °C as reported by Wu *et al.* [141] for the same stress conditions for low-k interconnect. For the same test temperatures, the temperature increment is proportional to the square of current density, which shows the temperature increment is indeed due to the Joule heating effect. It is also noted that under the same current density, the temperature increment is higher for higher test temperature.

For ε in Eq. (4.59), ΔT_{oven} is dependent on the oven temperature. The variation of temperature increment under Joule heating ε_{joule} is estimated by FEA. For illustration, we choose a typical stress current of 4 MA/cm² and a typical 10% variation in interconnect resistance [122]. The change of interconnect resistance is computed by changing Cu resistivity values in the material library in the FEA simulations. ε_{joule} in Eq. (4.59) under a combination of different oven temperatures and resistivity is simulated and the results are summarized in Table 4.10. It is noted that ε_{joule} is dependent on the resistivity variation and the Joule heating effect. The temperature variation will be much lower if a smaller current density is used in the EM test.

As shown in Table 4.10, lower Cu resistivity lead to a negative temperature variation since the generated Joule heat is linearly dependent on the resistivity. Table 4.10, together with ΔT_{oven} , will be used for the numerical calculations in the following sections.

Table 4.10: The temperature increment under Joule heating effect and its variations at different oven temperature and interconnect resistivity. The simulation is based on Cu/CDO interconnect with a current density of 4 MA/cm².

Oven temperature (°C)	ΔT_{joule} in Eq. (4.58) (°C)	ε_{joule} at $0.9\rho_0$ (°C)	ε_{joule} at $0.95\rho_0$ (°C)	ε_{joule} at ρ_0 (°C)	ε_{joule} at $1.05\rho_0$ (°C)	ε_{joule} at $1.1\rho_0$ (°C)
150.00	45.57	-6.43	-3.16	0.00	3.48	7.08
200.00	51.52	-7.19	-3.53	0.00	3.90	7.92
250.00	57.47	-7.95	-3.91	0.00	4.31	8.75
300.00	63.42	-8.71	-4.28	0.00	4.72	9.59
350.00	69.55	-9.47	-4.65	0.00	5.13	10.43
400.00	75.67	-10.23	-5.03	0.00	5.54	11.26

4.6.2 The effect of test temperature on Joule heating effect

The first law of thermodynamics states that energy is conserved. For Cu interconnect, majority of the heat is transferred to the substrate bottom through conduction [74, 138]. In the steady state, the temperature of interconnect is stabilized ($\delta T / \delta t = 0$), therefore, the Joule heating is fully balanced by the heat conduction down to the substrate. The amount of Joule heating at test temperature T_1 and T_2 can be written as

$$Q_1 = I^2 \cdot [R_0 \times (1 + TCR \cdot (T_1 + \Delta T_1 - 273))] \quad (4.60)$$

$$Q_2 = I^2 \cdot [R_0 \times (1 + TCR \cdot (T_2 + \Delta T_2 - 273))] \quad (4.61)$$

where Q_1 and Q_2 are the generated heat, I is the interconnect current, R_0 is interconnect resistance at 273 K, and TCR is the temperature coefficient of resistivity for the interconnect. It is noted here that the heat generated by Joule heating in Eqs. (4.60) and (4.61) is different due to the fact that interconnect resistance is different.

Through *Fourier's law*, the amount of heat Q_1 and Q_2 dissipated through conduction to the substrate bottom can be written as

$$Q_1 = -kA \frac{\Delta T_1}{dx} \quad (4.62)$$

$$Q_2 = -kA \frac{\Delta T_2}{dx} \quad (4.63)$$

where k is the thermal conductivity and A is the conduction area. k and A are the same for the same structure under consideration.

Equate Eqs. (4.60)-(4.63)

$$I^2 \cdot [R_0 \times (1 + TCR \cdot (T_1 + \Delta T_1 - 273))] = -kA \frac{\Delta T_1}{dx} \quad (4.64)$$

$$I^2 \cdot [R_0 \times (1 + TCR \cdot (T_2 + \Delta T_2 - 273))] = -kA \frac{\Delta T_2}{dx} \quad (4.65)$$

For the same test structure, divide Eq. (4.64) by Eq. (4.65),

$$\Delta T_2 \cdot (TCR \cdot T_1 + 1 - TCR \cdot 273) = \Delta T_1 \cdot (TCR \cdot T_2 + 1 - TCR \cdot 273) \quad (4.66)$$

It is noted that TCR is process dependent as it is correlated to the median grain size and the defectiveness of the crystal lattice [140]. For Cu interconnects, a departure from a linear dependence becomes evident for temperatures above 200 °C. With the correction function from JEDEC [119], the deviation is within 6 % for interconnect temperature below 400 °C. TCR is taken to be 0.0036 for extrapolation until 400 °C, and hence $TCR \cdot 273 \approx 1$. Therefore, Eq. (4.66) is simplified as

$$\Delta T_2 \cdot TCR \cdot T_1 = \Delta T_1 \cdot TCR \cdot T_2 \quad (4.67)$$

Simplify Eq. (4.67), we have

$$\frac{T_2}{T_1} = \frac{\Delta T_2}{\Delta T_1} \quad (4.68)$$

Equation (4.68) is also verified with our finite element simulation results in Table 4.9.

4.6.3 Activation energy variations

Activation energy E_a of EM is often estimated as the slope of t_{50} versus $1/k_B T$ in the lifetime plot. If the line fitting is based on the inaccurate interconnect temperature, the estimated E_a can be different from the actual E_a . It remains unknown how the variation of interconnect temperature affects the estimated E_a . Also, it is necessary to derive a correction function so that E_a can be re-estimated once the variation in interconnect temperature is known. The re-estimated E_a can fluctuate around a true E_a , depending on the interconnect temperature variations.

Consider the EM test at two different temperatures T_1 and T_2 ($T_1 < T_2$). The stress current j is the same for both cases. The temperature increments are different for both cases as shown in Table 4.9 and they are denoted as ΔT_1 and ΔT_2 . t_{50}^1 and t_{50}^2 are experimentally obtained EM lifetime.

Without considering the temperature increment by Joule heating,

$$t_{50}^1 = A \cdot j^{-n} \cdot e^{E_A' / k_B T_1} \quad (4.69)$$

$$t_{50}^2 = A \cdot j^{-n} \cdot e^{E_A' / k_B T_2} \quad (4.70)$$

where E_A' is the experimentally obtained activation energy without considering Joule heating effect. Combine Eqs. (4.69) and (4.70),

$$E_A' = \frac{\ln t_{50}^1 - \ln t_{50}^2}{1/k_B T_1 - 1/k_B T_2} \quad (4.71)$$

In fact, Eq. (4.71) is the mathematical representation of the slope of t_{50} versus $1/k_B T$ in the lifetime plot.

By including Joule heating effect,

$$t_{50}^1 = A \cdot j^{-n} \cdot e^{E_A/k_B(T_1+\Delta T_1)} \quad (4.72)$$

$$t_{50}^2 = A \cdot j^{-n} \cdot e^{E_A/k_B(T_2+\Delta T_2)} \quad (4.73)$$

where E_A is the Joule heating corrected activation energy. Combine Eqs. (4.72) and (4.73),

$$E_A = \frac{\frac{\ln t_{50}^1 - \ln t_{50}^2}{k_B(T_1+\Delta T_1)} - \frac{1}{k_B(T_2+\Delta T_2)}}{\frac{1}{k_B(T_1+\Delta T_1)} - \frac{1}{k_B(T_2+\Delta T_2)}} \quad (4.74)$$

ΔT_1 and ΔT_2 are correlated to the test temperatures by Eq. (4.68). Substitute Eq. (4.68) into Eq. (4.74),

$$E_A = \frac{\frac{\ln t_{50}^1 - \ln t_{50}^2}{k_B(T_1+\Delta T_1)} - \frac{1}{k_B(T_2+\Delta T_1 \cdot \frac{T_2}{T_1})}}{\frac{1}{k_B(T_1+\Delta T_1)} - \frac{1}{k_B(T_2+\Delta T_1 \cdot \frac{T_2}{T_1})}} \quad (4.75)$$

Combine Eqs. (4.71) and (4.75),

$$E_A = E_A' \cdot \left(1 + \frac{\Delta T}{T}\right) \quad (4.76)$$

Equation (4.76) is the formulation for the joule heating corrected activation energy by including Joule heating effect. It can be seen that the corrected activation energy is higher than the experimentally determined E_a , if Joule heating is not considered. In the derivations, temperature variations due to oven and sample resistance are excluded. It is noted that ΔT in Eq. (4.76) is the temperature rise due to Joule heating and T is the oven temperature. The above derivations reveals the relationship between E_A' evaluated at oven temperature and E_A evaluated at interconnect temperature including Joule heating effect.

Based on the same principles, we can consider the temperature variation $\mathcal{E}$ as ΔT in Eq. (4.76) and T in Eq. (4.76) is the interconnect temperature including Joule heating effect. Equation (4.76) can be re-written as

$$E'_A = E_A / \left(1 + \frac{\varepsilon}{T}\right) \quad (4.77)$$

In Eq. (4.77), E_A is the actual activation energy which is independent on test conditions, and E'_A is the experimentally determine Ea. For Cu/low-k interconnect with an E_A of 0.9 eV for interfacial diffusion [86], with the estimated ε and T in Table 4.10, the experimentally determined E'_A under different oven temperature and Cu resistivity is shown in Figure 4.33.

For interconnect resistivity at $0.9\rho_0$, the temperature variation is negative as shown in Table 4.10. In other words, the estimated interconnect temperature is lower than the actual interconnect temperature and this results in slightly higher estimated activation energy than the actual Ea of 0.9 eV for interfacial diffusion. With higher interconnect resistivity, the estimated Ea decreases. The variation of estimated Ea on oven temperature is small due to the low variation of oven temperature in EM test. For the same interconnect resistivity, higher oven temperature is associated with higher Ea variation as shown in Figure 4.33, but its effect is negligible.

Figure 4.33: The variation of Ea (E'_A) due to the variation of sample resistance and oven temperature. Actual Ea is assumed to be at 0.9 eV.

The variation of E_a in Figure 4.33 shall lead to large variations of t_{50} if these E_a is used in the Black's equation for lifetime extrapolation. The variation of t_{50} due to the variation of E_a is shown in Figure 4.34. The variation of t_{50} is much higher than that of E_a since t_{50} is exponentially dependent on E_a . For the same interconnect resistivity, higher oven temperature is associated with lower t_{50} variation as shown in Figure 4.34.

Figure 4.34: The variation of EM lifetime due to the variation in E_a .

Equation (4.77) is validated in the Joule heating corrected E_a work by Roy *et al.* [122]. The reported variation of E_a (ΔE_a) is within 0.01~0.02 eV with $\Delta T=13.83$ °C, $T=275$ °C, E_a is within 0.85~0.88 eV. Using Eq. (4.77), the variation E_a is estimated to be ~0.02 eV, close to the experimentally reported value.

4.6.4 Current density exponent variations

Current density exponent n is an indication of EM failure process. It is commonly accepted that $n=2$ is for void nucleation limited failure and $n=1$ is for void growth limited failure [99]. However, n can be larger than 2 due to Joule heating effect [17]. In this work, the correction function for n is derived so that the variation of n can be estimated once the

temperature variation is known. It is noted that n can be greater than two under Blech effect [142]. Therefore, we only consider long interconnect lines where the Blech effect can be ignored in this work.

Consider EM test at two different current densities, j_1 and j_2 ($j_1 < j_2$) with test temperature T . The temperature increment due to Joule heating is denoted as ΔT_1 and ΔT_2 .

$$t_{50}^1 = A \cdot j_1^{-n'} \cdot e^{E_A/k_B T} \quad (4.78)$$

$$t_{50}^2 = A \cdot j_2^{-n'} \cdot e^{E_A/k_B T} \quad (4.79)$$

where n' is the experimentally determined current density exponent excluding Joule heating effect. Combine Eqs. (4.78) and (4.79),

$$\ln t_{50}^1 - \ln t_{50}^2 = -n' \cdot (\ln j_1 - \ln j_2) \quad (4.80)$$

By considering Joule heating effect,

$$t_{50}^1 = A \cdot j_1^{-n} \cdot e^{E_A/k_B (T + \Delta T_1)} \quad (4.81)$$

$$t_{50}^2 = A \cdot j_2^{-n} \cdot e^{E_A/k_B (T + \Delta T_2)} \quad (4.82)$$

where n is the Joule heating effect corrected current density exponent. Combine Eqs. (4.81) and (4.82),

$$\ln t_{50}^1 - \ln t_{50}^2 = -n \cdot (\ln j_1 - \ln j_2) + \frac{E_A}{k_B} \left(\frac{1}{T + \Delta T_1} - \frac{1}{T + \Delta T_2} \right) \quad (4.83)$$

Combine Eqs. (4.80) and (4.83), we have

$$n' = n + \frac{E_A (\Delta T_1 - \Delta T_2)}{k_B (T + \Delta T_1) \cdot (T + \Delta T_2) (\ln j_1 - \ln j_2)} = n + \Delta n \quad (4.84)$$

The current density exponent correction factor Δn in Eq. (4.84) can be further simplified from the intrinsic nature of Joule heating. The temperature increment can be written as $\Delta T = K \cdot j^2$. Therefore, from Eq. (4.84), Δn can be re-written as

$$\Delta n = \frac{E_A (Kj_1^2 - Kj_2^2)}{k_B (T + Kj_1^2) \cdot (T + Kj_2^2) (\ln j_1 - \ln j_2)} = \frac{E_A \cdot K \cdot (j_1 + j_2) \cdot (j_1 - j_2)}{k_B (T + Kj_1^2) \cdot (T + Kj_2^2) (\ln j_1 - \ln j_2)} \quad (4.85)$$

To obtain Δn as a function of j , we take the limit of $(j_1 - j_2)$ such that $\lim(j_1 - j_2) = 0$, and we have

$$\begin{aligned} \Delta n &= \lim_{(j_1 - j_2 = 0)} \frac{E_A \cdot K \cdot (j + j)}{k_B (T + Kj^2) \cdot (T + Kj^2)} \cdot \frac{dj}{d(\ln j)} = \frac{E_A \cdot K \cdot (j + j)}{k_B (T + Kj^2) \cdot (T + Kj^2)} \cdot j \\ &= \frac{2 \cdot E_A \cdot Kj^2}{k_B \cdot (T + Kj^2)^2} = \frac{2 \cdot E_A \cdot \Delta T}{k_B \cdot (T + \Delta T)^2} \end{aligned} \quad (4.86)$$

In the above derivations, the temperature variations due to oven and interconnect resistivity are not taken into consideration. In Eq. (4.86), T is the oven temperature and ΔT is the temperature increment due to Joule heating. Similarly, ΔT in Eq. (4.86) can be replaced by ε and T shall represent interconnect temperature including Joule heating effect. Equation (4.86) can be rewritten as

$$\Delta n = \frac{2 \cdot E_A \cdot \varepsilon}{k_B \cdot (T + \varepsilon)^2} \quad (4.87)$$

The current density exponent variation factor Δn is dependent on the amount of temperature variation ε , test temperature T , as well as estimated E_a . In other words, the value of n will be seemingly temperature and current density dependent experimentally.

With the previous determined E_a in Figure 4.33 and temperature variation in Table 4.10, Δn is plotted with the variation of resistivity as shown in Figure 4.35. The estimated Δn is less than one for the temperature variation considered in this work. Also Δn is smaller for a higher oven temperature.

Figure 4.35: Joule heating corrected n due to the variation of sample resistance and oven temperature.

In the current density exponent correction work by Roy *et al.* [122], $E_a=0.87$ eV, $\varepsilon \approx 3$ °C, $T=300$ °C, substitute into Eq. (4.87), Δn is estimated to be 0.18, close to the experimentally corrected n of 0.1 and 0.2 for narrow and wide interconnects. Therefore, the estimation from Eq. (4.87) is consistent with the experimental values.

4.6.5 Summary

In the high current density EM test, the actual interconnect temperature can deviate from the estimated interconnect temperature under severe Joule heating effect. The Joule heating effect and the associated temperature variations are estimated by FEA under typical experimental conditions for Cu/low- k interconnect. The formulations for the variation of E_a and n are derived analytically and verified by the recent experimental work. Our numerical analysis show that a negative interconnect temperature variation lead to a higher experimentally determined E_a and a lower experimentally determined n . From this work, it is found that the experimentally determined E_a and n can deviate from the true E_a and n due to the interconnect temperature deviations under Joule heating effect.

4.7 Conclusion

In this chapter, we focus on the EM studies through both modeling and experiments. It mainly comprises two parts. In the first parts, a modified EM modeling methodology is proposed to improve the EM modeling accuracy. This methodology is based on the driving force approach. Three important driving forces have been considered: EWF, TGIDF, and SGIDF. Their individual mathematical formulations are derived based on Green's theorem. The formulations are implemented through finite element analysis (FEA), and the EM void nucleation and its growth can be simulated through the developed static and dynamic simulation FEA codes. Thermo-mechanical stress gradient induced driving force is found to be the dominant driving force for EM failure in M2 test structures. The modeling methodology is verified by the experimental results.

In the second part of the chapter, the effect of interconnect design factors on EM is investigated. Lifetime enhancement factor in EM reservoir structures is found to decrease with increasing EM stress current experimentally. The derived analytical formulation for the lifetime enhancement factor shows the reservoir extension is very effective to enhance the EM lifetime under normal operating conditions. In the width transitional structures, EM characteristic is found to be dependent on electron flow direction and ratio of the lengths in width transition Cu interconnects. EM lifetime significantly shorten when the electron flow direction is from narrow-to-wide segment. Lastly, the issue in high temperature and high stress current EM test is presented. The variation of activation energy and current density exponent in Black's equation is derived analytically. This variation can be taken into account in future EM test in low-k interconnects with severe Joule heating.

5. STRESS INDUCED VOIDING

5.1 Introduction

Stress-induced voiding has been a serious reliability challenge to IC interconnects based on either Al or Cu metallization. The physical mechanism active in interconnects during the development and the relaxation of mechanical stress have been intensively studied [143, 144]. However, there is still lack of explicit account of SIV dependence on material and process factors. In contrast with EM, where Black's equation has been widely accepted and validated, a closed form lifetime model for SIV has not yet reached a consensus [145]. A lifetime model for SIV is proposed from the energy perspective in Section 5.2. Besides the thermal stress, metallization grain structures, interconnect passivation integrity, interlayer dielectrics (ILD) confinement effect to interconnection and interconnect dimensions are also included in the model. The application of the model is also explored.

The magnitude and state of the stress in the interconnects is greatly affected by the thermo-mechanical properties of the surrounding dielectric materials. Dielectric materials are categorized by the way they are deposited: low-k materials are either chemical vapor-deposited (CVD) or spin-on applied. In the case where SiO_2 is used as dielectrics, tensile thermo-mechanical stress is developed in the metal lines because the metal lines have a much larger CTE than the substrate and passivation materials. However, low-k materials have a significantly lower elastic modulus and a higher CTE than Cu. Therefore, different stress characteristics of the interconnects are to be expected in low-k interconnects and

this in turn is expected to result in different failure behaviors of interconnects. Therefore, obtaining a better understanding of stress in both line and via structures is essential to understand the failure mechanism of SIV. Besides SIV, large von Mises stress in low-k interconnects may also result in interconnect failure in the form of plastic deformation [7]. In Section 5.3.1, we compare the SIV phenomena in Cu interconnect with SiO₂ and low-k dielectrics from both FEA and experimental results. In Section 5.3.2, the stress behaviors in Cu interconnects are studied systematically, in particular the effect of dielectrics and interconnect geometry.

5.2 SIV lifetime modeling

Mechanical and electrical reliabilities are the major concerns in modern ultralarge-scale integration (ULSI) interconnect for both Al and Cu based metallization. One cause of mechanical failure is the thermo-mechanical stress caused by the thermal expansion mismatch between the metal line and its surrounding materials. In the fabrication of interconnects, the process temperature can go up to 400 °C during film annealing and dielectrics deposition, thus causing a large thermo-mechanical stress in the interconnects upon their cooling down to room temperature. This high tensile stress can lead to stress-induced voiding (SIV) in the form of open circuit or substantial resistance increase [17].

Pre-existing micro-voids were found in both wide and narrow Cu interconnects under thermo-mechanical stress before electromigration (EM) test [146]. These micro-voids can grow during EM and become fatal voids at the cathode end of an interconnect [53]. Shen *et al.* [111] found that a large stress-induced void was more prone to growth during

subsequently EM test. Recent studies have also shown that SIV becomes more severe with the incorporation of low-k dielectrics [54].

All the above-mentioned facts lead to the necessity to understand the physics of SIV in metallization. Many studies have been carried out to investigate SIV from different perspectives such as the quality of passivation layer [147], the mechanical strength of interlayer dielectrics (ILD) [55], the microstructure of the film [148], etc, and they indeed affect the thermo-mechanical stress in metallization and hence SIV lifetime. However, there is no existing SIV lifetime model to account for the above-mentioned factors collectively at present. Furthermore, a closed form lifetime formulation for SIV is still under debate [19, 56, 149, 150].

The objective of this work is to present a detailed methodology and derivation of our SIV lifetime model so as to ease future related research works. Based on the fact that SIV is one of the means to release stored strain energy of an interconnection through mass redistribution, we propose a lifetime model from the energy perspective in the present work. The critical temperature at which SIV is the most severe will also be derived from the lifetime model proposed. Extension of our model to other applications will also be presented in this work.

5.2.1 Theoretical considerations

5.2.1.1 Review of existing lifetime models

Various models have been proposed to understand the SIV phenomenon during high temperature storage (HTS) test. McPherson *et al.* proposed a power-law creep model as the mechanism for stress relaxation where the thermo-mechanical stress gradient served

as the driving force for vacancy movement [56]. Further improvement was done by Ogawa *et al.* by introducing the “active diffusion volume” concept, and only those vacancies within the “active diffusion volume” were able to participate in the SIV process [149]. Fischer *et al.* also derived a phenomenological equation to describe the SIV lifetime [19]. Although some of the models seem to agree with the experimental data, a comprehensive understanding is still lacking. Moreover, lattice relaxation due to strain energy relief near the void region during SIV process has not been considered in the above-mentioned models.

In fact, the contribution by the strain energy relief is much more significant than the contribution by the vacancy diffusion in a typical SIV process. Korhonen *et al.* suggested that the relaxation of stress will be far more through the lattice volume than through the total vacancy volume [14]. Taking Cu interconnect as an example, a typical reported vacancy concentration in the interconnect is 0.01% in Cu bulk [151] and 0.25% at the Cu/cap interface [149]. Hence, the void volume fraction due to vacancy clustering will be within 0.01%-0.25% by assuming all the vacancies are able to participate in the clustering process. On the other hand, the void volume fraction due to the complete strain energy relaxation is $3 \cdot (\alpha_{\text{metal}} - \alpha_{\text{surr}}) \cdot \Delta T$, where α_{metal} and α_{surr} are the coefficients of thermal expansion (CTE) for Cu and the surrounding materials, respectively. ΔT is the difference between the SFT and the interconnect temperature. Using the typical values of $18 \times 10^{-6}/\text{K}$ for $(\alpha_{\text{metal}} - \alpha_{\text{surr}})$ and 300 K for ΔT [152], the void volume fraction is evaluated to be 1.62% for strain energy relief which is much larger than that contributed by the vacancy clustering alone. In other words, the severity of SIV will be underestimated if the contributions from the lattice relaxation are ignored in the void forming process.

5.2.1.2 Assumptions in our model derivation

In this work, we focus on the technological important case of Cu based interconnects, although the same methodology can be applied to Al based interconnects. Since a typical Cu interconnect is surrounded by cap layer on top and diffusion barrier on the side walls and bottom as shown in Figure 5.1, the cooling down of the interconnect from the final annealing temperature to room temperature induces high tensile stress in the metallization due to thermal mismatch. However, due to material and structure inhomogeneities in the interconnects, the interconnect system is not under uniform hydrostatic stress.

Figure 5.1: A segment of Cu interconnects. Cu is confined by its surrounding materials.

Hydrostatic stress is employed as a starting point (time zero) for SIV analysis in this work based on the following three reasons. Firstly, hydrostatic stress is proven to be the driving force for SIV [153]. Von Mises stress, which is normally used as a criterion for evaluating deformation, does not include the hydrostatic components and usually does not result in the volumetric changes of the material [154]. A gradient in hydrostatic stress can still exist after plastic deformation, which induces SIV subsequently [155]. Secondly, at the early stage in a typical SIV process, under the constraint by the surrounding materials, the shear stress is relaxed through either diffusion creep or dislocation glide [103, 156], causing an interconnect to be under a near perfect hydrostatic state. As reported by An *et*

al. [157] recently, the biaxial stress in wide Cu line (Cu film) is relaxed by plastic deformation through dislocation movement while the narrow Cu line failed through SIV due to the hydrostatic stress in interconnect. During void growing process, the duration of plastic deformation is found to be much shorter than the duration due to hydrostatic stress relaxation [66], and thus von Mises stress can be neglected. Lastly, the focus of this work is on SIV. If the von Mises stress is so high that it reaches the yield strength of the interconnects, deformation may cause the interconnect to fail through via barrier layer cracking as demonstrated by Paik *et al.* [7]. However, this failure mechanism is not within the scope of our present study.

After the stress in interconnects is relaxed to a hydrostatic state, the hydrostatic stress is almost uniform. Therefore under such a steady state condition, there is no driving force for atoms to diffuse from one location to another, and hence no formation of voids in interconnects.

However, this “steady state” is metastable. In practice, this “steady state” is destroyed in the presence of flaws/defects. A flaw may act like a mini-void for the stress field to relax. A high stress gradient will thus be resulted which drives Cu atoms to diffuse away from the flaw, causing a void to grow and relaxing the tensile stress simultaneously. Consequently, another equilibrium state is reached with void formation and stress relaxed interconnects [111].

The presence of the flaws/defects in metallization at time zero is justified as the process temperature can go up to 300~400 °C during deposition and annealing of dielectrics, so the thermo-mechanical stress in the metallization can reach to a level of several hundreds of MPa after cooling down to room temperature [158]. As a result, mini-voids are formed in the interface of Cu/SiN, and in particular at the intersection of grain

boundaries with the Cu/SiN interface [100, 159]. Chemical mechanical polishing (CMP) in dual-damascene Cu process also results in a high defect density at Cu/SiN interface [160].

In the next section, we will demonstrate that in the presence of the flaws/defects in the interconnects, the stress gradient responsible for atomic diffusion can reach to a level of 10 times higher than the case without flaws/defects through FEA. Such a high stress gradient is the driving force for the void growth in SIV.

5.2.1.3 Stress gradient computation using finite element analysis

Since the high stress gradient near the mini-void is the driving force for void growth in SIV, it is necessary to evaluate such a stress gradient numerically. Finite element analysis is employed to compare the thermo-mechanical stress distributions with and without the presence of a mini-void in Cu interconnects.

Multi-physics finite element (FE) analysis software ANSYS® is used to construct a 3D FE model for the line structure. By virtue of the symmetry of the structure, only half of the structure is considered. The model thickness and width are 0.35 and 0.28 μm respectively. The Ta diffusion barrier and SiN cap layer are also included as shown in Figure 5.2(a). The local coordinate system is the Cartesian system where the x-, y- and z-axes correspond to the direction along the metal length, width, and thickness, respectively.

The thermo-mechanical stress is simulated through the *solid45* thermal-mechanical analysis by assuming SFT and test temperature at 350 and 300 °C respectively. In the modeling, the substrate bottom is fixed with zero displacement. The vertical symmetrical

plane is constrained to remain vertical arising from the mirror symmetrical nature of the structure [22] while the nodal points are allowed to undergo in-plane movements during deformation. The top surface is not constraint. All the interfaces between dissimilar materials are treated as perfectly bonded.

The elements along the Cu/SiN interface are deleted physically to initialize a mini-void of size $0.02\mu\text{m}\times 0.01\mu\text{m}\times 0.01\mu\text{m}$ on the top interface as it is also observed experimentally [146]. Static equilibrium condition is maintained during the element removing process. The stress distributions for the line structures without and with a mini-void are shown in Figure 5.2(b) and Figure 5.2(c) respectively. For ease of visualization, only bare Cu is shown in Figure 5.2. As shown in Figure 5.2(c), the mini-void is located at the top interface of Cu/SiN along line edge.

Without the mini-void as shown in Figure 5.2(b), the stress distribution is uniform along the x direction and the maximum stress gradient is around $1\text{ GPa}/\mu\text{m}$, contributed by the stress gradient along the y and z directions. By taking the mini-void into consideration, the stress distributions are highly non-uniform in the vicinity of the mini-void, indicating a strong driving force for void growth and stress relaxation. The stress gradient can be as high as $10\text{ GPa}/\mu\text{m}$ from our simulations. In other words, the stress gradient in the presence of mini-void is at least one order higher than the case without the mini-void. Hence, the presence of defect/mini-void at the Cu/SiN interface accelerates the diffusion process and hence the formation of the stress-induced voids.

Figure 5.2: (a) Finite element model for Cu line structure. (b) Thermo-mechanical stress distribution without mini-void. (c) Thermo-mechanical stress distribution in the presence of mini-void.

5.2.2 SIV lifetime modeling

As shown previously, the locations of flaws/defects act as a void growing site for SIV. Within the context of continuum mechanics, SIV is one of the means to release the stored strain energy of an interconnect system by mass redistributions.

The stress evolution during SIV can be described by the following equation [14, 145]

$$\frac{\delta \sigma_H}{\delta t} = K \nabla^2 \sigma_H \quad (5.1)$$

where t is the time, σ_H is the local hydrostatic stress driving the mass transport, and K is the effective diffusivity defined as $K = \frac{DB\Omega}{k_B T}$. Here, D is the atomic diffusivity, Ω is the atomic volume, k_B is the Boltzmann's constant, T is the local temperature, and B is the effective bulk modulus which describes the confinement effect of the surrounding materials on the metal line. Equation (5.1), together with the boundary conditions, governs the stress evolution in the interconnects. The analytic solutions of Eq. (5.1) for 1D and 2D line structures can be found in the works of Korhonen *et al.* [14] and Zhai *et al.* [145].

Since Eq. (5.1) resembles Fick's diffusion equation, the diffusion length for stress relaxation along a particular diffusion path can be defined as

$$L_{I,GB,B} = \sqrt{K_{I,GB,B}t} \quad (5.2)$$

where t is the duration of the SIV process, e.g. the bake time during HTS testing, and $K_{I,GB,B}$ is the effective diffusivity defined earlier with the subscript I,GB,B to represent the diffusion path for the atomic diffusion along the interface, grain boundary and in the bulk, respectively.

Consider the instance just before hydrostatic stress relaxation, the initial hydrostatic stress σ_H due to thermal mismatch can be evaluated by [152]:

$$\sigma_H = 3(\alpha_{Cu} - \alpha_{SURR})(T_0 - T)B \quad (5.3)$$

where T_0 is the SFT which depends on the manufacturing process and T is the temperature of the interconnect. Although it is known that Cu interconnects can be partially inelastic at high temperature [131], the relaxation of plastic deformation in the form of diffusion creep or dislocation glide will stabilize the interconnects into an almost hydrostatic state without void formation [103, 156]. Therefore, for the modeling of the voiding process in SIV, only hydrostatic stress is considered without plastic deformation, and a perfectly elastic behavior for Cu interconnects is used in the present work as is done by Hau-Riege and Thompson [134].

With these considerations, the strain energy is formulated as

$$E_{strain} = \frac{3}{2} \varepsilon_H \sigma_H \quad (5.4)$$

where ε_H is the corresponding hydrostatic strain for σ_H . Here, we assume Cu as mechanically isotropic. Since $(\alpha_{Cu} - \alpha_{SURR})(T_0 - T) = \varepsilon_H$, we have from Eq. (5.3), $\sigma_H = 3\varepsilon_H B$, and the strain energy can be re-written as follows

$$E_{strain} = \frac{\sigma_H^2}{2B} \quad (5.5)$$

In the presence of the thermo-mechanical stress in ULSI metallization, Li *et al.* [100] showed that vacancies tend to cluster at the intersections of grain boundary and the passivation layer in order to reduce the strain energy, hence typically defects are found at these intersections along the line edge as indicated in Figure 5.3(a), and such a situation will be considered in this work. Figure 5.3(b)-(c) also provides an experimental proof that a void grows from an initial defect under thermo-mechanical stress [159]. Defects located at other sites where no dominant diffusion path is present will not undergo stress relaxation.

Stress in the vicinity of the defect is relaxed in the void growing process by atomic diffusion, and the diffusion volume can be determined using Eq. (5.2). Equation (5.2) shows that the effective diffusion length along a particular direction is determined by SIV duration and the effective diffusivity. Following the concept of atomic diffusion, we can define the stress relaxation volume by the volume bounded by the diffusion length along x , y and z axes.

Figure 5.3: (a) Schematic of an initial defect located at the cross section of grain boundary and passivation layer at the line edge. (b)-(c) Experimental result of a void formed due to thermo-mechanical stress.

Assuming the strain energy within the stress relaxation volume is completely relaxed by void growth, the energy conservation law leads us to the following [132, 135]

$$E_{strain} \cdot V = \gamma \cdot S \quad (5.6)$$

where γ is the interface energy at Cu/cap layer per unit area, S is the free surface area of a fatal void for a particular interconnect and V is the stress relaxation volume.

Based on the diffusion pathways available for stress relaxation volume growth, we can classify the interconnect SIV process into three categories as linear, square and cubic as shown in Figure 5.4 (a)-(c). Figure 5.4(a) shows the stress relaxation volume in the form of cuboids expanding along the line direction when Cu/SiN interface is the dominant diffusion path. This represents the case of SIV in very narrow Cu interconnects where stress along the width direction is relaxed in a very short time. Figure 5.4(b) demonstrates the case when the stress relaxation volume is in the shape of a half cylinder, expanding in both length and width directions. Figure 5.4(c) depicts the case when the grain boundary diffusion is as important as the interface diffusion. It is noted that the diffusion volume can always be modified in the future to more closely represent the actual microstructures in interconnects.

Figure 5.4: Three cases of stress relaxation volume evolution indicated by the grey area. The relationship between the stress relaxation volume and diffusion length is categorized as (a) linear, (b) square, and (c) cubic.

With these three categories, the respective stress relaxation volumes are given as follows, where w is the interconnect width, d is the interfacial thickness, and $L_{I,GB}$ is the effective diffusion length as defined in Eq. (5.2),

$$V = w \cdot d \cdot L_I \quad (5.7)$$

$$V = \pi \cdot L_I^2 \cdot d \quad (5.8)$$

$$V = \frac{\pi L_{GB}}{6} (3L_I^2 + L_{GB}^2) \quad (5.9)$$

By combining Eqs. (5.2)-(5.9), the time to failure can be obtained from the solutions of Eq. (5.6), and they are shown in Eqs. (5.10)-(5.12) for the cases of linear, square and cubic, respectively

$$t_f = C_1 \frac{\gamma^2 T}{B^3 D_I (T_0 - T)^4} e^{\frac{E_A}{k_B T}} + t_r \quad (5.10)$$

$$t_f = C_2 \frac{\gamma T}{B^2 D_I (T_0 - T)^2} e^{\frac{E_A}{k_B T}} + t_r \quad (5.11)$$

$$t_f = C_3 \frac{\gamma^{2/3} T}{B^{5/3} (3D_I D_G^{1/2} + D_G^{3/2}) (T_0 - T)^{4/3}} e^{\frac{E_A}{k_B T}} + t_r \quad (5.12)$$

where t_r is the time for plastic deformation relaxation to hydrostatic state for the interconnect, C_1 to C_3 are constants given as

$$C_1 = \frac{4k_B S^2}{81\Omega(\alpha_{Cu} - \alpha_{surr})^2 W^2 d^2} \quad (5.13)$$

$$C_2 = \frac{2k_B S}{9\pi\Omega(\alpha_{Cu} - \alpha_{surr})^2 d} \quad (5.14)$$

$$C_3 = \frac{(4S)^{2/3} k_B}{(3\pi)^{2/3} \Omega(\alpha_{Cu} - \alpha_{surr})^{4/3}} \quad (5.15)$$

From Eqs. (5.13)-(5.15), it can be seen that C_1 , C_2 , and C_3 are dependent on the void surface area at failure, the interfacial layer thickness of the cap layer/Cu interconnect, interconnect width and thickness. Equations (5.10)-(5.12) indicates that the SIV time to failure is strongly dependent on the interface energy of the interfacial layer, effective bulk modulus of the interconnect system, diffusivities of the interconnect atom in the dominant diffusion paths, SFT, and the line temperature. The SIV lifetime is also shown to be

inversely proportional to the diffusivities in the dominant diffusion paths from Eqs.(5.10)-(5.12). This model provides, to a first order, a good quantification of SIV lifetime dependence on these factors. The temperature exponent of the SIV lifetime is consistent with the commonly observed values from one to four by McPherson *et al.* [56] and Fischer *et al.* [19].

We validate Eqs. (5.10)-(5.12) by comparing the calculated SIV lifetime with experimental values taken from Ref. [161]. In Ref. [161], since the SIV failure extended throughout the line width, Eq. (5.10) is employed for the calculation. With T_0 at 280 °C, T at 200 °C, W at 0.4 μm [162], and d at 0.5 nm [76], E_A is within 0.65-0.75 eV, γ at 5 J/m [53, 132], the calculated lifetime is within 115-1360 hrs which is comparable to the experimentally observed values of 600 hrs.

5.2.3 Results and discussions

5.2.3.1 SIV in interconnects with low-k dielectrics

From Eqs. (5.10)-(5.12), one can see that SIV lifetime is strongly dependent on the passivation condition because good passivation leads to higher interface energy γ . This is in agreement with the experimental work by Lloyd *et al.* [163].

Bruynseraede *et al.* [164] stated that SIV shall improve due to a lower density of nano-defects generated by the plastic deformation in low-k interconnects. Suo [152] also reported that low-k interconnect should be more SIV resistant due to the reduced effective bulk modulus, resulting in a larger t_f in Eqs. (5.10)-(5.12). In fact, this improvement may

be partially contributed by the lower intrinsic stress in low-k interconnects due to lower biaxial modulus of porous low-k dielectric film [165].

On the other hand, Gan *et al.* [117] demonstrated that low-k interconnects suffered more from SIV at via bottom due to a higher stress gradient despite a lower thermo-mechanical stress. The same finding was also reported by Orain *et al.* [54] where low-k interconnects showed a shorter SIV lifetime compared with their oxide counterpart. This is probably due to the poor passivation which counteracts the benefit of low thermo-mechanical stress for low-k interconnects in Eqs. (5.10)-(5.12) and/or probably the lower t_r due to higher von Mises stress in the interconnect system with low-k dielectrics. With ΔT at 200 °C, our finite element calculation on 0.28 μm Cu line structure shows that the volume-averaged von Mises stresses are 500 and 420 MPa for low-k (carbon-doped oxide) and SiO_2 based interconnects, respectively.

Based on the SIV lifetime formulation in Eqs. (5.10)-(5.12), SIV performance for the low-k interconnects depends on the compromise between the confinement effect B and the passivation effect γ . Since the passivation condition is highly process dependent, if one can assume that the passivation on Cu surface is the same for both Cu/ SiO_2 and Cu/low-k interconnects, Cu/low-k interconnects will outperform its counterpart in SIV due to a lower thermo-mechanical stress. In reality, the passivation condition is poorer for Cu/low-k interconnect as indicated by a lower interface energy for low-k interconnects [132]. In short, the SIV performance for Cu/low-k interconnects is highly dependent on the process and materials used during fabrication.

5.2.3.2 Critical temperature for SIV

By grouping the temperature independent terms as a constant C in Eqs. (5.10)-(5.12), the generalized expression for the SIV time to failure can be expressed as

$$t_f = C \frac{T}{(T_0 - T)^N} e^{\frac{E_A}{k_B T}} + t_r \quad (5.16)$$

where N is the temperature exponent which depends on the particular geometries and microstructures of the interconnects. Equation (5.16) implies that the failure time approaches infinity when SIV test is carried out at either the SFT T_0 , or the absolute 0 K. As the HTS temperature increases, the tensile thermo-mechanical stress decreases linearly and the diffusivity increases exponentially. As a consequence, the SIV lifetime decreases with temperature up to a critical point, above which the lifetime increases with increasing temperature as shown in Figure 5.5. Therefore, to maximize acceleration in reliability test, SIV should be performed around T_{crit} . This T_{crit} can be determined by differentiating Eq. (5.16) with respect to T and t_r is assumed to be temperature independent, we have the following

$$T_{crit} = \frac{2E_A T_0}{\sqrt{(E_A - k_B T_0)^2 + 4E_A T_0 k_B N} + E_A + k_B T_0} \quad (5.17)$$

Equation (5.17) reveals that T_{crit} is dependent on the activation energy, temperature exponent, as well as SFT. Unlike the SIV lifetime, T_{crit} is independent of the passivation condition γ and confinement effect B . Setting SFT at 300°C, T_{crit} as a function of activation energies for different temperature exponents is plotted in Figure 5.6. It is observed that T_{crit} increases with increasing activation energy. Also, T_{crit} is larger for smaller N as shown in Figure 5.6.

Figure 5.5: SIV lifetime as a function of temperature. As temperature drops from stress free temperature T_0 , the strain energy increases, but the atomic diffusivity decreases, resulting an inverted bell shape for SIV lifetime.

It is noteworthy from Figure 5.6 that our numerical results are consistent with the experimental findings. Compared with the work by Ogawa *et al.* [149], where E_A was given as 0.74 eV and T_0 was found to be 270 °C, T_{crit} is evaluated to be within 172-228 °C using Eq. (5.17) for the different value of N used, and the computed T_{crit} agrees well with their experimental observations of 190 °C. In the recent work by An *et al.* [157] where the grain boundary diffusion is found to be as important as the interface diffusion, we use the temperature exponent of 4/3 for Eq. (5.17). Using the E_A at 0.74 eV as in the previous case, the critical temperature evaluated from Figure 5.6 is around 255 °C, in good agreement with the experimentally observed 250 °C. For Al interconnects, Fischer *et al.* also reported the similar critical temperature for Al interconnects at slightly higher activation energy [19].

Figure 5.6: Critical temperature profile as a function of activation energy and temperature exponent. Stress free temperature is set at 300°C.

From Eq. (5.17), by setting $N=4$ for the case of Cu narrow interconnect, T_{crit} as a function of SFT for different activation energies is plotted in Figure 5.7. From the graph, the following implications can be observed. Firstly, when the activation energy E_A increases, the differences between SFT and T_{crit} decreases. Secondly, larger E_A leads to larger T_{crit} , or to be more precisely, increasing E_A move T_{crit} towards SFT. Thirdly, for larger SFT, the difference between SFT and T_{crit} is also larger. In other words, if we can anneal the sample at a lower temperature before HTS test, T_{crit} will decrease at a slower rate than SFT, making them closer. All the above observations are in fact expected from the temperature dependence of the creep diffusion and the thermo-mechanical stress occur during the SIV process, thus qualitatively verify our model.

Figure 5.7: Critical temperature as a function of stress free temperature at different activation energies. The temperature exponent is assumed to be four.

5.2.3.3 Actual stress free temperature

Stress free temperature T_0 is an idealistic temperature at which the thermo-mechanical stress component in interconnects become zero. It is usually assumed to be the dielectric/cap layer deposition temperature or the final annealing temperature. However, the actual SFT is highly dependent on the manufacturing process due to many thermal process involved. As certain amount of thermo-mechanical stress may have been relaxed before the start of HTS test, the actual SFT could be different from the estimation obtained using the final annealing temperature. Using Eq. (5.17), the actual SFT can be derived as follows

$$T_0 = \frac{(N-1)k_B T_{crit}^2 + E_A T_{crit}}{E_A - k_B T_{crit}} \quad (5.18)$$

and T_{crit} , E_A , and N can be determined experimentally.

Setting T_{crit} at 200 °C as typically observed [149], actual SFT as a function of activation energy E_A and temperature exponent N is plotted in Figure 5.8. One can see that actual SFT increases slightly with decreasing activation energy, and it is higher with a larger temperature exponent. The estimated actual SFT is only 5~25 °C higher than the

critical temperature for activation energy around 0.7 eV. This value is much lower than the SFT estimated from the dielectric/cap layer deposition temperature or the final annealing temperature, which is usually between 350 and 400 °C for Cu interconnects [72].

As shown in Figure 5.8, the actual SFT is only slightly higher than the critical temperature, regardless of T_{crit} and N . Since experimentally, the critical temperature is around 200 °C [149], the above analysis reveals that, in practical situation, most of the thermo-mechanical stress has been relaxed before the HTS test as indicated by a low actual SFT from our analysis.

Figure 5.8: Actual stress free temperature as a function of activation energy and temperature exponent. The critical temperature is assumed to be at 200°C.

5.2.3.4 Limitation of the model

In our SIV model, the thermo-mechanical stress is considered as the only driving force for SIV. In reality, in an interconnect, besides the thermo-mechanical stress, there are also backflow stress, grain growth induced stress, intrinsic stress, etc. The backflow stress can be ignored since a very small current density is applied to monitor the

interconnect resistance so Joule heating effect is negligible. Therefore, the small current density in SIV test will not affect SIV lifetime. The grain growth induced stress and intrinsic stress need to be considered for more accurate SIV lifetime modeling in the future works.

In contrast to the typical behavior in Al lines, Paik *et al.* [166] showed that the mechanical stress is higher in wider Cu lines due to their larger grain size in the lines. These larger grains will induce higher grain growth induced stress in addition to the thermo-mechanical stress. As a result, the acceleration of SIV increases with temperature instead of being depicted in Figure 5.5 where a maximum acceleration exists at T_{crit} , and this is indeed observed by Hommel *et al.* [161]. Hence, the proposed model is more accurate for narrow Cu interconnects where the grain growth induced stress is negligible compared with thermo-mechanical stress. Besides, von Mises stress decreases with line width [167], indicating smaller driving force for plastic deformation in narrow interconnects.

5.2.4 Summary

In summary, we have presented a lifetime model for SIV from the energy perspective. A SIV lifetime equation is derived which is similar to the Black's equation for EM failure. It is shown that SIV lifetime is strongly dependent on the passivation quality at the cap layer interface, the confinement effect by the surrounding materials to interconnects, and the available diffusion paths in interconnects. Contrary to the traditional power-law creep model, we find that the temperature exponent in SIV lifetime formulation is determined by the available diffusion paths for the interconnect atoms and the interconnect geometries. The critical temperature for the SIV is found to be

independent of passivation integrity and dielectric confinement effect. Actual SFT during SIV process is also found to be different from the final deposition or annealing temperature of the metallization, and it can be evaluated analytically once the activation energy, temperature exponent, and critical temperature are determined experimentally. Our results show that our SIV lifetime model can be used to predict the SIV lifetime in nano-interconnects.

5.3 Effect of interconnect material on SIV

5.3.1 Comparison of SIV phenomena in Cu line-via structures with different dielectric materials

Different materials and processing steps involved in fabricating the interconnects in integrated circuits develop different types of stresses such as thermo-mechanical stress [168], grain-growth induced stress [166], backflow stress [128], intrinsic stress [143], etc. These stresses lead to different failure mechanisms for interconnects such as plastic deformation, cracking, void formation, etc. Among all these failure mechanisms, stress-induced voiding (SIV), also called stress migration (SM), has been a critical reliability concern for Cu interconnects and has attracted extensive research interests [135, 169]. This stress migration will be of increasing concern for interconnects with smaller dimensions because both the absolute stress level and stress gradient increase at smaller geometries [170].

While stress-induced voiding in line structures has been studied extensively [117, 118, 167, 169], the void formation and evolution behavior of SIV in line-via structures are

still not well understood [171] despite the presence of SIV void in via as observed experimentally [161, 171, 172]. This may be due to the complex geometry of line-via structures as compared to its line structure counterpart. For Cu interconnects, via structure is completely encapsulated by the diffusion barrier layer, whereas for line structures, top surface is covered by cap layer with diffusion barrier layers on the sidewalls and bottom.

However, as via bottom is blocked by diffusion barrier layer, the barrier layer discontinues Cu atomic flux and this can easily lead to the formation of voids in via. Also, the void size that causes SIV failure in via is considerably smaller than that in the line. Furthermore, the thermo-mechanical stress distribution is less uniform in via than that in the line, resulting in higher stress gradient in via. In other word, it is easier for SIV failure to occur in the line-via structure as compared to the line structure. As line-via structures are inevitable in ULSI multi-level metallization, and the number of line-via structures is increasing tremendously, it is necessary to extend the investigation of SIV from Cu line to Cu line-via structures.

Besides the complexity of via structure used in Cu interconnect, the inclusion of low-k materials as dielectrics further complicates SIV studies. Bruynseraede *et al.* stated that SIV shall improve due to a lower density of nano-defects generated by the plastic deformation in low-k interconnects [164]. Suo also reported that low-k interconnects should be more SIV resistant due to the reduced effective bulk modulus and a lower stress level [152]. Gan *et al.*, on the other hand, demonstrated that low-k interconnects suffered more from SIV at via bottom due to a higher stress gradient despite a lower thermo-mechanical stress [117]. The same finding was also reported by Orain *et al.* where low-k interconnects showed a shorter SIV lifetime compared with their oxide counterpart [54].

In this work, our primary objective is to compare the SIV performance between SiO₂ based dielectrics and low-k dielectrics through both experiment and finite element modeling. For low-k dielectrics, carbon-doped oxide (CDO) is chosen as it displays distinct thermo-mechanical properties compared with undoped silica glass (USG) dielectric. Package level SIV test of Cu dual-damascene interconnects for line-via structures is performed. Different SIV behaviors and performances between USG and CDO interconnects were found. We explore the observed differences using 3D finite element analysis (FEA), and the simulated void growing dynamics is consistent with the reported failure modes. With our FEA results, two intrinsic factors affecting the SIV performance for future Cu low-k interconnects will be discussed from the perspective of the driving force and the confinement effect.

5.3.1.1 Experiments

Stress-induced voiding test structures are fabricated using 0.18 μm Cu/oxide dual-damascene technology. The first inter-metal dielectric (IMD) stack consisted of plasma enhanced chemical vapor deposited (PECVD) layer of 50 nm SiN and 800 nm USG from the bottom up. M1 trench was patterned using 248 nm lithography. Formation of Cu metallization in these trenches involved depositing a stack of 25 nm Ta barrier, 150 nm Cu seed by physical vapor deposition (PVD) in Applied Materials PVD/CVD Endura HP 5500 followed by 600 nm electrochemically plated (ECP) Cu layer using Novellus SABRE system. A 50 nm thick SiN layer was deposited after CMP process to serve as the cap layer. Then layers of 800 nm USG, 50 nm SiN and 500 nm USG were deposited as IMD-2. M2 trench and via were then formed by a via-first dual-damascene process. M2 metallization stack was the same as that of M1. The width and thickness for both M1 and M2 are 0.28 and 0.35 μm respectively. Schematic drawing of the test structure is shown in Figure 4.14.

Two different dielectrics, USG and CDO dielectrics were used in this study. Both USG and CDO dielectrics were prepared by a Novellus Concept Two SEQUEL Express plasma enhanced chemical vapor deposited (PECVD) system. The process temperature was at 400 °C during deposition. The precursors used were liquid tetramethylcyclotetrasiloxane, O₂ and CO₂ gas. The process temperature for USG and CDO dielectrics are identical so that process variations to the final SIV reliability difference can be minimized, and they have the same thickness. Therefore, the experimental observed different SIV performance for the two dielectrics shall be mainly attributed to their different material properties.

Package level high temperature storage (HTS) test was performed at three different temperatures, i.e., 150, 200 and 250 °C to observe the temperature dependent effect on SIV failure. Two different dielectrics, USG and CDO were used in this study.

By assuming a lognormal distribution, the normalized resistance changes for USG interconnects at the three different test temperatures are shown in Figure 5.9. Since there is no current applied during HTS test, the resistance change and the associated void formation can only be caused by stress migration. For SIV, there exists a critical temperature at which the SIV lifetime is the minimum. This is anticipated since there are two main processes which determine the SIV failure rate [161], namely the driving force by stress gradient and the atomic diffusion. Such a critical temperature is also observed in Figure 5.9, where the median resistance change at 200 °C is higher than that at 150 and 250 °C. Therefore, the critical temperature is around 200 °C, close to 190 °C as reported by Ogawa *et al.* [149] for Cu line-via structures.

Figure 5.9: Normalized resistance change at three different test temperatures for USG interconnects after 1344 hours baking.

The resistance change for both USG and CDO interconnects after HTS at 200 °C is shown in Figure 5.10. It can be seen that the CDO interconnects show much larger resistance drift than that of USG interconnects. About 40% of the CDO samples show open circuit failure whereas the maximum resistance change in the USG samples is only 10%. The results show that the SIV reliability for USG interconnects is much better than that of CDO interconnects.

Figure 5.10: Normalized resistance change for both USG and CDO interconnects after 1334 hours baking at 200 °C.

Failure analysis is performed on the failed samples and their micrographs are shown in Figure 5.11. Voids are found to nucleate at the bottom of via for both USG and CDO interconnects. However, after void nucleation, the void growing dynamics between USG and CDO interconnects are found to be different. For USG interconnects, the nucleated voids grow horizontally along the via bottom as shown in Figure 5.11(a). On the other hand, for CDO interconnects, the nucleated voids grow vertically along the via sidewall as shown in Figure 5.11(b).

It is noted that SIV void can also be formed beneath the via due to grain growth, especially for the via connected to wide lines in line-via structures [149]. However, such SIV void is not observed in this experiment, probably due to the thorough annealing during sample fabrication and the relatively narrow line width of the samples. For low-k interconnect, plastic deformation can also lead to interconnect failure in via under high von Mises stress [7, 173], and again such a failure mode is not observed in this experiment. Hence we limit our discussion to SIV failure in the via in this work.

Figure 5.11: Failure analysis image by FIB (a) Failure mode I, USG interconnects; (b) Failure mode II, CDO interconnects.

5.3.1.2 Modeling of via SIV process

5.3.1.2.1 Void nucleation

As shown in our previous work [68], the presence of defects acts as the void nucleation site for SIV in Cu line structure. For Cu line-via structure considered in this work, such process-induced weak points are reported to be located at the sidewall at via bottom due to poor diffusion barrier coverage [69]. In fact, the SIV performance is shown to be strongly dependent on the adhesion strength of diffusion barrier/Cu interface as well as the step coverage of diffusion barrier layer [174]. Also as reported by Lim *et al.* [165], the presence of any intrinsic weak point around via was the dominant mechanism in determining the SIV reliability. Therefore, we consider via bottom as the void nucleation site.

Finite element analysis is employed to simulate the hydrostatic stress distribution in the via region. Multi-physics software ANSYS[®] is used to construct the 3D model for the Cu line-via structure. The dimensions of the finite element model are the same as the fabricated test structures. The finite element model is shown in Figure 4.4. The Ta diffusion barrier and SiN cap layer are also included as shown in Figure 4.4. The x, y, z axial directions are along the line length, line width and line thickness, respectively. The material properties are taken from Ref. [40].

The hydrostatic stress is simulated through the *solid45* thermo-mechanical analysis by assuming stress free temperature (SFT) and test temperature at 350 and 200 °C respectively. For the boundary conditions, the substrate bottom is fixed with zero displacement. The vertical symmetrical plane is constrained to remain vertical arising from the mirror symmetrical nature of the structure while the nodal points are allowed to

undergo in-plane movements during deformation. The top surface is not constrained. All the interfaces between dissimilar materials are treated as perfectly bonded.

Hydrostatic stress distributions of via for USG interconnects are shown in Figure 5.12. For both USG and CDO interconnects, it can be seen that the hydrostatic stress at via bottom is higher than that in the via body and the maximum hydrostatic stress is located at the outer corner of via bottom, which reinforce the previous statement that via bottom is the SIV void nucleation site. Therefore, the void nucleation site located at the outer corner of via bottom is due to the intrinsic nature of the structure as well as process-induced defects. Maximum hydrostatic stress at via bottom is also reported in the work by Wang *et al.* [171]. After the tiny void nucleation, the stress at the void site is small due to stress relaxation [111] and Cu atoms can diffuse away from the void nucleation site under the stress gradient, causing the void to grow and relaxing the tensile stress in the via simultaneously. The existence of the positive hydrostatic stress gradient from the void nucleation site will be shown in the subsequent section.

Figure 5.12: Hydrostatic stress distributions of via for USG interconnects (unit: MPa).

5.3.1.2.2 Void growth

As discussed in previous section, the void nucleation site is located at the outer corner of via bottom by employing the maximum hydrostatic stress as void nucleation criteria [153]. Using sub-modeling technique [175], the finite element mesh at the via bottom can be meshed very finely to adequately resolve the stress distribution in the presence of the tiny void. The tiny nucleated void volume is chosen to be $10 \times 10 \times 10 \text{ nm}^3$ [18]. The hydrostatic stress distribution in the presence of tiny void is shown in Fig. Figure 5.13 for both USG and CDO interconnects.

As shown in Figure 5.13, the stress on the tiny void surface is low and the stress distribution away from the void does not changed much as also reported by Shen *et al.* [111]. Therefore, a positive hydrostatic stress gradient is developed from the void nucleation site to its surrounding. This positive stress gradient drives Cu atoms to diffuse away from the void surface for stress relaxation, rendering void growth. It is also noted that the directions of the positive stress gradient are different for USG and CDO interconnects as indicated by the arrow in Figure 5.13(b) and Figure 5.13(c). For USG interconnect, the diffusion flux is along the via bottom while for CDO interconnects, the diffusion flux is along the via sidewall. The different diffusion flux directions lead to different void shapes and this is indeed observed experimentally as well as by the following dynamic simulations.

Figure 5.13: Hydrostatic stress distribution at via bottom after void nucleation by sub-modeling technique. b) USG interconnect; (c) CDO interconnect.

To simulate the void growing process after its nucleation, a numerical calculation is performed with the aid of element death technique, which has been implemented in the simulation and analysis of solder joint and package reliability [176] as well as SIV modeling in Cu interconnects [111]. After thermo-mechanical analysis, the element corresponding to the maximum hydrostatic stress gradient is deleted to simulate the voiding process. The simulation and element deletion are repeated over and over again to simulate the void growing process.

Figure 5.14 shows the simulated voiding process. The simulated voiding is consistent with the two failure modes observed in Figure 5.11. Figure 5.14(a)-(c) shows the voiding process for USG interconnects while Figure 3.3(d)-(f) shows the voiding process for CDO interconnects. In both cases, voids start to grow from the outer corner of the via bottom. After that, void grows horizontally along via bottom for USG interconnects as shown in Figure 5.14(a)-(c). For CDO interconnects, void grows along the inner via sidewall as shown in Figure 5.14(d)-(f).

Figure 5.14: Two different failure modes for SIV failure in via simulated by ANSYS[®]. (a)-(c): CDO interconnect; (d)-(f): USG interconnect.

5.3.1.3 SIV Comparisons

5.3.1.3.1 Stress gradient

As hydrostatic stress gradient is the main driving force for SIV failure, it is necessary to compare the stress gradient along different axial directions between USG and CDO interconnects. FEA shows that the maximum hydrostatic stress in via for CDO interconnects (125 MPa) is much lower than that for USG interconnects (215 MPa), in agreement with the work by Paik *et al.* [173]. However, the stress gradients for CDO interconnects are much higher than that of USG interconnects as shown in Figure 5.15 and it is believed that it is this high stress gradient attributes to a poor SIV performance observed for CDO interconnects [172].

Figure 5.15: Stress gradient comparisons between CDO and USG interconnects.

The stress gradients along x and y directions are comparable for both USG and CDO interconnects, arising from the symmetrical nature of the via. For USG interconnects, the maximum stress gradients are along x and y directions, driving Cu atoms to diffuse horizontally. This corresponds to the failure mode in Figure 5.11(a). For CDO interconnects, the maximum stress gradient is along z direction, driving Cu atoms to diffuse along the z direction. This corresponds to the failure mode in Figure 5.11 (b). The different magnitude of axial stress gradients in via between USG and CDO interconnects are within expectations due to the dramatic stress component differences between SiO₂ and low-k interconnects as reported by Paik *et al.* [173].

5.3.1.3.2 Confinement effect

Another contribution to the different SIV performance between USG and CDO interconnects is the different degree of confinement effect to the via by the surrounding materials. FEA is employed to calculate the effective bulk modulus for the via and line structures for both USG and CDO interconnects [94].

In confined metal interconnects, the change in the local hydrostatic stress and atomic concentration is given by [51]

$$\frac{dC}{C} = -\frac{d\sigma_H}{B} \quad (5.19)$$

where B is the effective bulk modulus relating the stress and strain, C is the atomic concentration and σ_H is the local hydrostatic stress. From Eq. (5.19), the volumetric strain is connected to the hydrostatic stress change through effective bulk modulus B . Atoms diffusing under the stress gradient give rise to local atomic concentration change, which re-establishes the local stress field according to Eq. (5.19), relaxing the local hydrostatic stress. Therefore the subsequent stress gradient driving force is smaller due to the above-mentioned stress relaxation in the void growing process. From Eq. (5.19), the local stress change $d\sigma_H$ is given by $-B \cdot dC / C$. For the same local atomic concentration changes or the same amount of atom redistribution in interconnects, interconnect structures with higher confinement effect will relax more local hydrostatic stress. It is noted here that the stress gradient is the driving force, the atomic concentration change is the result of diffusion under stress gradient, and the atomic concentration change relax the local stress under the confinement effect. These three processes are occurring simultaneously in the SIV process. Therefore B is a parameter to measure the stress relaxation due to atom redistribution in the context of SIV [145].

The concept is similar to “back diffusion” in Electromigration (EM) studies [48]. The stress gradient in SIV is analog to the electron wind force in EM. Backflow stress as a result of atomic concentration change at cathode and anode under diffusion in EM is analog to $d\sigma_H$ in Eq. (5.19) which is caused by atomic concentration change under stress gradient induced diffusion. From the previous discussion, $d\sigma_H$ is higher for interconnect structures with higher confinement effect for the same local atomic concentration

changes, so higher confinement effect shall lead to higher “back diffusion” in SIV process. This existence of “back diffusion” is also validated based on the fact that the diffusion controlled stress relaxation in unpassivated Cu interconnects is significantly higher than that in passivated Cu interconnects due to the “backflow diffusion” under confinement effect [131, 158].

The calculated effective bulk modulus is summarized in Figure 5.16, and it can be seen that B is dependent on the shape of the cross section for the structure and the dielectric type. B is smaller than the elastic modulus of the interconnect since the stress is partially shared with the surrounding dielectrics [14]. It is shown that the effective bulk modulus for CDO interconnect is lower than that of USG interconnect. In the line structure, effective bulk modulus of USG interconnect is two times higher than that of CDO interconnects. In the via structure, effective bulk modulus for CDO interconnect is only 1/3 of that of USG interconnects in via.

Figure 5.16: Effective bulk modulus calculations for both USG and CDO interconnects.

During the SIV process, the diffusion of Cu atoms is driven by the hydrostatic stress gradient. Since effective bulk modulus for USG interconnects is three times higher than that for CDO interconnects in via, the “back diffusion” in USG interconnects will be much higher than that in CDO interconnects. Besides that, the hydrostatic stress gradient

along the via direction in CDO interconnects is seven times higher than that in USG interconnects as shown in Figure 5.15. Therefore the effective atomic flux in USG interconnects will be very much lower than the case of CDO interconnects, leading to its much longer SIV lifetime, and the void is less likely to propagate along the via direction in USG interconnects. Instead, the voids are growing along the x and y direction at via bottom as shown in Figure 5.14(b) for USG interconnects.

5.3.1.4 Discussions

From the above discussion, we see that while the stress gradient determines the direction of the void growth, the rate of void growth is governed by the confinement effect through the effective bulk modulus and the magnitude of the stress gradient. In fact, SIV performance is also dependent on many other parameters such as diffusivity [177], the adhesion strength between metallic material and barrier layer [118], grain structure [149], defect density [164], etc., but all these factors are affected by the manufacturing process, and hence they are considered as the extrinsic factors to the SIV reliability.

Hence the two intrinsic factors affecting SIV reliability are the stress gradient and effective bulk modulus. Stress gradient is dependent on the geometry and materials of the interconnect system, SFT and test temperature. Effective bulk modulus is determined by the thermo-mechanical properties of the overall interconnect system. Therefore, these two factors are strongly dependent on the thermo-mechanical properties of dielectrics and they can be estimated using FEA as demonstrated in this work.

Besides CDO, there are other types of low-k dielectrics used in industry for different technology nodes [178]. As different low-k materials display different thermo-mechanical behaviors, their SIV reliability will be different. With the above findings, we extend our

discussions to three more commonly used low-k dielectrics: SiCOH, porous MSQ and SiLK. The objective here is to understand how the thermo-mechanical properties of the dielectrics affect the stress gradient as well as confinement effect in via. The concept can also be applied to line structures as well. The mechanical properties of these dielectrics are listed in Table 5.1 [82, 83, 179].

Table 5.1: Thermo-mechanical properties of different dielectric materials [82, 83, 179].

Dielectrics	Elastic modulus (GPa)	Poisson ratio	CTE (ppm/°C)
USG	71.4	0.16	0.62
SiCOH	16.2	0.3	12
CDO	4.47	0.3	12.9
Porous MSQ	3.6	0.25	7.3
SiLK	2.5	0.4	66

The simulated effective bulk modulus and total stress gradients are listed in Table 5.2. Due to the low elastic modulus and higher thermal expansion for low-k dielectrics, the stress gradients for low-k interconnects are much larger than that of USG interconnects. Among the four low-k dielectrics considered in this work, SiLK interconnect is associated with the highest stress gradient and the lowest confinement effect which is due to its very low modulus and high coefficient of thermal expansion (CTE) for SiLK, and thus its SIV reliability is expected to be the poorest. In short, the low elastic modulus and high CTE of various low-k dielectrics will impose significant challenges in the SIV reliability for a given interconnect line width. Further reduction in the line width will make the situation worse as will be studied in the future.

Table 5.2: Simulated total stress gradient and effective bulk modulus for different dielectric materials.

Dielectrics	Stress gradient (GPa/ μm)	Effective bulk modulus (GPa)
USG	9.1	36.6
SiCOH	16	14.24
CDO	16.4	12.9
Porous MSQ	16.03	15.8
SiLK	23.6	10.5

5.3.1.5 Summary

In this work, 3D finite element simulations are performed to simulate the void nucleation and void growing process during SIV for line-via structures with USG and CDO dielectrics, and the simulated void growing dynamics is found to be consistent with the two observed failure modes. With the aid of FEA, the poor SIV performance for CDO interconnect is understood to be due to a higher stress gradient at the via bottom and smaller confinement effect of via. In fact, the intrinsic factors that determine the SIV performance of a line-via structures are found to be the stress gradient and the effective bulk modulus. In view of the lower effective bulk modulus and higher stress gradients of the low k dielectrics, it is expected that line-via structure with low k dielectric will suffer more severe SIV reliability.

5.3.2 Thermo-mechanical stress modeling in Cu interconnects

Significant thermo-mechanical stress is built up during device fabrication and operating conditions, arising from the differences in the coefficient of thermal expansion (CTE) of the different materials in the device. High thermo-mechanical stress can lead to stress induced voiding (SIV) [68], plastic deformation [7], cracking [180], interface debonding, and eventually mechanical failure. Therefore, it is important to understand both the magnitude and nature of the thermo-mechanical stress in interconnects.

To reduce the RC delay and improve the performance of integrated circuits, various low-k dielectrics have been implemented in Cu interconnects. The characteristics of thermo-mechanical stress in interconnects depend on how effective the Si substrate and the dielectrics confine the metal interconnect from expanding freely. Therefore, the

thermo-mechanical properties of the dielectrics and the geometry of the structure can affect the magnitude and nature of the thermo-mechanical stress greatly. Compared with SiO₂, those low-k materials are expected to have poor mechanical properties and this shall lead to severe stress-related problems in future low-k interconnects.

The failure site varies in interconnects under thermo-mechanical stress. Ogawa *et al.* reported SIV void formation under via due to grain growth without thorough annealing [149]. Void in via in the form of copper pull up is attributed to poor interface adhesion in Cu/FSG interconnects [169]. Hommel *et al.* also reported SIV voids along via side walls and via bottom for Cu interconnects [161]. In the experimental work by An *et al.* [157], dislocation was observed for wide interconnect while SIV void was formed for narrow interconnect. Via deformation was also observed in Cu/SiLK line-via structure [181]. In fact, the type and location of the failure is strongly dependent on the interconnect geometry, dielectric type as well as the microstructure of the interconnect.

The effect of microstructure or process related factors on mechanical failure have been investigated extensively such as barrier film step coverage [169], adhesion strength between barrier metal and Cu [182], Cu grain growth [161, 183], impurity doping [184], texture of the film [185], etc. Thermo-mechanical stress is among the major driving forces for all the mechanical damages observed in ULSI interconnects. Unfortunately, the knowledge of thermo-mechanical stress with different dielectrics and line widths is still limited for Cu line-via structures, especially with the recent Cu/air-gap interconnect. This is believed to be that the stress characterization techniques (e.g. curvature measurement, x-ray diffraction and analytical modeling) are limited to simple interconnect test structures and have insufficient spatial resolution for the detailed stress distribution in complicated line-via interconnect structures. On the other hand, with finite element

analysis (FEA), the local stress distributions based on realistic interconnect structures can be simulated and analyzed.

In this section, we perform finite element modeling to compute the thermo-mechanical stresses in Cu interconnects and investigate the effect of dielectric materials as well as line width on the stress distributions in line-via structures. In the modeling, six different types of dielectrics ranging from SiO₂ to air-gap are chosen to study the effect of thermo-mechanical properties of dielectrics on the thermo-mechanical stress. Three different line widths are chosen to investigate the geometrical factor on the thermo-mechanical stress. In particular, the hydrostatic stress and von Mises stress are examined to reveal the potential failure locations systematically. The modeling results are also compared with our experimental findings as well as the literature reported works.

5.3.2.1 Finite element analysis

Finite element analysis has been employed in the investigation of thermo-mechanical stress in Al and Cu interconnects for line structures [55, 186]. Compared with the line structures, line-via structures are more complicated with a cylinder via and encapsulated diffusion barrier layer. Due to the structure and material inhomogeneities in the via region, the thermo-mechanical stress can be highly non-uniform. Figure 5.17 shows the finite element mesh of conventional dual-damascene (DD) Cu interconnect and air-gap DD Cu interconnect for line-via structures. Commercial finite element software ANSYS[®] is employed for the simulation.

To investigate the effect of different dielectrics on the conventional DD Cu interconnect as shown in Figure 5.17(a), the dielectric region is either filled with SiO₂, SiCOH, CDO, porous MSQ or SiLK in the simulations. For the air-gap DD Cu

interconnect in Figure 5.17(b), low-k dielectrics SiCOH is used as inter-level dielectric in via dielectric region while M1 and M2 dielectric region is filled by air. For the fabrication process flow of the air-gap DD Cu interconnect, one may refer to reference [187].

Figure 5.17: Finite element mesh (a) Conventional Cu interconnects (b) Cu/air-gap interconnects

The direction of Cu line is parallel to the x-axis while the line width and thickness are along the y- and z- directions respectively. As shown in Figure 5.17, M1-via-M2 is bound by the top and bottom layers of SiO₂, each having a thickness of 0.3 μm . Cu line is also surrounded by 50-nm-thick cap layer SiN and 25-nm-thick diffusion barrier layer Ta. The circular Cu via is located at the center in the x- direction with a diameter of 0.2 μm . Via height is 0.7 μm . Three different line widths of 0.26, 0.4, and 0.6 μm are chosen for the analysis while the line thickness is fixed at 0.35 μm . The thickness of the substrate Si is 100 μm . Some of the above mentioned dimensions are according to the works of Tan *et al.* [22].

As the simulation of thermo-mechanical stress is done by modeling a unit structure taken from a large repeated structure in realistic interconnects, the finite element model and its boundary conditions are critical to describe the periodic array of the line-via structures. The finite element model in Figure 5.17 represents one half of the unit

structure, with xz plane being the mirror symmetry plane showing the middle cut of the line-via structure. With different line widths in the simulation, the line spacing is kept the same as the line width. The substrate bottom plane is fixed while mirror symmetry is imposed on all the lateral surfaces and only the top surface is free to move during deformation.

The SFT is set at 350°C and the test temperature is at 200°C as is typically done [188]. All materials are assumed to be isotropic linear elastic solids. The thermo-mechanical properties of Cu, Si and all the dielectrics materials are shown in Table 5.3. It is noted that spin-on organic polymer-based SiLK dielectric has the lowest elastic modulus and highest CTE among all the dielectrics besides air-gap. As the microstructure-dependent nonlinear behavior of Cu is not considered in this work, the simulated thermo-mechanical stress is approximated to the first order effect only.

Table 5.3 Thermo-mechanical properties of Cu, Si and different dielectric materials [82, 83, 179].

Dielectrics	Elastic modulus (GPa)	Poisson ratio	CTE (ppm/°C)
Cu	104	0.352	17.7
Si	130	0.28	4.4
SiO ₂	71.4	0.16	0.62
SiCOH	16.2	0.3	12
CDO	4.47	0.3	12.9
Porous MSQ	3.6	0.25	7.3
SiLK	2.5	0.4	66
Air	10 ⁻⁸	0.3	100

5.3.2.2 Results and discussions

As via-M2 is an integral part of the DD line-via interconnect structure, we divide our discussion to M1 and via-M2, respectively.

5.3.2.2.1 Thermo-mechanical stress in M1

The maximum axial stress along x-,y-,z- directions in M1 are shown in Figure 5.18(a), Figure 5.18(b) and Figure 5.18(c), respectively. By comparing the magnitude of the axial stresses, stress along the line is the largest principle stress, followed by the stress across the line and the stress long the line thickness. This is consistent with experimental measured thermo-mechanical stress in line structures by x-ray diffraction technique [55].

Figure 5.18: Maximum axial stress in M1. (a) Stress along x- axis (b) Stress along y- axis (c) Stress along z- axis

The relative magnitudes of the stress components (σ_x , σ_y , σ_z) reflect different degrees of confinement in interconnect. Since the in-plane stress (σ_x , σ_y) are mainly attributed to the CTE mismatch and confinement between the interconnect and Si substrate, it is

relatively insensitive to the changing of dielectric materials. With different dielectrics from SiO₂ to air-gap, σ_x and σ_y decrease by 26% and 37% respectively at 0.26 μm line width.

On the other hand, σ_z is strongly dependent on the confinement effect between Cu and dielectrics, which can be revealed in Figure 5.18(c). As the dielectrics are changing from SiO₂ to air-gap, σ_z decreases by as much as 67% for 0.26 μm line width. This is because the elastic modulus of the low-k dielectrics is much lower than that of SiO₂ as shown in Table 5.3.

From Figure 5.18, we can see that σ_x decreases slightly and σ_y , σ_z increase slightly with increasing line width. The slight increase of σ_y is due to the increased constraint provided by the substrate for wider lines. It can be seen that the thermo-mechanical properties of dielectrics are more critical in determining the axial stress than the line width with an exception of σ_z for Cu/SiLK interconnects in Figure 5.18(c). σ_z increases from 81 MPa to 147 MPa with line width increasing from 0.26 μm to 0.6 μm , due to the a very high CTE and low elastic modulus of SiLK.

Hydrostatic stress is proven to be the driving force for SIV failure [153] while von Mises stress is usually used as a criterion for plastic deformation [154]. The maximum hydrostatic stress and von Mises stress in M1 are shown in Figure 5.19(a) and Figure 5.19(b), respectively. It can be seen that the hydrostatic stress is relatively constant with different line widths. Due to the low elastic modulus and high CTE of low-k dielectrics as shown in Table 5.3, the hydrostatic stress for Cu/SiO₂ is much higher than that of other Cu/low-k interconnect.

As shown in Figure 5.19, the magnitude of von Mises stresses is higher than that of hydrostatic stress for all the dielectrics, and this is also reported by Paik *et al.* [173]. This is because for low-k interconnects, the vertical confinement from the dielectrics is reduced dramatically while the in-plane confinement does not change significantly. Therefore, the magnitude of out-of-plane stress σ_z is much lower than σ_x and σ_y for low-k interconnects as shown in Figure 5.18 (a)-(c), which leads to a very high von Mises stress.

Figure 5.19: (a) Maximum hydrostatic stress in M1 (b) Maximum von Mises stress in M1.

It is also noted that von Mises stress increases with increasing line width, indicating an increasing driving force for plastic yield in metal line [131]. Since σ_z decreases with increasing line width as shown previously and

$$\sigma_{von} = \frac{1}{\sqrt{2}} \left[(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2 \right]^{1/2},$$

the increasing von Mises stress with line width can be expected. This possibly explains the recent work by An *et al.* [157] where SIV void was found in narrow line due to hydrostatic stress and the initiation and slip of dislocations were found in wide line due to the high von Mises stress.

Figure 5.20 (a)-(d) and Figure 5.21(a)-(d) show the hydrostatic stress and von Mises stress distributions for Cu/SiO₂, Cu/CDO, Cu/SiLK and Cu/air-gap interconnects in M1, respectively. For clearer visualization, only Cu is shown with surrounding materials removed. A transparent via is also placed in each figure to indicate the via position on top

of M1. It is noted that the hydrostatic stress distributions are different for interconnects with different dielectrics. For Cu/SiO₂ interconnect in Figure 5.20(a), the maximum hydrostatic stress is located at the lower corner of M1. The hydrostatic stress distributions for Cu/CDO and Cu/air-gap interconnect are similar, with their maximum hydrostatic stress located at the edge of M1, away from the via. Their only difference is the magnitude of the hydrostatic stress where it is higher for Cu/air-gap interconnect as compared to that of Cu/CDO interconnect. For Cu/SiLK interconnect in Figure 5.20(c), the hydrostatic stress beneath the via is negative, representing a compressive stress. This is caused by a very negative σ_z beneath via, resulting from the very low elastic modulus and very high CTE for SiLK dielectrics.

For von Mises stress distributions, a maximum von Mises stress is beneath via in M1 for Cu/SiLK interconnects as shown in Figure 5.21(c). This is also consistent with the observed negative σ_z beneath via. For other types of interconnects, the von Mises stress distributions are similar, and the maximum von Mises stress is located at the lower edge of M1.

Figure 5.20: Hydrostatic stress distribution in M1. (a) Cu/SiO₂ (b) Cu/CDO (c) Cu/SiLK (d) Cu/Air-gap. (Units: MPa)

Figure 5.21: Von Mises stress distribution in M1. (a) Cu/SiO₂ (b) Cu/CDO (c) Cu/SiLK (d) Cu/Air-gap. (Units: MPa)

5.3.2.2.2 Thermo-mechanical stress in via-M2

The maximum hydrostatic stress and von Mises stress in via-M2 are shown in Figure 5.22(a) and Figure 5.22(b), respectively. It is noted that the magnitudes for both hydrostatic stress and von Mises stress in via-M2 are slightly higher than those in M1. Similar to Figure 5.19, the hydrostatic stress in low-k interconnects is lower than that in SiO₂ interconnect while the opposite is true for von Mises stress. The hydrostatic stress is relatively insensitive to the line width while von Mises stress increase dramatically with increasing line width. In the extreme case of Cu/SiLK interconnect, the maximum von Mises stress can increase up to 1600 MPa for 0.6 μm line width.

Figure 5.22: (a) Maximum hydrostatic stress in M2 and via (b) Maximum von Mises stress in M2 and via

Figure 5.23(a)-(d) and Figure 5.24(a)-(d) show the hydrostatic stress and von Mises stress distributions for Cu/SiO₂, Cu/CDO, Cu/SiLK, and Cu/air-gap interconnects in via-M2, respectively. For Cu/SiO₂, Cu/CDO and Cu/air-gap interconnects, the maximum hydrostatic stress is located at the upper corner of M2. For Cu/SiLK interconnect, the maximum hydrostatic stress is located at the edge of M2, away from the via as shown in Figure 5.23(c).

Figure 5.23: Hydrostatic stress distribution in via-M2. (a) Cu/SiO₂ (b) Cu/CDO (c) Cu/SiLK (d) Cu/Air-gap. (Units: MPa)

Figure 5.24: Von Mises stress distribution in via-M2. (a) Cu/SiO₂ (b) Cu/CDO (c) Cu/SiLK (d) Cu/Air-gap. (Units: MPa)

The von Mises stress distributions are also different among different interconnects. For Cu/SiLK interconnect, the maximum von Mises stress is located in via while for the other interconnects, the maximum von Mises stress is located at the upper interface of M2. As via dimension is very small along x- and y- directions, the thermo-mechanical properties of via are mainly determined by the thermo-mechanical properties of the dielectrics. Since the CTE of SiLK is four times larger than that of Cu as shown in Table 5.3, σ_z is compressive in via, leading to very high von Mises stress in via. The CTEs of all other dielectrics are lower than that of Cu, resulting in a tensile σ_z in via and hence lower von Mises stress.

5.3.2.2.3 Discussions

As shown in Figure 5.20, the maximum hydrostatic stress is located at the lower corner of M1 for Cu/SiO₂ interconnects. However, there is no reported stress related failure at that location due possibly to the presence of process-induced weak points which supersede the intrinsic weak spots as determined using FEA. The commonly observed stress related damage in M1 for line-via structures is SIV void beneath via [149, 169], and this is attributed to either the contamination below via [169] or the grain growth during annealing [149]. As the dielectrics are migrating from SiO₂ to SiLK, the hydrostatic stress is decreasing and the von Mises stress is increasing. Therefore, the severity of SIV beneath via is decreasing with a decreasing hydrostatic stress. The hydrostatic stress beneath via is even become compressive for Cu/SiLK interconnect in Figure 5.20(c). On the other hand, the chances of plastic deformation (generation of dislocation, local debonding) is increasing, especially for Cu/SiLK interconnects as shown in Figure 5.21(c).

For the maximum hydrostatic stress located at the corner of M2 as shown in Figure 5.23(a), Figure 5.23(b) and Figure 5.23(d), such location is reported to be the void nucleation site for M2 EM test structures under high hydrostatic stress [22]. As shown in the TEM image from our recent experiment is shown in Figure 5.25(a) for Cu/SiO₂ interconnect. Via bottom is also a high hydrostatic stress site as shown in Figure 5.23(a), Figure 5.23(b) and Figure 5.23(d), and SIV void can form at via bottom due to a high hydrostatic stress and a poor diffusion barrier coverage [69]. A typical SIV void at via bottom is shown in Figure 5.25(b) for Cu/CDO interconnect [172].

Figure 5.25: TEM image of EM failure in M2 for Cu/SiO₂ interconnect. (b) SEM image of SIV failure in via bottom for Cu/CDO interconnect.

As shown in Figure 5.24(c) for Cu/SiLK interconnect, the high von Mises stress in via can lead to plastic deformation in via. The mechanically weak low-k dielectrics are unable to prevent this from occurring. Via failure through barrier layer cracking is indeed observed in the experimental work by Fayolle *et al.* [181] for Cu/SiLK interconnects. The same finding was also reported by Filippi *et al.* [189] for Cu/SiLK interconnects.

From the stress distribution results shown in Figure 5.20-Figure 5.21 and Figure 5.23-Figure 5.24, both hydrostatic and von Mises stress distributions are similar between Cu/CDO and Cu/air-gap interconnects. The magnitude of the hydrostatic stress and von Mises stress are also comparable between Cu/CDO and Cu/air-gap interconnects. Therefore, it can be inferred that the stress related damages will be similar for Cu/CDO and Cu/air-gap interconnects by assuming the same microstructures of the interconnects.

5.3.2.3 Summary

In this part of study, thermo-mechanical stresses in Cu interconnects are calculated to investigate the effect of dielectric materials as well as line width on the stress

distributions in line-via structures using finite element analysis. The simulation results are in good agreement with the experimental findings and the literature reported works.

It is found that both dielectric materials and line widths are important for the von Mises stress while hydrostatic stress is almost insensitive to the line widths. Von Mises stress is higher for larger line width, indicating a higher chance for plastic deformation for wider interconnects. For M1, the chance of SIV beneath via is decreasing as the dielectrics are migrating from SiO₂ to SiLK. However, the chance of plastic deformation is increasing, especially for Cu/SiLK interconnects. For via-M2, via bottom and upper corner of M2 failures are due to the high hydrostatic stress. The stress distributions for Cu/air-gap interconnects are found to be similar to those for Cu/CDO, and hence the failure mechanism for Cu/air-gap interconnects is expected to be similar to that of Cu/CDO interconnects.

5.4 Conclusion

In this chapter, we present a lifetime model from the energy perspective for SIV. The SIV lifetime is found to be strongly dependent on the passivation quality at the cap layer interface, the confinement effect by the surrounding materials to interconnects, and the available diffusion paths in interconnects.

In the subsequent sections of the chapter, the effects of interconnect design factors on SIV performance are explored with FEA. 3D finite element simulations are performed to simulate the void nucleation and void growing process during SIV for line-via structures with SiO₂ and low-k interconnects. With FEA, the mechanisms for poor SIV performance of low-k interconnects are revealed as a higher stress gradient at via bottom and smaller

confinement effect of via. In the last part of this chapter, both hydrostatic stress and von Mises stress are simulated as a function of interconnect line width and dielectric materials. Compared with SiO_2 based interconnects, low-k interconnects are associated with a higher von Mises stress, and this shall lead to severe stress related problems in future low-k interconnects.

6. CONCLUSION AND FUTURE WORK

6.1 Conclusion

Demand for higher speed ULSI with more complex functionality is driving the continuous change in the interconnects' structures and materials as well as the interconnects processing technology. On the other hand, their reliability requirements are expected to be higher with the increasing complexity of ULSI. Therefore, reliability evaluation and improvement of new interconnects require a more thorough understanding of the physics of EM and SIV from both physical-based modeling and experimental investigations. With finite element modeling, the various driving forces present in interconnect during EM or SIV test can be simulated with the coupling effect taken into consideration, and hence the failure physics for EM and SIV can be revealed. In this thesis work, we investigate EM and SIV performance for Cu interconnects through both finite element modeling and experiments.

Our study starts with a comprehensive review on the overall interconnect reliabilities with special focus on EM and SIV. The application of multi-physics FEA on the interconnect system of ULSI is rather limited in both industry and academic field. However, decades of advances in computational science have brought us smarter algorithms and faster, more powerful hardware that puts multi-physics FEA tools within reach for all engineers and scientists. It opens up new opportunities for modeling and simulating real-world applications as well as a world of technological investigation in the

interconnect system of the integrated circuit. Chapter 3 is devoted to the finite element analysis review with special focus on the interconnect reliability modeling by FEA.

In Chapter 4, a modified EM modeling methodology is proposed to improve the EM modeling accuracy. This methodology is based on the driving force approach and its mathematical formulations are derived based on Green's theorem. The formulations are implemented through FEA, and the EM void nucleation and its growth can be simulated through the developed static and dynamic simulation FEA codes. This EM modeling methodology is applied to investigate the EM dependence on interconnect design factors in the subsequent part of this chapter. The lifetime enhancement factor in EM reservoir structures is found to decrease with increasing EM stress current experimentally. The analytical formulation for the lifetime enhancement factor is derived to reveal the dependence of lifetime enhancement factor on EM test conditions. In the width transitional structures, EM characteristic is found to be dependent on electron flow direction and ratio of the lengths in width transition Cu interconnects. It is found that EM lifetime significantly shorten when the electron flow direction is from narrow-to-wide segment. For the Blech product, it is found that Blech product is lower for Cu interconnects at high temperature due to its inelastic behavior. Lastly, the issue in high temperature and high stress current EM test is presented. The variation of activation energy and current density exponent in Black's equation is derived analytically. This variation can be important in future EM test in low-k interconnects with severe Joule heating.

In Chapter 5, we propose a lifetime model from the energy perspective for SIV. A SIV lifetime equation is derived which is similar to the Black's equation for EM failure. In the subsequent part of the chapter, the effects of interconnect design factors on SIV

performance are explored with FEA. 3D finite element simulations are performed to simulate the void nucleation and void growing process during SIV for line-via structures with SiO₂ and low-k interconnects. Thermo-mechanical stresses in Cu interconnects are analyzed to investigate the effect of dielectric materials as well as line width on the stress distributions in line-via structures. The hydrostatic stress and von Mises stress distributions are simulated and their distributions show the potential failure sites for current and future Cu interconnects.

Reliability evaluation and improvement of new interconnects require a deep understanding of the physics of EM and SIV. However, experimental investigations can be very expensive and slow. Furthermore, not all underlying physics in EM and SIV can be captured experimentally. Both EM and SIV failure physics have been explored through FEA modeling in this thesis work and FEA is proven to be a necessary tool for future reliability research for interconnects.

6.2 Future work

In this thesis, we have developed and laid the groundwork on the finite element modeling to investigate both EM and SIV failure mechanisms in interconnect. The methodologies in this work can also be applied to other fields of microelectronics, e.g. packaging reliability, solder joint reliability, etc. Although the FEA explains many experimental results, however, it is by no means exhaustive, and from our point of view, more work still need to be further studied.

6.2.1 3D modeling of EM process using AFD

3D EM modeling using AFD is mainly studied by three research groups: Tan *et al.* [22, 40, 85], Dalleau *et al.* [91, 190] and Liu *et al.* [60]. AFD formulations have been improved in Section 4.3. However, there are still some limitations for EM modeling using AFD method (driving force approach). Also, the estimation of TTF using AFD is different among different research groups.

In the dynamic simulation, the element is considered to be a void when the atomic concentration reaches 10% of the initial concentration. The TTF is the summation of the time needed to delete all the elements for a critical void. Therefore, TTF in Eq. (4.12) can be re-written as

$$TTF = \sum_{i=1}^n T_i = \ln 10 \sum_{i=1}^n 1/F_i \quad (6.1)$$

n is the number of deleted elements simulating the whole void formation.

There are several limitations for the TTF calculation in this method:

1. From Eq. (6.1), TTF is the time for void growing process. For nucleation limited failure, void nucleation time is much longer than the void growing time and the void nucleation time is not accounted for in Eq. (6.1).
2. The element is considered to be a void with 10% reduction in the atomic concentration. The actual time needed for the element to be empty needs further justifications.
3. With the local atomic concentration change due to diffusion, the local stress state should also change under the confinement effect according to Eq. (5.19). In the case of Electron Wind Force (EWF), the change of local stress is reflected in the development of backflow stress. In the case of thermo-mechanical stress, the change

of local stress is the stress relaxation of the local thermo-mechanical stress. Both stress changes can be calculated through the effective bulk modulus.

In view of the limitations stated above, the stress change due to atomic concentration change under confinement effect should be considered in future EM modeling. By considering the stress change during EM, the backflow stress due to EWF and stress relaxation under thermo-mechanical stress can be taken into consideration.

The thermo-mechanical stress may be relaxed completely during EM process. Take Cu interconnect under typical EM stress conditions, hydrostatic stress is assumed to be 60 MPa, effective bulk modulus B is 36 GPa. The atomic concentration change needed to relax the hydrostatic stress is $60\text{MPa}/36\text{GPa}=0.167\%$. Therefore, the thermo-mechanical stress can be relaxed with less than 1% in atomic concentration change.

As AFD, atomic concentration and stress state are changing during EM process; local time dependent iterative scheme is needed for the dynamic simulation. The time interval can be chosen as

$$\Delta t_i = \frac{1}{F_i} \ln \frac{N_0}{N} \quad (6.2)$$

In Eq. (6.2), Δt_i can be chosen as the time needed for a certain percentage change in atom concentration. The proposed EM dynamic simulation is shown in Figure 6.1. For each time interval, the interconnect stress state, atomic concentration and AFD distribution need to be calculated. The elements will not be deleted as this only shows the void nucleation process. The element is considered to be voided if the atomic concentration is reduced to a certain level. It is noted that the backflow stress in EM is also taken into account by updating the concentration gradient in Figure 6.1.

Figure 6.1: Proposed EM dynamic simulation

6.2.2 The inclusion of surface migration induced driving force

In this thesis work, three important driving forces have been considered and they are EWF, TGIDF and SGIDF. These driving forces can lead to the void nucleation and growth through diffusion. Under the surface migration induced driving force, the migration at the immediate surface moves atoms from convex region to concave region [59], changing the void shape. Also the mechanical stress is zero normal to the void surface.

At void surface, the atomic flux due to the elastic energy is expressed as [59],

$$J_{Surface} = \gamma \Omega \nabla \kappa \quad (6.3)$$

where γ is the surface energy, Ω is the atomic volume and κ is the surface curvature.

With the flux equation in Eq. (6.3), the AFD due to the surface migration induced driving force can be simulated. With the inclusion of surface migration induced driving force, the void shape changes during EM or SIV process can be accounted for. The calculation of the curvature gradient ($\nabla \kappa$ in Eq. (6.3)) can be challenging.

6.2.3 Interconnect reliability in 3D circuit

The scope of this thesis work is limited to the simple two-level interconnects structure alone without considering the operation of the circuit. As IC reliability is gaining more and more concerns in IC technology nowadays with decreasing device size and the impact of different failure mechanisms increases significantly with decreasing interconnect dimension and increasing number of interconnect levels, the importance of interconnect reliability in IC circuit started gaining attention in recent times.

As EWF is no longer the dominant driving force for EM as shown in this thesis work and the surrounding materials and the interconnect structure are critical to the EM and SIV performance of interconnect, 3D interconnect structure at the circuit level is necessary in order to accurately assess the interconnect reliability in ULSI. Therefore, circuit layout design can be modified based on the EM and SIV modeling results, so as to enhance the circuit reliability.

6.2.4 EM and SIV under size effect

As the feature size of Cu interconnects has been scaled into nano-scale range, Cu interconnects are more prone to electrical and mechanical failures, not only because they are subjected to more severe use conditions, but also because the critical volume for the fatal void is smaller [191]. Since the interconnect dimensions are approaching the length of the mean free path (MFP) of the electron, size effects are becoming important. This is manifested in the increase of the resistivity for nano-interconnects [192] and the size dependency in elasticity [193]. New failure mechanisms start to appear with reduced barrier layer thickness and implementation of low-k ILD in Cu nano-interconnects. EM

failure may no longer follow a lognormal distribution as in Cu nano-interconnects due to a much smaller critical void. As the atom diffusion is through various diffusion paths under various driving forces during EM, their evolutions in nano-interconnects will also affect EM significantly, with continuous increased surface to volume ratio. Therefore, the changes in mechanical and electrical properties of Cu and ILD, together with the scaling in interconnect geometry dimensions, will pose new challenges in the reliability study for Cu nano-interconnects.

The impact of size effect on EM for nano-interconnects can be probed from the following few perspectives.

1. Interconnect resistance increases dramatically due to electron scattering in the dimension below 100 nm, According ITRS 2006 [194], the maximum current density in the interconnects will reach a level of $5.15\text{MA}/\text{cm}^2$ by 2010. The maximum current density allowed in interconnects is limited by two factors: Joule heating and electron wind force. Both factors are dependent on the size effect due to scaling.
2. According to ITRS 2006 [194], barrier layer thickness has to be scaled down to 3.3 nm in 2010. The barrier layer is an integrated part of the damascene interface contributing significantly to the mechanical confinement of the interconnect to sustain EM mass transport. Thinner barrier layer implies a reduced confinement effect and the impact to EM still needs further investigation.
3. It is widely accepted that Cu/cap interface layer is the most significant diffusion path for bamboo structures.[159],[76] However, it is also reported a dominant diffusion path at Cu/liner interface in Cu narrow line.[89]. As surface to volume ratio increases dramatically for narrower interconnect and the impact to EM remains unknown.

4. Traditionally, the lognormal distribution has been used to analyze EM failure data for both Al and Cu based interconnects [195, 196]. However, for deep submicron interconnects, the resistance degradation trends reveal that the lognormal model may not be suitable to describe the EM time to failure as the nature of failures is no longer completely “gradually”. As recently reported by Tan et al.[197], Gamma distribution is found to be much more accurate than the traditional lognormal distribution in the case of a narrow Cu interconnect. This may be attributed to the fact that the failures in a narrow interconnect are more “catastrophic” in nature and hence are better described by the Gamma model. The verification is carried out with interconnect of line width of $0.25\mu\text{m}$. Further verifications can be done with interconnect of even narrower width.

The SIV model proposed in Section 5.2 is based on conventional interconnects without taking the size effect into consideration. The simulated thermo-mechanical stress from FEA is based on classical continuum mechanics, by considering the size dependency in elasticity, the thermo-mechanical stress decreases as line width is below 50 nm [193]. As line width is scaling down, plastic deformation is less likely to happen [198], which means the narrower interconnect becomes more elastic. This was later confirmed by Shen *et al.* [131] where the hysteresis becomes smaller with decreasing film thickness during thermal cycling, implying increasing difficulty of plastic deformation due to the dimensional constraint. Therefore, it is necessary to consider the size effect when modeling the mechanical reliabilities of nano-interconnect.

7. AUTHOR'S PUBLICATIONS

Journals and books:

1. C. M Tan, Y. Hou et al., "Applications of Finite Element Methods for Reliability Studies on ULSI Interconnections", to be published by Springer UK in 2010.
2. A. Roy, Y. Hou and C. M. Tan, "Electromigration in width transition copper interconnect", *Microelectron. Reliab.* **49**, 1086 (2009).
3. C. M. Tan and Y. Hou, "The changing physics in metal interconnect reliability", book chapter, in press.
4. Y. Hou and C. M. Tan, "Comparison of Stress-induced Voiding Phenomena in Copper Line-via Structures With Different Dielectric Materials", *Semicond. Sci. Technol.* **24**, 085014 (2009).
5. Y. Hou and C. M. Tan, "Stress-induced voiding study in integrated circuit interconnects", *Semicond. Sci. Technol.* **23**, 075023 (2008).
6. C. M. Tan and Y. Hou, "Lifetime modeling for stress-induced voiding in integrated circuit interconnections", *Appl. Phys. Lett.* **91**, 061904 (2007). Also be selected in publication of Virtual Journal of Nanoscale Science & Technology (issue of August 20, 2007).
7. C. M. Tan, Y. Hou, and W. Li, "Revisit to the finite element modeling of electromigration for narrow interconnects", *J. Appl. Phys.* **102**, 033705 (2007).
8. W. Li, C. M. Tan, and Y. Hou, "Dynamic simulation of Electromigration in polycrystalline interconnect thin film using combined Monte Carlo algorithm and finite element modeling", *J. Appl. Phys.* **101**, 104314 (2007).

Conferences:

9. Y. Hou and C. M. Tan, "Requirement for accurate interconnect temperature measurement for Electromigration test", 12th International Symposium on Integrated Circuits, Singapore, pp. 522-525 (IEEE, 14-16 December 2009).
10. Y. Hou and C. M. Tan, "Transient electrical thermal analysis of ESD process using 3-D finite element method", 12th International Symposium on Integrated Circuits, Singapore, pp. 284-287 (IEEE, 14-16 December 2009).
11. Y. Hou and C. M. Tan, "The multiple temperature heater platforms for solder Electromigration test conducted at room temperature", Proceedings of the 10th Electronics Packaging Technology Conference (EPTC 2008), Singapore, pp. 1148-1153 (IEEE, 9-12 December 2008).
12. Y. Hou and C. M. Tan, "Stress-induced Voiding Studies in Copper Interconnect by Finite Element Analysis", presented in 7th ASEAN ANSYS Conferences, 30-31 Oct, Biopolis, Singapore, 2008.
13. Y. Hou and C. M. Tan, "Size effect in Cu nano-interconnects and its implication on Electromigration", Proceedings of the 2rd IEEE International Nanoelectronics Conference, Shanghai, China, pp. 610-613 (IEEE, 24-27 March 2008).
14. Y. Hou and C. M. Tan, "Blech effect in Cu interconnects with oxide and low-k dielectrics", Proceedings of the 14th International Symposium on the Physics and Failure Analysis of Integrated Circuits, Bangalore, India, pp. 65-69 (IEEE, 11-13 July 2007).
15. W. Li, Y. Hou and C. M. Tan, "Dynamic simulation of Electromigration in polycrystalline thin film using combined Monte Carlo algorithm and Finite Element modeling", Symposium of Microelectronics, 29 Sep, Institute of Microelectronics, Singapore, 2006.

8. REFERENCES

References

- [1] M. T. Bohr, "Interconnect Scaling-The Real Limiter to High Performance ULSI," *IEEE IEDM Technical Digest* pp. 241-244, 1995.
- [2] Q.-T. Jiang, M.-H. Tsai, and R. H. Havemann, "Line width dependence of copper resistivity," in *Proceedings of IEEE 2001 International Interconnect Technology Conference*, 2001, pp. 227-231.
- [3] J. Tao, N. W. Cheung, and C. Hu, "Electromigration characteristics of copper interconnects," *IEEE Electron Device Letters*, vol. 14, pp. 249-251, 1993.
- [4] L. Peters, "Pursuing the perfect low-k dielectric," *Semicon. Int.*, vol. 21, pp. 64-74, 1998.
- [5] J. Srinivasan, S. V. Adve, P. Bose, and J. A. Rivers, "The impact of technology scaling on lifetime reliability," in *2004 International Conference on Dependable Systems and Networks (DSN'04)*, Florence, Italy, 2004, pp. 177-186.
- [6] M. Tada, Y. Harada, H. Ohtake, *et al.*, "Improvement of TDDB reliability in Cu damascene interconnect by using united hard-mask and Cap (UHC) structure," in *Interconnect Technology Conference, 2003. Proceedings of the IEEE 2003 International*, 2003, pp. 256-258.
- [7] J.-M. Paik, H. Park, and Y.-C. Joo, "Effect of low-k dielectric on stress and stress-induced damage in Cu interconnects " *Microelectron. Eng.*, vol. 71, pp. 348-357, 2004.

-
- [8] V. B. Fiks, "On the Mechanism of the Mobility of Ions in Metals," *Sov. Phys. Solid State* vol. 1, p. 14, 1959.
- [9] H. B. Huntington and A. R. Grone, "CURRENT-INDUCED MARKER MOTION IN GOLD WIRES," *J. Phys. Chem. Solids.* , vol. 20, pp. 76-87, 1961.
- [10] J. R. Black, "Electromigration—A brief survey and some recent results," *IEEE Trans. Electron Devices*, vol. 16, pp. 338-347, 1969.
- [11] J. R. Black, "Physics of Electromigration," in *Proc. Conf. 12th IEEE/IRPS*, Las Vegas, NV, USA, 1974, pp. 142-149.
- [12] J. M. Schoen, "Monte Carlo calculations of structure-induced electromigration failure," *J. Appl. Phys.*, vol. 51, pp. 513-521, 1980.
- [13] J. Vancea, G. Reiss, and H. Hoffmann, "Mean-free-path concept in polycrystalline metals " *Phys. Rev. B*, vol. 35, pp. 6435-6437, 1987.
- [14] M. A. Korhonen, R. D. Black, and C.-Y. Li, "Stress evolution due to electromigration in confined metal lines," *J. Appl. Phys.*, vol. 73, pp. 3790-3799, 1993.
- [15] A. G. Domenicucci, R. G. Filippi, K. W. Choi, *et al.*, "Effect of copper on the microstructure and electromigration lifetime of Ti-AlCu-Ti fine lines in the presence of tungsten diffusion barriers," *J. Appl. Phys.*, vol. 80, pp. 4952-4959 1996.
- [16] M. J. Dion, "Electromigration lifetime enhancement for lines with multiple branches," Piscataway, NJ, USA, 2000, pp. 324-332.

-
- [17] M. A. Korhonen, P. Borgesen, D. D. Brown, and C. Y. Li, "Microstructure based statistical model of electromigration damage in confined line metallizations in the presence of thermally induced stresses," *J. Appl. Phys.*, vol. 74, pp. 4995-5004, 1993.
- [18] Z. Suo, "Reliability of Interconnect Structures," *Interfacial and Nanoscale Failure* vol. 8, pp. 265-324, 2003.
- [19] A. H. Fischer and A. E. Zitzelsberger, "The quantitative assessment of stress-induced voiding in processqualification," in *Proc. Conf. 39th IEEE/IRPS*, Orlando, Florida, 2001, pp. 334-340.
- [20] C. M. Tan and A. Roy, "Investigation of the effect of temperature and stress gradients on accelerated EM test for Cu narrow interconnects " *Thin Solid Films*, vol. 504, pp. 288-293, 2006.
- [21] C. M. Tan, W. Li, K. T. Tan, and F. Low, "Development of highly accelerated electromigration test," *Microelectron. Reliab.*, vol. 46, pp. 1638-1642, 2006.
- [22] C. M. Tan, Y. Hou, and W. Li, "Revisit to the finite element modeling of electromigration for narrow interconnects," *J. Appl. Phys.*, vol. 102, pp. 033705-033712, 2007.
- [23] A. Roy and C. M. Tan, "Experimental investigation on the impact of stress free temperature on the electromigration performance of copper dual damascene submicron interconnect," *Microelectron. Reliab.*, vol. 46, pp. 1652-1656, 2006.
- [24] I. A. Blech and H. Sello, "A study of failure mechanisms in silicon planar epitaxial transistors," *Physics of Failure in Electronics*, vol. 5, pp. 496-505, 1966.

-
- [25] J. Srinivasan, S. V. Adve, P. Bose, and J. A. Rivers, "The Impact of Technology Scaling on Lifetime Reliability," in *2004 International Conference on Dependable Systems and Networks (DSN'04)*, Florence, Italy, 2004, pp. 177-179.
- [26] V. N. Balashov, M. V. Fedkin, and S. N. Lvov, "Experimental system for electrochemical studies of aqueous corrosion at temperatures above 300C," *Journal of the Electrochemical Society*, vol. 156, pp. 209-213, 2009.
- [27] G. O. Davis, J. Kolts, and N. Sridhar, "Polarization Effects in Galvanic Corrosion," *Corrosion*, vol. 42, pp. 329-336, 1986.
- [28] G. D. Giacomo, *Reliability of electronic packages and semiconductor devices*: McGraw-Hill, 1997.
- [29] K. G. Compton, A. Mendizza, and S. M. Arnold, "Filamentary growths on metal surfaces-Whiskers," *Corrosion*, vol. 7, pp. 327-334, 1951.
- [30] S. E. Koonce and S. M. Arnold, "Metal whiskers," *J. Appl. Phys.*, vol. 25, pp. 134-135, 1954.
- [31] J. Liang, N. Dariavach, and D. Shangguan, "Tin whisker nucleation and growth on Sn-Pb eutectic coating layer inside plated through holes with press-fit pins," *IEEE Transactions on Components and Packaging Technologies*, vol. 31, pp. 152-158, 2008.
- [32] O. Fan-Yi, C. Kai, K. N. Tu, and L. Yi-Shao, "Effect of current crowding on whisker growth at the anode in flip chip solder joints," *Appl. Phys. Lett.*, vol. 91, pp. 231919-231921, 2007.

-
- [33] H. Mori, H. Okabayashi, and M. Komatsu, "Electromigration in layered Al lines studied by in-situ ultra-high voltage electron microscopy," *Thin Solid Films*, vol. 300, pp. 25-9, 1997.
- [34] K. Hinode, Y. Homma, and Y. Sasaki, "Whiskers grown on aluminum thin films during heat treatments," *J. Vac. Sci. Technol. A*, vol. 14, pp. 2570-2576, 1996.
- [35] H. Takatsuija, K. Tsujimoto, K. Kuroda, and H. Saka, "Relationship of grain nanostructure and orientation in whisker growth on aluminum thin films on glass substrates," *Thin Solid Films*, vol. 343-344, pp. 41-464, 1999.
- [36] C. A. Pico and T. D. Bonifield, "Thermal hillocks on half-micron aluminum lines: the next reliability issue?," in *1991 Proceedings. Eighth International IEEE VLSI Multilevel Interconnection Conference (Cat. No.91TH0359-0)*, New York, NY, USA, 1991, pp. 256-257.
- [37] E. Iwamura, T. Ohnishi, K. Yoshikawa, and K. Itayama, "In situ scanning electron microscope observation of hillock and whisker growth on Al-Ta alloy films for interconnections of thin film transistor-liquid crystal displays," *Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films)*, vol. 12, pp. 2922-2924, 1994.
- [38] W. J. Boettinger, C. E. Johnson, L. A. Bendersky, *et al.*, "Whisker and Hillock formation on Sn, Sn-Cu and Sn-Pb electrodeposits," *Acta Materialia*, vol. 53, pp. 5033-5050, 2005.
- [39] C. S. Hau-Riege and C. V. Thompson, "Electromigration in Cu interconnects with very different grain structures," *Appl. Phys. Lett.*, vol. 78, pp. 3451-3453, 2001.

-
- [40] C. M. Tan, G. Zhang, and Z. H. Gan, "Dynamic Study of the Physical Process in the Intrinsic Line Electromigration of Deep-Submicron Copper and Aluminum Interconnects " *IEEE Trans. Device Mater. Reliab.*, vol. 4, pp. 450-456, 2004.
- [41] S. P. Murarka, "Materials aspects of copper interconnection technology for semiconductor applications " *Mat. Sci. Technol.* , vol. 17, pp. 749-758, 2001.
- [42] T. Oku, E. Kawakami, M. Uekubo, *et al.*, "Diffusion barrier property of TaN between Si and Cu " *Appl. Surf. Sci.*, vol. 99, pp. 265-272, 1996.
- [43] D.-H. Kim, S.-L. Cho, K.-B. Kim, *et al.*, "Diffusion barrier performance of chemically vapor deposited TiN films prepared using tetrakis-dimethyl-amino titanium in the Cu/TiN/Si structure," *Appl. Phys. Lett.*, vol. 69, pp. 4182-4184, 1996.
- [44] C.-K. Hu and J. M. E. Harper, "Copper Interconnections and Reliability," *Mater. Chem. Phys.*, vol. 52, pp. 5-16, 1998.
- [45] S. P. Hau-Riege, "Probabilistic immortality of Cu damascene interconnects," *J. Appl. Phys.*, vol. 91, pp. 2014-2022, 2002.
- [46] F. Fantini, J. R. Lloyd, I. De Munari, and A. Scorzoni, "Electromigration testing of integrated circuit interconnections," *Microelectronic Engineering*, vol. 40, pp. 207-221, 1998.
- [47] J. R. Lloyd and J. J. Clement, "Electromigration in copper conductors," *Thin Solid Films*, vol. 262, pp. 135-141, 1995.
- [48] I. A. Blech and C. Herring, "Stress generation by electromigration," *Appl. Phys. Lett.* , vol. 29, pp. 131-133 1976.

-
- [49] M. A. Korhonen, T. M. Korhonen, D. D. Brown, and C. Y. Li, "Simulation of electromigration damage in chip level interconnect lines: a grain structure based statistical approach," Piscataway, NJ, USA, 1999, pp. 227-232.
- [50] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *J. Appl. Phys.*, vol. 47, pp. 1203-1208, 1976.
- [51] J. J. Clement and C. V. Thompson, "Modeling electromigration-induced stress evolution in confined metal lines " *J. Appl. Phys.*, vol. 78, pp. 900-904, 1995.
- [52] P. R. Besser, E. Zschech, W. Blum, *et al.*, "Microstructural characterization of inlaid copper interconnect lines," *Journal of Electronic Materials*, vol. 30, pp. 320-330, 2001.
- [53] C.-Y. Li, P. Borgesen, and T. D. Sullivan, "Stress-migration related electromigration damage mechanism in passivated, narrow interconnects," *Appl. Phys. Lett.* , vol. 59, pp. 1464-1466, 1991.
- [54] S. Orain, A. Fuchsmann, V. Fiori, and X. Federspiel, "Reliability issues in Cu/low-k structures regarding the initiation of stress-voiding or crack failure " *Microelectron. Eng.*, vol. 83, pp. 2402-2406, 2006.
- [55] S. H. Rhee, Y. Du, and P. S. Ho, "Thermal stress characteristics of Cu/oxide and Cu/low-k submicron interconnect structures," *J. Appl. Phys.* , vol. 93, pp. 3926-3933, 2003.
- [56] J. W. McPherson and C. F. Dunn, "A model for stress-induced metal notching and voiding in very large-scale-integrated Al-Si (1%) metallization," *J. Vac. Sci. Technol.*, vol. 5, pp. 1321-1325, 1987.

-
- [57] Y. Liu, C. L. Cox, and R. J. Diefendorf, "Finite element analysis of the effects of geometry and microstructure on electromigration in confined metal lines," *J. Appl. Phys.*, vol. 83, pp. 3600-3608, 1998.
- [58] R. W. Lewis, P. Nithiarasu, and K. N. Seetharamu, *Fundamentals of the Finite Element Method for Heat and Fluid Flow*: John Wiley & Sons, Ltd, 2004.
- [59] S. Rzepka, E. Meusel, M. A. Korhonen, and C.-Y. Li, "3-D finite element simulator for migration effects due to various driving forces in interconnect lines," in *Stress-Induced Phenomena in Metallization: Fifth International Workshop*, 1999, pp. 150-161.
- [60] L. Yong, L. Lihua, S. Irving, and T. Luk, "3D modeling of electromigration combined with thermal-mechanical effect for IC device and package," *Microelectronics Reliability*, vol. 48, pp. 811-824, 2008.
- [61] W. Dauksher, W. Dauksher, D. H. Eaton, and J. D. Rowatt, "A Finite-Element-Based Methodology for Evaluating Solder Electromigration Current Limits of Sn/Pb Eutectic Solder Bumps," *IEEE Transactions on Device and Materials Reliability*, vol. 8, pp. 222-228, 2008.
- [62] D. Dalleau, K. Weide-Zaage, and Y. Danto, "Simulation of time depending void formation in copper, aluminum and tungsten plugged via structures," UK, 2003, pp. 1821-1826.
- [63] T. L. Shao, S. W. Liang, T. C. Lin, and C. Chih, "Three-dimensional simulation on current-density distribution in flip-chip solder joints under electric current stressing," *J. Appl. Phys.*, vol. 98, pp. 44509-44511, 2005.

-
- [64] A. Inc., "Theory Reference for ANSYS and ANSYS Workbench " *ANSYS v.11.0 Documentation*, 2007.
- [65] A. Inc., *ANSYS v.11.0 Documentation*, 2007.
- [66] P. S. Ho, I. S. Yeo, C. N. Liao, *et al.*, "Thermal stress and relaxation behaviour of Al(Cu) submicroninterconnects," in *4th International Conference on Solid-State and Integrated Circuit Technology* Beijing, China, 1995, pp. 408-412.
- [67] G. Reimbold, O. Sicardy, L. Arnaud, *et al.*, "Mechanical stress measurements in damascene copper interconnects and influence on electromigration parameters," *IEEE IEDM Technical Digest* pp. 745-748, 2002.
- [68] Y. Hou and C. M. Tan, "Stress-induced voiding study in integrated circuit interconnects," *Semicond. Sci. Technol.* , vol. 23, pp. 075023-075031, 2008.
- [69] Y. K. Lim, Y. K. Lim, R. Arijit, *et al.*, "Stress migration reliability of wide CU interconnects with gouging vias," in *Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International*, 2005, pp. 203-208.
- [70] Y.-L. Shen, "Analysis of Thermal Stresses in Copper Interconnect/Low-k Dielectric Structures," *Journal of Electronic Materials*, vol. 34, pp. 497-505, 2005.
- [71] E. C. C. Yeh, W. J. Choi, K. N. Tu, *et al.*, "Current-crowding-induced electromigration failure in flip chip solder joints," *Appl. Phys. Lett.*, vol. 80, pp. 580-582, 2002.
- [72] C. M. Tan, A. Roy, A. V. Vairagar, *et al.*, "Current crowding effect on copper dual damascene via bottom failure for ULSI applications," *IEEE Trans. Device Mater. Reliab.*, vol. 5, pp. 198-205, 2005.

-
- [73] A. O. Cifuentes and A. Kalbag, "A performance study of tetrahedral and hexahedral elements in 3-D finite element structural analysis," *Finite Elem. Anal. Des.*, vol. 12, pp. 313-318, 1992.
- [74] S. Rzepka, K. Banerjee, E. Meusel, and C. Hu, "Characterization of Self-Heating in Advanced VLSI Interconnect Lines Based on Thermal Finite Element Simulation," *IEEE Trans. Compon. Pack.*, vol. 1998, pp. 406-411, 1998.
- [75] B. Vermeersch and G. De Mey, "Influence of substrate thickness on thermal impedance of microelectronic structures," *Microelectronics Reliability*, vol. 47, pp. 437-443, 2007.
- [76] C.-K. Hu, R. Rosenberg, and K. Y. Lee, "Electromigration path in Cu thin-film lines," *Appl. Phys. Lett.*, vol. 74, pp. 2945-2947, 1999.
- [77] Z. H. Gan, W. Shao, S. G. Mhaisalkar, *et al.*, "Reservoir effect and the role of low current density regions on electromigration lifetimes in copper interconnects," *J. Mater. Res.*, vol. 21, pp. 2241-2245 2006.
- [78] W. Shao, A. V. Vairagar, C. H. Tung, *et al.*, "Electromigration in copper damascene interconnects: reservoir effects and failure analysis " *Surf. Coat. Technol.*, vol. 198, pp. 257-261, 2005.
- [79] A. V. Vairagar, S. G. Mhaisalkar, and A. Krishnamoorthy, "Electromigration behavior of dual-damascene Cu interconnects—Structure, width, and length dependences," *Microelectron. Reliab.*, vol. 44, pp. 747-754, 2004.
- [80] C. Hau-Riege and R. Klein, "The effect of a width transition on the electromigration reliability of Cu interconnects," Piscataway, NJ, USA, 2008, pp. 377-380.

-
- [81] J. W. Pyun, X. Lu, J. Chung, *et al.*, "Effect of barrier thickness on electromigration reliability of Cu/porous low k interconnects," *Appl. Phys. Lett.*, vol. 87, pp. 061907-061909, 2005.
- [82] G. Dongwen, W. Guotao, and P. S. Ho, "Effects of dielectric material and linewidth on thermal stresses of Cu line structures," Piscataway, NJ, USA, 2002, pp. 271-273.
- [83] P. S. Ho, K.-D. Lee, S. Yoon, *et al.*, "Effect of low k dielectrics on electromigration reliability for Cu interconnects " *Mater. Sci. Semicond. Process.*, vol. 7, pp. 157-163, 2004.
- [84] J. R. Lloyd, M. R. Lane, X.-H. Liu, *et al.*, "Reliability challenges with ultra-low k interlevel dielectrics," *Microelectron. Reliab.*, vol. 44, pp. 1835-1841, 2004.
- [85] C. M. Tan and A. Roy, "Electromigration in ULSI interconnects," *Mater. Sci. Eng., Rev.*, vol. 342, 2007.
- [86] J. R. Lloyd, J. Clemens, and S. Snede, "Copper metallization reliability " *Microelectron. Reliab.*, vol. 39, pp. 1595-1602, 1999.
- [87] J. Cho and C. V. Thompson, "Grain size dependence of electromigration-induced failures in narrow interconnects," *Appl. Phys. Lett.*, vol. 54, pp. 2577-2579, 1989.
- [88] R. S. Sorbello, *Mater. Res. Symp. Proc.* , vol. 427, p. 73, 1996.
- [89] A. Roy, R. Kumar, C. M. Tan, *et al.*, "Electromigration in damascene copper interconnects of line width down to 100 nm," *Semicond. Sci. Technol.* , vol. 21, pp. 1369-1372, 2006.

-
- [90] M. J. Attardo and R. Rosenberg, "Electromigration Damage in Aluminum Film Conductors," *J. Appl. Phys.*, vol. 41, pp. 2381-2386, 1970.
- [91] D. Dalleau and K. Weide-Zaage, "Three-Dimensional Voids Simulation in chip Metallization Structures: a Contribution to Reliability Evaluation " *Microelectron. Reliab.*, vol. 41, pp. 1625-1630, 2001.
- [92] Y.-L. Shen, "Void nucleation in metal interconnects: Combined effects of interface flaws and crystallographic slip," *J. Mater. Res.*, vol. 14, pp. 584-591, 1999.
- [93] S. M. Alam, C. L. Gan, C. V. Thompson, and D. E. Troxel, "Reliability computer-aided design tool for full-chip electromigration analysis and comparison with different interconnect metallizations," *Microelectron. Reliab.*, vol. 38, pp. 463-473, 2007.
- [94] Y. Hou and C. M. Tan, "Blech effect in Cu interconencts with oxide and low-k dielectrics," in *14th International Symposium on the Physics and Failure Analysis of Integrated Circuits*, Bangalore, India, 2007, pp. 65-69.
- [95] J. J. Clement, "Electromigration modeling for integrated circuit interconnectreliability analysis," *IEEE Trans. Device Mater. Reliab.*, vol. 1, pp. 33-42, 2001.
- [96] B. D. Knowlton and C. V. Thompson, "Simulation of the temperature and current density scaling of the electromigration-limited reliability of near-bamboo interconnects," *J. Mater. Res.*, vol. 13, pp. 1164-1170, 1998.

-
- [97] C. L. Gan, C. V. Thompson, K. L. Pey, and W. K. Choi, "Experimental characterization and modeling of the reliability of three-terminal dual-damascene Cu interconnect trees," *J. Appl. Phys.*, vol. 94, pp. 1222-1228, 2003.
- [98] K. N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *J. Appl. Phys.*, vol. 94, pp. 5451-5473, 2003.
- [99] Y.-J. Park, V. K. Andleigh, and C. V. Thompson, "Simulations of stress evolution and the current density scaling of electromigration-induced failure times in pure and alloyed interconnects," *J. Appl. Phys.*, vol. 85, pp. 3546-3555, 1999.
- [100] W. Li, C. M. Tan, and Y. Hou, "Dynamic simulation of electromigration in polycrystalline interconnect thin film using combined Monte Carlo algorithm and finite element modeling," *J. Appl. Phys.*, vol. 101, pp. 104314-104320, 2007.
- [101] P. G. Shewmon, "Diffusion in Solids," ed: McGraw-Hill Series in Mat. Sci. and Eng., 1963, p. 189.
- [102] C. G. Shiley, "Steady-state temperature profiles in narrow thin-film conductors," *J. Appl. Phys.*, vol. 57, pp. 777-784, 1985.
- [103] H. Niwa, H. Yagi, H. Tsuchikawa, and K. Masaharu, "Stress distribution in an aluminum interconnect of very large scale integration," *J. Appl. Phys.*, vol. 68, pp. 328-333, 1990.
- [104] E. Kreyszig, *Advanced Engineering Mathematics*, 7th ed. New York: Wiley 1993.
- [105] Q. F. Duan and Y.-L. Shen, "On the prediction of electromigration voiding using stress-based modeling," *J. Appl. Phys.*, vol. 87, pp. 4039-4041, 2000.

-
- [106] E. T. Ogawa, K.-D. Lee, H. Matsuhashi, *et al.*, "Statistics of electromigration early failures in Cu/oxidizedual-damascene interconnects," in *Proc. Conf. 39th IEEE/IRPS*, Orlando, FL, USA, 2001, pp. 341-349.
- [107] A. H. Fischer, A. V. Glasow, S. Penka, and F. Ungar, "Electromigration failure mechanism studies on copper interconnects," in *Interconnect Technology Conference, 2002. Proceedings of the IEEE 2002 International*, 2002, pp. 139-141.
- [108] D. Ang and R. V. Ramanujan, "Hydrostatic stress and hydrostatic stress gradients in passivated copper interconnects " *Mater. Sci. Eng., A*, vol. 423, pp. 157-165, 2006.
- [109] A. V. Vairagar, S. G. Mhaisalkar, M. A. Meyer, *et al.*, "Reservoir effect on electromigration mechanisms in dual-damascene Cu interconnect structures " *Microelectron. Eng.*, vol. 82, pp. 675-679, 2005.
- [110] D. Padhi and G. Dixit, "Effect of electron flow direction on model parameters of electromigration-induced failure of copper interconnects," *J. Appl. Phys.*, vol. 94, pp. 6463-6467, 2003.
- [111] Y.-L. Shen, Y. L. Guo, and C. A. Minor, "Voiding induced stress redistribution and its reliability implications in metal interconnects " *Acta Mater.*, vol. 48, pp. 1667-1678, 2000.
- [112] M. Fujii, K. Koyama, and J. Aoyama, "Reservoir length dependence of EM lifetime for tungsten via chains under low current stress," Santa Clara, CA, USA, 1996, pp. 312-317.

-
- [113] H. A. Le, L. Ting, N. C. Tso, and C. U. Kim, "Analysis of the reservoir length and its effect on electromigration lifetime," *Journal of Materials Research*, vol. 17, pp. 167-171, 2002.
- [114] Y.-B. Park and I.-S. Jeon, "Effects of mechanical stress at no current stressed area on electromigration reliability of multilevel interconnects," *Microelectronic Engineering*, vol. 71, pp. 76-89, 2004.
- [115] R. Arijit, H. Yuejin, and T. Cher Ming, "Electromigration in width transition copper interconnect," *Microelectronics Reliability*, vol. 49, pp. 1086-1089, 2009.
- [116] C. A. Ross, "Stress and Electromigration in Thin Film Metallization," *Mat. Res. Soc. Proc.*, vol. 225, pp. 35-46, 1991.
- [117] Z. H. Gan, W. Shao, S. G. Mhaisalkar, *et al.*, "Experimental and Numerical Studies of Stress Migration in Cu Interconnects Embedded in Different Dielectrics," in *Stress-Induced Phenomena in Metallization: Eighth International Workshop*, 2006, pp. 269-274.
- [118] C. M. Tan and Y. Hou, "Lifetime modeling for stress-induced voiding in integrated circuit interconnections," *Appl. Phys. Lett.*, vol. 91, pp. 061904-061906, 2007.
- [119] "Standard Method for Measuring and Using the temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line," JEDEC SOLID STATE TECHNOLOGY ASSOCIATION JEDEC Standard No. 33B, Dec 2004.

-
- [120] E. T. Ogawa, K.-D. Lee, V. A. Blaschke, and P. S. Ho, "Electromigration reliability issues in dual-damascene Cu interconnections," *IEEE Transactions on Reliability*, vol. 51, pp. 403-419, 2002.
- [121] C. S. Hau-Riege and C. V. Thompson, "The effects of microstructural transitions at width transitions on interconnect reliability," *J. Appl. Phys.*, vol. 87, pp. 8467-8472, 2000.
- [122] A. Roy and C. M. Tan, "Very high current density package level electromigration test for copper interconnects," *J. Appl. Phys.*, vol. 103, pp. 093707-093714, 2008.
- [123] A. Roy and T. Cher Ming, "Probing into the asymmetric nature of electromigration performance of submicron interconnect via structure," *Thin Solid Films*, vol. 515, pp. 3867-3874, 2007.
- [124] J. R. Lloyd, "New models for interconnect failure in advanced IC technology," in *Proceedings of the International Symposium on the Physical and Failure Analysis of Integrated Circuits, IPFA*, Singapore, 2008, pp. 1-7.
- [125] E. T. Ogawa, A. J. Bierwag, K.-D. Lee, *et al.*, "Direct observation of a critical length effect in dual-damascene Cu/oxide interconnects," *Appl. Phys. Lett.*, vol. 78, pp. 2652-2654, 2001.
- [126] S. Thrasher, M. Gall, C. Capasso, *et al.*, "Examination of Critical Length Effect in Copper Interconnects With Oxide and Low-k Dielectrics," in *7th International Workshop, Stress-Induced Phenomenon in Metallization*, Austin, Texas, USA, 2004, pp. 165-172.

-
- [127] R. G. Filippi, P.-C. Wang, R. A. Wachnik, *et al.*, "The electromigration short-length effect in AlCu and Cu interconnects," in *Stress-Induced Phenomena in Metallization: Sixth International Workshop*, 2002, pp. 33-48.
- [128] P.-C. Wang and R. G. Filippi, "Electromigration threshold in copper interconnects," *Appl. Phys. Lett.*, vol. 78, pp. 3598-3600, 2001.
- [129] P.-C. Wang, R. G. Filippi, and L. M. Gignac, "Electromigration threshold in single-damascene copper interconnects with SiO₂ dielectrics," in *Proc. Int. Interconnect Technology Conf.*, Burlingame, CA, USA, 2001, pp. 263-265.
- [130] K.-D. Lee, "Electromigration Critical Length Effect and Early Failures in Cu/oxide and Cu/low k Interconnects," Ph. D, Ph.D Dissertation, University of Texas, Austin, 2003.
- [131] Y.-L. Shen and U. Ramamurty, "Temperature-dependent inelastic response of passivated copper films: Experiments, analyses, and implications," *J. Vac. Sci. Technol.*, vol. 21, pp. 1258-1264, 2003.
- [132] C. S. Hau-Riege, S. P. Hau-Riege, and A. P. Marathe, "The effect of interlevel dielectric on the critical tensile stress to void nucleation for the reliability of Cu interconnects," *J. Appl. Phys.*, vol. 96, pp. 5792-5796, 2004.
- [133] J. Hoekstra, A. P. Sutton, T. N. Todorov, and A. P. Horsfield, "Electromigration of vacancies in copper " *Phys. Rev. B*, vol. 62, pp. 8568-8571, 2000.
- [134] S. P. Hau-Riege and C. V. Thompson, "The effects of the mechanical properties of the confinement material on electromigration in metallic interconnects," *J. Mater. Res.*, vol. 15, pp. 1797-1802 2000.

-
- [135] C. J. Zhai, H. W. Yao, A. P. Marathe, *et al.*, "Simulation and experiments of stress migration for Cu/low-k BEoL," *IEEE Trans. Device Mater. Reliab.*, vol. 4, pp. 523-529, 2004.
- [136] Y. L. Cheng, Y. L. Wang, H. C. Chen, and J. H. Lin, "Effect of inter-level dielectrics on electromigration in damascene copper interconnect " *Thin Solid Films*, vol. 494, pp. 315-319, 2006.
- [137] F. Lacopi, S. H. Brongersma, B. Vandevelde, *et al.*, "Challenges for structural stability of ultra-low-k-based interconnects " *Microelectron. Eng.*, vol. 75, pp. 54-62, 2004.
- [138] Y. L. Shen, "Analysis of Joule heating in multilevel interconnects," *Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures)*, vol. 17, pp. 2115-2121, 1999.
- [139] T.-Y. Chiang, B. Shieh, and K. C. Saraswat, "Impact of joule heating on scaling of deep sub-micron Cu/low-k interconnects," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, Honolulu, HI, United States, 2002, pp. 38-39.
- [140] A. von Glasow, A. H. Fischer, and G. Steinlesberger, "Using the temperature coefficient of the resistance (TCR) as early reliability indicator for stressvoiding risks in Cu interconnects," in *Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International*, 2003, pp. 126-131.
- [141] W. Wu, S. H. Kang, J. S. Yuan, and A. S. Oates, "Thermal effect on electromigration performance for Al/SiO₂, Cu/SiO₂ and Cu/low-K interconnect systems," *Solid-State Electronics*, vol. 45, pp. 59-62, 2001.

-
- [142] D. Ney, X. Federspiel, V. Girault, *et al.*, "Stress-induced electromigration backflow effect in copper interconnects," *IEEE Transactions on Device and Materials Reliability*, vol. 6, pp. 175-180, 2006.
- [143] A. Sauter Mack and P. Flinn, "Effect of intrinsic passivation stress on stress in encapsulated interconnect lines," in *Materials Research Society Symposium - Proceedings*, Boston, MA, USA, 1995, pp. 465-470.
- [144] I.-S. Yeo and P. S. Ho, "Stress relaxation and microstructural change in passivated Al(Cu) lines," in *34th Annual Proceedings of Reliability Physics Symposium*, Dallas, 1996, pp. 131-138.
- [145] C. J. Zhai and R. C. Blish, "A physically based lifetime model for stress-induced voiding in interconnects," *J. Appl. Phys.*, vol. 97, pp. 113503-113508, 2005.
- [146] C. W. Chang, C. V. Thompson, C. L. Gan, *et al.*, "Effects of microvoids on the linewidth dependence of electromigration failure of dual-damascene copper interconnects," *Appl. Phys. Lett.*, vol. 90, pp. 193505-193507, 2007.
- [147] M. D. Thouless, K. P. Rodbell, and C. Cabral, "Effect of a surface layer on the stress relaxation of thin films," *J. Vac. Sci. Technol.*, vol. 14, pp. 2454-2461, 1996.
- [148] R.-M. Keller, S. P. Baker, and E. Arzt, "Quantitative analysis of strengthening mechanisms in thin Cu films: Effects of film thickness, grain size and passivation," *J. Mater. Res.*, vol. 13, pp. 1307-1317, 1998.
- [149] E. T. Ogawa, J. W. McPherson, J. A. Rosal, *et al.*, "Stress-induced voiding under vias connected to wide Cu metal leads," in *Proc. Conf. 40th IEEE/IRPS*, Dallas, Texas, 2002, pp. 312-331.
- [150] J. 139, *JEDEC Solid State Technology Association* December, 2000.

-
- [151] C. Kettel, *Introduction to Solid State Physics*: Wiley, Hoboken, New York 2005.
- [152] Z. Suo, *Elsevier Amsterdam*, vol. 8, p. 265, 2003.
- [153] P. A. Flinn, "Mechanical stress in VLSI interconnections: origins, effects, measurement, and modeling " *Mater. Res. Bull.* , vol. 20, pp. 70-73, 1995.
- [154] L. T. Shi and K. N. Tu, "Finite-element modeling of stress distribution and migration in interconnecting studs of a three-dimensional multilevel device structure," *Appl. Phys. Lett.*, vol. 65, pp. 1516-1518, 1994.
- [155] B. C. Valek, J. C. Bravman, N. Tamura, *et al.*, "Electromigration-induced plastic deformation in passivated metal lines," *Appl. Phys. Lett.*, vol. 81, pp. 4168-4170, 2002.
- [156] M. Kato, H. Niwa, H. Yagi, and H. Tsuchikawa, "Diffusional relaxation and void growth in an aluminum interconnect of very large scale integration," *J. Appl. Phys.*, vol. 68, pp. 334-338, 1990.
- [157] J. H. An and P. J. Ferreira, "In situ transmission electron microscopy observations of 1.8 μm and 180 nm Cu interconnects under thermal stresses," *Appl. Phys. Lett.* , vol. 89, pp. 151919-151921, 2006.
- [158] J. K. Mauro, C. V. Thompson, and E. G. Mihal, "Diffusional creep in damascene Cu lines," *J. Appl. Phys.*, vol. 89, pp. 91-98, 2001.
- [159] W. Shao, S. G. Mhaisalkar, T. Sritharan, *et al.*, "Direct evidence of Cu/cap/liner edge being the dominant electromigration path in dual damascene Cu interconnects," *Appl. Phys. Lett.*, vol. 90, pp. 052106-052108, 2007.

-
- [160] R. L. Guldi, J. B. Shaw, J. Ritchison, *et al.*, "Characterization of copper voids in dual damascene processes," in *Advanced Semiconductor Manufacturing 2002 IEEE/SEMI Conference and Workshop*, 2002, pp. 351-355.
- [161] M. Hommel, A. H. Fischer, A. V. Glasow, and A. E. Zitzelsberger, "Stress-induced voiding in aluminum and copper interconnects," in *Stress-Induced Phenomena in Metallization: Sixth International Workshop* vol. 612, S. P. Baker, *et al.*, Eds., ed: AIP, New York, 2002, pp. 157-168.
- [162] M. Hommel, A. H. Fischer, A. V. Glasow, and A. E. Zitzelsberger, in *Stress-Induced Phenomena in Metallization: Sixth International Workshop*, 2001, pp. 157-168.
- [163] J. R. Lloyd, M. W. Lane, E. G. Liniger, *et al.*, "Electromigration and adhesion," *IEEE Trans. Device Mater. Reliab.*, vol. 5, pp. 113-118, 2005.
- [164] C. Bruynseraede, Z. Tokei, F. Iacopi, *et al.*, "The impact of scaling on electromigration reliability " in *Proc. Conf. 43rd IEEE/IRPS*, 2005, pp. 7-17.
- [165] Y. L. Lim, K. L. Pey, P. S. Lee, *et al.*, "Design for Manufacturability and its Role in Enhancing Stress Migration Reliability of Porous Ultra Low-k Copper Interconnects," in *Proc. Conf. 45th IEEE/IRPS*, Phoenix, Arizona, 2007, pp. 134-140.
- [166] J.-M. Paik, I.-M. Park, Y.-C. Joo, and K.-C. Park, "Linewidth dependence of grain structure and stress in damascene Cu lines " *J. Appl. Phys.*, vol. 99, pp. 024509-024514, 2006.

-
- [167] C. J. Zhai, H. Y. Yao, P. R. Besser, *et al.*, "Stress modeling of Cu/low-k BEoL - Application to stress migration," in *Proc. Conf. 42rd IEEE/IRPS*, 2004, pp. 234-239.
- [168] Y.-L. Shen, "Thermo-Mechanical stresses in copper interconnects-A modeling analysis " *Microelectron. Eng.*, vol. 83, pp. 446-459, 2006.
- [169] T. C. Wang, T. E. Hsieh, M.-T. Wang, *et al.*, "Stress migration and electromigration improvement for copper dual damascene interconnection," *Journal of the Electrochemical Society*, vol. 152, pp. 45-49, 2005.
- [170] G. Alers, "Back end reliability," S. Lake Tahoe, CA, United States, 2005, p. 144.
- [171] R. C. J. Wang, C. C. Lee, L. D. Chen, *et al.*, "A study of Cu/Low-k stress-induced voiding at via bottom and its microstructure effect," *Microelectronics Reliability*, vol. 46, pp. 1673-1678, 2006.
- [172] Z. Gan, W. Shao, S. G. Mhaisalkar, *et al.*, "The influence of temperature and dielectric materials on stress induced voiding in Cu dual damascene interconnects," *Thin Solid Films*, vol. 504, pp. 161-165, 2006.
- [173] J.-M. Paik, H. Park, Y.-C. Joo, and K.-C. Park, "Effect of dielectric materials on stress-induced damage modes in damascene Cu lines," *J. Appl. Phys.*, vol. 97, pp. 104513-104519, 2005.
- [174] K. Ishikawa, T. Iwasaki, T. Fujii, *et al.*, "Impact of metal deposition process upon reliability of dual-damascene copper interconnects," Burlingame, CA, USA, 2003, pp. 24-26.

-
- [175] W. Tong Hong and L. Yi-Shao, "Submodeling analysis for path-dependent thermomechanical problems," *Transactions of the ASME. Journal of Electronic Packaging*, vol. 127, pp. 135-140, 2005.
- [176] K. Do-Seop, Y. Qiang, T. Shibutani, *et al.*, "Effect of void formation on thermal fatigue reliability of lead-free solder joints," Las Vegas, NV, USA, 2004, pp. 325-329.
- [177] M. Aoyagi, "Analysis of atomic diffusion mechanism of interconnect voiding failure caused by stress-induced migration," *J. Vac. Sci. Technol.*, vol. 24, pp. 1254-1258, 2005.
- [178] I. T. R. f. Semiconductors, <http://www.itrs.net/reports.html>, 2007.
- [179] M. C. Hsieh, H. Yung-Yu, and C. Chao-Liang, "Thermal stress analysis of Cu/low-k interconnects in 3D-IC structures," Piscataway, NJ, USA, 2006, pp. 25-28.
- [180] K. Dae-Yong and S. S. Wong, "Mechanism for early failure in Cu dual damascene structure," Piscataway, NJ, USA, 2003, pp. 265-267.
- [181] M. Fayolle, G. Passemard, M. Assous, *et al.*, "Integration of copper with an organic low-k dielectric in 0.12- μ m node interconnect," Netherlands, 2002, pp. 119-124.
- [182] T. Oshima, K. Hinode, H. Yamaguchi, *et al.*, "Suppression of stress-induced voiding in copper interconnects," Piscataway, NJ, USA, 2002, pp. 757-760.
- [183] J. Young-Chang, P. Jong-Min, and P. Il-Mok, "Effect of grain growth stress and stress gradient on stress-induced voiding in damascene Cu/low-k interconnects for ULSI," *Thin Solid Films*, vol. 504, pp. 284-287, 2006.

-
- [184] T. Tonegawa, M. Hiroi, K. Motoyama, *et al.*, "Suppression of bimodal stress-induced voiding using high-diffusive dopant from Cu-alloy seed layer," Piscataway, NJ, USA, 2003, pp. 216-218.
- [185] P. Gudmundson and A. Wikstrom, "Stresses in thin films and interconnect lines," Netherlands, 2002, pp. 17-29.
- [186] P. M. Igic and P. A. Mawby, "An advanced finite element strategy for thermal stress field investigation in aluminium interconnections during processing of very large scale integration multilevel structures," *Microelectronics Journal*, vol. 30, pp. 1207-1212, 1999.
- [187] S. Park, S. A. B. Allen, and P. A. Kohl, "Air-Gaps for high-performance on-chip interconnect part ii: Modeling, fabrication, and characterization," *Journal of Electronic Materials*, vol. 37, pp. 1534-1546, 2008.
- [188] W. Shao, Z. H. Gan, S. G. Mhaisalkar, *et al.*, "The effect of line width on stress-induced voiding in Cu dual damascene interconnects," *Thin Solid Films*, vol. 504, pp. 298-301, 2006.
- [189] R. G. Filippi, J. F. McGrath, T. M. Shaw, *et al.*, "Thermal cycle reliability of stacked via structures with copper metallization and an organic low-k dielectric," Piscataway, NJ, USA, 2004, pp. 61-67.
- [190] K. Weide-Zaage, D. Dalleau, and X. Yu, "Static and dynamic analysis of failure locations and void formation in interconnects due to various migration mechanisms," *Materials Science in Semiconductor Processing*, vol. 6, pp. 85-92, 2003.

-
- [191] N. L. Michael, C. Kim, P. Gillespie, and R. Augur, "Electromigration failure in ultra-fine copper interconnects " *J. Electron. Mater.*, vol. 32, pp. 988-993, 2003.
- [192] G. Schindler, S. Penka, G. Steinlesberger, *et al.*, "Reliability studies of narrow Cu lines " *Microelectron. Eng.*, vol. 82, pp. 645-649, 2005.
- [193] P. Sharma, S. Ganti, H. Ardebili, and A. Alizadeh, "On the scaling of thermal stresses in passivated nanointerconnects," *J. Appl. Phys.*, vol. 95, pp. 2763-2769, 2004.
- [194] I. T. R. f. Semiconductors, <http://www.itrs.net/reports.html>, 2006.
- [195] D. J. Pierce and P. J. Brusius, "Electromigration : A review," *Microelectron. Reliab.*, vol. 37, pp. 1053-1072, 1997.
- [196] B. Li, C. Christiansen, J. Gill, *et al.*, "Threshold electromigration failure time and its statistics for Cu interconnects," *J. Appl. Phys.*, vol. 100, p. 114516, 2006.
- [197] C. M. Tan, N. Raghavan, and A. Roy, "Application of Gamma Distribution in Electromigration for Submicron Interconnects " *J. Appl. Phys.*, vol. 102, pp. 103703-103709, 2007.
- [198] Y. Du, G. Wang, C. Merrill, and P. S. Ho, "Thermal Stress and Debonding in Cu/low-k Damascene Line Structures," in *52rd Electronic Components and Technology Conference 2002*, pp. 859-864.