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TOPOLOGICAL DESIGN AND CONTROL OF BUCK- BOOST MULTILEVEL INVERTERS

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Summary

Most dc-ac inverters developed to date can support only voltage buck energy conversion, and are therefore not suitable for use as interfacing inverters for tapping energy from renewable sources or other alternative clean sources like fuel cells, where an unrestrained voltage variation range is unavoidable. That obviously spells out the need to design inverters with both voltage buck and boost conversion abilities in order to gain maximum flexibility. Indeed, to cater for this rapidly growing interest in renewable / clean sources and other modern applications that require voltage buck-boost conversion, a number of buck-boost topological solutions have since been reported in the literatures with the most basic configuration being the series connection of a boost dc-dc converter at the front-end of a dc-ac voltage buck inverter. Although theoretically feasible, such a cascaded connection of two electronic converters is generally not attractive since it gives rise to a costly two-stage solution, which lacks optimization, and is also harder to control.

Other solutions involving only a single-stage inverter have also been reported with most researchers trying to integrate semiconductor switches in a two-stage inverter to give a more compact single-stage topological alternative. Another possibility that has recently been reported is the integration of a Z-source LC impedance network between the dc input source and dc-ac inverter circuitry, where the complementary inductive and capacitive properties are known to give the Z-source inverter many advantages that are not exhibited by conventional inverters. Despite their effectiveness in performing voltage buck-boost conversion, nearly all the buck-boost inverters proposed to date are of the two-level type, meaning that their output pole voltages can switch only between two discrete voltage levels. Deduced from past development trends of conventional inverters, it is anticipated that the next topic of interest is likely to be the development of buck-boost multilevel inverters that supposedly should have a

lower electromagnetic interference (EMI) emission and a better output waveform quality. With this anticipation in view, the theme of investigation chosen for this project is firmly fixed on the topological design and control of buck-boost multilevel inverters.

As a start, various three-level buck-boost inverters are designed based either on the Z-source or traditional $\dot{C}uk$ / SEPIC energy conversion concepts. For the former, the Z-source neutral-point-clamped (NPC) inverter, Z-source dc-link-cascaded (DCLC) inverter and Z-source dual inverter are proposed, and can be controlled using newly proposed modulation schemes that produce unique shoot-through states in addition to those traditional active and null states. For reducing the cost of the inverters, different cost saving modulation methods are also investigated with some of the designed schemes allowing the Z-source NPC and DCLC inverters to be implemented using only a single passive LC impedance network instead of two. Other schemes proposed offer the advantage of reducing the number of required dc sources to one for the Z-source dual inverter, and reducing the inverter generated common-mode voltage to zero for all the presented Z-source inverters.

Without being limited to only three-level Z-source inverter circuitries, the findings presented in the thesis can equally be applied to develop other three-level buck-boost inverters. To be more specific, three-level $\dot{C}uk$ / SEPIC buck-boost inverters are derived, and found to function equally well in terms of producing the desired voltage gain when the same modulation schemes are used for controlling them. Comparing with their three-level Z-source counterparts, the $\dot{C}uk$ / SEPIC-derived buck-boost inverters require an additional switch for dc inductive boosting and careful state sequencing for preventing capacitive short-circuiting. Although sounding more complex, the $\dot{C}uk$ / SEPIC-derived inverters might still appear to be better options since they use lesser passive components at the expense of experiencing a higher voltage stress, and might eventually be less costly options for certain applications.

Where possible, extension of the presented three-level buck-boost concepts to five-level inverters is also investigated, but unlike traditional dc-ac inverters, where higher level inverters can be extended easily, extending of three-level buck-boost inverters to their five-level variants is not that straightforward and not always possible. Indeed, after some careful thought, the only five-level topological option verified to be both economically and theoretically feasible is the five-level Z-source diode-clamped inverter configured with two X-shaped LC impedance networks. Again, modulation schemes for controlling it with the newly identified partial shoot-through states embedded are proposed, and can be proven to exhibit matching performance as for a traditional diode-clamped inverter.

Adding on to the investigative studies is the practically relevant topic of fault ride-through, which is especially important for multilevel inverters, where many switches are used. For that, the earlier presented topological options are reviewed with a few identified as interesting topologies that can ride through most fault scenarios smoothly as long as the newly proposed ride-through modulation schemes are used for controlling them. Last but not least, the investigation ends with a brief consideration on how to extend the presented buck-boost conversion concepts to ac-dc-ac converters. Of course, the simplest approach is to cascade either one or more diode rectifiers to the inverter front-end with no other modification made to the circuits, but that undoubtedly includes more components than are really needed. Therefore, instead of simply cascading converters, the objective set for this investigation is to seek a topologically challenging approach that can be used for implementing the ac-dc-ac converters with the least number of components needed. This, together with the rest of the presented buck-boost inverters, is tested thoroughly in simulation using either PSIM or PLECS, and experimentally using a number of constructed laboratory prototypes.

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List of Abbreviations

APOD	Alternative Phase Opposition Disposition
CCM	Continuous Conduction Mode
CSI	Current Source Inverter
DCLC	DC-Link-Cascaded
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
E-active	Equivalent Active
E-null	Equivalent Null
EMI	Electromagnetic Interference
EPLD	Erasable Programmable Logic Device
FDCL	Full DC-Link
IGBT	Insulated Gate Bipolar Transistor
NPC	Neutral-Point-Clamped
NTV	Nearest-Three-Vector
PD	Phase Disposition
PDCL	Partial DC-Link
PSCPWM	Phase-Shifted Carrier Pulse-Width Modulation
PV	Photovoltaic
PWM	Pulse-Width Modulation
RCM	Reduced Common-Mode
REC	Reduced Element Count
SPWM	Sinusoidal Pulse-Width Modulation
SVPWM	Space Vector Pulse-Width Modulation
VSI	Voltage Source Inverter
ZLV	Zero Line Voltage

List of Symbols

B	Boost factor of Z-source inverter
C	Capacitor
$\cos \phi$	Power factor
D	Diode
DX ($X = A, B$ or C)	Clamping diode
i_C	Capacitor current
i_{dc}	DC input current
i_L	Inductor current
i_{in}	DC-link current
I_o	Peak ac output current
k	Duty ratio of SW
L	Inductor
M	Modulation index
N	Neutral point
SW	DC side switch
SX ($X = A, B$ or C)	Switch in the inverter circuitry
SX' ($X = A, B$ or C)	Counterpart of SW
S_x ($x = a, b$ or c)	Switching function of inverter
T	Switching period
T_0	Shoot-through interval
T_0'	Common duration set for both upper and lower-shoot-through states
T_1	Non-shoot-through interval
V_C	Capacitor voltage
V_{cm}	Common-mode voltage
V_d	Negative linear reference in the Ćuk/SEPIC-derived

	buck-boost inverters
V_{dc}	DC input voltage
V_i	DC-link voltage in the Z-source inverters
$\hat{v}_i$	Peak dc-link voltage in the Z-source inverters
V_{lin}	Linear reference in the Z-source dual inverters
V_{In}	Inherent dc voltage produced by the front-end rectifier
v_L	Inductor voltage
$V_{\max}$	The sinusoidal reference with maximum value
V_{mid}	The sinusoidal reference with middle value
$V_{\min}$	The sinusoidal reference with minimal value
V_{off}	Triplen harmonic offset
V_S	Line rms voltage
V_{star}	Star point voltage
V_u	Positive linear reference in the Ćuk/SEPIC-derived buck-boost inverters
$V_{(-ve)}$	Negative dc-rail potential
$V_{(+ve)}$	Positive dc-rail potential
V_x ($x = a, b$ or c)	Modulation reference
$\hat{v}_x$	Peak ac output voltage in the Z-source inverters
V_{XN} ($X = A, B$ or C)	Normalized inverter phase voltage
θ	Rotating angle of reference phasor

Chapter 1 Introduction

1.1 Background and Motivation

To date, the applications of renewable and other clean energy sources like wind energy, solar energy and fuel cells in place of traditional fossil fuels have been growing rapidly, mainly in distributed energy systems, electric vehicles and many others that can help to protect the environment and maintain continuous sustainability. To cater for this growing interest in clean energy, the design of power converters must gradually be revised to strictly meet the specified load requirements regardless of how the clean sources vary in terms of their harnessed capacity.

Particularly in the case of dc-ac solar energy inversion, the implemented inverter must process the harnessed dc solar power to conditioned ac power for energizing the connected loads at the demanded fundamental frequency, amplitude and phase angle in either a single or three-phase configuration. Although it sounds straightforward, this energy conditioning process is relatively complex due to the continuous output variation of the photovoltaic (PV) panels, which heavily depends on the ambient conditions (temperature and irradiation). Because of this unpredictability, a recommended method for sizing the inverter is to have its most efficient operating point (at modulation depth of unity) firmly fixed on the nominal PV output characteristics, and allowing it to vary upwards or downwards as the PV output varies. That directly infers that the inverter must have some flexibility of performing buck-boost energy conversion, which unfortunately cannot be supported by traditional voltage or current source inverter, whose ac output amplitude is always lower or higher than its input dc voltage.

To overcome these inflexible drawbacks, a boost dc-dc converter is usually inserted

between the input source and voltage source inverter circuitry chosen as an example to stabilize the intermediate dc-link voltage of the resulting two-stage power converter, regardless of how the input fluctuates. Although functioning well, this cascading of converters lacks integration, which might cause the resulting two-stage power converter to use more components than necessary, and hence incurring a higher system cost. Therefore, instead of adapting to the two-stage simplicity in terms of concepts, a number of alternative single-stage solutions have been proposed, where integration of functionalities is implicitly embedded to reduce the number of system components needed.

Among the single-stage solutions proposed, the Z-source voltage-type inverter [1, 2] is viewed as one of the most interesting with an X-shaped impedance network connected between its dc source and inverter circuitry. This X-shaped network allows any of the inverter phase-legs to be shorted without damaging active switches, and in fact, is the phenomenon that gives the Z-source inverter its added voltage-boosting ability. Supplementing the Z-source inverter, other single-stage buck-boost inverters derived in [3] using the Ćuk and SEPIC energy conversion concepts can also be used with only slight control parameter variation needed for producing the same input-to-output voltage gain.

Although functioning well, the above-described inverter topologies are all based on two-level discrete switching, which might not be suitable for applications, where a better output waveform quality is needed. Motivated to address this concern which might likely affect future design of renewable energy harnessing systems, the main theme of investigation set for the project is strictly tuned towards the design of various multilevel buck-boost topological and modulation variants. Other related concerns like their ride-through ability and ac-dc-ac extension are also explored for comprehensiveness.

1.2 Major Contributions of the Thesis

Throughout the course of development of this research project, a number of theoretical contributions have been reported, and are respectively summarized as follows.

- *Present the careful integration of a newly proposed Z-source topological concept to the basic neutral-point-clamped inverter topology for designing a three-level inverter with both voltage-buck and -boost capabilities:* The designed inverter uses two unique X-shaped LC impedance networks connected between two isolated dc input power sources and its inverter circuitry for boosting its ac output voltage. Through the design of an appropriate pulse-width modulation algorithm, the two impedance networks can be shorted sequentially for voltage-boosting with minimized harmonic distortion and device commutations per half carrier cycle attained. With only a slight modification to the inverter pulse-width modulation (PWM) algorithm, the designed NPC inverter can also be operated with completely eliminated common-mode voltage.
- *Propose an alternative three-level Z-source topological and control combination that can produce optimal output waveform quality, while using lesser passive LC elements:* Through detailed operational analysis, new operating modes of the “reduced element count” (REC) Z-source inverters are identified, which when inserted appropriately to the inverter state sequence, will always produce the desired voltage transfer gain with minimized commutation count and optimized three-level switching.
- *Design a three-level Z-source dual inverter that can be powered by either a single dc source or two isolated dc sources:* At the ac output of the designed inverter, three-phase transformer is connected to allow the inverter to power all generic delta- or wye-connected loads with either three-wire or four-wire

configuration. Modulation wise, the designed inverter can be controlled using either the “Nearest Three Vectors” (NTV) or reduced common-mode (RCM) switching scheme, where the former offers better waveform quality, while the latter generates a zero common-mode voltage. An alternative phase-shift-carrier scheme is also proposed that would allow the inverter to function with only a single dc source instead of the more costly option of using two isolated sources.

- *Develop a three-level Z-source dc-link-cascaded inverter and its associated modulation schemes:* This inverter functions based on nearly the same operating principles as the Z-source NPC and dual inverters described above. It is studied here simply because it serves as an alternative with its own advantages that might suit a particular application.
- *Propose a five-level Z-source diode-clamped inverter with two Z-source networks functioning as intermediate energy storages coupled between dc sources and diode-clamped inverter circuitry:* Analyzing the operational principles of two Z-source networks with partial dc-link shoot-through states inserted reveals hidden theories in the five-level Z-source diode-clamped inverter. These theories are different from those found in two-level Z-source inverter, and are in fact the foundation that gives the five-level Z-source inverter its excellent waveform quality when operating in either voltage-buck or boost mode.
- *Propose various compensation methods for three-level Z-source inverters under semiconductor failure conditions:* Unlike the traditional fault tolerant techniques in three-level inverter by using either an additional phase-leg or collective switching states, the proposed methods simply reconfigure the gating signals in order to tolerate the failed semiconductor devices without significantly decreasing the ac output quality and amplitude by properly using the inherent boost characteristic of Z-source network. In addition, the Z-source

dual inverters can maintain the zero common-mode voltage under semiconductor failure conditions, which is the unique characteristic attained by the dual inverters only.

- *Present the design of a buck-boost three-level dual inverter supplied by a single dc source:* The proposed inverter is implemented by cascading two three-phase voltage-source bridges at their ac outputs with only an additional switch added to their common dc network for inductive energy boosting. The designed inverter can be controlled using a carefully formulated modulation scheme, which ensures the proper sequencing and placement of three distinct states in a switching cycle, while at the same time, avoids any short-circuiting of capacitive elements.
- *Propose new buck-boost three-level inverters implemented by integrating the neutral-point-clamped or dc-link-cascaded topology with the Ćuk- or SEPIC-derived front-end circuitry:* For minimizing the component count, only one voltage boost circuitry is assumed to regulate the dc-link voltage with the designed APOD modulation adopted. By separately controlling the switching signals of upper full-bridge in the dc-link cascaded inverter, the voltage boost circuitry can be simplified with single dc side switch, which significantly reduces whole system cost and switching losses.
- *Propose a new series of diode-assisted buck-boost inverters:* Using the unique diode-capacitor network inserted between voltage boost circuitry and simple two-level inverter circuitry, the voltage boost capability can be significantly enhanced.
- *Propose a new ac-dc-ac Z-source converter:* Extending the Z-source concepts from dc-ac to ac-dc-ac conversion, a three-level ac-dc-ac Z-source converter

with reduced component count is designed for riding through voltage sag or surge in the grid.

1.3 Organization of the Thesis

The thesis is organized into ten chapters with the main aim being to neatly present the theoretical findings in a streamlined manner. A brief description of each chapter is now provided to give an overview of the thesis before proceeding on to analyze the details in each of the individual chapters.

First of all, Chapter 1 introduces the background and motivation of this project, before describing the theoretical contributions discovered in the project. The organization of the thesis is also elaborated to give some insights on what to expect in each of the individual chapters.

Proceeding on, Chapters 2 and 3 review existing multilevel topological and modulation issues, and relevant buck-boost energy conversion concepts needed for developing various multilevel buck-boost inverters proposed from Chapter 4 onwards. To be more precise, Chapter 4 presents topological and modulation development of a three-level Z-source NPC inverter implemented with either two or one LC impedance network.

The same Z-source analysis is then performed in Chapter 5 to design the dc-link cascaded and dual inverters with the latter demonstrated to have the flexibility of including either a single or two sets of dc sources and impedance networks. Instead of solely relying on the Z-source energy conversion concept, the development of three-level buck-boost inverters using the Ćuk and SEPIC voltage boosting concepts is also explored and presented in Chapter 6, which then completes the development process for three-level buck-boost inverters.

Beginning with the next higher level inverters, Chapter 7 re-evaluates all buck-boost

Chapter 1 Introduction

energy conversion concepts, and eventually proposed a five-level Z-source diode-clamped inverter. This five-level inverter is viewed as the highest level variant that can be designed without degrading the inverter output waveform quality, while at the same time, using the minimum number of passive components for implementation.

Although proven to function well without any serious limitation on their performance, chances of the presented inverters failing to operate correctly are high because of their high semiconductor device count. To allow the inverters to ride-through semiconductor failure smoothly, their topological redundancies are reviewed with the few suitable variants with ride-through ability noted in Chapter 8. Modulation schemes for controlling these chosen variants are also discussed in Chapter 8, before moving forward to the last task planned for this project in Chapter 9, where a cost saving method for implementing ac-dc-ac buck-boost conversion is discussed.

Last but not least, Chapter 10 concludes the thesis, and recommends a number of possible future research areas that can be explored in the near coming future.

Chapter 2 Traditional Multilevel Inverter Topologies and Modulation Schemes

Inverters are widely used in the industry for performing dc to ac power conversion in adjustable speed motor drives, electric power interfaces and uninterruptible power supplies [6-17]. Traditionally, these applications use a two-level inverter, but as the power and switching ranges increase, the two-level topology is increasingly viewed as inappropriate, restricted mainly by the present semiconductor manufacturing technology with no immediate solution in view. Therefore, instead of waiting for a semiconductor fabricating breakthrough, a more effective and immediate approach for resolving the imposed restrictions is to adopt multilevel inverters [18-30], whose advantages for high power applications are well recognized and include increased power rating, improved harmonic performance, reduced EMI emission and a larger pool of discrete voltage levels for synthesizing the output voltage waveform [31-47].

Indeed, a good review summarizing all existing multilevel topologies would comprehend the thesis nicely, but realistically, an exhaustive comprehension is not possible given the large pool of existing knowledge covering all aspects of multilevel topological and control variants. Therefore, instead of aiming for completeness, this chapter would document only those multilevel topologies and modulation schemes that are more popularly adopted for application or research. Specific examples include the diode-clamped inverter, cascaded inverter, flying capacitor inverter and dual inverter, whose operating principles would help readers understand better those theoretical developments proposed for buck-boost multilevel inverters discussed in later chapters.

2.1 Diode-Clamped Inverter

Diode-clamped inverter is implemented by connecting multiple switches in series, and

Fig. 2-1. Topologies of (a) three-level and (b) five-level diode-clamped inverters.

using clamping diodes to distribute the dc-link voltage stress evenly among the switches per phase-leg [48-51]. For illustration, example three-level and five-level diode-clamped inverters are shown in Fig. 2-1(a) and (b) respectively, where the former is also referred to as neutral-point-clamped (NPC) inverter. In the illustrated circuits, the dc-link voltage is divided into three or five levels by the series-connected capacitors, C_1 and C_2 or C_1, C_2, C_3 and C_4 , respectively.

For tying to each of the distinct voltage levels, certain switch combinations must be assumed by the active switches with a list of possible combinations given in Table 2-1 for the case of a five-level diode-clamped inverter. In addition to that, a further point to

Table 2-1. Switching states of five-level diode-clamped inverter ($X = A, B$ or C).

ON Switches	Voltage
$X1, X2, X3, X4$	$V_{dc}/2$
$X2, X3, X4, X1'$	$V_{dc}/4$
$X3, X4, X1', X2'$	0
$X4, X1', X2', X3'$	$-V_{dc}/4$
$X1', X2', X3', X4'$	$-V_{dc}/2$

note is that the switches in the inverter are grouped in pairs (for example SA1 and SA'1) with the two switches in a pair being commanded in complement and with dead time inserted for protecting the inverter against large short-circuit current.

Although the diode-clamped inverter (particularly the three-level NPC inverter) has so far found many applications in the industry, it nonetheless is known to suffer from dc-link capacitor voltage imbalance, which in turn can cause low-order harmonic distortion of ac output and increased voltage stress across the capacitors and semiconductor switches [52-58]. To overcome these problems, a number of capacitive voltage or neutral point balancing techniques has since been reported with some requiring extra hardware and others operated with constant swooping of redundant states. These techniques are not reviewed here since they are not relevant to the dc-ac buck-boost inversion concepts proposed in the thesis.

Fig. 2-2. Topology of cascaded five-level inverter.

2.2 Cascaded Inverter

Cascaded multilevel inverter is implemented by connecting multiple single-phase power bridges, also referred to as H-bridges, in series [59-62]. A typical cascaded five-level inverter is illustrated in Fig. 2-2, where each H-bridge is powered by a separate dc source. Since each H-bridge generates three distinct voltage levels defined as $+V_{dc}$, 0 and $-V_{dc}$, the cascading of two power bridges in series for a phase can produce five distinct voltage levels labeled as $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$, respectively.

Although the cascaded inverter offers many inherent advantages to the users, its requirement for multiple isolated dc sources makes it an expensive topology used only for inverters with higher than five distinct voltage levels. This limitation is however slowly diluted away with the introduction of renewable sources, where multiple source units are now readily available. Upon solving the source limitation, the modular structure of the cascaded inverter will again appear as an attractive feature since it allows easier inverter construction and more streamlined manufacturing process.

2.3 Flying Capacitor Inverter

Besides diode-clamped and cascaded inverter, another popular multilevel topology

Fig. 2-3. Topology of three-level flying capacitor inverter.

attracting research interests is the flying capacitor inverter [63-69], whose single phase three-level topology is shown in Fig. 2-3. With the isolated capacitor C_1 regulated to half the dc-link voltage, the inverter can produce three distinct output voltage levels labeled as $V_{dc}/2$, 0 and $-V_{dc}/2$. Supposing that the voltage rating of the capacitors used are the same as that of the active semiconductor switches, a n -level inverter would then require a total of $(n - 1) \times (n - 2)/2$ clamping capacitors per phase-leg in addition to $(n - 1)$ dc-link capacitors. That obviously represents a drawback for the flying capacitor inverter since the number of capacitors needed and the system size increase tremendously as the number of output voltage levels increases. Despite the increase in capacitor number, no operating constraint is however expected to surface since with the appropriate modulation scheme imposed, the flying capacitor inverter can achieve natural voltage balancing of the capacitors, hence allowing higher level inverters to be implemented easily.

2.4 Dual Inverter

The connection of two traditional voltage-source inverters to form a three-level

Fig. 2-4. Schematics of dual inverter supplying motors with (a) open-end-windings and (b) two stator windings per phase.

inverter has previously been reported for use in either open-end-winding (see Fig. 2-4(a)) [70-72] or dual-voltage (Fig. 2-4(b)) [73] induction motor drives. Comparing with the popular NPC inverter, a dual inverter does not suffer from neutral-point voltage unbalance, does not require any clamping diodes and has more redundant states that can be used for equalizing the switching losses among the numerous controlled switches. It therefore represents an attractive topological alternative for implementing three-level inverter. The same dual concept can equally be applied to the parallel connection of two higher level inverters to produce an overall inverter with an even higher number of output levels. Specific examples include the dual connection of two three-level inverters to form a five-level inverter, and the connection of a three-level inverter and a two-level inverter to form a four-level inverter [74].

Although the dual inverter has many advantages, its single major limitation is its limited application range, which so far has been confined to those specialized motors mentioned earlier if no additional hardware is added. Therefore, unlike other multilevel inverters, the dual inverter cannot be used to supply energy to generic wye- or delta-connected loads, regardless of whether they are connected in three-wire or four-wire configuration.

2.5 Pulse-Width Modulation Schemes for Controlling Multilevel Inverters

A popular PWM method for controlling multilevel inverters is the classical carrier-based sinusoidal PWM (SPWM) scheme, to which many improvements have since been suggested for enhancing its overall performance. Among the improvements proposed, one recommendation is to add an appropriately tuned harmonic offset to the sinusoidal references to raise the inverter modulation index to 1.15, which happens to coincide with the maximum modulation depth attainable by space vector PWM (SVPWM) scheme [22, 75-83].

Fig. 2-5. Illustration of multicarrier arrangements for (a) PD modulation and (b) APOD modulation.

So far, several multicarrier techniques have already been developed for controlling multilevel inverters with various operating advantages noted, such as optimized harmonic performance and reduced common-mode voltage. Among them, the most widely adopted carrier arrangements used for modulating the diode-clamped inverters are illustrated in Fig. 2-5, where four carriers are used for controlling a five-level diode-clamped inverter stated as an example. Comparing the two arrangements shown in Fig. 2-5, it is noted that the first arrangement in Fig. 2-5(a) has zero phase shift between the carriers, giving the phase disposition (PD) scheme, which has previously been proven to produce a better output waveform quality than other carrier-based schemes [82].

Another possible arrangement is shown in Fig. 2-5(b), and is referred to as the alternative phase opposition disposition (APOD) scheme [83], whose four triangular carriers are displaced by 180° . Although the APOD scheme is known to produce a poorer output waveform quality, it favorably produces a lower output common-mode voltage than the PD scheme. This, needless to say, might favor applications like industrial variable-speed ac drives, where large common-mode voltage is known to cause premature motor bearing failure and induced leakage current to ground, which can cause false tripping of ground current protection relays [84, 85].

The same PD and APOD schemes can also be used for controlling a cascaded inverter, but additional logic is needed for equalizing switching losses among the switches. To avoid introducing the additional logic, an alternative phase-shifted carrier modulation scheme can be used, whose carrier arrangement is shown in Fig. 2-6 for controlling a five-level cascaded inverter, where a phase shift of 90° between the two carriers is noted. Although the phase-shifted carrier scheme is noted to produce a significant improvement in the inverter switch utilization, its spectral performance is proven to be the same as the APOD scheme when the same switching frequency is maintained for both schemes [83].

In addition to those traditional carrier-based schemes, other modulation methods that can further reduce the inverter common-mode voltage were recently proposed with a great deal of attention drawn from worldwide researchers [86-88]. In principles, the reduced common-mode schemes function by modifying the inverter PWM state

Fig. 2-6. Illustration of multicarrier arrangements for phase-shifted carrier modulation of five-level cascaded inverter.

patterns without introducing any extra hardware requirement [86, 87]. The cost involved is therefore relatively low, giving the PWM modification approach a competitive advantage over other solutions involving external hardware chokes for example. Although the PWM modification method does have a cost benefit, it unfortunately cannot fully eliminate the inverter produced common-mode voltage during the dead time protection intervals, during which inverter control is lost. Because of that, even though the technique reported in [88] can eliminate the inverter generated common-mode voltage in theory, the practical effect of dead time unavoidably introduces some common-mode spikes to the inverter output waveform. In short, perfect cancellation of common-mode voltage can never be achieved with the PWM modification approach so long as dead time protection is enforced.

Other than the carrier-based modulation theories, space vector modulation concepts have also been reported in the literatures for achieving various operational functions that might be physically hard to achieve using the carrier-based approach. This easiness of modifying the inverter operational characteristics is however accompanied by an increase in computational burden and memory storage. Because of that and given that most of the modulation schemes developed later in the thesis is based on the carrier-based approach, details of the space vector modulation principles are not elaborated further hereon.

2.6 Summary

This chapter reviews popular multilevel inverter topologies and carrier-based modulation schemes for controlling them. Although the inverters have already been proven to function well, and have already been widely adopted for high power or medium voltage applications, they still lack the flexibility of performing voltage-boost energy conversion. To introduce this additional boost capability to the inverter basic functionality, certain topological and modulation modifications need to be performed, whose underlying principles are described from Chapter 4 onwards, after reviewing

and designing relevant buck-boost energy conversion concepts in Chapter 3.

Chapter 3 Voltage Buck-Boost Concepts

Broadly, voltage buck-boost energy conversion can either be implemented using the two-stage or single-stage approach, where the latter includes the newly proposed Z-source, Ćuk and SEPIC buck-boost dc-ac inversion concepts. Comparing them, the only difference noted between the two approaches is that the derived single-stage topologies usually have some functionalities integrated so as to reduce the number of active and / or passive components where possible [89-98]. On the other hand, the two-stage approach is usually configured by simply cascading a dc-dc boost converter to a dc-ac voltage source inverter or a dc-dc buck converter to a dc-ac current source inverter without much integration. These two approaches are now reviewed, together with a description of the newly proposed diode-assisted energy conversion concept, before exploring for methods to extend them to higher level inverters from Chapter 4 onwards.

3.1 Two-Stage Buck-Boost Power Inversion

For illustration, Fig. 3-1 shows a two-stage buck-boost converter implemented by cascading a dc-dc boost converter to a rear-end dc-ac inverter [99]. Placed at its front-end, the dc-dc boost converter can boost the intermediate dc-link voltage to a value higher than its input voltage V_{dc} , before the rear-end inverter operates to produce an ac output whose amplitude can be higher or lower than V_{dc} . Although the two-stage

Fig. 3-1. Topological illustration of two-stage buck-boost inversion using a front-end dc-dc boost converter.

power inversion solution is easy to understand, it lacks integration with some component functionalities duplicated within the converter. That translates to a higher component count and converter size, which can be minimized if the identification and subsequent integration of common functionalities are performed.

3.2 Z-Source Inverter

Z-source voltage-type inverter is first proposed in [1] with its detailed continuous and discontinuous modulation principles documented in [100]. Its extension to the Z-source current-type topology is also pursued and documented in [101], together with other interesting topics like resonant damping reported in [102], modeling in [103] and closed-loop controller design in [104]. Application wise, Z-source inverter has been recommended for processing energy harnessed from photovoltaic (PV) and fuel cell stacks [105, 106], as well as for conditioning energy in hybrid vehicle traction systems [107]. Despite of its current rapid stage of development, most research work on Z-source inverter is still focusing on the two-level inverter type with its extension to higher level inverters still left unexplored. Before the extension can be pursued smoothly, a thorough review of the two-level Z-source conversion concepts needs to be described to build a strong theoretical foundation from which various complex multilevel Z-source inverters can be developed.

Beginning with the three-phase two-level Z-source inverter shown in Fig. 3-2, a unique feature noted in the figure is the presence of an X-shaped impedance network and a

Fig. 3-2. Voltage-type three-phase Z-source inverter.

series diode connected between the dc input source and inverter circuitry. Needless to say, the series diode placed adjacent to the source can be replaced by a switch with an anti-parallel diode if reverse flow of energy is desired, but for cases whereby the input sources are fuel cells or PV panels, this provision needs not be effected.

Despite its unique front-end impedance network, the rear-end switching circuitry of the Z-source inverter is simply a traditional voltage source bridge that can assume six active and two null states. In addition to the eight traditional switching states, the Z-source inverter can enter a number of unique shoot-through states initiated by turning ON the two switches in a phase-leg, four switches from two phase-legs or all six switches simultaneously to short the inverter bridge. These shoot-through states are obviously not allowed in a traditional inverter, where dead time protection is unavoidable. For the Z-source inverter, shorting of the inverter bridge is however considered conceptually safe since the current is now effectively limited by the introduced Z-source inductors. Therefore instead of avoiding it, the unique shoot-through condition is smartly explored by the Z-source inverter for voltage boosting, whose operating principles are better explained by considering those equivalent circuits shown in Fig. 3-3 for the cases of shoot-through and non-shoot-through states respectively.

When in the shoot-through state during time interval T_0 , the inverter bridge is undoubtedly shorted without any energy being transferred to the ac load, while the input diode D is noted to turn OFF naturally to give the equivalent circuit shown in Fig.

Fig. 3-3. Z-source inverter equivalent circuit (a) shoot-through state (b) non-shoot-through state.

3-3(a). From the circuit, the relevant state equations are then determined as:

$$\begin{cases} v_{L1} = v_{L2} = v_L = V_{C1} = V_{C2} = V_C \\ v_d = v_L + V_C = 2V_C \\ v_i = 0 \end{cases} \quad (3.1)$$

Where, a symmetrical Z-source impedance network is assumed with $L_1 = L_2 = L$ and $C_1 = C_2 = C$.

Alternatively, when in any of the non-shoot-through active and null states during time interval T_1 , current now flows from the dc source through the Z-source impedance network to the inverter bridge, whose equivalent circuit is drawn in Fig. 3-3(b), where the inverter bridge and load are represented by a current source and diode D is drawn conducting. From this equivalent representation, the relevant state equations are re-derived as:

$$\begin{cases} v_L = V_{dc} - V_C \\ v_d = V_{dc} \\ v_i = V_C - v_L = 2V_C - V_{dc} \end{cases} \quad (3.2)$$

Averaging the voltage across one of the Z-source inductors over a full switching cycle ($\int_0^T v_L dt = 0$, where $T = T_0 + T_1$) then gives rise to:

$$V_C = \frac{T_1}{T_1 - T_0} V_{dc} \quad (3.3)$$

By substituting (3.3) to (3.2), the peak dc voltage v_i' across the inverter phase-legs and the peak ac output voltage v_x' are then derived as:

$$\hat{v}_i = 2V_C - V_{dc} = \frac{1}{1 - \frac{2T_0}{T}} V_{dc} = B V_{dc} \quad (3.4)$$

$$\hat{v}_x = M \frac{\hat{v}_i}{2} = B \left\{ M \frac{V_{dc}}{2} \right\} \quad (3.5)$$

Where, B represents the boost factor, M refers to the modulation index commonly used for conventional voltage source inverter (VSI) modulation, and the term in $\{\}$ gives the ac output of a conventional VSI. Theoretically, for $0 \leq T_0 < 0.5$, the boost factor B can

Fig. 3-4. Continuous modulation of three-phase-leg Z-source inverter.

vary from 1 to infinity, which obviously represents a voltage boosting action that is not attainable by a conventional VSI.

Modulation wise, regardless of the specific PWM strategy used, the basic principle behind Z-source inverter control is always to insert appropriate shoot-through states to the inverter state sequence, as demonstrated in Fig. 3-4, where three shoot-through states are inserted per switching cycle for the case of continuous modulation [100]. The only constraint that needs to be observed when inserting the shoot-through states is that the active states must stretch over the same time durations as for a conventional VSI when the reference phasor is orientated at the same angular position. The rest of the switching cycle is then occupied by a combination of null and shoot-through states with both states producing a set of zero line voltages (ZLV) at the inverter ac output terminals. Doing so would ensure that the Z-source inverter accurately reproduces the reference phasor by maintaining the same normalized volt-sec average as for a conventional VSI [1].

As anticipated, the state sequence in Fig. 3-4 can also be produced using the reference-carrier comparison arrangement described in [100], where it is clearly stated that the required references (two per phase) for inserting shoot-through states at the three state transitions are expressed as:

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$$\begin{cases}
V_{\max(SX)} = V_{\max} + V_{\text{off}} + T_S \\
V_{\max(SX')} = V_{\max} + V_{\text{off}} + T_2 \\
V_{\text{mid}(SX)} = V_{\text{mid}} + V_{\text{off}} + T_2 \\
V_{\text{mid}(SX')} = V_{\text{mid}} + V_{\text{off}} - T_2 \\
V_{\min(SX)} = V_{\min} + V_{\text{off}} - T_2 \\
V_{\min(SX')} = V_{\min} + V_{\text{off}} - T_S
\end{cases}$$

$$V_{\text{off}} = -0.5(V_{\max} + V_{\min}), T_S = T_0/T, T_2 = T_0/3T$$

$$X = A, B \text{ or } C \quad (3.6)$$

Using (3.6), the Z-source inverter is always operating with the minimum of six device commutations per switching cycle, which indirectly means a lower switching loss produced by the inverter. Instead of (3.6), a second shoot-through insertion method is also possible, whereby the needed shoot-through states are always inserted by turning ON the same two switches in a selected phase-leg with the shoot-through duration kept constant [108, 109]. This method, although simple, gives rise to a higher commutation count per switching cycle, and hence a higher switching loss assuming that all other operating parameters are kept unchanged. Therefore, comparatively, the first method is viewed as more favorable, whose operating principles are subsequently adopted for designing modulation schemes for controlling those Z-source multilevel inverters proposed in later chapters.

Another issue of importance to a Z-source inverter is the sizing of its LC parameters found in the X-shaped impedance network. For that, the general guideline is to raise C and lower L to tilt more towards the dc voltage storage characteristics if a voltage-source inverter is connected to its rear end. In contrast, L should be raised and C should be lowered if a current-source inverter is connected to its rear end. Adding to those qualitative descriptions is a set of simple mathematical equations for determining the L and C values more precisely depending on the amount of ripple content allowed in the circuit. These equations can conveniently be derived by considering the inductive current ripple and capacitive voltage ripple in a shoot-through interval, expressed as:

$$\begin{cases} \Delta i_L = \frac{V_C T_0}{L} = \frac{T_1 \cdot T_0 \cdot V_{dc}}{(T_1 - T_0)L} \\ \Delta V_C = \frac{I_L T_0}{C} \end{cases} \quad (3.7)$$

Depending on the ripple content and nominal operating conditions (V_{dc} , I_L , T_1 and T_0) specified, the preferred L and C values can then be calculated using (3.7). Other than satisfying (3.7), it is also important to consider operation under light load condition, during which the inductance value should be high enough to avoid entering those unwanted operating states identified in [2]. Instead of raising L , an alternative method to avoid the six unwanted states is to replace the front-end diode with an active switch, as explained in Chapter 5 for the three-level Z-source inverters, whose sizing guidelines are no different from those described here.

3.3 Ćuk and SEPIC-Derived Buck-Boost Inverters

Besides the Z-source inverter, other topologies exhibiting single-stage buck-boost inversion ability can be deduced from those bidirectional buck-boost two-level rectifiers reported in [3]. Specifically in [3], the designed rectifiers are developed by

Fig. 3-5. Topologies of (a) Ćuk- and (b) SEPIC-derived buck-boost inverter.

Fig. 3-6. Equivalent circuits of Ćuk-derived two-level inverter when (a) SW is ON and (b) SW is OFF.

integrating either a Ćuk or Zeta dc-dc converter to the rear-end of a traditional voltage source rectifier. For illustration, example topologies drawn for dc-ac power inversion are shown in Fig. 3-5, where the added voltage boost circuitries are noted to include an additional switch, an inductor and a series capacitor. Discussion on how these added boost circuitries can introduce an additional degree of control freedom to the otherwise voltage-buck inverter is now elaborated so as to build the foundation needed for extending them to multilevel inverters.

3.3.1 Operational Principles and Modulation Schemes of Ćuk-Derived Buck-Boost Inverter

Distinguished by the ON and OFF states of switch SW in Fig. 3-5(a), the two equivalent circuits used for representing the Ćuk-derived two-level inverter are shown in Fig. 3-6(a) and (b) respectively. When SW is turned ON as shown in Fig. 3-6(a), the inductive current i_L flows through the dc source and switch SW to boost the energy stored in inductor L . Meanwhile, the capacitor C appears directly across the inverter dc rails for powering the external ac load when the inverter is commanded to assume an active state (six possibilities in total). Alternatively, when SW is turned off, the inductive current i_L shoots through all phase-legs (flowing through their anti-parallel diodes for dc-ac inversion) to charge the capacitor C , while producing a set of zero three-phase line voltages across the external load. Therefore, to the load, a shoot-through state appears similar to an inverter null state (two in total) since they uniformly produce zero line voltages.

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Based on the above-described operating modes, current i_L is noted to rise with a slope of V_{dc}/L during SW = ON and falls with a slope of $-(V_C - V_{dc})/L$ during SW = OFF. During steady-state operation, the incremental currents in both states must sum to zero to give a constant average value. Therefore, by manipulating this steady-state condition, the voltage gain expression of the Ćuk-derived inverter can eventually be derived as:

$$\frac{V_{dc}}{L} \cdot kT = \frac{V_C - V_{dc}}{L} \cdot (1-k)T; \quad V_C = \frac{1}{1-k} V_{dc} \quad (3.8)$$

where, T is the switching period and k represents the conductive duty ratio of switch SW. Given also that V_C is the physical dc-link voltage appearing across the inverter when in an active state during SW = ON, the peak ac output voltage can directly be written as:

$$V_{ac} = M \frac{V_C}{2} = \frac{M}{1-k} \frac{V_{dc}}{2} \quad (3.9)$$

where, M refers to the traditional modulation index and $1/(1-k)$ is the boost factor added by the voltage boost circuitry. Clearly, (3.9) states that the peak ac output voltage V_{ac} can be stepped up or down by setting $k > 0.5$ or $k < 0.5$ respectively. For M , its value is limited by the constraint of $M \leq k$, which directly restates the fact that active states can only occur within intervals during which SW = ON. While tuning these parameters, it is also beneficial to set M equal to k so as to minimize voltage stress ($V_{dc}/(1-k)$) across semiconductor devices, while producing the maximum possible output voltage at any particular instance.

From the above discussion, it is noted that the Ćuk-derived two-level inverter can

Fig. 3-7. PWM sequences for controlling Ćuk-derived buck-boost two-level inverter with SW = OFF states inserted (a) at the edges of each switching cycle and (b) at each state transition in a switching cycle.

effectively operate in three distinct states with the first two representing traditional active and null states that can be assumed when $SW = ON$, and the last state representing $SW = OFF$. Among these three switching states, the null and $SW = OFF$ states give rise to a set of zero three-phase line voltages, and to an externally connected ac load, both states appear similar. Therefore, as a preliminary step towards deriving PWM schemes for controlling the buck-boost inverter, a classical two-level carrier-based or space vector modulator is used first for dividing each switching period into two active intervals (Active 1 and Active 2, where at least one line voltage is finite) and two “zero-line-voltages” intervals, as illustrated by the top sequence in Fig. 3-7. The ZLV intervals are then divided into null and $SW = OFF$ intervals (using an appropriate technique to be formulated later), where two possible divisions are shown in Fig. 3-7(a) and (b) respectively (in [3], only the simple case of ZVL intervals fully replaced by $SW = OFF$ states is considered). Although both sequences appear visibly different, their normalized volt-sec averages are equal so long as their active intervals are kept constant (since both null and $SW = OFF$ states produce the same zero line voltages, as mentioned earlier).

In Fig. 3-7(a), the $SW = OFF$ states are inserted at the edges of every switching cycle, and the number of device commutations needed per switching cycle depends on whether the inverter is performing dc-ac power inversion or ac-dc power rectification. For dc-ac power inversion, besides the six device commutations (with dead-time protection) needed for active $\leftrightarrow$ active and active $\leftrightarrow$ null transitions when $SW = ON$, additional two commutations are needed for turning SW OFF near the edges of each switching cycle. Note that upon turning SW OFF, the anti-parallel diodes of a particular phase-leg start conducting naturally to short the inverter dc link since current is flowing upwards through the inverter circuitry, as illustrated in Fig. 3-6(b). Therefore, the explicit turning ON of the two switches from a particular phase-leg (e.g. SA1 and SA2) is not required. On the other hand, when ac-dc power rectification is commanded, current through the dc network reverses its direction, and the explicit turning ON of both switches from a phase-leg is now required, but the explicit turning

Fig. 3-8. Insertion of a short-circuit state to an active → null transition during ac-dc rectification.

OFF of SW is not necessary since only the free-wheeling diode of SW is conducting and it naturally reverse-biases upon the short-circuiting of a phase-leg.

Alternatively, in Fig. 3-7(b), six extra commutations are needed for inserting the three intermediate SW = OFF states, in addition to the six commutations used for three-phase dc-ac power inversion. Scoring a better performance, only six device commutations per switching cycle in total are needed for ac-dc power rectification since the shorting of an appropriate phase-leg can implicitly be inserted by introducing overlap delays to the inverter state sequence rather than using additional commutations. For example, referring to Fig. 3-8, the transition from an active to a null state can progress through an intermediate state during which both switches from phase A are turned ON simultaneously (see shaded state in Fig. 3-8). Counting the number of commutations used, it is noted that the number of commutations needed for completing the active→null transition is still two regardless of whether phase A short-circuit is inserted or not. Obviously, the short-circuit state is inserted by simply introducing an overlap delay between the ON→OFF transition of SA1 and OFF→ON transition of SA2. Another feature noted with the sequence in Fig. 3-7(b) is that dead-time protection is not needed for switching the three-phase inverter circuitry because each active↔active and active↔null transition is transited through a SW = OFF state, whose inherent free-wheeling diode commutation ensures smooth state transition.

Fig. 3-9. PWM scheme for buck-boost inverters.

Summarizing the above discussion on commutation counts in Table 3-1, it is noted that the sequence in Fig. 3-7(b) gives rise to the lowest forced commutation count when used for ac-dc power rectification, but the sequence in Fig. 3-7(a) is better conditioned for bi-directional operation. Therefore, the edge-insertion sequence in Fig. 3-7(a) is selected for future work, and a simple carrier-based implementation approach that can conveniently be programmed into the on-chip hardware modulator of a modern digital signal processor (DSP) is studied next with its carrier-reference arrangement shown in Fig. 3-9. As noted in the figure, three sinusoidal references $\{V_a, V_b, V_c\}$ are used for the initial dividing of a switching period T into active 1, active 2 and ZLV intervals, while two additional lines are used for inserting $SW = OFF$ states within the ZLV intervals when the triangular carrier is above the upper reference line and below the lower reference line respectively. To summarize, the references needed are mathematically expressed as:

$$\begin{cases} V_a = M \cos(\omega t) + V_{off} \\ V_b = M \cos(\omega t - 120^\circ) + V_{off} \\ V_c = M \cos(\omega t + 120^\circ) + V_{off} \\ V_u = -V_d = k \end{cases} \quad (3.10)$$

Where, V_{off} represents the triplen offset commonly added for obtaining a better high frequency waveform quality, and $|V_a|, |V_b|, |V_c| \leq k$ since as mentioned earlier, $M \leq k$.

3.3.2 Operational Principles and Modulation Schemes of SEPIC-Derived Buck-Boost Inverter

Table 3-1. Commutation count needed by state sequences in Fig.3-7.

	Number of Commutations Per Switching Cycle	
	dc-ac Inversion	ac-dc Rectification
Edge Insertion Fig. 3-7(a)	8	8
Intermediate Insertion Fig. 3-7(b)	12	6

Offering an alternative solution, the SEPIC-derived buck-boost inverter shown in Fig. 3-5(b) can perform the same bidirectional buck-boost energy conversion as for the Ćuk-derived inverter, and uses the same numbers of passive and active components. In brief, when SW turns ON as shown in the equivalent circuit of Fig. 3-10(a), the inductor current i_L is noted to rise with a slope of V_{dc}/L , while the dc source and capacitor C are noted to power the rear-end inverter together in series, giving a dc-link voltage of $V_C + V_{dc}$. On the other hand, when SW turns OFF as shown in Fig. 3-10(b), i_L starts to fall with a slope of $-V_C/L$, while flowing through the inverter anti-parallel diodes (effectively shorting the inverter bridge) and releasing its stored inductive energy to capacitor C . Upon reaching steady state, the amount of current rise in the first interval must equal to the dip in current in the second interval in order to give a constant average value. Mathematically, this equality can be expressed as:

Fig. 3-10. Equivalent circuits of SEPIC-derived two-level inverter when (a) SW is ON and (b) SW is OFF.

$$\frac{V_{dc}}{L} \cdot kT = \frac{V_C}{L} \cdot (1-k)T; V_C = \frac{k}{1-k} V_{dc} \quad (3.11)$$

where the calculated capacitive voltage V_C can then be used for computing the peak ac output voltage expressed as:

$$V_{ac} = M \frac{V_C + V_{dc}}{2} = \frac{M \cdot V_{dc}}{2(1-k)} \quad (3.12)$$

Comparing (3.12) with (3.9), both SEPIC and Ćuk-derived inverters are noted to produce the same input-to-output voltage gains even though their V_C expressions are different. This is more or less expected since their operating principles are closely similar, implying also that the same modulation principles described in Section 3.3.1 can equally be applied to the SEPIC-derived inverter without any modification needed.

3.4 Diode-Assisted Buck-Boost Inverters

Although the buck-boost topologies discussed in Section 3.3 can theoretically boost their ac output voltages to any desired value without an upper limit, the presence of parasitic influences generally lowers their attainable gain to a finite (sometimes unsatisfactory) value. This degradation is usually more prominent at high gain, high duty ratio operating conditions, during which the boost inductor is charged over a longer time duration, and discharged (or recovered back to its initial state) within an unrealistically short time interval. Therefore, extracting high transfer gain from the buck-boost inverters can at times be difficult in practice.

Contributing another series of single-stage inverters with a larger voltage boost ratio to the existing pool of buck-boost inverters, this section presents a number of newly proposed diode-assisted VSIs, whose topological layouts use only a single inductive element, similar to those reported in [3, 110]. In addition to the inductor, the proposed inverters use an X-shaped diode-capacitor (also referred to as diode-assisted) network connected between their front-end input source and rear-end traditional VSI circuitry. (Note that a similar network has previously been used in [111] for a dc-dc converter,

which intuitively is more straightforward than using it for dc-ac energy inversion, where more topological and modulation variants can be derived for meeting those requirements currently under consideration). With the diode-assisted network integrated, a voltage multiplication factor of two can easily be obtained with the same conductive duty ratio and capacitive rating, since the diodes in the network naturally conduct to perform parallel capacitive charging, before reverse-biasing in the next interval to effect a series capacitive discharging.

Despite having an additional diode-capacitor network, the proposed inverters can still be controlled relatively easily using standard VSI modulation schemes, but with a third switching state introduced to the existing active and null states for naturally effecting the above-described diode-assisted circuit reconfiguration. In total, two distinct modulation schemes are proposed with the first gaining a better symmetrical waveform quality, and the second gaining a lower commutation count without stressing the active and passive circuit elements. Both modulation schemes can generically be used for controlling all diode-assisted inverters proposed in this section with their experimental performances verified in a later subsection using a number of implemented laboratory prototypes.

3.4.1 Topologies and Operational Principles

3.4.1.1 Ćuk-Derived Buck-Boost Inverter with a Diode-Capacitor Network

Fig. 3-11. Ćuk-derived buck-boost inverter with a diode-capacitor network.

Although (3.9) infers that the Ćuk-derived inverter can theoretically attain an infinite gain, practical parasitic imperfections generally limit its maximum gain to a finite value. In addition to this limitation of maximum gain, its associated large k is expected to stress the switches considerably, since they are now forced to turn OFF and then ON within a short time duration. To produce a higher gain, while at the same time avoid using a large k , the diode-assisted inverter shown in Fig. 3-11 is proposed here, where an X-shaped diode-capacitor network is noted to replace the single dc capacitor C placed between SW and the three-phase VSI bridge shown in Fig. 3-5(a). As seen, the X-shaped network in Fig. 3-11 consists of two capacitors (C_1 and C_2) and two diodes (D_1 and D_2), with a shunt-connected switch SW preceding it. By turning ON SW, the inductive current i_L flows solely from the dc source to boost the magnetic energy stored in inductor L according to the equivalent circuit shown in Fig. 3-12. Besides inductive charging, diode D_1 and capacitor C_2 are found to be in parallel, and by noting the voltage polarity of C_2 , it is clear that D_1 is forced to block current flow, resulting in it being replaced by an open-circuit shown in Fig. 3-12(a). By symmetry, diode D_2 is also replaced by an open-circuit in the same figure. With both diodes OFF, capacitors C_1 and C_2 are observed to be in series with the ON switch SW connecting the positive

Fig. 3-12. Equivalent circuits of Ćuk-derived diode-assisted inverter when SW is turned (a) ON and (b) OFF respectively.

terminal of C_1 to the negative terminal of C_2 to give a total dc-link voltage of $V_i = V_{C1} + V_{C2} = 2 V_C$ (since $C_1 = C_2 = C$ is assumed) for powering the externally connected ac load. Having a larger dc-link voltage now also means the switches SX and SX' (X = A, B and C) in the rear-end three-phase bridge have to block a higher voltage, expressed as $2 V_C$.

On the other hand, with SW turned OFF, the inductor current i_L flows through the diode-capacitor network according to the equivalent circuit shown in Fig. 3-12(b), where SW is observed to block voltage V_C , and diodes D_1 and D_2 are now forward-biased to connect C_1 and C_2 in parallel. Each capacitor is therefore charged by half of the inductive current ($i_{1L} = i_{2L} = i_L/2$) to its peak voltage, before SW is turned ON again to start the next switching cycle. Obviously, the dc-link voltage V_i is not maintained constant over each full switching cycle, but rather assumed the two discrete values of $2V_C$ (SW = ON) and V_C (SW = OFF). Therefore, quite intuitively, for producing a higher voltage gain, the inverter active states (six in total) must be placed only within the SW = ON interval. In contrast, inverter null states (two in total) are not restricted, meaning that they can occupy either the SW = ON or SW = OFF interval without transferring the discretely varying dc-link voltage pattern to the ac load, since null states give rise to zero line voltages regardless of the dc link voltage variation.

For deriving the inverter voltage transfer gain expression, steady-state constraints applied to the inductor L are analyzed with the inductive current i_L observed to rise with a slope of V_{dc}/L during the SW = ON interval and fall with a slope of $-(V_C - V_{dc})/L$ during the SW = OFF interval. Equating the incremental rise and fall of i_L during the two intervals in a switching period T , voltage V_C across each capacitor can be derived as:

$$\frac{V_{dc}}{L} \cdot kT = \frac{V_C - V_{dc}}{L} \cdot (1-k)T; \quad V_C = V_{C1} = V_{C2} = \frac{1}{1-k} V_{dc} \quad (3.13)$$

Noting that $V_{C1} + V_{C2}$ is the dc-link voltage imposed across the external load during an active interval, the resulting peak ac output voltage is then derived as:

Fig. 3-13. SEPIC-derived buck-boost inverters with a diode-capacitor network.

$$\hat{v} = M \frac{V_{C1} + V_{C2}}{2} = \frac{MV_{dc}}{1-k} \quad (3.14)$$

Comparing (3.14) with (3.9), the ac output voltage of the diode-assisted buck-boost inverter is observed to experience double voltage boosting assuming that all control parameters are set equally. The proposed inverter is therefore suitable for use in those buck-boost applications, where a bias towards higher voltage boost is needed.

3.4.1.2 SEPIC-Derived Buck-Boost Inverter with a Diode-Capacitor Network

Besides the Ćuk topology described earlier, a second diode-assisted buck-boost topology with an enhanced voltage gain can be designed based on the SEPIC energy

Fig. 3-14. Equivalent circuits of SEPIC-derived diode-assisted inverter when SW is turned (a) ON and (b) OFF respectively.

conversion principles. For raising the voltage gain above that expressed in (3.12), a diode-capacitor network is inserted between the front-end dc circuit and rear-end inverter topology, as shown in Fig. 3-13, where the dc source polarity is now reversed.

Despite exhibiting similar output performance, operational principles of the SEPIC diode-assisted buck-boost inverter are considerably different from those of its Ćuk-derived variant. Specifically, when SW turns ON, inductor current i_L flows through the dc source, which then implies that $V_L = V_{dc}$, according to the equivalent circuit shown in Fig. 3-14(a). Noting also that diodes D_1 and D_2 are OFF during that interval, the dc-link voltage V_i is deduced as equal to $V_{C1} + V_{C2} + V_{dc}$, representing the series connection of the capacitive and dc source voltages. On the other hand, with SW turned OFF, the dc source is disconnected from its rear-end circuitry, causing the inductive current i_L to now flow through D_1 and D_2 to charge capacitors C_1 and C_2 equally ($i_{1L} = i_{2L} = i_L$). Although only half of i_L charges each capacitor, the capacitor voltage can still be derived as (3.11), giving rise to a peak ac output voltage of:

$$\hat{v} = \frac{MV_i}{2} = \frac{M(V_{dc} + V_{C1} + V_{C2})}{2} = \frac{M(1+k)V_{dc}}{2(1-k)} \quad (3.15)$$

Comparing (3.15) and (3.14), an additional factor of $(1+k)/2$ is noted in (3.15), which obviously implies that the SEPIC diode-assisted inverter in Fig. 3-13 has a slightly

Fig. 3-15. Typical symmetrical state sequence generated using two additional linear references.

lower voltage gain (since $k < 1$), as compared with its Ćuk-derived variant. Nevertheless, the gain in (3-14) is still higher than that produced by the SEPIC inverter reported in last section, with its voltage-buck feature preserved and freely tuned by adjusting M and k accordingly.

3.4.2 Pulse-Width Modulation Schemes

As noted in Section 3.4.1, inverter active states should only be commanded during the $SW = ON$ interval to fully utilize the maximum dc-link voltage available and to avoid possible volt-sec error caused by the frequently chopped dc-link voltage. That indirectly means that the $SW = OFF$ interval is fully spanned by null states with zero three-phase line voltages produced at the inverter output. With these modulation criteria in view, a number of modulation schemes are presented as follows, for controlling the proposed diode-assisted buck-boost VSIs with different performance features noted for each scheme.

3.4.2.1 PWM Scheme with Optimized Harmonic Switching

The diode-assisted buck-boost inverters discussed earlier can be controlled by switching SW and the rear-end inverter circuitry appropriately so as to produce undistorted ac outputs and preferably no excessive increase of voltage stress across both passive and active components. For achieving that, a possible modulation scheme is shown in Fig. 3-15, where symmetrical placement of $SW = OFF$ intervals at the edges of each half carrier cycle is intentionally planned for obtaining optimal waveform quality (similar in principle to the modulation of traditional two-level VSI).

Conceptually, this can be ensured by using two linear references for comparison with the single triangular carrier used in the modulation process. Upon the triangular carrier rising above the upper reference line V_u or falling below the lower line V_d , switch SW is commanded to turn OFF. After segregating the $SW = OFF$ interval, the remaining $SW = ON$ interval must appropriately be divided into active and null states, which conveniently can be enforced by using the traditional sine-triangle comparison method,

whose waveform placement is also shown in Fig. 3-15. As seen, by constraining three sinusoidal references within the vertical span bounded by V_u and V_d , active states are entered only during the $SW = ON$ interval, which then ensures that the “jumps” in dc-link voltage per half carrier cycle does not distort the inverter normalized volt-sec average. The reason for that is because the jumps always occur in null states during which the inverter ac output voltages are zero, implying that the externally connected load will not experience an impact.

This latter feature of null states appearing indifferent in either the $SW = OFF$ or ON

Fig. 3-16. Typical asymmetrical state sequences generated using one additional linear reference (a) without and (b) with sinusoidal reference shifting.

interval allows a degree of freedom for minimizing voltage stress across passive and active components of the inverter. For that, as a rule of thumb, it is recommended to tune the control parameters (M and k in (3.14) and (3.15)) so that the desired gain is obtained with active states spanning the full $SW = ON$ interval, and null states occupying the remaining $SW = OFF$ interval in a half switching cycle. For implementation purposes, the above-described modulation process can be summarized with its references also expressed mathematically as (3.10).

3.4.2.2 PWM Scheme with Minimal Commutation Count

Although (3.10) generally gives rise to a symmetrical null state placement in each half carrier cycle for optimizing the inverter waveform quality, V_u and V_d undesirably cause SW to switch twice per half carrier cycle, unlike the rear-end inverter bridge, where each switch commutates only once in the same period (see the gating signals for SA , SB and SC in the upper half of Fig. 3-15). For cases where SW should not be overstressed, a simple modification can be made to the modulation scheme to halve the commutation count of SW . The suggested modification is shown in Fig. 3-16(a), where only either the upper solid line V_u or lower dashed line V_d is used (not both). Obviously, using only V_u as an example causes $SW = OFF$ intervals to appear only at the peaks of the triangular carrier with two $SW = OFF$ intervals surrounding a full carrier cycle (no longer half carrier cycle). That also means that SW commutates only once per half carrier cycle, as intended unlike in Fig. 3-15, where two $SW = OFF$ intervals are observed per half carrier cycle since they are inserted at both the peaks and troughs of the triangular carrier. Further reduction of commutation count for the other switches found in the inverter bridge by adopting discontinuous PWM is however noted to be not possible since the buck-boost inverters require synchronized triggering between SW and the inverter bridge, which would give rise to imprecise boosting if discontinuous PWM is used to remove one of the null states.

Although the resulting state sequence is clearly no longer symmetrical per half carrier cycle, the overall active interval is still centrally placed within each half carrier cycle,

inferring that its waveform quality is not severely altered. In addition, the inverter duty ratio k' of SW is now no longer equal to k , but re-expressed as $k' = (1+k)/2$, assuming that the same linear reference of $V_u = k$ is used for modulation. This newly derived duty ratio k' gives rise to different dc capacitive voltages for the Ćuk-derived diode-assisted buck-boost inverter (for example), whose expressions are re-derived as:

$$V_{C1} = V_{C2} = \frac{1}{1-k'} V_{dc}; \quad k' = \frac{1+k}{2} \Rightarrow V_{C1} = V_{C2} = \frac{2}{1-k} V_{dc} \quad (3.16)$$

Where, a factor of two is noted between (3.16) for asymmetrical boosting and (3.8) for symmetrical boosting. Although this second modulation scheme indeed reduces the switching frequency of SW, it obviously introduces a limiting constraint to the inverter operation since null state $\{1, 1, 1\}$ can no longer be replaced by SW = OFF interval, implying that duty ratio of SW is always greater than 0.5 instead of 0 for the scheme shown in Fig. 3-15. This can unnecessarily stress semiconductor switches with a high dc link voltage even under low ac output voltage requirement.

To avoid the unnecessarily stressing of semiconductor switches, while preserving the advantage of lower commutation count, the three-phase sinusoidal references can be shifted down towards the trough of the triangular carrier, as illustrated in Fig. 3-16(b), where the upper linear reference V_u is used for commutating SW. Alternatively, the references can be shifted upwards if the lower linear reference V_d is used instead. Indeed, this shifting of sinusoidal references allow the linear reference V_u (V_d) to shift further downwards (upwards), even towards the negative (positive) carrier region with only a single SW = OFF interval maintained at every half carrier cycle. Using this method and arranging for the sinusoidal references to span the full range bounded by $V_u = k$ ($V_d = -k$) and the trough (peak) of the carrier for minimizing semiconductor stresses, the inverter peak ac output voltage is re-expressed as:

$$\hat{v} = \frac{M}{2} \cdot \frac{2 \cdot 2}{1-k} \cdot V_{dc}; \quad M = \frac{1+k}{2} \Rightarrow \hat{v} = \frac{1+k}{1-k} \cdot V_{dc} \quad (3.17)$$

Comparing (3.14) and (3.17), a feature noted is that the same ac output voltage can be produced by both expressions if their respective control parameters are set to $M = k = 0.5$ in (3.14) and $k = 0$ in (3.17). Therefore, both modulation schemes are comparable

in terms of voltage buck-boost capability, but of course, the latter scheme has a lower commutation count, albeit at the expense of a slightly poorer waveform quality, caused by the non-centering of active states within each half carrier cycle. If indeed, these features are desirable, the asymmetric modulator can conveniently be implemented using the modified references shown in (3.18). Comparing with (3.10), (3.18) is found to include an additional offset term written as $-(1-k)/2$, which obviously is introduced by the intended reference shifting process, and is limited by $(2M-1) \leq k < 1$.

$$\begin{cases} V_a = M \cos(\omega t) + V_{off} - (1-k)/2 \\ V_b = M \cos(\omega t - 120^\circ) + V_{off} - (1-k)/2 \\ V_c = M \cos(\omega t + 120^\circ) + V_{off} - (1-k)/2 \\ V_u = k \end{cases} \quad (3.18)$$

Before ending this subsection, a simple example is described here to illustrate cases, where k is set negative, which can at times cause confusion. Assuming initially that M is set to 0.3 to give a set of sinusoidal references that vary between -0.3 and 0.3 , the maximum offset that can be added to them is -0.7 to shift them downwards to touch the troughs of the carrier. The modified references then vary between -1 and -0.4 , inferring that the region above -0.4 can now be fully occupied by the SW = OFF state to produce the maximum gain at the lowest voltage stress. For achieving that, k should ideally be set to the negative value of -0.4 without affecting the state sequence shown in Fig. 3-16(b).

3.4.3 Experimental Results of Diode-Assisted Buck-Boost VSIs

The proposed diode-assisted buck-boost inverters were tested experimentally using a constructed laboratory prototype that can freely be configured as either the Ćuk or SEPIC-derived variants. For both topologies, the diode-capacitor network was constructed using $C_1 = C_2 = 220 \mu\text{F}$, and was powered from a 30V source through an inductor of $L = 4 \text{ mH}$. The constructed inverter was controlled using a digital signal processor (DSP) card, which conveniently allows modulation schemes discussed in Section 3.4.2 to be downloaded for testing.

Fig. 3-17. Experimental waveforms of Ćuk-derived diode-assisted inverter with $M = 0.7$ and $k = 0.7$, controlled using modulation scheme with optimized harmonic performance.

Fig. 3-18. Experimental waveforms of Ćuk-derived diode-assisted inverter with $M = 0.3$ and $k = 0.3$, controlled using modulation scheme with optimized harmonic performance.

Using this experimental setup with a RL load connected ($R = 50 \, \Omega$ and $L = 6.3 \, \text{mH}$), Fig. 3-17 shows the boost operating mode of the Ćuk-derived diode-assisted inverter controlled using the optimized modulation scheme discussed in Section 3.4.2.1, with its control parameters set to $M = 0.7$ and $k = 0.7$. Clearly, the dc link voltage, reflected by the pulse height of the line voltage, is boosted to 200 V, which indeed matches that calculated using (3.13) ($2V_C = 2V_{dc}/(1-k) = 200 \, \text{V}$). Multiplying with the modulation index M then gives rise to a fundamental line voltage amplitude of $\sqrt{3} \times 1.15 \times 0.7 \times 100 \approx 140 \, \text{V}$, where the factor of 1.15 is introduced by the added triplen offset.

Complementing its performance, Fig. 3-18 shows the captured experimental

waveforms for the same Ćuk-derived inverter operating with its control parameters retuned to $M = 0.3$ and $k = 0.3$. According to (3.13), the dc-link voltage is now given by $2V_C = 2V_{dc}/(1-k) \approx 86$ V, which again is reflected by the pulse height of the inverter line voltage. That then gives a line voltage amplitude of $\sqrt{3} \times 1.15 \times 0.3 \times 43 \approx 26$ V, which clearly is lower than the applied source voltage, and is approximately 5 times smaller than that calculated for Fig. 3-17. The smaller ac voltage also gives rise to a smaller ac current, where the factor of reduction is again 5, as reflected by the third traces in Fig. 3-17 and Fig. 3-18. (Note that the filtered ac voltage is not shown here since its wave-shape is expected to be the same as the line current because of the linear load used). Other than the decrease in amplitude, no other difference is noted for the waveforms in Fig. 3-18 since the designed modulation schemes are expected to produce the same high waveform quality (except with variable amplitude) under all modulation conditions.

With the DSP card reprogrammed for testing the modulation scheme with minimal commutation count (see Section 3.4.2.2), Fig. 3-19 and Fig. 3-20 show the waveforms probed from the Ćuk-derived inverter with $\{M = 0.7, k = 0.4\}$ and $\{M = 0.3, k = -0.4\}$ respectively (see Section 3.4.2.2 for explanation on why k can be set negative). These modulation parameters are chosen because they give rise to the same SW = ON durations and device voltage stresses as those respectively found in Fig. 3-17 and Fig. 3-18. That explicitly explains the same pulse heights observed for the two sets of results corresponding to the two different modulation schemes. Despite this similarity in voltage gain, the latter scheme is observed to have a thicker ripple band imposed on the inverter current waveform (see third traces in Fig. 3-17 to Fig. 3-20), which indeed represents the tradeoff predicted earlier in Section 3.4.2.2 for gaining the advantage of a lower commutation count. This poorer performance feature is also noted in Fig. 3-21, where the spectra of the optimal harmonic and minimal commutation schemes when producing the same output amplitude are placed together for comparison. Quite clearly, harmonic energy of the former is pushed to the second carrier sideband and above,

Fig. 3-19. Experimental waveforms of Ćuk-derived diode-assisted inverter with $M = 0.7$ and $k = 0.4$, controlled using modulation scheme with minimized commutation count.

Fig. 3-20. Experimental waveforms of Ćuk-derived diode-assisted inverter with $M = 0.3$ and $k = -0.4$, controlled using modulation scheme with minimized commutation count.

while the latter has most of its harmonic energy concentrated within the first carrier sideband, which is then harder to filter, and explain the thicker current ripple observed for the minimal commutation scheme.

Proceeding on, the experimental setup was reconfigured as a SEPIC-derived diode-assisted inverter with its probed results shown from Fig. 3-22 to Fig. 3-25, using the same boost and buck modulation parameters as those used earlier for the Ćuk-derived variant. As deduced from (3.15) in comparison with (3.14), the SEPIC-derived inverter is expected to produce slightly lower dc-link voltage and ac current amplitudes, which clearly are reflected by comparing the relevant figures (e.g. compare Fig. 3-17 and Fig. 3-22). Comparing the figures also reveals that the current

ripples in Fig. 3-24 and Fig. 3-25 are larger than those in Fig. 3-22 and Fig. 3-23, which again are due to the tradeoff imposed by a lower commutation count, regardless of the topological arrangement used.

Fig. 3-21. Line voltage harmonic spectrum of Ćuk-derived diode-assisted inverter. TOP: optimized harmonic switching, $M = 0.7$ and $k = 0.7$; BOTTOM: minimal commutation switching, $M = 0.7$ and $k = 0.4$.

Fig. 3-22. Experimental waveforms of SEPIC-derived diode-assisted inverter with $M = 0.7$ and $k = 0.7$, controlled using modulation scheme with optimized harmonic performance.

Fig. 3-23. Experimental waveforms of SEPIC-derived diode-assisted inverter with $M = 0.3$ and $k = 0.3$, controlled using modulation scheme with optimized harmonic performance.

Fig. 3-24. Experimental waveforms of SEPIC-derived diode-assisted inverter with $M = 0.7$ and $k = 0.4$, controlled using modulation scheme with minimized commutation count.

Fig. 3-25. Experimental waveforms of SEPIC-derived diode-assisted inverter with $M = 0.3$ and $k = -0.4$, controlled using modulation scheme with minimized commutation count.

3.5 Summary

This chapter first describes the two-stage buck-boost power inversion concept by referring to the example of directly connecting a dc-dc boost converter to the front-end of a VSI. Drawbacks of this two-stage power inversion is discussed before proceeding on to review those more integrated, single-stage buck-boost topologies including the Z-source inverter, Ćuk- and SEPIC-derived inverters. As improvements to the latter two topologies, the chapter next presents the newly proposed diode-assisted Ćuk- and SEPIC-derived inverters, which are proven to produce a gain doubling effect by using a unique diode-capacitor network. In effect, the diode-capacitor network actively reconfigures itself to perform parallel capacitive charging and series discharging to give an immediate voltage multiplication factor of two when used with either the Ćuk- or SEPIC-derived topologies.

So far, the presented buck-boost concepts have only been tried with a simple two-level VSI. Extension to higher level inverters is still left unexplored, which can insightfully range from relatively simple for the two-stage solution to relatively complex for the single-stage solution especially when reduced component count feature is desired. This research topic is viewed as challenging, and is fortunately identified as the main theme of investigation for this thesis. Therefore, starting from the next chapter onwards, all the buck-boost concepts discussed in this chapter are extended, where possible, except the diode-assisted configurations. The reason for not including the diode-assisted configurations is that they are accidentally designed near the end of the project, after all the planned multilevel buck-boost inverters are developed. The diode-assisted configurations are however still included in the thesis to provide more information to the readers with its extension to multilevel inverters left for the investigation of a next investigator.

Chapter 4 Three-Level Z-Source NPC Inverters

Neutral-point-clamped inverters are known to be the preferred topology for medium voltage applications like ac motor drives [112]. Recently, an interest in using NPC inverters for low voltage applications has also been initiated with a thorough comparative evaluation presented in [5]. To design a NPC inverter with both voltage-buck and -boost capabilities, this chapter presents the careful integration of the Z-source topological concept [1, 100-109, 113] to the basic NPC inverter topology. In principle, the Z-source NPC inverter can be constructed by using either two Z-source networks or a single Z-source network, whose topological characteristics and operational principles are thoroughly presented as follows.

4.1 Z-Source NPC Inverter with Two Z-Source Networks

With appropriate modulation concepts incorporated, the designed Z-source NPC inverter would always operate with the minimum number of device commutations per half carrier cycle, and can selectively be configured to switch with minimal harmonic distortion (“Nearest Three Vectors” modulation principle) or completely eliminated common-mode voltage (due partially to its omission of dead-time delays from its switching state sequence). It is also shown in this section that the same generic set of carrier-based modulation expressions, earlier applied to a two-level Z-source inverter, can equally be used for controlling the Z-source NPC inverter with and without reduced common-mode switching. This surely is an important implementation advantage in terms of portability.

4.1.1 Topology of Z-Source NPC Inverter with Two Z-Source Networks

Fig. 2-1(a) shows the topology of a conventional three-level NPC inverter, whose three-phase output voltages are commonly represented on the two-dimensional space-vector diagram drawn in Fig. 4-1. For modulating the three-level NPC inverter,

Fig. 4-1. Vectorial representation of conventional NPC inverter.

it is convenient to perform “origin-shifting” and subsequently perform three-level modulation using two-level principles [86, 87, 114]. An example of the origin-shifting process is illustrated in Fig. 4-1 for $-30^\circ \leq \theta < 30^\circ$, where the origin is shifted from $(\{-1,-1,-1\}; \{0,0,0\}; \{1,1,1\})$ to $(\{0,-1,-1\}; \{1,0,0\})$ shown shaded in the figure. Inverter modulation can then be viewed as reproducing the effective reference phasor using “equivalent active” (E-active) and “equivalent null” (E-null) states that respectively form the vertices and center of the bolded two-level hexagon in Fig. 4-1 (by symmetry, six two-level hexagons can be drawn in total depending on the value of θ). Using the simplified representation, the reference phasor orientation in Fig. 4-1 can be reproduced by using the state sequence of E-null $\{0,-1,-1\} \rightarrow$ E-active $\{0,0,-1\} \rightarrow$ E-active $\{1,0,-1\} \rightarrow$ E-null $\{1,0,0\}$, which always produces a non-zero set of three-phase line voltages. Shoot-through states with the full dc link short-circuited are therefore not suitable for insertion into the NPC inverter state sequence, and a Z-source NPC inverter cannot simply be implemented by replacing the capacitor bank in Fig. 2-1(a) with a single Z-source impedance network.

As a feasible solution, Fig. 4-2 shows a Z-source NPC inverter with an upper and a lower Z-source network connected to its dc link and supplied by two isolated dc sources (e.g. fuel cells or photovoltaic cells). For the upper Z-source network, voltage boosting can be effected by turning ON (e.g.) switches SA1, SA2 and SA'1 with DA2

Fig. 4-2. Topology of Z-source NPC inverter with two Z-source networks.

forward-biased, while for the lower Z-source network, similar effect can be achieved by turning ON SA2, SA'1 and SA'2 with diode DA1 forward-biased. Some points to note with the voltage boosting process are that the two Z-source networks must not be boosted simultaneously to avoid short-circuiting the full dc link, which can degrade the harmonic performance, and they preferably should be boosted for equal time intervals to avoid dc voltage unbalance. In addition, the shoot-through states should be inserted immediately adjacent to instants of state transitions with the appropriate switches from Phase A, B or C turned ON to avoid unnecessary extra device switching (as explained in Section 3.2).

4.1.2 Modulation of Z-Source NPC Inverter with NTV Switching

It is well-known that NPC inverter modulation functions distinctly with five-level line voltage switching generated under high modulation condition and three-level switching generated under low modulation condition. Defining M as the fundamental ac voltage normalized with respect to $\hat{v}_{i(U)} (= \hat{v}_{i(G)})$, the maximum value of M is 1.15 and the transition between five-level and three-level line voltage switching occurs around $M = 0.575$. A thorough evaluation of NPC inverter modulation would therefore require considerations of both cases of $M \geq 0.575$ and $M < 0.575$, representing high and low modulation conditions respectively, as described below.

4.1.2.1 High Modulation Ratio ($M \geq 0.575$, Five-Level Line Voltage Switching)

(a)

(b)

Fig. 4-3. Modulation of conventional and Z-source NPC inverters when voltage reference phasor is in triangle 2a of the vector diagram in Fig. 4-1 (a) full carrier period and (b) zoomed-IN view of half carrier period.

Based on the criteria mentioned in Section 4.1.1, a fulfilling state sequence under high modulation condition is formulated and shown in Fig. 4-3(a) (state sequence for a conventional NPC inverter is also shown for comparison) for the case of reference phasor located in triangle 2a, where the first falling carrier edge transition is triggered by reference V_b and the last is triggered by V_c . Note in Fig. 4-3(a) and its zoomed view in Fig. 4-3(b) that no shoot-through state is inserted at the first falling edge transition from $\{0,-1,-1\}$ to $\{0,0,-1\}$ since the insertion of a lower Z-source shoot-through to the $-1 \rightarrow 0$ transition of Phase B (corresponding gating signals = $\{SB1,SB2,SB'1,SB'2\} = \{0,0,1,1\} \rightarrow \{0,1,1,1\} \rightarrow \{0,1,1,0\}$) would result in the outputs of Phases B and C shorted to zero (Phase A output remains at 0). The resulting intermediate state $\{0,0,0\}$ can neither be inserted to the left $\{0,-1,-1\}$ interval nor the right $\{0,0,-1\}$ interval, and is not one of the three nearest vectors when in triangle 2a. Therefore, a lower Z-source shoot-through state cannot be inserted at the first state transition (alternatively, an upper Z-source shoot-through can be inserted by turning ON SA1, SA2 and SA'1, but this would result in additional device commutations, and is therefore not recommended).

For the second falling edge transition from $\{0,0,-1\}$ to $\{1,0,-1\}$, an upper Z-source shoot-through, indicated as “U”, can be inserted to the $0 \rightarrow 1$ transition of Phase A by gating $\{SA1,SA2,SA'1,SA'2\} = \{0,1,1,0\} \rightarrow \{1,1,1,0\} \rightarrow \{1,1,0,0\}$ (also indicated in the lower half of Fig. 4-3(a)). Since only the upper Z-source is short-circuited, only Phase A output is shorted to zero with Phase B and C outputs maintained at their original values of 0 and -1, giving an intermediate state of U $\{0,0,-1\}$, which can be shifted into the E-active $\{0,0,-1\}$ interval towards the left of the second transition (see Fig. 4-3(a) and (b)). At first sight, this shoot-through insertion might not work well since the length of the E-active $\{0,0,-1\}$ state constantly varies as the reference phasor rotates, where a possible scenario is illustrated in Fig. 4-4, during which the E-active $\{0,0,-1\}$ interval is shortened to less than half the specified shoot-through duration of $T_0/2$. Interestingly, a closer examination of Fig. 4-4 reveals that the turning ON of SA1 earlier at instant $(t_{Ec2} - T_0/2)$ and turning OFF of SA'1 later at t_{Ec2} to create

Fig. 4-4. Illustration of state sequence when in triangle 2a and the shoot-through interval $T_0/2$ becomes longer than the E-active $\{0,0,-1\}$ interval.

an upper shoot-through state with $SA1 = SA2 = SA'1 = ON$ will still function well even when $SA1$ is turned ON earlier than the transition of Phase B at t_{Ec1} (which is the first transition for the case shown in Fig. 4-3(a)).

This finding is better explained by noting that although the advanced turning ON of $SA1$ causes the upper shoot-through state to overlap the E-null $\{0,-1,-1\}$ state by an interval of $\delta T_0/2$, no volt-sec error is introduced during that interval since Phase A is shorted to zero, while Phases B and C remain at -1 since the lower Z-source network is not shorted. The resulting intermediate state is therefore expressed as $U\{0,-1,-1\}$, which obviously resembles the E-null $\{0,-1,-1\}$ state during the $\delta T_0/2$ interval. For the remaining shoot-through interval of $(1-\delta)T_0/2$ after the transition of Phase B from -1 $\rightarrow$ 0 at t_{Ec1} , a second intermediate state of $U\{0,0,-1\}$ (Phase B now tied to 0) is assumed, which certainly can be used in place of the E-active $\{0,0,-1\}$ state, as per described above, until the shoot-through duration ends upon turning OFF $SA'1$. Given that both intermediate states respectively resemble the original E-null and E-active states, the inverter volt-sec average is expected to remain unaltered, proving that the above-described upper shoot-through insertion of $T_0/2$ at the second $\{0,0,-1\} \rightarrow \{1,0,-1\}$ transition will function well, even if the E-active $\{0,0,-1\}$ state shortens to zero as the reference phasor rotates in triangle 2a.

Applying the above-described analytical technique to the third $-1 \rightarrow 0$ transition of Phase C, a lower Z-source shoot-through state, indicated as “G”, can similarly be inserted to that transition, causing its output to short to zero with Phase A and B outputs maintained constant at 1 and 0. The resulting intermediate $G\{1,0,0\}$ state can then be shifted to the right of the third transition into the E-null $\{1,0,0\}$ interval, as indicated in Fig. 4-3(a). From the above discussion, a distinct feature noted about Z-source NPC modulation is that shoot-through states can be inserted within both E-active and E-null intervals, unlike in two-level case, where they can only be inserted within null intervals.

Similar analysis can be performed when the reference phasor is located in other triangles on the vector diagram with Fig. 4-5 showing the formulated state sequence when it is in triangle 3 under high modulation condition. In the figure, $U\{0,-1,-1\}$ and $G\{1,0,0\}$ shoot-through states are inserted to the left of the first falling edge transition into the E-null $\{0,-1,-1\}$ interval and right of the third transition into the E-null $\{1,0,0\}$ interval respectively. For the middle transition, a $G\{1,0,0\}$ shoot-through state can theoretically be inserted (see the zoomed view in Fig. 4-5(b)), and to avoid unbalanced Z-source boosting, re-equalization must be performed to make the total lower shoot-through duration equals the single upper shoot-through duration. However, from a practical viewpoint, this middle shoot-through state should be excluded from the inverter state sequence since it gives rise to a more complex modulator with decision-making logics needed for selecting the appropriate number of shoot-through states (two for triangles 1a and 2a, and three for triangle 3) and for re-equalizing the shoot-through durations depending on the triangle that the reference voltage phasor is in. Because of these additional complications with no obvious improvement in performance, the middle $G\{1,0,0\}$ shoot-through state is not implemented in this work.

(a)

(b)

Fig. 4-5. Modulation of conventional and Z-source NPC inverters when voltage reference phasor is in triangle 3 of the vector diagram in Fig. 4-1 (a) full carrier period and (b) zoomed-IN view of half carrier period.

For carrier-based implementation, a comparative evaluation of Fig. 4-3 and Fig. 4-5 would reveal that in general, $V_{mid} = V_b$ in those figures needs not be modified for inserting shoot-through state, while $V_{max} = V_a$ and $V_{min} = V_c$ must be respectively modified for inserting a shoot-through state to the left of a state transition (second transition in Fig. 4-3 and first transition in Fig. 4-5) and to the right of another transition (third transition in both figures). A review of (3.6) would reveal that by setting T_1 and T_2 to a constant T_0/T and 0 respectively, $V_{mid(SX)} = V_{mid(SX')} = V_{mid}$ insert no shoot-through state, while $V_{max(SX)}$ and $V_{max(SX')}$ always insert a shoot-through state to the left of a transition (see the lower half of Fig. 4-3 and Fig. 4-5 for Phase A gating signals), and $V_{min(SX)}$ and $V_{min(SX')}$ always insert a shoot-through state to the right of another transition. This finding is interesting as it implies that the same two-level formulation in (3.6) can be used for modulating a Z-source NPC inverter with the correct shoot-through states (upper or lower) and state transitions (first, second or third transition) selected automatically to always give six device commutations per half carrier cycle, similar to a conventional NPC inverter.

As an enhancement to the steady-state voltage gain, the maximum constant boost concept reported in [109] for two-level Z-source inverter control can directly be applied to the proposed three-level Z-source modulation scheme with virtually no modification needed. Following that approach, a third harmonic offset with 1/6 of the fundamental amplitude is added to the three-phase sinusoidal references shown in Fig. 4-3 and Fig. 4-5, to extend the modulation ratio to a maximum of $M = 1.15$, and to visually center the maximum and minimum reference envelopes vertically within the carrier band. With ΔV_U and ΔV_G in Fig. 4-3 and Fig. 4-5 now forced to be equal, and noting from [109] that the boosting ratio across switching cycles should preferably be kept constant to minimize the low-order current ripples flowing through the Z-source inductors, the maximum constant upper and lower shoot-through durations that can be added are expressed as (4.1), similar to that reported in [109] since the references used for modulation appear the same for both two-level and three-level cases with the only

difference noted being that the latter uses an additional triangular carrier.

$$\left(\frac{T_0}{2T}\right)_{\max} = 1 - \frac{\sqrt{3}M}{2} \quad (4.1)$$

Although using (4.1) gives rise to the maximum constant steady-state voltage gain, its accompanied minimization of null intervals can to some extent degrade the inverter transient performance, as discussed in [103], where it is proven that having a “cushioning” null interval can significantly reduce the inverter undesired non-minimum-phase response. A tradeoff thus exists between optimizing the inverter steady-state and transient responses, whose weights of importance generally depend on the specific industry applications under consideration. But as a generic guideline, the inserted shoot-through intervals should have a constant length across switching cycles to minimize low-order current ripples flowing through the Z-source inductors, which indeed is the approach taken in this chapter. (A difference noted when comparing the state sequence presented in [109] and those presented in this chapter is that the shoot-through states for the former are placed at the start and end of each switching cycle, while for the latter, they are placed adjacent to the E-active states. From past knowledge on PWM control [115], this minor difference in shoot-through placements is anticipated to cause only a slight high frequency spectral difference with no significant low-order harmonics introduced).

Another feature noted with the modulation scheme presented above is that each Z-source network is shorted for only half the total shoot-through duration of T_0 , unlike a two-level Z-source inverter whose single Z-source network is shorted for the full shoot-through duration. The boost factor B_{NTV} of the proposed Z-source NPC inverter is therefore re-expressed as $B_{NTV} = 1/(1 - T_0/T)$, but the maximum shoot-through duration of each Z-source network is still theoretically kept at $T_0/2T = 0.5$, similar to that of a two-level Z-source VSI. Now, substituting (4.1) into B_{NTV} , the semiconductor voltage stress V_s experienced by the Z-source NPC inverter is expressed as (4.2), which conceptually can be used as a brief guide for sizing the inverter. (Note that in

[109], the same expression is derived with V_{dc} representing the full dc input voltage across a two-level Z-source inverter, unlike in this work, where V_{dc} represents half the dc input voltage. In other words, if the same dc input voltage is applied to both inverters, switches in the Z-source NPC inverter are subjected to only half the dc stress, as anticipated).

$$V_s = B_{NTV} V_{dc} = \frac{V_{dc}}{\sqrt{3M-1}} \quad (4.2)$$

4.1.2.2 Low Modulation Ratio ($M < 0.575$, Three-Level Line Voltage Switching)

Under low modulation condition and when the reference phasor is in triangle 1a (see Fig. 4-6(a)), the generated state sequence in Fig. 4-6(b) is similar to that shown in Fig. 4-3(a) except that E-active{0,0,0} is used for low modulation ratio M , while

Fig. 4-6. Modulation of Z-source NPC inverter when voltage reference phasor is in triangle 1a of the vector diagram in Fig. 4-1 (a) vectorial representation and (b) zoomed-IN view of state sequence per half carrier period.

E-active $\{1,0,-1\}$ is used for high M . Using the same generic carrier-based scheme described in Subsection 4.1.2.1, an upper shoot-through state $U\{0,0,0\}$ to the left of the third transition in Fig. 4-6(b) and a lower shoot-through state $G\{0,0,0\}$ to the right of the second transition can similarly be inserted with the first transition left unaltered by references $V_{mid(SX)} = V_{mid(SX')} = V_{mid}$. (Alternatively, a lower shoot-through state $G\{0,0,0\}$ can be inserted to the first transition, as illustrated in Fig. 4-6(b), but this insertion is not recommended due to implementation difficulties discussed earlier when describing state sequences in Fig. 4-5).

A feature noted with this insertion is that all shoot-through states are inserted within the E-active $\{0,0,0\}$ interval only, whose duration increases as M approaches zero. The extent of dc link voltage $\hat{v}_i$ boosting therefore increases when M approaches zero, but the inverter ac output voltage $\hat{v}_X$ ($X = A, B$ or C) can still decrease towards zero since $\hat{v}_X$ is directly dependable on M , according to (3.5). The overall effect is a higher dc link voltage stressing the semiconductor switches with no accompanied increase in ac output voltage and a poorer waveform quality due to the degradation from five-level to three-level line voltage switching. With the above disadvantages and the fact that the same dc link boosting can be achieved with $M \geq 0.575$, the proposed Z-source inverter should preferably operate under high modulation condition when voltage boosting (output voltage greater than V_{dc} and with shoot-through states inserted) is commanded. On the other hand, if voltage-buck operation is desired, the shoot-through duration should be set to zero with the required output voltage amplitude (now always smaller than the input voltage V_{dc}) obtained by tuning M between 0 and 1.15.

4.1.3 Modulation of Z-Source NPC Inverter with RCM Switching

It was reported in [86] that by restricting the switching of a conventional NPC inverter to only the seven inverter states shown on the right vector diagram of Fig. 4-7(b), common-mode voltage can be nearly eliminated except for narrow voltage spikes

produced during the inverter dead-time delays. For Z-source NPC inverter, these common-mode spikes can be further attenuated since dead-time delays are not needed for inverter protection, but of course the complete elimination of common-mode voltage can only be guaranteed after careful analysis of the inverter state sequence is conducted.

To begin with, a brief comparison of the vector diagrams in Fig. 4-7 would reveal close similarities between the two-level (left) and RCM NPC (right) vectorial representations with neat state mapping. Tapping on these similarities, an efficient approach for controlling the Z-source NPC inverter with RCM switching is to first generate the appropriate two-level Z-source state sequence using (3.6), before logically mapping the obtained two-level sequence to correct gating signals for switching the Z-source NPC inverter. Following this approach, the two-level Z-source state sequence shown in the upper half of Fig. 4-8(a) can be logically mapped to the Z-source NPC sequence shown in the lower half of the same figure. Specifically, the non-shoot-through states ($\{0,0,0\}$; $\{1,0,0\}$; $\{1,1,0\}$; $\{1,1,1\}$) of the upper two-level sequence are digitally mapped to the lower non-shoot-through states ($\{0,0,0\}$; $\{1,0,-1\}$; $\{0,1,-1\}$; $\{0,0,0\}$) needed for RCM switching. The identified features in Fig. 4-8(a) are that only two shoot-through states (indicated as “Y”) are inserted to the first and third falling edge state transitions, and each shoot-through state involves the short-circuiting of both the upper and lower Z-source networks simultaneously, which can be explained by analyzing intermediate states generated during the shoot-through

Fig. 4-7. Two-level to three-level state mapping for Z-source NPC inverter modulation (a) two-level and (b) RCM three-level vector diagrams.

Fig. 4-8. Generation of Z-source NPC state sequence (a) direct logic mapping from two-level Z-source state sequence and (b) zoomed-IN view of Z-source NPC state sequence per half carrier period.

intervals.

Using the first $\{0,0,0\} \rightarrow \{1,0,-1\}$ transition as an example, an upper Z-source shoot-through can be inserted to the $0 \rightarrow 1$ transition of Phase A by gating $\{SA1, SA2, SA'1, SA'2\} = \{0,1,1,0\} \rightarrow \{1,1,1,0\} \rightarrow \{1,1,0,0\}$, and a lower Z-source shoot-through can simultaneously be inserted to the $0 \rightarrow -1$ transition of Phase C by gating $\{SC1, SC2, SC'1, SC'2\} = \{0,1,1,0\} \rightarrow \{0,1,1,1\} \rightarrow \{0,0,1,1\}$. This simultaneous insertion of upper and lower shoot-through states short-circuits the inverter dc link, causing its ac output to assume the intermediate state of Y $\{0,0,0\}$ (see the zoomed representation in Fig. 4-8(b)). The resulting Y $\{0,0,0\}$ state resembles the extreme left null $\{0,0,0\}$ state, and can therefore supplement it. Similar analysis can be performed on the third $\{0,1,-1\} \rightarrow \{0,0,0\}$ transition with the same Y $\{0,0,0\}$ state noted, but now this intermediate state is inserted to the extreme right null $\{0,0,0\}$ state.

For the second $\{1,0,-1\} \rightarrow \{0,1,-1\}$ transition, only an upper Z-source short-circuit can be inserted to the $1 \rightarrow 0$ transition of Phase A or $0 \rightarrow 1$ transition of Phase B (a lower Z-source shoot-through can be inserted but only with extra device commutations, and hence increased switching losses), and if inserted, it will short Phase A and B outputs to zero, while Phase C output remains at -1. The resulting intermediate state of $\{0,0,-1\}$ (see Fig. 4-8(b)) unfortunately is not one of the seven RCM switching states in Fig. 4-7, and therefore, shooting through the Z-source networks at the second transition is not desirable.

Another disadvantage associated with the middle shoot-through state is the overall reduction in voltage boosting when the middle state is inserted. This reduction can be explained by noting that the Z-source networks are boosted simultaneously only in the first and third shoot-through states with only one of the networks boosted in the middle shoot-through state (if inserted). On average, each Z-source network is therefore boosted for only $5/6$ of the full shoot-through duration T_0 , giving a boost factor of $B_{RCM1} = 1/(1 - 5T_0/3T)$ according to (3.4). Alternatively, with the middle shoot-through state omitted, each network is now boosted for the full T_0 , giving a boost factor of $B_{RCM2} = 1/(1 - 2T_0/T)$, which is the same as (3.4) and greater than B_{RCM1} .

Before ending this subsection, it is important to comment that the above-described RCM scheme can effectively eliminate the inverter generated common-mode voltage only if the reference grounding point shown in Fig. 4-2 is chosen. Unlike the conventional NPC inverter, where the shifting of grounding point to either the positive or negative dc rail simply introduces a dc offset to the common-mode voltage, the selection of a different grounding point for the Z-source NPC inverter, other than that shown in Fig. 4-2, will introduce an additional switched component (e.g. $v_{i(G)}$ if the inverter negative dc rail is chosen as the ground) to its common-mode voltage, which is not eliminated by the RCM scheme. Therefore, it is important to fix the grounding

point as shown in Fig. 4-2 with the two dc sources floated and isolated, if common-mode elimination using the presented RCM scheme is desired.

4.2 Z-Source NPC Inverter with Single Z-Source Network

Although theoretically feasible and with optimized switching pattern noted at its output, the inverter in Fig. 4-2 is not a favorable economical solution since it uses two isolated dc sources and a number of passive LC elements, which can significantly increase the cost, size and weight of the inverter. Therefore, instead of adopting the double-network circuitry directly without modification, alternative topological configurations that use only one impedance network would generally be preferred, judging from an economical viewpoint. However, noted from past developmental trends that by using a lower component count, performance degradations are usually unavoidable, inferring that a tradeoff exists, which must seriously be considered before deciding on the appropriate topology to adopt.

At first sight, the design of reduced element count (REC) three-level Z-source inverters might experience the same performance tradeoff, but through detailed operational analysis, it is shown in this subsection that REC inverters can indeed be designed with no degradation in performance. This unique complementary (rather than supplementary) behavior is attributed to the introduction of two new operating modes to the inverter modulation control, which has not yet been previously discussed. Therefore, when compared to the double-network Z-source inverter shown in Fig. 4-2, the designed REC inverters use only half the LC elements at a significantly reduced cost, but can produce the same output waveform quality, voltage transfer gain (when the same control parameters are used) and device switching frequency. The proposed optimally controlled REC inverters, with their performance and practicality, are therefore competitive buck-boost alternatives that can seriously be considered for industry applications (especially for renewable energy harnessing, where the input source voltage varies continuously).

Fig. 4-9. Topology of Z-source NPC inverter using only a single LC impedance network.

4.2.1 Topology and Operating Modes of REC Three-Level Z-Source NPC Inverter

Simplifying from the NPC topology shown in Fig. 4-2, Fig. 4-9 shows the first feasible REC Z-source inverter, where only a single Z-source impedance network, consisting of a split-inductor (L_1 and L_2) and two capacitors (C_1 and C_2), is connected between the input split-dc source (instead of two isolated sources) and a traditional NPC inverter circuitry. Intuitively, the rear-end NPC circuitry allows the inverter to assume three distinct voltage levels per phase-leg, whose expressions and corresponding gating signals are shown in Table 4-1.

Table 4-1. Example switching states of Z-source NPC inverter (ST $\equiv$ Shoot-Through).

State Type	ON Switches	ON Diodes	V_A
Non-ST	SA1, SA2	D1, D2	$+v_i/2$
Non-ST	SA2, SA'1	D1, D2, {DA1 or DA2}	0
Non-ST	SA'1, SA'2	D1, D2	$-v_i/2$
Full-ST (Not Preferred)	SA1, SA2, SA'1, SA'2	---	0
Full-ST (Preferred)	SA1, SA2, SA'1, SC2, SC'1, SC'2	DA2, DC1	0
Upper-ST	SA1, SA2, SA'1	DA2, D1	See (4.18)
Lower-ST	SA2, SA'1, SA'2	DA1, D2	See (4.19)

Inferring from the two-level Z-source energy conversion concept documented in [1, 100], boosting of voltages within the Z-source NPC inverter is effected by introducing full dc-link shoot-through states to its modulation state sequence, which otherwise, consists of only non-shoot-through active and null states commonly associated with a traditional NPC inverter. For distinctly representing the non-shoot-through and shoot-through states, Fig. 4-10 shows their simplified equivalent circuits for analysis, where in Fig. 4-10(a), the inverter circuitry and external load are represented by a simplified current source for representing the non-shoot-through condition. Using this equivalent representation with input diodes D1 and D2 conducting, the inductive voltage of the single symmetrical Z-source network ($\Rightarrow v_{L1} = v_{L2} = v_L$ and $V_{C1} = V_{C2} = V_C$) and the three distinct dc-link voltage levels ($v_{(+N)}, V_N, v_{(-N)}$) are respectively expressed as:

Fig. 4-10. Simplified representations of REC three-level Z-source inverters when in (a) non-shoot-through and (b) full dc-link shoot-through states.

$$v_L = 2V_{dc} - V_C \quad (4.3)$$

$$v_{(+N)} = +v_i/2; \quad V_N = 0V; \quad v_{(-N)} = -v_i/2; \quad v_i = 2(V_C - V_{dc}) \quad (4.4)$$

Alternatively, when a full dc-link shoot-through state is commanded by for example turning ON all switches {SA1, SA'1, SA2, SA'2} from phase A simultaneously to give the simplified circuit representation shown in Fig. 4-10(b) with input diodes D1 and D2 blocking, the relevant mathematical expressions are re-written as:

$$v_L = V_C \quad (4.5)$$

$$v_{(+N)} = V_N = v_{(-N)} = 0V \text{ since } v_i = 0V \quad (4.6)$$

Averaging v_L over a switching cycle T then gives:

$$V_C = \frac{2V_{dc}(1 - T_0/T)}{1 - 2T_0/T} \quad (4.7)$$

where T_0 represents the shoot-through duration. Using (4.7), the peak inverter dc-link voltage $\hat{v}_i$, peak ac output voltage $\hat{v}_x$ ($x = A, B$ or C), and the three distinct voltage levels when in a non-shoot-through state are derived as:

$$\hat{v}_i = V_C - v_L = 2V_C - 2V_{dc} = \frac{2V_{dc}}{1 - 2T_0/T} \quad (4.8)$$

$$\hat{v}_x = M \hat{v}_i / 2 = \frac{MV_{dc}}{1 - 2T_0/T} = MBV_{dc} \quad (4.9)$$

$$v_{(+N)} = +\hat{v}_i/2; \quad V_N = 0V; \quad v_{(-N)} = -\hat{v}_i/2 \quad (4.10)$$

where M is the modulation ratio and $B = 1/(1 - 2T_0/T)$ is the boost factor, which preferably should be set to unity ($T_0/T = 0$) for voltage-buck operation and $B > 1$ for voltage-boost operation. (For voltage-buck operation, $\hat{v}_i = 2V_{dc}$ since $B = 1$, implying that the three distinct voltage levels that the inverter can assume are $+V_{dc}$, $0V$ and $-V_{dc}$, which in principle, are similar to those of a traditional three-level inverter).

Although the non-shoot-through and shoot-through states described above are sufficient for voltage boosting when used correctly, it would definitely be interesting to

Fig. 4-11. Simplified representations of REC three-level Z-source inverters when in (a) upper-shoot-through and (b) lower-shoot-through states.

explore whether alternative voltage-boosting states exist, which might be helpful for gaining other performance advantages. Indeed, due to the presence of an additional neutral-point N , the REC three-level Z-source inverter shown in Fig. 4-9 can assume two new operating modes that are not linked to the two-level Z-source inverter reported in Section 3.2, and therefore not yet explicitly identified in the literature. The new operating modes are represented in Fig. 4-11, where a common feature noted is the short-circuiting of either the upper or lower dc source through the single Z-source impedance network. Also unlike the full dc-link shoot-through state, where both input diodes D1 and D2 are reverse-biased, the new operating states result in only D2 blocking for the upper-shoot-through and only D1 blocking for the lower-shoot-through. Deducing from those equivalent circuits, the corresponding mathematical expressions for representing the two new operating states are written as:

Upper-Shoot-Through

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$$v_L = V_{dc} \quad (4.11)$$

$$v_{(+N)} = V_N = 0 \text{ V}; \quad v_{(-N)} = V_{dc} - V_C \quad (4.12)$$

Lower-Shoot-Through

$$v_L = V_{dc} \quad (4.13)$$

$$v_{(+N)} = -V_{dc} + V_C; \quad v_{(-N)} = V_N = 0 \text{ V} \quad (4.14)$$

If only the non-shoot-through state in Fig. 4-10(a) and the shoot-through operating modes in Fig. 4-11 are used for inverter operation, state-space averaging performed on v_L in (4.3), (4.11) and (4.13) gives rise to:

$$V_C = \frac{2V_{dc}(1 - T_0'/(2T))}{1 - T_0'/T} \quad (4.15)$$

where T_0' represents the common duration set for both upper and lower-shoot-through states needed for achieving balanced voltage-boosting. Substituting (4.15) into (4.4), (4.12) and (4.14), the peak dc-link voltage $\hat{v}_i$ and dc-rail potentials in the respective operating states are summarized as:

$$\hat{v}_i = \frac{2V_{dc}}{1 - T_0'/T} \quad (4.16)$$

Non-Shoot-Through

$$v_{(+N)} = +\hat{v}_i/2; \quad V_N = 0 \text{ V}; \quad v_{(-N)} = -\hat{v}_i/2 \quad (4.17)$$

Upper-Shoot-Through

$$v_{(+N)} = V_N = 0 \text{ V}; \quad v_{(-N)} = -V_{dc}/(1 - T_0'/T) = -\hat{v}_i/2 \quad (4.18)$$

Lower-Shoot-Through

$$v_{(+N)} = V_{dc}/(1 - T_0'/T) = \hat{v}_i/2; \quad v_{(-N)} = V_N = 0 \text{ V} \quad (4.19)$$

Comparing (4.16) and (4.8), it is noted that the same peak dc-link voltage can be obtained by setting $T_0' = 2T_0$, where the maximum values for T_0' and T_0 are T and $0.5T$ respectively. Also, by comparing (4.17) and (4.19), an interesting feature distinctly

noted is that the lower dc-rail voltage $v_{(-N)}$ remains unaltered when transiting from a non-shoot-through to an upper-shoot-through state. Similarly, transiting from a non-shoot-through to a lower-shoot-through state will not affect the upper dc-rail voltage $v_{(+M)}$. Therefore, for the two phases connected to either the neutral point or the dc-rail not shorted by the third phase, their potentials remain unaffected, which happens to be an important feature needed for optimal modulation scheme development, as discussed in the next subsection.

4.2.2 Modulation Scheme Development

While inserting full dc-link or a balanced combination of upper and lower-shoot-through states to the inverter state sequence, it is important to ensure that the correct normalized volt-sec average is preserved at all instances, regardless of the reference phasor position on the three-level vector diagram shown in Fig. 4-1. With this criterion in view, two possible modulation techniques are proposed in the following subsections with their advantages and disadvantages discussed in details.

4.2.2.1 Alternative Phase Opposition Disposition Scheme

As known from past literatures, a method for controlling the traditional NPC inverter is to use two vertically disposed, 180° phase-shifted triangular carriers for comparison with a set of normalized three-phase sinusoidal references (labeled as V_x , $x = a, b$ or c), to produce two independent gating signals per phase (e.g. SA1 and SA2 in Fig. 4-9 with their logically NOT signals used for driving SA'1 and SA'2). This style of carrier arrangement is commonly referred to as the alternative phase opposition disposition scheme with a typical state sequence produced by it shown in the upper half of Fig. 4-12. (Noted that in that figure, a triplen offset, defined as $V_{off} = -0.5(\max(V_x) + \min(V_x))$, is intentionally added to the sinusoidal references to gain an important switching advantage, whose details are described later).

Fig. 4-12. APOD modulation of traditional and REC three-level Z-source inverters.

Certainly, the illustrated traditional sequence in Fig. 4-12 can be used for controlling the proposed REC three-level Z-source inverter, since it uses a NPC circuitry at its rear-end. However, that sequence will only give rise to voltage-buck operation with the voltage-boosting capability of the Z-source network left unexplored. To initiate this voltage-boosting ability, shoot-through states must appropriately be inserted to the inverter state sequence without altering its normalized volt-sec average appearing across the externally connected load. Based on this insertion principle and by referring to the traditional APOD state sequence shown in the upper half of Fig. 4-12, an immediate clue noted is that full dc-link shoot-through states should be used, rather than a combination of upper and lower-shoot-through states, and they should overlap the existing $\{0,0,0\}$ states placed at either the start or end of a half carrier cycle. The

reason for that is because both $\{0,0,0\}$ and full dc-link shoot-through states indistinctly produce a set of zero three-phase line voltages, hinting that they can replace each other for altering the inverter output gain, without introducing distortion to the external load.

Based on the above reasoning, a possible sequence for controlling the REC three-level Z-source inverter is shown in the lower half of Fig. 4-12, where full dc-link shoot-through states are inserted to the left (right) of the first $\{0,0,0\} \rightarrow \{1,0,-1\}$ (last $\{1,0,-1\} \rightarrow \{0,0,0\}$) transition of the falling (rising) upper carrier edge. Another feature noted in Fig. 4-12 is that the full dc-link shoot-through states are not inserted by turning ON all switches from the same phase-leg (see fourth row of Table 4-1). Rather, the shoot-through states are inserted by synchronizing the turning ON of switches from two naturally selected phase-legs (a process auto-built-in within the carrier-based modulator). For example, observing the gating signals shown in the lower half of Fig. 4-12, the first shoot-through state between states $\{0,0,0\}$ and $\{1,0,-1\}$ is initiated by the synchronized turning ON of switch SA1 from phase A and SC'2 from Phase C at time $(t_1 - T_0)$. Doing so creates a time interval during which switches $\{SA1, SA2, SA'1\}$ from phase A and $\{SC2, SC'1, SC'2\}$ from phase C are gated ON simultaneously to create the “bolded” short-circuited path shown in Fig. 4-13, where only conducting switches and diodes of the REC Z-source NPC inverter are shown.

Fig. 4-13. Intermediate shoot-through path of a REC Z-source NPC inverter with only conducting semiconductor devices shown.

This shoot-through of the Z-source impedance network only terminates at time t_1 , during which switch SA'1 from phase A and SC2 from phase C are turned OFF to initiate state $\{1,0,-1\}$. Similarly, the second shoot-through state added during the rising upper carrier edge is inserted by turning ON SA'1 and SC2 at time t_4 and turning OFF SA1 and SC'2 at a later time of $(t_4 + T_0)$, which again create an intermediate time interval during which $\{SA1, SA2, SA'1\}$ and $\{SC2, SC'1, SC'2\}$ are gated ON simultaneously. Using this approach, the visible advantage is that the number of device commutations needed for a switching cycle is the same as that needed by a traditional three-level inverter (minimum of six per half carrier cycle for continuous modulation), which is two less than that needed by the approach of turning ON all switches from a phase simultaneously (e.g. switching phase A from the positive dc rail $\rightarrow$ shoot-through $\rightarrow$ 0V would require $\{SA1, SA2, SA'1, SA'2\}$ to transit from $\{ON, ON, OFF, OFF\} \rightarrow \{ON, ON, ON, ON\} \rightarrow \{OFF, ON, ON, OFF\}$).

Given that now the four gating signals per phase-leg are not explicitly arranged as complementary pairs at all instances, they need to be controlled using two references per phase (instead of one) if the same APOD carrier set is used for comparison. Therefore, in total, three additional references are needed and their expressions can easily be formulated by first linearly converting the horizontal shoot-through time of T_0 to a normalized vertical offset of T_0/T (assuming a carrier peak of unity). The obtained vertical offset should then be added to the uppermost waveform of the original three-phase reference set (represented by $\max(V_x)$), where in the upper half of Fig. 4-12, it corresponds to V_a . The resulting two references used for controlling phase A are then written as $V_{a(SA)} = V_a + T_0/T$ and $V_{a(SA')} = V_a$, shown in the lower half of Fig. 4-12. Because both references are shown intersecting with the upper disposed carrier, their generated gating signals are used for driving SA1 and SA'1, also shown in the same figure. In particular, reference $V_{a(SA)}$ is used for turning SA1 ON at an earlier intersection time of $(t_1 - T_0)$, and $V_{a(SA')}$ is used for turning SA'1 OFF at a later intersection time of t_1 . This in turns creates an interval during which three switches

SA1, SA2 and SA'1 from phase A are ON.

Proceeding on using the same approach, but now with T_0/T subtracted from the lowermost waveform V_c shown in the upper half of Fig. 4-12, the derived references for controlling phase C are written as $V_{c(SC)} = V_c$ and $V_{c(SC')} = V_c - T_0/T$. Since both references cross the lower carrier, the produced gating signals are for switching SC2 and SC'2 respectively. Indeed, an interval, during which SC'1, SC2 and SC'2 are ON, is easily created by using $V_{c(SC')}$ to turn SC'2 ON at a time advance of T_0 , before using $V_{c(SC)}$ to turn SC2 OFF at a later instant. Moving forward to create a full dc-link short-circuit, a second offset $v_{off} = -0.5(\max(V_x) + \min(V_x))$ is added to the reference set to always center its maximal and minimal envelopes vertically within the full carrier band. That naturally aligns the intersecting points of the uppermost and lowermost references to always create a short-circuit interval, during which three switches from phase A and another three from phase C are turned ON simultaneously for voltage boosting.

Generalizing the above reference generation process to all sextants on the vector diagram, the generic rules for producing the six references are to add the vertical offset of T_0/T to the “maximum” reference $V_{\max}$, and subtract the same offset from the “minimum” reference $V_{\min}$, while keeping the “middle” reference V_{mid} unchanged. In equation form, these rules are summarized as (4.20), with their implementation giving rise to the voltage transfer gains expressed from (4.8) to (4.10), and the sequence shown in Fig. 4-12.

$$\left\{ \begin{array}{l} V_{\max(SX)} = V_{\max} + V_{off} + T_0/T \\ V_{\max(SX')} = V_{\max} + V_{off} \\ V_{\text{mid}(SX)} = V_{\text{mid}} + V_{off} \\ V_{\text{mid}(SX')} = V_{\text{mid}} + V_{off} \\ V_{\min(SX)} = V_{\min} + V_{off} \\ V_{\min(SX')} = V_{\min} + V_{off} - T_0/T \end{array} \right. \quad (4.20)$$

$X = A, B \text{ or } C$

4.2.2.2 Phase Disposition Scheme

An alternative shoot-through scheme that can be developed is based on the traditional phase disposition carrier-based approach, conventionally known to produce a lower harmonic content [82, 83, 115, 116]. For that approach, two vertically disposed in-phase carriers are used instead for comparison with the three-phase references to produce the typical state sequence shown in the upper half of Fig. 4-14, assuming that the reference phasor is in triangle 3 on the vector diagram in Fig. 4-1. An implication immediately noted from Fig. 4-14 is that $\{0,0,0\}$ state is no longer produced, hinting that the full dc-link shoot-through state might not be a favorable choice for insertion if the normalized volt-sec average is to be preserved. Therefore, for the PD case, inserting a combination of upper and lower-shoot-through states might be the only option left with its analysis presented as follow.

Fig. 4-14. PD modulation of traditional and REC three-level Z-source inverters.

Beginning with the traditional state sequence shown in the upper half of Fig. 4-14, an observation noted is the switching of phase A from 0V to the positive dc rail potential labeled as $v_{(+N)}$ to give the first state transition $\{0,-1,-1\} \rightarrow \{1,-1,-1\}$. During this transition, phases B and C remain clamped to the negative dc rail $v_{(-N)}$, and according to (4.18), they will stay unaltered even if an upper-shoot-through state is intentionally inserted by switching $\{SA1, SA2, SA'1, SA'2\}$ from $\{0,1,1,0\} \rightarrow \underline{\{1,1,1,0\}} \rightarrow \{1,1,0,0\}$ (underlined signals correspond to the inserted upper-shoot-through). The observed three-phase pole voltages during the upper-shoot-through interval therefore resemble those of state $\{0,-1,-1\}$, inferring that they can supplement each other for voltage-boosting without modifying the produced volt-sec average.

Applying the same analysis and moving on to the second transition ($\{1,-1,-1\} \rightarrow \{1,0,-1\}$), where phase B is triggered to switch from the negative dc rail to the neutral 0V potential, no shoot-through state should be inserted since its inclusion will cause either phase A or C to collapse to zero unintentionally, introducing volt-sec error in turns. Moving forward again to the third transition ($\{1,0,-1\} \rightarrow \{1,0,0\}$) initiated by raising the potential of phase C from $v_{(-N)}$ to 0V, inserting a lower-shoot-through state appears feasible since the gating of $\{SC1, SC2, SC'1, SC'2\}$ from $\{0,0,1,1\} \rightarrow \underline{\{0,1,1,1\}} \rightarrow \{0,1,1,0\}$ (underlined signals represent the inserted lower-shoot-through) will not affect phases A and B, which remain clamped to $v_{(+N)}$ and 0V respectively, according to (4.19). The resulting pole voltages therefore resemble those of $\{1,0,0\}$, inferring that both states are interchangeable for voltage gain tuning without introducing volt-sec distortion.

Based on the above reasoning, a modified state sequence that can be used for controlling the REC Z-source NPC inverter is shown in the lower half of Fig. 4-14, where an upper and a lower-shoot-through interval are inserted immediately to the left of the first transition and to the right of the third transition per half carrier cycle respectively. The reason for having adjacent placements is to again make use of the

time advance / delay technique for inserting shoot-through states without increasing the inverter commutation count. Specifically, for the example shown in Fig. 4-14, the first shoot-through state is inserted by using a modified reference $V_{a(SA)} = V_a + 0.5T_0'/T$ for turning SA1 ON at an earlier time of $(t_1' - 0.5T_0')$, and another reference $V_{a(SA')} = V_a$ for turning SA'1 OFF at a later time of t_1' (maximum envelope). Since SA2 is already ON within the illustrated carrier cycle, an interval with SA1 = SA2 = SA'1 = DA2 = ON is therefore created for shorting the upper dc source as intended, with the commutation count maintained at two (also reflected by the gating signals shown in Fig. 4-14). Similarly, by using $V_{c(SC)} = V_c$ to turn ON SC2 at t_3' and $V_{c(SC')} = V_c - 0.5T_0'/T$ to turn OFF SC'2 at $t_3' + 0.5T_0'$ (minimum envelope), an interval, during which SC2, SC'1, SC'2 and DC1 are ON, is created for shorting the lower dc source with the commutation count kept unchanged.

The same analysis, when applied to the second distinct triangle on the vector diagram for $0^\circ \leq \theta \leq 30^\circ$, will again validate the technique of adding $0.5T_0'/T$ to the maximum envelope and subtracting the same offset from the minimum envelope to always guarantee the correct insertion of shoot-through states. (Triangles 1a and 1b are not considered here since they are used mainly for low modulation condition, during which B is set to unity (no shoot-through state inserted) to avoid unnecessary stressing of the semiconductor devices, while producing a low output). Therefore, generalizing across the full fundamental cycle, the set of six modified references needed for PD shoot-through insertion is again given by (4.20), except for the replacement of T_0/T by $0.5T_0'/T$ in those expressions.

Note that although the triplen offset V_{off} is now not needed for aligning the commutations of phases A and C, as discussed previously for the APOD scheme, its inclusion is still needed for the PD scheme to maintain (e.g.) equal $\{0, -1, -1\}$ and $\{1, 0, 0\}$ intervals at the start and end of each half carrier cycle for inserting balanced upper and

lower-shoot-through states. Conceptually, balanced insertion is needed for undistorted voltage boosting, and is automatically guaranteed in all sextants on the vector diagram, so long as V_{off} is added to the set of modified references. (For knowledge sharing, it is highlighted here that balanced shoot-through insertion at both edges of a switching cycle is also encouraged in [109] for the reduction of network current ripple flowing through a two-level Z-source inverter. This reason is equally valid for the REC three-level Z-source inverter, but avoiding unbalanced voltage boosting is a more prominent concern here).

Besides the APOD and PD modulation schemes, the RCM modulation scheme can also be implemented in the Z-source NPC inverter with single Z-source network. Since for RCM modulation, the same modulation method can be assumed as that analyzed in subsection 4.1.3, therefore, the RCM modulation in the Z-source NPC inverter with single Z-source network would not be illustrated here again.

4.3 Simulation and Experimental Verification

4.3.1 Simulation and Experimental Results for the Z-Source NPC Inverter with Two Z-Source Networks

For verifying the PWM concepts presented, simulations were first performed in Matlab/Simulink before the optimized algorithms were confirmed experimentally using a Z-source NPC prototype. The hardware Z-source networks were implemented using 6.3 mH inductors and 2200 μ F capacitors found in the laboratory, and were powered by two isolated dc power supplies with V_{dc} set to 70 V (see Fig. 4-2 for the inverter topology). The conditioned dc link outputs of the Z-source networks ($\hat{v}_{i(u)} = \hat{v}_{i(o)} = \hat{v}_i$) were then connected to an existing three-phase NPC inverter for generating the required ac five-level line voltage waveform. The constructed Z-source system was controlled using a commercially available digital signal processor (DSP) and a digital erasable/complex programmable logic device (EPLD or CPLD), arranged

Fig. 4-15. Experimental implementation of Z-source NPC modulator.

as in Fig. 4-15. Specifically, the DSP was used for computing (4.20) and performing preliminary PWM comparisons, while the EPLD was used as an interface for mapping out the correct Z-source NPC gating signals (needed only for RCM PWM). The same setup was used for testing both the NTV (Subsection 4.1.2) and RCM (Subsection 4.1.3) algorithms with their captured results presented in the following subsections.

4.3.1.1 Simulated Results for NTV Algorithms

As a basis for comparison, Fig. 4-16 shows the inverter output waveforms when no shoot-through state is inserted to the NTV sequence. The inverter dc link voltage is obviously not boosted and maintained at 70 V (reflected by the pulse height of the phase-leg voltage) with a significant common-mode voltage generated. Now, with T_1 and T_2 programmed for inserting three shoot-through states (expressions for T_1 and T_2 are found in (3.6)), Fig. 4-17 shows the boosted inverter waveforms (dc link voltage

Fig. 4-16. Simulated (TOP to BOTTOM) Z-source NPC line voltage, phase-leg voltage, common-mode voltage and line currents with “nearest three vectors” switching, $M = 0.66$ and $T_0/2T = 0$ representing **no** shoot-through.

Fig. 4-17. Simulated (TOP to BOTTOM) Z-source NPC line voltage, phase-leg voltage, common-mode voltage and line currents with “nearest three vectors” switching, $M = 0.66$, $T_0/2T = 0.245$ and **three** shoot-through states inserted.

$\hat{v}_i = V_{dc} / (1 - T_0/T) = 137 \text{ V}$ since $T_0/2T = 0.245$) with an inferior line voltage switching and distorted line currents observed (note the different scales used in Fig. 4-16 and Fig. 4-17). Referring to Fig. 4-3(b), the distorted waveforms are caused by the erroneous intermediate state $G\{0,0,0\}$ introduced by the first shoot-through state at the $\{0,-1,-1\} \rightarrow \{0,0,-1\}$ transition. To be precise, the erroneous state causes a volt-sec error (and hence a distorted set of line currents) and the frequent dipping of inverter line voltage to zero around its fundamental peak, which indeed corresponds to the duration when the reference phasor is in triangles 2a and 2b, as predicted.

With T_1 and T_2 next set to T_0/T and 0 for inserting the correct two shoot-through states only, Fig. 4-18 shows the simulated output waveforms with $\hat{v}_i$ again boosted to 137 V. The line voltage waveform is now observed to switch neatly between adjacent voltage levels with a set of smooth line currents produced. This improvement in performance is of course achieved through the proper elimination of the unwanted shoot-through state (e.g.) from the $\{0,-1,-1\} \rightarrow \{0,0,-1\}$ transition in Fig. 4-3(b). The same “two shoot-through” technique can be applied under low modulation condition with Fig.

Fig. 4-18. Simulated (TOP to BOTTOM) Z-source NPC line voltage, phase-leg voltage, common-mode voltage and line currents with “nearest three vectors” switching, $M = 0.66$, $T_0/2T = 0.245$ and **two** shoot-through states inserted.

4-19 showing the same $\hat{v}_i$ boosting to 137 V, but as predicted, the obtained ac line currents are much lower than in Fig. 4-18 even though they have the same shoot-through duration T_0 (note the different scales used in Fig. 4-18 and Fig. 4-19 for the line current waveforms).

Fig. 4-19. Simulated (TOP to BOTTOM) Z-source NPC line voltage, phase-leg voltage, common-mode voltage and line currents with “nearest three vectors” switching, $M = 0.085$, $T_0/2T = 0.245$ and **two** shoot-through states inserted.

4.3.1.2 Simulated Results for RCM Algorithms

Providing a basis for comparison, Fig. 4-20 shows the waveforms obtained when no shoot-through state is inserted to the RCM sequence with $\hat{v}_i$ maintained at 70 V (reflected by the pulse height of the phase-leg voltage) and the common-mode voltage eliminated. With three shoot-through states inserted, Fig. 4-21 shows the dc link

Fig. 4-20. Simulated (TOP to BOTTOM) Z-source NPC line voltage, phase-leg voltage, common-mode voltage and line currents with reduced common-mode switching, $M = 0.66$ and $T_0/T = 0$ representing **no** shoot-through.

Fig. 4-21. Simulated (TOP to BOTTOM) Z-source NPC line voltage, phase-leg voltage, common-mode voltage and line currents with reduced common-mode switching, $M = 0.66$, $T_0/T = 0.245$ and **three** shoot-through states inserted.

Fig. 4-22. Simulated (TOP to BOTTOM) Z-source NPC line voltage, phase-leg voltage, common-mode voltage and line currents with reduced common-mode switching, $M = 0.66$, $T_0/T = 0.245$ and **two** shoot-through states inserted.

voltage boosted to $\hat{v}_i = V_{dc} / (1 - 5T_0/3T) = 118 \text{ V}$ (T_0/T set to 0.245), but now with a finite common-mode voltage generated. Referring to Fig. 4-8(b), the observed common-mode voltage is caused by the erroneous $Y\{0,0,-1\}$ state inserted at the middle $\{1,0,-1\} \rightarrow \{0,1,-1\}$ transition, and always has an amplitude of $1/3 \hat{v}_i$. With the erroneous state removed, Fig. 4-22 shows the simulated waveforms with only two shoot-through states inserted. As anticipated, the common-mode voltage is now completely eliminated and $\hat{v}_i = V_{dc} / (1 - 2T_0/T) = 137 \text{ V}$ (since $T_0/T = 0.245$), which is higher than that obtained using three shoot-through states (see Subsection 4.1.3 for an explanation).

4.3.1.3 Experimental Verification

The above subsections clearly identify algorithms with only two shoot-through states as the best PWM schemes. This finding is experimentally confirmed by the results presented from Fig. 4-23 to Fig. 4-26 with Fig. 4-23 and Fig. 4-25 providing a basis for comparison when no shoot-through state is inserted. Tuning the DSP controller to insert the correct two shoot-through states, Fig. 4-24 shows the boosting of $\hat{v}_i$ to $\approx 137 \text{ V}$ and the characteristic five-level line voltage switching of the presented NTV

scheme. Exhibiting equally good performance, Fig. 4-26 shows the same boosting of $\hat{v}_i$ to ≈ 137 V and the simultaneous elimination of common-mode voltage when the presented RCM scheme is used. These features are obviously unachievable with a conventional NPC inverter.

Fig. 4-23. Experimental (TOP to BOTTOM) Z-source NPC line voltage (200V/div), phase-leg voltage (120V/div), common-mode voltage (120V/div) and line current (3A/div) with “nearest three vectors” switching, $M = 0.66$ and $T_0/2T = 0$ representing **no** shoot-through.

Fig. 4-24. Experimental (TOP to BOTTOM) Z-source NPC line voltage (320V/div), phase-leg voltage (240V/div), common-mode voltage (240V/div) and line current (3A/div) with “nearest three vectors” switching, $M = 0.66$, $T_0/2T = 0.245$ and **two** shoot-through states inserted.

Fig. 4-25. Experimental (TOP to BOTTOM) Z-source NPC line voltage (200V/div), phase-leg voltage (120V/div), common-mode voltage (120V/div) and line current (3A/div) with reduced common-mode switching, $M = 0.66$ and $T_0/T = 0$ representing **no** shoot-through.

Fig. 4-26. Experimental (TOP to BOTTOM) Z-source NPC line voltage (320V/div), phase-leg voltage (240V/div), common-mode voltage (240V/div) and line current (3A/div) with reduced common-mode switching, $M = 0.66$, $T_0/T = 0.245$ and **two** shoot-through states inserted.

4.3.2 Experimental Results for the Z-Source NPC Inverter with Single Z-Source Network

The designed modulation schemes were tested experimentally using a REC Z-source NPC prototype, assembled with network parameters of $L = 6.3$ mH and $C = 2200$ μ F, readily found in the laboratory. The constructed inverter was next interfaced to a digital signal processor (DSP), to which, modulation codes were compiled and

downloaded. The generated gating signals with a switching frequency of 5 kHz were then sent to a gate driver board, whose outputs drove the inverter semiconductor switches directly.

Using this experimental setup, and with the modulation depth M and shoot-through time T_0/T set to 1.15 and 0 respectively, Fig. 4-27 shows the captured experimental results when a split-dc source of $2V_{dc} = 60V$ was used for powering the APOD-controlled REC inverter. As anticipated, the line voltage wave-shape does not switch between adjacent voltage levels (see central region in either the positive or negative cycle), which indeed is a characteristic feature of the APOD scheme. Also noted from the figure is that the current amplitude of approximately 1 A reflects the

Fig. 4-27. Experimental line voltage v_{AB} , phase voltage v_{AN} and line current i_A of APOD-controlled REC three-level Z-source inverter when $M = 1.15$ and $T_0/T = 0$.

Fig. 4-28. Experimental line voltage v_{AB} , phase voltage v_{AN} and line current i_A of APOD-controlled REC three-level Z-source inverter when $M = 0.7 \times 1.15$ and $T_0/T = 0.3$.

maximum current that can be obtained from a traditional three-level inverter when M is set to 1.15. Next with M decreases to 0.7×1.15 and T_0/T increases to 0.3, Fig. 4-28 shows the experimental waveforms, which clearly have a higher peak line voltage level of 150 V (implying that $2V_{dc} = 60\text{V}$ is boosted to $v_i = 2V_{dc}/(1-2T_0/T) = 150\text{V}$ in Fig. 4-9). In addition, the line current is now boosted to approximately 2 A, which is nearly two times that reflected in Fig. 4-27.

With the DSP reprogrammed to perform PD modulation, Fig. 4-29 shows the recaptured waveforms of the REC Z-source inverter with $M = 1.15$ and $T_0/T = 0$. As anticipated, that figure shows a peak line voltage pulse height of 60 V and a peak output current of 1 A since no voltage-boosting is commanded. But unlike the APOD

Fig. 4-29. Experimental line voltage v_{AB} , phase voltage v_{AN} and line current i_A of PD-controlled REC three-level Z-source inverter when $M = 1.15$ and $T_0/T = 0$.

Fig. 4-30. Experimental line voltage v_{AB} , phase voltage v_{AN} and line current i_A of PD-controlled REC three-level Z-source inverter when $M = 0.7 \times 1.15$ and $T_0/T = 0.3$.

scheme, the PD scheme always gives rise to adjacent level switching throughout the full fundamental cycle, which is known to produce a better spectral quality and hence a lower output current ripple (compare third traces in Fig. 4-27 and Fig. 4-29). Repeating the experiment with the control parameters retuned to $M = 0.7 \times 1.15$ and $T_0/T = 0.3$, Fig. 4-30 shows the corresponding waveforms, which clearly have a higher peak line voltage pulse height of ≈ 150 V and a boosted current peak of 2 A. While boosting the output quantities, the adjacent level switching characteristics is preserved, hence giving rise to a smaller current ripple in Fig. 4-30, as compared to that depicted in Fig. 4-28.

4.4 Summary

This chapter presents two newly proposed Z-source NPC inverters with their modulation principles carefully formulated for controlling the inverters with voltage buck-boost capability and always achieving the minimum number of device commutations per half carrier cycle. With an appropriate digital mapping logic added, the presented NPC inverters can switch with no common-mode voltage generated, due partially to its omission of dead-time delays from its switching state sequence. Through vectorial analysis, it is interestingly shown that the same (generic) carrier-based modulation expressions can be used for controlling both Z-source two-level and NPC inverters with and without RCM switching.

Moreover, it is shown in the chapter that the Z-source NPC inverter can function with reduced passive element count, without experiencing any drop in performance characteristics. This is because through analytical studies, it is proven that REC three-level inverters can freely assume three different shoot-through states, as compared to only one for the previously reported two-level Z-source inverter. This flexibility allows different combinations of shoot-through and non-shoot-through states to be formed, which in turns give rise to two different modulation schemes. The presented concepts have been verified in simulation and experimentally using the

constructed three-phase Z-source NPC prototypes.

Chapter 5 Three-Level Z-Source Inverters with Cascaded Connection

This chapter presents the development of two three-level Z-source inverters with cascaded connection, whose output voltage can be stepped down or up unlike a traditional buck three-level inverter. The proposed inverters are designed using two three-phase voltage-source inverter bridges, supplied by two uniquely designed Z-source impedance networks. These three-phase bridges can either be cascaded at their dc sides to form a Z-source dc-link-cascaded inverter or at their ac outputs using single-phase transformers to form a Z-source dual inverter. The dc-link-cascaded inverter has the advantages of not using any clamping diodes and transformers, but does not have redundant switching states within a phase-leg for equalizing switching losses among the power devices. This constraint limits the modulation options for the dc-link-cascaded inverter, and indeed, it can only be controlled using the modified carrier disposition technique with appropriate “Z-source shoot-through” states inserted for achieving balanced voltage boosting and optimal “nearest-three-vectors” switching.

On the other hand, the Z-source dual inverter with transformer isolation can be controlled using different modulation approaches due to the presence of redundant switching states within a phase-leg. Particularly, using a modified phase-shifted-carrier scheme with shoot-through states inserted, it is shown that the dual inverter can be implemented using only a single Z-source network, while still achieving the correct volt-sec average and switching loss equalization. This represents a significant reduction in cost, and can more than compensate for the slightly degraded spectral characteristics of the phase-shifted-carrier scheme. Modulation-wise, the dual inverter can also be controlled using a carefully designed carrier-based pulse-width modulation scheme that will always ensure balanced voltage boosting of the Z-source network, while simultaneously achieving reduced common-mode switching. Because of the

omission of dead-time delays in the dual inverter PWM scheme, its switched common-mode voltage can be completely eliminated, unlike in traditional inverters where narrow common-mode spikes are still generated.

5.1 Z-Source DC-Link-Cascaded Inverter

The Z-source dc-link-cascaded inverter is shown in Fig. 5-1, where two isolated power sources are connected through two Z-source impedance networks to a uniquely configured inverter circuitry. Obviously, this proposed inverter uses only twelve switches with no clamping diodes required unlike a Z-source NPC inverter. Its operational principles and modulation technique are now described in details before a thorough comparison with the Z-source NPC inverter can be pursued.

5.1.1 Principles of Operation

As illustrated in Fig. 5-1, the dc-link-cascaded inverter is configured such that the output terminals of the upper three-phase bridge are used as independent positive rails for the lower three-phase bridge. In addition, the negative dc rail of the upper Z-source network is linked to the positive rail of the lower Z-source network to form a common neutral point with a potential of 0V. Using this topological connection, the proposed

Fig. 5-1. Topology of Z-source dc-link-cascaded inverter.

Table 5-1. Switching states of Z-source DC-link-cascaded inverter ($X = A, B$ or C , and $V_{i(U)} = V_{i(G)} = V_i$).

State Type	ON Switches	Voltage
Non-Shoot-Through	$SX_{(U)}, SX_{(G)}, SW_{(U)}, SW_{(G)}$	$+V_i$
Non-Shoot-Through	$SX'_{(U)}, SX_{(G)}, SW_{(U)}, SW_{(G)}$	0
Non-Shoot-Through	$SX'_{(U)}, SX'_{(G)}, SW_{(U)}, SW_{(G)}$	$-V_i$
*Non-Shoot-Through	$SX_{(U)}, SX'_{(G)}, SW_{(U)}, SW_{(G)}$	$-V_i$
Upper Shoot-Through (U)	$SX_{(U)}, SX'_{(U)}$	0
Lower Shoot-Through (G)	$SX'_{(U)}, SX_{(G)}, SX'_{(G)}$	0

Z-source inverter can generate three distinct output voltage levels, as illustrated in Table 5-1, where the different switch combinations are grouped under shoot-through and non-shoot-through states.

During shoot-through, the inverter output voltage is boosted by either short-circuiting the upper or lower Z-source network (distinctly identified as “U” and “G” in Table 5-1) with the only limitation being that the boosting durations of the two networks must be equal to ensure balanced voltage boosting. Alternatively, shooting through of both Z-source networks simultaneously by turning ON all switches is possible, but modulation analysis presented in the next subsection would reveal that this state introduces a volt-sec error and therefore should be avoided. Another point to note while shooting through the Z-source networks is that the corresponding input switches $SW_{(U)}$ and $SW_{(G)}$ must be turned OFF appropriately to disconnect the dc sources from the Z-source networks during voltage boosting, as noted in [1, 100, 117] (for unidirectional operation, where only input diodes are used, the diodes will reverse-bias accordingly depending on which Z-source network is shorted).

The stored inductive energy during shoot-through can next be transferred to the ac load by transiting to any of the non-shoot-through states (see Table 5-1), where the switches now are grouped into two complementary pairs ($\{SX_{(U)}, SX'_{(U)}\}$ and $\{SX_{(G)}, SX'_{(G)}\}$) per phase. A feature noted with the non-shoot-through states is that the voltage level of $-V_i$ (assuming $V_{i(U)} = V_{i(G)} = V_i$) can be generated by two distinct switch combinations, but closer observation would reveal that for single step transition between 0V and $-V_i$,

transiting from $\{SX'_{(U)}, SX_{(G)}\}$ ON to $\{SX_{(U)}, SX'_{(G)}\}$ ON (indicated with an asterisk in Table 5-1) would give rise to two switch commutations, as compared to only a single commutation for all other state transitions. Therefore, to minimize switching losses, only the state with $\{SX'_{(U)}, SX'_{(G)}\}$ ON should be used for generating $-V_i$. In other words, no phase-leg redundancy is available within the dc-link-cascaded topology for equalizing losses among the semiconductor switches.

(a)

(b)

Fig. 5-2. Modulation of traditional and Z-source inverters when the reference phasor is in (a) triangle 3 and (b) triangle 2a on the three-level vector diagram shown in Fig. 5-3.

Another feature noted with the dc-link-cascaded topology is that when an output voltage of $+V_i$ is commanded, the blocking voltage across the reverse-biased switch $SX'_{(G)}$ (marked using a dashed circle in each phase in Fig. 5-1) is $+2V_i$, which is two times larger than those of the other switches. For implementing this lower switch $SX'_{(G)}$ per phase, either two switches connected in series or a single switch with double the blocking voltage of $2V_i$ (if available) can be used. If the former is selected, additional care must be devoted to the design of its gate-driving circuitry for ensuring that both series switches turn ON and OFF simultaneously to achieve balanced voltage sharing. Despite this additional constraint linked to $SX'_{(G)}$, the dc-link-cascaded inverter certainly has the advantage of using no clamping diode unlike the Z-source NPC inverter.

5.1.2 Modulation Development

Fig. 5-2(a) shows appropriate PWM sequences for modulating a traditional three-level and a dc-link-cascaded inverter when the reference phasor is in triangle 3 on the vector diagram shown in Fig. 5-3 (which is the same vector diagram as Fig. 4-1 illustrated here again for easily browsing). For both inverters, the Phase Disposition carrier arrangement is used, where the upper and lower carriers are in phase, and the gate pulses obtained from the reference and upper (lower) carrier comparison are used for

Fig. 5-3. Vector diagram of a three-level inverter.

driving switch $SX_{(U)}$ ($SX_{(G)}$). Generally, the PD approach is preferred for controlling three-level inverters with no redundant states (including the NPC and dc-link-cascaded inverters) since it always ensures that the nearest three vectors are used and therefore has a better performance, as compared to the alternative phase opposition disposition technique, where the two carriers are phase-shifted by 180° . For the PD method, it is also convenient to view inverter modulation as reproducing the effective reference phasor drawn in the bold hexagon on the vector diagram in Fig. 5-3, with its origin and vertices representing “equivalent null” and “equivalent active” states respectively. Using this representation, three-level modulation is explicitly simplified to a two-level modulation problem that can readily be solved using the rich pool of existing two-level PWM knowledge.

Comparing the sequences shown in Fig. 5-2(a), it is noted that the only difference between them is the insertion of an upper and a lower Z-source shoot-through to the left of E-active state $\{1,-1,-1\}$ and right of E-active state $\{1,0,-1\}$ respectively within each half carrier period. Insertion of shoot-through states at these instants will not result in additional switching since (for example) the transition from $\{0,-1,-1\}$ to $\{1,-1,-1\}$ can be progressed by turning ON $SA_{(U)}$ at an advanced time of $t_{EC1} - T_0/2T$, while the turning OFF of $SA'_{(U)}$ occurs at the same time instant of t_{EC1} (see gate signals of phase A in Fig. 5-2(a)). Therefore, from $t_{EC1} - T_0/2T$ to t_{EC1} , a shoot-through of the upper Z-source network is introduced with both $SA_{(U)}$ and $SA'_{(U)}$ intentionally turned ON. Note that the inserted upper shoot-through “U” state appears similar to the E-null $\{0,-1,-1\}$ state since phase A is short-circuited while the other two phases remain unchanged at -1.

Similarly, a short interval for shooting through the lower Z-source network, with $SC'_{(U)}$, $SC_{(G)}$ and $SC'_{(G)}$ turned ON simultaneously, can be introduced by delaying the turning OFF of $SC'_{(G)}$ to $t_{EC3} + T_0/2T$ during the transition from $\{1,0,-1\}$ ($SC'_{(U)}$ and $SC'_{(G)}$ of phase C ON in this state) to $\{1,0,0\}$ ($SC'_{(U)}$ and $SC_{(G)}$ ON). The resulting “G” state then appears similar to the E-null $\{1,0,0\}$ state since phase C is shorted while the

other two phases remain unchanged. Inserting of “U” and “G” states within the E-null intervals with the E-active intervals kept constant would therefore ensure that the same normalized volt-sec average, as for traditional PWM, is applied across the external ac load. In view of this volt-sec constraint, it is commented that the simultaneous shooting through of both Z-source networks cannot be performed since it gives rise to an intermediate state of $\{0,0,0\}$ (all phases shorted), which would give rise to a volt-sec error when used.

With the above analytical procedure applied to another distinct triangle (triangle 2a), a second modified state sequence is derived and shown in Fig. 5-2(b), where it is noted that the upper Z-source shoot-through is inserted to the left of the middle $\{0,0,-1\} \rightarrow \{1,0,-1\}$ transition, unlike that when in triangle 3. This modified insertion is needed for ensuring that the same normalized volt-sec average is continuously preserved when the reference phasor rotates around the symmetrical vector diagram, comprising of triangles matching either triangle 3 or 2a in terms of modulation features. Note that for this work, triangles corresponding to a low modulation ratio (e.g. triangle 1a) are not considered because they cause the inverter to degenerate into three-level line voltage switching with no additional voltage boost produced.

Using carrier-based implementation, the time advance and delay described earlier can be commanded by using two additional modified references (for example, $V_{a(SA)}$ and $V_{c(SC')}$ in Fig. 5-2(a)) for turning ON $SA_{(U)}$ (from the phase with the maximum amplitude) earlier and turning OFF $SC'_{(G)}$ (from the phase with the minimum amplitude) later respectively. For the other switches, the original set of three-phase sinusoidal references is used for gating them without modification. Therefore, linearly mapping the horizontal time offset of $T_0/2T$ to vertical amplitude offset of T_0/T (note the factor of two introduced by this normalized mapping from a time range of $0 \leftrightarrow 1$ to an amplitude range of $-1 \leftrightarrow 1$), the resulting set of modified references for controlling the dc-link-cascaded Z-source inverter can be summarized as (4.20). The resulted references can also be used for the rising edge half carrier period, and is equally

applicable when the reference phasor rotates to other triangles on the three-level vector diagram.

Since the DC-link-cascaded inverter has the similar operational principles and can use the same modulation techniques as the NPC inverter, therefore, the DCLC inverter can also be designed to perform buck-boost operation with single Z-source network added between two dc sources and inverter circuitry, which can be controlled using PD or APOD modulation referring to the particular shoot-through operation of partial dc-link shoot-through and full dc-link shoot-through, respectively, as analyzed in Chapter 4. The detailed analysis for the DCLC inverter with single Z-source network would not be addressed in this thesis because it's quite similar to the analysis in subsection 4.2 and the above illustration for the topological and modulation development can cover the main issues appeared in the Z-source DCLC inverter.

5.2 Z-Source Dual Inverter

The second cascaded topology designed in this work is the Z-source dual inverter, whose circuitry is shown in Fig. 5-4(a). In that figure, two dc sources are again connected to the inverter circuitry through two Z-source impedance networks. Comparing with the dc-link-cascaded and NPC inverters, the dual inverter has some redundant states, and therefore additional modulation approaches can be used for controlling it with a better equalization of switching losses among the semiconductor devices achieved. The operational principles and modulation schemes for controlling the Z-source dual inverter are now described, as follows.

5.2.1 Principles of Operation

As its name implies, a Z-source dual inverter is implemented through the series connection of two three-phase Z-source bridges using three single-phase transformers, whose secondary terminals are wye-connected for supplying all generic three-phase loads with either three- or four-wire configuration. Unlike the traditional cascaded

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Fig. 5-4. Topologies of Z-source dual inverter with (a) two and (b) one Z-source network respectively.

H-bridge topology, the use of single-phase transformers at the ac side of the inverter allows only two Z-source networks to be used instead of three needed by a traditional cascaded configuration.

Within the dual inverter, each Z-source bridge is controlled to switch between shoot-through and non-shoot-through states with the former corresponding to the

Table 5-2. Switching states and switch combinations of Z-source dual inverter ($X = A, B$ or C , and $V_{I(U)} = V_{I(G)} = V_I$).

State Type	ON Switches	Voltage
Non-Shoot-Through	$SX_{(U)}, SX'_{(G)}, SW_{(U)}, SW_{(G)}$	$+V_i$
Non-Shoot-Through	$SX_{(U)}, SX_{(G)}, SW_{(U)}, SW_{(G)}$	0
Non-Shoot-Through	$SX'_{(U)}, SX'_{(G)}, SW_{(U)}, SW_{(G)}$	0
Non-Shoot-Through	$SX'_{(U)}, SX_{(G)}, SW_{(U)}, SW_{(G)}$	$-V_i$
Upper Shoot-Through (U)	$SX_{(U)}, SX'_{(U)}$	0
Lower Shoot-Through (G)	$SX_{(G)}, SX'_{(G)}$	0

short-circuiting of a phase-leg and the later corresponding to the eight switching states of a traditional VS inverter. Operating the bridges with an appropriate phase-shift then gives rise to three distinct voltage levels, as given in Table 5-2, together with the upper and lower Z-source shoot-through conditions. A feature noted from Table 5-2 is that the output voltage of zero can effectively be generated by two redundant switch combinations, which in turn can be used for equalizing switching losses among the semiconductor devices, and to achieve other advantages highlighted next while developing the appropriate PWM schemes.

5.2.2 Modulation Development

Fig. 5-5. Modulation of traditional and Z-source two-level inverters.

The Z-source dual inverter proposed in this section can also be controlled using the modified PD modulation scheme presented in subsection 5.1.2 with the only modification needed being that the reference and upper carrier comparison is used for modulating $SX_{(U)}$, while the reference and lower carrier comparison is used for gating $SX'_{(G)}$ (not $SX_{(G)}$). Unfortunately, using the PD scheme results in only one switch combination ($SX'_{(U)} = SX'_{(G)} = \text{OFF}$, third row in Table 5-2) being used for producing the 0V output. For a better utilization of the redundant switching states, the alternative Phase-Shifted-Carrier (PSC) modulation approach should be used although it has a poorer spectral performance, as compared to PD PWM [59].

In principle, the PSC modulation scheme controls the upper Z-source bridge using the same reference set expressed in (4.20) together with a common triangular carrier, as illustrated in Fig. 5-5 (the arrangement in Fig. 5-5 is previously used for two-level Z-source inverter control in Section 3.2). Using the same carrier, but now the negation of (4.20) as the references, another set of gate pulses can be mapped out for controlling the lower bridge. With this modulation approach, example cases showing the relative placements of the generated state sequences are given in Fig. 5-6(a) and (b) for $V_{off} = 0$ (no triplen offset added) and $V_{off} = -0.5(V_{max} + V_{min})$ (standard offset used for two-level centered space-vector-modulation) respectively.

A feature noted from the sequences in Fig. 5-6(b) is that their active intervals start and end at the same time instants of t_{Ec1} and t_{Ec3} respectively. Inserting of shoot-through states immediately to the left and right of their total active intervals then results in simultaneous boosting of the two Z-source bridges although they are shorted by different phase-legs (e.g. phase A of the upper bridge and phase C of the lower bridge at the first shoot-through instant in Fig. 5-6(b)). Simultaneous boosting, together with transformer isolation in this case, allows the Z-source dual inverter to be powered by a single Z-source impedance network, as illustrated in Fig. 5-4(b), with a significant saving in cost expected. The resulting inverter in fact resembles the parallel connection of three H-bridges to form a three-phase system, which fortunately is still capable of

Fig. 5-6. Phase Shifted Carrier state sequences with (a) $V_{off} = 0$ and (b) $V_{off} = -0.5(V_{max} + V_{min})$ for Z-source dual inverter.

producing the three distinct voltage levels of $+V_i$, $0V$ and $-V_i$ per phase-leg shown in Table 5-2, and is therefore included here for study as an alternative three-level Z-source inverter. Because of the topological merit gained in Fig. 5-4(b), the PSC modulation scheme with $V_{off} = -0.5(V_{max} + V_{min})$ is recommended for dual inverter control even though its spectral performance is slightly inferior, as compared to PD modulation.

Besides the PSC sequences shown in Fig. 5-6, an alternative method for implementing PSC PWM with only a single dc source is illustrated in Fig. 5-7. Intuitively, the sequences in Fig. 5-7 can be implemented using three sinusoidal references (per inverter bridge) for dividing the switching period among the different inverter switching states, and two linear lines, expressed as $V_{lin(U)} = 1 - T_0/T$ and $V_{lin(U)} = -1 + T_0/T$, for inserting shoot-through states when the triangular carrier is above (below) the upper (lower) line $V_{lin(U)}$ ($V_{lin(G)}$). An advantage noted for this method is that the inserted shoot-through states of the two inverter bridges are always aligned, allowing simultaneous boosting of the Z-source networks regardless of the triplen offset added.

Fig. 5-7. Alternative Phase Shifted Carrier state sequence with no restriction on V_{off} but requires two additional device commutations.

Unfortunately, it is expected to have higher switching losses since it requires two additional device commutations per half carrier cycle. In view of this disadvantage, the method presented in Fig. 5-6 is preferred.

5.3 Other Operating Concerns Demonstrated Using Z-Source Dual Inverters

Indeed, those topological and modulation principles discussed earlier are sufficient for proving the proper functioning of the two described Z-source inverters with a cascaded connection. It would however be more comprehensive if two more concerns are addressed in details. The first is linked to the inverter operation under low modulation conditions or with small inductances used for assembling the Z-source impedance networks, while the second is related to the possibility of operating the inverters with RCM switching. Both concerns are in fact associated with all Z-source inverters presented in this thesis with the former discussed here using the Z-source dual inverters since they offer an easier to understand platforms extended directly from those two-level operating concepts discussed in [2]. For the second, it has in fact already been addressed earlier for the Z-source NPC inverters, and is now reapplied to the Z-source dual inverters representing inverters with a cascaded connection described in this chapter. To be more specific, the Z-source dual inverters are chosen as examples here since they have more redundant states, and are therefore likely to be

more challenging to deal with.

5.3.1 Low Modulation Complications and Mitigation Techniques

Two-level Z-source VSI is first proposed in [1] with its operating modes broadly classified under shoot-through and non-shoot-through states, which are subsequently shown in [2] to be part of a larger pool of operating modes that can be assumed by a Z-source inverter with low Z-source inductance. To demonstrate the existence of additional operating modes, it is assumed that the inverter is initially in a non-shoot-through state with its dc input current expressed as $i_{dc} = i_{L1} + i_{C1} = i_{L1} + (i_{L2} - i_{in}) = 2i_L - i_{in} > 0$ (see Fig. 3-2 and assuming that $i_{L1} = i_{L2} = i_L$ for a symmetrical Z-source impedance network). With i_{dc} maintained above zero, input diode D continues to conduct until i_L falls towards $0.5i_{in}$, during which $i_{dc} = 0$ (implying $i_L = 0.5i_{in}$), and the diode stops conduction. The inverter then enters a new operating mode, which can give rise to non-linear voltage boost, distorted ac current and a more complex set of transfer gain equations [2]. In passing, it is commented that in [2], the new operating mode is further divided into two sub-modes depending on whether the inverter is in a null ($i_{in} = 0$) or active state ($i_{in} = i_{aX}$, $X = a, b$ or c in Fig. 3-2), but this distinction and other operating modes identified in [2] are not the theme of this subsection, and are therefore not further discussed here.

The new operating mode described above is obviously not solely linked to low inductance condition studied in [2], but can equally occur under low modulation and light load conditions during which the “ripple-to-average” ratio of i_L is high. To avoid entering this operating mode and its associated complications, the Z-source inductance must be large (implying that $i_L \approx I_L$, where I_L is the average inductive current) and M must satisfy a constraining inequality derived as (5.1) under the worst case operating condition.

$$\begin{cases} I_L \geq 0.5I_{in} \\ V_{dc}I_{dc} = V_{dc}I_L = 3\hat{v}_x I_o \cos \varphi / 2 \\ I_{in} = I_o \quad (\text{worst case condition}) \end{cases} \Rightarrow \frac{3V_o I_o \cos \varphi}{2V_{dc}} \geq \frac{1}{2} I_o; \quad M \geq \frac{2}{3 \cos \varphi} \quad (5.1)$$

where $\cos \varphi$ is the load power factor, $\hat{v}_x$ and I_o are the peak ac output voltage and current, and $M = \hat{v}_x / (V_{dc}/2)$ gives the modulation ratio under low output voltage condition without boosting (implying $V_i = V_{dc}$).

A feature noted with the Z-source networks used here, as compared to those in Section 3.2, is that the series input diode D used in Fig. 3-2 is now replaced by an insulated gate bipolar transistor (IGBT) with an anti-parallel diode (see $SW_{(U)}$ and $SW_{(G)}$ in Fig. 5-4). This replacement is required to provide for bi-directional power conversion, and more importantly, to avoid erroneous voltage boosting under low modulation and light load operating conditions, during which the input source becomes disconnected from the Z-source network if only a diode is used. With the controlled IGBT switch added, a slight hardware modification needed is to provide for a seventh gating signal for driving $SW_{(U)}$ (an eighth signal for $SW_{(G)}$ is also needed if two isolated sources are used as in Fig. 5-4(a)), in addition to the six independent signals needed for driving the twelve switches in the two full-bridges with RCM switching, adopted as an example (it is shown later that both full-bridges use the same signals in a rotated sequential manner, and therefore only six gating signals are needed for the resulting inverter).

This seventh gating signal can be generated using the simple logic structure shown in Fig. 5-8, where SX and SX' ($X = A, B$ or C) are the gating signals for controlling the upper and lower switches of each phase-leg in a full-bridge. In brief, when a phase-leg shoot-through is commanded (e.g. $SA = 1$, $SA' = 1$), a turn-OFF signal is automatically

Fig. 5-8. Logic for controlling $SW_{(U)}$ and $SW_{(G)}$ (see Fig. 5-4).

sent to $SW_{(U)}$ (and $SW_{(G)}$), whose anti-parallel diode naturally reverse-biased, to disconnect the dc source from the Z-source network. On the other hand, when in a non-shoot-through active or null state, an ON signal is sent to $SW_{(U)}$ (and $SW_{(G)}$) for connecting the source to the Z-source network. Together, these operating states result in voltage boosting with bi-directional power conversion ability.

Alternatively, if only unidirectional dc-ac operation is required, $SW_{(U)}$ (and $SW_{(G)}$) can be turned OFF permanently during voltage boosting (shoot-through states inserted) with only its anti-parallel diode now connected in series between the input source and Z-source network. This diode would then naturally reverse-bias in a shoot-through state, and start conducting immediately upon the re-entry into a non-shoot-through state. On the other hand, when voltage boosting is not required (no shoot-through state inserted), $SW_{(U)}$ can still remain OFF until a boundary limit below which unintended reverse-biasing of the anti-parallel diode of $SW_{(U)}$ occurs. Depending on whether one or two dc sources are used, this boundary limit assumes different expressions, which can conveniently be derived using the same mathematical procedure documented above.

Specifically, when a single dc source is used with its dc link powering six phase-legs (two for each phase) simultaneously as in Fig. 5-4(b), the inverter dc link current and peak ac output voltage under RCM switching are expressed as $i_{in} = i_{in1} + i_{in2} \leq 1.5I_o$ and $\hat{v}_x = (\sqrt{3}/2) * M * V_{dc}$ respectively, assuming that a 1:1 transformer is used. (Note that the factor of $(\sqrt{3}/2)$ in the expression of $\hat{v}_x$ is introduced by the three-level RCM PWM, as explained in [86, 87]). Using these operating expressions and the inequality of $I_L \geq 0.5I_{in}$, the boundary constraint that M must satisfy is derived as:

$$\frac{3\sqrt{3}}{2} M \cos \varphi \geq \frac{3}{2} \Rightarrow M \geq \frac{1}{\sqrt{3} \cos \varphi} \quad (5.2)$$

Alternatively, when two isolated sources are used as in Fig. 5-4(a), the two full bridges in the dual inverter virtually have no direct connection between their dc links, and

therefore, their dc link currents are expressed as $i_{in1} = i_{in2} = i_{in} \leq I_o$. In addition, with RCM switching, their peak output voltages are expressed as $(\sqrt{3}/2) * M * V_{dc}$. Noting also that the ac output power is now equally shared between the two full bridges and considering the constraining inequality of $I_L \geq 0.5I_{in}$, the boundary limit imposed on M with two isolated dc sources is derived as:

$$\frac{3\sqrt{3}}{4} M \cos \varphi \geq 1 \Rightarrow M \geq \frac{4}{3\sqrt{3} \cos \varphi} \quad (5.3)$$

5.3.2 Three-Level RCM Modulation

Fig. 5-9 shows the space vector diagrams of the two full-bridges in a Z-source dual inverter with each having six active states and two null states, labeled as SV0 to SV7 for inverter U and SV0' to SV7' for inverter G. With the two full-bridges working simultaneously, the resulting dual inverter can output 64 switching states, arranged into 19 space vectors, as shown in Fig. 5-10 (the vertices of the hexagon are labeled with the first number representing inverter U switching state and the second number representing inverter G switching state). Obviously, the 19 vectors form a three-level inverter vector diagram with numerous redundant states, which should be optimally used for equalizing voltage boosting and switching losses between the two full-bridges. Being a three-level inverter, it is also possible to restrict the dual inverter to switch only among the seven space vectors shown shaded in Fig. 5-11 so as to generate zero common-mode voltage. Note that in [86], this vector restriction has been used for

Fig. 5-9. Space vector diagrams of full-bridges in dual inverter.

Fig. 5-10. Combined space vector diagram of dual inverter.

controlling a conventional three-level NPC inverter, but it is subsequently discussed in [87] that common-mode spikes can still appear during dead-time intervals introduced for inverter protection. Fortunately, for the Z-source dual inverter, dead-time delays are not required, and therefore a more thorough elimination of common-mode voltage can be expected.

Another feature noted in Fig. 5-11 is that there are more redundant states associated with the seven permitted vectors (two for each vertex and eight at the origin), as compared to those of an NPC inverter. The presence of these redundant states allows the authors of [70] to classify them into two state-sequencing options using either states $\{13', 15', 35', 31', 51', 53', 11', 33', 55'\}$ or $\{64', 24', 26', 46', 42', 62', 22', 44', 66'\}$. These state-sequencing options result in zero alternating common-mode voltage at each of the two full bridges in addition to the elimination of overall common-mode voltage at the output terminal of the dual inverter. The combined effect is a further reduction of bearing and leakage currents induced through electrostatic coupling when the inverter is used for driving an open-end-winding induction motor. Although both techniques function well, they generally result in discontinuous PWM switching at one of the full bridges, which at most would result in a larger current

Fig. 5-11. Reduced common-mode voltage space vectors of dual inverter.

ripple at the inverter dc link when the dual inverter is powered by a single dc source (see Fig. 5-4(b)). On the other hand, when a second isolated source is added (see Fig. 5-4(a)), discontinuous switching would result in unbalanced voltage boosting across the two Z-source networks, giving rise to a distorted output and an incorrect voltage transfer gain.

For controlling the Z-source dual inverter in this work, an alternative carrier-based approach with continuous PWM switching and rotated sequential order is therefore recommended. For a simple illustration of the modulation principle, Fig. 5-12 shows a possible state combination (labeled as combination 1 in the figure) with two state sequences for controlling the two full-bridges in a Z-source dual inverter. Comparing the sequences, it is noted that the second sequence is derived from the first by logically shifting the state bits towards the LEFT. These bit-shifted sequences then result in a set of normalized inverter phase voltages V_{AN} , V_{BN} and V_{CN} , calculated (e.g.) as $V_{AN} = 1 - 0 = 1$, $V_{BN} = 0 - 1 = -1$ and $V_{CN} = 0 - 0 = 0$ for the first active states $\{100\}$ and $\{010\}$ in both sequences. Further calculating the common-mode voltage as $V_{cm} = (V_{AN} + V_{BN} + V_{CN})/3$ gives rise to a value of zero, implying a complete elimination of common-mode voltage. The same computation can be performed for the remaining switching states

Fig. 5-12. State combinations 1 and 2 for controlling Z-source dual inverter with three-level reduced common-mode switching.

with the same conclusion anticipated. Besides eliminating common-mode voltage, it is anticipated that the above-described bit-shifting process can spontaneously minimize high frequency zero-sequence current circulating between the two full-bridges. As mentioned in [118], high frequency current ripple will circulate around the inverter when one full-bridge is in null {111}, while the other is in null {000}. Fortunately, this scenario does not happen when the proposed bit-shifting scheme is used (see Fig. 5-12), and therefore, no high circulating current will flow.

Obviously, a second state combination can also be derived by shifting the state bits towards the RIGHT (labeled as combination 2 in Fig. 5-12). Performing these bit-shifting methods for a full fundamental cycle then gives rise to the complete list of state combinations shown in Table 5-3. Regardless of which combination is used, it is important to maintain equal total shoot-through durations per switching cycle in the two PWM sequences for controlling the two full-bridges so as to equalize the amount of voltage boosting between them.

Table 5-3. Reduced common-mode state sequences.

Vector	State Combination 1	State Combination 2
OS (1,-1,0)	13'	64'
OH (1,0,-1)	24'	15'
OJ (0,1,-1)	35'	26'
OL (-1,1,0)	46'	31'
ON (-1,0,1)	51'	42'
OQ (0,-1,1)	62'	53'
Origin	77', 88'	77', 88'

Fig. 5-13. State combinations for controlling Z-source dual inverter: (a) correct and (b) incorrect shoot-through state sizing.

In addition, each shoot-through state in both sequences must start and end at the same time instants so as to avoid imperfect common-mode cancellation when active states are assumed. For an illustration, Fig. 5-13(a) and (b) show examples of correct and incorrect shoot-through state sizing respectively. In Fig. 5-13(b), overlapping of shoot-through states in one sequence with active states in the other sequence is observed. This overlapping is expected to result in a finite common-mode voltage, an unwanted volt-sec error and unbalanced voltage boosting when two isolated dc sources

Fig. 5-14. Experimental line voltage ($v_{ab}=v_{an}-v_{bn}$), phase-leg voltage (v_{an}), common-mode voltage ($v_{cm}=(v_{an}+v_{bn}+v_{cn})/3$) and line current (i_{oa}) of Z-source dc-link-cascaded inverter in Fig. 5-1 with PD modulation, $M = 0.7$ and $T_0/T = 0$.

are used, as in Fig. 5-4(a). Equal sizing and precise timing of shoot-through intervals are therefore important, and can automatically be implemented by using a single standard VSI modulator for generating inverter U state sequences in Fig. 5-12 (for example), and subsequently using the LEFT or RIGHT bit-shifting technique described above for generating inverter G state sequences.

5.4 Simulation and Experimental Verification

5.4.1 Experimental Results for the Z-Source Inverter with Cascaded Connection

For verifying the Z-source topologies designed and modulation concepts presented, a laboratory prototype that can be configured as either a Z-source dc-link-cascaded or Z-source dual inverter was constructed for physical testing. In both cases, the Z-source networks were assembled using $L = 6.3$ mH and $C = 2200$ μ F, and the inverter was built using insulated gate bipolar transistor (IGBT from *SEMIKRON*) modules and diodes. The resulting system was powered from two (or one for PSC-modulated Z-source dual inverter) dc sources set at $V_{dc} = 30$ V each, and was controlled using a

Fig. 5-15. Experimental line voltage ($v_{ab}=v_{an}-v_{bn}$), phase-leg voltage (v_{an}), common-mode voltage ($v_{cm}=(v_{an}+v_{bn}+v_{cn})/3$) and line current (i_{oa}) of Z-source dc-link-cascaded inverter in Fig. 5-1 with PD modulation, $M = 0.7$ and $T_0/T = 0.3$.

digital signal processor (DSP) for performing the reference-carrier comparison using (4.20) with the appropriate carrier arrangement selected for PD and PSC PWM. The generated gating signals, besides used for driving the inverter, were also fed to a complex programmable logic device (CPLD) for mapping out the correct signals for gating $SW_{(U)}$ and $SW_{(G)}$ needed for bidirectional operation (see Fig. 5-1 and Fig. 5-4).

With the described laboratory prototype configured as a PD-modulated dc-link-cascaded inverter shown in Fig. 5-1, the captured experimental waveforms are shown in Fig. 5-14 and Fig. 5-15 for shoot-through durations of $T_0/T = 0$ and 0.3 respectively (modulation ratio M set to 0.7). Comparing the two figures, it is observed that the insertion of shoot-through states effectively boosts the dc voltage by 2.5 times ($= (1 - 2T_0/T)^{-1}$ as given in Section 3.2) from $V_{dc} = 30$ V to $V_{i(U)} = V_{i(G)} = V_i \approx 75$ V (reflected by the vertical height of the phase-leg voltage pulses). This boosting action is also reflected by an increase of current from 1.3 A (peak) in Fig. 5-14 to 3.3 A (peak) in Fig. 5-15, which again gives a boost ratio of 2.5. The same observations are noted when the PD modulation scheme with the same shoot-through interval of $T_0/T = 0.3$ is used for controlling the Z-source dual inverter shown in Fig. 5-4(a) with two dc sources and two Z-source networks. As illustrated in Fig. 5-16, neat characteristic

Fig. 5-16. Experimental line voltage ($v_{ab}=v_{an}-v_{bn}$), phase-leg voltage (v_{an}), common-mode voltage ($v_{cm}=(v_{an}+v_{bn}+v_{cn})/3$) and line current (i_{oa}) of Z-source dual inverter in Fig. 5-4(a) with PD modulation, $M = 0.7$ and $T_0/T = 0.3$.

single-step switching and common-mode voltage of $2V_i/3$ are again noted. (For T_0/T set to zero, the corresponding waveforms for the Z-source dual inverter in Fig. 5-4(a) are similar to those shown in Fig. 5-14, and are therefore not shown here without compromising the quality).

With the DSP reprogrammed to perform single-source PSC PWM, Fig. 5-17 and Fig.

Fig. 5-17. Experimental line voltage ($v_{ab}=v_{an}-v_{bn}$), phase-leg voltage (v_{an}), common-mode voltage ($v_{cm}=(v_{an}+v_{bn}+v_{cn})/3$) and line current (i_{oa}) of Z-source dual inverter in Fig. 5-4(b) with PSC modulation, $M = 0.7$ and $T_0/T = 0$.

Fig. 5-18. Experimental line voltage ($v_{ab}=v_{an}-v_{bn}$), phase-leg voltage (v_{an}), common-mode voltage ($v_{cm}=(v_{an}+v_{bn}+v_{cn})/3$) and line current (i_{oa}) of Z-source dual inverter in Fig. 5-4(b) with PSC modulation, $M = 0.7$ and $T_0/T = 0.3$.

5-18 show the corresponding waveforms produced by the dual inverter shown in Fig. 5-4(b) with only a single Z-source network, and using the same parametric values described earlier. Again, the same boosting effects are observed, but the inverter line voltage now does not switch between adjacent voltage levels because the three nearest space vectors are not used for reproducing the reference phasor, which unfortunately is a characteristic feature of PSC PWM, identified in [82, 83, 87]. The immediate effect of the non-adjacent level switching is a suboptimal spectral performance, which also is already confirmed in those references. The above-degraded performance is however more than compensated by the possibility of using fewer passive LC components and the possibility of generating a lower common-mode voltage of $V_i/3$ (the latter being a characteristic feature of PSC PWM).

5.4.2 Simulation and Experimental Results for the Z-Source Dual Inverter with RCM Switching

The designed Z-source dual inverter with three-level RCM switching is first verified in simulation using PSIM with Matlab/Simulink coupler. For verifying the Z-source dual inverter performance under light load condition, Fig. 5-19 and Fig. 5-20 show simulated results for a single-source inverter and a dual-source inverter respectively with $M = 0.4$, $T_0/T = 0$, $\cos\phi = 0.99$ and $V_{dc} = 30\text{V}$ (according to (5.2) and (5.3), boundary constraints for both inverters are given as $M \geq 0.58$ for the single-source case and $M \geq 0.78$ for the dual-source case). Clearly, with the proper control of switches $SW_{(U)}$ and $SW_{(G)}$ in Fig. 5-4, both inverter configurations function well with the correct volt-sec average generated and common-mode voltage eliminated. Next with a finite shoot-through interval added ($T_0/T = 0.3$ and $M = 0.7$), Fig. 5-21 and Fig. 5-22 show the boosting of inverter output voltage to a pulse height of $\approx 75\text{ V}$ from an input voltage of only 30 V , while still maintaining a zero common-mode voltage with no erroneous spikes (boost factor of $B = 75/30 = 2.5$, which agrees well with that calculated using (3.4) ($B = 1/(1-2*0.3) = 2.5$)).

The optimally tuned inverter design simulated above is next tested experimentally

Fig. 5-19. Simulated (TOP to BOTTOM) line voltage, phase voltage, common-mode voltage and line current of Z-source dual inverter with a single dc source, $T_0/T = 0$ and $M = 0.4$.

using a constructed laboratory prototype switched at 5 kHz. The prototype is assembled using Semikron IGBT modules (rated at 600 V, 50 A), Z-source parameters of $L_1 = L_2 = 6.3$ mH (rated at 10 A) and $C_1 = C_2 = 2200$ μ F (rated at 400 V), and is controlled digitally using a DSP with embedded PWM peripheral and an erasable programmable logic device. The assembled inverter is next connected to a star-connected RL load ($R = 15$ Ω , $L = 6.3$ mH), which is deemed appropriate since the theme of this subsection is simply to test the open-loop modulation concepts proposed for controlling the Z-source dual inverter.

With this arrangement, the inverter common-mode voltage is measured by probing the load star-point and the transformer secondary neutral, labeled as “N” in Fig. 5-4. Note that in practice, the load star-point might not be available, meaning that a better way of measuring the common-mode voltage is to simultaneously probe the three secondary voltages of the transformer (with respect to N), and then summing them to give a measure of the common-mode voltage. For this work, the latter approach is not adopted because of the limited number of scope channels available, and the intention of displaying four distinct waveforms in all figures included herein.

Fig. 5-20. Simulated (TOP to BOTTOM) line voltage, phase voltage, common-mode voltage and line current of Z-source dual inverter with two isolated dc sources, $T_0/T = 0$ and $M = 0.4$.

For demonstrating the inverter performance under the same low modulation condition simulated earlier ($M = 0.4$, $T_0/T = 0$ and $V_{dc} = 30\text{V}$), Fig. 5-23 and Fig. 5-24 show the corresponding experimental waveforms, which again show the proper functioning of the proposed dual inverter with zero common-mode voltage generated. Proceeding further to demonstrate its voltage boosting feature, Fig. 5-25 and Fig. 5-26 show the captured experimental waveforms with $T_0/T = 0.3$ and $M = 0.7$. These results again

Fig. 5-21. Simulated (TOP to BOTTOM) line voltage, phase voltage, common-mode voltage and line current of Z-source dual inverter with a single dc source, $T_0/T = 0.3$ and $M = 0.7$.

show the boosting of voltage by a factor of 2.5 with the inverter common-mode voltage kept at zero at all instants (measured value of ≈ 7 V and occasional short peaks in the figures can safely be ignored after taking the physical measurement noises into consideration).

Fig. 5-22. Simulated (TOP to BOTTOM) line voltage, phase voltage, common-mode voltage and line current of Z-source dual inverter with two isolated dc sources, $T_0/T = 0.3$ and $M = 0.7$.

Fig. 5-23. Experimental (TOP to BOTTOM) line voltage 100V/div, phase voltage 50V/div, common-mode voltage 20V/div and line current 1A/div of Z-source dual inverter with a single dc source, $T_0/T = 0$ and $M = 0.4$, time scale: 5ms/div.

Fig. 5-24. Experimental (TOP to BOTTOM) line voltage 100V/div, phase voltage 50V/div, common-mode voltage 20V/div and line current 1A/div of Z-source dual inverter with two isolated dc sources, $T_0/T = 0$ and $M = 0.4$, time scale: 5ms/div.

Fig. 5-25. Experimental (TOP to BOTTOM) line voltage 200V/div, phase voltage 100V/div, common-mode voltage 20V/div and line current 3A/div of Z-source dual inverter with a single dc source, $T_0/T = 0.3$ and $M = 0.7$, time scale: 5ms/div.

Fig. 5-26. Experimental (TOP to BOTTOM) line voltage 200V/div, phase voltage 100V/div, common-mode voltage 20V/div and line current 3A/div of Z-source dual inverter with two isolated dc sources, $T_0/T = 0.3$ and $M = 0.7$, time scale: 5ms/div.

Table 5-4. Feature summary of proposed three-level Z-source inverters.

Performance Feature	Neutral-Point-Clamped Z-Source	DC-Link-Cascaded Z-Source	Dual Z-Source	
No. of Switches	12	12	12	Common for Fig. 5-4(a) and (b)
No. of Clamping Diodes	6	0	0	
Transformer Isolation	No	No	Yes	
Max. Switch Blocking Voltage	V_i	$2V_i$	V_i	
Phase-Leg Redundancy	No	No	Yes	
Switching Loss Equalization	Poor	Poor	Good	
PWM Schemes	PD	PD	PD for Fig. 5-4(a) PSC for Fig. 5-4(b)	
Line Voltage Spectrum	Optimized	Optimized	Optimized (PD) Slightly Degraded (PSC)	
DC Link Voltage	Constant	Constant	Constant (PD) Varying (PSC)	
Phase-Leg Switching	Single-Step	Single-Step	Single-Step (PD) Multi-Step (PSC)	
No. of Z-Source Networks	1 or 2	1 or 2	2 (PD) 1 (PSC)	
Common-Mode Voltage	$2V_i/3$ (PD) 0 (RCM)	$2V_i/3$ (PD) 0 (RCM)	$2V_i/3$ (PD) $V_i/3$ (PSC) 0 (RCM)	

5.5 Summary

This chapter presents two three-level Z-source inverters, whose ac output voltages can be stepped down or up, as desired. Both inverters use two three-phase bridges, which can either be connected at their dc sides for forming the Z-source dc-link-cascaded inverter, or ac sides using single-phase transformers for forming the Z-source dual inverter. Control wise, the dc-link-cascaded inverter can be modulated using the modified PD PWM scheme like the Z-source NPC inverters analyzed in Chapter 4 because of its lack of redundant switching states, while the dual inverter can be controlled using both modified PD and PSC schemes. Using the PSC scheme, further analysis has revealed that with an appropriate triplen offset added, the resulting dual inverter can be powered using only a single Z-source impedance network to significantly minimize the system costs.

To expand their operating advantages further, the design of a Z-source dual inverter with three-level RCM switching and voltage buck-boost capability is also presented. With controlled switches added to the inverter source-ends, the proposed inverter can perform bidirectional power transfer and can operate well under both low and high voltage operating conditions. Control-wise, the inverter can be easily controlled using state sequences shifting with shoot-through states inserted. All findings presented in the chapter have been confirmed in simulation and experimentally using laboratory implemented prototypes, and all features identified for the presented inverters are summarized in Table 5-4 for easier reference by the readers.

Chapter 6 Three-Level Ćuk / SEPIC Buck-Boost Inverters

Proceeding on to further develop other three-level buck-boost concepts, this chapter presents the three-level Ćuk / SEPIC buck-boost inverters with dual topology, NPC topology and DCLC topology adopted, whose single-stage buck-boost operations are achieved practically by adding an appropriate voltage boost circuitry between the input dc source and the corresponding multilevel inverter circuitry. Assuming the specifically designed modulation schemes, the unique voltage boost circuitries are always intentionally assembled with minimal passive and active elements needed to perform three-level voltage buck-boost operation, meanwhile achieving satisfied ac output performance.

6.1 Buck-Boost Dual Inverter

The schematic of the proposed buck-boost dual inverter is shown in Fig. 6-1, where a single dc source is connected to the inverter circuitry through an active dc network. At

Fig. 6-1. Schematic of buck-boost dual inverter with a single dc source.

Table 6-1. Phase-leg switching states of buck-boost dual inverter ($X = A, B$ or C , and SC $\equiv$ short-circuit).

Output Voltage	ON Switches (dc-ac Inversion)	ON Switches (ac-dc rectification)
+	SX1, SX2', SW	SX1, SX2'
0	SX1, SX1', SW	SX1, SX1'
0	SX2, SX2', SW	SX2, SX2'
-	SX2, SX1', SW	SX2, SX1'
0 (SC)	Don't Care as long as SW = OFF	SX1, SX2 OR SX1', SX2'

the output of the dual inverter, three single-phase transformers are connected to form three ac output terminals $\{a, b, c\}$ and a neutral star-point N for powering all generic three- or four-wire loads connected in wye or delta. With this arrangement, the output of the inverter can switch between three distinct voltage levels per phase-leg, as demonstrated in Table 6-1. Combining all output voltage possibilities from the three phase-legs, a total of sixty-four switching states is identified, and collectively arranged as nineteen space vectors on the inverter vector diagram as shown in Fig. 5-10. In addition to the switching possibilities shown in Fig. 5-10, inverter short-circuit state can be assumed by turning OFF SW during dc-ac power inversion or turning ON two switches from any phase-leg simultaneously during ac-dc power rectification (see last row of Table 6-1). Alternatively, a SEPIC-derived voltage boost circuitry can also be assumed to perform the voltage boost operation replacing the currently used Ćuk-derived voltage boost circuitry. Since both voltage boost circuitries have the similar operational principles and modulation scheme in the presented buck-boost dual inverter, therefore, only the topology with Ćuk-derived front-end circuitry would be analyzed in this section.

As predicted, for buck-boost operation, the state sequence used for controlling the proposed dual inverter must again incorporate three types of switching states with the SW = OFF state observed to produce a set of zero line voltages (inverter short-circuit). This observation implies that the well-known “nearest-three-vectors” modulation concept with a low harmonic content cannot be used since it does not create ZLV

(a)

(b)

Fig. 6-2. State sequences for controlling buck-boost dual inverter (a) without and (b) with triplen offset added.

intervals for inserting the $SW = OFF$ states. Therefore, the alternative phase-shifted-carrier approach is studied to evaluate whether ZLV intervals are created even though it is known to produce a slightly poorer high frequency switching spectrum [119].

Using the PSC approach, the carrier-reference comparison shown in Fig. 3-9 is first used to produce an appropriate state sequence for controlling the upper VSI bridge (labeled as inverter 1 in Fig. 6-1) in the dual inverter, while the negation of the references in (3.10) and the same carrier are compared to produce another sequence for driving the lower VSI bridge (labeled as inverter 2). The generated sequences and resulting dual inverter output states obtained by subtracting the bridge sequences are shown in Fig. 6-2(a), where it is observed that both VSI bridges request for the $SW = OFF$ state at the same time instant and for the same duration. This is important because

the resulting dc-link short-circuit caused by (e.g.) inverter 1 (initiated by turning OFF SW) will then not affect the volt-sec average of inverter 2 connected to the same dc network. The combined dual inverter output then gives the correct volt-sec average with three-level switching and the appropriate SW = OFF intervals inserted for buck-boost control.

For comparison, another set of state sequences is shown in Fig. 6-2(b), where now a

Fig. 6-3. Topologies of Ćuk buck-boost (a) NPC inverter and (b) DCLC inverter with two additional dc-side switches.

triplen offset is added for centering the active states within the switching cycle. Adding the offset extends the inverter linear modulation range M by a factor of 1.15, but at the same time, it removes state $\{1,0,0\}$ from the resulting dual inverter state sequence. This removal of state causes the dual inverter to appear switching at a “visually” lower frequency because of the lesser number of state transitions per switching cycle, even though the VSI bridges are physically switching at the same frequency for both sequences in Fig. 6-2. Therefore, it is recommended that the triplen offset should only be added when M approaches k ($M \leq k$), and a yet higher M is desired.

6.2 Ćuk-Derived Buck-Boost NPC and DCLC Inverters

6.2.1 Topological Analysis and Modulation Scheme

6.2.1.1 Topological Structures and Operational Principles

Fig. 6-3 shows the topologies of the proposed buck-boost NPC and DCLC inverters, where a single voltage boosting circuitry, comprising one inductor (L), two capacitors (C_1 and C_2) and two dc-side switches (SW1 and SW2), is inserted between the single dc source with reversed polarity and a three-level inverter circuitry. Unlike the two-level case shown in Fig. 3-5, two capacitors are needed for the three-level case shown in Fig. 6-3, to create a third voltage level for inverter switching. Formation of this third voltage level is obvious upon considering the turning ON of the two common-collector switches SW1 and SW2 to affect the magnetic energy boosting of inductor L . Besides inductive boosting, the turning ON of switches also causes C_1 and C_2 to tie up immediately as a split dc-link capacitive bank for powering active and null states of the three-level inverter circuitry. (The three diode-clamped legs of the NPC inverter and the middle dc rail of the DCLC inverter are now tied to the neutral point N of the split capacitive arrangement).

Therefore, for a lower output harmonic content, C_1 and C_2 must be charged equally to maintain balanced upper and lower dc-rail voltages. For that, it can easily be achieved

by turning OFF SW1 and SW2 with the inverter phase-legs now shorted by the conduction of all anti-parallel diodes in the phase-legs. The resulting equivalent circuit is similar to that shown in Fig. 3-6 (b) with the only difference noted being that two capacitors are now located within the shorted path for charging by the inductive current i_L . Although for the proposed inverters, other states like {SW1 = ON & SW2 = OFF} and {SW1 = OFF & SW2 = ON} are also logically feasible, but for proper operation, they should generally be avoided, since the former does not introduce the necessary neutral point needed for three-level switching, while the latter leads to unbalanced charging of C_1 since i_L now bypasses C_2 . To be precise, keeping SW2 ON while SW1 is OFF causes i_L to flow pass the reverse-polarized dc source, SW2, DX1 (X = A, B and C), SX1 and C_1 for the NPC inverter, and the dc source, SX1', SX1 and C_1 for DCLC inverter. Both described paths exclude C_2 , meaning that C_2 will never be charged with its voltage expected to collapse to zero as time progresses.

Fig. 6-4. APOD modulation of buck-boost three-level inverter.

6.2.1.2 Modulation Scheme

Noted from the earlier subsection that during the $\{SW1 = SW2 = \text{OFF}\}$ interval, inductor current i_L will shoot through the rear-end inverter circuitry to give rise to a set of zero three-phase line voltages. Therefore, similar to the Ćuk-derived two-level inverter shown in Fig. 3-5, ZLV intervals must intentionally be included within the three-level inverter state sequence, which can then be freely divided between the null and $\{SW1 = SW2 = \text{OFF}\}$ states. For null, it includes the three redundant states labeled as $\{0, 0, 0\}$, $\{1, 1, 1\}$ and $\{-1, -1, -1\}$, shown in Fig. 4-1.

With this criterion in view, the widely adopted “Nearest Three Vectors” modulation scheme cannot be used as the preliminary base for development since it does not produce the desired ZLV intervals. Instead, the alternative phase opposition disposition scheme should be adopted as the developmental base since it produces ZLV intervals in every switching cycle. For clearer illustration, an example state sequence produced using the APOD scheme is illustrated in Fig. 6-4. As noted, three sinusoidal references $\{V_a, V_b, V_c\}$ and two vertically disposed carriers with a 180° phase-shift between them are first compared to divide the switching cycle into ZLV intervals and distinct active states. An additional linear reference of either V_u or V_d can then be used for dividing the ZLV intervals into either $\{SW1 = SW2 = \text{OFF}\}$ or null $\{0, 0, 0\}$ state, where the decisions to turn OFF SW1 and SW2 are enforced when either the upper carrier rises above V_u or lower carrier falls below V_d .

Based on the above description, it is relatively obvious that the same reference set listed in (3.10) can be used for controlling the proposed buck-boost three-level inverters without major modification needed. This similarity implies that most modern digital signal processors (DSPs) with PWM modulators embedded can also be used for controlling the proposed three-level inverters with ease, since only one additional linear reference and no external digital logic is needed (the latter is needed for the Ćuk-derived two-level inverter presented in Section 3.3). The similarity in reference

Fig. 6-5. Alternative topology of buck-boost DCLC inverter with only a single dc-switch.

requirements also infers that the proposed three-level inverters exhibit the same boost factor of $1/(1-k)$, similar to that of the Ćuk-derived two-level inverter expressed in (3.9). But of course, the proposed inverters exhibit a spectrally improved three-level output voltage waveform, which indeed is one of its unique advantages.

6.2.2 Topological Improvement with Reduced Component Count

From the above discussion, one important feature noted for proper operation of the proposed three-level inverters is the regulation of their current flow paths for charging the two dc capacitors equally. Following this criterion, an alternative DCLC topology with one lesser active switch can be derived, and is drawn in Fig. 6-5, where the switch SW2 is removed from the voltage boost circuitry and the middle dc-link is directly connected to the emitter of SW1.

To illustrate the operational principle of this topology and to determine whether modifications need to be imposed on its modulation scheme, the switching pattern of each IGBT must be analyzed carefully when in different switching states and during their transitions. Assuming initially that the same modulation principle described earlier for the two dc-switch variant is used for controlling the present simplified

DCLC inverter, the gate signals fed into SA1, SB1 and SC1 can then be similarly represented by the lower gate combination shown in Fig. 6-4. For active and null switching states imposed in that combination, no complication is expected since both correspond to the intentional turning ON of SW1 to charge inductor L , and to form the split capacitive bank with C_1 and C_2 in series for powering the rear-end three-level circuitry. But when transiting from a null $\{0, 0, 0\}$ state to the SW1 = OFF state (and vice versa), an unstable scenario can happen if the inverter switches are not coordinated appropriately. This can be explained by noting that when in a null $\{0, 0, 0\}$ state, $\{SA1', SB1', SC1'\}$ from the upper bridge and $\{SA2, SB2, SC2\}$ from the lower bridge are supposed to turn ON to allow the load current to free-wheel through the middle dc link. Assuming now that SW1 is commanded to turn OFF with the statuses of the other inverter switches kept unchanged, current i_L would then flow through the dc source $\rightarrow C_2 \rightarrow SX2' \rightarrow SX2 \rightarrow SX1' \rightarrow L$, as indicated by the dotted path shown in Fig. 6-5. Along this path, capacitor C_1 will never be charged, while C_2 will be overcharged, giving rise to a set of degraded two-level waveforms and possibly shortened lifetime of C_2 .

The above problem can be resolved by using simple logic and replacing the null $\{0, 0, 0\}$ state by its redundant $\{1, 1, 1\}$ state. The latter modification causes SA1', SB1' and SC1' to stay OFF, while keeping SA1, SB1 and SC1 ON during the null intervals, resulting in the new SA1, SB1 and SC1 gate patterns shown in the upper half of Fig. 6-4. (In the figure, only the three upper independent signals for SA1, SB1 and SC1 are shown because the lower signals for SA2, SB2 and SC2 are the same for both gate combinations illustrated). With this modification and upon turning SW1 OFF, the new current path is redrawn in Fig. 6-5 with i_L now flowing along the solid path, passing through the dc source $\rightarrow C_2 \rightarrow SX2' \rightarrow SX2 \rightarrow SX1 \rightarrow C_1 \rightarrow L$. Clearly, with the conduction of the anti-parallel diode of SX1, C_1 and C_2 are charged equally along the redrawn path, inferring that the problem identified earlier is resolved. In addition, it is noted that the load current now circulates through the upper dc rail instead of the middle dc rail, which of course changes the phase voltage waveform, but fortunately,

these changes are common among the phases, implying that the line voltage waveform remains unchanged.

Although the above proposed redundant null replacement can smoothly solve the problem of unbalanced capacitive charging, additional device commutations can result if only gate signals within the null intervals are changed from $SA1' = SB1' = SC1' = ON$ to $SA1 = SB1 = SC1 = ON$. To avoid these additional commutations, SC1 should intentionally be tied to ON even during the active intervals without modifying the switching states produced (active $\{1, 0, -1\}$ and $\{1, -1, -1\}$), as shown in Fig. 6-4. Counting the total commutation instances in Fig. 6-4 then reveals that the two gate combinations in the figure give rise to the same commutation count of six per half carrier cycle when respectively used for controlling the rear-end DCLC three-level topology. But for the single dc-switch front end shown in Fig. 6-5, one lesser commutation is expected at either the start or end of each full switching period because of the exclusion of SW2. The modified inverter with only a single dc switch is therefore a reasonably favorable variant for consideration since it saves an active switch and can give rise to a sizable drop in average switching loss for high frequency operation.

Although the component reduction technique has successfully been applied to the DCLC circuitry, its application to the Ćuk-derived NPC inverter is not feasible since omitting SW2 in Fig. 6-3(a) would mean that the diode-clamping branches of the inverter are now directly connected to the collector of SW1. With SW1 next turned OFF, clamping diode DX1 would naturally bypass capacitor C_2 along the inductive charging path, giving rise to the unbalanced charging of capacitors. (Alternatively, if the diode-clamping branches are connected to the emitter of SW1, and upon turning it OFF, DX2 would bypass C_1 , again giving rise to unbalanced charging). Therefore, for the NPC option, single dc-switch topology is not possible due to its inherent structural constraints.

Fig. 6-6. Topologies of SEPIC buck-boost (a) NPC inverter and (b) DCLC inverter with two additional dc-side switches.

6.3 SEPIC-Derived Buck-Boost NPC and DCLC Inverters

Besides the Ćuk-derived topologies, another set of buck-boost NPC and DCLC inverters that can be derived as anticipated are the alternative SEPIC buck-boost three-level inverters with totally different topological structures and operational principles presented as below.

6.3.1 Topological Analysis and Control Scheme

6.3.1.1 Topologies and Operational Principles

One problem for coupling single voltage boost circuitry with the rear-end three-level inverter circuitry in SEPIC-derived topologies is the formation of an appropriate neutral potential served for three-level switching. A possible solution for improving the SEPIC-derived circuitry analyzed in Section 3.3.2 is to link another capacitor C_2 to the negative dc rail of rear-end NPC or DCLC inverter whose clamping legs or middle dc rail will connect to the positive terminal of single input source through an active switch SW2 as shown in Fig. 6-6, where the same amount of passive and active elements are assumed as the corresponding Ćuk-derived topologies.

To fully investigate the operational characteristics of the proposed front-end circuit, ON and OFF states of SW1 and SW2 must be first analyzed carefully. In detail, when SW1 and SW2 turn OFF simultaneously, inductor current i_L flows through capacitor C_2 , SX2', SX1'/DX2, SX2/DX1, SX1 and C_1 for NPC topology in Fig. 6-6(a) or C_2 , SX2', SX2, SX1 and C_1 for DCLC topology in Fig. 6-6(b) to fully charge C_1 and C_2 . Alternatively, when SW1 and SW2 turn ON, i_L free-wheels through dc source and SW1, meanwhile capacitor C_1 , C_2 and dc source connect in series to power the rear-end inverter unlike the Ćuk-derived topologies. Besides these two state combinations, other remaining state combinations of SW1 and SW2 would induce the undesired operational performance. For example, as SW1 = OFF and SW2 = ON, i_L would flow through dc source, SW2, DX1, SX1 and C_1 for NPC inverter (or dc source, SW2, SX1', SX1 and C_1 for DCLC inverter), which never charges C_2 in this process causing the voltage of C_2 drops to zero as unwanted. Another combination of SW1 = ON and SW2 = OFF would degrade three-level switching to two-level switching because during which neutral point N is not completely available for three-level switching.

Because the single dc source gets involved in capacitor discharging process, hence the unsymmetrical placement between dc source and two capacitors (C_1 and C_2) results in

the unequal voltage dispatch on the capacitors whose voltage relationship is $V_{C1} = V_{dc} + V_{C2}$. The unequal capacitor voltages can be derived below according to the theory of constant average inductor current under steady state the same as that analyzed for SEPIC-derived two-level inverter.

$$\frac{V_{dc}}{L} \cdot kT = \frac{V_{C1} + V_{C2}}{L} \cdot (1-k)T; V_{C1} = V_{dc} + V_{C2} \Rightarrow V_{C1} = \frac{V_{dc}}{2(1-k)}; V_{C2} = \frac{2k-1}{2(1-k)} V_{dc} \quad (6.1)$$

Note that V_{C2} in (6.1) can theoretically be positive or negative depending on the value of conductive duty ratio k . But in practice when dc capacitors are used in the voltage boost circuitry, the generated negative value should be intentionally avoided for safe operation meaning that the designed SEPIC three-level inverter is only suitable for voltage boost operation, where k is always higher than 0.5. In contrast, when ac capacitors are assembled into the voltage boost circuitry, the constraint of only voltage boost operation can then be removed. For both cases, the resulting ac output voltage can be expressed as (3.9) either regardless of the voltage difference between capacitors.

6.3.1.2 Control Scheme

Because inductor current i_L would shoot through upper and lower dc rails during $SW1 = SW2 = \text{OFF}$ interval causing three zero line voltages, therefore, absolute null state ($\{0, 0, 0\}$, $\{1, 1, 1\}$ or $\{-1, -1, -1\}$ shown as the center states in Fig. 4-1) must be

Fig. 6-7. Modified buck-boost DCLC inverter with SEPIC-derived voltage boost circuitry.

intentionally involved in the switching sequence so that the $SW1 = SW2 = \text{OFF}$ interval can be easily inserted. For achieving such modulation in three-level inverter, alternative phase opposition disposition modulator with two triangular carriers disposed with a 180° phase-shift is adopted, where three sinusoidal references V_a , V_b and V_c can define the ZLV intervals at the beginning and end of each switching cycle being similar to the initial division between ZLV and active intervals illustrated for modulating Ćuk-derived topologies. Consequently, the SEPIC-derived topologies can assume the same modulation strategies reported in Subsection 6.2.1.2 without any modification needed for controlling its desired voltage buck-boost operation. The details of modulation scheme for SEPIC-derived topologies would therefore not be presented here.

6.3.2 Derivation for Reducing Active Switch

Comparing the SEPIC-derived voltage boost circuitry used in three-level inverter to that of the corresponding two-level inverter, it is observed that an additional dc side switch $SW2$ is added to regulate inductive current flow path which obviously introduces extra switching losses and complicates topological structure. To further simplify the voltage boost circuitry and reduce system cost, $SW2$ can be removed from the voltage boost circuitry in DCLC inverter but with a reconnection of the middle dc-link, as shown in Fig. 6-7. To verify the validity of modified topology, the operational analysis, especially the capacitor charging and discharging process, should be carefully analyzed again to discover its unique characteristics. In detail, upon $SW1$ turns ON, inductor current i_L flows through dc source with capacitors C_1 , C_2 and dc source in series powering the rear-end inverter circuitry which is similar to the performance during $SW1 = SW2 = \text{ON}$ interval analyzed in last subsection. If semiconductors in rear-end inverter are commanded with their original switching pattern developed from APOD modulation without any change, upon $SW1$ turns OFF, i_L would flow through C_2 , $SX2'$, $SX2$ and $SX1'$ in DCLC inverter because of the ON status of $SX1'$ during null interval $\{0, 0, 0\}$, causing V_{C1} drop to zero. Therefore, the switching pattern for rear-end DCLC inverter circuitry should be modified by changing

null state $\{0, 0, 0\}$ to its redundant state $\{1, 1, 1\}$ as the exemplified sequence in the upper half of Fig. 6-4 for analyzing the Ćuk-derived DCLC inverter with single dc-side switch. Doing so, the capacitor charging current i_L shoots through upper and lower dc rails because $SX1'$ is now forced to be OFF to block i_L and more importantly, $SW1 = \text{OFF}$ interval is intentionally inserted in null interval to maintain normalized volt-sec average unchanged, which is naturally in accordance with the switching modification. With this kind of modification, load currents are forced to circulate through the up dc rail instead of the middle dc rail during null intervals. In addition, the same modulation technique presented in Subsection 6.2.2 can be equally assumed for controlling the present inverter in Fig. 6-7.

One point should be mentioned is that the effort for simplifying SEPIC-derived voltage boost circuitry also cannot be equally implemented for the buck-boost NPC inverter because of the same reason analyzed for Ćuk-derived voltage boost circuitry in Subsection 6.2.2.

Examining the proposed topologies in Fig. 6-3, Fig. 6-5, Fig. 6-6 and Fig. 6-7, a common feature noted in the capacitor discharging process (where $SW1 = SW2 = \text{ON}$

Fig. 6-8. Simulated (TOP to BOTTOM) line voltage, phase-leg voltage, common-mode voltage and line current when controlled using phase-shifted carrier PWM with $M = 0.3$ and $k = 0.3$.

or $SW = ON$) is that the single inductor does not involve in the capacitor discharging path as intended because the involvement of inductor would change the original current flow in the dc side fed from load, which in turn influence the capacitive discharging process. Therefore, the above proposed topologies can be treated as the appropriate development for realizing three-level buck-boost switching without any component redundancy added.

6.4 Simulation and Experimental Verification

6.4.1 Simulation and Experimental Verification for Buck-Boost Dual Inverter

The proposed theoretical concepts for buck-boost dual inverter were firstly verified by coupling a PSIM-drawn dual inverter circuit to the Matlab/Simulink simulation platform with the dc input source set to $V_{dc} = 30$ V, and the control parameters set to $\{M = 0.3, k = 0.3\}$ for buck operation and $\{M = 0.7, k = 0.7\}$ for boost operation. Using these parameters, the simulated waveforms for PSC PWM are displayed in Fig. 6-8 and Fig. 6-9 respectively, where the ac output current of ≈ 4 A and switched

Fig. 6-9. Simulated (TOP to BOTTOM) line voltage, phase-leg voltage, common-mode voltage and line current when controlled using phase-shifted carrier PWM with $M = 0.7$ and $k = 0.7$.

voltage pulse height of ≈ 100 V (see the phase-leg voltage waveform) in Fig. 6-9 are clearly larger than those in Fig. 6-8 since larger control parameters are used for the former figure. These simulated plots are next verified experimentally by constructing a dual inverter prototype, whose component values and results are described in more details as follow.

Specifically, the prototype inverter was constructed using insulated gate bipolar

Fig. 6-10. Experimental (TOP to BOTTOM) line voltage, phase-leg voltage, common-mode voltage and line current when controlled using phase-shifted carrier PWM with $M = 0.3$ and $k = 0.3$.

Fig. 6-11. Experimental (TOP to BOTTOM) line voltage, phase-leg voltage, common-mode voltage and line current when controlled using phase-shifted carrier PWM with $M = 0.7$ and $k = 0.7$.

transistors, and its dc network was assembled using a 2 mH inductor and a 220 μ F capacitor. The inverter was powered from a single dc power source with V_{dc} set to 30 V, and its immediate dc link voltage was controlled freely by setting M and k in (3.10) using a DSP. Before feeding the DSP gating signals to the inverter, an EPLD was used to condition the signals and to generate appropriate signals for inserting multiple SW = OFF states.

Fig. 6-12. Simulated voltage and current waveforms of three-level DCLC inverter with two dc switches, $M=0.3*1.15$ and $k=0.3$.

Fig. 6-13. Simulated voltage and current waveforms of three-level DCLC inverter with two dc switches, $M=0.7*1.15$ and $k=0.7$.

For demonstrating the inverter buck-boost operation, Fig. 6-10 and Fig. 6-11 show the experimental waveforms captured when PSC PWM is used with its control parameters set to those previously simulated values of $\{M = 0.3, k = 0.3\}$ and $\{M = 0.7, k = 0.7\}$ respectively (the line voltage waveforms are slightly “rounded” because they are measured on the secondary sides of the transformers). Using these control parameters

Fig. 6-14. Simulated voltage and current waveforms of three-level DCLC inverter with a single dc switch, $M=0.3*1.15$ and $k=0.3$.

Fig. 6-15. Simulated voltage and current waveforms of three-level DCLC inverter with a single dc switch, $M=0.7*1.15$ and $k=0.7$.

Fig. 6-16. Experimental voltage and current waveforms of three-level NPC inverter with two dc switches, $M=0.3$ and $k=0.3$.

Fig. 6-17. Experimental voltage and current waveforms of three-level NPC inverter with two dc switches, $M=0.7$ and $k=0.7$.

and according to (3.8) and (3.9), the inverter dc link voltage and peak ac output voltage are expressed as:

- $V_{C1} = \frac{30}{1-0.3} = 42.9 \text{ V}$ and $\hat{v}_{x1} = \frac{0.3 \times 30}{1-0.3} = 12.9 \text{ V}$ for $M = 0.3$ and $k = 0.3$.
- $V_{C2} = \frac{30}{1-0.7} = 100 \text{ V}$ and $\hat{v}_{x2} = \frac{0.7 \times 30}{1-0.7} = 70 \text{ V}$ for $M = 0.7$ and $k = 0.7$.

Clearly, the calculated dc link values match those reflected by the phase-leg pulse heights in Fig. 6-10 and Fig. 6-11, and the calculated peak ac ratio of $\hat{v}_{x2}/\hat{v}_{x1} = 5.4$ also matches that reflected by the measured current peaks of $\approx 3\text{A}$ in Fig. 6-11 and $\approx 0.5\text{A}$ in Fig. 6-10 (giving a ratio of ≈ 6).

6.4.2 Simulation and Experimental Verification for Ćuk-Derived

Buck-Boost NPC and DCLC Inverters

The proposed buck-boost three-level inverters were first verified in Matlab/PLECS simulation before testing them experimentally using a laboratory prototype, interfaced to the designed APOD modulator. For consistency, parameters used for the simulation were similar to those adopted for the experimental system, where $C_1 = C_2 = 220\mu\text{F}$ and $L = 2\text{mH}$ were used for the dc network with its input source voltage set as 80V. Using the same experimental setup, both the NPC and DCLC topologies were tested, but only results for the DCLC inverters are shown without degrading the verification quality since waveforms for both configurations are relatively similar.

With the above settings, Fig. 6-12 and Fig. 6-13 show the simulated waveforms of the

Fig. 6-18. Experimental voltage and current waveforms of three-level DCLC inverter with a single dc switch, $M=0.3$ and $k=0.3$.

Fig. 6-19. Experimental voltage and current waveforms of three-level DCLC inverter with a single dc switch, $M=0.7$ and $k=0.7$.

buck-boost three-level inverter with two dc switches and the control parameters set to $\{M = 0.3 \times 1.15, k = 0.3\}$ and $\{M = 0.7 \times 1.15, k = 0.7\}$ respectively (the factor of 1.15 is introduced by the added triplen offset). Clearly, in Fig. 6-12, the dc input voltage of 80V is boosted to a total dc-link voltage of 114V (reflected by the line voltage highest pulse height), which matches well with the calculated boost factor of $1/(1-0.3)$ using (3.8). With k increases to 0.7, Fig. 6-13 shows an even larger boosting gain with the input voltage now boosted to a dc-link voltage of 267V, which again agrees well with the theoretically calculated value of $1/(1-0.7)$. Using (3.8) to determine the ac-side response for the two defined conditions also reveals that an ac gain factor of 5 exists between the two figures, which physically is reflected by the approximately 1A and 5A currents in Fig. 6-12 and Fig. 6-13 respectively.

Next, using the proposed inverter with only a single dc switch, Fig. 6-14 and Fig. 6-15 show the simulated waveforms captured using the same control parameters described earlier. Comparing Fig. 6-12 to Fig. 6-14, it is observed that the same voltage and current gains are produced by both inverters, but as discussed in Subsection 6.2.2, their phase voltages are expected to be different, while their line voltages are the same. Because of the latter, for a balanced three-phase load without neutral, both inverters would appear similar to the load, which clearly is demonstrated by the same ac current waveforms that they drawn.

Proceeding on to the experimental testing, Fig. 6-16 and Fig. 6-17 show the corresponding captured waveforms for the buck-boost DCLC inverter with two dc switches, and $\{M = 0.3, k = 0.3\}$ and $\{M = 0.7, k = 0.7\}$ respectively. Agreeing well with the simulated results, the dc input voltage of 80V is boosted to a dc-link voltage of approximately 114V in Fig. 6-16 and 267V in Fig. 6-17, as noted from the highest pulse heights of the line voltage waveforms. Also observed from those figures is the anticipated 5 times higher ac current amplitude in Fig. 6-17, which certainly agrees well with the simulated waveforms. With the experimental prototype reconfigured as a single dc-switch DCLC topology, Fig. 6-18 and Fig. 6-19 show the recaptured

waveforms using the same control parameters. Comparatively, the phase voltage waveforms in these figures look unbalanced, as predicted earlier, but their corresponding line voltages appear unaffected, giving rise to the same desired set of sinusoidal current waveforms, whose partial discontinuous switching is induced by the fixed switching signal for the particular upper switch SA1, SB1 or SC1. The DCLC inverter with a single dc switch is therefore proven to exhibit comparable waveforms even though it uses one lesser active switch and a smaller commutation count, as discussed in Subsection 6.2.2.

6.4.3 Simulation and Experimental Verification for SEPIC-Derived Buck-Boost NPC and DCLC Inverters

The proposed topologies and theoretical findings of SEPIC-derived NPC and DCLC inverters were first verified in Matlab\PLECS simulations. Generally, the unique voltage boost circuitries were constructed with $C_1 = C_2 = 100\mu\text{F}$ and $L = 5\text{mH}$ for all topologies whose front-end dc source voltage is tuned to be 80V.

Fig. 6-20 and Fig. 6-21 show the simulated waveforms of buck-boost DCLC inverter with single voltage boost circuitry and two dc side switches, where the modulation

Fig. 6-20. Simulated waveforms of buck-boost DCLC inverter with single voltage boost circuitry and two dc side switches, $M = 0.3$ and $k = 0.3$.

parameters are set as $M = 0.3$ and $k = 0.3$ for voltage buck operation in Fig. 6-20 where peak ac output voltage is 34.2V according to (3.8) and $M = 0.7$ and $k = 0.7$ for voltage boost operation in Fig. 6-21 where peak ac output voltage will be 186.9V. Since DCLC and NPC inverter use the same modulation scheme and exhibit similar output performance, only the captured results of DCLC inverter are presented for visual confirmation. It is observed that five-level line voltage in both figures exactly reflects the boosted dc-link voltage in accordance with the calculation of (6.1).

Fig. 6-21. Simulated waveforms of buck-boost DCLC inverter with single voltage boost circuitry and two dc side switches, $M = 0.7$ and $k = 0.7$.

Fig. 6-22. Simulated waveforms of buck-boost DCLC inverter with single dc side switch, $M = 0.3$ and $k = 0.3$.

Next, Fig. 6-22 and Fig. 6-23 show the simulated waveforms of buck-boost DCLC inverter with single dc side switch with the same modulation conditions used for above verifications. As expected, phase voltages demonstrate unsymmetrical features due to the upper dc-link circulation of load currents during null intervals, but line voltages and currents still have the satisfied output performance without any degradation comparing to Fig. 20 and Fig. 21.

After the simulation verification, the experimental tests were carried out using the constructed laboratory prototypes where ac capacitors with $100\mu\text{F}$ were used. Besides

Fig. 6-23. Simulated waveforms of buck-boost DCLC inverter with single dc side switch, $M = 0.7$ and $k = 0.7$.

Fig. 6-24. Experimental waveforms of buck-boost DCLC inverter with single voltage boost circuitry and two dc side switches, $M = 0.3$ and $k = 0.3$.

Fig. 6-25. Experimental waveforms of buck-boost DCLC inverter with single voltage boost circuitry and two dc side switches, $M = 0.7$ and $k = 0.7$.

that, inductors in the dc network were selected with 5mH and total dc input voltage was tuned to be 80V again for consistency. Moreover, for proving the validation of buck and boost operations, the modulation parameters M and k in experimental verifications were again set to be equal with 0.3 for buck operation and 0.7 for boost operation as those used in simulations. Fig. 6-24 and Fig. 6-25 show the captured experimental waveforms of SEPIC-derived buck-boost DCLC inverter with single voltage boost circuitry and two dc side switches in front. Clearly, both buck and boost operations well match with the simulated results with balanced five-level line voltage and three-level phase voltage switching. Further, to verify the DCLC inverter with simplified voltage boost circuitry, Fig. 6-26 and Fig. 6-27 show the captured waveforms for voltage buck and boost operations, respectively, which demonstrate that the buck-boost DCLC inverter with single dc-side switch can well perform buck and boost operations without performance degradation for powering balanced three-phase load regardless of the discontinuous switching shape appeared in the captured phase voltage.

6.5 Summary

For enriching the buck-boost concepts in three-level application, this chapter first presents the design of a buck-boost three-level dual inverter implemented by cascading

Fig. 6-26. Experimental waveforms of buck-boost DCLC inverter with single dc side switch, $M = 0.3$ and $k = 0.3$.

Fig. 6-27. Experimental waveforms of buck-boost DCLC inverter with single dc side switch, $M = 0.7$ and $k = 0.7$.

two two-level VSI bridges and supplied by a single dc network. The designed inverter can be controlled using carefully formulated PSC modulation scheme with three types of inverter switching states incorporated for inverter buck-boost operation.

In addition to the development of dual inverter, new three-level inverter topologies with buck-boost capability, improved from the Ćuk- and SEPIC-derived two-level energy conversion concept, were proposed. With proper topological layouts and modulation developments, balanced capacitive charging are always enforced within the inverters, resulting in three-level phase and five-level line voltage switching produced at the inverter output terminals at all instances. Implementation wise, embedding an appropriately designed modulation scheme allows the system to be easily controlled using any existing modern DSP designed for motion control. As an

alternative option, the proposed DCLC inverters are also redesigned with one lesser switch used in the voltage boost circuitry, and with proper current path regulation, the same output performance can be obtained with a sizable drop in switching loss.

Chapter 7 Five-Level Z-Source Diode-Clamped Inverter

Comparing the above addressed three-level alternatives with their two-level counterparts, the general conclusion deduced is that unlike traditional inverter development, extending the buck-boost conversion concept to inverters with more discrete voltage levels is not as straightforward. This is especially true for cases where achieving reduced element count is desired, and will always involve some amount of theoretical reasoning if the inverter is at all realizable.

In fact, after analyzing all options presented in the thesis, the candidate would comment that the five-level Z-source inverter proposed in this chapter and implemented using the minimum of two impedance networks is the highest extended variant with satisfactory waveform quality that can be constructed using the diode-clamped topology. For more than five discrete voltage levels, Z-source, Ćuk and SEPIC-derived inverters implemented using the cascaded topology with non-minimized number of boosting networks are realizable, but this extension is straightforward and is therefore not explicitly discussed in the thesis. Instead, only the development of a five-level Z-source diode-clamped inverter is explained in details with attention focused mainly on the unobvious partial shoot-through states, which are previously not assumable by two-level inverters.

A further comment emphasized here is that although the five-level Z-source inverter is demonstrated to be practically realizable in this chapter, its adoption by the industry might be slow because of those traditional drawbacks like difficulty in balancing the multiple source voltages and high manufacturing cost experienced by the diode-clamped topology. Despite of that, applications where the diode-clamped topology can interestingly be used still exist with one recent example stated in [132], where it is used as a solar converter for controlling and tracking the maximum power

Fig. 7-1. Topology of proposed five-level Z-source diode-clamped inverter.

points of individual solar panels independently. Therefore, although its rate of adoption is slower, chances of the proposed five-level inverter finding its niche applications are there, especially for cases where both buck-boost feature and high waveform quality are needed, hence justifying its investigation in this project.

7.1 Operational Principles of Five-Level Z-Source Diode-Clamped Inverter

As emphasized at the start of Section 4.2, the Z-source NPC inverter shown in Fig. 4-9 is indeed the simplest three-level variant that can be constructed using only a single Z-source network, unlike that proposed in Section 4.1 where two Z-source networks are used as drawn in Fig. 4-2. At first sight, the method illustrated in Fig. 4-2 might appear as a feasible method for implementing a five-level diode-clamped inverter, where four Z-source networks and four isolated sources are cascaded in series at their dc input front-ends. But a closer examination of its operating principles would reveal

Fig. 7-2. Equivalent circuits of five-level Z-source diode-clamped inverter when in (a) non-shoot-through, (b) upper shoot-through and (c) lower shoot-through states.

that full dc-link shoot-through of any of the two middle Z-source networks initiated by a particular phase-leg will cause the voltages of the other two phase-legs to drop by one voltage level occasionally, which unfortunately will introduce volt-sec error at the inverter three-phase output (partial shoot-through scheme not applicable here). The circuit in Fig. 4-2 is therefore not a viable building block, inferring that it will not be explored further.

Instead, the method illustrated in Fig. 4-9 is reexamined with the general conclusion being that its extension to a five-level diode-clamped inverter is only possible if two Z-source networks are used and connected as shown in Fig. 7-1. As illustrated, the five-level inverter is constructed by using two split dc sources, two Z-source networks and a traditional diode-clamped circuitry. Within the diode-clamped circuitry, three clamping branches $\{DX1, DX'1\}$, $\{DX2, DX'2\}$ and $\{DX3, DX'3\}$ per phase are noted with their midpoints respectively connected to N1, N and N2 with N taken as the reference neutral potential. As expected, the resulting inverter can operate in either the non-shoot-through or any of the partial shoot-through states, where the latter is undoubtedly needed for inductive voltage-boosting.

Beginning with analyzing the non-shoot-through state whose equivalent representation is drawn in Fig. 7-2(a), its operating principles are noted to be similar to those exhibited by the three-level Z-source inverter in Fig. 4-9, except there are now two three-level units linked at point N. Proceeding on to analyze the first partial shoot-through state illustrated in Fig. 7-2(b), the upper short-circuit is effectively inserted by turning ON switches SX1, SX2, SX3, SX4 and SX'1 (five in total, as compared to four needed by the traditional active and null states) with DA'1 and D1 conducting, DA1 and D2 blocking, and the lower Z-source network remaining in its own non-shoot-through state. The resulting five-level equivalent circuit is no doubt similar to the three-level representation shown in Fig. 4-11(a), except with a second non-shoot-through three-level unit connected below it.

The same analytical approach when applied to the lower partial shoot-through state shown in Fig. 7-2(c) would similarly reveal that it is introduced by turning ON SA4, SA'1, SA'2, SA'3 and SA'4 with DA3 and D4 conducting, DA'3 and D3 blocking, and the upper Z-source network staying in its own non-shoot-through state. The simplified equivalent circuit in Fig. 7-2(c) is in principle similar to the three-level case shown in Fig. 4-11(b), except with a second non-shoot-through three-level unit tied in series

above it. Collectively, the three equivalent circuits in Fig. 7-2 would impart to the five-level inverter its voltage-boosting ability, whose mathematical expressions are again derived as (4.8) and (4.9) if the same total normalized dc source voltage is used for powering the inverter. In addition to that, it is important to set the durations assumed by the two circuits in Fig. 7-2(b) and (c) to be equal so as to boost the upper and lower dc-link voltages by the same extent, needed for producing a set of balanced three-phase output.

Another operating point to note is that so far only the outer partial shoot-through states are considered, but not the two inner partial shoot-through states initiated by turning ON SA2, SA3, SA4, SA'1 and SA'2 to short N1 with N, or SA3, SA4, SA'1, SA'2 and SA'3 to short N to N2. Although both inner states appear to be feasible from a single phase-leg prospective, they unfortunately are not viable for implementation in a three-phase system. The reason is because the insertion of an inner partial shoot-through state by a particular phase-leg would inevitably cause the voltages of either one or two of the other phase-legs to collapse by one voltage level, hence introducing volt-sec error to the three-phase inverter output, which of course is undesirable. In contrast, partially shorting of either of the outer load current sources in Fig. 7-2(b) or (c) will not introduce any volt-sec error if it is inserted appropriately to the relevant state sequence, as demonstrated in the following section, where modulation schemes are developed.

7.2 Modulation Schemes of Five-Level Z-Source Inverter

In this section, two different carrier-based modulation schemes are presented for controlling the five-level Z-source diode-clamped inverter with each having its own advantages like optimized harmonic performance or minimized common-mode voltage. In spite of their differences, both schemes share the common principle of carefully introducing a fifth ON switch to the four already ON switches without introducing any additional commutation and volt-sec error to the inverter ac output. An example illustrating that is easily formulated by assuming phase A transiting from $2V_{dc}$ to V_{dc}

Fig. 7-3. Example PD state sequences for controlling five-level (a) traditional and (b) Z-source diode-clamped inverters.

with its switches transiting from $\{SA1, SA2, SA3, SA4, SA'1, SA'2, SA'3, SA'4\} = \{ON, ON, ON, ON, OFF, OFF, OFF, OFF\}$ to $\{OFF, ON, ON, ON, ON, OFF, OFF, OFF\}$, giving two commutation counts in total.

If an upper partial shoot-through state needed to be inserted now, the intermediate condition of $\{ON, ON, ON, ON, ON, OFF, OFF, OFF\}$ can be added, which again gives two commutation counts in total, since the shoot-through state is simply inserted by turning $SA'1$ ON earlier and $SA1$ OFF slightly later, rather than simultaneously. An

interval whereby all upper five switches are ON is therefore created for partially shorting the upper Z-source network to boost its inductive voltage. The same operating mechanism can also be applied to the lower Z-source network, which when integrated with the three-phase analysis presented below, will give rise to a flexibly tuned inverter with no volt-sec error produced.

7.2.1 Phase Disposition Modulation

Comparing a set of three-phase sinusoidal references with a set of vertically disposed, zero-phase-shifted triangular carriers, the resulting inverter state sequence is known to produce output line voltages with optimized harmonic performance. Classically, that style of arranging the vertically disposed carriers is known as Phase Disposition modulation method, which does appear to be a good platform for inserting partial shoot-through states so as to derive buck-boost schemes for controlling the proposed five-level Z-source diode-clamped inverter.

To clearly illustrate how the shoot-through insertion can be performed, two example state sequences for controlling traditional and Z-source five-level inverters are illustrated in Fig. 7-3. For controlling the former, its state sequence is generated by comparing three sinusoidal references with the four zero-phase-shifted carriers, while for the latter, the only difference noted is the addition of two other references labeled as Ref. $A_{(SA)}$ and Ref. $C_{(SC')}$. With five references in total, instead of the conventional method of assigning one reference per phase, two phases (phases A and C) of the Z-source inverter are now controlled by two references each, while the third phase is controlled by one reference. To be more specific, the reference assignment is summarized as:

- Ref. $A_{(SA)}$ for turning SA1 ON and Ref. $A_{(SA')} = \text{Ref. A}$ for turning SA'1 OFF when they rise above the triangular carrier.
- Ref. B for turning SB2 ON and SB'2 OFF when it rises above the triangular carrier.

- Ref. $C_{(SC)} = \text{Ref. } C$ for turning SC4 ON and Ref. $C_{(SC')}$ for turning SC'4 OFF when they rise above the triangular carrier.

Using the above reference assignment, the first transition in Fig. 7-3(a) from $\{1, 0, -2\}$ to $\{2, 0, -2\}$ would have an intermediate upper partial shoot-through state inserted to the right of that transition, partially overlapping the $\{1, 0, -2\}$ state. What really happened is that SA1 is turned ON earlier, while SA'1 is turned OFF at the original instant without any increase in commutation count. That then creates an interval whereby SA1, SA2, SA3, SA4 and SA'1 are ON simultaneously. During this interval, the phase A normalized voltage (relative to $\hat{v}_i/2$, see (4.18)) is noted to be 1p.u. since SA'1 and DA'1 are conducting, while those of phases B and C remain unaffected. The resulting three-phase voltages are therefore similar to those of state $\{1, 0, -2\}$, implying that the overlapping caused by the upper shoot-through state will not result in any volt-sec variation.

The same analytical approach can be applied to the third transition from $\{2, 1, -2\}$ to $\{2, 1, -1\}$ shown in Fig. 7-3(a), where it is quite easily to deduce that the additional reference cause SC'4 to turn OFF later, while SC4 turns ON at the original time instant. This unarguably inserts a lower shoot-through state with SC4, SC'1, SC'2, SC'3 and SC'4 ON simultaneously, and is overlapping the $\{2, 1, -1\}$ interval without introducing any volt-sec error. To conclude, it is generally commented that by simply raising the maximum reference and lowering the minimum reference to create two new references, the appropriate partial shoot-through states are always inserted to the inverter state sequence correctly without any volt-sec error introduced. Mathematically, the full set of references is then expressed as:

$$\begin{cases} V_{\max(SX)} = V_{\max} + V_{\text{off}} + T_S \\ V_{\max(SX')} = V_{\max} + V_{\text{off}} \end{cases}$$

$$\begin{cases} V_{\text{mid}(SX)} = V_{\text{mid}} + V_{\text{off}} \\ V_{\text{mid}(SX')} = V_{\text{mid}} + V_{\text{off}} \end{cases}$$

$$\begin{cases} V_{\min(SX)} = V_{\min} + V_{\text{off}} \\ V_{\min(SX')} = V_{\min} + V_{\text{off}} - T_s \end{cases}$$

$$T_s = \frac{T_0}{T} \quad X = A, B \text{ or } C \quad (7.1)$$

where V_{off} represents the triplen offset added to maintain equal $\{1, 0, -2\}$ and $\{2, 1, -1\}$ intervals at the two edges of each half switching cycle for overlapping by the upper and lower shoot-through states respectively. Ensuring that would force balanced voltage-boosting of the two Z-source networks in the five-level diode-clamped inverter at all times so as to avoid unnecessary distortion and voltage stress across the devices. Last but not least, for illustrating the wave shapes of (7.1), Fig. 7-4 plots the references, where it is noted that the maximum and minimum envelopes have two references each, separated by a vertical displacement of $T_s = T_0/T$.

7.2.2 Alternative Phase Opposition Disposition Modulation

Instead of the PD scheme, a second carrier arrangement is possible, and is shown in Fig. 7-5 for controlling both the traditional and Z-source five-level inverters. In the diagrams, the four carriers are shown alternating with a 180° phase-shift observed between them, which then gives it the name of alternative phase opposition disposition. This second scheme is reported to have a comparatively poorer waveform quality when used for controlling a traditional inverter, but it produces a lower common-mode

Fig. 7-4. Modified references for controlling five-level Z-source diode-clamped inverter.

Fig. 7-5. Example APOD state sequences for controlling five-level Z-source diode-clamped inverters.

voltage, which might be of interest for some applications. Therefore, its extension to a five-level Z-source control scheme is also pursued here using the example state sequences shown in Fig. 7-5, which are again produced using the reference set listed in (7.1), except with V_{off} replaced by:

$$V_{off(APOD)} = -0.5 \{ \max(V_A, V_B, V_C) + \min(V_A, V_B, V_C) \}$$

$$V_A = \text{Ref. A}, V_B = \text{Ref. B}, V_C = \text{Ref. C} \quad (7.2)$$

In effect, (7.2) causes the two $\{1, 1, -1\}$ intervals placed at the start and end of a full switching cycle (no longer half a switching cycle) to become equal for balanced insertion of partial shoot-through states to the left of the first transition and right of the fifth transition. Specifically, for the first $\{1, 1, -1\}$ to $\{2, 1, -2\}$ transition, an upper shoot-through state is inserted by using Ref. A_(SA) to turn ON SA1, before Ref. A_(SA') turns OFF SA'1, hence creating an interval whereby the five relevant switches are ON simultaneously without introducing any additional commutation. Happening simultaneously at the first transition is the insertion of a lower shoot-through state triggered by using Ref. SC_(SC') to turn ON SC'4, before Ref. SC_(SC) turns OFF SC4 at a later time. The same analytical approach can be applied to the fifth $\{2, 1, -2\}$ to $\{1, 1, -1\}$ transition, where it is again noted that an upper and a lower shoot-through state are inserted simultaneously. To summarize, balanced voltage-boosting of the two Z-source

networks is always attained with no significant volt-sec distortion introduced, while yet producing a lower common-mode voltage as demonstrated in the next section.

7.3 Experimental Verification

Fig. 7-6. PD experimental results of five-level Z-source diode-clamped inverter controlled with $M = 1.15$ and $T_0/T = 0$. Top to bottom: line voltage, phase voltage, common-mode voltage and line current.

Fig. 7-7. PD experimental results of five-level Z-source diode-clamped inverter controlled with $M = 0.7 \cdot 1.15$ and $T_0/T = 0.3$. Top to bottom: line voltage, phase voltage, common-mode voltage and line current.

For verifying the conceptual findings developed in the paper, a scaled down experimental setup was constructed in the laboratory for physical testing. The setup consisted of a five-level Z-source diode-clamped inverter with its two Z-source networks assembled using capacitors $C_1 = C_2 = C_3 = C_4 = 1000\mu\text{F}$ and inductors $L_1 = L_2 = L_3 = L_4 = 3.3\text{mH}$. The five-level inverter was powered from four dc programmable supplies configured to form two split dc sources with V_{dc} set to 80V, and was connected to a 1.6kVA induction motor as load. The resulting system was controlled using a digital signal processor, to which PD or APOD modulation code could be downloaded for testing.

With the system configured to perform PD modulation, Fig. 7-6 shows the experimental waveforms captured using the control parameters of $M = 1.15$ and $T_0/T = 0$. Obviously, the desired nine-level line voltage switching and five-level phase voltage switching are produced with the current flowing into the motor noted to be sinusoidal. With the control parameters retuned to $M = 0.7 \times 1.15$ and $T_0/T = 0.3$ for introducing some amount of voltage-boosting, Fig. 7-7 shows the recaptured PD waveforms, where the peaks of all voltage traces are noted to increase as intended (the current was intentionally lowered during the experiment to keep the motor well within its kVA

Fig. 7-8. APOD experimental results of five-level Z-source diode-clamped inverter controlled with $M = 1.15$ and $T_0/T = 0$. Top to bottom: line voltage, phase voltage, common-mode voltage and line current.

Fig. 7-9. APOD experimental results of five-level Z-source diode-clamped inverter controlled with $M = 0.7 \cdot 1.15$ and $T_0/T = 0.3$. Top to bottom: line voltage, phase voltage, common-mode voltage and line current.

rating).

For comparison, the APOD scheme was next tested under the same operating conditions with its corresponding results captured and presented in Fig. 7-8 and Fig. 7-9. As expected, the same voltage-boosting is noted between the two sets of waveforms, whose generated common-mode voltages are both noted to be lower than those produced by the PD scheme. Also noted in the figures is the slightly more distorted current waveform in Fig. 7-9 as compared to that of the PD scheme in Fig. 7-7. The reason for the distortion might be linked to implementation difficulties associated with synchronizing the upper and lower partial shoot-through states within the same time span, as illustrated in Fig. 7-5. Regardless of that, the presented results clearly verify the boosting ability of the developed modulation schemes with the decision on which to use solely determined by other features like optimized waveform quality or a lower common-mode switching.

In passing, it is commented here that the common-mode voltages captured in Fig. 7-6 to Fig. 7-9 switch at finite values, which can be reduced to zero by extending those zero common-mode schemes discussed in Chapters 4 and 5. This extension is viewed

as trivial, compared with the topological design and shoot-through insertion method discussed in the chapter for higher level Z-source inverter, and will therefore not be explicitly discussed here. Instead, interested readers can refer to [19], where the same steps discussed for extending reduced common-mode schemes for traditional inverters with higher number of voltage levels can equally be applied here.

7.4 Summary

This chapter presents the design of a five-level Z-source diode-clamped inverter that can perform buck-boost dc-ac energy inversion. Using those newly identified partial shoot-through states, the proposed inverter can produce a non-degraded voltage gain, while at the same time, switch with more distinct voltage levels for achieving a better output waveform quality. Depending on the state placements adopted, different modulation schemes can be developed for controlling the proposed five-level inverter with different operating characteristics achieved. These characteristics, together with the practicality of the inverter, have already been verified experimentally using a digitally controlled laboratory prototype operating under both normal and voltage-boost conditions.

Chapter 8 Performance Evaluation under Semiconductor Failure Conditions

To date, multilevel (particularly neutral-point-clamped) inverters have found extensive applications in the industry due to their many inherent advantages like a lower electromagnetic interference level, better waveform quality and lower semiconductor stress achieved by appropriately connecting multiple static switches in series. Despite this popularity, a possible complication associated with multilevel inverters is their higher risk of experiencing semiconductor failure (both open- and short-circuit) since more switches are used for constructing the inverters. For enhancing the inverter ride-through capability, many fault-tolerant schemes have since been proposed with some solutions focusing on the timely replacement of faulty switches using extra pre-installed switches [120, 121] and others focusing on the appropriate selection of switching states that will give rise to the lowest waveform distortion [122].

For the former approach, the addition of a standby fourth phase-leg for replacing any faulty phase-leg in a three-phase inverter through simple triac reconfiguration is considered the most effective strategy with virtually no distortion observed except during the short fault-sensing interval [120]. But of course, this added redundancy is relatively expensive to implement especially for inverters with more output voltage levels. As an alternative low cost solution, the inverter modulation state sequence can be modified to provide some ride-through capability, which is usually accompanied by a serious degradation of the inverter performance (for some inverter topologies, this latter approach might not even work under certain fault conditions) [122-124].

The abovementioned fault tolerant strategies have indeed contributed significantly to the maintaining of smooth process operations, and it is expected that similar fault-tolerant investigation when performed on other inverter topologies can bring

equally valuable benefits. With that belief in view, this chapter first presents a detailed study and the subsequent development of a number of fault ride-through schemes that can be used for controlling those three-level Z-source inverters implemented using two LC impedance networks. The study reveals that nearly all the chosen three-level Z-source inverters can ride-through semiconductor failure smoothly with their output waveform quality and amplitude kept nearly unchanged except for a slight degradation of their high frequency switching content. These performance improvements are achieved by performing only slight reconfiguration of the inverter state sequences and gating arrangements with no additional hardware requirements imposed.

Additionally, for cases where the Z-source, Ćuk- or SEPIC-derived dual inverters are used and configured to operate with reduced common-mode switching, the simple reconfiguration of the inverter gating signals would continue to allow the inverters to operate with zero common-mode voltage generated, while at the same time maintaining their output waveform quality and amplitude. This simultaneous retaining of multiple desired performance features is not possible with a traditional three-level inverter, and can only be attained through the careful reconfiguration of the dual inverter state sequence.

The above-described ride-through analysis is however not performed on those three-level inverters implemented using a single LC impedance network or active boosting circuitry, and the Z-source five-level converter. The reason is because their common feature of reduced component count, although helps to reduce the system cost, would undoubtedly render them as inappropriate choices for fault ride-through due to the lack of operating redundancies. They are therefore not included in the chapter without degrading the overall analytical quality.

8.1 Fault Tolerant Strategies for Z-Source Neutral-Point-Clamped Inverter

Fig. 8-1 shows the topology of the Z-source neutral-point-clamped (NPC) inverter proposed in Section 4.1, where two unique Z-source impedance networks (each consisting of a split-inductor and two capacitors) are connected between two input dc sources and a NPC inverter circuitry. For supporting bidirectional conversion of energy and to avoid undesirable operating modes under light load condition, two active switches with anti-parallel diodes ($SW_{(U)}$ or $SW_{(G)}$) are also used in place of those front-end diodes indicated in Fig. 4-2. With these added components, it can easily be shown that the peak ac output voltage $\hat{v}_x$ ($x = a, b$ or c) of the resulting Z-source inverter can be stepped up or down, and is also mathematically expressed as (4.9).

Fig. 8-1. Topology of Z-source neutral-point-clamped inverter.

Fig. 8-2. Three-level vector diagram illustrating switching states used for traditional inverter failure ride-through.

Quite intuitively, a requirement that must be imposed is for both impedance networks to be shorted for the same time durations so as to maintain balanced voltage-boosting of the overall inverter under normal operating conditions, as already verified in Section 4.1. Now if a switch from phase A fails, the traditional approach is to restrict the “allowed” inverter switching states to those shown in Fig. 8-2, where it is assumed that SA1 fails short-circuit (unwanted states in the diagram are cancelled using bold lines). The illustrated diagram clearly shows that the faulted vector diagram is unsymmetrical, which to some extent obstructs the symmetrical shorting of the two Z-source networks. This in turns gives rise to an unbalanced voltage boosting, an unwanted waveform distortion and a likely drop in output voltage amplitude (similar to those experienced by a traditional NPC inverter).

To avoid the above-described performance limitations, another approach recommended here is to constrain the “allowed” switching vectors to those on the bold hexagon shown in Fig. 8-3. Depending on the failed switch location and its nature of failure (open- or short-circuit), the correct redundant states are then selected for switching the inverter. As an example, the case of open-circuit switch SA1 failure in Fig. 8-1 is considered, whose immediate effect is that phase-leg A is now prevented from

Fig. 8-3. Three-level vector diagram illustrating shaded switching states used for Z-source inverter failure ride-through.

Fig. 8-4. Possible state sequences (a) (c) without and (b) with shoot-through states used during semiconductor failure.

outputting voltage level $+V_{dc}$ and effecting the upper shoot-through state. That would mean that only those shaded states on the bold hexagon in Fig. 8-3 and the lower Z-source shoot-through state can be used since other redundant states would require a $+V_{dc}$ output from phase-leg A. For illustrating, a possible state sequence having zero shoot-through state interval is shown in Fig. 8-4(a), where the active states are noted to be centrally placed.

In principle, the discussed fault ride-through scheme is equivalent to the simplification of three-level to two-level modulation, which can easily be implemented using the on-chip carrier-based modulator found in most modern digital signal processors. But, when applied to a traditional three-level inverter, it unfavorably results in a significant dip in ac output, which fortunately can be resolved by effecting voltage boosting for the case of a Z-source inverter. For doing that, while at the same time preserving its normalized volt-sec average, the allowable lower shoot-through state during fault interval should ideally be inserted to the null $\{0,0,0\}$ and $\{-1,-1,-1\}$ state intervals only since they produce the same set of zero three-phase line voltages as when in the lower shoot-through state. This replacement is illustrated in Fig. 8-4(b), where the $\{0,0,0\}$ and $\{-1,-1,-1\}$ state intervals are partially replaced by lower shoot-through states, whose total duration T_0 (and hence B) is tuned according to (4.9) so that its output is kept at the pre-fault level even though the inverter is now constrained to use the inner hexagonal vectors. But of course, the rating of the semiconductor switches used in the inverter must correspondingly be raised during the design stage before T_0 can be raised during operation.

The same modulation principles can be applied to the case when SA1 fails short-circuit, but rather than switching phase A between $-V_{dc}$ and 0 V, it should transit between $-V_{dc}$ with {SA'1, SA'2} conducting and $+V_{dc}$ with {SA1, SA2} conducting. In addition, shoot-through states are now initiated by turning ON all switches from phase A to short the two Z-source networks simultaneously. Obviously, both dc sources are used for this latter case, which means that the increase in shoot-through interval T_0 needs not be as high as that needed for the case where SA1 fails open-circuit.

Similar analysis with other faulted switches or clamping diodes would reveal that when the above two two-level simplification schemes are correctly selected for application, the inverter can ride-through all faults with minimal distortions except for the case when an inner switch (SA2 or SA'1) fails open-circuit. When the exceptional case really happens (e.g. SA2 fails open-circuit), the 0 and 1 indexes in Fig. 8-3 are not achievable physically for phase A, implying that switching operation for phase A is now not possible (phase A always tied to $-V_i$ or left floating), and an alternative fault mitigation technique needs to be implemented like (e.g.) connecting a second set of parallel inner switches. As a convenient reference for all possible fault scenarios, Table 8-1 summarizes the above discussions, together with those for other topologies discussed in the remaining sections, for easier comparison purposes.

8.2 Fault Tolerant Strategies for Z-Source DC-Link-Cascaded Inverter

An alternative three-level Z-source inverter proposed that does not use clamping diodes is illustrated in Fig. 5-1 referring to the dc-link-cascaded inverter. Similar to the Z-source NPC inverter, the DCLC inverter has its two Z-source networks connected in series, and indeed, its operation is similar to the series connection of two two-level bridges on their dc sides with appropriate switching combinations of the inverter listed in Table 5-1. The DCLC inverter is also controlled using the NTV modulation concept

with balanced voltage boosting of the two Z-source networks needed during normal steady-state conditions. Under semiconductor failure mode, its operation is again left unexplored previously, but surely can be investigated using the same approach documented earlier for the Z-source NPC inverter.

Beginning with the first assumed fault whereby outer switch $SA_{(U)}$ fails open-circuit, the upper dc rail potential of $+V_{dc}$ can now no longer be assumed, leaving only the dc potentials of $0V$ and $-V_{dc}$ for the inverter to switch to if undistorted, symmetrical three-phase operation is preferred. Effortlessly, this can be achieved by permanently turning $SX_{(U)}$ OFF and $SX'_{(U)}$ ON, while controlling the lower inverter G to operate like a two-level Z-source inverter. In addition, the proper shoot-through duration, effected by turning ON $SX_{(G)}$ and $SX'_{(G)}$ to short the lower inverter bridge, should rightfully be inserted for compensating ac amplitude drop happening immediately at the instant of fault occurrence. On the other hand, if $SA_{(U)}$ is assumed to fail short-circuit, $SX_{(U)}$ should rightfully be commanded ON to give the two allowable voltages needed for symmetrical three-phase operation as $+V_{dc}$ and $-V_{dc}$. As for their complements $SX'_{(U)}$, they are turned ON together with $SX_{(G)}$ and $SX'_{(G)}$ ($SX_{(U)}$ already ON) to effect full dc-link shoot-through of the two Z-source networks simultaneously, similar to the case of SA1 short-circuit failure in a Z-source NPC inverter.

Proceeding on to analyze failures of other switches, it is generally observed that most failures can be compensated by introducing similar schemes as described above, except for the cases of $SX_{(G)}$ open-circuit failure and $SX'_{(G)}$ short-circuit failure. For both cases, only the negative dc potential of $-V_{dc}$ is accessible, while the other two (0 and $+V_{dc}$) are effectively isolated from the output terminal by either open-circuit failing of $SX_{(G)}$ or short-circuit failing of $SX'_{(G)}$. Riding through of these failures by simply tuning the modulation algorithm is therefore not possible, unless redundant parallel switches are added across switches of the lower bridge. Again, the discussed compensation strategies for DCLC inverter are summarized in Table 8-1 for easier comparison with other Z-source topologies.

8.3 Fault Tolerant Strategies for Z-Source Dual Inverters¹

The Z-source dual inverters, supplied by either two isolated dc sources or a single source, are shown in Fig. 5-4(a) and (b), respectively (see also Table 5-2 for the possible phase-leg switching combinations), where the former is controlled using the NTV phase disposition scheme whereas the latter is controlled using the phase-shifted carrier scheme. With only slight logic modifications, both inverters can also function with zero common-mode voltage generated if their switching states are limited to those that have a zero common-mode average (aided also by the omission of dead-time delay, which is an inherent feature of all Z-source inverters). Detailed descriptions of these modulation schemes and their steady-state buck-boost operational characteristics are documented in Chapter 5, and therefore not elaborated here. Instead, this section aims to extend the work by studying how the inverters should be reconfigured to allow them to ride-through virtually all types of semiconductor failure with minimized waveform distortion, negligible drop in voltage amplitude and the elimination of common-mode voltage, where the latter is characteristically achievable by the Z-source dual inverter only.

A feature noted from the dual inverter topologies shown in Fig. 5-4(a) and (b) is that the switches are functionally identical with no distinction like inner and outer switch classifications found in the NPC inverter. Therefore, the ride-through study for dual inverters can simply be performed by considering the open- and short-circuit failure of any single switch. As an example, if $SA_{(G)}$ is assumed to fail short-circuit (open-circuit), the lower inverter (labeled as inverter G in Fig. 5-4(a) and (b)) can be forced to tie firmly to state $\{1,1,1\}$ ($\{0,0,0\}$), while the upper inverter (labeled as inverter U) gets reconfigured to switch like a two-level inverter with a similar sequence shown in Fig. 8-4(c). To avoid a drop in output voltage, shoot-through states with the upper impedance network shorted can still be inserted with its duration

¹ The analysis presented here is equally applicable to the Ćuk- and SEPIC-derived dual inverters with very close similarities noted, and are therefore not explicitly duplicated here.

properly adjusted to compensate for the loss of energy supplied by the lower source. In addition, for the case where two isolated sources are used, it is noted that the output terminals of the lower inverter G are now constantly shorted to form a floating star point on the primary side of the transformer whose potential is expressed as:

$$V_{star} = \frac{S_a + S_b + S_c}{3} V_i \quad (8.1)$$

where S_a , S_b and S_c represent the switching functions of inverter U in two-level mode and V_i is its dc link voltage. The “phase to star point” voltage V_x ($x = a, b$ or c) appearing across the primary and secondary phase windings of the transformer is then expressed as (assuming a 1:1 turn ratio):

$$V_x = S_x V_i - V_{star} \quad (8.2)$$

Using (8.2), the generated common-mode voltage at the secondary terminals of the transformer is derived as (8.3), whose value is zero. This extra feature and the symmetrical structure of the dual inverter allow it to ride-through virtually all types of semiconductor failure with negligible disturbances incurred on its output voltage amplitude, waveform quality and common-mode elimination capability, which to date, cannot be achieved by the other three-level Z-source inverters.

$$V_{cm} = \frac{V_a + V_b + V_c}{3} = \frac{S_a + S_b + S_c}{3} V_i - V_{star} = 0 \quad (8.3)$$

Fig. 8-5. Topology of Z-source dual inverter with single dc source and additional triacs.

Unfortunately, the above-described zero common-mode ride-through capability cannot be retained if only a single dc source is used for implementing the dual inverter, as shown in Fig. 5-4(b). But by adding additional triacs as illustrated in Fig. 8-5 and by turning OFF the lower two triacs to isolate the failed inverter G (tied to a null state), the common floating point can again be formed with the same common-mode ride-through ability maintained. This solution is relatively less costly but using only one source in Fig. 8-5 is indeed definitely not as reliable as using two isolated sources, as illustrated in Fig. 5-4(a). Considering the modification in the dual inverter with single dc source, all ride-through results in the Z-source dual inverters with either single dc source or two isolated dc sources always demonstrate zero common-mode voltage in all types of semiconductor failure no matter what modulation schemes are used before the simple two-level reconfiguration.

Before ending the conceptual discussion on failure of rear-end inverter switches, a brief consideration of failure of the front-end switches $SW_{(U)}$ and $SW_{(G)}$ might be of interest for completeness, and equally holds true for all presented inverter topologies. Considering first the short-circuit malfunctioning of either $SW_{(U)}$ or $SW_{(G)}$, the relevant input dc source affected is now firmly tied to its accompanied Z-source network,

Table 8-1. Summary of the proposed compensation strategies.

	Failed Semiconductor		Boosted Z-Source Network	Alternating Phase Voltage
	Open-circuit	Short-circuit		
NPC Inverter	SX1	SX'1, DX1	G	$0, -V_i$
	SX'2	SX2, DX2	U	$+V_b, 0$
		SX1, SX'2	G and U simultaneously	$+V_b, -V_i$
	SX2, SX'1		N/A	N/A
DCLC Inverter	$SX_{(U)}$	$SX'_{(U)}$	G	$0, -V_i$
	$SX'_{(G)}$	$SX_{(G)}$	U	$+V_b, 0$
	$SX'_{(U)}$	$SX_{(U)}$	G and U simultaneously	$+V_b, -V_i$
	$SX_{(G)}$	$SX'_{(G)}$	N/A	N/A
Dual Inverter	$SX_{(U)}, SX'_{(U)}$	$SX_{(U)}, SX'_{(U)}$	G	$(2/3, 1/3, 0, -1/3, -2/3) V_i$
	$SX_{(G)}, SX'_{(G)}$	$SX_{(G)}, SX'_{(G)}$	U	$(2/3, 1/3, 0, -1/3, -2/3) V_i$

causing it to lose its voltage-boosting capability (periodic disconnection of the source from its accompanied Z-source network is needed for effecting voltage-boosting). In other words, the affected inverter bridge has degraded to a traditional two-level bridge, which supports only voltage-buck operation. For this case, symmetrical voltage-boost operation can only be attained by performing the same three-level to two-level reconfiguration explained earlier for all the investigated topologies.

Instead of failing short-circuit, if $SW_{(U)}$ or $SW_{(G)}$ now fails open-circuit, two different scenarios can appear depending on whether their free-wheeling diodes are intact. If the diodes are operating normally, the Z-source inverter can still operate with buck-boost capability in the forward energy flow direction, but can no longer support reverse energy flow. On the other hand, if the diodes fail open-circuit indefinitely, one dc source is considered lost, leaving only the other for powering the inverter, which should now be reconfigured to operate with two-level switching.

8.4 Simulation and Experimental Verification

The proposed fault tolerant strategies were initially verified in PLECS simulation with the Z-source network parameters chosen as $C = 2200\mu\text{F}$ and $L = 5\text{mH}$, and the

Fig. 8-6. Simulated results of Z-source NPC inverter when SA1 fails open-circuit.

Fig. 8-7. Simulated results of Z-source NPC inverters when SA1 fails short-circuit.

switching frequency set to 5kHz. In common, all the tested inverters were powered from two dc sources with each set to 40V, which was subsequently boosted to $\approx 100V$ for powering the rear-end inverter circuitry during various fault conditions set to occur at $t = 40ms$. With these settings, Fig. 8.6 shows the simulated waveforms produced by a Z-source NPC inverter operating with SA1 failing open-circuit. Before fault occurrence, the pre-fault control parameters are set to $M = 1$ and $T_o/T = 0$, and immediately upon sensing the fault, the control parameters are retuned to $M = 0.67$ and $T_o/T = 0.33$ needed for producing enough voltage-boosting to keep the three-phase ac output currents unchanged (see (4.9)). Besides retuning the control parameters, conversion from three-level to two-level boosted switching is also performed with the line currents brought back to their pre-fault value without distortion in a fundamental cycle (inductive boosting transient). Other than that, only a slightly larger post-fault current ripple is noted to impose on the overall three-phase currents, which still appear as balanced and undistorted.

Alternatively, when SA1 in the Z-source NPC inverter fails short-circuit, Fig. 8-7 shows the simulated results obtained with the same pre- and post-fault parameters of $M = 1$ and $T_o/T = 0$, since the faulted circuitry is still being powered by the two separate dc sources, instead of one like in the first case. Therefore, the proposed strategy simply

Fig. 8-8. Simulated results of Z-source dual inverter with two dc sources connected.

needs to reconfigure the inverter to two-level switching without needing to readjust its shoot-through duration for compensating voltage dip. Because of the uniform control parameters used, the one-cycle transitional period caused by Z-source capacitive charging in Fig. 8-6 does not appear in Fig. 8-7, where the only post-fault distinct feature noted is the larger ripple content imposed on the line current waveforms. Quite obviously, the Z-source DCLC inverter would produce a similar set of waveforms as for the Z-source NPC inverter under the same simulated fault conditions, since they share almost the same operating principles. Results for the Z-source DCLC inverter are therefore not explicitly shown.

With the testing now performed on a Z-source dual inverter implemented with either two dc sources or a single source plus triacs, Fig. 8-8 and Fig. 8-9 show the waveforms obtained with $M = 1$ and $T_0/T = 0$ set as the pre-fault parameters, and $M = 0.67$ and $T_0/T = 0.33$ set as the post-fault parameters. Clearly, the inverter transits smoothly to its post-fault boosted switching scheme immediately after the occurrence of the $SA_{(G)}$ short-circuit failure at $t = 40$ ms, with the three-phase line currents again kept virtually undisturbed except during the short one-cycle transitional period. Also noted in the figures are the modified three-level line and five-level phase switching waveforms, which obviously are different from those shown in Fig. 8-6 and Fig. 8-7. As explained

Fig. 8-9. Simulated waveforms of dual Z-source inverter with single dc source and triacs connected.

Fig. 8-10. Experimental waveforms of Z-source NPC inverter captured when SA'2 fails open-circuit.

in Section 8.3, these wave shapes introduce the third advantage of producing zero common-mode voltage (see third traces in Fig. 8-8 and Fig. 8-9) to the system, in addition to its ability in maintaining minimal harmonic distortion and constant output amplitude. (Note that the pre-fault condition simulated for the dual inverter can be modified to produce zero common-mode voltage if needed, but is not explicitly implemented here so as to keep the pre-fault conditions of all studied inverters on a single common comparative basis).

After confirming in simulation, a number of laboratory prototypes were constructed

Fig. 8-11. Experimental waveforms of Z-source NPC inverter captured when SA1 fails short-circuit.

using the same source and passive parameters as those used in simulation. Beginning by introducing a SA'2 open-circuit fault to the Z-source NPC inverter, Fig. 8-10 shows the experimentally captured results with $M = 1$ and $T_0/T = 0$ set as the pre-fault parameters, and $M = 0.67$ and $T_0/T = 0.33$ set as the post-fault parameters. Unarguably, the results shown in Fig. 8-10 are close to those shown in Fig. 8-6 with the ac line current restored back to its pre-fault value in slightly longer than one fundamental cycle. In spite of their observed close similarity, a minor difference is noted between the two figures in the sense that a reversal of phase voltage switching polarity is observed in Fig. 8-10, which no doubt is caused by emulating open-circuit failure of the lowermost switch SA'2, rather than the uppermost switch SA1 considered in Fig. 8-6. Next with SA1 considered to fail short-circuit in the Z-source NPC inverter, Fig. 8-11 shows the measured waveforms corresponding to the fault scenario simulated in Fig. 8-7. As explained, since two dc sources are still available for powering the inverter, the pre- and post-fault control parameters remain unchanged at $M = 1$ and $T_0/T = 0$, meaning that no voltage-boost is needed for riding through the fault.

Moving on to the dual inverter prototype, Fig. 8-12 and Fig. 8-13 show the waveforms captured for the cases of one and two dc sources used for powering the inverter. In common, both cases have their control parameters set to $M = 1$ and $T_0/T = 0$ before fault, and $M = 0.67$ and $T_0/T = 0.33$ after fault. These chosen parameters cause the ac

Fig. 8-12. Experimental waveforms of dual Z-source inverter with two dc sources connected.

line current to rise back to its pre-fault amplitude, and the adopted ride-through modulation scheme forces the inverter common-mode voltage to reduce to zero. Clearly, these observations match closely with those simulated in Fig. 8-8 and Fig. 8-9, hence confirming the effectiveness of the proposed ride-through schemes.

8.5 Summary

This chapter presents and evaluates fault tolerant strategies for a number of chosen three-level Z-source inverters with enough operating redundancies for riding through most fault scenarios. Particularly, for the Z-source NPC and DCLC topologies, simple three-level to two-level reconfiguration of their modulation schemes and tuning of their shoot-through durations are found to be an effective method that can be used for

Fig. 8-13. Experimental waveforms of dual Z-source inverter with single dc source and triacs connected.

Chapter 8 Performance Evaluation under Semiconductor Failure Conditions

riding through semiconductor faults with minimized waveform distortion and no dip in output voltage amplitude. The same concept can equally be used for improving the ride-through ability of the Z-source dual inverters supplied by either a single dc source with added triacs or two isolated dc sources, with a third advantage of producing zero common-mode voltage noted. For verifying these performance features, simulation and experimental testing were performed with closely matching results produced for all tested semiconductor failure conditions.

Chapter 9 AC-DC-AC Z-Source Converter

AC-DC-AC power converters are commonly used for converting the invariant ac utility grid supply to either a variable voltage/frequency output for powering ac motor drives or a user-specified regulated output for powering sensitive loads in an uninterruptible manner. Among the ac-dc-ac topologies that have been reported, those that use a front-end diode rectifier are competitively appealing because of its low cost, albeit at the expense of a loss in controllability at its ac input regardless of the dc-ac inverter topology connected after the front-end rectifier [43, 125].

In addition, using a passive diode rectifier is known to constrain the converter to operate in only the forward power transfer mode, and generally support only voltage-buck or boost operation, which to some extent constrains its disturbance (e.g. voltage sag and surge) ride-through ability. For a significant enhancement of the converter performance, either an actively controlled back-to-back converter or a dc-dc boost pre-regulator [126, 127], inserted between the input diode rectifier and output inverter, is recommended, but these solutions are generally expensive and harder to control due to the use of more actively controlled semiconductor switches, even though they usually cater for both bi-directional and buck-boost operation.

Offering an intermediate solution, [113] has proposed an ac-dc-ac converter, formed by cascading a two-level Z-source dc-ac inverter to a front-end diode rectifier, as depicted in Fig. 9-1. As firstly described in [1], the Z-source inverter allows the system output voltage to be stepped down or up as desired by inserting a unique X-shaped LC impedance network, comprising of two inductors and two capacitors, between the rectifier and inverter circuitries. On the diode rectifier ac input side, three small delta-connected filter capacitors are added for filtering the three-phase ac input currents so as to eliminate frequent high current peaks that are drawn by traditional diode rectifiers with large dc capacitive storages. The proposed Z-source converter

Fig. 9-1. Topology of two-level ac-dc-ac Z-source converter.

therefore appears as a compromising solution between the traditional ac-dc-ac diode-front-end converter and the back-back controlled converter, since it supports voltage buck-boost operation at a low cost, while constrained by its unidirectional energy conversion and a less than perfect input current waveform, which is still harmonically less distorted as compared to that drawn by a traditional diode rectifier.

Adding an alternative to the low cost intermediate approach, this chapter proposes the design of a three-level ac-dc-ac Z-source converter that can produce a three-level output waveform with the use of only minimal passive and semiconductor components for implementation. Specifically, the proposed converter uses only six diodes for its ac-dc rectification and only a single X-shaped LC impedance network for performing its buck-boost operation with no increase in its front-end element count as compared to that needed by the two-level converter documented earlier in [113] (see Fig. 9-1).

On its ac output end, the proposed converter uses a three-level dc-ac inverter, which can either be of the neutral-point-clamped or dc-link cascaded topology, now commonly adopted in the industry (at least for the former). That then infers that the proposed topology is no different from a traditional three-level inverter supplied passively by a front-end diode rectifier, except for the inclusion of a LC impedance network for flexible voltage buck-boost operation. Retrofitting of large number of existing converter systems is therefore possible, hence strengthening the likely adoption of the Z-source concept in the industry. But of course, some amount of distortion would still be present in the system caused by the front-end diode rectifier,

although that distortion would later be demonstrated to be lower than before performing the retrofit. Therefore comparatively, the proposed solution is a simple, low cost alternative with improved performance, while yet avoiding those complex (at times expensive) sensing, synchronization and feedback control circuitries associated with active front-end rectification.

Although not intuitively obvious, the neutral potential needed by the proposed three-level inverter circuitry can uniquely be tapped from the wye-connected filter capacitors placed before the front-end diode rectifier for input current filtering, with no explicit bulky split-capacitors, diodes and other passive components needed (unlike the two-level converter illustrated in Fig. 9-1, capacitors connected in delta cannot be used here because of the absence of a “hidden” neutral point that can only be found in a wye-connected configuration).

Through careful design of its modulation schemes, the proposed ac-dc-ac converter can be proven to operate with no significant increase in semiconductor commutations, and hence maintain a relatively low switching loss, as compared to that of a traditional three-level voltage-source (buck) inverter. The resulting ac-dc-ac converter therefore offers a low cost alternative that can ride-through deep voltage sags, while producing an improved three-level voltage waveform for powering the externally connected ac load. These findings have been verified experimentally using a scaled down laboratory prototype, and for better identification of contributions, the differences between this chapter and Chapter 4 are summarized as follow:

- Unlike Chapter 4 where only simpler dc-ac energy inversion is considered, this chapter focuses on the more challenging ac-dc-ac energy conversion with a low-cost topology proposed, using only a single LC impedance network, simple six-diode rectifier and small filter capacitors at its front-end.
- An effort is made towards investigating the cost saving option of tapping the neutral potential for three-level output switching from the star-point of the input filter capacitors. Likely tradeoffs are discussed to provide readers with

the necessary details before deciding on whether to adopt the converter for their specific applications.

- An effort to test and compare different modulation schemes for the proposed ac-dc-ac converter is performed using a common experimental platform.

Before beginning with the analytical studies, it is generally commented that the proposed ac-dc-ac technique is not discussed for the other three-level and five-level buck-boost topologies because it is not conceptually applicable to them based on the candidate's current level of understanding.

9.1 Review of Two-Level AC-DC-AC Converter

Fig. 9-1 shows the two-level ac-dc-ac Z-source converter, where a Z-source LC impedance network is connected between an input diode rectifier and an output inverter. Under normal ac input condition, the rear-end dc-ac inverter should preferably

Fig. 9-2. Equivalent circuits of two-level ac-dc-ac Z-source converter when in (a) non-shoot-through (active or null) and (b) shoot-through states.

be controlled to switch between the eight active and null states conventionally assumed by a two-level VSI. In these states, the overall converter can be represented by the equivalent circuit shown in Fig. 9-2(a), where only one upper rectifier diode (DR, DY or DW) with the highest anode potential and one lower diode (DR', DY' or DW') with the lowest cathode potential are shown conducting. With the diodes conducting, effectively one filter capacitor ($3C_f$) is connected across the input terminals of the Z-source network. On the other side of the Z-source network, the dc-ac inverter and its external inductive filter are represented by a current source, whose value is non-zero when in an active state and zero when in a null state.

Besides the above-described switching states and unlike a traditional VSI, the converter can assume a third shoot-through state upon sensing an ac input voltage sag while controlled to keep its output constant, or when an increase in ac output voltage is needed. Upon entering the normalized shoot-through interval T_0/T (where T represents the switching period), the rear-end dc-ac inverter is modulated to turn ON two switches from the same phase-leg simultaneously to create a short-circuit across its dc-link ($v_i = 0$ V) without damaging any semiconductor devices due to the presence of the two Z-source inductors.

While in the shoot-through state, the converter equivalent circuit is re-drawn as in Fig. 9-2(b), where an intended feature is to short-circuit the Z-source network, forcing $v_i = 0$ V. In addition, all rectifier diodes are drawn reverse-biased, effectively disconnecting the ac input source from the Z-source network. Using these equivalent representations and by equating the average Z-source inductive voltage per switching cycle to zero, it is proven in Section 3.2 that the converter peak dc link ($\hat{v}_i$) and ac output ($\hat{v}_x$, $x = A, B$ or C) voltages are expressed as:

$$\hat{v}_i = \frac{1}{1 - 2T_0/T} V_{in} = BV_{in}; \quad \hat{v}_x = M \frac{\hat{v}_i}{2} = B \left\{ M \frac{V_{in}}{2} \right\}; \quad V_{in} = \frac{3\sqrt{2}}{\pi} V_s = 1.35V_s \quad (9.1)$$

where V_{in} is the inherent dc voltage produced by the front-end rectifier fed from an

input source, whose line rms voltage is represented by V_s (voltage drop across the line impedance is neglected), M is the modulation ratio commonly used for VSI control, and $B (\geq 1)$ is the boost factor introduced by a non-zero shoot-through interval added for inductive voltage boosting.

Another issue that needs consideration, while introducing multiple shoot-through states to the converter switching sequence, is that the resulting normalized volt-sec average seen by the externally connected ac load must remain unchanged with the converter commutation frequency kept preferably unmodified (implying no significant increase in switching losses). A commutation technique that meets these criteria is illustrated in Fig. 9-3, where unlike traditional VSI, the commutation of phase A at the first transition is performed by turning SA ON earlier by $T_0/2T$ before turning SA' OFF at a later instant to enter state $\{1,0,0\}$. Doing so creates an overlapping interval during which SA and SA' are ON to short-circuit the inverter dc rails (see shaded gating signals in Fig. 9-3(b)).

Similarly, the second shoot-through state can effectively be inserted by turning SC ON, while delaying the turning OFF of SC' by $T_0/2T$ at the last transition. (Note that a third shoot-through state can be inserted between states $\{1,0,0\}$ and $\{1,1,0\}$, but this is not shown in Fig. 9-3 for clearer illustration). Obviously, this insertion method does not create additional device commutation, but simply relies on the re-timing of existing commutations in a switching cycle. In addition, the total active duration is clearly kept

Fig. 9-3. State sequences and gating signals for controlling (a) traditional and (b) Z-source two-level converters.

constant, and by noting that both shoot-through and null states produce the same set of zero three-phase line voltages, the derived Z-source state sequence is expected to have the same normalized volt-sec average.

9.2 Topology of Three-Level AC-DC-AC Z-Source Converter

While extending the ac-dc-ac Z-source energy conversion concept to a three-level NPC (or DCLC) system with a better conditioned ac output voltage, it is important to keep the passive and semiconductor element counts low so as to preserve its low cost characteristics. In addition, the front-end rectifier of the designed converter must now have a third neutral terminal for powering the rear-end NPC inverter with three-level switching characteristics. Fulfilling these design considerations, Fig. 9-4 shows the proposed ac-dc-ac converter, where in principle, a three-level NPC inverter is cascaded to the output of a single Z-source LC impedance network. The input of the Z-source network is in turn connected to a three-phase diode-bridge rectifier, whose input currents are smoothed by a set of wye-connected filter capacitors.

Note that a wye-connected network is used here, instead of the delta arrangement shown in Fig. 9-1 for the two-level system, because it offers a simple way for extracting the neutral potential needed by the rear-end NPC inverter by simply connecting the capacitive star-point to each of the inverter diode-clamping arms,

Fig. 9-4. Topology of proposed ac-dc-ac Z-source NPC converter.

Fig. 9-5. Normalized envelope variations per source fundamental cycle at the (a) input and (b) output ends of the Z-source network measured with reference to the input capacitive star-point.

without the need for additional bulky split-capacitors and diodes connected before the Z-source network. This natural formation of a neutral potential is better illustrated by analyzing equivalent circuits assumed by the converter in different switching states.

But before performing the analysis, a quick view of the converter would reveal that besides the standard additional semiconductor switches and clamping diodes needed for implementing three-level dc-ac switching, the number of rectifier diodes and passive elements used remains the same as that shown in Fig. 9-1 for a two-level system. Because of this, the extra cost incurred by the proposed converter is comparable to that needed for upgrading a traditional inverter from two-level to three-level switching, and comparing to the technique reported in Section 4.1, where two Z-source networks are used for implementing a dc-ac Z-source NPC inverter, it represents a significant cost saving since lesser passive LC components are used. (In Section 4.1, only dc-ac energy conversion is considered, but ac-dc-ac conversion can intuitively be derived by adding two diode-bridge rectifiers with 12 diodes in total and an isolated transformer with two sets of three-phase secondary windings to the dc-ac circuit. These items, together with the two Z-source networks used, collectively render the technique presented in Section 4.1 being a costly solution for ac-dc-ac energy conversion).

But surely, the use of only a single impedance network and without any additional split-capacitors, diodes and passive components for forming the neutral potential would incur some performance degradations, mainly linked to the larger low-order envelope variations measured within the intermediate dc stage. To be more specific, the positive voltage fed by the rectifier to the input end of the Z-source network would have a three-pulse maximum envelope per fundamental cycle imposed by diodes DR, DY and DW. Similarly, the negative voltage would have a matching, 60°-phase-shifted minimum envelope imposed on it by diodes DR', DY' and DW'. These variations are shown in Fig. 9-5, which also includes their influences at the output end of the Z-source network, whose reasoning behind is better explained at a later stage after understanding the converter modulation principles presented in the next two sections. In spite of the variations, the proposed method of forming a capacitive neutral star-point is definitely stable with its adoption for three-level matrix converters already reported in [128-130] at about the same time as this work, if not subsequently (also briefly mentioned in the conclusion of [131] without any conceptual explanation and proving given).

Despite its lower LC component count and the absence of explicit split capacitors, the proposed converter can still boost its ac output voltage to a comparably high value for riding through voltage sags or tracking a higher command reference by introducing shoot-through states to its modulation scheme to create two distinct operational modes. These operational modes are broadly referred to as shoot-through and non-shoot-through states, where the latter collectively represents the 27 active and null switching states that can be assumed by a traditional NPC inverter by gating its phase-legs according to Table 9-1. In total, two different modulation schemes can be formulated, and are respectively referred to as full dc-link (FDCL) and partial dc-link (PDCL) shoot-through schemes. Both schemes are described next in the following sections with two additional shoot-through states, not previously reported with the two-level Z-source converter, identified for the PDCL-controlled three-level Z-source converter.

Table 9-1. Example switching states of Z-source NPC converter and their corresponding phase-leg voltage values V_X ($X, Y = A, B$ OR $C, X \neq Y$).

State Type	ON Switches	V_X
Non-Shoot-Through	SX1, SX2	$\approx +v_i/2$
Non-Shoot-Through	SX2, SX'1	0
Non-Shoot-Through	SX'1, SX'2	$\approx -v_i/2$
Full Shoot-Through	SX1, SX2, SX'1, SY2, SY'1, SY'2	0
Upper Shoot-Through	SX1, SX2, SX'1	0
Lower Shoot-Through	SX2, SX'1, SX'2	0

9.3 Full DC-Link Shoot-Through Scheme

When commanded to enter a non-shoot-through state, the converter front-end equivalent circuit can again be drawn as the conduction of one upper diode with the highest anode potential and one lower diode with the lowest cathode potential since the

Fig. 9-6. Equivalent circuits of three-level ac-dc-ac Z-source NPC converter when in (a) non-shoot-through and (b) full dc-link shoot-through states.

same low cost diode rectifier as in Fig. 9-1 is used. Together, both conducting diodes connect a pair of filter capacitors across the Z-source input terminals, where the mid-point (star-point) of the capacitors clearly forms the neutral potential to which the rear-end clamping diodes are linked (see Fig. 9-6(a)). Using the newly created dc voltage levels of $+v_i/2$, 0 and $-v_i/2$ (ignoring voltage envelope variations for the time being), the rear-end NPC inverter can now switch to any of the 27 possible active and null states, during which the Z-source inductors discharge their stored magnetic energy for boosting the total power delivered to the external load.

While powering the load, the Z-source capacitors are also charged to their peak steady-state value before releasing their stored electrostatic energy in the next operational mode for powering the FDCL shoot-through equivalent circuit shown in

Fig. 9-7. Non-optimized FDCL scheme for controlling ac-dc-ac Z-source NPC converter: (a) state sequence generation and (b) shoot-through insertion at the first state transition.

Fig. 9-6(b). Specifically in Fig. 9-6(b), the shoot-through equivalent circuit is drawn with a FDCL short-circuit appearing across the Z-source impedance network ($v_i = 0$), and with all input diodes drawn reverse-biased for naturally disconnecting the ac source from the Z-source impedance network. Having no source and load connected to it, the net energy stored in the Z-source network is expected to remain unchanged (assuming a loss-less network), implying that electrostatic energy released by the Z-source capacitors must fully be recaptured as magnetic energy stored in the inductors, getting them ready for inductive voltage boosting in the next non-shoot-through state.

Comparing the three-level equivalent circuits shown in Fig. 9-6 with those in Fig. 9-2 for a two-level system, the close similarities between the two sets of circuits directly

Fig. 9-8. Optimized FDCL scheme for controlling ac-dc-ac Z-source NPC converter: (a) state sequence generation and (b) shoot-through insertion at the first state transition.

imply that the boosted peak dc-link voltage and ac output voltage of the proposed three-level ac-dc-ac converter are again expressed by (9.1), where inductive voltage boosting is affected by setting $B > 1$ and $T_0/T \neq 0$. Theoretically, $T_0/T \neq 0$ can be implemented by placing shoot-through states anywhere within the switching cycle as long as the resulting volt-sec average is kept constant, but practically, a method that can insert FDCL shoot-through with the lowest commutation count per switching cycle is desired since it minimizes the converter switching losses.

While designing the method with the lowest commutation count, a criterion described in Section 9.1 is similarly applied, which states those shoot-through states must be inserted with no volt-sec error introduced. Noting also that a FDCL shoot-through state would inevitably introduce a short-circuit across the rear-end inverter dc-link, causing its three-phase output to appear as a set of zero line voltages, a preliminary base from which appropriate modulation scheme can be formulated is shown in Fig. 9-7(a), where a set of three-phase sinusoidal references (V_a, V_b, V_c) is compared with two vertically disposed and 180°-phase-shifted carriers.

Obviously, the produced state sequence has two null {0,0,0} states with zero line voltages placed at the start and end of each switching cycle, implying that FDCL shoot-through states can appropriately be inserted within these intervals without introducing any volt-sec error (total active time kept constant), while still producing the desired voltage boosting. But using this sequence directly without modification cannot guarantee a minimal commutation count because the most probable way of introducing a FDCL shoot-through state to (e.g.) the first state transition between {0,0,0} and {1,0,0} is by turning ON all switches from phase A simultaneously, as depicted in Fig. 9-7(b). Comparing the commutation counts of the two sequences in Fig. 9-7(b) reveals that two additional device commutations are introduced by each inserted shoot-through state, which definitely is unfavorable for high switching frequency.

To avoid additional device switching, a simple, but not visibly obvious, technique is proposed, which can pictorially be viewed as the adding of a triplen offset $V_{off} = -0.5(\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c))$ to the original references for creating an alternative state sequence. As observed from Fig. 9-8(a), a unique feature of the modified sequence is that the first and last transitions are initiated by switching phases A and C simultaneously with the total commutation count per switching cycle still kept at 12. Having two phases switched simultaneously allows FDCL shoot-through states to be inserted at the first and last transitions of a full switching period without an increase in commutation count (see Fig. 9-8(b) for an illustration of shoot-through insertion at the first transition, where the commutation count remains at four). This is because a shorted path can now be formed by (e.g.) turning SA1, SA2 and SA'1 from phase A ON and SC2, SC'1 and SC'2 from phase C ON during each shoot-through interval of T_0/T . For a clearer illustration, the short-circuit path formed by the synchronized switching of phases A and C is shown in Fig. 9-9, which certainly offers a means for minimizing commutation count if FDCL shoot-through insertion is desired.

Note that this method of shoot-through insertion will not unnecessarily raise the blocking voltage requirement of the rear-end inverter switches because at the instant of shoot-through insertion, v_i , which also represents the blocking voltages across

Fig. 9-9. Illustration of shoot-through path with minimized commutation count.

non-conducting switches SA'2 and SC1, immediately collapses to zero. No raising of current-carrying requirement is also noted since currents flowing along all possible dc flow paths are effectively limited by the added Z-source inductors. Therefore, the rating of the switches is solely determined by the non-shoot-through state, which in turns means that the sizing approach recommended is similar to that imposed on a traditional NPC inverter (with a dc-dc boost converter connected at its front-end to step-up v_i if voltage-boosting operation is needed) with each switch expected to block half the dc-link voltage v_i , and carry the maximum load current.

Another point to note with the proposed modulation scheme is that it is more appropriate for use in applications with high operating frequency, where its minimized commutation count would have significant advantages. A number of recent likely examples are reported in [113, 127], where low power NPC inverters are investigated for drives, traction and utility adoptions. On the other hand, the proposed scheme is not

Fig. 9-10. Equivalent circuits of three-level ac-dc-ac Z-source NPC converter when in (a) upper shoot-through and (b) lower shoot-through states.

particularly suitable for low frequency operation because of its higher conduction loss with six transistors and two clamping diodes connected in series for forming the rear-end short-circuit. For this range of applications, the obvious approach of turning four switches from the same phase-leg ON (discussed earlier) is a more viable option since only four devices are in series for forming the short-circuit, albeit with a higher commutation count. In short, the right choice to make for any particular case under consideration would depend on the tradeoffs imposed, and the specific device characteristics chosen for implementation. In spite of that, the minimal commutation scheme proposed here is no doubt not a visibly obvious technique, which surely must be described in details, instead of leaving it to the readers to perceive.

9.4 Partial DC-Link Shoot-Through Scheme

Instead of inserting FDCL shoot-through, the topological structure of the proposed three-level converter allows alternative PDCL shoot-through states to be inserted for attaining the same voltage gain, while producing a better output waveform quality. The alternative PDCL states are shown in Fig. 9-10(a) and (b) respectively, where the former represents an upper shoot-through with (e.g.) SA1 = SA2 = SA'1 = DA2 = ON, and the latter represents a lower shoot-through with SC2 = SC'1 = SC'2 = DC1 = ON. In both states, $v_i \neq 0$, and only one input diode naturally reverse-biases, while the other remains ON (DR = ON, DW' = OFF for upper shoot-through, and DR = OFF, DW' = ON for lower shoot-through). Because of these characteristics, analysis for the proposed ac-dc-ac converter is performed here with its respective state equations in different states written from (9.2) to (9.4), assuming a symmetrical impedance network with $L_1 = L_2 = L$ and $C_1 = C_2 = C$, and ignoring the envelope variations shown in Fig. 9-5 for the time being, whose influences on the system are discussed near the end of this section:

Non-Shoot-Through Fig. 9-6(a):
$$v_L = V_{in} - V_C \quad (9.2)$$

Upper-Shoot-Through Fig. 9-10(a):
$$v_L = V_{in} / 2 \quad (9.3)$$

Lower-Shoot-Through Fig. 9-10(b): $v_L = V_{in}/2$ (9.4)

Applying state-space-averaging to (9.2) to (9.4), and by setting equal time span of $0.5T_0'/T$ for balanced voltage boosting of both PDCL states, the relevant expression for V_C is derived as:

$$(V_{in} - V_C)(1 - T_0'/T) + (V_{in}/2)(T_0'/(2T)) + (V_{in}/2)(T_0'/(2T)) = 0 \Rightarrow$$

Fig. 9-11. PDCL scheme for controlling ac-dc-ac Z-source NPC converter: (a) state sequence generation, (b) upper shoot-through insertion at the first state transition, and (c) lower shoot-through insertion at the third transition.

$$V_C = \frac{1 - T_0'/T}{1 - T_0'/T} V_{In} \quad (9.5)$$

Using (9.5), the governing dc-link voltages in different converter states are deduced as:

Non-Shoot-Through Fig. 9-6(a):

$$\begin{cases} v_{(+ve)} = V_C - V_{In}/2 = 0.5V_{In}/(1 - T_0'/T) \\ v_{(-ve)} = -V_C + V_{In}/2 = -0.5V_{In}/(1 - T_0'/T) \end{cases} \quad (9.6)$$

$$\hat{v}_i = v_{(+ve)} - v_{(-ve)} = V_{In}/(1 - T_0'/T) = B'V_{In}$$

Upper-Shoot-Through Fig. 9-10(a):

$$\begin{cases} v_{(+ve)} = 0 \quad (\text{Shorted to the neutral star-point}) \\ v_{(-ve)} = -V_C + V_{In}/2 = -0.5V_{In}/(1 - T_0'/T) \end{cases} \quad (9.7)$$

Lower-Shoot-Through Fig. 9-10(b):

$$\begin{cases} v_{(+ve)} = V_C - V_{In}/2 = 0.5V_{In}/(1 - T_0'/T) \\ v_{(-ve)} = 0 \quad (\text{Shorted to the neutral star-point}) \end{cases} \quad (9.8)$$

where $v_{(+ve)}$ and $v_{(-ve)}$ represent the dc-rail potentials measured with respect to the zero neutral point, indicated in Fig. 9-6 and Fig. 9-10, and $B' (= 1/(1 - T_0'/T))$ represents the boost factor for the PDCL scheme. Clearly, the last equation in (9.6) shows that the peak dc-link voltage imposed across the external load during non-shoot-through active states is the same as that expressed in (9.1) for two-level and FDCL-controlled three-level converters, as long as T_0'/T is set to $2T_0/T$ to make $B' = B$. Also noted from (9.6) to (9.8) is that the converter three-phase line voltages will never fall to zero simultaneously, meaning that an alternative carrier arrangement, without state $\{0,0,0\}$ generated, might offer a better solution, as compared to that shown in Fig. 9-8(a), where the nearest space vectors are not solely used for reference generation. Therefore, instead of Fig. 9-8(a), alternative vertically disposed carriers with zero phase-shift between them are used with their typical relative placements and resulting state sequence produced shown in Fig. 9-11(a).

By analyzing the three state transitions per half carrier cycle shown in Fig. 9-11(a), appropriate instances for inserting upper and lower shoot-through states without introducing extra commutations are noted, and drawn in Fig. 9-11(b) and (c). For the

former, an upper shoot-through state is inserted to the left of the first phase A transition by advancing the turning ON of switch SA1 by $0.5T_0/T$, while keeping the turning OFF instant of its complementary switch SA'1 unchanged (see circled gate signals in Fig. 9-11(b)). Doing so creates an intermediate interval with $SA1 = SA2 = SA'1 = DA2 = ON$ for shorting the upper dc-link with the commutation count kept constant at 2. In addition, mapping of the converter phase-leg voltages in the first non-shoot-through state $\{0, -1, -1\}$ and its adjacent upper shoot-through state reveals that their voltage levels remain unchanged in both states, since the negative dc-rail potential, to which phases B and C are tied, remains unchanged even when effecting the upper shoot-through (see (9.2) and (9.3)). Overlapping of the $\{0, -1, -1\}$ state by the upper shoot-through state to the left of the first transition therefore will not introduce any volt-sec error.

Similarly, by delaying the turning OFF of SC'2 by $0.5T_0/T$ at the third state transition, while preserving the turning ON instant of its complementary switch SC2, a lower shoot-through state with $SC2 = SC'1 = SC'2 = ON$ is inserted to the right of that transition with the commutation count again kept unchanged. Noting that the lower shoot-through overlaps the fourth $\{1, 0, 0\}$ state and that the positive dc-rail potential remains unaltered during the shorting of the lower dc rail (compare (9.2) and (9.4)), no volt-sec error is again expected since both $\{1, 0, 0\}$ and lower shoot-through states give rise to the same converter phase-leg voltages. Generalizing the above analysis to the other sextants of a full fundamental reference cycle, the generic rules governing the insertion of shoot-through states for the PDCL scheme can therefore be summarized as:

- **Upper** shoot-through state should be inserted to the **left** of the transition triggered by the **maximum** sinusoidal reference.
- **Lower** shoot-through state should be inserted to the **right** of the transition triggered by the **minimum** reference.

Before ending the conceptual analyses, a likely visible feature to be noted from the

captured experimental results is discussed here to facilitate understanding when studying the results. As noted earlier in Section 9.1 and illustrated in Fig. 9-5(a), the input voltages (measured with reference to the filter capacitive star-point) fed to the single Z-source network have a maximum v_{InU} and a minimum envelope v_{InD} imposed by the front-end diode rectifier. The influences of these variations on voltages $v_{(+ve)}$ and $v_{(-ve)}$ (also measured from the capacitive star-point) at the output end of the Z-source network can be deduced by considering the instantaneous variants of (9.6) in the non-shoot-through state, which are equally valid for both FDCL and PDCL schemes. Beginning with the first equation in (9.6), the instantaneously measured $v_{(+ve)}$ is expected to exhibit a maximum envelope that resembles the minimum envelope of v_{InD} since $v_{(+ve)} = V_C - v_{InD}$. Similarly, $v_{(-ve)}$ is expected to have a minimum envelope that matches in shape with v_{InU} since $v_{(-ve)} = v_{InU} - V_C$. These dc-link variations are shown in Fig. 9-5(b) for the case of no shoot-through insertion, where three concave arcs per fundamental cycle are noted for both the positive and negative envelopes.

Needless to say, the variations are expected to distort the converter ac output as the modulation ratio M increases, but it nonetheless represents a tradeoff (almost always experienced by reduced element count circuitries) incurred by gaining three-level switching with no additional front-end split-capacitors and other passive components needed. Also worth mentioning is that as the boost factor increases to raise V_C and the converter ac output, the dc-link envelope variations would appear comparatively smaller, hence giving rise to a set of smoother ac output waveforms. (Surely, the dc-link variations can be measured and compensated to produce smoother waveforms, but it would impose sensor cost and computational burden, which are both not in line with the low cost, reduced element count focus of the chapter. The method of compensation is thus left for a future investigation).

Fig. 9-12. Experimental voltage and current waveforms of the FDCL-controlled ac-dc-ac Z-source NPC converter under normal grid operating condition with $M = 1.15$ and $T_0/T = 0$.

9.5 Experimental Verification

The proposed three-level ac-dc-ac Z-source converter was tested experimentally using an implemented laboratory prototype. Semiconductor diodes and insulated gate bipolar transistors used for building the hardware were purchased from *Semikron*, while the hardware Z-source network was assembled using 6.3 mH inductors and 2200 μF capacitors found in the laboratory. For powering the converter, an ac power supply with variable amplitude was connected to the converter input through an ac LC filter used for suppressing switching frequency harmonics ($L_f = 1$ mH and $C_f = 15$ μF in Fig. 9-4). The constructed power stage was next interfaced to a control platform with a digital signal processor onboard used for processing either the FDCL or PDCL modulation scheme. Both schemes, when used for driving the ac-dc-ac Z-source converter, produce noticeable differences, whose details are described as follow.

Fig. 9-13. Experimental voltage and current waveforms of the FDCL-controlled ac-dc-ac Z-source NPC converter under normal grid operating condition with a reduced $M = 0.7 \times 1.15$ and $T_0/T = 0$.

9.5.1 FDCL Shoot-Through Scheme

Under normal operating condition, the ac source was set to 120 V (line-rms) with a frequency of 60 Hz, and for efficient utilization of the dc-link, the converter modulation ratio M was set to 1×1.15 with its shoot-through time T_0/T set to zero (shoot-through state was intended for use only under voltage sag condition). Also, for illustration of the frequency conversion ability of the proposed ac-dc-ac converter, its output frequency was set to a different value of 50 Hz. With these settings, Fig. 9-12 shows the experimentally captured input and output waveforms, where five-level line voltage and three-level phase voltage switching are observed at the converter output with the correct 60→50 Hz frequency conversion performed. Neat single-level line voltage switching is however not observed here because as noted from Fig. 9-8, the nearest three space vectors are not solely used here for the FDCL scheme.

Also noted at the output of the converter is the concave envelope of the phase-leg

voltage, obtained by switching the rear-end inverter to either a dc-link potential ($v_{(+ve)}$ or $v_{(-ve)}$) or the capacitive neutral point, to give slightly more than one and the half concave arcs per positive or negative half cycle (noting the slightly longer period of the output as compared to the input). The concave arcs, analytically predicted at the end of Section 9.4, are similarly reflected on the output current trace, and are noted to drift as time progresses because of the non-integer ratio set for the input and output frequencies. For illustrating a second feature deduced in Section 9.4, the experimental plots for M reduced to 0.7×1.15 and with T_0/T kept at 0 are also captured, and consolidated in Fig. 9-13, where the envelope arcing is again observed to affect the phase-leg waveform. However, the arcing influence on the ac output current is observed to be less significant because of the lower M used, which clearly agrees well with the conclusion drawn at the end of Section 9.4. At the converter input end, the illustrated line current waveforms in both Fig. 9-12 and Fig. 9-13 are also noted to be less than sinusoidal because of the converter low cost nature, where only a single impedance network and a simple diode front-end rectifier is used. But comparing with the periodic huge current spikes drawn by a diode rectifier with a large storage capacitor, the current drawn by the proposed ac-dc-ac converter is relatively less distorted.

Next, with the ac source voltage lowered to 70 V (line-rms) for emulating a prolonged voltage dip, the converter control parameters are re-tuned to $M = 0.65 \times 1.15$ and $T_0/T = 0.35$, giving a boost factor of $B = 3.33$. Using these re-tuned parameters, Fig. 9-14 shows the recaptured set of experimental voltage and current waveforms, which clearly show that the same output current amplitude of approximately 2 A (see fifth plot in Fig. 9-12 for a comparison) can be produced even when the input voltage falls by 42% ($=100\% \times (120-70)/120$) with the rest of the system kept unchanged. Therefore, to the connected load, the system appears undistorted with its energy demand being continuously met by an accompanied increase in input current (see second plot in Fig. 9-14) during the interval of voltage sag.

Fig. 9-14. Experimental voltage and current waveforms of the FDCL-controlled ac-dc-ac Z-source NPC converter under voltage sag condition with $M = 0.65 \times 1.15$ and $T_0/T = 0.35$.

9.5.2 PDCL Shoot-Through Scheme

Using the same input and control parameters of 120 V (line-rms), 60 Hz, $M = 1.15$ and $T_0/2T = 0$ for normal operating mode, Fig. 9-15 shows the corresponding input and output waveforms of the converter when the PDCL shoot-through scheme is used. For evaluating the predicted envelope variations with changes in M , the second scenario of M reduced to 0.7×1.15 and T_0/T kept at 0 is also tested with the results plotted in Fig. 9-16. Comparing with those shown in Fig. 9-12 and Fig. 9-13, virtually the same input waveform quality is noted in Fig. 9-15 and Fig. 9-16 using the PDCL scheme, but on the converter output end, notable improvements are observed with the two line voltage waveforms, shown as third traces in both figures. To be specific, the line voltage waveforms now exhibit neat single-level switching with the dc-link envelope variations observed to have lower impact on the ac output current as M reduces.

Illustration of advantages linked to this single-level switching is more prominent under

voltage sag condition, during which M is reduced and shoot-through states are inserted to give the boosting results shown in Fig. 9-17. In that figure, the input voltage is lowered to 70 V (line-rms), and the control parameters are re-tuned to $M = 0.65 \times 1.15$ and $T_0/2T = 0.35$. Again, virtually the same input waveforms are noted in both Fig. 9-14 and Fig. 9-17, but when comparing their output performances, a better rear-end line voltage switching is observed in Fig. 9-17, where the PDCL scheme is used. Specifically, the single-level line voltage switching in Fig. 9-17 gives rise to a smaller high frequency current ripple superimposed on the output current waveform (fifth trace), whose fundamental amplitude is controlled to the pre-sag value of approximately 2 A.

Fig. 9-15. Experimental voltage and current waveforms of the PDCL-controlled ac-dc-ac Z-source NPC converter under normal grid operating condition with $M = 1.15$ and $T_0/T = 0$.

Fig. 9-16. Experimental voltage and current waveforms of the PDCL-controlled ac-dc-ac Z-source NPC converter under normal grid operating condition with a reduced $M = 0.7 \times 1.15$ and $T_0/T = 0$.

Fig. 9-17. Experimental voltage and current waveforms of the PDCL-controlled ac-dc-ac Z-source NPC converter under voltage sag condition with $M = 0.65 \times 1.15$ and $T_0/T = 0.35$.

9.6 Summary

This chapter presents the design of a low cost Z-source NPC converter that can perform buck-boost ac-dc-ac energy conversion. Conceptually, the converter is constructed by cascading a NPC inverter through a single Z-source impedance network to a front-end diode rectifier. At the ac input of the diode rectifier, three wye-connected filter capacitors are used for smoothing out periodic current spikes that are frequently drawn by diode rectifiers with large capacitive energy storages, and for providing the neutral potential needed by the rear-end NPC inverter for three-level phase voltage switching. Modulation wise, the proposed converter can be modulated using either the FDCL or PDCL shoot-through scheme with no increase in device commutation needed and the correct normalized volt-sec average always produced. These findings, together with the practicality of the converter, have been tested experimentally in the laboratory under both normal and voltage sag conditions.

Chapter 10 Conclusions and Recommendations

10.1 Conclusions

This thesis addresses the challenging topics of topological and modulation design of buck-boost multilevel inverters. The development starts with the design of a pulse-width modulated Z-source NPC inverter with either two or a single Z-source network coupled between its input dc sources and NPC inverter circuitry, needed for inductive boosting of its output voltage when necessary. In total, three modulation schemes are discussed, and are respectively named as PD, APOD and RCM modulation schemes. Despite them exhibiting different operating advantages, they in common function by introducing unique shoot-through states to the inverter state sequence, which otherwise consists only of the traditional active and null states. While inserting the shoot-through states, attention is also devoted to sequence the states appropriately so that all the presented modulation schemes operate with the minimum of six device commutations per half carrier cycle, without introducing any normalized volt-sec error to the inverter ac output.

For the case of a Z-source NPC inverter powered by a single Z-source network, additional partial shoot-through states are also identified, which when used in place of the full dc-link shoot-through states, allows the inverter to function with optimized harmonic performance, while using reduced number of passive components. Therefore, in terms of optimizing both cost and performance, the proposed Z-source NPC inverter using only a single LC impedance network represents the ideal choice to adopt, and can even be used for constructing an ac-dc-ac converter, utilizing minimized number of diodes and a specially created capacitive neutral point. However, if fault ride-through ability is desired, the single Z-source NPC inverter is not viewed as a wise choice because of its lack of operating redundancies, imposed by its inclusion of

only a single LC impedance network, as explained in the introduction of Chapter 8. Instead, adding a second impedance network to the inverter offers a better solution since it can ride through most faults without any appreciable degradation in performance except for cases whereby the inner inverter switches fails open-circuit.

Next, using knowledge acquired from two-level Z-source inverter and by cascading two of them in series, new three-level Z-source dc-link cascaded and dual inverters are designed with them again controlled using modulation schemes with shoot-through states inserted. Among the two topologies discussed, special emphases are devoted to the Z-source dual inverter since it is proven that by using either the PSC or RCM modulation scheme with an appropriate offset added, the dual inverter can simply be powered by a single Z-source network without any volt-sec error introduced. In addition, if the appropriate fault ride-through scheme is programmed to the inverter control platform, the dual inverter can ride through all fault conditions with no prominent degradation in waveform quality and amplitude, while at the same time, preserving zero common-mode voltage during the fault interval. Therefore, judging from the angles of cost and performance, the single Z-source dual inverter represents a competitive option for consideration so long as the transformer at its ac output end is not a major concern.

Other than the Z-source energy conversion concept, the Ćuk and SEPIC conversion theories can also be extended to design new three-level buck-boost inverters. Again topological variants like NPC, DCLC and dual inverters are explored with the DCLC configuration noted to benefit from semiconductor saving and a lower switching loss. On the other hand, the dual inverter is shown to be the most flexible with many different advantages obtainable by simply downloading the right modulation scheme to the inverter. In spite of their performance differences, these newly derived Ćuk and SEPIC-derived three-level inverters can again be controlled using modulation theories inferred from those of Z-source inverter discussed earlier with comparably matching results obtained. In addition to showing matching results, an important feature

demonstrated from the captured results is the generic portability of the proposed modulation schemes, allowing them to control any three-level buck-boost inverters using only a single common hardware platform.

Besides three-level inverters, focus is also devoted to analyze the possibility of developing higher level buck-boost inverters. Unfortunately, nearly all the examined buck-boost theories fails to simultaneously meet the basic requirements of simplicity, low cost, good waveform quality and optimized number of voltage level switching, except for the Z-source energy conversion concept. Using this only feasible concept, a new five-level Z-source diode-clamped inverter is proposed, and is structurally powered by two split-dc sources and two Z-source impedance networks. Unlike most Z-source inverters, this five-level Z-source inverter functions by inserting partial shoot-through states rather than full dc-link shoot-through, and is again verified to produce the anticipated results when either the PD or APOD modulation scheme is used for controlling it.

10.2 Recommendations for Further Research

Indeed, quite a sizable amount of materials has already been covered by this Ph.D. investigation, but like most other topics of investigation, no firm ending point can strictly be placed on the research of buck-boost multilevel inverters, which is still viewed as a relatively new area of investigation for dc-ac and ac-dc-ac energy conversion. Although not extensive, a number of possible immediate topics that can be thought of for future investigation are briefly summarized as:

1. The diode-assisted energy conversion concept presented in Chapter 3 has so far been developed for two-level inverters only with its extension to higher level buck-boost inverters not yet been explored. Surely, that represents a good topic for future investigation, since the doubling of voltage gain exhibited by the diode-assisted network might favor certain applications.

2. Concepts proposed in the thesis are mainly devoted to the inverter steady-state modulation, and not to their transient performance. Although relevant transient analysis has previously been studied for two-level Z-source inverters, its extension to higher level inverters might not be that straightforward, and might need some fine tuning. This investigation is unarguably challenging since it is expected to open up a new topic on dynamic control of buck-boost inverters with better conditioned output waveform quality.
3. Although the inverter topologies proposed in the thesis have already been proven to function well, their economical implementation issues have not yet been addressed to an appropriate extent that justifies their wide-spread commercial applications. That means further exploration of the component choices, integrating and packaging issues, efficiency measurement, and electromagnetic interference quantification need to be performed before their final commercial values and targeted markets can be determined.
4. All inverter topologies presented in the thesis are derived from the voltage-type configuration, which traditionally has been identified as the more popularly adopted option. Despite this popularity, there might still be cases, where the current-type configuration is preferred, and to address that preference, future investigation of current-type buck-boost inverters is also recommended as a possible topic for future investigation.
5. As mentioned in Chapter 1 and occasionally highlighted in the other chapters, the proposed multilevel Z-source inverters (mostly three-level) are designed with the renewable industry in view, where their improved waveform quality is expected to better match those continuously tightened power quality codes set for grid interconnection. For this planned interfacing to the grid, high frequency switching in the range of 5 to 20 kHz is reasonably common, and the tracking of maximum power points of individual PV panels is at times pursued, as discussed in [132]. Noting further is the observation that semiconductor devices found in renewable grid inverters might not require special design or protection by snubber circuits

Chapter 10 Conclusions and Recommendation

because of its lower voltage level. Therefore, these design issues are not pursued to any extent in the thesis. (For justifying the lower voltage consideration adopted in the thesis, readers can refer to [4] and [5], where three-level inverters have been reasoned as competitive alternatives for lower voltage motor drives, traction systems and grid converters, instead of their more traditional medium voltage applications). Another reason for not pursuing sizing and design issues related to higher voltage applications is linked to the lack of facilities at the host university for verifying higher voltage design. Therefore, the practical design of inverters for sustaining higher voltage has to be left for the investigation by other researchers with the appropriate laboratory supports.

Author's Publications

Premium Journal Publications

1. Poh Chiang Loh, Sok Wei Lim, **Feng Gao** and Frede Blaabjerg, "Three-level Z-source inverters using a single LC impedance network," *IEEE Trans. Power Electron.*, vol. 22, pp. 706-711, Mar. 2007.
2. Poh Chiang Loh, **Feng Gao**, Frede Blaabjerg, Shi Yun Feng and Jamies Soon, "Pulse-Width Modulated Z-Source Neutral-Point-Clamped Inverter," *IEEE Trans. Ind. Applicat.*, vol. 43, no. 5, pp. 1295-1308, Sep./Oct. 2007.
3. **Feng Gao**, Poh Chiang Loh, Frede Blaabjerg and D. Mahinda Vilathgamuwa, "Dual Z-source Inverter with Three-Level Reduced Common Mode Switching," *IEEE Trans. Ind. Applicat.*, vol. 43, no. 6, pp. 1579-1608, Nov/Dec. 2007.
4. Poh Chiang Loh, **Feng Gao** and Frede Blaabjerg, "Topological and Modulation Design of Three-Level Z-Source Inverters," *IEEE Trans. Power Electron.*, in press.
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6. Poh Chiang Loh, **Feng Gao**, Pee Chin Tan and Frede Blaabjerg, "Three-Level AC-DC-AC Z-Source Converter Using Reduced Passive Component Count," *IEEE Trans. Power Electron.*, in press.
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11. **Feng Gao**, Poh Chiang Loh, Frede Blaabjerg and D Mahinda Vilathgamuwa, "Performance Evaluation of Three-Level Z-Source Inverters Under Semiconductor Failure Conditions," *IEEE Trans. Ind. Applicat.*, in press.

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2. **F. Gao**, P. C. Loh, D. M. Vilathgamuwa, and F. Blaabjerg, "Performance Analysis of Random Pulse-Width Modulated Z-Source Inverter with Reduced Common Mode Switching," in *Proc. IEEE-PESC'06*, 2006, pp. 1-7.
 3. P. C. Loh, **F. Gao**, and F. Blaabjerg, "Topological and Modulation Design of Three-Level Z-Source Inverters," in *Proc. IEEE-IPEMC'06*, 2006, pp. 1-5.
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