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**Study of Erbium Disilicide and its application in Schottky
Source/Drain Silicon Nanowire MOSFETs**

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ABSTRACT

For ideal scaling, per generation (~3 years), a 0.7x reduction in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) dimensions is necessary to produce circuits with increased performance at reduced cost. 2 particular scaling factors to consider are : (1) source/drain (S/D) scaling which leads to increasing contact resistance (R_{co}), sheet resistance (R_{sh}), and limitations in obtaining sharp lateral doping profiles, and (2) limitations in obtaining required effective drive current ($I_{d,sat}$), and Subthreshold off-state leakage current ($I_{d,leak}$) with conventional planar transistor architecture.

In this work, Erbium Disilicide (ErSi_{2-x}) was investigated as possible S/D material for Schottky S/D MOSFET (SSDMOS) architecture in an effort to address (1). In addition, various non planar transistor architectures using Gate-All-Around (GAA) Silicon Nanowire (SiNW) channel was fabricated in conjunction with SSDMOS architecture (SSDNWMOS) to address (2).

ErSi_{2-x} is advantageous for N-SSDMOS due to its low barrier to the inverted n -channel and epitaxy on Si substrates. However, to successfully implement ErSi_{2-x} for N-SSDMOS applications, problems related to intrinsic physical properties of ErSi_{2-x} thin films (e.g. ease of oxidation, and pyramidal structural defects etc.) have to be solved.

The solid phase reaction mechanism in Er/Si system for disilicide formation as well as the characterization of the structural and electrical properties of different phases formed was carried out. The physical nature of pyramidal structural defects found on the silicide thin film was found to be due to several factors including biaxial compressive stress exerted by the Si substrate and fast diffusion of Si through the ErSi_{2-x} lattice. The ErSi_{2-x} /Si

Schottky diodes show degraded Schottky barrier height (ϕ_{Beff}), and ideality factor (n) due to the structural defects which are likely sources of trap states.

By applying Si substrate amorphization using a light Ar plasma sputter and Si pre-amorphization implant (PAI), the ErSi_{2-x} thin film was found to be free of structural defects, leading to an overall improvement electrical performance which can be modeled using an inhomogeneous Schottky contact model. In addition, *in-situ* capping layers of TiN and TiN/Ti were found to reduce structural defects density by $\sim 5\times$ which is believed to be due to a reduction in the biaxial compressive stress on the ErSi_{2-x} film during rapid thermal annealing. The capping layers also serve to prevent oxidation of the Er film during silicidation.

Using this knowledge, back-gated ErSi_{2-x} SSDNWMOS was fabricated which demonstrated good electrical characteristics with high $I_{\text{on}}/I_{\text{off}}$ ratio $\sim 10^5$, high drive current $\sim 900\mu\text{A}/\mu\text{m}$, which is significantly higher than previously reported Schottky S/D MOSFETs without barrier modified junctions. The effect of physical characteristics such as metal silicided junction depth, no. of nanowire channels, and metal-semiconductor junction size were investigated and found to have a direct impact on the electrical performance of the devices.

GAA ErSi_{2-x} SSDNWMOS were also fabricated along with NiSi and PtSi GAA SSDNWMOS. The GAA devices show excellent electrical performance in terms of Short channel effect (SCE) control and is believed to be due to the GAA structure which provides excellent gate electrostatic control of the Schottky barrier and Schottky barrier thinning due to the nanometer sized metal-semiconductor junction.

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CHAPTER 1

INTRODUCTION

1.1 Background

Metal silicide thin films are essential in the semiconductor integrated circuit (IC) industry. They are often used for source/drain (S/D) contacts as well as local interconnects to reduce the parasitic series resistance of the devices and to enhance the speed of electronic circuits [1]. TiSi_2 was used for technology nodes down to $0.25\mu\text{m}$ and CoSi_2 down to 90nm [1]. NiSi and Ni(Pt)Si have emerged as the leading candidates to replace CoSi_2 for 65nm node and beyond [2-4].

Erbium disilicide (ErSi_{2-x}) films are of considerable technological interest for potential use for SSDMOS due to their epitaxy on Si substrates and low Schottky barriers heights (Φ_b) of $\sim 0.27\text{ eV}$ to $n\text{-Si}$ [5]. However, to successfully implement ErSi_{2-x} for SSDMOS applications, problems related to the intrinsic physical properties of ErSi_{2-x} thin films such as ease of oxidation, and defective morphology, etc. have to be solved.

For ideal scaling per generation (~ 3 years), a $0.7\times$ reduction in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) dimensions is necessary to produce circuits with increased performance at reduced cost. Classical MOSFETs are reaching the scaling limit as confined by the physical laws of nature. These limits include higher subthreshold leakage current due to reduced threshold voltage, gate oxide leakage, lithographic variation and dopant fluctuation induced degraded performance, etc. [6-9].

Figure 1.1. Schematic of various MOSFETs architectures showing their respective resistance components. (a) Conventional doped Source/Drain MOSFET, and (b) Metallic Schottky Source/Drain MOSFET.

Particular to S/D scaling in the conventional MOSFETs, there exist several limiting factors including increasing contact resistance (R_{co}) at the silicon/silicide interface to the inverse square of the scaling factor, increasing sheet resistance (R_{sh}) due to ultra shallow p-n junction formation, and limitations in doping/activation techniques for sharp lateral doping profiles, and increasing spreading resistance, (R_{sp}) with scaling [6]. These resistances are schematically depicted in Figure 1.1(a).

Figure 1.1(b) shows the schematic of a Schottky S/D MOSFET (SSDMOS) which is one of the non-classical CMOS technologies proposed to solve the problems associated with a conventional MOSFET (i.e. parasitic S/D resistance) [7]. The SSDMOS does so by minimizing the previously mentioned parasitic series resistances by removing R_{sp} associated with S/D extension (SDE). R_{acc} is removed due to the non-overlapping (to gate) metal-semiconductor (MS) junction. R_{sh} is also reduced by an increased silicide thickness. The major resistance component of the SSDMOS would be R_{co} which is directly proportional to Φ_b and inversely proportional to the semiconductor doping concentration. As will be shown in later chapters, Φ_b can be modified with dopant segregation and MS junction size.

In addition, this architecture removes the constraint of using ultra shallow p-n junction for SDE by replacing it with a metallic S/D electrode [10-14].

Figure 1.2. The ITRS 2006 R_{sh} requirements for various MOSFET architectures from Ref. [15], and measured R_{sh} values considering SSDMOS featuring ErSi_{2-x} , PtSi, or NiSi.

The International Technology Roadmap for Semiconductors (ITRS) forecasts that starting in 2008, there is no known solution for the parasitic S/D resistance challenge [15]. Figure 1.2 depicts graphically the critical challenges with respect to R_{sh} and how a SSDMOS architecture would alleviate the problem as scaling continues toward the sub-22nm technological node.

In high performance logic systems, effective N-MOSFET saturation current ($I_{d,sat}$) and subthreshold off-state leakage current ($I_{d,leak}$) requirements are moving beyond planar transistor capability for sub-65nm technology nodes which are graphically represented in

Figure 1.3. These limitations in turn increase transistor intrinsic delay, inverse subthreshold slope, and short channel effects (SCE) etc.

Multiple gate FETs have been proposed as a method to improve $I_{d,sat}$, and to reduce SCE by enhancing transistor gate-to-channel coupling [15]. Examples of multiple gate FETs include double gated FinFET [16], π -gated [17] and Ω -gated FETs [18].

MOSFETs with ultra thin body (UTB) have also been proposed to provide improved electrostatic control of the channel. It also relaxes the need for channel doping resulting in reduced SCE [15]. Multiple gate FETs usually incorporate thin channel bodies with an increase in the effectiveness of electrostatic control with decreasing channel width and thickness [19].

Figure 1.3. The ITRS 2006 effective N-MOSFET $I_{d,sat}$ requirements for various MOSFET architectures and measured $I_{d,sat}$ values from Ref. 17, 18.

A particular example of combination of UTB MOSFET and a multiple gated FET structure is the gate-all-around (GAA) MOSFET in which the gate is completely

surrounded by an ultra narrow silicon nanowire (SiNW) channel (width $\sim 5\text{nm}$). This method involves subjecting the lithographically defined silicon fin to oxidation to obtain nanowire channels. This architecture provides the best possible electrostatic control resulting in greatly reduced SCE and improved drive current which satisfy the ITRS $I_{d,sat}$ requirements as shown in Figure 1.3 [20, 21].

A generic schematic of a MOSFET having a GAA narrow channel body is shown in Figure 1.4. The GAA MOSFET usually consists of a lithographically defined three dimensional fin/nanowire, and surrounding gates which are self aligned to each other and to the S/D.

Figure 1.4. The author's depiction of a generic multiple gated MOSFET with narrow body.

SiNW have been fabricated by several techniques, including 'bottom up' approaches such as chemical vapor deposition [22, 23] and 'top down' nanoscale definition as mentioned in the previous paragraph. From a technological viewpoint, it is advantageous for processes to be CMOS compatible such that 'top down' methods are more suitable for nanowire device fabrication.

Using ‘top-down’ conventional CMOS processes, SSDMOS using FinFET as the channel body incorporating YbSi_{1.8}, Ti metal, or NiSi for the S/D metal as well as SSDMOS using large dimension SiNW (~50nm width) as the channel body have been demonstrated [12-14, 24]. The devices showed moderate $I_{on}/I_{off} \sim 10^4$ ratios with large drain induced barrier lowering (DIBL) $\sim 0.26\text{V/V}$ [14]. Using Φ_b modification techniques like dopant segregation, Schottky S/D FinFETs have improved I_{on}/I_{off} ratios and reduced SCE [12, 13]. Nanowire transistors, when fabricated with metal silicided (ErSi_{2-x}, PtSi, NiSi) Schottky S/D, could be the one of the important structures for future device scaling [8, 9].

1.2 Objectives

The project aims to demonstrate SSDMOS with SiNW as the channel body (SSDNWMOS) with ErSi_{2-x} as the S/D metal silicide. This will be achieved in 4 phases as follows:

- 1 To study ErSi_{2-x} films formed by solid state erbium/silicon reaction via rapid thermal annealing (RTA) and to characterize the structural defects typically found in erbium disilicide and propose its formation mechanism.
- 2 To study the effects of using low energy Ar ions, Si pre-amorphization implant (PAI), and Ti based capping layers before and after erbium deposition on the material and electrical characteristics of thin ErSi_{2-x} films and ErSi_{2-x}/Si Schottky diodes.
- 3 To study SSDNWMOS with SiNW dimensions of < 10nm utilizing a back-gated configuration and to investigate the materials and electrical performance of the ErSi_{2-x}

SSDNWMOS with respect to device physical parameters and to analyze the current transport mechanisms across the MS interface.

- 4 To study SiNW (~5nm) CMOS transistors with metal silicided ($\text{ErSi}_{2-x}/\text{NiSi}/\text{PtSi}$) S/D and GAA channel. To investigate the electrical performance of the SSDNWMOS and to study to effect of silicided nano-junction size on the electrical performance of the SSDNWMOS.

1.3 Scope of the Project

This project involves the understanding of the solid phase reaction mechanism in the Er/Si system using RTA for ErSi_{2-x} formation as well as the characterization of the structural and electrical properties of different phases formed. The project studies the nature of structural defects found on the silicide films so that the physical mechanism can be understood. The effects of substrate amorphization and *in-situ* TiN and Ti capping layers on the ErSi_{2-x} film texture, morphology and subsequently electrical performance were investigated. Using this knowledge, various SSDMOS architectures were fabricated, including back-gated ErSi_{2-x} SSDNWMOS and GAA ErSi_{2-x} SSDNWMOS. Experiments on the SSDNWMOS devices were performed to elucidate the physical and electrical mechanisms of carrier transport, barrier height modulation etc.

The ErSi_{2-x} film and $\text{ErSi}_{2-x}/\text{Si}$ junction were characterized by x-ray diffraction (XRD), secondary ion mass spectroscopy (SIMS), transmission electron microscopy (TEM), and R_s measurements etc. Electrical measurements were also conducted on $\text{ErSi}_{2-x}/p\text{-Si}$ Schottky diodes. The SSDNWMOS devices were fabricated using ‘top down’ CMOS wafer fabrication processes including nano-scale lithographic definition and

thermal (stress-limited) oxidation. Electrical characterization was carried out on the silicon nanowire MOSFETs over a temperature range including room temperature.

1.4 Organization of the Thesis

The organization and outline of various chapters of this thesis are provided as follows.

Chapter 1 provides the introductory overview pertaining to metal silicide technology, in particular ErSi_{2-x} , ($x = 1/3$) and its use in SSDMOS, and an overview of the current multiple gated, UTB MOSFETs with an emphasis on SiNW MOSFETs. It also describes the objectives and scope of this project.

Chapter 2 gives a detailed review on key findings in the earlier work on ErSi_{2-x} , its growth kinetics, and formation and its use in SSDMOS. It covers the physics and operation of the SSDMOS and its performance advantages and disadvantages. It covers the formation methodologies of silicon nanowires and their device applications. In addition, current state-of-the-art SSDMOSs and SiNW MOSFETs are reviewed.

Chapter 3 describes the experimental methodology that includes experimental setup, sample preparation, device fabrication, materials and electrical characterization techniques used in this project.

Chapter 4 presents the material and electrical performance of thin ErSi_{2-x} films on Si with and without surface preparation or post-Er deposition capping layers. Improved characteristics by using a light plasma amorphization, Si PAI, and a Ti based capping layers were investigated.

Chapter 5 presents the electrical characteristics of N-MOSFETs using silicon nanowire (~8nm width) as the channel and ErSi_{2-x} as the S/D in a SSDNWMOS architecture. The current transport mechanisms together with the effects of physical transistor parameters are discussed.

Chapter 6 presents the electrical characteristics of high performance N-MOSFET transistors using SiNW (~5nm width) as the channel and ErSi_{2-x} as the S/D in SSDNWMOS architecture. Complementary SSDNWMOSs using PtSi S/D and NiSi S/D are characterized and their performance is discussed. The effects of the nano-scale MS junction size on the electrical performance were also investigated.

Chapter 7 summarizes the major results and findings in this project. It also offers future research direction based on the results of this project.

CHAPTER 2

Literature Review

2.1 Introduction

This chapter provides the background and relevant theories on ErSi_{2-x} formation kinetics and its unique properties, and the concepts in metal-semiconductor (MS) Schottky barrier formation. SSDMOS operation and architecture are described, along with the properties and formation of SiNW. In addition, state-of-the-art SSDMOS devices as well as SiNW based MOSFETs are summarized and presented.

2.2 Metal Silicides

2.2.1 Metal silicide ohmic contacts in CMOS technology

Metal silicide thin films are essential in semiconductor IC technology. They are often used to form S/D ohmic contacts as well as local interconnects to reduce the series resistance of devices and to enhance the speed of electronic circuits. Parasitic capacitances and resistances should both be minimized to reduce the resistive capacitive (RC) delay and hence increase the clock frequency [2]. In CMOS technology, a self-aligned silicide (SALICIDE) process forms the metal silicide at the gate and S/D simultaneously [1, 3].

TiSi_2 was used in the SALICIDE process for technology nodes down to $0.25\mu\text{m}$ in the early 1990s due to its low resistivity ($10 - 15\mu\Omega/\text{cm}$) and high thermal stability. At the sub- $0.25\mu\text{m}$ node, conversion of the C49 to C54 phase became increasingly difficult as agglomeration of TiSi_2 occurs during the phase transformation at high temperatures. This is a result of the reduction of nucleation sites when the linewidth reduces [1].

Subsequently CoSi_2 was used up to the 90nm node due to its smaller linewidth dependence than TiSi_2 . However, Co consumes ~25% more Si to form CoSi_2 as compared to Ti. For sub-65nm technology, NiSi is being used due to its low silicidation temperature, linewidth independence, low Si consumption, and non-bridging nature etc. The disadvantages of NiSi include the low endurance of NiSi film to high process temperatures, and relatively higher diffusivity of Ni atoms in silicon [3].

2.2.2 Erbium Disilicide Schottky contacts for SSDMOS

2.2.2.1 General Properties

Rare earth (RE) metals have a higher chemical activity than most other metals. This means that contacts to Si can be formed at relatively low temperatures (~350°C) [25]. Their thermal expansion coefficients are closer to Si than TiSi_2 or CoSi_2 . RE metal silicides react with oxygen only at high temperatures and are stable up to ~1300K. RE metals also consume less Si to form metal silicides as compared to TiSi_2 and CoSi_2 . The Φ_b of RE metals on *n*-Si have values of only 0.3-0.4eV which are the lowest known values for metal/*n*-Si contacts [26]. This makes RE metals suitable for N-SSDMOS devices. RE silicides crystallize in a defective hexagonal AlB_2 structure with 1 in 6 Si atoms missing. They are nearly latticed matched in the growth of their (100) planes on Si(111) and Si(100) [27, 28]. Among the RE silicides, ErSi_{2-x} has been attracting the most attention, due to its ease of handling, lowest resistivity [25], and optical properties.

2.2.2.2 Advantages of RE silicides as Schottky contacts

For a metal film deposited on Si or polysilicon and annealed at low temperatures, metal rich silicides form first. For suitable kinetic conditions, the formation of metal rich

silicide continues until all metal is consumed [29]. On the other hand, reaction of thin Er films with Si substrates at temperatures from 300°C to 500°C leads directly to the formation of Si rich RE silicides (~ 63 at. % Si) with no or barely detectable formation of metal rich silicides [25, 30]. ErSi₂ has a substrate dependence on the formation temperature [31]. Hexagonal Si rich ErSi_{2-x} compounds with A1B₂ structure on Si(111) requires temperatures about 100°C higher than that on Si(100) for silicidation. The silicide formation reaches completion within temperature limits as narrow as 5-10°C.

From a metallurgical point of view, ErSi_{2-x} can be epitaxially grown on silicon with a high crystallographic quality [27, 28, 32, 33]. ErSi₂ on Si(111) forms exclusively hexagonal phase silicide whereas on Si(100), the tetragonal phase has been observed as well. The tetragonal crystalline phase of ErSi_{2-x} grown on Si(100) has been considered as a structural phase induced by the substrate orientation. However apart from the substrate orientation which plays a major role, the composition of silicide is an important factor as well. Enrichment of the ErSi_{2-x} layers with Si and higher annealing temperature favors the formation of the tetragonal phase [27].

Hexagonal ErSi_{2-x}(100) // Si(100) with the a_{hex} and c_{hex} axes (3.79Å and 4.09Å respectively [28, 32]) parallel to the Si <110> direction (nearest spacing 3.84Å) results in lattice mismatch of +1.1% and -6.5%. ErSi_{2-x} like other RE silicides forms a high Schottky barrier (0.8eV) on *p*-Si and low Schottky barrier on *n*-Si (0.28 eV) (See Table 1). The low Schottky barrier on *n*-Si makes it attractive for use as the S/D metal for N-SSDMOSs which shall be explained in Section 2.3.3.3.

2.2.2.3 Disadvantages of RE silicides as Schottky contacts

The surface of ErSi_{2-x} formed by the reaction of thin erbium layers on single crystal Si substrate results in rough morphology characterized by deep ‘pits’ [25, 34-37]. Macroscopic structural defects on the surface of the thin film were also observed. The presence of ‘pits’ result in an increase of barrier height to the n -channel as well as increased reverse currents [34]. The characteristic ‘pits’ formed by solid phase reaction could be detrimental to the electronic performance of Schottky barrier devices as well as cause inaccurate determination of barrier heights from I - V measurements. Currently, there is a wealth of literature on the mechanism regarding the rough morphology and square shaped ‘pit’ formation in ErSi_2 film. Various authors have reported surface ‘pitting’ caused by contaminant barriers [35], selective Stranski-Krastanov growth of epitaxial silicide islands [38, 39], and the lifting off of RESi_{2-x} from the substrate [37]. All these involve a preferential path for Si diffusion resulting in rough morphology. Also, there is a strong substrate orientation effect as evidenced by square and triangular shaped ‘pits’ found on RESi_{2-x} films grown on Si(100) and Si(111) respectively [25].

Deposition of Si either by capping [38, 39], intermixing [40] or co-evaporation [27] have been attempted to remove surface roughness yielding successful results. However, from a SSDMOS device process integration point of view, these methods are not feasible in a SALICIDE process. Also, removal of rough morphology has been done using pre-treatment of the interface between Si and RE metal. Interfacial treatment has been done using Xe ion bombardment [36], Si ion bombardment [41] or electron beam treatment of the Si/RE [35, 42] interface. The authors postulated that the primary effect of surface pre-treatment is for the removal of a contaminant barrier at the interface.

Rare earth metals oxidize easily, even at room temperature [25]. The presence of a thin layer of SiO_2 between Si and a metal film can be instrumental in inhibiting metal-Si interaction and therefore modifying the intermetallic formation [29]. Er layers have been reported to be extremely reactive with oxygen and the layers quickly oxidize in air [43]. ErSi_{2-x} reduces SiO_2 at temperatures greater at 600°C to give Er_2O_3 [44], which is stable up to 1073K (798°C).

RE_2O_3 is more thermodynamically stable than SiO_2 at 600°C [45]. However, the presence of RE_2O_3 at the metal-Si interface slows down the formation of epitaxial RESi_{2-x} . At higher annealing temperatures up to 700°C , RE_2O_3 phase disappears, while the crystalline growth of the RESi_{2-x} layers steadily improves. The degradation of the interfacial RE_2O_3 barrier enables Si from the substrate to react with the RE for silicide growth.

2.2.3 MS Schottky barriers

2.2.3.1 Schottky barrier theories

When a metal makes an intimate contact with a semiconductor, the Fermi levels in the two materials must be coincident at thermal equilibrium. The Φ_b is defined as the energy distance from the metal Fermi level (E_f) to the top of the valence band or to the bottom of the conduction band at the MS interface for p and n -type semiconductor respectively. It can also be defined as the difference between the metal work function (Φ_m) and the electron affinity (χ_s) of the semiconductor as proposed by Schottky and Mott, shown in Figure 2.1(a) and can be expressed as follows [46].

$$\Phi_b = \Phi_m - \chi_s \text{ (Equation 2.1)}$$

Figure 2.1. (a) Φ_b band diagram of an arbitrary MS Schottky contact. (b) Energy band diagram (left) depicting Fermi level pinning at the MS interface.

The Fermi level pinning effect disassociates the Φ_m with the experimental Φ_b , which led to the assumption that the Φ_b is dependent on interface structure. Many Schottky barrier models have been proposed based on Fermi level pinning and have a general form as follows [47]

$$\Phi_B = \Phi_m - \chi_s + qV_{int} \text{ (Equation 2.2)}$$

where V_{int} is the voltage drop due to charge rearrangement between metal and semiconductor upon the formation of the interface, and q is the electronic charge.

The metal induced gap states (MIGS) model proposes that the wave function of electrons decay into a semiconductor leading to forbidden gap states in the semiconductor. The MIGS model has been used for metal gate/high- κ interfaces [48]. The MIGS model assumes a charge neutrality level (E_{CNL}) at the semiconductor interface which is average of the energies of acceptor-like and donor-like states at the

semiconductor interface. A dipole between Φ_m and the Φ_{CNL} energy level drives Φ_m towards the charge neutrality level, resulting in Fermi level pinning as depicted in Figure 2.1(b).

Recently, Tung proposed that chemical bonding to achieve thermodynamic equilibrium at the MS interfaces is the cause of Fermi level pinning [47]. The nature and the morphology of the very first interfacial layer of the MS contact depend on chemical reactions, surface diffusion, and interdiffusion etc. These phenomena will create defects at the interface and will govern the value of Φ_b . The effect of interface structure can be seen by the experimental dependence of the Φ_b on the epitaxial orientation NiSi₂ [49]. The morphology of the interface is also an important factor to consider in Φ_b measurements [50]. Planar NiSi₂/Si(100) interfaces show a Φ_b which is significantly lower on *n*-type Si as compared to faceted, rough interfaces.

The Φ_b controls the electronic transport across MS interfaces and is vital to the operation of semiconductor devices. The two main current transport mechanisms involving Schottky barriers include emission over the barrier, also known as thermionic emission (TE), and quantum mechanical tunneling through the barrier, i.e., thermionic-field emission (TFE) [51]. Tunneling increases with temperature, and more importantly, with the modification of the barrier thickness by the application of the gate potential. Almost all metals can form silicides, but most of them result in high Φ_b on *n*-type silicon and low barrier heights on *p*-type silicon. Rare earth silicides, unlike transition metal silicides, have low Φ_b to *n*-type silicon and high barrier on *p*-type silicon. In general, the Φ_B displays a systematic increase with Φ_m , but the rate of increase is far less than that

predicted by the Schottky-Mott theory [46]. It follows that RE metals with low work functions (Er = 3.12eV, Yb = 2.59eV etc.) will have low Φ_B .

2.2.3.2 Experimental measurements

Tu *et al.* [52] fabricated RESi_{2-x} Schottky diodes formed by furnace silicidation of RE metals (Er, Dy, Ho, Gd). The RESi_{2-x} Φ_b on n -Si were determined to be low, ranging from 0.37 to 0.39eV. Norde *et al.* [53] used I - V and photoresponse measurements to determine that the Φ_b on n -Si is around 0.4eV for Tb, Er and Yb. Zhu *et al.* have fabricated RESi_{2-x} Schottky diodes by RTA silicidation and found that the Φ_b on n -Si measured by the I - V method ranges from 0.52eV for TbSi_{2-x} to 0.3eV for YbSi_{2-x} [54]. Unewisse *et al.* studied the photoresponse of ErSi_{2-x} diodes on silicon over a wide range of temperatures (25K to 160K) [55]. Φ_b was found to have a constant value of ~0.28eV when plotted as a function of temperature. Huda *et al.* used C - V measurements on ErSi_{2-x} Schottky contacts formed on H terminated Si substrates and found a Φ_b of 0.27eV for $\text{ErSi}_2/n\text{-Si}(001)$ [56]. Table 2.1 summarizes the Φ_b of various metal silicides on n -Si.

2.2.3.3 Factors affecting Schottky barrier height

Wu *et al.* studied the effect of ErSi_{2-x} film surface morphology on the Φ_b . Rough morphology was removed by depositing a layer of amorphous Si (a-Si) after Er deposition. The Φ_b of ErSi_{2-x} diodes was found to be ~0.7eV for Er/Si and ~0.76eV for a-Si/Er/Si. In addition, the reverse current was higher for the sample with rough morphology [34].

It was found that presence of a thin interfacial oxide lowers the Φ_b by a considerable amount [57]. Samples with a layer of interfacial oxide exhibit a lower Φ_b of 0.68eV compared to samples without interfacial oxide which showed a higher Φ_b of 0.8eV. In addition, Knapp *et al.* found that the electron beam annealing (50kW/cm⁻², 1200K) method of silicidation resulted in a higher Φ_b with a lower n compared to the sample which was furnace annealed [35, 42]. The improvement was postulated to be due to the dissolution of an interfacial oxide barrier followed by uniform silicide growth. Muret *et al.* have also shown experimentally that oxygen concentrations of 0.3% and below are necessary to obtain the lowest Φ_b value of ErSi₂ on n -Si of 0.28eV [5].

Table 2.1. Φ_b and n of various metal silicides on n -Si.

Silicide	Φ_b (eV)	n	Preparation	Measurement	Ref.
TiSi ₂	0.61	-	-	-	[3]
CoSi ₂	0.65	-	-	-	[3]
NiSi	0.67	-	-	-	[3]
YSi _{1.7}	0.39	-	Furnace	I -Temp	[52]
ErSi _{1.7}	0.39	-	Furnace	I -Temp	[52]
ErSi _{1.7}	0.36/0.35	1.1	Furnace	Photo/ I - V	[52]
ErSi _{2-x}	0.41	1.57	RTA	I - V	[54]
ErSi _{1.7}	0.43/0.29	1.23	RTA	I - V / C - V	[58]
ErSi ₂	0.27	-	UHV 10 ⁻¹¹ Torr	C - V	[56]
ErSi ₂	0.283	-	Furnace	Photoresponse	[55]
DySi _{1.7}	0.37	-	Furnace	I -Temp	[52]
YbSi _{1.7}	0.27	1.04	RTA	I - V	[54]
TbSi _{2-x}	0.52	1.83	RTA	I - V	[54]

2.3 Schottky Source/Drain MOSFETs

2.3.1 Introduction

Various problems are associated with S/D scaling in conventional MOSFETs. These include increasing R_{co} at the silicon/silicide interface to the inverse square of the scaling

factor, decreasing thickness of ultra shallow S/D junction, which result in increasing of R_{sh} , and steeper S/D extension profile and hence the need for sharp lateral doping techniques [7]. SSDMOS is one of the non-classical CMOS technologies proposed to solve the problems associated with a conventional MOSFET architecture and to provide a path for scaling to the end of the ITRS roadmap [15].

Figure 2.2. Schematic representation of a SSDMOS.

Figure 2.2 shows the schematics of a SSDMOS with metal silicide at the S/D instead of doped p - n junctions. The structure is quite simple and can be formed easily and accurately by controlling the deposited metal thickness and annealing temperature in a solid state reaction with silicon.

SSDMOSs have the advantages of low S/D resistance and absence of abrupt S/D doping. As a result of the lower S/D resistance of the SSDMOS, the circuit performance can be up to 44% faster compared to a doped S/D MOSFET [11]. Also, as a result of the replacement of the n +/ p junction with a Schottky junction, the floating-body effect is reduced owing to the reduction in electric field near the drain and the “smoother” absorption of excess holes in the channel [59]. In addition, the SSDMOS is less sensitive

to punchthrough current even without extra doping as a result of the S/D Schottky barrier [60].

2.3.2 Operating principles

The device operation is based on modifying the Schottky barrier between the S/D and channel with the gate bias. Consider N-SSDMOS formed on p -Si substrate as shown in Figure 2.3(a), the Φ_b to electrons is $\sim 0.27\text{eV}$ (while the Φ_b to holes is $\sim 0.85\text{eV}$), at the $\text{ErSi}_{2-x}/\text{Si}$ Schottky junction.

Figure 2.3. Band diagram on the surface and sub-surface of (a-c) N-SSDMOS, and (d-f) conventional N-MOSFET. Reproduced from Ref [61].

When a gate voltage is applied, the barrier to electron injection from the source into the channel is lowered, as in a conventional MOSFET, and TE occurs. With increasing

gate voltages, the barrier is further lowered. Eventually, when the barrier is lowered to be equal to Φ_b , the on-state current becomes limited by TFE, i.e., tunneling through the Schottky barrier. Note that the subthreshold swing is degraded as a result which will be described in Section 6.4.2. As this point, the carriers flow from the source to the drain by tunneling through the barrier as well as by emission over the barrier at the silicon/silicide interface. As can be seen in Figure 2.3(b) and (c), the off-state current is a combination of the tunneling and thermionic current caused by the reverse biased Schottky diode at the drain, as well as the thermionic current over the source Schottky barrier at low gate bias. The absence of the Schottky barrier however for conventional MOSFETs as shown in Figure 2.3(d), means that the device on current is higher.

The flow of current for both positive and negative gate biases is thus due to the flow of both electrons from the source and holes from the drain. This characteristic is termed ambipolar conduction. Ambipolar conduction is absent in conventional MOSFETs as the doped S/D has carriers of a single doping type (either n or p -type), resulting in only electron flow for the N-MOSFET as can be seen in Figure 2.3(e) and (f). This is in contrast with metal silicide S/D which has free electrons, as well as holes which will contribute to reverse current when the channel is in accumulation.

It should be mentioned that SSDMOS devices have two main disadvantages compared to doped S/D MOSFETS as follows: (1) SSDMOS devices have degraded on-state currents as the current is TFE-limited (unless Φ_b is low), which is evident in larger subthreshold swings. (2) SSDMOS devices have higher off-state current due to TFE of carriers from the drain. These differences will be clearly shown in Table 2.2 and Table 2.3, together with methods for surmounting the disadvantages.

2.3.3 SSDMOS architecture

2.3.3.1 Doping / Shallow doped extension (SDE)

Doping is usually employed in the SSDMOS to alter the Schottky barrier height. Off state leakage can be minimized by implantation of a thin (fully depleted) layer of fully depleted carriers beneath the active region to increase Schottky barrier height [62]. Incorporation of the doped SDE can increase the drive current by about 2 orders of magnitude due to the reduction of the effective Φ_b [59, 63]. It can also reduce leakage currents due to the reduced field at the Schottky contact.

2.3.3.2 Source/drain material

For complementary performance in SSDMOSs, both P-SSDMOS and N-SSDMOS are required. This has been achieved by using (1) complementary silicides, i.e., two different silicides, one having low Φ_b on p -Si, and one having low Φ_b on n -Si. Traditionally, ErSi_{2-x} with Φ_b to electrons of $\sim 0.27 - 0.32\text{eV}$ [61] is typically used for N-SSDMOS, while PtSi with Φ_b to holes of $\sim 0.15 - 0.24\text{eV}$ [61], is typically used for P-SSDMOS.

Alternatives to ErSi_{2-x} and PtSi have been proposed to achieve superior electrical performance. In 2004, Zhu *et al.* [54] fabricated N-SSDMOSs using YbSi_{2-x} as S/D material and found better drive current and lower leakage current compared to ErSi_{2-x} S/D. They postulated that better performance is due to the lower barrier height of YbSi_{2-x} to Si and smoother YbSi_{2-x} /Si interface. For P-SSDMOS, IrSi has been proposed as it presents the lowest Φ_b to holes with an experimentally extracted value of $\sim 0.11\text{eV}$ [64]. However, IrSi has not been applied experimentally to P-SSDMOSs.

Since 2004, there has been significant research on using mid-gap (to Si bandgap) silicides, including CoSi₂ and NiSi, which have Φ_b close to 0.56eV ($E_g/2$) [13, 65-71]. This silicide scheme incorporates various Schottky barrier modification techniques, and usually involves an interfacial layer between the silicide and the semiconductor, resulting in reduced Φ_b .

2.3.3.3 Dopant Segregation

Dopant segregation works on the principle of difference in solid solubility of dopants in the silicide and silicon. Point defects at the silicide/silicon front enhances the diffusivity of dopants in silicon. The dopants are then “pushed” out of the silicon after silicide is formed, where it then piles up at the interface. This can result in dopant concentrations above the solid solubility limit in silicon owing to the strain induced point defects [73].

Specific to SSDMOSs, dopant segregation has been applied to the S/D regions in an effort to reduce Φ_b , so as to improve device drive current. This was first attempted by Kinoshita *et al.* for CoSi₂ SSDMOS [67]. In order to achieve Φ_b modulation without losing the merits of Schottky junctions, the dopant layer must be sufficiently thin (<5nm) to be fully depleted, with a concentration $> 1 \times 10^{20}$ atoms.cm⁻³.

Dopant segregation has been applied to NiSi based SSDMOS [12, 13, 65-71, 74, 75] as well as PtSi based SSDMOS [72], with the most commonly used dopants being As and Sb for N-SSDMOS [66, 68, 74], and B for P-SSDMOS [65, 66, 68].

2.3.3.4 Other Methods of Φ_b modulation

Other than dopant segregation, other methods of Φ_b reduction have been employed and they are listed as follows : (1) Biaxial tensile strain provided by strained Si which causes Si conduction/valence band splitting to lower/higher energy levels resulting in reduction of Φ_b [76]. (2) Deposition of ultra thin (0.25nm) layer of Si_3N_4 at the Erbium/*n*-Si interface resulting in reduced Φ_b as a result of suppression of Fermi level pinning [77]. (3) Sulphur passivation at the MS interface which makes use of silicidation induced S segregation to reduce the interface states at the NiSi/Si interface [66]. (4) Metal segregation to the MS interface which makes use of a capping layer of Y for N-SSDMOS, and Pt for P-SSDMOS, on top of NiSi/Si Schottky junctions. By using a low temperature anneal, the capping metal diffuses through the NiSi grain boundary and segregates at the NiSi junction, resulting in a meta-stable state with reduction in Φ_b by $\sim 0.1 - 0.15\text{eV}$ for both Y capped N-SSDMOS and Pt capped P-SSDMOS [78]. (5) By increasing the *n*-Si substrate doping, the Φ_b to holes can be lowered through an image force mechanism, resulting in improvements in drive current for PtSi P-SSDMOSs [79, 80].

2.3.3.5 Germanium/GOI

In SSDMOSs using Si as the substrate, it is difficult to achieve high drive current due to the relatively high potential barrier between the source and the channel. This problem may be solved by using a Ge substrate because of the low Φ_b of germanide/Ge contact and the high carrier mobility of Ge. Ge based P-SSDMOSs have been fabricated showing improved threshold voltage and larger drive current [81]. However the lower barrier at

the drain/substrate contact results in a large I_{off} . This problem can be alleviated by using Germanium-on-insulator (GOI) substrate [82]. Recently, PtGe SSDMOS with HfO₂/TaN gate stack have been demonstrated with much reduced I_{off} due to the higher Φ_b to electrons by 0.16eV of the PtGe₂/n-Ge contacts (when the channel is in accumulation) as compared to NiGe/n-Ge. In addition, PtGe/p-Si has a negative Φ_b , which provides the possibility of high drive current [83, 84].

2.3.3.6 Metal Gate

Polysilicon gate depletion increases the electrical gate oxide thickness and consequently, decreases the MOSFETs drive current. Using a metal gate removes the polysilicon depletion effect as depletion layer does not exist in a metal.

Larrieu *et al.* have fabricated PtSi P-SSDMOSs with SiO₂/W midgap gate down to $L_g = 40\text{nm}$ which showed excellent I_{on}/I_{off} characteristics $\sim 10^4$ at $V_d = -1.6\text{V}$ for $L_g = 100\text{nm}$ devices [85]. Zhu *et al.* have fabricated YbSi_{2-x} N-SSDMOS with HfO₂/TaN metal gate with I_{on}/I_{off} characteristics $\sim 10^7$ at $V_d = 1\text{V}$ for $L_g = 4\mu\text{m}$ devices [54]. Aggressively scaled UTB NiSi₂ N-SSDMOS with $L_g = 10\text{nm}$ have been fabricated with HfAlO_x/NiSi fully silicided (FUSI) metal gates with good I_{on}/I_{off} ratio at $V_d = 50\text{mV}$ [69]. The gate leakage is small owing to the high- κ dielectric.

2.3.3.7 Effects of MS size

First principles calculations of a 1nm NiSi/Si interface show that the Φ_b of NiSi/p-Si can be reduced to $\sim 0.1\text{eV}$ (from a value of 0.4eV) if B atoms can be placed precisely at the substitutional site at the Si layer [86]. This effect is due to induced dipoles (caused by

the B atoms), which un-pins the Fermi level, and shifts it closer to the valance band edge. Note that this method is dependent upon B implantation and segregation to the Si substitutional sites.

As SOI thickness is scaled down (below 20nm), carrier injection from the NiSi source to the UTB Si channel improves [87]. By solving a modified Poissons equation, it was found that the reduction in the Si thickness leads to a thinner Schottky barrier, thus improving the tunneling probability.

Simulations of UTB (silicon thickness (t_{Si}) = 5nm) SSDMOS shows that the I_{on} is relatively independent of L_g up to 5nm, in contrast with I_{off} , which increases drastically with when $L_g < 30$ nm ($\sim 10^{-10}$ $\mu A/\mu m$ for $L_g = 30$ nm versus $\sim 10^{-1}$ $\mu A/\mu m$ for $L_g = 10$ nm). In addition, threshold voltage decreases until $L_g = 10$ nm, whereby it starts to increase. Ahn *et al.* attributed the increase to the depletion regions of the Schottky barrier, which raises the channel potential in short L_g s. This leads to a greater V_g needed to overcome the built in potential (of the depletion region) to induce tunneling [88].

2.3.4 State-of-the-art SSDMOS

SSDMOS literature encompasses simulations, novel silicides for S/D [54, 64], Schottky barrier height modification [13, 65-73], and proof of concept [78, 86]. Table 2.2 presents the key electrical performance indices for the state-of-the-art SSDMOS devices.

Device simulations by various methods have shown the theoretical feasibility of implementing SSDMOS in the nanometer regime [60, 90], including immunity to SCE when scaled to 10nm in channel length, and reduced gate delay. In addition, it was found that the drivability of the SSDMOS for sub-30nm channel lengths is comparable with the

conventional MOSFETs when barrier height is sufficiently low, $\sim 0.25\text{eV}$ for p and $\sim 0.15\text{eV}$ for N-SSDMOS [63]. Subsequently, it was found that a negative Φ_b ($\sim -0.25\text{eV}$) is needed for the SSDMOS to achieve ballistic transport with no parasitic resistance [90]. Simulations techniques include using current continuity between channel and tunneling current [91], Monte Carlo technique [92], solving of the non equilibrium Green's function (NEGF) [88], and first principles study of the metal silicide to Si cell [86].

Traditionally, SSDMOSs were fabricated on bulk Si or SOI without any barrier modification techniques. Experimental P-SSDMOS using PtSi as S/D showing good electrical characteristics were first reported in 1999 by Wang *et al.* [62] which showed scalability down to sub-40nm. In 2000, Kedzierski *et al.* reported PtSi, and ErSi_{2-x} complementary SSDMOS on SOI with $t_{\text{Si}} = 14\text{nm}$ and L_g down to 15nm. I_{on} of $270\mu\text{A}/\mu\text{m}$ for P-SSDMOS, I_{on} of $190\mu\text{A}/\mu\text{m}$ for N-SSDMOS, and $I_{\text{on}}/I_{\text{off}}$ ratio $\sim 10^4$ were reported [10].

In 2005, Jang *et al.* reported $\text{ErSi}_{1.7}$ SSDMOS with $L_g = 23\text{nm}$ on SOI with $t_{\text{Si}} = 100\text{nm}$. The I_{on} recorded was $10\mu\text{A}/\mu\text{m}$ with a subthreshold swing (SS) of $120\text{mV}/\text{decade}$ [93]. This was followed in 2006 by $\text{ErSi}_{1.7}$ SSDMOS with $L_g = 10\text{nm}$ on a similar substrate but with n -doped SOI [94]. The I_{on} recorded was $100\mu\text{A}/\mu\text{m}$ with an SS of $84\text{mV}/\text{decade}$. In 2005, Larrieu *et al.* reported PtSi P-SSDMOSs on SOI with $t_{\text{Si}} = 10\text{nm}$ and L_g down to 40nm which showed I_{on} of $\sim 50\mu\text{A}/\mu\text{m}$, $I_{\text{on}}/I_{\text{off}}$ of $\sim 10^4$ for the $L_g = 100\text{nm}$ devices [85]. In 2006, Larson *et al.* reported PtSi P-SSDMOS on bulk Si with $L_g = 25\text{nm}$ which showed I_{on} of $\sim 460\mu\text{A}/\mu\text{m}$, and $I_{\text{on}}/I_{\text{off}}$ of $\sim 10^3$ [61].

Subsequently, barrier modification techniques were applied to SSDMOSs on bulk Si or SOI in order to lower the Schottky barrier height. The 'oldest' and thus most often

used barrier modification technique is dopant segregation even though several other methods have been reported recently as described in Section 2.3.3.4. The first instance of dopant segregation as applied to metallic S/D was in 2004 where Kinoshita *et al.* reported CoSi₂ C-SSDMOS on bulk Si with L_g down to 50nm [67]. Low energy dopant implantation was carried out before Co-silidation to induce dopant silicidation. A 20% improvement in the drive current was observed over the conventional N-MOSFET. In 2006, Ko *et al.* reported NiSi C-SSDMOS on bulk Si with L_g down to 39nm utilizing dopant segregation as well as process induced strain (tensile for N-SSDMOS and compressive for P-SSDMOS) [70]. The N-SSDMOSs showed an I_{on}/I_{off} performance gain of 10% when compared to the doped S/D SSDMOS control devices. In addition, highest P-SSDMOS I_{on} was recorded at 821 μ A/ μ m. In 2007, Larrieu *et al.* reported PtSi P-SSDMOS on SOI with $t_{Si} = 20$ nm and L_g down to 25nm. Implant of BF₂ through both unsilicided Pt and PtSi were carried out followed by RTA to achieve dopant segregation [72]. The $L_g = 50$ nm devices showed an improvement in the current drive accompanied by an improved immunity against SCE when compared to the dopant free approach.

In addition to bulk or SOI substrates, SSDMOSs have also been applied to multiple gated FinFets with and without dopant segregation. In 2005, Lin *et al.* have reported $L_g = 49$ nm FinFET with fin width (W_{fin}) = 60nm and fin height (H_{fin}) = 40nm with modified NiSi/Si Schottky barriers [12, 65]. B or P segregation was achieved by an implant through silicide followed by subsequent furnace annealing. The devices showed high I_{on}/I_{off} ratio of $\sim 10^7$, as well as good SS of ~ 60.4 mV/decade and DIBL of ~ 39 mV/V. In 2006, Kaneko *et al.* reported NiSi C-SSDMOS with $W_{fin} = 15$ nm, $H_{fin} = 50$ nm and L_g down to 15nm [13]. In their devices S/D implantation were carried out (usually absent in

SSDMOSs) by low energy As and B implantation. Finally, Ni was deposited followed by silicidation, which resulted in dopant segregated junctions. The $L_g = 15\text{nm}$ devices showed high I_{on} of $\sim 960\mu\text{A}/\mu\text{m}$, I_{on}/I_{off} ratio of $\sim 10^4$ and SS of $\sim 125\text{mV}/\text{decade}$. In 2007, Lee *et al.* reported $\text{YbSi}_{1.8}$ N-SSDMOS with $W_{fin} = 30\text{nm}$, $H_{fin} = 40\text{nm}$ and L_g down to 25nm [14]. The reported I_{on} is $\sim 100\mu\text{A}/\mu\text{m}$, I_{on}/I_{off} ratio is $\sim 10^4$ and SS is $\sim 125\text{mV}/\text{decade}$.

For the SBMOS reviewed thus far, the device fabrications do not require channel implants (retrograde well implants, punchthrough implants etc.) or S/D implants (S/D extensions, S/D implants) [6, 8, 9]. The fewer implant steps, and reduced implant doses of the SBMOS process yield potential economic benefits. Besides improving device performance via increased carrier mobility, a simpler process, with fewer mask sets leads to lower costs in the semiconductor manufacturing process.

Also, one notices that there is no reliability related information reported in this section, i.e., there is limited data with regards to the reliability of SBMOS transistors

Table 2.2. Key electrical performance indices for the state-of-the-art SSDMOS

S/N	S/D	Channel	L_g (nm)	Gate	EOT (nm)	V_d (V)	I_{on} ($\mu\text{A}/\mu\text{m}$)	I_{off} ($\mu\text{A}/\mu\text{m}$)	I_{on}/I_{off}	SS (mV/dec)	DIBL (mV/V)	Year	Ref
N-SSDMOS													
1	NiSi DS	FinFET, FH = 50nm, FW = 15nm	15	Poly	1.3	1	1000	5.00 E-02	2.00 E+04	125	~ 100	2006	13
2	CoSi_2 DS	Bulk	50	Poly	p2.5	1	500	2.00 E-02	2.50 E+04	-	-	2005	67
3	$\text{ErSi}_{1.7}$ $n\text{-Si}$	SOI, tSi = 100nm	10	Poly	5	1	100	7.00 E-03	1.43 E+04	84	380	2006	95
4	$\text{ErSi}_{1.7}$	SOI, tSi = 100nm	23	Poly	6	1	10	9.00 E-05	1.11 E+05	120	100	2005	94
5	$\text{ErSi}_{1.7}$	SOI, tSi = 14nm	15	Poly	4	1.4	40	2.00 E-02	2.00 E+03	150	-	2000	10

6	NiSi DS	Bulk, tensile CESL	39	Poly	p1.2	1.2	1389	1.00 E-01	1.39 E+04	99	-	2006	71
7	NiSi DS	Bulk	39	Poly	p1.2	1	900	1.00 E-02	9.00 E+04	-	-		72
8	NiSiGe DS	Strained Si	500	Poly	10	1.2	70	5.70 E-05	1.23 E+06	120	-		76
9	YbSi _{2-x}	Bulk	4000	TaN	2.5	1	2	3.00 E-06	6.67 E+05	75	-	2004	54
10	YbSi _{1.8}	FinFET, FH = 40nm, FW = 30nm	25	Poly	3	1.1	100	6.00 E-03	1.67 E+04	125	260	2007	14
11	NiSi DS	FinFET, FH = 40nm, FW = 60nm	49	Poly	p4	1	167	8.35 E-06	2.00 E+07	71	-	2005	12
12	NiSi DS	SOI, tSi = 25nm	1000	Poly	3.7	1.1	30	1.00 E-03	3.00 E+04	70	-	2006	66
13	NiSi	SiNW, width ~6nm	90	Poly	9	1.2	399	5.20 E-03	1.50 E+05	60	13	2008	This work
14	ErSi _{2-x}	SiNW, width ~6nm	90	Poly	9	1.2	464	3E-02	1.55 E+04	79	53	2008	This work
P-SSDMOS													
1	NiSi DS	FinFET, FH = 50nm, FW = 15nm	15	Poly	1.3	-1	500	8.00 E-02	6.25 E+03	150	~100	2006	13
2	NiSi DS	Bulk, SiGe stressor	39	Poly	p1.2	1.2	821	1.00 E-01	8.21 E+03	113	-	2006	71
3	NiSi DS	Bulk	39	Poly	p1.2	1	400	4.00 E-03	1.00 E+05	-	-	2006	72
4	NiSiGe DS	SiGe	500	Poly	10	-1.2	30	4.10 E-05	7.32 E+05	120	-	2006	76
5	PtSi	SOI, tSi = 14nm	20	Poly	4	-1.4	200	2.00 E-03	1.00 E+05	100	-	2000	10
6	PtSi	SOI, tSi = 10nm	100	W	2.2	-1.1	50	2.00 E-05	2.50 E+06	80	85	2005	86
7	PtSi DS	SOI, tSi = 20nm	50	W	2.4	-1.1	200	4.00 E-04	5.00 E+05	-	-	2007	73
8	PtSi	Bulk	60	Poly	1.8	-1.2	311	1.20 E-02	2.59 E+04	96	-	2005	61
9	PtSi	Bulk	25	Poly	1.8	-1.2	460	1.68 E-01	2.74 E+03	117	-	2005	61
10	NiSi DS	FinFET, FH = 40nm, FW = 60nm	49	Poly	p4	-1	84	1.67 E-07	5.00 E+08	94	-	2005	12
11	NiSi DS	SOI, tSi = 25nm	1000	Poly	3.7	-1.1	10	1.00 E-05	1.00 E+06	67	-	2006	66
12	NiSi	SiNW, width ~6nm	90	Poly	9	-1.2	513	5.00 E-03	2.30 E+05	60	10	2008	This work

13	PtSi	SiNW, width ~6nm	90	Poly	9	-1.2	618	1.00 E-03	5.62 E+05	60	10	2008	This work
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p - physical oxide thickness, FH - Fin height, FW-Fin width, DS - dopant segregation, CESL - compressive etch stop layer.

2.4 Silicon Nanowire

2.4.1 Low dimensional systems

In order to maintain the drive current with scaling, low SS and DIBL is required to decrease the threshold voltage as power supply decreases [9]. UTB SOI MOSFETs can achieve this owing to the improved electrostatics in the undoped channel. The UTB MOSFET can be used in conjunction with multiple gates which further improves the gate control of the channel. SiNW MOSFET allows for the ultimate scaling of the silicon body for optimum transistor performance. However, scaling the transistor channel to one dimension results in the confinement of carriers (quantum confinement), and results in the splitting of the six equivalent Δ conduction valleys ($\langle 100 \rangle$ direction) into the Δ_4 and Δ_2 subband valleys with the following effects [95, 96] as depicted in Figure 2.4.

Firstly, the conduction band rises to higher energy values, and becomes direct bandgap [96]. The Si bandgap increases from 1.13eV for a 3nm thick wire to 2.5eV for a 1.2nm wire. This has a significant impact on the performance of thin body SOI MOSFETs. As silicon reduces in thickness, the threshold voltage decreases owing to the reduction in ionized impurity scattering. However, as thickness reduces beyond a certain thickness, the 3D classical picture will break down due to subband splitting leading to higher threshold voltages [97]. Depending on the amount of subband modulation as wire diameter decreases, the threshold voltage is also shifted by a proportionate amount. As

the silicon thickness of UTB MOSFETs reduces from 10nm to 2nm, the threshold voltage was found to increase from 0.03V to 0.15V [97].

Figure 2.4. Schematic view of a SiNW MOSFET with a surrounding gate electrode. Electron transport is assumed to be one-dimensional in the x-direction. Reproduced from Ref [95].

Secondly, there is an increase of the effective mass in the transport direction along the length of the wire. The effective mass increases by ~36% as the dimensions decreases from 5nm to 2nm [95]. An increase in the effective mass due to quantum confinement would also degrade the mobility of the device [51]. Thirdly, the density of states ($N(E)$) reduces. The $N(E)$ of bulk semiconductor is continuously varying with energy as follows, $N(E) = m^*(2m^*E)^{1/2}/\pi^2 \hbar^2$ where m^* is the effective mass, E energy, and $\hbar$ is the reduced Planck constant. For a quantum wire, $N(E)$ is reduced and has an inverse energy relation as follows $N(E) = (2m^*)^{1/2} \sum_{i,j} (E - E_{i,j})^{-1/2} / \pi^2 \hbar L_x L_y$, where i and j are integers, and L_x and L_y are the height and width of the quantum wire [51]. The reduction in $N(E)$ results in reduced scattering events which enhances phonon mobility [98]. However, this is balanced by the increase in the electron-phonon wavefunction overlap which results in mobility degradation. The net result is that in narrow wires less than 30nm in diameter,

the phonon limited mobility decreases with decreasing wire diameter [98]. In addition, it has been shown that carrier transport for GAA SiNW transistors (diameter $\sim 7\text{nm}$) at low temperatures, and low drain biases are subject to inter subband scattering [99]. This reduces current in the strong inversion region.

It must also be mentioned that the AC performance and device delay for 1-dimensional devices can be degraded as compared to 2-dimensional devices owing to the fact that narrower devices suffer more parasitic capacitances due to an increased fringing effect [176]. This increased parasitic capacitances can potentially take away the improvement in the carrier transport and electrostatic control of 1D devices over 2D devices.

In spite of the above mentioned issues of using SiNW as the channel body for MOSFETs, there are several factors which offset the disadvantages as long as the SiNW dimensions are large enough to suppress the quantum confinement effects. The volume inversion effect in narrow wires suppresses surface scattering, i.e., carriers are not confined to the surface of the wire, but are further from the surface [98]. The decreased surface scattering results in a mobility enhancement at higher electric fields.

In addition, it has been experimentally shown that SiNW maximum current density and mobility increases as diameter decreases down to a minimum diameter of $\sim 4\text{nm}$ [100]. In addition, the ballistic efficiency increases as diameter decreases as the volume inversion effect exceeds surface, phonon, and back scattering. This trend continues until a diameter of $\sim 4\text{nm}$ where ballistic efficiency decreases when various scatterings dominate.

2.4.2 Formation

2.4.2.1 “Bottom up” approach

Morales *et al.* first reported synthesis of crystalline semiconductor nanowires in 1998 using vapor-liquid-solid (VLS) growth [101]. They started with laser ablation of SiFe target to form Si, Fe liquid clusters. These clusters form the starting material and define the size of the Si nanowire (6 - 20nm diameter) which grows from the super-saturated clusters. Using similar laser assisted catalytic growth, a wide range of binary and ternary III-V, II-VI, and IV-IV group single crystal semiconductor nanowires have been grown [102].

Holmes *et al.* reported the growth of Si nanowires using a fluid solution phase approach [103]. In short, Au nanocrystals were dispersed in a heated liquid solution of diphenylsilane which decomposes to Si atoms. Si atoms dissolve in the Au nanocrystal until it reaches supersaturation, whereby Si is expelled from the nanocrystal as a crystalline nanowire.

Assembly of VLS synthesized Si nanowires into functional networks on SiO₂/Si substrates was then demonstrated [104]. Si nanowires grown by laser assisted catalytic growth were suspended in ethanol solution. The solution was then passed through fluidic channels in molds on a flat substrate. By pre-patterning the substrate chemically, nanowires were preferentially assembled at positions defined by the chemical pattern.

In 2000, Cui *et al.* reported the doping (*p* and *n*-type) of Si nanowires by controlled introduction of B or P during the vapor phase growth of the nanowires [105]. Using a back gated transistor structure and Al or Au contacts to either end of the doped nanowires, they verified the wires were electrically *p* or *n*-type by conductance

measurements and observed ohmic current conduction whose magnitude depended on the amount of doping.

Cui *et al.* and Huang *et al.* then reported assembly of the Si nanowires into functional electronic devices (logic gates etc.) formed by the assembly of one or more Si nanowire/Si nanowire crosses using *p* and *n*-type material respectively [106, 107]. These *p-n* crosses/junctions were made by sequential deposition of solutions of *p* and *n*-type materials and demonstrated current rectification. FETs were made by the same crossed junctions but showed drive currents 10x lower ($\sim 50\mu\text{A}/\mu\text{m}$) than Si MOSFETs (with 50nm gate length) but with comparable I_{on}/I_{off} ratio $\sim 10^5$. They again utilized the crossed Si nanowires to create electrically addressable arrays to allow multiplexing and demultiplexing of information and demonstrated its functionality in 2x2 and 4x4 arrays [108]. Selectivity is achieved as a result of adjusting the threshold voltage by chemically treating the junction.

In November 2005, Yang *et al.* described a method to selectively dope segments of nanowires(*n+/n/n+ etc...*) by varying the dopant modulation, i.e., changing the quantity of dopants during the VLS growth process [109]. They believe that the formation of regions with different electronic properties during the growth phase would reduce the subsequent lithographic patterning steps. They used this varying doped nanowire segment to address individual nanowires in an array.

2.4.2.2 “Top down” approach

Most research on SiNWs conducted thus far has been on SiNWs fabricated by the “bottom up” approach. The “bottom up” approach often encounters problems in

controlling the doping and contact properties of Si nanowires. On the other hand, “top down” approach shows better control and reproducibility of these parameters. For compatibility with Si VLSI technology, it is important that processes are CMOS compatible such that photolithography and self-limiting oxidation methods are more suitable for nanowire fabrication.

Self-limiting oxidation of sub-10nm diameter vertical Si nanowire columns with a tolerance of $\pm 1\text{nm}$ was first reported using a combination of ebeam lithography, reactive ion etching and thermal oxidation [110,111]. The authors found that by using dry oxidation at a temperature of 800°C , the final core diameter self-limits at a minimum of 11nm . At a temperature of 850°C , the core limits at 6nm . Subsequently, they found that the self-limiting phenomenon was found only to occur for oxidation temperatures below 950°C . They postulated that this self limiting phenomenon is due to the increase in activation energy of oxidant diffusivity in a highly stressed oxide. In other words, newly formed SiO_2 has to push out the old oxide to accommodate volume expansion. This oxide layer has to expand more to accommodate a given increase in volume for the Si-O reactions. The smaller the core, the greater the oxide layer has to expand, which causes a greater stress normal to the interface. This retards the process of further oxidation.

Using Deal-Grove’s oxidation model (diffusion limited) with cylindrical boundaries, the oxidation rate dx_o/dt can be expressed as follows.

$$\frac{dx_o}{dt} = \frac{1}{N} \frac{C^*}{(x_o / D)r_c \ln(r_c / r_0)} \quad (\text{Equation 2.3})$$

where N is oxide density, C^* is oxidant solubility in oxide, r_c is the Si core radius, r_0 is the outer radius of oxidized column, and D is the activation energy of diffusion. Using

experimental oxidation rate data, the activation energy of diffusivity were plotted against r_0/r_c . It was found that as r_0/r_c increases, D increases.

As vertical Si nanowire pillars as described above are hard to integrate into a planar technology, Kedzierski *et al.* attempted to fabricate horizontal nanowires [112]. They successfully fabricated 8nm diameter Si nanowires by lithographically defining lines on SOI followed by metal lift-off and Si plasma etch. Stress limited oxidation was done at 875°C to shrink the lines to < 10nm. A key issue is the anisotropic oxidation rates of single crystal Si in the (111), (110) and (100) planes resulting in non-circular Si nanowires. Subsequently in another investigation [114], they found that for the post-oxidation profile to be that of a circular thin wire, Si lines in the <110> direction should be wider than in the <100> direction. This is because the linear oxidation rates for the (100) plane is ~1.6x slower than the rate for the (110) plane.

2.4.3 Electrical characteristics of SiNW MOSFETs

Initial studies of back-gated Si nanowire MOSFETs (10-20nm diameter) by Cui *et al.* showed relatively low transconductance and mobility which was attributed to poor contacts between nanowire and S/D electrodes [105]. By performing S/D Ti-silicidation and passivation of oxide defects, they found improved characteristics [23]. *P*-type transistors were fabricated using the methods described above. A comparison with the planar Si technology showed that nanowire MOSFETs have hole mobilities and SS which are an order of magnitude higher than that of planar Si devices.

N-type back-gated Si nanowire transistors (20nm diameter) were then fabricated using the methods described above and characterized [22]. High series resistance was

measured at $50\text{k}\Omega/\mu\text{m}$ and the current does not saturate at negative biases. Large I_{on} of $10\mu\text{A}$ at $V_d = 1\text{V}$ were observed for $L_g = 2\mu\text{m}$ devices. However, the device does not turn off at $V_g = 0\text{V}$ due to high carrier concentration in heavily doped nanowire. The I_{on}/I_{off} ratio is $> 10^4$ and SS is 300mV/decade . The mobility values measured were comparable to planar Si MOSFETs.

NiSi/Si Schottky contacts have been demonstrated by selective transformation of Si nanowires into metallic NiSi nanowires utilizing evaporation of Ni with thickness equivalent to nanowire diameter and RTA [114]. The heterostructures formed had atomically sharp interfaces. Back-gated transistors showed high I_{on} values. Note that the transistors mentioned here so far utilize metal S/D as ohmic contact and back-gate to induce accumulation or depletion.

Using the method described in Ref [113], Kedzierski fabricated Si nanowires with doped polysilicon gate and measured $I_{on} \sim 800\mu\text{A}/\mu\text{m}$. High $100\text{k}\Omega$ series resistance was measured and is caused by regions of nanowire not covered by the gate. A good SS of 60mV/decade is achieved. It was found that oxide thickness does not strongly affect the threshold voltage due to the improved electrostatics on the reduced dimensions of the nanowire.

Koo *et al.* fabricated back gated SSDMOS using a top down method [24]. By lithography and etch process to define Ti/Cr metal S/D and reactive ion etching to define a 60nm channel width, the transistor was formed without any high temperature steps. The device showed ambipolar characteristics and high threshold voltage $\sim 2\text{V}$. I_{on} did not saturate for $V_g < 0\text{V}$ (accumulation) at high values of V_d which is believed to be due to thinning of the Schottky barrier at the drain end as drain bias increases. The I_{on}/I_{off} ratio

increases as the channel width decreases which is believed to be due to significantly reduced leakage paths of ultra narrow channel body.

Subsequently, dual gated (top and bottom) Schottky barrier silicon nanowire FETs were fabricated in an effort to remove ambipolar conduction [115]. The transistor was fabricated in the manner described above with an extra step to define a Au top electrode. The role of the back gate is to accumulate or invert the channel while the top gate controls the energy profile of the channel. I_{on} was still quite low 40nA at $V_d = 1V$. Scaled transconductance values were high at 1400mS/mm and $SS = 80mV/decade$.

2.4.4 State-of-the-art SiNW MOSFETs

In 2006, ultra narrow p and n GAA SiNW transistors (diameter $\sim 3-6nm$) were fabricated by the Institute of Microelectronics (IME) using top down CMOS processes [20, 116]. The I_{on} values are $\sim 2400\mu A/\mu m$ for NMOS and $\sim 1300\mu A/\mu m$ for PMOS, measured at $V_d = 1.2V$. In addition, excellent $SS \sim 60mV/decade$ and DIBL $\sim 6mV/V$ were achieved. Also, stacked arrays of SiGe nanowires in a GAA MOSFET were demonstrated with $SS \sim 70mV/decade$, high I_{on} / I_{off} ratio, and low leakage current [117, 118]. Recently, CMOS inverters based on the GAA SiNW transistor have been demonstrated which showed sharp transitions, high noise margins, and low power dissipation [119].

From 2005, Samsung Electronics have demonstrated twin SiNW MOSFETs (TSNWFET) with L_g down to 30nm and diameter $\sim 10nm$ on bulk Si [21]. The I_{on} currents are $2640\mu A/\mu m$ and $1110\mu A/\mu m$ at $V_d = 1V$ for NMOS and PMOS respectively, with no threshold voltage roll-off, $SS \sim 70mV/decade$, and DIBL $\sim 20mV/V$. Hot carrier lifetime is ~ 10 years and gate induced drain leakage is smaller than planar MOSFET due

to the low electric fields. This was followed in 2006 by more aggressive scaling of L_g down to 15nm, as well as nanowire diameter down to 4 nm [120]. The PMOS I_{on} was found to exceed NMOS due to the enhanced hole mobility as SiNW diameter is reduced. The gate delays reported were within the ITRS requirements for $L_g = 16\text{nm}$ devices. Subsequently, in 2007, they demonstrated improved PMOS performance by 85% using embedded SiGe S/D stressors as well as an 80% improvement by using $\langle 110 \rangle$ orientation wafers [121].

In addition to SiGe S/D stressors reported by Samsung, Tezuku *et al.* have reported in 2007 strained SiNW N-MOSFET and strained SiGe SiNW P-MOSFETs utilizing a starting substrate of strained SOI and silicon germanium on insulator (SGOI) [122]. The N-MOSFET mobility enhancement is 1.9, while the P-MOSFET mobility enhancement is 1.6 against unstrained SiNW MOSFETS.

Enhanced carrier mobility was also reported in GAA SiNW MOSFETs in 2007 due to oxidation induced tensile stress [123]. The tensile stress have values from 200MPa to 2GPa and are the result of bending of the SiNW due to oxidation induced stress and subsequent removal of SiO_2 by wet etching. The bended SiNW transistors showed a maximum transconductance ~ 2 orders higher than the non-bended SiNW transistors.

GAA SiNW transistors have also been fabricated from bulk wafers without the use of SOI [20, 116-119] or selective epitaxial processes [21, 120, 121] which greatly reduce cost and complexity [124]. The electrical characteristics are comparable with previously reported SiNW transistors with $I_{on} = 1039\mu\text{A}/\mu\text{m}$, $\text{SS} = 72\text{mV}/\text{decade}$, and $\text{DIBL} = 4 - 12\text{mV}/\text{V}$.

Non-volatile flash memory based on semiconductor-oxide-nitride-oxide-semiconductor (SONOS) have recently been investigated using SiNW MOSFETs. In 2007, Suk *et al.* reported for the first time GAA TSNWFET SONOS memory with nanowire diameter ~2-3nm. ΔV_{th} of 5V (between program-erase (P/E) states) is observed with a P/E speed of 100 μ s/10ms and P/E voltage of 10V/-11V. In addition, they observed that as SiNW diameter decreases, faster program speed is observed due to the larger vertical electric field [125]. Lee *et al.* reported a SONOS non-volatile memory using GAA SiNW MOSFET with SiNW diameter ~8nm. The ΔV_{th} is ~1.7V with a 12V/80 μ s program and a -12V/1ms erase time [126]. Fu *et al.* reported a GAA SiNW SONOS with Si nanocrystal on nitride as the trap layer and SiNW diameter of 5nm [127]. The ΔV_{th} is ~3.2V with a 11V/1 μ s program and a -10V/1ms erase time.

Table 2.3. Key electrical performance indices for the state-of-the-art SiNW MOSFETs.

S/N	Diameter (nm)	Channel	L_g (nm)	Gate	T_{ox} (nm)	V_d (V)	I_{on} (μ A/ μ m)	I_{off} (μ A/ μ m)	I_{on}/I_{off}	SS (mV/dec)	DIBL (mV/V)	Year	Ref
N-SiNW MOSFET													
1	3	Si	350	Poly	4	1.2	1.10E+03	5.00E-04	2.20E+06	60	6	2006	20
2	15	Si	30	Poly	2	1	3.45E+03	2.00E-02	1.73E+05	71	31	2005	21
3	10	Si	30	TiN	2	1	2.64E+03	2.00E-03	1.32E+06	71	31	2005	21
4	5	Si	180	Poly	9	1.2	1.00E+03	2.00E-04	5.00E+06	63	10	2006	116
5	30	SiGe	500	Poly	4	1.2	3.00E+02	6.67E-04	4.50E+05	70	20	2007	117
6	8	Si	775	Poly	10	1.2	200	2.00E-05	1.00E+07	71	18	2007	119
7	8	Si	15	TiN	3.5	1	1.44E+03	2.00E-06	7.20E+08	72	50	2006	120
8	8	Si	25	TiN	3.5	1	1.33E+03	2.00E-04	6.65E+06	87	61	2007	121
9	10	Si	130	Poly	5		1.04E+03	2.00E-05	5.20E+07	72	4	2007	124

10	5	Si	55	Poly	ONO 3.8/6.4 /5.1	1	3.00E +02	1.00E- 05	3.00E +07	64	30	2007	126
11	5	Si	850	Poly	ONO 4.5/4.5 /8	1.2	6.00E +02	4.00E- 03	1.50E +05	84	26	2007	127
P-SiNW MOSFET													
4	3	Si	350	Poly	4	-1.2	6.00E +02	6.00E- 04	1.00E +06	65	13	2006	20
5	10	Si	30	TiN	2	-1	1.11E +03	5.60E- 05	1.98E +07	66	15	2005	21
2	5	Si	180	Poly	9	-1.2	8.00E +02	1.00E- 04	8.00E +06	66	20	2006	116
1	30	SiGe	500	Poly	4	-1.2	1.67E +02	6.67E- 06	2.50E +07	62	10	2007	117
3	8	Si	275	Poly	10	-1.2	2.00E +02	8.00E- 06	2.50E +07	63	50	2007	119
6	8	Si	15	TiN	3.5	-1	1.94E +03	1.00E- 06	1.94E +09	71	43	2006	120
7	8	Si	25	TiN	3.5	-1	1.53E +03	3.00E- 04	5.10E +06	78	86	2007	121
8	5	Si	55	Poly	ONO 3.8/6.4 /5.1	-1	2.00E +01	5.00E- 07	4.00E +07	61	45	2007	126

2.5 Summary

The background and relevant theories on ErSi_{2-x} have been discussed. The relevant concepts in MS Schottky barrier formation have been covered, together with the operation and architecture of SSDMOS and the properties, and formation of SiNW. In addition, state-of-the-art SSDMOSs as well as SiNW-based MOSFETs were summarized and presented. Further discussion with regards to the theories will be made in the following sections.

CHAPTER 3

CHARACTERIZATION AND DEVICE FABRICATION METHODS

3.1 Introduction

This chapter describes the material and electrical characterization techniques for the analysis of silicided samples and devices. In addition, Schottky diode and SSDNW MOS fabrication processes are also shown. Several key processing steps will also be described in detail.

3.2 Physical and Chemical Characterization

3.2.1 X-Ray Diffraction

When x-rays interact with a crystalline substance, a diffraction pattern is formed. The XRD pattern of (poly)crystalline material is, therefore, like a fingerprint of the substance. The relationship between the diffraction pattern and the material structure can be described by the Bragg's law [128]. Mathematically,

$$n\lambda = 2d\sin\theta \text{ (Equation 3.1)}$$

where n is an integer, θ is the incident x-ray angle, d is the distance between atoms at a particular plane, and λ is the x-ray source (Cu $K\alpha$) wavelength.

Figure 3.1(a) shows 2 x-ray beams, 1 and 2, with wavelength λ incident at an angle θ on a crystal lattice plane with lattice spacing d . X-ray 2 needs to travel 3 + 4 distance ($2d\sin\theta$) more than 1 to interfere constructively. From Figure 3.1(b), the measurement, r , made from the diffraction pattern, tells us about 2θ . From this, using Bragg's law, we can deduce $1/d$. d spacing is specific for a particular crystal structure or a particular element/compound.

For single crystals, the diffracted beams point to discrete directions each corresponding to a family of diffraction planes. On the other hand, for polycrystalline samples, the diffraction pattern forms a series of diffraction cones as a large number of crystals are oriented randomly. Each diffraction cone corresponds to the diffraction from the same family of crystalline planes in all participating grains. The distance between atoms at a particular plane, d_{hkl} and lattice parameter, a , can be obtained via the following equation [129]

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \quad (\text{Equation 3.2})$$

where h , k , l are the miller indices of the crystal which provides information on the crystal structure.

By continuously varying incident angle θ over a range of values, to satisfy Bragg's law, diffracted beams will be produced, allowing a θ versus intensity plot to be produced. The detected intensities are referenced to joint committee for powder diffraction standards (JCPDS) library for phase and crystal structure identification [130].

A Siemens/Bruker D5005 XRD system was used in our experiments with two main methods of film analysis. Firstly, thin film analysis (Seeman-Bohlin scan) is used when lateral resolution, rather than depth resolution, is important. By using a glancing angle of incidence $\sim 1^\circ$, a large area of the thin film sample is analyzed. An x-ray diffractometer with the Seeman-Bohlin geometry is usually used for phase identification. Secondly, single crystal θ - 2θ scan (Bragg-Brentano scan) is used when depth resolution is important. Single crystal θ - 2θ XRD is not an ideal technique for ultra thin film characterization because of the low sensitivity and the interfering effect of the substrate.

However, due to the highly textured, almost epitaxial to Si substrate ErSi_{2-x} film formed, single crystal θ - 2θ XRD scan was used for phase and crystal structure analysis.

Figure 3.1. Schematics showing (a) diffraction of a light wave incident on lattice points of the sample, and (b) diffracted pattern whose length, r allows θ to be determined.

Bruker D8 AXS general area detector diffraction system (GADDs) utilizes a two-dimensional (2D) detector and high speed electronics for rapid processing of XRD pattern. The background noise is removed, with reduced collection time and greater sensitivity. Each 2D pattern, i.e., Debye diffraction ring, is a plot of diffraction intensity for a particular diffraction angle 2θ (x-axis) with χ (y-axis). High intensity and well-defined spots, either located in the center of the Debye diffraction ring (i.e., $\chi = 0^\circ$) or off-center positions symmetrically, are due to diffractions from highly textured or even epitaxial film while polycrystalline film on the other hand would be typified by rings with uniformly distributed intensity. The main advantage of the GADDs XRD is the improved speed of data collection and 2D collection of diffracted beams which are impossible to detect in the Siemens D5005 XRD with point detector. Pole figure scans were also carried out using the GADDs XRD. In this configuration, the source and the detector

were fixed so that θ is centered at a particular ErSi_{2-x} peak. The sample then rotates from 0° to 360° in 2° intervals. The radius of the circle is the lateral (χ) spread of the detected x-ray. The images give a clearer picture of the preferred orientation or texture of the thin films.

3.2.2 Scanning electron microscopy (SEM)

SEM is a type of electron microscopy capable of producing high-resolution images of a sample surface [131]. Due to the manner in which the image is created, SEM images have a characteristic three-dimensional appearance and are useful for judging the surface structure of the sample. In SEM, focused electron beams of energy $\sim 5 - 30\text{KeV}$ are scanned on a sample. The signal from the reflected secondary and backscattered electrons is used to form a magnified image with dramatically better resolution and depth of view than an optical microscope can give. This is due to the much smaller electron wavelength and higher depth of field compared to the photon.

Secondary electrons which are emitted from the surface atoms form the conventional SEM image whose contrast is determined by the sample morphology. In field emission SEM (FESEM), the images are brighter due to the greater number of electrons emitted per unit area than the traditionally used thermal emitters of tungsten or lanthanum hexaboride. The system is capable of high resolution imaging as well as high quality real time image display at all scan speeds, enabling observation and recording of superior images even in a bright room. Interaction of electron beam with atoms in the sample can also cause shell transitions resulting in the emission of x-rays which have energy characteristics of the element under study. Detection and measurement of the x-ray

energy permits elemental analysis and is known as energy dispersive x-ray spectroscopy (EDS). A JEOL FESEM JSM 6700 was used in our experiments.

3.2.3 Transmission electron microscopy (TEM)

TEM is an imaging technique whereby a beam of electrons is transmitted through very thin specimens. An image is formed, magnified and directed to appear on a fluorescent screen [131]. The main strength of the TEM technique lies in its extremely high resolution $\sim 0.08\text{nm}$. The three primary imaging modes are bright field, dark field, and high resolution TEM (HRTEM). Images formed with only the transmitted electrons are bright field images and images formed with a specific diffracted beam are dark field images. HRTEM gives structural information on the atomic size level and has become very important for interface analysis. A FEI FETEM CM200 and a Philips Tecnai F20 TEM with 200keV acceleration voltage, and 0.2 – 0.15nm spot size were used in our experiments.

3.2.4 Secondary ion mass spectroscopy (SIMS)

The basis of SIMS is a destructive removal of material from a sample by sputtering and the analysis of the removed material by a mass analyzer [131]. A small fraction of the atoms are ejected as positive or negative ions, which are referred to as secondary ions. The mass/charge ratio of the ions is analyzed, detected as a mass spectrum, as a count, or displayed on a fluorescent screen or on a CRT. Quantitative depth profiling, i.e., one selected mass plotted as secondary ion yield versus sputtering time, is a major strength of SIMS. In our experiments, an Ion time-of-flight SIMS (ToF-SIMS) system was used. The

incident beam consists of pulsed ions from a liquid Ga⁺ gun with beam diameters as small as 0.3 μm. For pulse widths on the order of ns, ions are sputtered in a brief burst and the time for these ions to travel to the detector is measured. The kinetic energy of secondary electrons,

$$KE = \frac{1}{2}mv^2 = qV \quad (\text{Equation 3.3})$$

where v is the ion velocity given by L/t_t , V is the accelerating voltage, t_t is the transit time, and L is the distance to the detector. Thus by rearranging the above equation, the mass/charge ratio = $\frac{2Vt_t^2}{L^2}$, which gives the relation of mass/charge to time of flight. A major advantage of ToF-SIMS is the absence of narrow slits in the spectrometer, increasing the ion collection by 10 - 50%. The sputtering rate can be reduced and is so low that it may take an hour to remove a fraction of a monolayer which allows for more accurate depth profiling. Since mass/charge is determined by time of flight, both large and small ion fragments can be detected.

3.3 Electrical Characterization

3.3.1 Electrical Sheet Resistance

Four-terminal probing technique is an electrical impedance measuring technique that uses separate pairs of current-carrying and voltage-sensing electrodes for accurate measurements [131]. Four-point probes are mostly used to measure sheet resistance of thin films. The unit of sheet resistance is Ω/square and is used to describe the surface resistivity of the measured material and is given by

$$R_s = F \frac{V}{I} \text{ (Equation 3.4)}$$

where F is a correction factor depending on sample geometry, V is the voltage measured by the inner 2 probes, and I is the current flowing through the outer 2 probes. This four-point configuration provides for accurate measurement as separation of V and I probes allows the elimination of the impedance contribution of the wiring and contact resistances, given that the voltage electrodes have high output impedance. The resistivity (ρ) is related to the measured sheet resistance by $\rho = R_s \times t$ where t is the film thickness.

3.3.2 Current-voltage measurements

The current-voltage (I - V) characteristics were extracted from the Schottky diodes using MDC semiconductor measurement system equipped with QuietCHUCK 490 DC system for the temperature dependent I - V measurements. The I - V characteristics were extracted from the SSDMOS using Agilent 4157B modular semiconductor parameter analyzer. For the temperature dependent measurement, a Temptronic ThermoChuck System was used.

Φ_b for the Schottky contacts were calculated from the saturation current (I_s) from the room temperature I - V using Equation 4.1. The Φ_b determined in this way is the zero bias Φ_b . Using temperature dependent I - V , zero bias Φ_b for the Schottky contacts and bias dependent Φ_b for the SSDMOS were also determined. The Richardsons plot ($\ln(I_s/T^2$ vs. $1/T$) can be graphed and used to obtain the activation energy or Φ_b .

3.3.3 Capacitance-voltage

The capacitance-voltage (C - V) characteristics were extracted from the Schottky diodes using MDC semiconductor measurement system. When a small ac voltage is superimposed upon a dc bias, the incremental charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. The depletion capacitance is given by [51]

$$C = \sqrt{\frac{q\epsilon_s\epsilon_0 N_a}{2(V_{bi} + V - kT/q)}} \quad (\text{Equation 3.5})$$

where q is the electronic charge, k is the boltzmanns constant, ϵ_s and ϵ_0 are the relative and free space permittivities, N_a is the doping concentration, V_{bi} is the built in potential, and V is the applied voltage. By extracting the V_{bi} from the C - V curve, the Φ_b for the Schottky contacts can be derived using the relation $\Phi_{beff} = V_{bi} + V_0 + kT/q$ where $qV_0 = E_c - E_f$, and E_c and E_f are the semiconductor conduction band and Fermi levels, respectively.

3.4 Fabrication of Schottky Source/Drain Silicon Nanowire MOSFETs

3.4.1 Key device fabrication equipment

Metal deposition

Sputter deposition is a method based on physical vapor deposition (PVD) and involves the erosion of material from a source target which then deposits onto a substrate [132]. It is one of the most widely used techniques for the deposition of thin metal films for vias and lines, diffusion barriers, and metal contacts etc [133].

This method uses bombardment of metal targets by highly energetic chemically inert ions which in our case is Ar^+ . A magnetron utilizes strong electric and magnetic fields to trap electrons in helical paths close to the surface of the magnetron which in turn ionizes the Ar gas. The bombardment causes ejection of the target atoms which are subsequently deposited on the surface of the Si substrate located below the metal target. The advantages of sputtering as a deposition technique is that firstly, the deposited films have the same composition as the source material and secondly, the deposition rate is high. The higher rate of deposition would result in lower impurity incorporation because fewer impurities are able to reach the surface of the substrate in the same amount of time.

A Discovery 18 DC/RF Research Magnetron Sputter Deposition System was used with features such as automation, DC and RF power supply, base vacuum of 3×10^{-7} Torr and 3 confocally-mounted cathodes which provide better than $\pm 5\%$ uniformity. The targets used for the deposition were of 99.99 at. % purity and included Er, Ti, Ni and Pt targets.

Rapid thermal annealing

RTA is a process that rapidly increases the temperature of the wafer sample and maintains it at set temperatures (up to 1200°C) for short periods of time (typically less than 60sec) [6]. The wafer temperature must be brought down slowly to minimize thermal shock. The rapid heating is accomplished using high power halogen-quartz lamps. RTA is able to achieve short processing times as the radiant energy from the lamps are selectively absorbed by the wafers while the quartz chamber does not absorb the radiant energy.

For our purposes, RTA was carried out for silicidation, i.e., the solid state reaction of the metal and Si into a thermodynamically more stable state. Silicidation by RTA is a fast method to obtain silicides with good film uniformity [134]. All RTA experiments were carried out by a XM80 rapid thermal annealing system.

3.4.2 Fabrication of ErSi_{2-x} thin films and Schottky contacts

P-type Si wafers with resistivities of 5 – 10 $\Omega\text{-cm}$ were used as starting substrates to fabricate ErSi_{2-x} thin films and Schottky contacts. The wafers were cleaned using standard Radio Corporation of America (RCA) process which is used in the semiconductor industry to remove oxide and other contaminants [6]. The RCA cleaning consists of two steps. The wafers were immersed in SC1 ($\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$) with a ratio of (1 : 1: 5) for 10 min at 75°C. This was followed by a 10 cycle de-ionized (DI) water rinse. This step is to remove organic residue. Subsequently, the wafers were immersed in SC2 ($\text{HCl} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$) with a ratio of (1:1: 6) for 10min at 75°C, followed by a 10 cycle of DI water rinse. This step is to remove non-oxide contaminants such as metal. Native oxide removal was achieved through immersing the wafers in HF solution ($\text{HF} : \text{H}_2\text{O}$) with a ratio of (1 : 5) for 1 minute. The wafers were then dried by N_2 flow before immediately loading it into the sputtering vacuum chamber.

To investigate the effects of amorphization, two methods were used to amorphize the Si substrates and are described as follows. (1) *in-situ* Ar plasma sputtering was carried out on some wafers by RF Ar for 120s at a power of 100W within the sputter chamber. Ar pre-sputtering is a dry cleaning method to physically sputter surface impurities away from the wafer however it also induces Si surface amorphization and roughness [135]. (2)

In some wafers, prior to the RCA clean, amorphization of the Si substrates was carried out using Si implantation (30keV and 1×10^{15} atoms.cm⁻²). Table 3.1 shows the parameters for the respective amorphization species. The projected range was taken to be the upper depth limit of the amorphous layer on the Si(100) substrate.

Table 3.1. Projected range of Si and Ar implanted in Si substrate by stopping and range of ions in matter (SRIM) calculations.

Species	Dosage (cm ⁻²)	Energy (eV)	Projected Range (nm)
Si	1×10^{15}	30000	44.4
Ar	5×10^{14}	180	1.4

The dosages for the respective species are above the threshold dose for amorphization.

A 50nm thick Er film was then deposited at room temperature in the DC magnetron sputtering chamber with a base pressure of 3×10^{-7} torr. In some samples, a contact mask with 1mm diameter circular holes was used as a physical barrier for selective erbium deposition during the sputter deposition process to fabricate Schottky contacts.

To investigate the effect of Ti based capping, the Er deposition was followed by a sequential deposition of (1) 20nm TiN capping, (2) 30nm TiN capping, or (3) 10nm Ti/20nm TiN double capping layer without breaking vacuum. RTA was then carried out with temperature ranging from 400°C – 800°C in an N₂ ambient for 60s. For the Schottky contact samples, a layer of 2000Å Au was deposited on the backside of the wafer samples to form ohmic contact for electrical measurements.

3.4.3 Process flow

This section gives an overview of the CMOS processing steps of the back-gated ErSi_{2-x} SSDNWMOS and the GAA ErSi_{2-x} , PtSi and NiSi SSDNWMOS. PtSi SSDNWMOS is fabricated to provide complementary transistor action with ErSi_{2-x} while NiSi is fabricated in an attempt to use a single silicide for complementary transistor action.

Figure 3.2. Schematic of SiNW processing up to nanowire oxidation. (a) Starting 200-mm *p*-type (001) SOI wafers, (b) after fin (~40 - 60nm wide) lithography, (c) after top silicon etch down to the BOX layer, and (d) after dry oxidation at 875°C for 4 ½ hours.

The CMOS processing steps are simplified with only two lithography steps, active area definition (fin channel connected to large area 100 μ m by 100 μ m Si pads), and gate definition.

Figure 3.2 shows the schematics of the processing steps common to both back-gated and GAA SSDNWMOS [20, 117]. Figure 3.2(a) shows the starting wafers on which the devices were fabricated. The wafer specifications are as follows: 200-mm *p*-type (100) SOI wafers with resistivity of 5 – 10 Ω -cm and a top silicon thickness of 120nm sitting on a 150nm buried oxide. In some wafers designated as PMOS devices, P with a 50keV energy and a dose of 2×10^{11} atoms.cm⁻² was implanted into the top SOI layer followed by furnace activation for 30min at 950°C. For the back-gated devices, B with a 60KeV energy and a dose of 4×10^{15} atoms.cm⁻² was implanted on the Si wafer backside to serve as a gate electrode. Figure 3.2(b) shows the lithographic patterning of the active area. Each device consists of a thin fin (~120nm fin width) connected to two wider S/D extension regions which are in turn connected to 100 μ m by 100 μ m pads (for electrical probing). They were patterned using 248nm KrF lithography in conjunction with alternating phase shift mask to achieve the target developed photoresist (PR) critical dimension (CD) of ~140nm [133]. Subsequently, after PR trimming, the PR CD attains a value of ~40nm to 60nm. Figure 3.2(c) shows the transferred PR pattern onto the SOI layer achieved by deep reactive ion etching (DRIE) of the 120nm top SOI layer down to the BOX layer which will be explained in Section 3.4.4. Figure 3.2(d) shows the SiNW channels converted from the thin Si fin. This is achieved by oxidation of the wafer in dry O₂ at 875°C for 4 ½ hours in a furnace tube which results in two stressed limited SiNWs [113] formed at the top and bottom of the Si fin [20, 117].

Figure 3.3 shows the processing steps specific to the back-gated ErSi_{2-x} SSDNWMOS which are continued from the processing steps of Figure 3.2. Figure 3.3(a) shows the device after the top SiNW was removed by using a timed 500Å SiO_2 plasma etch. The plasma etch removes $\sim 350\text{\AA}$ of thermal SiO_2 formed from the SiNW dry oxidation. The plasma etch also removes $\sim 50 - 100\text{\AA}$ of Si resulting in the removal of the top SiNW.

Figure 3.3. Schematic of back-gated SSDNWMOS processes continued from Figure 3.2. (a) after top SiNW removal, (b) after Si_3N_4 deposition and dummy gate lithography, (c)

after Si_3N_4 etch down to the BOX layer and metal deposition, and (d) after silicidation using an optimized RTA condition.

Figure 3.3(b) shows the device after a 1000Å Si_3N_4 PECVD deposition and gate lithography. The Si_3N_4 gate was etched using a plasma etcher utilizing end point detection. The main purpose of the Si_3N_4 dummy gate serves to isolate the source and drain during silicidation process and does not serve as a gate electrode. Erbium and TiN/Ti (protective capping layer) were sputtered sequentially using a PVD system without breaking vacuum as shown in Figure 3.3(c). Silicidation was done by RTA at 450°C for 60s in an N_2 ambient. The TiN and unreacted Er were then chemically etched and the final back gated ErSi_{2-x} SSDNWMOS is shown in Figure 3.3(d).

Figure 3.4 shows the processing steps specific to the GAA SSDNWMOS which are continued from the processing steps of Figure 3.2(d). Figure 3.4(a) shows the exposed SiNWs connected to the larger Si pads after immersing in a DHF solution for 5 mins which etches the thermal SiO_2 formed during SiNW dry oxidation (See Figure 2.2(d)) and also part of the BOX layer.

Figure 3.4(b) shows the device after the gate stack deposition and gate lithography. The gate stack consists of a 90Å thermal SiO_2 grown by a dry oxidation process at 700°C followed by a 1300Å polysilicon deposition at 550°C. The polysilicon was then P doped to a dose of $5.5 \times 10^{15} \text{ atoms.cm}^{-2}$ at 40keV or BF_2 doped to a dose of $4 \times 10^{15} \text{ atoms.cm}^{-2}$ at 35keV for N and P-SSDNWMOS respectively. Gate lithography was then carried out followed by etching using Cl_2 and HBr chemistry in a plasma etcher which utilizes end point detection as shown in Figure 3.4(c).

- SiNW release by etching in DHF (1:25) solution for 5 mins, DI water rinse, and low spin 300rpm spin dry.

- 90Å SiO₂ gate oxide growth by furnace oxidation for 700° C, 60min.

- 1300Å polysilicon deposition by furnace LPCVD at 550° C.

- Gate implantation and activation.

- 4100Å PR on 600Å BARC deposition followed by exposure using gate recticle.

- 1300Å gate etch by end point detection using an Applied Materials P5000 plasma etcher.

- 100Å USG PECVD deposition.

- 350Å SiN LPCVD furnace deposition.

- Spacer etch using TEL dielectric etcher.

- In some wafers, low energy ion implantation was done without activation.

- Ni, Er, and Pt deposition using PVD sputtering system.

Figure 3.4. Schematic of GAA SSDNWMOS processes continued from Figure 3.2(d). (a) SiO₂ removal, (b) after polysilicon/SiO₂ gate stack formation lithography, (c) after polysilicon etch down to the BOX layer, (d) after SiO₂/Si₃N₄ spacer formation, (e) after metal deposition, and (f) after silicidation using optimized RTA conditions.

A 100Å PECVD SiO₂ was then deposited followed by a 350Å LPCVD Si₃N₄ which serves as the self-aligned spacer as shown in Figure 3.4(d). The Si₃N₄ was then etched using CHF₃ chemistry in a plasma etcher utilizing end point detection which resulted in a 350Å wide spacer. For some of the NiSi NMOS wafers, a low energy As implant (4×10^{14} atoms.cm⁻²/10keV) was conducted without activation after the spacer formation and prior to the metal deposition to introduce dopant segregation during silicidation. Er/Ti/TiN, and Ni for N-SSDNWMOS, and Pt, and Ni for P-SSDNWMOS were sputtered using a PVD system as shown in Figure 3.4(e). Silicidation was done by RTA from 400°C - 450°C for 60s in an N₂ ambient followed by unreacted metal etch and the final GAA ErSi_{2-x}, PtSi and NiSi SSDNWMOS as shown in Figure 3.4(f). A few important processing steps will be highlighted in the next few sections.

3.4.4 Formation of Silicon nanowires

The physics of nanowire formation has already been discussed in Chapter 2. In this section, the processes involved in the SiNW formation are described. Figures 3.5(a) and

(b) shows the tilted view SEM image of a single SiNW device after ~120nm SOI etch and PR removal. The Si etching was carried out by a STS DRIE etcher. In this process, deep vertical anisotropic Si etch is achieved at a fast rate by using alternating passivation and etching steps.

Figure 3.5. Tilted view SEM images of the channel region of a single device showing the lithographically defined Si fin with $L_{ch} = 350\text{nm}$. (a) SEM at 0° stage rotation, and (b) SEM at 45° stage rotation. SiNW channels converted from the thin Si fin. (c) Single SiNW channel, and (d) single stacked SiNW channel.

Firstly, C_4F_8 based plasma is used to conformally condense a few monolayers of polymer across all surfaces exposed to the plasma. Secondly, the plasma gas is then switched to SF_6 to create a plasma chemistry that anisotropically etches silicon. Lastly, through the application of a dc bias to the plate, ions from the plasma bombard the Si surface parallel to the wafer surface at a much higher rate. This etching is done by a fluorine-based species while the remaining polymer protects the vertical walls of the trench from etching.

The 40 – 60nm wide Si fin was then oxidized in a dry O_2 at 875°C for 4 ½ hours which results in two self limited Si nanowires [20, 113, 117], one at the top and the other at the bottom of the Si fin as shown in Figure 3.5(c) and (d). The oxidation was done in an 8 inch furnace tube where dry O_2 is introduced and reacts with silicon at a rate of $\sim 100\text{\AA/hr}$. The SiNW L_{ch} of interest varies from 100nm – 1000nm which is defined by the active area lithography (see Figure 3.2(c)).

The cross sectional TEM (XTEM) micrographs of the single SiNW channel shown Figure 3.5(c) are shown in Figures 3.6(a) and (b). The TEM analysis shows that the nanowire is triangular in shape with a base of $\sim 8\text{nm}$ and $\sim 9\text{nm}$ for channel length (L_{ch}) = 500nm and 1000nm devices respectively. The apex of the triangle is directed upwards in the $\langle 100 \rangle$ direction. The SiNWs of Figure 3.6(a) and (b) were eventually further processed to form the back-gated $ErSi_{2-x}$ SSDNWMOS.

The XTEM micrographs of a single stacked SiNW channel shown in Figure 3.5(d) are shown in Figures 3.6(c) and (d). From the TEM analysis in Figure 3.6(c), it can be seen that the top SiNW has a width of $\sim 8\text{nm}$, and the bottom SiNW has a width of $\sim 5\text{nm}$. The apexes are facing down in the $\langle \bar{1}00 \rangle$ direction for the top SiNW and up in the

$\langle 100 \rangle$ direction for the bottom SiNW. The triangular shape of the stacked wires is a result of the faster oxidation rates in the $\langle 110 \rangle$ directions, i.e., the sidewalls of the Si fin, resulting in the meeting of oxidation fronts of the opposite sidewalls “pinching” off the Si fin. Figure 3.6(d) shows the HRTEM micrograph of the bottom SiNW surrounded by a layer of 90Å thermally grown SiO_2 gate dielectric followed by a layer of polysilicon. The SiNWs of Figure 3.6(c) and (d) were then used to fabricate the GAA ErSi_{2-x} , PtSi and NiSi SSDNWMOS.

Figure 3.6. (a) XTEM of a SiNW with $L_{ch} = 1000\text{nm}$ showing a triangular shaped SiNW with a $\sim 9\text{nm}$ width, and (b) HRTEM of a SiNW with $L_{ch} = 500\text{nm}$ and $\sim 8\text{nm}$ width. (c) XTEM of a GAA SSDNWMOS showing a single stacked SiNW of widths $\sim 8\text{nm}$ (top) and $\sim 5\text{nm}$ (bottom), and (d) HRTEM of the bottom SiNW.

3.4.5 Metal-semiconductor junction size control

The developed SSDNWMOS gate electrode wraps around the SiNW channel. Each gate length (L_g) can be controlled by lithography exposure and dose and is unique for each L_{ch} varying between 100nm and 1000nm.

Varying gate length

Figure 3.7. SEM micrographs of a back-gated SSDNWMOS Si_3N_4 dummy gate with $L_{ch} = 300\text{nm}$. Tilted-view SEM (a) after smaller L_g lithography, and (b) after larger gate length lithography. Top-view SEM of completed device with (c) smaller Si_3N_4 dummy gate, and (d) larger Si_3N_4 dummy gate. The inserts show the schematic representations of the two different gates.

For the back-gated SSDNWMOS, the Si_3N_4 dummy gate only serves to separate the source from the drain to allow for self-aligned Er-silicidation. Furthermore, we are able to approximately control the size of the $\text{ErSi}_{2-x}/\text{Si}$ metal-semiconductor junction. This is determined by varying the dummy Si_3N_4 L_g as indicated in Figure 3.7, and is possible due to the presence of intermediate curved extensions that increases in width from the SiNW channel to the larger S/D pads as can be seen in Figure 3.5(c). The dummy Si_3N_4 L_g can be determined by lithography as indicated in Figures 3.7(a) and (b). Note that the size of the $\text{ErSi}_{2-x}/\text{Si}$ metal-semiconductor junction is approximately determined from the top-view SEM images as seen in Figures 3.7(c) and (d).

For example, Figure 3.7(d) shows that the larger dummy Si_3N_4 L_g is ~50nm larger per side as compared to the smaller dummy Si_3N_4 L_g in Figure 3.7(c). After silicidation, the $\text{ErSi}_{2-x}/\text{Si}$ junction for the larger Si_3N_4 dummy gate is larger by ~10 times (80nm for the larger Si_3N_4 dummy gate vs. 8nm for the smaller Si_3N_4 dummy gate as shown in the inserts to Figure 3.7(c) and (d)). The L_{ch} of interest for the back-gated SSDNWMOS is from 200nm – 1000nm.

Gate misalignment

In the GAA SSDNWMOS with the Si_3N_4 spacer, the SiO_2 gate dielectric and the polysilicon gate electrode completely surround the SiNW channel as can be seen in Figure 3.6(d). In order to create a nano-sized MS junction, the polysilicon gate was lithographically misaligned slightly to the left by 20nm. This resulted in MS junction size of ~35nm at the source (left) and ~6nm at the drain (right) for the 90nm gate length (L_g) device as shown in from Figure 3.8(a). Depending on whether a potential is applied to the

source or drain, electrons/holes can be made to travel through either the (reverse biased) MS Schottky junction having a size of $\sim 35\text{nm}$ or the MS Schottky junction having a size of $\sim 6\text{nm}$.

Figure 3.8. (a) Top view SEM micrograph of GAA SSDNWMOS with $L_{ch} = 140\text{nm}$ and a misaligned gate of $\sim 20\text{nm}$ to the left. The inset shows lower magnification SEM image. (b) Plot of exposed junction size against L_g and L_{ch} for the GAA SSDNWMOS. Exposed junction size and L_g are determined from the top view SEM micrographs. Note that L_{ch} is

determined by the active area lithography while L_g is defined by gate lithography/resist trimming with $L_g < L_{ch}$.

Using the top view SEM analysis of GAA SSDNWMOS with different L_{ch} , we are able to match L_{ch} with the equivalent L_g and MS junction size. This relation is plotted in Figure 3.8(b). In this way, we are able to empirically observe the difference in electrical transport with varying MS junction size.

3.4.6 Source/Drain metal silicide formation

Figure 3.9. SEM micrograph of a complete back-gated SSDNWMOS with $L_{ch} = 300\text{nm}$ (a) before silicidation, and (b) after silicidation.

The silicide films were formed by sputter depositing metal on the devices followed by rapid thermal annealing. A back-gated SSDNWMOS device after the Si_3N_4 dummy gate etch and prior to the silicidation is shown in Figure 3.9(a). The corresponding GAA SSDNWMOS device after the Si_3N_4 spacer etch and prior to the silicidation is shown in Figure 3.10. A single stacked SiNW device is shown in Figure 3.10(a), and (c), while the

twin stacked SiNW device in Figure 3.10(b). All wafers were cleaned before metal deposition using the method described in Section 3.4.2.

Figure 3.10. Tilted view SEM of a completed GAA SSDNWMOS before silicidation. (a) Single stacked SiNW device with $L_{ch} = 350\text{nm}$, (b) twin stacked SiNW device with $L_{ch} = 200\text{nm}$, and (c) top view SEM micrograph of a GAA SSDNWMOS before silicidation with $L_{ch} = 350\text{nm}$. (d) Top view SEM of a completed GAA NiSi SSDNWMOS after silicidation with $L_{ch} = 350\text{nm}$.

For the formation of the SSDNWMOS devices, the deposition conditions were similar to the fabrication of ErSi_{2-x} thin films and Schottky contacts described in Section

3.4.2, i.e., room temperature sputtering in a chamber with a base pressure of 3×10^{-7} torr. All devices were *in-situ* capped with a layer of 20nm TiN on top of 10nm Ti. In addition, silicidation was carried out at an optimized temperature of 450°C for 60 seconds in an N₂ ambient. The TiN, Ti and unreacted Er were removed by immersing it into a sulphuric peroxide mixture (SPM) with H₂SO₄:H₂O₂ ~ 1:1 for 5 minutes and a completed back-gated ErSi_{2-x} SSDNWMOS is shown in Figure 3.9(b). The Er-silicidation process for the GAA ErSi_{2-x} SSDNWMOS is similar.

For the PtSi and NiSi films, the deposition conditions were similar to that of the ErSi_{2-x} films except that no capping layers were used. Both silicidations were carried out at an optimized temperature of 400°C for 60 seconds at in an N₂ ambient. The unreacted Pt and Ni were chemically etched by immersing it in a heated aqua regia (HNO₃:HCL~3:1) and Piranha solution (H₂SO₄:H₂O₂~4:1) for 5 minutes. The completed GAA NiSi SSDNWMOS is shown in Figure 3.10(d).

Figure 3.11. SIMS depth profile of silicided S/D pads of SSDNWMOS. (a) Back-gated ErSi_{2-x} annealed at 450°C for 60secs. (a) GAA NiSi annealed at 400°C for 60secs.

The silicide depth composition and thickness were studied using a SIMS depth profile analysis on the S/D pads and the results are shown in Figure 3.11. The entire active Si pads were fully consumed, leading to the formation of $\text{ErSi}_{2-x}/\text{SiNW}$ and NiSi/SiNW Schottky barrier at the two ends of the SiNW channel.

3.5 Summary

Various topics in semiconductor metrology for materials and electrical characterization of the ErSi_{2-x} thin films, Schottky diodes and SSDNWMOS were briefly discussed. The device fabrication processes for SSDNWMOS were also described with emphasis on several key process steps. Unless otherwise stated, the subsequent chapters follow the experimental procedures and processes described in this chapter.

CHAPTER 4

METHODS OF RTA SILICIDED ErSi_{2-x} THIN FILM IMPROVEMENTS FOR DEVICE APPLICATIONS

4.1 Introduction

In this chapter, we characterize the ErSi_{2-x} thin film formed by the solid state erbium/silicon reaction by RTA with a particular emphasis on new pyramidal structural defect. We discuss the defect formation and its electrical signature. The effects of surface preparation techniques (e.g. low energy Ar ions sputter and Si PAI) and post erbium deposition *in-situ* Ti capping layers were studied and the subsequent improvements in material and electrical characteristics are discussed.

4.2 Materials Characterization of RTA Silicided ErSi_{2-x}

As mentioned in Chapter 2, ErSi_{2-x} is being heavily investigated for SSDMOS applications due to its low barrier to the inverted *n*-channel [136], low formation temperature [25] and epitaxy of silicide layer to the underlying Si substrate [27]. However, ErSi_{2-x} is extremely sensitive to oxidation [25] and also exhibits rough morphology in solid state reactions of Er and Si [35, 137] which can potentially degrade the electrical characteristics of devices.

In this section, materials study of $\text{ErSi}_{2-x}/\text{Si}(001)$ as a potential material system for SSDMOS applications is studied. Substrate amorphization and *in-situ* Ti capping were not carried out. The material characterization was done in an effort to understand the

mechanism of defect formation.

4.2.1 Structural and chemical characteristics

Figure 4.1 shows a typical θ - 2θ single crystal XRD general area detector diffraction system (GADDs) pattern for an Er film deposited on Si(001) and annealed for 60secs at 500°C (temperatures up to 800°C showed similar results) in an N₂ ambient. This figure shows the $\{1\bar{1}00\}$, $\{2\bar{2}00\}$, $\{1\bar{1}01\}$, and $\{1\bar{1}02\}$ peaks of AlB₂ hexagonal erbium disilicide. The observation of dominant $\{1\bar{1}00\}$ and $\{2\bar{2}00\}$ peaks in the 2θ scans suggests that ErSi_{2-x} $\{1\bar{1}00\}$ is oriented parallel to the (001) Si substrate surface, i.e., the c-axis of ErSi_{2-x} lies parallel to the substrate. Furthermore, the observation of the two $\{1\bar{1}01\}$ peaks symmetrically displaced from the central axis (containing the $\{1\bar{1}00\}$ and $\{2\bar{2}00\}$ peaks) implies that this is not simply a fiber texture, but that there is a strong in-plane texture as well.

To study the residual strain on the ErSi_{2-x} film after RTA, a comparison between the experimental 2θ values and the relaxed ErSi_{2-x} film was carried out. The relaxed 2θ value was found using the ErSi_{2-x} JCPDS file. The d-spacing of the $(1\bar{1}00)$ plane for ErSi_{2-x} extracted from the experimental 2θ values is 0.48% larger than the corresponding values for the relaxed ErSi_{2-x} film. The observation of a larger d-spacing of the $(1\bar{1}00)$ planes from the θ - 2θ XRD measurement is due to the presence of a biaxial and compressive strain in the epitaxial ErSi_{2-x} film (-2.7% for ErSi_{2-x} [139]), which results in the increase of the d-spacing of the ErSi_{2-x} $(1\bar{1}00)$ planes oriented parallel to the (001) Si substrate plane.

Figure 4.1. GADDS θ - 2θ single crystal XRD scans of an ErSi_{2-x} film formed on a Si(001) substrate annealed at 500°C for 60s in an N_2 ambient. The x-axis are 2θ and the y-axis are χ . The counts vs. 2θ plot is an integration of χ along the entire range of 2θ . The insert on the top right corner is the pole figure along the ErSi_{2-x} $\{1\bar{1}00\}$ direction.

The insert in Figure 4.1 shows a pole figure of the same film. The four-fold symmetry (rather than the two-fold symmetry expected if the ErSi_{2-x} were a single crystal) confirms that there are two distinct ErSi_{2-x} epitaxial orientations relative to the Si substrate. That is, the ErSi_{2-x} film contains both regions where the [0001] (i.e., c-axis) is parallel to Si[110] and regions where it is parallel to Si[1 $\bar{1}$ 0], in agreement with the previous reports [27, 37, 43]. All films grown on the crystalline Si substrate and annealed between 500 and 800°C exhibited epitaxy.

Figure 4.2(a) shows an optical image of the ErSi_{2-x} film on a Si(001) substrate and annealed at 500°C for 60 s in an N_2 ambient. The samples show the presence of square-

shaped structural defects of length 4–8 μm , and have a density in the order of $\sim 10^5 \text{ cm}^{-2}$. The edges of the square-shaped defects align along the Si $\langle 110 \rangle$ directions of the underlying Si(001) substrate. The structural defects were also observed in samples annealed at $500 \leq T \leq 800^\circ\text{C}$.

Figure 4.2(b) shows a higher magnification image of the region marked by a dotted box in Figure 4.2(a). The surface of the ErSi_{2-x} thin film shows the presence of many square shaped depressions or ‘pits’. Atomic force microscopy (AFM) results of the depressions/‘pits’ are shown in Figure 4.2(c). They form simultaneously with the square-shaped structural defects during RTA, but are believed to have different formation mechanisms. These ‘pits’ have been similarly observed in ErSi_{2-x} thin films formed by furnace annealing [25, 35, 37, 39, 41].

Figure 4.2(c) shows AFM images of the ErSi_{2-x} film from a similar area as Figure 4.2(b). The ErSi_{2-x} film shows that the surface is rough and undulating with the presence of ‘pits’ with an average length of 2 μm and an average depth of $\sim 25\text{nm}$ as determined from the AFM linear scan. The surface roughness of the film measured in RMS (RQ) is $\sim 6.07\text{nm}$. Figure 4.2(d) shows a cross sectional SEM micrograph across the square-shaped structural defect marked by a dotted line in Figure 4.2(a). From the image, the ErSi_{2-x} film appears to be delaminated from the Si surface, suggesting a formation mechanism that is stress related [37]. Further analysis of the square-shaped defect will be carried out in Section 4.2.2.

Figure 4.2. (a) Optical plane view image of an ErSi_{2-x} film surface showing pyramid structural defects. (b) Optical plane view image at higher magnification of the area bounded by the dotted square in (a). (c) AFM of the area bounded by the dotted square, and (d) cross-sectional SEM image of a pyramid structural defect across the defect shown by the dotted line in (a).

These ‘pits’ formed could be detrimental to the electrical performance of SSDMOS as well as causing inaccurate determination of Φ_b . Contaminant barrier induced surface ‘pitting’ [35], Stranski-Krastanov growth of epitaxial silicide islands leading to polycrystalline silicide recessed regions [38, 39], and lifting off of RESi₂ from the substrate induced surface pitting have been reported [37]. All these involve a preferential path for Si diffusion resulting in the observed rough morphology and ‘pitting’. Also, there is a strong substrate orientation effect as evidenced by the square and triangular shaped pits found on RESi₂ films grown on Si(100) and Si(111) respectively [140]. It is believed that the ‘pit’s observed in our RTA-ed ErSi_{2-x} films are similar and have similar

formation mechanisms as the ‘pits’ found on the furnace annealed ErSi_{2-x} films previously reported.

Figure 4.3. 3D XPS Er4d depth profile of an ErSi_{2-x} film on a Si(001) substrate annealed at 500°C for 60 s in an N_2 ambient.

Figure 4.3 shows the x-ray photoelectron spectroscopy (XPS) Er4d spectrum of the ErSi_{2-x} thin film shown in Figure 4.2. The first layer near the surface has a binding energy near 169eV which is between the reported peak of Er/O and Er_2O_3 [141] indicating that the top two layers consist of polycrystalline Er_2O_3 or erbium silicate. RE elements are extremely prone to oxidation and form RE_2O_3 readily even at room temperature, leading to the inhibition of the formation of the RESi_2 [140]. Layers 3 to 7 have characteristic double peaks at 167.4 and 169.5eV [44] which indicate the formation of ~45nm thick ErSi_{2-x} from a depth of 35nm – 80nm.

4.2.2 Pyramidal structural defects in ErSi_{2-x} thin films : Physical analysis and formation mechanism

In order to further analyze the square-shaped structural defects seen in Figure 4.2(a) and (d), SEM, AFM and XTEM characterization were carried out so as to propose a defect formation mechanism.

Figure 4.4. ErSi_{2-x} film on a Si(001) substrate annealed at 500°C for 60 s in an N_2 ambient. Plane view SEM micrograph of a square-shaped structural defect with (a) flat apex, and (b) pointed apex. (c) AFM micrograph showing the pyramidal shape of the defect. The linear scan across the pyramidal defect shows the shape and height profile more clearly.

Figure 4.4(a) shows a plane view SEM micrograph of a particular square-shaped structural defect. This defect is cracked along three of the four side edges providing evidence that the cracks could have been caused by stress induced by the thin ErSi_{2-x}

film. This defect exhibits a sunken surface in the middle leading to a flat apex, which suggests that it could be hollow in the middle. On the other hand, some square-shaped defects appear to have a pointed apex as shown in Figure 4.4(b), leading to a pyramidal shape. Figure 4.4(c) shows an AFM image of the defect shown in Figure 4.4(b). The cross height profile confirms that the square-shape structural defects are indeed pyramidal in nature with the apex pointing away from the Si/ErSi_{2-x} interface.

Figure 4.5. XTEM micrographs of pyramidal structural defects on an erbium silicide film annealed at 500°C for 60s in an N₂ ambient. (a) shows a buckled region that is completely filled with Si, while (b) shows a void at the center of the defect that extends from film to interface. (c) shows a HRTEM image and the corresponding electron diffraction pattern of the defective Si region between the buckled film and the original interface.

In the samples that were annealed in vacuum or capped with an *in-situ* Ti based capped layer, similar defects were also found indicating that the formation of these defects is not associated with oxidation. To our knowledge, the presence of such

pyramidal defects has not previously been reported. On the other hand, earlier reports suggest that pits penetrating into the Si substrate form when ErSi_{2-x} films are grown on Si(100) at low temperatures [35, 41, 140].

In order to observe the details of the ‘pyramids’ with better resolution, TEM was carried out on the sample. Figure 4.5 shows XTEM of pyramidal defects similar to those shown in Figure 4.4. In Figure 4.5(a), the space between the ErSi_{2-x} film and the original Si substrate surface is filled with Si, as confirmed using electron dispersive spectroscopy. In Figure 4.5(b), the intervening space is only partially filled with Si; i.e., there is a void below the pyramid apex that extends from the film to the substrate. In both cases, the silicon between the film and original substrate surface is highly defective. The electron diffraction and high resolution TEM analysis of the defective area (see the insets in Figure 4.5) shows that the defective region of the Si consists of a dense array of parallel stacking faults on $\{111\}$ ($(a/6)\langle 110 \rangle$ translations).

It must be mentioned that the pyramidal defects are absent from ErSi_{2-x} films that were formed on Si wafers with substrate amorphization (amorphous layer extends 45nm and 1.4nm from the wafer surface for the PAI-ed substrate and Ar plasma cleaned substrate respectively) as described in Section 3.4.2. The substrate dependence indicates that ErSi_{2-x} epitaxy with underlying Si substrate is essential in pyramid structural defect formation. The effect of substrate amorphization will be discussed in Section 4.3.

The hexagonal ErSi_{2-x} forms on Si(100) with its $[0001]$ axis parallel to $\text{Si}\langle 110 \rangle$. The mismatch parallel to the c-axis is -6.5% (compressive) and $+1.1\%$ (tensile) perpendicular to the c-axis. The diffraction data and previous reports [27, 28, 142] show that the ErSi_{2-x} film consists of alternating grains with the c-axis parallel to $[110]$ and $[\bar{1}10]$. The grain

size is typically 50–150 nm [28, 142], which is much smaller than the lateral extent of the pyramidal defects. Therefore, the misfit strain, as measured on a scale larger than several grains is biaxial and compressive with a value of -2.7% .

Figure 4.6. Schematic representations of the formation and evolution of the pyramidal defect, showing (a) the initial, compressively stressed ErSi_{2-x} film on a Si substrate, (b) the buckling of the silicide film and its separation from the substrate, (c) Si atom diffusion along Si(001) free surface and within the ErSi_{2-x} film, (d) a partially filled pyramidal defect as in Figure 4.5(b), (e) a completely filled defect as in Figure 4.5(a), and (f) the formation of a crack in the ErSi_{2-x} film in the pyramidal defect upon cooling.

The proposed pyramidal defect formation mechanism is illustrated in Figure 4.6. The film buckles away from the substrate to relieve the very large epitaxial strain energy as shown in Figure 4.6(b). We note that the pyramidal defect density is too low ($\sim 10^5 \text{ cm}^{-2}$) to significantly relieve the total strain energy stored in the film. Such buckling or

blistering must originate at a pre-existing defect or region where the bonding between substrate and film is weak. These may either be processing defects or form as the result of plastic deformation. While it is possible for a compressively stressed film to buckle while remaining attached to the substrate, the observations of voids beneath the pyramidal defect (Figure 4.5(b)) and the highly defected Si where the void was filled (see the insets to Figure 4.5(b)), both suggest that the film separates from the substrate upon buckling. Further, if the film is still attached to the substrate upon buckling, the strain energy stored in the ErSi_{2-x} film would be higher, resulting in a greater density of pyramidal defects than what is actually observed.

After the pyramidal defect forms by buckling as shown in Figure 4.6(b), the open region between the film and substrate begins to fill with Si as shown in Figures 4.6(c) – (e). This filling occurs in order to lessen the surface energies; filling the void below the buckled ErSi_{2-x} film covers part of both the Si free surface and the ErSi_{2-x} free surface. One indication that Si filling occurs is the observation that the Si in the void under the buckled ErSi_{2-x} film has a very different crystal structure compared to the original Si substrate. That is, the Si contains a high density of $\{111\}$ stacking faults (see Figure 4.5(b)). The Si atoms located at the ErSi_{2-x} /Si interface close to the defect diffuse along or near the interface towards the defect.

The stoichiometry of ErSi_{2-x} obtained from Rutherford backscattering spectrometry (RBS) indicates that 1 in 6 Si sites is vacant [31], hence the notation ErSi_{2-x} with $x = 1/3$. Therefore, we expect that the Si diffusivity through the ErSi_{2-x} , perpendicular to the c-axis is very high. It is worth noting that ErSi_{2-x} consists of layers of Si and Er perpendicular to the c-axis [143]. When the Si atoms reach the edge of the defect, they

can diffuse either on the Si(001) surface or on the free ErSi_{2-x} surface (see Figure 4.6(c)). As shown in Figure 4.6(c), silicon may grow simultaneously from the two surfaces. In the case of Si growing on the Si(001) surface, only one crystal orientation is possible. In contrast, there is considerable evidence that Si formed on free ErSi_{2-x} surfaces may grow with different orientations [144]. Eventually, the two re-crystallization fronts meet as shown schematically in Figure 4.6(e), resulting in the filled pyramidal defect of Figure 4.5(a). Figure 4.5(b) shows the case where a void remains (i.e., where the two fronts have not yet met) as in Figure 4.6(d).

Figure 4.7. Average size of the defects formed at 600°C as a function of annealing time. Time = 0 corresponds to the beginning of RTA and the first data point is at one second.

Examination of a large number of the pyramidal defects in SEM shows that many of the defects are cracked (these can also be seen in the optical image in Figure 4.4(a)). The cracking, represented in Figure 4.6(f), is likely a result of large tensile stresses formed near the four edges of the pyramid that meet at the apex and the contraction of the ErSi_{2-x}

film upon cooling. The coefficient of thermal expansion of RE silicides (like most metal silicides [158]) is larger than that of silicon, hence large differential strains occur on cooling from the annealing temperature to the room temperature.

The mechanistic model described above suggests that a balance between the elastic energy stored in the unbuckled film and the surface and interface energies determines the size of the pyramidal defects. Therefore, once the ErSi_{2-x} film forms and buckles upon RTA, the size of the pyramidal defects should not increase on further annealing. As a check on the validity of the mechanistic model, we measured the pyramidal defect size in several films, formed by annealing for different times. The results are shown in Figure 4.7. Except for very short times corresponding to incomplete silicide formation, the pyramidal defect size is independent of the annealing time. This is in agreement with the predictions of the mechanistic model.

4.3 Effect of Substrate Amorphization

It is known that amorphization of substrates will enhance the metal-silicon interaction and reduce the roughness of silicide films [1]. PAI method is a method that is commonly used in semiconductor industry to enhance the completion of the silicide processes [135]. In the PAI process, amorphization of the semiconductor substrate is achieved by implantation of Si, Ge or As into the substrate prior to metal deposition. Ar plasma cleaning is a dry cleaning method that physically sputters surface impurities away from semiconductor wafer. However, it also induces Si surface amorphization and roughness [145]. The implant energy is less than that of PAI and is kept as low as possible to avoid damaging the underlying junctions and gate oxides. In this section, substrate

amorphization was applied before Er deposition in an effort to improve the morphology and eliminate pyramidal defects and the resulting ErSi_{2-x} films and Schottky diodes were analyzed. The experimental details are described in Section 3.4.2.

4.3.1 Effect of amorphization on ErSi_{2-x} film structure

Figure 4.8 shows the single-crystal θ - 2θ XRD diffraction results for ErSi_{2-x} films formed on various Si(100) substrate. The presence of hexagonal ErSi_{2-x} of the AlB_2 type is observed on the non-amorphized Si substrate and Ar plasma cleaned Si substrate. Both the non-amorphized and Ar plasma cleaned samples exhibit XRD patterns containing ErSi_{2-x} $\{1\bar{1}00\}$ and $\{2\bar{2}00\}$ peaks.

The observation of the strong $\{1\bar{1}00\}$ and $\{2\bar{2}00\}$ peaks using the single-crystal θ - 2θ scan indicates that the ErSi_{2-x} formed in these two samples are highly textured or epitaxial with an orientation relation $\text{ErSi}_{2-x}(100)//\text{Si}(100)$. However the lower intensities of the $\{1\bar{1}00\}$ and $\{2\bar{2}00\}$ peaks in the Ar plasma cleaned samples, as compared to the non-amorphized samples, suggests less epitaxy with Si(100). On the other hand, it is surprising to see that no ErSi_{2-x} peaks in the PAI samples were detected. This could be due to the presence of a relatively thick Er_2O_3 and Er-Si-O in the PAI samples as compared to that of the non-amorphized and Ar plasma cleaned samples. Alternatively, the absence of ErSi_{2-x} peaks in the PAI sample could be a result of the formation polycrystalline ErSi_{2-x} , rather than textured or epitaxial ErSi_{2-x} . Note that as mentioned in Section 4.2, in both Ar plasma cleaned and PAI samples, no pyramidal structural defects were observed.

Figure 4.8. XRD single-crystal θ -2 θ scan of an $ErSi_{2-x}$ film formed on a Si(100) substrate annealed at 600°C for 60s in N_2 ambient. (a) Non-amorphized, (b) Ar plasma cleaned, and (c) PAI samples.

In order to clarify if poly-crystalline $ErSi_{2-x}$ was formed in the PAI samples and to further investigate the $ErSi_{2-x}$ crystallinity, further analysis was carried out using the 2D GADDs XRD. Figure 4.9(a) shows the 2D GADDs XRD of the Ar plasma cleaned sample. The plot shows lower intensity and greater spread in the χ direction for all peaks when compared to the non-amorphized sample (See Figure 4.1). $ErSi_{2-x} \{1\bar{1}00\}$ is the dominant peak although with greater χ spread than that of the non-amorphized sample. $ErSi_{2-x} \{1\bar{1}01\}$ peak is almost continuous across the χ range. In the range studied, the $ErSi_{2-x}$ film is less textured as compared to the film in the non-amorphized sample. Figure 4.9(b) shows the 2D GADDs XRD of the PAI sample which shows the absence of $ErSi_{2-x} \{1\bar{1}00\}$ peaks. However, a continuous $ErSi_{2-x} \{1\bar{1}01\}$ peak is observed across the χ

range, which confirms the formation ErSi_{2-x} in the PAI samples. The uniform distribution of $\text{ErSi}_{2-x} \{1\bar{1}01\}$ peak intensity across the χ range indicates that the ErSi_{2-x} film formed is poly-crystalline in nature.

Figure 4.9. GADDS θ - 2θ single crystal XRD scans of an ErSi_{2-x} film formed on a Si(100) substrate annealed at 500°C for 60s in a N_2 ambient of (a) Ar plasma cleaned sample, and (b) PAI sample. The x-axes are 2θ and the y-axes are χ . The Counts vs. 2θ plot is an integration of χ along the entire range of 2θ . The insets are the pole figures along the $\text{ErSi}_{2-x} \{1\bar{1}00\}$ direction.

A comparison of the of the strain on the ErSi_{2-x} film extracted from the average experimental 2D GADDS XRD $\text{ErSi}_{2-x} \{1\bar{1}00\}$ peak value shows that the strain of the Ar plasma cleaned sample is 0.12% compressive compared to 0.48% compressive in the non-amorphized sample. The strain is calculated by taking the d-spacing of the ErSi_{2-x} JCPDS file, d_{ref} as a reference [130], and using the formula $\epsilon = (d_a - d_{\text{ref}})/d_{\text{ref}}$ where ϵ is the

strain, and d_a is the d-spacing of the Ar plasma cleaned or non-amorphized sample. Note that the d-spacing is calculated by using Equation 3.1.

It has been shown in the previous section that one of the conditions for pyramidal structural defect formation is the presence of a compressive stress which leads to film buckling. Hence, the absence of the pyramidal structural defects in the Ar plasma cleaned sample is a result of the less textured ErSi_{2-x} film being under less compressive stress. Although, the PAI samples show the absence of the ErSi_{2-x} $\{1\bar{1}00\}$ peak, the reasons for the absence of the pyramidal structural defects are the same, i.e., the polycrystalline ErSi_{2-x} film is under less compressive stress.

The inserts of Figure 4.9 show the pole figure plots along the ErSi_{2-x} $\{1\bar{1}00\}$ direction. The Ar plasma cleaned sample shows more peaks with greater spread in the rotational as well as χ axis. This indicates that the ErSi_{2-x} film exhibits weak 4-fold symmetry (with two distinct ErSi_{2-x} epitaxial orientations) relative to the Si substrate, and is less textured as compared to the non-amorphized sample. The PAI sample shows no detected peaks at the same power settings confirming that it is polycrystalline.

Figure 4.10 shows the XTEM of the respective $\text{ErSi}_{2-x}/\text{Si}$ interfaces parallel to the $\text{Si}[011]$ axis. Figure 4.10(a) shows that the $\text{ErSi}_{2-x}/\text{Si}$ interface is smooth as expected due to the epitaxy of ErSi_{2-x} to the underlying $\text{Si}(001)$ substrate. An almost 1:1 relationship is observed for the ErSi_{2-x} $(1\bar{1}00)$ and $\text{Si}(111)$ lattice planes across the interface. The selective area electron diffraction (SAED) pattern confirms that the film is epitaxially oriented along the $\langle 110 \rangle$ axis with $\text{ErSi}_{2-x}(1\bar{1}00)[0001]//\text{Si}(001)[110]$ orientation

relationship. Figure 4.10(b) shows that the Ar plasma cleaned samples is slightly less smooth compared to the non-amorphized samples.

Figure 4.10. Bright field XTEM of $\text{ErSi}_{2-x}/\text{Si}(100)$ interface and SAED micrograph of ErSi_{2-x} films formed on a $\text{Si}(100)$ substrate annealed at 500°C for 60s in an N_2 ambient. (a) Non-amorphized sample, (b) Ar plasma cleaned sample, and (c) PAI sample. The various crystal planes and directions have been marked.

The SAED pattern which shows both slight ErSi_{2-x} film epitaxy along the $\langle 110 \rangle$ axis as well as slight concentric circles indicating that the ErSi_{2-x} film exhibits epitaxy to the Si substrate but is less textured compared to the non-amorphized sample. This is because the low power Ar plasma is only sufficient to create a very shallow amorphous layer of 1.4nm such that the ErSi_{2-x} grains are only slightly randomized.

The smoothest ErSi_{2-x} /Si interface is observed for the PAI sample in Figure 4.10(c). In the case of PAI sample, the ErSi_{2-x} thin film changes from nucleation controlled to diffusion controlled due to a larger heat of crystallization of amorphous silicon [39] which results in a smoother ErSi_{2-x} film. This would also lead to removal or weakening of the ErSi_{2-x} to Si(001) epitaxy. The SAED pattern of Figure 4.10(c) shows that the ErSi_{2-x} film is a random polycrystal in accordance to the XRD patterns in Figure 4.9(b).

4.3.2 Effect of amorphization on silicidation

The SIMS depth profile in Figure 4.11 shows that in all samples, a layer of ErSi_{2-x} was formed which corresponds to the relatively smooth portion of the Er and Si signals. The ErSi_{2-x} thickness decreases from 80nm to 55nm and to 45nm from the non-amorphized sample to the Ar plasma cleaned sample and then to the PAI sample, respectively. On the other hand, the amount of oxygen incorporated into the ErSi_{2-x} films increases from 24nm to 48nm and to 57nm, respectively.

The oxygen and gradually reducing Si signal towards the surface indicate that the surface consists of a double layer of $\text{Er}_2\text{O}_3/\text{Er-Si-O}$. The Er-Si-O was probably transformed from the original amorphous Er-Si intermixed layer, which typically forms as the first phase at the initial stage of Er-Si reaction [145]. RE metals are extremely

prone to oxidation and form RE_2O_3 readily even at room temperature, which inhibits the formation of the RESi_2 [45]. It must be noted that this is in contrast to RE silicides which are relatively stable up to high temperatures [44]. The Ar plasma cleaned and PAI samples are polycrystalline which results in higher number of diffusion paths along grain boundaries as compared to diffusion in single crystal. These polycrystalline grain boundaries are associated with a more open structure and the oxygen atoms (from residual oxygen in the annealing ambient, i.e., N_2 in this case) migrating along these grain boundaries is higher than that for diffusion in the crystal lattice.

Figure 4.11. SIMS depth profile of ErSi_{2-x} films formed on a $\text{Si}(100)$ substrate annealed at 600°C for 60s in an N_2 ambient. (a) Non-amorphized, (b) Ar plasma cleaned sample, and (c) PAI samples.

To investigate the uniformity of the ErSi_{2-x} layers, we calculated the ratio of Si to Er in Figure 4.11(a) and found that the Si count is constant from the $\text{ErSi}_{2-x}/\text{Si}$ interface toward the surface until $\sim 40\text{nm}$ from the surface whereby the Si counts decreases by $\sim 1.5\%/ \text{nm}$. This decrease occurs until $\sim 22\text{nm}$ from the surface whereby the presence of the oxygen signal interferes with the calculation. The decreasing Si count from $\sim 40\text{nm}$ onwards toward the surface can be understood on the basis that Si is the diffusing species in the Er to Si solid state reaction [139]. For a RTA time of 60s, the ErSi_{2-x} film is unable to achieve its preferred stoichiometry of ErSi_{2-x} ($x = 1/3$), hence the Si deficiency nearer to the surface. Similar Si deficiencies towards the ErSi_{2-x} surface were also observed in the Ar plasma cleaned and PAI Si samples.

The problem of oxygen penetration can be addressed by the application of Ti based capping layers. The Ti based layers were found to be able to effectively suppress the oxygen penetration into the amorphized layers and resulted in pure ErSi_{2-x} films with similar thicknesses as that of the non-amorphized samples. XRD scans showed that the film structures of the non-amorphized and amorphized samples are the same as those without the Ti based capping layer, indicating that the substrate amorphization is the controlling factor in determining the crystallinity of the ErSi_{2-x} film rather than the presence of oxygen. The effects of Ti based capping layers on Er-silicidation will be discussed in detail in Section 4.4.

4.3.3 Effect of amorphization on room temperature electrical characteristics

Figure 4.12 shows the I - V characteristics of ErSi_{2-x} Schottky diodes formed by using the techniques described in Section 3.4.2. An *in-situ* TiN capping was applied to all

samples as a protective capping layer. It can be seen that the plots are linear under forward bias (from ~ 0.05 V – 0.2V) for the non-amorphized diode and Ar plasma cleaned diodes [146]. The PAI diodes showed a ‘hump’ under forward bias. Under reverse bias, there is a considerable scatter for the non-amorphized Si diodes while a tightly distributed reverse current is observed for the Ar plasma cleaned Si and PAI Si diodes.

Figure 4.12. I - V characteristics of $\text{ErSi}_{2-x}/p\text{-Si}$ Schottky diodes measured at room temperature. (a) Non-amorphized Si diode, (b) Ar plasma cleaned diode, and (c) PAI diode. Φ_{Bpeff} and n are extracted using the TE model. The Richardson's constant used is $32 \text{ A/cm}^2\text{K}^2$ [148]. There are fifteen samples in each plot. Note that the sample size is 15 per sample type.

From the Thermionic Emission (TE) theory, the diode current flowing in the linear forward biased region is typically given by [51, 147]

$$I = AA^*T^2 \exp\left(-\frac{q\phi_{beff}}{kT}\right) \left(\exp\left(-\frac{qV}{nkT}\right) - 1\right) = I_s \left(\exp\left(-\frac{qV}{nkT}\right) - 1\right) \quad (\text{Equation 4.1})$$

where ϕ_{beff} is the effective Schottky barrier height, k is the Boltzmann constant, T is the temperature, q is the electronic charge, A is the diode area, and A^* is the Richardson constant. The ϕ_{beff} is empirically determined and takes into account non-idealities (e.g. various leakage currents). Hence, its value is slightly lower than the actual ϕ_b .

The observed ideality factors of $n = 1.31$ and $n = 1.8$ are much larger than unity, which suggest that there exists a considerable recombination current component in both the non-amorphized and PAI diodes. The recombination currents are probably due to the presence of electrically active defects caused by the pyramidal structural defects and ion induced damage for the non-amorphized and PAI diodes respectively. In addition, some non-amorphized diodes (see Figure 4.13) exhibit n values close to 2. The near ideal n of ~ 1.05 for the Ar plasma cleaned diodes suggest the absence of defects at the MS interface.

Table 4.1. ϕ_{beff} and n of various ErSi_{2-x} Schottky diodes.

No.	Amorphization	Capping	Ave. ϕ_{beff} (eV)	Ave. n
1	non-amorphized	TiN	0.72 ± 0.06	1.31 ± 0.25
2	Ar plasma cleaned	TiN	0.73 ± 0.02	1.05 ± 0.03
3	PAI	TiN	0.73 ± 0.01	1.8 ± 0.02
4	non-amorphized	TiN/Ti	0.76 ± 0.04	1.1 ± 0.03

The ϕ_{beff} to holes (ϕ_{bpeff}) and n were then extracted using Equation 4.1 for typical non-amorphized, Ar plasma cleaned, and PAI Si diodes. The results are $\phi_{bpeff} = 0.72 \pm 0.06\text{eV}$ and $n = 1.31 \pm 0.25$ for the non-amorphized Si diodes, $\phi_{bpeff} = 0.73 \pm 0.02\text{eV}$ and

$n = 1.05 \pm 0.03$ for the Ar plasma cleaned diodes, and $\Phi_{bpeff} = 0.73 \pm 0.01\text{eV}$ and $n = 1.8 \pm 0.02$ for the PAI diodes. Table 4.1 summarizes the effect of process variations, including the effect of the substrate amorphization on the Φ_{bpeff} and n of the ErSi_{2-x} Schottky diodes.

The Φ_{bpeff} measured separately using C-V method are 0.79eV and 0.77eV for the Ar plasma cleaned and non-amorphized diodes, respectively. These Φ_{bpeff} values are higher than those extracted from the I - V measurements and are believed to be due to (1) the local variation of Schottky barrier at the silicide/silicon interface and/or (2) the presence of a non-negligible recombination current and/or other parasitic leakage components, which contribute to an increase in the apparent I_s value and consequently result in a lower Φ_{bpeff} when Equation 4.1 is used for the calculation of Φ_{bpeff} . The C-V Φ_{bpeff} for the PAI diodes are unusually high and are believed to be due to ionized electronic trap states leading to a measured Φ_{bpeff} larger than the actual value [148].

Figure 4.13 shows the Φ_{bpeff} and n extracted using Equation 4.1 for the $\text{ErSi}_{2-x}/p\text{-Si}$ diodes. A structurally non-uniform MS interface due to non-perfect epitaxy or polycrystallinity results in an inhomogeneous MS interface with varying Φ_{bpeff} across adjacent grains [148]. This causes the Φ_{bpeff} and n to vary from diode to diode and their values (measured by the TE method) represent a direct measure of the interface uniformity i.e., the larger the density of grains/patches, the larger n value. Thus, there is an approximately linear relationship between Φ_{bpeff} and n as a function of inhomogeneity with an extrapolation of n to 1 giving the value of the homogeneous Φ_{bpeff} [150].

As can be seen from Figure 4.13, the extrapolation to $n = 1$ of the Ar plasma cleaned diodes gives a homogeneous $\Phi_{bpeff} \sim 0.82\text{eV}$. By assuming the bandgap $E_g =$

$q(\Phi_{bpeff} + \Phi_{bneff})$, $\Phi_{bneff} = 0.3\text{eV}$ which is close to the lowest reported values $\Phi_{bneff} \sim 0.28\text{eV}$ for $\text{ErSi}_{2-x}/n\text{-Si}$ diodes [151]. Note that Φ_{bneff} is the Φ_{beff} to electrons. The extracted Φ_{bpeff} are $\sim 0.76\text{eV}$ and $\sim 0.77\text{eV}$ for the non-amorphized Si and PAI diodes respectively, which are much lower than what one would expect for a homogenous Φ_{bpeff} . This supports the previous argument that there are dominant recombination current components in the non-amorphized and PAI diodes.

Figure 4.13. Φ_{bpeff} plotted against n both extracted using TE model plotted against temperature for a typical non-amorphized Si, Ar plasma cleaned, and PAI $\text{ErSi}_{2-x}/p\text{-Si}$ diode. The Richardson's constant used is $32 \text{ A/cm}^2\text{K}^2$ [149].

4.3.4 Effect of substrate amorphization on the temperature dependent electrical characteristics : Modelling of electrical transport and defect characterization

Figure 4.14 shows the temperature-dependence of Φ_{bpeff} and n values extracted using the TE model for typical non-amorphized, Ar plasma cleaned, and PAI $\text{ErSi}_{2-x}/p\text{-Si}$ Schottky diodes. The Ar plasma cleaned diode shows a very weak dependence on the

temperature whereas the non-amorphized and PAI diode exhibits a strong temperature dependence. This dependence of the Φ_{bpeff} and n values on the temperature can be understood on the basis that there exists a dominant recombination current component for the non-amorphized and PAI diodes due to the high concentration of electrically active defects in the depletion regions of the structural defects and the ion damaged region respectively.

The forward current in this case can be expressed by [151]

$$I = I_{TE} + I_{rec} \approx AA * T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \left(\exp\left(-\frac{qV}{nkT}\right) - 1\right) + B \exp\left(-\frac{q\phi_r}{kT}\right) \left(\exp\left(-\frac{qV}{2kT}\right) - 1\right) \text{ (Equation 4.2)}$$

where B is a pre-exponential factor independent of T , Φ_b is the Schottky barrier height measured in the absence of the dominant recombination centers, $q\phi_r = E_c - E_t$ (or $E_t - E_v$, depending on whichever is larger than $(E_c - E_v)/2$) with E_c and E_v as the conduction and valence band edges of Si and E_t as the energy position of the electrically active defects within the Si bandgap.

In the presence of a dominant recombination current at room temperature i.e.,

$$\frac{I_{rec}}{I_{TE}} = \left(\frac{B}{AA * T^2}\right) \exp\left(\frac{q(\phi_b - \phi_r)}{kT}\right) \left(\frac{n}{2}\right) > 1 \text{ for small forward bias, it is obvious that}$$

Equation 4.1 would yield a Φ_{bpeff} value much smaller than ϕ_B and a n value much larger

$$\text{than unity. With increasing temperature, however, } \frac{I_{TE}}{I_{rec}} = \left(\frac{AA * T^2}{B}\right) \exp\left(\frac{-q(\phi_b - \phi_r)}{kT}\right) \left(\frac{2}{n}\right)$$

rapidly increases when $\phi_B - \phi_r > 0$ (note: a deep trap level is most effective as a recombination center when its E_t is located close to middle of Si bandgap, which means

that ϕ_r is most likely smaller than $\Phi_{bpeff} = 0.73\text{eV}$). This results in $I_{TE} > I_{rec}$ and a Φ_{bpeff} value close to ϕ_B . The increasing $\frac{I_{TE}}{I_{rec}}$ with increasing temperature would also yield an n value close to unity. To summarize, Equation 4.1 would yield a smaller Φ_{bpeff} value and n value much larger than unity when I_{rec} is dominant at low temperatures and a larger Φ_{bpeff} with n close to unity when I_{TE} is dominant at high temperatures.

Figure 4.14. Φ_{bpeff} and n extracted using the TE model plotted against temperature for a typical non-amorphized, Ar plasma cleaned, and PAI $\text{ErSi}_{2-x}/p\text{-Si}$ Schottky diode. The Richardson's constant used is $32 \text{ A/cm}^2\text{K}^2$ [149].

Knowing that any variation in Φ_{bpeff} and n with temperature does not fit within the framework of the TE model, Tung's model of inhomogenous MS contacts was adopted to further analyze the Schottky diode performance. The model assumes low barrier patches with size less than the depletion width embedded in a uniformly high barrier background,

leading to saddle point barriers in front of the patches which may limit the current flowing through it. The total current flowing in the linear forward biased region is [150]

$$I = AA * T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \left(\exp\left(-\frac{qV}{kT}\right) - 1 \right) \times \left(1 + \frac{8\pi p_p \sigma^2 \eta^{1/3}}{9(V_{bo} - V)^{1/3}} \exp\left(\frac{q^2 \sigma^2 (V_{bo} - V)^{2/3}}{2(kT)^2 \eta^{2/3}}\right) \right) \quad (\text{Equation 4.3})$$

where p_p is the low barrier patch density, σ is the patch standard deviation, $\eta = \epsilon_b \epsilon_o / q N_d$ where $\epsilon_b \epsilon_o$ is the bulk dielectric constant and N_d is the dopant density of the semiconductor. V_{bo} is the band-bending of the uniform barrier outside the patches, and Φ_b is the Schottky barrier height.

Figure 4.15. I - V characteristics in the linear region of Ar plasma cleaned diodes at various temperatures. Solid lines were calculated using Equation 4.3 with the following fitting parameters: $p_p = 2.55 \times 10^{11} \text{ cm}^{-2}$, $\sigma = 6 \times 10^{-5} \text{ cm}^{2/3} \text{ V}^{1/3}$, and $\Phi_b = 0.76 \text{ eV}$. The fitting parameters are obtained by least squares fitting of the I - V curve at 273K. Subsequent fitting was done by changing the values of T from 273K to 352K. V_{bo} and N_d are obtained from C - V measurement. The scatter plot represents the experimental data.

Least squares curve fitting method was carried out for the linear forward biased region of the Ar plasma cleaned diode using Equation 4.3. The results show a close fit between the experimental and simulated I - V curves as seen in Figure 4.15. On the other hand, Equation 4.3 does not correlate well with the data from the non-amorphized and PAI diode. This is in agreement with our argument that there exists a high concentration of electrically active defects within the microstructural defect regions and within the ion induced damage PAI region.

Hence, the non-amorphized and PAI diode should be modeled using Equation 4.2 which consists of a TE component and a recombination current component. In order to isolate the recombination current component, a linear subtraction was carried out on the TE current from the measured current i.e., $I_{rec} = I - I_{TE}$. Figure 4.16(a) shows the I_{rec} - V plot against the measurement temperature of the non-amorphized diode which indicates a clear temperature dependence as expected from Equation 4.2. A similar I_{rec} - V curve was also exhibited by the PAI diode.

Figure 4.16. (a) I_{rec} - V curves of the non-amorphized diode against temperature. Arrhenius plots of the temperature dependent I_{rec} - V curves for (b) non-amorphized diode, and (c) PAI diode.

From the I_{rec} - V for the various temperatures, we are able to plot the Arrhenius curves. Subsequently, from the slopes of the Arrhenius plots (shown in Figures 4.16(b), and (c) for the Ar plasma cleaned and PAI diodes respectively) i.e., the plot of $\ln(I_{rec, V=0})$ against $1/T$, the activation energy which is equivalent to ϕ_r as defined in Equation 4.2, was calculated. For the non-amorphized Si and PAI diodes, ϕ_r extracted is $\sim 0.68\text{eV}$ and $\sim 0.51\text{eV}$. In other words, deep level trap sites 0.68eV and 0.51eV from the valence band exists in forbidden bandgap region which contribute to the recombination current in the diodes under forward bias. It must be mentioned that Frenkel-Poole emission from deep trap levels in the depletion region of ErSi_{2-x} Schottky diodes has been proposed as a possible source of the leakage current [58].

4.4 Effect of *in-situ* Ti-based Capping

As shown in the previous section, the application of various substrate amorphization techniques can essentially eliminate pyramidal structural defects. However, the degree of amorphization is directly related to ion damage and should be carefully controlled in order to improve the MS interface. In this section, we will investigate *in-situ* Ti-based capping layers as a method of pyramidal structural defect reduction (as opposed to defect elimination in the substrate amorphization methods). The effect of capping on the structural and electrical properties on the ErSi_{2-x} thin film were investigated.

5.4.1 Relation of defect density to electrical characteristics

Figure 4.17(a) (similar to Figure 4.2(a)) shows a typical plane view optical image of an uncapped ErSi_{2-x} sample annealed at 500°C which is uniformly covered with pyramidal structural defects. As described in Section 4.2.2, these structural defects originate from the biaxial compressive stress on the ErSi_{2-x} thin film exerted by the Si substrate during RTA followed by a fast Si diffusion [139, 143].

Figure 4.17. (a) Plane view optical image of a control sample showing structural defects, (b) defect coverage against annealing temperature for various ErSi_2 samples, (c) I - V characteristics of an ErSi_{2-x}/p -Si diode showing increased 'leakage' current with increasing structural defect coverage and, (d) structural defect coverage against diode ideality factor.

Figure 4.17(b) shows the percentage of structural defect coverage for the capped samples and the control as a function of RTA temperature. At the RTA temperature of 500°C, the capped samples (~0.8% defect coverage) show a structural defect coverage reduction of up to five times against the uncapped samples (~4% defect coverage). This translates into a structural defect density of $\sim 9 \times 10^4 \text{ cm}^{-2}$ against $\sim 7 \times 10^5 \text{ cm}^{-2}$ for the capped and uncapped samples, respectively. It can also be observed that there is an increase in the defect coverage with annealing temperature, which is believed to be due to (1) greater thermal stress leading to greater compressive stress on the ErSi_{2-x} thin film and/or, (2) increased thermal diffusion of Si, both of which are essential in structural defect formation [139, 143].

In addition, it can be seen from Figure 4.17(b) that there is a 2x defect density reduction in the TiN/Ti capped samples as compared to the TiN capped samples. Ti has a smaller thermal expansion coefficient as compared to TiN ($8.6 \times 10^{-6} \text{ K}^{-1}$ vs. $9.4 \times 10^{-6} \text{ K}^{-1}$). It is possible that during RTA temperature ramp up, a larger tensile stress is exerted by the TiN/Ti cap (which opposes the compressive stress exerted by Si substrate) on the underlying ErSi_{2-x} thin film due to a larger thermal expansion difference between TiN/Ti and ErSi_{2-x} as compared to TiN and ErSi_{2-x} .

Figure 4.17(c) shows the room temperature I - V curves of the ErSi_{2-x} Schottky diodes which was modeled using Equation 4.1. With an increase in the defect coverage present in the diodes, there is a corresponding increase in the recombination current component which leads to a reduced $\Phi_{b\text{eff}}$ and an increased n when the Equation 4.1 is used. This is graphically represented in Figure 4.17(d) which also shows that a 2% to 1% defect structural density reduction has a significant impact on n .

For the TiN/Ti capped samples, the defect coverage ranges from 0.5 – 0.9% with around 75% of the diodes having good I - V characteristics ($n \approx 1.1$). Among the diodes with good I - V characteristics, the TiN/Ti capped diodes have $\Phi_{bpeff} = 0.76 \pm 0.04\text{eV}$ and $n = 1.1 \pm 0.03$ obtained experimentally which is better than the previously discussed non-amorphized, Ar plasma cleaned and PAI diodes with TiN cap as can be seen in Table 4.1 (see Section 4.3.3). Therefore, the TiN/Ti capping layers will be applied to the SiNW devices in Chapter 5 and 6 as the TiN/Ti capped Schottky diodes have the highest Φ_{bpeff} .

5.4.2 Effect of capping on silicidation

Figure 4.18. R_{sh} against annealing temperature of ErSi_{2-x} thin film samples. TiN and TiN/Ti capping layers were not removed during the 4-point measurement.

Figure 4.18 shows the change in the R_{sh} against annealing temperature of the samples. Generally, the sheet resistance is lower with increasing annealing temperature as thicker ErSi_{2-x} layers are formed. In the uncapped samples, very high sheet resistance values

were measured at RTA temperatures $< 500^{\circ}\text{C}$ due to a surface oxidation of the extremely reactive Er. ErSi_{2-x} is formed at a lower RTA temperatures $< 500^{\circ}\text{C}$ in the samples with capping as evidenced from the relatively low sheet resistance values. At RTA temperatures $> 600^{\circ}\text{C}$ (not shown), the sheet resistance of the TiN capped sample increased exponentially showing that TiN is inefficient as an effective diffusion barrier at those temperatures. Note that it has been shown that reactively sputtered TiN oxidizes at temperatures $\approx 600^{\circ}\text{C}$ to form a layer that is predominantly TiO_2 [154]. On the other hand, inter-diffusion of Ti with TiN at elevated temperatures causes grain coarsening [155], which reduces the path for oxygen diffusion from the RTA ambient. This resulted in the TiN/Ti capped samples showing lowest sheet resistances at all RTA temperatures.

Figure 4.19. SIMS depth profile of ErSi_{2-x} thin film samples annealed at 500°C for 60sec in a N_2 ambient.

Figure 4.19 shows the SIMS elemental depth profile of the samples annealed at a temperature of 500°C. The capped samples have a thicker ErSi_{2-x} formation, in agreement with the R_{sh} data in Figure 4.18, with a thickest ErSi_{2-x} layer formed in the TiN/Ti capped samples. Although, the total deposited thickness of the TiN cap and the TiN/Ti capped layers are the same (~30nm), the TiN/Ti cap samples showed the least oxygen penetration. This illustrates the extra effect of Ti which serves as sacrificial layer by converting any oxygen already present in the capping layers and the annealing ambient into TiO_2/TiO [156] in addition to the diffusion barrier provided by the TiN.

Figure 4.20. XTEM micrographs of ErSi_{2-x} thin film samples annealed at 500°C for 60sec in a N_2 ambient with (a) 20nm TiN/10nm Ti cap, and (b) 30nm TiN cap.

Figure 4.20 shows the XTEM micrographs of ErSi_{2-x} thin films with TiN and TiN/Ti capping. There is no diffusion of Ti into the ErSi_{2-x} film to form a ternary compound as determined by using energy dispersive X-ray spectroscopy. This is in agreement with the SIMS results in Figure 4.19. The larger percentage of Ti in the capping layer for the

TiN/Ti cap in Figure 4.20(a) suggests that there is indeed intermixing of the Ti with TiN in agreement with the R_{sh} results in Figure 4.18. The decreasing Si percentage from the $\text{ErSi}_{2-x}/\text{Si}$ interface toward the surface is a result of Si being the diffusing species in the Er to Si solid state reaction (note that $x = 1/3$) [139]. This results in Si deficiency nearer to the surface of the ErSi_{2-x} film for short RTA times.

It must be mentioned that the application of the Ti capping on Ni films has been shown to promote silicidation by Ti diffusion through Ni films for the removal of native SiO_2 on the Si substrate [155]. Assuming that Ti diffuses through the Er layers to reduce the native SiO_2 on the Si substrate, it is possible that the defect density could be reduced. This is because native SiO_2 on the Si substrate serve as weak points where ErSi_{2-x} film buckling originates. However, the absence of Ti in the ErSi_{2-x} film makes it unlikely that Ti diffusion through Er/ ErSi_{2-x} occurs. Therefore the reduction in defect density is most likely a result of reduction of compressive stress on the ErSi_{2-x} films as will be described in Section 4.4.3. Note that the absence of ternary ErTiSi compounds could be beneficial in the silicide process as Ti, TiN and unreacted Er can be etched off with SPM in a single step.

5.4.3 Role of capping on defect reduction

Figure 4.21 shows the single crystal θ - 2θ XRD plots of the in-plane and out-of-plane ErSi_{2-x} thin film. The in-plane $\{1\bar{1}00\}$ and $\{2\bar{2}00\}$, and out-of-plane $\{1\bar{1}01\}$ peaks indicate the formation of AlB_2 hexagonal ErSi_{2-x} . The ErSi_{2-x} thin films with capping layers showed a right shift of the in-plane XRD peaks and a left shift of the out-of-plane XRD peaks. This corresponds to a decrease in the d-spacing of the in-plane lattice planes

and an increase in the d-spacing of the out-of-plane lattice planes. Taking the d-spacing of the uncapped sample, d_0 as a reference, the strain, ϵ acting in the ErSi_{2-x} thin film with a capping layer can be calculated from the change in the d-spacing, i.e., $\epsilon = (d_{\text{capping}} - d_0)/d_0$.

Figure 4.21. (a) single crystal θ - 2θ XRD scan of ErSi_{2-x} thin film samples in-plane peaks, $\text{ErSi}_{2-x}(11\bar{0}0)$ and $\text{ErSi}_{2-x}(2\bar{2}00)$, and (b) plot of 2θ against $11\bar{0}0$ and $2\bar{2}00$ plane. (c) 2D GADDS single crystal θ - 2θ XRD scan of ErSi_{2-x} thin film out-of-plane peak, $\text{ErSi}_{2-x}(11\bar{0}1)$, and (d) plot of 2θ against $11\bar{0}1$ plane. XRD scans were calibrated to Si substrate peak for reference.

The in-plane strains are of a negative value indicating a compressive strain normal to the film surface while the out-of-plane strains (39° to film surface) are positive indicating

a tensile strain. This indicates that the post annealed ErSi_{2-x} thin film with capping layers are under tensile stress compared to the uncapped samples. It is highly likely that this tensile stress experienced by the ErSi_{2-x} film is due to the capping layer. During RTA, the tensile stress partially relieves the biaxial compressive stress in the ErSi_{2-x} film (caused by the Si substrate), thereby reducing the density of structural defects. The measured strains of the TiN capped and the TiN/Ti capped samples are similar and do not reflect the observed reduction of defects with a TiN/Ti cap. This could be due to the resolution of the XRD measurement or the fact that the strain measured is the post annealed strain and might not accurately reflect the actual strain during RTA.

4.5 Summary

ErSi_{2-x} films formed by RTA of Er films on Si(001) have been characterized. The ErSi_{2-x} films exhibit a pyramidal structural defect that has not previously been reported. The defect forms in order to relax epitaxial misfit stresses through a separation of the film from the substrate and subsequent filling up of the void with Si. Ar plasma cleaning and pre-amorphization implants were then employed to amorphize Si(001) substrate prior to Er film deposition. Improved electrical performance was observed for the Ar plasma cleaned Si diodes due to the removal of structural defects. The PAI Si diodes show degraded performance due to ion induced damage even though structural defects were eliminated. *In-situ* capping layers of TiN and TiN/Ti on Er effectively prevents oxidation of highly reactive Er layers. The capping layers also serve to partially relieve the compressive stresses experienced by the ErSi_{2-x} films during RTA which reduces structural defect density.

CHAPTER 5

BACK-GATED ErSi_{2-x} SCHOTTKY SOURCE/DRAIN SILICON NANOWIRE MOSFET

5.1 Introduction

This chapter presents the electrical characteristics of N-MOSFETs using SiNW (~8nm width) as the channel and ErSi_{2-x} as the S/D in a SSDMOS architecture. A brief materials study of the thin film processed under similar conditions as the ErSi_{2-x} SSDNWMOS is presented. The ErSi_{2-x} SSDNWMOS electrical characteristics (I_d - V_g , I_d - V_d) are presented along with a discussion of the current transport mechanism across the Schottky junction along with two terminal S/D (back to back diode) electrical characteristics. The effects of physical transistor parameters, e.g., number of SiNW channels, silicided S/D depth and Schottky junction size, are discussed. Modulation of Φ_b as a function of gate and drain voltage is also presented.

5.2 Materials Study

This section characterizes the material properties of ErSi_{2-x} thin films done on blanket Si wafers processed under the same metal deposition and annealing condition as the SiNW devices (i.e., 20nm TiN / 10nm Ti / 50nm Er followed by RTA at 450°C for 60s). As shown in Chapter 4, a double layer TiN/Ti protective capping not only suppresses oxygen contamination during RTA, it also gives the lowest R_{sh} values and lowest pyramidal defect density which in turn leads to reduced ‘leakage’ currents.

Figure 5.1. R_{sh} of ErSi_{2-x} and ITRS requirements vs. MPU/ASIC $\frac{1}{2}$ pitch for various MPU/ASIC design architectures.

Figure 5.1 shows the measured R_{sh} values of a $\sim 85\text{nm}$ thick ErSi_{2-x} thin film processed with the above mentioned conditions plotted with the required R_{sh} as specified by the ITRS [15]. The R_{sh} requirements increase as a result of a decrease in silicide thickness as transistor scaling occurs. Briefly, as S/D silicide thickness reduces by $0.7\times$ per generation, R_{sh} correspondingly increases according to $R_s = \rho/\text{thickness}$. In other words, there is a $1.4\times$ R_{sh} increase per generation. As mentioned in Chapter 1, R_{sh} is a key component of the MOSFET series resistance and should be reduced so as to reduce the RC time delay, leading to increasing clock frequency, and hence enhancement of the speed of the electronic circuit [158].

Fully depleted SOI (FDSOI) and multi-gate devices are able to extend the R_{sh} roadmap due to the relaxed silicide thickness constraints as specified in the ITRS. However, as device scaling proceeds toward sub-22nm technological node, there is no

known solution to the rising R_{sh} values. With a SSDMOS architecture, due to the replacement of ultra-shallow doped SDE with thicker ErSi_{2-x} Schottky junction, the projected R_{sh} of the ErSi_{2-x} remains constant at the measured value of $\sim 11 \text{ } \Omega/\text{sq}$ beyond the 22nm technological node, considering a bulk Si substrate or a raised S/D architecture [159]. This is so because the ErSi_{2-x} film thickness can remain the same in a SSDMOS device architecture and is hence always maintained at $\sim 11 \text{ } \Omega/\text{sq}$. Even if partially depleted (PD) SOI is used, the ErSi_{2-x} R_{sh} is able to meet the sub-22nm requirements.

Note that only R_{sh} is compared in Figure 5.1. In SSDMOS, R_{sp} are eliminated so that the total parasitic series resistance is further reduced such that the series resistance requirements can be easily met with SSDMOS architecture.

Figure 5.2. I - V diode characteristics of a $\text{ErSi}_{2-x}/p\text{-Si}(100)$ diode fabricated using the proposed approach.

Figure 5.2 shows the I - V characteristics of a $\text{ErSi}_{2-x}/p\text{-Si}$ Schottky diode processed with the above mentioned conditions. It can be observed that the I - V characteristics are linear under forward bias showing the absence of parasitic recombination currents. This translates into low leakage currents in the ErSi_{2-x} SSDNWMOS under positive V_g . The reverse current of the Schottky diode gives an indication of the junction leakage current ('hole' current from the drain terminal) of the ErSi_{2-x} SSDNWMOS during 'off-state' or negative V_g bias. The measured Schottky diode reverse current is $8.95\text{fA}/\mu\text{m}^2$ and is comparable if not better than most reported values [61]. Using the thermionic emission equation (Equation 4.1), $I = AA^*T^2 \exp(-q\Phi_{bpeff}/kT)(\exp(-qV/nkT)-1)$ [51] where Φ_{bpeff} is the effective Schottky barrier height to holes, k is the Boltzmann constant, T is the temperature, q is the electronic charge, A is the diode area, A^* is the Richardson constant, and n is the ideality factor. The extracted Φ_{bpeff} is 0.8eV and the corresponding Schottky barrier height to electrons, Φ_{bneff} is 0.32eV . n is a fit to the I - V slope in the forward biased region and the a value of 1.07 is extracted indicating a near ideal $\text{ErSi}_{2-x}/\text{Si}$ contact.

5.3 Electrical Characteristics

This section characterizes the electrical characteristics of the ErSi_{2-x} SSDNWMOS whose fabrication steps have been described in Chapter 3. Unless specified otherwise, the characterized ErSi_{2-x} SSDNWMOSs have a single SiNW channel, fully silicided S/D and a non-overlapping (to curved extension) Si_3N_4 dummy gate (see Figure 3.9).

5.3.1 Transfer, I_d - V_g and output characteristics, I_d - V_d

Figure 5.3(a) shows a large current flow in the positive V_g direction and a slight current flow in the negative V_g direction but with a less steep slope, characteristics of a N-SSDMOS.

Figure 5.3. (a) I_d - V_g , g_m - V_g and (b) I_d - V_d characteristics of an ErSi_{2-x} SSDNWMOS with $L_{ch} = 500\text{nm}$.

With increasingly positive V_g , conduction occurs as electrons tunnel through the Schottky barrier at the source when the semiconducting SiNW channel potential is pushed down. With increasingly negative V_g , the conduction occurs as holes tunnel through the Schottky barrier at the drain end when the semiconductor energy band is

pushed up. This ambipolar conduction is a characteristic of SSDMOS. In this respect, the SSDMOS, although providing lower parasitic series resistance, is disadvantageous as compared to the doped S/D MOSFET which exhibits only majority carrier current flow from the doped S/D and hence, the absence of a reverse current seen in Figure 5.3(a) [51].

The device shows high drive current ($\sim 900 \mu\text{A}/\mu\text{m}$ at $V_d = 1.2\text{V}$, $V_g = V_t + 5\text{V}$, $V_t = 2.8\text{V}$) with an I_{on}/I_{off} ratio of $\sim 10^5$, where V_t is the threshold voltage. Note that the gate oxide capacitance using a 145nm thick gate dielectric (i.e. the BOX layer for the back-gated configuration) requires $V_g \sim 5\text{V}$ to induce the same charge as a 6nm thick gate dielectric biased at $V_g = 1.2\text{V}$ [160]. The DIBL is $\sim 500\text{mV/V}$ and the SS is $\sim 180\text{mV/dec}$. The large values are attributed to the thick gate oxide which reduces the gate electrode electrostatic control and is not evidence of SCE. However, considering the thick gate dielectric, the drain current is extremely responsive to V_g . This attributed to the compensating effect of the fully depleted nanometer sized channel and GAA architecture [117] which allows a small ΔV_g to achieve the required inversion charge, as well as improved carrier injection as silicon channel thickness is reduced [161].

The curve exhibits a 2-slope SS ($\sim 180\text{mV/dec}$ and $\sim 450\text{mV/dec}$) with increasingly positive V_g indicating a sequential thermionic emission followed by a tunneling dominated current [162]. A larger value of SS is expected for tunneling due to the less responsive barrier modulation through a thick gate oxide. Although the value of 180mV/dec is relatively high, it is still better/comparable than the reported SS for back gated SiNW transistors of 300mV/dec [22] and 174mV/dec [23] even though SS for the doped S/D MOSFET is generally lower due to the absence of Schottky barrier at the

source which allows for greater thermal emission. With increasingly negative V_g , there is only a single SS ($\sim 660\text{mV/dec}$) indicating tunneling is the main conduction mechanism. This is due to the large Φ_{bpeff} of ErSi_{2-x} to $p\text{-Si}$ $\sim 0.76 - 0.85\text{eV}$ [61]. Fig. 5.5(a) also shows the transconductance (g_m) against V_g of the same device. The g_m has a well defined peak, indicating the device is biased into saturation. In addition, the peak g_m $577\ \mu\text{S}/\mu\text{m}$ is comparable or better than the reported SSDMOS g_m values [61].

Fig. 5.5(b) shows the I_d - V_d characteristics of the same ErSi_{2-x} SSDNWMOS. The device does not exhibit an upwardly sloping (S-shaped) sub-linear slope except at $V_g \geq V_t + 1.8\text{V}$. This upwardly sloping sub-linear characteristic is typical of SSDMOS and is a signature of a non zero ϕ_{bn} at the drain which impedes current flow until the drain bias is sufficiently high [93]. The absence of the sub-linear slope of ErSi_{2-x} SSDNWMOS as compared to NiSi based SSDMOSs [68] is due in part to the lower ϕ_{bn} of $\text{ErSi}_{2-x}/n\text{-Si}$ $\sim 0.3\text{eV}$ as compared to ϕ_{bn} of $\text{NiSi}/n\text{-Si}$ $\sim 0.64\text{eV}$, as well as the improved carrier injection to the nanometer-sized SiNW channel. There is a presence of linear and saturation region for low V_g values. However, ‘pinch-off’ is not reached for larger V_g biases due in part to the higher V_{dsat} . (V_d not biased to a large enough value), and the possibility that there exist a large R_{co} in the back-gated configuration which is limiting I_d .

5.3.2 Current Transport Mechanism

The carrier transport mechanism across a SSDMOS can be approximated by a combination of thermionic and thermionic-field current (i.e. $I = I_{TE} + I_{TN}$) and can be expressed in the forms [51, 92]

$$I_{TE} = AA * T^2 \exp\left(-\frac{q(\phi_b + \psi_c)}{kT}\right) = I_s \exp\left(-\frac{q\psi_c}{kT}\right) \text{ (Equation 5.1)}$$

and

$$I_{TN} = \frac{Aq^2 E^2}{8\pi\hbar\phi} \exp\left[-\frac{8\pi}{3\hbar q E} \{2m^* (q\phi_b)^3\}^{1/2}\right] \text{ (Equation 5.2)}$$

where ϕ_b is the Schottky barrier height, ψ_c is the channel potential (conduction band across the channel modulated by V_g), E is the electric field across ϕ_b , h is the plancks constant, and m^* is the effective mass.

The relative contributions from I_{TE} and I_{TN} is dependent on the width of the Schottky barrier. To determine the dominant current contribution, an energy value E_{00} , defined as diffusion potential of an electron across a Schottky barrier, can be used [51].

Quantitatively, $E_{00} = q\hbar / 2\sqrt{N_{a,SiNW} / m^* \epsilon_s}$, where $\hbar$ is the reduced Plancks constant, and ϵ_s is the semiconductor permittivity, and $N_{a,SiNW}$ is the carrier density in the semiconductor channel.

At low V_g values, $E_{00} < kT$, I_{TE} dominates the current flow and only carriers with energy greater than $\phi_b + \psi_c$ contribute to the current. From Equation 5.1, I_{TE} varies exponentially with ψ_c and the SSDMOS behaves like a conventional MOSFET with an $SS \approx \ln 10(kT/q)$.

At higher V_g values, $E_{00} > kT$, and I_{TN} dominates the current flow. From Equation 5.2, I_{TN} is dependent on E and hence the shape of the Schottky barrier which is a function of the nanowire and gate oxide thickness [162]. This implies that the rate of increase of I_{TN} will be less responsive to V_g due to the thick gate oxide (BOX ~ 145nm) used. The SS of a thin body SSDMOS device in this region can be expressed as $SS \approx \ln 10(kT/q)(1 -$

$\exp(-d/(\epsilon_{si}t_{si}t_{ox}/\epsilon_{ox})^{1/2}))^{-1}$ where d is the thickness of the Schottky Barrier beyond which tunneling can be neglected, ϵ_{si} and ϵ_{ox} are the Si and SiO₂ dielectric constants respectively, and t_{si} and t_{ox} are the Si and SiO₂ thicknesses respectively [161]. Thus, SS in the thermionic-field region will be larger than in the thermionic region, as shown in Figure 5.3(a).

Figure 5.4. (a) SS, and (b) DIBL extracted from the I - V of ErSi_{2-x} SSDNW MOSs as a function of L_{ch} from 200nm – 1000nm.

In addition, the presence of sequential SS and single SS for the positive and negative V_g , respectively, is due to the difference in $\Phi_{b\text{eff}}$ of ErSi_{2-x} to $n\text{-Si}$, ($\Phi_{b\text{neff}} \sim 0.32\text{eV}$) and $p\text{-Si}$, ($\Phi_{b\text{peff}} \sim 0.8\text{eV}$). In the negative V_g arm, due to the larger $\Phi_{b\text{peff}}$, thermionic emission does not occur, hence the appearance of a single SS with a larger value and a smaller I_{on} due to the exponential dependence of I_{TN} on $\Phi_{b\text{peff}}$.

Figure 5.4 examines the short channel characteristics of ErSi_{2-x} N-SSDNWMOs. In MOSFETs, a reduction in L_{ch} causes a decrease in the source barrier height. This causes the injection of extra carriers, thereby increasing the off-state leakage current leading to increased SS and DIBL which occurs even at long L_{ch} [51]. Figure 5.4(a) shows the variation of SS with L_{ch} . It has an almost constant SS $\sim 300\text{mV/dec}$ for all L_{ch} . The constant SS extracted indicates that the leakage current is suppressed and this is due to the existence of an $\text{ErSi}_{2-x}/\text{Si}$ Schottky barrier at the source which is relatively immune to the drain bias applied at the L_{ch} measured.

Figure 5.4(b) shows the plot of DIBL against L_{ch} and shows a constant value $\sim 500\text{mV/V}$ consistent with the constant SS value observed. The constant DIBL observed is due to the presence of the Schottky barriers at the source and drain ends which reduce the bending of the SiNW channel potential [63]. Hence, it can be shown that I_{on} is determined mainly by the S/D Schottky barriers (as opposed to the L_{ch}) and is less affected by SCE as compared to conventional MOSFET. SCE starts to have a significant impact only at FinFET and SiNW $L_{ch} \leq 90\text{nm}$ [13].

Figure 5.5(a) is a plot of I_{on}/I_{off} against L_{ch} for the ErSi_{2-x} SSDNWMOs showing an almost constant value of $\sim 10^5$ for all L_{ch} . The absolute values of I_{on} and I_{off} which are not shown here are also independent of L_{ch} . In other words, the variations in the I_{on}/I_{off} ratio

is due to the slight differences in ϕ_p and not due to the difference in channel length which is consistent with the SS and DIBL against L_{ch} shown in Figure 5.4 and is also consistent with the reported values on ‘bottom up’ NiSi SiNW transistors [164].

Figure 5.5. (a) I_{on}/I_{off} versus L_{ch} , and (b) I_{on}/I_{off} characteristics under $V_d = 0.2V$ and $1.2V$ bias of $ErSi_{2-x}$ SSDNW MOS with various L_{ch} s. For $V_d = 0.2V$: I_{off} measured at $V_t - 1.5V$, I_{on} measured at $V_t + 3.5V$. For $V_d = 1.2V$: I_{off} measured at $V_t - 2V$, I_{on} measured at $V_t + 3V$. ‘■’ indicate devices fabricated in this work, ‘X’ indicate Planar bulk/SOI SSDMOS [61], ‘*’ indicate FinFET SSDMOS [12-14], ‘+’ indicates GAA SiNW doped S/D MOSFET [20, 21, 117, 121].

Figure 5.5(b) shows the I_{on}/I_{off} characteristics for $V_d = 0.2V$ and $1.2V$ for various $ErSi_{2-x}$ SSDNWMOSs. The experimental fit shows a close match to the 10^5 constant line which is high in comparison to most Schottky source/drain NMOSFETs [51], opening up the possibility of using the $ErSi_{2-x}$ SSDNWMOS for high performance logic circuits. Also plotted in Figure 5.5(b) are the I_{on}/I_{off} characteristics of various devices found in the literature [12-14, 20, 21, 61, 117, 121]. The fabricated SiNW transistors show better I_{on}/I_{off} characteristics when compared to the ‘top gated’ planar bulk/SOI Schottky transistors and are comparable with the multiple gated Schottky FinFETs even though a back gated geometry is used for our $ErSi_{2-x}$ SSDNWMOS. The GAA SiNW doped S/D MOSFET shows superior I_{on}/I_{off} characteristics due to the excellent electrostatic control offered by the GAA ultra-narrow SiNW channel.

5.3.3 Two-terminal measurements

Two-terminal measurements whereby a potential difference is applied to the S/D without a gate bias is essentially a measurement of a back-to-back Schottky diode [165]. Since both S/D are expected to be similar (except for slight S/D silicide variations), a symmetrically low I - V characteristic is expected due to the reverse biased Schottky diode on both S/D sides except at large voltages. Figure 5.6 shows a typical I - V_{ds} curve of the $ErSi_{2-x}$ SSDNWMOS which shows 3 distinct regions - low V_{ds} bias, medium V_{ds} bias, and high V_{ds} bias, each with its own distinct I - V_{ds} characteristic.

Figure 5.6. Typical two-terminal I - V_{ds} curves of the back to back Schottky diodes across a ErSi_{2-x} SSDNWMOS channel.

At low bias ($2\text{V} \geq V_{ds} \geq 0\text{V}$), the voltage drop is minimal and occurs mainly across the S/D Schottky barriers. At high biases ($8\text{V} \geq V_{ds} \geq 5\text{V}$), most of the voltage drop is across the SiNW channel and the current increases linearly with V_{ds} . The I - V_{ds} can then be differentiated to obtain the resistance of the SiNW (R_{SiNW}), i.e., $R_{\text{SiNW}} = dV_{ds}/dI$. Note that ErSi_{2-x} R_{sh} and $\text{ErSi}_{2-x}/\text{Si}$ R_{co} at high bias are negligible compared to R_{SiNW} .

At medium bias ($5\text{V} \geq V_{ds} \geq 2\text{V}$), the voltage drop is mainly across the reverse biased Schottky barrier at the source which dominates the I - V_{ds} curve. The current mechanism is mainly thermionic-field emission and can be expressed as follows [165].

$$\ln I = V_{ds} \left(\frac{q}{kT} - \frac{1}{E_0} \right) + \ln I_s \quad (\text{Equation 5.3})$$

where I_s is a slowly varying function of applied voltage, $E_0 = E_{00} \coth(qE_{00}/kT)$, $E_{00} = \hbar/2 [N_{a,\text{SiNW}}/m_h \epsilon_s \epsilon_0]^{1/2}$ (same definition as in Section 5.3.2), m_h is the hole effective mass, ϵ_0 is

the permittivity of free space. Thus from the slope of Equation 5.3 in the medium bias region, $N_{a,SiNW}$ can be extracted.

Figure 5.7. Typical two-terminal I - V_{ds} curves at high V_{ds} bias ($8V \geq V_{ds} \geq 5V$) across a $ErSi_{2-x}$ SSDNWMOS channel with $L_{ch} = 300nm$.

Figure 5.7 shows a typical I - V_{ds} curve at high bias (region 3 in Figure 5.6) with an extracted $R_{SiNW} \sim 7.3M\Omega$ obtained by differentiating the I - V_{ds} curve. Nanowire resistivity (ρ_{SiNW}) was determined from R_{SiNW} by using $\rho_{SiNW} = R_{SiNW} \times (A/L_{ch})$ where A is the SiNW cross-sectional area that was derived using the observed TEM SiNW cross-sectional width of $\sim 8nm$.

The R_{SiNW} and ρ_{SiNW} against L_{ch} of the $ErSi_{2-x}$ SSDNWMOS are plotted in Figure 5.8 which shows a slight increase of R_{SiNW} (from $\sim 7M\Omega$ – $14M\Omega$) and a slight decrease of ρ_{SiNW} (from $\sim 100m\Omega.cm$ - $\sim 50m\Omega.cm$) with increasing L_{ch} . The observation of an increasing R_{SiNW} with increasing L_{ch} is expected as I_{on} decreases with increasing L_{ch} . However, the observation of a non-constant ρ_{SiNW} is unexpected and is possibly due to the

slight decrease in A as L_{ch} increases which was not accounted for in the calculation of ρ_{SiNW} and/or an additional contribution from possible SiO_2/Si interface states which have a greater impact as channel length increases due to a the larger surface area to volume ratio.

Figure 5.8. (a) R_{SiNW} and (b) ρ_{SiNW} extracted from the two-terminal I - V_{ds} curves at high V_{ds} bias ($8V \geq V_{ds} \geq 5V$) of ErSi_{2-x} SSDNWMOSs as a function of L_{ch} from 200nm – 1000nm.

To investigate the occurrence of interface states, $N_{a,SiNW}$ was extracted using the following 2 methods. Firstly using the relation $N_{a,SiNW} = 1/q\mu\rho_{SiNW}$ where q is the electronic charge and μ is the effective carrier mobility calculated using field effect

method, i.e., $\mu = g_m L_{ch}^2 / C V_{ds}$, an average $N_{a,SiNW}$ value of $\sim 10^{17} \text{ cm}^{-3}$ was extracted. Note that C is the capacitance given by $C = 2L_{ch} \pi \epsilon_0 \epsilon_r / \ln(2t/w)$ [160] where L_{ch} is the SiNW channel length, ϵ_0 and ϵ_r are the free space and relative permittivities respectively, t is the gate dielectric thickness and w is the SiNW width.

Figure 5.9. Typical two-terminal I - V_{ds} curves at medium V_{ds} bias ($5\text{V} \geq V_{ds} \geq 2\text{V}$) across a $L_{ch} = 300\text{nm}$ ErSi_{2-x} SSDNWMOS channel.

Secondly, using the typical I - V_{ds} curve at medium bias (region 2 in Figure 5.6) as shown in Figure 5.9, $N_{a,SiNW} \sim 8 \times 10^{15} \text{ cm}^{-3}$ obtained by using the slope of the $\ln I$ - V_{ds} curve and applying it to the E_0 and E_{00} relations described above. Figure 5.10 shows a plot of the extracted $N_{a,SiNW}$ against L_{ch} using the Schottky junction model at medium bias. The results indicate that the $N_{a,SiNW}$ is relatively constant at a value of $\sim 1 \times 10^{16} \text{ cm}^{-3}$. The $N_{a,SiNW}$ values calculated using the field effect method are slightly higher than the Schottky junction model at medium bias by around 1 order ($\sim 10^{17} \text{ cm}^{-3}$ versus $\sim 10^{16} \text{ cm}^{-3}$) and may be due to the discrepancy in obtaining an accurate value of C [165].

A comparison of the SOI wafer specifications (Boron doped, $\sim 1 \times 10^{15} \text{ cm}^{-3}$, $\rho \sim 15 \Omega\text{-cm}$) with the extracted SiNW values show that the $N_{a,\text{SiNW}}$ and ρ_{SiNW} are larger by 1 order and smaller by 2 orders respectively. This provides some evidence of a conduction mechanism other than the ideal thermionic, thermionic-field emission characteristic of SSDMOS.

Figure 5.10. Carrier concentration extracted using the Schottky junction model at medium bias as a function of L_{ch} from 200nm – 1000nm.

It is known that the formation of shallow trench isolation induces SiO_2/Si interface defects caused by intrinsic and mechanical stresses generated by thermal mismatch strain and intrinsic volume expansion strain created by the SiO_2/Si interface [166]. Similarly, in stress limited oxidation of Si Fins for the formation of SiNW, the deformation of the oxide around the SiNW causes a stress normal to the SiO_2/Si interface [113] which may also induce SiO_2/Si interface defects. SOI wafers formed by layer transfer (wafer bonding) process have intrinsic trap states at the SOI/BOX interface of $\sim 10^{14} \text{ cm}^{-3}$ [167].

In addition, it has been reported that the conduction of the SiNW might be enhanced by a surface state conduction mechanism [168]. It has been previously reported that intrinsic SiNW (~70nm diameter) grown by the VLS method exhibited $\rho_{SiNW} \sim 0.85 \Omega \cdot \text{cm}$ corresponding to a carrier concentration of $\sim 10^{16} \text{ cm}^{-3}$ which was attributed to surface or interface states at the SiNW surface [169]. Certainly it is probable that interface SiO_2/SiNW defects are present in the ErSi_{2-x} SSDNWMOS devices. These defects provide interface states for “hopping conductivity” to occur and results in the experimentally observed high $N_{a,SiNW}$ and low ρ_{SiNW} than expected as compared to the SOI specifications.

5.4 Effect of Physical Parameters

In this section, various physical parameters (e.g., number of wire channels, S/D silicide material, $\text{ErSi}_{2-x}/\text{Si}$ junction size and silicided depth) are varied with respect to the SSDNWMOS characterized in Section 5.3. The ErSi_{2-x} SSDNWMOSs with a single SiNW channel, fully silicided S/D and non-overlapping Si_3N_4 dummy gate is defined as the control device.

5.4.1 Impact of number of nanowire channels

Figure 5.11 shows the output characteristics, I_d-V_d and g_m-V_g of the ErSi_{2-x} SSDNWMOS control device vs. a side-by-side SiNW channels (2-wire) formed by lithographically patterning side-by-side Si fins. The fabrication process has been described in detail in Section 3.4.5. The output current and peak g_m for the 2-wire configuration is higher for all values of V_g by approximately two times indicating that

ErSi_{2-x} SSDMOS output parameters can be scaled in an approximately linear fashion with the number of SiNW channels. Subsequently, the g_m and I_{on} (measured at $V_g = V_t + 5V$, $V_d = 1.2V$, $V_t = 3.1V$ and $2.9V$ for the control and 2-wire configuration respectively) for all L_{ch} s from 200nm - 1000nm were extracted as shown in Figure 5.12.

Figure 5.11. Comparison of I_d - V_d and g_m - V_g for the control device ($\square$) and 2 wire ($—$) ErSi_{2-x} SSDNWMOS with $L_{ch} = 500nm$.

The peak g_m and I_{on} for the 2-wire ErSi_{2-x} SSDMOS is consistently higher as compared to the control sample for all channel lengths confirming that the device performance can be scaled with number of SiNW channels. The enhancement of I_{on} with number of SiNW

channels is similar to increasing the channel width of a planar MOSFET, i.e., a linear relationship is expected with the addition of each SiNW channel assuming the uniformity of SiNW channels are good.

The peak g_m and I_{on} are almost independent of the channel length for $L_{ch} \leq 500\text{nm}$, which is also agreeable to the results shown in Figure 5.4 (DIBL, SS against L_{ch}) showing that the carrier transport at the measured lengths is less dependent on the semiconducting SiNW channel but more on the Schottky barriers at the S/D [63, 170].

Figure 5.12. Comparison of ErSi_{2-x} SSDNWMOS (a) g_m against L_{ch} , and (b) I_{on} against L_{ch} for control devices (■) and 2 wires (□) devices.

5.4.2 S/D silicide

For N-SSDMOSs, Φ_{bneff} should be as low as possible in order to achieve reasonable I_{on} , SS , g_m etc. Thus ErSi_{2-x} with a $\Phi_{bneff} \sim 0.32\text{eV}$ should theoretically give a higher I_{on} as compared to DySi_{2-x} with a $\Phi_{bneff} \sim 0.38\text{eV}$ as shown in Chapter 2. Figure 5.13 shows the I_d-V_g and g_m-V_g of the control device and DySi_{2-x} SSDNWMOS with a similar L_{ch} . For comparison, the DySi_{2-x} I_{on} , SS , and g_m are $\sim 2290\mu\text{A}/\mu\text{m}$, $\sim 173\text{mV}/\text{dec}$, and $\sim 1310\mu\text{S}/\mu\text{m}$ respectively as compared to the control device I_{on} , SS , and g_m of $\sim 900\mu\text{A}/\mu\text{m}$, $\sim 180\text{mV}/\text{dec}$, and $\sim 577\mu\text{S}/\mu\text{m}$.

Figure 5.13. I_d-V_g , g_m-V_g characteristics of ErSi_{2-x} SSDNWMOS ($\square$) and DySi_{2-x} SSDNWMOS ($—$) with $L_{ch} = 500\text{nm}$. The I_d-V_g , and g_m-V_g of DySi_{2-x} have been shifted by $+2.2\text{V}$ for easier comparison.

As can be seen, although the DySi_{2-x} Φ_{bneff} is larger than the ErSi_{2-x} Φ_{bneff} by 0.06eV , the electrical characteristics are clearly better than the control devices. This gives an indication that there are other factors other than the Φ_{bneff} which have greater influence on the electrical performance of the SSDNWMOS.

5.4.3 Impact of ErSi_{2-x}/Si junction size

In order to study the particular effects of S/D Schottky junction size on the performance of ErSi_{2-x} SSDNW MOSs, two different Si₃N₄ dummy gates (to define ErSi_{2-x}/Si junction size) were lithographically patterned (see Chapter 3.4.5).

Figure 5.14. Comparison of ErSi_{2-x} SSDNW MOS (a) I_{on} against L_{ch} , and (b) SS against L_{ch} for the larger ErSi_{2-x}/Si junction devices with $\sim 80\text{nm}$ ErSi_{2-x}/Si junction ($\square$) and control devices with $\sim 8\text{nm}$ ErSi_{2-x}/Si junction ($\blacksquare$).

The overlapping Si₃N₄ dummy gate is approximately longer by $\sim 50\text{nm}$ on each side compared to the non-overlapping Si₃N₄ dummy gate which results in the formed ErSi_{2-x}.

x /Si junction size to be larger by ~ 10 times (80nm for the larger ErSi_{2-x} /Si junction device vs. 8nm for the control devices). Note that the overlapping Si_3N_4 dummy gate devices would have a longer L_{ch} by $\sim 100\text{nm}$. However, it is believed that the effect of L_{ch} is almost negligible as compared to ErSi_{2-x} /Si junction size as can be seen by the almost constant I - V characteristics with length (e.g. I_{on} , SS etc.).

Figure 5.15. Comparison of ErSi_{2-x} SSDNW MOS V_t against L_{ch} for the larger ErSi_{2-x} /Si junction devices with $\sim 80\text{nm}$ ErSi_{2-x} /Si junction ($\square$) and control devices with $\sim 8\text{nm}$ ErSi_{2-x} /Si junction ($\blacksquare$).

Figure 5.14 shows the comparison of the ErSi_{2-x} /Si junction size for various I - V parameters, I_{on} measured at $V_d = 1.2\text{V}$, $V_g = V_t + 5\text{V}$ and SS against L_{ch} from 200nm – 1000nm of the ErSi_{2-x} SSDNW MOS. The control devices showed a consistently higher I_{on} and lower SS which are essentially the result of improved electrostatics of the narrower ErSi_{2-x} /Si junction and a smaller junction size. As a MS Schottky junction is scaled down in size, the electrical transport deviates from that of a conventional Schottky diode leading to a thinner Schottky barrier with enhanced tunneling current [171].

Figure 5.15 shows the comparison of the $\text{ErSi}_{2-x}/\text{Si}$ junction size for V_t against L_{ch} of the ErSi_{2-x} SSDNWMOS. The larger V_t for the control devices as compared to the larger $\text{ErSi}_{2-x}/\text{Si}$ junction devices is related to the difference in the SiNW channel size due to (1) a decrease in the effective density of states [98], and/or (2) an increase in Φ_{beff} due to the conduction subband shifting to higher energy levels [172], as nanowire dimensions reduce to $<10\text{nm}$. On the other hand, V_t is independent of L_{ch} for all samples which can be attributed to the fact the effect of the diameter and surface states could be of greater importance compared to the length of SiNW devices [20]. Certainly, a larger V_t for the control devices compared to the larger $\text{ErSi}_{2-x}/\text{Si}$ junction devices is undesirable. However, as shown in Figure 5.16, the control devices showed a higher I_{on} and better SS.

5.4.4 Impact of S/D silicided thickness

Figure 5.16 shows the comparison of R_{SiNW} of the ErSi_{2-x} SSDNWMOSs with two different S/D ErSi_{2-x} thicknesses.

Figure 5.16. Comparison of ErSi_{2-x} SSDNWMOS R_{SiNW} against L_{ch} for control devices (■) and partially silicided S/D devices (□).

The S/D ErSi_{2-x} thickness was controlled by the deposited Er thickness (control - 80nm deposited Er vs. partially silicided S/D devices - 50nm deposited Er) which resulted in the following S/D stacks : control - 120nm ErSi_{2-x} /5nm Si/BOX and partially silicided S/D devices - 75nm ErSi_{2-x} /50nm Si/BOX. This is depicted in the TEM images of the S/D pad in Figure 5.17.

Figure 5.17. TEM micrographs of ErSi_{2-x} SSDNWMOS S/D pads. (a) Partially silicided S/D devices - 75nm ErSi_{2-x} /50nm Si/BOX, and (b) control - 120nm ErSi_{2-x} /5nm Si/BOX.

The R_{SiNW} against L_{ch} of the partially silicided devices shows a slight increase of R_{SiNW} (from $\sim 8\text{M}\Omega - 14\text{M}\Omega$), similar to the control devices (from $\sim 7\text{M}\Omega - 14\text{M}\Omega$). The R_{SiNW} of the partially silicided devices is approximately $\sim 1\text{M}\Omega$ larger than the control devices and is a result of an additional resistance contribution of a 50nm unsilicided SOI. Note that the SiNW channel is located at the bottom of the SOI epi-layer as depicted in Figure 3.3(a).

Figure 5.18 shows a comparison of the $I_{\text{on}}/I_{\text{off}}$ characteristics for the control devices as well as the partially silicided S/D devices. In addition, 2-wire devices and larger ErSi_{2-x}

x /Si junction devices ($\sim 80\text{nm}$ junction size) are also plotted in the same figure. The 2-wire devices showed a similar I_{on}/I_{off} ratio ($\sim 10^5$) derived from the expected 2 times larger absolute I_{on} and I_{off} values. The larger ErSi_{2-x} /Si junction and partially silicided S/D devices exhibited average I_{on}/I_{off} ratios of $\sim 2 \times 10^4$ and $\sim 9 \times 10^3$, respectively, largely due to a smaller I_{on} as a result of an increased series resistance and degraded electrostatic gate control.

Figure 5.18. (a) I_{on}/I_{off} versus L_{ch} , and (b) I_{on}/I_{off} characteristics under $V_d = 0.2\text{V}$ and 1.2V bias of ErSi_{2-x} SSDNWMOS with various L_{ch} . For $V_d = 0.2\text{V}$: I_{off} measured at $V_t - 1.5\text{V}$, I_{on} measured at $V_t + 3.5\text{V}$. For $V_d = 1.2\text{V}$: I_{off} measured at $V_t - 2\text{V}$, I_{on} measured at $V_t + 3\text{V}$. ‘■’ indicates control and 2-wire devices, ‘□’ indicates larger ErSi_{2-x} /Si junction devices, and ‘Δ’ indicates partially silicided S/D devices.

5.4 Schottky Barrier Height Modulation

As mentioned in Section 5.3.2, the current flowing through the SiNW channel is a combination of thermionic emission, which is dependent on the height of the barrier, and tunneling current, which is dependent on both the height and shape/thickness of the

barrier [162]. The barrier thickness can be modulated by both the gate and the source-drain field. Temperature dependent electrical I_d - V_g and I_d - V_d were thus carried out in order to obtain the Φ_{beff} modulation by V_d and V_g as it gives an indication of the ErSi_{2-x} SSDNWMOS I_{on} , SS and subthreshold performance.

Figure 5.19. Temperature dependent I_d - V_g characteristics of an ErSi_{2-x} SSDNWMOS with $L_{ch} = 350\text{nm}$.

Figure 5.19 shows the temperature dependent I_d - V_g characteristics of an ErSi_{2-x} SSDNWMOS with a L_{ch} of 350nm, measured at $V_d = 1.2\text{V}$ for a temperature range of 136K - 280K. This temperature range is sufficient to suppress kinetic thermal emission as the ErSi_{2-x} Φ_{beff} is $\sim 0.32\text{eV}$ as shown in Section 5.1. Also, it must be mentioned that the Φ_{beff} extracted is the effective barrier height taking into account both thermionic and tunneling and thus is a measure of the height and shape of the barrier as opposed to just solely the barrier height. The increase in the I_{on} with increasing temperature is due to an

increase in the temperature dependent thermionic and thermionic-field emission. The difference in the slopes of the forward and reverse I_d - V_g gives an indication of different conduction mechanisms as discussed in Section 5.3.2.

Figure 5.20. (a) Extracted E_a against V_g at $V_d = 0.2V$ (□) and $1.2V$ (■), and (b) E_a against V_d at the V_g of $8V$. The error bars indicate fitting errors.

The associated Arrhenius plot, i.e., the plot of $\ln(I_d/T^2)$ against $1/T$ for various values of V_g or V_d was derived. From the Arrhenius plot, the corresponding extracted activation

energy against the applied potential is shown in Figure 5.20. This activation energy (E_a) corresponds to the Φ_{beff} (both hole and electron), as the gate and drain potential modulates the SiNW band profile.

Figure 5.20(a) shows the variation in Φ_{beff} as V_g is swept from -12 to 12V. When V_g is biased at 0V, the maximum Φ_{beff} value occurs at 0.72eV which is approximately the value measured on the bulk diode. When V_g is biased at V_t (~7V), Φ_{beff} is at 0.06eV at which thermionic-field emission occurs. Φ_{beff} is then effectively 'transparent' to electrons and is then limited by the SiNW channel body. As can be seen from Figure 5.20(a), the Φ_{beff} modulation is more responsive in the positive V_g region due to the lower Φ_{bneff} (~0.32eV) as compared to the negative V_g region which modulates a higher Φ_{peff} (~0.8eV).

From the slope of Figure 5.20(a) in the subthreshold region for the positive V_g direction, the Φ_{beff} modulation is ~0.1eV/V. A comparison of the responsiveness of the Φ_{beff} modulation can be attained from the Φ_{beff} modulation of NiSi SSDMOS with dopant segregation which is ~0.9eV/V [173]. Although a much weaker capacitive coupling ~50x is expected from ErSi_{2-x} SSDNWMOS compared to the NiSi SSDMOS due to the difference in gate electrostatic control (planar top polysilicon gate with a gate oxide thickness of ~3nm as compared to back-gated silicon with gate oxide thickness ~145nm), the ErSi_{2-x} SSDNWMOS Φ_{beff} modulation is only ~10x smaller compared to the NiSi SSDMOS indicating that the SSDNWMOS S/D Schottky barrier is extremely responsive.

Figure 5.20(b) shows the variation in Φ_{beff} as V_d is swept from -2V to 2V. Φ_{beff} is almost independent of V_d , indicating that saturation has been reached as well as absence of SCE. This indicates that the dominant current control mechanism is the applied gate

potential with minimal effect by the drain potential once the effective barrier is lowered sufficiently for the thermionic-field emission to occur. Also observed is a slight decrease in Φ_{beff} in the negative V_d region. The observed S/D Φ_{beff} asymmetry is probably due to the sensitivity of MS interface to process variations.

5.5 Summary

We have demonstrated N-SSDMOS utilizing Si nanowire with reduced dimensions $\sim 8\text{nm}$ as the channel body and ErSi_{2-x} as the S/D metal silicide using a ‘top-down’ CMOS compatible technology. Low temperature silicidation (450°C) was shown to be a viable approach as good ErSi_{2-x} material characteristics were demonstrated.

The devices show Schottky barrier transistor behavior with high I_{on}/I_{off} ratio $\sim 10^5$ and high drive current $\sim 900\mu\text{A}/\mu\text{m}$ because of the low ϕ_{bn} of $\text{ErSi}_{2-x}/n\text{-Si}$ and the improved electrostatics on the $\sim 8\text{nm}$ wire channel. The carrier transport is mainly determined by the MS interface instead of the channel body.

Two-terminal measurements indicate that the ρ_{SiNW} is relative low and $N_{a,SiNW}$ is relatively high which indicates that a surface conduction mechanism may be present in the ErSi_{2-x} SSDNWMOS. The device performance is shown to be strongly affected by device physical structure, e.g., multiple SiNW channels, $\text{ErSi}_{2-x}/\text{Si}$ junction size, and S/D silicided depth. Φ_{beff} modulation by the gate potential is shown to be extremely responsive due to the excellent electrostatic control of the SSDNWMOS S/D Schottky barrier.

CHAPTER 6

GATE-ALL-AROUND ErSi_{2-x}, PtSi, and NiSi SCHOTTKY SOURCE/DRAIN (S/D) SILICON NANOWIRE MOSFETs

6.1 Introduction

This chapter presents the electrical characteristics of N-MOSFETs using twin stacked SiNW with a bottom wire ~5nm and a top wire ~8nm as the semiconductor channels, ErSi_{2-x} as the S/D, and GAA channel in a SSDMOS architecture. PtSi P-SSDNWMOS and NiSi P and N-SSDNWMOS were then fabricated for complementary SSDNWMOS (C-SSDNWMOS) operation. Lastly, the effects of MS junction size were studied by analyzing the electrical characteristics of Schottky diodes and SSDNWMOSs with varying MS junction sizes. It should be mentioned that the I - V characteristics of the GAA SSDNWMOS described in this section are expected to have better performances compared to the previous Chapter due to the different electrostatic control mechanisms (gate-all-around SiNW with thin oxide versus back-gated with thick gate oxide).

6.2 Electrical Characteristics of GAA ErSi_{2-x} N-SSDNWMOS

6.2.1 Transfer and Output Characteristics

Figure 6.1 shows the I_d - V_g and I_d - V_d curves of a GAA ErSi_{2-x} N-SSDNWMOS with a gate length (L_g) = 90nm. The I_d - V_g curve shows high drive current with increasing positive V_g due to the low Φ_{beff} to electrons (of ~0.32eV) at the ErSi_{2-x}/n-Si interface, and low current in the negative V_g region due to the high Φ_{beff} to holes (of ~0.8eV) at the

ErSi_{2-x}/p-Si interface. The Φ_{beff} were determined experimentally in Section 5.2. This electrical behavior is characteristic of N-SSDMOSs.

Figure 6.1. (a) I_d - V_g and (b) I_d - V_d characteristics of a GAA ErSi_{2-x} N-SSDNWMOS with $L_{ch} = 140\text{nm}$ and $L_g = 90\text{nm}$.

Examination of the I_d - V_g curve shows that I_d is increasing in the negative V_g arm with a profile similar to gate induced drain leakage (GIDL) [174]. However, this reverse current is a signature of SSDMOS devices, i.e., ambipolar behavior, and is due to the hole

current for N-SSDMOS when the channel is in accumulation. This hole current becomes more pronounced at $V_d = 1.2\text{V}$ (in comparison with $V_d = 0.05\text{V}$) as the Schottky barrier at the drain end becomes thinner at higher V_d , allowing more holes to tunnel through the drain Schottky barrier.

The drive current is high with a measured value of $\sim 464\mu\text{A}/\mu\text{m}$ at $V_d = 1.2\text{V}$. The SS is $79\text{mV}/\text{decade}$, with a DIBL of $53\text{mV}/\text{V}$, an I_{on}/I_{off} ratio of $\sim 1.1 \times 10^5$ measured at $V_d = 50\text{mV}$, and a V_t of 0.14V . The SS and DIBL are close to the lowest values reported of SS = $70\text{mV}/\text{decade}$, DIBL = $30\text{mV}/\text{V}$ that were extracted from $\text{ErSi}_{1.7}$ N-SSDMOSs with $L_g = 100\text{nm}$ on bulk Si. However, the reported I_{on} is significantly lower ($90\mu\text{A}/\mu\text{m}$ at $V_d = 1.2\text{V}$) [94]. The reasons for the reasonably low SS and larger I_{on} is believed to be due to the improved electrostatics of the GAA channel [116] as well as Schottky Barrier thinning [171] at the MS junction that will be discussed in Section 6.4.

In addition, the GAA ErSi_{2-x} N-SSDNWMOS shows a very slight change in SS as compared to the BG ErSi_{2-x} SSDNWMOS which shows pronounced sequential SS. Note that the sequential SS is due to transition from TE at low V_g to TFE at higher V_g . The range of V_g in which TE dominates depends on the rate of the Φ_{beff} change with the applied V_g (Φ_{beff} modulation). Since the GAA SSDNWMOS has thinner gate oxide (9nm versus 145nm), and a smaller MS junction size (5nm versus 8nm), we expect a larger Φ_{beff} modulation. This leads to a smaller TE range as well as a less pronounced transition between TE and TFE.

The I_d - V_d characteristics in Figure 6.1(b) shows an absence of an upwardly sloping sublinear turn-on found in most SSDMOSs [61, 92], which is due to low Φ_{beff} . There is a

clear presence of linear and saturation regions for all V_g biases, indicating that the channel pinch-off has been reached.

Figure 6.2. Extracted transistor characteristics from the I_d - V_g of GAA ErSi_{2-x} N-SSDNWMOSSs. (a) I_{on}/I_{off} against L_g from 155nm – 70nm, and (b) I_{on}/I_{off} characteristics for various L_g . I_{off} measured at $V_t - 0.6V$, I_{on} measured at $V_t + 0.6V$.

Figure 6.2(a) shows the I_{on}/I_{off} against L_g characteristics of GAA ErSi_{2-x} N-SSDNWMOSSs. The I_{on}/I_{off} shows an almost constant value of $\sim 6.5 \times 10^4$ for all L_g s. The absolute values of I_{on} and I_{off} are also independent of L_g which implies that the variations in the I_{on}/I_{off} ratio is due to the slight differences in Φ_{beff} and not due to the difference in

L_g . This observation is consistent with the I_{on}/I_{off} against L_g characteristics of the back-gated ErSi_{2-x} SSDNWMOSSs discussed in Section 5.3.2.

Figure 6.2(b) shows the I_{off} versus I_{on} characteristics of the GAA ErSi_{2-x} N-SSDNWMOSSs for various L_g values. Also included in Figure 6.2(b) are the I_{off} versus I_{on} characteristics of the best RESi_{2-x} SSDMOS results reported [10, 14, 54, 94, 175]. The GAA ErSi_{2-x} N-SSDNWMOSSs I_{on} values are higher than the reported I_{on} values even with longer L_g . The largest reported I_{on} values thus far are from devices in which the L_g ranges from 15nm [10] to 25nm [14] respectively. The reason for the increased I_{on} is believed to be a result of enhanced tunneling current due to a possible Schottky barrier thinning effect with MS junction size reduction [171].

Figure 6.3 shows the short channel characteristics of the GAA ErSi_{2-x} N-SSDNWMOSSs. In MOSFETs, a reduction in L_{ch} causes a decrease in source barrier height which causes the injection of extra carriers, thereby increasing the off state leakage current and leading to increased SS and DIBL even at $L_{ch} \sim 3\mu\text{m}$ [51]. Figure 6.3(a) shows the SS (extracted from the TE region of the I_d - V_g) curve against L_g . The SS values extracted are larger than that of conventional MOSFETs even at the longer L_{ch} . The SS of SSDMOSs in the thermionic region is higher than that defined by thermal limit in conventional MOSFETs (i.e., $SS \sim \ln 10 kT/q$ [51]) due to the semiconductor region under the spacer which is not controlled by the gate which reduces the control of the drain current by V_g [63].

The SS increases slightly from $\sim 65\text{mV/decade}$ to 87mV/decade as L_g decreases from 155nm to 70nm. From $L_g = 155\text{nm}$ to 85nm, the SS increases only slightly (65mV/decade to 76mV/decade). These SS values are comparable with the lowest SS reported

(70mV/decade) for an ErSi_{1.7} SSDMOS with $L_g = 100\text{nm}$. At L_g less than 85nm, SS increases to values greater than 100mV/decade. Large SS values at short L_g s have also been observed for RESi_{2-x} (rare earth silicide) based SSDMOSs with $L_g = 25\text{nm}$ (SS = 125mV/decade) [14] and $L_g = 23\text{nm}$ (SS = 120mV/decade) [94].

Figure 6.3. Extracted transistor characteristics from the I_d - V_g of GAA ErSi_{2-x} N-SSDNWMOSs. (a) SS measured at $V_d = 50\text{mV}$, and (b) DIBL as a function of L_g from 155nm – 70nm.

Figure 6.3(b) shows the DIBL, also known as drain induced barrier thinning (DIBT) [175], against L_g . The DIBL increases from around 21mV/V to 101mV/V as L_g decreases from 155nm to 70nm. From $L_g = 155\text{nm}$ to 90nm, the DIBL increases only slightly from 21.3mV/V to 45mV/V and its value is close to the theoretical DIBL of SSDMOSs (25mV/V to 33mV/V) [94] indicating the absence of SCE. At L_g less than 90nm, the DIBL increases to values greater than 100mV/V, certainly larger than the theoretical values. Large DIBL values have also been reported experimentally for RESi_{2-x} based SSDMOSs with $L_g = 25\text{nm}$ (DIBL = 260mV/V) [14] and $L_g = 23\text{nm}$ (DIBL = 100mV/V) [94].

Note that the theoretical DIBL values for SSDMOS is expected to scale better at L_g less than 30nm as compared to planar or double gated conventional MOSFETs. This is due to the presence of a Schottky barrier at the source which reduces the modulation of the channel potential by the drain [63, 92]. Hence the GAA ErSi_{2-x} SSDWNMOS shows excellent electrical characteristics with short channel performance equal to or better than the reported RESi_{2-x} based SSDMOS [10, 14, 54, 94, 175].

6.2.2 Current Transport Mechanisms

Figure 6.4(a) shows the temperature dependent I_d - V_g characteristics of a GAA ErSi_{2-x} SSDNWMOS with $L_g = 90\text{nm}$, measured at $V_d = 50\text{mV}$ for a temperature range of 288K - 353K. The Φ_{beff} extracted is the effective Schottky barrier height taking into account both thermionic and tunneling current. It is thus a measure of the Schottky barrier height and Schottky barrier thickness. From Figure 6.4(a), the current increases with increasing

temperature which is due to an increase in the temperature dependent thermionic plus thermionic field currents.

Figure 6.4. (a) Temperature dependent (288K to 353K) I_d - V_g measured at $V_d = 50$ mV. (b) Φ_{beff} against V_g . The error bars indicate fitting errors.

The associated Arrhenius plot, i.e., the plot of $\ln(I_d/T^2)$ against $1/T$ for various values of V_g was derived and shown in the inset of Figure 6.4(a). The corresponding extracted Φ_{beff} against V_g from $V_g = -0.3$ V to 0.1 V is shown in Figure 6.4(b). From the slope of Figure 6.4(b), for $V_g = -0.3$ V to -0.15 V, the current transport mechanism is dominated by

TE with a slope of $\sim 2.2\text{eV/V}$. In this region, V_g modulates the Schottky barrier height towards a value $\sim 0.32\text{eV}$. At $V_g = -0.15\text{V}$, the Schottky barrier height is equal to 0.32eV . Beyond this value, V_g modulates the Schottky barrier thickness and TFE starts to dominate the current flow. The Φ_{beff} modulation at this point then reduces to $\sim 1.09\text{eV/V}$. Thus, the change in Φ_{beff} modulation is due to the different current conduction mechanisms.

Eventually at even larger V_g values, the Schottky barrier thickness is then effectively ‘transparent’ to electrons and current is limited by the SiNW resistance. This occurs at $V_g = 0.03\text{V}$ whereby $\Phi_{\text{beff}} = 0.097\text{eV}$. The transition to resistance (R)-limited current transport can be observed as a change of slope at $V_g > 0.03\text{V}$ in both Figures 6.4(a) and 6.4(b).

6.3 Electrical Characteristics

For complementary performance in SSDNWMOS, P-SSDNWMOS and N-SSDNWMOS are required. This can be achieved by using (1) complementary silicides, i.e., two different silicides, one having low Φ_{beff} on $p\text{-Si}$, and one having low Φ_{beff} on $n\text{-Si}$ [10, 94], or (2) mid-gap (to Si bandgap) silicides incorporating Schottky barrier modification techniques [12, 13, 65-71, 78].

6.3.1 GAA PtSi P-SSDNWMOS

Rare earth silicides (e.g. ErSi_{2-x} , $\text{YbSi}_{1.8}$) with Φ_{beff} to electrons $\sim 0.27 - 0.32\text{eV}$ [10, 54, 61], are typically used for N-SSDMOS, while PtSi with Φ_{beff} to holes $\sim 0.15\text{eV}$ [10, 61] is typically used for P-SSDMOS. It must be mentioned that barrier modification by

strain [76] and dopant segregation [72] have also been applied to PtSi P-SSDMOS in an effort to improve the transistor characteristics.

Figure 6.5. (a) I_d - V_g and (b) I_d - V_d characteristics of a GAA PtSi P-SSDNWMOS with $L_{ch} = 140\text{nm}$ and $L_g = 90\text{nm}$.

Figure 6.5 shows the I_d - V_g and I_d - V_d characteristics of a PtSi SiNW GAA P-SSDNWMOS with $L_{ch} = 140\text{nm}$ and $L_g = 90\text{nm}$. The I_d - V_g curve shows high current in the negative V_g region and low current in the positive V_g region characteristic of P-

SSDMOSs. This characteristic allows GAA PtSi P-SSDNWMOSs to be used together with GAA ErSi_{2-x} N-SSDNWMOS to provide complementary transistor action. Examination of the I_d - V_g curve shows GIDL-like behavior similar to the N-SSDNWMOSs. In this instance, the reverse current is due to the electron current when the channel is in accumulation.

From Figure 6.5, the extracted P-SSDNWMOS characteristics show near ideal SS = 60mV/decade, low DIBL = 10mV/V, I_{on}/I_{off} ratio of $\sim 5.6 \times 10^5$ at $V_d = -50$ mV, $V_t = -0.3$ V, and $I_{on} = 618\mu\text{A}/\mu\text{m}$ with $I_{off} = 1.1 \times 10^{-3}\mu\text{A}/\mu\text{m}$ at $V_d = 1.2$ V. From the existing reports on PtSi P-SSDMOS using SOI or bulk silicon as the starting substrate without barrier modification techniques [61, 85], the I_{on} values range from $60\mu\text{A}/\mu\text{m}$ to $629\mu\text{A}/\mu\text{m}$, the I_{off} values range from $2 \times 10^{-5}\mu\text{A}/\mu\text{m}$ to $15\mu\text{A}/\mu\text{m}$, with the highest I_{on}/I_{off} reported $\sim 2.5 \times 10^6$ [85]. Note that the highest I_{on} , I_{on}/I_{off} and lowest I_{off} values are reported for different devices. Thus, a comparison of PtSi P-SSDNWMOS with the reported PtSi P-SSDMOS devices shows that the PtSi P-SSDNWMOS has excellent overall characteristics comparable with the reported values.

In addition, the PtSi P-SSDNWMOS SS and DIBL values extracted from Figure 6.5 are lower than the best reported PtSi P-SSDMOS SS and DIBL values of SS = 80mV/decade and DIBL = 85mV/V respectively [85]. The excellent I_{on} and SS characteristics for the P-SSDNWMOS are in agreement with the N-SSDNWMOS, and are believed to be a result of improved electrostatics of the GAA channel [116] and enhanced tunneling current due to a possible Schottky barrier thinning effect with MS junction size reduction [171].

The I_d - V_d characteristics are also similar to the N-SSDNWMOS showing an absence of an upwardly sloping sublinear turn-on [61, 92], and a clear presence of linear and saturation regions for low V_g biases, indicating that the channel pinch-off has been reached.

6.3.2 GAA NiSi C-SSDNWMOS

Figure 6.6. I_d - V_g characteristics of a NiSi N-SSDNWMOS with L_{ch} = 140nm and L_g = 90nm.

In midgap (to the silicon bandgap) silicide scheme, silicides (including CoSi_2 and NiSi) having Φ_{beff} close to 0.56eV (silicon bandgap energy/2) for both p and n -type silicon can be used [13, 65-71, 78]. These silicides are used in conjunction with Φ_{beff} modification techniques including (1) dopant segregation to the MS interface [13, 65-71], (2) interfacial oxide at the MS interface [77], (3) sulphur passivation at the MS interface [66], (4) metal segregation to the MS interface [78], and (5) strain induced Φ_{beff} lowering [70]. In the dopant segregation scheme, arsenic and antimony are usually used for N-

SSDMOS [66, 68, 74] while boron is used for P-SSDMOS [65, 66, 68]. In this section, NiSi having Φ_{beff} to electrons of $\sim 0.65\text{eV}$ at the NiSi/*n*-Si Schottky junction, and Φ_{beff} to holes of $\sim 0.47\text{eV}$ at the NiSi/*p*-Si Schottky junction [3], were used to implement C-SSDNWMOSs.

Figure 6.7. (a) I_d - V_g and (b) I_d - V_d characteristics of an GAA NiSi C-SSDNWMOS with $L_{\text{ch}} = 140\text{nm}$ and $L_g = 90\text{nm}$. Note that N-SSDNWMOS employed arsenic segregated S/D.

Figure 6.6 shows the I_d - V_g characteristics of a NiSi N-SSDNWMOS with $L_g = 90\text{nm}$. A higher current in the negative arm compared to the positive arm is observed. Certainly, this behavior is undesirable for an N-MOSFET and occurs because NiSi is used as the S/D silicide for the N-SSDNWMOS. A metal silicide is a source of free carriers (both electron and hole) at the S/D unlike a conventional N-MOSFET which has only electrons (from n -type doping) at the S/D [92]. Therefore, for NiSi N-SSDNWMOSs, we would expect the existence of a hole current during channel accumulation, as well as an electron current during channel inversion. Owing to the lower Φ_{beff} of NiSi/ p -Si compared to NiSi/ n -Si ($\sim 0.47\text{eV}$ versus $\sim 0.65\text{eV}$), it follows naturally that the hole current during channel accumulation will be larger than the electron current during channel inversion. In order for NiSi to function effectively as a N-SSDNWMOS, arsenic segregation was employed for the N-SSDNWMOS to reduce Φ_{beff} to electrons from a value of $\sim 0.65\text{eV}$.

Figure 6.7 shows the I_d - V_g and I_d - V_d characteristics of a GAA NiSi C-SSDNWMOS with $L_{\text{ch}} = 140\text{nm}$ and $L_g = 90\text{nm}$. The N-SSDNWMOS was implanted with arsenic before Ni silicidation to induce dopant segregation. Clearly, complementary transistor action is observed with high/low current in the positive V_g region and low/high current in the negative V_g region for N-SSDNWMOS/P-SSDNWMOS respectively. In addition, the I_d - V_g curves are almost symmetrical which raises the possibility of using a single metal for the S/D silicide formation, greatly simplifying device processing. GIDL-like behavior is again observed due to the electron/hole current for P-SSDMOS/N-SSDMOS when the channel is in accumulation [174].

A comparison of the N-SSDNWMOS characteristics with (Figure 6.7(a)) and without (Figure 6.6) arsenic Segregation shows an enhancement of I_d in the positive V_g region and

suppression of I_d in the negative V_g region, indicating the successful reduction of Φ_{beff} to electrons. Note that for a arsenic segregated concentration of $\sim 5 \times 10^{19}$ atoms/cm³ at the NiSi/*n*-Si interface, the Φ_{beff} to electrons reduces to ~ 0.15 eV from a value of 0.67eV [66].

Figure 6.8. I_{on}/I_{off} characteristics of GAA NiSi (a) N-SSDNWMOS, and (b) P-SSDNWMOS. I_{off} measured at $V_t - 0.6$ V, I_{on} measured at $V_t + 0.6$ V.

The I_d - V_g plots show a low SS of $\sim 60\text{mV/decade}$ for both N and P-SSDNWMOSs. In addition, the P-SSDNWMOS showed DIBL of $\sim 10\text{mV/V}$, $V_t = -0.32\text{V}$, a I_{on}/I_{off} ratio of 2.28×10^5 measured at $V_d = 50\text{mV}$, $I_{off} \sim 5.2 \times 10^{-3}\mu\text{A}/\mu\text{m}$, with $I_{on} \sim 399\mu\text{A}/\mu\text{m}$ measured at $V_d = 1.2\text{V}$, while the N-SSDNWMOS showed DIBL of $\sim 13\text{mV/V}$, $V_t = 0.54\text{V}$, a I_{on}/I_{off} ratio of 1.46×10^5 measured at $V_d = 50\text{mV}$, $I_{off} \sim 5.19 \times 10^{-3}\mu\text{A}/\mu\text{m}$, with $I_{on} \sim 513\mu\text{A}/\mu\text{m}$ measured at $V_d = 1.2\text{V}$. Certainly, the extracted transistor characteristics are comparable or better than the reported NiSi based SSDMOS even though barrier modification techniques were not used (for P-SSDNWMOS).

The I_d - V_d characteristics of the same device show the absence of an upwardly sloping sublinear turn-on, an indication of low effective Schottky barrier height [61, 92]. For the P-SSDNWMOS, there is a clear presence of linear and saturation regions for all V_g biases, indicating that the channel pinch-off has been reached and also the absence of SCE. On the other hand, the N-SSDNWMOS does not show clear saturation region at higher V_g biases due to the higher Φ_{beff} to electrons. The higher Φ_{beff} during N-SSDNWMOS ‘on’ state can also be observed in the I_d - V_g curve which has a smaller forward current and larger reverse current compared to that of the P-SSDNWMOS current.

Figure 6.8 shows the I_{on}/I_{off} characteristics of various NiSi C-SSDNWMOSs. The experimental fit of the slope shows the I_{on}/I_{off} ratios for both the N and P-SSDNWMOS are slightly higher than 10^5 (N-SSDNWMOS : $\sim 3 \times 10^5$, P-SSDNWMOS : $\sim 2 \times 10^5$). A comparison of the I_{on}/I_{off} ratios of the C-SSDNWMOS and NiSi SSDMOS without barrier modification techniques [66, 68] shows that the ratio has increased by more than 15 and 7 times for the N and P-SSDMOS, respectively. Also plotted in Figure 6.8 are the I_{on}/I_{off}

characteristics of the best SSDMOS results published [10, 12, 13, 66-72, 76], all of which employed some forms of barrier modification technique. It should be noted that for the NiSi P-SSDNWMOS, no barrier modification techniques was used in our experiments, and the improvements is owing to the device architecture (i.e., SiNW channel and GAA architecture) without additional process steps.

It has been reported that the SS (in the TFE region) of a thin body SSDMOS device can be expressed as:

$$SS \approx \ln 10(kT/q)(1 - \exp(-d/(\epsilon_{si}t_{si}t_{ox}/\epsilon_{ox})^{1/2}))^{-1} \text{ (Equation 6.1)}$$

where d is the thickness of the Schottky Barrier beyond which tunneling can be neglected, ϵ_{si} and ϵ_{ox} are the Si and SiO₂ dielectric constants respectively, and t_{si} and t_{ox} are the Si and SiO₂ thicknesses respectively [161]. Thus, it is not surprising for the GAA NiSi C-SSDNWMOS to exhibit low SS and hence large I_{on} . In addition, the absolute values of I_{on} and I_{off} are independent of L_g which implies that the variations in the I_{on}/I_{off} ratio is due to the difference in Φ_{beff} (owing to process variations) and not due to the difference in L_g .

The short channel characteristics of the C-SSDNWMOS will be investigated in Figure 6.9 which shows average values of (a) SS, and (b) DIBL of the GAA NiSi C-SSDNWMOSs at varying L_g . In Figure 6.9(a), from $L_g = 105\text{nm}$ to 85nm , the SS varies around 65 – 70mV/decade, for both N and P-SSDNWMOSs. The SS values are comparable with the lowest SS reported (N-SSDMOS : 60.4mV/decade, P-SSDMOS : 71mV/decade) for a NiSi SSDMOS with $L_g = 49\text{nm}$ and modified Schottky barriers by dopant segregation [12].

Figure 6.9. (a) SS, and (b) DIBL extracted from the I_d - V_g of GAA NiSi C-SSDNWMOSSs as a function of L_g from 105nm – 70nm.

Also observed in Figure 6.9(a), for L_g less than 85nm, SS increases to values greater than 100mV/decade. This large SS values at L_g less than 80nm have also been observed for NiSi FinFET SSDMOS with dopant segregated MS junctions [13]. Note that for a long channel NiSi P-SSDMOS on bulk Si ($t_{si} = 25$ nm) without barrier modification, the reported SS is 70mV/dec [68]. Certainly, for the GAA NiSi P-SSDNWMOSSs, the observation of SS close to 60mV/decade is owing to the device architecture. As a MS

junction is scaled, electrostatics due to the metal charge on nanometer size Si channel contacts affect the Schottky barrier shape, i.e., the Schottky barrier is thinner with MS junction scaling [171]. Thus, it is not surprising for the GAA NiSi C-SSDNWMOS to exhibit near ideal SS.

Figure 6.10. Comparison of I_d and g_m for single stacked (2 wires) and side by side stacked (4 wires) GAA NiSi N-SSDNWMOS with $L_g = 90\text{nm}$.

In Figure 6.9(b), from $L_g = 105\text{nm}$ to 90nm , the DIBL value ranges from 12mV/V to 20mV/V for both N and P-SSDNWMOSs. The DIBL measured for the SSDNWMOSs is lower than values previously reported [13, 61, 65]. DIBT is caused by the drain bias thinning the Schottky Barrier at the source, which results in enhanced tunneling current [175]. In the C-SSDNWMOS, substantial barrier thinning occurs due to the nano-scale MS junction. This seems to reduce the impact of thinning by the drain potential and results in the low DIBL values observed for the C-SSDNWMOS. Also observed in Figure 6.9(b), at L_g less than 90nm , DIBL gradually increases to values greater than

100mV/V. It must be said that the onset of SCE has been observed to occur around 60nm – 90nm for SSDMOSs [13, 63].

Figure 6.10 shows the I_d - V_d of GAA NiSi N-SSDNWMOS of a single stacked NW channel (2 wires) and a side-by-side stacked NW channel ($2 \times 2 = 4$ wires). The maximum I_d is consistently higher by $\sim 2\times$ for the 4-wire configuration as compared with the 2-wire configuration, showing a linear relation between the number of wires and the corresponding maximum g_m and I_d . This demonstrates that scaling of device parameters is possible with multiple nanowire arrays.

6.4 Effect of Schottky Junction size scaling

In this section, the effects of MS junction size on the performance of SSDNWMOSs are studied by analyzing the electrical characteristics of Schottky diodes and SSDNWMOSs with varying MS junction sizes. Implantation was not carried out on the SSDNWMOSs in this section, i.e., the devices in this section do not have dopant segregated S/D junctions

6.4.1 Back-to-back diode measurements

Figure 6.11 shows the reverse biased Schottky diode characteristics of a NiSi GAA N-SSDNWMOS with $L_g = 90\text{nm}$, MS junction width (X_{MS}) = 35nm at the source, and $X_{MS} = 6\text{nm}$ at the drain. The Schottky diode characteristics are derived from the NiSi/SiNW/NiSi structure in the SSDNWMOS which can be represented by a back-to-back Schottky diode configuration. I - V measurements were done by sweeping a voltage from -2V to 2V while keeping the gate terminal open as shown in Figure 6.11(a).

Figure 6.11. (a) Schematic of the N-SSDNW MOS showing the physical difference in MS junction size at the source and drain. SEM micrograph of the schematic can be seen in Figure 3.8(a). (b) Two-terminal source to drain sweep showing rectifying characteristics. The inserts show the simplified Schottky barrier diagrams at the source and drain. V_{min} is indicated, the definition of which will be described in Figure 6.14.

When the voltage is positive, most of the voltage drop will be across the reverse biased MS junction at the drain with minimal contribution by the forward biased MS junction at the source. The measured current reflects the carrier transport across the reversed biased Schottky barrier at the drain. Conversely, when voltage is negative, the

measured current reflects the carrier transport across the reversed biased Schottky barrier at the source.

Considering that the current through both positive and negative regions are across reverse biased Schottky diodes, we would expect symmetrically low currents in the I - V curve. However, as seen in Figure 6.11(b), the I - V curves shows a rectifying behavior with the current through the drain ~ 2 orders of magnitude higher than the current through the source. This provides evidence that the current transport mechanisms through the source and drain are different as indicated in the inserts of Figure 6.11(b).

In an attempt to understand the current transport mechanisms, the experimental I - V curves were modeled using Tung's theory of inhomogeneous metal-semiconductor contacts [150]. Note that Tung's theory is a modified TE theory taking into account the presence of low barrier patches embedded in a uniformly high barrier background.

For most I - V curves in the negative I - V region, the least squares curve fitting method were successfully carried out using Tung's equation (Equation 4.3), fixing the homogeneous Schottky barrier height (ϕ_{B0}) at 0.47eV (as determined from the bulk NiSi/Si Schottky diode measurements). The results show a close fit between the experimental and simulated I - V curves as can be seen from the negative I - V region in Figure 6.11(b). The extracted low barrier patch density (p_p) and patch standard deviation (σ) have average values of $\sim 2.02 \times 10^{13} \text{ cm}^{-2}$ and $\sim 1.25 \times 10^{-4} \text{ cm}^{2/3} \text{ V}^{1/3}$, respectively. The p_p and σ are close to typical inhomogeneous Schottky barrier values, which indicate that TE is the dominant current conduction mechanism across the source Schottky barrier.

On the other hand, Equation 4.3 cannot be fitted with the data in the positive I - V region, indicating that tunneling may be the dominant current conduction mechanism in this region. Tunneling current can be expressed analytically by the TFE equation derived by Padovani *et al.* which was expressed in Section 5.3.3 (Equation 5.3). Equation 5.3 can be re-arranged in the form shown below [163].

$$J_{TFE} = \frac{A^*T}{k} \sqrt{\pi E_{00} q \left[V + \frac{\phi_b}{\cosh^2(E_{00}/kT)} \right]} \exp\left(\frac{-q\phi_b}{E_0}\right) \exp\left(\frac{qV}{\varepsilon'}\right) \quad (\text{Equation 6.2})$$

where

$$\varepsilon' = \frac{E_{00}}{(E_{00}/kT) - \tanh(E_{00}/kT)} \quad (\text{Equation 6.3})$$

and $E_0 = E_{00} \coth(qE_{00}/kT)$, E_{00} is the tunneling potential of an electron across a Schottky barrier and equivalent to $\hbar/2 [N_d/m_h \varepsilon_s \varepsilon_0]^{1/2}$.

For most I - V curves in the positive I - V region, the least squares curve fitting method were successfully carried out using Equation 6.2. Φ_b was fixed 0.45eV, which is the bulk NiSi/ n -Si value, N_d was fixed at $1 \times 10^{15} \text{cm}^{-3}$, which is the SOI background doping concentration, and E_{00} was the curve fitting variable. For the particular I - V curve shown in Figure 6.11(b), the simulated curve shows a close fit to the experimental curve with an extracted E_{00} of $\sim 23 \text{ meV} \approx kT/q = 26 \text{ meV}$ (at 300K). A value of E_{00} close to kT/q confirms that the current conduction mechanism through the reverse biased drain Schottky barrier is TFE [51].

Figure 6.12. (a) Diode I - V in TFE region (negative I - V region) showing increasing I with decreasing X_{MS} . (b) E_{00} against X_{MS} , showing increasing E_{00} with decreasing X_{MS} .

In addition, by fitting Equation 6.2 to the negative I - V region (TE region), the extracted E_{00} is $\sim 3\text{meV} < kT/q$, confirming that the current conduction mechanism through the source Schottky barrier is TE, consistent with the curve fitting results by Tung's theory of inhomogeneous MS junctions. As V becomes more positive ($V < -0.75\text{V}$), most of the voltage drop is across the SiNW channel and the current increases linearly with voltage.

By using Equation 6.2 to examine the current conduction through the drain Schottky barrier at the negative voltages for various N-SSDNWMOSs with various X_{MS} , we are able to relate the current conduction with X_{MS} . Note that at the positive voltages, the current conduction mechanism is TFE. As can be seen from Figure 6.12(a), the current density (measured at $V = -0.6V$) through the drain Schottky barrier increases from $\sim 2.4 \mu A/\mu m$ to $\sim 8.5 \mu A/\mu m$ to $\sim 24.8 \mu A/\mu m$ as X_{MS} decreases from 25nm to 15nm to 6nm, respectively.

To quantitatively study the current density across the whole range of X_{MS} , we extracted E_{00} using Equation 6.2 for various X_{MS} values. The results show increasing tunneling potential from 7meV to 21meV with decreasing X_{MS} from 35nm to 6nm. This confirms that the tunneling current increases with decreasing X_{MS} .

Figure 6.13. Plot of ϵ' against kT/q for a particular GAA NiSi N-SSDNWMOS. Experimental ϵ' ($\square$) extracted from the I - V curve using Equation 6.2. Theoretical ϵ' (-) curve obtained from determining ϵ' at 300K and varying the temperature in Equation 6.2. The error bars indicate fitting errors.

In order to determine the validity of using the TFE equation (Equation 6.2) with regards to the experimentally obtained results, the experimental results were checked against the theoretical results.

By applying Equation 6.2, i.e. $J_{TFE} \propto \exp(qV/\varepsilon')$ to the experimental temperature dependent I - V curves, the actual ε' was obtained from the slope of the J_{TFE} against V curve and plotted as squares in Figure 6.13. By applying Equation 6.3, i.e., $\varepsilon' = E_{00}/((E_{00}/kT) - \tanh(E_{00}/kT))$, and by substituting T values, we obtain the theoretical ε' which is plotted as a dotted line in Figure 6.13. As can be seen, the curves show a fit between the theory and experiment within an experimental error which proves the validity of applying the TFE equation to the GAA NiSi N-SSDNW MOS I - V curves.

Figure 6.14. Theoretical plot of V_{min} versus X_{MS} . V_{min} extracted from the substituting the values of E_{00} from Figure 6.12 into Equation 6.3.

The minimum applied voltage required to induce TFE (V_{min}) can be expressed as follows [163].

$$V_{\min} > \Phi_{\text{beff}} + \frac{3E_{00} \cosh^2(E_{00}/kT)}{2 \sinh^3(E_{00}/kT)} \text{ (Equation 6.4)}$$

From Figure 6.11, by using $\Phi_{\text{beff}} = 0.45\text{eV}$, $E_{00} = 0.023\text{eV}$, and $T = 300\text{K}$, the calculated $V_{\min} = -0.54\text{V}$. This is approximately the “turning point” in the I – V curve in Figure 6.11.

When Equation 6.4 was applied to the ErSi_{2-x} N-SSDNWMOS I – V curves (Figure 5.6 in Chapter 5.3.3), using $\Phi_{\text{beff}} = 0.8\text{eV}$ (which is the bulk ErSi_{2-x}/p -Si value) and $E_{00} = 0.005\text{eV}$ (extracted from Figure 5.6), the calculated $V_{\min} = 1.85\text{V}$ which explains the larger voltages needed to induce TFE for the ErSi_{2-x} SSDNWMOSs.

By plotting the theoretical $V_{\min}$ using the extracted values of E_{00} from Figure 6.12, the “turning point” in the diode I – V and hence the SSDNWMOS V_t can theoretically be reduced with X_{MS} as shown in Figure 6.14. This provides a means of tuning V_t if X_{MS} can be controlled precisely. Note that $V_{\min}$ is derived from the diode sweep and is not exactly equivalent to V_t (which depends on gate potential). However, the smaller the value of $V_{\min}$ is, i.e., the smaller the voltage whereby TFE starts to dominate from TE, the lower V_t will be.

The analytical formula by Padovani *et al.* describes increased current density in terms of an increased tunneling potential dependent only on temperature, voltage bias and semiconductor doping density for a particular MS system [163]. However, in order to understand increased tunneling potential and hence increasing current density with reduced X_{MS} , the model proposed by Smit *et al.* to describe the Schottky barrier shape in ultra-small Schottky diodes was adopted [171]. They propose that thinner Schottky barriers are formed, with the consequence of greatly enhanced tunneling current, due to electrostatic effects in small diodes.

In a ‘large’ diode, the extent of space charge layer in the semiconductor that compensates the surface charge in the metal is set by the concentration of free carriers and doping atoms. The width of the space charge layer and thus the Schottky barrier thickness, is equal to the depletion width (W_D) and can be expressed as follows [51].

$$W_D = \sqrt{\frac{2\epsilon_s}{qN_d} \left(\psi_{bi} - V - \frac{kT}{q} \right)} \quad (\text{Equation 6.5})$$

where ψ_{bi} is the built in potential, and V is the applied voltage. For the NiSi/*p*-Si system, using $N_d = 1 \times 10^{15} \text{ cm}^{-3}$, and $\psi_{bi} = 0.3\text{eV}$ from *C-V* measurements, the calculated $W_D \sim 587 \text{ nm}$ as determine from Equation 6.5. For ‘small’ diodes of finite size where $X_{MS} < W_D$, the potential in the semiconductor is due to the charged metal only, with negligible effect by the semiconductor space charge. Gauss’s law is used, which states that a charged object (metal) in a dielectric medium (semiconductor in this case) gives rise to a potential which varies with size and distance, $V(x) \propto \text{size}/x$.

The Schottky barrier shape in the semiconductor can be obtained by solving the Poisson equation in the semiconductor and can be expressed as follows [171].

$$\frac{q\psi(x)}{kT} = \frac{1}{2L_D} \left[(X_{MS} + W_D)^2 - \frac{2(X_{MS} + W_D)^3}{3(X_{MS} + x)} - \frac{(X_{MS} + x)^2}{3} \right] \quad (\text{Equation 6.6})$$

where L_D is the debye length given by $\sqrt{\epsilon_s kT / (q^2 N_d)}$, $\psi(x)$ is the channel potential from S/D to channel, and x is the distance from the S/D into the SiNW channel.

Figure 6.15(a) shows a plot of $\psi(x)$ against x for various X_{MS} showing the differences in Schottky barrier shapes with X_{MS} of 6nm, 35nm and 600nm. For $X_{MS} = 600\text{nm}$, equivalent to the case of ‘large’ diodes ($X_{MS} > W_D$), the width of the Schottky barrier (X_{SB}), which is determined from the value of x at $\psi(x)$ full-width-half-maximum, is

138nm. For $X_{MS} = 35\text{nm}$ and 6nm , X_{SB} have reduced to 34nm and 10nm respectively. Figure 6.15(b) shows the plot of X_{SB} for X_{MS} in the ‘small’ diode regime ($X_{MS} < W_D$) from $0 - 200\text{nm}$ showing decreasing X_{SB} with decreasing X_{MS} . Certainly, the enhanced tunneling current observed in Figure 6.12 can be understood on the basis that the tunnel potential increases because of a reduction of X_{SB} .

Figure 6.15. (a) Plot of $\Psi(x)$ versus x ($X_{MS} = 0$ is at the MS junction) showing thinner barrier with decreasing X_{MS} . (b) Plot of X_{SB} against X_{MS} .

6.4.2 Transistor Characteristics

The impact of a smaller X_{SB} with X_{MS} scaling can also be observed in the transistor characteristics as will be shown in this section.

Figure 6.16. I_d - V_g of GAA NiSi P-SSDNWMOS with $L_g = 90\text{nm}$, and (a) drain $X_{MS} = 6\text{nm}$, and (b) source $X_{MS} = 35\text{nm}$.

Figure 6.16 shows the I_d - V_g characteristics of a NiSi GAA P-SSDNWMOS with $L_g = 90\text{nm}$, and (a) $X_{MS} = 6\text{nm}$ at the drain, and (b) $X_{MS} = 35\text{nm}$ at the source. Note that the I_d - V_g curve for Figure 6.16(a) is obtained by grounding the drain, and biasing the source, while the I_d - V_g curve for Figure 6.16(b) is obtained by grounding the source, and biasing the drain.

By examining the I_d - V_g plots, the transistor characteristics extracted for the $X_{MS} = 6\text{nm}$ device are I_{on}/I_{off} ratio $\sim 5 \times 10^5$ measured at $V_d = 50\text{mV}$, SS $\sim 61\text{mV/decade}$, $V_t = -0.3\text{V}$, and DIBL $\sim 29\text{mV/V}$. For the $X_{MS} = 35\text{nm}$ device, the values extracted are I_{on}/I_{off} ratio $\sim 7 \times 10^4$ measured at $V_d = 50\text{mV}$, SS $\sim 81\text{mV/decade}$, $V_t = -0.34\text{V}$, and DIBL $\sim 73\text{mV/V}$.

Clearly, the $X_{MS} = 6\text{nm}$ device showed superior transistor characteristics compared to the $X_{MS} = 35\text{nm}$ device. The main improvements observed for the $X_{MS} = 6\text{nm}$ device are (1) increased current resulting in a larger I_{on}/I_{off} ratio, (2) more responsive current modulation to V_g , leading to a smaller SS, (3) faster onset of tunneling leading to a smaller V_t , and (4) smaller DIBL as X_{SB} is mainly affected by X_{MS} as compared to V_d as explained in Section 6.3.2.

Figure 6.17. (a) g_m against V_g showing higher peak g_m with a steeper slope for $X_{MS} = 6\text{nm}$ compared with $X_{MS} = 35\text{nm}$ device. (b) SS against X_{MS} showing decreasing SS with decreasing X_{MS} . The error bars indicate fitting error.

Points (1) and (2) (the increased and more responsive current to gate control with decreasing X_{MS}) can be more readily observed in Figure 6.17. Figure 6.17(a) shows the g_m comparison of the 2 devices ($X_{MS} = 6\text{nm}$ vs. $X_{MS} = 35\text{nm}$) measured at $V_d = 50\text{mV}$. The g_m curves indicate that the smaller X_{MS} device is more responsive and has a larger peak g_m than the larger X_{MS} device, in agreement with the diode results in Figure 6.12. Figure 6.17(b) shows the plot of SS against X_{MS} measured at $V_d = 50\text{mV}$ for 4 different X_{MS} values. The smaller SS with smaller X_{MS} shows that the thinner Schottky barrier is more responsive to V_g .

Figure 6.18. Temperature Dependent I_d - V_g measured at $V_d = 50\text{mV}$ from 298K – 348K of GAA NiSi P-SSDNWMOS with $L_g = 90\text{nm}$, and metal semiconductor junction sizes (a) $X_{MS} = 6\text{nm}$, and (b) $X_{MS} = 35\text{nm}$.

In order to further investigate the impact of X_{MS} scaling on the more responsive current to V_g control, temperature dependent I_d - V_g were carried out on the (a) $X_{MS} = 6\text{nm}$ and (b) $X_{MS} = 35\text{nm}$ devices, as shown in Figure 6.18, in order to extract Φ_{beff} against V_g .

Three main observations can be seen from the I_d - V_g curves. Firstly, the increase in the I_d with increasing temperature is due to an increase in the TE and TFE current conduction mechanisms, both of which increase with temperature. Secondly, the I - V curve shows three regions as can be seen from the change in slopes which correspond to TE region, TFE region and finally R-limited (by SiNW) region. This sequential TE and TFE was described in Chapter 5.3.2 for the BG ErSi_{2-x} SSDNWMOS and is a characteristic of SSDMOS. Thirdly, the V_g where TE transits to TFE is less negative for the $X_{MS} = 6\text{nm}$ device compared to the $X_{MS} = 35\text{nm}$ device (0.1V versus 0.05V). The less negative V_g is due to the fact that carriers can more readily tunnel through a MS junction with a smaller X_{SB} which is in turn dependent on X_{MS} as seen in Figure 6.15. Since X_{SB} is modulated by the V_g in the SSDNWMOSs, a smaller V_g is required to modulate the channel potential for tunneling to occur. Hence, the $X_{MS} = 6\text{nm}$ device has a lower TE to TFE transition V_g .

Figure 6.19. Φ_{beff} against V_g of NiSi GAA P-SSDNW MOS with $L_g = 90\text{nm}$. (a) $X_{MS} = 6\text{nm}$, and (b) $X_{MS} = 35\text{nm}$. The Φ_{beff} is not plotted for the increasingly positive V_g due to uncertainty in Arrhenius plots. The error bars indicate fitting error.

Using the TE equation, $I_d = AA^*T^2 \exp(-q\Phi_{beff}/kT)$ (Equation 4.1) on the measured I_d for each value of V_g in Figure 6.18, the Arrhenius plot ($\ln I_d/T^2$ vs. $1/T$) was graphed and from its slope, Φ_{beff} was extracted for each value of V_g , and is shown in Figure 6.19. It must be mentioned that the Φ_{beff} extracted is the effective barrier height taking into account both TE and TFE, and thus is a measure of the height and shape of the barrier as opposed to just solely the barrier height.

The Φ_{beff} shows a direct relation to the I_d - V_g curve in Figure 6.18 with the corresponding three distinct regions; TE during low V_g , followed by TFE in the intermediate V_g and finally, at increasingly negative V_g , the change in Φ_{beff} saturates as the current is no longer limited by the Schottky barriers at the S/D but with the resistance of the SiNW channel. For both the devices, V_t occurs when Φ_{beff} is at $\sim 0.12\text{eV}$ and this corresponds to $V_g = -0.25\text{V}$ for $X_{MS} = 6\text{nm}$ device and $V_g = -0.37\text{V}$ for the $X_{MS} = 35\text{nm}$

device. Therefore, the V_t would be lower if Φ_{beff} reduction with V_g is at a greater rate in the subthreshold region. Note that the subthreshold region comprises both the TE dominated and TFE dominated regions.

In the TFE dominated region, it can be clearly observed that the $X_{MS} = 6\text{nm}$ device's Φ_{beff} modulation is greater than that of the $X_{MS} = 35\text{nm}$ device. This greater rate of change is due to the greater rate change of X_{SB} with the same applied V_g bias, and will result in increased tunneling and a faster onset of tunneling with the same applied V_g .

Figure 6.20. Φ_{beff} modulation by V_g against X_{MS} showing increasing modulation with decreasing X_{MS} . Error bars indicate fitting error. Φ_{beff} modulation obtained from the slope of Figure 6.19.

In the TE dominated region, the $X_{MS} = 6\text{nm}$ device's Φ_{beff} modulation also changes at a greater rate. From Figure 6.19, when $V_g = 0.22\text{eV}$, $\Phi_{beff} = 0.18\text{eV}$ for the $X_{MS} = 6\text{nm}$ device, whereas $\Phi_{beff} = 0.22\text{eV}$ for the $X_{MS} = 35\text{nm}$ device. This means that for the same increase in V_g , the channel potential (conduction band profile) has a greater rate of

change, leading to a smaller Schottky barrier height at the MS junction. The improved modulation in this region is due in part to the improved electrostatics on a smaller body, as well as increased tunneling through the smaller X_{MS} . Note that a small amount of tunneling occurs in this region as well. The more responsive Φ_{beff} modulation results in the greater g_m and smaller SS seen in Figure 6.17.

In order to illustrate the size effects of Φ_{beff} modulation with more clarity, Φ_{beff} modulation in both the TE and TFE region were plotted against X_{MS} in Figure 6.20. Each I_d - V_g curve yields two slopes; one from the TE region, as well as one from the TFE region. For both the TE and TFE regions, the Φ_{beff} modulation decreases with increasing X_{MS} . This is due to the more responsive Schottky barrier control of a smaller X_{MS} .

6.5 Summary

We fabricated GAA ErSi_{2-x} N-SSDNWMOS with excellent electrical characteristics (I_{on}/I_{off} ratio of $\sim 1.1 \times 10^5$, SS = 65mV/decade – 87mV/decade, DIBL = 21.3mV/V to 45mV/V), with short channel performance equal to or better than reported RESi_{2-x} based SSDMOS. In addition, GAA PtSi P-SSDNWMOSs with excellent electrical characteristics were fabricated for complementary MOSFET operation with ErSi_{2-x} N-SSDNWMOS. The extracted P-SSDNWMOS characteristics are comparable or better than the currently reported PtSi P-SSDMOSs. NiSi GAA C-SSDNWMOSs were also fabricated with near ideal SS ~ 60 mV/decade, DIBL ~ 10 mV/V, and I_{on}/I_{off} ratio $\sim 2.28 \times 10^5$. The improved performance of the SSDNWMOSs is a result of (1) excellent GAA electrostatics on a narrow SiNW body, (2) increased tunneling current, and (3) a more

effective Φ_{beff} modulation. The latter two occur as a result of scaling of the MS junction size, i.e., SSDMOS performance improves as MS junction size reduces.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

ErSi_{2-x} films formed by RTA of Er films on Si(001) have been characterized. The ErSi_{2-x} films is highly defective, and exhibit pyramidal structural defects that have not been previously reported. The defects are detrimental to electrical characteristics of devices and are a source of leakage currents. In order to minimize the defects for better device performance, the origin of defect formation is investigated. It was found that the structural defect forms in order to relax epitaxial misfit stresses through a buckling process. The buckling process occurs simultaneously with separation of the film from the substrate below the pyramidal defect. Silicon diffusion, subsequent to buckling can fill in the space between the buckled film and substrate. Depending on the size of the defect and the annealing time, this can lead to complete filling or partial voids inside the pyramidal defects.

Ar plasma cleaning and Si pre-amorphization implants were then employed to amorphize Si(001) substrate prior to Er film deposition. Improved electrical performance was observed for the Ar plasma cleaned Si diodes due to the removal of structural defects even though the ErSi_{2-x} film have poorer interfaces and are less textured. The PAI Si diodes show degraded performance due to ion induced damage even though structural defects were eliminated. *In-situ* capping layers of TiN and TiN/Ti were also applied prior to Er deposition without substrate amorphization. The TiN and TiN/Ti cappings effectively prevent oxidation of highly reactive Er layers. The capping layers also serve to partially relieve the compressive stresses experienced by the ErSi_{2-x} films during RTA

which reduces structural defect density. The TiN/Ti capped samples was found to have the lowest defect density.

Although the Ar plasma cleaned Si diodes have more consistent Schottky barrier height and ideality factor n , they are inhomogenous due to the less textured ErSi_{2-x} film. This results in a lower Φ_b , and a higher n as compared to the TiN/Ti capped samples. Hence, TiN/Ti capping layer are determined to be suitable for ErSi_{2-x} based silicon nanowire SiNW transistors.

Back-gated SSDNWMOS with reduced dimensions $\sim 8\text{nm}$ as the channel body and ErSi_{2-x} as the S/D metal silicide were fabricated using a ‘top-down’ CMOS compatible technology. The devices exhibited Schottky barrier transistor behavior with high I_{on}/I_{off} ratio $\sim 10^5$ and high drive current $\sim 900\mu\text{A}/\mu\text{m}$ because of the low Φ_b of $\text{ErSi}_{2-x}/n\text{-Si}$ and the improved electrostatics on the $\sim 8\text{nm}$ wire channel.. These results are significantly better than previously reported Schottky barrier MOSFETs without barrier modified junctions. The devices exhibited ambipolar transfer characteristics with sequential thermionic/thermionic-field characteristics for a positive gate bias and only tunneling characteristic for a negative gate bias. The carrier transport is mainly determined by the MS interface instead of the channel body. Relatively large values of SS and DIBL are due to the thick gate oxide.

Two terminal measurements indicate that the ρ_{SiNW} is relative low and $N_{a,\text{SiNW}}$ is relatively high which indicates that a surface conduction mechanism may be present in the ErSi_{2-x} SSDNWMOS. Device performance is shown to be strongly affected by device physical structure, e.g., multiple SiNW channels, $\text{ErSi}_{2-x}/\text{Si}$ junction size and S/D

silicided depth. Φ_b modulation by the gate potential is shown to be extremely responsive due to the excellent electrostatic control of the SSDNWMOS S/D Schottky barrier.

GAA N-SSDNWMOS with reduced SiNW dimensions of ~5nm were also fabricated using ErSi_{2-x} as the S/D metal silicide. Excellent electrical characteristics were observed with I_{on}/I_{off} ratio of $\sim 1.1 \times 10^5$, SS = 65mV/decade and DIBL = 21.3mV/V. The ErSi_{2-x} N-SSDNWMOSs are comparable or better than currently reported state-of-the-art RE silicide based SSDMOSs. GAA PtSi P-SSDNWMOS were also fabricated in order to achieve complementary transistor action.

In addition, GAA NiSi P and N-SSDNWMOSs were fabricated with near ideal SS ~60mV/decade, DIBL ~10mV/V, and I_{on}/I_{off} characteristics. The excellent transistor characteristics were achieved without the use of barrier modification techniques. From the Schottky diode and transistor characterization, it was found that the excellent characteristics are due to the excellent electrostatics of the GAA structure on the nanometer sized channel, and Schottky barrier thinning for nano-sized MS junction which results in increased tunneling current, and a more efficient Φ_b modulation.

7.2 Recommendations for Further Research

Several areas of research related to SSDNWMOSs should be studied for possible integration in the semiconductor industry. These include:

- 1) Additional electrical measurements should be carried out in order to further investigate the intrinsic properties of SSDNWMOSs. By using C-V measurements, possible SiNW defects, gate oxide charges could be identified and quantified. Mobility, as well as ballistic efficiency in the SiNW channel can be calculated

from the C-V curves. The obstacle to C-V measurement is due to the absence of a suitable nanowire array for the measurements. A SiNW array is required as a single SiNW capacitance is in the range of $\sim 10^1$ aF, based on the ideal cylindrical conductor model. Low temperature measurements are required so as to minimize inaccuracies from thermal fluctuations which would cause large errors if the Φ_b is low. Quantum effects like coulomb blockade oscillations are more readily observed at low temperatures, i.e., kT has to be substantially smaller than an addition of one electron to the quantum dot (~ 100 meV for ~ 10 nm island). Additional measurements would also include radio frequency (RF) measurements to determine SSDNWMOSs' cut-off frequency and hence, its suitability for RF applications and reliability and failure analysis measurements to determine SSDNWMOSs' failure modes etc.

2) Strain as a method of Φ_b lowering could be carried out in together with the SSDNWMOS architecture. The strain could be achieved by tensile or compressively strained capping nitride by the addition of minimal wafer processing steps. Furthermore, SiGe S/D stressors could be formed in place of the Si S/D by the epitaxial regrowth of deposited SiGe on recessed Si S/D pad or other methods. In addition, a germanide or germanosilicide on Ge or SiGe S/D would also result in a smaller Φ_b . As Ge concentration increases, due to valence band edge E_v position moving up, as well as a larger germanide work function, the Schottky barrier height of a germanide/Ge MS junction will be smaller than silicide/Si MS junction. Further effective Φ_b reduction with reduction in MS dimensions would result in a much improved drive current.

3) A Schottky S/D architecture could be incorporated to non-volatile memory based on MOSFETs with SONOS as the gate stack. The abrupt voltage drop across a MS

junction results in high electric fields at the source. Carriers injected from the source are accelerated by the electric field and will result in higher carrier velocity. This could provide for improved hot carrier injection into the SONOS gate dielectric. This project has shown the improved injection efficiency of when Schottky junctions are scaled. A SONOS flash memory utilizing a SiNW body in conjunction with MS junctions could be investigated for extremely scaled high performance non-volatile memory devices. In addition, Si/Ge nanocrystals could be implanted into the ONO layers to further improve charge storage.

4) Quantum device simulation using the non equilibrium greens function should be attempted to model the electrical transport of SSDNWMOSs. In addition, ab initio simulations using density functional theory may be used to model the electronic properties of the nanoscale MS interface.

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LIST OF PUBLICATIONS

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