A unity power factor current injection technique for three phase controlled bridge rectifier

Eka Firmansyah

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**A Unity Power Factor
Current Injection Technique For Three Phase
Controlled Bridge Rectifier**

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School of Electrical & Electronic Engineering

A Thesis submitted to the Nanyang Technological University
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SUMMARY

Over the last decade, power electronic converters are widely applied in industrial, commercial, residential, aerospace, utility, and military applications. Several factors like lightweight, compact size, low-cost, compatibility with digital control, and energy saving, support the widespread of its application.

A rectifier that converts AC to DC is included in this task. In applications requiring power control and large power handling capability, i.e. aluminum smelter, HVDC, high power DC drives, a three-phase controlled rectifier is the main player among rectifiers. The three-phase controlled rectifier is a mature application. Due to its long usage, its benefits are well understood and so are its drawbacks. Two of its drawbacks are high input current harmonics and low input power factor. Those drawbacks affect the input power quality of the rectifier.

As power quality has become a major issue in recent years, authorities have launched several regulations like IEEE-519 about harmonic emission. Several proposed methods to improve the waveform and power factor of the controlled rectifier have been investigated. However, these methods lack of several power electronic features such as, lightweight, low cost, and high efficiency.

A method, called third harmonic current injection, has been proven very effective in solving the current harmonic problem of a three-phase diode rectifier. The method has some good features i.e. high efficiency, low cost, simple upgrading to the current three-phase rectifier, and lightweight. A three-phase controlled rectifier has similar but not identical problem characteristics with a three-phase diode rectifier. This led to an investigation of the third harmonic current injection method on a three-phase controlled rectifier.

Some prior researches were conducted in this area. Those resulted in power factor improvement and lower content of current harmonic on the input current of a three-phase controlled rectifier. Investigation of the technique and benefits of third harmonic current injection on a three-phase controlled rectifier are the objective of this research. The research emphasis is on achieving a high input power quality three-phase controlled rectifier that is characterized by low cost, lightweight, capability to simple upgrading of existing controlled rectifier, and high efficiency. Analytical background work, digital simulation and hardware verifications are conducted. Those efforts resulted in a new current injection topology. The topology consists of a current processor that is simple, lightweight, and robust. A digitally controlled current injector that is transformerless, lightweight, and low-cost also characterizes it.

Two methods have been adopted to investigate the current injection technique; MATLAB based simulation and the experiment results. MATLAB application is used

to verify the theoretical idea and predicted result. It is also used to preview the voltage and current condition that should be anticipated during a real application of the current injection scheme into a three-phase controlled rectifier. In MATLAB environment, a real circuit was built and the circuit performance could be seen. An experiment work based on a real 1kW three-phase rectifier has also been conducted to verify the MATLAB simulation result.

Result shows that the proposed scheme yields encouraging results when operating in zero to fifty-degree delay angle range. Input current THD can be reduced from 30% without the proposed scheme to about 15% when operates at fifty degree delay angle (worst-case condition). While operates at lower delay angle, input current THD of the rectifier with the proposed scheme decreases.

It concludes that through its simplicity, lightweight, and low cost features of the proposed scheme, the proposed scheme improves the input power quality of a three-phase controlled rectifier.

1 INTRODUCTION

1.1 Motivation

Over the last decade, power electronic converters are widely applied in industrial, commercial, residential, aerospace, utility, and military applications. Several factors like lightweight, compact size, low-cost, compatibility with digital control, and energy saving, support the widespread of its application [1,2].

The tasks of power electronic devices are to process and control the flow of electric energy. It converts voltage and current in a form that is optimally suited for user load. A rectifier that converts AC to DC is included in this task. In applications requiring power control and large power handling capability, i.e. aluminum smelter, HVDC, high power DC drives, a three-phase controlled rectifier is the main player among rectifiers [3].

The three-phase controlled rectifier is a mature application. It was started about 1930 when grid-controlled mercury arc rectifier was invented. The invention of thyristor in 1957 led to further investigation [4]. Due to its long application time, its benefits are well understood as well as its drawbacks. Generate high current harmonic and have low input power factor are two major drawbacks of it. The drawbacks impact on reducing its input power quality [5].

The number of three-phase controlled rectifier application has increased recently. The increase affects the AC power quality by introducing large current harmonic on it. As power quality has become a major issue in recent years, authorities have launched several regulations like IEEE-519 about harmonic emission. Series connection, parallel connection, static power factor and filtering, and sequential operation of controlled rectifier are several proposed method to improve the waveform and power factor of the controlled rectifier that have been investigated [4]. However, these methods lack of several power electronic features such as, lightweight, low cost, and high efficiency.

A method called third harmonic current injection has been proven effective in solving the current harmonic problem of a three-phase diode rectifier [1,6-21]. The method has some features i.e. high efficiency, low cost, simple upgrading to the current three-phase rectifier, and lightweight [12].

A three-phase controlled rectifier has similar but not identical problem characteristics with a three-phase diode rectifier. This led to an investigation of the third harmonic current injection method on a three-phase controlled rectifier.

Some prior researches were conducted in this area [20]. That resulted in power factor improvement and lower content of current harmonic on the input current of a three-phase controlled rectifier. However, bulky item, tendency to be a high cost solution,

and weight problem were still present. Overall characteristics of the converter after application of the method also have not been investigated yet.

It is still required to look into an alternative scheme to rid the bulky equipments, lowering the cost, and solving the weight problem. However, thorough research about overall rectifier characteristics after application of the new method is also needed.

1.2 Objective

Investigate the technique and benefits of third harmonic current injection on a three-phase controlled rectifier are the objective of this research. The emphasis is on achieving a high input power quality three-phase controlled rectifier that is characterized by low cost, lightweight, capability to simple upgrading of existing controlled rectifier, and high efficiency. Analytical background work, digital simulation and hardware verification are conducted.

1.3 Contribution

The following will summarize the contributions of this work:

1. Define a better method than existing methods [20] in terms of input power quality, cost, and weight to upgrade the existing rectifier based DC drives.
2. Some detailed analytical expression governing the three phase-controlled rectifier input current and PF are derived based on the proposed circuit.

3. A control method is proposed which enables the three-phase controlled rectifier to achieve a high power factor under a wide load and delay angle (α) range.

1.4 Organization of the Thesis

This report is organized as follows,

Chapter 2 gives a brief working principle of the three-phase controlled rectifier and reviews the input current harmonic during its operation.

Chapter 3 discusses the application of the current injection methods on a three-phase rectifier and gives a brief discussion of its application on a three-phase controlled rectifier.

Chapter 4 analyzes the characteristics of a recent generic topology and presents a novel control technique to achieve optimum current and power factor of the three-phase controlled rectifier.

Chapter 5 presents and analyzes hardware modeling and the hardware experimental results.

Finally, **chapter 6** presents the conclusions and future work.

2 THREE-PHASE CONTROLLED RECTIFIER

A brief working principle of a three-phase controlled rectifier is described here to define the problems faced. The working principle is also important for providing a foundation for the solution that will be presented in the next chapter.

2.1 Introduction

The three-phase controlled rectifier is one of the most widely used rectifiers. Its simplicity, maturity, high efficiency, high power handling, robustness and light weight are factors that boost its popularity [3].

A three-phase controlled rectifier consists of six thyristors connected to a three-phase line source (Figure 2.1). In practice, a delta-wye transformer may be added between the three-phase line source and the three-phase controlled rectifier [4]. Its functions are:

1. to provide a specific DC output voltage by providing a specific transformer windings ratio,
2. to reduce the effects of the rectifier on the a.c. system voltage waveform,
3. to provide electrical isolation of the DC output from the a.c. system.

Later in this thesis, controlled rectifier will be presented without the presence of a delta-wye transformer for the simplicity.

Figure 2.1 A three-phase controlled rectifier

The active components of a three-phase controlled rectifier are the thyristors (Figure 2.2). Table 2.1 lists the general characteristics of those thyristors [1]. As a unidirectional device, thyristor's current can only flow in one direction, which is from anode to cathode. Therefore, current flow in reverse direction is not possible.

Figure 2.2 Schematic symbol of a Thyristor

Output voltage controllability is one advantage of the three-phase controlled rectifier. It can be varied by controlling the delay or firing angle (α) of the thyristors. A thyristor is turned on by applying a short pulse to its gate and turned off due to line

commutation [16, 17]. In a highly inductive load, it is turned off if another thyristor in the rectifier is turned on during the negative cycle of input voltage [1].

Figure 2.3 Two quadrant operation of a three-phase controlled rectifier

A three-phase controlled rectifier operates at α higher than 90° may cause its DC output voltage become negative when it is loaded with a highly inductive load. However, It is dictated by the thyristor characteristics, current in the rectifier only flows in a positive direction that is from anode to cathode and not in opposite direction. Thus, the working area of the controlled rectifier is only on quadrants one and two (Figure 2.3).

Theoretically, a three-phase controlled rectifier operates at very high efficiency. Efficiency of above 95% is possible in its application [1,2,4]. Its simple control circuit and large power handling make the three-phase controlled rectifier the only player in megawatt power level variable speed drives [1]. However, it has the well-

documented drawbacks of poor input power factor and large input line currents harmonic [4].

Table 2.1 Common Thyristor Characteristics

Pulse Gating Controlled On- Naturally commutated Bipolar Voltage Unidirectional Current			
Voltage/Current Rating	Upper Frequency (Hz)	Switching Time (μs)	On-State Resistance (Ω)
6500 V / 4200 A	60	100-400	0.58m
2800 V / 1500 A			0.72m
5000 V / 4600 A			0.48m
5000 V / 3600 A			0.50m
5000 V / 5000 A			0.45m
2800 V/1850A	20k	20-100	0.87m
1800 V/2100A			0.78m
4500 V/3000A			0.5m
6000V/2300A			0.52m
4500V/3700A			0.53m

2.2 Input Current of a Three-Phase Controlled Rectifier

2.2.1 Zero delay angle

Ideally, the input voltage of a three-phase controlled rectifier is a balance three-phase voltage source. It can be stated by equations (2.1) to (2.3) or by vectors representation on Figure 2.4.

$$v_a = V \sin(\omega t + 0^\circ)$$
 (2.1)

$$v_b = V \sin(\omega t + 120^\circ)$$
 (2.2)

$$v_c = V \sin(\omega t - 120^\circ)$$
 (2.3)

Each thyristor in a three-phase controlled rectifier conducts for 120° period. Referring to Figure 2.1, the upper group (T_1 , T_3 , and T_5) conducts on positive cycle, and the lower group (T_2 , T_4 , and T_6) conducts on negative cycle.

Figure 2.4 Three-phase input voltage vector representation

Figure 2.5 describes the conduction period of the input voltage vectors. The vectors deliver currents while they are on the P or N region. Each region is 120° wide or $\frac{1}{3}$ of a complete cycle period. Thus, in a complete cycle, a voltage vector is in conduction state for $\frac{2}{3}$ period and leave on un-conducting state for $\frac{1}{3}$ period (equation (2.4) to (2.6)).

$$T_P = T_N = T_{off} = \frac{1}{3} T \quad (2.4)$$

$$F_P = F_N = F_{off} = 3F \quad (2.5)$$

$$T_{on} = T_P + T_N = \frac{2}{3} T \quad (2.6)$$

Where, F is the input voltage frequency, and T is $\frac{1}{f}$

The instantaneous input current of a three-phase controlled rectifier is the same as the instantaneous current that is flowing on the DC bus side. Meanwhile, the instantaneous DC bus current is a function of instantaneous DC bus voltage. The voltage is actually a vector summation of two vectors that is active on the P and N region. Consider a state that V_a is currently on P region, V_b is starting to enter N region, and V_c is leaving the conduction state (Figure 2.6 (a)), the instantaneous DC bus voltage is V_{ab} , that is 30° lagging of V_a . Its magnitude is $\sqrt{3} V_a$. In general

$$V_{ab} = V_L = 2 \cdot V_s \cos(30) = \sqrt{3} V_s \angle -30 \quad (2.7)$$

$$I_L = \frac{V_L}{Z} \quad (2.8)$$

Figure 2.5 Input voltage vectors and the conduction area

With V_L is the line to line voltage or the instantaneous load voltage, V_s is the line to neutral voltage, I_L is the load current, and Z is the DC bus load.

Figure 2.6 Instantaneous DC bus vector voltage

The V_{ab} voltage vector that forms the voltage on the load side lasts until V_a is leaving the conduction state and V_c is entering the P region (Figure 2.6 (b)). Hence, the V_a - V_b combination lasts for 60° (Figure 2.6 (c)).

There are six voltages voltage vectors, V_{ab} , V_{ac} , V_{ba} , V_{bc} , V_{ca} , and V_{cb} . Each has period of,

$$T_{V_L} = \frac{60^\circ}{360^\circ} T = \frac{1}{6} T \quad (2.9)$$

In terms of frequency

$$F_{V_L} = 6F \quad (2.10)$$

Where T_{V_L} and F_{V_L} are period and frequency of the above combined vector respectively.

Based on above facts, a three-phase controlled rectifier depicted on Figure 2.1 has an input current as shown in Figure 2.7. It is evident that the input current period is segmented by 120° while its magnitude is a function of the DC bus voltage and its load. In a purely resistive load, without any inductance on the DC bus, input current looks like on Figure 2.7.(a). While in practical application, it is normally loaded with highly inductive load hence current will be purely DC current without any ripple (Figure 2.7.(b)).

Further examination on Figure 2.7, even though it is not continuously flowing, the fundamental current frequency is said to be in phase with the input voltage. Hence the displacement power factor (DPF) value is

$$\text{DPF} = \cos(\phi) = 1 \quad (2.11)$$

where ϕ is angle between V_1 and I_1 .

Figure 2.7 Input voltage and current of a Three-phase Controlled rectifier

A *Fast Fourier Transform* (FFT) algorithm can extract spectrum components of any waveform. Using the algorithm to analyze the three-phase controlled rectifier input current results in Figure 2.8. It is shown that the input current contains fifth, seventh, eleventh, etc harmonic beside the fundamental component. This factor can be stated using a parameter called total harmonic distortion (THD) that is stated in (2.12).

Figure 2.8 Harmonic Spectrum of a three-phase controlled rectifier with purely resistive dc side load

$$\%THD = 100 \sqrt{\sum_{h \neq 1} \left(\frac{I_h}{I_1} \right)^2} \quad (2.12)$$

where I_h is the harmonic component with $h=2, 3, 4, \dots$. And I_1 is the fundamental component.

The higher the THD value, the more the harmonic contents are on the input current. Experiments show that typical THD value of a controlled rectifier is more than 30%. This condition is not acceptable in terms of power quality concern.

2.2.2 Increasing the delay angle

The conduction area is shifted as far as α degree in the direction of the vector rotation (Figure 2.9) while delay-angle (α) changes. The change of α will not affect the instantaneous vector voltages relation; however it affects the average output voltage.

The average output voltage value on the DC bus is the same as the average value of 60° segment on Figure 2.9.(a), or stated in equation as

$$V_{avg} = \frac{1}{2\pi/6} \int_{-\pi/6+\alpha}^{\pi/6+\alpha} V_L \cos(\theta) d(\theta) \quad (2.13)$$

$$V_{avg} = \frac{3}{\pi} V_L \cos(\alpha) \quad (2.14)$$

If the DC bus has been stated in its average value, the voltage variation is stated by using the ripple term. The output ripple voltage mainly contains 6ω frequency component and other even triplen components. Equation (2.15) states its RMS value.

$$V_{ripple} = \frac{3\sqrt{2}}{\pi} V_s \sqrt{\left(\frac{\pi^2}{18} - \frac{1}{2}\right) - \left(\frac{1}{2} - \frac{\pi}{4\sqrt{3}}\right) \cos(2\alpha)} \quad (2.15)$$

Figure 2.9 The conduction area at various delay angles (α)

As the conduction area is shifted by α , the input currents will also be shifted. It results in the voltage-current relation as shown in Figure 2.10. It is clear from the figure that except the non-linearity relation of the voltage-current, the fundamental current is also displaced by α degree from the voltage waveform. Consequently, the DPF (*Displacement Power Factor* – equation (2.11)) increases and results in a further power quality reduction.

Figure 2.10 Input current of a Three-phase Controlled rectifier at $\alpha > 0$

Performing FFT algorithm to the input current on the Figure 2.10 yields the same graphs as shown on Figure 2.8. It means high THD problem continues to persist. Furthermore, as voltage and current waveform is outphase, its DPF value decreases. Figure 2.11 shows the experimental measurements of the delay angle (α) and its relation to the input current THD in a three-phase controlled rectifier application.

Figure 2.11 Experiment result: relation between α and input current THD of a conventional three-phase controlled rectifier

3 CURRENT INJECTION METHOD – AN OVERVIEW

3.1 Some Popular Topologies

In a three-phase diode rectifier, there is a method to reduce the input current harmonic by injecting triplen harmonic to the input side of the rectifier. Bird [6] initially proposed this method. Ametani [7] further investigated it. Simple upgrade of existing three-phase rectifier, low power dissipation in the current injection circuit, and no resonance problem are several factors that led to further investigation of this current injection technique.

Figure 3.1 Typical Current Injection Circuit

The technique consists of two main parts; those are a current injector and a current injection network. The current injector can be implemented using a zigzag connected transformer [9,16], delta-star transformer [10,12,13,17,18], tuned inductor-capacitor

[19], special magnetic device injector [15], and three bi-directional semiconductor switches [11,14]. It injects the current generated by the current injection network to the input side of the controlled rectifier. The current injection network is the circuit that generates the third harmonic current. In general, it can be implemented using passive [6, 7, 10, 11, 12, 14] or active [8,9,15,16] approach. Figure 3.1 shows an overall circuit configuration of the current injection method.

Theoretically by injecting an optimal third harmonic to the input side of a three-phase diode rectifier, the input current THD of the rectifier reduces from 30% to about 5.1% (Figure 2.11). The injection circuit uses about 8.5% of power drawn by the rectifier to achieve the above result [10].

Figure 3.2 The rectifier circuit according to [10] proposed by Pejovic

Selection of a proper current injection network and a current injection circuit are the main concern in the recent researches of this current injection method. The preferred result is to gain a lightweight, simple and robust method while maintaining low power dissipation on the injection circuit and achieving low input current THD.

Figure 3.3 Current injection networks according to [10] proposed by Pejovic

To give a clear description about the third harmonic current injection method, Figure 3.2 depicts a detailed circuit diagram [10]. One of two proposed circuits on Figure 3.3 processed the injection current and is considered as a *Current Injection Network* in Figure 3.2. Both circuits consist of R, L, and C components tuned to the third harmonic of input voltage. Thus, only the third harmonic was injected to the input

side of the diode rectifier. The inductor was the most bulky and expensive component among the other two. The simplicity of the scheme (a) should be paid by less performance compared to scheme (b). The current injector used in the circuit was a bulky Δ -Y transformer. Figure 3.4 and Figure 3.5 display the voltage and current waveforms of the proposed rectifier.

Figure 3.4 Input voltage and current waveform according to [10] proposed by Pejovic

Figure 3.5 Injected current waveform according to [10] proposed by Pejovic

3.2 Previous Works

A number of previous research works have been conducted regarding the application of current injection method in a three-phase controlled rectifier. In one of the more notable ones, the circuit consists of a Δ -Y transformer as the current injector and

tuned R-L-C based on [10] circuit for generating the third harmonic current. Between the current shaping and the current injector there is a bi-directional switch composed of a back-to-back thyristor. It synchronizes the injection time and thyristor gating pulse. Figure 3.6 shows the circuit for this scheme.

It has been proven that the input current THD of the three-phase controlled rectifier reduces from more than 30% to about 3.8% (maximum achievable) with the application of current injection method. Meanwhile, an input current THD as low as about 20% is possible when the proposed rectifier operates at delay angle beyond 30° . However, it is still a better result compared to a conventional rectifier with 30% input current THD [20].

Figure 3.6 The rectifier circuit according to [20] proposed by Poh and Lim

For a detailed description about this scheme, several results from the previous works are attached. Figure 3.7, Figure 3.8, and Figure 3.9 show the hardware verification result when rectifier operates at zero firing angle, while Figure 3.10, Figure 3.11, and Figure 3.12 show the result at sixty degree firing angle.

Figure 3.7 Input Voltage and Current at $\alpha=0$, according to [20] proposed by Poh and Lim

Figure 3.8 Input Current Spectrum at $\alpha=0$, according to [20] proposed by Poh and Lim

Figure 3.9 Input Current Waveform at $\alpha=0$, according to [20] proposed by Poh and Lim

Figure 3.10 Injected Current at $\alpha=60$, according to [20] proposed by Poh and Lim

Figure 3.11 Input Voltage at $\alpha=60$, according to [20] proposed by Poh and Lim

Figure 3.12 Input Current at $\alpha=60$, according to [20] proposed by Poh and Lim

To achieve a good performance result; scheme proposed in [20] still faced several problems, such as poor performance at high delay angle and bulky and heavy weight component. Even this scheme offers a simple upgrade to current existing three-phase controlled rectifier; it tends to be an expensive method. The heavy weight, bulky, and high cost matters come from components with magnetics like inductor and the delta-star transformer.

4 CURRENT INJECTION IN A THREE-PHASE CONTROLLED RECTIFIER

4.1 Basic Principle

A three-phase controlled rectifier can be thought as a combination of two three-phase three-pulse controlled rectifier like drawn on Figure 4.1. The upper three thyristors (T_1 , T_3 , and T_5) supply V_1 on Z_1 and the lower three thyristors (T_2 , T_4 , and T_6) supply V_2 on Z_2 . The dashed line between n and N points indicates that those points are virtually in the same potential. Furthermore, it has no physical connection among them hence no current flows through.

Figure 4.1 Three-phase controlled rectifier equivalent circuit

Based on the fact stated and considering the vector on Figure 2.5, a three-phase controlled rectifier can be modeled by three impedances connected in Y (star)

connection (Figure 4.2). However, one of the three legs of the rectifier stays unconnected all the time. Two switches, S_1 and S_2 , represent the thyristors on a real three-phase controlled rectifier circuit. Z_1 and Z_2 values are half the actual load impedance connected to the DC bus of a three-phase controlled rectifier ((4.1) to (4.3)).

$$Z_1 = Z_{An} \quad (4.1)$$

$$Z_2 = Z_{Kn} \quad (4.2)$$

$$Z_1 = Z_2 = \frac{1}{2} Z_{load} \quad (4.3)$$

Figure 4.2 Y connected load equivalent circuit

The imaginary n point is defined in equation (4.4) as :

$$V_n = \frac{1}{2} V_{AK} \quad (4.4)$$

If the loads, Z_1 and Z_2 , are purely resistive, one of the three input currents waveform will look like on Figure 4.3. The figure indicates a squared input current waveform with 60° discontinuity every half a cycle of it.

Introducing the current injection network to the circuit as shown in Figure 4.4 (b) makes the equivalent circuit of a rectifier looks like the circuit on figure 4.4 (c). The figure shows that the equivalent circuit of a three-phase controlled rectifier is similar to a three-phase star-connected resistive load. The resistive star-connected load is a linear load. As a result, the input current waveform is transformed from nearly squared and discontinuous into a fully sinusoidal waveform (Figure 4.5). It is noted that the equivalent resistors on figure 4.4 (c) are,

$$Z_1 = Z_2 = Z_3 = R_e \quad (4.5)$$

Figure 4.3 Input voltage and current of the circuit shown in Figure 4.2

In the circuit implementation, there are three *complementary bidirectional* switches as a current injector on the current injection circuit blocks. The *complementary* term means that the switch connects Z_3 on Figure 4.4 to one of the three input voltages that is not connected to S_1 and S_2 switches. The *bidirectional* term means that the current

flows through this switch is AC current. It differs from S_1 and S_2 where in those switches current flows are DC currents.

(a) A conventional three-phase rectifier

(b) A three-phase rectifier with proposed current injection network

(c) Equivalent circuit of point (b)

Figure 4.4 Modified Y-connected equivalent circuit

Figure 4.5 Input voltage and current of Figure 4.4

4.2 Parameter Determination in the Current Injection Circuit

Z3 and S3 in Figure 4.4 are equivalent representation of the current injection circuit. This sub-chapter presents how to construct the circuit and how to determine its parameter value. Two parameter determination methods are presented. One of the methods is the spectrum analysis. This method is a standard technique in the current injection application to determine the injection current parameter. Here, it is used as a reference to verify the second method that is the circuit transformation method.

While both methods result in the same parameter value, the later provides a simpler solution. Recognizing the basic idea of the current injection scheme is another advantage of the second method. The basic idea is important to solve problems such

as : calculate the power dissipation in the current injection circuit, estimate the input current of the proposed rectifier under unbalanced input voltage, and predict the effect of input inductance on the proposed circuit.

4.2.1 DC Bus Voltage Spectra Analysis

Figure 4.6 shows typical positive and negative DC bus voltage waveforms (V_A and V_K) of a three-phase controlled rectifier of Figure 4.1 with respect to ground (N point). Fourier series expresses V_A on the figure as:

$$A_n = \frac{3}{\pi} \int_{\alpha - \frac{\pi}{3}}^{\alpha + \frac{\pi}{3}} V_{S_{peak}} \cos(\theta) \cos(n\theta) d\theta \quad (4.6)$$

$$B_n = \frac{3}{\pi} \int_{\alpha - \frac{\pi}{3}}^{\alpha + \frac{\pi}{3}} V_{S_{peak}} \cos(\theta) \sin(n\theta) d\theta \quad (4.7)$$

$$n = k \cdot 3 \text{ with } k = 0, 1, 2, \dots \quad (4.8)$$

Where n is the n^{th} harmonic, $V_{S_{peak}}$ is the amplitude of the supply line-to-neutral voltage and α is the delay angle.

Evaluating integrals on (4.6) and (4.7) give,

$$A_n = \frac{3}{\pi} V_{S_{peak}} \left\{ \frac{\sin[(n+1)\frac{\pi}{3}] \cos[(n+1)\alpha]}{n+1} + \frac{\sin[(n-1)\frac{\pi}{3}] \cos[(n-1)\alpha]}{n-1} \right\} \quad (4.9)$$

$$B_n = \frac{3}{\pi} V_{S_{peak}} \left\{ \frac{\sin[(n+1)\frac{\pi}{3}] \sin[(n+1)\alpha]}{n+1} + \frac{\sin[(n-1)\frac{\pi}{3}] \sin[(n-1)\alpha]}{n-1} \right\} \quad (4.10)$$

Figure 4.6 DC bus voltage waveforms of a three-phase controlled rectifier with respect to ground

From (4.8), variable k is integers, then

$$\sin(k\pi) = 0 \quad (4.11)$$

$$\cos(k\pi) = (-1)^k \quad (4.12)$$

Substitution of (4.11) and (4.12) in (4.9) and (4.10) yield some simpler expression,

$$\sin\left[(n+1)\frac{\pi}{3}\right] = \cos\left(\frac{n}{3}\pi\right) \sin\left(\frac{\pi}{3}\right) = \frac{(-1)^{n/3}}{2} \sqrt{3} \quad (4.13)$$

$$\sin\left[(n-1)\frac{\pi}{3}\right] = -\cos\left(\frac{n}{3}\pi\right) \sin\left(\frac{\pi}{3}\right) = -\frac{(-1)^{n/3}}{2} \sqrt{3} \quad (4.14)$$

Then, substitution of (4.13) and (4.14) to (4.9) and (4.10) makes,

$$A_n = \frac{(-1)^{n/3}}{2} \sqrt{3} \frac{3}{\pi} V_{S_{peak}} \left\{ \frac{\cos[(n+1)\alpha]}{n+1} - \frac{\cos[(n-1)\alpha]}{n-1} \right\} \quad (4.15)$$

$$B_n = \frac{(-1)^{n/4}}{2} \sqrt{3} \frac{3}{\pi} V_{S_{peak}} \left\{ \frac{\sin[(n+1)\alpha]}{n+1} - \frac{\sin[(n-1)\alpha]}{n-1} \right\} \quad (4.16)$$

The equation can also be stated in polar notation using magnitude (C_n) and phase (Φ_n) notation below,

$$C_n = \sqrt{A_n^2 + B_n^2} \quad (4.17)$$

$$C_n = \frac{3\sqrt{3}}{2\pi} V_{S_{peak}} \sqrt{\frac{1}{(n+1)^2} + \frac{1}{(n-1)^2} - \frac{2\cos(2\alpha)}{(n+1)(n-1)}} \quad (4.18)$$

With phase angle Φ is found from equation below,

$$\phi_n = \arctan \left(\frac{\frac{\cos(n+1)\alpha}{n+1} - \frac{\cos(n-1)\alpha}{n-1}}{\frac{\sin(n+1)\alpha}{n+1} - \frac{\sin(n-1)\alpha}{n-1}} \right) \quad (4.19)$$

V_K is similar with V_A . However, delay angle for V_K is shifted by further π . Hence,

$$\alpha_K = \pi - \alpha_A \quad (4.20)$$

$$\cos(2\alpha_K) = \cos(2\alpha_A) \quad (4.21)$$

Where, α_A and α_K are delay angle for V_A and V_K respectively. From (4.20) and (4.21), both positive and negative waveform will have the same magnitude. Since

$$\cos(\alpha_K) = -\cos(\alpha_A) \quad (4.22)$$

$$\sin(\alpha_K) = \sin(\alpha_A) \quad (4.23)$$

Equation (4.22) and (4.23) indicates that the odd triplens have the same phase angle, but the even triplens have the opposite sign. As a result, even V_A and V_K in Figure 4.6

have odd and even triplens components, the load voltage, as the resultant, has only DC ($k=0$) and even triplen components ($k=2,4,6,\dots$; equation (4.8)).

Dc component can be found by substituting n by zero in (4.18), and its result should be divided by two, or

$$C_0 = \frac{1}{2} \frac{3\sqrt{3}}{2\pi} \sqrt{2} \cos^2(\alpha) V_{S_{peak}} \quad (4.24)$$

Where C_0 is the DC component of the V_A or V_K in Figure 4.6. The total DC component on (2.14) can be found by summing the DC component on both V_A and V_K and substitute (4.25) below to (4.24),

$$V_{S_{peak}} = \frac{\sqrt{2}}{\sqrt{3}} V_L \quad (4.25)$$

Where, V_L is the *rms* line-to-line input voltage. It is clear that the DC value decreases as the delay angle (α) increases. On the other hand, from (4.18) other components of the DC bus voltage, the odd and even triplens, increase proportional to,

$$G_n = \sqrt{\frac{1}{(n+1)^2} + \frac{1}{(n-1)^2} - \frac{2\cos(2\alpha)}{(n+1)(n-1)}} \quad (4.26)$$

Where, G_n is the gain factor of the n^{th} harmonic and equation (4.8) determines the n values as multiple of three. Figure 4.7 shows how delay angle affects the gain (G_n) on a certain n value. It shows that the higher the n value, the lower its gain. The maximum spectra gain is reached when $\alpha = 90^\circ$. It is evident that the third harmonic ($n=3$) is the dominant component of V_A and V_K .

Figure 4.7 The rectifier DC bus spectrum gain (G_n) with $n=3, 6, 9, 12, 15$ and α from 0° up to 180°

4.2.2 Injection Current

Fourier series expansion on (4.18) for V_A can be stated by,

$$V_A = C_0 + \sum_{n=1, \infty} C_n \cos(\phi_n) \quad (4.27)$$

Substitution of α equal to zero to (4.18) and (4.27) resulted in (4.28) below:

$$V_A = \frac{3\sqrt{3}}{\pi} V_{S_{peak}} \left(\frac{1}{2} + \sum_{n=1}^{+\infty} \frac{(-1)^{n+1}}{9n^2 - 1} \right) \cos(3n\omega_0 t) \quad (4.28)$$

Repeating above sequence for negative DC bus voltage (V_K) at the same α will find

$$V_K = \frac{3\sqrt{3}}{\pi} V_{S_{peak}} \left(-\frac{1}{2} + \sum_{n=1}^{+\infty} \frac{1}{9n^2 - 1} \right) \cos(3n\omega_0 t) \quad (4.29)$$

The circuit is treated as a balance three-phase circuit hence, voltage at point n on Figure 4.1 (V_n) can be found by calculating:

$$V_a + V_b + V_c = V_A + V_K + V_n = 0 \quad (4.30)$$

with all voltages are referenced to N. Hence,

$$V_n = -(V_A + V_K) = -\frac{3\sqrt{3}}{\pi} V_{S_{peak}} \sum_{n=1}^{+\infty} \frac{1 + (-1)^{n+1}}{9n^2 - 1} \cos(3n\omega_0 t) \quad (4.31)$$

And normally, no current flows from n to N points as there should be an equal but opposite phase of V_A and V_K on the DC bus.

Voltage at load side thus can be stated as

$$V_{Load} = V_A - V_K \quad (4.32)$$

$$V_{Load} = \frac{3\sqrt{3}}{\pi} V_{S_{peak}} \left(1 - \sum_{k=2,4,6,\dots}^{+\infty} \frac{2}{9k^2 - 1} \cos(3k\omega_0 t) \right) \quad (4.33)$$

With load DC component stated as

$$V_{LoadDC} = \frac{3\sqrt{3}}{\pi} V_s \quad (4.34)$$

To simplify the notation, V_{odd} and V_{even} are introduced. V_{odd} is voltage spectral frequency that only contains odd triplens spectra sequence. V_{even} is voltage spectral frequency that contains even triples spectra sequence. V_{odd} and V_{even} harmonic component can be expressed by:

$$V_{odd} = \frac{3\sqrt{3}}{\pi} V_{S_{peak}} \sum_{k=1,3,5,\dots}^{+\infty} \frac{1}{9k^2 - 1} \cos(3k\omega_0 t) \quad (4.35)$$

$$V_{even} = \frac{3\sqrt{3}}{\pi} V_{S_{peak}} \sum_{k=2,4,6,\dots}^{+\infty} \frac{1}{9k^2 - 1} \cos(3k\omega_0 t) \quad (4.36)$$

Substitution of (4.35) and (4.36) to (4.28),(4.29),(4.31), and (4.33), lead to the following,

$$V_A = \frac{1}{2} V_{LoadDC} + V_{odd} + V_{even} \quad (4.37)$$

$$V_K = -\frac{1}{2} V_{LoadDC} + V_{odd} - V_{even} \quad (4.38)$$

$$V_n = -(V_A + V_K) = -2V_{odd} \quad (4.39)$$

$$V_{Load} = (V_A - V_K) = V_{LoadDC} + 2V_{even} \quad (4.40)$$

Current flows from point A to point K, (shown in Figure 4.1) then:

$$I_{AK} = \frac{V_A - V_K}{Z_L} = \frac{\left(-\frac{1}{2} V_{LoadDC} + V_{odd} - V_{even}\right) - \left(-\frac{1}{2} V_{LoadDC} + V_{odd} - V_{even}\right)}{Z_L} \quad (4.41)$$

$$I_{AK} = I_{LoadDC} + 2I_{even} \quad (4.42)$$

From the above equations, current that flows in the DC bus consist of DC current and even triplen components. No odd triplens can be found.

In fact, the absence of the odd triplens component should be avoided. It makes the system become not linear as odd and even component are treated in different ways. In

a linear system, all voltage components (DC, odd triplens, and even triplens) should be a function of currents with R as the constant. It can be stated by

$$V_n = R \cdot I_n \quad (4.43)$$

where n is integers (0,1,2,...).

Letting current flow through S3 (Figure 4.4), based on (4.39) lets the odd triplen components flow in the circuit. If the equivalent resistive load is stated with R_e notation, current that flows in the branch A , K , and n on Figure 4.4 are I_A , I_K , and I_n respectively. The definition of each current can be described by the equations below:

$$i_A = \frac{V_A}{R_e} = \frac{1}{R_e} \left(\frac{1}{2} V_{LoadDC} + V_{odd} + V_{even} \right) \quad (4.44)$$

$$i_K = \frac{V_B}{R_e} = \frac{1}{R_e} \left(-\frac{1}{2} V_{LoadDC} + V_{odd} - V_{even} \right) \quad (4.45)$$

$$i_n = \frac{V_C}{R_e} = -\frac{2}{R_e} V_{odd} \quad (4.46)$$

Where i_n is the injection current and R_e is equal to Z_1 , Z_2 , and Z_3 and are half the Z_{load} .

Equation (4.46) states that i_n contains only odd triplen harmonic.

From equation (4.26), it can be found that all odd triplen voltages will increase with G_n factor as delay angle increase up to $\alpha=90^\circ$. Hence, the injection current (i_n) increases along with the delay angle (α). This phenomenon is to be highlighted, as

this is an important factor to determine the power loss in the current shaping network and current rating of the bi-directional switches.

4.2.3 Selection of the resistor value in the current shaping network

The first step to achieve purely resistive load for all the three-phase is to determine the resistive equivalent load (R_e). R_e can be calculated using equation below,

$$R_e = \frac{1}{2} \frac{V_{DCrms}}{I_{DCrms}} \bigg|_{\alpha=0} \quad (4.47)$$

Assuming that load is highly inductive, only DC component current will flow into load, which is found as:

$$i_{LoadDC} = \frac{1}{2} \frac{V_{LoadDC}}{R_e} = \frac{3\sqrt{3}}{2\pi} \frac{V_{pk}}{R_e} \quad (4.48)$$

AC current component will flow to i_{IA} and i_{IK} ,

$$i_{IA} = i_A - i_{LoadDC} \quad (4.49)$$

$$i_{IK} = i_K + i_{LoadDC} \quad (4.50)$$

i_{IA} and i_{IK} can also stated by its spectra component by:

$$i_{IA} = \frac{1}{R_e} (V_{odd} + V_{even}) \quad (4.51)$$

$$i_{IK} = \frac{1}{R_e} (V_{odd} - V_{even}) \quad (4.52)$$

Figure 4.8 is a graphical explanation of above current equation.

Figure 4.8 Current flow in proposed the DC bus circuit

The *current shaping* equations above shows that the rectifier load should be highly inductive and ideally, it should contain only DC component. Otherwise, injection circuit should only contain AC component. In fact, it is obvious that DC component should be present on the DC bus. To prevent the DC current flow in the current injection circuit, two capacitors are put in series on the current injection circuit (Figure 4.9). To simplify the calculation, it is assumed that the capacitor reactance is negligible for all AC component frequency.

From Figure 4.8, if V_{An} and V_{Kn} is defined as

$$V_{An} = V_A - V_n = \frac{1}{2} V_{LoadDC} + 3V_{odd} + V_{even} \quad (4.53)$$

$$V_{Kn} = V_K - V_n = -\frac{1}{2} V_{LoadDC} + 3V_{odd} - V_{even} \quad (4.54)$$

After passing series capacitor with negligible voltage drop, V_{An} and V_{Kn} contain only AC components,

$$V_{An_{ac}} = 3V_{odd} + V_{even} \quad (4.55)$$

$$V_{Kn_{ac}} = 3V_{odd} - V_{even} \quad (4.56)$$

From Figure 4.12, i_n can be found that,

$$i_n = -(i_{oddA} + i_{oddB}) \quad (4.57)$$

Substitution of equation (4.46), (4.55) and (4.56) to equation (4.57) above will yield

$$-\frac{2}{R_e} V_{odd} = -\left(\frac{3V_{odd} + 3V_{odd}}{R_{odd}} \right) \quad (4.58)$$

Hence, it can be found that

$$R_{odd} = 3R_e \quad (4.59)$$

With $R_{odd}=3R_e$ it can be found that:

$$i_{oddA} = \frac{V_{An_{ac}}}{3R_e} = \frac{3V_{odd} + V_{even}}{3R_e} = \frac{1}{R_e} \left(V_{odd} + \frac{1}{3} V_{even} \right) \quad (4.60)$$

$$i_{oddK} = \frac{V_{Kn_{ac}}}{3R_e} = \frac{3V_{odd} - V_{even}}{3R_e} = \frac{1}{R_e} \left(V_{odd} - \frac{1}{3} V_{even} \right) \quad (4.61)$$

The even harmonic portion (i_{even}) is introduced here to complete the definition of i_{LA} and i_{LK} on equations (4.51) and (4.52) apart from what has been explained in equations (4.60) and (4.61). Its expression can be stated as,

$$i_{evenA} = i_{LA} - i_{oddA} = \frac{V_{odd} + V_{even}}{R_e} - \frac{V_{odd} + \frac{1}{3} V_{even}}{R_e} = \frac{2}{3} \frac{V_{even}}{R_e} \quad (4.62)$$

$$2V_{even} = 3I_{even}R_e \tag{ 4.63}$$

$$2I_{even}R_{even} = 3I_{even}R_e \tag{ 4.64}$$

$$R_{even} = \frac{3}{2}R_e \tag{ 4.65}$$

If the same equation is applied to i_{IK} it will conduct the same result of R_{even} .

The complete current shaping network as prescribed by above equation can be shown in Figure 4.9.

Figure 4.9 Current shaping network

The parameters that has been determined based on α equal to zero above are applicable for all other α . This is true as the circuit emulates a three-phase star-connected resistive load on a three-phase controlled rectifier (figure 4.4) therefore

maintain its power factor to be unity through out its operating condition. As a result, the higher the delay angle (α) the higher the power dissipated in the injection circuit as heat loss. The heat loss is present as the current injection circuit try to compensate the discontinuity on the original input currents. This claims will be proven later in chapter 5.

4.3 Circuit Transformation, Alternative Approach of Determining The Injection Circuit Parameter

For the real life application, the circuit of Figure 4.4 is not practical. It transforms a three-phase controlled rectifier from *a two-port output device* into *a three-port output device*. Consequently, the load connected to it should be two identical impedance loads. The loads should also be two purely resistive loads. Thus, its behavior is unlike a conventional rectifier.

Realizing that the figure is actually a Y connected resistive load, it can easily be transformed to its Δ equivalent while still preserving the voltage and current behavior of the prior connection. In fact, the transformation process can be used to determine R_{odd} and R_{even} from another approach compared to the spectra analysis method in the subchapter 4.2.

Figure 4.10 Y-Δ equivalent circuit

4.3.1 Resistance values of Z_{AI} and Z_{KI}

The resistance values of Z_{AI} and Z_{KI} are actually an R_{odd} equivalent of the harmonic analysis method. Defining the resistances based on Figure 4.10 is straight forward, that is,

$$|\bar{V}_{AI}| = \sqrt{3} \cdot |\bar{V}_{An}| \quad (4.66)$$

$$|\bar{V}_{AI}| = |\bar{V}_{IK}| = |\bar{V}_{KA}| \quad \text{and} \quad |\bar{V}_{An}| = |\bar{V}_{In}| = |\bar{V}_{Kn}| \quad (4.67)$$

$$|\bar{I}_A| = \sqrt{3} \cdot |\bar{I}_{AI}| \quad (4.68)$$

$$|\bar{I}_{AI}| = |\bar{I}_{IK}| = |\bar{I}_{KA}| \quad \text{and} \quad |\bar{I}_{An}| = |\bar{I}_{In}| = |\bar{I}_{Kn}| \quad (4.69)$$

$$\bar{V}_{An} = Z_1 \cdot \bar{I}_A \quad (4.70)$$

$$\bar{V}_{AI} = Z_{AI} \cdot \bar{I}_{AI} \quad (4.71)$$

$$\frac{1}{\sqrt{3}} \frac{\bar{V}_{An}}{\bar{V}_{An}} = \frac{Z_1}{Z_{AI}} \frac{\sqrt{3} \cdot \bar{I}_{AI}}{\bar{I}_{AI}} \quad (4.72)$$

$$Z_{AI} = 3 \cdot Z_{An} \quad (4.73)$$

As the circuit is a balanced three-phase circuit,

$$Z_{AI} = Z_{KI} = Z_{AK} \quad (4.74)$$

From equation (4.1) to (4.3), it has defined that

$$Z_{An} = Z_{Kn} = \frac{1}{2} Z_{load} \quad (4.75)$$

Substitute the equation (4.75) above to equation (4.73) yields equation (4.46) below,

$$Z_{AI} = Z_{IK} = \frac{3}{2} Z_{load} \quad (4.76)$$

4.3.2 Resistance Value of Z_{AK}

The resistance of Z_{AK} is actually an R_{even} equivalent of the harmonic analysis method.

In a balance load, Z_{AK} value should be

$$Z_{AK} = 3 \cdot Z_{An} \quad (4.77)$$

In fact equation (4.1) to (4.3) stated that

$$Z_1 = Z_2 = \frac{1}{2} Z_{load} \quad (4.78)$$

Or in other words, the reality is

$$Z_{AK} = 2 \cdot Z_{An} \quad (4.79)$$

Therefore, it is easy to conclude that the AK branch draws more currents than AI and KI.

Prior to the above conclusion, the basic idea of this current injection method should be remembered. The Idea is making all the three-phase voltage sources to sense a

balance resistive three-phase Y connected load or its equivalent (Figure 4.4). In other words

$$\bar{V}_s = \bar{I}_s \cdot R_s \quad (4.80)$$

Where $\bar{V}_s$ is the source voltage vectors ($\bar{V}_a$, $\bar{V}_b$, and $\bar{V}_c$), $\bar{I}_s$ is the source current vectors ($\bar{I}_a$, $\bar{I}_b$, and $\bar{I}_c$), and R_s is the line to neutral resistance (Z_1 , Z_2 , and Z_3).

Another fact is, actually a three-phase controlled rectifier is composed of two three-phase half bridge rectifier connected in series (Figure 4.1). The output voltage of each three-phase half bridge controlled rectifier consists of AC and DC components (equation (2.14) and (2.15)).

$$V_{An} = V_{An_{DC}} + V_{An_{AC}} \quad (4.81)$$

$$V_{Kn} = V_{Kn_{DC}} + V_{Kn_{AC}} \quad (4.82)$$

$$V_{AK} = V_{An} + V_{nK} \quad (4.83)$$

From the DC component point of view, the individual three-phase half bridge controlled currents are,

$$I_{An_{DC}} = \frac{V_{An_{DC}}}{Z_1} \quad (4.84)$$

$$I_{Kn_{DC}} = \frac{V_{Kn_{DC}}}{Z_2} = \frac{-V_{nK_{DC}}}{Z_2} \quad (4.85)$$

Therefore, current flows in the AK branch is,

$$I_{AK_{DC}} = \frac{V_{AK_{DC}}}{Z_{Load}} = \frac{V_{An}}{Z_1} + \frac{V_{nK}}{Z_2} = 2 \cdot \frac{V_{An_{DC}}}{Z_1} \quad (4.86)$$

Therefore, the circuit transformation from Y to Δ is still preserving its voltage and current relationship for the DC component. However, from AC components point of view,

$$|\bar{I}_{An_{AC}}| = \frac{|\bar{V}_{An_{AC}}|}{Z_1} \quad (4.87)$$

$$|\bar{I}_{Kn_{AC}}| = \frac{|\bar{V}_{Kn_{AC}}|}{Z_2} = \frac{-|\bar{V}_{nK_{AC}}|}{Z_2} \quad (4.88)$$

While actually the An and Kn components are 120° out of phase. It means,

$$|\bar{I}_{AK_{AC}}| \neq \frac{|\bar{V}_{An_{AC}}|}{Z_1} + \frac{|\bar{V}_{nK_{AC}}|}{Z_2} \quad (4.89)$$

$$|\bar{I}_{AK_{AC}}| = \frac{|\bar{V}_{An_{AC}} + \bar{V}_{nK_{AC}}|}{Z_1 + Z_2} = \frac{\sqrt{3}V_s}{Z_{Load}} \quad (4.90)$$

To preserve the voltage and current relation on a balance three-phase circuit, based on equation (4.73) it is compulsory for the AC component to have

$$Z_{AK_{AC}} = 3 \cdot Z_1 \quad (4.91)$$

Considering to equation (4.91) above, it can be stated in terms of Z_{Load} .

$$Z_{AK_{AC}} = \frac{3}{2} \cdot Z_{Load} \quad (4.92)$$

In fact, the calculation result of $Z_{AK_{AC}}$ on (4.91) and (4.92) results in similar value to

R_{even} on (4.65).

4.4 Circuit Realization

Figure 4.11 displays a complete transformation the circuit of Figure 4.4. As it was stated in the previous section, the current flowing through S_3 is AC, and contains only the odd triplens harmonic. Therefore, DC voltage component in the DC bus should be prevented to be present on the current processing circuit. Here, two capacitors (C_1 and C_2) are introduced to prevent the DC current to flow in the current injection circuit.

Figure 4.11 Proposed Equivalent Circuit Realization

As Z_{AI} , Z_{KI} , and Z_{AKAC} process the current that will be injected back through the current injector S_3 . Therefore, the networks later will be called *the current processor network*.

In real application, the circuit in the Figure 4.11 is translated into a three-phase controlled rectifier on Figure 4.12. The S_1 and S_2 on Figure 4.11 are actually T_1 to T_6 in Figure 4.12 while S_3 is actually the bidirectional switch S_a , S_b , and S_c .

4.5 Selection of Injection Circuit Capacitor and Limitation of DC Bus Ripple Current

Bus Ripple Current

The best result is achieved when the capacitor on the injection circuit is infinite. Therefore, no voltage drop occurs on the injection circuit. It is also ideal to have no ripple current flows in the DC bus. The no DC bus ripple current requirement means an infinite load inductance.

The capacitor optimum value can be found from the equation (4.33) below. Here parameter γ is used to determine the optimum capacitance. Where, parameter γ means the cut off frequency (-3 dB point) of the equivalent load resistance (R_e) related to the preferred optimum capacitance (C). The γ value and its relation to the rectifier input current rectifier is presented on Figure 4.13 and is used to obtain the capacitor value [12].

$$\gamma = 3\omega_0 R_e C \quad (4.93)$$

Figure 4.13 Dependence of Input current to γ

Numerous trial and errors were done to determine the optimum value of the load inductance. As the ripple current is a function of inductance (4.94), this parameter is used as the variable. In the simulation, the variable is stated in percent of DC current component.

$$i_{ripple} = f(L) \quad (4.94)$$

From MATLAB model and experiment, it was found that the correlation of the i_{ripple} and input THD is quite linear and can be stated by equation (4.95) below,

$$THD = 95.5\% \cdot i_{ripple} \quad (4.95)$$

Hence, THD below 5% while the operating point of the controlled rectifier below 30° can be reached by adjusting the inductance value to suppress the current ripple (i_{ripple}) below 5.3% of the DC current component.

In fact, keeping the DC ripple current below 5% within a wide operation range of delay angle is difficult and requires an additional series smoothing inductance. Equation 2.15 has shown that the ripple voltage increases by factor of cosine two times the delay angle. It results in the 100% of ripple current while rectifier operates at 90° delay angle. This condition dictates that in real application, the input current THD of the rectifier increases inline with the changes of delay angle.

4.6 Intervals of The Conduction Period

When the conduction angle is increased, as shown in Figure 4.14, the conduction area is shifted in the same direction of the vector rotation as far as α . Where α is the delay angle. Up to 30° delay angle, the full 360° conduction mode of the three-phase balanced circuit will be kept maintained. It means, as long as the Z_{AI} , Z_{KI} , and $Z_{AK,BC}$ is perfectly tuned to the load parameter, the input current is still almost purely sinusoidal. In terms of THD, it is confidently stated nearly 0%.

Figure 4.14 Conduction intervals for $\alpha > 30^\circ$

However, as the delay angle goes beyond 30° , the circuit behavior will change. Figure 4.14 describes the change. The figure shows the input voltage vectors diagram when the delay angle is slightly beyond 30° . On the figure, V_C is always the voltage connected to S_3 (Figure 4.11) or S_a , S_b , and S_c in the real application (Figure 4.12).

On Figure 4.14(a), V_A is the vector voltage connected to the circuit through S_1 . On the position indicated in the figure, the anode of the S_1 connected to V_A is more negative than its cathode. As a thyristor stop conducting when the condition occurs, current will stop to flow through S_1 . This creates a current discontinuity. Hence, it creates some current harmonic.

The current discontinuity angle can be found from equation (4.96) below. The wider the angle the higher the harmonic generated and therefore increasing its current THD.

$$\theta_d = \alpha - 30^\circ \quad (4.96)$$

Similar condition occurs while V_A is connected to S_2 as shown in the Figure 4.14.(b). On that position, voltage on the cathode of S_2 is higher than the voltage on its anode. As a result, current discontinuity is also present on the negative cycle. Both conditions are illustrated through Figure 4.15.

The above facts restrict the operating area of the proposed scheme to 50° delay angle. The limit is determined based on some MATLAB simulations and experiments. It was found that, beyond 50° delay angle, the input current discontinuity become too large. Therefore, the input current distortion of the rectifier becomes excessive.

Figure 4.15 Conduction area for $\alpha > 30$ in time domain waveform

4.7 Rectifier Output Voltage

The upgraded three-phase controlled rectifier DC output characteristic slightly differs from a conventional three-phase controlled rectifier. It is especially so when it works at delay angle (α) more than 30° . The condition is due to the characteristic stated on the previous chapter (sub chapter 4.6). It has stated that the output voltage of each individual half-bridge controlled rectifier on Figure 4.1 cannot yield negative voltage as illustrated in Figure 4.14. As a result, beyond 30° delay angle, the average output voltage of the proposed rectifier is higher than a conventional three-phase controlled rectifier. The output voltage characteristic different is shown in Figure 4.16.

Figure 4.16 Variation of the output voltage in a conventional and a rectifier with the proposed current injection technique

While the rectifier operates below 30° delay angle, the output voltage characteristic is similar to a conventional three-phase controlled rectifier. Its output voltage can be stated by equation (2.14). Beyond 30° delay angle, the output voltage is decreasing linearly with slope of about (-0.476) , or can be expressed by equation (4.37). The output voltage waveform of the proposed rectifier is shown on Figure 4.17.

$$V_{dc_{>30}} = V_{dc_{max}} (\cos 30 - 0.476\alpha) \quad (4.97)$$

Figure 4.17 DC output voltage waveform (upper trace) of the modified rectifier

beyond $\alpha = 30^\circ$

4.8 Power Dissipated in The Injection Circuit

Let us consider Figure 4.8. The power dissipated by the current processor network can be divided into two sources. Firstly, the power dissipated by Z_{AI} and Z_{KI} . Secondly, the power dissipated by the $Z_{AK,JO}$

The power dissipated by the Z_{AI} and Z_{KI} can be calculated by

$$P_l = P_m - P_{AK} \quad (4.98)$$

Where, P_l is the power losses or dissipated by Z_{KI} and Z_{AI} . P_m is the input power drawn by the three-phase controlled rectifier, and P_{KA} is the power delivered to the K_A node or the output voltage.

As the upgraded three-phase controlled rectifier is actually a constant resistive three-phase load emulation, power drawn by the rectifier up to 30° is constant and is equal to:

$$P_m = 3(V_s \cdot Z_l) \quad (4.99)$$

Above 30° delay angle, due to the input current discontinuity, its rms value is decreasing (sub chapter 4.6). This relationship is shown as the input power vs delay-angle characteristic in the following figure.

Figure 4.18 Variation of the three-phase normalized input power of the proposed scheme with respect to α

While power drawn by the rectifier is constant (equation (4.99)), power delivered to the load is proportional to the DC output voltage (equation (2.14)). In other words, power delivered to the load decreases proportional to cosine of delay angle. Equation (4.98) shows that such phenomenon will increase the power loss and hence decreasing the efficiency of the scheme as a consequence.

Power dissipated by the Z_{AKAC} is proportional to the ripple voltage at the DC bus.

Hence,

$$P_{AKAC} = \frac{(V_{AKAC})^2}{\frac{3}{2} Z_{AKAC}} \quad (4.100)$$

From [4], the V_{AKAC} can be calculated by,

$$V_{KAC} = \frac{3\sqrt{2}}{\pi} V_s \sqrt{\left(\frac{\pi^2}{18} - \frac{1}{2}\right) - \left(\frac{1}{2} - \frac{\pi}{4\sqrt{3}}\right) \cos(2\alpha)} \quad (4.101)$$

Where V_s is r.m.s. a.c. input line to line voltage

The total power dissipated by the current injection scheme is

$$P_{dissipated} = P_l + P_{AK_{ic}} \tag{4.102}$$

In three-phase rectifier with optimal current injection, its power loss will be about 8.5% [10]. Realizing the fact that mainly power lost is due to power dissipated on Z_{AI} and Z_{KI} branch, an approximation equation to the power loss can be stated through equation (4.103) below. To verify such fact, some real efficiency measurements on a modified rectifier had been done to the proposed scheme and its results are represented in Figure 4.19.

$$P_l = 8.5\%(1 + 10.76 \cdot \cos \alpha) \tag{4.103}$$

Figure 4.19 Efficiency vs delay angle characteristics of the proposed scheme

4.9 Effect of Line Inductance

In a practical thyristor converter, the presence of the line inductance cannot be ignored. This inductance can be from the nature of the line conductor, transformer

leakage, or even added one to meet certain condition. As an example, VDE (The association for electrical, electronic, and information technology of Germany) require that the inductance must be [2],

$$\omega L_s = 0.05 \frac{V_s}{I_s} \quad (4.104)$$

For a given delay angle (α), the current commutation takes a finite commutation interval u . The relation between α and u is [2],

$$\cos(\alpha + u) = \cos \alpha - \frac{2\omega L_s}{\sqrt{2}V_{LL}} I_d \quad (4.105)$$

While it is known that the input inductance will introduce an input voltage harmonic distortion (Figure 4.20) [2], line inductance will reduce the input current $\frac{di}{dt}$. Therefore the input current discontinuity while the rectifier operates beyond 30° delay angle will be minimized. The condition stated will reduce the input current THD. The simulation result will show the THD reduction effect.

However it should be noted that during interval u , one thyristor is slowly reducing its conduction while another one is slowly increasing its conduction. Therefore, to recreate the actual current, a circuit like shown in Figure 4.21 is assembled.

Figure 4.20 Voltage glitch due to input inductance

Figure 4.21 Equivalent circuit of a three-phase rectifier with line inductance at the event of commutation

Considering a condition as shown on the figure, where V_a is increasing its conduction and V_b is decreasing it. It is shown that at the moment all three phases are in conduction state. This condition should be carefully examined due to the presence of the bi-directional injection current switches. Connecting the switches at that moment

to V_A , for example, may cause a commutation failure. Hence, it should be assured that during the thyristor commutation process, the bidirectional switches are in off state. The switches activation should wait until u period is finished.

Another condition that should be considered is the lower input current DPF while line induction is counted. After the current injection scheme is applied to the rectifier circuit, its equivalent circuit looks like the one Figure 4.22. From the figure it is evident that the input currents will be lagging compared to the input voltages due to the presence of three line inductances. The Voltage and Current displacement angle (ϕ) can be found from equation (4.46). This fact should be considered as the current lagging makes the DPF is less than unity thus lowering the input power quality.

$$\phi = \tan^{-1} \frac{x_L}{x_Z} \quad (4.106)$$

Figure 4.22 Proposed scheme equivalent circuit

4.10 Effects of Unbalance Input Voltages

An unbalanced input voltage results in worst input current harmonics on a conventional three-phase controlled rectifier [22]. If assumed that the line to neutral supply voltages is V_a , V_b , and V_c , then their corresponding zero, positive, and negative sequence voltages can be expressed as:

$$V_z = \frac{1}{3}(V_a + V_b + V_c) \quad (4.107)$$

$$V_p = \frac{1}{3}(V_a + a \cdot V_b + a^2 \cdot V_c) \quad (4.108)$$

$$V_n = \frac{1}{3}(V_a + a^2 \cdot V_b + a \cdot V_c) \quad (4.109)$$

To investigate the effect of the input voltage unbalance on the proposed three-phase controlled rectifier, in the simulation and experiment, the voltage unbalance is stated by unbalanced factor u such that:

$$u = \left| \frac{V_n}{V_p} \right| \quad (4.110)$$

In an ideal condition, considering the circuit on Figure 4.4, the input current THD of the proposed rectifier can be predicted similar to input currents of a three-phase resistive load under unbalanced input voltages. It is clear that unbalanced input voltages would not create any harmonic on a three-phase resistive load. Based on that fact, the unbalance input voltages will have a minimum effect on the THD

suppression performance of the proposed method. This claim will be established on the simulation and experiment result.

Table 4.1 shows the normalized values of the phase voltages that would result in a certain amount of unbalance.

In an ideal condition, considering the circuit on Figure 4.4, the input current THD of the proposed rectifier can be predicted similar to input currents of a three-phase resistive load under unbalanced input voltages. It is clear that unbalanced input voltages would not create any harmonic on a three-phase resistive load. Based on that fact, the unbalance input voltages will have a minimum effect on the THD suppression performance of the proposed method. This claim will be established on the simulation and experiment result.

Table 4.1 Normalized Three-Phase Voltages and Corresponding Unbalance Factor

<i>Unbalance factor (%)</i>	V_a	V_b	V_c
0	$1\angle 0^\circ$	$1\angle 120^\circ$	$1\angle 240^\circ$
2	$1\angle 0^\circ$	$0.95\angle 120^\circ$	$1.01\angle 240^\circ$
5	$1\angle 0^\circ$	$0.861\angle 120^\circ$	$0.863\angle 240^\circ$
10	$1\angle 0^\circ$	$1.4\angle 120^\circ$	$1.1\angle 240^\circ$
14	$1\angle 0^\circ$	$1.55\angle 120^\circ$	$1.13\angle 240^\circ$
20	$1\angle 0^\circ$	$1.9\angle 120^\circ$	$1.1\angle 240^\circ$

In a real application, input current THD of the proposed scheme is affected by the unbalanced input voltage. That occurs due to the increase of the ripple voltage on the DC bus due to input voltage unbalance. This fact is based on the Fourier equations of the DC bus voltages on (4.6) through (4.19); any unbalance in the input voltages makes voltage segments on Figure 4.6 non-uniform. That makes the even triplen components on the DC bus to increase. These components are normally known as output voltage ripples.

The higher the input voltage unbalance, the higher the ripple voltage on the DC bus. As the ripple increases, the AC current flowing through the DC load will increase. This affects the current flowing through point A to K in Figure 4.11 (I_{AK}), so it deviates from ideal value as stated in the subchapters 4.2 and 4.3, thus increasing the input current THD.

4.11 The Bi-directional Switch Controller

In three-phase controlled rectifier at any given time, there are two phases in conduction state and one in non-conduction state. With the proposed method, line that is in non-conducting state will be connected to the injection circuit by means of a bi-directional switch. Since there are three lines, it needs be determined which line is to be connected.

To realize which of the three lines should be connected to current shaping network, one has to analyze the following thyristor gating timing table presented in Table 4.2

Table 4.2 Thyristor Gate Timing
(Shaded square-switch on while non-shaded square-switch off)

[illegible]

If T1 or T4 is triggered (see Figure 4.12), then phase R will enter into conduction state. Phase R will leave the conduction state while phase S is activated by triggering T3 or T6. Phase S will leave its conduction state while phase T is activated by triggering T2 or T5.

Figure 4.23 The switch controller schematic

It can be shown from table 4.2 that if T1 or T4 is triggered, phase T should be connected to the current shaping network. This is because when T1 or T4 are

triggered, phase R and phase S are in conduction state. At that moment phase T is left non-conducted. In other word, the switch on phase T is controlled by trigger pulse on T1 or T4. Respectively switch on phase S is controlled by trigger pulse on T2 or T5, and switch on phase R are controlled by trigger pulse on T3 or T6.

Figure 4.24 Main process flowchart

In the proposed method, the above control scheme is implemented in an MC68HC908KX2 microcontroller (Figure 4.23). Its program consists of two main parts. First is the main routine (figure 4.24) that in its entire live will only do an endless loop. The second function is the interrupt routine (figure 4.25). Thyristors trigger pulses are monitored by using the controller’s keyboard interrupt capability (PTA2-PTA4). Every time a trigger pulse is detected, an interrupt routine is generated. This interrupt routine will switch off all bi-directional switches, look-up the table 4.2 to determine next bidirectional switch that should be turned on, adjusting the dead time, then activate corresponding bi-directional switch through the I/O lines.

The flow chart presented in Figure 4.24 and Figure 4.25 show the routine for controlling the bi-directional switch states while Figure 4.26 show the bi-directional switches state changes based on table 4.2.

Figure 4.25 Interrupt Flowchart

Figure 4.26 Switch determination state diagram

Figure 4.27 Switch controller hardware realization

Figure 4.28 Bidirectional switch hardware realization

Figure 4.29, Figure 4.30, and Figure 4.31 show real measurements taken from the switching controller of the experimental prototype. Figure 4.29 illustrates the controller computation time. The computation time is the amount of time required to compute the output command after the controller receives a thyristor trigger pulse. It is shown that the computation time is 12.3 μSec . This time is fast enough for switches

controller requirement, as at least the new command should be ready at the end of the dead time period, which is 100 μSec (Figure 4.30).

The dead time is periode where all switches are in “off” state. This state should be present to prevent short circuit caused by two bi-directional switches stay in “on” state at the same moment.

Figure 4.29 Hardware based result of the controller computational time in response to a gating pulse command

Figure 4.30 Hardware based result of the bi-directional switch dead time

Figure 4.31 shows the proposed controller in its operation. It is shown that the controller produces three square pulses to control phase R, S, and T bi-directional switches. The control signal is shown aligned to phase R when the rectifier operate at $\alpha=10^\circ$.

Figure 4.31 Hardware based result of phase R, S, and T switches control signal referenced to phase R

5 PROPOSED RECTIFIER PERFORMANCE PARAMETERS

This chapter is divided into two major divisions; MATLAB based simulation results and the experimental results. MATLAB modeling is used to verify the theoretical idea and predicted result. It is also used to preview the voltage and current waveform that should be anticipated during a real application of the current injection scheme into a three-phase controlled rectifier. In MATLAB environment, a real circuit (switching devices, capacitors, inductors, resistors, etc) was built and the circuit performance could be verified.

5.1 MATLAB Results

5.1.1 Ideal Condition

A three-phase controlled rectifier is presented considering only its ideal behavior i.e.: no input inductance, ideal DC load current and minimum or no commutation time are considered. Its ideal condition yields the best achievable result of the proposed current injection scheme.

Figure 5.1 through Figure 5.11 show the waveform of the proposed controlled rectifier. The waveforms are presented in per-unit that is normalized to its maximum value. The spectra graphs are presented by normalizing to its fundamental component or third harmonic whichever is having the highest magnitude on the respective snapshots.

It shows in Figure 5.1 that in this ideal condition, voltage and current is in-phase hence resulted in a unity DPF (Displacement Power Factor).

Figure 5.1 Rectifier input voltage and current waveform up to 30° delay angle under the proposed scheme

Figure 5.2 shows the input current spectrum of Figure 5.1. It is shown that only the fundamental component is present. From numerical calculation of the FFT (Fast Fourier Transform) result, the THD of the input current is around 0% under this ideal condition.

Figure 5.2 Typical input current spectrum up to 30° delay angle under the proposed scheme

Up to 30° delay angle, the input voltage and current waveform will not differ from what has shown in Figure 5.1. However, it was found that the injection current shape and magnitude is increased as α increases. Figure 5.3 and Figure 5.4 show the injection current at zero delay angle (α) and at twenty-degree delay angle. The spectra characteristics show that the injection current is mainly the third harmonic ($3f$).

Figure 5.3 Injection current waveform and its spectrum at $\alpha=0$ under the proposed scheme

Figure 5.4 Injection current waveform and its spectrum at $\alpha=20$ under the proposed scheme

Figure 5.5 Input voltage and current waveform at $\alpha=40$ under the proposed scheme

Beyond 30° delay angle, input current waveform starts to be distorted (Figure 5.5 and Figure 5.8). The higher the delay angles the higher the distortion present. However, distortion is observed in the input current beyond 30° delay angle. But, at that operating point, the fundamental current is still in-phase with the input voltage. It results in unity DPF.

Figure 5.6 Input current spectrum at $\alpha=40$ under the proposed scheme

Figure 5.7 and Figure 5.10 show the injection current waveform and its spectrum when the delay angle is above 30° .

The input current spectra graphs (Figure 5.6 and Figure 5.9) show that beside the fundamental current other harmonic components have started to show up. These spectra components affect the input power quality by increasing the input current THD. Figure 5.11 shows the input current THD response curve under its recommended operating area of the proposed controlled rectifier (0 - $50^\circ \alpha$).

Figure 5.7 Injection current waveform and its spectrum at $\alpha=40$ under the proposed scheme

Figure 5.8 Input voltage and current waveform at $\alpha=60$ under the proposed scheme

Figure 5.9 Input current spectrum at $\alpha=60$ under the proposed scheme

Figure 5.10 Injection current waveform and its spectrum at $\alpha=60$ under the proposed scheme

The overall input current THD under ideal condition is summarized on Figure 5.11. It is shown that beyond 30° delay angle the input current THD is increasing sharply. This is happened as the input current discontinuity is become larger as described in sub chapter 4.6.

Figure 5.11 Input Current THD vs. delay angles under ideal operating condition for the proposed converter

5.1.2 Effect of Line Inductance

The input inductance makes the input current waveform slightly out of phase from the input voltage waveform. Figure 5.12 shows the input voltage and current waveform when the input inductance between one to four mili-Henry is considered in the simulation. The phase difference between voltage and current waveform is stated by using Φ symbol on the figure. The difference makes the DPF less than unity.

Figure 5.12 Typical input voltage and current waveform with certain line inductance

Figure 5.13 shows the input current THD while the effects of the input inductance are incorporated. It is evident on the graphs that the higher the line inductance, the lower the THD especially after $\alpha=30^\circ$. Below 30° delay angle, input current THD is minimal and are negligible due to the proposed circuit is performing the resistive emulation perfectly as stated on the subchapter 4.6.

Figure 5.13 THD vs delay angle for various value of line inductances

5.1.3 Effect of Unbalanced Input Voltages

The proposed scheme is tested under unbalanced input voltage condition as well. V_a is the phase that is used as a reference. Its amplitude will be kept constant all the time. V_b and V_c are the variables. Their amplitudes will be varied to test the scheme response to the unbalance input voltage conditions. V_b will be set lower by some percentage of V_a while V_c will be set higher (Figure 5.14). Therefore, certain value of the degree of unbalance (u) in equation (4.110) can be achieved.

Figure 5.14 Input voltages at unbalance condition

The simulation result is presented on Figure 5.15. It is shown in the figure that under balance condition, delay angle vs. THD characteristic is similar to Figure 5.11. At this condition, the transition point where the delay angle vs. input current THD gradient changes into a steepest slope is about 30° . The point is called a *knee point*.

The figure also shows that the knee-point advances as the degree of unbalance increases. It is evident from Figure 5.11 that the knee point become about 23° delay angle on 50% input voltage unbalance from 30° delay angle under balance input voltage condition. This results in higher average input current THD when higher degree of input voltage unbalance presents.

Figure 5.15 Input current THD response with unbalance factors and delay angle

5.1.4 Finite Load Inductance Effect

It is unlikely to have an infinite smoothing inductance on the DC load side in a real controlled rectifier. This condition results in the lower THD suppression capability of the proposed scheme. Equation (4.41) shows that the ripple voltage component on the

DC side will increase by factor $\sqrt{\cos 2\alpha}$ while α is increased, hence the THD response of the proposed scheme will also increase by that factor.

Figure 5.16 shows the THD response on a finite load inductance condition. It can be shown that up to 30° delay angle, the THD increases proportional to the DC ripple voltage factor. However, beyond 30° delay angle, the steepest THD response curve is present due to the present of a non-conduction factor stated on sub-chapter 4.6. The factor generates current discontinuities that increase the current non-linearity and hence generate more harmonic distortion on the input current.

Figure 5.16 Input current THD response for various delay angles and load time constants

5.2 Experimental Result

An experimental work based on a prototype 1kW three-phase rectifier was conducted to verify the MATLAB simulation result (Figure 5.17). The rectifier has line inductances of 2 mH each, DC bus inductance of 10 mH, and a resistive load of 10 ohms. Slightly unbalanced input voltages of about 2% were measured. This is because the inherent unmatched impedance on the variac that was used on the experiment. The proposed circuit schematic on Figure 5.18 is used as a reference of the voltages and currents that subsequently will be presented.

Figure 5.17 Proposed rectifier hardware implementation

Figure 5.18 Circuit schematic of the proposed rectifier power factor corrector

Figure 5.19 and Figure 5.22 show the input voltage (V_a), input current (I_a) and the injection current captured by oscilloscope. The waveforms verify the result of the MATLAB model. The waveforms are shown for a certain delay angles (α)

Figure 5.19 Experimental waveform for input voltage and current at $\alpha=10$

Figure 5.20 Experimental waveform of the Injection current at $\alpha=10$

Figure 5.21 Experimental waveform of input voltage and current at $\alpha=50$

Figure 5.22 Experimental waveform of the injection current waveform $\alpha=50$

In addition to the conventional oscilloscope based waveforms, the results are also captured using a FLUKE 43B power analyzer. This advanced harmonic analyzer shows real time values of important performance parameter, i.e. THD, DPF, PF, etc.

Figure 5.23 and Figure 5.24 show power analyzer results. On-line power quality parameter like, THD (Total Harmonic Distortion), PF (Power Factor), DPF (Displacement Power Factor), and the spectra characteristics are presented. Table 5.1 presents the overall performances of the hardware experimental result, where THD is rectifier input current total harmonic distortion, η is the rectifier efficiency, P_{inj} is ratio of the power dissipated in the injection circuit to the rectifier total input power, and PF is the rectifier power factor. They are defined as follows:

$$\eta = \frac{P_{load}}{P_{in}} = \frac{(V_{Load} \cdot I_{Load})}{(V_a \cdot I_a) + (V_b \cdot I_b) + (V_c \cdot I_c)} \tag{5.1}$$

$$P_{inj} = \frac{P_{in} - P_{load}}{P_{in}} = 1 - \eta \tag{5.2}$$

$$PF = \frac{I_1}{I_{in\,RMS}} \cos \angle V - 1 \tag{5.3}$$

Table 5.1 On line Performance Parameters at Various Delay Angles Obtained Through Spectrum Analyzer

	$\alpha=0$	$\alpha=20$	$\alpha=40$	$\alpha=60$
THD	4.7%	5.1%	7.5%	18.7%
η	91.0%	78.7%	52.8%	33.1%
P_{inj}	8.9%	21.2%	47.1%	66.8%
P.F	0.99	0.99	0.99	0.98

Table 5.2 below compares the input current THD parameters of the experimental setup on table 5.1 to matlab result in sub chapter 5.1.1, 5.1.2, and 5.1.3. However, it is taken only on the condition that is closely related to the experimental setup that is 2mH input line inductance, 10mH and 10Ω load and about 2% input voltage unbalance. It is shown that the experimental setup THD is higher than all Matlab simulations result. This is can be explained by realizing that the matlab models are only calculating the THD based on the individual parameters, i.e. ideal condition, particular input inductance, and specific load time constant while experimental results are the real world mixture interaction between the mentioned paramenterers.

Table 5.2 Comparison of the input current THD of experimental result and Matlab model

THD	$\alpha=0$	$\alpha=20$	$\alpha=40$	$\alpha=60$
Experimental Setup	4.70%	5.10%	7.50%	18.70%
Matlab-Ideal Condition	0.20%	0.35%	5.10%	14.00%
Matlab-2mH input inductance	0.18%	0.31%	5.00%	13.10%
Matlab-1mSec Time Constant	0.27%	0.40%	6.90%	16.98%

In order to show the effectiveness of the proposed scheme, the results are compared to that of a conventional converter. Figure 5.25 shows the input voltage and current of a conventional three-phase controlled rectifier at $\alpha=0^{\circ}$. It is shown that the rectifier input current harmonic is high. Therefore, the input current THD of the rectifier is nearly 30%. It results in a poor AC power quality.

Figure 5.23 Proposed rectifier input voltage and current waveforms, their harmonic, and power quality parameter (PF, DPF, THD) at $\alpha=10^\circ$

Figure 5.24 Proposed rectifier input voltage and current waveforms, their harmonic, and some power quality parameter (PF, DPF, THD) at $\alpha=45^\circ$

Figure 5.25 Input voltage and current waveforms of a conventional three-phase controlled rectifier, their harmonic, and some power quality parameter (PF, DPF, THD) at $\alpha=0^\circ$

6 CONCLUSIONS AND RECOMMENDATION

6.1 Conclusion

Three-phase thyristor based controlled rectifier is common in high power AC-DC conversion. However, rectifier exhibits nonlinear characteristics resulting in poor input power factor. Further, the nonlinear nature of rectifier injects significant harmonic currents into the utility resulting in a number of undesirable effects such as disturbing the operation of nearby sensitive equipment and over-current in a three-phase distribution system neutral conductor [3]. With stricter regulations on network harmonic pollution, the three-phase controlled rectifier at present day is required to be harmonic-free, preferably at unity power factor and highly efficient.

This work proposes the current injection method to enhance the input power quality of a three-phase controlled rectifier. It also enhances the previous research works conducted by previous researchers with several improvements such as lower cost, lighter weight, and superior input current THD suppression capability.

The new scheme uses three static semiconductor bi-directional switches to change the three-phase transformer on the previous schemes. This upgrading drastically reduces the proposed rectifier overall weight, as the bidirectional switches is much lighter than a transformer with the same power rating. In addition, the transformer used in

the previous schemes tends to be more expensive and slow in response than the proposed switches. Therefore, this also reduces the overall cost and enhances compactness of the proposed rectifier.

A superior input current THD suppression capability can be achieved by utilizing a new type of current processor circuit [11]. The circuit reduces the input current THD by injecting all odd triplen harmonic current to the input side of the rectifier. This in contrast to the previous scheme that only injects the third harmonic current to the rectifier input. In addition to performing a superior input current THD suppression capability, the proposed scheme current processor is simpler than the previous schemes. It does not require a tuned circuit to select a particular harmonic current. Therefore, a simple, light weight, and low cost R-C current processor replaces the previous bulky and expensive R-L-C circuit. Two methods to select the R-C parameters on the current processors has been presented and can be summarized as follows :

Table 6.1 Summary of R-C Parameter Selection on The Proposed Current Processor

	Spectra Analysis Based		Circuit Transformation Based	
	Symbol	Value	Symbol	Value
Base Parameter	R_e	$\frac{1}{2} \frac{V_{DC(rms)}}{I_{DC(rms)}} \Big _{\alpha=0}$	Z_{load}	$\frac{V_{DC(rms)}}{I_{DC(rms)}} \Big _{\alpha=0}$
1 st R Parameter	R_{odd}	$3 \cdot R_e$	$Z_{AI} \text{ \& } Z_{KI}$	$\frac{3}{2} \cdot Z_{load}$
2 nd R Parameter	R_{even}	$2 \cdot \frac{3}{2} \cdot R_e$	Z_{AKAC}	$\frac{3}{2} \cdot Z_{load}$
Capacitors	$\gamma = 3\omega_o R_e C$ & Figure 6.1			

A microprocessor based novel switch control scheme is incorporated in the proposed rectifier. Detailed algorithm, expression, and the controller circuit diagram are developed. Its performance is also analyzed. The controller is characterized by fast, low cost, simple, lightweight, and robust properties.

The proposed scheme performs very well up to certain delay angles yielding very high PF and low input current THD. However, the performance degrades somewhat toward high delay angles, but a converter rarely operates in that range. The proposed topology can be a good retrofit to the existing thyristor based DC drives and uninterrupted power supply (UPS) application.

6.2 Future Work

Based on the basic principle of the current injection that is presented in this thesis, a *non-unity* displacement power factor (DPF) solution for the three-phase controlled rectifier can be proposed and is worth working upon. The non-unity term means that instead of keeping the DPF unity and reducing its input current THD like on the proposed scheme, the future scheme works only by reducing the input current THD, therefore the higher the delay angle, the lower the DPF. However, the input current THD of the rectifier will be kept low by injecting the delay angle synchronized odd harmonic to the rectifier input side. This should be done to improve the proposed

rectifier efficiency as in the currently proposed scheme; efficiency is reducing when the delay angle is increasing.

Figure 6.2 gives an ideal condition of the idea described. The current injection circuit will modify the input current behavior as if the three-phase voltage sources are connected to a three-phase L-R star connected load. In fact, Figure 6.1 is almost similar to Figure 4.4 (c). The Z_1 to Z_3 represents the same concept, which is representing resistive loads. The difference lays on the inductors. The inductors shown on the figure are virtual variable inductors. Those inductors represent the delay angle concept. The higher the delay angle of a three-phase controlled rectifier will make the voltage sources sense the higher inductance connected to it. Therefore, the lower the DPF is.

When the delay angle increases, the phase angle between voltage and current is also increases. Similar condition happens when the inductance on the equivalent circuit of Figure 6.2 increases. The same voltage-current phase displacement phenomena are also happened on a conventional three-phase controlled rectifier. But, with future injection current scheme, the input current THD of the rectifier will be kept low even the DPF is increasing. This can be done by injecting an optimal current magnitude and phase of the odd triplens harmonic synchronously with the delay angle. However, in order to keep the input current THD low, it should be noted that the even triplens

harmonic on the DC bus should also be managed so it should be in its optimal value as described in chapter 4.

Figure 6.2 Future low input current THD controlled rectifier with variable DPF ideal circuit

An active current processor will be unavoidable for the future works. Careful examination of the existing active current processor to be matched with the future scheme requirements should be done prior to its application. Even the complexity will increase; the active solution will give some possibility to apply this scheme on an active load like motor application.

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BIOGRAPHY

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APPENDIX A
IEEE 519 HARMONIC LIMITS

Table A.1. Current Distortion Limits for General Distribution Systems
(120V-69kV)

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	<11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.						
*All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L .						
where						
I_{sc} = maximum short-circuit current at PCC.						
I_L = maximum demand load current (fundamental frequency component) at PCC.						

Note: harmonic current limits for non-linear load connected to a public utility at the point of common coupling (PCC) with other loads at voltages of 2.4-69kV. I_{sc} is the maximum short circuit current at PCC. I_L is the maximum fundamental-frequency load current at PCC. Even harmonic are limited to 25% of the harmonic limits above[23].

Table A.2. Current Distortion Limits for General Distribution Systems
(69kV-161kV)

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	<11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD
<20*	2.0	1.0	0.75	0.3	0.15	2.5
20<50	3.5	1.75	1.25	0.5	0.25	4.0
50<100	5.0	2.25	2.0	0.75	0.35	6.0
100<1000	6.0	2.75	2.5	1.0	0.5	7.5
>1000	7.5	3.5	3.0	1.25	0.7	10.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.						
*All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L .						
where						
I_{sc} = maximum short-circuit current at PCC.						
I_L = maximum demand load current (fundamental frequency component) at PCC.						

Table A.3. Current Distortion Limits for General Distribution Systems
(>161kV)

Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	<11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	THD
<50	2.0	1.0	0.75	0.3	0.15	2.5
≥50	3.0	1.5	1.15	0.45	0.22	3.75
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.						
*All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L .						
where						
I_{sc} = maximum short-circuit current at PCC.						
I_L = maximum demand load current (fundamental frequency component) at PCC.						

Table A.2 Maximum Amplitudes of Harmonic Current in TCR

Harmonic Order Present		Harmonic Order Present	
1	100	3	(13.78)
5	5.05	7	2.59
9	(1.57)	11	1.05
13	0.75	15	(0.57)
17	0.44	19	0.35
21	(0.29)	23	0.24
25	0.20		

NOTE: Those harmonics in parentheses are triplens.

Table A.3 Six Pulse Converter Harmonics

Harmonic Order	Frequency Hz	Sequence Network	Stator Harmonic	Harmonic Rotation	Rotor Harmonic
1	60	+	1	Forward	—
5	300	—	5	Backward	6
7	420	+	7	Forward	6
11	660	—	11	Backward	12
13	780	+	13	Forward	12
17	1020	—	17	Backward	18
19	1140	+	19	Forward	18
23	1380	—	23	Backward	24
25	1500	+	25	Forward	24

Fig. A.1. Six Pulse Rectifier with DC Ripple 5th Harmonic as a Function of DC Ripple

Fig. A.2. Six Pulse Rectifier with DC Ripple 7th Harmonic as a Function of DC Ripple

Fig. A.3. Six Pulse Rectifier with DC Ripple 11th Harmonic as a Function of DC Ripple

Fig. A.4. Total Power Factor of Six-Pulses and 12-Pulses at $\alpha=0$

APPENDIX B

Controller and Bi-directional Switch

Fig B.1 Controller circuit

Fig B.2 bi-directional switch circuit

Figure B.1 is the controller unit. It senses the thyristors trigger pulses through PTA2, 3, and 4. PTA2 senses thyristors number 1 and 4, PTA3 senses thyristors number 3 and 6, while PTA4 senses thyristors 2 and 5. After processed by the controller routines, PTB2, 3, and 4 produce the bidirectional switches (figure B.2) control pulses. The output *Phase 1*, 2, and 3 in Fig. B.1 are connected to *control* in figure B.2. All input and output ports of the microcontroller are isolated from the high voltage by opto-isolators.

APPENDIX C

Controller Routine

The controller routine consists of two main parts :

1. The Main Routine
2. KBI Interrupt Service Routine

The Main routine is doing the following jobs:

1. **Initialization of the Timer Unit.** This is important, as the controller should have a precise base time for generating correct dead time in the switching sequences.
2. **Port Initialization.** This step makes a correct assignment on each port being used. Whether it is an input with interrupt or assigned as output.
3. **RAM Initialization.** This step will make all cells in the RAM zero (0).
4. Initialization of the Keyboard interrupt to capture the thyristors trigger pulses.

The KBI Interrupt Service Routine is doing the switching control algorithm. This interrupt is interrupting the main routine every time a thyristor trigger pulse arise and producing a correspondence output command through port B to a particular bi-directional switch. The control flowchart of main routine and KBI interrupt are shown in figure 4.24, 4.25, and 4.26.

 *BIDIRECTIONAL SWITCH CONTROLLER

*Project : NOVEL NEAR UNITY POWER FACTOR CONTROLLED RECTIFIER
 *Microcontroller : Motorola MC68HC908KX2
 *compiler : Pemicro-WinIDE for KXseries
 *clock : 10 MHz external crystal = 0.4uSecBus
 *input : active low on PTA2, PTA3, PTA4
 * : PTA2=D1, D4;PTA3=D3,D6; PTA4=D5,D2
 * : captured with Keyboard Interrupt (KBI)
 *output : active high on PTB2, PTB3, PTB4

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 *Supervisor : Assoc Prof Ali Iftekhhar Maswood
 *Power Division, School of Electrical and Electronic Engineering
 *Nanyang Technological University - Singapore

 *REVISION HISTORY

*Rev1 : 23 September 2003 : 15.41
 *Rev2 : 03 Oktober 2003 : 00.00 adding delay before on,
 * : routine on CONFIG register set
 *Rev3 : Faster response on interrupt, main just doing endless loop
 *Rev4 : Dead time change to 100uSec

 *CONVENTION

\$BASE 10T ;Unless stated different, number is in decimal

 *EQUATE

RAMStart EQU \$0040 ;
 ROMStart EQU \$F600 ;This is valid ROM address on the KX2 and KX8
 VectorStart EQU \$FFDC ;Starting address of KX Vector address
 ClockSpeed EQU 10 ;10Mhz/4*4 clock Speed for delay function
 \$Include 'D:\pemicro\ics08kxz\kxregs.inc' ;Predefined KX Register Equate

 *MACRO DEFINITION

\$MACRO dly time ;Inserting delay multiple of 12uS
 lda #ClockSpeed ;(all finish in 9 cycle)
 ldx #%1\12 ;
 bsr DELAY ;
 \$MACROEND

 *VARIABLE DECLARATION

org RAMStart
 State_Counter rmb 1 ;track current state of input

```

*****
*CODE
*****
        org     ROMStart           ;The Program Start here at this address

*****

*DELAY
*This sub will delay 12 * n ms Delay
*entry conditions : register X contains the time/12 of delay (in uSec)
*register A contains the cpu speed*4 (rounded by 2 bits of precision)
*****
delay:   deca                     ;1cycle
nxtx:    psha                     ;2 (* by regX)
         deca                     ;1 (* by regX)
         deca                     ;1 (* by regX)
         dbnza *                  ;3 (* by regA-1)
         pula                     ;2 (* by regX)
         dbnzx nxtx               ;3 (* by regX)
         rts                      ;4
****ENDSUB*****

*****

*Initialize RAM and Register
*all RAM position and A, H, X register will be cleared
*****
Init_RAM:  clra                   ;
          clrh                    ;
          clrx                    ;
          ldx    #$FF-5-$40+1      ;RAM address is $40 to $FA, still maintain the stack
loop_Init_RAM: sta    $3F,x        ;
          dbnzx  loop_Init_RAM    ;
          rts                      ;
****ENDSUB*****

*****

*Initialize Port A and Port B
*PTA is Input, PTB is Output
*****
Init_PORT:  mov     #$00,PTAPUE    ;
          mov     #$00,DDRA        ;
          mov     #$00,PTB         ;
          mov     #%00111100,DDRB ;
          rts                      ;
****ENDSUB*****

*****

*Initialize The clock Source (ICG) to 10MHz External Crystal
*Clock Monitor and clock interrupts are not enabled
*This routine SHOULD NOT be called when debugging!
*****
Init_ICG:   mov     #%00001010,CONFIG2 ;r,r,extxtalen,extslow,extelkon,r,osceninstop,scibdsrce
          mov     #%01001101,CONFIG1 ;coprs,lvistop,lvirstd,lvipwrdr,lvi5/3,ssrec,stop,copd
          lda     #$13              ;Mask for CS, ECGON, ECGS
loop_ICG:   sta     icger            ;Try to set CS, ECGON and clear ICGON
                                     ;ICGON will not clear until CS is set
                                     ;CS will not set until ECGON and ECGS are set.

```



```

        cmpa   icger                ;Check to see if ECGS set, then CS set,
                                   ;then ICGON clear
        bne    loop_ICG             ;Keep looping until ICGON is clear.
        rts                          ;
****ENDSUB*****

*****
*Initialize KBI
*Interupt happened on Edge only
*****
Init_KBI:   mov     #$02,KBSCR       ;interrupt on falling only, but interupt still not allowed
            mov     #$04,KBIER       ;KBD2 is current interupt source
            bset    2,KBSCR          ;acknowledge any KB interupt
            bclr    1,KBSCR          ;ready to receive KB interupt
            rts ;
****ENDSUB*****

*****
*MAIN PROGRAM
*****
start:      bsr     Init_ICG         ;initialize the Clock Generator
            bsr     Init_PORT        ;initialize Input and Output function of The Port A and B
            bset    5,PTB            ;a sign that the timer initialization is finish
            bsr     Init_RAM         ;Clear All Register and RAM
            bsr     Init_KBI         ;initialize for capturing the pulse
            dly     3000             ;wait for 3000 us, until rectifier stabilized
            cli     ;                ;ready for interupt
loopStart:  bra     *                ;endless loop

****ENDMAIN*****

*****
*KBI_ISR
*****
;after ON, first interupt should come from phase R first
kbi_isr:    pshh     ;                ;saving the H register state
            clr      KBIER           ;Prevent another interupt
            ldx      State_Counter   ;the state counter. Implemented through ring counter
            lda      TABLE_IntSeq,x ;load next interupt and new switch state
            mov      #0,PTB          ;make all bidirectional switch off

            psha     ;
            pshx     ;
            dly      72              ;about 400nSec offtime
            pshx     ;
            psha     ;

            sta      PTB             ;(3)set a new state on bidirectional switch
            sta      KBIER           ;KBIER point to next phase int source
            incx     ;                ;X is current state counter value holder.
            cpx      #3              ;state counter will be resetted to 0 if current count is 3
            bne      kbi_isrNext    ;
            clrx     ;
kbi_isrNext: stx      state_Counter   ;renew the current state counter value
            bset     2,KBSCR          ;guard for re-triggering of the interupt
            pulh     ;
            rti     ;

```



```
****ENDISR*****

*****
*TABLE
*****
TABLE_IntSeq: db %00010000,%00001000,%00000100 ;C,B,A
*****
*DUMMY_ISR-Dummy Interrupt Service Routine.
*Just does a return from interrupt.
*****
dummy_isr: rti ;return
****ENDISR*****

*****
*Vectors-Specifying Reset, Timer, ADC Interrupt Routines
*****
org VectorStart
dw dummy_isr ;Time Base Vector
dw dummy_isr ;ADC Conversion Complete
dw kbi_isr ;Keyboard Vector
dw dummy_isr ;SCI Transmit Vector
dw dummy_isr ;SCI Receive Vector
dw dummy_isr ;SCI Error Vector
dw dummy_isr ;Reserved
dw dummy_isr ;Reserved
dw dummy_isr ;Reserved
dw dummy_isr ;Reserved
dw dummy_isr ;Reserved
dw dummy_isr ;TIM Overflow Vector
dw dummy_isr ;TIM Channel1 Vector
dw dummy_isr ;TIM Channel0 Vector
dw dummy_isr ;CMIREQ Vector
dw dummy_isr ;~IRQ1 Vector
dw dummy_isr ;SWI Vector
dw start ;Reset Vector
****ENDVECTOR*****
```