Nano-scale characterization of advanced gate stacks using transmission electron microscopy and electron energy loss spectroscopy

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

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GATE STACKS USING TRANSMISSION ELECTRON
MICROSCOPY AND ELECTRON ENERGY LOSS
SPECTROSCOPY**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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SUMMARY

This thesis introduces a series of characterization methodologies which bridge the microscopic properties of material at interfaces with the macroscopic characteristics of a semiconductor device. The gate stacks of metal-oxide-semiconductor field effect transistors (MOSFETs) are used in this study as examples to demonstrate the advance of the nano-scale characterization. The objective of this thesis focuses on decoding the nature of the post-breakdown insulator-to-conductor transition when a leakage path is formed in the gate dielectrics, and its impact on device performance and reliability. The failure of the gate dielectrics in both conventional polycrystalline-silicon/silicon-oxynitride (Poly-Si/SiON) and new generation metal-gate/high- κ (MG/HK) gate stacks have been studied both electrically and physically with the aid of transmission electron microscopy (TEM), energy dispersive X-ray spectrometry (EDS) and electron energy loss spectrometry (EELS). The associated dielectric degradation has been correlated with the microstructural changes during the breakdown (BD) to understand the mechanisms of the dielectric failure. It is found that the oxygen deficiency is one of the fundamental physical defects responsible for the formation of the percolation path in both SiON and HK gate dielectrics. However, the post-breakdown degradations of MG/HK gate stacks show remarkable differences as compared with Poly-Si/SiON and depend strongly on the gate material. The physical defects that responsible for the novel failure mechanisms in MG/HK systems are identified. The impacts of the physical defects on device reliability are also addressed in this thesis.

For Poly-Si/SiON gate stack, oxygen deficiency in the percolated SiON is measured

using EELS and suggested to be the dominating defect responsible for the formation and evolution of the percolation path. The atomistic changes of the chemical bonding in the nano-scale breakdown path are extensive and irreversible. Oxygen atoms are washed-out with formation of the intermediate bonding states of silicon (Si^{1+} , Si^{2+} , and Si^{3+}) in the percolation path. The distribution of the oxygen deficiency in the percolation path is non-uniform and spreads out radially from the center to surrounding areas. The conduction band edges of the defective oxide are lowered from 0.14 eV to 0.78 eV when the Si-O composition changes from $\text{SiO}_{1.76}$ to $\text{SiO}_{0.7}$. In addition, the outer shells of the percolation path contribute significantly to the random switching of current levels in the early stage of the progressive breakdown, which is also known as digital-breakdown. When the oxygen in the inner core of the percolation path is fully depleted, the defective oxide network transforms into a stable configuration and pushes the post-breakdown conduction to analog-breakdown in which the random telegraphic noise of the gate leakage current is no longer visible.

The degradation of percolation path also depends on the gate material, especially for metal gate stacks. For TaN/HfZrO₄/SiO_x gate stack under high current injections, Ta metal atoms from the gate electrode can migrate into the percolated HK dielectrics and form highly conductive filament. The metal filament induces a ultrafast post-breakdown degradation and significantly reduces the reliability margin of the transistor. On the other hand, the percolation path in the SiON and HK dielectrics can be partially repaired for NiSi gated stacks. The dielectric breakdown induced metal migration (DBIM) constructs a metal-insulator-metal structure which facilitates the diffusion of oxygen vacancies and/or Ni metal filamentation in the vicinity of the percolation path under different biasing conditions.

Moreover, the flatband voltage (V_{FB}) shift induced by varying metal gate Ti/N ratio is investigated. The interfacial dipoles formed at the metal-gate/high- κ and high- κ /interfacial-layer interfaces are identified to be responsible for the negative V_{FB} shift for sub-stoichiometric TiN_x gate.

In summary, leveraging on the nano-scale physical characterizations, the local material properties are extracted and comprehensive understanding of the post-BD device performance is achieved for better device design for reliability improvement and new innovations.

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LIST OF ABBREVIATIONS

BD	Breakdown
CVS	Constant voltage stress
CMOS	Complimentary metal-oxide-semiconductor
C	Capacitance
DBIE	Dielectric-breakdown-induced epitaxy
DBIM	Dielectric-breakdown-induced migration
D	Drain
EELS	Electron energy loss spectrometry
EDS	Energy dispersive X-ray spectrometry
EOT	Equivalent oxide thickness
E	Electric field
FIB	Focused ion beam
g_m	Transconductance
HBD	Hard breakdown
HRTEM	High resolution transmission electron microscopy
HfO ₂	Hafnium oxide
Hf	Hafnium
I	Current
I_g	Gate leakage current
I_s	Source leakage current
I_d	Drain leakage current
I_{sub}	Substrate leakage current
I_{ds}	Source to drain current
I_{sd}	Drain to source current
I_{gl}	Gate leakage compliance current limit
I_{dsat}	Drain saturation current
IL	Interfacial layer

IC	Integrated circuit
L	Gate length
MOSFET	Metal-oxide-semiconductor field effect transistor
M	Metal
mA	Mili ampere
μ A	Micro ampere
μ m	Micro meter
nm	Nano meter
N	Nitrogen
Ni	Nickel
O	Oxygen
Poly-Si	Polycrystalline silicon
PBD	Progressive breakdown
SCVS	Successive constant voltage stress
S	Source
SRAM	Static random access memory
Si	Silicon
SiO ₂	Silicon di-oxide
SBD	Soft breakdown
SiO _x N _y	Silicon oxynitride
SILC	Stress induced leakage current
Ta	Tantalum
TaN	Tantalum nitide
TEM	Transmission electron microscopy
Ti	Titanium
TiN	Titanium nitride
TDDDB	Time dependent dielectric breakdown
T	Temperature
T _B	Barrier thickness of constriction
V	Voltage
V _s	Source voltage

V_g	Gate voltage
V_d	Drain voltage
V_{sub}	Substrate voltage
V_{ds}	Source to drain voltage
V_{sd}	Drain to source voltage
$V_{gstress}$	Applied gate stress voltage
V_T	Threshold voltage
W	Gate width
Zr	Zirconium

LIST OF SYMBOLS

A	ampere
F	farad
μ	micro
κ	Dielectric constant
K	Kelvin
eV	Electron-volt
Ω	Ohm

CHAPTER ONE

INTRODUCTION

1.1 Background

The metal oxide semiconductor field-effect transistor is currently the device of choice for integrated circuits. A thermally grown silicon dioxide (SiO_2), forming the insulating layer between the control “gate” and the conducting “channel”, is considered as the most critical component of a MOSFET. Modern silicon processing technology has allowed MOSFET to be scaled down to sub-micron dimensions, realizing incredible gains in performance [1-3]. With the rapid scaling of CMOS devices, the thickness of the SiO_2 gate dielectric layer is approaching its physical limits ($\sim 12\text{\AA}$) due to the high leakage current caused by the quantum-mechanical tunneling. To overcome the fundamental limits for SiO_2 gate dielectric, a global effort is directed at both conventional and unconventional technologies that will remove obstacles to the next evolutionary step in scaling. Revolutionary approaches include introducing innovations in materials (e.g., dielectrics with higher κ values), transistor design, and packaging. High- κ materials such as La_2O_3 , ZrO_2 , CeO_2 and HfO_2 have been explored as the alternative gate dielectrics to overcome the leakage current problem.

The continuous downward scaling of gate oxide thickness, regardless of the advantages mentioned above, comes with some drawbacks [4-8]. One of the most severe drawbacks is that the reliability of gate dielectric largely degrades due to the presence of a considerably huge

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electric field across the gate dielectric and large gate leakage current (I_g). In particular, gate dielectric breakdown will lead to partial or total malfunctioning of a MOSFET. This may eventually degrade the overall performance of integrated circuits. Therefore, gate dielectric breakdown is one of the important fields in the study of device or circuit reliability, especially for nowadays advanced nanoscale CMOS technology.

Gate dielectric breakdown is generally defined as the loss of the insulating properties of gate dielectric. In other words, the occurrence of a dielectric breakdown event corresponds to a substantial decrease in the resistances of some of the local areas in gate dielectric. When the gate dielectric is subjected to a constant-voltage or current stress, electronic traps, such as electron, hole and neutral traps, will be gradually generated within the gate dielectric. A conductive percolation path [9-12], which allows the flow of a huge amount of I_g , will be formed in the gate dielectric as the density of electronic traps in the gate dielectric exceeds a critical threshold, and hence, a dielectric breakdown event is said to occur. As reported in all the related studies, the occurrence of a dielectric breakdown event is often associated with a sudden, abrupt increase in I_g . The overall process of stressing the gate oxide under a constant voltage or current and continuously creating electronics traps within the gate oxide until the occurrence of a dielectric breakdown event is known as time-dependent dielectric breakdown (TDDB) [13]. Typically, the reliability tests of gate oxide are carried out under accelerated stressing conditions such that the data of TDDB can be collected within reasonable windows of time, such as a few hours or days. Therefore, the results obtained from the reliability tests implemented under accelerated stressing conditions have to be extrapolated to nominal operating conditions. This process will be complicated by the fact that the physical mechanisms responsible for the gate dielectric wear-out and breakdown under accelerated stressing conditions could be different from those under

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nominal operating conditions [14-16]. Therefore, we need to study the mechanisms of oxide breakdown and use the physical model that best fits the experimental results for projection.

Gate dielectric breakdown tends to alter the electrical characteristics of a MOSFET. A breakdown mode is primarily applied to describe the effects of gate dielectric breakdown on the device performance. There are two major types of breakdown modes, which are soft and hard breakdown [17-21]. A MOSFET that experiences a soft breakdown will be considered as a partially failed device as it can still operate with degraded performance. Conversely, a MOSFET that experiences a hard breakdown will be considered as a totally failed device. The mechanism of dielectric breakdown for gate oxide has been studied for over 20 years, but the physical mechanism responsible for the breakdown or percolation path formation has yet to be clarified. This is mainly because the nature of dielectric breakdown for gate oxide is very complex and random. Several gate oxide intrinsic breakdown models have been proposed to interpret phenomena that have been observed during the occurrence of dielectric breakdown. Anode hole injection (AHI) model, thermochemical model and anode hydrogen release (AHR) model are some of the widely accepted gate oxide intrinsic breakdown models. Essentially, none of these models is capable of perfectly fitting all the experimental and simulation results.

Most of the breakdown phenomena are studied from the electrical point of view. Very few reports on the physical analysis of the breakdown phenomena can be found in the literature. Radhakrishnan *et al.* [22] and Pey *et al.* [23] reported that a dielectric-breakdown-induced epitaxy (DBIE) in the vicinity of gate area is associated with ultrathin gate oxide breakdown. The physical analysis results showed that DBIE is highly localized, and its formation depends on the stressing voltage polarity (i.e., cathode to anode) regardless of the compliance current and hardness of the breakdown. The suggested driving force behind the DBIE formation was thermal

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electromigration effect [24]. Recently, Rakesh *et al.* [25-27] reported several new failure mechanisms for breakdown in high- κ gate dielectrics. For poly-Si gate with HfO₂, grain boundary and field assisted multiple breakdowns were observed. Spacer interfacial breakdown and ball-shaped capping layer were also found for poly-Si/HfO₂ stack. Meanwhile, formation of metal-like filament was reported for TiN/TaN/HfO₂/SiO_x stack during substrate injection mode.

1.2 Motivation

Gate dielectric reliability has been an intensively researched topic for more than three decades, especially when the device dimensions are continuously scaled down. According to the report of the *International Technology Roadmap for Semiconductors (ITRS)*, equivalent oxide thickness (EOT) of 0.8-1.2 nm will be used for the conventional CMOS devices for the technology nodes of 65 and sub-65 nm, while the insulating layer is still made of silicon oxynitride. This is due to the very stringent requirements of I_g and device speed for microprocessor applications. At the same time, there is a very high level of activities in replacing the gate dielectric by high- κ materials. Intel has announced their high- κ and metal gate process for 45nm node in the 2007's International Electron Device Meeting (*IEDM*), which allows device scaling to continue until year 2013. From the reliability point of view, progressive breakdown (PBD) for ultrathin silicon oxynitride gate dielectrics is particularly important as it provides extra post-breakdown reliability margin. New failure mechanisms of metal-gate/high- κ gate stacks need to be identified and further studied, too. Hence, there is a need to study the physical mechanisms responsible for the post-breakdown degradation (e.g., the PBD) of the gate oxide in greater details and the microstructural defects associated with various degrees and hardness of breakdown for better

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understanding of the failure mechanisms in various high- κ gate stack MOSFETs. In this project, the electrical characteristics of the MOSFETs are measured by semiconductor parameter analyzer (SPA) and the physical properties of the dielectric layer are studied by transmission electron microscopy (TEM), scanning transmission electron microscopy (STEM), electron energy loss spectrometry (EELS), and electron dispersive X-ray spectrometry (EDS).

1.3 Objectives

The objectives of the research work are the following: (1) To understand the chemical nature of the insulator-to-conductor transition in ultrathin SiO₂ gate dielectrics; (2) To study the physical defects responsible for the digital and analog post-breakdown degradation of ultrathin SiO₂ gate dielectrics; (3) To investigate the failure mechanisms in the metal-gate/high- κ gate stack MOSFETs; and (4) To correlate the physical analysis results with the electrical results. The ultimate goal of this study is to link up the material properties of a breakdown path in gate dielectrics such as electronic and chemical structures with the electrical characteristics of a MOSFET on device level. By combining all the critical results, a complete theoretical framework can be built up to study the phenomenon and the evolution of dielectric breakdown. Based on the finding, it is envisioned that an accurate lifetime projection would be made for device reliability.

1.4 Organization of Thesis

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This thesis is divided into seven major chapters. The organization of thesis is presented as follows:

- *Chapter One* provides the background, the motivation, the objectives and the contributions of this project.
- *Chapter Two* is a literature review on the related research that has been done and gives an overview of ultrathin gate dielectric breakdown as well as physical characterization techniques based on TEM.
- *Chapter Three* explains the procedure and the details of experiments that are carried out in our studies.
- *Chapter Four* is the study of the chemical nature of the percolation path formed in ultrathin silicon oxynitride dielectrics.
- *Chapter Five* reveals the physical origin of digital-to-analog post-breakdown evolution.
- *Chapter Six* studies the novel failure mechanisms of high- κ /metal gate stack MOSFETs.
- *Chapter Seven* summarizes the impact of the physical defects found in the gate dielectrics on device reliability.
- *Chapter Eight* provides the conclusion and the future work of this project.

1.5 Contributions

Our studies focus on the physical characterization of the percolation path formed in gate dielectrics using Transmission Electron Microscopy, Electron Energy Loss Spectroscopy and Energy Dispersive X-ray Spectroscopy. Complementary to the understanding from electrical characterization, the local change in material properties such as electronic structure and chemical

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composition is acquired and analyzed. This thesis introduces a series of nanoscale characterization methodologies which bridge the microscopic properties of the material with the macroscopic characteristics of a semiconductor device. The gate stacks of metal-oxide-semiconductor transistors are used in this study as examples to demonstrate the advance of the nano-scale characterization. The key objective of this thesis focuses on decoding the post-breakdown chemical nature of the insulator-to-conductor transition when a leakage path is formed in the gate dielectrics, and its impact on device performance and reliability. The oxygen deficiency in the percolated silicon oxynitride is measured using electron energy loss spectroscopy and suggested to be the dominating defect responsible for the formation and evolution of the percolation path in ultrathin gate oxide. It is shown that the silicon nano-cluster formed at the inner core of the percolation path transforms the defective oxide network to a stable configuration and pushes the post-breakdown conduction to a higher level where the random telegraphic noise of the gate leakage current is no longer visible. The impact of the gate dielectric breakdown also depends on the gate electrode, especially for the new generation high- κ /metal-gate stacks. Our results show that under high current injection, the Ta metal atoms from the gate electrode migrate into the percolated high- κ dielectrics and form highly conductive filament. The metal filament induces an ultrafast degradation and significantly reduces its post-BD reliability margin. On the other hand, the percolation path in the high- κ dielectrics can be partially repaired for fully silicided NiSi-gated stacks. The dielectric breakdown induced metal migration forms a metal-insulator-metal structure which facilitates the diffusion of oxygen vacancies and/or Ni metal filamentation in the vicinity of the percolation path under different biasing conditions. Moreover, the flatband voltage shift induced by varying the gate Ti/N ratio is investigated. The interfacial dipoles formed at the metal-gate/high- κ and high- κ /interfacial-layer

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interfaces are identified to be responsible for the negative V_{FB} shift for sub-stoichiometric TiN_x gate.

The above work has been published in world-renowned conferences, such as *IEEE International Electron Device Meeting (IEDM)* and *International Reliability Physics Symposium (IRPS)*, as well as prestigious journals, includes *Applied Physics Letters (APL)*.

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LITERATURE REVIEW

2.1 Introduction

This chapter provides a review of the breakdown mechanisms in conventional silicon dioxide gate stacks and new generation high- κ gate stacks reported in the literature. A few dominant dielectric breakdown models, various failure mechanisms of breakdowns associated with gate dielectric breakdown, and different analysis methods are discussed.

2.2 Breakdown Modes

A breakdown mode is primarily used to describe the effects of gate dielectric breakdown on its device performance. There are two major types of breakdown modes, namely soft and hard breakdown [1-5]. A MOSFET that experiences a soft breakdown will be considered as a partially failed device as it can still operate with a degraded performance. Conversely, a MOSFET that experiences a hard breakdown will be considered as a totally failed device. Since a universal physical model explaining the failure mechanism in ultrathin gate oxide is still lacking; thus, the criterion in determining a dielectric breakdown event (i.e., soft or hard breakdown) still remains ambiguous. The breakdown mode of thick gate oxide with T_{ox} above 3-5 nm is mostly hard

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breakdown, while the breakdown mode of thin and ultrathin gate oxide with T_{ox} below 3-5 nm is either soft or hard breakdown. This also implies that gate dielectric breakdown in thin or ultrathin gate oxide may not be catastrophic.

Substantial progress has been made towards the understanding of soft and hard breakdown [1-5] on device operations and circuit functions, although a universally accepted criterion has yet to emerge. One of the common methods in differentiating soft and hard breakdown is based on the magnitude of post-breakdown conduction. Several detailed studies of the effects of gate dielectric breakdown on device failure show that gate dielectric breakdown at the source or drain terminal is more detrimental to device operations than that at the device channel. Moreover, it is found that the susceptibility of gate dielectric breakdown to hard breakdown, which is defined as the ratio of the prevalence of soft breakdown to hard breakdown, is voltage-dependent. Many studies have reported that ultrathin gate oxide is associated with a new type of dielectric breakdown mode, which is named as progressive breakdown. In general, progressive breakdown occurs when there is an anomalous increase in SILC with the absence of a thermal runaway. As compared with hard breakdown, progressive breakdown is still identified as a low-conduction state. Progressive breakdown has been at least classified into three different types, which are [6-8]:

1. Digital soft breakdown – It is characterized by a telegraph-switching pattern.
2. Analog soft breakdown – It is characterized by random noise.
3. Micro-breakdown – It is characterized by a current that is smaller than I_g in typical soft breakdown. It has yet been detected in devices with large gate oxide areas.

According to S. H. Lee *et al.* [10], soft breakdown corresponds to a localized physical damage at the interface of anode caused by tunneling electrons that travel in the conduction band of gate

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oxide. The damaged interface of the anode is then modeled as a series resistance with a trapezoidal potential barrier of a reduced “electrical” thickness of gate oxide. Since devices with soft breakdown normally do not experience significant variation, for some of the applications, the occurrence of soft breakdown does not necessarily imply device failure.

Hard breakdown, which is believed to be due to the presence of a thermal runaway, is a catastrophic damage in gate oxide. As compared with soft breakdown, hard breakdown is identified as a high-conduction state. When hard breakdown occurs, the characteristics of a device normally appear in a nearly resistor-like shape. S. Lombardo *et al.* studied hard breakdown from the point of views of stored energy in capacitors [11]. However, some of the researchers reported that the concept or model of stored energy in capacitors could not provide convincing explanation on occurrence of hard breakdown [12, 13]. Basically, most of the researchers agree that the physical origin of soft and hard breakdown is similar. It is believed that the major difference between soft and hard breakdown is the process of energy dissipation [12, 13]. During the occurrence of hard breakdown, the localized temperature at the vicinity of the percolation path may rise above the silicon melting point [14, 15]. As a result, this could lead to severe, irreversible microstructure damages [14, 16-21] within and in the vicinity of the gate oxide. S. Lombardo *et al.* suggested that if a high E_{ox} is maintained after the occurrence of hard breakdown, then the location of a percolation path formed within the gate oxide will propagate with the sound velocity from the initial position [11].

2.3 Silicon Dioxide Gate Oxide

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Silicon dioxide has been intensively used for more than four decades as the dielectric material to insulate the gate electrode from the channel of a field-effect transistor. With a large energy bandgap of 8-9 eV, silicon dioxide is considered as an excellent insulator. The nearly exclusive use of silicon dioxide in conventional complementary metal-oxide-semiconductor application is mainly due to the reason that silicon dioxide uniquely possesses the required combination of several chemical and physical properties. The interface between silicon dioxide and silicon is very stable. This results in good mobility of electrons and holes and low electronic states (or surface states) at the Si-SiO₂ interface. Furthermore, silicon dioxide is associated with relatively low trapping rates of holes and electrons and consists of excellent compatibility with the CMOS technology. The bulk resistivity of silicon dioxide is about 10^{15} Ω -cm, and the dielectric breakdown strength of silicon dioxide is about 10^7 MV/cm. The films of silicon dioxide can be grown by thermal oxidation on clean silicon surfaces, and hence, they can be made with extremely low densities of trapped charges. Note that the energy barrier between silicon and silicon dioxide for electrons and holes are about 3.1 eV and 4.5 eV respectively. The gate oxide plays an important role to couple the electric potential from the gate electrode to the channel of a field-effect transistor. Therefore, the best control of the channel of a field-effect transistor by the gate electrode can be obtained when the gate oxide is made as thin as possible.

2.3.1 Electronic Properties of Silicon Dioxide

The electronic structure and optical properties of silicon dioxide have attracted the attention of many researchers for years. This is because SiO₂ is one of the most fundamental oxide systems in terms of crystal structure, bonding, and its relationship to physical properties. SiO₂ exists in many polycrystalline, as well as amorphous forms under different thermodynamic conditions.

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Amorphous SiO_2 is vital to the electronic and glass industries; and crystalline varieties are important as precision oscillators and dielectric materials. The structures of almost all of these forms have been well determined and show a great variety in the local short-range order. The various allotropic forms of silicon dioxide include quartz, cristobalite, tridymite, coesite, stishovite and vitreous silica. With the exception of stishovite, all of these are known to be constructed from the same fundamental structural unit, the SiO_4 tetrahedron. In quartz, silica glass, cristobalite, and low tridymite, the SiO_4 tetrahedron is apparently quite perfect, with O-Si-O angles almost exactly equal to the tetrahedral value of 109.5° [22].

The primary differences in the structures of the various polymorphs can therefore usually be traced to the differences in the Si-O-Si angle. In α -quartz, the angle is 143.5° , while in silica glass it appears to vary between ~ 120 and 180° with a most probable value of $\sim 144^\circ$. Thus the amorphous form of SiO_2 has been thought to comprise networks of SiO_4 tetrahedra, with each oxygen atom being shared between two tetrahedra according to a random Si-O-Si angle. An accurate treatment of the electronic bonding is therefore essential to describe the disordered forms of SiO_2 . However, due to the complexity of the system, first-principles electronic structure calculations have only been performed so far for crystalline forms of SiO_2 . Numerical studies of amorphous (*a*-) SiO_2 have been limited to empirical classical potentials, which do not explicitly contain information on the electronic structure. Approaches like short range disordered cluster and *ab initio* molecular dynamics (MD) simulations [23] have been applied to extract the electronic band structures of amorphous SiO_2 . In practice, α -quartz SiO_2 is often used to simulate the properties of amorphous SiO_2 due to the similarities in the crystal and band structures, as shown in Fig. 2.1 (b). The short-range order (SRO) of *a*- SiO_2 is the same as in the 4:2

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coordinated crystals. However, it is the intermediate range order (IRO) and the lack of long-range order (LRO) that distinguished the α -SiO₂ from its c -SiO₂ counterpart [23].

Figure 2.1. (a) Band structure of α -quartz calculated with the pseudo-potential method, with the total density of states (DOS) superimposed on it (thick line). (b) Density of states (DOS) of (i) amorphous SiO₂ using MD (solid) and (ii) α -quartz SiO₂ (solid). Inserted dashed lines are XPS data [23].

The α -quartz has a hexagonal cell containing three SiO₂ molecular units. Structure of this crystal is considered to be the paradigm of all silicate compounds. The average Si-O bond length is 1.61 Å and the average Si-O-Si bond angle is 143.5°. Band structure calculation shows that the occupied bands consist of an upper valence band (VB) in between -4 eV and -9 eV derived from the nonbonding O 2p orbital and a lower VB of O 2p bonding orbital [24]. They are separated by a sizable gap. The O 2s band is much lower (-17~-20 eV). Furthermore, an indirect band gap of 5.59 eV was obtained, which was being underestimated. The VB top is very flat with a large hole effective mass. The conduction band (CB) has a minimum at Γ with an electron effective mass of

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about 0.5. The DOS show multiple structures in all three band regions. Such fine structures in DOS delineate the details of the bonding interaction in relation to the local structure [24], as shown in Fig. 2.1(a).

It had been reported that the calculated electronic density of states of *c*-SiO₂ and *a*-SiO₂ have subtle differences [22]. But these subtle differences of the DOS between two phases appear to be negligible compared to the similarity of their optical properties as has been suggested by previous experimental optical spectra [25]. Experimentally, the optical spectra in all SiO₂ phases with 4:2 coordination are the same [25]. Since SiO₂ is used in many different forms for various purposes, defects in SiO₂ have therefore attracted wide attention. The oxygen vacancy related defects in SiO₂ are called E' centers [26]. Six of these have been identified in quartz: E₁' , E₂' , E₄' , E₁'', E₂'', and E₃''. The single or double primes denote one or two unpaired electrons associated with the center and the subscripts distinguish between various centers having the same spin. A neutral O vacancy is generally assumed to be the precursor of this defect, prior to the trapping of a hole. When an oxygen atom linking two silicon dioxide tetrahedrons is missing, the short and the long-bond silicon atoms would symmetrically relax towards each other and interact to form a so-called strained silicon-silicon bond, as shown in Fig. 2.2.

Figure 2.2. Minimum energy configuration of the neutral O vacancy V_o^0 by forming Si-Si long bond.

2.3.2 Phenomenological Models for Gate Oxide Breakdown

The BD phenomenon in thin SiO₂ has been analyzed with several most probable physical mechanisms. First, an empirical model has been suggested on the basis of the experimental data showing the electric field dependence of TDDB [27]. The plot of the logarithm of the time-to-failure (t_{BD}) versus the applied electric field exhibited a straight line, i.e. $t_{BD} \sim \exp(-\gamma E)$, where E is the electric field and γ is electric field acceleration factor [28]. Later, a thermochemical model was hypothesized based on the electric field driven defect generation process, which supported the same observed dependence of the oxide lifetime on the electric field [29]. This model is named as the E-model. It describes that the applied electric field interacts with the weak Si-Si bonds (associated with the oxygen vacancies in the amorphous silicon dioxide film), and eventually breaks the weak bond and creates a permanent defect or trap [30].

A second physical model proposed was based on anode hole injection mechanism, which is also known as 1/E model [31-33]. In this model, tunneling electrons (due to Fowler-Nordheim tunneling) transferred energy to holes in the anode, where holes are injected back into the oxide film. The injected holes became trapped and modified the oxide potential barrier to enhance the additional electron injection and eventually a positive feedback process caused a current runaway, leading to breakdown. In this case the time to BD is proportional to the inverse of the applied electric field, i.e. $t_{BD} \sim \exp(\beta/E)$, where β is the electric field acceleration factor. It was also reported that holes could be generated in the oxide by impact ionization process at higher applied voltages ($\sim 9V$) [34]. At energies below $\sim 9V$ the anode hole injection was believed to take place via surface plasmon process [35-36]. There is evidence that energetic tunneling electrons release the atomic hydrogen from the anode, which causes defects in the oxide film [37].

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Another breakdown model known is anode hydrogen release (AHR) model. It is based on the release of atomic hydrogen from the anode by energetic tunneling electrons, which causes defects in the oxide film. This model postulated that electrons with sufficient energy could tunnel through the gate oxide potential and reach the anode. These energetic electrons release hydrogen (H) from the anode/gate oxide interface. The threshold voltage for this process to take place is approximately 5 V. The process has been shown to continue at voltages as low as 1.2 V [38, 39]. The released hydrogen diffuses through the gate oxide and generates electron traps in the gate oxide as shown in Fig. 2.3 (a).

Electron trap generation model has been established on the basis of the percolation theory known as the percolation model [40-42]. The parameters used to fit the experimental data are the trap radius and the fraction of defects to initiate the breakdown. Figure 2.3 (b) illustrates the percolation model where defects are generated randomly throughout the volume of the oxide film. As defect generation continues, defects can connect electrically between the cathode and anode, shown as the shaded spheres in Fig. 2.3 (b). It is clear that if the oxide thickness is made thinner, a percolation path can be formed with lower defect density. A device with larger area would also have a higher probability of having overlapping defects for the same oxide thickness.

The percolation model predicts that only one defect is necessary to initiate BD as oxide thickness approaches the diameter of a single defect (~ 0.9 nm). It is the most widely accepted model. But it should be mentioned that although the percolation model predicts many statistical features of ultrathin oxide BD, the parameters chosen, such as the defect's physical dimensions and density, may not relate to the actual defect's physical dimensions, density and the range of interaction. It has been also reported that the defect density used in the percolation model differs by a factor of 1000 when compared to the defect density determined by stress induced leakage

current (SILC) measurements. Also, defect generation may not be truly random in some structures where gate edge effects dominate the breakdown. The percolation model does not predict the temperature dependent breakdown either.

Figure 2.3. (a) The hydrogen release model. (b) Schematic illustration of the percolation-model based on traps generation and conduction via traps. A breakdown path is indicated by shaded spheres.

The objective of a gate dielectric breakdown model is to describe the lifetime of the gate oxide as a function of various parameters, such as, electric field, voltage, temperature, gate oxide thickness and device area. The basis of a gate dielectric intrinsic breakdown model may not be a physical model but it is a phenomenological model to describe the damage to the gate oxide and eventually leads to the occurrence of a dielectric breakdown event. In addition, the practical application of a gate dielectric intrinsic breakdown model is the projection of device lifetime from accelerated stressing conditions to nominal operating conditions.

2.3.3 Progressive Breakdown of Ultrathin Gate Oxide

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Progressive breakdown is a unique breakdown phenomenon that can only be observed in thin or ultrathin gate oxide [43-45]. After the occurrence of a dielectric breakdown event, instead of experiencing an instantaneous jump, I_g will degrade towards a device current criterion with a relatively gradual profile, and thus, this breakdown transient is known as progressive breakdown. In other words, progressive breakdown can be treated as a process for the evolution of soft breakdown into hard breakdown. The study of progressive breakdown becomes increasingly important as the post-breakdown reliability margin or residual time of a MOSFET is believed to be closely dependent on progressive breakdown. Until recently, various new electrical approaches and physical characterization techniques have been developed or employed to study progressive breakdown. More useful insights can be obtained from different aspects, and thus, this further improves the understanding on the physical processes involved in causing gate oxide to break down. This in turn would make the lifetime extrapolation of very narrow devices with thin or ultrathin gate oxide become more accurate and help in exploring new avenues for the enhancement of device or circuit reliability. Progressive breakdown starts by the digital fluctuation of I_g . After a certain period, I_g will rapidly degrade until a point at which I_g becomes gradually saturated. After which the occurrence of a thermal runaway can be identified by a sudden, very abrupt jump in I_g after the saturation of I_g for a certain period. At this point, the device experiences catastrophic or hard breakdown. According to J. S. Suehle *et al.* [45], the early stage of progressive breakdown is classified as digital breakdown, while the later stage of progressive breakdown is classified as analog breakdown. A device will not fail at the onset of progressive breakdown. However, the failure of a device will occur when I_g progressively evolves to a leakage level that causes device performance disruption. Therefore, the

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understanding of the physical mechanisms responsible in governing the evolution of I_g during progressive breakdown is critical for projecting the long-term reliability of devices.

2.3.4 Physical Analysis of Failures in Ultrathin Gate Oxide: The Dielectric-breakdown-induced Epitaxy (DBIE)

Dielectric-breakdown-induced epitaxy (DBIE) [14, 16-21] is one type of severe, irreversible microstructural damage that can be observed in a device suffering from soft or hard breakdown. Fig. 2.4 shows typical examples for DBIE in n- and a p-MOSFETs suffering from gate dielectric breakdown, in which these are observed using transmission electron microscopy (TEM) [18]. The formation of DBIE is dependent on stressing polarity, in which DBIE will be formed at the cathode and then grow from the cathode to the anode [18]. As shown in Fig. 2.4, in the inversion-mode stressing, DBIE in a p-MOSFET stressed using negative V_g is formed at the poly-silicon gate, while DBIE in a n-MOSFET stressed using positive V_g is formed at the silicon substrate. It has been found that for a given stressing condition, the size of DBIE in a n-MOSFET is nearly twice larger than that in a p-MOSFET [19]. The results suggest that the direction of electron wind force during electrical stressing serves as one of the crucial factors in forming DBIE. The studies of DBIE are particularly important as it is believed that the formation and the evolution of DBIE play a critical role in affecting the conduction mechanisms during progressive breakdown.

A model has been proposed to describe the formation and the evolution of DBIE during progressive breakdown [14]. At a constant V_g , energetic electrons that tunnel through the gate oxide from cathode to anode will result in defect generation.

Figure 2.4. Typical example for DBIE in a n- and a p-MOSFET suffering from gate dielectric breakdown, in which these are observed using the TEM technique [18]. In the inversion-mode stressing, DBIE in a p-MOSFET stressed using negative V_g is formed at the poly-silicon gate, but DBIE in a n-MOSFET stressed using positive V_g is formed at the silicon substrate.

A percolation path will be formed within the gate oxide after the defect density reaches a critical threshold, electrically linking the poly-silicon gate to the silicon substrate. A large amount of I_g will locally surge through the narrow percolation path. Since Joule heating is proportional to the square of the current density; thus, the localized temperatures in the vicinity of the percolation path will be substantially high due to the high resistivity of the percolation path [14, 18-19]. The percolation path is believed to be a dynamically grown conductive channel, in which it could laterally dilate with increasing stressing time [20]. As the localized temperatures at the vicinity of the percolation path rise, more defects around the percolation path will be thermally activated and created. Eventually, the enhanced localized Joule heating effect will cause the percolation path to laterally dilate towards the Source and/or Drain [20]. This model assumes that I_g flowing through the percolation path increases with increasing localized temperatures. According to M. Houssa *et al.* [46], the temperature dependence of I_g flowing through a percolation cluster is

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believed due to the scattering of electrons by a random array of dangling bonds and defects that are present at the vicinity of the percolation path [46]. Obviously, as I_g increases, the localized temperatures will be further enhanced. This current-temperature positive feedback loop ensures the continuous increase in I_g and the localized temperature in the vicinity of the percolation path, as long as the stressing on the gate oxide is maintained.

When the localized temperatures in the vicinity of the percolation path become comparable to or higher than the silicon melting point, silicon-silicon bonds at the silicon substrate will be broken. The formation of DBIE begins with the migration of the dislodged silicon atoms from the silicon substrate to the gate oxide. The silicon flux that contributes to the formation of DBIE contains two main components [14, 18-19]: i.) the accelerated self-diffusion of the dislodged silicon atoms due to the presence of a very steep thermal gradient in the vicinity of the percolation path and ii.) the enhanced migration of the dislodged silicon atoms due to the presence of a very strong current wind force from the cathode to the anode through the percolation path. After DBIE is formed, thermal runaway may be alleviated through the consumption of the free energy in the system as well as the reconfiguration of the percolation path.

Besides the DBIE formation, several other forms of microstructural damage such as DBIM, severe substrate defects, implosion, poly recrystallization, gate and contact plug burn out take place due to joule heating in the vicinity of breakdown spot [47]. On the basis of microstructural changes, Tung *et al.* [48] defined different modes of the oxide breakdown and its effect on the device performance. Figure 2.5 shows the sequence of several microstructural damages with the gate leakage current which leads to the joule heating in the vicinity of the percolation path [16].

Figure 2.5. General representation summarizing the degree of microstructural damages induced by dielectric BD in an ultrathin-SiO_xN_y/poly-Si gate stack. The severity of the damage is directly related to the gate leakage current [16].

2.4 High- κ Gate Dielectrics

For sub-65 technology node, materials whose dielectric constant is above 20 and compatible with complimentary metal-oxide-semiconductor process have been investigated for new gate dielectric material over the past years. Many high- κ materials such as La₂O₃, ZrO₂, Ta₂O₃, HfO₂ etc. have been explored as the alternative gate dielectrics to overcome leakage current problem, which is a major concern for ultrathin oxynitride gate dielectrics. Among the high- κ alternatives, HfO₂ is a very promising candidate because it has good material properties ($\kappa = \sim 25$, energy band gap = 5.7 eV), has demonstrated better device characteristics and is compatible with the polysilicon gate process [49-56].

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2.4.1 Reliability Issues of High- κ Dielectrics

The reliability study of HfO_2 gate dielectric is getting more attention by the researchers. McPherson *et al.* [57-59] reported that the ultimate breakdown strength (E_{bd}) of a dielectric material decreases with increasing κ and has a relationship of E_{bd} proportional to $\kappa^{-1/2}$. It is suggested that a very high local electric field (Lorentz-relation/Mossotti-field) in the high- κ dielectrics tends to distort/weaken the polar molecular bonds making them more susceptible to bond breakage by standard Boltzmann processes and/or by hole-capture, resulting in lower E_{bd} [57-59]. The statistics of gate dielectric breakdown are usually described using the Weibull distribution, which is given by

$$F(x) = 1 - \exp\left[-\left(\frac{x}{\alpha}\right)^\beta\right] \quad (\text{Eqn. 2.1})$$

where β is known as the slope parameter. Weibull distribution is an extreme-value distribution in $\ln(x)$ and is appropriate for problems involving the weakest link. From elementary statistics, if the probability for which any one unit fails is p , then the probability for which any one of N independent units fails is

$$F = 1 - (1 - p)^N \quad (\text{Eqn. 2.2})$$

Eqn. (2.2) can be reorganized as

$$W = \ln[-\ln(1 - F)] = \ln(N) + \ln(-\ln(1 - p)) \quad (\text{Eqn. 2.3})$$

W is known as the Weibit. Note that β is an important parameter in the evaluation of gate dielectric reliability. It has been reported that β decreases with decreasing T_{ox} . One of the important advantages of the percolation model is to establish the direct correlation between β and the critical number of defects required in triggering the occurrence of a dielectric breakdown

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event. Kim *et al.* [60] reported that the Weibull slopes β of the BD distribution in ultrathin HfO_2 (which is related to the reliability of the gate dielectric; larger the β value, the better reliability) for SBD and HBD are different, and β for HBD is greater than that of SBD. It has also been reported that β of thick HfO_2 is smaller than that of SiO_2 of similar physical thickness. Whereas, β of thinner HfO_2 is similar to that of SiO_2 . Furthermore, the BD in high- κ is intrinsic and can be explained by the percolation model [61]. It has been suggested that the HfO_2 layer may have smaller critical defect density (N_{BD}) for BD or larger spacing between the defects where tunneling of trapped electron becomes probable in comparison with SiO_2 [61]. This would result in a smaller β with HfO_2 .

Figure 2.6. (a) Gate leakage current evolution with stress time for SiO_2 IL/ HfAlO_x gate stacks. The up and down arrows indicate HBD and SBD, respectively. (b) Schematics show that the successive multiple soft breakdowns in high- κ gate stacks is due to the breakdowns in the high- κ layer, and the hard breakdown takes place only after the interfacial layer breakdown [67].

Degraeve *et al.* [62] reported that the breakdown in HfO_2 high- κ / SiO_2 gate stack is stress-polarity dependent due to asymmetric band-diagram. For substrate injection, steep increase in the bulk

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trap density of HfO_2 is likely to trigger the BD of the HfO_2 -layer, while during gate injection SiO_2 interfacial layer (IL) controls the BD. Similar stress polarity dependent BD has also been reported for other high- κ gate stacks [63, 64]. Garros *et al.* [65] observed a smaller time-to-breakdown during substrate injection compared to gate injection. Furthermore, for the same equivalent oxide thickness, the HfO_2 gate dielectric shows higher reliability than SiO_2 .

Recent research shows that the sub-oxide SiO_x ($x < 2$) interfacial layer in the high- κ gate stacks plays a very important role in the degradation of the HfO_2 gate dielectric devices. Young *et al.* [66] reported that voltage stress-induced generation of the defects contributing to threshold voltage instability in high- κ gate stacks occurs primarily within the interfacial SiO_2 layer. It is also reported that the gradual increase in the gate leakage is due to occurrence of successive multiple soft breakdowns of the high- κ layer, and hard breakdown occurs only after the interfacial layer breakdown (see Fig. 2.6) [67]. On the other hand, Wang *et al.* [68] categorized the soft breakdown in Hf-based gate dielectric into two modes-digital soft breakdown and analog soft breakdown. It was reported that the low energy dissipation in the oxide layer, trapping and emission of electrons at the traps located near the breakdown path in the high- κ gate dielectric contribute to the digital soft breakdown. Whereas, the existence of various breakdown paths in the high- κ dielectric film with high density of localized traps owing to the large Joule heating under stress is responsible for the analog soft breakdown.

Recently, on the basis of conductive atomic force microscopy (C-AFM) analysis of HfO_2 gate dielectric, Blasco *et al.* [69] reported that breakdown is a reversible phenomenon, i.e., the BD path can be switched on and off. It is also suggested that the $\text{HfO}_2/\text{SiO}_2$ stacks BD is controlled by the SiO_2 interfacial layer, and the HfO_2 layer has a protective effect during the BD transient, which allows the observation of the reversibility of the BD phenomenon. Furthermore,

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the C-AFM study also revealed different conduction regimes at different voltage ranges in virgin $\text{HfO}_2/\text{SiO}_2$ gate stacks: in the lower-field regime carrier injection through triangular HfO_2 barrier (and through trapezoidal SiO_2 barrier), whereas in the intermediate field regime the carrier injection is at energies above the HfO_2 barrier, and at large enough fields, breakdown of the gate stacks were observed [70]. It is also found that the size of breakdown spots in the $\text{HfO}_2/\text{SiO}_2$ stacks are of the same order as the BD spots in SiO_2 -based dielectrics.

Figure 2.7. Gate leakage current evolution with stress time. It showed the range of behavior in 9 high- κ /metal gate stack MOSFETs [35].

Palumbo *et al.* [71] reported that high degradation rate is very common in SiO_2 breakdown with tungsten gate electrode MOS capacitors. It was reported that the large abrupt gate leakage current increase associated with BD in high- κ /metal gate stack MOSFETs (see Fig. 2.7) compared to poly-Si gate electrode is an intrinsic property of the metal gate electrode. The results raise a potential limitation for the reliability of metal gate-based devices [72]. Degraeve *et al.* [73] reported the existence of two phases of breakdown in high- κ /metal gate stack transistors;

the transistor first suffers progressive/digital soft breakdown before an abrupt increase in the gate leakage current resulting in catastrophic failure of the transistor. But the exact mechanism responsible for BD in metal gate stacks remains unclear.

2.4.2 New Failure Mechanisms of High- κ Gate Dielectrics

Most of the analysis of the BD phenomenon of HfO_2 in literature is based on pure electrical analysis. Very few reports in the literature describe the physical analysis of the BD phenomenon in HfO_2 gate dielectric.

Figure 2.8. (a) TEM micrograph of $\text{SiO}_x/\text{HfO}_2$ high- κ /poly-Si gate stack nMOSFET showing a “ball-shaped” capping layer above the breakdown spot at the anode electrode of the device, (b) EELS spectra of oxygen K edge at various locations of a nMOSFET shown in (a). Oxygen K edge at SiO_2 spacer, HfO_2 gate dielectric (position 1), and “ball-shaped” capping layer (position 2) as seen. The solid arrows indicate the oxygen K edge peaks [74].

Rakesh *et al.* [74] reported the chemical analysis performed at the breakdown spot for poly-Si/ HfO_2 gate stack using TEM/EELS. A dielectric breakdown induced “ball-shaped” capping layer on the anode side (i.e., the poly-Si) of the MOSFET can be seen in the vicinity of the

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breakdown spot, as shown in Fig. 2.8 (a). The oxygen in the capping layer has a different chemical bonding from that in the HfO_2 gate dielectrics as shown from an EELS elemental dot mapping analysis, see Fig 2.8 (b). The capping layer consists of Hf-based compounds, whose chemical properties lie between the HfO_2 and HfSiO_4 . HfO_2 high- κ /TaN/TiN gate stack n/pMOSFETs have been studied as shown in Fig. 2.9 [75]. Ultrafast progressive breakdown is polarity dependent and is found only in the case of substrate injection in metal gate n/pMOSFETs. The ultrafast progressive breakdown observed is due to a metal-like filament formation at the breakdown spot during the substrate injection of the TaN/TiN n/pMOSFETs. The progressive BD transient of the metal gate pMOSFET is much slower than nMOSFET in inversion mode stress, which is a normal operating condition for CMOS transistors. Due to the ultrafast progressive BD in the metal gate nMOSFET, pMOSFET in inversion mode will have a longer progressive transient than that of nMOSFET.

Figure 2.9. (a) TEM micrograph of a BD of another TaN/TiN gate nMOSFET stressed under inversion mode CVS with $V_{gstress}$ of 3.7 V and $I_{gl} = 7$ mA. (b) TEM micrographs of a HfO_2 high- κ /TaN/TiN gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under accumulation mode (i.e., gate injection) CVS with $V_{gstress}$ of -4.5 V and $I_{gl} = 20 \mu\text{A}$ having the source and drain floated. The insert shows the BD location in the channel. [75]

2.5 Electronic Structure Measurement Using Electron Energy Loss Spectroscopy (EELS)

Modern microelectronics industry has entered into the word of ‘nano’ as a result of the constant miniaturization of device size, which is driven by the well known ‘Moore’s Law’. The smallest feature in a MOSFET device can be in nanometer or sub-nanometer scale, e.g., the interfacial oxide layer beneath the high- κ gate dielectric layer. Functional structures like this are too small to be resolved and characterized with conventional techniques like light microscopes or even SEMs. Therefore, electron microscopes with higher spatial resolution are the instruments of choice to study the physical structures of the nano-size device. Moreover, the local chemical information of the material can be accessed with a scanning transmission electron microscope equipped with detectors like electron energy loss spectrometer and energy dispersive X-ray spectrometer. This is done by placing the nanometer sized electron beam on the specimen and measuring the signal of the electrons after passing through the specimen as well as the X-ray signals generated. The local electronic structure as well as the chemical composition of the specimen can be extracted with the EELS/EDS spectra.

Figure 2.10. Left, dark field image of the Si-SiO₂ interface. Right, EELS spectra obtained at eight locations indicated by the circles at the left. The bulk Si (Si⁰) onset is near 100 eV. The SiO₂ (Si⁴⁺) structures lies between 105 and 108 eV. At the interface, a fairly strong Si²⁺ signal is seen for the first time in the bulk. Some structure corresponding to electronic defect states in the silicon gap also appears to be present. [76]

Figure 2.10 shows one of the pioneer work to realize the electronic structure characterization in nanometer scale (i.e., atomic resolution) using STEM/EELS. P. E. Batson in his paper [76] studied the Si-SiO₂ interface with Si-L_{2,3} edge EELS (i.e., transitions from Si 2p band to conduction band unoccupied density of states) and resolved the different bonding states of Si. As shown in the figure, the Si⁰ peak located at 99.84 eV shifts to 106-108 eV (i.e., Si⁴⁺) as crossing the interface. Si²⁺ bonding was identified to be present at the Si-SiO₂ interface.

Figure 2.11. The measured EELS O K edges of bulk a-SiO₂ and for O atoms at an atomically smooth interface between [100] Si and native a-SiO₂. The 3-eV reduction in the edge onset at the interface aligns the unoccupied O interfacial states with the Si conduction band edge, as would be expected for induced gap states. This pre-peak (a) can be thought of as tunneling states leaking in from the bulk Si. The figure to the right is the annular dark field (ADF) image of the interface between the a-SiO₂ and the silicon substrate [77].

D. A. Muller [77] extended the work to sandwiched Si-SiO₂-Si structure. To improve the contrast and sensitivity, he used the O-K edge which is more localized [78]. The O-K edge EELS provides information on the unoccupied O-p electronic densities of states. The O K edge at the Si-SiO₂ interface is different from that for bulk SiO₂ (as shown in Fig. 2.11) in two ways. First, the edge onset (a in Fig. 2.11) is reduced by 3 eV at the interface with respect to the bulk. As the O K edge reflects the portion of the conduction band projected onto the probed O atom, the reduced edge onset implies a reduced bandgap. Second, the sharp peak (b in Fig. 2.11), which is the first extended-fine-structure peak in the bulk near edge spectrum, is absent at the interface. The almost complete absence of this peak implies that more O second-nearest neighbours are missing.

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A similar interfacial spectrum is observed at the interface between Si and the thermally grown oxides. Figure 2.12 shows EELS spectra recorded point by point across a gate stack whose oxide thickness was nominally measured at 1 nm by ellipsometry. The change in the conduction band DOS is clearly shown at the Si-SiO₂ interface and bulk SiO₂.

Figure 2.12. EELS spectra recorded point by point across a gate stack containing a thin gate oxide. The annular dark field (ADF) image (left panel) shows where each spectrum was taken. The right panel shows the background-corrected O K edges. For a 10-nm-thick sample, the ADF resolution is 0.23 nm and the EELS spatial resolution at the O K edge is reduced to 0.26 nm due to delocalization [77].

2.6 Summary

Gate dielectric breakdown is one of the most important reliability concerns in the MOSFET miniaturization. Many studies have demonstrated that gate dielectric breakdown becomes more serious as T_{ox} is continuously scaled down in order to achieve excellent device performance. Several intrinsic breakdown models, such as the thermo-chemical, the anode hole injection, the

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hydrogen release and the percolation model, have been developed and proposed to understand the underlying mechanisms that govern the occurrence of a dielectric breakdown event. In addition, progressive breakdown, which is a unique phenomenon that can only be observed in ultrathin gate dielectric breakdown, has been intensively studied as it provides extra post-breakdown reliability margin. DBIE is reported as one type of important, irreversible microstructural damages, which could play a critical role in affecting the conduction mechanisms during progressive breakdown. The advantages, concerns and breakdown mechanisms in new generation high- κ gate dielectrics are reviewed. It is realized that most of the breakdown models describing the dielectric degradation are based on electrical analysis results, and are not adequate to explain all the experimental data. In HfO_2 high- κ /poly-Si gate stacks and metal gate stacks, the dielectric degradation is more complicated due to several new intrinsic properties of high- κ and metal gate and its dependency on the processing conditions. Hence, the electrical analysis results are not sufficient to explain the breakdown mechanism in HfO_2 high- κ /poly-Si gate stacks and metal gate stacks. In order to better understand the dielectric degradation and its impact on the device and the circuit performance, nanoscale physical analysis of the breakdown mechanism is needed.

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EXPERIMENTAL PROCEDURE AND DETAILS

3.1 Introduction

In this chapter, the details of various electrical and physical characterization methodologies that were used to study the dielectric degradation and reliability are thoroughly discussed. Constant voltage stress (CVS) consisting of successive, 2-stage and multiple stage modes are used to study the evolution of percolation paths formed in the gate dielectrics. Pre- and post-breakdown device performances are characterized using four terminal probe station and semiconductor parameter analyzer. Transmission electron microscopy and electron energy loss spectroscopy are then used as the key platform to examine the structural as well as chemical change of the broken down dielectrics. Electronic and chemical information are extracted and compared with theoretical calculations. The physical analysis results are subsequently linked back to the electrical characteristics of the device. With the knowledge acquired from the physical analysis, a comprehensive understanding of the dielectric degradation process is developed. It is therefore feasible to accurately predict the lifetime of a BD transistor and integrated circuit (IC) chip. The design and fabrication technologies can be improved too. The overall flow of the methodology is illustrated in the schematic diagram in Fig. 3.1.

Figure 3.1. Flowcharts describing the methodologies used for dielectric reliability study.

3.2 Sample Information

In this study, *small* gate area (i.e., gate width $W \times$ gate length $L \leq 1 \mu\text{m}^2$) SiO_xN_y/poly-Si gate stack nMOSFETs, fully silicided NiSi gate with HfSiO_x/SiO_x gate dielectric, and SiO_x interfacial layer/HfZrO₄ high-κ/TaN/TiN gate stack nMOSFETs were studied. The details of the devices

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are listed in Table 3.1. Figure 3.2 shows the respective TEM micrographs of the poly-Si and high- κ /metal-gate MOSFETs listed in Table 3.1.

Figure 3.2. (a) Poly-Si/SiON(2.2nm)/Si, (b) NiSi/HfSiO_x(2.6nm)/SiO_x(1.2nm)/Si, and (c) TiN/TaN/HfZrO₄(2.5nm)/SiO_x(1.3nm)/Si gate stack used in this study.

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Table 3.1 Details of the devices used in study.

Devices	Device dimensions (gate width W (nm) and gate length L (nm))	Equivalent oxide thickness (EOT) (nm)	Physical thickness revealed by TEM
Polycrystalline silicon gated silicon oxynitride (SiO _x N _y) nMOSFETs	$W = 150$ $L = 150 - 500$	EOT = 2.2	2.1 nm
TiN/TaN metal gated HfZrO ₄ /SiO _x gate dielectric nMOSFETs	$W = 130 - 150$ $L = 130 - 250$	EOT = 1.8	2.5 nm of HfZrO ₄ and 1.2 nm of SiO _x interfacial layer
Fully silicided NiSi metal gated HfSiO _x /SiO _x gate dielectric nMOSFETs	$W = 150$ $L = 130 - 500$	EOT = 1.8	2.6 nm of HfSiON and 1.2 nm of SiO _x interfacial layer

3.3. Electrical Characterization

The equipment used for the electrical characterization includes a 8-inch Cascade Microtech wafer probe station and a Agilent Technologies E4156/5280 precision semiconductor parameter analyzer, which are shown in Figs. 3.3(a) & 3.3(b) respectively. The 8-inch Cascade Microtech wafer probe station including a thermo-chuck serves as a platform for the stressing on the gate oxide and various electrical measurements of a MOSFET. The stressing on the gate oxide and various electrical measurements of a MOSFET are performed using the Agilent Technologies E4156/5280 precision semiconductor parameter analyzer, which consists of four highly accurate source-monitor units (SMUs) with a current resolution of 1 fA and a voltage resolution of 2 μ V, as shown in Fig. 3.3(b). These SMUs are separately connected to four Cascade Microtech probe heads placed on the 8-inch Cascade Microtech wafer probe station via Kelvin tri-axial cables with low leakage current. These probe heads are primarily used to steadily hold tungsten needles,

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which are separately connected to the drain terminal, the source terminal, the gate electrode and the substrate of a MOSFET.

Figure 3.3. (a) 8-inch Cascade Microtech wafer probe station. (b) Agilent Technologies E4156/5280 precision semiconductor parameter analyzer.

3.3.1 Stress Methodologies to Induce a Breakdown

Before stressing the gate oxide of a n-MOSFET, the breakdown voltage (V_{BD}) of the nMOSFET sample must be determined. V_g represents a voltage that is applied to the gate electrode of an nMOSFET, while V_d , V_s and V_{sub} denote the drain, the source and the substrate voltage respectively. The I_g - V_g measurement of a device is carried out by sweeping V_g from 0 V to a higher value with a constant voltage increment of 0.05 or 0.1 V, while the Drain, Source and substrate terminals are grounded (i.e., $V_d = V_s = V_{sub} = 0$). I_g will exponentially increase with increasing V_g due to the direct tunneling of charge carriers through the gate oxide. When I_g experiences a sudden, abrupt increase, the device is said to encounter a dielectric breakdown, and the corresponding V_g will be treated as V_{BD} . Fig. 3.4 shows a typical example for the I_g - V_g ramping test in determining V_{BD} of an nMOSFET with $T_{ox} = 16 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$. This procedure will be repeated for about 10-20 devices that possess the same dimensions and

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are well distributed over a wafer. Eventually, the average breakdown voltage (V_{BDA}) of a n-MOSFET can be obtained.

Figure 3.4. (a) Typical example for the I_g - V_g ramping test in determining V_{BD} for a n-MOSFET with $T_{ox} = 16 \text{ \AA}$ and $L \times W = 0.5 \times 0.6 \text{ \mu m}^2$. (b) β versus V_g relationship reported in Ref. [1].

By knowing V_{BDA} , a constant stressing voltage ($V_{gstress}$) that will be used to stress the gate oxide of a device can be determined. $V_{gstress}$ must be lower than V_{BDA} such that a dielectric breakdown event will not immediately occur upon stressing the gate oxide starts. $V_{gstress}$ can be calculated using the following equation [1]:

$$\ln(t_{BD}) = \ln(t_{BD}') + \beta(V_{BDA} - V_{gstress}) \quad (3.1)$$

where t_{BD} and t_{BD}' are the time-to-breakdown for the gate oxide of a device at $V_{gstress}$ and V_{BDA} respectively. Note that t_{BD} is specified in the range of 100-2000 s. β is referred to as the voltage acceleration factor [2], as shown in Fig. 3.4(b).

A standard constant-voltage stress is a widely used stressing methodology in the study of gate dielectric breakdown [2-4]. For thin or ultrathin gate oxide, the direct tunneling of charge carriers through the gate oxide is ballistic or quasi-ballistic in nature, and the generation of

defects within the gate oxide depends on the energy of charge carriers at the anode. This is primarily controlled by V_g . Therefore, in order to more precisely study the gate dielectric breakdown, a standard constant-current stress, which is normally used for thick gate oxide, has been replaced by a standard CVS.

Figure 3.5. Evolution of I_g for a nMOSFET ($T_{ox} = 22$ Å and $L \times W = 0.5 \times 0.15$ μm^2) that was stressed using a standard CVS in inversion mode with $V_{gstress} = 4.2$ V at the room temperature. The process from the SILC to the occurrence of a dielectric breakdown event is referred as TDDB.

In a standard CVS, a constant voltage is applied to the gate electrode of a device (i.e., $V_g = V_{gstress}$) until specific dielectric breakdown criteria are met, while the Drain, Source and substrate terminals are grounded (i.e., $V_d = V_s = V_{sub} = 0$). Fig. 3.5 shows a typical evolution of I_g for a n-MOSFET ($T_{ox} = 22$ Å and $W \times L = 0.15 \times 0.5$ μm^2) that was stressed using a standard CVS in inversion mode with $V_{gstress} = 4.1$ V at the room temperature. The stressing on the gate oxide of the n-MOSFET is terminated when a sudden, abrupt increase of I_g with a magnitude of more than two times larger than the fresh or non-breakdown I_g is detected. Besides the standard CVS,

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stressing methodologies frequently used in our studies include successive CVS, two-stage CVS and K-cycle multiple-stage CVS.

A successive CVS, which is a current-limited stressing methodology, is developed on the basis of a standard CVS. A suitable $V_{gstress}$ was applied to the transistors until a breakdown occurred at a relatively low gate leakage compliance current limit (I_{gl}) of typically less than 10 μ A. Subsequently, the stress was continued by successively (or stepwise) relaxing I_{gl} to higher values while keeping the stress voltage unchanged. This method is useful to study the evolution of different stages of breakdown, the associated microstructural damages, and the effect of the post-BD evolution of the gate leakage current on the device performance.

However, in order to acquire more insightful data that can improve the understanding on the physical mechanisms responsible for progressive breakdown, the characteristics of a device at the different stages of progressive breakdown must be studied in detail. This can only be achieved if progressive breakdown evolves with a relatively slower rate. For that reason, the major objective of using a two-stage CVS, which is developed by modifying a successive and standard CVS, is to prolong progressive breakdown [5, 6]. Obviously, a two-stage CVS is constituted by two main phases of implementation: The 1st-stage CVS is responsible for accelerating the process of generating electronic traps within the gate oxide until the occurrence of a dielectric breakdown event is observed. Then, a lower $V_{gstress}$ is applied to further stress the gate oxide of the device. During the 2nd-stage CVS, either the stressing time or I_{gl} serves a controlling parameter in selectively halting progressive breakdown such that the characteristics of the device at the different stages of progressive breakdown can be studied in details.

A two-stage CVS has been further developed into a K-cycle multiple-stage CVS [7]. Using a K-cycle multiple-stage CVS, we discover that the physical mechanism responsible in

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governing progressive breakdown at high V_g could be different from that at low V_g , affecting the lifetime prediction of gate oxide. Our findings reveal that at low V_g , digital breakdown is dominant at the early stage of progressive breakdown, in which this could hardly be observed using a two-stage, successive or standard CVS. In general, a K-cycle multiple-stage CVS is a process of repetitively stressing the gate oxide of a device with one particular group of V_g , which could be as low as the nominal operating voltage of the device. Similar to a two-stage CVS, a K-cycle multiple-stage CVS starts by stressing the gate oxide of a device under accelerated stressing conditions, ensuring that the TDDB of the device can be completed within a reasonable window of time. A low I_{gl} of 1-10 μA is applied to limit I_g at a low level during the occurrence of a dielectric breakdown event such that the early stage of progressive breakdown can be successfully arrested. After the TDDB of the device is completed with the detection of a sudden, abrupt increase in I_g , the 1st-cycle multiple-stage CVS is carried out. V_{init} and V_{final} define an initial and a final $V_{gstress}$ that are used in the 1st-cycle multiple-stage CVS. The device is stressed with $V_{gstress} = V_{init}$ for a specific constant duration, which is represented as t_{stress} . The stressing on the gate oxide of the device is repeated by increasing $V_{gstress}$ with a constant voltage increment, which is denoted as ΔV , until V_{final} is reached. Moreover, V_{final} could be set at a voltage lower than a certain threshold value to prevent the further evolution of progressive breakdown, depending on the purpose of the experiments. Since the gate oxide of the device is stressed from V_{init} to V_{final} with a step-like increment of ΔV , this stressing methodology is referred to as a multiple-stage CVS. The details of this stressing methodology can be found in Ref. 7.

3.3.1 Pre- and Post-BD Characterization

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The hardness and device performance of progressive breakdown can be monitored through various post-breakdown electrical measurements. Figure 3.6 displays an example of an nMOSFET ($T_{ox} = 22 \text{ \AA}$ and $W \times L = 0.15 \times 0.20 \text{ \mu m}^2$) that was stressed using a 2-stage CVS. The BD location, I_d - V_d , and I_g - V_g measurements are applied to investigate the device characteristics in the progressive breakdown.

- For the I_d - V_d measurement, I_d is measured at a given constant V_g by sweeping V_d , while the source terminal and the substrate are grounded (i.e., $V_s = V_{sub} = 0$).
- For the I_g - V_g measurement, I_g is measured by sweeping V_g , while the drain terminal, the source terminal and the substrate are grounded (i.e., $V_d = V_s = V_{sub} = 0$).

The breakdown location, which is denoted as S , defines the location of a percolation path along a device channel [116-118]. S serves as an important parameter in the study of gate dielectric breakdown. B. Kaczer *et al.* proposed that S can be calculated as [8-10]

$$S = \left(\frac{\Delta I_d}{\Delta I_d + \Delta I_s} \right) \times L \quad (3.2)$$

where ΔI_d and ΔI_s are the increase in I_d and I_s after the occurrence of a dielectric breakdown event. Eqn. (3.2), which is derived in according to a current-separation methodology, demonstrates the location of a percolation path as a fraction of the device channel. $S = 0L$ represents the source terminal, while $S = 1L$ represents the drain terminal. The post-breakdown electrical measurements in evaluating Eqn. (3.2) should be carried out in accumulation mode. In inversion mode, the accuracy of Eqn. (3.2) will be affected by two factors: (a) the presence of a voltage offset between the drain and the source terminal, as well as (b) the series resistances on the source and the drain terminal [10].

Figure 3.6. (a) Time evolution of the gate leakage current I_g in a 2-step CVS. The TDDB failure at $I_{gl} = 1 \mu A$ was induced by a high voltage stress, $V_{gstress} = 4.2$ V and a lower $V_{gstress} = 3.2$ V was used in the subsequent stress to achieve the respective current limited BDs. The final failure current was $I_{gl} = 200 \mu A$. In the 2nd step stress, post-BD I - V measurements were performed at different I_{gl} BDs. (b) BD location measurement shows that the BD spot was located at center of the channel. (c) I_g - V_g characteristics after the occurrence of a dielectric breakdown event at $I_{gl} = 1$, 70 and 200 μA , respectively. (d) I_d - V_d characteristics at $V_g = 0.3$, 0.6, 0.9, 1.2 and 1.5 V after the occurrence of a dielectric breakdown event at $I_{gl} = 1$ and 200 μA .

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It can be observed that a device suffering from dielectric breakdown is associated with degraded I_d and I_g . This is mainly due to the presence of an excessively large I_g in the device. Similar phenomenon can be noticed in the I_s - V_s characteristics of a device, where I_s denotes the source current. Obviously, when progressive breakdown evolves, the curve of I_g - V_g will continuously degrade.

3.4 TEM Sample Preparation

It is necessary to know the microscopic nature of the defects/microstructural change which causes the breakdown or develop during a breakdown event for a better understanding of the failure mechanisms in different gate stack MOSFETs. TEM analysis of the breakdown spots was performed after stressing the devices to study the microscopic nature of microstructural changes physically. EDS/EELS [11, 12] technique was used to study the elemental composition, the chemical composition and the atomic bonding states of the compounds at the breakdown spot. In order to facilitate the TEM analysis, the failure transistor must be isolated and thinned down to electron transparency. Dedicated sample preparations are needed to achieve a successful TEM analysis. In this section, several sample preparation techniques used in this study are discussed.

3.4.1 Mechanical Polishing with Ion Milling

The specimen is firstly mounted onto a tripod tool and polished mechanically using SiC and diamond lapping films. In this stage, it is thinned down to thickness less than 1 micron. The specimen is then ion milled to electron transparency. Low energy (~ 2 kV) Ar^+ ion milling is used in the latter step with 4-6° tilting to minimize sample damage/artifact induced by the Ar^+

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ions. The advantage of this method is that there are large thin area (thickness can be down to 10 nm) for TEM analysis. The damaged/amorphized region induced by ion milling on both sides of the specimen can be controlled within 2 nm thick. However, this method can not be performed on a specific location so that it is usually used for blanket thin film. Figure 3.7 shows two TEM micrographs prepared by mechanical polishing.

Figure 3.7. (a) Cross-sectional view HRTEM micrograph of HfO₂/SiO_x gate dielectrics and (b) planar view TEM of the same high-k dielectrics prepared by mechanical polishing.

3.4.2 Site-specific Focused Ion Beam (FIB) Milling

Precision TEM sample preparation was used to prepare TEM lamella of thickness less than 100 nm to study the microstructural defects responsible for dielectric failure. Only focused ion beam (FIB) technique was able to meet this requirement as very small devices located at specific locations must be used in our study. The working mechanism of FIB is based on the sputtering of sample material by highly energized Ga⁺ ions (~ 30 kV acceleration voltages) in the presence of electric and magnetic field. The Ga⁺ ions can be well focused and controlled by the FIB

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equipment electric and magnetic field. Hence, the minimum beam size can be scaled down to less than 15 nm diameter for ion-milling. Figure 3.8 shows the FIB equipment used in our study.

Figure 3.8. (a) FEI Nova and (b) FEI Helios FIB were used to prepare the site-specific samples for our TEM analysis. Both FIB systems are dual-beam system. The e-beam enables an unambiguous sample preparation by monitoring the cross section of the sample during ion-milling.

In order to increase the success rate of catching the BD dielectrics, very *narrow* transistors consisting of widths of 250 nm or less were used. Using this method, the probability of capturing the defects associated with a dielectric BD in a MOSFET in the final TEM lamella of about 100 nm of thickness is more than 90 percent (see Fig. 3.9).

Figure 3.9. Schematic showing the top view of a MOSFET. It can be seen that for a *narrow* width device, the probability of capturing the BD defects in the final TEM lamella of about 100 nm of thickness after thinning is higher than 90%.

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Figure 3.10. (a) Optical image showing the pre-thinned slice attached to a copper ring polished to $\sim 15 \mu\text{m}$ thick; (b) optical image showing transistor area after pre-thinning; scanning electron microscope (SEM) micrographs showing (c) further FIB thinning of transistor area; (d) deposition of platinum (Pt) protective layer on the area of interest; (e) FIB thinning of the specimen from both sides when the device emerges and (f) the transistor sample after final thinning with the marking on source side by ion beam. The SEM micrographs were acquired at a tilt angle of 52° of the FIB sample stage.

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In the precision TEM sample preparation, 1) “pre-thinning”, 2) “lift-off” and 3) “in-situ lift-off” methods can be used. In the pre-thinning method as illustrated in Fig. 3.10, the area containing the transistor of interest is pre-thinned by mechanical polishing to $< 20\ \mu\text{m}$. After that, the specimen was mounted onto a copper ring to enhance the sample mechanical hardness. Then the specimen was fixed on a specific FIB sample holder and loaded into the FIB chamber. FIB was used to further thin the specimen to the location of interest from both sides of the membrane to have a TEM lamella of thickness of about 100 nm. Using this method, we can avoid any unwanted signals during the chemical analysis since the TEM lamella is free standing.

On the other hand, the “lift-off” sample preparation method uses FIB thinning of the specimen from both sides of the target location to a thickness of about 100 nm without any pre-mechanical polish, as shown in Fig. 3.11. The TEM lamella was detached partially from one corner in the end of the FIB thinning process. After that, the partially detached TEM lamella was unloaded from the FIB and loaded onto a semiconductor characterization probe station where the lift-off was carried out. As shown in Fig. 3.12, the TEM lamella was fully detached from the wafer by a tungsten needle using static charge and it was later transferred onto a carbon film, which is mounted on a copper ring. This method introduces one ‘foreign’ element, carbon, during chemical analysis and therefore it is not recommended for decent EELS measurements especially low loss and core loss near the C-K edge at around 280 eV.

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Figure 3.11. SEM micrographs show FIB thinning of a specimen and detachment of the required TEM lamella from the rest of the specimen using a “lift-off” method: (a) SEM micrograph showing two transistors; (b) deposition of Pt protective layer on the area of interest; (c) FIB thinning of the specimen from both sides; (d) a U-cut of the thinned specimen at 7° stage tilting; (e) further thinning of the TEM lamella and (f) detached TEM lamella from one corner for lift-off.

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Figure 3.12. Optical images showing the process of lifting-off the TEM lamella to a copper ring using tungsten probe: (a) Probe approaching the TEM lamella; (b) TEM lamella “attached” onto the probe by electrostatic charges; (c) TEM lamella lifted-off by the probe, (d) TEM lamella approaching a carbon film, (e) TEM lamella released onto the carbon film and (f) low magnification TEM micrograph showing the TEM lamella on a Cu-grid.

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Figure 3.13. SEM micrographs showing FIB thinning of a specimen and *in-situ* lift-off of the required TEM lamella: (a) SEM micrograph showing the pre-thinned sample welded onto the W-tip; (b) the sample was transferred onto a special Cu-grid; (c) sample approaching the Cu-grid before Pt-welding; (d) after Pt-welding and the W-probe was released by ion milling; (e) further thinning of the TEM lamella when device emerged and (f) TEM lamella after final milling with low-kV clean.

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The third method is the “*in-situ* lift-off” process applicable only for recent FIB systems, e.g., FEI Helios. This newly designed FIB is equipped with a computer controlled probe named Omni-probe. The probe tip can be inserted into the FIB chamber (i.e., *in-situ*) during the milling process. As illustrated in Fig. 3.13, the TEM specimen is thinned down to $\sim 1\ \mu\text{m}$ from both sides and welded onto the probe tip. It is then transferred to a special copper grid by Pt-welding and thinned down to less than 100 nm thickness. This method introduces no additional signals like the ‘pre-thinning’ method and less time consuming. It is used for the EELS/EDS chemical analysis in this study.

The FIB based technique allows the sample preparation to be site-specific, which fulfills the requirements for BD defect studies. However, the main drawback is the beam-induced damage problem. The damage/amorphization region on each side of the specimen is $\sim 20\text{-}30\ \text{nm}$ thick for Si using 30 kV Ga^+ ion milling. This limits the final thickness of the specimen to be at least 60 nm ($\sim 100\ \text{nm}$ for chemical analysis). Fortunately, the sample damage can be reduced by lowering the energy of Ga ion. For example, the thickness of the amorphization region on each side of the Si sample can be decreased to 5-7 nm using 5 kV acceleration and 2-3 nm using 2 kV Ga ion milling. The TEM samples used in this study for EELS experiment analysis are low-kV cleaned (i.e., 2 kV, 5° tilting). Figure 3.14 shows a high resolution STEM-HAADF micrograph of a poly-Si/SiO₂/Si nMOSFET at one gate corner prepared by *in-situ* lift-off and low-kV clean.

Figure 3.14. High resolution STEM-HAADF micrograph of a poly-Si/SiO₂/Si nMOSFET at the gate corner prepared by *in-situ* lift-off and low-kV clean.

3.5 Physical Characterization Using TEM/EDS/EELS

3.5.1 Transmission Electron Microscopy

Transmission Electron Microscopy allows the visualization of thin slices of material with nanometer resolution. A TEM operates much like a light microscope, but uses electrons instead of visible light, since the wavelength of electrons is much smaller than visible light (recall that the resolution limitation of any microscopy is based on the wavelength of the probe radiation). In a conventional transmission electron microscope, a thin specimen is irradiated with an electron beam of uniform current density. Electrons are emitted from the electron gun and illuminate the specimen through a two or three stage condenser lens system. Objective lens provides the

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formation of either image or diffraction pattern of the specimen. The electron intensity distribution behind the specimen is magnified with a three or four stage lens system and viewed on a fluorescent screen. The image can be recorded by direct exposure of a CCD camera. A TEM can be modified and operate in a scanning transmission electron microscope (STEM) mode by the addition of a system that rasters the beam across the sample to form the image, combined with suitable detectors. Scanning coils are used to deflect the beam, such as by an electrostatic shift of the beam, where the beam is then collected using a current detector. By correlating the electron count to the position of the scanning beam (known as the "probe"), the transmitted component of the beam may be measured. The non-transmitted components may be obtained either by beam tilting or by the use of annular dark field detectors. STEM is distinguished from conventional transmission electron microscopes (CTEM) by focusing the electron beam into a narrow spot which is scanned over the sample in a raster. The rastering of the beam across the sample makes these microscopes suitable for analysis techniques such as mapping by energy dispersive X-ray (EDX) spectroscopy, electron energy loss spectroscopy (EELS) and annular dark-field imaging (ADF). These signals can be obtained simultaneously, allowing direct correlation of image and quantitative data. By using a STEM and a high-angle detector, it is possible to form atomic resolution images where the contrast is directly related to the atomic number (z-contrast image). The directly interpretable z-contrast image makes STEM imaging with a high-angle detector appealing. Electron energy loss spectroscopy (EELS) as a STEM measurement technique made possible with the addition of an electron spectrometer. The high-energy convergent electron beam in STEM provides local information of the sample, even down to atomic dimensions. With the addition of EELS, elemental identification is possible and even additional capabilities of determining electronic structure or chemical bonding of atomic

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columns. The low-angle inelastically scattered electrons used in EELS compliments the high-angle scattered electrons in ADF images by allowing both signals to be acquired simultaneously. The microstructural and chemical analyses of the breakdown gate dielectrics are performed on an FEI Titan 80-300kV monochromatic TEM/STEM shown in Fig 3.15. An EDS detector and a Gatan Image Filter (GIF) are attached to the TEM to record the chemical information of the characteristic x-ray generated from the sample and electron energy loss of transmitted electrons.

Figure 3.15. An FEI Titan 80-300kV TEM/STEM used in this study. It is equipped with an EDS detector, a GIF detector and a monochromator. The energy resolution for EELS is 0.16 eV.

3.5.2 Electron Energy Loss Spectroscopy

Electron energy loss spectroscopy is commonly referred to as EELS. This technique takes advantage of inelastic collisions that incident electrons sometimes travel through the sample. As shown in Fig. 3.16, electrons that strike the sample and lose some energy in the process are the source of information in EELS. The lost energy is unique to each type of atom that the incoming electron interacts with. By measuring the energy of the scattered electron and subtracting that from the known energy of the incident beam, the energy lost can be calculated. This energy loss indicates what type of atom the electron interacted with and allows chemical identification of the sample.

Figure 3.16. Schematic drawing of the EEL spectroscopy showing its working principle.

The lost energy is unique to each type of atom that the incoming electron interacts with. By measuring the energy of the scattered electron and subtracting that from the known energy of the incident beam, the energy lost can be calculated. EELS and EDS spectroscopy are

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complementary techniques, while EELS is preferred for light element detection and has a higher spatial resolution. The pros and cons of EELS are summarized in Table 3.2.

Table 3.2 Advantages and disadvantages of electron energy loss spectroscopy.

Advantages	Disadvantages
<ul style="list-style-type: none"> • Analysis of elemental composition • Band structure and chemical bonding information • Chemical binding information • Atom-specific radial distribution of near neighbors • Measurement of sample thickness • Valence and conduction electron density • Polarization response (complex dielectric function) 	<ul style="list-style-type: none"> • Expensive and destructive technique • Sample preparation is very time consuming • Sample dimension small • Energy and spatial resolution limited by the TEM

A typical electron energy loss spectrum is shown in Fig. 3.17(a). It consists of three parts:

1. Zero-loss peak (at 0eV) which is the forward scattered electrons that having the original beam energy E_0 , i.e., they have only interacted elastically or not at all with the specimen.
2. Low-loss region (<50eV) consists phonon excitations, Čerenkov radiation, inter/intra-band transitions and plasmon excitations. Plasmon is longitudinal wave-like oscillations of weakly bound electrons. It dominates in materials with free electron structures. Typical value of plasmon mean free path is about 100nm. Thick sample gives plural plasmon scattering, thus degrade the accuracy of analysis.
3. High-loss region (>50eV) corresponds to inner-shell ionization. Source electron transfers sufficient energy to K, L, M, N, or O shell electron to move it outside the attractive field of nucleus. Since the excitation process is not affected by the fluorescence yield of x-ray (i.e., heavier atom gives higher x-ray emission probability when excited), it is successfully used for light element analysis comparing with x-ray related techniques.

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Figure 3.17(a) illustrates the 3 different regions using NiO as an example. The peaks arise from different oscillations or transitions based on energy band theory.

Figure 3.17. (a) EELS spectra for NiO with zero loss, plasmon loss and high loss Ni and O peaks. (b) Energy Loss Near Edge Structure (ELNES) with relation to the unoccupied DOS [13].

In solid state material studies, we are dealing with atoms integrated into a crystal lattice or an amorphous structure. We will usually see some fine structure near or extended from the ionization edge, which is termed as Energy Loss Near-Edge Structure (ELNES) and Extended Energy Loss Fine Structure (EXELFS), as shown in Fig. 3.17 (b) [13].

A core electron may receive enough energy to be ejected from its core states to the unbound states. The final state of the electron will be in some state above the Fermi surface, but not with equal probability due to the uneven distribution of electron density states and transition selection rules. The near edge structures are strongly affected by the unoccupied electron density of states and therefore important since DOS is extremely sensitive to changes in the bonding, or

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the valence state of the atom. If the ejected electron does not fill an empty state, its excess energy can also be interpreted as an electron wave which can be diffracted by surrounding atoms in the structure, giving rise to EXELFS. Because the electron has higher energy than those which give rise to ELNES, the diffraction is assumed to be single scattering. We are interested in EXELFS because of the structure information contained in the intensity oscillations. We can determine the partial Radial Distribution Function (RDF) around a specific atom. But it is difficult to see EXELFS modulations experimentally because they are only about 5% of the edge intensity.

The EELS signal processing is critical for result interpretation. Here outlines the basic processing procedures used in this study. A typical energy range of a core loss spectrum is 200 eV with 0.1eV/channel dispersion setting. Therefore, it is not always possible to include the zero loss peak during core edge acquisition for energy calibration. Instead, the low loss spectrum is acquired before and after the core edge acquisition (e.g., a core loss line scan across the gate stack) to determine the drift of the zero loss peak. An alternate way is to use some well-defined core loss edges to calibrate the onset energies of other edges. In this study, the gate stack consists of metal or polycrystalline Si gate, dielectrics and single crystal Si as the substrate. The Si $L_{2,3}$ edge at 99.8 eV can be used to calibrate the energy of the line scan. Figure 3.18 shows the low loss spectrum and O K edge core loss spectrum collected from bulk SiO_2 . The zero loss peak in Fig. 3.18(a) was aligned at 0 eV energy loss before the O K edge was collected for energy calibration. The second step of the data processing after energy calibration is to remove the background and extract the edge signals. Figure 3.18(b) depicts the power-law background fitting of the O K edge of SiO_2 .

Figure 3.18. (a) Low loss EELS spectrum collected from bulk SiO₂. (b) O K edge core loss EELS collected from bulk SiO₂ with power-law background fitting.

The O K edge after background removal is shown in Fig. 3.19(a), where 10, 20 and 30 eV window is used respectively for background subtraction. The variation in edge signal is small in this case since the background fitting is smooth. However, it gives smaller energy window for background fitting for Ti L edge as the tail of N K edge in front raises the signal background, as

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displayed in Fig. 3.19(b). The background subtraction needs to be done carefully by choosing an optimum energy window.

(a)

(b)

Figure 3.19. (a) O K edge signal after background removal using 10eV, 20eV and 30eV window (b) N K and Ti L edge of TiN showing small window of background fitting.

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The third step after background removal is to remove the plural scattering signals. This can be easily done using the Fourier-Log and Fourier-Ratio algorithm in commercial software package Gatan DM. An example is shown in Fig. 3.20 for SiO₂ low loss and O K edge core edge EELS.

Figure 3.20. (a) Low loss EELS and (b) O K edge EELS of bulk SiO₂ after plural scattering removal using Fourier-Log and Fourier-Ratio algorithm in Gatan DM package.

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As introduced in section 3.4, the TEM samples used in this study are prepared with *in-situ* lift-off with a final thickness less than 80 nm. The probe diameter during EDS/EELS signal acquisition is half a nanometer. Therefore, the spatial resolution of the chemical analyses is not degraded by beam spreading. However, beam damage is observed when putting a 0.2nm electron probe on Si substrate for around 60 seconds at 300kV acceleration voltage, as shown in Fig. 3.21. In order to minimize the beam damage, 80kV acceleration was used for Si/SiO₂ samples where no observable change was shown before and after EELS acquisition. For high- κ /metal gate stacks, 300kV acceleration was used.

Figure 3.21. Beam damage on Si substrate after putting a 0.2nm electron probe at locations indicated by arrows for about 60 seconds at 300kV acceleration voltage.

3.5.3 Sample Configuration and Experimental Details of EELS Chemical Analysis

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Figure 3.22 are the schematic plots of the sample configuration with a BD in the gate dielectrics which are subjected to physical analysis.

Figure 3.22. Schematic diagrams of **(a)** the BD transistor after FIB thinning. For presentation purposes, the poly-Si gate and other materials above the dielectric are not shown. The BD spot is included within the TEM sample for EELS analysis, **(b)** the orientation of the BD transistor in TEM chamber, where the sub-nanometer electron probe transmits through the sample in its thickness direction. Please note that the electrons that pass through the sample carry information from the percolation path as well as the rest of the non-BD oxide volume.

In Fig. 3.22(a), the BD transistor after FIB milling is shown. The poly-Si gate and other materials above the dielectric are removed for presentation purpose. A successful sample preparation retains the BD gate oxide within the TEM sample after milling from gate width W to TEM lamella thickness t . However, there are still possibilities to lose the BD spot if it lies at the edges

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of W since we do not know the BD location along W (we can only measure its location along L as discussed in earlier section). The TEM sample is then analyzed by TEM/EELS from its cross-sectional view of the gate stack, see Fig. 3.22(b). The STEM sub-nanometer electron probe scans through the gate stack at the BD location and carries information from the BD spot and the rest of the non-BD gate oxide when transmitting through the sample. Therefore, a reference scan is always needed from the surrounding non-BD area where the sample thickness should be as close as the one from the BD scan. In this case, a direct comparison between BD and non-BD is possible to reveal the ‘real’ signal from the BD dielectrics.

Figure 3.23 shows the schematic diagrams of both the top view (a) and cross sectional view (b) of the BD gate stacks under STEM/EELS analysis. The STEM scans at BD and non-BD (reference) locations are illustrated in the figures. STEM line scans with a point-to-point separation of 5 Å and 3-4 Å probe size are employed to access the chemical information of the gate stack. At each point, signals carrying sample’s chemical information are detected by EELS and EDS simultaneously. Both ‘horizontal’ and ‘vertical’ scans can be used. But the ‘vertical’ line scan is preferred to minimize the signal uncertainty induced by sample drift.

An example of ‘horizontal’ scan in a 2-nm gate oxide is shown in Fig. 3.24. In moving the electron probe from the spacer oxide of the MOSFET into the gate oxide, the oxygen counts (integrated from 532 to 552 eV) decreases and stabilizes at one particular value which is determined by the number of oxygen atoms in the TEM sample thickness direction. However, there are some fluctuations of the O intensity observed over 3 nm range in the later stage of the line scan.

Figure 3.23. Schematic diagrams of (a) top view and (b) cross-sectional view of the STEM/EELS experiment details when analyzing the BD gate dielectric. The STEM scans at BD and non-BD (reference) locations are illustrated in the figures. STEM line scans with a point-to-point separation of 5 Å and 3-4 Å probe size are employed to access the chemical information of the gate stack. At each point, signals carrying sample's chemical information are detected by EELS and EDS simultaneously. 'Vertical' line scan is preferred to minimize the signal uncertainty induced by sample drift.

This signal uncertainty is believed to be originated from the thermal drift of the sample. Since the O concentration is very sensitive to the position in the 2-nm thick gate oxide (refer to Fig. 3.25), even a sub-nanometer drift of the sample will induce a change in the signal intensity.

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Moreover, the gate dielectric breakdown sometimes also induces microstructural change (e.g., DBIE) at adjacent electrodes; and this morphological change affects the signal too during the horizontal line scan. Therefore, it is not recommended to use horizontal line scan. Instead, a vertical line scan is used.

Figure 3.24. (a) STEM-HAADF micrograph of a poly-Si/SiON/Si gate stack at the gate corner. A horizontal line scan is performed in the gate oxide. (b) The oxygen counts integrated from 532 to 552 eV at each position of the line scan. As moving from the spacer oxide into the gate oxide, the oxygen content decreases and stabilizes at certain value proportional to the sample thickness. The signal fluctuation is observed as indicated in (b) due to the sample drift.

A vertical scan across the gate stack probes the elemental distribution in the gate dielectric layer as well as the local information from the top and bottom electrodes. In Fig. 3.25, the profiles of oxygen in the 2 nm SiO₂ and 2.5 nm HK (HfSiO_x) with 1.2 nm IL (SiO_x) are plotted using O-K edge (532-552 eV) intensities. It is clearly shown that the intensity counts of oxygen are very sensitive to the position in the gate dielectrics. For the 2 nm SiO₂ in Fig. 3.25(a), the O counts drop significantly from the center of the oxide layer (i.e., the local maximum) to the sub-oxide region and causes a signal uncertainty in a horizontal line scan for a slight drift in sample

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position. In a vertical scan however, the drift problem can be minimized since we have the full distribution of the elements across the gate stack. In order to find out the compositional change of the BD gate dielectrics, spectra with maximum intensities (assuming at the center of the gate dielectric) from different locations, both BD and non-BD gate dielectrics, are acquired and plotted together for comparison.

Figure 3.25. O-K edge EELS line profiles across (a) 2 nm SiO₂ and (b) 2.5 nm HfSiO_x/1.2 nm SiO_x HK gate dielectrics.

Figure 3.26(a) shows the O-K edge EELS at the center of a 2-nm gate oxide from 5 non-BD locations under same experimental conditions. It shows similar oxygen counts in the gate oxide, which indirectly confirms that the sample prepared by FIB milling is very uniform in thickness over a relatively large region. The signal fluctuation can be controlled well using vertical line scans. In this case, the O signal variation integrated from 532 to 552 eV is less than 5%. Therefore, any signal variation larger than 5% can be considered as change in oxygen density (e.g., induced by BD) for this case.

Figure 3.26. (a) O-K edge EELS acquired at the center of a 2-nm gate oxide from 5 different locations. The experimental conditions are kept identical during the signal acquisitions. (b) Relative compositions of Si and O in a vertical line scan across a 2-nm SiO_2 gate stack. Si- $L_{2,3}$ and O-K edges are used for the profile extractions with 10 eV (99-109 eV) and 20 eV (532-552 eV) energy window, respectively.

The distribution of the elemental composition can be quantified in an EELS line profile. Figure 3.26(b) shows the relative composition of Si and O in a vertical line scan across the 2-nm SiO_2 gate stack. Si- $L_{2,3}$ edge (10 eV energy window) and O-K edge (20 eV energy window) are used for the calculation. This method is implemented in the following chapters to study the degree of oxygen deficiency in the BD gate oxide.

Generally speaking, the following experimental measures can be used to increase the signal-to-noise ratio and enhance the detectability: i). Increase the acquisition time to suppress instrumental noise and the drawback is sample drift during acquisition; ii). Control FIB sample uniformity to eliminate the signal variations from sample thickness; iii). Use smaller probe size with finer point-to-point separation to increase the resolving power during the line scan but the drawback is the weaker beam intensity. From TEM/EELS point of view, thinner TEM sample is

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required for better imaging and signal acquisition (e.g., less multiple scattering). But thinner sample increase the possibility of losing the BD spot as discuss in Section 3.3. Therefore, significant efforts are needed to fine-tune the experimental setups so as to find out the most optimized sample configuration to achieve a successful nano-scale physical analysis.

3.6 Summary

This chapter describes the details of the devices, electrical stressing methods, and electrical and physical analysis equipment used. The samples used in this study are conventional poly-Si/SiO₂ as well as new generation metal-gate/high- κ gate stacks. In order to study the failure mechanisms of the gate dielectrics, both electrical and physical analysis are implemented. Various electrical device characterization and stressing methodologies have been discussed. Precision TEM sample preparation methods using focused ion beam are described. To extract the physical information of defects in the gate dielectric layer, scanning transmission electron microscopy and electron energy loss spectroscopy techniques were used. The sample configuration and EELS setup are introduced. Experimental challenges are discussed and possible methods to minimize the experimental uncertainties are proposed.

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CHAPTER FOUR

CHEMICAL NATURE OF PERCOLATION PATH FORMED IN ULTRATHIN SILICON OXYNITRIDE GATE DIELECTRICS

4.1 Introduction

Dielectric breakdown is a universal process underlying a broad variety of natural phenomena, from corona discharge to thunder lightning, as well as man-made electrical devices such as laser printer and disruptive components in a circuit [1]. Mathematical models [2] have been made available to explain the randomness and fractal nature of a breakdown. Dielectric breakdown model typically describes the macroscopic behavior combining diffusion-limited aggregation with electric field for solids, liquids, and gases. Despite the success of the mathematical models, these phenomenological descriptions failed to reveal fundamental physical mechanism responsible for an insulating material transforming into a conductive path locally at the breakdown site. In this chapter, we study dielectric failure in a SiO₂ gate oxide and the chemical nature of the post-breakdown percolation path is revealed for the first time.

4.2 How to Choose the Best Sample for Physical Analysis

The lack of understanding on the physical process of a dielectric breakdown is largely due to the difficulties involved in determining and analyzing the microscopic breakdown path within the dielectric materials. The experimental challenges pose two key difficulties to overcome. Firstly, the nano-scale breakdown path needs to be accurately located and isolated for analysis. Depending on the analytical tools chosen, sample preparation plays an important role in the analysis process. Not only that the size of the breakdown path is only a few nanometers in diameter, but also the dielectric breakdown spot is buried underneath the electrode, such as metal line conductors and protective insulator coatings. Secondly, despite of the efforts over the years [3-5], the nature of a breakdown percolation path remains unknown today and there is no simple way to know whether the sample prepared contains the percolation path. Since the percolation path is typically invisible under the analytical tools used, a clear signature or nano-marker must be present to aid the navigation and eventually confirmation of the existence of a percolation path.

To overcome the above difficulties, a proper sample structure must be used to aid and identify the breakdown location for sample preparation, and subsequently to navigate to the breakdown spot even though the breakdown path is invisible under microscope. The metal-oxide-semiconductor transistor is an ideal structure for dielectric breakdown studies. The electrical behavior of the dielectric layer is easily characterized using the four electrodes of the transistor. The size of the transistor can be selected to be as small as a typical transmission electron microscopy sample thickness so that a breakdown spot can be obtained. Moreover, dielectric breakdown due to electrical stressing or testing can trigger damages to the physical integrity and microstructure in the surroundings of the breakdown spot of the device [6, 7]. It

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was demonstrated that dielectric breakdown induced epitaxy marks an important physical signature of breakdown location where the invisible percolation path can be located unambiguously [8, 9].

The current limited 2-step CVS is the methodology adopted in this study to induce the breakdown in the gate dielectrics for physical analysis. Narrow transistor samples with gate width $W \leq 0.15 \mu\text{m}$ were selected as the test devices to increase the success rate of catching the BD spot after FIB milling. The success rate of finding the BD defects under TEM can be as high as 90% for samples with high failure current I_{gl} . However for chemical analysis, we need the samples to be failed at the desired BD hardness but yet the gate dielectric must be intact for EELS/EDS probing. We will discuss how to choose the right sample in this section and its issues.

4.2.1 Controlled Breakdown Using Compliance Current Limit I_{gl}

As discussed in Chapters 2 and 3, the breakdown hardness can be controlled by the compliance current limit I_{gl} . Various microstructural defects associated with the progressive BD have been identified [6, 7]. Generally speaking, higher failure current corresponds to harder BD hardness and severer physical damage. As shown in Fig. 4.1, DBIE and local amorphization are observed for harder BDs. At the respective BD locations, the gate oxide is ruptured and the physical change (e.g., DBIE) at the top and bottom electrodes effectively creates a short circuit and gives rise to a high gate leakage current.

Since one of the main objectives of this study is to investigate the chemical change in the gate dielectric material when it loses its insulating properties and becomes conductive, it is obviously not possible for samples with a ruptured oxide and local melting to be used for EELS/EDS analysis, even though we have captured the defective BD spot. Therefore, samples

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with controlled damage at the BD are desired for chemical analysis. This can be easily achieved by lowering the I_{gl} to softer BDs, e.g., $I_{gl} < 20 \mu\text{A}$.

Figure 4.1. STEM-HAADF and HRTEM micrographs of four poly-Si/SiON nMOSFET samples ($T_{ox} = 2.2 \text{ nm}$) with the gate oxide failures at their respective breakdown locations. The final failure was stressed using $V_{gstress} = 3.1 \text{ V}$ and (a) $I_{gl} = 20 \mu\text{A}$, (b) $I_{gl} = 90 \mu\text{A}$, (c) $I_{gl} = 130 \mu\text{A}$ and (d) $I_{gl} = 500 \mu\text{A}$. Severe structural damage like DBIE and local amorphization are observed. The TDDB failure was induced by a CVS of $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \mu\text{A}$.

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Figure 4.2 shows the HAADF micrograph of a sample failed at $I_{gl} = 2 \mu\text{A}$, the gate oxide at the BD location is intact and a minor DBIE is found. Even though we have limited the physical damage using a small I_{gl} and captured the BD, it poses a challenge for the signal detection in the EELS analysis since the BD spot can be extremely small in size for soft BDs [10]. As introduced in Chapter 3, the “real” signal from the BD area is superimposed with the non-BD signal (in TEM sample thickness direction when the electrons transmit through). It therefore limits the detectability of the BD chemistry for very soft BDs. On the other hand, harder BDs give rise to stronger signals for detection but bear higher possibility of having severe physical damage, which also limits the feasibility of a decent STEM/EELS analysis. As a result, extra attention/efforts are needed here to control the electrical stress and make the best sample for the subsequent physical study.

Figure 4.2. STEM-HAADF micrograph of a poly-Si/SiON nMOSFET sample ($T_{\text{ox}} = 2.2 \text{ nm}$) failed at $I_{gl} = 2 \mu\text{A}$.

4.2.2 DBIE as Nano-marker

As a lower I_{gl} is used, the physical defects associated with the BD are less visible [6, 7]. Therefore, we need a ‘nano-marker’ to help us in pin-pointing the exact location of the BD. DBIE [7, 9] is served for the best marker as it is induced by the BD event and proved to be an universal physical signature of a BD. Figure 4.3 illustrates BD samples with minor DBIE nano-markers at their BD locations for different I_{gl} . The gate oxide atop of the DBIE shows no clear physical change as compared with the surrounding non-BD oxide. It is therefore important to have the nano-marker to locate the BD, especially for very soft-BDs.

Figure 4.3. HRTEM micrographs of four poly-Si/SiON nMOSFET sample ($T_{ox} = 2.2 \text{ nm}$) with minor DBIE nano-markers at their respective BD locations for TEM/EELS analysis. The compliance current limits are $I_{gl} =$ (a) $50 \mu\text{A}$, (b) $200 \mu\text{A}$, (c) $70 \mu\text{A}$ and (d) $20 \mu\text{A}$.

4.3 Characterization Using Valence Electron Energy Loss Spectroscopy (VEELS)

The BD in the gate oxide is created by the electrical stress with a preset I_{gl} and located using the DBIE nano-marker after TEM sample preparations. In this section, the chemical information of the BD oxide is studied using low loss EELS or valence-EELS. However, the analysis is severely limited by the thickness of the gate oxide in a MOS structure due to the delocalization nature of inelastic scattering [11].

4.3.1 Difficulties Due to Delocalization

The concept of delocalization can be introduced using the simple experiment performed in 1974 by Isaacson [12], who found that the inelastic signal changed more gradually than the elastic one, showing inelastic scattering to be more delocalized than high-angle elastic scattering. R. F. Egerton [13] calculated the localization diameter of the electron probe with a 100 keV incident energy, as shown in Fig. 4.4(a). The incident electrons can be inelastically scattered (with energy transfer) by the local atoms of the sample within a range of $\sim 3\text{-}4$ nm at 10 eV energy loss and ~ 0.6 nm at 100 eV energy loss. If we increase the incident energy of the electron probe from 100 keV to 300 keV, the localization length increases by 10% as illustrated in Fig. 4.4(b).

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Figure 4.4. (a) Measurements and calculations of the localization distance for inelastic scattering, plotted as a function of energy loss. The data has been adjusted to the 100 keV electron energy. (b) Localization length (relative to the value at $E_0 = 100$ keV) as a function of incident energy E_0 . [13]

The delocalization nature of the inelastic scattering has a significant impact on nano-structure characterization such as the gate oxide, especially the low-loss EELS. As introduced in Chapter 3, the low loss part of the EELS consists of inter/intra-band transitions and plasmon peak. It reflects the electronic structure of the valence band as well as dielectric response of the valence electrons. The band gap can usually be measured using low-loss EELS when the onset of the inter-band transition occurs. However, due to the large localization length (i.e., more delocalized) at lower energies, the incident electrons could access the materials not only at the probing site, but also the materials in the vicinity of the electron probe by inelastic scattering. This limits the analysis for structures smaller than the localization length, e.g., ultrathin gate oxide. Figure 4.5 are the low-loss EELS extracted from bulk Si, bulk SiO_2 and gate SiO_2 (6 spectra acquired at the center of a 22Å-thick oxide layer). The spectra are normalized to the zero loss peak. The EELS energy resolution is around 0.7 eV and the microscope was operated at 80 kV.

Figure 4.5. Low loss spectra of bulk Si, bulk SiO₂ and gate SiO₂ (6 spectra acquired at the center of a 22Å-thick oxide layer). The spectra are normalized to the zero loss peak. The EELS energy resolution is around 0.7 eV and the microscope was operated at 80 kV.

As shown in Fig. 4.5, the bulk plasmon peak for Si and SiO₂ is located at 16.6 eV and 23 eV, respectively. The onset of SiO₂ interband transition starts at 9.5 eV (bandgap). However, the SiO₂ low loss peaks behave differently for a sandwiched Si/SiO₂/Si structure (i.e., gate stack in MOSFETs) from its bulk case. The SiO₂ bulk plasmon peak (23 eV) is suppressed by the adjacent Si plasmon peak even with a 3 Å probe analyzing at the center of the 22Å-thick oxide layer. The bandgap onset (~10 eV) is no longer visible as a result of delocalization such as Si interband transition, coupling of interface plasmon peaks (~8 eV) and other relativistic effects (e.g. Čerenkov radiation) [14]. The data interpretation in this case becomes much more complex.

Figure 4.6. Si-L_{2,3} edge EELS of bulk Si, bulk SiO₂ and 22Å-thick gate SiO₂ layer. The delocalization effect is still present at 100 eV energy loss.

The effect of delocalization can also be found at 100 eV energy loss (i.e., core loss EELS). Figure 4.6 shows the Si-L_{2,3} edge EELS of the bulk Si, bulk SiO₂ and 22Å-thick gate SiO₂ layer collected from the same transistor sample. The STEM probe size was around 3-4 Å during EELS acquisition. It is clearly shown that the spectrum of the gate oxide consists of both Si⁰ (delocalized signal) and Si⁴⁺ signal. In summary, the delocalization effect must be taken into consideration when analyzing the results of the breakdown gate oxide.

4.3.2 Delocalized Low Loss Spectra from Breakdown Oxide

VEELS analysis has been performed on the percolated gate oxide in an attempt to extract its local dielectric properties and bandgap information. Figure 4.7(a) shows the electrical results of

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one sample ($W \times L = 0.15 \times 0.20 \mu\text{m}^2$) stressed using the 2-step CVS. The final failure current was capped at $70 \mu\text{A}$ I_{gl} . Pre- and post-breakdown I_g - V_g characteristics are shown in Fig. 4.7(b).

Figure 4.7. (a) Time evolution of the gate leakage current I_g for a poly-Si/SiON nMOSFET sample ($T_{ox} = 2.2 \text{ nm}$ & $W \times L = 0.15 \times 0.2 \mu\text{m}^2$) failed under a 2-step CVS. The final failure current limit I_{gl} is $70 \mu\text{A}$. **(b)** Pre- and post-breakdown I_g - V_g characteristics.

In Fig. 4.8(a), the TEM micrograph was collected at the gate edge near the drain terminal. At the breakdown location, $0.83L$, a minor DBIE was identified as shown in the inset. VEELS analysis was performed at the gate oxide above the DBIE hump using a monochromatic mode. The energy resolution as shown from the zero loss peak acquired at the Si substrate in Fig. 4.8(b) was around 0.28 eV .

Figure 4.8. (a) Cross-sectional TEM micrograph of a sample failed at $I_{gl} = 70 \mu\text{A}$. At the breakdown location, $0.83L$, a minor DBIE was identified as shown in the inset. VEELS analysis was performed at the gate oxide above the DBIE hump. (b) Zero loss peak acquired from the Si substrate in monochromatic mode. The energy resolution at the full-width-half-maximum (FWHM) of the zero loss peak is 0.28 eV.

Figure 4.9 are the plots of low loss spectra of bulk Si, bulk SiO_2 , BD and non-BD gate SiO_2 . Two spectra acquired from the center of a $22\text{\AA}$ -thick gate oxide layer at the BD and non-BD locations are shown for direct comparison. All the spectra are normalized to the respective zero loss peak. Due to the delocalization effect, the only difference observed for BD and non-BD gate oxide is the plasmon peak, both at the Si and SiO_2 bulk plasmon peaks. As indicated in the figure, the BD oxide shows higher Si bulk plasmon intensities but lower bulk SiO_2 plasmon intensities. We also performed similar measurements for other breakdown hardness, i.e., $I_{gl} = 2 \mu\text{A}$ & $35 \mu\text{A}$ at 80 kV acceleration. The EELS energy resolution degraded to around 0.7 eV without using the monochromator. Nevertheless, similar results were observed as shown in Fig. 4.10.

Figure 4.9. Low-loss spectra of bulk Si, bulk SiO₂, BD and non-BD gate SiO₂ (2 spectra acquired from the center of a 22Å-thick gate oxide layer at the BD and non-BD locations). The spectra are normalized to the zero loss peak. The EELS energy resolution is around 0.28eV and the microscope was operated at 300kV.

Figure 4.10 shows the low loss spectra of gate oxide for two breakdown hardness ($I_{gl} = 2 \mu\text{A}$ & $35 \mu\text{A}$) at the respective BD and non-BD locations. Again, the only noticeable difference is at the bulk SiO₂ plasmon peaks. The BD oxide shows lowered intensities, as highlighted in the inserted plot. The harder BD sample (35 μA) gives a larger difference at ~23 eV since the volume ratio of the defective oxide to non-defective oxide (in the STEM sample thickness direction) is bigger, leading to stronger signals.

Figure 4.10. Low-loss spectra of 22Å-thick gate oxide for two breakdown hardness (2 & 35 μA) at the BD and non-BD locations. Bulk SiO₂ low loss spectrum is also shown for comparison purpose. The separation of the spectra for 2 & 35 μA is due to the thickness difference of STEM samples as highlighted in the inset. The spectra are normalized to the respective zero loss peak. The EELS energy resolution is around 0.7 eV and the microscope was operated at 80 kV.

4.3.3 Theoretical Calculation of Delocalized Spectra

In order to understand the low-loss intensity decrease observed for the defective oxide at ~23 eV, a model developed by Bolton and Chen [15] was used to simulate the low loss spectra of a stratified system with relativistic and interface effects. The model is simplified to Eqn. (4.1) for a special case (i.e., the electron probe is at the center of the m^{th} layer for a symmetrical system with $n = 2m-1$ slabs).

$$I(\hbar\omega) = \frac{d^3P}{d\omega dk_y dz} = \frac{e^2}{4\pi^2 \epsilon_0 \hbar v^2} \text{Im}\{\chi_m^{(n)}\} \quad (4.1)$$

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$$\chi_m^{(2m+1)} = \frac{1}{q_m \epsilon_m k^2} \left\{ \epsilon_m k_y^2 \frac{v^2}{c^2} \frac{\tilde{L}_{m-1,0}^+}{\tilde{L}_{m-1,0}^-} - q_m^2 \frac{L_{m-1,0}^-}{L_{m-1,0}^+} \right\} \quad (4.2)$$

where the energy loss probability density per unit path length I for the transferring energy $\hbar\omega$ and the y -momentum $\hbar k_y$ is proportional to the imaginary part of the loss function χ . The symbols in Eqns. (4.1) & (4.2) carry their usual meaning [15] and the detailed theoretical formulation are presented in Appendix-I [15]. Figure 4.11 shows the schematic of the 3-layer (1 slab + 2 infinite Si) and 5-layer (3 slabs + 2 infinite Si) symmetrical systems used in the simulation models.

Figure 4.11. Schematic diagram of a 3-layer (1 slab + 2 infinite Si) and 5-layer (3 slabs + 2 infinite Si) symmetrical systems. The sample thickness t is infinite in the calculation and oxide thickness $T_{ox} = 2$ nm.

Using the complex dielectric functions of bulk Si, SiO₂ and monoxide SiO [16], the loss function χ (and the EELS spectrum) is calculated for Si/2nm SiO/Si, Si/0.5nm SiO/1nm SiO₂/0.5nm SiO/Si, Si/2nm SiO₂/Si and Si/10nm SiO₂/Si systems. As shown in Fig. 4.12, the intensities at SiO₂ bulk plasmon region decrease as we gradually replace the 2nm SiO₂ with SiO. Figs. 4.10 and 4.12 suggest that the dielectric properties of the defective oxide appear to be SiO-like. There are also changes at the Si plasmon, Si interband and interface plasmon regions in Fig. 4.12.

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However, we did not see similar results in our experimental results shown in Fig. 4.10, probably due to the poor energy resolution and the complex geometries of the sample. The theoretical formulation [15] and C++ programming code are shown in Appendix-I.

Figure 4.12. Simulation results of the low loss spectra for 4 different symmetrical systems. The kinetic energy of incident electron is estimated based on the 80kV acceleration, and a cutoff frequency q_c of 15nm^{-1} (6mrad) is used.

4.4 Characterization of Using Core Loss EELS

The use of low-loss EELS on ultrathin gate oxide is limited by the poor spatial resolution as a result of the delocalization. However, the delocalization effect can be successfully suppressed by higher energy edges, i.e., the core-loss EELS. Recall that the high-loss region (> 50 eV) includes various inner-shell ionization edges. In this section, we present the core loss EELS results obtained from breakdown gate oxide in an attempt to reveal the chemical nature of the percolation path.

4.4.1 Si L_{2,3} and O K Edge EELS and Near Edge Structures

Figure 4.13(a) shows the electrical results of one sample ($W \times L = 0.15 \times 0.2 \mu\text{m}^2$) stressed using the 2-step CVS. The final failure current was capped at $I_{gl} = 200 \mu\text{A}$. Pre- and post-breakdown I_g - V_g characteristics are shown in Fig. 4.13(b).

Figure 4.13. (a) Time evolution of the gate leakage current I_g for a poly-Si/SiON nMOSFET sample ($T_{\text{ox}} = 2.2 \text{ nm}$ & $W \times L = 0.15 \times 0.2 \mu\text{m}^2$) failed under a 2-step CVS. The final failure current limit I_{gl} is $200 \mu\text{A}$. **(b)** Pre- and post-breakdown I_g - V_g characteristics.

Figure 4.14 shows the HRTEM and STEM cross-sectional views of a transistor sample with a breakdown in the gate oxide layer. The electrical location of the leakage path is at the center of the channel length. The HRTEM micrograph, Fig. 4.14 (b), shows the 2 nm gate oxide at the breakdown location with a DBIE identified and delineated. Figure 4.14(c) is the corresponding STEM annular dark field (ADF) micrograph. As shown in Fig. 4.14(b) and Fig. 4.14(c), the percolation path directly atop of DBIE is invisible in ordinary TEM/STEM imaging modes. Subsequently, EELS analysis was performed at the breakdown location (i.e., above the DBIE), in an attempt to analyze the chemical nature of the percolation path.

Figure 4.14. TEM/STEM cross-sectional views of a transistor with dielectric breakdown. (a) Low magnification TEM cross-sectional micrograph of a failed transistor ($W \times L = 0.15 \times 0.2 \mu\text{m}^2$). The breakdown location measured electrically is at the center of the channel length, as highlighted in the dotted circle. (b) High resolution TEM lattice micrograph of the breakdown location. DBIE is marked and the oxide area on top of the DBIE bump is displayed. (c) Annular Dark field (ADF) micrograph of the breakdown location. It shows no difference for the oxide area on top of the DBIE bump as compared to the non-breakdown oxide.

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Figure 4.15 illustrates the close-up view of the sample configuration and beam-sample interaction. STEM/EELS spectra were collected using point-to-point vertical scan across the dielectric layer at the breakdown site and at the non-breakdown site.

Figure 4.15. Schematic diagram of the STEM-EELS point-to-point scan across the gate dielectric layer at breakdown and non-breakdown locations. The percolation path is located at the oxide areas on top of the DBIE.

Figure 4.16 shows the background corrected Si- $L_{2,3}$ edge spectra from 3 different positions, including a spectrum at a non-breakdown oxide/Si interface (short-dashed line) for comparison. The edge intensities have been normalized with the same incident electron dose. The spectrum for a non-breakdown (normal) gate oxide (dash-dotted line) has a Si^{4+} bonding characteristic between 106 and 108 eV [17] with a shoulder peak extended down to 100 eV. The additional energy states appeared below 106 eV are attributed to the delocalized signals [11, 13, 18] from the interface suboxide [17], which can also be seen in spectrum from the oxide/substrate interface. The Si $L_{2,3}$ edge for the breakdown oxide (solid line) as compared to the non-breakdown oxide (dash-dotted line) shows reduced intensities at 108 eV (Si^{4+}) but increased intensities between 100 eV and 105 eV (Si^0 and intermediate oxidation states, Si^{1+} , Si^{2+} and Si^{3+}). From our momentum resolved density of state calculation using all electron density functional theory (DFT) performed on α -quartz SiO_2 , the effect of oxygen vacancy will lower the s -states

[19] at 108 eV but create more *s*- and *d*-states below 106 eV, which agree with the current experimental observations. The obvious increase in the EELS intensities from 100 eV to 105 eV suggests the presence of Si atoms coordinated with less than 4 oxygen atoms (i.e., suboxide) and possible Si nanoscopic clustering [17].

Figure 4.16. The background corrected Si-L_{2,3} edge spectra from breakdown (solid), non-breakdown (dash-dotted) gate oxide and oxide/Si interface (short-dashed). The breakdown oxide shows less Si⁴⁺ signals at 108 eV but more Si⁰ and Si intermediate oxide state signals below 106 eV as a result of oxygen deficiency. The inserted figure shows the enlarged plot from 105 eV to 110 eV for breakdown and non-breakdown oxide. The EELS measurements were performed on a FEI-TITAN 300 kV TEM/STEM. The probe size was set to be approximately 4 Å in diameter and the EELS energy resolution is 1.5 eV with a 0.3 eV/channel dispersion (600 eV energy range). The spectra collected from the central region of gate oxide at breakdown and non-breakdown locations are extracted for comparison.

The normalized O-K edge core-loss from the bulk oxide (solid), the non-breakdown (dashed), and the breakdown (dash-dotted) gate oxide are presented in Fig. 4.17. The first

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absorption peak at 537.8 eV as shown for the bulk oxide (solid line) is originated from the multiple scattering [20] of the ejected O 1s electron to its 6 second-nearest neighboring O atoms (1st O shell) [18]. It can be directly related to the local conduction band electronic properties [21, 22]. The spectrum for the non-breakdown gate oxide (dashed line) has the same absorption peak at 537.8 eV. However, the rising portion of the edge onset at ~530 eV is shifted to a lower energy as compared with the bulk oxide (solid line). This is likely due to the delocalized scattering from the interface suboxide which lowers the conduction band minimum [18, 22]. The reduced edge onset is also observed for the breakdown gate oxide (dash-dotted line). It is thus difficult to distinguish, from the O-K edge study for ultrathin gate oxide with signal delocalization, if the breakdown oxide has induced a local conduction band lowering. Comparing the first peak position between the non-breakdown and breakdown gate oxide, the peak position shifts from 537.8 eV to 536.3 eV upon breakdown. It is believed such shift is a result of conduction band *p*-DOS redistribution within the percolation path. Noted that a red shift (to a lower energy of about 4 eV) is observed in the second absorption peak (~560 eV) for both breakdown and non-breakdown gate oxide. This shift originates from the presence of stretched O-O bonds [23-25] in ultrathin gate oxide and was not affected by the breakdown.

Figure 4.17. The background corrected O-K edge spectra measured from bulk oxide (solid), breakdown (dash-dotted) and non-breakdown (dashed) gate oxide. The first peak position (537.8 eV) shifts to a lower energy (536.3 eV) as a result of conduction band p -states redistribution. The arrow indicates the edge onsets for non-breakdown gate oxide is lowered as compared to the bulk oxide. Si/O ratio was quantified using the edge intensity integrated from 99 to 129 eV for Si-L and 532 to 542 eV for O-K. The missing of O atoms at the breakdown area is reflected from the lowered intensities (dash-dotted line). The ratio for the breakdown oxide is $\text{SiO}_{0.9}$ normalized using the non-breakdown oxide as SiO_2 . However, this value is underestimated due to the difference between the percolation path diameter and TEM sample thickness.

The breakdown gate oxide as compared with the non-breakdown gate oxide shows significantly lower O-K core-loss signals. The decrease in the intensity arises from the missing O atoms [18] at the breakdown site. The deficiency of O atoms within the breakdown SiO_2 can be calculated using the core-loss signal intensities [26]. As shown in Fig. 4.18, the core loss Si-L_{2,3}, N-K and O-K edges are collected in one single spectrum. The N-K edge signal is extremely weak due to

its low atomic percentage ($N\% \sim 3\%$). The Si-L and O-K edge intensities in a vertical line scan are used for the relative quantifications of Si/O ratios.

Figure 4.18. Core-loss EELS of Si-L_{2,3}, N-K and O-K edges collected in one single spectrum. The N-K edge signal is extremely weak due to its low atomic percentage ($N\% \sim 3\%$). The Si-L and O-K edge intensities are used for the relative quantifications of Si/O ratios.

Using 10 eV (99-109 eV) and 20 eV (532-552 eV) energy window for Si-L_{2,3} and O-K edge respectively, the Si/O ratio across a 2-nm SiO₂ gate stack at the BD and non-BD locations are plotted in Fig. 4.19. All the Si and O relative compositions are purposely aligned at the oxygen maximum for comparison due to the topographical changes (e.g., DBIE) of the top or bottom electrode in the vicinity of the BD. The vertical line scan at the non-BD location is used as the reference, assuming a stoichiometric SiO₂. The Si/O ratios extracted from two line scans across the BD gate oxide, namely BD-1 and BD-2, are compared with the non-BD scan (i.e., reference) using the same energy window. Since the line scans are performed under the same experimental conditions and the thickness variation of FIB sample is low, it is believed that the change in the Si/O ratio are caused by the oxygen areal density difference induced by the BD. It is also

interesting to note that at the BD locations, the oxygen profiles shift towards the gate terminal, which follows the electron wind direction (substrate injection in this case).

Figure 4.19. Relative compositions of Si and O across a 2-nm SiO_2 gate stack at the BD and non-BD (as reference) locations. Si- $L_{2,3}$ and O-K edges are used for the profile extractions with 10 eV (99-109 eV) and 20 eV (532-552 eV) energy window, respectively. All the profiles are aligned at the oxygen maximum for comparison purpose. The Si/O ratio in the center of the BD oxide layer (i.e., oxygen maximum) is extracted using the non-breakdown oxide calibrated as SiO_2 with $\text{Si/O} = 1/2$.

As shown in Fig 4.19, the Si/O ratios at the maximum oxygen density (assuming it is at the center of the gate oxide layer) are 43/57 (non-BD reference), 46/54 (BD-1) and 54/46 (BD-2). If we calibrate the ratio of the non-BD oxide 43/57 to be 1/2 (i.e., SiO_2), the Si/O ratios of the BD oxide are $\text{SiO}_{1.8}$ at BD-1 and $\text{SiO}_{1.3}$ at BD-2. The results are illustrated in Fig. 4.20. The oxygen deficiency within the breakdown path calculated using this approach is as high as 50-60%. From the results shown in Figs. 4.16 and 4.17, the intensity change in the Si- $L_{2,3}$ edge is minimum compared with the O-K edge. This suggests that oxygen depletion, instead of silicon

accumulation, is the chemical and atomistic mechanism responsible for the ultra-thin SiO_2 oxide breakdown path formation.

Figure 4.20. TEM micrograph of a poly-Si/SiON nMOSFET sample ($T_{\text{ox}} = 2.2$ nm) failed at $200 \mu\text{A } I_{\text{gl}}$ at its BD location. Si/O ratios in the center of the gate oxide layer as measured by Si- $L_{2,3}$ and O-K edge EELS are SiO_2 at the non-BD location, $\text{SiO}_{1.8}$ and $\text{SiO}_{1.3}$ at BD location 1 and 2, respectively.

4.4.2 Band Structure Calculation of an Oxygen Deficient SiO_2 Supercell Using Density Functional Theory

The core-loss EELS contains the ionization edges that originate from the transitions of core shell electrons to the conduction band (CB) unoccupied density of states (u-DOS). The core-loss edge and near edge structures are usually the fingerprint of the local u-DOS as well as the atomic bonds [19]. In order to understand the experimental results of core-loss spectra (i.e., Si $L_{2,3}$ and O K edge), DOS calculation using density functional theory was done on α -quartz SiO_2 for a 36-atom supercell.

A large number of theoretical and experimental researches have reached a general consensus that the neutral oxygen vacancy (V_{O}) is a good candidate to describe deficient centers in SiO_2 breakdown [27-30]. Since the short range order of amorphous SiO_2 is known to be very

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similar to that of α -quartz [31], the α -quartz is used in this work. We used a periodic supercell of $2 \times 2 \times 1$ unit cells containing 36 atoms (12 Si atoms, 24 O atoms) to model crystalline α -quartz. It is demonstrated that with large supercell model, first-principles calculations are promising tools to investigate the geometrical and electronic structures of SiO_2 [31]. In order to study the effect of V_O concentration, we remove one ($1-V_O$) and two ($2-V_O$) oxygen atoms from the Si-O-Si network in α -quartz, respectively, as shown in Fig. 4.21. In the construction, we ensure the Si atoms in the $\equiv\text{Si}-\text{Si}\equiv$ bonds are not on the supercell boundary, therefore in this $2 \times 2 \times 1$ supercell, the maximum number of V_O is *two*. After the initial configurations were constructed, geometry optimizations were performed using all electron density functional theory implemented in a DMOL³ package [32]. The DFT calculations were performed using generalized gradient approximation (GGA) with the functional parameterized by Perdew, Burke, and Enzerhof (PBE) [33] and the double-numerical-polarization (DNP) basis set that includes all occupied atomic orbitals plus a second set of valence atomic orbitals plus polarized *d*-valence orbitals was employed. It was shown that the PBE functional gives electronic structure for a large set of tested molecules closer to the experimental values than any other method available in DMol³ [34]. Self-consistent field calculations were done with a convergence criterion of 10^{-6} hartree on the total energy. The Brillouin zone integration was performed using a $6 \times 6 \times 6$ Monkhorst-Pack *k*-point grid. All the structures were fully optimized with a convergence criterion of 0.002 hartree/Å for the forces and 0.005 Å for the displacement. A real-space cutoff of 4.0 Å for the atom-centered basis set was chosen to increase computational efficiency while not significantly affecting the magnitude of inter-atomic forces or the total energies. The Gaussian smearing of electron density was applied with the energy range of 0.2 eV.

Figure 4.21. Schematic picture of the α -quartz used in the calculation. Left column: side-view; right column: top-view. From top to bottom, are undefected α -quartz, 1- V_O α -quartz, and 2- V_O α -quartz, respectively. The blue dotted cage represents the $2 \times 2 \times 1$ supercell volume. Si and O atoms are represented in yellow and red, respectively. The arrows indicate the V_O centers.

The equilibrium structures of α -quartz, SiO_2 with 1- V_O , and with 2- V_O are shown in Fig. 4.21. To benchmark the computational method, preliminary calculation on the α -quartz has been performed. Our predicted quartz structure exhibits Si-O bond lengths of 1.625 and 1.631 Å, respectively. The bond lengths are 1% longer than the experimental values [35] and agree with the previous calculations [36, 37] within 0.1%. Our bond angle is 2° smaller than the previously reported values [35], which results from the slight expansion in the bond lengths compared to the experiment. The asymmetry between the short and long bonds, 0.4%, is close to the experimental value of 0.5%. [35]

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In the V_O center, an oxygen atom is removed and the silicon dangling bonds combine to form a direct silicon-silicon bond. Figure 4.21(b) and 4.21(c) show the relaxed configurations of 1- V_O and 2- V_O centers in α -quartz. The formation of a V_O center results in a short $d_{Si-Si}=2.44$ Å for 1- V_O and 2.46 Å for 2- V_O , due to the formation of a two-center two-electron bond. The features of the local configurations are in good agreement with the previous first-principles calculations [38], providing support for the accuracy of the current model. It is interesting that the generation of the second V_O does not affect the local configuration of the first V_O , and only increases the Si-Si bond length slightly.

(a)

Figure 4.22. (a) Total DOS, (b) Si partial-DOS and (c) O partial-DOS for undefected α -quartz, 1- V_O α -quartz and 2- V_O α -quartz, respectively. The highest occupied states are aligned at 0 eV.

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The calculated density of states of α -quartz, with 1- V_O and 2- V_O are shown in Fig. 4.22 (a-c). Here the highest occupied states (valence band maximum) are aligned at 0 eV. In the total DOS of α -quartz, one sees four distinct bands, the oxygen S states (-20 to -16 eV), the strong-bonding states (-9 to -4 eV), the lone-pair-like band (-3 to 0 eV), and the weak-antibonding conduction states (6 eV and above). It should be noted that the calculated band gap of α -quartz is 5.8 eV, which is substantially lower than the true band gap of about 9 eV. This magnitude of underestimation is typical of the Kohn-Sham equations. As shown in the partial-DOS (PDOS) plot in Figs. 4.22(b) & (c), at the V_O centers, from the combination of the sp^3 hybrids on each Si, a doubly occupied σ bonding and an empty σ^* antibonding state appear in the band gap. The effect of V_O is remarkable in the conduction band, while almost negligible in the valence band. With the V_O concentration increases, the intensity of the defect state at the conduction band edge increases obviously, while the peak position changes slightly.

Figure 4.23. Plot of core loss spectra and u-DOS (calculated from the atomic structures in Fig. 4.21) for (a) Si $L_{2,3}$ edge & $s + d$ DOS and (b) O K edge & p DOS, for defective and non-defective oxide. The DOS peaks are shifted and aligned at the respective edge onsets for comparison purpose.

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Figure 4.23 shows the comparison between normalized experimental spectra and DOS calculations for defective and non-defective oxide. Since the transitions close to the edge onset (small scattering vectors) are governed by the dipole selection rules, the change in the orbital angular momentum quantum number must be ± 1 . Therefore, Si $L_{2,3}$ edge (initial p states) probes the unoccupied s and d states and O K edge (initial s states) probes the unoccupied p states. As shown in Fig. 4.23(a), the oxygen vacancy lowers the $s + d$ DOS at around 108eV and creates more states at around 105eV. The DOS redistribution matches well with the experimental results of Si^{4+} peak for the BD oxide. For the O K edge and p DOS shown in Fig. 4.23(b), similar results are observed. The generation of oxygen vacancies shifts the O-K edge energy states from 537eV to 533-534eV and the same change is shown in the theoretical calculation. This simple comparison between the theoretical prediction and experimental fact implies that the oxygen vacancy is the dominating structural defect in defective oxide after a BD.

4.5 Summary

In summary, the site-specific chemical analysis using STEM-EELS was performed on dielectric breakdown percolation path. The atomistic changes of the chemical bonding in a nano-scale breakdown path are extensive and irreversible. Oxygen atoms in dielectric SiO_2 are washed-out with sub-stoichiometric silicon oxide (SiO_x with $x < 2$) formation, and local energy gap lowering with intermediate bonding state of silicon atoms (Si^{1+} , Si^{2+} , and Si^{3+}) in the percolation leakage path. Oxygen deficiency within the breakdown path is estimated to be as high as 50-60%. The oxygen deficiency is the key signature for the structural change at molecular level in the breakdown path. Chemical bond breakage and the local joule heating due to large current surging

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through the percolation path are believed to be the main driving forces leading to the oxygen dissociation and washed-out. Since different among of the oxygen atoms at the nearest neighbors results in different local energy gaps, it is believed that the local energy gap at the breakdown path could have collapsed after the removal of oxygen atoms and there is a rearrangement of local atomic structures. The electronic structures of BD oxide are similar to the oxygen deficient suboxide as confirmed by the theoretical calculation and modeling. The presence of a nanoscopic conduction path is therefore possible in the highly oxygen deficient breakdown oxide.

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PHYSICAL ORIGIN OF DIGITAL TO ANALOG POST BREAKDOWN EVOLUTION

5.1 Introduction

Over the past 30 years, efforts have been made to understand the trap/defect generation [1-3], percolation path formation [4-6] and degradation [7-9] in amorphous SiO₂ in attempts to predict the occurrence of the time dependent dielectric breakdown accurately under device operating conditions. There are a few well accepted physical models [2, 10-11] which describe the importance of different trap/defect generation processes as well as their impacts to the dielectric breakdown. It is commonly agreed that the defects generated during pre- and post-BD stress are responsible for various leakage current profiles observed in the accelerated tests. Among the proposed defects, the oxygen vacancy and its related species serve as strong candidates responsible for the oxide wearing-out process, from stress induced leakage current [1, 2] to progressive breakdown (or soft-BD) [8]. It is therefore important to know the distribution of oxygen deficiency in a BD path and understand its role in the oxide degradation process. Recently, the random telegraph noise (RTN) observed from gate leakage current I_g has attracted a lot of attention in the field of metal oxide semiconductor reliability [12-15]. The randomly fluctuating current profile has been found for both conventional SiON and high- κ dielectrics

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during accelerated tests. It is believed that this phenomenon is related to the trapping/detrapping of carriers [12] as well as the ON/OFF state of the percolation path due to defect transformations [9]. Lo *et al.* [15] has reported a critical voltage V_{crit} in ultrathin SiON, above which the visibility of the digital noise in the early stage of post breakdown is suppressed. Two distinct I_g profiles, namely digital-BD and analog-BD, are identified where a low current level with no net increase and a high current level are demarcated by V_{crit} . The discovery of V_{crit} is important. The post-BD reliability margin can be effectively enlarged if the digital-BD is maintained (i.e., $V_g < V_{\text{crit}}$). In this chapter, we study the distribution of oxygen deficiency in a percolation path and investigate the defect formation in digital- and analog-BD in order to reveal the physical origin of the digital-to-analog transition.

5.2 Post Breakdown Digital to Analog Transition and Critical Gate Voltage

The progressive breakdown is mainly constituted by the digital and the analog breakdown, which are a low and a high conduction state, respectively [16-18]. Based on our results, the digital breakdown will take place before the occurrence of the analog breakdown. Since the digital breakdown is dominant in the early stage of the progressive breakdown for which an nMOSFET is still functioning; thus, the study of the digital breakdown is particularly important.

Figure 5.1 shows a typical example for the evolution of I_g for a breakdown n-MOSFET ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.6 \text{ \mu m}^2$) stressed using a three-cycle multiple-stage CVS in inversion mode at the room temperature [9]. The TDDB of the n-MOSFET was carried out with $V_{\text{gstress}} = 4.1 \text{ V}$ and $I_{\text{gl}} = 1 \text{ \mu A}$. The stressing conditions of the 1st-, the 2nd- and the 3rd-cycle

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multiple-stage CVS were $V_{init}(1) = V_{init}(2) = V_{init}(3) = 1.2$ V, $\Delta V(1) = \Delta V(2) = \Delta V(3) = 0.2$ V, $t_{stress}(1) = t_{stress}(2) = t_{stress}(3) = 500$ s, $V_{final}(1) = V_{final}(2) = 3.4$ V and $V_{final}(3) = 3.6$ V. Figs. 5.2(a) and 5.2(b) show an enlarged view of the 1st- and the 3rd-cycle multiple-stage CVS at $V_{gstress} = 1.6$, 1.8, 2 and 2.2 V for the n-MOSFET in Fig. 5.1, respectively. It can be observed that the behaviors of I_g at a specific $V_{gstress}$ in the 1st-cycle multiple-stage CVS are different from those in the 2nd- and the 3rd-cycle multiple-stage CVS. The 1st-cycle multiple-stage CVS corresponds to the digital breakdown, while the 2nd- and the 3rd-cycle multiple-stage CVS correspond to the analog breakdown [9, 15].

The digital and the analog breakdown are demarcated with each other by the V_{final} of the 1st-cycle multiple-stage CVS. This voltage is a critical gate voltage specifically denoted as V_{crit} (i.e., $V_{crit} = V_{final}(1)$). The effects of V_{crit} on the progressive breakdown will be discussed in details. Some of the specific properties associated with the digital and the analog breakdown are described as follows:

- Digital Breakdown:

The 1st-cycle multiple-stage CVS corresponds to the early stage of the progressive breakdown, in which the progressive breakdown was initially arrested at a low I_{gl} of 1 μ A. As shown in Figs. 5.1 and 5.2(a), I_g exhibited an irreproducible, random step-like profile, analogous to the results reported in Refs. [17, 18]. This region of the progressive breakdown is commonly referred to as digital breakdown [9].

Figure 5.1. Evolution of I_g for a breakdown n-MOSFET ($T_{ox} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.6 \text{ \mu m}^2$) stressed using a three-cycle multiple-stage CVS in inversion mode at the room temperature. The TDDDB of the n-MOSFET was carried out with $V_{gstress} = 4.1 \text{ V}$ and $I_{gl} = 1 \text{ \mu A}$. The three-cycle multiple-stage CVS was performed with $V_{init}(1) = V_{init}(2) = V_{init}(3) = 1.2 \text{ V}$, $\Delta V(1) = \Delta V(2) = \Delta V(3) = 0.2 \text{ V}$, $t_{stress}(1) = t_{stress}(2) = t_{stress}(3) = 500 \text{ s}$, $V_{final}(1) = V_{final}(2) = 3.4 \text{ V}$ and $V_{final}(3) = 3.6 \text{ V}$. Note that $V_{final}(1) = V_{crit}$. [9]

The digital fluctuation of I_g can be identified by obvious, drastic “switching” effects. As shown in Fig. 5.2(a), I_g could instantaneously and randomly increase (or decrease) to a high (or low) level that could be more than one order of magnitude difference. For instance, I_g at $V_{gstress} = 2 \text{ V}$ could suddenly increase from $\sim 8 \times 10^{-9} \text{ A}$ to $\sim 1 \times 10^{-7} \text{ A}$ (i.e., {2} in Fig. 5.2(a)), while I_g at $V_{gstress} = 2.2 \text{ V}$ could suddenly decrease from $\sim 1.5 \times 10^{-8} \text{ A}$ to $\sim 1 \times 10^{-9} \text{ A}$ (i.e., {3} in Fig. 5.2(a)). Furthermore, it can be observed that I_g randomly fluctuated or oscillated at two specific values for a given $V_{gstress}$ in most of the times. For instance, it can be seen that at $V_{gstress} = 1.6 \text{ V}$,

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the random oscillation in I_g took place between $\sim 2.8 \times 10^{-8}$ A and $\sim 4 \times 10^{-8}$ A (i.e., {1} in Fig. 5.2(a)).

- Analog Breakdown:

In the 2nd- and the 3rd-cycle multiple-stage CVS, as shown in Figs. 5.1 and 5.2(b), I_g is reproducible and steadily increased with increasing $V_{gstress}$, in which no apparent digital fluctuation of I_g can be observed. This region of the progressive breakdown is named as the analog breakdown. In addition, the relationship between I_g and V_g can be modeled using power law, that is

$$I_g = K \times V_g^\alpha \quad (5.1)$$

where K and α are experimentally fitting parameters [9].

Figure 5.2. Enlarged view of (a) the 1st- and (b) the 3rd-cycle multiple-stage CVS at $V_{gstress} = 1.6, 1.8, 2$ and 2.2 V for the n-MOSFET in Fig. 5.1. As shown in (a), the digital fluctuation of I_g can be characterized as: {1} the random oscillation at two specific values, {2} a sudden huge increase and {3} a sudden huge decrease. [9]

The V_{crit} versus T_{ox} relationship is shown in Fig. 5.3 [9, 15-16]. V_{op} with various T_{ox} , which are obtained from ITRS and some of the published data, are also plotted. The red and the black color

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refer to the n-MOSFETs fabricated by Manufacturers A and B, respectively. As mentioned above, if V_{crit} is much larger than V_{op} , the transition of the digital breakdown into the analog breakdown can hardly occur during the normal device operations. This means that the post-breakdown reliability margin can largely be extended [16]. It can be noticed from Fig. 5.3 that for T_{ox} larger than 1.6 nm, V_{crit} steadily decreases with decreasing T_{ox} . This leads to a major post-breakdown reliability concern. It is initially predicted that at a lower T_{ox} where V_{crit} is equal to V_{op} , the digital breakdown will vanish upon the occurrence of a dielectric breakdown event, and I_g will spontaneously evolve into a stable high leakage state.

Figure 5.3. V_{crit} versus T_{ox} relationship. A saturation of V_{crit} at 2-2.4 V implies that the extra advantage provided by the digital breakdown in extending the post-breakdown reliability margin still exists at T_{ox} below 1.6 nm. The red and the black color refer to the n-MOSFETs fabricated by Manufacturers A and B, respectively. [16]

If V_{op} is larger than V_{crit} , the progressive breakdown could totally vanish, and a device may immediately experience a catastrophic breakdown once a dielectric breakdown event is triggered to occur. However, as shown in Fig. 5.3, for T_{ox} smaller than 1.6 nm, a saturation of V_{crit} at 2-2.4

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V can be observed. The difference between V_{op} and V_{crit} remains constant at 0.9-1.4 V. This implies that the shrinkage of the progressive breakdown due to the absence of the digital breakdown will not occur when T_{ox} is continuously scaled below 1.6 nm.

5.3 Physical Origin of Digital to Analog Transition

The digital-BD in the early stage of the progressive breakdown helps to prolong the lifetime of the device, if the operating voltage is kept below V_{crit} . It is therefore important to find out the physical origin of this digital to analog transition. By knowing the chemical structure of the percolation path, creative means could be proposed to prevent the transition to analog-BD from happening.

5.3.1 Radial Distribution of Defects in Percolation Path

Since the oxygen vacancy and its related species are the physical defects responsible in the oxide wearing-out process, it is important to know the distribution of the oxygen deficiency in a BD path first. The characterization techniques using TEM/EELS as introduced in Chapter 4 are further developed here to access the chemical information of the percolation path. Figure 5.4 shows the electrical results of one nMOSFET sample ($W \times L = 0.15 \times 0.5 \mu\text{m}^2$) stressed using a 2-step CVS. The final failure current was capped at $I_{gl} = 2 \mu\text{A}$. Pre- and post-breakdown I_g - V_g characteristics of the transistor are shown in Fig. 5.4(b).

Figure 5.4. (a) Time evolution of the gate leakage current I_g for a poly-Si/SiON nMOSFET sample ($T_{\text{ox}} = 2.2$ nm & $W \times L = 0.15 \times 0.5$ μm^2) failed under a 2-step CVS. The final failure current limit I_{gl} is 2 μA . (b) Pre- and post-BD I_g - V_g characteristics.

Figure 5.5 shows the corresponding high angle annular dark field micrograph of the gate oxide at its BD location [19], which is isolated using (FIB) milling. The dielectric layer is a 22 Å nitrated amorphous SiO_2 (N% $\sim 3\%$). A dielectric breakdown induced epitaxy [20] nano-marker is identified at the BD location. Electron energy loss spectra, both Si $L_{2,3}$ edge and O K edge, were acquired at Positions 1 to 6 in the oxide layer to obtain the information of the breakdown oxide. To access the local properties from a 22-Å gate oxide layer, a fine probe size as well as a good energy resolution is needed. In this experiment, the STEM probe size was set to be around 3 Å in diameter and the EELS energy resolution was 0.7 eV.

Figure 5.5. HAADF micrograph showing the gate stack of a typical metal oxide semiconductor (MOS) transistor after dielectric breakdown (compliance current limit $I_{gl} = 2 \mu\text{A}$). A DBIE nano-marker is identified. EEL spectra at Positions 1 to 6 (indicated in the oxide layer) were acquired at the breakdown spot, respectively. The TEM sample was prepared using FIB with low energy (2 kV) clean and *in-situ* lift-off. The STEM/EELS experiments were performed on an FEI Titan microscope operated at 80 kV. The STEM probe size was optimized to be around 3 Å in diameter and the EELS energy resolution was 0.7 eV (0.05 eV/channel).

The plots of Si $L_{2,3}$ edge spectra are shown in Fig. 5.6, and only spectra at Positions 1, 2 and 3 (half of the symmetrical DBIE) are shown for discussion. The different Si oxidation states are labeled in the figure, respectively. The Si^{4+} signals (onsets at 105 eV) are originated from the bulk SiO_2 bonding in the central region of the oxide layer. It reveals the electronic structures at the bottom of the oxide conduction band [21]. The changes in the peak shape and intensity for defective oxide at Positions 2 and 3 (outer and inner shell of percolation path) are similar as observed in Chapter 4. Since the weaker signals below 105 eV are delocalized counts from the adjacent suboxide region [21], we could then separate the contributions and use the flat portion of the peak below 105 eV as the reference for the Si^{4+} peak onsets. The inserted graph in Fig. 5.6 shows the zoomed-in plot of the spectra from 103 eV to 106.5 eV, which highlights the onset

part of the Si^{4+} signal. As illustrated in the plot, the intersections of the fitted onset slopes shift from 104.76 eV (Position 1) to 104.62 eV (Position 2), 104.55 eV (Position 3 upper slope between 109.5 eV and 111 eV) and 103.98 eV (Position 3 lower slope between 107 eV and 109 eV). This suggests that the local oxide conduction band minimum is lowered for 0.14 eV to 0.78 eV, as moving from Position 1 to 3.

Figure 5.6. Plot of Si $L_{2,3}$ edge spectra collected at Positions 1, 2 and 3. The different Si oxidation states are labeled. The inserted graph shows the zoomed-in plot from 103-106.5 eV, which are the onset portion of Si^{4+} signals. The intersections of the fitted onset slopes shift from 104.76 eV (Position 1) to 104.62 eV (Position 2), 104.55 eV (Position 3 upper slope) and 103.98 eV (Position 3 lower slope). The local oxide conduction band minimum as shown from the Si^{4+} signal are lowered for 0.14 eV to 0.78 eV as moving from Position 1 to 3.

The as-measured O-K edge intensities between 532 eV and 552 eV of the 6 positions are shown in Fig. 5.7 in box-plot inclusive of signal variations from background subtraction and thickness

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non-uniformity. The parabolic profile of the oxygen defect distribution shows clearly that the defects composed of the percolation path are radially distributed. The deficiency of oxygen is higher at/near to the center of the percolation path. The diameter of the percolation path (defective oxide area laterally) is estimated to be 30 nm for the post-BD leakage current of 2 μA , corresponding to a very soft breakdown case in our study. Since the O-K edge intensities are originated from the entire oxide volume in the thickness direction of the TEM sample, it is therefore essential to fine-tune the calculation to determine the exact contribution from the defective oxide and extract the signals only from the percolation path. Generally, the inner shell signal depends proportionally on 1) the core edge ionization cross section σ , 2) the number of atoms per area and 3) the number of incident electrons (which can be measured using low loss spectrum including the unscattered and inelastically scattered electrons) [22]. In this experiment, we focus on only the O-K edge signals at different locations near the breakdown spot with exactly the same experimental conditions such as the collection semiangle β and acquisition time. The variables in 1) and 3) could be neglected here since we compare the relative change in oxygen intensities with respect to the same reference spectrum (assumed as SiO_2). Based on the low-loss spectra acquired at the area of interest, the local sample thicknesses are relatively uniform (± 1 nm), which is also a characteristic of a FIB sample [23]. It is therefore believed that the oxygen intensity difference in Fig. 5.7 are originated from the defective oxide in the percolation path which give rise to the different number of oxygen atoms per area in 2). Like the usual EELS composition quantification, we could then be able to decouple the signal contributions from the defective oxide in the percolation path.

Figure 5.7. Box-plot of the as-measured O K edge intensities (532-552 eV) at all the 6 positions near the breakdown spot. The diameter of the percolation path (defective oxide area laterally) is estimated to be 30 nm.

Figure 5.8 illustrates the top view schematic diagram of the oxide area with a breakdown path embedded in the TEM sample. Based on the separation of probing positions in Fig. 5.5, a 3-shell percolation path model is proposed for the thickness correction. The defective oxide in each shell is denoted as SiO_{x1} , SiO_{x2} and SiO_{x3} , respectively. The as-measured O-K edge intensities at Positions 3, 5 and 6 are used for the calculation. The TEM sample thickness T from the low loss measurement was found to be around 80 nm and the percolation path diameter D is 30 nm.

Figure 5.8. Top view schematic diagram of the oxide area with a breakdown path embedded in a TEM sample. A 3-shell percolation model is proposed for the thickness correction. The O K edge intensities at Position 3, 5 and 6 are used for the calculation. The different dimensions in the percolation path are labeled as d and the TEM sample thickness is T .

The electron probe at Position 6 transmits through the sample with d_1 in shell-1 of the percolation path and $(T - d_1)$ in the non-defective oxide. The as-measured intensity at Position 6 is therefore:

$$\int_0^T O_{\text{Position 6}} dt = \int_0^{d_1} O_{x1} dt + \int_0^{T-d_1} O_2 dt \quad (5.2)$$

where O_{x1} and O_2 are the number of oxygen atoms at the defective oxide (shell-1) and non-defective oxide, respectively.

We can also formulate the intensities at Positions 3 and 5 as follows:

$$\int_0^T O_{\text{Position 5}} dt = \int_0^{d_{21}} O_{x2} dt + \int_0^{d_2-d_{21}} O_{x1} dt + \int_0^{T-d_2} O_2 dt \quad (5.3)$$

$$\int_0^T O_{\text{Position 3}} dt = \int_0^{d_{31}} O_{x3} dt + \int_0^{d_{11}-d_{31}} O_{x2} dt + \int_0^{d_3-d_{11}} O_{x1} dt + \int_0^{T-d_3} O_2 dt \quad (5.4)$$

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If we use the oxygen signal measured outside the percolation path, i.e. Position 1, as the reference signal for SiO_2 , we get:

$$\int_0^T O_{\text{Position 1}} dt = \int_0^T O_2 dt \equiv 2.0 \quad (5.5)$$

By knowing the separation of the probing position to the origin of the percolation path, we can calculate every distance d labeled in each shell according to the geometries. From Eqns. (5.2) & (5.5), we can obtain the x_1 value in shell-1. Using Eqns. (5.3), (5.4) & x_1 value, we can obtain the value for x_2 in shell-2. The x_3 value in shell-3 is therefore obtained from Eqns. (5.4), (5.5), x_1 & x_2 . The corrected oxygen deficiency in the percolation path is shown in Fig. 5.9. As probing from the outer shell to the inner shell of the percolation path, the deficiency of oxygen changes from 10% to 30% and reaches a maximum 65% in the center of the percolation path.

Figure 5.9. Box-plot of the corrected oxygen deficiency in the percolation path shown in Fig. 5.5 using the 3-shell model. The O-deficiency in the center shell is as high as 65% ($\text{SiO}_{0.7}$) as calculated from the as-measured oxygen intensities. Source side is marked by arrow.

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The radial distribution of the oxygen vacancies suggests that the defect generation as a result of electrical stress is non-uniform. The inner shell of the percolation path (somewhere near Position 3) was likely to be the location where the percolation path initially formed. Since the local current density is enormous, it is believed that the trap/defect generation rate in the vicinity of the percolation path is much faster than the surrounding oxide area. The percolation path therefore dilates radially as more defects are generated at the BD site. Meanwhile, it is worth noting that this radially distribution profile is not symmetrical. One of the possible reasons for the asymmetrical pattern could be the location of the percolation path along the channel length L . For this transistor, the location of the BD spot is located at $0.36L$ from the Source terminal (i.e., at 180 nm from the Source terminal). The current leaked through the percolation path goes to the Source and Drain terminals via the inversion channel with different magnitudes (determined by the respective channel resistances) [24]. In this case, it is expected to have a faster growth rate towards the Source terminal since there is more current flowing to the Source side. Eventually, the asymmetrical growth of the percolation path creates a positive feedback to the leakage current and Si-O bond breakage. It further degrades the oxide and leads to a hard breakdown when a direct short between the gate and S/D is formed. The location of the percolation path is therefore significant in the post-breakdown reliability assessment [25]. Comparing the results in Fig. 5.6 and Fig. 5.9, we could also correlate the oxygen deficiency with the local conduction band lowering. The onset of Si^{4+} signal shifts by 0.14 eV at Position 2, which corresponds to a defective oxide $\text{SiO}_{1.76}$. At Position 3, the edge onset drop is 0.78 eV for a defective oxide $\text{SiO}_{0.7}$. The actual lowering SiO_2 conduction band edge could be different from the value obtained from fitting the slopes of the Si^{4+} edge onset, especially with signal delocalization [26, 27]. However, this semi-quantitative correlation still provides us a clear evidence of the material property

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change in the percolation path. The energy gap of the oxide shrinks as the oxygen atoms are washed-out.

5.3.2 Si Nano-cluster in Center of Percolation Path

Figure 5.10. HAADF micrographs of four poly-Si/SiON nMOSFET samples ($T_{\text{ox}} = 2.2$ nm) with BD hardness $I_{\text{gl}} =$ (a) 2 μA , (b) 5 μA , (c) 35 μA and (d) 40 μA at their respective BD locations. The sample details are shown in Table 5.1.

After knowing the distribution of oxygen deficiency in the percolation path, we are ready to further investigate the physical origin of the digital to analog transition observed in Fig. 5.1. In order to find out the physical difference(s) of the BD path in digital-BD and analog-BD, nMOSFET samples were stressed to different hardness (i.e., the I_{gl}) and studied using

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TEM/EELS. In Fig. 5.10, the HAADF results of the four samples with $I_{gl} = 2, 5, 35$ and $40 \mu\text{A}$ are shown at their respective BD locations. The detailed sample information is listed in Table 5.1.

Table 5.1. The nMOSFET sample details used for STEM/EELS experiments. The L used in the BD location measurements [19] refers to the effective channel length. The percolation resistance is measured using PRM method [28] at $V_g = 1.5\text{V}$.

Sample number	Sample 1	Sample 2	Sample 3	Sample 4
Dimension (μm^2)	$W \times L = 0.15 \times 0.50$	$W \times L = 0.15 \times 0.50$	$W \times L = 0.15 \times 1.0$	$W \times L = 0.15 \times 0.20$
BD location (to Source terminal in L)	$0.360 L$	$0.575 L$	$0.137 L$	$0.843 L$
BD hardness I_{gl} (μA)	2.0	5.0	35.0	40.0
Percolation path resistance R_{perc} ($\times 10^6 \Omega$)	~ 30	~ 20	~ 3	$\sim 1\text{-}2$
Leakage current profile	Digital-BD	Digital-BD	Analog-BD	Analog-BD

Since the stress conditions have direct effect on the defect formation, we shall discuss this issue in more details. Figure 5.11 shows the gate leakage current profile of a sample ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \mu\text{m}^2$) stressed using a one-cycle multiple-stage CVS. The initial breakdown was created with $V_{\text{gstress}} = 4.1 \text{ V}$ and $I_{gl} = 1.0 \mu\text{A}$. The one-cycle multiple-stage CVS was performed with a initial stress voltage $V_{\text{init}} = 2.6 \text{ V}$, voltage increment $\Delta V = 0.1 \text{ V}$, time interval for each stage $t_{\text{stress}} = 500 \text{ s}$ and final stress voltage $V_{\text{final}} = 3.4 \text{ V} \geq V_{\text{crit}}$. The digital- and analog-BD I_g profiles are clearly displayed in this figure. In the digital-BD region, the gate leakage current could hardly evolve beyond $1 \mu\text{A}$ as the stress voltage varying from 2.6 V to 3.2 V . This low current level in the digital-BD region can be applied to samples with different sizes (i.e., oxide areas) since the post-BD degradation is a local phenomenon. However, the gate current jumps to

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a high leakage state (e.g. $> 20 \mu\text{A}$) in the analog-BD region once V_{crit} is reached. Knowing the current level difference for digital- and analog-BD, we can therefore stress the sample to the desired breakdown hardness by controlling I_{gl} in the 2-stage CVS. Considering also the EELS detection (harder BD gives better signal-to-noise ratio), the following I_{gl} values were chosen to prepare the required BD samples: 1) $2 \mu\text{A}$ (digital-BD), 2) $5 \mu\text{A}$ (digital-analog transition), 3) $35 \mu\text{A}$ (end of digital-analog transition) and 4) $40 \mu\text{A}$ (analog-BD).

Figure 5.11. The electrical stress of n-MOSFETs ($T_{\text{ox}} = 22 \text{ \AA}$ and $L \times W = 1 \times 0.3 \mu\text{m}^2$) stressed using a one-cycle multiple-stage CVS in inversion mode at the room temperature. The initial breakdown was created with $V_{\text{gstress}} = 4.1 \text{ V}$ and $I_{\text{gl}} = 1.0 \mu\text{A}$. The one-cycle multiple-stage CVS was performed with $V_{\text{init}} = 2.6 \text{ V}$, $\Delta V = 0.1 \text{ V}$, $t_{\text{stress}} = 500 \text{ s}$ and $V_{\text{final}} = 3.4 \text{ V} \geq V_{\text{crit}}$. The digital-BD and analog-BD regions are marked respectively. In the digital-BD region, I_{g} fluctuates at a relatively low leakage level (i.e., $1.0 \mu\text{A}$ for this sample). The gate current enters into a high leakage level (e.g. $> 20 \mu\text{A}$) in the analog-BD region once V_{crit} is reached.

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The defect distribution in a percolation path is discussed in Section 5.3 and we adopt the same analysis procedure here by calculating the oxygen deficiency in the defective oxide with suitable corrections. The corrected oxygen deficiency line profiles (A-A' cross section) are displayed in Fig. 5.12 for the 4 samples shown in Fig. 5.10. The A-A' cross section is located on one plane of a cylinder-shaped percolation path shown in the inserted schematic diagram. As indicated in the figure, the lateral sizes of the defective oxide based on oxygen deficiency are around 30 nm (2 μ A) and 35 nm (5 μ A) for digital-BD samples. It increases to 60 nm and 55 nm for 35 μ A and 40 μ A samples, respectively. Please note that the size measurement is dependent on the location of the BD. In case of the 40 μ A sample ($W \times L = 0.15 \times 0.20 \mu\text{m}^2$), the BD location is near the Drain terminal (i.e., $s = 0.843 L$ from the Source terminal). The actual distance to the Drain terminal is 31.4 nm. Since the EELS signal is affected by the geometries of the sample, the size measurement is limited for such near-terminal cases. However, we can still estimate the BD size based on one side measurement and mirror image the other side. The distribution of O-deficiency also exhibits apparent differences. The outer shells of the breakdown path, for all 4 samples, show similar and gentle oxygen deficiencies (e.g., less than 50%) while for the inner core, severe oxygen depletion (up to 98%) is observed for the analog-BD samples. The total amount of oxygen deficiency in the percolation path can be evaluated using the defect distribution profiles. Assuming that the distribution is identical in the longitudinal and lateral directions (i.e., symmetrical radial distribution) and the same distribution is applied throughout the percolation path in the T_{ox} direction, the total O-deficiency can be calculated by integrating the defects in the volume of the cylinder for each of the 4 samples and the results are discussed in Fig. 5.13.

Figure 5.12. The corrected oxygen deficiency A-A' line profile in the percolation path of the 4 BD samples shown in Fig. 5.10, respectively. The inserted diagram shows the A-A' cross-section of a percolation in a broken down oxide. Both the oxygen deficiency and the size of the percolation path change as a function of the breakdown hardness.

Figure 5.13(a) shows the change of the percolation resistance R_{perc} and the maximum oxygen deficiency in the percolation path as a function of the breakdown hardness. Figure 5.13(b) shows the total O-deficiency calculated using the defect distribution profiles for the 4 samples. The total amount of oxygen depletion in the defective oxide increases continuously as the BD is getting harder (i.e., the bigger defective oxide volume). However, the maximum oxygen deficiency at the center of the percolation path experiences different degradation rates and increases to almost 100% once the sample enters into the analog-BD region. Meanwhile, the percolation resistance R_{perc} decreases by one order of magnitude from the digital-BD to the analog-BD and stabilizes when the parasitic resistance R_{para} becomes comparable to R_{perc} [28].

(a)

(b)

Figure 5.13. (a) Plot of the percolation resistance R_{perc} and the maximum oxygen deficiency in the percolation path as a function of the breakdown hardness. (b) Total O-deficiency for the 4 BD samples. The value of R_{perc} decreases by one order of magnitude from the digital-BD to analog-BD samples while the oxygen deficiency increases to almost 100% at the center of the percolation path.

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This observation implies that the electrical conduction in a percolation path is effectively determined by the minimum oxygen content (maximum O-deficiency) portion of the defective oxide at the inner core. For the defective oxide containing sufficient amount of oxygen, the random switching of current levels are feasible due to the defect transformations [9]. This digital current is observed in the digital-BD region and also believed to be present in the outer shells of the percolation path of the analog-BD samples. However, in the analog-BD region, not only the defective area with oxygen deficiency of more than 50% becomes much larger, but also the maximum oxygen deficiency in the inner shell of the percolation path could be as high as 98%.

Figure 5.14. Box plot of the oxygen deficiency (as SiO_x) at the inner core of the percolation path for different current limited BDs. The variations of local sample thickness ($\pm 3\%$) are included in the signal corrections.

Hence a highly conductive path possibly a pure Si nano-cluster is formed at the center of the percolation path. The formation of the nanosize Si-path sustains a large analog current and suppresses the visibility of the digital noise arising from outer shell of the percolation path. Moreover, the presence of the Si-path agrees well with the Schottky-like barrier measured at the

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interface between the percolation path and *p*-type Si substrate in the later stage of the progressive BD [29].

Figure 5.15. (a) Time evolution of the gate leakage current I_g for a poly-Si/SiON nMOSFET sample ($T_{ox} = 2.2$ nm & $W \times L = 0.15 \times 0.5 \mu m^2$) failed under a 2-step CVS. The final failure current limit I_{gl} was $100 \mu A$. (b) TEM micrograph of the BD location. Nano-size Si cluster was found. (c) HRTEM of the Si nano-cluster of (b) showing crystalline structures.

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The oxygen deficiency in the center of the percolation path is further confirmed by including $\pm 3\%$ thickness variation into the signal correction process. Figure 5.14 shows the box plot of the x value (where x denotes the oxygen deficiency SiO_x) at the inner core of the percolation path for BDs with I_{gl} ranging from $2\ \mu\text{A}$ to $200\ \mu\text{A}$. It is clearly shown that the oxygen is fully depleted at the inner core once the analog-BD is reached. The Si-clustering in the BD path is experimentally observed for some samples too. Figure 5.15 shows an example of a device failed at $I_{gl} = 100\ \mu\text{A}$ (i.e., analog-BD). At the BD location, nano size Si-cluster (crystalline structure) is clearly seen in Figs. 5.15 (b) and (c).

Another example of the Si nano-cluster is observed in an $I_{gl} = 40\ \mu\text{A}$ BD sample as shown in Fig. 5.16. A Si nano-cluster was found in the low-angle annular dark field (LAADF) STEM micrograph at the BD location.

Figure 5.16. STEM micrograph using low-angle annular dark field (LAADF) detector of a poly-Si/SiON nMOSFET sample ($T_{\text{ox}} = 2.2\ \text{nm}$ & $W \times L = 0.15 \times 0.2\ \mu\text{m}^2$) failed at $I_{gl} = 40\ \mu\text{A}$. A nano-size Si cluster was found at its BD location as indicated by the arrow.

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The microscopic structure of the percolation path in the post-BD wear-out phase is controlled by oxygen deficiencies. Due to the detection limit, the pre-BD oxide defects could not be studied directly using STEM/EELS. However, electron spin resonance (ESR) measurement [30] has shown that the E' center (i.e., one of the oxygen vacancy defect types) plays dominating roles in the stress induced leakage current before percolation path formation. The experimental evidence obtained from the pre- and post-BD phase suggests that the oxygen vacancy related defects are the dominating defects throughout the oxide degradation. Since the defect generation process in pre- and post-BD creates more oxygen vacancies in the oxide, similar voltage and temperature acceleration parameters (i.e., governed by defect generation mechanism) are expected [31-33]. On the other hand, the acceleration factors such as the voltage acceleration factor and power law exponent are not entirely identical for first-BD and post-BD [18, 31]. As reported by Wu *et al.* [31], the values of the acceleration factor for initial post-BD, when the percolation path is just formed, are quite close or slightly smaller than first-BD. But they differ from each other as the percolation path degrades further and eventually stabilize at the failure current level of around 40 μA (which corresponds to the analog-BD). The different value of the acceleration factor is believed to be caused by how different the oxygen atoms are removed from the SiO_2 network during the pre-BD stress and from the localized percolation path during the post-BD stress. The formation of oxygen vacancy in the pre-BD phase has been investigated by several authors [1, 3, 11, 34-35]. For the post-BD, the details of the defect generation still remain unclear due to the complex atomic structure of the percolation path. Nevertheless, a lower activation energy of the post-BD ($\sim 304 \text{ meV}$) as compared with the first-BD ($\sim 575 \text{ meV}$) [33] is required to generate the defect in the percolated oxide with the presence of existing defects. In general, the local degradation in the percolation path is initially similar to the pre-BD stress and becomes easier

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and faster as the percolation path wears out (i.e., digital-BD). It finally stabilizes with the Si-path formation in the center of the percolation path and enters the analog-BD when the effects of external resistance and local bandgap drop must be considered.

In general, it is believed that V_{crit} serves as a factor in rapidly wearing out the percolation path such that a sufficiently huge amount of I_g can be generated. For $V_{gstress}$ smaller than V_{crit} , the percolation path could not be easily worn out. Since I_g is small, the digital breakdown could hardly evolve into the analog breakdown. For $V_{gstress}$ larger than V_{crit} , the percolation path will easily be worn out, allowing more I_g to flow through the percolation path. However, if I_g is limited, the local temperature in the vicinity of the percolation path may be insufficient to transform the percolation path into a silicon-like nano-structure. As a result, the transition of the digital breakdown into the analog breakdown will not occur [36].

Based on the understanding of the physical structure of the percolation path, it is believed that I_g is constituted by two components, which are $I_g = I_{DIG} + I_{ANA}$, where I_{DIG} defines the “digitally” fluctuated I_g flowing through a percolation path. Upon the occurrence of a dielectric breakdown event, it is believed that the percolation path only involves a few effective electronic traps that are sufficient to allow the hopping of the electrons from the cathode to the anode, where some of the portions of the percolation path are still non-defective, as shown in Fig. 5.17(a) [36]. I_{ANA} defines the relatively stable I_g flowing through a percolation path associated with the physical structure in Fig. 5.17(b) [36].

Figure 5.17. Physical structure of a percolation path in (a) digital and (b) analog breakdown. In the digital breakdown, the percolation path only involves a few electronic traps that are sufficient to allow the hopping of the electrons from the cathode to the anode, where some of the portions of the percolation path are still non-defective. On the contrary, in the analog breakdown, the percolation path is proposed to possess a silicon-like conductive channel at the core. [36]

The digital breakdown prevails in the early stage of the progressive breakdown. With the flow of a higher I_g through the percolation path, the wear out of the percolation path can be enhanced. The local temperature in the vicinity of the percolation path could be high when a huge amount of I_g flows through a very narrow conductive channel [24, 37]. As a result, this could transform some of the defective areas in the percolation path into a relatively stable silicon-like structure, which contribute to I_{ANA} . During the gradual growth of the percolation path from the physical structure in Fig 5.17(a) into 5.17(b), I_{ANA} starts to increase but I_{DIG} remains almost unchanged, and thus, I_g is the combined effects of I_{DIG} and I_{ANA} where $I_{DIG} \ll I_{ANA}$. When the percolation path possesses the physical structure in Fig. 5.17(b), I_{ANA} dominates over I_{DIG} , leading to a

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relatively stable I_g with a noisy profile. In this case, the analog breakdown prevails. If I_g is limited at a low I_{gl} , the local temperature in the vicinity of the percolation path may be insufficient to transform the defective areas in the percolation path into a relatively stable silicon-like nano-structure. This means that the transition of the digital breakdown into the analog breakdown is limited by I_{gl} . By setting I_{gl} to a higher value, some of the defective areas in the percolation path could be transformed into the silicon-like structure, causing I_{ANA} to increase and I_g will enter into the analog breakdown.

5.4 Summary

In summary, the lateral distribution of defects in a dielectric breakdown induced percolation path is determined experimentally. It is shown that the deficiency of oxygen spreads out radially from the center of the percolation path to its surrounding area. The Si/O composition changes from $\text{SiO}_{1.76}$ to $\text{SiO}_{0.7}$ while moving from the center towards outside of the percolation path, which corresponds to a lowering of the SiO_2 conduction band minimum from 0.14 eV to 0.78 eV. The percolation paths formed in digital- and analog-BD are studied and the physical origin of the digital telegraph noise is identified. The digital noise is originated from the defective oxide with low oxygen ratios (e.g., at the outer shells of percolation path). The digital fluctuation of I_g is less detectable as the current following through the core of the defective path increases. With the formation of a conductive Si-path, the percolation path transforms into a stable state (i.e., analog-BD) where the digital noise is so low that it is being overwhelmed by analog leakage current. Since the digital-BD significantly prolongs the reliability margin of post-BD oxide, efforts should be made to prevent the analog-BD from happening. In our study, the gate dielectric

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failure is usually a single breakdown event as a result of the small gate area (i.e., $W \times L < 0.075 \mu\text{m}^2$) used to facilitate the TEM analysis. However, multiple breakdowns in the gate dielectric are also observed for very limited number of samples. In appendix-II, an example of multiple breakdowns is shown. Physical analysis was performed to find out the failure mechanism responsible for such multiple-BD cases.

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CHAPTER SIX

CHARACTERIZATION OF MG/HK GATE STACKS AND FAILURE ANALYSIS

6.1 Introduction

The characterization methodologies developed in the earlier chapters can be applied to various novel nanoscale devices. In this chapter, the advance of the electrical and physical characterization is demonstrated using MG/HK gate stacks. It is shown that the physical characterization provides us with useful information in solving the fundamental problems faced in device fabrication and reliability. Firstly, flatband voltage shift induced by varying the metal gate Ti/N ratio is investigated. The interfacial dipoles at both the MG/HK and HK/IL interfaces are identified to be the mechanism responsible for the negative V_{FB} shift for sub-stoichiometric TiN_x gate. Secondly, the impact of gate electrode on post-BD device reliability is studied. For fully silicided NiSi gate on SiON and HK gate dielectrics, percolation conduction recoveries are found to be a feasible way to prolong the post-BD device lifetime. The breakdown induced metal migration helps to construct a metal-insulator-metal structure which facilitates the diffusion of oxygen vacancies and/or Ni metal filamentation in the vicinity of the percolation path under different biasing conditions. On the other hand, Ta metal filamentation in a $\text{TaN}/\text{HfZrO}_4/\text{SiO}_x$

gate stack gives rise to ultrafast post-BD degradation and significantly reduces the post-BD reliability margin of the TaN gate devices.

6.2 Modulation of Oxygen Distribution in High- κ Gate Dielectrics by Gate TiN Composition

Microprocessor speeds have steadily increased over the past decades by continuous miniaturization of MOSFETs. A critical barrier has now been reached in the use of doped polycrystalline silicon as traditional gate material. Near the gate dielectric, doping depletion in the gate material is unavoidable; the resulting lower gate capacitance and channel current gives an overall degradation in the device performance. To facilitate further MOSFET miniaturization, one solution around this problem is the introduction of metal gate materials. Of these, TiN is an important candidate for implementation in future MOSFETs, which will be combined with high- κ gate dielectric technologies [1-6]. Depending on the deposition methods, the work function of TiN could be as high as 5.1 eV [2], which makes it suitable for pMOSFET integration. On the other hand, efforts have been made to reduce the work function value (to ~ 4.1 eV ideally) for nMOSFET by controlling either the thickness of the TiN [5, 6] or the nitrogen concentration, x , of TiN_x [1, 3]. For TiN thickness variation, it has been shown that the work function can be tuned between 4.2 and 4.6 eV for TiN/ HfO_2 [5] and 4.44 to 4.7 eV for TiN/ HfSiON [6]. By changing x , on the other hand, the work function can be reduced from 4.9 eV (TiN_x , $x = 1$) to 4.2 eV (sub-stoichiometric TiN_x , $x < 1$) for TiN/ SiO_2 [3]. It is worth noting that based on theoretical calculation, the effective work function of TiN on HfO_2 can be changed from 6.2 eV (stoichiometric interface) to 6.1-5.9 eV by either inter-diffusion at the interface or the

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introduction of oxygen vacancies, while the effective work function for a pure Ti/Hf interface is 5.2 eV [4]. However, poor thermal stabilities have been found for TiN on SiO₂ and HK, which always drive the work function to mid-gap values (~ 4.7 eV) [2, 3, 7] after high temperature annealing. At the same time, various metals, metal alloys and/or dopings in the dielectrics have been studied to further tune the work function to the required values for n and pMOSFETs [8-17]. Recently, the creation of interface dipoles at HK/IL (IL is the SiO₂ based interfacial layer between the HK and Si substrate) interface shows very promising results for flatband voltage V_{FB} tuning [9-17] with high thermal stability. The key to realize a successful V_{FB} tuning is found in the modulation of the oxygen distribution in the dielectrics [11, 15-17]. In this section, we investigate the nanoscale modulation of oxygen at the MG/HK and HK/IL interfaces by changing the gate Ti/N ratio and its effect on V_{FB} .

Figure 6.1. Illustration of (a) Nitrogen-rich and (b) Titanium-rich TiN metal-gate/high- κ gate stack. The only variation in the process is the deposition of the metal gate, where two Ti/N ratios are used.

The details of the gate stacks used in this study are illustrated in Fig. 6.1, in which standard SiO_x IL and HfO₂ (2.5 nm) HK with nitridation are deposited on Si substrate. The TiN metal gates, N-rich (Fig. 6.1(a)) and Ti-rich (Fig. 6.1(b)), were deposited using physical vapor deposition (PVD)

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followed by a 30-minute forming gas annealing (FGA) at 425°C and a high temperature rapid thermal annealing (RTA) at 1000°C for 30 seconds. The physical and chemical information of the gate stack was analyzed using STEM, EELS and EDS. The EELS energy resolution was about 0.7 eV with the 0.1 eV/channel dispersion. The probe semi-convergence angle is around 10mrad using 50 micron C2 aperture. The EELS collection semi-angle is 7.6 mrad using 77mm camera length and 2.5mm Gatan image filter entrance aperture. The STEM probe size was set to be around 2-3 Å in diameter during imaging and 3-4 Å in diameter during the EELS/EDS signal acquisition. The samples were mechanically thinned down with low energy ion milling to electron transparency for TEM analysis.

In Fig. 6.2, the high resolution TEM and HAADF micrographs of the N-rich (Fig. 6.2(a)) and Ti-rich (Fig. 6.2(b)) samples are shown, respectively. The thicknesses of the HK/IL gate dielectrics are 2.6/1.6 nm for the N-rich sample and 2.6/1.3 nm for the Ti-rich sample. An apparent IL thickness reduction for the Ti-rich sample was found. The effective oxide thickness (EOT) extracted from C - V capacitance measurements is 2.25 nm (N-rich) and 2.13 nm (Ti-rich), respectively. The flatband voltages are also extracted and plotted in Fig. 6.3(a). The samples had gone through either low temperature FGA or high temperature RTA. As shown in the figure, the Ti-rich samples have an average negative V_{FB} shift of -0.7 V and -1.2 V for the FGA and RTA samples, respectively. On the other hand, the N-rich samples exhibit very good thermal stability, and the V_{FB} shift is around -0.05 V and -0.12 V for FGA and RTA samples, in agreement with the reported values for $\text{TiN}_x/\text{SiO}_2$ [3]. However, unlike the TiN_x on SiO_2 , whose work function collapses to the mid-gap values after an 800°C RTA process for both Ti- and N-rich TiN_x [3], the $\text{TiN}_x/\text{HfO}_2$ stacks used in this study demonstrate relatively good thermal stability. This has been attributed to an insignificant generation of extrinsic states at the MG/ HfO_2 interface upon

annealing [7]. Nevertheless, the gate dielectrics have already been affected by the thermal treatment to a certain extent as shown from the I - V measurements (see Fig.6.3(b)), especially for the Ti-rich samples.

Figure 6.2. High resolution TEM and HAADF micrographs of (a) N-rich and (b) Ti-rich TiN MG/HK gate stacks. The HK and IL layers in the TEM and HAADF micrographs were not aligned since they were acquired at different regions from samples at different magnifications. The thicknesses of the gate dielectrics are labeled respectively. The Ti-rich sample shows apparent IL thickness reduction.

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As shown in Fig. 6.3(b) for the N-rich samples, the gate dielectrics break down around $V_g = -5$ V. In contrast, the gate dielectrics of the Ti-rich samples are more leaky (red-colored curves) and even show initial BDs for some fresh capacitors (blue-colored curves). The BD voltages for the Ti-rich samples also reduce to around $V_g = -4.2$ V. Since the gate dielectrics of the Ti-rich samples are clearly degraded after annealing, they show large variations in the capacitance measurements and V_{FB} extraction.

Figure 6.3. (a) Flatband voltages extracted from C - V measurements for the N- and Ti-rich samples. Results for both the low temperature FGA and the high temperature RTA are presented. (b) Respective I - V ramp test results.

Microscopic analysis was then carried out in an attempt to find out the origin of the V_{FB} shift observed here. Fig. 6.4 depicts the elemental profiles of the N-rich (Fig. 6.4(a)) and Ti-rich (Fig. 6.4(b)) samples measured using EELS/EDS. Line scans with a point-to-point separation of 6 Å and 4 Å probe size were performed across the gate stack. At each point, the signals carrying the sample's chemical information were simultaneously detected by the EELS and EDS detectors.

(a)

(b)

Figure 6.4. EELS/EDS elemental line profiles of (a) Nitrogen-rich and (b) Titanium-rich TiN metal-gate/high- κ gate stack. The dashed lines are the respective HAADF intensity (Z-contrast) profiles of the line scans. With respect to the Hf profile, the O in the gate dielectrics for the Ti-rich sample shows a broader distribution towards the gate. The reduced N concentration in the gate dielectrics for the Ti-rich sample is also observed.

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The N, Ti and O signals were analyzed by the core-loss EELS signals, which include N-K (~ 401 eV), Ti-L (~ 456 eV) and O-K (~ 532 eV) edges. EDS was used for better detection of Hf. We use Hf-L edge at around 8 keV due to the fact that there is an overlap of Hf-M and Si-K edges at 1.7 keV [18]. The distribution of Hf was then plotted together with the EELS data and normalized to the oxygen maximum for comparison purpose. The dashed lines in the figures are the respective HAADF intensity (Z-contrast) profiles of the line scans. We can quantify the Ti/N ratio using the EELS signals in the gate, which are $\text{TiN}_{0.56}$ (N-rich) and $\text{TiN}_{0.43}$ (Ti-rich) using a 20 eV window for the N-K edge and a 10 eV window for the Ti-L edge. The O profile for the Ti-rich sample has more overlap with the Hf profile towards the TiN gate side. The N concentration is also reduced for the Ti-rich sample.

Figure 6.5. Normalized elemental profiles of the gate stacks acquired at three different locations on each N-rich and Ti-rich TEM sample. They are aligned at the TiN/HK interface and normalized to their maximum intensities respectively.

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In order to show the repeatability of our measurements, the Hf, Ti, O, and N profiles acquired at three different locations on each sample are plotted in Fig. 6.5. The elemental profiles are aligned at the TiN/HK interface and normalized to their maximum intensities for comparison purpose. As shown in the figure, the Ti and N profiles align well for N-rich and Ti-rich samples at the TiN/HK interface with small variations. However, the Hf profiles of the N-rich samples (black-curves) display more overlap with the TiN at the TiN/HK interface as compared with Ti-rich samples (red-curves). There is a presence of nitrogen in the HK/IL dielectrics for N-rich sample, while for Ti-rich sample the signal is low. The oxygen distribution in this case is critical, and they are plotted separately in Fig. 6.7. As indicated by the arrows in Fig. 6.6(a), two regions show apparent differences. The first region appears in the IL where a more abrupt slope is observed for Ti-rich sample, which accounts for the IL reduction. The second region is the Hf shift for N-rich sample at the TiN/HK interface. In another word, the TiN/HK interface of N-rich sample has excess Hf or it is an oxygen deficient interface. Likewise, the TiN/HK interface of Ti-rich sample is oxygen rich. This is clearly demonstrated in Fig. 6.6(b). The separation of Hf and O maximum is less for Ti-rich sample. In the earlier work on the mechanism of O transport in MG/HK/IL, it was concluded that the oxygen enthalpy difference [17] and/or oxygen density [16] play important roles in driving the diffusion of O^{2-} and V_O^{2+} . We employ the same mechanism here to explain the observed O movement. The sub-stoichiometric TiN_x contains excess Ti atoms which are very reactive [3]. At high temperatures, the Ti at the TiN_x /HK interface gathers O (and/or N) from HK and leaves V_O . In order to compensate the O loss in HK, the O from bottom of the HK and IL moves up (V_O moves down) until an equilibrium is reached. The electrical dipoles (e.g., O^{2-} - V_O^{2+} pair) formed at both the TiN/HK and HK/IL interfaces create a negative V_{FB} shift [11].

(a)

(b)

Figure 6.6. (a) Comparison of Hf and O profiles in the gate dielectrics for the N-rich and Ti-rich samples shown in Fig. 6.5. (b) The Hf and O profiles plotted separately for N-rich and Ti-rich samples.

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Since the variation in TiN crystal orientation has very limited effect on the work function shift [1, 3], the dipole formation at TiN/HK and HK/IL interfaces as a result of the O diffusion is suggested to be the physical mechanism responsible for the negative V_{FB} shift for the Ti-rich sample. Despite the fact that a large negative V_{FB} shift is created using the Ti-rich gate, defect centers (e.g., V_O) are also generated in the dielectrics especially at higher temperatures. The reliability of the dielectrics is therefore a potential concern for such devices as reflected from the I - V results shown in Fig. 6.3(b).

6.3 Recovery of Percolation Conduction in NiSi Gate Stacks

Even through the ‘ultrafast’ degradation was observed for some MG/HK gate stacks, the post-BD reliability margin was considerably underestimated for other MG/HK systems. Our recent studies show that for nickel-based fully silicided metal gate (Ni-FUSI), I_g recovery (from very severe BD) is observed. This new failure mechanism (with recovery) is studied in details in this section since it could facilitate the on-chip repairing of the failure transistor and prolong its lifetime.

6.3.1 Recovery of Percolation Conduction

The post-BD I_g recovery was firstly observed on NiSi/SiON pMOSFETs. As shown in Fig. 6.7(a) for a NiSi/SiON pMOSFET stressed in accumulation mode (i.e., substrate injection) at $V_{gstress} = 2.7$ V, the gate leakage current I_g shows switching between high and low conduction levels (i.e., recovery from a harder BD to a softer BD). Since a successive CVS was used by relaxing the I_{gl} gradually from 10 μ A to 1 mA, the 2.7 V stress was interrupted whenever the current or time

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compliance was reached. The BD transistor was then subjected to standard electrical measurements such as I_d-V_d and I_g-V_g before the next stress was applied. For this sample, the I_g recoveries took place after the $I_{gl} = 50$ & $300 \mu\text{A}$ stress. The I_g recovered not only after the interruption of the post-BD stress but also happened during the post-BD stress, as shown in the first $I_{gl} = 1 \text{ mA}$ stress. It is worth to mention that the recovery of I_g shown here is different from the digital fluctuation in the early stage of the progressive BD introduced in Chapter 5. The main differences are: 1) a higher biasing voltage was used (i.e., $V_{g\text{stress}} = 2.7 \text{ V} > V_{\text{crit}}$) and 2) the magnitudes of the high and low conduction states differ by 2-3 orders of magnitudes (e.g., Fig. 6.7(a)). The I_g recovery is also revealed from the post-BD I_g-V_g measurements (on the same sample) shown in Fig. 6.7(b). In particular, the I_g after $I_{gl} = 100 \mu\text{A}$ stress shows huge leakage current (i.e., HBD characteristic). However, the I_g recovers to a much lower leakage state after the first $I_{gl} = 1 \text{ mA}$ stress applied.

Figure 6.7. (a) Time evolution of the post-BD gate leakage current of a NiSi/SiON pMOSFET ($W \times L = 0.15 \times 0.15 \mu\text{m}^2$, EOT = 1.4 nm) stressed in accumulation mode (i.e., substrate injection) with a constant $V_{g\text{stress}}$ of 2.7 V and $I_{gl} = 10 \mu\text{A} - 1 \text{ mA}$. The initial BD location is near the Source terminal. (b) Pre- and post-BD I_g-V_g measurements of the same sample after the stress being stopped by I_{gl} . It shows I_g recovery after $I_{gl} = 10 \mu\text{A}$ & $I_{gl} = 100 \mu\text{A}$ stress.

Figure 6.8. Time evolution of I_g for NiSi/SiON pMOSFETs (a) $W \times L = 1.0 \times 0.15 \mu\text{m}^2$, stressed using $V_{gstress} = 2.7$ V and $I_{gl} = 10 \mu\text{A} - 600 \mu\text{A}$. The inset shows a random switching between two conduction levels during the $I_{gl} = 600 \mu\text{A}$ stress. (b) $W \times L = 0.15 \times 0.18 \mu\text{m}^2$, stressed using $V_{gstress} = 3.0$ V and $I_{gl} = 10 \mu\text{A} - 300 \mu\text{A}$. No post-BD I - V measurements were performed after the stress being stopped by I_{gl} .

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In Fig. 6.8, the results obtained from two more NiSi/SiON pMOSFETs are shown. Figure 6.8(a) is the time evolution of I_g for one sample ($W \times L = 1.0 \times 0.15 \mu\text{m}^2$) under $V_{g\text{stress}} = 2.7 \text{ V}$ and I_{gl} relaxed from $10 \mu\text{A}$ to $600 \mu\text{A}$. As shown, I_g recovered from $I_{gl} = 50 \mu\text{A}$ stress and reduced to a very low leakage state in the beginning of the $I_{gl} = 100 \mu\text{A}$ stress. The I_g switching between two conduction levels was observed during the $I_{gl} = 600 \mu\text{A}$ stress, as highlighted in the inset. Furthermore, the I_g evolution of another sample ($W \times L = 0.15 \times 0.18 \mu\text{m}^2$) stressed using $V_{g\text{stress}} = 3.0 \text{ V}$ and $I_{gl} = 10 \mu\text{A} - 300 \mu\text{A}$ without any post-BD $I-V$ measurements is shown in Fig. 6.8(b). Similarly, the gate leakage current I_g recovered from $I_{gl} = 20, 50, 100, 150$ and $250 \mu\text{A}$ stress and decreased to a low leakage level (i.e., $< 10 \mu\text{A}$) at the next stress. In this case, there was no post-BD $I-V$ measurements applied and the I_g recovery was able to take place.

Figure 6.9. (a) Post-BD gate leakage current evolution with time of a NiSi/HfSiON nMOSFETs ($W \times L = 1.0 \times 0.25 \mu\text{m}^2$) stressed in the inversion mode (i.e., substrate injection) with a constant $V_{g\text{stress}}$ of 3.0 V and $I_{gl} = 2 \mu\text{A} - 2 \text{ mA}$. The initial BD location is near Drain terminal. (b) Pre- and post-BD gate leakage current I_g of the same sample.

Similar results have been obtained for NiSi/HfSiON high- κ gate stacks, as shown in Fig. 6.9. Figure 6.9(a) shows the time evolution of I_g for a NiSi/HfSiON nMOSFET stressed in inversion

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mode at $V_{gstress} = 3.0$ V. It shows significant I_g recovery after $I_{gl} = 2, 5, 10, 20$ and 50 μ A stress. As shown in Fig. 6.9(b), I_g recovered to a very low leakage level (as see after the $I_{gl} = 10$ μ A stress) from a high conduction state after $I_{gl} = 2$ μ A stress. This recovery behavior has also been observed for gate injection when stressed in accumulation mode. The recovery of I_g indicates possible switching off of the percolation path in the SiON and HfSiON gate dielectrics. As shown, it can happen when the post-BD stress is applied or interrupted and/or during the post-BD I - V measurements.

Figure 6.10. Post-BD I_D - V_D characteristics of two NiSi/HfSiON nMOSFETs at $V_g = 0.375, 0.75, 1.125$ and 1.5 V after a successive relaxing of I_{gl} to (a) 10 μ A and (b) 500 μ A. For both samples, I_D at $V_g = 0$ V shows linear relationship with V_D (resistor-like behavior for terminal short case) before the recovery happens. After recovery, the transistor regains its normal characteristics.

Figure 6.10 displays two post-BD I_D - V_D measurements for two NiSi/HfSiON nMOSFETs after $I_{gl} = 10$ μ A (Fig. 6.10(a)) and $I_{gl} = 500$ μ A (Fig. 6.10(b)) stress. For both samples, the I_D at $V_g = 0$ V shows linear relationship with V_D (resistor-like behavior) before the recovery happens. After the recovery, the I_D - V_D curves returns back to normal transistor characteristics as shown from the V_g

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= 1.5 V curves. At $V_g = 0V$, there is no conduction channel formed in the substrate and the I_D current flow from the Drain terminal to the gate terminal through the percolation path directly. In order to further understand the I_g recovery observed in the electrical characterizations, physical analysis (i.e., TEM/EELS) was carried out as discussed in the following section.

6.3.2 Physical Analysis of Percolation Path Recovery

In this section, we study specifically the physical structure and BD chemistry of the Ni-FUSI/high- κ samples showing good I_g recovery and devices which are very difficult to be recovered from the high leakage state in attempts to find out the mechanism of the recovery behavior observed in the post-BD electrical characterization shown in Figs. 6.7 to 6.10. Based on the TEM analyses of BD locations, two main categories of physical failure were identified: 1) BD at S/D corners (denoted as corner-BD) and 2) BD in the channel of the transistor (denoted as channel-BD). Figure 6.11 shows the TEM micrographs of four post-BD nMOSFETs failed under substrate injection (i.e., gate positive biased) stress. In Figs. 6.11(a) and (b), corner-BD was found at one of the gate corners with dielectric breakdown induced metal-migration from the S/D silicide. On the other hand, channel-BD was found in Figs. 6.11(c) and (d), where Si-DBIE from the substrate was clearly shown in the vicinity of the BD. Significant damage in the substrate was also observed. The location of the BD has direct effect on the post-BD conduction [19] where the corner-BDs lead to less channel resistance since they are closer to the S/D terminal. Thus the percolation path near the corner shows a faster degradation rate as compared with the channel-BD. As a result, the recovery of the percolation path resistance also depends on the BD location (i.e., channel resistance).

Figure 6.11. TEM micrographs of four post-BD transistors failed under substrate injection (i.e., gate positive biased) stress. (a) NiSi/SiON pMOSFET of $W \times L = 0.15 \times 0.11 \mu\text{m}^2$ shows damage created at one corner with Ni-silicide DBIM, (b) NiSi/HfSiON nMOSFET of $W \times L = 0.15 \times 0.20 \mu\text{m}^2$ shows corner BD damage with Ni-silicide DBIM, (c) NiSi/HfSiON nMOSFET of $W \times L = 0.18 \times 0.25 \mu\text{m}^2$ shows channel BD with Si-DBIE from substrate, and (d) NiSi/HfSiON nMOSFET of $W \times L = 0.15 \times 0.25 \mu\text{m}^2$ shows channel BD and DBIE from substrate.

Figure 6.12. TEM micrographs of four post-BD NiSi/HfSiON nMOSFETs failed under substrate injection stress for (a) $W \times L = 0.15 \times 0.50 \mu m^2$ with $I_{gl} = 100 \mu A$, (b) $W \times L = 0.15 \times 0.35 \mu m^2$ with $I_{gl} = 10 \mu A$, (c) $W \times L = 0.15 \times 0.25 \mu m^2$ with $I_{gl} = 30 \mu A$, and gate injection stress for (d) $W \times L = 0.15 \times 0.35 \mu m^2$ with $I_{gl} = 500 \mu A$. The insets are the respective low magnification TEM and/or HAADF micrographs.

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Figure 6.12 shows the TEM micrographs of four NiSi/HfSiON nMOSFET samples failed under either inversion or accumulation CVS stress. The recovery of I_g was observed either during stressing or after the post-BD I - V measurements. One common observation is that the location of the BD is at the gate corner (i.e., corner-BD). The physical damage is closely related to the final failure current I_{gl} . For $I_{gl} = 100$ & $500 \mu\text{A}$ as shown in Figs. 6.12(a) and (d), DBIM is found at the respective gate corner shorting the nearby Drain terminal and the gate terminal. The degree of damage is less significant if we keep the current compliance low, as shown in Figs. 6.12 (b) and (c) for $I_{gl} = 10$ & $30 \mu\text{A}$. For lower I_{gl} cases, DBIM and physical damage in the Si substrate are clearly observed as well. Since the metal migration is driven by the electron wind flow from cathode to anode, the current density (both the magnitude of the leakage current and the cross-section of the leakage path) plays important role in determining the formation of the DBIM [20]. Since the DBIM in Figs. 6.12(a) and (d) are created by CVS biased under different polarities, which is substrate injection for Fig. 6.12(a) and gate injection for Fig. 6.12(d), we study in details of the DBIM formation in these two cases.

The nano-scale chemical characterization using EDS/EELS were performed on the samples with DBIM failure found at the BD locations. Figure 6.13(a) shows the TEM micrograph of the sample failed under substrate injection CVS with $I_{gl} = 100 \mu\text{A}$. The compositions of the material at different locations were quantified using the respective EDS signals as labeled in the solid circles. It can be seen that Ni atoms originating from the Drain silicide migrate towards the NiSi-gate at the gate corner. Please note that the source/drain silicide is also Ni-monosilicide, NiSi. One interesting finding is that the Ni concentration in the NiSi-gate near the BD location is decreasing, from NiSi_{1.33} to NiSi_{2.0} and NiSi_{3.88}. It therefore reveals two driving forces for Ni migration: 1) the electron wind force which moves the Ni atoms to the

anode side (silicide to gate), and 2) the ionic drift force due to the electric field which drives the positively charged Ni ions in the gate towards the cathode direction.

(a)

(b)

Figure 6.13. (a) TEM micrograph of the sample failed under substrate injection CVS with $I_{gl} = 100 \mu\text{A}$. DBIM was found at the gate corner near the Drain terminal. The compositions of the material at different locations (solid circles) were quantified using the respective EDS signals as labeled in the figure. (b) Ni- $L_{2,3}$ edge EELS acquired at five locations (numbers 1-5) in the vicinity of the BD as indicated in Fig. 6.13(a) by the red dotted circles.

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The DBIM formation due to the first mechanism is clearly displayed in Figs. 6.12(a) and (d) where the Ni atoms are driven from the cathode to the anode. The Ni migration due to the second mechanism is confirmed in Fig. 6.12(c). Despite the electron injections from the Source terminal to the gate, there is DBIM formation at the gate corner from the NiSi-gate to the Si substrate. It therefore shows that DBIM can be formed under both polarities, i.e., cathode to anode and/or anode to cathode. However, the prerequisite of the second mechanism is that the high- κ gate dielectrics must be broken down, so that there is no barrier to block the metal ions from drifting.

The Ni-L_{2,3} edge EELS were also acquired at five locations (numbers 1-5 as indicated in Fig. 6.13(a) by the dotted circles) and presented in Fig. 6.13(b). Spectra 1 & 2 were collected in the NiSi-gate where Spectrum-2 near the BD displays slightly lower Ni intensities. For Spectra 3 & 4 acquired from the DBIM region in the substrate, the positions of L₃ edges shifted to a higher energy loss as compared with the NiSi-gate, indicating a formation of Ni-Si solid solution with lower Ni%. Since the elemental quantifications using EDS and EELS signals are an average over the TEM sample thickness, the results are only accurate at the locations where the TEM sample contains only the materials of interest. This includes the gate or S/D silicide. However, the quantification of DBIM composition in the Si substrate can be significantly underestimated (e.g., NiSi_{8.0} and NiSi_{4.67} in Fig. 6.13(a)) due to the fact that the DBIM migrated into the substrate may not be as thick as the TEM sample. There are additional Si signals coming from the pure Si region in the substrate (similar to the quantification problem introduced in Chapter 5). Fortunately, the Ni-L_{2,3} edge EELS probes only the Ni atoms in the Ni-DBIM. The Ni intensities in the DBIM are low as compared with the gate or Drain silicide, but the positions of L₃ and L₂ edges reflect the true Ni% in the Ni-DBIM. Since the edge positions shift to a higher energy loss as the Ni% decreases [21], the composition of the DBIM in the Si substrate is likely to be NiSi₂

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or NiSi_x (x less than 2) using Spectrum-5 (from the Drain silicide) as a reference. Please note that the resistivity of NiSi_2 is about 2-3 times higher than NiSi .

(a)

(b)

Figure 6.14. (a) TEM micrograph of the sample failed under gate injection CVS with $I_{gl} = 500$ μA . DBIM was found at the gate corner near the Drain terminal. The compositions of the material at different locations (solid circles) were quantified using the respective EDS signals as labeled in the figure. (b) Ni- $L_{2,3}$ edge EELS acquired at five locations (numbers 1-5) in the vicinity of the BD as indicated in Fig. 6.14(a) by the red dotted circles.

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Similar analysis was performed for the sample failed under gate injection CVS with $I_{gl} = 500 \mu\text{A}$. As shown in Fig. 6.14, the HK gate dielectrics near the gate edge are completely ruptured and fused locally as shown in Figs. 6.12(d) and 6.14(a). At the gate edge, it shows apparent burnt damage and a decreased Ni% ($\sim \text{NiSi}_2$). The Ni-L_{2,3} edge of Spectrum-3 in Fig. 6.14(b) has lower Ni counts as compared with the NiSi-gate (i.e., Spectra-1 & 2). The lower Ni% at the gate edge is believed to be caused by Ni migration from the gate to the substrate and Drain. On the other hand, high Ni% ($\sim \text{Ni}_2\text{Si}$) is found at some positions near the gate dielectrics and in the DBIM, e.g., $\text{NiSi}_{0.5}$, $\text{NiSi}_{0.67}$ and $\text{NiSi}_{0.56}$. Spectra-4 & 5 acquired from the DBIM region in the substrate show similar Ni-L₃ edge positions in Fig. 6.14(b) comparing to the NiSi-gate. The DBIM compositions at Positions-4 & 5 in the substrate are therefore close to NiSi. Based on the EDS and EELS results, it does not show uniform Ni-silicide distributions. Instead, different phases of Ni-silicide, Ni_2Si , NiSi and NiSi_2 , are observed at different positions from the gate to the DBIM. Since the Ni concentration is determined by the BD induced migration process and the phase of the Ni-silicide depends on the local temperature (i.e., the current density) as well as the bulk limited diffusion, the formation of the DBIM with different Ni% is rather location dependent. Nevertheless, the BD induced DBIM (with different phases and resistivity) has direct effect on the recovery of the gate leakage current I_g and “switching off” of percolation path.

There are exceptional cases in our analysis in which no I_g recovery and HBD I - V characteristics are found for devices failed under low I_{gl} . Figure 6.15 shows two samples failed at $I_{gl} = 2 \mu\text{A}$ (Fig. 6.15(a)) and $10 \mu\text{A}$ (Fig. 6.15(b)) under substrate injection CVS. The BD locations are at the respective gate corners and severe physical damage is observed. For the two samples, DBIE protrusion from the substrate to the gate and Ni-DBIM from the gate to the substrate are clearly shown at the BD locations. The HK/IL gate dielectrics are ruptured and a

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direct short between the gate and the S/D terminal is created. The only difference from the pervious corner-BD samples which show I_g recovery is that DBIE protrusions are observed in this case. The corner-BD in this case shows fast post-BD degradation and quickly evolves to a HBD failure even though we have capped the current compliance low.

Figure 6.15. TEM micrographs of two corner-BD NiSi/HfSiON nMOSFETs failed under substrate injection stress for (a) $W \times L = 0.15 \times 0.15 \mu\text{m}^2$ with $I_{gl} = 2 \mu\text{A}$, and (b) $W \times L = 0.15 \times 0.25 \mu\text{m}^2$ with $I_{gl} = 10 \mu\text{A}$. The insets are the respective low magnification TEM and/or HAADF micrographs.

In contrast to the HBD damage found for the corner-BDs, the microstructural damage for channel-BD cases is less catastrophic. Figure 6.16 shows two samples failed at $I_{gl} = 5 \mu\text{A}$ (Fig. 6.16(a)) and $10 \mu\text{A}$ (Fig. 6.16(b)) under substrate injection CVS. The BD locations are at $0.86L$ and $0.33L$ from the Source terminal. There is no clear physical damage observed. In Figs. 6.15 and 6.16, the effect of BD location is demonstrated [19]. The post-BD degradation for the channel-BD sample is limited by the channel resistance [22] and therefore exhibits a slower degradation rate and the “softer” physical damage [23].

Figure 6.16. TEM micrographs of two channel-BD NiSi/HfSiON nMOSFETs failed under substrate injection stress for (a) $W \times L = 0.15 \times 0.20 \mu\text{m}^2$ with $I_{gl} = 5 \mu\text{A}$, and (b) $W \times L = 0.15 \times 0.15 \mu\text{m}^2$ with $I_{gl} = 10 \mu\text{A}$. The insets are the respective HAADF micrographs. The BD locations are at $0.86L$ and $0.33L$ from the Source terminal.

Figure 6.17(a) shows the HAADF micrograph of another channel-BD sample failed under substrate injection CVS with $I_{gl} = 100 \mu\text{A}$. The BD location is at the center of the channel as indicated in the inserted low magnification TEM micrograph. No obvious microstructural change is observed at the BD location. In Fig. 6.17(b), EELS elemental line profiles across the gate stack at BD and non-BD locations are presented. The O and Ni distributions are plotted using the O-K edge and Ni-L_{2,3} edge EELS. As compared with the non-BD gate dielectrics, the BD locations show O diffusion to the gate and Ni accumulation and diffusion to the substrate. The inset is the enlarged plot of the O profiles at the HK/NiSi interface. It can be seen that in the vicinity of the BD, the oxygen atoms from the gate dielectrics are dislodged and pushed towards the NiSi-gate while the nickel atoms/ions drift to the substrate through the percolated gate dielectrics.

Figure 6.17. (a) STEM-HAADF micrograph of the sample $W \times L = 0.15 \times 0.20 \mu m^2$ failed under substrate injection CVS with $I_{gl} = 100 \mu A$. The BD location is at the center of the channel as indicated in the inserted low magnification TEM micrograph. No obvious physical damage is observed. (b) EELS elemental line profiles across the gate stack at the BD and non-BD locations. The O and Ni distributions are shown using O-K edge and Ni-L_{2,3} edge EELS. The inset is an enlarged plot of the O profiles at the HK/NiSi interface.

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Figure 6.18 shows another example of channel-BD which failed under substrate injection CVS with $I_{gl} = 500 \mu\text{A}$. As shown in the TEM and HAADF micrographs in Figs. 6.18(a) and (b), DBIE and Ni spiking are found at the BD location. The BD location is at $0.81L$ from the Source terminal as indicated in the inserted low magnification TEM/HAADF micrographs. In Fig. 6.18(b), the Ni and O EELS elemental line profiles across the gate stack at BD and non-BD locations are shown. Using the non-BD line profile as the reference, the O and Ni intensities at the DBIE region (in the gate dielectrics and the NiSi-gate) decrease significantly. At both edges of the DBIE, there is a lowering of O intensity in the HK as well as Ni migration into the gate dielectrics forming metal filament. This correlates well with the observation of the Ni spiking at the edge of the DBIE (Fig. 6.18(a)). Based on the physical results shown in Figs. 6.15 and 6.18, we can conclude that the physical damage of the channel-BDs are similar with the corner-BDs, which are the Si-DBIE, Ni-DBIM and O redistributions. However, the physical change of the channel-BDs is only observed for high I_{gl} (e.g., $I_{gl} = 500 \mu\text{A}$ in Fig. 6.18). Since the channel resistances help to limit the BD hardness, we can use the channel-BD cases to study the early stage of the defect formation. The I_g recovery for channel-BD is not easily observed and higher biasing voltages are usually required to switch off the leakage path.

The physical analysis results obtained from the Ni-FUSI gate stacks are summarized in Table 6.1. It can be seen that the formation of DBIM is the common physical signature associated with the I_g recovery. The DBIM in the Si substrate, HK gate dielectrics and NiSi-gate effectively form a metal-insulator-metal (MIM) structure where the diffusion of oxygen and/or Ni filament formation could take place as reported in various resistive switching memory structures [24-26]. On the other hand, the formation of DBIE creates a permanent leakage path by punching through the HK gate dielectrics and prohibits the I_g recovery. Since the Ni migration

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depends strongly on the electron current density J , the DBIM can be formed more easily for the corner-BD cases.

Figure 6.18. (a) TEM and (b) STEM-HAADF micrographs of an nMOSFET sample $W \times L = 0.15 \times 0.50 \mu\text{m}^2$ failed under substrate injection CVS with $I_{gl} = 500 \mu\text{A}$. The BD location is at $0.81L$ from Source terminal as indicated in the inserted low magnification TEM/HAADF micrographs. DBIE and Ni spiking are observed at the BD location. (c) Ni and O EELS elemental line profiles across the gate stack at the BD and non-BD locations.

Table 6.1 Summary of the physical analysis results for Ni-FUSI gate stacks.

Breakdown location	Gate compliance current (I_{gl}) LOW	Gate compliance current (I_{gl}) HIGH	Gate leakage current recovery
Corner BD I	DBIM	DBIM	Yes
Corner BD II	DBIM/DBIE	Channel short	No
Channel BD	No damage	DBIM/DBIE	Yes (but difficult)

6.4 Metal Filamentation of TaN/HfZrO₄/SiO_x Gate Stacks

In this section, migration of Ta atoms from a transistor gate electrode into the percolated high- κ gate dielectrics is directly shown. A nanoscale metal filament that formed under high current injection is identified to be the physical defect responsible for the ultrafast transient breakdown of the metal-gate/high- κ gate stacks. This highly conductive metal filament poses reliability concerns for MG/HK gate stacks as it significantly reduces the post-BD reliability margin of a transistor.

6.2.1 Ultrafast Breakdown

Ultrafast transient breakdown reported by several research groups [27-29] is one of the unique failure mechanisms associated with the MG/HK gate stacks. It is important to pay attention to this new failure mechanism since it severely limits the post-BD lifetime of transistors [27-29]. Based on the reported literature, the physical defect responsible for the ultrafast BD has been attributed to a metal-like filament formation in the percolation path [29, 30]. Rakesh *et al.* [30]

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have found a mixture of Ta, N and Hf in the Si substrate after a BD occurred in the gate dielectrics with a compliance current $I_{gl} = 7$ mA. However, no visible microstructural damage was found in the vicinity of the BD for I_{gl} less than 2 mA. Even though the concept of a metal-like percolation path has been proposed, there is no direct proof and/or in-depth study of the properties of the metal filament at the BD site due to the experimental difficulties in capturing and characterizing this nano-size defect. In this section, we experimentally demonstrate metal filament formation in MG/HK gate stacks and reveal its chemical nature, as well as addressing its impact on transistor reliability.

Figure 6.19. Time evolution of the gate leakage current I_g for seven nMOSFET samples (denoted as S1 to S7) under $V_{gstress} = 3.8$ V CVS with a compliance current limit I_{gl} varying from 2 μ A to 2 mA. Progressive degradations were first observed before the ultrafast transient BDs were reached, as indicated by the arrows.

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The samples used in this study are n-type MOSFETs with a dual layer TiN/TaN metal electrode and HfZrO₄/SiO_x gate dielectrics. The thicknesses of the HfZrO₄ and SiO_x interfacial layer are 2.5 nm and 1.2 nm, respectively. The channel width W of the sample was kept at 0.15 μm while the channel length L varied from 0.13 to 0.15 μm . The BD in the gate dielectrics was created using a constant voltage stress of $V_{gstress} = 3.8 \text{ V}$ (substrate injection) and $I_{gl} = 2 \text{ }\mu\text{A} - 2 \text{ mA}$.

The time evolution of the gate leakage current I_g under the CVS stressing for seven nMOSFET samples (denoted as S1 to S7) are shown in Fig. 6.19. When the BD occurred in the gate dielectrics, progressive degradations of I_g were first observed (e.g., S1, S3 and S5 as indicated by arrows in the figure). The current leaking through the percolation path is relatively low in magnitude (e.g., $< 1 \text{ }\mu\text{A}$) and increases slowly with time. It is likely that either the HK or the IL layer is broken down in this stage such that the remaining intact layer holds the entire electrical stress [31]. The random fluctuations of I_g displayed during the slow degradations are caused by the reconfigurations of trapping centers in the percolation path, similar to the digital breakdown of the silicon oxynitride devices [32]. In contrast, I_g quickly surges through the percolation path once an ultrafast degradation is reached. The current jump could reach the preset I_{gl} up to 2 mA almost instantaneously as shown in Fig. 6.19. In agreement with an earlier proposed mechanism [30], we will now show direct evidence for the formation of a metal-like percolation path as the physical origin of the fast transient BDs.

6.2.2 Ta metal Filamentation

Figure 6.20 shows TEM micrographs of Samples S1 (Fig. 6.20(a)) and S2 (Fig. 6.20(b)) at the respective BD locations [33]. As observed in Fig. 6.19, the compliance current limit for these two samples was capped at $I_{gl} = 2 \text{ }\mu\text{A}$ & $5 \text{ }\mu\text{A}$ and fast transient BDs were reached.

Figure 6.20. TEM micrographs of samples (a) S1 with a BD at location $s = 0.97L$ with $I_{gl} = 2 \mu\text{A}$, and (b) S2 at $s = 0.55L$ with $I_{gl} = 5 \mu\text{A}$, where L is the effective channel length of the MOSFET. The inset in (b) is a HAADF micrograph of S2 at gate center. (c) As-measured O K-edge EELS collected from the gate dielectric layer at gate center (i.e., BD) and gate corner (i.e., non-BD) of S2. There is no major change in the O K-edge peaks.

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For S1 shown in Fig. 6.20(a), there are some morphological changes in the IL at the BD location near the gate corner where crystalline structures are found throughout the HK/IL. Similarly, the BD gate dielectric at the gate center of S2 does not show any obvious structural damage except some morphological changes in the IL, as shown in Fig. 6.20(b). The inset of Fig. 6.20(b) is the corresponding HAADF micrograph (Z-contrast) which does not display any abnormal contrast at the BD gate dielectrics. The oxygen densities in the BD gate dielectrics of S2 were also measured using EELS as shown in Fig. 6.20(c). There was no observable difference in the oxygen concentration at the BD location as compared with the corresponding non-BD gate dielectrics. Based on the results, there could be two possible scenarios. The first possibility is that the metal filament is just formed in the percolation path, but the metal atoms migrated into the HK/IL are too few to be detected in the TEM and HAADF micrographs, especially for thicker TEM samples. The other possibility is that there is no metal filament formation in the percolation path under such low current injection conditions. It is very likely that the sudden jump in I_g at the onset of the transient BD corresponds to the BD of both HK and IL layers [31]. On the other hand, the metal migration and filament formation can be clearly observed for $I_{gl} \geq 5 \mu\text{A}$ as shown in Fig. 6.21. $I_{gl} = 5 \mu\text{A}$ is the lowest current level to trigger the metal migration in this study. Fig. 6.21(a) is the TEM micrograph of S3 having a BD at the gate center (as indicated in the inset) and there is a semi-spherical damage region in the Si substrate in the vicinity of the BD location. The HAADF micrograph of the BD gate dielectrics is shown in Fig. 6.21(b), where the damage region in the IL and Si substrate appears brighter in the contrast suggesting that the presence of heavy element(s), e.g., Ta or Hf.

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(a)

(b)

(c)

(d)

Figure 6.21. TEM micrographs of samples (a) S3 has a BD at $s = 0.51L$ with $I_{gl} = 5 \mu A$, (b) the corresponding HAADF micrograph of S3, (c) S4 at $s = 0.45L$ with $I_{gl} = 8 \mu A$, (d) S5 at gate center with $I_{gl} = 10 \mu A$ and (e) S6 at $s = 0.46L$ with $I_{gl} = 500 \mu A$. The insets in the figures are the respective low magnification TEM micrographs and/or HAADF micrographs. (f) As-measured O K-edge EELS acquired from the gate dielectrics of S3. Spectra collected from the BD dielectrics show apparent lowering of O counts.

The oxygen density measurement on this sample shown in Fig. 6.21(f) reveals that there is a significant lowering of the oxygen concentration in the BD gate dielectrics. It is worth noting that both S2 and S3 failed at $I_{gl} = 5 \mu A$, but they show apparent structural differences at the BD locations. It is therefore reasonable to assume that the $5 \mu A$ leakage (at $V_{gstress} = 3.8 V$) is the threshold of the metal migration that can be detected, which is also in agreement with the data reported by Rakesh *et al.* [30]. The size of the metal-like percolation path can be estimated based on Figs. 6.21 (a) & (b). Assuming the percolation path is cylindrical, its lateral diameter ($2r$, where r is the radius) is around 12 nm. The current density J that flowing through this leakage path is therefore $4.42 \times 10^6 A/cm^2$. However, the sizes of the metal filament and metal-silicon

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mixture in the substrate do not scale proportionally with J . As demonstrated on S4 ($I_{gl} = 8 \mu\text{A}$), S5 ($I_{gl} = 10 \mu\text{A}$) and S6 ($I_{gl} = 500 \mu\text{A}$) in Figs. 6.21(c), (d) & (e), the metal migration into the percolation path as well as the semi-spherical damage region in the substrate are clearly shown in the TEM and HAADF micrographs at their respective BD locations. The local structural damage is similar for samples S3, S4, S5 and S6. There is remarkably little variation in shape and size of the metal filament for BDs with different I_{gl} . For example, the lateral size of the metal filament in the BD dielectrics increases from 12 nm ($I_{gl} = 5 \mu\text{A}$) to 20 nm ($I_{gl} = 500 \mu\text{A}$). The metal migration also depends on the local temperature T , which is a critical parameter for the formation of the metal-silicon alloy or compound. Since the temperature is induced by joule heating, it is proportional to $J^2 R$ (R is the local resistance). As the current flux increases, the metal filament dilates and metal atoms migrate to a larger volume in the substrate. At the same time, the metal concentration of the metal filament and metal-silicon alloy becomes higher, which leads to a lower R . The combination effect of J and T determines the shape and size of the metal filamentation in the dielectrics and substrate.

We can stimulate the metal migration further by raising the current flux. As shown in Fig. 6.22(a) for sample S6 ($I_{gl} = 2 \text{ mA}$), the metal migration starts at the percolation path in the gate dielectrics and extends to the nearby Drain terminal. At this high I_{gl} , the migration of metal is so severe that the HK/IL layers have completely ruptured and no longer visible at the BD location. In order to identify the origin of the metal, EDS spectra were collected from five positions indicated in Fig. 6.22(a) and plotted in Fig. 6.22(b) for comparison. In Fig. 6.22(b), the EDS spectra at around 8 keV (i.e., Ta & Hf-L peaks) instead of the stronger Ta and Hf-M peaks were used to study the local chemistry, due to the overlap of the latter with the Si-K peak around 1.7 keV [18].

Figure 6.22. (a) HAADF micrograph of sample S6 at $s = 0.96L$ with $I_{gl} = 2 \text{ mA}$. Significant metal migration is shown at the gate corner near the Drain terminal. (b) EDS spectra collected at five positions indicated in (a). Excess Ta signals are found in the percolated HK and the bright regions in the Si substrate confirming that the heavy element is Ta from the TaN gate.

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As shown in Fig.6.22 (b), the HK at the BD and brighter regions in the substrate show excess Ta and low Hf signals. It therefore indicates that no Hf, but Ta has migrated from the TaN gate electrode towards the electron channel in the Si substrate. Crystal structures different from the Si lattice are also observed at the BD dielectrics and in the substrate. The hybrid mixture is likely to be Ta-silicide with certain amount of N and O. It should be noted that the direction of the Ta migration shown here is from the anode to the cathode, against the electron current. The driving forces of the Ta migration could be the hole-migration [29, 34] and/or the ionic drifting enhanced by the large electric field and high temperature [35]. Generally speaking, the metal migration and filament formation can be completed in three steps: 1) oxygen atoms are washed out from the gate dielectrics by percolation; 2) diffusion/drift of Ta atoms/ions into the percolation path at TaN/HK interface and possibly neutralization of the Ta ions by recombining with electrons from the leakage current; and 3) local electric field is greatly enhanced by the sharpness of the nucleating Ta filament; further diffusion of Ta towards the sharp tip is stimulated and the filament rapidly grows. Since the metal filament is conductive in nature, the degradation of the percolation path is extremely fast once the metal filament is formed (as shown in Fig. 6.19). It is therefore of great reliability concern for the MG/HK gate stacks as there is no margin to prolong the lifetime of the BD transistor. On the other hand, if I_g can be limited to $I_{gl} < 5 \mu\text{A}$ in this case, the ultrafast BD transient can be controlled.

6.5 Summary

In this chapter, we show that the formation of interfacial dipoles induces a flatband voltage shift for Ti-rich TiN_x metal gate. The percolation path in the SiON and HfSiON dielectrics with NiSi

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gate can be partially repaired by changing the local oxygen distribution and/or Ni metal filamentation. The post-BD reliability margin was considerably underestimated for such MG/HK systems. However for TaN metal gate on HK dielectrics, highly conductive metal filamentation can be formed under “high” current injections and shown to be the physical origin of the ultrafast post-BD degradation of the percolation path.

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CHAPTER SEVEN

IMPACT OF POST-BREAKDOWN PHYSICAL DEFECTS ON DEVICE PERFORMANCE

7.1 Summary of Post-BD Physical Defects and Their Impact on Device Performance

The degradation process of the percolation path shows distinct differences for various gate stacks. As summarized in Fig. 7.1, the conventional poly-Si/SiON gate stack depicts fast degradation at the initial stage of breakdown and progressive wear-out in the later stage. For fully silicided NiSi gate on HfSiO_x/SiO_x dielectrics, it follows the profile of the progressive degradation observed on poly-Si/SiON, but with gate leakage current I_g recoveries (shown as the current spiking). In contrast, the TaN metal gate on HfZrO₄/SiO_x dielectrics demonstrates fastest post-BD degradation with a very rapid current transient. It gives the shortest residual time and post-BD reliability margin as compared with the poly-Si/SiON and NiSi/HfSiO_x/SiO_x gate stacks. Hidden behind each of these unique dielectric failure mechanisms, there is a single or multiple physical defects associated with local structural change in the vicinity of the percolation path responsible for the specific electrical characteristics. As such, physical characterization is needed to identify various physical defects after the dielectric breakdown. With the additional information from the physical analysis, the degradation process of the gate dielectrics can be better understood and

modeled for a post-BD lifetime projection. In this chapter, the physical defects governing the degradation of the percolation path are summarized and discussed. Their impacts on the device reliability are also addressed.

Figure 7.1. Typical time evolutions of the gate leakage current I_g for poly-Si/SiON, NiSi/HfSiO_x/SiO_x and TaN/HfZrO₄/SiO_x gate stacks under constant voltage stress before and after the gate dielectric breakdown. Different percolation degradation profiles are clearly displayed for various gate stacks.

7.1.1 Role of Oxygen Vacancy

The oxygen vacancy and its related species are one of the common defects that can be found throughout the oxide wearing-out process, from stress induced leakage current [1, 2] to progressive breakdown [3]. Our experimental results show that oxygen deficiencies are the predominant physical defects in the percolation path for both poly-Si/SiON and metal-gate/high-

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κ gate stacks, especially when the leakage path is just formed. In the early stage of the post-BD, oxygen atoms are removed from the dielectric network, giving rise to digital fluctuations of the leakage current, such as the digital-BD in poly-Si/SiON gate stacks. The oxygen vacancy centers also serve as the prerequisite lattice sites for material migration from the adjacent gate or substrate electrodes. As a result of oxygen depletion in the percolation path, the local current density increases drastically and other physical defects like DBIE, DBIM can be subsequently formed. It is shown in Fig. 7.2 that the movement of the oxygen under substrate injection stress is towards the gate electrode for both poly-Si/SiON (Fig. 7.2(a)) and NiSi/HfSiO_x/SiO_x (Fig. 7.2(b)) gate stacks. It therefore poses an interesting question that can we put back the oxygen atoms into the percolated gate dielectrics by reversing the electrical bias? Based on our results, the percolation path formed in SiON or HK gate dielectrics can be “switched off” in the early stage of the post-BD, e.g., digital-BD and $I_{gl} < 2 \mu\text{A}$ for TaN/HK. Moreover, partial recoveries of post-BD conduction, both unipolar and bipolar recoveries, are observed on NiSi/SiON and NiSi/HfSiO_x/SiO_x gate stacks. It is believed that the oxygen stored in the gate electrode in the vicinity of the BD can diffuse back and passivate the percolation path under the correct biasing conditions. However, it is difficult to shut off the percolation path once other defects like DBIE protrusion or metal filamentation formed in the percolation path. In summary, oxygen vacancy is the universal defect type in various gate stack failures and it dominates the early stage of the post-BD.

Figure 7.2. (a) Relative compositions of Si and O across a 2-nm SiO_2 gate stack at the BD and Non-BD (as reference) locations. The positions of the profiles are aligned at the oxygen maximum for comparison purpose. (b) EELS elemental line profiles across a gate stack at the BD and non-BD locations. The O and Ni distributions are shown using O-K edge and Ni- $L_{2,3}$ edge EELS. The inset is the enlarged plot of the O profiles at the HK/NiSi interface.

7.1.2 Role of Si Epitaxy

The dielectric breakdown induced Si epitaxy was observed for both poly-Si/SiON and NiSi/HfSiO_x/SiO_x gate stacks. It is generally believed that the Si epitaxy is an irreversible physical defect (or extremely difficult to reverse it). As shown in Fig. 7.3(a), the oxygen is fully depleted at the inner core of the percolation path once the analog-BD is reached. In Fig. 7.3(b), an example of a Si nano-cluster at the BD location is captured in the TEM micrograph for an analog-BD sample. As introduced in Chapter 2, the DBIE is formed under high local temperature and current flux. It is a stable configuration which could sustain a large leakage current. The transformation from digital-BD to analog-BD is therefore irreversible once the conductive inner core of the percolation path transforms into a Si nano-cluster.

The impact of the Si epitaxy is also demonstrated on the NiSi/HfSiO_x/SiO_x gate stacks. As shown in Fig. 7.4, two nMOSFETs were failed under substrate injection stress with a compliance current limit $I_{gl} = 2 \mu\text{A}$ (Fig. 7.4(a)) and $I_{gl} = 500 \mu\text{A}$ (Fig. 7.4(b)). The gate leakage current of the two samples differs by 2 orders of magnitude. However, both samples show similar structural damage at the BD locations, where Si-DBIE and Ni-DBIM are found. As reported earlier by our group [4], the BD location or the position of a percolation path in the channel of a MOSFET has been found to be an important parameter in controlling the post-BD degradation. The degradation rate (dI_g/dt) of the percolation path depends strongly on the BD location, in which a BD MOSFET with an initial percolation path located near the center of the channel could have a dI_g/dt of 1-2 orders of magnitude smaller than that near the S/D [4].

(a)

(b)

Figure 7.3. (a) Box plot of the oxygen deficiency (as SiO_x) at the inner core of the percolation path for different current limited BDs. (b) TEM micrograph of a sample failed at $I_{gl} = 100\ \mu\text{A}$ at its BD location. Nano-size Si cluster was found.

Figure 7.4. TEM micrographs of two NiSi/HfSiON nMOSFETs failed under substrate injection stress for (a) $W \times L = 0.15 \times 0.15 \mu m^2$ with $I_{gl} = 2 \mu A$, and (b) $W \times L = 0.15 \times 0.50 \mu m^2$ with $I_{gl} = 500 \mu A$. The insets are the respective low magnification TEM micrographs.

The difference in the degradation rate for corner and channel BD is explained in the schematic diagram in Fig. 7.5. For a BD in the channel, there is a serial channel resistance R_{ch} which helps to limit the magnitude of the gate leakage current and degradation rate of the percolation path. In case of the corner BD, the percolation resistance R_{perc} is directly connected to the S/D terminal. As such, it leads to a fast degradation rate of the percolation resistance and easily evolves to a thermal runaway as shown in Fig. 7.4(a). It will be a serious problem for short channel transistors where the possibility of having a corner or near-corner BD increases significantly. Additionally, the formation and dilation process of the DBIE defect need to be clearly understood and addressed since it may eventually constrain the ultimate size of transistors due to the reliability limit.

Figure 7.5. Schematic representation showing the effect of percolation resistance R_{perc} , channel resistances R_{ch} and the BD location on dI_g/dt . [4]

7.1.3 Role of Metal Migration

Dielectric breakdown induced metal migration was discovered in poly-Si/SiON gate stacks for the first time, where the metal atoms from the S/D or gate silicide migrated into the percolation path, creating a low resistance path between the gate and S/D [5]. The DBIM defect is usually formed in the later stage of the progressive BD in poly-Si/SiON gate stacks when the leakage current reaches a high magnitude. Despite the fact that DBIM typically triggers the catastrophic failure of a transistor, our recent studies on the NiSi/HfSiO_x/SiO_x gate stacks show that DBIM could be a ‘useful’ defect for the recovery of the percolation conduction. Figure 7.6 shows the TEM micrographs of two post-BD NiSi/HfSiON nMOSFETs failed under substrate injection stress with $I_{gl} = 100 \mu\text{A}$ (Fig. 7.6(a)) and gate injection stress with $I_{gl} = 500\mu\text{A}$ (Fig. 7.6(b)). Both samples display I_g recoveries during the post-BD CVS stress as discussed in Fig. 7.1. The DBIM in the Si substrate, the HK gate dielectrics and the NiSi-gate effectively form a metal-insulator-metal (MIM) structure where the diffusion of oxygen and/or Ni filament formation could take place as reported in various resistive switching memory structures [6-8].

Figure 7.6. TEM micrographs of two post-BD NiSi/HfSiON nMOSFETs. (a) Substrate injection stress, $W \times L = 0.15 \times 0.50 \mu m^2$ with $I_{gl} = 100 \mu A$. (b) Gate injection stress, $W \times L = 0.15 \times 0.35 \mu m^2$ with $I_{gl} = 500 \mu A$. The insets are the respective low magnification TEM and/or HAADF micrographs.

7.1.4 Role of Metal Gate

The replacement of metal gate on high- κ dielectrics makes the further miniaturization of the MOSFETs possible and has also been adopted by the industry. However, the introduction of new materials in constructing the MOS transistor poses great reliability challenges. Some unique failure mechanisms associated with the MG/HK gate stacks have been identified recently [9, 10]. Among which the metal filamentation is one of the most undesirable defects since it gives rise to the ultrafast degradation of the percolation path (e.g., TaN/HfZrO₄/SiO_x in Fig. 7.1). Figure 7.7 shows the STEM-HAADF micrographs of the metal filamentation in both TaN gate (Fig. 7.7(a)) and NiSi gate (Fig. 7.7(b)).

Figure 7.7. (a) HAADF micrographs of a BD TaN/HfZrO₄/SiO_x sample ($W \times L = 0.15 \times 0.15 \mu\text{m}^2$) failed under substrate injection stress with $I_{gl} = 5 \mu\text{A}$. The Ta metal filamentation is found at the BD location $s = 0.51L$ (L is the effective channel length of a transistor). (b) HAADF micrographs of a BD NiSi/HfSiO_x/SiO_x sample ($W \times L = 0.15 \times 0.50 \mu\text{m}^2$) failed under substrate injection stress with $I_{gl} = 500 \mu\text{A}$. There is a Ni filament spiking through the gate dielectrics into the substrate at the BD location. The insets are the respective low magnification HAADF micrographs.

The migrations of Ta and Ni from the gate electrode into the percolation path are clearly displayed in Fig. 7.7, but with apparent differences in size and shape. The characteristics of the metal filament directly determine the conductivity of the percolation path and post-BD device reliability. Our recent study using atomistic simulation [11] shows that the band gaps of the HfO₂ dielectrics drops to 0 eV, 1.587 eV and 0.296 eV if one oxygen atom in a unit HfO₂ cell is replaced with Ta, Ni and Ti metal atom, respectively. This result correlates well with the experimental observation shown in Fig. 7.1 and Fig. 7.7 and the effect of the gate metal on device reliability is demonstrated. The TaN metal gate suffers most rapid post-BD I_g and gives

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the smallest post-BD reliability margin. On the other hand, the NiSi and TiN gates provide longer post-BD device lifetime even with metal filamentation (i.e., not as conductive as Ta filament). Moreover, partial recoveries of the percolation conduction are found for both NiSi and TiN gated MOSFETs. It is also worth noting that the metal filamentation depends on the polarity of the electrical stress. The formation of metal filament could be due to two driving forces: 1) electric field driven ionic conduction to cathode side for positively charged metal ions, and 2) electron wind force driven electromigration to anode side. It is an exception for Ta since it has the negative electromigration nature. Therefore, the Ta injection is only to the cathode side and the filament cannot be formed in the gate dielectrics for p-MOSFET under inversion mode conditions. For TaN gate, the conductive Ta filament can only be formed under substrate injection stress [10]. The nMOSFETs are severely affected under normal operation conditions (i.e., positive gate bias, substrate electron injection) while the pMOSFETs are excluded from the ultrafast degradation since they are operated under gate injection stress.

7.2 Summary

The physical defects associated with the dielectric breakdown are summarized and discussed in this chapter. As results of the applied electric stress and leakage current, physical and/or structural change like the modulation of oxygen distribution and various breakdown induced material migration from the adjacent electrodes are identified using physical analysis. Based on their respective roles in determining the device performance, the post-BD degradation of the percolation path shows progressive, partial recovery and ultrafast transient profiles for poly-

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Si/SiON, NiSi/HK and TaN/HK gate stacks. Physical characterization is shown to be very useful for identifying various physical defects in the vicinity of the broken down dielectrics.

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CHAPTER EIGHT

CONCLUSION AND RECOMMENDATION

8.1 Conclusion

This thesis introduces a series of characterization methodologies which bridge the microscopic properties of material changes with the macroscopic characteristics of a semiconductor device. The analyses of the MOSFET gate dielectric failure are used in this study as examples to demonstrate the advance of the nano-scale characterization. Using the nano-characterization techniques developed in this thesis, the mystery of the insulator-to-conductor transition occurred in a dielectric material upon stressing is revealed and various physical defects are identified to be impactful on device performance and reliability. The failure of the gate dielectrics in both conventional polycrystalline-silicon/silicon-oxynitride and new generation metal-gate/high- κ gate stacks have been studied electrically and physically. It is found that the oxygen deficiency is one of the fundamental physical defects responsible for the formation and early degradation of the percolation path in both SiON and HK gate dielectrics. In the later stage of the post-BD degradation, the electrical characteristics of the percolation path and device performances are dominated by other physical defects, such as the Si nano-clustering and metal filamentation. Their roles in determining the post-BD device reliability are addressed.

For conventional poly-Si/SiON gate stack, the oxygen deficiency in the percolated SiON is measured using electron energy loss spectroscopy and suggested to be the dominating defect

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responsible for the formation and evolution of the percolation path. The atomistic changes of the chemical bonding in the nano-scale breakdown path are extensive and irreversible. Oxygen atoms are washed-out with the formation of the intermediate bonding states of silicon (Si^{1+} , Si^{2+} , and Si^{3+}) in the percolation path. The distribution of the oxygen deficiency in the percolation path is non-uniform and spreads out radially from the center to surrounding areas. The conduction band edges of the defective oxide are lowered for 0.14 eV to 0.78 eV when the Si-O composition changes from $\text{SiO}_{1.76}$ to $\text{SiO}_{0.7}$. In addition, the percolation path contributes significantly to the random switching of current levels in the early stage of the progressive breakdown, which is also known as digital-breakdown. When the oxygen in the inner core of the percolation path is fully depleted, the defective oxide network transforms into a stable configuration and pushes the post-breakdown conduction to analog-breakdown where the random telegraphic noise of the gate leakage current is no longer visible easily.

The post-BD degradation of the percolation path strongly depends on the gate electrode, especially for metal gate stacks. For TaN/HfZrO₄/SiO_x gate stack under high current injections, Ta metal atoms from the gate electrode can migrate into the percolated HK dielectrics and form highly conductive filament. The metal filament induces an ultrafast post-breakdown degradation and significantly reduces the reliability margin of the transistor. On the other hand, the percolation path in the SiON and HK dielectrics can be partially repaired for using NiSi gated stacks. The dielectric breakdown induced metal migration constructs a metal-insulator-metal structure which facilitates the diffusion of oxygen vacancies and/or Ni metal filamentation in the vicinity of the percolation path under different biasing conditions. Moreover, the flatband voltage shift induced by varying metal gate Ti/N ratio is investigated. The interfacial dipoles formed at

the MG/HK and HK/interfacial-layer interfaces are identified to be responsible for the negative V_{FB} shift for sub-stoichiometric TiN_x gate.

8.2 Recommendation

We believe that this project could be further extended. Some of the possible directions for future investigations and studies are given as follows:

- The proposed methodologies, both electrical and physical characterizations, can be further applied to thoroughly analyze the gate dielectric failure in sub-45 nm MOSFETs, especially the new materials systems such as Al or La doped high- κ . New failure mechanisms and defects can be identified using the physical characterization techniques and correlate with the electrical characteristics of the device.
- The basic operation mechanism of the resistive switching random access memory (RRAM) is the switching between the insulating and conducting states of the dielectric material. There are several models proposed recently in attempts to describe the physical process of the switching. In general, oxygen ion and oxygen vacancy as well as metal filament play important roles in the switching mechanism of RRAM devices. But direct experimental evidences are still lacking. The characterization techniques introduced in this thesis can be implemented to unearth the physical origin of the switching mechanisms. Moreover, the reliability issues can be further studied since the working principle of the RRAM is a destructive process.
- Besides the electron microscopy, another group of physical characterization techniques, which are used to study the material properties at nanoscale, is the scanning probe

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microscopy including scanning tunneling microscopy, ballistic electron emission microscopy and conductive atomic force microscopy. The advance of the scanning probe technologies is that it can simultaneously access the structural and electrical properties of the material at a very fine spatial resolution. Therefore, it is worth to explore the possibility of correlating the SPM study with TEM and dielectric breakdown is one of the good examples to showcase the power of these two nano-characterization techniques.

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APPENDIX I: LOW LOSS CALCULATION

A.1 Sample Configuration and Theoretical Formulation

$\epsilon_0 = \text{Re_ep0} \pm j \text{Im_ep0} = (n_0^2 - k_0^2) \pm j (2n_0k_0)$	0		0
$\epsilon_1 = \text{Re_ep1} \pm j \text{Im_ep1} = (n_1^2 - k_1^2) \pm j (2n_1k_1)$	1		1
			2
			3
$\epsilon_2 = \text{Re_ep2} \pm j \text{Im_ep2} = (n_2^2 - k_2^2) \pm j (2n_2k_2)$	2		4

$$m = 1, n = 2m - 1 = 1$$

$$m = 2, n = 2m - 1 = 3$$

Consider a stratified slab which extends to infinity in the x- and y- directions and from $z = 0$ to $z = a$. The slab comprises n layers, labelled 1, 2, ..., n . The external regions, which need not be vacuum, are labelled 0 and $n+1$, in our case, is Si. Even if we have a slab that is symmetrical about its central layer, the energy loss function for parallel incidence does not simplify unless the beam is in the middle of the center layer. We consider a slab of $n = 2m - 1$ layers, symmetrical about the central m^{th} layer, with central beam. In this case, the energy-loss function then simplifies to

$$\chi_m^{2m+1} = \frac{1}{q_m \epsilon_m k^2} \left\{ \epsilon_m k_y^2 \frac{v^2}{c^2} \frac{\tilde{L}_{m-1,0}^+}{\tilde{L}_{m-1,0}^-} - q_m^2 \frac{L_{m-1,0}^-}{L_{m-1,0}^+} \right\}$$

$$\text{where } k^2 = k_x^2 + k_y^2 = \left(\frac{\omega}{v} \right)^2 + k_y^2, \quad q_m = \sqrt{\left(\frac{\omega}{v} \right)^2 + k_y^2 - \epsilon_m \frac{\omega^2}{c^2}}$$

We need to find the following expressions:

$$\begin{aligned} L_{m-1,0}^+ &= [C_{m-1,0}] f_m + [E_{m-1,0}] & L_{m-1,0}^- &= [C_{m-1,0}] f_m - [E_{m-1,0}] \\ \tilde{L}_{m-1,0}^+ &= [\tilde{C}_{m-1,0}] f_m + [\tilde{E}_{m-1,0}] & \tilde{L}_{m-1,0}^- &= [\tilde{C}_{m-1,0}] f_m - [\tilde{E}_{m-1,0}] \end{aligned}$$

Case I: m = 1

$$\chi_1^3 = \frac{1}{q_1 \epsilon_1 k^2} \left\{ \epsilon_1 k_y^2 \frac{v^2}{c^2} \frac{\tilde{L}_{0,0}^+}{\tilde{L}_{0,0}^-} - q_1^2 \frac{L_{0,0}^-}{L_{0,0}^+} \right\}$$

$$L_{0,0}^+ = [C_{0,0}] f_1 + [E_{0,0}], \quad L_{0,0}^- = [C_{0,0}] f_1 - [E_{0,0}]$$

$$\tilde{L}_{0,0}^+ = [\tilde{C}_{0,0}] f_1 + [\tilde{E}_{0,0}], \quad \tilde{L}_{0,0}^- = [\tilde{C}_{0,0}] f_1 - [\tilde{E}_{0,0}]$$

$$L_{0,0}^+ = [C_{0,0}] f_1 + [E_{0,0}]$$

$$= \text{Re_C00}[o] * \text{Re_fl}[o] - \text{Im_C00}[o] * \text{Im_fl}[o] + \text{Re_E00}[o]$$

$$+ j (\text{Re_C00}[o] * \text{Im_fl}[o] + \text{Im_C00}[o] * \text{Re_fl}[o] + \text{Im_E00}[o])$$

$$L_{0,0}^- = [C_{0,0}] f_1 - [E_{0,0}]$$

$$= \text{Re_C00}[o] * \text{Re_fl}[o] - \text{Im_C00}[o] * \text{Im_fl}[o] - \text{Re_E00}[o]$$

$$+ j (\text{Re_C00}[o] * \text{Im_fl}[o] + \text{Im_C00}[o] * \text{Re_fl}[o] - \text{Im_E00}[o])$$

$$\tilde{L}_{0,0}^+ = [\tilde{C}_{0,0}] f_1 + [\tilde{E}_{0,0}]$$

$$= \text{Re_tC00}[o] * \text{Re_fl}[o] - \text{Im_tC00}[o] * \text{Im_fl}[o] + \text{Re_tE00}[o]$$

$$+ j (\text{Re_tC00}[o] * \text{Im_fl}[o] + \text{Im_tC00}[o] * \text{Re_fl}[o] + \text{Im_tE00}[o])$$

$$\tilde{L}_{0,0}^- = [\tilde{C}_{0,0}] f_1 - [\tilde{E}_{0,0}]$$

$$= \text{Re_tC00}[o] * \text{Re_fl}[o] - \text{Im_tC00}[o] * \text{Im_fl}[o] - \text{tRe_E00}[o]$$

$$+ j (\text{Re_tC00}[o] * \text{Im_fl}[o] + \text{Im_tC00}[o] * \text{Re_fl}[o] - \text{tIm_E00}[o])$$

$$C_{ji} = h_{j+1,j}^+ f_j^2 \dots h_{i+1,i}^+ f_i^2 \quad \text{with } C_{ii} = h_{i+1,i}^+ f_i^2 \text{ and } C_{i,i+1} = 1$$

$$E_{ji} = h_{j+1,j}^- f_j^2 \dots h_{i+1,i}^+ f_i^2 \quad \text{with } E_{ii} = h_{i+1,i}^- f_i^2 \text{ and } E_{i,i+1} = 0$$

$$h_{ij}^\sigma = q_i \epsilon_j + \sigma q_j \epsilon_i \quad \tilde{h}_{ij}^\sigma = q_i + \sigma q_j$$

$f_j = e^{q_j a_j}$ with $f_0 = f_{n+1} = 1$ and a is j th layer thickness

$$\begin{aligned} f_1 &= e^{q_1 a_1} = \exp[a_1 (\text{Re}_- q_1 + j \text{Im}_- q_1)] \\ &= \exp[a_1 \text{Re}_- q_1] \exp[j a_1 \text{Im}_- q_1] \\ &= \exp[a_1 \text{Re}_- q_1] [\cos(a_1 \text{Im}_- q_1) + j \sin(a_1 \text{Im}_- q_1)] \\ &= \exp[a_1 \text{Re}_- q_1] \cos(a_1 \text{Im}_- q_1) + j \exp[a_1 \text{Re}_- q_1] \sin(a_1 \text{Im}_- q_1) \end{aligned}$$

$$\begin{aligned} [C_{0,0}] &= [h_{1,0}^+ f_0^2] = h_{1,0}^+ f_0^2 = q_1 \varepsilon_0 + q_0 \varepsilon_1 \\ &= (\text{Re}_- q_1 + j \text{Im}_- q_1)(\text{Re}_- \varepsilon_0 + j \text{Im}_- \varepsilon_0) + (\text{Re}_- q_0 + j \text{Im}_- q_0)(\text{Re}_- \varepsilon_1 + j \text{Im}_- \varepsilon_1) \\ &= (\text{Re}_- q_1 \text{Re}_- \varepsilon_0 - \text{Im}_- q_1 \text{Im}_- \varepsilon_0 + \text{Re}_- q_0 \text{Re}_- \varepsilon_1 - \text{Im}_- q_0 \text{Im}_- \varepsilon_1) \\ &\quad + j(\text{Re}_- q_1 \text{Im}_- \varepsilon_0 + \text{Im}_- q_1 \text{Re}_- \varepsilon_0 + \text{Re}_- q_0 \text{Im}_- \varepsilon_1 + \text{Im}_- q_0 \text{Re}_- \varepsilon_1) \\ &= \text{Re}_- q1[o] * \text{Re}_- ep0[o] - \text{Im}_- q1[o] * \text{Im}_- ep0[o] + \text{Re}_- q0[o] * \text{Re}_- ep1[o] - \text{Im}_- q0[o] * \\ &\quad \text{Im}_- ep1[o] + j (\text{Re}_- q1[o] * \text{Im}_- ep0[o] + \text{Im}_- q1[o] * \text{Re}_- ep0[o] + \text{Re}_- q0[o] * \text{Im}_- ep1[o] + \\ &\quad \text{Im}_- q0[o] * \text{Re}_- ep1[o]) \end{aligned}$$

$$\begin{aligned} [E_{0,0}] &= [h_{1,0}^- f_0^2] = h_{1,0}^- f_0^2 = q_1 \varepsilon_0 - q_0 \varepsilon_1 \\ &= (\text{Re}_- q_1 + j \text{Im}_- q_1)(\text{Re}_- \varepsilon_0 + j \text{Im}_- \varepsilon_0) - (\text{Re}_- q_0 + j \text{Im}_- q_0)(\text{Re}_- \varepsilon_1 + j \text{Im}_- \varepsilon_1) \\ &= (\text{Re}_- q_1 \text{Re}_- \varepsilon_0 - \text{Im}_- q_1 \text{Im}_- \varepsilon_0 - \text{Re}_- q_0 \text{Re}_- \varepsilon_1 + \text{Im}_- q_0 \text{Im}_- \varepsilon_1) \\ &\quad + j(\text{Re}_- q_1 \text{Im}_- \varepsilon_0 + \text{Im}_- q_1 \text{Re}_- \varepsilon_0 - \text{Re}_- q_0 \text{Im}_- \varepsilon_1 - \text{Im}_- q_0 \text{Re}_- \varepsilon_1) \\ &= \text{Re}_- q1[o] * \text{Re}_- ep0[o] - \text{Im}_- q1[o] * \text{Im}_- ep0[o] - \text{Re}_- q0[o] * \text{Re}_- ep1[o] + \text{Im}_- q0[o] * \\ &\quad \text{Im}_- ep1[o] + j (\text{Re}_- q1[o] * \text{Im}_- ep0[o] + \text{Im}_- q1[o] * \text{Re}_- ep0[o] - \text{Re}_- q0[o] * \text{Im}_- ep1[o] - \\ &\quad \text{Im}_- q0[o] * \text{Re}_- ep1[o]) \end{aligned}$$

$$\begin{aligned} [\tilde{C}_{0,0}] &= [\tilde{h}_{1,0}^+ f_0^2] = \tilde{h}_{1,0}^+ f_0^2 = q_1 + q_0 \\ &= \text{Re}_- q_1 + j \text{Im}_- q_1 + \text{Re}_- q_0 + j \text{Im}_- q_0 \\ &= (\text{Re}_- q_1 + \text{Re}_- q_0) + j (\text{Im}_- q_1 + \text{Im}_- q_0) \\ &= (\text{Re}_- q1[o] + \text{Re}_- q0[o]) + j (\text{Im}_- q1[o] + \text{Im}_- q0[o]) \end{aligned}$$

$$\begin{aligned} [\tilde{E}_{0,0}] &= [\tilde{h}_{1,0}^- f_0^2] = \tilde{h}_{1,0}^- f_0^2 = q_1 - q_0 \\ &= (\text{Re}_- q_1 + j \text{Im}_- q_1) - (\text{Re}_- q_0 + j \text{Im}_- q_0) \\ &= (\text{Re}_- q_1 - \text{Re}_- q_0) + j (\text{Im}_- q_1 - \text{Im}_- q_0) \\ &= (\text{Re}_- q1[o] - \text{Re}_- q0[o]) + j (\text{Im}_- q1[o] - \text{Im}_- q0[o]) \end{aligned}$$

$$\begin{aligned}
 \chi_1^3 &= \frac{1}{q_1 \varepsilon_1 k^2} \left\{ \varepsilon_1 k_y^2 \frac{v^2}{c^2} \frac{\tilde{L}_{0,0}^+}{\tilde{L}_{0,0}^-} - q_1^2 \frac{L_{0,0}^-}{L_{0,0}^+} \right\} = \frac{1}{T_1} \{ T_2 T_3 - q_1^2 T_4 \} \\
 &= \frac{1}{\text{Re_}T_1 + j \text{Im_}T_1} \{ [\text{Re_}T_2 + j \text{Im_}T_2][\text{Re_}T_3 + j \text{Im_}T_3] - [\text{Re_}sq1 + j \text{Im_}sq1][\text{Re_}T_4 + j \text{Im_}T_4] \} \\
 &= \frac{\text{Re_}T_1 - j \text{Im_}T_1}{\text{Re_}T_1^2 + \text{Im_}T_1^2} \times \left\{ (\text{Re_}T_2 \text{Re_}T_3 - \text{Im_}T_2 \text{Im_}T_3 - \text{Re_}sq1 \text{Re_}T_4 + \text{Im_}sq1 \text{Im_}T_4) \right. \\
 &\quad \left. + j(\text{Re_}T_2 \text{Im_}T_3 + \text{Im_}T_2 \text{Re_}T_3 - \text{Re_}sq1 \text{Im_}T_4 - \text{Im_}sq1 \text{Re_}T_4) \right\} \\
 &= \frac{\text{Re_}T_1 - j \text{Im_}T_1}{\text{Re_}T_1^2 + \text{Im_}T_1^2} \times (\text{Re_}T_5 + j \text{Im_}T_5) \\
 \therefore \text{Im}(\chi_1^3) &= \frac{\text{Re_}T_1 \text{Im_}T_5 - \text{Im_}T_1 \text{Re_}T_5}{\text{Re_}T_1^2 + \text{Im_}T_1^2}
 \end{aligned}$$

Where

$$\begin{aligned}
 T_1 &= q_1 \varepsilon_1 k^2 = (\text{Re_}q_1 + j \text{Im_}q_1)(\text{Re_}\varepsilon_1 + j \text{Im_}\varepsilon_1) k^2 = \text{pow}(k, 2.0) * (\text{Re_}q1[o] * \text{Re_}ep1[o] - \\
 &\text{Im_}q1[o] * \text{Im_}ep1[o]) + j \text{pow}(k, 2.0) * (\text{Re_}q1[o] * \text{Im_}ep1[o] + \text{Im_}q1[o] * \text{Re_}ep1[o])
 \end{aligned}$$

$$T_2 = \varepsilon_1 k_y^2 \frac{v^2}{c^2} = k_y^2 \frac{v^2}{c^2} (\text{Re_}\varepsilon_1 + j \text{Im_}\varepsilon_1)$$

$$\begin{aligned}
 T_3 &= \frac{\tilde{L}_{0,0}^+}{\tilde{L}_{0,0}^-} = \frac{\text{Re_}tL_{p00} + j \text{Im_}tL_{p00}}{\text{Re_}tL_{m00} + j \text{Im_}tL_{m00}} = \frac{(\text{Re_}tL_{p00} + j \text{Im_}tL_{p00})(\text{Re_}tL_{m00} - j \text{Im_}tL_{m00})}{(\text{Re_}tL_{m00} + j \text{Im_}tL_{m00})(\text{Re_}tL_{m00} - j \text{Im_}tL_{m00})} \\
 &= 1 / (\text{pow}(\text{Re_}tLm00[o], 2.0) + \text{pow}(\text{Im_}tLm00[o], 2.0)) * [(\text{Re_}tLp00[o] * \text{Re_}tLm00[o] + \\
 &\text{Im_}tLp00[o] * \text{Im_}tLm00[o]) + j (-\text{Re_}tLp00[o] * \text{Im_}tLm00[o] + \text{Im_}tLp00[o] * \text{Re_}tLm00[o])]
 \end{aligned}$$

$$\begin{aligned}
 T_4 &= \frac{L_{0,0}^-}{L_{0,0}^+} = \frac{\text{Re_}L_{m00} + j \text{Im_}L_{m00}}{\text{Re_}L_{p00} + j \text{Im_}L_{p00}} = \frac{(\text{Re_}L_{m00} + j \text{Im_}L_{m00})(\text{Re_}L_{p00} - j \text{Im_}L_{p00})}{(\text{Re_}L_{p00} + j \text{Im_}L_{p00})(\text{Re_}L_{p00} - j \text{Im_}L_{p00})} \\
 &= 1 / (\text{pow}(\text{Re_}Lp00[o], 2.0) + \text{pow}(\text{Im_}Lp00[o], 2.0)) * \\
 &[(\text{Re_}Lm00[o] * \text{Re_}Lp00[o] + \text{Im_}Lm00[o] * \text{Im_}Lp00[o]) + j (-\text{Re_}Lm00[o] * \text{Im_}Lp00[o] + \\
 &\text{Im_}Lm00[o] * \text{Re_}Lp00[o])]
 \end{aligned}$$

$$\begin{aligned}
 T_5 &= (\text{Re_}T_2 \text{Re_}T_3 - \text{Im_}T_2 \text{Im_}T_3 - \text{Re_}sq1 \text{Re_}T_4 + \text{Im_}sq1 \text{Im_}T_4) \\
 &+ j(\text{Re_}T_2 \text{Im_}T_3 + \text{Im_}T_2 \text{Re_}T_3 - \text{Re_}sq1 \text{Im_}T_4 - \text{Im_}sq1 \text{Re_}T_4)
 \end{aligned}$$

$$= \text{Re_T2[o]} * \text{Re_T3[o]} - \text{Im_T2[o]} * \text{Im_T3[o]} - \text{Re_sq1[o]} * \text{Re_T4[o]} + \text{Im_sq1[o]} * \text{Im_T4[o]} + j (\text{Re_T2[o]} * \text{Im_T3[o]} + \text{Im_T2[o]} * \text{Re_T3[o]} - \text{Re_sq1[o]} * \text{Im_T4[o]} - \text{Im_sq1[o]} * \text{Re_T4[o]})$$

Case II: m = 2

$$\chi_2^5 = \frac{1}{q_2 \epsilon_2 k^2} \left\{ \epsilon_2 k_y^2 \frac{v^2}{c^2} \frac{\tilde{L}_{1,0}^+}{\tilde{L}_{1,0}^-} - q_2^2 \frac{L_{1,0}^-}{L_{1,0}^+} \right\}$$

$$\begin{aligned} L_{1,0}^+ &= [C_{1,0}]f_2 + [E_{1,0}] & L_{1,0}^- &= [C_{1,0}]f_2 - [E_{1,0}] \\ \tilde{L}_{1,0}^+ &= [\tilde{C}_{1,0}]f_2 + [\tilde{E}_{1,0}] & \tilde{L}_{1,0}^- &= [\tilde{C}_{1,0}]f_2 - [\tilde{E}_{1,0}] \end{aligned}$$

$$C_{ji} = h_{j+1,j}^+ f_j^2 \dots h_{i+1,i}^+ f_i^2 \quad \text{with } C_{ii} = h_{i+1,i}^+ f_i^2 \text{ and } C_{i,i+1} = 1$$

$$E_{ji} = h_{j+1,j}^- f_j^2 \dots h_{i+1,i}^+ f_i^2 \quad \text{with } E_{ii} = h_{i+1,i}^- f_i^2 \text{ and } E_{i,i+1} = 0$$

$$h_{ij}^\sigma = q_i \epsilon_j + \sigma q_j \epsilon_i \quad \tilde{h}_{ij}^\sigma = q_i + \sigma q_j$$

$$f_j = e^{q_j a_j} \quad \text{with } f_0 = f_{n+1} = 1 \quad a \text{ is } j\text{th layer thickness}$$

$$\begin{aligned} f_1 &= e^{q_1 a_1} = \exp[a_1 (\text{Re_} q_1 + j \text{Im_} q_1)] \\ &= \exp[a_1 \text{Re_} q_1] \cos(a_1 \text{Im_} q_1) + j \exp[a_1 \text{Re_} q_1] \sin(a_1 \text{Im_} q_1) \end{aligned}$$

$$f_1^2 = \exp(2*a1*\text{Re_}q1[o])* \cos(2*a1*\text{Im_}q1[o]) + j \exp(2*a1*\text{Re_}q1[o])* \sin(2*a1*\text{Im_}q1[o])$$

$$\begin{aligned} f_2 &= e^{q_2 a_2} = \exp[a_2 (\text{Re_} q_2 + j \text{Im_} q_2)] \\ &= \exp[a_2 \text{Re_} q_2] \cos(a_2 \text{Im_} q_2) + j \exp[a_2 \text{Re_} q_2] \sin(a_2 \text{Im_} q_2) \end{aligned}$$

$$f_2^2 = \exp(2*a2*\text{Re_}q2[o])* \cos(2*a2*\text{Im_}q2[o]) + j \exp(2*a2*\text{Re_}q2[o])* \sin(2*a2*\text{Im_}q2[o])$$

$$[C_{1,0}] = [h_{2,1}^+ f_1^2 h_{1,0}^+ f_0^2] = h_{2,1}^+ f_1^2 h_{1,0}^+ + h_{2,1}^- h_{1,0}^-$$

$$\begin{aligned} &= (\text{Re_hp21[o]} * \text{Re_sf1[o]} - \text{Im_hp21[o]} * \text{Im_sf1[o]}) * \text{Re_hp10[o]} - (\text{Re_hp21[o]} * \text{Im_sf1[o]} \\ &+ \text{Im_hp21[o]} * \text{Re_sf1[o]}) * \text{Im_hp10[o]} + \text{Re_hm21[o]} * \text{Re_hm10[o]} - \text{Im_hm21[o]} * \end{aligned}$$

$$\begin{aligned} & \text{Im_hm10[o]} + j \{ (\text{Re_hp21[o]} * \text{Re_sf1[o]} - \text{Im_hp21[o]} * \text{Im_sf1[o]}) * \text{Im_hp10[o]} + \\ & (\text{Re_hp21[o]} * \text{Im_sf1[o]} + \text{Im_hp21[o]} * \text{Re_sf1[o]}) * \text{Re_hp10[o]} + \text{Re_hm21[o]} * \text{Im_hm10[o]} \\ & + \text{Im_hm21[o]} * \text{Re_hm10[o]} \} \end{aligned}$$

$$\begin{aligned} \left[E_{1,0} \right] &= \left[h_{2,1}^- f_1^2 h_{1,0}^+ f_0^2 \right] = h_{2,1}^- f_1^2 h_{1,0}^+ + h_{2,1}^+ h_{1,0}^- \\ &= (\text{Re_hm21[o]} * \text{Re_sf1[o]} - \text{Im_hm21[o]} * \text{Im_sf1[o]}) * \text{Re_hp10[o]} - (\text{Re_hm21[o]} * \\ & \text{Im_sf1[o]} + \text{Im_hm21[o]} * \text{Re_sf1[o]}) * \text{Im_hp10[o]} + \text{Re_hp21[o]} * \text{Re_hm10[o]} - \text{Im_hp21[o]} \\ & * \text{Im_hm10[o]} + j \{ (\text{Re_hm21[o]} * \text{Re_sf1[o]} - \text{Im_hm21[o]} * \text{Im_sf1[o]}) * \text{Im_hp10[o]} + \\ & (\text{Re_hm21[o]} * \text{Im_sf1[o]} + \text{Im_hm21[o]} * \text{Re_sf1[o]}) * \text{Re_hp10[o]} + \text{Re_hp21[o]} * \\ & \text{Im_hm10[o]} + \text{Im_hp21[o]} * \text{Re_hm10[o]} \} \end{aligned}$$

$$h_{2,1}^+ = q_2 \mathcal{E}_1 + q_1 \mathcal{E}_2$$

$$\begin{aligned} &= \text{Re_q2[o]} * \text{Re_ep1[o]} - \text{Im_q2[o]} * \text{Im_ep1[o]} + \text{Re_q1[o]} * \text{Re_ep2[o]} - \text{Im_q1[o]} * \\ & \text{Im_ep2[o]} + j (\text{Re_q2[o]} * \text{Im_ep1[o]} + \text{Im_q2[o]} * \text{Re_ep1[o]} + \text{Re_q1[o]} * \text{Im_ep2[o]} + \\ & \text{Im_q1[o]} * \text{Re_ep2[o]}) \end{aligned}$$

$$h_{1,0}^+ = q_1 \mathcal{E}_0 + q_0 \mathcal{E}_1$$

$$\begin{aligned} &= \text{Re_q1[o]} * \text{Re_ep0[o]} - \text{Im_q1[o]} * \text{Im_ep0[o]} + \text{Re_q0[o]} * \text{Re_ep1[o]} - \text{Im_q0[o]} * \\ & \text{Im_ep1[o]} + j (\text{Re_q1[o]} * \text{Im_ep0[o]} + \text{Im_q1[o]} * \text{Re_ep0[o]} + \text{Re_q0[o]} * \text{Im_ep1[o]} + \\ & \text{Im_q0[o]} * \text{Re_ep1[o]}) \end{aligned}$$

$$h_{2,1}^- = q_2 \mathcal{E}_1 - q_1 \mathcal{E}_2$$

$$\begin{aligned} &= \text{Re_q2[o]} * \text{Re_ep1[o]} - \text{Im_q2[o]} * \text{Im_ep1[o]} - \text{Re_q1[o]} * \text{Re_ep2[o]} + \text{Im_q1[o]} * \\ & \text{Im_ep2[o]} + j (\text{Re_q2[o]} * \text{Im_ep1[o]} + \text{Im_q2[o]} * \text{Re_ep1[o]} - \text{Re_q1[o]} * \text{Im_ep2[o]} - \\ & \text{Im_q1[o]} * \text{Re_ep2[o]}) \end{aligned}$$

$$h_{1,0}^- = q_1 \mathcal{E}_0 - q_0 \mathcal{E}_1$$

$$= \text{Re_q1}[o] * \text{Re_ep0}[o] - \text{Im_q1}[o] * \text{Im_ep0}[o] - \text{Re_q0}[o] * \text{Re_ep1}[o] + \text{Im_q0}[o] * \text{Im_ep1}[o] + j (\text{Re_q1}[o] * \text{Im_ep0}[o] + \text{Im_q1}[o] * \text{Re_ep0}[o] - \text{Re_q0}[o] * \text{Im_ep1}[o] - \text{Im_q0}[o] * \text{Re_ep1}[o])$$

$$\left[\tilde{C}_{1,0} \right] = \left[\tilde{h}_{2,1}^+ f_1^2 \tilde{h}_{1,0}^+ f_0^2 \right] = \tilde{h}_{2,1}^+ f_1^2 \tilde{h}_{1,0}^+ + \tilde{h}_{2,1}^- \tilde{h}_{1,0}^-$$

$$= (\text{Re_thp21}[o] * \text{Re_sfl}[o] - \text{Im_thp21}[o] * \text{Im_sfl}[o]) * \text{Re_thp10}[o] - (\text{Re_thp21}[o] * \text{Im_sfl}[o] + \text{Im_thp21}[o] * \text{Re_sfl}[o]) * \text{Im_thp10}[o] + \text{Re_thm21}[o] * \text{Re_thm10}[o] - \text{Im_thm21}[o] * \text{Im_thm10}[o] + j \{ (\text{Re_thp21}[o] * \text{Re_sfl}[o] - \text{Im_thp21}[o] * \text{Im_sfl}[o]) * \text{Im_thp10}[o] + (\text{Re_thp21}[o] * \text{Im_sfl}[o] + \text{Im_thp21}[o] * \text{Re_sfl}[o]) * \text{Re_thp10}[o] + \text{Re_thm21}[o] * \text{Im_thm10}[o] + \text{Im_thm21}[o] * \text{Re_thm10}[o] \}$$

$$\left[\tilde{E}_{1,0} \right] = \left[\tilde{h}_{2,1}^- f_1^2 \tilde{h}_{1,0}^+ f_0^2 \right] = \tilde{h}_{2,1}^- f_1^2 \tilde{h}_{1,0}^+ + \tilde{h}_{2,1}^+ \tilde{h}_{1,0}^-$$

$$= (\text{Re_thm21}[o] * \text{Re_sfl}[o] - \text{Im_thm21}[o] * \text{Im_sfl}[o]) * \text{Re_thp10}[o] - (\text{Re_thm21}[o] * \text{Im_sfl}[o] + \text{Im_thm21}[o] * \text{Re_sfl}[o]) * \text{Im_thp10}[o] + \text{Re_thp21}[o] * \text{Re_thm10}[o] - \text{Im_thp21}[o] * \text{Im_thm10}[o] + j \{ (\text{Re_thm21}[o] * \text{Re_sfl}[o] - \text{Im_thm21}[o] * \text{Im_sfl}[o]) * \text{Im_thp10}[o] + (\text{Re_thm21}[o] * \text{Im_sfl}[o] + \text{Im_thm21}[o] * \text{Re_sfl}[o]) * \text{Re_thp10}[o] + \text{Re_thp21}[o] * \text{Im_thm10}[o] + \text{Im_thp21}[o] * \text{Re_thm10}[o] \}$$

$$\tilde{h}_{2,1}^+ = q_2 + q_1 = (\text{Re_q2}[o] + \text{Re_q1}[o]) + j (\text{Im_q2}[o] + \text{Im_q1}[o])$$

$$\tilde{h}_{1,0}^+ = q_1 + q_0 = (\text{Re_q1}[o] + \text{Re_q0}[o]) + j (\text{Im_q1}[o] + \text{Im_q0}[o])$$

$$\tilde{h}_{2,1}^- = q_2 - q_1 = (\text{Re_q2}[o] - \text{Re_q1}[o]) + j (\text{Im_q2}[o] - \text{Im_q1}[o])$$

$$\tilde{h}_{1,0}^- = q_1 - q_0 = (\text{Re_q1}[o] - \text{Re_q0}[o]) + j (\text{Im_q1}[o] - \text{Im_q0}[o])$$

A.2 C-programming Code

```
//This program is for m = 1 system: Si / SiO2 / Si    or    Si / SiO / Si
//The layer of slab is n = 2m - 1 = 1
//The total layer number including the bulk = 2m + 1 = 3
//The layer number is j = 0, 1, 2, where the properties of 0 and 2 are same

#include <iostream>
#include <fstream>
#include <iomanip>
#include <cmath>
#include <math.h>
#include <vector>
#include <stdio.h>
#include <stdlib.h>
using namespace std;

const double pi                = 3.14159265;
const double epsilon0         = 8.85*1.0e-12;           //permittivity of free space
const double m0               = 9.10956*1.0e-31;        //electron rest mass in unit of kg
const double e                = 1.6*1.0e-19;           //elementary charge
const double h_bar            = 1.0545715*1.0e-34;      //Planck's constant
const double ky_limit = 15*1.0e9;                       //the limit for integration over delta_ky
const double delta_ky = 0.001*1.0e9;                   //the increment for integration over delta_ky
const double Eeff = 64.5*1.0e3;                         //the effective kinetic energy with relativistic effect
const double LightSpeed = 3.0 * 1.0e8;                 //the speed of light
const double a = 2 * 1.0e-9;                           //the thickness of the slab of n layer
const int OmegaNumber0 = 350;
const int OmegaNumber1 = 246;

int main()
{
    FILE *outfile1;
    outfile1=fopen("m=1_n=1_a=2nm_E0=80keV_Si(1)_SiO2(0).dat","w");
    if(outfile1==NULL){
        cout<<"Error!cannot open file m=1.dat\n";
        exit(1);
    }
}
```

```

        ifstream inputFile0;
inputFile0.open("Si.dat");
if (!inputFile0) cout << "Error opening file!" << endl;
        ifstream inputFile1;
inputFile1.open("SiO2.dat");
if (!inputFile1) cout << "Error opening file!" << endl;

        /*-----To read in the Omega, n and k for layer 0, 1, 2-----*/
        vector< vector< double > >      Read0(      OmegaNumber0+1,      vector<double>(3,
0)),Read1( OmegaNumber1+1, vector<double>(3, 0));
        int j,i,o,p;
        vector<double>
Omega(OmegaNumber1+1),n0(OmegaNumber1+1),k0(OmegaNumber1+1),n1(OmegaNumber1+1),k1(OmegaNum
ber1+1), ntemp(OmegaNumber1+1),ktemp(OmegaNumber1+1);

//Step 1: read in the matrix
for(j=0; j<=OmegaNumber0;    j++){
        for(i=0; i<=2;    i++){
                inputFile0 >> Read0[j][i];
        }
}
for(j=0; j<=OmegaNumber1;    j++){
        for(i=0; i<=2;    i++){
                inputFile1 >> Read1[j][i];
        }
}

//Step 2: separate the matrix into vectors
for(o=0; o<=OmegaNumber1;    o++){
        Omega[o] = 2.0 * pi * LightSpeed / (Read1[o][0] * 1.0e-10);
        for(p=0; p<=OmegaNumber0;    p++){
                if(Read0[p][0] >= Read1[o][0]) break;
        }
n0[o] = Read0[p][1] - (Read0[p][1]-Read0[p-1][1]) / (Read0[p][0]-Read0[p-1][0]) * (Read0[p][0]-Read1[o][0]);
k0[o] = Read0[p][2] - (Read0[p][2]-Read0[p-1][2]) / (Read0[p][0]-Read0[p-1][0]) * (Read0[p][0]-Read1[o][0]);
n1[o] = Read1[o][1];

```

```

        k1[o] = Read1[o][2];
        //fprintf(outfile1, "%e\t%e\t%e\t%e\t%e\n", Omega[o], n0[o], k0[o], n1[o], k1[o]);
    }

//step 3: swap layer 1 and layer 0 --> now layer 0 = SiO2 and layer 1 = Si
for(o=0; o<=OmegaNumber1; o++){
    ntemp[o]=n1[o];      ktemp[o]=k1[o];
    n1[o]=n0[o];         k1[o]=k0[o];
    n0[o]=ntemp[o];      k0[o]=ktemp[o];
    cout<<Omega[o]<<"\t"<<n0[o]<<"\t"<<k0[o]<<"\t"<<n1[o]<<"\t"<<k1[o]<<"\n";
}
getchar();

/*-----To define the parameters for calculation the loss function-----*/
double a1;           //the thickness of center layer 1
a1 = a;
double speed;        //the speed of the incident electrons
speed = sqrt(2.0*Eeff*e/m0);
double ky;
vector <double> kx(OmegaNumber1+1), F(OmegaNumber1+1),
//layer 0
Re_ep0(OmegaNumber1+1), Im_ep0(OmegaNumber1+1),           //complex dielectric constant 0
Re_sq0(OmegaNumber1+1), Im_sq0(OmegaNumber1+1),           //complex square of q0
Re_q0(OmegaNumber1+1), Im_q0(OmegaNumber1+1),              //complex q0
Re_f0(OmegaNumber1+1), Im_f0(OmegaNumber1+1),              //complex f0
//layer 1
Re_ep1(OmegaNumber1+1), Im_ep1(OmegaNumber1+1),           //complex dielectric constant 1
Re_sq1(OmegaNumber1+1), Im_sq1(OmegaNumber1+1),           //complex square of q1
Re_q1(OmegaNumber1+1), Im_q1(OmegaNumber1+1),              //complex q1
Re_f1(OmegaNumber1+1), Im_f1(OmegaNumber1+1),              //complex f1
//interaction terms
Re_C00(OmegaNumber1+1), Im_C00(OmegaNumber1+1),           //C00
Re_E00(OmegaNumber1+1), Im_E00(OmegaNumber1+1),           //E00
Re_tC00(OmegaNumber1+1), Im_tC00(OmegaNumber1+1),         //tilde C00
Re_tE00(OmegaNumber1+1), Im_tE00(OmegaNumber1+1),         //tilde E00

Re_Lp00(OmegaNumber1+1), Im_Lp00(OmegaNumber1+1),         //Lp00

```

```

Re_Lm00(OmegaNumber1+1),Im_Lm00(OmegaNumber1+1),          //Lm00
Re_tLp00(OmegaNumber1+1),Im_tLp00(OmegaNumber1+1),        //tilde Lp00
Re_tLm00(OmegaNumber1+1),Im_tLm00(OmegaNumber1+1),        //tilde Lm00

Re_T1(OmegaNumber1+1),Im_T1(OmegaNumber1+1),              //Term 1 of LossFunction
Re_T2(OmegaNumber1+1),Im_T2(OmegaNumber1+1),              //Term 2 of LossFunction
Re_T3(OmegaNumber1+1),Im_T3(OmegaNumber1+1),              //Term 3 of LossFunction
Re_T4(OmegaNumber1+1),Im_T4(OmegaNumber1+1),              //Term 4 of LossFunction
Re_T5(OmegaNumber1+1),Im_T5(OmegaNumber1+1),              //Term 5 of LossFunction

Im_LossFunc(OmegaNumber1+1);

/*-----First loop: for one value of Omega-----*/
for(o=0; o<=OmegaNumber1;    o++){
    F[o] = 0;kx[o] = Omega[o] / speed;
    Re_ep0[o] = pow(n0[o],2.0)-pow(k0[o],2.0);
    Im_ep0[o] = 2.0*n0[o]*k0[o];

    Re_ep1[o] = pow(n1[o],2.0)-pow(k1[o],2.0);
    Im_ep1[o] = 2.0*n1[o]*k1[o];

    /*-----Second loop: for one value of ky-----*/
    for(ky=0;        ky<=ky_limit;    ky+=delta_ky){

        //step 1: expression for q0 and q1
        Re_sq0[o] = pow(ky,2.0)+pow(kx[o],2.0)-Re_ep0[o]*pow(Omega[o]/LightSpeed,2.0);
        Im_sq0[o] = Im_ep0[o]*pow(Omega[o]/LightSpeed,2.0);
        Re_q0[o] = sqrt( ( Re_sq0[o]+sqrt(pow(Re_sq0[o],2.0)+pow(Im_sq0[o],2.0)) ) / 2.0 );
        Im_q0[o] = sqrt( ( -Re_sq0[o]+sqrt(pow(Re_sq0[o],2.0)+pow(Im_sq0[o],2.0)) ) / 2.0 );

        Re_sq1[o] = pow(ky,2.0)+pow(kx[o],2.0)-Re_ep1[o]*pow(Omega[o]/LightSpeed,2.0);
        Im_sq1[o] = Im_ep1[o]*pow(Omega[o]/LightSpeed,2.0);
        Re_q1[o] = sqrt( ( Re_sq1[o]+sqrt(pow(Re_sq1[o],2.0)+pow(Im_sq1[o],2.0)) ) / 2.0 );
        Im_q1[o] = sqrt( ( -Re_sq1[o]+sqrt(pow(Re_sq1[o],2.0)+pow(Im_sq1[o],2.0)) ) / 2.0 );

        //step 2: expression for f0 and f1

```

```

Re_f0[o] = 1;
Im_f0[o] = 0;

Re_fl[o] = exp(a1*Re_q1[o])*cos(a1*Im_q1[o]);
Im_fl[o] = exp(a1*Re_q1[o])*sin(a1*Im_q1[o]);

//step 3: expression for C00, tC00 and E00, tE00
//C00
Re_C00[o] = Re_q1[o] * Re_ep0[o] - Im_q1[o] * Im_ep0[o] + Re_q0[o] * Re_ep1[o] - Im_q0[o] * Im_ep1[o];
Im_C00[o] = Re_q1[o] * Im_ep0[o] + Im_q1[o] * Re_ep0[o] + Re_q0[o] * Im_ep1[o] + Im_q0[o] * Re_ep1[o];
//E00
Re_E00[o] = Re_q1[o] * Re_ep0[o] - Im_q1[o] * Im_ep0[o] - Re_q0[o] * Re_ep1[o] + Im_q0[o] * Im_ep1[o];
Im_E00[o] = Re_q1[o] * Im_ep0[o] + Im_q1[o] * Re_ep0[o] - Re_q0[o] * Im_ep1[o] - Im_q0[o] * Re_ep1[o];
//tilde C00
Re_tC00[o] = Re_q1[o] + Re_q0[o];
Im_tC00[o] = Im_q1[o] + Im_q0[o];
//tilde E00
Re_tE00[o] = Re_q1[o] - Re_q0[o];
Im_tE00[o] = Im_q1[o] - Im_q0[o];

//step 4: expression for Lp00, Lm00, tLp00, tLm00
//Lp00
Re_Lp00[o] = Re_C00[o] * Re_fl[o] - Im_C00[o] * Im_fl[o] + Re_E00[o];
Im_Lp00[o] = Re_C00[o] * Im_fl[o] + Im_C00[o] * Re_fl[o] + Im_E00[o];
//Lm00
Re_Lm00[o] = Re_C00[o] * Re_fl[o] - Im_C00[o] * Im_fl[o] - Re_E00[o];
Im_Lm00[o] = Re_C00[o] * Im_fl[o] + Im_C00[o] * Re_fl[o] - Im_E00[o];
//tilde Lp00
Re_tLp00[o] = Re_tC00[o] * Re_fl[o] - Im_tC00[o] * Im_fl[o] + Re_tE00[o];
Im_tLp00[o] = Re_tC00[o] * Im_fl[o] + Im_tC00[o] * Re_fl[o] + Im_tE00[o];
//tilde Lm00
Re_tLm00[o] = Re_tC00[o] * Re_fl[o] - Im_tC00[o] * Im_fl[o] - Re_tE00[o];
Im_tLm00[o] = Re_tC00[o] * Im_fl[o] + Im_tC00[o] * Re_fl[o] - Im_tE00[o];

//step 5: calculate Im_LossFunc
Re_T1[o] = (pow(kx[o],2.0)+pow(ky,2.0)) * (Re_q1[o] * Re_ep1[o] - Im_q1[o] * Im_ep1[o]) ;
Im_T1[o] = (pow(kx[o],2.0)+pow(ky,2.0)) * (Re_q1[o] * Im_ep1[o] + Im_q1[o] * Re_ep1[o]);

```


APPENDIX II: MULTIPLE BREAKDOWNS

A.3 Electrical Characterization

Along with the physical studies of defects formed in the post-breakdown degradation process [1-8], there are interesting findings such as oxygen vacancy formation [7-8], dielectric breakdown induced epitaxy [2-4] and metal migration [5] as well as other structural damages associated with BD [1, 5-6] ranging from soft-BD (or progressive-BD) to hard-BD. Devices suffering from dielectric breakdown often experience partial or total malfunctioning of their electrical characteristics [9]. Despite all the unfavorable consequences of the BD, there are cases of “super-reliable” transistors which remain functional even with HBD damages. In this appendix, one example is shown and discussed.

The device used here was an nMOS ($W \times L = 0.15 \times 0.35 \mu\text{m}^2$) transistor. A 2-step constant voltage stress was performed to create the BD in the 22 Å SiON gate dielectric. As shown in Fig. 1(a), the stressing voltage $V_{\text{gstress}} = 4.2 \text{ V}$ (step 1) and 3.3 V (step 2) with current compliances $I_{\text{gl}} = 1 \mu\text{A}$ (step 1) and 10-180 μA (step 2) were used, respectively. The BD spot evolved to a severe SBD at 180 μA before HBD was reached. Fig. 1(b) shows the corresponding BD location measurements [10] along the effective channel length L in both inversion and accumulation mode during and after each post-BD stress. It indicates one single BD location at $0.39L$ (Inv) and $0.23L$ (Acc), which is nearer to the source terminal.

Fig. 1 (a) Gate leakage current I_g profile of an nMOS (22 Å SiON and $W \times L = 0.15 \times 0.35 \mu\text{m}^2$) stressed using a 2-step CVS. Step-1: $V_{g\text{stress}} = 4.2\text{ V}$ & $I_{gl} = 1\mu\text{A}$. Step-2: $V_{g\text{stress}} = 3.3\text{ V}$ & I_{gl} relaxed from $10\mu\text{A}$ to $180\mu\text{A}$. (b) Inversion (Inv) and accumulation (Acc) BD location measurements during and after each post-BD stress. The BD is located at $0.39L$ (Inv) and $0.23L$ (Acc) away from the source terminal.

The post-BD electrical characteristics of the device are shown in Fig. 2. The gate leakage current I_g (Fig. 2(a)) degrades by 3 orders of magnitude, e.g. from 18 nA to $1.7\mu\text{A}$ at $V_g = 1.5\text{ V}$. The channel drive current also degrades as shown in the I_D - V_D and I_S - V_S plots in Figs. 2(b) & 2(c). At this stage, it is clear that the device still maintains its transistor characteristics but with degraded drive current and gate leakages. However, this degraded performance looks not acceptable after the physical analysis.

Fig. 2 (a) Pre- and post-BD ($I_{gl} = 1, 50$ & $180 \mu A$) gate leakage I_g - V_g plot, the gate leakage increases by 3 orders of magnitude after BD. (b) & (c) Pre- and post-BD ($I_{gl} = 180 \mu A$) I_d - V_d and I_s - V_s plots of the device. The drive current degrades from $56 \mu A$ to $28 \mu A$ at $V_g = 1.5 V$.

A.4 Physical Characterization

Subsequently, the BD transistor was isolated and thinned down using focused ion beam milling. The transmission electron microscopy analysis results are shown in Fig. 3. The low-magnification bright field TEM micrographs (Figs. 3(a) & 3(b)) show two BD spots; the primary one (BD-1) is located near source terminal ($\sim 0.23L$) and the other (BD-2) is located at the edge of the gate near the drain terminal.

The high resolution TEM images of the two BD spots are shown in Figs. 3(c) & 3(d), respectively. For BD spot 1, the circular-shaped burnt mark is filled with amorphous material where the contact region between the BD and Si/poly-Si consists of Si crystal defects [4]. The oxide layer is completely ruptured after the local intermixing induced by the BD event. BD spot 2 is found at the gate edge (i.e., corner-BD) with a partial Si amorphization in the gate and a relatively clear oxide layer. The structural damage also shows a circular shape centered at the oxide layer but with a less extent of damage than that of BD spot 1. The circular-shaped BD spots are believed to be driven by the thermal gradient during a high temperature melting. It shows how much massive energy can be created by the BD which then dissipates the heat in the vicinity of the oxide. It is very rare to see multiple BD spots in such a small dimension ($0.15 \times 0.35 \mu\text{m}^2$). Please note that BD spot 2 is not measurable in the BD location measurements in Fig. 1(b). Furthermore, the defect does not create a short between the gate and the drain terminal as reflected from the drain current (Fig. 2(b)). It is believed that the oxide associated with BD-2 is still intact and maintains insulating properties as shown in Fig. 3(d), where no punch through or direct contacting is found. Since the size and damage of BD-2 are much softer than BD-1, the leakage profile in this case is dominated by BD-1 (as measured in Figs. 1(b) & 2(a)). But how can a device with such severe damage i.e., BD-1 still maintain its transistor characteristics?

Fig. 3 (a) & (b) Low-magnification TEM images of the BD device where 2 BD spots are found. BD-1 locates at $\sim 0.23L$ from the source terminal while BD-2 is at gate edge near the drain terminal. (c) & (d) HRTEM of BD-1 & BD-2, respectively. Circular shaped burnt marks are found to be Si amorphization and other Si defects [4].

The answers are found in Fig. 4 where N, O, Co and Si elemental mappings are shown. The gate is defined by the Si_3N_4 spacer capping (Fig. 4(a)) and Co migration is found at the drain side (BD-2) from the gate silicide to LDD along the gate/spacer sidewall or interface [5]. However, this DBIM did not give rise to a very low resistance path between the gate and drain terminal, and only contributed to the gate leakage current. The amorphous material filled in BD-1 is confirmed to be Si as shown from the Si & O mapping in Figs. 4(b) & 4(d). Since dopant redistribution [11] is expected under such extreme conditions, the amorphous Si is assumed to be undoped. The formation of n-i-p junction across the MOS stack prohibits a direct short and works like a diode. The reverse-biased diode (e.g. $V_g = 1.5 \text{ V}$) leaks $1.7 \mu\text{A}$ current (Fig. 2(a)) through the gate but is still able to induce a channel which carries $28 \mu\text{A}$ drive current (Fig. 2(b)).

In summary, transistor with multiple BD and severe structural damages (e.g., amorphization and DBIM) is demonstrated to be functional. Physical analysis provides additional information which cannot be otherwise derived from the standard electrical characterization technologies. The results also explain some very rare cases in which circuits could still be functional in the post-BD reliability test while the transistor has already suffered a very severe BD.

Fig. 4 (a) N (b) O (c) Co (d) Si EELS elemental mappings of the BD transistor. Co DBIM is found at the drain side. The amorphous material at BD-1 is confirmed to be pure Si.

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