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A Novel Sampling Process with Low Harmonic Distortion for a Digital Class D Amplifier

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of my original research and has not been submitted for a higher degree to any other University or Institution.

19/12/2005
Date

Fang Yu

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Finally, from the bottom of my heart, I want to thank my parents for their love and support.

Abstract

Digital Class D amplifiers offer the advantages of higher power efficiency and reduced hardware (when connected to a digital input source) compared to conventional classical linear amplifiers such as Class A and Class AB amplifiers. These attributes are particularly advantageous in applications whose critical parameters include micropower low-voltage operation and small integrated circuit (IC) area.

In this dissertation, we investigate the sampling processes and pulse generators for a Pulse Width Modulator (PWM) for a digital Class D amplifier. The emphases of the Class D amplifier design are micropower operation, small IC area and low harmonic distortion. We propose a novel sampling process, termed 'Second-Order Polynomial' sampling process. This sampling process requires three sampled points and aims to emulate the Natural Sampling process. We derive the double Fourier series expression for the proposed sampling process to analytically determine the non-linearity of the sampling process. We show that the derivation is correct by comparing it against the time-domain expression. The double Fourier series expression is also useful as it provides insight to a designer on how different parameters for a given design may be compromised to meet its specifications.

We compare our Second-Order Polynomial sampling process against the prevalent Delta-Compensation (δC) and Linear Interpolation (LI) sampling processes. We show that the Second-Order Polynomial sampling features lower harmonic distortion. Although the drawback of the Second-Order Polynomial sampling process is the slight increase in computation, its reduced non-linearity is worthwhile.

We synthesize the hardware for the PWM, including the Second-Order Polynomial process and pulse generator, and investigate various design variations.

List of Symbols

n	=	signal harmonic index
m	=	carrier harmonic index
ω_v	=	signal frequency
ω_c	=	carrier frequency
M	=	modulation index ($0<M<1$)
J_n	=	Bessel function of first kind, with order n
k	=	DC bias of modulating signal
p	=	sampling ratio (ω_c/ω_v)
t_p	=	pulse duration
T	=	sampling period
S_1	=	current sampling point
S_0	=	previous sampling point before S_1
S_2	=	next sampling point after S_1
S_{NS}	=	Natural sampling point
S_{LI}	=	Linear Interpolation sampling point
S_{UN}	=	Uniform sampling point
$S_{\delta C}$	=	Delta-compensation sampling point
ε	=	variable sampling factor of Enhanced Sampling Process
S_{sop}	=	Second-Order Polynomial sampling point
e_{RMS}	=	mean square value of quantization noise
E	=	spectrum density of noise
f_0	=	input signal bandwidth

f_s	=	sampling frequency
a, b, c (A, B, C)	=	coefficient of the second order polynomial function
t_{sop}	=	pulse duration of the second order polynomial sampling point
K_{mn}	=	double Fourier series coefficient
A_{mn}	=	cosine component of double Fourier series coefficient
B_{mn}	=	sine component of double Fourier series coefficient
Δ	=	amplitude difference between S_1 and S_2

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Chapter 1 Introduction

1.1 Applications of Power Amplifiers

Traditionally audio amplifiers are linear analogue amplifiers whose transistors operate in the linear region, and are typically Class A or Class AB; Class B is generally avoided due to its gross crossover distortion. These linear amplifiers have low power efficiency – Class A amplifiers (bridge output) have a maximum power efficiency of 50% [Gray and Hurst, 2000] while Class AB have a maximum efficiency between 50% and 78.5%, depending on the biasing. The maximum efficiency of these linear analogue amplifiers is when the signal swing is largest and this is not the usual operating condition of the amplifiers. Consequently, in practice, these linear amplifiers have substantially lower efficiencies, typically 10%-30% because the nominal signal swing is usually substantially lower than the maximum swing, that is where the crest factor is high. As the power efficiency is low, much of the wasted power is dissipated as heat. These amplifiers, if they are high power, are hence usually large (and heavy) due to the added heat sinks required to safely dissipate the heat.

With the advent of digital technology and in particular digital audio sources, it is highly desirable to perform audio power amplification directly in the digital domain, as opposed to usual approach of digital-to-analogue conversion followed by a linear analogue power amplifier. Audio amplifiers, both digital and analogue, using Class

D output stages tend to have higher power conversion efficiency, largely due to the fact that the output transistors therein operate digital-like, that is either in the ohmic or cut-off regions [Tan *et. al.*, 2003].

Digital audio devices are now prevalent and are found in living rooms, broadcast studios, cars, etc. These include compact discs (CD), mini-discs (MD), MP3, DVDs, etc, and many of these devices are portable. In an audio system, the power amplifier is often used to offer the necessary gain and drive to the output load. In these audio systems, particularly portable devices, it is desirable to obtain the power efficiency to be as high as possible to enable the device with a sufficiently long battery life. The digital Class D amplifier is particularly advantageous in these applications because when properly designed, it features high power efficiency (of the order of 90%) over a large modulation index range (signal swing), and at the same time, can feature low non-linearities (for example the Total Harmonic Distortion (THD) < 0.5%). The digital Class D amplifier is also advantageous when interfaced to a digital processor (for example, in a digital hearing instrument (hearing aid) and the like) because the need for a digital-to-analogue (D/A) converter is eliminated, hence the immediate power savings and reduced hardware.

1.2 Motivation

An increasing number of portable audio devices, including devices with critical power considerations such as hearing instruments, employ Class D amplifiers, primarily

because when appropriately designed [Chang *et. al.*, 2000], Class D amplifiers can feature high power efficiency, greater than 90% over a wide range of signal swing (modulation index, *M*).

Class D amplifiers may be generally classified into two groups: Analogue and Digital amplifiers. Analogue Class D amplifiers are perhaps more conventional and are semi-analogue circuits, in the sense that the modulation process, usually the Pulse Width Modulation (PWM) process, employs an analogue comparator and the input is an analogue (modulating) signal. It is probably of interest to note that other methods of modulation (for an analogue Class D amplifier) include Sigma Delta Modulation [Candy and Themes, 1992], and more recently Bang-Bang Control Modulation [Takagishi, 2002]. However, the PWM approach is most prevalent. This is largely due to the simplicity of the required hardware for the PWM, in particular where power is a critical parameter, for example in hearing instrument applications. When these analogue Class D amplifiers are interfaced to a digital signal processor (DSP), a D/A conversion is required to obtain the modulating analogue signal.

The current-art method would be to directly employ a digital Class D amplifier, thereby eliminating the need for the D/A converter, hence a more hardware efficient design. Furthermore, a digital Class D amplifier offers greater programmability and repeatability (more tolerant to fabrication process variations), easier (direct)

interface to digital processors and a higher immunity to noise [Gwee *et. al.*, 2002]. As in the analogue Class D amplifier, there are also a number of modulation techniques and they include Sigma Delta [Melanson, 1998] and the Click Modulation [Logan, 1984], in addition to PWM. However, both the Sigma Delta and the Click Modulation methods are substantially more complex than the PWM and consequently dissipate higher power [Gwee *et. al.*, 2003]. In view of the objectives of this research work that pertains to the power critical applications, in particular the hearing instrument, we will restrict our work to a Class D amplifier based on the PWM approach.

In Chapter 2, we will review the different modulation methods, including the different sampling processes for the PWM approach. In view of these sampling processes, there is a need for a simple sampling process (for low power dissipation considerations) that also features low non-linearity, particularly low THD (< 0.1%).

In summary, the motivation of this research is to design a micropower low-distortion digital PWM process for digital Class D amplifiers.

1.3 Objectives

The objective of this project is to investigate the design of a micropower low-voltage and low THD digital Class D power amplifier and its implementation for low-voltage power-critical applications, including digital hearing instruments. Specifically, the

design parameters are:

Table 1.1 Specifications of the design parameters

Voltage	1.1 V
Carrier Signal Frequency	44.1 kHz
Data Bandwidth	20 Hz - 4 kHz
Internal Frequency	<100 MHz
Power dissipation	<100 μW
Signal Noise Ratio (SNR)	>80 dB
THD	<0.1%

To be specific, the objective of this project is to propose a novel sampling process and its subsequent implementation to achieve micropower operation and with low non-linearities, for a low voltage Class D amplifier. The further objective is to analytically derive the double Fourier series expression for the proposed sampling process, and its subsequent verification.

1.4 Major Contribution of Thesis

This dissertation presents the analysis, design and implementation of a micropower, low-voltage and low distortion digital pulse width modulator for a digital Class D amplifier. The major contributions of this thesis are:

1. A novel digital sampling process, specifically the Second-Order Polynomial sampling process is proposed, and thereafter simplified and implemented;

2. The double Fourier series mathematical expression of the proposed Polynomial sampling process to depict the frequency components of the sampling process is derived and verified.

1.5 Thesis Organization

In this chapter, we have described the motivation, objectives and major contributions of this research programme. The remaining chapters of this dissertation are organised as follows. Chapter 2 provides an overview of reported PWM generating approaches, PWM sampling processes and PWM pulse generators of Class D amplifiers. Chapter 3 describes the proposed Polynomial Sampling and its spectrum analysis. Chapter 4 describes hardware description of the proposed sampling process, and provides the simulation results. Chapter 5 concludes this dissertation and lists several directions for future work.

Chapter 2 Literature Review

2.1 Introduction

The methods for generating the PWM signal for a digital Class D amplifier may be classified into three general approaches: (i) algorithmic PWM, (ii) oversampled Delta-Sigma ($\Delta\Sigma$) PCM (Pulse-Code Modulation)-PWM, and (iii) Click Modulation [Logan, 1984]. The first two methods are popular while the last remains largely academic due to its complexity. In view of this, we will only review in detail digital Class D amplifiers based on the first two approaches.

We will now briefly describe an overview of the three approaches and thereafter provide a somewhat comprehensive review of the formal two approaches. This review provides a good perspective of our proposed sampling process and its simplification (and subsequent implementation).

Figure 2.1 depicts a block diagram of a generic digital Class D amplifier based on algorithmic PWM. The input is the output of a digital source whose data is read from a digital medium such as a CD, digital audio tape (DAT), digital versatile disc (DVD), a digital communications receiver, etc. The first step in digital amplification is a sampling process to determine the digital value of the pulse width that is equivalent to the amplitude of the modulating signal sampled by the carrier. The second step is to generate the corresponding modulated pulses based on the

digital value provided by the sampling process. The output stage is a cascade of inverters whose transistors have increasing aspect ratios where the final output transistors have a low output impedance, typically <30Ω. This stage provides sufficient drive ability to drive a low impedance load (subminiature hearing instrument receiver), typically <600Ω. The low-pass filter removes the carrier components (pulses from the pulse generator) and delivers the amplified input equivalent in analogue form to the output device. In audio application systems, the output device is usually a loudspeaker.

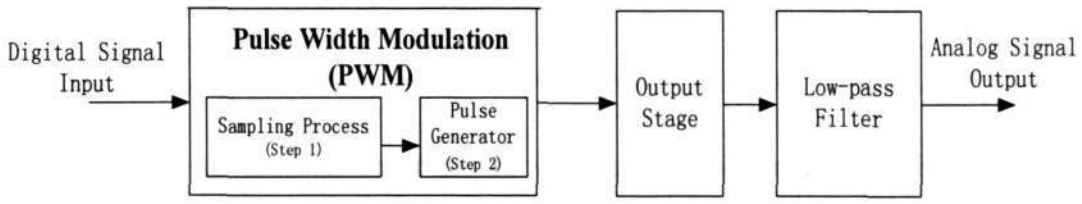


Figure 2.1 A digital Class D amplifier

The Pulse Width Modulation is the fundamental component of a Class D amplifier, which produces a train of pulses having widths corresponding to the level of input modulating signal. It is composed of two stages: sampling process and pulse generation.

The algorithmic PWMs essentially involve a signal sampling process to digitally emulate the Natural Sampling (NS) process, followed by a pulse generator. This signal sampling process is sometimes termed the cross-point deriver and as its name

implies, the process simply involves estimating the cross-point or intersection of the modulating signal and the carrier signal - the NS process, see later in this chapter.

One of impetuses for the wealth of reported algorithmic PWM sampling processes in literature is the desire for a low distortion PWM output (THD < 0.5%) with a low sampling rate (for example, f_s = 48 kHz) and with modest computation complexity (for example, 2 additions/subtractions and 1 division operation per sample). These attributes are highly desirable in view of micropower operation for power critical portable applications and devices such as hearing instruments. This is because a high sampling frequency, increased computation rate arising from more samples per unit time and the corresponding higher clock rate in the pulse generator, all translate to undesirable higher power dissipation. Further, a low computation complexity translates to simpler hardware, hence lower cost and usually higher reliability.

The reported sampling processes for the algorithmic PWM methods include the Linear Interpolation (LI) [Mellor *et. al.*, 1991; Goldberg and Sandler, 1994], Pseudo-Natural PWM [Goldberg and Sandler, 1994], Static-Filter PWM [Risbo and Morch, 1998], Weighted PWM and its variants [Johansen and Nielsen, 1999], Derivative PWM [Song, 2001], Parabolic Correction PWM [Pascual and Roeckner, 2000], Prediction Correction PWM [Roeckner *et. al.*, 2003; Midya *et. al.*, 2000] and more recently, the Delta Compensation (δC) PWM [Gwee *et. al.*, 2002] sampling processes from our research group. At the outset, we remark that the LI process offers low

non-linearities with very modest computation complexity and with low sampling rate. The other processes may offer lower non-linearities but at the high cost of substantially more complex computation and in some cases, requiring a higher sampling rate. We will qualify and quantify these parameters and briefly describe these different algorithmic sampling processes in our review in this chapter.

For completeness, we remark that the mechanisms of the non-linearities of low-voltage analogue Class D amplifiers, based on NS but with a quasi-linear carrier, for power-critical analogue hearing instruments are now well understood from a recent publication [Tan *et. al.*, 2003] from our research group.

Pulse generators for the algorithmic PWM include the clock-counter [Wei and Horowitz, 1996], tapped-delay-line [Dancy and Chandrakasan, 1997], a hybrid combination of clock-counter cum tapped-delay-line [Dancy and Chandrakasan, 1998], and the clock-counter cum noise-shaper approach [Hiorns *et. al.*, 1990; Tewksbury and Hallock, 1978] abbreviated the CNS pulse generator. Of these designs, the CNS pulse generator is the preferred design because of its robustness (in the sense that its parameters are virtually independent of fabrication process variations) in design and all its building blocks are compatible with standard digital CMOS fabrication processes. As in the case of the sampling processes, it is highly desirable that the sampling rate of the counter embodied in CNS pulse generator be low for low power dissipation. This

is because the pulse generator dominates the power dissipation in the Class D amplifier, and its clock counter is the functional block that dissipates the largest power.

In the later sections (Sections 2.2 – 2.4) in this chapter, we will provide a somewhat comprehensive review of reported PWM sampling processes and pulse generators.

The oversampled ΔΣ PCM-PWM method [Melanson, 1998] is essentially a PCM-to-PWM converter where the PCM signal is the original sampled signal, the Uniform Sampled (US, see section 2.2 later) data. This conversion process is usually complex, including the following chronological processes: oversampling by interpolation, ΔΣ modulation and a Pulse-Density-Modulation (PDM)-to-PWM converter. The oversampling effectively reduces the wordlength of the input samples in the interpolation process but at the cost of a higher clock frequency (typically 27-28 times, thereby reducing the wordlength of the input samples by 3-4 LSBs) and increased computation, including the need for digital filtering. The subsequent ΔΣ modulation is also usually relatively complex and involves a delta sigma modulator (typically 4th order or higher), and a PDM output is obtained. In the final conversion, a table look-up may be used instead of direct computation to reduce the intensity of the computation. To reduce the high frequency of the PDM output, bit-flipping techniques [Magrath and Sandler, 1997; Esslinger *et. al.*, 2002] are sometimes used. However, these techniques result in some errors and as a result, may compromise the low linearities attribute of the oversampled ΔΣ PCM-PWM method and may possibly

lead to instability. Finally, a PWM output is obtained via a PDM-to-PWM converter and the PWM output is usually low resolution (~5-bit) but timed to a medium speed clock (~10s MHz). The analogue output can be obtained by low pass filtering the high frequency PDM signal directly or the lower frequency PWM signal.

In short, it is instructive to appreciate that the computation of the oversampled ΔΣ PCM-PWM method is substantially more intensive than the algorithmic PWM method. However, the primary advantage [Melanson, 1998] of the oversampled ΔΣ PCM-PWM method hitherto is its low THD, typically 0.08% (compared to ~0.2% in typical algorithmic PWMs), negligible intermodulation distortion is over the entire audio bandwidth and high Signal-to-Noise Ratio (SNR). The reduced THD, however, is obtained at considerable hardware (including a larger IC area) and power dissipation costs, and these costs may be prohibitive for power critical applications.

Click Modulation PWM [Streitenberger *et. al.*, 2001; Logan, 1984] involves the application of Hilbert transform to convert the audio signal into a complex signal. It further involves an analytic exponential modulation to generate a binary signal having a separated baseband and finally the PWM signal is generated. Despite of the computation complexity of Click Modulation PWM, it does not appear, in practice, to offer any advantage in terms of non-linearities. This is because both the algorithmic PWM and ΔΣ PCM-PWM methods can offer comparable low non-linearities but with lesser computation demands.

2.2 Review of Different PWM Sampling Processes

In this section, we will review different reported PWM sampling processes. We will first describe the PWM signals in general and qualify the most common figure-of-merit that qualifies the PWM signals and/or a Class D amplifier. Thereafter we will provide an overview of the most common PWM sampling process and review other reported sampling processes.

2.2.1 PWM signals

PWM schemes can be generally categorised [Black, 1953] into single-edge PWM and double-edge PWM, and this is illustrated in Figure 2.2. In the single-edge PWM (Figure 2.2(a) and (b)), either the leading or the trailing edge of the rectangular PWM output pulse is presented to a given carrier frequency, while the position of the other edge is determined by the value of the input modulating signal. The single-edge PWM consequently produces a sequence of rectangular pulses whose widths are proportional to the signal values.

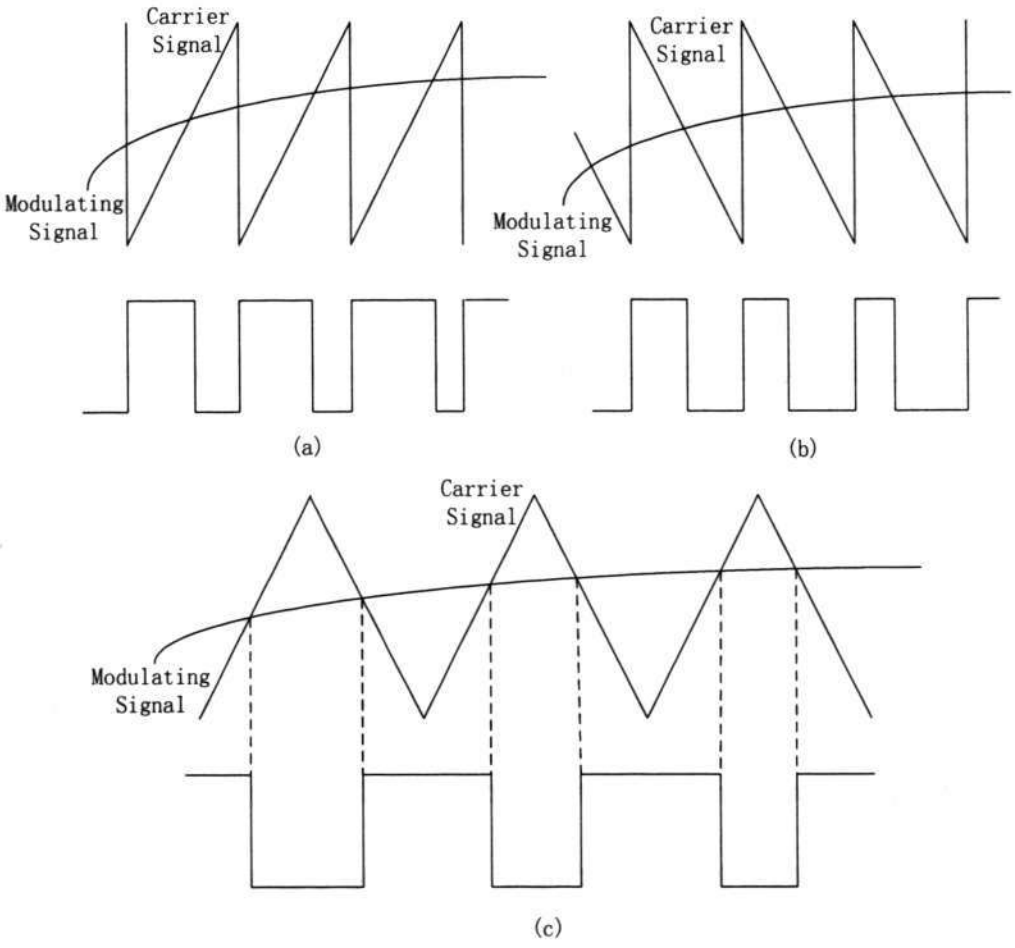


Figure 2.2 Classification of Pulse Width Modulations: (a) Leading edge modulation, (b) Trailing edge modulation, and (c) Double edge modulation

In double-edge PWM (Figure 2.2 (c)), both the leading and the trailing edges of the pulses are modulated by the input signal, either in a symmetric fashion (a single sample value determines both edges) or an asymmetric fashion (the leading and trailing edges correspond to two successive sample values). Since the double-edge PWM is usually more difficult and more expensive to implement than the single-edge PWM, the single-edge PWM is the more common accepted form of modulation, and this is the only form of interest in this dissertation. For completeness, note that in principle, the approaches adopted to analyze single-edge PWM signals can be applied

to the double-edge PWM signals as well.

2.2.2 Total Harmonic Distortion (THD)

One of the qualifications or figure-of-merits to qualify a sampling process and/or a Class D amplifier is the harmonic distortion non-linearity. The mathematical expression for THD is

$$THD = \frac{\sqrt{V_{2f_0}^2 + V_{3f_0}^2 + \ldots}}{V_{f_0}} \times 100\% \qquad (2.1)$$

where V_{f_0} : amplitude of fundamental component,

V_{2f_0} : amplitude of 2nd harmonic component, and

V_{3f_0} : amplitude of 3rd harmonic component.

In general, it is desirable for the THD to be low and the lower the THD, the higher quality (fidelity) is the output.

2.2.3 Overview of Different Sampling Processes

There are generally three classes of sampling processes for the PWM process, namely the Natural Sampling (NS) process, the Uniform Sampling (US) process and the algorithm-based sampling processes. Some of the reported algorithm-based sampling processes, already described earlier, include the Delta-Compensation (δC) sampling process [Gwee *et. al.*, 2002; Li, 2001], the Linear Interpolation (LI) sampling process [Gwee, 2003; Mellor, 1991] and other myriad of hybrid sampling processes [Sandler, 1993; Goldberg and Sandler, 1994; Streitenberger *et. al.*, 2000; Pascual and Roeckner, 2000].

It is of interest to note that the double Fourier series expression of the PWM sampling [Bennett, 1948] provides a highly effective, systematic and rigorous treatment of complex modulation problems. In most cases, the non-linear components of the PWM signal (arising from the sampling process) can be identified from the double Fourier series expression. We will discuss the double Fourier series expression for analyzing PWM signals in this section and will use it in the analytical work in this dissertation, including for our proposed sampling process.

The common four different sampling processes, namely the NS, US, δC, and LI, and their sampling points are shown in Figure 2.3. The following sampling point expressions are for the four common sampling processes.

The sampling point expression of NS is:

$$S_{NS} = S_{NS} \tag{2.2a}$$

The sampling point expression of US [Black, 1953] is:

$$S_{US} = S_1 \tag{2.2b}$$

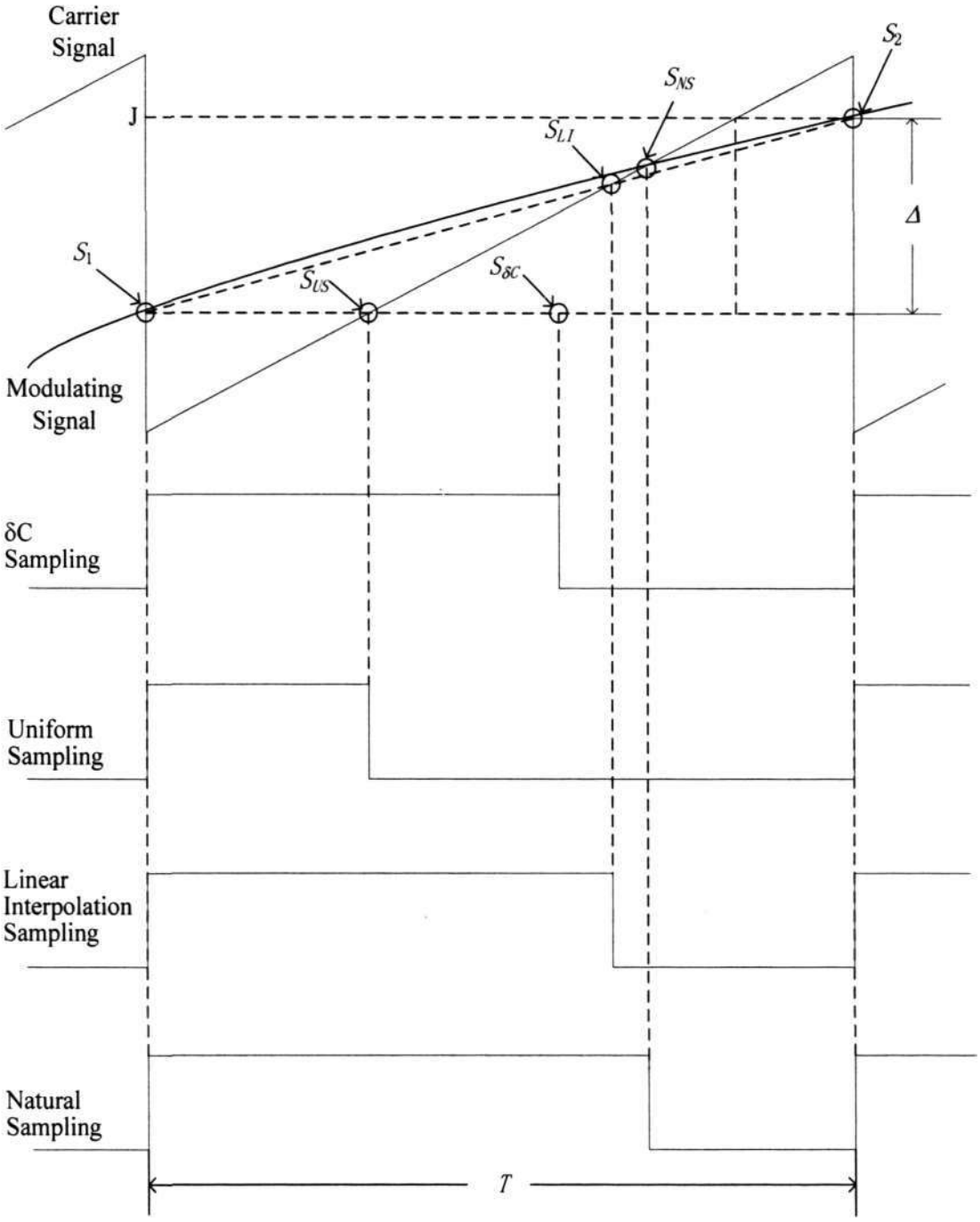
The sampling point equation of δC [Gwee *et. al.*, 2002] is:

$$S_{\delta C} = S_1 + (S_2 - S_1)\,(S_1 + S_2)\,/\,2 \tag{2.2c}$$

The sampling point equation of LI [Gwee *et. al.*, 2003] is:

$$S_{LI} = S_1/(1 + S_0 - S_2) \tag{2.2d}$$

Using the double Fourier series expression, the signal and harmonics in the frequency domain can be identified. These will now be delineated these.



S_{NS}: Natural sampled point

S_{LI}: Linear Interpolation sampled point

S_{US}: Uniform sampled point

$S_{\delta C}$: Delta-compensation sampled point

Δ: magnitude difference between S_1 and S_2

T: Sampling period

S_1: Current sampling point

S_2: Next sampling point

O: Sampled point

Figure 2.3 The Natural, Uniform, Delta-Compensation and Linear Interpolation

sampling processes

2.2.3.1 Natural Sampling Process

The double Fourier series expression for the one-sided NS process PWM spectrum [Black, 1953] is:

$$f(x,y) = k + \frac{M}{2}\cos(\omega_v t) + \sum_{m=1}^{\infty}\left\{\frac{1}{m\pi}\sin(m\omega_c t) - \frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t - 2m\pi k)\right\} + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\left\{-\frac{J_n(m\pi M)}{m\pi}\sin(m\omega_c t + n\omega_v t - 2m\pi k - \frac{n\pi}{2})\right\} \quad (2.3)$$

Equation (2.3) manifests the PWM spectral characteristics: the first term is the DC component, the second term corresponds to the modulating signal, the third term corresponds to the carrier frequency and its harmonics and the last term corresponds to the inter-modulation harmonics. From equation (2.3), it is apparent that if the carrier frequency ω_c is high, the output of the PWM taken at the output of the low-pass filter in Figure 2.1 is:

$$F_{LPF} = k + \frac{M}{2}\cos(\omega_v t) \quad (2.4)$$

Equation (2.4) depicts that a Class D amplifier theoretically has zero THD, assuming negligible inter-modulation harmonics. From Figure 2.3 and equation (2.4), it can be seen that the NS process is, in fact, an analogue sampling process where all values of the signals (in time and in magnitude) must be known. In other words, for the NS

process in digital form, the sampling frequency needs to be infinite, hence impractical for a digital emulation, which the sampling frequency needs to be very high.

2.2.3.2 Uniform Sampling Process

The one-sided PWM spectrum of Uniform Sampling (US) [Black, 1953] is

$$
\begin{aligned}
f(x,y) = k
&+ \sum_{n=1}^{\pm\infty} -\frac{J_n(\frac{n\pi M}{p})}{\frac{n\pi}{p}} \sin(n\omega_v t - \frac{n}{p}2\pi k - \frac{n\pi}{2}) \\
&+ \sum_{m=1}^{\infty} \left\{ \frac{1}{m\pi}\sin(m\omega_c t) - \frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t - 2m\pi k) \right\} \\
&+ \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} -\frac{J_n\left[(m+\frac{n}{p})\pi M\right]}{(m+\frac{n}{p})\pi} \sin(m\omega_c t + n\omega_v t - (m+\frac{n}{p})\pi 2\pi k - \frac{n\pi}{2})
\end{aligned}
\tag{2.5}
$$

The DC component (first term), carrier and its harmonics of the Uniform Sampling (third and fourth terms) are similar to the NS expression in equation (2.3). However, the second term in Equation (2.5) consists of the modulating signal and its harmonics. With the presence of signal harmonics, the THD is non-zero. By computation, we can easily show that the THD of the Uniform Sampling process is less than 3% at 11-bit resolution and this level of THD is generally unacceptable in many audio applications.

2.2.3.3 Algorithm-based Sampling Processes

The double Fourier series expression for the one-sided PWM spectrum of an algorithm-based sampling process based on the LI and δC sampling process is:

$$F_{algorithm}(t) = k - \sum_{n=1}^{\infty} \frac{I_{0n}}{2\frac{n}{p}\pi^2}\sin(n\omega_s t - 2\frac{n}{p}\pi k)$$

$$+ \sum_{m=1}^{\infty} [\frac{\sin(m\omega_c t)}{m\pi} - \frac{I_{m0}}{2m\pi^2}\sin(m\omega_c t - 2m\pi k)]$$

$$- \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} \frac{I_{mn}}{2(m+\frac{n}{p})\pi^2}\sin(m\omega_c t + n\omega_s t - 2m\pi k - 2\frac{n}{p}\pi k) \qquad (2.6)$$

In the case of LI process, the coefficients are [Gwee *et. al.*, 2003]:

$$I_{mn} = \int_0^{2\pi} \exp(-jn\Phi)\exp\left\{-j(m+\frac{n}{p})[\frac{2\pi Q\cos\Phi - 2BQ\sin\frac{\pi}{p}\sin(\Phi+\frac{\pi}{p})}{2\pi + 2Q\sin\frac{\pi}{p}\sin(\Phi+\frac{\pi}{p})}]\right\}d\Phi$$

(2.7a)

$$I_{m0} = \int_0^{2\pi} \exp\left\{-jm[\frac{2\pi Q\cos\Phi - 2BQ\sin\frac{\pi}{p}\sin(\Phi+\frac{\pi}{p})}{2\pi + 2Q\sin\frac{\pi}{p}\sin(\Phi+\frac{\pi}{p})}]\right\}d\Phi$$

(2.7b)

$$I_{0n} = \int_0^{2\pi} \exp(-jn\Phi)\exp\left\{-j\frac{n}{p}[\frac{2\pi Q\cos\Phi - 2BQ\sin\frac{\pi}{p}\sin(\Phi+\frac{\pi}{p})}{2\pi + 2Q\sin\frac{\pi}{p}\sin(\Phi+\frac{\pi}{p})}]\right\}d\Phi$$

(2.7c)

where $\left.\begin{array}{l} B = 2\pi k \\ Q = \pi M \end{array}\right\}$.

For the δC sampling process, the coefficients are [Gwee *et. al.*, 2002]:

$$I_{mn} = \int_0^{2\pi} \exp(-jn\Phi)\exp\left\{-j(m+\frac{n}{p})[Q\cos\Phi - \frac{4BQ\sin(\Phi+\frac{\pi}{p})\sin\frac{\pi}{p} + Q^2\sin 2(\Phi+\frac{\pi}{p})\sin\frac{2\pi}{p}}{4\pi}]\right\} d\Phi$$

(2.8a)

$$I_{m0} = \int_0^{2\pi} \exp\left\{-jm[Q\cos\Phi - \frac{4BQ\sin(\Phi+\frac{\pi}{p})\sin\frac{\pi}{p} + Q^2\sin 2(\Phi+\frac{\pi}{p})\sin\frac{2\pi}{p}}{4\pi}]\right\} d\Phi$$

(2.8b)

$$I_{0n} = \int_0^{2\pi} \exp(-jn\Phi)\exp\left\{-j\frac{n}{p}[Q\cos\Phi - \frac{4BQ\sin(\Phi+\frac{\pi}{p})\sin\frac{\pi}{p} + Q^2\sin 2(\Phi+\frac{\pi}{p})\sin\frac{2\pi}{p}}{4\pi}]\right\} d\Phi$$

(2.8c)

Similar to the earlier processes described, equation (2.6) for the algorithm-based sampling process can be interpreted as follows. The first term k is the DC term of the output PWM. The third term represents the carrier and its associated harmonics. The fourth term represents the inter-modulated signal component between the modulating signal and the carrier signal. Notice that the low pass filter characteristics at the output stage, the third and the fourth term have small, often negligible effect on the overall THD. The second term represents the modulating signal and its harmonics, and is the source of the harmonic distortion.

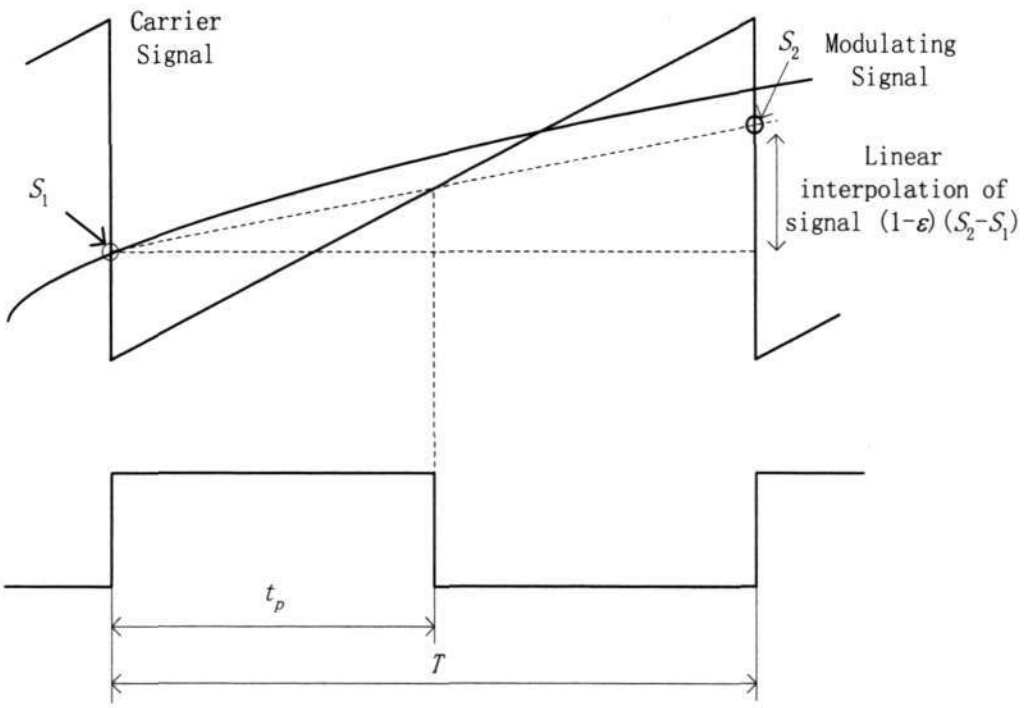
To determine the value of the harmonic distortion, the numerical integration method is often employed to determine the magnitude of each signal harmonic, and eventually, the THD. The THDs for the Linear Interpolation and δC sampling process are less than 0.044% and less than 0.13% at 11-bit resolution respectively, implying that the

LI process can better emulate the NS than the δC process; note that although the abovementioned THDs are relatively low, the THDs do not include that due to the pulse generator – the THD from the sampling process will be 'multiplied' by the non-linearities of the pulse generator (see later). However, the computation for the δC process is simpler [Gwee *et. al.*, 2003].

2.3 Review of other reported sampling processes

2.3.1 Enhanced Sampling

Mellor [Mellor *et. al.*, 1991] proposed an enhanced sampling process similar to the LI process. The enhancement involved a predefined ε that adjusts the specified sampling point and is shown in Figure 2.4.



t_p: pulse duration T: Sampling Period

Figure 2.4 Enhanced sampling based on LI [Mellor *et. al.*, 1991]

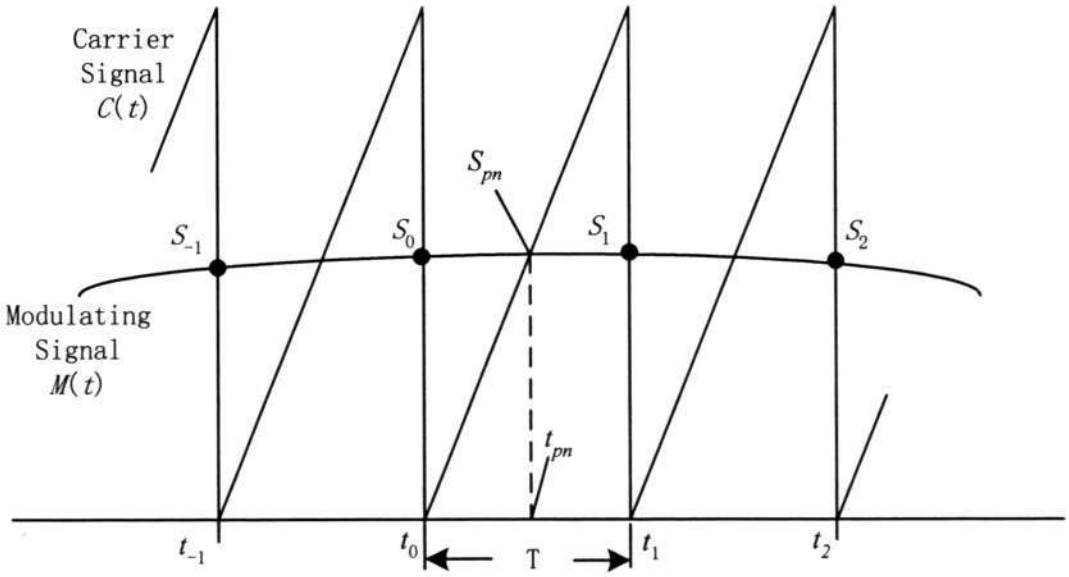
The pulse duration, t_p, can be expressed in terms of the pulse period T and the sample values S_1 and S_2, normalized between 0 and 1, as

$$t_p = T \frac{S_1}{1+(1-\varepsilon)(S_1 - S_2)} \tag{2.9}$$

The variable sampling factor ε can be interpreted as a means of controlling the influence of the second sample S_2 on the sampling process. When the ε=0, this enhanced sampling is the LI process and is closer to the natural sampled point, and if ε=1, it is the uniform sampling process with worse performance. We are of the opinion that this enhanced LI process does not have any advantage because the best setting for ε is when ε=1 and is the same as the LI process.

2.3.2 Pseudonatural PWM (PNPWM)

Sandler [Sandler, 1993] proposed the PNPWM process, a more precise PWM process (compared to LI) based on digital-to-analogue converter (DAC) techniques. This approach employed a third-order interpolation polynomial approximation to approximate NS and each derived sample is based on four data samples (S_i, $i \in \{0, 1, 2, 3\}$) as shown in Figure 2.5.



S_{pn}: the PNPWM sampling point t_{pn}: time index of S_{pn}

Figure 2.5 Third order interpolation polynomial approximation

The corresponding third-order approximation of the modulating signal is:

$$f(t) = C(t) - M(t) = t - \{c_{-1} + c_0(t - t_{-1}) + c_1(t - t_{-1})(t - t_0) + c_2(t - t_{-1})(t - t_0)(t - t_1)\} \quad (2.10)$$

where c_0, c_1, c_2 and c_3 are the coefficients of the third-order interpolation polynomial.

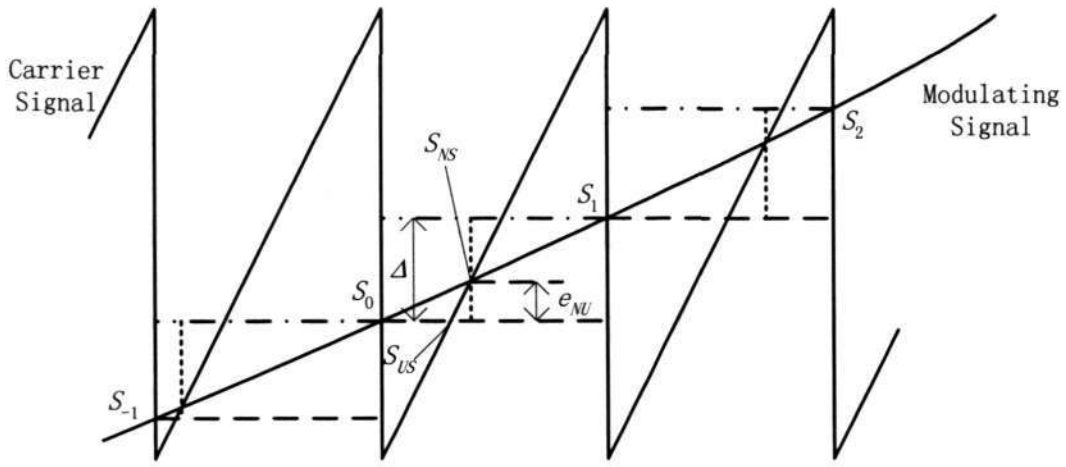
From a hardware perspective, the hardware required to realize this implementation is complex and inappropriate for power critical applications. In [Sandler, 1993], a dedicated DSP was used to compute the above equations.

2.3.3 Weighted Pulse Width Modulation (WPWM)

Johansen and Nielsen [Johansen and Nielsen, 1999] proposed the WPWM and with

error correction. The WPWM may be categorized as a hybrid scheme, a hybrid of the LI PWM and PNPWM.

The basis for PNPWM is illustrated in Figure 2.6. This sampling process is formulated on the observation that the error between NS and US increases (not proportionally) as the magnitude of the input modulating signal increases. The error is zero when the magnitude of the input modulating signal is zero and largest when the latter is maximum, normalized to 1.



Δ: magnitude difference between continuous samples

e_{NU}: error between Natural and Uniform sampled points

Figure 2.6 Illustration of pulse edge placement error in WPWM

The iterative process is carried out by successive insertions of parameters into the iterative expression and after N iterations, the general expression is formed as:

$$S_{W,N} = \sum_{i=0}^{N-1} S_0 \Delta^i + S_{W,0} \Delta^N \tag{2.11}$$

where N is the total iteration number

S_W is the magnitude of WPWM,

$\Delta = S_1 - S_0$, magnitude difference between the consecutive samples, and

i is the iteration number.

If the initial guess $S_{W,0}$ is chosen to be S_0, the iterative expression reduces to

$$S_{W,N} = \sum_{i=0}^{N} S_0 \Delta^i \tag{2.12}$$

In [Johansen and Nielsen, 1999], it is sufficient to get the WPWM by two iterations, requiring four multiplications and five additions for each derived sample.

The error correction works as an "add on" scheme for further correction after the initial correction with the WPWM process. This method aims to minimize the following expression:

$$S_{NS} - (S_{LI} + \alpha e_{NL}) \tag{2.13}$$

where α is a empirically chosen coefficient, and

e_{NL} is the magnitude difference between the NS and LI.

We note that, at best, the WPWM with error correction approaches the LI process. Although the advantage of WPWM is that its computation does not require a division operation, the overall computation is still more complex than the LI process.

2.3.4 PCM to Single-Edge NS Conversion

Pascual and Roeckner [Pascual, and Roeckner, 2000] proposed two algorithms to convert uniformly sampled data to emulate the NS process. Both algorithms use four consecutive input samples to compute each output value. Figure 2.7 illustrates the method for the two algorithms.

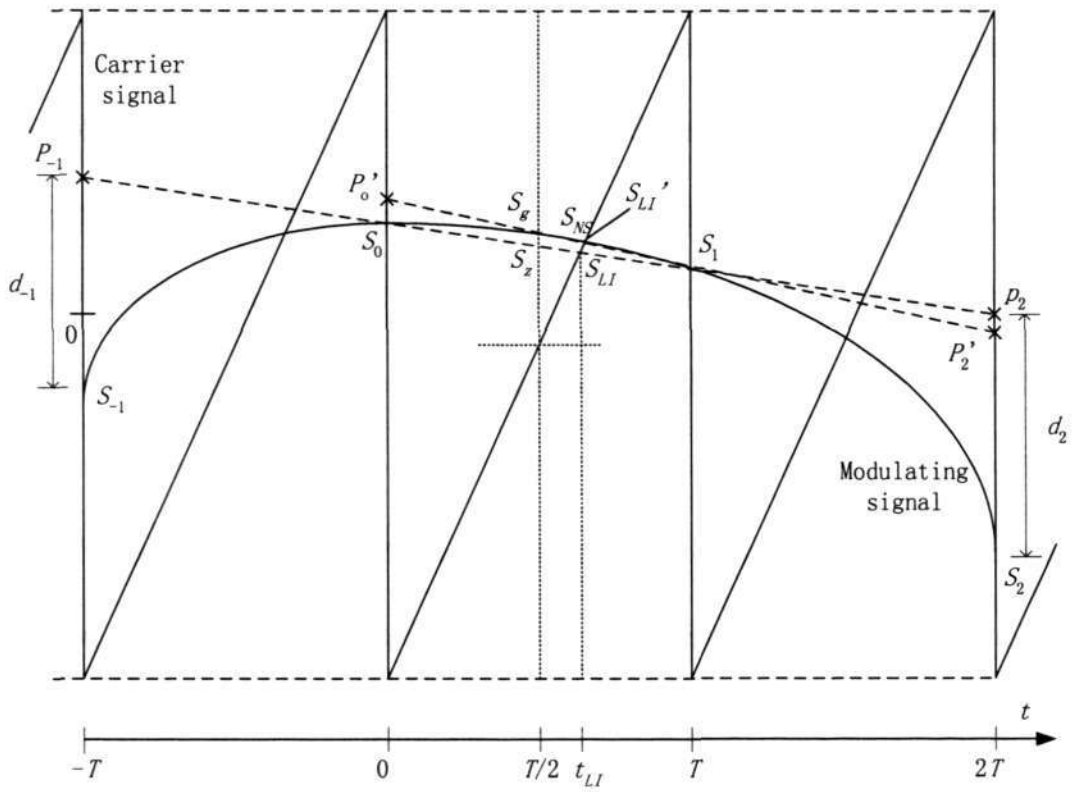


Figure 2.7 PCM to single-edge NPWM conversion algorithms

The algorithm works in the following fashion. The straight line that passes through S_0 and S_1 is constructed, where P_n is the point projected on the corresponding time index, d_n is the magnitude difference between the projection and sample, defined as P_n-S_n.

Analytically, the first algorithm is expressed as:

$$S_A \approx S_{LI} + \alpha(d_{-1} + d_2)(t_{LI}T - t_{LI}^2) \tag{2.14}$$

where S_A is the sampling point magnitude of the first algorithm, and

α is a constant that needs to be chosen empirically and depends only on the absolute sampling period.

The second algorithm is a two-step version of the abovementioned single-step first algorithm. S_z is the middle point between S_0 and S_1. S_g is guessed by adding a certain correction factor to S_z in the following expression:

$$S_g \approx S_z + \beta(d_{-1} + d_2) \tag{2.15}$$

where constant β is also chosen empirically.

The second step is to find approximations for S_{LI}' and S_{NS} by S_g. Again, P_n' is the projection on the time index based on the line connecting S_g and S_1. If S_g is positive, following expressions are employed:

$$S_B \approx S_{LI}' + \alpha(d_0' + \gamma d_2')S_{LI}'(1 - S_{LI}') \approx S_{LI}'(1 - \alpha(d_0' + \gamma d_2')(S_{LI}' - 1)) \tag{2.16a}$$

where S_B is the sampling point of the second algorithm, and

λ is an empirically chosen coefficient.

If S_g is negative, the equations employed are:

$$S_B \approx S_{LI}' - \alpha(\gamma d_0' + d_2')S_{LI}'(1 + S_{LI}') \approx S_{LI}'(1 - \alpha(\gamma d_0' + d_2')(S_{LI}' + 1)) \tag{2.16b}$$

This second algorithm involves the optimisation of parameters α, β and γ, whereas the first algorithm deals with α only; the two αs are unrelated.

Although these algorithms can yield an estimation of the Natural by Sampled points better than LI, the computation involved is very complex and inappropriate for low voltage power critical applications.

In summary, our reviews shows that most reported PWM sampling processes are considerably more complex than the three most common practical PWM sampling processes, namely US, δC and LI. In view of this review, the objective of this dissertation, as outlined in Chapter 1, is to propose a PWM sampling process that feature better performance (in particular THD non-linearity) than the three common practical PWM sampling processes and get retain the simplicity of the processes, hence the simple hardware and low power dissipation attributes – appropriate for power critical applications.

2.4 Review on PWM pulse generators

The block diagram of the digital Class D amplifier based on the PWM approach was earlier given in Figure 2.1. In the PWM block, the second sub-block (second step) is the Pulse Generator. The PWM output is obtained at the output of the Pulse Generator.

PWM pulse generators may be classified into: (i) Fast-clock counter [Wei and Horowitz, 1996], (ii) Tapped-delay-line [Dancy and Chandrakasan, 1997], (iii) Hybrid counter-delay-line [Dancy and Chandrakasan, 1998] and (iv) Noise shaper

[Tewksbury and Hallock, 1978; Hiorns *et. al.*, 1990]. We will now review these different approaches to the pulse generator and from this review, we will explain why we adopt the noise shaper approach.

2.4.1 Fast-Clock Counter

Figure 2.8 depicts the block diagram of the Fast-clock counter based [Wei and Horowitz, 1996] PWM pulse generator that comprises a counter, a D-flip-flop and a zero detector. The operation of this pulse generation is as follows. Initially, the F_{sw} (carrier frequency) clock sets the output PWM signal to high and at the same time, it enables data to be loaded into the counter. This counter counts down the input data until all are zeros detected, triggers the D-flip-flop and resets the output to low. In this way, the output PWM signal is precisely generated.

The shortcoming of this pulse generator design is that it dissipates relatively high power if high precision is desired. For example, if the resolution is 12 bits, the frequency of the F_{clk} will be 197 MHz (48 kHz $\times 2^{12}$). For a 0.35 μm CMOS process, this high frequency clock will dissipate ~70 μW, hence inappropriate for power critical applications; we hope to obtain lower dissipation, ~30 μW.

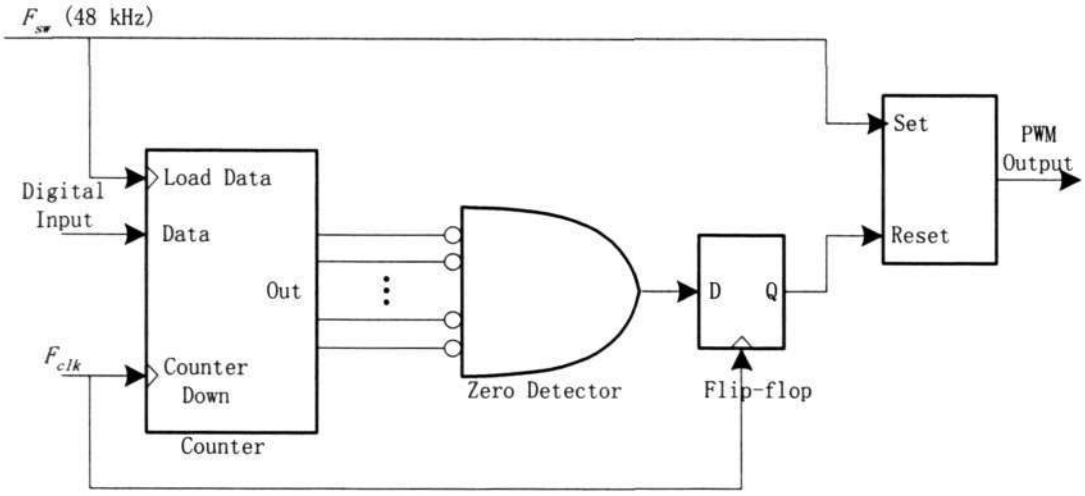


Figure 2.8 Fast-clock-counter based PWM pulse generator

2.4.2 Counter-Delay-Line

The second reported pulse generator to generate the PWM signal uses the tapped-delay-line [Dancy and Chandrakasan, 1997] approach. It contains a D-flip-flop, a chain of delay buffers and a multiplexer as show in Figure 2.9. This process begins when the F_{sw} (carrier frequency) clock sets the output PWM signal to high and at the same time, the latter traverses through the delay line until the loaded digital input number is met, triggers the D-flip-flop and resets the output to low.

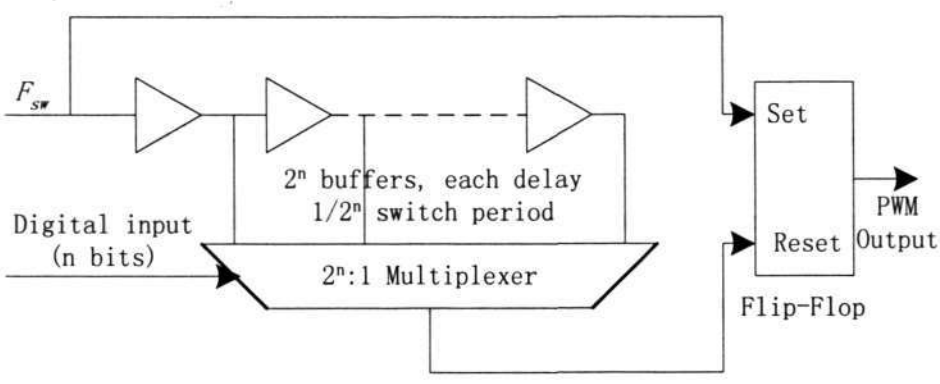


Figure 2.9 Tapped-delay-line base PWM pulse generator

Compared with the fast counter approach, the advantage of the tapped-delay-line is the lower operation frequency, resulting in lower power dissipation. However, it needs large number of the delay units. For example, if the wordlength of the input data is 12-bit, the number of delay units required is 4096 (2^{12}). If an additional bit is desired, the number of delay units will double. Moreover, the requirement for the fabrication process for this method is critical for precise delay time. In other words, this approach is highly sensitive to process variations and not suitable for standard digital CMOS processes. Furthermore, the IC area requirements may be excessively large.

2.4.3 Hybrid Counter-Delay-Line

The Hybrid counter-delay-line [Dancy and Chandrakasan, 1998] is the combination of two abovementioned approaches. The concept here is to reduce the number of bits required of the fast counter by having the delay line to process part of the wordlength of the data. For example, in Figure 2.10, the 12-bits input data is separated into a 9-bit MSB and 3-bit LSB. The 9-bit MSB is loaded into the Fast clock counter, and the 3-bit LSB is loaded into the tapped-delay-line. Initially, the F_{sw} clock sets the output PWM to high, and the counter counts down until the 9-bit MSB is zero. Thereafter, the counter output propagates through the delay-line for the remaining 3-bit LSB and finally triggers the reset the D-flip-flop to generate the PWM pulse.

Although this approach alleviates the complexity of the counter, it does suffer from

the process variation of the fabrication process – although to a lower degree than the second method.

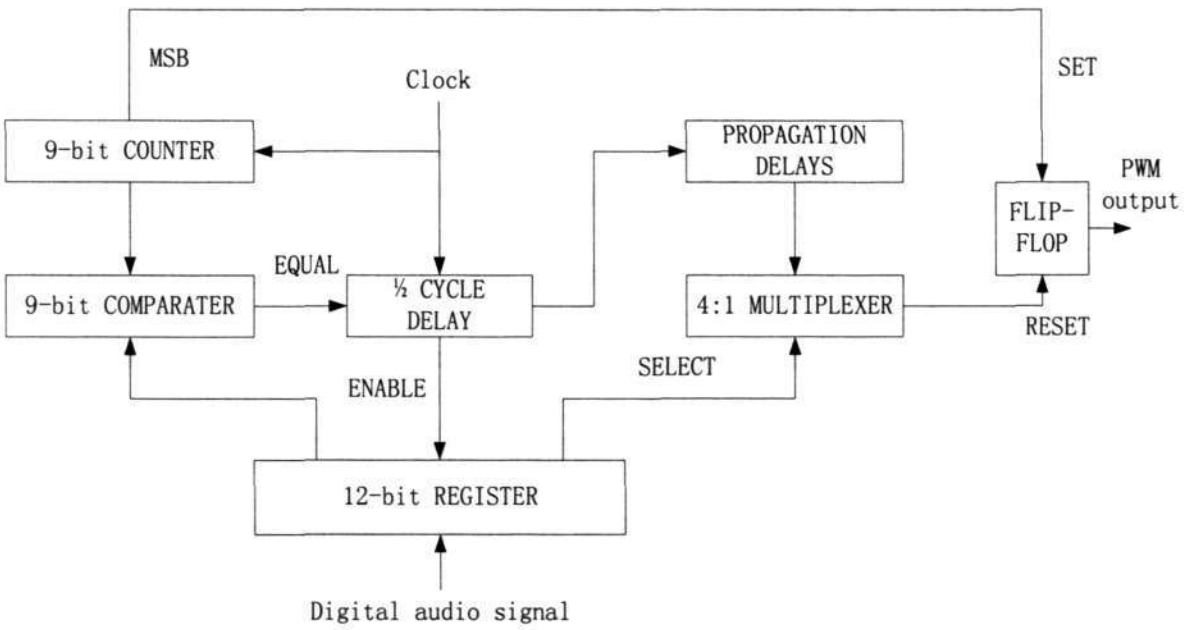


Figure 2.10 Hybrid counter-delay-line pulse generator

The three abovementioned approaches are essentially 'brute-force' approaches that do not utilize signal processing techniques to reduce the complexity of the hardware. The fourth reported pulse generator approach, noise shaper, differs in this important aspect.

2.4.4 Noise Shaping

We have already described that the high clock frequency in the pulse generator is the dominant parameter that dissipates power – the higher the clock frequency, the higher the power. From a digital circuit viewpoint, the primary mechanism is dynamic power

$$P_d = \alpha \cdot C_{Tot} \cdot Vdd^2 \cdot f_{clk}$$

where α is the activity factor,

C_{Tot} is the total switched capacitance,

Vdd is the supply voltage, and

f_{clk} is the clock frequency.

In very high quality audio such as 16-bit PCM data sampled at 44.1 kHz, the fast-clock approach pulse generator would require $2^{16} \times 44.1$ kHz ≈ 2.9 GHz. This clock rate would be inappropriate for power critical applications.

Li [Li, 2000] has plotted the relationship between the power dissipation and the number of bits assigned to the counter and this is shown in Figure 2.11. We note that the power dissipation increases exponentially-like with counter bits. In view of this, it is easy to appreciate the rationale for the counter-delay-line and the hybrid counter-delay-line approaches, albeit their poor sensitivity to process variations.

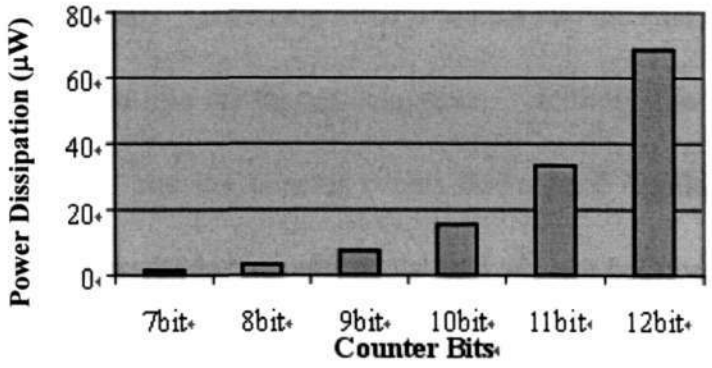


Figure 2.11 Relationship between power dissipation and counter bits of PWM pulse generator

One of the earlier noise shapers [Tewksbury and Hallock, 1978] is depicted in Figure 2.12. From the preceding review on the earlier three pulse generator design approaches, it is apparent that they have somewhat severe limitations if low power and consistency are important design parameters. The fourth reported method largely circumvents these limitations by employing a well known signal processing algorithm already embodied in ΔΣ modulators (see next section) – noise shaping.

The basic concept of noise-shaping is the noise spectrum of an input signal can be modified so that most of the in-band noise is moved out-of-band, thereby allowing a shorter wordlength for signal representation. From the preceding discussion, this immediately translate to a lower frequency clock rate for the pulse generator (based on the Fast-Clock Counter method), and hence lower power dissipation. For example, in Figure 2.12, the schematic of a 16-bit to 11-bit 1st order noise shaper is depicted.

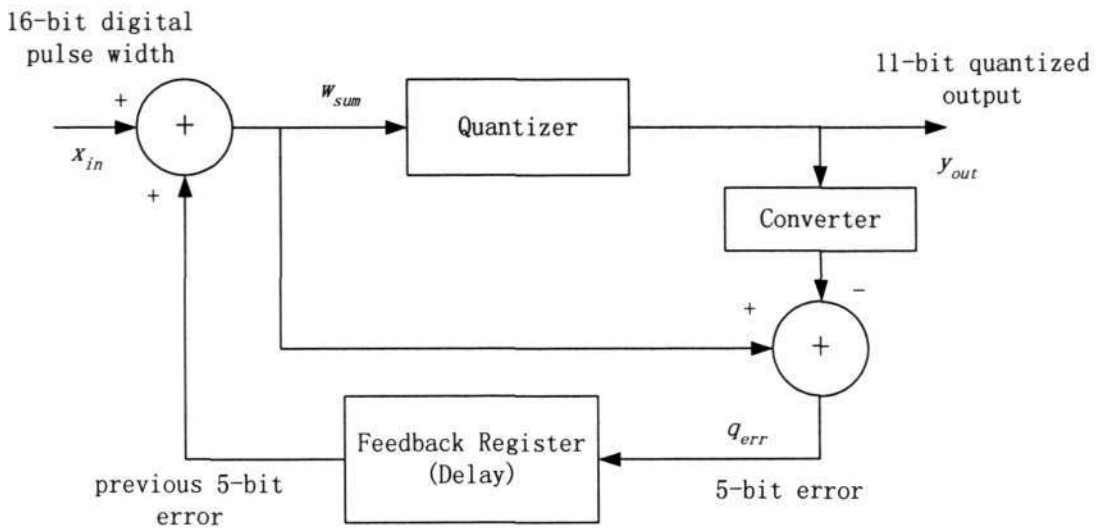


Figure 2.12 16-bit to 11-bit 1st order noise shaper

In this example, the 16-bit digital pulse width x_{in} determined by the sampling process is summed with the 5-bit quantization error q_{err} obtained from the previous output of the noise shaper. The 16-bit digital value w_{sum} from this addition is then quantized into an 11-bit output signal y_{out} by removing the least significant 5 bits. This y_{out} output is also input to a converter that pads 5 zero bits to obtain the 5-bit quantization error, which is then fedback to the summer to correct the next input. In this manner, the noise shaping technique allows the digital signal data to be represented with fewer bits, enabling a lower clock frequency, hence lower power [Smith *et. al.*, 1995], without seriously degrading (see later for qualification) the signal.

The required shorter digital wordlength arising from noise shaping is well established. From the time domain viewpoint,

$$w_{sum}[i] = x_{in}[i] + q_{err}[i-1]$$

$$y_{out}[i] = w_{sum}[i] - q_{err}[i] = x[i] + q_{err}[i-1] - q_{err}[i] \qquad (2.18)$$

where i is the time index.

In the frequency domain viewpoint, the signal transfer function, $S_{TF}(z)$, is

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = 1 \qquad (2.19)$$

and the noise transfer function, $N_{TF}(z)$, is

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = 1 - z^{-1} \qquad (2.20)$$

assuming that the quantization noise approximates white noise, a reasonable assumption in most cases. For $z = e^{j\omega T_s}$,

$$N_{TF}(z) = 1 - z^{-1} = 1 - e^{-j\omega T_s} = 1 - e^{-\frac{j2\pi f}{f_s}} = 2\sin(\frac{\pi f}{f_s})e^{-\frac{j\pi f}{f_s}} \quad (2.21)$$

where T_s is the sampling period, and

f_s is the sampling frequency.

The magnitude of the transfer function depicts a high-pass function

$$|N_{TF}(f)| = 2\sin(\frac{\pi f}{f_s}) \quad (2.22)$$

In other words, the noise transfer function is equivalent to a discrete-time differentiator (i.e., a high-pass filter), that is, most of the noise power is now pushed into the high frequency out-of-band range.

It is well known that noise shaper modulators of higher order can further improve (over lower order modulators) the performance but at the cost of higher hardware costs.

The transfer function of a higher order noise shaper modulator is

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = (1 - z^{-1})^{N_{ons}} \quad (2.23)$$

where N_{ons} is the order of noise shaper.

Figure 2.13 depicts the characteristics of zero-, first-, second- and third-order noise-shapers. In the band of interest (from 0 to f_0), the noise power decreases as the noise-shaping order increases, and the out-of-band noise increases for the higher-order modulators.

This noise reduction has also an effect on THD – the THD is reduced. We will further explore this in Chapter 4 later.

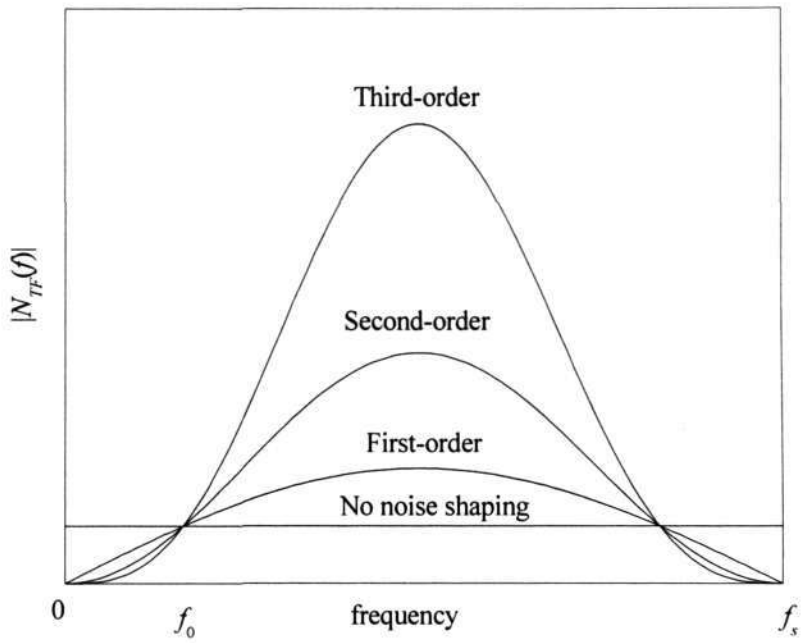


Figure 2.13 Some different noise-shaping transfer function

2.4.5 Frequency Doubler

In view of the preceding discussion where we noted that for low power dissipation considerations, it is always of interest to reduce the clock rate of the reported clock generator in the pulse generator. One reported method to do this is by employing the frequency doubler [Gwee *et. al.*, 2003] as shown in Figure 2.14.

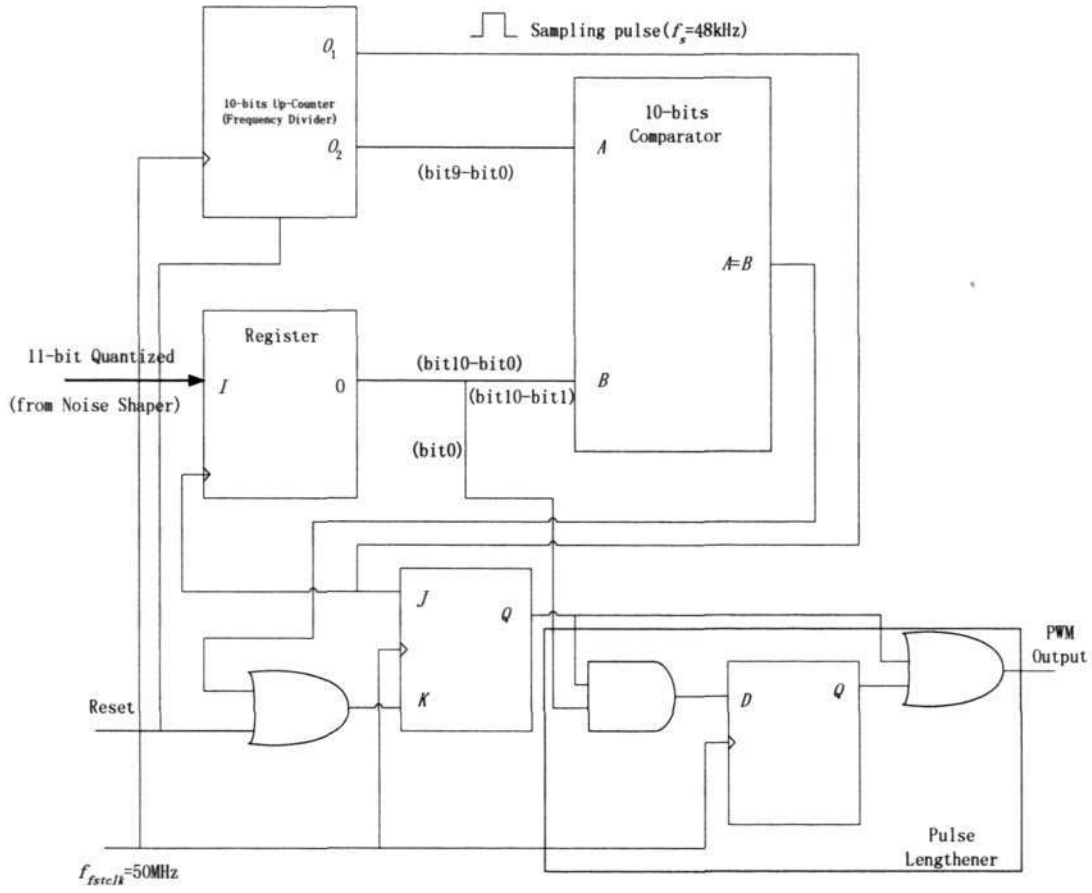


Figure 2.14 Block diagram of the 10-bit counter, comparator, and the 1-bit frequency doubler

The operation of this reported frequency doubler is as follows. Initially, the digital input data is loaded into the Register. At the same time, the '*J*' input of the JK flip-flop is asserted to set the flip-flop's output to high, this output passes through the OR gate and sets the PWM output pulse to high. The fast-clock-counter, which has 10-bit output, will then count up from zero. Its output compares with the 10-bit MSB of the 11-bit digital input. When the condition *A=B* is met, the comparator will assert the '*K*' input of the JK flip-flop to toggle its output to low, generating the corresponding 10-bit PWM pulse – this 1-bit LSB serves as a pulse extender. If the

digital input data is an even number, the LSB will be zero and nothing will be done with this extender. If the input data is an odd number, the LSB will be one and a 1/2 pulse width of the fast-clock period is extended to the 10-bit PWM pulse output – this half period is obtained by using the 1-bit PWM Pulse Extender. When the JK flip-flop output and the LSB of digital input data are high, the D flip-flop output goes high and extends the PWM pulse output continuously on every falling edge of the fast-clock. When the JK flip-flop output goes low at the rising edge of the fast-clock, it asserts logic low to the D flip-flop input and toggles the PWM pulse output to low at the falling edge. The correct PWM pulse output is hence generated without the need for doubling the frequency, hence saving approximately 50% of the pulse generator power dissipation.

2.5 Delta-Sigma (ΔΣ) Modulator

2.5.1 Introduction

At this juncture, we have completed our review of digital Class D amplifiers based on the PWM approach. In this section, we will review the approach for generating the PWM signal of a digital Class D amplifier based on Delta-Sigma. To put this approach succinctly, the ΔΣ modulator approach is a method to reduce the number of bits (resolution) at the expense of increased sampling rate. For a digital Class D amplifier based on ΔΣ with a PWM output, the process typically involves three steps: oversampling by interpolation, delta-sigma (ΔΣ) modulation and a Pulse-Density-Modulation (PDM)-to-PWM converter.

2.5.2 Applications

It is generally agreed that a digital Class D amplifier based on a higher order ΔΣ approach yield better digital amplification. For this reason, we note that several medium-to-high power digital Class D amplifiers are based on this approach. In these applications, high power efficiency and low power dissipation are lesser concerns compared to audio quality. In other words, the ΔΣ approach does not lend itself well to power critical applications when power dissipation and simple hardware complexity are critical parameters.

Reported digital Class D amplifiers based on ΔΣ approach include Essingler [Esslinger *et. al.*, 2002], Margath [Margath and Sandler, 1997], AudioLogic Incorporated [Melanson, 1998] and Yamaha Corporation [Kohdaka *et. al.*, 1993].

One commercial device, the CS44L10 from Cirrus Logic [Melanson, 1998] using the abovementioned approach is a good example. Figure 2.17 shows its architecture. From this figure, one can easily identify the core components: interpolation, multibit ΔΣ modulator and PWM conversion. In this system, the oversampling ratio is 256. The second order sigma-delta modulator will output 4-bit PDM data, which is further converted to PWM signal by the PWM Conversion. The THD plus Noise of this product is about 0.08%, while the output frequency is about 12.288MHz.

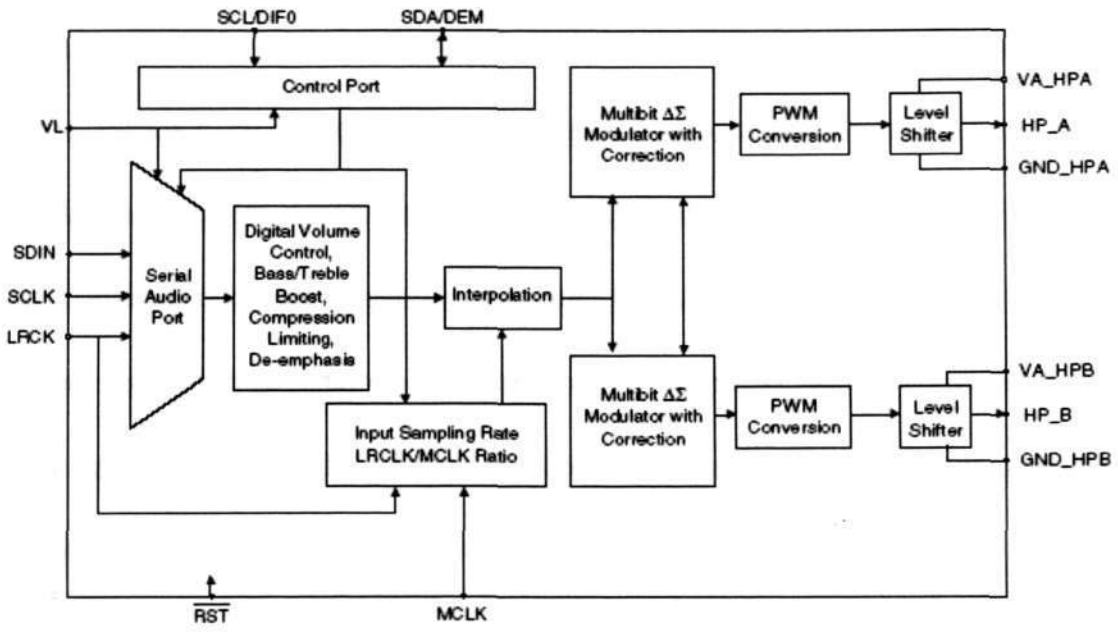


Figure 2.15 The CS44L10 digital-to-PWM Class D audio amplifier system controller

2.6 Conclusions

This chapter has reviewed and described reported approaches (algorithmic PWM, oversampled ΔΣ PCM-PWM, Click modulation) for the implementation to digital Class D amplifiers. For the algorithmic PWM approach, we have briefly reviewed the general sampling processes including NS, US, δC and LI sampling process, and other arguably less known processes including PNPWM and WPWM. We have also described the different approaches for the design of pulse generators: Fast-clock-counter, tapped-delay-line, hybrid-counter-delay, noise shaper and pulse extender. Finally, we reviewed the ΔΣ modulator approach.

Chapter 3 Proposed Second-Order Polynomial Sampling Algorithm

3.1 Introduction

We provide in this chapter our proposed algorithm-based sampling method and we name it the Second-Order Polynomial sampling. In this chapter, we will also present the derivation, simplification and spectrum analysis (derivation of the double Fourier series) of this proposed sampling process. We will also provide verification to our derivation of the double Fourier series expression for our proposed sampling process.

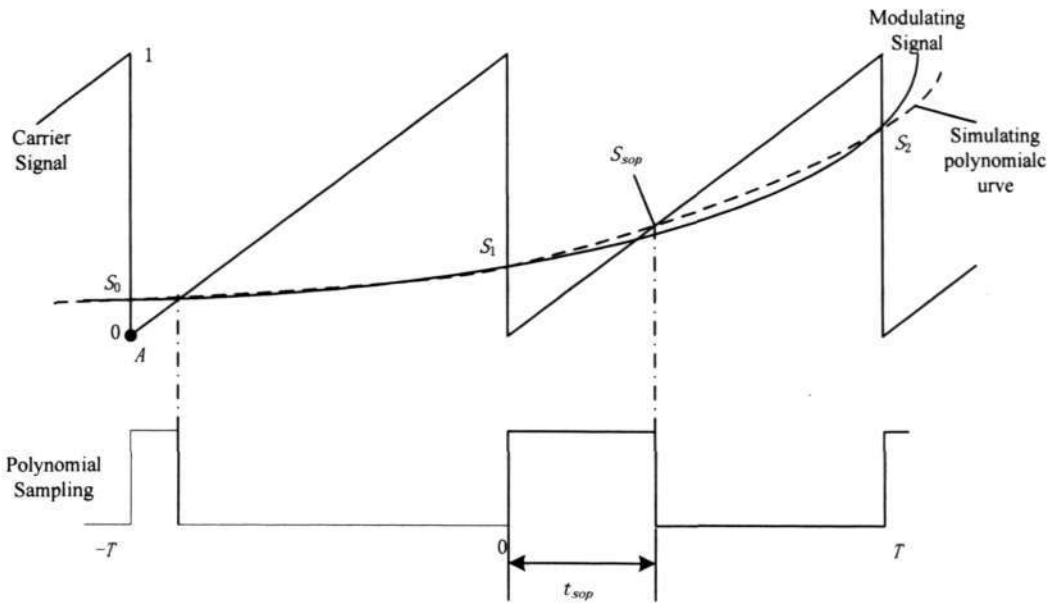
In view of Chapters 1 and 2, our objectives for the Second-Order Polynomial Sampling process are to obtain a process that approaches the Natural Sampling process and with minimum computation. Specifically, we aim to improve on the prevalent LI sampling process (particularly lower THD) without excessive overheads.

3.2 Proposed Polynomial Sampling Algorithm

In the previous chapter, we have reviewed the LI sampling process – a sampling process that connects two consecutive sampling points to simulate the modulating curve. Similarly, as its name implies, we propose a Second Order Polynomial Sampling – a process that uses three consecutive sampling points to construct a polynomial curve and simulate the modulating signal. At this outset, it would be

reasonable to expect that an additional sample will yield more accurate result and the cost, in terms of the intensity of computation, will be higher. In view of the latter, we are especially careful about the cost of the overheads and we will show how we simplify our Second-Order Polynomial sampling process.

Figure 3.1 depicts how we obtain the pulse width of the Polynomial Sampling process (trailing-edge modulation). In this diagram, point *A* along the abscissa time axis is referenced as time t=-T, and the magnitude of the carrier signal along the ordinate is normalized to 1 unit with point *A* referenced as the initial zero point. The simulated polynomial curve passes through three consecutive Uniform sampled points. Its intersection with the carrier signal becomes the Polynomial sampled point.



t_{sop} = pulse width T = sampling period

S_{sop} = current polynomial sampled point S_0 = past Uniform sampled point

S_1 = present Uniform sampled point S_2 = next Uniform sampled piont

Figure 3.1 Polynomial Sampling process

Analytically, we define the polynomial function of this simulating curve as:

$$M(t) = at^2+bt+c \tag{3.1}$$

where $M(t)$ is the function of simulating curve, and

a, b and c are second polynomial function coefficients.

In order to determine the value of coefficients a, b and c, we use the information on three known points: $(-T, S_0)$, $(0, S_1)$ and (T, S_2).

By simple algebra, we can show that the coefficients of the simulated curve are:

$$a = \frac{S_0 + S_2 - 2S_1}{2T^2} \tag{3.2a}$$

$$b = \frac{S_2 - S_0}{2T} \tag{3.2b}$$

$$c = S_1 \tag{3.2c}$$

Note that if the second order term coefficient a is zero, the simulated curve will be a straight line, and simplifies to the LI sampling process. We will only consider the case of $a > 0$ in the following derivation, a similar derivation step and the same result can also be achieved for the case of $a < 0$.

By substituting equation (3.2) into (3.1), we obtain:

$$M(t) = \frac{S_0 + S_2 - 2S_1}{2T^2} t^2 + \frac{S_2 - S_0}{2T} t + S_1 \tag{3.3}$$

The carrier signal function with slope $1/T$ can be written as:

$$C(t) = \frac{1}{T} t \tag{3.4}$$

As in all algorithmic PWM processes, the intersection of above two curves is the sampled point. In our case,

$$M(t) - C(t) = 0 \quad \text{for } t = t_{sop} \tag{3.5}$$

Specifically,

$$\frac{1}{T}t = \frac{S_0 + S_2 - 2S_1}{2T^2}t^2 + \frac{S_2 - S_0}{2T}t + S_1 \tag{3.6}$$

For simplification, we define the variables d and L as follows:

$$d = S_0 + S_2 - 2S_1 \tag{3.7a}$$

$$L = 2 + (S_0 - S_2) \tag{3.7b}$$

We note here that if the sampling frequency is large enough, S_0, S_1 and S_2 have similar amplitude. Hence, $d \approx 0$

By substituting these variables, equation (3.6) becomes

$$dt^2 - LTt + 2S_1T^2 = 0 \tag{3.8}$$

$$\Rightarrow\ t^2 - \frac{LT}{d}t + \frac{2S_1T^2}{d} = 0 \tag{3.9}$$

There are two roots for this equation:

$$t_{sop1} = \frac{1}{2}\left[\frac{L}{d} - \sqrt{(\frac{L}{d})^2 - 8\frac{S_1}{d}}\right]T$$

(3.10a)

$$t_{sop2} = \frac{1}{2}\left[\frac{L}{d} + \sqrt{(\frac{L}{d})^2 - 8\frac{S_1}{d}}\right]T \tag{3.10b}$$

Notice that the range of t_{sop} is $0 < t_{sop} < T$. It is possible that t_{sop2} is larger than T (in case $S_0 > S_2$ and $S_0 \approx S_1 \approx S_2$, resulting in $L/d>2$), and t_{sop2} cannot hence satisfy the requirement that $0<t_{sop}<T$. In other words, equation (3.10a) is the only possible root.

From a computation viewpoint, this derived Polynomial sampled point expression is very complex. It involves division, square and square root operations, and in view of our objectives, we will now explain how we simplify the equation (3.10a).

We first multiply this term by $(\frac{L}{d}+\sqrt{(\frac{L}{d})^2-8\frac{S_1}{d}})$ in both the numerator and the denominator. Equation (3.10a) becomes:

$$t_{sop} = \frac{4\frac{S_1}{d}}{\frac{L}{d}+\sqrt{(\frac{L}{d})^2-8\frac{S_1}{d}}}T$$

$$= \frac{4S_1}{L+\sqrt{L^2-8S_1 d}}T \qquad (3.11)$$

Noting that $d \ll L$ and $S_1 \leq 1$, we insert a second order term $(4\frac{S_1}{L}d)^2$ that can be neglected into the square root of equation (3.11) and by linear algebra

$$t_{sop} \approx \frac{2S_1}{L-2\frac{S_1}{L}d}T \qquad (3.12)$$

At this juncture, we would like to analyze the denominator term, $L-2\frac{S_1}{L}d$:

$$L - 2\frac{S_1}{L}d = 2 + S_0 - S_2 - 2\frac{S_1}{2 + S_0 - S_2}d$$

$$= 2 + S_0 - S_2 - 2\frac{S_1(2 - S_0 + S_2)}{4 - (S_0 - S_2)^2}d$$

$$= 2 + S_0 - S_2 - \frac{4S_1}{4 - (S_0 - S_2)^2}d + \frac{2S_1}{4 - (S_0 - S_2)^2}(S_0 - S_1)d \qquad (3.13)$$

Note that $(S_0 - S_1)$ and d have the same order of magnitude and are negligible if the sampling frequency is relatively high compared to the input modulating frequency. Hence the last term, $\frac{2S_1}{4 - (S_0 - S_2)^2}(S_0 - S_1)d$, is a product of small numbers, can be ignored. Similarly, we have $4 - (S_0 - S_2)^2 \approx 4$. Equation (3.12) can hence be simplified as:

$$t_{sop} \approx \frac{2S_1}{L - \frac{4S_1}{4 - (S_0 - S_2)^2}d}T \approx \frac{2S_1}{L - S_1 d}T \qquad (3.14)$$

From Figure 3.1, we obtain

$$S_{sop} = \frac{t_{sop}}{T} \qquad (3.15)$$

Hence, the pulse width of the Second-Order Polynomial sampling process is:

$$S_{sop} = \frac{2S_1}{(2 + S_0 - S_2) - S_1(S_0 + S_2 - 2S_1)} \qquad (3.16)$$

In summary, equation (3.16) is the expression of proposed Second-order Polynomial sampled point. We will describe the hardware implementation and simulation

result of this sampling process in next chapter.

It is worthwhile to note that we have presented our proposed Polynomial Sampling process using a trailing edge PWM and it is relatively straightforward to derive the same for the leading edge PWM. Note that the pulse width of our polynomial sampling process is obtained after a two-cycle delay, while in the case of the LI and δC processes, the same are obtained after one cycle. These delays are inconsequential in audio applications.

3.3 Spectrum Analysis for the Second-Order Polynomial Sampling

In the previous section, we derived the time-domain expression for the proposed Second-Order Polynomial sampling. When this expression is compared to the LI and δC expressions, we note that our derived expression is more complex than these first-order polynomial sampling processes. The added overhead can be justified by the lower non-linearity of the proposed Second Order Polynomial sampling. In this section, we will analytically derive the double Fourier series expression that will depict all signal components, signal and non-linearities. Using this derivation, we can analytically show that the non-linearities of the proposed Second-Order Polynomial sampling is indeed lower, and the magnitude can be quantified analytically (see Chapter 4). Our derivation also provides insight to a better design by allowing the designer to trade off different parameters for a given design.

For a two dimensional signal, its double Fourier series expansion [Bennett, 1948] is:

$$f(x,y) = \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} K_{mn} e^{j(mx+ny)}$$

$$= \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} A_{mn}\cos(mx+ny) + j\sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} B_{mn}\sin(mx+ny) \qquad (3.17)$$

where $$K_{mn} = \frac{1}{4\pi^2}\int_0^{2\pi}\int_0^{2\pi} f(x,y)e^{-j(mx+ny)}dxdy \qquad (3.18a)$$

$$A_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} f(x,y)\cos(mx+ny)dxdy \qquad (3.18b)$$

$$B_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} f(x,y)\sin(mx+ny)dxdy \qquad (3.18c)$$

The relationship between K_{mn}, A_{mn} and B_{mn} is:

$$K_{mn} = \frac{1}{2}A_{mn} - \frac{j}{2}B_{mn} \qquad (3.19)$$

Figure 3.2 depicts a 3-dimentional visualisation of the width of a modulated pulse train as part of the double Fourier series analysis method. The θ-axis of the graph represents a time scale normalised to the pulse width modulation carrier frequency ω_c, such that $\theta = \omega_c t$. Similarly the ϕ-axis represents a time scale normalised to the fundamental frequency of the input signal ω_s, where $\phi = \omega_s t$. The third axis represents the pulse amplitude $F(\theta, \phi)$, which has a value equal to either 0 or H, and is defined by

$$F(\theta,\phi) = \begin{cases} H & 0 \le (\theta - |\theta|_{2\pi}) \le \Omega(\theta,\phi) \\ 0 & otherwise \end{cases} \qquad (3.20)$$

where $|\theta|_{2\pi}$ denotes the nearest multiple of 2π less than or equal to θ,

$F(\theta, \phi)$ is determined by the input signal and the type of PWM sampling, and

H is the height of the wall (or amplitude of the PWM pulse) and is

usually normalized to unity.

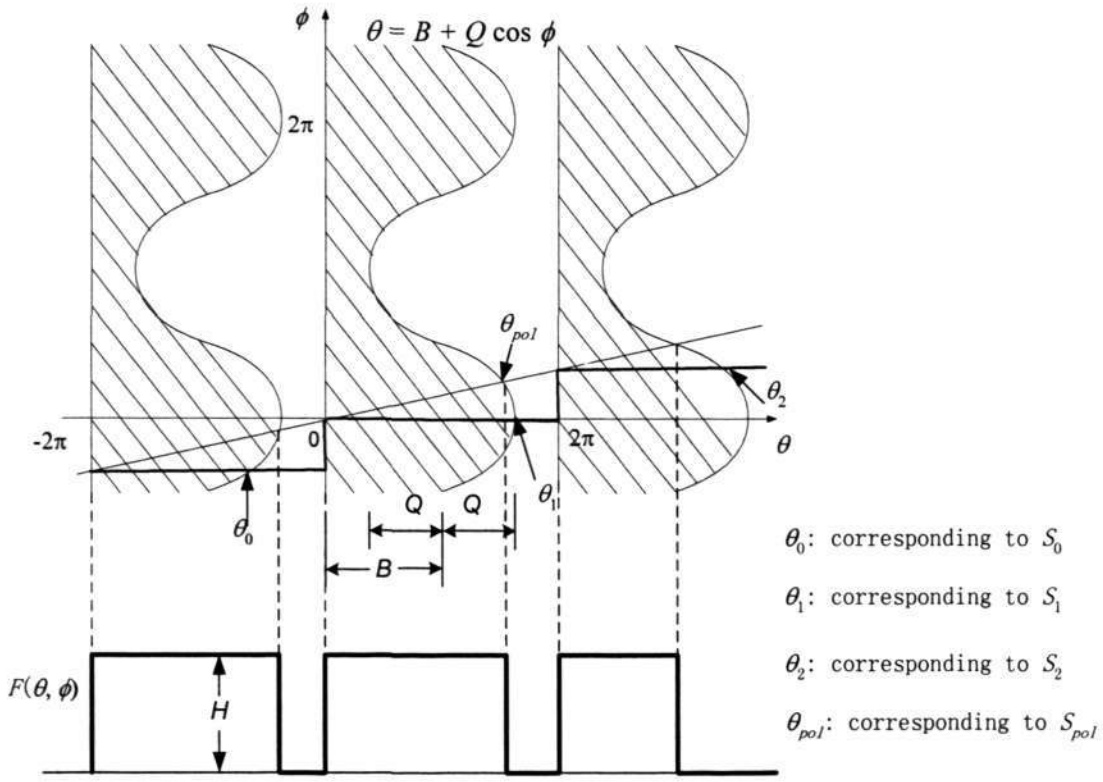


Figure 3.2 Spectrum analysis by double Fourier series

The example illustrated in Figure 3.2 is for a trailing-edge single-sided Pulse Width Modulation of a cosine wave. The function $F(\theta, \phi)$ takes the form of an infinite series of parallel walls placed at uniform intervals of 2π along the θ axis. The pulse width function in this case is defined by

$$\Omega(\phi) = B + Q\cos\phi \tag{3.21}$$

where $B = 2\pi k$ and $Q = \pi M$,

M is the modulation depth, and

the constant k, between 0 and 1, determines the width of the unmodulated pulses. When k = 0.5, the pulse train has equal

mark/space ratio before modulation.

A train of pulses of variable widths can be formed from the graph. The value of the variable ϕ at each intersection of the contour and the wall edge defines the point in the signal from which the pulse is generated. Thus, the shape of the contour defined the type of sampling required.

For our Polynomial sampling, as shown in Figure 3.3, the points θ_0, θ_1 and θ_2 respectively correspond to the sampled points S_0, S_1 and S_2 in Figure 3.1, and can be represented as

$$\theta_0 = B + Q\cos\phi_0 \tag{3.22a}$$

$$\theta_1 = B + Q\cos\phi_1 \tag{3.22b}$$

$$\theta_2 = B + Q\cos\phi_2 \tag{3.22c}$$

$F(\theta, \phi)$ is a periodic function of both variables and can be expressed as a double Fourier series. The pulse train spectrum can be obtained by evaluating the Fourier series along the sampling contour. This method cannot be directly applied to the Polynomial sampling because of the discontinuities that exist in the Polynomial sampling contour. This difficulty can be overcome by transforming the discontinuous contour into a continuous straight line. We will now derive the contour of our polynomial sampling process and explain how we overcome this discontinuity problem.

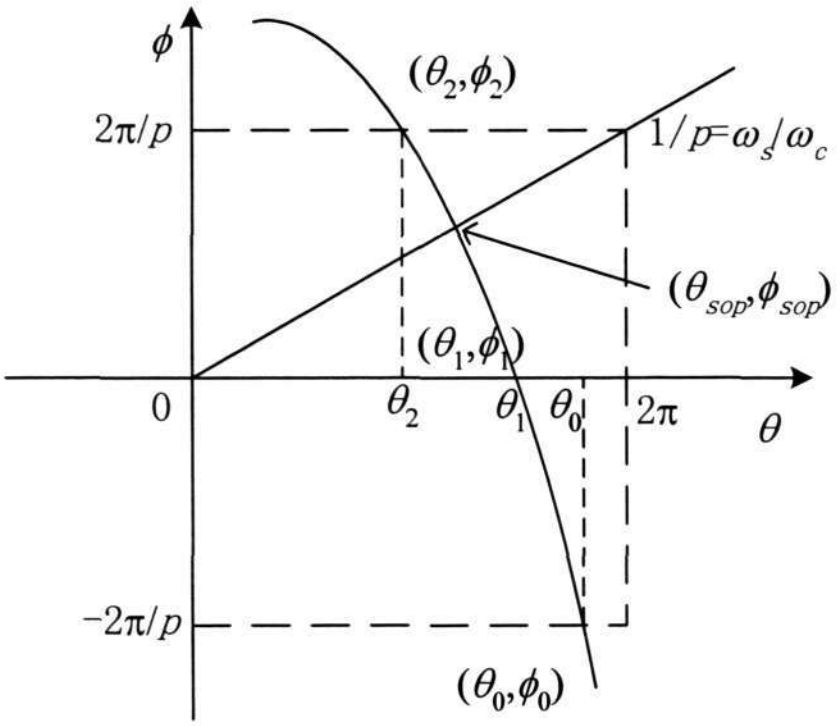


Figure 3.3 Detailed illustration of the Second-Order Polynomial single-sided trailing edge PWM sampling

The carrier function is:

$$\phi = \frac{1}{p}\theta \tag{3.23}$$

and assuming the second-order polynomial curve is

$$\theta = A\phi^2 + B\phi + C \tag{3.24}$$

with the given three points: $(\theta_0, -\frac{2\pi}{p})$, $(\theta_1, 0)$ and $(\theta_2, \frac{2\pi}{p})$,

we obtain the coefficients

$$A = \frac{\theta_2 + \theta_0 - 2\theta_1}{2(\frac{2\pi}{p})^2} \tag{3.25a}$$

$$B = \frac{\theta_2 - \theta_0}{4\pi} p \tag{3.25b}$$

$$C = \theta_1 \tag{3.25c}$$

This curve can then be expressed as:

$$\theta = \frac{\theta_2 + \theta_0 - 2\theta_1}{2(\frac{2\pi}{p})^2}\phi^2 + \frac{\theta_2 - \theta_0}{4\pi}p\phi + \theta_1 \tag{3.26}$$

and we can obtain the point ϕ_{sop},

$$\phi_{sop} = \frac{\frac{4\pi - \theta_2 + \theta_0}{4\pi}p - \sqrt{\left(\frac{4\pi - \theta_2 + \theta_0}{4\pi}\right)^2 p^2 - 2\frac{\theta_1(\theta_2 + \theta_0 - 2\theta_1)}{\left(\frac{2\pi}{p}\right)^2}}}{\frac{\theta_2 + \theta_0 - 2\theta_1}{\left(\frac{2\pi}{p}\right)^2}} \tag{3.27}$$

From equation (3.23), we can get the solution for θ_{sop} :

$$\theta_{sop} = \frac{\frac{4\pi - \theta_2 + \theta_0}{4\pi}p^2 - p\sqrt{\left(\frac{4\pi - \theta_2 + \theta_0}{4\pi}\right)^2 p^2 - 2\frac{\theta_1(\theta_2 + \theta_0 - 2\theta_1)}{\left(\frac{2\pi}{p}\right)^2}}}{\frac{\theta_2 + \theta_0 - 2\theta_1}{\left(\frac{2\pi}{p}\right)^2}} \tag{3.28}$$

We can simplify this to

$$\theta_{sop} = \pi\frac{(4\pi - \theta_2 + \theta_0) - \sqrt{(4\pi - \theta_2 + \theta_0)^2 - 8\theta_1(\theta_2 + \theta_0 - 2\theta_1)}}{(\theta_2 + \theta_0 - 2\theta_1)} \tag{3.29}$$

As

$$\theta_1 = B + Q\cos\phi_1, \quad \theta_2 = B + Q\cos\phi_2, \quad \theta_0 = B + Q\cos\phi_0 \tag{3.30}$$

and

$$\phi_1 = \left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p}, \quad \phi_2 = \left\lfloor\frac{\theta}{2\pi} + 1\right\rfloor\frac{2\pi}{p} \quad \text{and} \quad \phi_0 = \left\lfloor\frac{\theta}{2\pi} - 1\right\rfloor\frac{2\pi}{p} \tag{3.31}$$

We now obtain the polynomial sampling process contour as:

$$\Omega(\theta, \phi) = \pi\frac{4\pi - Q\cos\phi_2 + Q\cos\phi_0}{Q(\cos\phi_2 + \cos\phi_0 - 2\cos\phi_1)}$$

$$-\pi\frac{\sqrt{\left(4\pi-Q\cos\phi_2+Q\cos\phi_0\right)^2-8Q(B+Q\cos\phi_1)(\cos\phi_2+\cos\phi_0-2\cos\phi_1)}}{Q(\cos\phi_2+\cos\phi_0-2\cos\phi_1)}$$

$$=\pi\frac{\left[4\pi+2Q\sin\frac{2\pi}{p}\sin(\left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p})\right]}{-4Q\sin^2\frac{\pi}{p}\cos(\left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p})}$$

$$+\pi\frac{\sqrt{[4\pi+2Q\sin\frac{2\pi}{p}\sin(\left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p})]^2+32Q\sin^2\frac{\pi}{p}\cos(\left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p})[B+Q\cos(\left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p})]}}{4Q\sin^2\frac{\pi}{p}\cos(\left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p})} \tag{3.32}$$

As explained earlier, we need to transform this discontinuous contour into a continuous one, we will now do this. By introducing a new variable,

$$u=\phi-\left\lfloor\frac{\theta}{2\pi}\right\rfloor\frac{2\pi}{p}+\frac{\theta}{p} \tag{3.33}$$

We obtain

$$\phi=u-\frac{\theta}{p} \tag{3.34}$$

Equation (3.32) can now be written as:

$$\Omega(\theta,\phi)=\pi\frac{4\pi+2Q\sin\frac{2\pi}{p}\sin(u-\frac{\theta}{p})}{-4Q\sin^2\frac{\pi}{p}\cos(u-\frac{\theta}{p})}$$

$$+\pi\frac{\sqrt{[4\pi+2Q\sin\frac{2\pi}{p}\sin(u-\frac{\theta}{p})]^2+32Q\sin^2\frac{\pi}{p}\cos(u-\frac{\theta}{p})[B+Q\cos(u-\frac{\theta}{p})]}}{4Q\sin^2\frac{\pi}{p}\cos(u-\frac{\theta}{p})} \tag{3.35}$$

We introduce another term Φ to represent $(u-\frac{\theta}{p})$:

$$\Phi = u - \frac{\theta}{p} \quad \text{and} \quad d\Phi = du \tag{3.36}$$

and the contour now becomes:

$$\Omega(\theta,\phi) = \pi \frac{4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)}{-4Q\sin^2\frac{\pi}{p}\cos(\Phi)} + \pi \frac{\sqrt{[4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)]^2 + 32Q\sin^2\frac{\pi}{p}\cos(\Phi)[B + Q\cos(\Phi)]}}{-4Q\sin^2\frac{\pi}{p}\cos(\Phi)} \tag{3.37}$$

By multiplying with

$$[4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)] + \sqrt{[4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)]^2 + 32Q\sin^2\frac{\pi}{p}\cos(\Phi)[B + Q\cos(\Phi)]}$$

in both the numerator and denominator of equation (3.36), we obtain:

$$\Omega(\theta,\phi) = 8\pi \frac{B + Q\cos(\Phi)}{[4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)] + \sqrt{[4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)]^2 + 32Q\sin^2\frac{\pi}{p}\cos(\Phi)[B + Q\cos(\Phi)]}} \tag{3.38}$$

Similarly, by adding the following into the square root of equation (3.37)

$$\left(\frac{16Q\sin^2\frac{\pi}{p}\cos(\Phi)[B + Q\cos(\Phi)]}{4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)}\right)^2$$

equation (3.37) becomes:

$$\Omega(\theta,\phi) = 8\pi \frac{B + Q\cos(\Phi)}{2[4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)] + \frac{16Q\sin^2\frac{\pi}{p}\cos(\Phi)[B + Q\cos(\Phi)]}{4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)}} \tag{3.39}$$

If p is large, we can neglect the difference between θ_0 and θ_2, and we can simplify equation (3.39) to

$$\Omega(\theta,\phi) = 8\pi \frac{B+Q\cos(\Phi)}{2[4\pi + 2Q\sin\frac{2\pi}{p}\sin(\Phi)] + 4M\sin^2\frac{\pi}{p}\cos(\Phi)[B+Q\cos(\Phi)]}$$

$$= \frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)] + M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]} \qquad (3.40)$$

By substituting equation (3.40) into the Fourier coefficients in Equation (3.18a), we can determine the Fourier coefficient K_{mn}

$$K_{mn} = \frac{1}{4\pi^2}\int_0^{2\pi}\int_0^{2\pi} f(\theta,u)\exp\left[-j(m\theta+nu)\right]d\theta du$$

$$= \frac{1}{4\pi^2}\int_0^{2\pi}\int_0^{\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}} f(\theta,\Phi)\exp\left\{-j\left[m\theta+n(\Phi+\frac{\theta}{p})\right]\right\}d\theta d\Phi$$

$$= \frac{jH}{4(m+\frac{n}{P})\pi^2}\int_0^{2\pi}\exp(-jn\Phi)$$

$$(\exp\left\{-j(m+\frac{n}{p})\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)] + M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\} - 1)d\Phi$$

(3.41)

There are four possible cases. They are:

Case 1: Inter-modulated term ($m \neq 0$ and $n \neq 0$)

$$K_{mn} = \frac{jH}{4(m+\frac{n}{P})\pi^2}\int_0^{2\pi}\exp(-jn\Phi)$$

$$\exp\left\{-j(m+\frac{n}{p})\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)] + M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\}d\Phi$$

(3.42)

Letting

$$I_{mn} = \int_0^{2\pi} \exp(-jn\Phi) \exp\left\{-j(m+\frac{n}{p})\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\} d\Phi \tag{3.43}$$

$$\therefore \quad A_{mn} = 0 \tag{3.44a}$$

$$B_{mn} = -\frac{H}{2(m+\frac{n}{P})\pi^2} I_{mn} \tag{3.44b}$$

Case 2: Modulating signal ($m \neq 0$ and $n = 0$)

$$K_{m0} = \frac{jH}{4m\pi^2}\int_0^{2\pi} e^{-jm\{\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\}} d\Phi - \frac{jH}{2m\pi} \tag{3.45}$$

Letting

$$I_{m0} = \int_0^{2\pi} \exp\left\{-jm\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\} d\Phi \tag{3.46}$$

$$\therefore \quad A_{m0} = 0 \tag{3.47a}$$

$$B_{m0} = \frac{H}{m\pi} - \frac{H}{2m\pi^2} I_{m0} \tag{3.47b}$$

Case 3: DC component ($m = 0$ and $n = 0$)

$$K_{00} = \frac{1}{4\pi^2}\int_0^{2\pi}\int_0^{\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}} f(\theta,\Phi)d\theta d\Phi$$

$$\approx \frac{H}{4\pi^2}\int_0^{2\pi}(B+Q\cos\Phi)d\Phi$$

$$= \frac{HB}{2\pi}$$

$$= Hk \tag{3.48}$$

$$\therefore \quad A_{00} = 2Hk \tag{3.49a}$$

$$B_{00} = 0 \tag{3.49b}$$

Case 4: Carrier and its associated harmonics ($m = 0$ and $n \neq 0$)

$$F_{0n} = \frac{1}{4\pi^2} \int_0^{2\pi} \int_0^{\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}} f(\theta,\Phi)$$

$$\exp\left[-jn(\Phi+\frac{\theta}{p})\right] d\theta d\Phi$$

$$= \frac{jH}{4\frac{n}{P}\pi^2} \int_0^{2\pi} \exp(-jn\Phi)$$

$$\exp\left\{-j\frac{n}{p}\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\} d\Phi$$

(3.50)

Letting,

$$I_{0n} = \int_0^{2\pi} \exp(-jn\Phi)$$

$$\exp\left\{-j\frac{n}{p}\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\} d\Phi$$

(3.51)

$$\therefore \quad A_{0n} = 0 \tag{3.52a}$$

$$B_{0n} = -\frac{H}{2\frac{n}{P}\pi^2} I_{0n} \tag{3.52b}$$

Finally, the one-sided PWM spectrum of our Polynomial sampling is

$$F_{sop}(t) = k - \sum_{n=1}^{\infty} \frac{I_{0n}}{2\frac{n}{p}\pi^2}\sin(n\omega_s t)$$

$$+\sum_{m=1}^{\infty}\left[\frac{\sin(m\omega_c t)}{m\pi} - \frac{I_{m0}}{2m\pi^2}\sin(m\omega_c t)\right]$$

$$-\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{I_{mn}}{2(m+\frac{n}{p})\pi^2}\sin(m\omega_c t + m\omega_s t) \qquad (3.53)$$

where

$$I_{0n} = \int_0^{2\pi} \exp(-jn\Phi)$$

$$\exp\left\{-j\frac{n}{p}\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\}d\Phi$$

(3.54a)

$$I_{m0} = \int_0^{2\pi} \exp\left\{-jm\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\}d\Phi$$

(3.54b)

$$I_{mn} = \int_0^{2\pi} \exp(-jn\Phi)$$

$$\exp\left\{-j(m+\frac{n}{p})\frac{2[B+Q\cos(\Phi)]}{[2+M\sin\frac{2\pi}{p}\sin(\Phi)]+M\sin^2\frac{\pi}{p}\cos(\Phi)[2k+M\cos(\Phi)]}\right\}d\Phi$$

(3.54c)

As in the other double Fourier series expressions for reported sampling processes, we will now interpret equation (3.53). The first term k is the DC component of the

resultant PWM output and, as before, is of no consequence as it is easily accommodated. The second term represents the input modulating signal and its harmonics – the main source of THD. The third term corresponds to the carrier and its associated harmonics, and can be effectively attenuated by the low-pass filter at the output of the output stage. As the carrier frequency is well above the audio band, the effect of this term on THD is negligible. The last term represents the modulating signal and its harmonics inter-modulated with the carrier and its harmonics. It is the second term that we are particularly interested in and in Chapter 4, we will compare the THD of our proposed sampling against other processes using the double Fourier series expressions and by other simulations. We will also compare the derived double Fourier series expression equation (3.53) against our derived time domain equation (3.16) in Chapter 4 and show that they agree well.

3.4 Conclusions

In this chapter, we have proposed a novel sampling process – the Second-Order Polynomial sampling process and we have derived its double Fourier series expression.

Chapter 4 Hardware Description and Simulation Results

4.1 Introduction

In this chapter, we will describe how we implement our Second-Order Polynomial sampling process and the accompanying pulse generator, hence the complete PWM in Fig 2.1. We will also present the simulation results of the complete PWM using hardware synthesized from EDA tools and compare them with the analytical double Fourier series expression we derived in Chapter 3. This comparison serves to verify our analytical derivation in Chapter 3. Finally we will compare our Second-Order Polynomial sampling process against the LI and δC, and compare several PWM designs based on different pulse generator resolutions. In presenting the results of our Second-Order Polynomial sampling process, we will use both the time-domain and the double Fourier series expression. A comparison of the results from both expressions serves to verify the derivation of double Fourier series.

4.2 Hardware Description of the Second Order Polynomial Sampling Process

We depict in Figure 4.1 the block diagram of our hardware implementation of our Polynomial sampling process. This hardware realises equation (3.16) in Chapter 3. We will now explain the operation of the circuit in Figure 4.1.

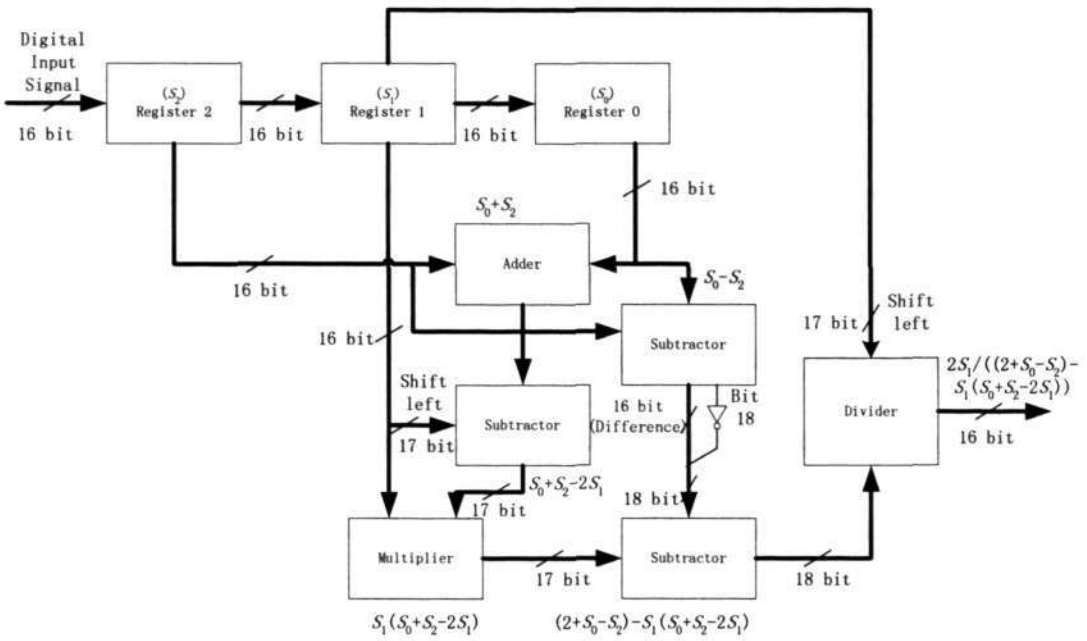


Figure 4.1 Block diagram of the Second–Order Polynomial sampling process

Registers 0, 1, and 2 are 16 bits in wordlength. The operation commences when Register 2 stores the present sampled digital input signal as S_2. The previous sampled input signal from Register 2 is, at the same time, passed to Register 1 as S_1 and the sample two sampling periods before from Register 1 is passed to Register 0 as S_0. The adder adds S_0 and S_2, thereby obtaining (S_0+S_2), a sum with a 17-bit wordlength. Similarly, the result of the first subtraction $(S_0+S_2-2S_1)$ may be up to 17-bit wordlength, and is multiplied by S_1 to obtain $S_1(S_0+S_2-2S_1)$, an 18-bit wordlength result. The second subtraction will subtract the value of S_2 from S_0 to obtain S_0-S_2. This S_0-S_2 is added with a normalised '2' as in Equation (3.16). We note that the subtraction process of S_0-S_2 results in a 17-bit two's complement output comprising the difference bits and an MSB as the borrow bit which also acts as a sign bit. When the sign bit is logic 0, the addition process of $2+(S_0-S_2)$ is a normal

binary addition. When the sign bit is logic one, the value of S_0-S_2 is a negative number in two's complement form with the difference bits indicating the amount of overflow from the full scale value. An addition of the negative number in two's complement number with the full scale will always yield the amount of overflow from full scale value (the difference bits). From these two cases, we summarise the addition operation as follows: the MSB of full scale (logic 1) will always invert the borrow bit while the remaining bits (all logic 0), will not change the value of the difference bits. The result of the final subtraction $(2+S_0-S_2)-S_1(S_0+S_2-2S_1)$ is also 18 bits and goes to the input of the divider. The final result of $2S_1/((2+S_0-S_2)-S_1(S_0+S_2-2S_1))$ will be available at the quotient output of the divider.

For the multiplier, we use the sequential method [Parhami, 2000], an approach that dissipates lower power than the usual parallel approach based on a partial product Generator and Adder Block. In this approach, from the LSB to the MSB of S_1, if the value of corresponding bit is 1, we will add the value $2+S_0-S_2$ to the result of and then shift the value $2+S_0-S_2$ one bit left. If the corresponding bit is 0, the result remains, that is, there is no operation. The upper 18 bits of result will be the output of multiplier. Division, on the other hand, is the opposite operation of the multiplier. In this case, the dividend will be compared to the divisor. If the former is smaller, the corresponding output bit will be 0 and while if it is larger, the output bit will be 1 and a subtraction process will be performed. After 16 above iterations, the result of $2S_1/[(2+S_0-S_2)-S_1(S_0+S_2-2S_1)]$ will be obtained.

In our design, the following sub-circuit of the PWM circuit, the pulse generator, contains a Noise Shaper and a Fast-Clock Counter, shown in Figure 4.2. The noise shaper is constructed by an adder and two D-flip-flops. The 16-bit Second-Order Polynomial sampled data will be added with previous 5-bit LSB (feedback error), the resultant 11-bit MSB (quantized output) is output to port *A* of the comparator through a D-flip-flop, and the 5-bit LSB is fedback to be added with the next input. The counter will count up from zero and outputs to port *B* of the comparator. Initially, the F_{sw} clock will set the output PWM signal to high and upon the condition *A*=*B* meets, it resets the PWM signal. The PWM pulse output is hence generated.

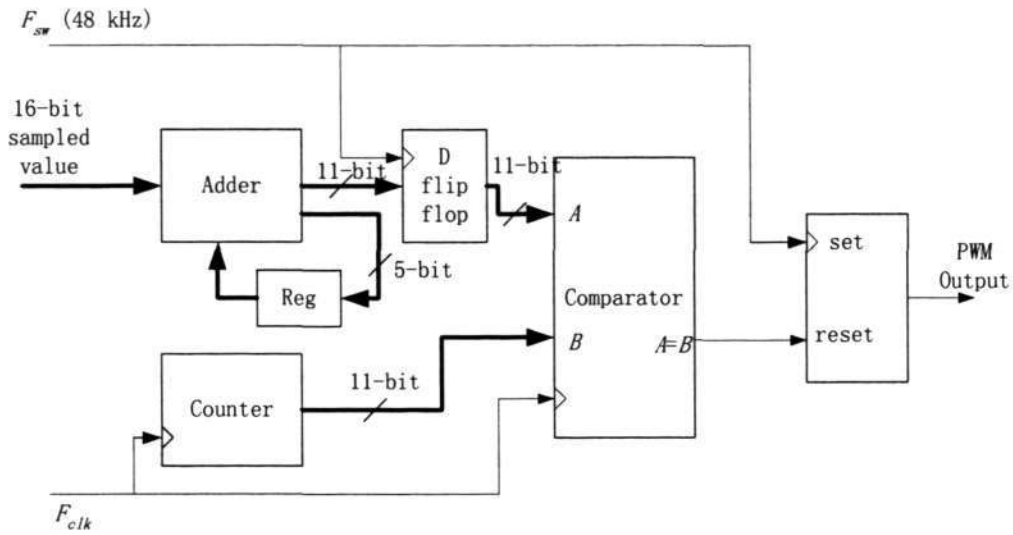


Figure 4.2 PWM pulse generator structure

At this juncture, we note that the data flow in the hardware for the Polynomial sampling process is sequential. This means that a new sequence of operations begins only when the input changes. With a sequential approach, the data that will

be sent from the registers to the divider and finally to the PWM pulse generator are actual data – there is essentially no spurious data that would otherwise result in unnecessary power dissipation.

Using EDA tools, we depict in Figure 4.3 to Figure 4.5 the circuit schematic of synthesized hardware. In Figure 4.3, we plot the whole synthesized solution of this design, it contains four sub-block with specific functions:

(1) the "se_polynomial" block serves to generate the corresponding sampled value, it contains 3 subtractors, 1 multiplier and 1 divider;

(2) The "noise_shaper" block serves to reduce the wordlength of the sampled value;

(3) The "freqdivider_90MHz" serves to generate the related clocks and the counter, and

(4) The "pwmgen" block serves to generate the PWM pulse.

Figure 4.4 depicts the details of the synthesized noise shaper where the 16 sub-blocks are full adders. The output of five full adders on the left of Figure 4.4 is looped back as the input of full adders at next clock edge. The output of the eleven full adders on the right will be output to the pulse generator. Figure 4.5 depicts the synthesized pulse generator, a very simple structure.

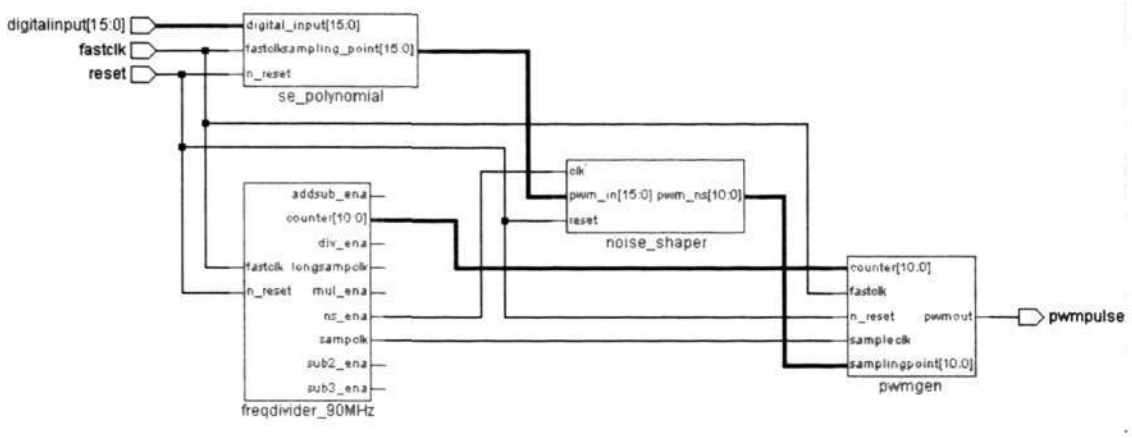


Figure 4.3 Circuitry of Polynomial PWM

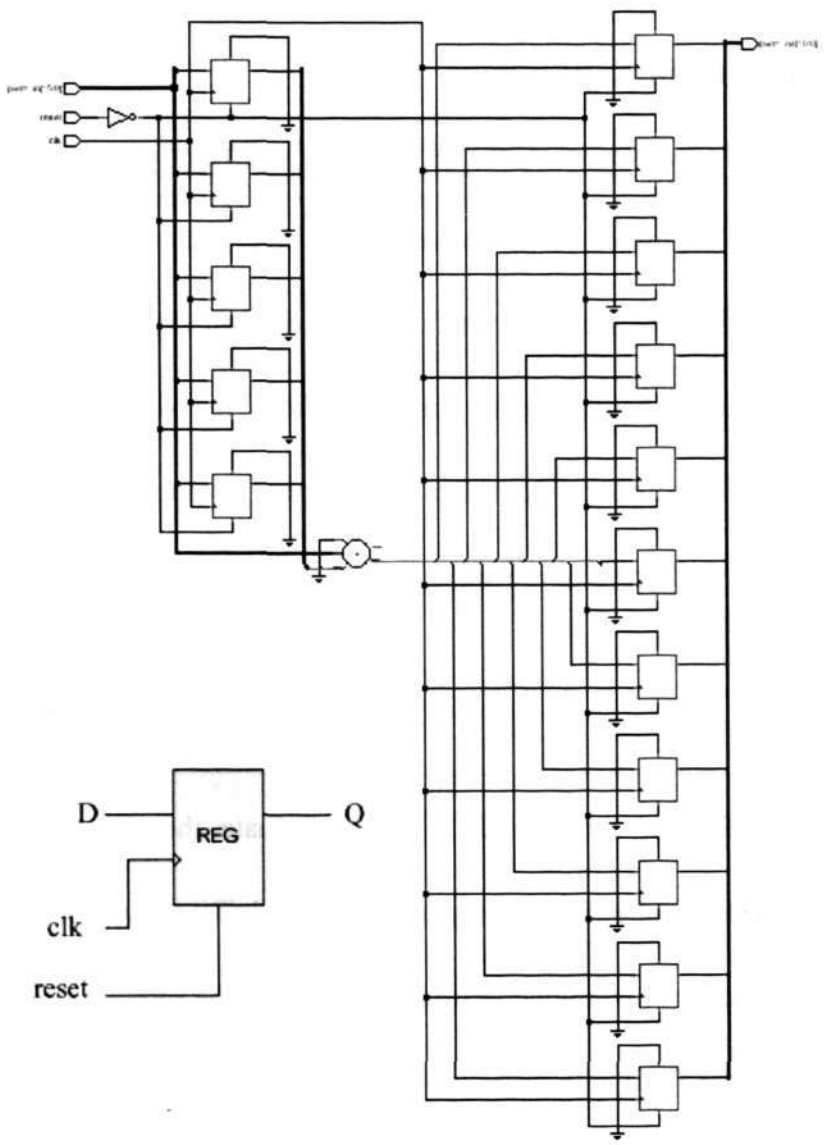


Figure 4.4 Synthesized Noise Shaper

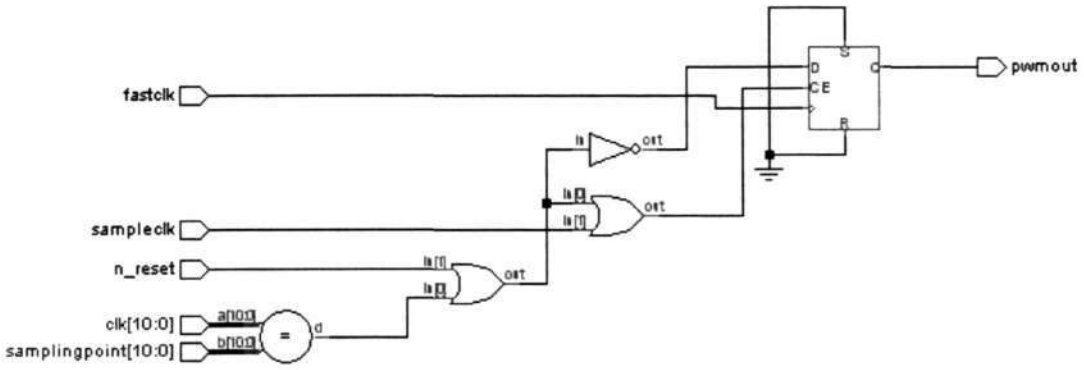


Figure 4.5 Synthesized pulse generator based on Fast-Clock Counter approach

4.3 Simulation Results Based on Double Fourier Series and Time-domain Expressions

In Chapters 2 and 3, we presented our proposed sampling process and derived the corresponding double Fourier series expression. We will now use our derived double Fourier series expression and verify that the derived expression is precise by comparing the harmonic components (obtained from the double Fourier series expression) against simulations from the time-domain expression (obtained from equation (3.16)). Both results are taken at the output of the low-pass filter (in Figure 2.1).

Using the double Fourier series expression to evaluate the extent of harmonic distortion on the THD of the different algorithmic-based sampling processes, we use MATLAB to compute the magnitude of each harmonic of the sampling processes and thereafter calculate the THD with respect to the modulation index, M. We note that the integral in the second term of equation (3.54a) is a complex term comprising real

and imaginary components. As this term appears to be mathematically intractable, we employ the numerical integration method in the simulations to determine the magnitude of the individual signal harmonics. Based on the definition of THD in equation (2.1), we determine the discrete harmonics component up to the 20^{th} term where each harmonic component is determined by numerically integrating in the range from 0 to 2π and the step is 0.00001. The THD of the different sampling processes based on the double-Fourier series expression is given in Figure 4.6 below.

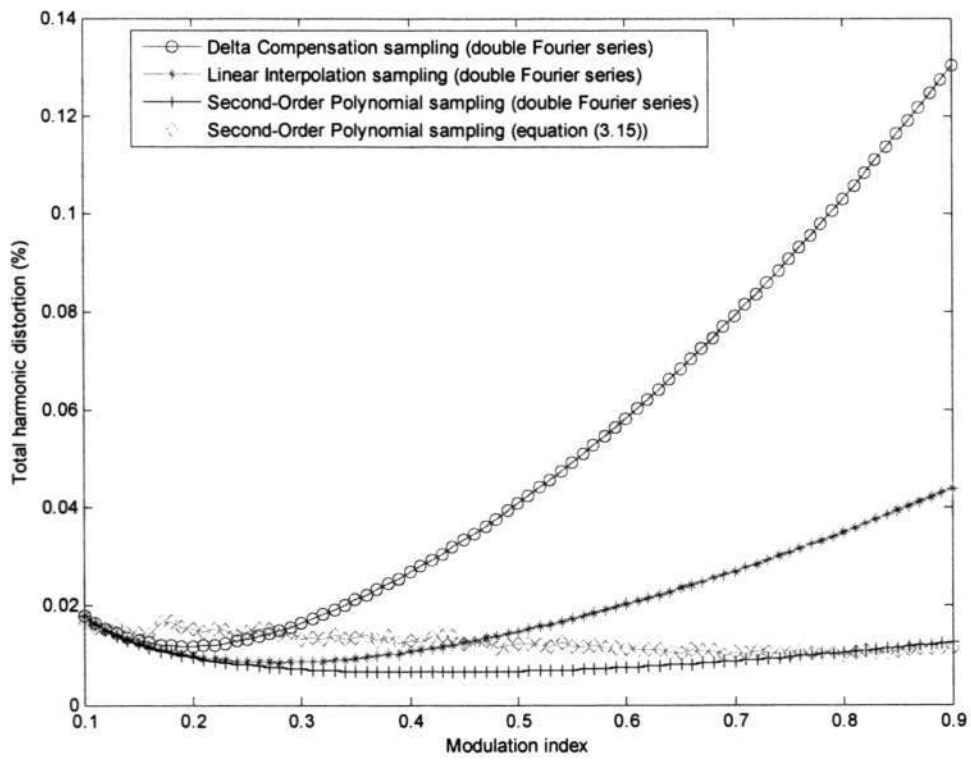


Figure 4.6 THD of different sampling processes based on double Fourier series expressions

For the proposed Second-Order Polynomial sampling, we also plot the THD based on

simulations obtained from equation (3.16); this serves to verify the derived double Fourier series expression. For completeness, we remark that we do not need to include the simulations from the time domain expression for the LI and δC processes as the double Fourier series for these processes have been verified elsewhere [Gwee, *et.al.*, 2002; Gwee, *et.al.*, 2003].

In Figure 4.6, the abscissa is modulation index of the input signal while the ordinate is the %THD. As the THD of the NS process is zero, we exclude it in Figure 4.6. For all these algorithmic-based sampling processes, they take a "U" shape. The reason for this is that at the small modulation indexes, the noise component is relatively larger and affects (masks) the THD, while at the large modulation indexes, the THD is as expected, larger. For the Second-Order Polynomial sampling process, we remark that as its sampled point is closer to the Natural sampled point, its THD is the lowest of the processes compared. As a case in point, for p=48 and at near maximum signal swing at modulation index M=0.9, the THD of the Second-Order Polynomial process is respectively ~3 times and ~10 times better than the LI and δC processes.

As a means to verify the derived double Fourier series expression for the Second Order Polynomial expression, we use the pulse width given in equation (3.16) and by using the Fast Fourier Transform (FFT) in MATLAB, we can determine the discrete harmonic components. The THD performance in simulation was evaluated until

the 9th harmonic component and we superimpose the THD in Figure 4.6.

From Figure 4.6, the THDs obtained from both methods agree well, hence verifying our derived double Fourier series expression.

4.4 Simulation Results Based on Synthesized Hardware

In the last section, we presented results based on the sampling processes alone. In this section, we will present results for the entire PWM comprising both the sampling process and the pulse generator. The different sampling processes include the δC, LI and our SOP. In these simulations, we will employ the synthesized hardware described earlier.

The table below summarises the computation complexity of the various processes. Compared to δC and LI sampling processes, the added hardware of our Second-Order Polynomial sampling process is one addition, two subtractions and one multiplication (division).

Table 4.1 Comparison of the computation complexity for different processes

Process	Addition	Subtraction	Shifter	Multiplication	Division
δC	1	1	1	1	0
LI	0	1	1	0	1
SOP	1	3	1	1	1

We depict the harmonic distortions of the different PWMs embodying the different PWM processes with the same pulse generator with 11-bit resolution, in Figure 4.7.

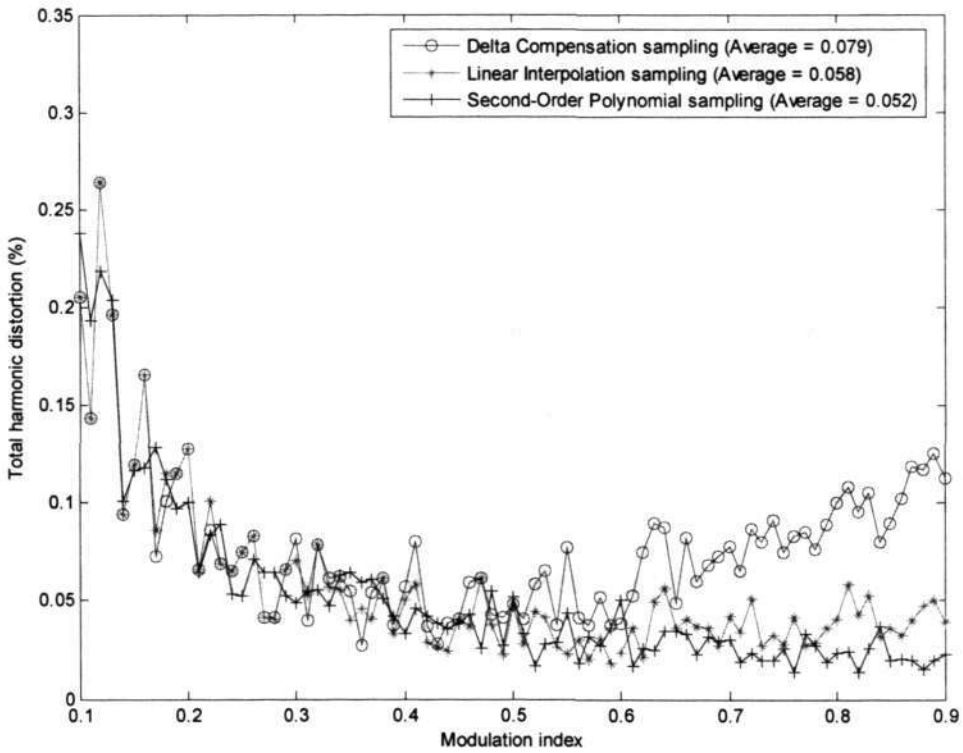


Figure 4.7 The THD comparison between different sampling processes using time domain expressions and with 11-bit pulse generator resolution

We note here that the harmonic distortion of the Class D amplifier embodying the proposed Polynomial sampling and the 11-bit pulse generator is better than the Class D amplifier embodying the δC or LI sampling processes and the 11-bit pulse generator. The THD of the PWMs between that based on LI and the Second-Order Polynomial sampling process is somewhat close and this is largely due to the low resolution pulse generator; the comparison of the sampling processes was presented in the last section.

We described in Chapter 3 that with the noise shaper applied to our proposed sampling process, we can reduce the resolution and this results in reduced power dissipation. We depict in Figure 4.8 the THD of the PWM embodying the proposed Second-Order Polynomial sampling process and a pulse generator with first order, second order and without Noise Shaper. As expected, the design embodying the 2nd order pulse generator yields the best design but at the cost of increased hardware complexity.

We note that the average THD of a digital Class D amplifier embodying 1st order Noise shaper and 11-bit resolution, is 0.030%. This is the approach that we recommend for a mid-level high-fidelity digital Class D amplifier.

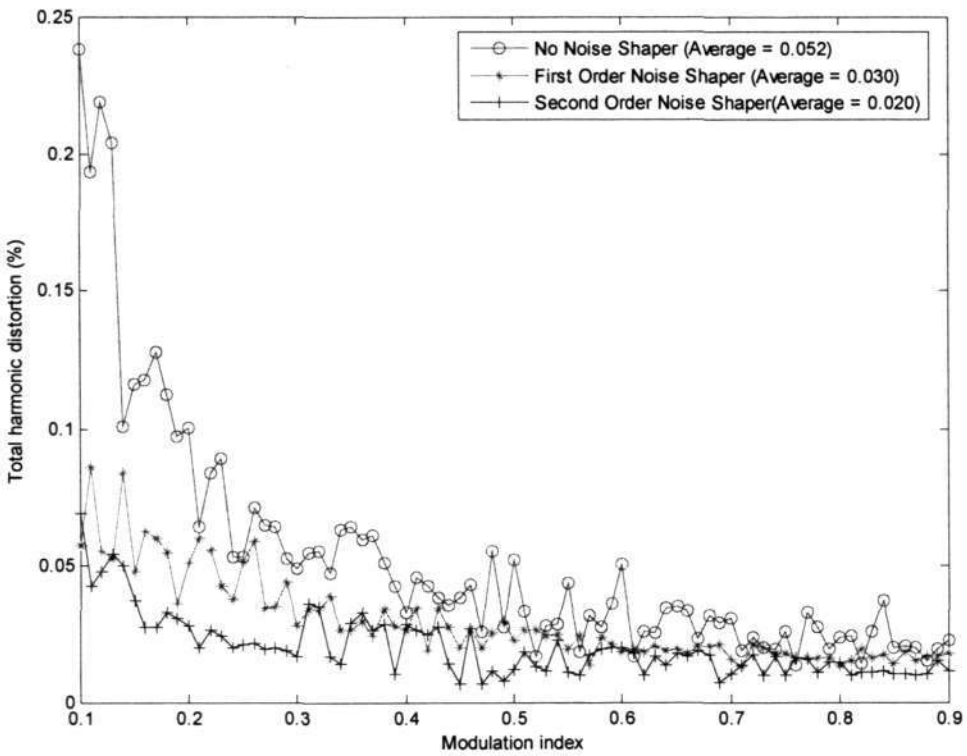


Figure 4.8 THD comparison of noise shaper effect (11-bit resolution)

4.4 Conclusions

In this chapter, we have described the hardware implementation for our proposed Second-Order Polynomial sampling process, together with simulation results and comparison with other sampling processes. Based on these results, we have shown that the proposed sampling process featured lower harmonic non-linearity than the prevalent δC and LI sampling processes. We have also verified our derived double Fourier series expression by comparing its harmonic components against that obtained from the time-domain expression.

Chapter 5 Conclusions and Recommendation for Future Work

5.1 Conclusions

In this dissertation, we have described the motivation, objectives, literature review and details of our research work and they all pertain to the design and implementation of a digital Class D amplifier based on the PWM approach. The primary criteria for this design include low THD, low computation leading to low power dissipation and small IC area.

In this dissertation, we have reviewed digital Class D amplifiers. Our focus has been on the digital Class D amplifier based on the PWM for its low hardware complex, lending itself appropriate for power-critical small IC-area application and with low Total Harmonic Distortion non-linearity. In view of this, we have proposed a new sampling process termed Second-Order Polynomial sampling that aims to emulate the NS process but with low computation needs.

We have also analytically derived the double Fourier expression for the Second-Order Polynomial sampling process. The analysis has yielded an expression that analytically describes all signal components of the Second-Order Polynomial sampling, including the non-linearity terms (and harmonic components of the fundamental modulating signal). We have explained that this analysis is useful

because it provides insight to the designer, enabling him/her to trade different parameters of the design to achieve a given set of specifications.

We have reviewed pulse generators, the sub-circuit following the sampling process in a PWM-based digital Class D amplifier. We have designed a pulse generator for our Class D amplifier. The emphasis in our design is to reduce the wordlength of the data, thereby reducing the clock rate of the counter embodied in the pulse generator. Reducing the clock rate would reduce the power dissipation of the Class D amplifier.

We have compared our proposed sampling process against the common PWM sampling processes that feature low computation, the δC and LI sampling processes. Although the computation of our sampling process is more complex than the δC and LI processes, we are of the opinion that the lower non-linearity of our proposed process makes it worthy for consideration in power-critical application where lower non-linearity is desired.

We have verified that our derived double Fourier series expression is precise.

5.2 Recommendation for Future Work

We propose the following for future work:

(ii) Due to the limited duration in a Master of Engineering candidature, the work presented herein would be more complete if our design were to be realized in an integrated circuit and measurements made.

(iii) We propose to employ a more mathematically-oriented computation to better estimate the sampling point using 3 data points. At present, our methodology appears to be somewhat simplistic and this is largely due to our preserving the simplicity of the computation. Nevertheless, we believe that it may be possible to simplify a more mathematical-oriented computation approach to yield even lower non-linearity.

(iv) We observe that the digital Class D amplifiers based on the PWM approach are essentially feed-forward designs. We suggest an investigation into the application of negative feedback. We are of the opinion that if negative feedback can be effectively applied, the wordlength and associated clock rate can be further reduced, thereby obtaining an even lower power design.

(v) The double Fourier series expression presented in our review and in our derivation for our proposed sampling process depicts non-linearities other than harmonic distortion. We propose an investigation into these non-linearities, in particular when the ratio of the sampling

frequency/modulating input frequency is low and where the modulation index is high.

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