Effect of thermal-induced stress on SOI power devices

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**The Effect of Thermal-induced Stress on
SOI Power Devices**

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SUMMARY

Silicon-on-insulator (SOI) technology presents one way of fabricating semiconductor devices on an insulating substrate rather than in a semiconductor bulk. It is a promising potential technology for the next generation ULSI because of its many advantages over its bulk silicon substrate counterpart, such as immunity to radiation, reduction in parasitic capacitance, reduction in power delay product, high packing density and simplicity in manufacturing process, and elimination of metal spike etc. Owing to these advantages, SOI CMOS technology has been gradually recognized as a promising ULSI technology. In addition to ULSI application, SOI technology has also been used to realize communication circuits, microwave devices, and even fiber optics application for its superior performance. With the growing trends of the portable systems, low-voltage and low-power designs have been indispensable. In this aspect, SOI technology is suitable for integration of the low-voltage and low-power VLSI circuits, because of the steeper subthreshold slope feature of SOI CMOS devices.

However, direct application of SOI technology to power semiconductor devices would result in poor heat dissipation that is unacceptable. Meanwhile, there are other shortcomings arising, such as reduction in breakdown level and self-heating problem. To overcome these disadvantages, one promising structure, namely partial SOI (PSOI), was proposed. This new partial SOI structure, which combines the advantages of SOI and junction isolation (JI) technologies, realizes an improved RESURF effect, higher breakdown voltage and reduced self-heating effect as compared to the conventional SOI structure. Although this structure is much better

than conventional SOI, especially in the application of power devices and PICs, its Electrical-Thermal-Stress coupled-field effects and fabrication remain the key issues.

Devices on partial SOI structure in other research groups have shown improved performance compared with those on full SOI structure. However, few studies in literature were focused on the thermal-induced stresses generated in the PSOI structure during device fabrication, which affect the device performance accordingly.

In this work, finite element models are built to study the distribution of thermal-induced stresses in partial SOI structure. It is found that the stress distribution at the work layer/substrate interface is more non-uniform than that at the surface since stress concentration is expected at the oxide edge and corner. Maximum stresses at both the surface and the interface are dependent on structural parameters, including oxide length (and width), oxide thickness, substrate thickness and work layer thickness. Such stress concentration could pose a reliability problem of PSOI devices if its value is too excessive due to improper device design.

In order to assist device designers to take into account of the stress distribution in a partial SOI structure effectively, empirical stress model as a function of the various structural parameters were built using the Response Surface Method (RSM). These statistical models were applied to optimize the structural parameters.

Following that, an electrical-thermal-stress (E-T-S) coupled-field simulation is developed, taking into consideration of the E-T-S interaction in a semiconductor device from the first principle via semiconductor band structure modification. This model is then applied to the study of SOI and PSOI lateral power diodes as well as LDMOSFETs. Their static I-V characteristics as well as the temperature and thermo-

mechanical stress distributions in the devices are computed using E only, E-T and E-T-S models. Comparing the electrical characteristics of SOI and PSOI power devices using the E-T-S model, we observed that power devices in PSOI possesses higher reverse breakdown voltage due to its better RESURF and lower device temperature.

In addition, fabrication of partial SOI with wafer bonding is proposed. A new method that combines SIMOX and wafer bonding for the fabrication of partial SOI structure is suggested in this work.

Chapter 1 INTRODUCTION

1.1 Motivation

While Silicon on insulator (SOI) has already become a mature technology for low power CMOS circuits when IBM launched the first fully-functional SOI mainstream microprocessor in 1999, it is still an emerging technology for high voltage integrated circuits [1,2]. However, it was found that conventional SOI power devices suffer from reduced breakdown voltage and the self-heating effect [3,4].

Over the past few years, a promising technology, partial Silicon on Insulator (PSOI), has attracted much attention in power integrated circuits (PICs) to overcome these problems efficiently. PSOI structure had been proposed due to its higher breakdown voltage and better heat dissipation than full SOI structure [5,6,7,8]. Researchers in Cambridge University started to focus on the partial SOI technology from 1997 [8,9,10,11]. Numerical simulations demonstrate that PSOI technology solved the two major problems associated with conventional SOI technology, namely the reduced breakdown voltage and self-heating. At the same time, PSOI maintain good isolation between the low power CMOS circuits and the high power cells. In integrated circuit research community, increased effort is now directed towards

developing SOI power device for system on chip (SOC). PSOI could be the future technology for power integrated circuits [12,13].

In PSOI technology, one of the key issues is the fabrication of the PSOI structure. To date, PSOI power devices have not been fabricated with good performance, even though a numerous numerical simulations have been done. Although PSOI structure can be achieved by selective SIMOX, recrystallisation, or selective silicon and oxide etching followed by selective epitaxial growth, local oxidation followed by wafer bonding is also possible[14, 15, 16, 17]. The first technique mentioned above has the shortcomings of traditional SIMOX, such as the low quality of the films. Large thermal stresses and film non-uniformity occur with the second technique, recrystallisation. The third one is very complicated and not suitable for mass production. A large thermal stress is also one serious issue in wafer bonding if we use the traditional method that needs high temperature annealing. Thus, one of the crucial factors faced now is PSOI structure fabrication. Recently, low temperature wafer bonding was developed [18], and with this technology, a method of fabricating PSOI is proposed.

PSOI has the material structure of a substrate with multiple-thin-layer (patterned buried oxide and SOI work layer) overlays and especially with disconnected regions in buried oxide layer. Stresses are always concomitant with this multi-layer structure considering the higher thermal field in the PICs. As we known, stresses are small in the substrate by virtue of its much larger thickness than the overlays. However, in the discontinuities of the patterned buried oxide, large localized stresses can occur at the interface [19].

The thermal-induced stresses are pervasive and critical in many issues of power devices in PSOI structure. For example, residual stress in the silicon work layer

will affect the electron mobility [20,21] and hall mobility [22] in the layer. The influence of externally applied stress on electrical characteristics of electronic devices has been investigated for many years such as the piezoelectric effect [23]. However, most of the investigations applied to sensor development rather than digital or analog IC. In this work, electrical-thermal-stress (E-T-S) coupled-field simulation of power devices in PSOI structure using the low temperature wafer bonding technique will be performed.

With the above-mentioned effect of stress on device performance, and the serious self-heating effects in power devices, the study of the distribution of thermal-induced stresses in PSOI structure and stress effects on PSOI power devices are necessary. The E-T-S coupled field model for PSOI was build and the severity of the thermal and stress effects will be examined in this work.

1.2 Objective

This project can be divided into the following three phases.

The first phase mainly focuses on the distribution of thermal-induced stresses in PSOI structures. Finite Element Method (FEM) was used in this work. With the statistical models, the geometrical parameters of the structure could be optimized to effectively reduce the thermal-induced stresses in the PSOI structures.

The analysis and quantitatively modeling of the electrical-thermal-stress effects on power devices is the second phase. Theoretical analysis along with coupled-field simulation validates the results and allows a better understanding of the E-T-S effect interactively.

The third phase explores the application of E-T-S coupled-field model to partial SOI and conventional SOI power devices including lateral power rectifier and LDMOSFETs. Their thermal characteristics and stress effects will be compared at the same operating conditions. The comparison of the E only, E-T and E-T-S models will also be made from the calculation to examine the significance of the E-T-S model.

1.3 Contribution of the Thesis

The major contributions of the thesis cover four aspects

(1) Analysis of the thermal-induced stresses in PSOI structure fabricated on the low temperature wafer bonding technology using ANSYS. The maximum stresses at the surface and interface of PSOI are reduced dramatically by optimized structure dimension as compared to the conventional SOI. Two important parameters in device structure, namely buried oxide thickness and work layer thickness, are identified in Partial SOI structure.

(2) Electrical-Thermal-Stress coupled-field model is developed for power devices. For the E-T coupled-field simulations, the heat transfer equation was solved together with the Poisson and continuity equations for electrons and holes. The thermal-induced mechanical stresses in T-S are mainly due to non-uniform temperature distribution within a material and thermal expansion mismatch between the materials. For E-S coupled-field simulation, the stress effect in a semiconductor device is investigated from the first principle via semiconductor band structure modification.

(3) The use of finite element analysis for E-T-S coupled-field device simulation is demonstrated, for the first time, to be possible using finite element

method through a commercial software COMSOL. The model is applied to the study of SOI and PSOI lateral power devices, and their static I-V characteristics as well as the temperature and thermo-mechanical stress distributions in the devices are computed using E only, E-T and E-T-S models.

(4) New method, namely hybrid of SIMOX and Wafer Bonding (HSW), combining SIMOX and wafer bonding to fabricate partial SOI is proposed. HSW can obtain partial SOI without damage in the device layer, and the process is also simple.

1.4 Organization of the Thesis

The thesis is organized in six chapters.

Chapter one is the introduction of the thesis, including motivation, objective, contribution and organization. The literature reviews of SOI and Partial SOI technology, thermal-induced stresses, stress effects on device characteristics, finite element method used in semiconductor analysis, and power devices are present in Chapter two. The computational simulations of thermal-induced stresses on PSOI structure are presented in chapter 3. Chapter 4 is devoted to the building of electrical-thermal-stress coupled field model. Chapter 5 presents the applications of E-T-S model in Partial SOI and conventional SOI power devices including lateral power diode and LDMOSFETs. Finally, chapter 6 summarizes the results in this work and gives recommendation for future work.

Chapter 2 LITERATURE REVIEW

2.1 SOI and Partial SOI Technology

SOI technology presents one way of fabricating semiconductor devices on an insulated substrate rather than in a semiconductor bulk. In the standard silicon technology the bulk substrate is associated with undesirable effects such as high leakage currents, parasitic bipolar components, defects and moreover, the interference between individual active devices or circuits built in the same integrated chip[24,25,26].

The insertion of the insulation layer beneath the devices in SOI structure is the major difference from its bulk counterpart [27]. The absence of latch-up, the reduced parasitic source and drain capacitances, and the ease of making shallow junctions are merely three obvious examples of advantages provided by SOI technology over bulk.

Recently, it was demonstrated that SOI has considerable better performance and attracts more attention in a wide variety of applications [1,3]. The applications are mainly in smart power devices and power integrated circuits, which integrate monolithically power devices with control circuitry. These ICs reduce the volume and weight, improve the reliability and the efficiency of a system [3,4].

SOI technology is becoming a mature technology for low-power CMOS circuits and represents the promising manufacturing technology for the next generation of ULSI low-power circuits. However, full SOI technology is not suitable for high power and high voltage device applications. There are many shortcomings arising, such as reduced breakdown level and self-heating effect [3,6]. A SOI structure that combines the advantages of SOI and JI (Junction Isolation) technologies, namely the partial SOI structure, was introduced [8]. This partial SOI structure realizes an improved RESURF effect, higher breakdown voltage and reduced self-heating effect as compared to the conventional SOI structure.

2.1.1 Evolutions of SOI and PSOI Technology

The PSOI fabrication technology was developed initially from the SOI technology. In order to understand both SOI and PSOI technologies, these two technologies are introduced in this section, respectively.

2.1.1.1 SOI Technology and Fabrication Methods

SOI structure is similar to normal bulk Si technology but the major difference is the insulated layer beneath the devices. Creating defect free films of single-crystal silicon on an insulated layer is a technological challenge. Several techniques have been developed to do this, but only a few have been successful commercially. Separation by implantation of oxygen (SIMOX), Unibond wafers produced by the Smart-Cut process, and the wafer bonding technology are the three representative examples of these [24], which will be briefly introduced in the following part.

A. SIMOX [28]

In this technique, an oxygen implant is performed on an epitaxial wafer before any other processing. The high energy implant forces a large dose of oxygen to reside deeply beneath the surface. Once the implantation is completed, it is then followed by a high temperature annealing process to form the silicon dioxide insulating region. This annealing also helps to recrystallize the silicon in the epitaxial layer. Due to the high energy and high dosage of the implant, the epi-layer is heavily damaged. The post-implant anneal will reproduce a high quality silicon for the subsequent process as shown in Figure 2.1 [28].

Figure 2.1 The principle of SIMOX: a heavy-dose oxygen implantation into silicon followed by an annealing step produces a buried layer of silicon dioxide below a thin, single-crystal silicon overlayer.

B. Smart Cut [29]

This technique starts with the oxidation of a silicon wafer. The wafer is implanted with protons (hydrogen nucleus) through the oxide layer. Then the surface of the oxide is cleaned. A second silicon wafer is bonded to this oxide layer. This wafer is now the substrate for the SOI wafer. A thermal anneal creates a stress

fracture along the plane of the hydrogen implant. The original silicon wafer can be removed from the tri-layer stack leaving behind a thin layer of silicon on the top of the buried oxide. The removed portion of the silicon wafer will become the substrate for another smart cut wafer. In this manner, no silicon is wasted. To complete the process, the SOI wafer is annealed and polished to prepare as the surface for conventional CMOS processing steps. Versatility is the key advantage of the Smart Cut method, as it can be used to create SOI wafers with a wide range of buried oxide thickness, and with silicon thickness from 200nm to 1.5um [29]. Figure 2.2 shows the steps in the smart cut process.

Figure 2.2 The principle of Smart cut: hydrogen implantation into silicon followed by substrate wafer bonding creates a stress fracture leaving behind a thin silicon layer

C. Wafer bonding and etch back [30]

Bonded SOI wafers create the buried oxide without ion implantation. First, two silicon wafers are fabricated to form a silicon dioxide layer on the surface. The two oxide surfaces are bonded together to form the buried oxide. The backside of silicon wafers is ground down to the desired thickness. Finally the SOI wafer is annealed and polished to leave a thin layer of silicon above the buried oxide [30]. This wafer is then ready for the next processing. One problem with the bonded wafers is that it requires the use of two silicon wafers to provide one SOI wafer. Figure 2.3 shows the process steps for wafer bonding.

Figure 2.3 The principle of wafer bonding: wafers bonded together followed by etching top layer to leave a thin silicon layer above the buried oxide

2.1.1.2 Partial SOI Technology and Fabrication Methods

Partial SOI which combines the advantages of SOI and JI technologies has been mainly investigated by Cambridge University as shown in Figure 2.4 [2,4,5,8,9,11].

Figure 2.4 Schematic of the (a) SOI structure and (b) partial SOI structures

In contrast to the conventional SOI structure, the PSOI device structure has an interrupted oxide at one electrode of the devices. PSOI can be achieved by various techniques such as selective SIMOX, selective recrystallisation and selective etching-epitaxial growth as well as wafer bonding technology as shown in Figure 2.5-2.7 [14,15,16,17].

The first technique has the shortcomings of traditional SIMOX, such as the low quality of the films [14,15]. Large thermal stresses and film non-uniformity occur with the second technique, recrystallisation [16]. The third one is very complicated and not suitable for the mass production [17]. A larger thermal stress is also one serious issue in wafer bonding if we use the traditional method that needs high temperature annealing [30].

Figure 2.5 Selective SIMOX to fabricate partial SOI

Figure 2.6 Schematic of recrystallisation to fabricate partial SOI

Figure 2.7 Selective etching and selective epitaxial growth to fabricate partial SOI

A promising technology, low temperature medium vacuum wafer bonding (MVWB) technology for Si-Si and Si-SiO₂, is recently developed [18] by our group. This method can be used for the fabrication of the partial SOI structure and SOI structure. In this work, the coupled-field simulation is developed based on the MVWB technology for both SOI structure and partial SOI structure. Conventional direct

wafer bonding requires high-temperature annealing above 1000°C to achieve strong bonding between wafers [30]. However, such a high temperature process will give rise to the following three major problems:

- (1) thermal-induced mechanical stress due to different thermal expansion coefficients of the bonded materials.
- (2) Undesirable changes and reactions for materials and structures which are sensitive to high temperature.
- (3) The occurrence of precipitates of oxides and vacancies at the bonded interface during heat treatment.

Low temperature wafer bonding methods are cost-effective and compatible with the standard IC process in mass production. It can be a promising method to fabricate the partial SOI structure and SOI structure using MVWB. The principle is shown in Figure 2.8 [18].

Figure 2.8 Schematic of medium vacuum wafer bonding (MVWB) process flow

2.1.2 Why Partial SOI -- RESURF and Self-heating Effects

Today PSOI technology is implemented as the one of promising technology for monolithic integration of CMOS and bipolar devices. PSOI technology offers the possibility of building logical devices in thin layer of silicon that is electrically isolated from the thick semiconductor substrate through the use of a patterned buried insulating layer.

For low power devices, besides immunization from ionization by atoms and radiations, the PSOI technology provides several important advantages, such as reduced parasitic capacitances, improved short-channel effects, reduced hot-carrier effects and static consumption. Meanwhile, another important feature that establishes the PSOI technology as a strong option for generations of ULSI is that it also provides significant isolation between individual device cells. The use of reverse-biased junctions as isolation in bulk technology has major drawbacks, such as increased parasitic capacitances and high leakage currents [31]. Furthermore, latch-up structures such as npnp parasitic thyristors present in bulk CMOS inverters are effectively eliminated in PSOI technology.

For high power IC, the more important aspect is the isolation between power ICs and control circuits. PSOI structure remains isolation in place. In JI technology, the operation of power devices is often associated with the injection of carriers into the silicon substrate, especially if such devices employ conductivity modulation to achieve a low on-state resistance. Parasitic collection of these injected carriers in the substrate by an adjacent large-area power device can cause it to turn-on.

The promising structure Partial SOI realizes an improved Resurf effect because the substrate plays an active role to reduce the electric field at the surface, unlike in conventional SOI power devices, which has the potential lines crowded in

the top SOI layer. From the numerical simulations of JI, SOI and partial SOI structure, it is worthwhile to note that the breakdown voltage of the partial SOI is even higher than that of junction isolation (JI) [6,9]. This can be explained by the fact that the oxide layer near the silicon window can support part of the voltage. Furthermore, since in both SOI and partial SOI structures the current and the plasma injection are confined to the SOI layer, the switching speed of these structures is considerably superior to that of equivalent JI structure, where during turn-off a slow process of recombination of the excess charge in the substrate [4]. Meanwhile, the self-heating effect in partial SOI is drastically reduced since heat can be dissipated from the silicon window to the substrate [1,10].

2.1.2.1 RESURF Effect

The principle of RESURF effect was first introduced by Appels in 1979 [32] for JI devices. Huang and Baliga extended it to SOI devices in 1991[33].

RESURF stands for Reduced SURface Field principle. It's an important method for the design of lateral high voltage, low on-resistance devices. The technique has allowed the integration of HV devices with bipolar and MOS transistor [34]. The principle of operation was explained in [32,34]. This phenomenon is the result of the depletion region in the epitaxial layer being generated by both the vertical n-epi/p- substrate and the lateral n-epi/p+ anode junctions. This yields a reduction in the electric field peaks that occur at the surface, leading to considerably higher breakdown voltages than those specific to one-dimensional lateral structures. The electric field and potential distributions are purely two-dimensional.

Figure 2.9 Potential contours in (a) conventional JI and (b) SOI structures

Figure 2.9 shows a cross section view of a RESURF diode structure on JI and SOI respectively [5]. Because PSOI structure has the advantage of both JI and SOI, the review of the RESURF in JI and SOI is introduced first.

For JI structure, the RESURF model considers an approximation for the electric field distribution resulted from one-dimension Poisson's equation in the vertical direction. The reason is that the effective RESURF means n- drift layer must be depleted by the vertical p- substrate/n- drift junction. From the condition for full depletion of the epitaxial layer, the relationship between the epitaxial doping concentration and epitaxial layer thickness of an optimally designed RESURF diode is found [9].

$$N_{epi} \times d_{epi} < \frac{\epsilon_0 \epsilon_r E_{crit,surface}}{q(1 + \frac{N_{epi}}{N_{sub}})^{1/2}} \quad (2.1)$$

To find out the breakdown voltage of the vertical diode, the electric field in the vertical cross-section is integrated, resulting in the following equation:

$$V_{BR} = \frac{\epsilon_0 \epsilon_{si} E_{crit,surface}^2}{2qN_{sub}} + E_{crit,surface} (d_{epi} - y_i) - \frac{qN_{epi} (d_{epi} - y_i)^2}{2\epsilon_0 \epsilon_{si}} \quad (2.2)$$

where the y_i is the thickness of n+ cathode, d_{epi} is depletion thickness and $E_{crit,surface}$ is its electric field. This model results in the very simple and effective optimization criteria for the epitaxial layer thickness and doping concentration.

For SOI devices, the potential lines cannot expand into the substrate due to the presence of the buried oxide, and the buried oxide must be able to support the entire voltage across it. Generally, thicker oxide will withstand higher breakdown voltage. One solution to solve this problem is to use a thin SOI film with a linearly graded doping profile.

In the PSOI device the silicon window allows the potential lines to spread into the substrate silicon, as shown in Figure 2.10 [5]. We can find that the potential lines are more uniform. Moreover, PSOI allows the insulator layer thickness to be reduced to a level since the voltage is supported across the depletion layer associated with the device/substrate junction. Figure 2.11 shows a numerical study of the RESURF effect in bulk, SOI and PSOI power devices [8]. The results indicate that PSOI has better RESURF.

A uniform Resurf model was reported by Cambridge [9]. As mentioned, any model for breakdown operation of Resurf structure is to solve the two-dimensional Poisson's equation in the epitaxial layer.

$$\begin{aligned} \frac{\partial^2 V(x, y)}{\partial x^2} + \frac{\partial^2 V(x, y)}{\partial y^2} &= -\frac{q}{\epsilon} N_{epi} \\ \frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} &= \frac{q}{\epsilon} N_{epi} \end{aligned} \quad (2.3)$$

Figure 2.10 Potential distribution in a partial SOI structure

Figure 2.11 Breakdown characteristics for (a) SOI, (b) bulk and (c) partial SOI structure;

$d_{\text{epi}}=10\mu\text{m}$, $N_{\text{epi}}=7e14\text{cm}^{-3}$, $t_{\text{ox}}=0.5\mu\text{m}$, $d_{\text{cathode}}=5\mu\text{m}$.

The main idea of this model is to express the potential and electric field functions using simple polynomial approximations justified by physical considerations. Thus, the total electric field at a constant y-coordinate can be approximated as a parabolic function in x:

$$V(x, y) = \int (f_1(y)x^2 + f_2(y)x + f_3(y))dy + f_4(x) \quad (2.4)$$

Solve the expression for V(x,y) in the Poisson equation, can obtain

$$\int 2f_1(y)dy + \frac{d^2 f_4(x)}{dx^2} + \frac{df_1(y)}{dy}x^2 + \frac{df_2(y)}{dy}x + \frac{df_3(y)}{dy} + \frac{qN_{epi}}{\epsilon} = 0 \quad (2.5)$$

and follows

$$\begin{aligned} f_1(y) &= -c_1 y + c_7 \\ f_2(y) &= -c_2 y + c_8 \\ f_3(y) &= -2\left(-\frac{1}{6}c_1 y^3 + \frac{1}{2}c_7 y^2\right) - c_3 y - \frac{qN_{epi}Y}{\epsilon} + c_6 \end{aligned} \quad (2.6)$$

where c1 to c8 are constants that need to be calculated from the boundary conditions for the potential and the electric field.

The advantage of this model is its versatility and can be also applied in both JI and SOI technologies with same assumptions and algorithm. Moreover, it also can be used for 3-D devices study, even for PSOI with linearly graded doping concentration in the expitaxial layer.

2.1.2.2 Self-heating Effect

In power devices it is essential to consider the self-heating effect since the power devices work at high current and high voltage condition. Firstly, sever self-

heating during the on-state operation and during large transient power overloads [10] may lead to performance degradation and raise reliability issues in devices design. Self-heating in power devices also causes an increase in the on-state resistance and may lead to latch-up and threshold voltage shift of adjacent CMOS devices in real power integrated circuits. For example, a 40°C increase in the temperature results in an increase in the on-state resistance by as much as 25% [10] mainly due to degradation of channel mobility. Moreover, self-heating will result in the mechanical stress, which is induced by temperature gradient and the differential thermal expansion in different materials. This result would be analyzed in next Chapter.

A simplified model for the heat generation rate per unit volume is given by

$$H = J * E + U * E_g \quad (2.7)$$

where J is the current density and E is the electrical field, U is the recombination rate and E_g is the bandgap of the semiconductor. The first term of the equation is the Joule heating which caused by the electrical resistance that associates with the semiconductor. The second term is account for the released energy by recombination of carriers [35].

2.2 Thermal-Induced Stresses

In power devices the thermal-induced stresses should be considered and cannot be ignored. For example, the maximum junction temperature of the punch-through insulated gate bipolar transistors (IGBT) varies with circuit conditions and is in the range of 115-170°C. The non-punch-through IGBT can typically operate at

junction temperatures up to 230°C in various circuits which is typical junction temperature in power devices [36]. The novel PSOI structure introduces more stress than SOI due to the presence of the partial buried oxide edges. The higher temperature of the thermal expansion mismatches between Si and Oxide accounts for this additive stress. In this work, we focus on the electrical characteristics variation aroused by the thermal-induced stresses. Firstly, the thermal-induced stress would be introduced in the following sections.

2.2.1 A Brief Review of Mechanical Stress and Strain Model

The intention of this section is to introduce the theory and notation of continuum mechanics. References [37] provides for more complete description. The stress tensor is first introduced in this section. Next the strain tensor is described. Finally this section concludes with the different stress-strain relationships, which will mainly focuses on the elastic solid such as silicon at the normal temperature.

Figure 2.12 An infinitesimal cubic element located within a continuous body with stress tensor components shown

To illustrate the tensor nature of stress present at point P in the continuous body, consider a cubic element shown in Figure 2.12 of infinitesimal dimensions. For simplicity of the notation, let the cube be aligned perpendicularly with the system axis. The stress vector T_x acting on the plane normal to the x-direction is

$$T_x = \sigma_{xx} \cdot \hat{x} + \sigma_{xy} \cdot \hat{y} + \sigma_{xz} \cdot \hat{z} \quad (2.8)$$

The stress tensor on that volume is defined by nine on the three surfaces of the cubic element, which make up the three stress vectors T_i :

$$\sigma_{ij} = \begin{bmatrix} \sigma_{xx} & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_{yy} & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_{zz} \end{bmatrix} \quad (2.9)$$

where σ_{ii} are the normal stress components acting on the faces perpendicular to i -direction and τ_{ij} are the shear stress components oriented in the j -direction on the face with normal in the i -direction. At mechanical equilibrium, it can be shown that the stress tensor is symmetrical [37]

$$\tau_{ij} = \tau_{ji} \quad (2.10)$$

The strain is related to the displacements by the following strain components:

$$\begin{aligned} \epsilon_{xx} &= \frac{\partial u}{\partial x} & \epsilon_{xy} = \epsilon_{yx} &= \frac{1}{2} \left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \right) \\ \epsilon_{yy} &= \frac{\partial v}{\partial y} & \epsilon_{yz} = \epsilon_{zy} &= \frac{1}{2} \left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \right) \end{aligned}$$

$$\epsilon_{zz} = \frac{\partial w}{\partial z} \qquad \epsilon_{zx} = \epsilon_{xz} = \frac{1}{2} \left(\frac{\partial u}{\partial z} + \frac{\partial w}{\partial x} \right)$$

In the definition above, u , v , w are the displacements in the x , y , and z directions, respectively. These components make up the strain tensor that is analogous to the stress tensor:

$$\epsilon_{ij} = \begin{bmatrix} \epsilon_{xx} & \epsilon_{xy} & \epsilon_{xz} \\ \epsilon_{yx} & \epsilon_{yy} & \epsilon_{yz} \\ \epsilon_{zx} & \epsilon_{zy} & \epsilon_{zz} \end{bmatrix} \quad (2.11)$$

Elastic solid, Viscosity and Viscoelasticity are three type of body states. Crystal silicon has diamond cubic crystal strong directional covalent bonds. It is a typical elastic solid in our research region where temperature under 300⁰C and pressure about 0.2-0.3Gpa. For a Hookean elastic solid, the stress tensor is linearly proportional to the strain tensor over a specific range of deformation:

$$\sigma_{ij} = c_{ijkl} \epsilon_{kl} \quad (2.12)$$

where C_{ijkl} indicates the tensor of elastic constants. σ_{ij} is the stress tensor. ϵ_{kl} is the strain tensor. Due to the crystal's lattice temperature dependence, the elastic constants are also thermally dependent. For silicon crystals, C_{ijkl} has the following form due to their cubic symmetry [38]:

$$c_{ijkl} = \begin{bmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{bmatrix} \quad (2.13)$$

Thus, for silicon the tensor of elastic stiffness constants reduces to the three independent components: c_{11} , c_{12} , and c_{44} .

For a uniaxial compressive stress of $-\sigma_1$ along the $\langle 100 \rangle$ axis, the matrix $\{\sigma_{ij}\}$ and the six vector $\{\sigma_i\}$ have the form shown as the following. The procedure for calculating the deformation matrix is analyzed in [39].

$$\sigma_{ij} = \begin{bmatrix} -\sigma_1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad (2.14)$$

2.2.2 Thermal-Induced Stresses

Stress problems are quite complicated and critical in the silicon technology. The most effective analysis on this problem was done by Hu [40]. In the present study, we focus on the power devices in SOI and PSOI structure. Based on the introduction at the beginning of the chapter, self-heating induces distinctly the temperature distribution variation. Thus, the stress effects emerge with the temperature variation. In order to analyze our model effectively and efficiently, we need to consider the effects of thermal-induced stress on partial SOI structure which compared with SOI structure.

The thermal-induced stresses considered in this work include thermo-mechanical stress due to thermal expansion mismatch of materials and non-uniform temperature distribution within a material.

(1) Thermo-mechanical stress due to non-uniform temperature distribution

Thermal stress arises from nonuniform temperature distribution in silicon. It is determined by the transient temperature gradients. The thermal stress is considered in silicon wafers during heating up and cooling down, and in the case of power devices, the temperature gradients within a wafer are even higher due to the much higher processing temperatures. Once the temperature distribution is calculated, the thermal stress distribution can be found based on formulas for axisymmetric plane stress problems. The thermal stress is given by [40,41]

$$\varepsilon = \alpha(T_2 - T_1) \quad (2.15)$$

where α is the thermal expansion coefficient.

(2) Thermo-mechanical stress due to thermal expansion mismatch

Thermal expansion mismatch stress exists between the silicon and oxide. The maximum stress distributes mainly at the interface and the corner.

As the temperature changes from T_1 to T_2 from silicon to oxide, and the strain experienced by the oxide is given as [41]

$$\epsilon_{ox} = (\alpha_{ox} - \alpha_{si})(T_2 - T_1) \quad (2.16)$$

where α is the thermal expansion coefficient and the subscripts ox and si denote oxide and silicon respectively.

2.3 Stress Effects on Devices Characteristics

The influence of externally applied stress on electrical characteristics has been investigated for many years. Most of the research focused on the piezoelectric effect reported by Smith et al [23] at first. It is long been recognized that the externally applied stress has a direct influence on the energy band structure of a semiconductor [42]. Since the minority carrier density is a function of the band gap, the influence of the band gap is noticeable in minority carrier devices such as diode and bipolar transistor.

2.3.1 Si Crystal Structure

Si belongs to the cubic system and has the diamond structure. The space lattice of diamond is face-centered cubic. Its cubic unit cell is shown in Figure 2.13(a). it is composed of two face-centered cubic lattices displaced from each other by one quarter of a body diagonal. Each silicon atom has four valence electrons, which provide tetrahedral covalent bonding with the nearest neighbors.

The diamond structure has tetrahedral point symmetry, which is one of the five crystal point groups in the cubic crystal system.

Figure 2.13 (a) The cells of the Si structure (b) The first Brillouin zone for Si.

The first Brillouin zone is the well-known truncated octahedron shown in Figure 2.13(b). Some of the properties of Si are shown in Table 2.1 [40]

Table 2.1 The properties of Silicon.

Property	Si	Property	Si
Atomic No.	14	Atoms per unit volume (m^{-3})	5×10^{28}
Atomic weight	28.08	ϵ/ϵ_0	11.8
Density (kg m^{-3})	2.33×10^3	Unit cell length a (nm)	0.357
Melting point ($^{\circ}\text{C}$)	1420	Atomic diameter (nm)	0.357

2.3.2 Stress Models in Device Simulation

PSOI has the substrate with multiple-thin-layer (patterned buried oxide and SOI work layer) overlays and especially with disconnected regions in buried oxide layer. Stresses are always concomitant with this multi-layer structure considering the higher thermal field in the PICs. As we know, stresses are small in the substrate by virtue of its much larger thickness than the overlays. However, in the discontinuities of the patterned buried oxide, very large localized stresses can occur at the interface

[19]. To investigate the distribution of thermal-induced stresses in PSOI and optimization of the PSOI structure has been one important issue also.

In order to assist device design to take into account of the stress distribution in a PSOI structure effectively and efficiently, studying the effects of stresses on power devices is necessary. The influence of externally applied stress on electrical characteristics has been investigated for many years such as the piezoelectric effect [23]. However, at the beginning most of the research applies to sensor development rather than logical IC or analog IC. Until recent years, stress layer deposition in 65nm and below for MOSFET technology considers the stress effects to improve transport electrical characteristics [43]. The thermal-induced stresses are pervasive and critical in many issues of power devices in PSOI structure. Therefore, analyzing and modeling these stress effects quantitatively in power devices has been another critical issue.

2.3.2.1 Piezoelectric Effect

The modification of the carrier mobility of Silicon through the application of stress, the piezoelectric effect, is a well-known effect and was first reported by Smith et. al. [23], who observed increased carrier mobility with the application of stress to bulk-Si material.

The change in resistivity, ρ for a particular direction can be related to the applied stress, assuming zero shear stress, as:

$$\frac{\Delta\rho_i}{\rho} = \pi_i^j \sigma_j \quad (2.17)$$

The piezoelectric coefficients measured for moderately doped p-type and n-type silicon, shown in Table 2.2 indicate that an applied tensile stress parallel to the direction of current flow will result in reduced resistance or increased electron mobility for n-type Si, while a perpendicular stress will increase the resistance.

Table 2.2 Piezoresistive coefficients for n and p-type silicon [23]

Material <100> Si	Piezoresistive coefficient [$10^{-6}/\text{atm}$]		
	π_{11}	π_{12}	π_{44}
p-type ($1.5 \times 10^{15} \text{cm}^{-3}$)	6.8	-1.1	142.7
n-type ($4.0 \times 10^{14} \text{cm}^{-3}$)	-105.6	55.2	-14.0

2.3.2.2 Simplified Rigid-shift Stress Model

In semiconductor devices, device reliability is affected by the mechanical stresses [44]. For example, stress-induced band gap narrowing increases junction leakage and reduces carrier mobility. Stress-induced extended defect generation and growth might either increase or reduce the leakage currents depending on the defect position related to the p/n junction.

Normally, there are four ways that elastic strain can affect the transport parameters [45]: (1) change of the phonon spectrum; (2) changes in coupling between electrons and phonons; (3) strain induced recombination-generation centers; (4) changes in the energy spectrum. In these four aspects, only the changes in the band

structure have the most distinct effects [44]. In this study, we do mainly focus on this part.

In silicon $\langle 1\ 0\ 0 \rangle$ directions, the conduction band is made up of states that come from six ellipsoidal-shaped minima. A sketch of the constant-energy surfaces for these minima is shown in Figure 2.14(a). Each minimum is characterized by the larger, longitudinal effective mass, m_L , along each axis and the smaller, transverse effective mass perpendicular to the axis, m_T . The six minima are equivalent with same minimum energy and the electron transport is isotropic if without strain. For low energies, the valence band is made of states that comes from two spherically symmetric maxima at the center of the Brillouin zone. The light-hole effective mass, m_{LH} , and the heavy-hole effective mass, m_{HH} , characterize the valence band.

Figure 2.14 (a) constant-energy surfaces of the ellipsoidal minima (b) splitting of the band extrema due to uniaxial tensile stress along $[0\ 0\ 1]$ [44].

The rigid shifting of the band extrema is considered in the stress model where the conduction band minima splits into two sets under the application of a uniaxial tensile stress along the [0 0 1] axis [44].

Based on the standard deformation potential theory from Bir and Pikus [46], the shifts in the band extrema for a general strain tensor ϵ in the crystallographic coordinate system can be computed as:

$$\Delta E_{C_i} = \Xi_d Tr[\epsilon] + \Xi_u \epsilon_{ii} \quad (2.18)$$

$$\Delta E_{V(h,l)} = a Tr[\epsilon] \pm \sqrt{\xi} \quad (2.19)$$

where

$$\xi = \frac{b^2}{2} [(\epsilon_{xx} - \epsilon_{yy})^2 + (\epsilon_{yy} - \epsilon_{zz})^2 + (\epsilon_{zz} - \epsilon_{xx})^2] + c^2 (\epsilon_{xy}^2 + \epsilon_{xz}^2 + \epsilon_{yz}^2) \quad (2.20)$$

and ϵ_{ij} represents the strain components. Tr represents the trace, ΔE_{C_i} is the shift in the band edge of the i th ellipsoidal conduction minimum, the shifts in the band edges for the heavy and light maxima are denoted as ΔE_{V_h} and ΔE_{V_l} . The deformation potential parameters are given by Ξ_d , Ξ_u , a , b , and c . Normally, based on these shifts to the band extrema, effective changes to the conduction and valence band edges used in continuum device simulation can be generated. The band gap and carrier transport are directly modified by these modifications to the band structure.

Mobility is also influenced by the bandgap[44,45]. It is another main impact of stress-induced band structure change on device simulation. In the rigid-shift stress model [45] modifications to the electron mobility are induced by a change in the

occupancy of the different conduction band minima whose energies are split by the stress. Compared to the unstrained case, more electrons would transport with a smaller conductivity mass resulting in a larger mobility as well as a larger conductivity mass which induce a smaller mobility. In the example of Figure 2.14, for transport along the [001] axis, the electrons in the [100] and [010] minima would transport with a conductivity mass m_T and electrons in the [001] minima would transport with a conductivity mass m_L . Thus, the mobility must be represented by a tensor. The electron mobility tensor is diagonal in the crystallographic coordinate system and is shown

$$\mu_n = \mu_0 \begin{pmatrix} 1 + \beta_1 & 0 & 0 \\ 0 & 1 + \beta_2 & 0 \\ 0 & 0 & 1 + \beta_3 \end{pmatrix} \quad (2.21)$$

where μ_0 is the nominal, isotropic mobility without stress and

$$\beta_i = \left(\frac{1 - m_L / m_T}{1 + 2m_L / m_T} \right) \left(\exp\left(\frac{\Delta E_C - \Delta E_{Ci}}{kT}\right) - 1 \right) \quad (2.22)$$

ΔE_C denotes the net effective shift of the conduction band. The holes mobility model can also be developed based on the relative occupancy of the hole valleys [45,46].

2.4 Finite Element Method in Semiconductor Device Analysis

2.4.1 Introduction

The system of partial differential equations (PDEs) which forms the basic semiconductor equations together with appropriate boundary conditions had been

characterized analytically to investigate some of the existing analytical results [47,48]. In both the theoretical and the practical aspects, these are important since the knowledge of the structure and smoothness properties of solutions is indeed essential for the selection of appropriate numerical solution procedures. Meanwhile, they also provide the theoretical background for semiconductor devices.

However, in general, it is not possible to find an exact analytic solution to a system of coupled nonlinear PDEs. It is because

1. The PDE is not linear and cannot be linearized without seriously affecting the result.
2. The solution region is complex.
3. The boundary conditions are mixed types.
4. The boundary conditions may be time dependent.
5. The medium is inhomogeneous or anisotropic.

Numerical techniques must be used to find the approximate solutions to such system of equations when it is not possible to find an analytic solution. The numerical techniques should include the following:

1. appropriate model
2. a simulation mesh which provides adequate precise resolution
3. the computational problem considering the available resources

2.4.2 Numerical techniques for solving PDEs

Numerical techniques are used to discretize the basic semiconductor PDEs. Any numerical approach for the solution of a system consists essentially of three steps. First, the domain, i.e. the simulation geometry of the devices, has to be partitioned into a finite number of subdomains, in which the solution can be approximated easily

with desired accuracy. Secondly, the differential equations have to be approximated in each of the subdomains by algebraic equations which involve only values of the continuous dependent variables at discrete points in the domain. Knowledge of the structure of the chosen functions approximates the dependent variables within each of the subdomains. In that way one obtains a fairly large system of, in general nonlinear, algebraic equations with unknowns comprised of approximations of the continuous dependent variables at discrete points. The solution of this system is the final third step to be carried out.

2.4.2.1 Finite Difference Method (FDM)

The goal of finite difference method [47] is to approximate differential equations by a system of difference equations.

Three steps of FDM to solve PDEs:

1. dividing the solution region into a grid of nodes
2. approximating the given PDEs by finite-difference equivalents. The node variables in the solution region are related to same variables of neighboring nodes same variable
3. solving the difference equations subject to prescribed boundary conditions and initial conditions

In the conventional five points discretization, the domain is partitioned into subregions by a mesh which is a set of mesh lines parallel to the coordinate axes. X lines parallel to the y-axis and Y lines parallel to the x-axis through a rectangular domain. The first and last lines coincide with the boundaries. The differential equations at the inner points are replaced by difference equations. The adopted nomenclature is shown in Figure 2.15. $x_i(y_j)$ is assumed to be the distance from the

origin to the i -th (j -th) mesh line parallel to the y -axis (x -axis). The following abbreviation can be obtained:

$$\begin{aligned} h_i &= x_{i+1} - x_i, \quad i = 1, X-1 \\ k_j &= y_{j+1} - y_j, \quad j = 1, Y-1 \end{aligned} \quad (2.23)$$

To simplify the notation, we further define the following::

$$\begin{aligned} u_{i,j} &= u(x_i, y_j) & i = 1, X, \quad j = 1, Y \\ u_{i+1/2,j} &= u\left(\frac{x_i + x_{i+1}}{2}, y_j\right) & i = 1, X-1, \quad j = 1, Y \\ u_{i,j+1/2} &= u\left(x_i, \frac{y_j + y_{j+1}}{2}\right) & i = 1, X, \quad j = 1, Y-1 \end{aligned} \quad (2.24)$$

Figure 2.15 Adopted nomenclature for finite difference

In 2D semiconductor simulations [47], the finite box method is also important and it is a subset of finite difference methods. It provides a convenient method of discretizing a large class of PDEs. The mesh lines are allowed to start and to terminate in each direction compared with finite difference method. In the case of classical finite differences it is a trivial task to find the location of quantities at neighboring points if the quantities are stored by columns or rows, because the number of points in a column or row is a mesh specific constant. In the case of terminating lines one needs four additional variables for each point, i.e., two indices for the neighboring points in the direction perpendicular to the direction in which mesh lines may terminate and the space coordinates. For finite boxes, six variables per mesh point are required to fully describe the mesh. There are the four indices for all neighboring points and the space coordinates. Details on this subject can be found in [47,48].

2.4.2.2 Finite Element Method

The use of finite elements started in the early 1940's as attempted by Hrenikoff [49] and McHenry [50] in the field of structural engineering. The term of "finite element" was introduced by Clough [51] in 1960. Since then the finite element method has developed enormously and it can be seen as "a general discretization procedure of continuum problems posed by mathematically defined statements" [52]. More introductions can be found in [53].

In order to use finite element method (FEM) we have to partition the simulation domains without overlap or exclusion into a finite number of subregions, or finite element [47]. Depending on the nature of the structure, there are various types of elements available. Figure 2.16 shows the typical and most commonly used elements. Bar elements are frequently used in modeling trusses and frames, and plate elements

are suitable for plate type structures, or when the variation of the physical quantities is limited to a plane (i.e. plane stress case). For structures with an axis of symmetry, e.g. cylinders and pressure vessels, torus elements can be used. Finally, for structures of extremely complicated geometry, when a three-dimensional model becomes a necessity, tetrahedron or hexahedron elements are commonly used. Some elements have additional nodes on the sides which can be either curved or straight.

Figure 2.16 Typical element geometries

The finite element method seeks an approximation u_a to the exact solution u in each of the elements. u_a is usually the polynomial approximation because it is easy to manipulate and accurate for smooth functions. A quadratic polynomial suitable for triangular elements is:

$$u^a(x, y) = a_0 + a_1 \cdot x + a_2 \cdot y + a_3 \cdot x^2 + a_4 \cdot x \cdot y + a_5 \cdot y^2 \quad (2.25)$$

Six values of the approximate solution are required to fully determine the coefficients a_i . As shown in Figure 2.17, these may be taken at the nodes and in the middle of the edges of triangle.

Figure 2.17 Nomenclature for triangular element with quadratic approximation function

Analogously the quadratic approximation transforms in the coordinates (ξ, η)

to

$$\begin{aligned}
u^q(\xi, \eta) = & u_1 + (4 \cdot u_2 - 3 \cdot u_1 - u_3) \cdot \xi + (4 \cdot u_6 - 3 \cdot u_1 - u_5) \cdot \eta \\
& + (2 \cdot u_1 + 2 \cdot u_3 - 4 \cdot u_2) \cdot \xi^2 + 4 \cdot (u_1 - u_2 + u_4 - u_6) \cdot \xi \cdot \eta \\
& + (2 \cdot u_1 + 2 \cdot u_5 - 4 \cdot u_6) \cdot \eta^2
\end{aligned} \quad (2.26)$$

u_i , $i=1..6$ are the values of the approximate solution at the respective nodes of the triangle.

Particularly for the semiconductor equations with rectangular elements have also been proven to be suitable. The solution is simply approximated for a rectangle with a bilinear form.

$$u^a(x, y) = a_0 + a_1 \cdot x + a_2 \cdot y + a_4 \cdot x \cdot y \quad (2.27)$$

By numbering the nodes of the general rectangular element counter-clockwise as shown in Figure 2.18, it can be transformed into a unit square defined as follow.

$$\begin{aligned}
x &= x_1 + (x_2 - x_1) \cdot \xi + (x_4 - x_1) \cdot \eta \\
y &= y_1 + (y_2 - y_1) \cdot \xi + (y_4 - y_1) \cdot \eta
\end{aligned} \quad (2.28)$$

Thus, we can get:

$$u^q(\xi, \eta) = u_1 + (u_2 - u_1) \cdot \xi + (u_4 - u_1) \cdot \eta + (u_1 - u_2 + u_3 - u_4) \cdot \xi \cdot \eta \quad (2.29)$$

Normally, these approximations are more attractively formulated by the aid of so called shape function (trial function) $\varphi_i(\xi, \eta)$ that the approximations are transformed into:

$$u^a(\xi, \eta) = \sum_{i=1}^m u_i \cdot \varphi_i(\xi, \eta) \quad (2.30)$$

Figure 2.18 Nomenclature for rectangular element with bilinear approximation function

where m is the number of variable degrees of freedom in an element. Note that the shape functions which outside of the specified element are identically zero. The shape functions are only non-vanishing within the element for which they are defined.

Compared with FDM, the attractive feature of the FEM is its ability to handle complicated geometries and boundaries with relative ease. Meanwhile, the accuracy of a FEM approximation is normally higher than in the corresponding FDM approach. The literature devoted to the subject of FDM and FEM are referred to in [47,48,52,53].

2.5 Power Semiconductor Devices

A brief overview of power semiconductor devices and device operations of lateral power devices for smart power applications is presented in this section.

Power semiconductor devices are semiconductor devices used as switches or rectifiers in power electronic circuits. They are also called power devices or when used in integrated circuits, called power ICs. An ideal power device must be able to control the flow of power to the loads with zero power dissipation. The loads may be inductive, resistive, or capacitive [54].

Power semiconductor devices first appeared in 1952 with the introduction of the power diode by R.N. Hall [55]. It was made of Germanium and had a voltage capability of 200 volts and a current rating of 35 amperes.

The thyristor appeared in 1957. Thyristors are able to withstand very high reverse breakdown voltages and are also capable of carrying high current. One disadvantage of the thyristor for switching circuits is that once it is 'latched-on' in the conducting state it cannot be turned off by external control. The thyristor turn-off is passive, i.e., the power must be disconnected from the device.

The first bipolar transistors devices with substantial power handling capabilities were introduced in the 1960s. These components overcame some limitations of the thyristors because they can be turned on or off with an applied signal.

With the improvements of the Metal Oxide Semiconductor technology (initially developed to produce integrated circuits), power MOSFETs became available in the late 1970s. International Rectifier introduced a 25 A, 400 V power MOSFET in 1978. These devices allow operation at higher frequency than bipolar transistors, but are limited by the low voltage applications.

The Insulated Gate Bipolar Transistor (IGBT) developed in the 1980s became widely available in the 1990s. This component has the power handling capability of

the bipolar transistor, with the advantages of the isolated gate drive of the power MOSFET.

The evolution naturally involves the integration of the whole or part of the low-voltage elements with the power devices [56,57] in order to improve performance and to reduce the chip (or system) size. The application of IC technologies on power semiconductor devices has offered efficient protection components, simple drive characteristics, and good control dynamics together with a direct interface to the monolithic integration with the signal processing circuitry on the same chip [58,59]. As a result, power electronic systems have greatly benefited from advances in power semiconductor technology.

2.5.1 Power Rectifier

Power rectifiers are essential components in all power electronic circuits. They are used to provide control to current flow and to block high voltage in a circuit [60,61]. The P-i-N or P^+-N-N^+ rectifier was one of the very first semiconductor devices developed for power circuit application. In this device, the i-region is flooded with minority carriers during forward conduction. Due to this, the resistance of the i-region becomes very small during forward current flow, allowing these diodes to carry a high current density during forward conduction. Because of the low doping at i-region, the development of P-i-N rectifiers with very high breakdown voltages ranging up to 5000 volts has been possible [54].

A PIN diode obeys the standard diode equation for low frequency signals. At higher frequencies, the diode looks like an almost perfect (very linear, even for large signals) resistor. There is a lot of stored charges in the intrinsic region. At low

frequencies, the charge can be removed and the diode turns off. At higher frequencies, there is not enough time to remove the charge, so the diode never turns off. That is the reason why the PIN diode has a poor reverse recovery time [54].

Figure 2.19 Cross section of a power PiN diode

The high-frequency resistance is inversely proportional to the DC bias current through the diode. A PIN diode, suitably biased, therefore acts as a variable resistor. This high-frequency resistance may vary over a wide range [62].

The wide intrinsic region also means the diode will have a low capacitance when reverse biased.

As one of the main functions of a power rectifier is to block the current flow in the reverse direction at high reverse voltage, measurement of its reverse breakdown voltage is an essential test for the power rectifier manufacturers and users. The systematic study on the reverse breakdown voltage measurement using the forced voltage test (FVT) and the forced current test (FCT) is investigated in our group [63].

2.5.2 Lateral Double-diffused MOSFETs

The full dielectric isolation provided by SOI substrate allows fabricating HV devices without the use of a complicated junction isolation process. Power devices can be integrated on the same substrate as CMOS logic to produce “smart power”

circuits [31]. Double-diffused MOSFET (DMOS) is one of these power devices. It is formed by using a double ion implantation with two separate implantation masks. The DMOS structure uses a diffused junction rather than photolithography to form the MOS channel. Two types of DMOS transistors are presently in use as shown in Figure 20. The vertical DMOS (VDMOS) transistors uses both sides of the chip; and lateral DMOS (LDMOS) transistors have electrodes located only on the top of the chip [64]. Typically, LDMOS transistors are chosen for integrated smart-power applications as they are more compatible with standard CMOS processing and can be easily integrated by the addition of some extra process layers. VDMOS transistors, however, are less cost-effective to integrate because the current has to be collected at the surface of the silicon and not at the backside, as is the case in discrete devices [65]. The DMOS transistor has some major advantages such as low on-resistance (R_{ON}), high transconductance, small parasitic capacitance, high current and power gain, high voltage operation, as well as fast switching speed without the necessity of extraordinary process and mask [66].

In general, a LDMOS transistor distinguished from a typical MOS transistor in that LDMOS transistor additionally has a drift region extending in a lateral direction between an edge of a control gate and a drain region of the transistors. Reduced surface field (RESURF) technique is usually adopted to design LDMOS transistors to reduce the electric-field in this relatively long drift region, thereby avoiding an electric-field peak at PN junctions [31]. The higher doping concentration in the drift region, the lower conduction resistance it has. These characteristics can be utilized to have a MOS transistor with high breakdown voltage (BV) and low specific on-resistance (R_{ON}) [67].

Figure 2.20 Cross Section of VDMOS & LDMOS [64].

SOI Bipolar/CMOS/DMOS (BCD) device is used in devices/circuit requiring a mix of transistor characteristics and/or operation voltages. It enables simultaneously handling analog and digital power to realize smart power devices for automotive, telecommunication and consumer electronics [68]. Bipolar component is used for analog control; CMOS component is used for digital control; and DMOS component is used for high currents/voltage application.

2.6 Summary

SOI and Partial SOI technology were reviewed in this chapter. Owing to some advantages over the conventional SOI and bulk silicon substrate, PSOI technology gains position in the fabrication of next generation PICs. A number of PSOI fabrication methods have been developed such as selective SIMOX, recrystallisation,

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selective silicon and oxide etching followed by selective epitaxial growth, as well as low temperature wafer bonding.

Related to PSOI technology, thermal-induced stresses, stress effects on device characteristics, and finite element method (FEM) used in semiconductor device analysis are also presented in the Chapter.

Chapter 3 STRESS SIMULATION OF PSOI STRUCTURES

3.1 Introduction

Due to the temperature distribution and the differential thermal expansivities between silicon and silicon dioxide [69], stresses will be induced in the structure [70]. For full SOI structure, it has been shown that the geometry of the full SOI structure does not affect the thermal-induced stress during the high temperature processing [71]. On the other hand, in a partial SOI structure, since the embedded oxide islands are less than the chip length and width, a high stress concentration will be present around the embedded oxide, and its magnitude will likely be affected by the structure geometry [72].

As low temperature medium vacuum wafer bonding (MVWB) is the novel and promising fabrication approach for SOI and PSOI power semiconductor devices since it results in low defect density within the work layer [18], we try to build the embedded oxide substrate model first and then bond it with the work layer which followed MVWB approach in our study.

The normal field oxide fabrication process was used to construct the partial oxide structure. The furnace temperatures used in this work is therefore chosen to be 950°C, which will be the boundary condition in the substrate model. So the stresses

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in substrate wafer are high enough and we cannot ignore it. The residual stress distribution in the substrate will couple to the work layer. In our simulation, we transfer the stresses from substrate wafer structure to all the PSOI structures which will be more accurate and similar to the true bonding process. Meanwhile, CMP process effect is also considered.

In present work, the effects of the structure geometry on the thermal-induced stresses in a partial SOI structure were studied as the results of the power devices self-heating. In order to build more efficient model, the work layer surface temperature is defined as the maximum operating junction temperature of non-punch through IGBT [36]. The surface temperature distribution decides the thermal-induced stresses for the entire PSOI structure.

The residual stresses investigated in the present study are the von-Mises equivalent stresses which relate to all the three normal stresses and the three shear stresses. Two stresses, namely the maximum stress at the surface of the work layer (MSAS) as well as the maximum stress in the work layer (MSAI), are analyzed in this work as they will likely affect the device performance significantly. For example, residual stress will affect the electron mobility [73,74] and hall mobility [75] in the silicon work layer. It will also cause boron re-distribution at the Si/SiO₂ interface [76]. In order to study the effect of the structure geometry on the mechanical residual stress in the partial SOI structure, ANSYS, a powerful Finite-Element software, was used to analyze the stress distribution in partial SOI structure induced by fabrication processes.

In order to identify the importance of the various structural geometric parameters, design-of-experiment (DOE) method was employed. A statistical software package STATGRAPHIC from Manugistics was used to analyze the data.

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To reduce the number of parameters to be studied, some parameters are confined based on the references [7,10,33,34]. Upon identification of the critical parameters, response surface method will be used to build empirical models for the two stresses MSAS and MSAI respectively. The calculation of the two stresses is performed using finite element analysis.

3.2 Computational Approach for Thermal-induced Stresses

3.2.1 Theoretical Background of the Simulation

3.2.1.1 Von-Mises Stress

The stresses studied in this work are the von-Mises equivalent stresses. Von-Mises stress is defined as the internal resistance per unit area of a body to an external applied force. Its yielding does not depend on individual normal stresses or shear stresses alone. Von-Mises proposed in 1913 that yielding occurs when a combination of stresses, i.e., von- Mises stress exceeds the yield strength of material [77].

$$\sigma_0 = \frac{1}{\sqrt{2}} [(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2 + 6(\tau_{xy}^2 + \tau_{yz}^2 + \tau_{zx}^2)]^{\frac{1}{2}} \quad (3.1)$$

where σ_x , σ_y , and σ_z stand for the normal stresses in the x, y, or z directions, respectively; τ_{xy} , τ_{yz} , and τ_{zx} stand for the shear forces which are applied on the planes. When the object is at equilibrium, it can be shown that $\tau_{xy} = \tau_{yx}$, $\tau_{xz} = \tau_{zx}$, and $\tau_{yz} = \tau_{zy}$ based on a moment balance. Thus, the state of stresses at a point is

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completely described by six components, three normal stresses and three shear stresses. The normal stresses are responsible for the normal strain while the shear stresses cause the shear strain.

We considered using Chemical-Mechanical Polishing (CMP) process to polish our substrate wafer surface. CMP provides global and local planarization that can meet the requirements of our wafer bonding. In CMP, the stress on the wafer surface comes from two sources (1) down force from the carrier and (2) shear force from friction on the wafer due to the relative motion of the pad and wafer [78]. The von-Mises stress applied in CMP model developed to investigate the polishing process. Based on the correlation between the calculated von-Mises stress distributions and the distance from the wafer center, found that near the wafer center, von-Mises stress distribution was almost uniform. The von-Mises stress on wafer surface is only 0.04 MPa [79]. Compared with the thermal-induced stress we computed later, it is much smaller. The substrate wafer surface stress distributions change a little after the CMP process. Therefore, we can ignore the influence of CMP process on substrate wafer.

3.2.1.2 Theoretical background of ANSYS

(a) Thermal Energy Equation

The first law of thermodynamics states that thermal energy is conserved. In general, this can be applied to a differential control volume [80,81]:

$$\rho c \left(\frac{\partial T}{\partial t} + \{v\}^T \{L\} T \right) + \{L\}^T \{q\} = \ddot{q} \quad (3.2)$$

Where: ρ = density, c = specific heat, T = temperature, t = time

$$\{L\} = \begin{Bmatrix} \frac{\partial}{\partial x} \\ \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} \end{Bmatrix} = \text{Vector operator}, \{V\} = \begin{Bmatrix} V_x \\ V_y \\ V_z \end{Bmatrix} = \text{Velocity vector for mass transport of}$$

heat, $\{q\}$ = Heat flux vector, and $\ddot{q}$ = Heat generation rate per unit volume.

Next, Fourier's law is used to relate the heat flux vector to thermal gradients:

$$\{q\} = -[D]\{L\}T \quad (3.3)$$

$$\text{Where } [D] = \begin{bmatrix} K_{xx} & 0 & 0 \\ 0 & K_{yy} & 0 \\ 0 & 0 & K_{zz} \end{bmatrix} = \text{thermal heat conductivity matrix, } K_{xx}, K_{yy},$$

K_{zz} = thermal heat conductivity in the element in x, y, and z directions, respectively.

From Equations (3.2) and (3.3), we have

$$\rho c \left(\frac{\partial \cdot T}{\partial \cdot t} + \{V\}^T \{L\}T \right) = \{L\}^T ([D]\{L\}T) + \ddot{q} \quad (3.4)$$

Expanding Equation (3-4) to its more familiar form, it expresses as

$$\rho c \left(\frac{\partial T}{\partial t} + V_x \frac{\partial T}{\partial x} + V_y \frac{\partial T}{\partial y} + V_z \frac{\partial T}{\partial z} \right) = \ddot{q} + \frac{\partial}{\partial x} \left(K_x \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(K_y \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(K_z \frac{\partial T}{\partial z} \right) \quad (3.5)$$

Two types of boundary conditions are considered for a unit volume in the following calculation.

- i. Specified temperature acting over the entire surface:

$$T = T^* \quad (3.6)$$

where T^* is the specified temperature

- ii. Specified convection surfaces acting over the entire surface (Newton's law of cooling)

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$$\{q\}^T \{\eta\} = -h_f \cdot (T_B - T_S) \quad (3.7)$$

where: h_f = film heat transfer coefficient

T_B = Bulk temperature of adjacent fluid

T_S = Temperature at the surface of the model

Combining Equation (3.3) with Equations (3.7), we have

$$\{\eta\}^T [D] \{L\} T = q^* \quad (3.8)$$

$$\{\eta\}^T [D] \{L\} T = h_f \cdot (T_B - T) \quad (3.9)$$

Premultiply Equation (3.4) by a virtual change in temperature, integrate over the volume of the element, and combine with Equations (3.8) and (3.9), we have:

$$\begin{aligned} \int_{vol} \rho c \cdot \delta T \left(\frac{\partial T}{\partial t} + \{v\}^T \{L\} T + \{L\}^T (\delta T) [D] \{L\} T \right) d(vol) = \int_{S2} \delta T \cdot q^* d(S2) + \\ \int_{S3} \delta T \cdot h_f (T_B - T) d(S3) + \int_{vol} \delta T \cdot \ddot{q} d(vol) \end{aligned} \quad (3.10)$$

where vol = volume of the element and δT = allowable virtual temperature ($=\delta T(x, y, z, t)$).

The above equations consider only conduction and convection. Another heat transfer is radiation equation, the heat transfer rate between two surfaces i and j due to radiation is given by:

$$Q_i = \sigma \epsilon_i F_{ij} A_i (T_i^4 - T_j^4) \quad (3.11)$$

where Q_i = heat transfer rate from surface i

σ = Stefan-Boltzmann constant

ϵ_i = Effective emissivity

F_{ij} = View factor from surface i to surface j

A_i = Area of surface i

T_i, T_j = Absolute temperature at surfaces i and j , respectively

(b) Theoretical Stress Analysis

To justify elastic materials, the stress is related to the strain by :

$$\{\zeta\} = [D]\{\varepsilon^{el}\} \quad (3.12)$$

where: $\{\zeta\}$ = stress vector = $\begin{bmatrix} \sigma_{xx} & \sigma_{yy} & \sigma_{zz} & \sigma_{xy} & \sigma_{yz} & \sigma_{xz} \end{bmatrix}^T$

$[D]$ = Elastic matrix which is related to Young's, shear modulus, and Poisson's ratio

$$\{\varepsilon^{el}\} = \{\varepsilon^{to}\} - \{\varepsilon^{th}\}$$

$$\{\varepsilon^{to}\} = \text{Total strain vector} = \begin{bmatrix} \varepsilon_{xx}^{to} & \varepsilon_{yy}^{to} & \varepsilon_{zz}^{to} & \varepsilon_{xy}^{to} & \varepsilon_{yz}^{to} & \varepsilon_{xz}^{to} \end{bmatrix}^T$$

$$\{\varepsilon^{th}\} = \text{Thermal strain vector} = \Delta T \begin{bmatrix} \beta_x & \beta_y & \beta_z & \beta_{xy} & \beta_{yz} & \beta_{xz} \end{bmatrix}^T$$

β_x = thermal expansion coefficient in the x direction

$$\Delta T = T - T_{ref}$$

T = current temperature at the point in question

T_{ref} = reference (strain-stress) temperature

Equation (3.12) may also be inverted to:

$$\{\varepsilon^{to}\} = \{\varepsilon^{th}\} + [D]^{-1}\{\zeta\} \quad (3.13)$$

3.2.2 Simulation Model

In the study of the local effect within a die, we assume that the wafer is large enough so that the wafer edge effect can be ignored. The partial SOI structure

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consists of a periodic array of SiO_2 islands embedded in Si background as shown in Figure 3.1. Here, the SiO_2 layout on a representative x-y plane is shown as blank rectangles. The shaded area, which is elaborated in three-dimension at perspective view in Figure 3.2, refers to the domain used for finite element analysis in this work.

Figure 3.1 Schematic cross-sectional view of SiO_2 islands embedded inside Si substrate on a representative x-y plane. The blank rectangles represent SiO_2 . The shaded area refers to the domain used for finite element analysis.

The substrate wafer structure is shown in the Figure 3.2(a). It is fabricated separately and oxide is grown using standard field oxide fabrication process. Simulation steps follow the real fabrication condition. After CMP, the two wafers, work layer wafer and substrate are bonded together to form the final Partial SOI structure as shown at Figure 3.2(b).

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Figure 3.2 Schematic three-dimensional view of the shaded domain (a) Substrate wafer before wafer bonding, (b) final PSOI structure. This geometric configuration is employed in the finite element analysis to study the local effect.

In the modeling, five parameters, namely oxide length (L_1), oxide width (W_1), oxide thickness (t_{ox}), thickness of the work layer (WL), and thickness of the substrate (Sub) are chosen as the variables. L_0 and W_0 are fixed as $100\ \mu m$ as it is a typical dice size for power semiconductor devices. Note that when $L_0 = W_1 = L_0 = W_0 = 100\ \mu m$, the structure becomes a full SOI structure.

The following boundary conditions were used in the finite element analysis for Figure 3.2. As planes $x = 0$, $L_0/2$ and $y = 0$, $W_0/2$ are mirror symmetrical constraints due to the repetitive structure shown in Figure 3.1, $u_x = 0$ in planes $x = 0$ and $x = L_0/2$; and $u_y = 0$ in planes $y = 0$ and $y = W_0/2$. Here u_x and u_y correspond to the displacements along the x - and y -directions, respectively.

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In the analysis, all materials are assumed to be isotropic and deform elastically. This is justifiable as the yield strength of silicon and silicon oxide are greater than 2 GPa [82,83,84]. Our calculation shown later indicated that the maximum stress in the partial SOI structure calculated using an elastic model is only about 500MPa, which is much lower than their yield strength and located at substrate wafer just after the anneal process. Therefore, an elastoplastic model is not necessary and computational time could be saved using the elastic models. Temperature dependent materials properties are applied to the models and listed in Table 3.1 [46,85,86,94].

Table 3.1 Materials properties of Si and SiO₂ (T in °C)

	SiO ₂ [85,86]	Si [85,94]
Young's modulus (GPa)	$71.4+7.0 \times 10^{-3}T$	$168.9-1.2 \times 10^{-2}(T-273)$
Poisson ratio	0.16	0.262
Coefficient of thermal expansion (°C ⁻¹)	$0.51 \times 10^{-6}+0.54 \times 10^{-9}T$	$2.56 \times 10^{-6}+1.88 \times 10^{-9}(T-273)$
Thermal conductivity (W/(m K))	1.3376	$1/(3 \times 10^{-4}+1.56 \times 10^{-5}T+1.65 \times 10^{-8}T^2)$

In this work, it is assumed that the stress in the substrate wafer has been relieved during the high temperature process, and the structure is in a stress-free state at the furnace temperature of 950°C after annealing process. The stress-free state could be achieved due to the viscous flow of SiO₂ at the high furnace temperature [87]. The thermal loading is modeled by prescribing a uniform temperature change from 950°C to room temperature.

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The residual stress in the substrate wafer is coupled to the final PSOI structure in the simulation. Considering the low temperature wafer bonding process we choose in fabrication, the initial work layer of PSOI has no stress distribution. It means the initial wafers are stress-free states.

The analysis simulation process is shown as following.

(1) Building the module of substrate wafer and work layer: at high temperature which used to grow the partial oxide similar to the LOCal Oxidation of Silicon (LOCOS), the initial stress in substrate wafer is defined as zero. Stresses will thus be induced in the structure due to the differential thermal expansivities between silicon and silicon dioxide in the structure when the substrate wafer cooled down to room temperature. The initial wafer used as work layer is stress-free at room temperature before bonding. The low temperature wafer bonding process is shown in Figure 3.3.

(2) Building the temperature distribution module for the final PSOI structure: the work layer surface temperature is the maximum operating junction temperature of non-punch through IGBT [36] that is typical for power devices. The bottom of the structure is assumed to be isothermal. The substrate wafer backside temperature is defined as normal room temperature. The initial condition of the thermal module is as indicated at step 6, Figure 3.3.

(3) Couple the temperature distribution module to the bonded PSOI structure: the coupled temperature distribution induced the stress redistribution in the PSOI structure.

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Figure 3.3 The processes of forming the simulation for PSOI structure

* T_R denotes the room temperature and the subscript expresses the temperature in Celsius

3.2.3 Numerical Stress Calculation with ANSYS

A general purpose Finite Element Analysis (FEA) software ANSYS was employed for the thermal stress analysis in this study. The finite element analysis tool ANSYS has many powerful capabilities. It could be used from a simple, linear, static analysis to a complex, nonlinear, transient dynamic analysis. ANSYS can analyze thermal field, structural field, electromagnetic field, fluid field, and coupled field.

Normally, a thermal analysis calculates the temperature distribution and related thermal quantities in a system or component. The basis for thermal analysis in ANSYS is a heat balance equation obtained from the principle of conservation of

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energy. There are two typical thermal quantities, including (1) the temperature distributions; (2) the amount of heat lost or gained; (3) thermal gradients; and (4) thermal fluxes. The finite element solution by ANSYS calculates nodal temperatures, and then uses the nodal temperatures to obtain other thermal quantities. ANSYS supports two types of thermal analysis: (1) a steady-state thermal analysis; (2) a transient thermal analysis. In this work, a steady-state thermal analysis is followed by the stress analysis to calculate the thermal stress. Meanwhile, the residual stress obtained from substrate wafer is coupled into the PSOI model.

The nodal thermal stresses in the PSOI structure are calculated by combining a thermal analysis. Since the thermal analysis and respective temperature distribution induced stresses are needed, coupled field analysis is employed in the present work. A coupled field analysis is an analysis that takes into account the interaction between two or more fields. One can couple the two fields by applying the results from the first analysis as load for the second analysis. The data flow diagram is shown in Figure 3.4.

The element type is eight-node element SOLID45 [88] used for substrate wafer. The final PSOI structure used coupled field element SOLID70 and SOLID45. SOLID45 is an element in ANSYS used for the three-dimensional modeling of solid structures. The element is defined by eight nodes for up to six degrees of freedom at each node. SOLID70 has a three-dimensional thermal conduction capability. The element has eight nodes with a single degree of freedom, temperature, at each node. The element is applicable to a three-dimensional steady state or transient thermal analysis. In this study, SOLID70 is used as a thermal element together with an equivalent structural element. SOLID45 to analyze thermal-stress induced in the partial SOI structure.

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Figure 3.4 ANSYS data flow diagram. T(temperature) and S(stress)

3.3 Simulated Stress Distribution

Figure 3.5 Representative finite element discretization for the geometry in Figure

3.2. The mesh shown is for $L_0 = W_0 = 100 \mu m$ and $L_1 = W_1 = 50 \mu m$.

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A representative finite element mesh is shown in Figure 3.5. A mesh refinement was adapted in the silicon dioxide layer since a high stress distribution is expected at these locations.

3.3.1 Maximum Stress at Surface and at Interface

To understand the stress distribution of the partial SOI structure, we choose a particular set of structural parameters as follows: $L_1 = 60 \mu\text{m}$, $W_1 = 50 \mu\text{m}$, $t_{\text{ox}} = 2.75 \mu\text{m}$, $WL = 5 \mu\text{m}$, and $\text{Sub} = 150 \mu\text{m}$. Figure 3.6 shows the contours of von-Mises equivalent stresses at the surface of the work layer and at the Si/SiO₂ interface respectively. The maximum stress in the work layer is found to be at the Si/SiO₂ interface.

(a) the surface of WL

(b) the interface of WL and sub wafer

Figure 3.6 Contours of von-Mises equivalent with $WL = 5 \mu\text{m}$, $t_{\text{ox}} = 2.75 \mu\text{m}$ and $\text{sub} = 50 \mu\text{m}$

The boundaries chosen in Figure 3.5 are the mirror symmetrical constraints previously set in the model as shown Figure 3.2. In the Figures, the bottom-left

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square is the location of the embedded silicon dioxide. From Figure 3.6 the pattern of the stress contour at the surface is influenced by the interface stress distribution.

The stress distribution at the interface is more non-uniform than that at the surface as expected shown in Figure 3.6(b). The high stress region is approximately concentrated on the edge of SiO₂.

Therefore, from the analysis of the stress distribution, one can see that the interfacial stress is very location-dependent, and care must be taken to consider it during wafer bonding and device design.

It is worth emphasizing that, for full SOI structure, the stress fields of both interfacial and surface stresses (i.e., $L_1 = W_1 = L_0 = W_0$) are fully uniform. Hence, the full SOI structure provides a lower stress level compared to the corresponding partial SOI structure.

3.3.2 Statistical Analysis of the Simulated Stresses

In order to take the stress distribution in a partial SOI structure effectively into account, stress model as a function of the various structural parameters is necessary. As the parameter ranges are big, Design of Experiment (DOE) approach is chosen in this study.

3.3.2.1 Response Surface Method [89,90]

To identify the critical structural parameters in the PSOI structure, they determine the stress distribution and its magnitude. These parameters mainly considered the electrical characteristics and would be the foundation in this work. $WL = 5 \mu\text{m}$ and $t_{\text{ox}} = 2 \mu\text{m}$ was used in SOI power devices [9]. The numerical study

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considering the PSOI structure used the parameters $WL = 10 \mu\text{m}$ and $t_{\text{ox}}=0.5\mu\text{m}$. In the breakdown analysis the $WL = 10 \mu\text{m}$ and $t_{\text{ox}}=1\mu\text{m}$ are also the choice [1]. $WL=7\mu\text{m}$, $t_{\text{ox}}=2\mu\text{m}$ and $t_{\text{sub}}=36\mu\text{m}$ as well as $WL=10\mu\text{m}$, $t_{\text{ox}}=1\mu\text{m}$ referred to [7,91] respectively.

Table 3.2 The parameters and levels for the response surface method

symbol	parameters	level		
		1	2	3
t_{ox}	Oxide thickness(μm)	0.5	2.75	5
WL	thickness of work layer(μm)	5	10	15
L_1	Oxide length(μm)	20	60	100
Sub	thickness of sub(μm)	50	150	250

Based on the parameters used in the reference [1,7,91], a more detail experimental design can be employed to establish models for the Maximum Stress At Surface (MSAS) and Maximum Stress At Interface (MSAI) respectively. Response Surface Method (RSM) is employed in this work since it is efficient in terms of the number of runs required. Meanwhile, RSM maintains the accurate results [92]. The parameters and levels for the response surface method are listed in Table 3.2.

Table 3.3 shows the ANalysis Of VAriance (ANOVA) table for the maximum surface stress. P-values less than 0.05 indicate the parameter significantly influence the results. We can see that the key structural parameters in affecting the surface stress are the work layer thickness and the oxide length and thickness. The corresponding model equation for surface stress is given as:

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$$\begin{aligned}\sigma_{MSAS} = & 159.88 - 4.23 \times 10^{-3} * sub + 0.19 * L_1 - 1.66 * WL + 6.59 * t_{ox} + \\ & 2.37 \times 10^{-5} * sub^2 - 1.40 \times 10^{-3} * L_1^2 - 3.15 \times 10^{-3} * L_1 * WL + \\ & 6.25 \times 10^{-2} * L_1 * t_{ox} + 9.90 \times 10^{-2} * WL^2 - 0.49 * WL * t_{ox} - 5.35 \times 10^{-2} * t_{ox}^2\end{aligned}\quad (3.14)$$

where all the dimensions are in μm , and the stress is in MPa.

For the case where maximum stress at interface in Table 3.4, the critical structural parameters are the oxide length, thickness as well as the substrate thickness. The corresponding model equation is shown as follows.

$$\begin{aligned}\sigma_{MSAI} = & 148.38 + 0.14 * sub + 0.14 * L_1 - 2.13 * WL + 34.73 * t_{ox} - \\ & 4.03 \times 10^{-4} * sub^2 + 1.76 \times 10^{-4} * sub * L_1 + 7.22 \times 10^{-3} * sub * WL - \\ & 8.05 \times 10^{-3} * sub * t_{ox} - 1.35 \times 10^{-3} * L_1^2 - 3.92 \times 10^{-3} * L_1 * WL + \\ & 2.90 \times 10^{-2} * L_1 * t_{ox} - 1.53 \times 10^{-2} * WL * t_{ox} - 3.30 * t_{ox}^2\end{aligned}\quad (3.15)$$

where all the dimensions are in μm , and the stress is in MPa.

Table 3.3 Response surface method: analysis of variance (ANOVA) for MSAS

Analysis of Variance for stress					
Source	Sum of Squares	Df	Mean Square	F-Ratio	P-Value
A:sub	6.96316	1	6.96316	2.94	.1120
B:L1	498.843	1	498.843	210.80	.0
C:WL	470.602	1	470.602	198.86	.0
D:tox	1422.21	1	1422.21	600.99	.0
AA	.299779	1	.299779	.13	.7281
AB	.025281	1	.025281	.1	.9194
AC	.085264	1	.085264	.4	.8526
AD	1.09098	1	1.09098	.46	.5100
BB	26.5767	1	26.5767	11.23	.58
BC	1.58256	1	1.58256	.67	.4294
BD	126.63	1	126.63	53.51	.0
CC	32.6623	1	32.6623	13.80	.30
CD	119.749	1	119.749	50.60	.0
DD	.391444	1	.391444	.17	.6914
Total error	28.3975	12	2.36646		
Total (corr.)	2766.02	26			
R-squared = 98.9733 percent					
R-squared (adjusted for d.f.) = 97.7756 percent					
Standard Error of Est. = 1.53833					
Mean absolute error = .759244					
Durbin-Watson statistic = 2.375 (P=.1591)					

Table 3.4 Response surface method: analysis of variance (ANOVA) for MSAI

Analysis of Variance for stress					
Source	Sum of Squares	Df	Mean Square	F-Ratio	P-Value
A:sub	674.265	1	674.265	264.83	. 0
B:L1	44.7297	1	44.7297	17.57	. 13
C:WL	557.562	1	557.562	218.99	. 0
D:tox	17503.4	1	17503.4	6874.70	. 0
AA	86.7077	1	86.7077	34.06	. 1
AB	1.9881	1	1.9881	.78	.3942
AC	52.244	1	52.244	20.52	. 7
AD	13.137	1	13.137	5.16	. 423
BB	24.8189	1	24.8189	9.75	. 88
BC	2.45392	1	2.45392	.96	.3456
BD	27.2432	1	27.2432	10.70	. 67
CC	.0137815	1	.0137815	. 1	.9426
CD	.118336	1	.118336	. 5	.8329
DD	1485.45	1	1485.45	583.43	. 0
Total error	30.5527	12	2.54606		
Total (corr.)	20602.2	26			
R-squared = 99.8517 percent					
R-squared (adjusted for d.f.) = 99.6787 percent					
Standard Error of Est. = 1.59564					
Mean absolute error = .810395					
Durbin-Watson statistic = 1.6688 (P=.1935)					

3.3.2.2 Comparison between Simulation and Models

To estimate the accuracy of the response surface method used in this work, a comparison of maximum interfacial and surface stresses between the simulation results (from ANSYS) and that from Equations (3.14) and (3.15) is done as shown in Figure 3.7, using the structural parameters that are not included in the DOE runs previously. Five runs of L_1 splits are performed with $t_{ox} = 2.75 \mu\text{m}$; $WL = 10 \mu\text{m}$; $Sub = 150 \mu\text{m}$. It is clearly seen in Figure 3.7 that the empirical models established using the response surface method for both the maximum interfacial and surface stresses are in good agreement with the simulated data.

Figure 3.7 Comparison of maximum interfacial and surface stresses between the simulation results and the corresponding empirical models derived from the response surface method.

The full SOI structure is absolutely different from the PSOI structure. The maximum stresses at interface and surface of the full SOI are uniform and equal about to 135MPa. Its break point is at $L_1=100\mu\text{m}$ as analyzed by ANSYS.

3.4 Simulation Analysis

3.4.1 Effect of Geometrical Variables on Maximum Stresses

Table 3.3 and 3.4 indicate that the determining geometrical variables for the MSAS are oxide length (L_1), oxide thickness (t_{ox}) and the work layer thickness (WL). The critical parameters of MSAI are oxide length (L_1), oxide thickness (t_{ox}) and substrate thickness (sub). To illustrate the effect of geometrical variables on the maximum stresses, we choose two of the determining parameters at one time. Since the effects of L_1 and W_1 are equivalent to each other, we arbitrary set $W_1 = 50 \mu\text{m}$ and

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hence only L_1 , t_{ox} and WL , sub are considered. The response surfaces of MSAS and MSAI with respect to any two geometrical parameters are given in Figures 3.8. The key geometrical variables for the MSAS and MSAI were used to analyze, respectively.

From Figure 3.8(a), we see that MSAS increases with increasing t_{ox} . However, the effect of L_1 on MSAS is not significant when t_{ox} is less than $1\mu m$.

MSAI shows a similar variation with increasing t_{ox} as shown in Figure 3.8 (b). In both (a) and (b), the stresses of MSAS and MSAI decrease if L_1 increases more than $70\mu m$ as well as t_{ox} is less than $1\mu m$. The range of parameters can be used as a series of the optimized condition in PSOI structure.

(a) Response surface of MSAS with L_1 and t_{ox} ,

(b) Response surface of MSAI with L_1 and t_{ox} ,

(c) Response surface of MSAS with L_1 and WL (d) Response surface of MSAI with L_1 and sub (e) Response surface of MSAS with t_{ox} and WL(f) Response surface of MSAI with t_{ox} and sub**Figure 3.8** Response surface analysis of MSAS and MSAI

Figure 3.8 (c) also shows that L_1 has less effect on the variation of MSAS. However, MSAS decreases abruptly when WL increases continuously from 5 μm till approximately 10 μm . Figure 3.8 (e) shows the WL effect similar to (c). Further increase of WL did not decrease MSAS.

Figure 3.8 (d) indicates that MSAI will decrease with decreasing L_1 and sub. However, the rate of increase MSAI with decreasing sub is much lower than that with increasing t_{ox} as shown in Figure 3.8 (f). It is similar to MSAS shown as (e).

3.4.2 Determination of Optimal Conditions

Table 3.5 can be utilized to determine the optimal geometric parameters of a partial SOI structure so as to effectively reduce the stresses in the structure.

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Table 3.5 Effects of geometrical variables on maximum stresses

Parameters	Maximum-stress-at-surface (MSAS)	Maximum-stress-at-interface (MSAI)
t_{ox}	Positive	Positive (strong)
WL	Negative	Negative (Not significant)
L_1 (or W_1)	Positive (change with t_{ox})	Positive (change with t_{ox})
Sub	Not significant	Positive

As both MSAS and MSAI depend on the thickness of oxide (t_{ox}) positively, thinner oxide is better for reducing the maximum stresses. This is good since thin oxide is also required in partial SOI LIGBT, a common type of power semiconductor device, in order to obtain high gate control and low subthreshold swing, thus low off-state current [92].

As the work layer thickness (WL) affects both MSAS and MSAI negatively, the work layer should be thick enough to effectively reduce the maximum stresses. According to the results shown in Figures 3.8 (c) and (e), work layer thickness of 8 μm would be a good choice to ensure the magnitudes of the stresses are acceptable.

Also, as indicated by Table 3.5, the effect of L_1 (and W_1) on the variation of MSAI and MSAS is not significant. However, MSAI and MSAS reduce with increasing L_1 (and W_1) over 70 μm . This is because of the stress concentration around the edges of the embedded oxide. The larger area (i.e., $L_1 \times W_1$) of the oxide leads to lower stress at the interface. Therefore, considering the results shown in

Figure 3.8, L_1 larger than $70\text{ }\mu\text{m}$ will be better to reduce the MSAS without increasing the MSAI.

The influence of substrate thickness (Sub) can be excluded in the optimization consideration in MSAS. However, the substrate thickness affects the MSAI positively, the substrate layer should be thin enough to effectively reduce the MSAI since the process of wafer bonding have to consider the interface stress more seriously.

3.5 Summary

Devices fabricated on partial SOI structure have shown improved performance compared with those on full SOI structure. However, few studies in literature were focused on the thermal stresses generated in the partial SOI structure during device under work condition, which affect the device performance.

In this work, finite element models were built to study the distribution of thermal-induced stresses in partial SOI structures. It is found that the stress distribution at the work layer/substrate interface is more non-uniform than that at the surface as expected since high stress is expected at the oxide edge and corner. Maximum stresses at both the surface and the interface are dependent on structural parameters, including oxide length (and width), oxide thickness, substrate thickness and work layer thickness.

The work layer stress distributions from interface to surface are shown as Figure 3.9 where d denotes the distance away from the surface of work layer. The middle parameters we used in DOE have been chosen to illuminate the typical stress distribution.

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In order to assist device designers to take into account of the stress distribution in a partial SOI structure effectively, empirical stress model as a function of the various structural parameters were built using the response surface method (RSM). These statistical models were applied to optimize the structural parameters. It is found that, to effectively reduce the maximum stress in the structure, the following can be adopted:

- (1) the oxide should be as thin as possible
- (2) work layer thickness should be in the range of 8-10 μm and
- (3) substrate layer should be thin enough

The results are the foundation of the power device fabrication and construction when investigates E-T-S coupled-field effects in Chapter 4 and Chapter 5.

(a) side view from y-direct

(b) $d=0\mu\text{m}$ (c) $d=2.5\mu\text{m}$ (d) $d=5\mu\text{m}$

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(e) $d=7.5\mu\text{m}$

(f) $d=10\mu\text{m}$

Figure 3.9 Crosssection of work layer von-Mises equivalent stress with $WL = 10 \mu\text{m}$,
 $t_{\text{ox}}=2.75 \mu\text{m}$ and $\text{sub}=150 \mu\text{m}$

Chapter 4 ELECTRIC-THERMAL-STRESS COUPLED-FIELD MODELING

4.1 Why E-T-S coupled field modeling

The ITRS2006 indicates the necessity of considering the electrical-thermal-stress (E-T-S) interaction in the device simulation since the heat dissipations of electronic devices are increasing, and the induced mechanical stresses in the devices can no longer be neglected as the device dimension is shrinking. This stress can cause a change in the bandgap of the semiconductor material, which in turn affects the carrier mobilities, rendering non-uniform current flow and non-uniform temperature and stress distributions. Therefore, the effects of electrical, thermal and mechanical stresses on device characteristics are inter-relating, and their effect should be considered concurrently. As power electronic devices dissipate much higher power, the necessity of the E-T-S interaction may arrive earlier.

While the effect of self-heating has been considered in the power device simulation, the modeling of the mechanical stress due to non-uniform temperature distribution in the device is still lacking due to the present limitation of Medici, a commonly used device simulator, on the thermal-stress (T-S) simulation. Although ANSYS, a popular commercial finite element analysis software can perform the

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thermal-stress simulation easily, it cannot be used for semiconductor device simulation due to its limitation on conductive electrostatic simulation.

In this work, we employ another finite element analysis software, COMSOL for the E-T-S coupled-field simulation of a power diode, a basic building blocking for power electronic devices and circuits, and as an initial attempt, we limit the scope of our work here to only the steady state operation of the diodes.

To verify the correctness and accuracy of our E-T-S model, our E-T sub-model of the power diode is compared with the results from Medici, and our T-S sub-model of the power diode is compared with the results from ANSYS. To account for the effect of stress on the electrical characteristics of the power diode, a S-E sub-model is developed. This S-E sub-model computes the effect of stress on semiconductor materials parameters such as carrier mobility and energy bandgap [45,93].

4.2 Physics of the Electrical-Thermal Modeling

For the electrical-thermal (E-T) coupled simulations, the heat transfer equation was solved together with the Poisson and continuity equations for electrons and holes given below [47].

$$\nabla(\nabla\phi) = \frac{q}{\epsilon} \cdot (n - p - N) \quad (4.1)$$

$$\nabla \vec{Jn} - q \cdot \frac{\partial n}{\partial t} = q \cdot R \quad (4.2)$$

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$$\nabla \vec{Jp} + q \cdot \frac{\partial p}{\partial t} = -q \cdot R \quad (4.3)$$

$$\rho \cdot c \cdot \frac{\partial T}{\partial t} - \nabla(K(T)\nabla T) = H \quad (4.4)$$

$$R = R_{SRH} + R_{Auger} \quad (4.5)$$

$$H = \vec{Jn} \bullet \vec{En} + \vec{Jp} \bullet \vec{Ep} + R \cdot E_g \quad (4.6)$$

$$K(T) = (a_1 + a_2 \cdot T + a_3 \cdot T^2)^{-1} \quad (4.7)$$

where ϕ indicates the electrostatic potential; n and p are the respective electron and hole concentrations in the n-drift region; N represents the fixed charge in the n-drift region that is associated with ionized donors; ρ and c are the specific mass density and specific heat of silicon respectively. R is the net generation/recombination rate of the carriers, H is the heat generated per unit volume due to carrier transport and carrier recombination/generation, and $K(T)$ is the thermal conductivity of silicon [47, 94]. R_{SRH} and R_{Auger} are the Shockley-Read-Hall and Auger generation-recombination rate in the n-drift region respectively; E_g is the silicon band gap. The constants a_1 , a_2 and a_3 in equation (4.7) are shown in Table 4.1 for silicon [46,85,86,94,95].

As the power diode structure consists of both very low and high doping concentrations, and the device could operate under high level injection over a wide temperature range, the Shockley-Read-Hall (SRH) and Auger recombination processes, bandgap narrowing effect, the temperature and concentration dependant lifetime are considered. The Arora mobility model including a temperature and doping concentration dependence in addition to the high field effect is also considered in the electrical (E) modeling here.

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Figure 4.1 Schematic cross section of a high power P+NN+ rectifier for this work. the doping concentrations are $N_a = 1 \times 10^{19} \text{cm}^{-3}$, $N_d = 1 \times 10^{16} \text{cm}^{-3}$, $N_{d+} = 1 \times 10^{19} \text{cm}^{-3}$, $d = 125 \mu\text{m}$.

Figure 4.2 Power P+NN+ Diode mesh structure used in COMSOL. The units of x-axis and y-axis are m.

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The schematic cross sections of the devices under study are shown in Figure 4.1. The map mesh structure used in this work is shown in Figure 4.2 where the highest mesh density can be observed in the depletion region. The map mesh structure has better convergence rather than the triangular mesh due to its efficient mesh density definition at the boundary and depletion region in COMSOL. Meanwhile the map mesh consumes less computing time.

Figure 4.3 Comparison of the static forward IV characteristics obtained using COMSOL and Medici

In the E model, for the boundaries in contact with the insulator, symmetric boundary conditions are used where normal flux is zero across the line, and the electric field and carrier currents have zero normal components at these boundaries. These boundary conditions are described with Neumann boundary conditions [47,96]. In the T model, the boundaries in contact with the anode and cathode are held at a

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reference temperature T_{ref} . This corresponds to the boundaries in an air stream of T_{ref} . The other boundaries are defined as heat insulation.

Comparison of the results from COMSOL and Medici are shown in Figures 4.3, 4.4 and 4.5, and good agreement can be observed. The slight discrepancies in the comparison results are found to be due to the different mesh density used in Medici and COMSOL. When denser mesh structure is used, the temperature distribution of COMSOL simulation results is closer to Medici especially in the P+ region as shown in Fig 4.5, but the required simulation time becomes very long, in the order of 10 hours.

Figure 4.4 Comparison of the maximum temperature characteristics versus anode voltage obtained using COMSOL and Medici

Figure 4.5 Comparison of the temperature distributions (at $x=0\mu\text{m}$, $V_a=2.5\text{V}$) computed using COMSOL and Medici

4.3 Physics of the Thermal-Stress Modeling

The thermal-induced mechanical stresses are mainly due to non-uniform temperature distribution within a material and thermal expansion mismatch between the materials [40,41].

Non-uniform temperature distribution within a material produces a temperature gradient. Once the temperature distribution is calculated, the strain produced in the material due to the temperature gradient is given by

$$\varepsilon = \alpha(T_2 - T_1) \quad (4.8)$$

where α is the thermal expansion coefficient of the material. The corresponding thermo-mechanical stress distribution can then be determined using the formulas for axis symmetric plane stress [40].

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Thermal expansion mismatch exists between the silicon and oxide due to the different thermal expansivities which in turn produces mechanical stress in the material. The maximum stress usually occurs at the interface and the corner of a device structure. As the temperature changes from T_1 to T_2 from silicon to oxide, and the strain experienced by the oxide is given as [40,41]

$$\epsilon_{ox} = (\alpha_{ox} - \alpha_{si})(T_2 - T_1) \quad (4.9)$$

where α is the thermal expansion coefficient and the subscripts ox and si denote oxide and silicon respectively.

The inclusion of mechanical stress in the device complicates the device simulation, requiring the use of physics-based modeling to obtain more accurate results.

The stresses studied here are the von-Mises equivalent stresses because it includes all the three normal stresses and the three shear stresses. In this work, all materials are assumed to be isotropic and deform elastically. This is justifiable as the yield strengths of silicon and silicon oxide are greater than 2 GPa [82,97]. In the power diode structure, the calculation indicated that the maximum stress by the elastic model is only about 50MPa, which is much lower than their yield strengths.

The COMSOL T-S model is verified by ANSYS. The two-dimensional von-Mises stress distribution is shown in Figures 4.6 and 4.7 where the temperature distribution in the structure is obtained at the applied forward voltage $V_a=2.5V$. Due to the three-dimensional structure of real power device, the plane strain application model is used to analyze the two-dimensional thermal strain effect when the z displacement is restricted due to z-direct symmetry. In this case, the ϵ_z , ϵ_{yz} and ϵ_{xz} components of the strain tensor are assumed to be zero. The temperature distribution

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of E-T simulation results in power diode from Medici is transferred to ANSYS as body load. This step results in a slight difference in the stress distribution in the device as computed from ANSYS since the temperature approximation and mesh structures change between Medici and ANSYS.

Figure 4.6 2D Stress distribution in the power diode simulated by COMSOL. The units of x-axis and y-axis are m.

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Figure 4.7 2D stress distribution in power diode using ANSYS. The units of x-axis and y-axis are m.

4.4 Physics of Stress-Electrical Modeling

The change in the electrical performance of a silicon device due to mechanical stress was noticed when piezoresistive effect was reported by Smith [23]. This piezoresistance effect is due to the distortion of its band structure in a strained semiconductor [98,99]. Among the various approaches such as the pseudopotential method [100], the linear coupled atomic orbital method [101], the free-electron approximation method, and the $k \cdot p$ perturbation method [46], the $k \cdot p$ method is the most suitable method since it provides sufficiently high accuracy and requires less

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computing resources. Furthermore, the $k \cdot p$ method can incorporate the spin-orbit coupling effect fairly efficiently [102].

In S-E modeling, the conduction band, valence band as well as electron and hole mobilities are analyzed respectively as follows.

Under the mechanical stress, the band structure of a semiconductor will be modified either in the form of energy shifting, change in the shape of the band structure, change in the degeneracy of the bands or any combination of the above-mentioned [102]. Since the conduction band only shift in energy in strained silicon, the effective mass is unchanged due to the unaltered shape of the conduction band.

The shift in energy of the conduction band in our stress-electrical (S-E) model is computed using the deformation potential theory from Bir and Pikus [46]. In this model, the mechanical stress effects on the electron are considered, and the stress-induced sub-band splitting for conduction band with associated effective masses are included [103]. Material properties of silicon used in simulation are listed in Table 4.1. The shifts in the band extrema for a general strain tensor ε is given as

$$\Delta E_{Ci} = \Xi_d Tr[\varepsilon] + \Xi_u \varepsilon_{ii} \quad (4.10)$$

where ΔE_{Ci} represents the shift in the band edge of the i^{th} ellipsoidal conduction minimum, Tr indicates the trace of a matrix, and Ξ_d , Ξ_u are deformation potential parameters. From theses shift of the band extrema, effective adjustments to the conduction band edges used in transport equation can be generated. With this model, the stress-induced changes to the bandgap and electron affinity are computed [46].

On the other hand, the effects of strain on the valence band are different from its effect on the conduction band due to its degenerate nature. The shape of the band

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structure is altered by the strain, resulting in a change in the hole effective mass and mobility. In addition, the symmetry of the band structure is reduced and bands are shifted in energy by an amount related to the strain. The spin-orbit coupling effects need to be taken into account in the stress-electrical (S-E) model for the valence band. Adopting the method employed by Manku and Nathan who developed an analytical expression for the band structure [104], we first proceed to establish the notations to be used and obtain the corresponding solution to the problem without the spin-orbit effects. Subsequently, the spin-orbit effect is included as a perturbation.

Table 4.1. Material properties of Si used in simulation

parameter	Value or expression	Units
Young's modulus	$168.9-1.2 \times 10^{-2}(T-273)^{a,b}$	[GPa]
Poisson ratio	$0.262^{a,b}$	-
Coefficient of thermal expansion	$2.56 \times 10^{-6} + 1.88 \times 10^{-9}(T-273)^{a,b}$	[K ⁻¹]
Thermal conductivity	$1/(3 \times 10^{-4} + 1.56 \times 10^{-5}T + 1.65 \times 10^{-8}T^2)^{c,e}$	[W/(m K)]
Heat capacity	$850.9 + 152.2 \times 10^{-3}T - 158.2 \times 10^{-5}T^2^{d}$	[J/(kg K)]
density	2329^a	[kg/m ³]
^a Reference 85 ^b Reference 86 ^c Reference 94 ^d Reference 95 ^e Reference 46		

Given the Schrödinger equation at wave vector $k=k_0$ for a periodic lattice as

[46]

$$\left(\frac{p^2}{2m} + V(r) + \frac{\hbar}{m} k_0 \cdot p\right) u_{nk_0} = \left(E_0 - \frac{\hbar^2 k_0^2}{2m}\right) u_{nk_0} \quad (4.11)$$

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where $V(r)$ is the potential of the unstrained unit cell, E_0 is the energy spectrum of the unstrained material at k_0 , and u_{nk_0} is the unstrained degenerate electron Bloch wave function at k_0 . When the semiconductor material is strained, its unit cell will be deformed. Assuming the strain is not severe enough to destroy the periodicity of the material, the new Bloch wave function u'_k will satisfy the following equation [104]

$$\left(\frac{p'^2}{2m} + V(r') + \frac{\hbar}{m}(k_0 + k) \cdot p'\right)u'_k = \left(E_k - \frac{\hbar^2}{2m}(k_0 + k)^2\right)u'_k \quad (4.12)$$

where $V(r')$ is the potential within the deformed cell, $k_0 + k$ is the new wave vector, and E_k is the new energy spectrum at k . For silicon, this is reasonable if the stress is below 1GPa [103].

Comparing Eqn (4.11) and (4.12), the perturbation term in the potential can be written as

$$\Delta V = \sum_{i,j=1}^3 \Xi_{ij} \varepsilon_{ij} + \left(\frac{\hbar}{m} k \cdot (p + \hbar k_0) + \frac{\hbar^2 k^2}{2m}\right) + i \frac{\hbar^2}{m} \sum_{i,j=1}^3 k_i \varepsilon_{ij} \frac{\partial}{\partial x_j} \quad (4.13)$$

where

$$\Xi_{ij} = \frac{\hbar^2}{m} \frac{\partial^2}{\partial x_i \partial x_j} + V_{ij}(r) + i \frac{\hbar^2}{m} k_{0i} \frac{\partial}{\partial x_j} \quad (4.14)$$

ε_{ij} denotes the strain tensor in the coordinate system.

Next, we obtain the solution of either k_2 or E_k for the heavy-hole (HH), light-hole (LH), or spin-orbit (SO) as follows [87]

$$(k^2, E_k) = \begin{cases} \zeta \cos(\psi) - P_2^\sigma / 2 & \text{(HH)} \\ \zeta \cos(\psi + 4\pi/3) - P_2^\sigma / 2 & \text{(LH)} \\ \zeta \cos(\psi + 2\pi/3) - P_2^\sigma / 2 & \text{(SO)} \end{cases} \quad (4.15)$$

where σ can be either E_k or k_2 , and

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$$\begin{aligned}\zeta &= 2\sqrt{-\rho/3}, & \cos(3\psi) &= 3\xi/\zeta\rho \\ \rho &= \frac{1}{3}[3P_1^\sigma - (P_2^\sigma)^2], & \xi &= \frac{1}{27}[2(P_2^\sigma)^3 - 9(P_2^\sigma)^2 P_1^\sigma + 27P_0^\sigma]\end{aligned}\quad (4.16)$$

$$\begin{aligned}P_j^{(E)} &= \frac{1}{a_{30}} \sum_{i=0}^{3-j} a_{ji}(\theta, \phi, \varepsilon) E_k^i & \forall \quad \sigma = E_k \\ P_j^{(k^2)} &= \frac{1}{a_{03}} \sum_{i=0}^{3-j} a_{ji}(\theta, \phi, \varepsilon) k^{2i} & \forall \quad \sigma = k^2\end{aligned}$$

the coefficient a_{ij} are functions of the deformation potentials θ and ϕ , strain element ε , and the energy difference between the two ellipsoids. With the above equations, the valence band structure of the strained silicon can be obtained.

Mobility is also influenced by the strain in the devices. In the rigid-shift stress model [45], modifications to the electron mobility are induced by a change in the occupancy of the different conduction band minima whose energies are split by the stress. In the crystallographic coordinate system, the electron mobility is represented by a tensor as follows [103]

$$\mu_n = \mu_0 \begin{pmatrix} 1 + \beta_1 & 0 & 0 \\ 0 & 1 + \beta_2 & 0 \\ 0 & 0 & 1 + \beta_3 \end{pmatrix} \quad (4.17)$$

Where μ_0 is the nominal, isotropic mobility without stress and

$$\beta_i = \left(\frac{1 - m_L / m_T}{1 + 2m_L / m_T} \right) \left(\exp\left(\frac{\Delta E_C - \Delta E_{Ci}}{kT} \right) - 1 \right) \quad (4.18)$$

here ΔE_C denotes the net effective shift of the conduction band; ΔE_{Ci} is the shift in the band edge of the i^{th} ellipsoidal conduction minima; m_L and m_T are the effective mass of electron along the [100] and [001] axes at the conduction band minima.

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The stress enhanced hole mobility model was also reported by [45] where the deformation potential theory was used. Fischetti [105] also provided a $k \cdot p$ mobility model for holes, but the model is not computationally efficient. Recently, Intel presented a physics-based stress induced hole mobility enhancement model which is suitable for the implementation in a continuum transport simulation based on the drift-diffusion theory or the energy balance principle [106]. Furthermore, the model can work in conjunction with a standard non-stressed mobility model, and it is suitable for a wide range of stress magnitudes, crystal orientations, and biasing conditions.

Under a wide range of stress conditions, it is found that the majority of the holes carriers reside in the heavy hole band due to their preponderance [107]. The heavy hole band is represented by two overlapping prolate ellipsoids in the k -space, and the ellipsoids are separated by an energy. Each ellipsoid is described by two hole effective masses, m_T and m_L , in the transverse and longitudinal directions respectively. The hole mobility tensor μ_p in the principle coordinates is expressed as [106]

$$\bar{\mu}_p = \begin{pmatrix} \frac{\langle \tau \rangle f_1}{m_{t1}} + \frac{\langle \tau \rangle f_2}{m_{t2}} & 0 \\ 0 & \frac{\langle \tau \rangle f_1}{m_{l1}} + \frac{\langle \tau \rangle f_2}{m_{l2}} \end{pmatrix} \quad (4.19)$$

where f_1 and f_2 are the fraction of the total hole population in ellipsoids 1 and 2 respectively, and $\langle \tau \rangle$ is the mean-free time of holes .

Giles et. al. [107] showed that the mean-free time between collisions for holes can be considered as constant, and hence the scalar mobility of holes can be simplified as [106]

$$\mu_p = 2\mu_0 \frac{m_t m_l}{m_t + m_l} [\cos^2 \theta (\frac{f_1}{m_{t1}} + \frac{f_2}{m_{t2}}) + \sin^2 \theta (\frac{f_1}{m_{l1}} + \frac{f_2}{m_{l2}})] \quad (4.20)$$

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where μ_0 refers to the unstrained mobility, θ is the angle between the axis of the ellipsoid of the HH and the direction of the local field in the device coordinates. f_1 and f_2 are given as

$$\begin{aligned}
 f_1 &= \frac{\exp(\frac{\Delta}{2kT})}{\exp(\frac{\Delta}{2kT}) + \exp(-\frac{\Delta}{2kT})} \\
 &= \frac{1}{1 + \exp(-\frac{\Delta}{kT})} \\
 f_2 &= 1 - f_1
 \end{aligned} \tag{4.21}$$

and Δ is the energy difference of the two ellipsoids.

If the stress tensor is expressed in the crystal coordinates with the components of shear stress (s), biaxial stress (b), and asymmetric uniaxial stress (a), using n^{th} -order Taylor expansion, the above-mentioned model parameters can be simplified as given below, where the coefficient d relates the energy shift of the ellipsoids to the shear stress [106].

$$\begin{aligned}
 \Delta &= \sum_{i=0}^n d_i s^i \\
 \frac{1}{m_{ti}} &= \frac{1}{m_{ti0}} [1 + \sum_i m s_{ti} s^i + \sum m b_{ti0} b^i] \\
 \frac{1}{m_{li}} &= \frac{1}{m_{li0}} [1 + \sum_i m s_{li} s^i + \sum m b_{li0} b^i]
 \end{aligned} \tag{4.22}$$

Under the high field condition where the electron energy is much greater than the energy shift due to stress, the hole population becomes essentially symmetric, and mobility enhancement is reduced with the saturated mobility dominated by the saturation velocity of the electrons. In this case, the carrier temperature rather than lattice temperature is used in the calculation of the relative populations of holes in the HH and LH bands.

4.5 Discussions for the E-T-S coupled field modeling

In this discussion, we investigate the mobility changes with the thermal-induced stress in the power diode under DC forward behavior. The thermal-induced stress distributed in power diode structure is mainly a biaxial compressive stress. Thus, in order to analyze the stress effect systematically, the impact of asymmetric compressive stress on electron and hole mobilities is shown in the Table 4.2. Improvement/degradation is reversed for tensile stress. The subscripts // and $\perp$ refer to the directions parallel and perpendicular to the uniaxial compressive stress in the plane of the power diode, and $\angle$ indicates the transverse direction out of plane.

Table 4.2 The impact of asymmetric compressive strain on N-type and P-type Si mobility.

		<100>		
Direction of stress change		//	$\perp$	$\angle$
Performance	N	Degrade	Improve	Improve
Impact	P	Improve	Degrade	Degrade
		<110>		
Direction of stress change		//	$\perp$	$\angle$
Performance	N	Degrade	Improve	Degrade
Impact	P	Improve	Degrade	Degrade

The results are also consistent with 3D strain engineering in process-strained Si [108,109] and with nanotechnology featuring strained-Silicon based on the piezoresistive effects reported in [110,111] for <100> and <110> channel devices on (001) silicon substrate. Meanwhile, the different crystal orientation has significantly

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different stress which enhances or reduces the carrier mobility. Hence, the changes of carrier mobilities depend on not only the stress magnitude but also the crystal orientation.

Figure 4.8. σ_{xx} and σ_{yy} along the x-axis at $y=100\mu\text{m}$ in power diode

Since uniform doping across a wafer is usually obtained, the doping concentration perpendicular to the current flow direction can be assumed to be constant. Hence, the change in mobility in x direction depends only on the stress effect and temperature changes. For illustration, the stress σ_{xx} and σ_{yy} along the x-axis at $y=100\mu\text{m}$ in a power diode are plotted in Figure 4.8. The analysis of the stress effect on electron mobility in N region and hole mobility in P+ region are shown in Figure 4.9.

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Figure 4.9 Relative electron mobility tensor components (at $y=100\mu\text{m}$) and hole mobility (at $y=25\mu\text{m}$) in strained-Si power diode along x-axis

Figure 4.10 Simulated DC forward current with and without stress effects

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A change in device static forward current with strain can result from the changes in the carrier effective mass and mobility, arising from the strain-induced changes in the energy band-structure. The effects of strain on the DC performance of power diode are shown in Figure 4.10. Comparing the forward characteristic with and without stress effects, the forward current is found to be reduced at a given forward bias due to the induced stress. The change is about 5% maximum.

One of the most critical aspects of a power diode is its switching characteristics. A high power diode differs from its small signal counterpart in the drift region parameters. Because of the significantly longer drift region with low doping density, recovery transients occur when a forward conducting diode is turn off rapidly, and the internally stored charges cause transient reverse current to flow at reverse voltage. In this work, step application voltage is assumed. The power diode is operated in the steady state before turn-off and turn-on in the simulation. However, by comparing the recovery transient current waveforms obtained from COMSOL with stress effect and Medici without stress effect, we found that the effect of stress on the transient characteristics is negligible. This is because of the limited increase in temperature during device operation.

4.6 Summary

The requirement of E-T-S coupled-field modeling of semiconductor devices demands the use of finite element analysis for device simulation. In this work, a coupled electrical-thermal-stress model is developed, taking the stress-induced modification of the Si band structure into account. Comparison of the results from COMSOL and Medici as well as COMSOL with ANSYS shows good agreement.

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Meanwhile, the stress effects are computed using the E-T-S coupled field model and we have demonstrated that the electron and hole mobilities of (010) biaxial stressed power diode are changed due to band energy splitting. The strain-induced changes of bandgap and effective mobilities cause the static drive current to reduce by about 5%, but their effect on diode transient characteristics seems to be insignificant.

Chapter 5 APPLICATION OF E-T-S COUPLED-FIELD MODELING ON PSOI/SOI POWER DEVICES

The requirement of electrical-thermal-stress (E-T-S) modeling of semiconductor devices as indicated by ITRS2006 demands the use of finite element analysis (FEA) for device simulation. In this work, we perform E-T-S coupled-field simulation from first principles by considering the stress-induced modification of the Si band structure, and employ the finite element analysis software COMSOL to apply the E-T-S model to the study of lateral power diodes and LDMOSFETs as examples. This power diode is a basic building blocking for power electronic devices and circuits, and only the steady state characteristics of the lateral power devices are considered as a first attempt for the E-T-S model application.

5.1 Electrical-Thermal-Stress Coupled-field Effect in SOI and Partial SOI Lateral Power Diode

5.1.1 Introduction

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Simulation is performed on two types of power diodes, namely the SOI and partial SOI (PSOI) diodes because the temperature and mechanical stress distributions are very different in these diodes even under the same operating conditions. Temperature contours and stress distribution in the devices are analyzed under both the forward and reverse bias conditions.

Silicon-on-insulator diodes are considered in this work because SOI is becoming an important silicon technology for the near future owing to its many advantages such as the improved isolation, reduced leakage currents and faster switching speed [2]. However, direct application of SOI technology to power semiconductor devices would result in poor unacceptable heat dissipation [2, 5]. Partial SOI (PSOI) technology was proposed so that the advantages of SOI devices can be retained while good heat dissipation can be ensured [10].

The purposes of this work are two folds. Firstly, we like to present a methodology to study the E-T-S interaction in a semiconductor device via semiconductor band structure modification. This is done through the integration of various existing E-T, T-S and S-E models. As the E-T-S interaction is complex, we would like to see the necessity of the E-T-S model by comparing the simulation results from E only, E-T only and E-T-S. Secondly, we like to apply our E-T-S model to examine the potential of PSOI for power devices.

Due to the complexity of the E-T-S model, we limit our scope to 2D modeling. Such a 2D modeling approach is suitable for devices with a periodic structure as well as long-width structures [94,96] which are used in power device simulation [112,113,114,115] or novel device simulation [116].

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5.1.2 Device Structure and Simulation of Fabrication Process

The schematic cross sections of the devices under study are shown in Figure 5.1. Generally, the breakdown voltage of a conventional SOI power diode is limited by the buried oxide thickness, SOI thickness and the length of the n- drift region [7,10]. The above-mentioned parameters are shown in Figure 5.1.

As an example, a conventional SOI lateral power diode with an SOI layer thickness t_{SOI} of 8 μm and a buried oxide thickness t_{ox} of 0.5 μm has a maximum breakdown voltage (BV) of 200V if the light-doping region of the device is doped according to the RESURF principle [33,34]. If t_{SOI} is increased to 12 μm while keeping other device parameters unchanged, the maximum breakdown voltage is about 270V. With further optimization on the RESURF, the breakdown voltage can be even higher, however, the optimization is not the scope of this work.

Table 5.1 Device parameters used in present study

	PSOI	SOI
work layer thickness t_{soi} [μm]	8	8
buried oxide thickness t_{ox} [μm]	0.5	0.5
diode dimension [μm]	20	20
open window length [μm]	10	0

For a partial SOI lateral power diode, a silicon window is placed under the cathode as shown in Figure 5.1(a). In this work, the t_{SOI} , t_{ox} , and SOI work layer doping concentration of both the partial SOI and full SOI lateral power diode are

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identical. The widths of both types of diodes are $20\text{ }\mu\text{m}$ which is adequate to withstand a high breakdown voltage at reverse bias condition [9, 33]. The values of the structure parameters are shown in Table 5.1 [117].

Figure 5.1 The schematic cross sections of Lateral power rectifier on (a)Partial SOI and (b)SOI structure

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The fabrication process for the PSOI diodes is compatible with power LDMOSFETs used in industry, which involves confidential information from the manufacturer, shown in Figure 5.2. As the impurity profiles of the P+ and N+ regions are important to the device's performance, the device fabrication process were simulated by Tsuprem4 [118].

Tsuprem4 is a simulator of Synopsys for simulating the semiconductor process used in the manufacturing of silicon integrated circuits and discrete devices. It simulates the incorporation and redistribution of impurities in a two-dimensional device cross-section perpendicular to the surface of the silicon wafer. The output information provided by the program includes boundary of various layers of materials in the structure as well as distribution of impurities within each layer.

Figure 5.2 Process flow of fabrication lateral power rectifier

Fabrication of partial SOI power semiconductor devices is presently still under exploration. One of the possible methods is through the use of low temperature wafer bonding process [119], and the induced stress in the wafer was analyzed previously

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and found to be low [7]. Also, the devices are covered with thin layer of PE-TEOS (plasma enhanced tetra-ethyl ortho silicate) deposited at low-stress condition which does not induce high-stress in device region and the induced stress is normally lower. Thus, the stress that remains in the device after its manufacturing need not be considered as initial condition in our case. However, for other fabrication process such as SIMOX etc, the induced stress from manufacturing and packaging can be high, and the effect of the induced stresses remain in the device on its performance can be an interesting and useful study extended from our present work, and it will be our future work.

Figure 5.3 Doping profile of lateral power diode in PSOI and SOI. The units of x-axis and y-axis are μm .

The P+ anode and N+ cathode region are formed by high dose, low energy of BF_2 and arsenic respectively after the thermal circle for gate oxide, poly deposition and spacer. A rapid thermal annealing (RTA) step was followed to produce a shallow

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junction. The doping profile of lateral power diodes in PSOI and SOI are shown in Figure 5.3. The doping distribution results are then transferred to COMSOL for E-T-S coupled field analysis.

5.1.3 Results and Discussions

With the selection of the appropriate models as discussed earlier, an integration of the models is necessary in order to study the E-T-S interaction in a device. Figure 5.4 shows the flow chart of the integration methodology. In this work, we employ the finite element analysis method for the integration using a commercial finite element software COMSOL as platform as it allows flexibility for users to input partial differential equations easily.

The meshing for the device under study is chosen map-mesh for the finite element analysis which consists of quadrilateral (quad) elements. The quad mesh is generated using a mapping technique. For each subdomain, the mapping algorithm defines a regular grid on a logical unit square and then maps it onto the real geometry using transfinite interpolation [96].

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Figure 5.4 Flow chart of the interaction of E-T-S simulation

For the boundary condition, in the E model, a Neumann boundary condition [47,96] is used at the boundaries of the contact with the insulator around the drift region, i.e. the top boundaries. This symmetric boundary condition is used where the normal flux is zero across the boundary, and the electric field and carrier currents have zero normal components at these boundaries.

Considering the device temperature, it is necessary to include the self-heating effect in the device simulation. Under forward bias conditions, there are generally four possible sources of dynamic power dissipation in the diode model [120]. The first is (a) the current induced by the junction capacitance, which is clearly non-dissipative.

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The other sources are: b) current due to recombination in the drift zone, c) current due to diffusion of carriers in the drift region, and d) current due to charge sweep-out effects. These effects are considered dissipative and are included in the total power dissipation calculation in this work through self-consistence solution to the device equations.

The bottom of the devices is assumed to be isothermal. In the simulation, a heat sink is attached to the bottom of the device via a thermal interface material (TIM) with thermal resistance of 105 K/W- μm which corresponds to an inclusion of an additional about 128 μm thick silicon region at the bottom of the device [94]. A constant temperature sink of 300K is used as the thermal boundary at the bottom of the device (Dirichlet). To reduce the simulation time, a substrate thickness of 22 μm is used which is enough for the accuracy of simulation [71]. With the TIM, the effective substrate thickness is about 150 μm . By introduction of TIM with specific thermal resistance, realistic thermal boundary conditions for the nonisothermal simulation of power devices can be achieved without the necessity to include very large material regions.

The strain tensor used in the band shift calculations is computed from the stress tensor via the compliance tensor, S , using a generalized form of Hooke's law to account for anisotropy. For cubic semiconductors like silicon, this can be written in the crystallographic coordinate system in terms of three unique coefficients known as S_{11} , S_{12} , and S_{44} [38]. In the study of the residual stress within the structure, we assume that the wafer is large enough so that the edge effect of the wafer can be ignored. The partial SOI structure consists of a periodic array of SiO_2 islands embedded in Si background. Therefore, the sides of the domain are assumed to have zero horizontal displacements.

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With the E-T, T-S and S-E models described above, we apply the integrated model to study the effect of stress and self-heating on the SOI and partial SOI lateral diodes. Their thermal characteristics and stress effects will be compared at the same operating conditions. The comparison of the E only, E-T and E-T-S models will also be made from the calculation to examine the significance of the E-T-S model.

We perform the simulation to examine the static electrical characteristic of the SOI and PSOI lateral diode, and the results are discussed below.

5.1.3.1 Forward Electrical Characteristics

Figure 5.5 compares the current-voltage simulation results of SOI and PSOI lateral power diodes using the electrical model, the coupled electrical-thermal model, and the fully coupled E-T-S model, respectively. From Fig 5.5, two comparisons can be made as follows.

1. Comparison of the models

Looking at the diode forward characteristics, one can see that E-T-S model predicts a lower current at high forward voltage condition as compared to the other two models, but negligible difference for the three models when the forward voltage is low. This is likely to be due to the increased severity of the self-heating at higher forward voltage which in turn causes a higher strain in the material. Hence, one would expect that the difference of the E-T-S model with the other two models will likely to be larger if the operating temperature of the devices becomes higher due to prolonged operation. Table 5.2 shows the difference in the forward current at a forward voltage of 1.2 V.

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(a)

(b)

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(c)

Figure 5.5 Forward I-V characteristics of the PSOI and SOI lateral power diodes computed using the E, E-T and E-T-S models

Table 5.2 Current density of lateral power diodes at forward bias 1.2V

$V_f @ 1.2V$	E Model	E-T model	E-T-S model
SOI I_f (A/μm)	1.60×10^{-3}	1.30×10^{-3}	1.28×10^{-3}
SOI Diode Power dissipation (W)	0.960	0.780	0.768
Partial SOI I_f (A/μm)	1.25×10^{-3}	1.09×10^{-3}	1.03×10^{-3}
PSOI Diode Power dissipation (W)	0.750	0.654	0.618

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From the above comparison, one can see that if the power diode is operating at a constant forward current, the forward voltage drop of the diode will be higher than the estimation from the E model. This means that the actual power dissipation in the diode given as $I_F \cdot V_F$ will be higher, and the rating of the heat sink design based on the E model will be under-estimated. On the other hand, the error introduced by the E-T model is not significantly as compared to the E-T-S model, and hence the accuracy of E-T coupled-field simulation is acceptable.

2. Comparison of SOI and PSOI diodes

Examining the E-T-S results of the forward characteristics of SOI and PSOI diodes shown in Figure 5.5(c) as reproduced from Figure 5.5(a) and (b), we can see that the PSOI diode gives a smaller current at a given V_F . Table 5.2 lists the forward current with forward bias at 1.2V for SOI and PSOI lateral power diodes. Again, if the power diode is operating at a constant forward current, the power dissipation of PSOI will be higher than SOI diode.

The smaller current at a given V_F for PSOI diode is believed to be due to the reduction in the injection efficiency and device temperature in the PSOI diode as elaborated in the following.

In a PSOI diode, there is a parasitic PNP transistor under the silicon window. The lightly doped N- region is acting as its base, P+ as the emitter and the P- substrate as its collector. Figure 5.6 shows the computed electric potential distribution of the partial SOI diode which spread out from the SOI work layer into the substrate. Thus, during on-state operation of the lateral PiN diode, the potential distribution can turn on the parasitic PNP transistor which diverts some on-state current into the substrate.

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Higher current diversion will occur when higher forward bias is applied since the parasitic PNP will be biased at deeper conduction mode.

(a)

(b)

Figure 5.6 Electric potential in PSOI and SOI power rectifiers under forward biasing condition

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Figure 5.7 Substrate currents change with anode forward bias in partial SOI later power diode.

As a result, the forward current through the PiN diode is reduced for a given forward bias as compared to its SOI counterpart. In order to eliminate the substrate current in parasitic PNP transistor, a buried N+ layer at partial SOI silicon window is chosen. Figure 5.7 shows the substrate current changed with anode bias for structure with buried N+ layer is more than one order smaller than the structure without the buried N+ layer. With the buried N+ layer, I_{sub} diverted by the parasitic PNP transistor reduces from 7.5% of the diode anode current to 0.4% in partial SOI lateral power diode.

Figure.5.8 shows the temperature distributions inside the PSOI lateral PiN and that of SOI under the same forward bias condition. In the PSOI lateral PiN with the silicon window under the cathode, the highest temperature zone of 460K is spread out

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from the junction region and decreases towards the cathode and substrate as can be seen in Figure 5.8. This is because the silicon window provides a good thermal conductive path to the bottom Si substrate. In comparison, the SOI diode has a more uniform temperature distribution in the work layer due to the thermal isolation of the buried oxide, but the temperature in the SOI diode is much higher than its partial SOI counterpart at the junctions and in the drift region with the highest temperature of the diode reaches to about 516K for SOI diode. It is the reduction in the device temperature in PSOI diode that causes a right shift in the forward I-V curve as commonly known [47].

On the other hand, the non-uniform temperature distribution in the PSOI diode induces a thermo-mechanical stress in the device. The stress distributions in both the SOI and PSOI diodes are shown in Figure 5.9. As expected, the maximum stress in the PSOI diode is much higher than that in SOI diode due to the higher non-uniformity of the temperature distribution in the device. The higher stresses in PSOI diode are mainly located at the interface and the corner regions of the diode as shown in Figure 5.9, and hence they affect the lateral PiN electrical performance slightly. However, reliability of the diode is expected to be affected by the presence of the thermo-mechanical stress, especially at the bonded interface which could result in the delamination or crack along the interface.

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(a)

(b)

Figure 5.8 Temperature distribution at forward biasing condition in PSOI and SOI power rectifiers. The x-axis and y-axis units are μm . z-axis units is K.

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(a)

(b)

Figure 5.9 Thermal-induced stress distribution at forward biasing condition in PSOI and SOI. The x-axis and y-axis units are μm .

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For full SOI structure, the stress fields of both interfacial and surface stresses are almost uniform as can be seen in Figure 5.9. The stress is about 400MPa at the interface and surface of work layers.

5.1.3.2 Reverse Electrical Characteristics

1. Comparison of the models

The reverse bias voltage between cathode and anode is usually high for power diodes. Figure 5.10 shows the current-voltage curves of lateral power diode with E, E-T, and E-T-S model in the partial SOI and SOI structure. One can see that the leakage current for both the PSOI and SOI diodes increases in the E-T-S model simulation. The reason is that the stress-induced bandgap narrowing increases the concentration of the generated carriers within the depletion region near the area of compressive stress. Table 5.3 lists the leakage current at 80% of the reverse breakdown voltage. Comparing the leakage current in simulation results with and without stress effect, stress-induced bandgap narrowing causes the leakage current to increase by a factor of about two in both PSOI and SOI diodes.

This two times increase in the reverse leakage current represents the minimum effect of the stress on the reverse leakage current. In the presence of imperfection and defects in actual devices, the effect of stress on leakage current will be much more severe. This is because the SRH generation and recombination rates will increase with the reduction of the bandgap due to stress. Also, the presence of stress/strain is often the source of material degradation and its reliability issue [121], and the computation of the stress/strain is a first step for the reliability modeling of the semiconductor devices.

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Figure 5.10 Reverse I-V characteristics of the PSOI and SOI lateral power diodes computed using the E, E-T and E-T-S models.

This increase in the leakage current increases the power dissipation of the diode. Ideally, the leakage current should be zero and hence no power dissipation occurs in the diode when it is off (or reverse bias). With a high reverse voltage, even a small leakage current can cause a significant power dissipation.

Table 5.3 Leakage current density of lateral power diode at reverse bias 80% BV

$V_r @ 0.8 \cdot BV$	E Model	E-T model	E-T-S model
SOI $I_{leakage}$ (A/ μm)	1.55×10^{-12}	1.63×10^{-12}	2.56×10^{-12}
Partial SOI $I_{leakage}$ (A/ μm)	4.13×10^{-12}	5.03×10^{-12}	1.18×10^{-11}

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Also, the higher reverse leakage current of a diode will affect its circuit performance. For example, if the diode is used as an input rectifying circuit, higher leakage current will increase the output voltage ripple since it increases the rate of capacitor discharge. A common practice to face with non-zero reverse leakage current is to use the concept of Peak-Inverse-Voltage (PIV). Circuit design will specify the PIV of a diode requirement where PIV is a reverse voltage such that the leakage current is at a specified value and its effect on circuit performance is minimized. If the PIV is estimated using the E model, then the actual PIV will be much smaller since the actual leakage current is 2 times higher than that predicted by the E model, and the diode thus fabricated based on the E modeling will be found unsuitable for its intended circuit applications.

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(a)

(b)

Figure 5.11 Electric potential in (a) PSOI and (b) SOI power diodes at reverse biasing condition

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2. Comparison of SOI and PSOI diodes

The electrical potential distributions in the work layer for both the SOI and PSOI diodes are shown in Figure 5.11. Unlike in SOI power diodes where the potential lines are crowded in the top SOI layer, the substrate plays an active role in reducing the electric field at the surface in the PSOI structure. Thus the PSOI structure realizes an improved RESURF effect with effectively balanced two-dimensional distribution of the electric field at the silicon surface layer. As a result, PSOI diodes possess higher breakdown voltage of 287V than that of 203V in SOI diode with identical device and structural parameters.

While the breakdown voltage of the PSOI diode is higher, its leakage current is also higher. This is because of the parasitic PNP transistor in the PSOI structure as mentioned earlier in the forward characteristic discussion. With the more severe thermo-mechanical stress in the PSOI diode due to the larger non-uniform temperature in the work layer, the leakage current is even higher.

Figure 5.12 shows the temperature distributions inside the PSOI and conventional SOI lateral power diode at their respective breakdown voltages. In the PSOI power diode with the silicon window under the cathode, the highest temperature of 355K is found in the junction region and the temperature decreases towards substrate (306 K) as shown in Figure 10. On the other hand, as expected, SOI has a higher but more uniform temperature distribution (375 K) in the work layer due to the heat barrier provided by the buried oxide layer.

The non-uniform temperature in the PSOI diode produces a more severe thermo-mechanical stress distribution in the work layer as shown in Figure 5.13. Hence, more severe stress-induced bandgap narrowing occurs in PSOI which in turn causes a higher leakage current.

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Figure 5.12 Temperature distribution in (a) PSOI and (b) SOI power diodes at reverse biasing condition

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Figure 5.13 Stress distribution in (a) PSOI and (b) SOI power diodes at reverse biasing condition

5.2 Electrical-Thermal-Stress Coupled-field Effect in SOI and Partial SOI Lateral LDMOSFETs

5.2.1 Introduction

Smart power ICs which monolithically integrates low-loss power devices and control circuitry, have attracted much attention in a wide variety of applications [1,122]. Commonly used smart power devices are the lateral double diffused MOS transistors (LDMOSFETs) and lateral insulated gate bipolar transistors (LIGBTs) implemented in bulk silicon or SOI.

This study focuses on LDMOSFETS which is better suited for high frequency telecommunication applications [123]. The lateral surface effect device is, however, susceptible to hot carrier currents that induce several breakdown mechanisms. Certain features such as linearly graded doping profiles in the drift region and large series resistances have been proposed to mitigate these undesirable effects [124,125]. The concept using deep depletion (DD) for lateral SOI power devices has been also proposed [126]. These attempts represent a modest improvement in thermal management but the devices are still likely to exhibit thermal problems. It is for this reason that the thermal simulation of LDMOSFETS is crucial for accurate estimates of device performance.

On the other hand, one of the key issues in the realization of such ‘smart power’ technology is the isolation of power devices from the low-voltage circuitry. SOI technology constitutes an attractive alternative to the traditional junction isolation. However, the operation of SOI power devices is also limited by self-heating effects. To solve this problem, partial SOI technology was suggested, where a silicon window helps to reduce self-heating. In addition, potential lines spread into the substrate.

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Therefore it is possible to obtain higher breakdown voltages than those of conventional SOI devices. However, thermal-induced stress in PSOI LDMOSFETS emerges as an interest topic due to self-heating. To the best of our knowledge, it is the first time an E-T-S coupled field simulation is applied to LDMOSFETS. The steady state characteristics of LDMOSFETS are considered as a first attempt for the E-T-S model application.

5.2.2 Device structure and simulation of the fabrication process

The schematic cross section of the devices under study are shown in Figure 5.14. The buried oxide thickness, SOI thickness and the length of the n- drift region is crucial for the breakdown voltage of a conventional SOI power LDMOSFETS.

As an example, a conventional n-channel SOI LDMOSFET with an SOI thickness t_{SOI} of 8 μm and a buried oxide thickness t_{ox} of 0.5 μm has a maximum breakdown voltage (BV) of 32V if the light-doping n-drift region of the device is doped according to the RESURF principle. If t_{SOI} is increased to 12 μm while keeping other device parameters unchanged, the maximum BV is about 42V.

For a partial SOI LDMOSFET, a silicon window is placed under the drain as shown in Figs. 5.14(a). In this work, the t_{SOI} , t_{ox} , and SOI layer doping concentration of both the partial SOI and full SOI lateral power LDMOSFET are identical. The n-drift lengths L_{drift} in both types of LDMOSFETs are 4.5 μm which is adequate to withstand high breakdown voltage at work condition [5,33]. The values of the structure parameters are shown in Table 5.4 [117].

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Figure 5.14 The schematic cross sections of lateral power rectifier on (a)SOI and (b)partial SOI structure

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The device fabrication process is shown in Figure 5.15 which is compatible to the one used in industry. As the impurity profiles of the P+/N+ regions and n-drift region are important to the device's performance, the device fabrication process were simulated by Tsuprem4.

Figure 5.15 Process flow for the fabrication of the LDMOSFET.

Table 5.4 Device parameters used in this study

	PSOI	SOI
work layer thickness t_{soi} [μm]	8	8
buried oxide thickness t_{ox} [μm]	0.5	0.5
Open window length [μm]	3	0
Gate length	1	1
n-Drift length [μm]	4.5	4.5

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The LDMOSFETS fabrication process was developed based on the $0.35\mu\text{m}$ high voltage bulk silicon technology used in industry but incorporated certain modifications in thickness of the buried oxide layer and substrate wafer sheet resistance which improve the RESURF effect to achieve high breakdown voltage.

The doping profiles of the LDMOSFETs in PSOI and SOI are shown in Figure 5.16. The results are transferred to COMSOL for the E-T-S coupled field analysis.

Figure 5.16 Doping profile of lateral power diode in PSOI and SOI. The units of x-axis and y-axis is μm .

5.2.3 Results and Discussions

With the E-T, T-S and S-E models derived, we study the effect of stress and self-heating on the SOI and partial SOI lateral LDMOSFETs. Their thermal characteristics and stress effects will be compared at the same operating conditions.

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The comparison of the E only, E-T and E-T-S coupled-field simulation will also be made from the calculation to examine the performance of the E-T-S model.

5.2.3.1 Forward Electrical Characteristics

Figure 5.17 compares the current-voltage simulation results of SOI and PSOI LDMOSFETs using the three models. From Fig 5.17, two comparisons can be made as follows.

1. Comparison of the models

Looking at the LDMOSFET forward characteristics, one can see that the E-T-S model predicts a lower current at high drain voltage condition as compare to the other two models, but negligible difference for the three models when the drain voltage is low. The difference is larger when the gate voltage is high. This is due to the increasing severity of the self-heating at higher drain current which in turn causes a higher strain in the material. Therefore, the different of the E-T-S model with the other two models will to be even more if the operating temperature of the devices is higher after some prolonged operation. Table 5.5 shows the difference in the drain current at the gate voltage of 5 V.

Due to the reduced current predicted by the E-T-S model, the on-resistance of the LDMOSFETs under forward condition is larger than that predicted using the other two models. Table 5.5 compares the on-resistance $R_{on.sp}$ of E only, E-T model, and E-T-S model at the gate voltage of 5V. In the case of PSOI LDMOSFETS, the on-resistance of the device is increased about 7.1% when compared with those calculated by E and E-T model.

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(a)

(b)

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Figure 5.17 Forward I-V characteristics of the PSOI and SOI LDMOSFETs computed using the (a) E, (b) E-T and (c) E-T-S models

Table 5.5 Current density of LDMOSFETs at gate bias 5V

$V_{\text{gate}} @ 5\text{V}; V_{\text{drain}} @ 21\text{V}$	E Model	E-T model	E-T-S model
SOI I_{on} ($\mu\text{A}/\mu\text{m}$)	388	182	177
SOI on-Resistance $R_{\text{on-sp}}$ ($\text{m}\Omega \cdot \text{mm}^2$)	78.2	77.8	83.2
Partial SOI I_{f} ($\mu\text{A}/\mu\text{m}$)	349	222	213
PSOI on-Resistance $R_{\text{on-sp}}$ ($\text{m}\Omega \cdot \text{mm}^2$)	78.7	78.6	84.3

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2. Comparison of SOI and PSOI LDMOSFETs

For low gate voltages (3 V) the curves are similar to each other. Note that the two devices are expected to have similar $I_d - V_d$ curves for the same gate voltage. This is because the only difference between them is the buried oxide layer, which does not influence electrical performance obviously at low gate bias conditions. The simulated electric potential distribution at the partial SOI spreads out of the work layer into substrate as shown in Figure 5.18.

For E-T coupled model, however, with an increase in the gate voltage, self-heating effects become prominent and cause the lattice temperature to rise. Meanwhile, the buried oxide layer causes this heat to be trapped in the active region. In Figure 5.17 (a) and (b), the thermal effect is seen clearly for $V_g=5V$ where the behavior of the two devices diverge after $V_d=7 V$. The partial SOI device has a better heat conduction capability because the silicon window permits this heat to partially dissipate into the substrate region. The SOI device suffers from a higher heat confinement and thus exhibits the more divergent behavior.

The curve also undergoes transconductance at high gate voltage and high drain voltage, and therefore the drain current decreases with an increase in drain voltage. This is primarily due to a decrease in mobility as carrier velocities saturate. The rise in lattice temperature will be attributed to carrier velocity saturation, which induced by an increased rate of scattering between the carriers and the lattice. Perugupalli et al. (1998) [127] reported similar results based on the analysis of their devices.

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Figure 5.18 Electric potential in (a) PSOI and (b) SOI LDMSOFETs during conduction.

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Compared in Figure 5.17(c), the stress effect is not significant for LDMOSFETs in the partial SOI and SOI structure because the device's electrical performance is mainly determined by the channel region under the gate and n-drift region which is away from the high stress region of the interface around the oxide. Table 5.5 lists the forward current with gate bias at 5V and drain bias at 21V for conventional SOI and partial SOI lateral power LDMOSFETs. The effect of thermal-induced stress degrades the device performance by about 4% in the partial SOI structure and by about 3% in SOI structure due to mobilities degraded by compressive stress.

The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the LDMOSFETs [128]. As majority carrier devices, there is very little carrier recombination and as a result heat generation is mainly caused by Joule heating. This effect can be seen in partial SOI and SOI LDMOSFETs. It is proportional to the local resistances of the n-drift and channel region. Due to silicon window, the temperature in partial SOI LDMOSFETs reaches 457K which is much lower than that the 548K of SOI as shown in Figure 5.19. Also the highest temperature zone is spread out from the LDD region.

In the LDMOSFETs, the main stresses at surface are induced from LOCOS and buried oxide interface. Figure 5.20 shows the high compressive stress that is generated under the bird's peak of LOCOS. When the substrate wafer has been coupled to the work layer, the vertical direct tensile stress at the SiO₂ edge of the interface couples to the compressive work layer and forms another main stress region. The corner stress is minimal in the substrate due to the huge compressive stress effect at film-edge in the work layer induced by the temperature distribution.

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Figure 5.19 Temperature distribution at forward bias condition in (a) PSOI and (b) SOI LDMOSFETs.

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Figure 5.20 Thermal-induced stress distribution at forward biasing condition in (a) PSOI and (b) SOI LDMOSFETs

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5.2.3.2 Reverse Electrical Characteristics

1. Comparison of the models

Figure 5.21 shows the current-voltage curves of LDMOSFETs with E, E-T, and E-T-S model in partial SOI and SOI structure. One can see that the leakage current for both the PSOI and SOI LDMOSFETs increases under the E-T-S model. The reason is that the stress-induced bandgap narrowing produces a larger generation rate within the depletion region near the area of compressive stress. Table 5.6 lists the leakage current at 32V drain bias condition. Comparing the leakage current simulated with and without stress effect, stress-induced bandgap narrowing causes the leakage current to increase about one and a half times in both partial SOI and conventional SOI structure.

Figure 5.21 Reverse I-V characteristics of the PSOI and SOI LDMOSFETs computed using the E, E-T and E-T-S models

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Table 5.6 Leakage current density of LDMOSFETs at $V_{\text{drain}} 32\text{V}$

$V_g @ 0\text{V}$ and $V_d @ 32\text{V}$	E Model	E-T model	E-T-S model
SOI I_d (pA / μm)	0.81	0.81	1.46
Partial SOI I_f (pA / μm)	1.12	1.11	1.58

2. Comparison of SOI and PSOI LDMOSFETs

In the partial SOI with a silicon window under the drain, both the buried oxide and depletion region of substrate help to increase the breakdown voltage as shown in Figure 5.22, where the potential lines spread into substrate. The maximum breakdown voltage of this structure is 45V at substrate doping concentration $1 \times 10^{15} \text{cm}^{-3}$ and a length of drift region about $4.5 \mu\text{m}$. The improvement in the voltage handling capability is about 15% compared to the conventional 39V SOI LDMOSFET shown in Figure 5.21.

Figure 5.23 show the temperature distributions inside the partial SOI LDMOSFETs with a drain-source voltage V_{DS} of 21V. In the partial SOI LDMOSFETs, the temperature reaches the highest under the gate region at 313 K and decreases towards the drain at 307 K. Under the same operating condition, the temperature distribution of the conventional SOI device is more uniform than that of the partial SOI structure.

The stress distribution at work layer is indicated at Figure 5.24. The thermal-induced stress is not significant at the junction region and mainly located at the Si-SiO₂ interface. The stresses increase the leakage current of both partial SOI and SOI LDMOSFETs as shown by the I-V curves in Figure 5.21.

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Figure 5.22 Electric potential in (a) PSOI and (b) SOI LDMOSFETs under reverse bias.

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Figure 5.23 Temperature distribution in (a) PSOI and (b) SOI LDMOSFETs under reverse bias.

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Figure 5.24 Stress distribution in (a) PSOI and (b) SOI LDMOSFETs at reverse biasing condition

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5.3 Summary

A coupled electrical-thermal-stress (E-T-S) model has been developed in this work, taking into account the stress-induced modification of the Si band structure. This model is applied to the study of SOI and PSOI lateral power diodes as well as LDMOSFETs, and their static I-V characteristics as well as the temperature and thermo-mechanical stress distributions in the diodes are computed using E only, E-T and E-T-S models. From the comparison of the computational results using the three models, it is found that the error introduced by the E-T model is not significant as compared to the E-T-S model, and hence the accuracy of E-T coupled-field simulation is acceptable. Comparing the leakage current in the simulation between with and without stress effect, the stress-induced bandgap narrowing causes the leakage current to increase. With a high reverse voltage, even a small leakage current can cause a significant power dissipation.

PSOI has higher breakdown voltage, and lower device temperature. But it also has larger reverse current, higher thermo-mechanical stress that can lead to reliability issues.

Comparing the electrical characteristics of SOI and PSOI power diodes as well as LDMOSFETs using the E-T-S model, we observed that PSOI possesses higher reverse breakdown voltage due to its better RESURF as well as lower device temperature. The observed electrical characteristics can be explained from the electrical potential distribution, temperature and thermo-mechanical stress distributions in the devices.

Chapter 6 CONCLUSION AND FUTURE WORK

6.1 Conclusions

In the present study, finite element models were built to study the distribution of thermal-induced stresses in partial SOI structures. It is found that the stress distribution at the work layer/substrate interface is more non-uniform than that at the surface since stress concentration is expected at the oxide edge and corner. Maximum stresses at both the surface and the interface are dependent on structural parameters, including oxide length (and width), oxide thickness, substrate thickness and work layer thickness.

In order to assist device designers to take into account of the stress distribution in a partial SOI structure effectively, empirical stress model as a function of the various structural parameters were built using the response surface method (RSM). These statistical models were applied to optimize the structural parameters.

The requirement of E-T-S coupled-field modeling of semiconductor devices demands the use of finite element analysis for device simulation. A coupled electrical-thermal-stress coupled-field simulation is developed in this work, taking into consideration of the stress-induced modification of the Si band structure. Comparison of the results from COMSOL and Medici as well as COMSOL with ANSYS shows good agreement. Meanwhile, the stress effects are computed using the deformation

potential theory and we have demonstrated that the electron and hole mobilities of (010) biaxial stressed power diode are changed due to band energy splitting. The strain-induced changes of bandgap and effective mobilities cause the static drive current to reduce by about 5%, but their effect on diode transient characteristics seems to be insignificant.

E-T-S coupled field model is applied to the study of SOI and PSOI lateral power diodes as well as LDMOSFETs, and their static I-V characteristics as well as the temperature and thermo-mechanical stress distributions are computed using E only, E-T and E-T-S models. From the comparison of the computational results using the three models, it is found that the error introduced by the E-T model is not significantly as compared to the E-T-S model, and hence the accuracy of E-T coupled-field simulation is acceptable. Comparing the leakage current in simulation results with and without stress effect, stress-induced bandgap narrowing causes the leakage current to increase. With a high reverse voltage, even a small leakage current can cause a significant power dissipation.

Comparing the electrical characteristics of SOI and PSOI power devices using the E-T-S model, we observed that PSOI possesses higher reverse breakdown voltage due to its better RESURF and lower device temperature. The observed electrical characteristics can be explained from the electrical potential distribution, temperature and thermo-mechanical stress distributions in the devices.

6.2 Future Work

In this thesis we have developed and laid the groundwork on PSOI structure and E-T-S coupled field effects, both on technologies and mechanisms. However, it is by no means exhaustive, and more work still need to be further studied.

6.2.1 Modeling of STI Process

In the present study, E-T-S coupled field model is mainly focused to analyze the power devices which are isolated by LOCOS. However, STI technologies are rapidly becoming the standard isolation process in modern integrated circuits as minimum transistor channel lengths decrease below 0.25-micron. This scaling leads to an increase in the importance of isolation effects on device characteristics such as electric fields and leakage currents.

The main obstacle encountered in modeling of the STI process is a moving boundary grid handling problem. STI processes include multiple etch and depositions. These processes as well as the material growth processes encounter occasional problems for handling the grid as the boundary front advances. Developments for handling these problems are being made which result in an increasingly robust grid handling in two-dimensions [129]. It is recommended to analyze the STI in E-T-S coupled-field simulation for the further study.

6.2.2 New Method to Fabricate of PSOI structure

6.2.2.1 Introduction

Wafer bonding methods are investigated in our group. Although wafer bonding is by no means a new technique, recently it has been gaining popular interest for a number of microprocessing applications, such as, high performance microelectronics, photonics and optoelectronics, and MEMS. The power of wafer bonding to create layers of high quality, crystalline materials without regard to their microstructure, orientation and lattice constant means that it can open up new directions of research into design of all of these kinds of devices. Additionally, the capability of layering dissimilar materials makes it possible to integrate devices on a single chip that until now have been incompatible. Medium Vacuum Wafer Bonding can be used in MEMS for wafer level packaging, such as hermetic sealing. But among all the applications of wafer bonding, SOI has certainly provided the biggest impetus to it. Therefore, in this section, fabrication of SOI is focused, which includes fabrication of full and partial SOI structures.

6.2.2.2 New Method to Fabricate of Partial SOI: Low temperature wafer bonding

The process flow of fabrication of partial SOI is shown in Figure 6.1, which includes 4 main steps, i.e., fabrication of patterned oxide wafer, polishing of patterned oxide wafer, MVWB and polishing or Smart Cut TM to obtain the appropriate thickness of device wafer. Among them, the first two critical steps will be discussed below.

Figure 6.1 Schematic of the process flow to fabricate partial SOI

1. Fabrication of Patterned Oxide Wafer

The patterned wafers are fabricated at Micro-fabrication Lab (MFL), NTU. The fabrication processes of patterned substrate wafers are as same as the field oxide processes. They are shown in following Figure 6.2.

Step 1: Pad Oxide

Pad oxide is used to prevent structural stress between the nitride and the substrate. Since a very thin layer is required, dry oxidation is used.

Step 2: Nitride Deposition

This is used to prevent unwanted areas from being exposed to the oxide. Nitride deposition is done using LPCVD. A temperature ramp of 785-790-800C in the LPCVD nitride furnace from the entrance end to the rear end of the processing tube was adopted to keep the rate of deposition more or less constant.

Step 3: Active Mask for Patterned Oxide

Define the area of the patterned oxide. The mask used is clear field, where the other area will be protected by the photoresist.

Figure 6.2 Schematic of fabrication of patterned oxide wafer

Step 4: Nitride Etch

Plasma etching is used to etch away the Silicon Nitride deposited. This is for the growing of patterned oxide. Plasma nitride etch was used for this etching process to ensure an anisotropy profile. Over etching was done to ensure complete etching.

Step 5: Photoresist Strip

Dry ashing and wet and wet cleaning were used to strip off the photoresist.

Step 6: Field Oxide

Wet oxidation is used to create the patterned oxide, which form the partial oxide at substrate wafer in PSOI structure. Immediately after this step, the wafer is annealed in N₂ to release oxide-trapped charges and decrease the number of fixed charges on the oxide. The temperature of wet oxide is 950°C.

Step 7: Nitride Strip

The nitride and pad oxide layer used in the previous steps are to be removed in this step. Before performing this step, the wafers were dipped in BOE to remove oxynitride that was formed on top of the nitride. If this is not done, the oxynitride can prevent phosphoric acid from reaching the nitride. The fabricated patterned substrate wafers was prepared for wafer bonding process. The wafers are fabricated at Microfabrication Lab in NTU. The oxide thickness is about 0.885µm.

2. Polishing of the Patterned Oxide Wafer

In order to measure the surface of patterned substrate wafer, the surface roughness tests were performed using STYLUS PROFILOMETER Taylor-Hobson. The result is shown at Figure 6.3. Thus, the partial oxide thickness above the substrate

wafer is about 0.44 μm and further polishing is needed to obtain flat surface required by next step, wafer bonding.

Both pure mechanical polishing and chemical-mechanical-polishing (CMP) can achieve a high degree of flatness, parallelism and smoothness of Si and oxide wafers. Regarding pure mechanical polishing, it does introduce a significant subsurface damage layer of $\sim 20\text{ }\mu\text{m}$ in depth [69], but in fabrication of partial SOI by wafer bonding, the damaged layer is on the substrate wafer and won't degrade the performance of the device on this structure. Thus, pure mechanical polishing is applicable of polishing of the patterned oxide wafer. The study on this is still in process in our group.

Figure 6.3 Surface analysis of the fabricated partial oxide wafer by stylus profilometer. The units of y-axis is μm .

Therefore, it looks like that the polishing of the partial oxide wafer to obtain the surface for wafer bonding is not an obstacle for the fabrication of partial SOI by wafer bonding.

6.2.2.3 New method to Fabricate Partial SOI: Hybrid of SIMOX and Wafer Bonding

Figure 6.4 The schematic of HSW

Another method to fabricate partial SOI that combines the advantages of SIMOX and wafer bonding is shown in Figure 6.4, named hybrid of SIMOX and Wafer Bonding (HSW). To our knowledge, our group is the first to propose this method. When the conventional SIMOX is used for fabricating the partial SOI structure, high-energy implantation will be needed (especially for the fabrication of power device). However, such high-energy implantation will induce severe damage to the active wafer. In our method, we need only low energy implantation because the thickness of the silicon layer over the oxide layer could be very thin and the device

layer with high quality can be bonded on the handle wafer. Therefore, HSW can obtain partial SOI without damage in the device layer, and the process is also simple.

Fabrication methods of partial SOI, as shown in Figures 6.1 and 6.4, were proposed, but experiments cannot be performed due to the lack of equipments.

The crucial step of the fabrication method shown in Figure 6.1 is the polishing of the surface of patterned oxide wafer. Pure mechanical polishing and CMP with special slurry should be tried in the future for our group.

The fabrication method shown in Figure 6.4, hybrid of SIMOX and wafer bonding also deserve for further study.

6.2.3 High power LEDs E-T-S coupled-field simulation

LED stands for Light-Emitting Diode, which works with the effect of electroluminescence and discovered at an accident in 1907 [130]. The first practical visible-spectrum (red) LED was developed in 1962 by Nick Holonyak Jr., while working at General Electric Company. Holonyak is seen as the "father of the light-emitting diode" [131,132]. M. G. Craford, a former graduate student of Holonyak, invented the first yellow LED and improved the brightness of red and red-orange LEDs by a factor of ten in 1972. In 1976, T.P. Pearsall created the first high-brightness, high efficiency LEDs for optical fiber telecommunications by inventing new semiconductor materials specifically adapted to optical fiber transmission wavelengths [133].

The first high-brightness blue LED was demonstrated by Shuji Nakamura of Nichia Corporation and was based on InGaN. The existence of blue LEDs and high efficiency LEDs quickly led to the development of the first white LED, which

employed a $\text{Y}_3\text{Al}_5\text{O}_{12}:\text{Ce}$, or "YAG", phosphor coating to mix yellow (down-converted) light with blue to produce light that appears white.

Over the past forty years this compound semiconductor-based light source has evolved to become a bright, efficient source of white, red, green and blue light that is giving cars, interior lighting and signage a radical new look. The development of LED technology has caused their efficiency and light output to increase exponentially, with a doubling occurring about every 36 months since the 1960s, in a way similar to Moore's law. The advances are generally attributed to the parallel development of other semiconductor technologies and advances in optics and material science. This trend is normally called Haitz's Law after Dr. Roland Haitz [134].

Figure 6.5 Architecture of white light LEDs [135]

LED consists of a chip of semiconducting material doped with impurities to create a p-n junction. Quantum wells are inserted in between the p and n doped material and the wavelength of the light emitted [135], and therefore its color, depends on the band gap energy of the materials forming the p-n junction. Architecture of white light LEDs is shown at Figure 6.5.

Compared with normal incandescent bulbs, LEDs are preferred due to its following advantages. 1) Efficiency: LEDs produce more light per watt than incandescent bulbs. 2) Lifetime: LEDs can have a relatively long useful life. One report estimates 35,000 to 50,000 hours of useful life, though time to complete failure may be longer. Fluorescent tubes typically are rated at about 10,000 to 15,000 hours, depending partly on the conditions of use, and incandescent light bulbs at 1,000–2,000 hours. 3) Size: LEDs can be very small (smaller than 2 mm²) and are easily populated onto printed circuit boards.

However, heat and current settings can extend or shorten LEDs lifetime significantly. The most common symptom of LED (and diode laser) failure is the gradual lowering of light output and loss of efficiency. Sudden failures, although rare, can occur as well. Early red LEDs were notable for their short lifetime.

With the development of high power LEDs (HPLEDs) the devices are subjected to higher junction temperatures and higher current densities than traditional devices. This causes stress on the material and may cause early light output degradation. At the current levels needed for general lighting, “droop” kicks in, and the light delivers below 100 lm/W [135].

Figure 6.6 Band diagram of conventional GaInN/GaN active region and new polarization-matched GaInN/GaN active region of LEDs [104].

The droop is a phenomena that blue LEDs lost its efficiency at high power when its current is cranked up. It threatens the future of the electric lighting industry.

The cause of this droop is not yet fully understood. Krames' team [136] used a laser to probe a layer of GaInN, the semiconductor used for quantum wells in the nitride LED. The results of photoluminescence against different intensities impinging

on the sample show closely fit the equation that described the effects of Auger recombination [136]. However, Hader' team [137] proved the Auger recombination may not be the roots of droop by simulation. Meanwhile, a group headed by Schubert blames droop on the leakage of too many electrons from the quantum well. By carefully selecting the materials for the active region, switching from the conventional gallium nitride barrier to an aluminum gallium indium nitride version as shown in Figure 6.6, they say such "polarization matching" consistently cuts droop, raising power output by 25 percent at high currents[138,139]. While Schubert's theory of electron leakage could explain the results, there may well be other things that can also account for them [135].

To make an LED, you must grow a series of highly defined semiconductor layers on a thin wafer of a crystalline material, called a substrate. Unlike the GaAs LEDs, blue LEDs lack such a good platform since it has proved impossible to grow the large, perfect crystals of gallium nitride substrate. So the makers of blue LEDs typically build their devices on wafers of sapphire, whose crystalline structure does not quite match that of the nitrides, and that discrepancy gives rise to many defects.

At high current work condition, HPLEDs sandwich structure suffers high temperature and thus large thermal-induced stress, and defects movement and density increases may have occurred which could be a possible reason for the droop phenomena. The E-T-S coupled-field simulation will provide a promising approach to look into these defect behavior in HPLEDs. It is recommended for further study.

Publication List

1. Guangyu Huang, Cher Ming Tan, “Electrical-Thermal-Stress Coupled-field Effect in SOI and Partial SOI LDMOSFETs,” submitted to IEEE Transaction on Power Electronics.
2. Guangyu Huang, Cher Ming Tan, “Electrical-Thermal-Stress Coupled-field Effect in SOI and Partial SOI Lateral Power Diode,” IEEE Transaction on Power Electronics (in press).
3. Guangyu Huang, Cher Ming Tan, “Reverse Breakdown Voltage Measurement for Power P+NN+ Rectifier,” Journal of Electronic Testing: Theory and Applications, 24, pp. 473-479, 2008.
4. Guangyu Huang, Cher Ming Tan, “Device Level Electrical-Thermal-Stress Coupled-Field Modeling,” Microelectronics Reliability, 46, pp. 1823–1827, 2006.
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6. Guangyu Huang, Cher Ming Tan, “Device Temperature and Stress Distributions in Power Diode- A Finite Element Method,” International Conference on Power Electronics and Drive Systems (PEDS), IEEE, pp. 700-703, 2005.
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Coauthored publications in the period of study as a candidate of PhD:

8. Cher Ming Tan, Lina Sun; Raghavan, N., Guangyu Huang; Chuck Hsu, Chase Wang, “The Physical Limit and Manufacturability of Power Diode with Carrier Lifetime Control,” Conference on Industrial Electronics and Applications (ICIEA), IEEE, pp. 46-51, 2007.
9. Weibo Yu, Cher Ming Tan, Jun Wei, Shusheng Deng, Guangyu Huang, “Mathematical model of low temperature wafer bonding under medium vacuum and its application,” IEEE Transactions on Advanced Packaging, V28, 4, pp. 650–658, 2005.
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13. Tan C M, Wong Y.F., Teoh P.H, Huang, G.Y., “Improving the reverse blocking capability of carrier stored trench-gate bipolar transistor,” Power Electronics and Drive Systems (PEDS), IEEE, pp. 89-92, 2003.

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