Design of wideband CMOS low-noise amplifiers for ultra-wideband receivers

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Design of Wideband CMOS Low-Noise Amplifiers for Ultra-Wideband Receivers

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A thesis submitted to the
Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

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STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

Lu Yang

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ABSTRACT

The ultra-wideband (UWB) wireless transmission system is drawing tremendous attention from both the industry and the academia because of its unique potential to supply the gap for short-range high-speed wireless data communication. The WiMedia Alliance's Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) proposal finished its standardization with the European Computer Manufacturers Association International (Ecma International) and has virtually become the industry standard for the UWB wireless transmission systems. The ultra-wideband low-noise amplifier (LNA), which is the first building block in an integrated UWB receiver, is of significant importance to the performance of the whole receiver chain. By reviewing the worldwide UWB regulations and the WiMedia Alliance's MB-OFDM UWB standard, it is well understood that the ultra wide bandwidth required for the UWB low-noise amplifier calls for a different set of target specifications and trade-offs comparing with conventional narrow-band LNAs. Thus, novel circuit architectures need to be investigated and established for UWB LNAs to achieve these specifications.

The objective of this research work is to design and implement the circuit architectures for the UWB LNAs that can achieve the target specifications simultaneously. A cost effective 0.18- μm complementary metal-oxide-semiconductor (CMOS) process technology is adopted in the implementation of the proposed LNA designs to facilitate the integration with other building blocks on the same substrate for a low-cost fully-integrated UWB receiver. The source inductive degeneration architecture, which is classical for narrow-band LNA designs, is re-visited to investigate its capability to achieve wideband operation. The common-gate architecture, which is seldom

considered as an option for the input stage of LNAs, is also investigated regarding its capability of achieving low noise figure and sufficient gain over a wide bandwidth. The optimization techniques for matching bandwidth and noise figure have been developed in details for both architectures, which are important factors for the design of wideband LNAs. It is demonstrated through simulation and silicon-verification that both architectures are capable of achieving the target specifications for the UWB LNA.

The proposed UWB LNA design based on the cascoded source inductive degeneration architecture employs small source and gate inductors for matching bandwidth extension. The shunt inductive peaking and feedback techniques are adopted to further improve the gain and matching bandwidth. The fabricated design is measured to exhibit 6.0-GHz bandwidth from 2.0 to 8.0-GHz, a maximum gain of 17.5-dB and a minimum noise figure of only 1.8-dB over this bandwidth. The total current consumption is 4.8-mA, supplied by a 1.8-V DC voltage.

Another proposed UWB LNA design is based on the common-gate architecture, where two stages are cascaded to improve the overall gain and bandwidth. The staggering-tuning technique is adopted to peak the gain curve at two different frequencies, which substantially increases the bandwidth. According to the experimental results, the bandwidth of the fabricated design is 5.3-GHz, covering from 4.0 to 9.3-GHz. The maximum gain in this bandwidth is 19.8-dB and the minimum noise figure is 3.2-dB. This proposed common-gate LNA draws totally 5.6-mA current from a 1.8-V DC supply.

To further extend the bandwidth of the LNA to full UWB bandwidth, a three-stage staggering-tuning common-gate LNA is proposed. According the post-layout simulation, this design is capable of covering the 3.1 to 10.6-GHz UWB bandwidth. Variable gain mechanism with minimum influence to other critical specifications is introduced. At the 20.0-dB gain step, the minimum in-band noise figure is 3.5-dB and the current consumption is 8.0-mA from a 1.8-V DC supply.

The DC biasing generation circuits as well as the electro-static discharge (ESD) protection circuits for input and output (I/O) pads are designed and fabricated as the supplementary to complete all the building blocks for the full LNA circuits. Both circuits are designed based on the same CMOS process that all the proposed LNAs are designed.

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CHAPTER 1 Introduction

1.1 Background and Motivation

The ultra-wideband (UWB) system operation within the 3.1-10.6-GHz spectrum was approved in the United States in February 2002 by the Federal Communications Commission (FCC) [1]; similar approvals have been announced in the world's major wireless market regions in the years thereafter, such as Japan, Korea, the European Union (EU) and China [2][3][4][5]. As the UWB signal occupies very wide frequency spectrum, the UWB transmission system is an excellent candidate for establishing a high-data-rate short-range wireless connection.

Figure 1.1 High Speed Data Links Based on UWB Transmission Systems

As shown in Figure 1.1, such high speed wireless connection is highly appreciated in the computer and consumer electronics market since it can provide fast data links between computers and their peripherals, personal digital assistant (PDA), mobile

phones and even multimedia entertainment devices for the transmission of large data packages in a short time. On the other hand, the emission power spectral density of the UWB signal is strictly dictated to be below a low spectral mask (typically -41.3-dBm/MHz) so as not to interfere with the other incumbent wireless systems. This opens a window for the implementation of a short-range, high-data-rate yet low-power UWB wireless transmission system [6].

The ever-continuing scaling and developing of integrated circuit (IC) process technology has enabled the implementation of various complex signal processing circuits on a single small die. The CMOS process technology, which finds vast applications in implementation of digital circuits due to its intrinsic excellent on-off characteristic, has gradually become a decent candidate for radio-frequency (RF) circuit implementation resulting from the substantial increase of transit frequency as well as the introduction of good quality on-chip passive components through process scaling and development [7][8]. Consequently, the implementation of RF front-end circuits on CMOS process technology and the integration of those RF circuits with low-frequency analog and digital circuits on a single die are now viable. This system level integration, together with the low-price wafers as well as the relatively low mask count, paves the way for achieving a low-cost fully-integrated solution using CMOS process technology.

The transmitters and receivers for the short-range high-data-rate UWB wireless system are suitable to be fully integrated on CMOS technology since the required transmission power is low on the transmitter side and the requirement for the noise figure is not as stringent as on some other receivers for long-distance wireless systems,

such as the Global Positioning System (GPS). Moreover, the relatively low cost of the modern CMOS technology ensures that the UWB transceivers designed and integrated on a single CMOS silicon die will achieve the low-cost target. The complete integration of the UWB transceiver on CMOS technology will reduce the overall power consumption of the complete transmitting-receiving system. The physical dimension of the complete system solution will be small due to compactness achieved by full integration. All the features of the fully-integrated UWB transceiver fits in very well with the market requirement of the computer and consumer electronics. Consequently, it is highly desirable to implement the integration of a UWB transceiver on a single die based on a low-cost CMOS process technology.

The low-noise amplifier is normally the first functional block implemented on-chip in the wireless receiver chain. The LNA amplifies the radio frequency (RF) signal received by the antenna (and sometimes filtered by a front-end RF filter) and feeds the amplified RF signal to the next functional block of the receiver chain, which is normally a mixer that down-converts the RF signal to some intermediate frequency (IF) or base-band (BB) directly. The amplification of the received RF signal by the LNA enlarges the signal's amplitude so that it is less vulnerable to the noise of the following blocks in the receiver chain. Meanwhile, the LNA should exhibit a low noise figure so that the signal-to-noise ratio (SNR) of the RF signal does not degrade much by the low-noise amplifier stage itself.

The design of a UWB LNA on CMOS process technology confronts serious challenges both from the UWB standard requirement and the process technology capability.

Unlike most of the preceding wireless communication system standards, the UWB system occupies tremendous frequency spectrum, over which the UWB transmission signal resides. For example, the spectrum licensed for UWB application in the US covers 7500-MHz bandwidth from 3.1 to 10.6-GHz [1]. Although the regulatory bodies in other regions tend to allocate the UWB spectrum in dual-band format and the upper operation frequency limit is sometimes reduced to 9.0-GHz (in the EU and China [3][5]), the bandwidth of the UWB system is still no less than 3-GHz. The LNA in the UWB receiver needs to amplify the large-bandwidth UWB signal with minimum gain ripple in the system bandwidth; meanwhile, the LNA should also provide 50-Ohm termination to the antenna or bandpass filter that precedes it in the receiver over the same wide bandwidth. The demand for large matching and gain bandwidth invalidates the conventional design technique for narrowband on-chip LNAs [9][10][11]; new design methodology needs to be developed to achieve the large matching and gain bandwidth simultaneously.

The active devices in CMOS technology employed in RF circuits, namely the RF NMOS and PMOS, generally exhibit lower transit frequency and higher noise figure comparing with their bipolar counterparts. The lack of high quality on-wafer passive components adds to the design difficulties. This is especially true for the integrated spiral-shaped inductors made from the top metal layers, which exhibits a typical quality factor of no more than 10 in conventional CMOS process technologies. Furthermore, due to the significant parasitic capacitance to the lossy silicon substrate, the on-wafer inductors exhibit low self-resonant frequency. Consequently, the inductance and quality factor of an on-wafer inductor vary significantly within the

UWB operation frequencies, bringing about additional design challenges for the LNA circuits, most of which employs on-wafer inductors in their input matching and load networks. The parasitic capacitances and the lossy substrate of the CMOS process technology also induce impedance shift and power loss in the critical signal paths.

To sum up, it is highly desirable to implement the UWB LNA based on CMOS process technology to pave the way for full integration of the UWB receiver and the many technical challenges for the implementation of CMOS UWB LNA require many endeavors.

1.2 Objectives

The goal of this research work is to develop a methodology to design and implement an ultra-wideband low-noise amplifier on GLOBALFOUNDRIES 0.18- μm 1P6M RF CMOS process, which is a conventional low-cost CMOS process on the 0.18- μm technology node. The wideband input matching architectures are to be investigated to achieve high quality 50-Ohm termination at the LNA input port. The noise figure, which directly relates to the input matching architectures, is to be studied and the optimization techniques for different architectures are to be proposed. The techniques for increasing the gain bandwidth of the LNA are to be established so that a large portion of the UWB frequency spectrum can be covered. Other important performance parameters of the LNA circuit, such as its linearity and stability, will also be investigated to make sure that the LNA will meet all the requirements of the UWB system. The LNA circuits implemented based on the proposed design methodologies will be fabricated and characterized, so as to verify the methodology on silicon.

1.3 Organization of the Thesis

The thesis is organized into eight chapters.

Chapter 1 introduces the background of the problem to be solved, the targeting goal for the solution as well as the outline of the thesis.

In Chapter 2, worldwide ultra-wide band regulations and standards are reviewed and compared. The WiMedia Alliance's UWB physical layer (PHY) and media access control (MAC) standards, which are published at Ecma International, will be studied as they are directly related to the specification requirements for the UWB receiver and hence the LNA.

The key specifications for the LNA design will be discussed in Chapter 3. The conventional design methodologies for narrowband LNAs will also be re-visited in the same chapter. Based on the design technique for narrow-band LNAs, the techniques to extend the matching and gain bandwidth will be discussed, followed by a review of the state-of-art UWB LNA architectures.

Chapter 4 presents a design of the UWB LNA based on the conventional source inductive degeneration technique but with shunt feedback tapped from the common node of a differential inductor at the load to extend the matching and gain bandwidth.

In Chapter 5, a common-gate LNA design employing two-stage staggering-tuning technique is demonstrated. The staggering-tuning technique, which extends the gain bandwidth by peaking the gain at different frequencies in the interested bandwidth, will be discussed in detail.

Chapter 6 takes a step further based on the technique introduced in Chapter 5. It is demonstrated that by adding one more stage, the gain bandwidth can be further extended to cover the whole 3.1-10.6-GHz UWB band.

The design of the auxiliary circuits including the DC biasing generation circuits and the ESD protection circuits is described in Chapter 7.

Finally, Chapter 8 concludes the thesis with a summary of the results and the areas for further research work.

CHAPTER 2 Review of the Ultra-Wideband Regulations and Standards

To fully understand the specification requirements for the ultra-wideband wireless receiver and subsequently its low-noise amplifier, it is necessary to not only know the specifications explicitly stated in the regulations and standards but also comprehend those items that are implicitly indicated. The wireless communication regulation bodies of different countries and areas in the world have their respective rulings over the allocation of spectrum for UWB operation. Meanwhile, the UWB standards proposed by different supporter campaigns also have their respective features. In this chapter, the UWB regulations in the world's major wireless markets are briefly introduced, as well as the standardization process. The WiMedia Alliance's MB-OFDM standard, which is the virtual industrial standard, is investigated with the emphasis on its indications on the UWB receiver and LNA design.

2.1 UWB Regulations and Standardization

The wireless spectrums in various countries and areas around the world are managed by different regulatory organizations under their respective jurisdictions. For instance, in the United States, the spectrum jurisdiction is charged by the Federal Communications Commission (FCC) and the National Telecommunications and Information Administration (NTIA); the European Commission (EC) dictates the wireless spectrum in the European Union; in China, the Ministry of Industry and Information Technology (MIIT) formulates and develops the policies and regulations on use of the spectrum, and etc.

The standards announced and supported by those regulatory organizations for a certain application would directly impact the implementation of commercial products built for those standards. To implement a globally operable and inter-operable commercial device, all the technical requirements of the standards in different countries and areas need to be strictly followed and incorporated. For example, the operation frequency range of the device needs to exactly fit in the allocated spectrum of its operating location; the emission power of the signal needs to meet the specified spectrum mask; the mandatory modulation schemes should be supported and etc.

As has been observed in many cases, it is extremely difficult to achieve a worldwide common standard for a wireless system due to various reasons and even more barriers are faced when it comes to the case of the UWB system. First of all, since the existing spectrum allocations for different countries and areas are quite different from each other, the spectrum allocations for UWB operation could also be different due to the non-uniform considerations regarding the co-existence and protection between these systems. On the other hand, since the operation frequencies of many other incumbent wireless systems are in or near the UWB frequency range, the methods taken to mitigate the interference between the UWB and the incumbent wireless systems could be different. Furthermore, due to the same reason, different restrictions exist on whether to limit the use of UWB devices in door or not.

On 14 February 2002, the FCC adopted the ‘First Report and Order’ [1], which allows the marketing and operation of devices incorporating the UWB technology. This decision makes the United States the first country in the world to officially allow the

UWB operation. Different technical standards and restriction for three types of UWB operation are defined, namely

- a. Imaging System (including ground penetrating radars, wall/through-wall/medical imaging and surveillance devices)
- b. Vehicular Radar Systems, and
- c. Communications and Measurement Systems.

The significance of FCC's adoption does not only lie in the large spectrum approved for UWB operation, moreover, the approval of the coexistence of UWB signal with other incumbent wireless systems in the same spectrum is truly historical. To avoid the undue interference to the existing wireless systems from the UWB signals, the FCC defined certain emission power limitation together with the bandwidth for UWB system.

According to the FCC's ruling, the definition of a UWB signal is as follows:

- a. Signal bandwidth

A UWB signal's bandwidth is defined to be bounded by the frequencies where the power spectral density is 10-dB below the maximum spectrum power density (-10-dB bandwidth). A signal is a UWB signal only if:

- i) its -10-dB bandwidth is at least 20 percent of its center frequency f_C ,

$$\frac{f_H - f_L}{f_C} \geq 0.2, \quad (2.1)$$

$$\text{where } f_C = (f_H + f_L) / 2 \quad (2.2)$$

Or ii) its -10-dB bandwidth is at least 500-MHz.

$$f_H - f_L \geq 500\text{MHz} \quad (2.3)$$

b. Power emission limits

In the 3.1-10.6-GHz UWB operation band, the maximum average radiation power density is limited to -41.3-dBm/MHz in terms of Effective Isotropic Radiated Power (EIRP). This limit is directly in line with the FCC Part 15 rules, where all unintentional radiators are allowed to emit a maximum power spectral density of -41.3-dBm/MHz in this band. The radiation power spectral density out of the UWB operation band is also defined by FCC, with differentiation between indoor and outdoor applications. Figure 2.1 shows the UWB signal power spectral density limits defined by FCC and this power spectral mask must be satisfied when measured with a 1-ms integrated time.

Figure 2.1 UWB Signal Power Spectral Density Defined by the FCC

As can be seen from Figure 2.1, the out-of-band emission level is suppressed in the 960-MHz to 3.1-GHz band to minimize the possible interference to the incumbent wireless systems, such as the GSM, WiMAX and WLAN systems. The allowed emission level is lowest in the GPS bands as the GPS signal is very weak after traveling a long way from the satellites to the earth. Beside the average power spectral density specification, a limit of 0-dBm in a 50-MHz bandwidth is also defined as peak power level limit by the FCC.

Frequency hopping operation mode is allowed for the UWB devices according to the FCC rules in the 3.1-5.03-GHz and 5.65-10.6-GHz, leaving the gap between 5.03 and 5.65-GHz to protect some important existing applications such as the Microwave Landing System (MLS). This is exactly favorable for the WiMedia's MB-OFDM UWB standard, which adopts frequency hopping between the bands within a band group according to certain pre-defined patterns. It is also interesting to note that there is no mandatory requirement for any interference-mitigation mechanism to minimize its interference to other wireless systems according to the FCC's definition of UWB system, which substantially eases the implementation of the FCC compliant UWB systems.

Most of the major wireless markets around the world have announced their respective regulations for UWB operation thereafter, including Korea, Japan, European Union and China [2][3][4][5]. The allocated spectrum in these countries and areas are summarized in Table 2.1 and their respective regulations are described in Appendix A in details.

Table 2.1 UWB Spectrum Allocation in Other Countries and Areas

Countries and Areas	Allocated Spectrum for UWB Operation	Year
Korea	3.1~4.8-GHz and 7.2~10.2-GHz	Jul, 2006
Japan	3.4~4.8-GHz and 7.25~10.25-GHz	Aug, 2006
European Union	3.1~4.8-GHz and 6.0~9.0-GHz	Feb, 2007
China	4.2~4.8-GHz and 6.0~9.0-GHz	Dec, 2008

The spectrum allocations for UWB system in different countries and areas differ from each other, however, some general coherence can be observed. First of all, the allocated spectrums for UWB operation are mostly in a dual-band form except in the US, revealing the intention to protect the unlicensed wireless operations in the 5-GHz ISM band as well as other specific wireless operations up to about 7-GHz in Korea and Japan.

As a matter of fact, to further minimize the interference to other incumbent wireless systems, most of the regulations demand use of certain interference-mitigation mechanisms in part of its allocated UWB spectrum, except in the US. The introduction of those mitigation mechanisms really increases the design complexity and the implement difficulty of the baseband algorithm for the UWB system. Meanwhile, the mitigation mechanisms generally reduce the overall data throughput efficiency of the UWB system by literally requesting the UWB system to “give way” to the other existing wireless systems.

As such, to develop a UWB transmission system that is worldwide operable, the frequency band where the mitigation techniques are not imposed draws much interest due to the relatively simpler implementation. The 7.2-9.0-GHz is the maximum

commonly allocated bandwidth after EU approved the 8.5-9.0-GHz for UWB operation, although it is still under constraint of mitigation mechanisms.

Various spectrum utilization schemes have been proposed ever since FCC opened the 3.1-10.6-GHz spectrum for UWB operation, ranging from direct forward short-impulse methods to multi-band plans with complex modulation schemes. The pioneering industrial and academic parties sought to standardize the UWB PHY definition under the framework of the Institute of Electrical and Electronics Engineers (IEEE) and the IEEE 802.15 WPAN High Rate Alternative PHY Task Group 3a (TG3a) was launched to evaluate and consolidate the PHY proposals. The TG3a successfully reduced many initial proposals to two final candidates, namely, the Direct-Sequence UWB (DS-UWB) and the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) UWB.

Figure 2.2 Band Scheme of the DS-UWB Proposal

The DS-UWB proposal is supported by the UWB FORUM, a Special Interest Group (SIG) of UWB PHY mainly led by Motorola and Freescale. The DS-UWB proposal

divides the allocated spectrum into two bands to minimize the interference with the 5-GHz ISM band; the lower band occupies 3.1 to 4.8-GHz and the higher band occupies 6.2 to 9.7-GHz, as shown in Figure 2.2. In each band, this proposal employs Direct Sequence Spread Spectrum (DSSS) technique to spread the spectrum of binary phase shift keyed UWB pulses for utilization of the full bandwidth. By introducing the DSSS technique, the multiple access capability of the proposed system is obtained by the differentiating sequences.

The MB-OFDM proposal is supported by the WiMedia Alliance, another UWB PHY SIG led by Intel, Texas Instrument, Nokia and etc. This proposal uses the available spectrum in a more complex way, where multiple bands and band groups are introduced. Six band groups are defined over the 3.1 to 10.6-GHz frequency band; each band group contains two or three bands. Each band has 528-MHz bandwidth and their center frequencies are given by

$$f_n = 2904 + 528 * n \quad (2.4)$$

where $n = 1, 2, \dots, 13, 14$. The detailed band and band group planning is shown in Figure 2.3.

Figure 2.3 Band Scheme of the MB-OFDM UWB Proposal

As shown in the figure,

- Band group 1 comprises band 1~3;
- Band group 2 comprises band 4~6;
- Band group 3 comprises band 7~9;
- Band group 4 comprises band 10~12;
- Band group 5 comprises band 13 and 14;
- Band group 6 was defined after the issue of UWB regulation in countries and areas other than the US. It includes band 9~11 to accommodate the lower high-end frequency of the spectrum allocated for UWB operation in those countries and areas.

As evidently suggested by its name, the MB-OFDM UWB wireless system transmits information using the OFDM modulation scheme. During its operation, each band is occupied by a 528-MHz bandwidth OFDM symbol. The OFDM symbol consists of 128 subcarriers with 4.125-MHz spacing, of which 100 subcarriers are data tones, 12 subcarriers are pilot tones, 10 subcarriers are guard tones and the remaining 6 subcarriers are zero tones. The subcarriers are modulated by quadrature phase shift

keying (QPSK) for lower data rate links or dual carrier modulation (DCM) technique for high data rate links. Frequency hopping technique is used to increase the transient transmission power as well as to reduce the requirement for the sampling rate of the analog-to-digital converter (ADC) in the receiver chain.

The supporters of the DS-UWB and MB-OFDM UWB proposals formed their respective campaigns in the IEEE 802.15 TG3a. Neither of the two campaigns was able to create sufficient advantage to hit the 75 percent supporting ratio in the multi-round votes and the progress of the TG3a had been stuck in the voting procedure [12]. No compromise had been reached between the two campaigns and the stalemate led to the fact that Freescale and Motorola, the main leaders of the DS-UWB proposal, pulled out from the UWB FORUM SIG and directly pursued marketing of its “Cable Free” UWB chipset solution. Meanwhile, the WiMedia Alliance managed to standardize its proposal for UWB PHY and MAC specifications to be published as Ecma International standards in December 2005. The WiMedia Alliance’s mandatory specification for PHY layer and MAC sub-layer are published in the ECMA-368 single standard document [13]; and the WiMedia’s proposed PHY layer and MAC sub-layer interface (WiMedia PHY-MAC Interface) is published in ECMA-369 [14]. The ECMA-368 and ECMA-369 standards are later approved as the International Organization for Standardization (ISO) standards [15][16] and European Telecommunications Standards Institute (ETSI) standard (ETSI IS 102 455 for ECMA-368) [17] respectively.

Hence, the WiMedia Alliance’s MB-OFDM UWB PHY proposal, or in other words the ECMA-368 UWB PHY standard, has virtually become the real industrial UWB

PHY standard, given the fading-out of the other competing campaign. Consequently, it is necessary to investigate the portion of the WiMedia Alliance's UWB PHY that is directly related to the receiver front-end circuits design, based on which some specifications required for the UWB LNAs can be deduced.

2.2 WiMedia Alliance's UWB PHY Standard Overview

In the Open Systems Interconnection (OSI) reference model, the PHY layer is the bottom-most layer that serves as the bridge between the MAC sub-layer and the physical propagation medium. In a transmitter, the PHY layer converts the data received from MAC sub-layer to waveforms suitable for transmitting in the physical medium; while in a receiver, the PHY layer converts the waveform received from the physical medium to data recognizable by MAC sub-layer, as shown in Figure 2.4. For the UWB wireless transmission system, the propagation path between the transmitting antenna and the receiving antenna is the physical medium of the radio signal.

Figure 2.4 Function of PHY Layer in Wireless Communication Systems

In the WiMedia Alliance's UWB PHY standard, the waveform to be transmitted and received by the PHY layer is a frequency-hopping OFDM signal. As shown in Figure 2.3, a total of six band groups are defined in the WiMedia Alliance's UWB PHY

standard and the frequency hopping only occurs between the three (or two for Band Group 5) bands in one band group under certain predefined hopping pattern. Thus, the instantaneous active RF bandwidth is only 528-MHz; the total active bandwidth during an operation period is 1,584-MHz if the device is operating in Band Group 1-4 and 6 or 1,056-MHz if the device is operating in Band Group 5. According to the bandpass sampling theorem, the 528-MHz instantaneous RF bandwidth allows the ADC data converter in the receiver PHY to be sampling only 1/3 (or 1/2 for Band Group 5) of the total active RF bandwidth at a time, requiring a relatively low sampling rate of 528M samples per second. On the other hand, the hopping nature of the UWB signal indicates that the OFDM signal only exists in each of the bands for 1/3 of the overall operation time (1/2 for Band Group 5 operation) when the integration period is long enough. Consequently, while the worldwide regulations define the maximum allowed power spectral density for UWB transmission as averaged over a relatively long time frame of 1-mS, this frequency hopping mechanism actually allows the transient transmission power of the WiMedia Alliance's UWB PHY to be three time larger than the maximum average power spectral density.

The UWB low-noise amplifier is the first circuit block that directly follows the antenna in a UWB receiver; it should amplify the received UWB signal in the operation band while adding little noise and distortion to it. Since the operation band has been well defined by the regulation bodies, it is important to understand the power level of the received UWB signal so that the LNA's linearity could be designed to be

sufficient to handle the maximum signal power level without distortion. Hence, the structure of a UWB OFDM symbol should be examined in detail.

As defined by the WiMedia Alliance, an OFDM symbol consists of 128 subcarriers, which are located evenly in the 528-MHz bandwidth. The frequency spacing between the subcarriers is uniform and can be calculated by

$$\Delta f = 528\text{MHz} \div 128 = 4.125\text{MHz} \quad (2.5)$$

As such, we can express the 128-subcarrier OFDM symbol as the sum of a serial of vectors given by Equation (2.6), with each vector representing data on the corresponding subcarrier.

$$S = \sum_{k=-64}^{64} X[k] \quad (2.6)$$

where $k=-64, -63, -62, \dots, -3, -2, -1, +1, +2, +3, \dots, +62, +63, +64$, corresponding to the 128 subcarriers constitute the OFDM symbol. It is quite difficult for a subcarrier located at zero frequency offset to the center frequency of the symbol to carry useful information due to the DC offset problem. Consequently, the DC component is not employed to carry data in the OFDM symbol, i.e., $X[0]=0$.

It is easily seen that with the center frequency of the adjacent bands located exactly 528-MHz between each other and the 128 subcarriers in one band spaced 4.125-MHz between each other, the spectral spacing between the right-most subcarrier of the lower band and the left-most subcarrier of the upper band is just 4.125MHz. This leaves no extra gap for filtering the interference from the adjacent band before

sampling, which potentially introduces the aliasing problem into the desired signal and degrades the signal-to-noise ratio. Consequently, certain frequency gap needs to be guaranteed to avoid the undesirable adjacent band aliasing. The WiMedia Alliance's UWB PHY standard defines the outmost 6 subcarriers in an OFDM symbol to be constant zero to provide the spectral gap desirable to deal with the adjacent band aliasing problem. This puts the subcarrier numbered -64, -63, -62 and +62, +63, +64 to be constant zero, so we have

$$X[-64] = X[-63] = X[-62] = X[+62] = X[+63] = X[+64] = 0 \quad (2.7)$$

This arrangement leaves 12.375-MHz frequency gap on each side of the OFDM symbol, so the total spacing between the right-most data-carrying subcarrier of the lower band and the left-most data-carrying subcarrier of the upper band is 24.75-MHz, which puts relaxed but still stringent demand for the baseband filter roll-off response. As a matter of fact, such spectrum arrangement also reduces the total actual RF bandwidth of the OFDM symbol to 503.25-MHz, which still meets the regulation bodies' requirement.

To further loosen the requirement for the anti-aliasing filter, the WiMedia Alliance's UWB PHY standard assigns the five subcarriers adjacent to the three zero carriers to be guard carriers on both sides, resulting in ten total guard carriers $X[-61, -60, -59, -58, -57, +57, +58, +59, +60, +61]$. Since assigning the guard carriers to zero would further reduce the actual RF bandwidth of the OFDM symbol to below 500-MHz, which fails to meet the UWB signal definition of some regulatory bodies, the WiMedia Alliance's standard defines the guard carriers to be simple replicas of some inner data subcarriers.

The ten guard carriers and six zero carriers between the right-most data subcarrier of the lower band and the left-most data subcarrier of the higher band create a total of 66-MHz spacing for the anti-aliasing filter to roll off from pass-band to stop-band, which greatly reduces its implementation difficulties.

In order to allow for coherent detection as well as to ensure robustness under frequency offset and degraded phase noise conditions, twelve pilot subcarriers, $X[-55, -45, -35, -25, -15, -5, +5, +15, +25, +35, +45, +55]$, are defined in the inner 112 subcarriers with equal spacing.

Finally, the remaining 100 subcarriers are all data carriers. So among all the 128 subcarriers in the OFDM symbol defined by WiMedia Alliance's UWB standard, there are 100 data carriers, 12 pilot carriers, 10 guard carriers and 6 zero carriers.

Besides the arrangement in the frequency domain to avoid adjacent band interference, the WiMedia Alliance's UWB standard also makes certain arrangement in the time domain to mitigate the Inter-Symbol Interference (ISI) and multi-path fading issue. The 128-subcarrier OFDM symbol is sampled at 128 points and obviously, if no time interval is introduced between consecutive OFDM symbols at the transmitter side, the received OFDM symbols will be polluted by the multipath components of previous symbols that arrive later in time. Meanwhile, time intervals between OFDM symbols are also desirable from hardware's point of view, i.e., the transmitter and the receiver both need some time to hop and settle when frequency hopping between OFDM symbols takes place. Based on this, the WiMedia Alliance's UWB standard dictates a fixed time interval between two consecutive OFDM symbols, which is termed as zero-

padded suffix (ZPS). The length of the ZPS is fixed at 37 samples, during which the hardware finishes settling after hopping within 5 samples and the multipath transient effect is mitigated by the “overlap-and-add” method defined by the standard. The 128-sample OFDM symbol and the 37-sample ZPS constitute a symbol with a total length of 165 samples in the time domain.

As discussed above, to sample the 528-MHz RF bandwidth of a UWB OFDM symbol without aliasing, the chosen sampling rate f_s is 528M samples per second. This translates into a sampling interval Δt of

$$\Delta t = 1 / f_s = 1.89ns \quad (2.8)$$

So the time duration of the OFDM symbol T_{OS} is

$$T_{OS} = 128 \times \Delta t = 242.5ns \quad (2.9)$$

And the time duration of the ZPS T_{ZPS} is

$$T_{ZPS} = 37 \times \Delta t = 70ns \quad (2.10)$$

Consequently, the total symbol time T_S is

$$T_S = T_{OS} + T_{ZPS} = 312.5ns \quad (2.11)$$

Based on the discussion above, we can summarize the important parameters related to the OFDM symbol defined in the WiMedia Alliance’s UWB PHY standard in Table 2.2 [13].

Table 2.2 Key Parameters of WiMedia Alliance's UWB Symbol [13]

Parameters	Value	Description
f_s	528-MHz	sampling frequency as well as the RF bandwidth being sampled
N	128	total number of subcarriers, also number of samples in an OFDM symbol and FFT size
N_D	100	number of data carriers in an OFDM symbol
N_Z	6	number of zero carriers in an OFDM symbol zero carriers are $X[-64,-63,-62,+62,+63,+64]$
N_G	10	number of guard carriers in an OFDM symbol guard carriers are $X[-61,-60,-59,-58,-57,+57,+58,+59,+60,+61]$
N_P	12	number of pilot carriers in an OFDM symbol pilot carriers are $X[-55,-45,-35,-25,-15,-5,+5,+15,+25,+35,+45,+55]$
N_{ZPS}	37	number of samples in zero-padded suffix
Δt	1.89-ns	sample interval; $\Delta t = 1/f_s$
Δf	4.125-MHz	subcarrier spacing; $\Delta f = f_s/N$
N_S	165	number of samples per symbol; $N_S = N + N_{ZPS}$
T_S	312.5-ns	total symbol time $T_S = \Delta t * N_S$

A serial of Time-Frequency Codes (TFC) are defined by the WiMedia Alliance's UWB standard to specify the frequency hopping pattern. According to the definition, the device can operate in either fixed frequency mode or frequency hopping mode; frequency hopping can take place in pre-defined orders between two or three bands within a band group. Figure 2.5 shows an example of the actual frequency hopping UWB signal, taking the TFC=1 as the signal's frequency hopping pattern [13].

Figure 2.5 Frequency Hopping UWB Signal with TFC=1

As can be easily observed from Figure 2.5, the symbol only exists one-third of the total time in a relatively long time frame, which allows the maximum power spectral density of the symbol to be three times of the allowed maximum average power spectral density. The introduction of the ZPS after the OFDM symbol actually further increases the maximum power spectral density of the OFDM symbol since there is also no emission power during the 37 sample ZPS period.

As the increase of transient power is allowed by the frequency hopping and ZPS mechanism, it is important to understand the maximum transient power spectral density of the OFDM symbol and the maximum power of each subcarrier since they are fundamental parameters to determine the linearity of the receiver. The maximum transient power spectral density of a symbol PSD_s can be calculated by

$$PSD_s = -41.3 + 10 \log_{10} 3 = -36.5 \text{ dBm/MHz} \quad (2.12)$$

And the maximum transient power spectral density of the OFDM symbol PSD_{OS} can be calculated by

$$PSD_{OS} = PSD_s + 10 \log_{10} \frac{N_s}{N} = -35.4 \text{ dBm/MHz} \quad (2.13)$$

Considering the maximum transmitting power is achieved only when the OFDM symbol has an ideally flat power spectral density, the 4.125-MHz frequency spacing between the nearby subcarriers can be used as the bandwidth of the subcarrier to determine its maximum possible power. So the maximum power of the subcarrier P_{SC} can be calculated by

$$P_{SC} = PSD_{OS} + 10 \log_{10} BW_{SC} = -29.2 \text{ dBm} \quad (2.14)$$

And the total power of the OFDM symbol P_{OS} can be calculated by

$$P_{OS} = PSD_{OS} + 10 \log_{10} 122 \times BW_{SC} = -8.4 \text{ dBm} \quad (2.15)$$

Based on those numbers, we are able to perform a system link budget analysis and determine the required specifications for the UWB receiver as well as the low-noise amplifier in the following chapter.

2.3 Summary

This chapter reviews and compares the existing regulations of ultra-wideband transmission system in the main wireless markets all over the world. The UWB standardization process is reviewed and the development of the WiMedia Alliance's UWB PHY standard toward the actual industrial UWB standard is described. Combining the worldwide UWB spectrum allocation and the WiMedia Alliance's UWB PHY standard, Figure 2.6 best describes the regulatory status up to date [18].

Figure 2.6 Worldwide UWB Regulatory Status [18]

As can be observed from Figure 2.6, the common operable spectrum for the five countries and areas are Band 3, Band 9, Band 10 and Band 11. However, mitigation mechanisms are required for device operating in Band 3 after 2010 except in the US and the EU requires mitigation mechanisms for device operating in Band 11.

Finally, the important parameters of the frequency-hopping OFDM signal employed in the WiMedia Alliance's UWB PHY standard are studied in detail in this chapter, which will help to develop the UWB system link budget and specifications of the UWB receiver and its LNA.

CHAPTER 3 Overview of the CMOS Low-Noise Amplifier Designs

Understanding the basic design principles, specifications, considerations and techniques for the low-noise amplifier is an important fundament for design of the CMOS UWB LNA. In this chapter, the general LNA design considerations and specifications will be discussed. The conventional design methodologies for narrow band CMOS LNAs will be reviewed, followed by the discussion on the techniques to extend the matching and gain bandwidth toward the requirement of the LNA for a UWB receiver. The target specifications of the UWB LNA will be derived based on the understanding of the design principles and the parameters of the UWB signal. The state-of-the-art UWB LNA architectures will be reviewed in the last section.

3.1 LNA Design Considerations and Specifications

The low-noise amplifier is generally the first circuit block that is integrated on silicon in a CMOS receiver chain since the preceding antennas and pre-selection filters are normally implemented discretely using other technologies. In a fully integrated receiver solution where the direct conversion architecture is prevalent, the LNA is normally followed directly by an on-chip mixer; while in super-heterodyne receivers, possibly the amplified RF signal will be routed off-chip to a discrete filter to reject the image signal before being routed back to the on-chip mixer for down-conversion. The LNA needs to exhibit certain input impedance to the circuit blocks precede it since the termination impedance will significantly influence the characteristics of those blocks. Similarly, the output impedance of the LNA needs to match to the input impedance of next stage conjugately to ensure the condition of maximum power transfer is satisfied.

Sufficient gain needs to be provided by the LNA in the desired frequency band to boost the power level of the useful RF signal while adding as little noise as possible. The signal transmission in the reverse direction needs to be suppressed to ensure stability and minimize the unwanted interferers. The LNA should be capable of handling large signals with minimum distortion since the power of the useful signals as well as the power of the interfering signals could be quite high if their transmitters are placed close to the receiver. While the LNA is dealing with high-bandwidth signals, the delay of the signal at different frequencies is desired to remain constant so as to minimize the dispersive distortion, which put constant group delay an important figure-of-merit for wideband LNAs. The general design considerations for the low-noise amplifier circuits are discussed below.

3.1.1 Input Matching

In a typical wireless receiver, the LNA follows the RF band pass filter (BPF), the diplexer/duplexer or the antenna directly, all of which are normally implemented on technologies other than the silicon-based CMOS. The characteristics of those passive components are heavily dependent on the quality of termination to them. Consequently, the input impedance of the LNA, which terminates those components, needs to exhibit as little deviation from the ideal termination impedance as possible. The ideal termination impedance for an off-chip passive component is usually designed to be the standard characteristic impedance of the RF system, which is 50-Ohm.

The four scattering parameters (S_{11} , S_{21} , S_{12} and S_{22}) are commonly used to describe the transmission characteristics of a two-port network in RF and microwave

frequencies. The input port and the output port of a two-port network are normally denoted at Port 1 and Port 2 respectively. Under this designation, S_{11} is the input reflection coefficient with output port matched; S_{21} is the forward transmission coefficient with the output port matched; S_{12} is the backward transmission coefficient with the input port matched; and S_{22} is the output reflection coefficient with the input port matched. The definition of the S-Parameters of a two-port network is shown in Figure 3.1, where a_1 and a_2 are incident waves at the input port and output port respectively and b_1 and b_2 are reflected waves at the input port and output port respectively. Z_S is the source impedance at the input port, Z_L is the load impedance at the output port and Z_O is the characteristic impedance of the RF system.

Figure 3.1 Definition of S-Parameters

Hence, S_{11} represents the degree that the input impedance of the LNA matches to 50-Ohm. S_{11} can be given by Equation (3.1) below according to its definition.

$$S_{11} = \Gamma_{in} \Big|_{Z_L=Z_o} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o} \Big|_{Z_L=Z_o} \quad (3.1)$$

where Γ_{in} is the reflection coefficient at the input port and Z_{in} is the input impedance.

Although perfect matching to 50-Ohm is desirable, real implementation suffers from non-ideal effects as well as constraints from other specifications; so deviation from 50-Ohm is permitted to a certain degree. Generally, input port with S_{11} of better than -10-dB is considered to be in good matching condition. This corresponds to a magnitude of around 0.316 for the reflection coefficient at the input port and a voltage standing wave ratio (VSWR) of around 1.92. Figure 3.2 shows the input impedance region in the Smith chart where the corresponding S_{11} is better than -10-dB.

Figure 3.2 Good Input and Output Matching Region in the Smith Chart

3.1.2 Output Matching

In conventional discrete receiver implementations, the output impedance of the LNA should be matched to 50-Ohm since the amplified RF signal will be routed to the input of the next stage through a 50-Ohm transmission line. This is also true in some integrated receiver implementations, where the amplified RF signal needs to be routed off chip for certain processing, such as image rejection filtering, before being routed

back onto the chip. However, in a fully integrated solution where the output of the LNA is directly connected to the input of the next stage, the output impedance of the LNA does not necessarily need to match to 50-Ohm. This is because the length of the on-chip interconnecting metal trace is negligible comparing with the wave length of the signal and maximum voltage swing is important at this interface for delivery of the amplified signal to next stage. Consequently, in an integrated narrow band receiver design, an inductive load of the LNA usually resonates with the input impedance of the next stage at the operating frequency. For a wideband system, the input capacitance of the next stage can also be co-designed with the wideband load network of the LNA and absorbed in the network.

Figure 3.3 Insertion of Output Buffer for Measurement

Although the LNA in the fully integrated receiver design does not require 50-Ohm matching at its output port, such matching is still needed while the LNA is pulled out from the receiver chain and measured as a standalone device. As shown in Figure 3.3, the standard 50-Ohm input impedance of the network analyzer or spectrum analyzer will be loaded directly at the output of the LNA. Most of the times, this is disastrous to the performance of the LNA without an output buffer since the impedance of the load is desired to be quite high at the interested frequency band to acquire sufficient gain.

In such case, an output buffer is normally added on-chip after the core LNA circuits for measurement purposed only, as shown in Figure 3.3. The output reflection coefficient S_{22} defined in Figure 3.1 is adopted to represent the degree that the output impedance of the LNA matches to 50-Ohm. S_{22} of better than -10-dB is considered to be good enough and the region of corresponding output impedance is shown in Figure 3.2. The gain (or loss) of the buffer needs to be de-embedded from the measured gain to acquire the actual gain of the core LNA circuit; the input impedance of the buffer needs to be understood, since the input impedance of the next stage circuit needs to be the same to ensure the gain characteristic of the LNA in an integrated receiver is identical to the de-embedded result.

3.1.3 Forward Gain

The low-noise amplifier needs to provide sufficient gain to the RF signal so that it can acquire sufficient amplitude to be properly processed by the following stages. The gain of the LNA plays a significant role in determining the noise contribution by the following stages; a high gain LNA reduces the contribution of the subsequent stages on the overall receiver noise figure and is normally desirable. However, achieving high gain normally associates with increased power consumption and reduced linearity performance, thus those specifications need to be traded off properly in the LNA design. The forward gain of the LNA is depicted by the forward transmission coefficient S_{21} as defined in Figure 3.1.

Conventionally, the gain bandwidth of the LNA is defined as the range of frequency spectrum within which the gain is no more than 3-dB less than the maximum gain, namely, the -3-dB bandwidth. For narrowband receiver, the gain is desirable to peak at

the operation frequency of the wireless transmission system; while for wideband receiver, the gain is desirable to be relatively flat over the interested operation frequency band, with less than 3-dB gain ripple throughout the entire operation band. As discussed above, due to the introduction of the output buffer for measurement purpose, the actual gain and bandwidth of the LNA in an integrated receiver can only be obtained after de-embedding the effect of the output buffer.

3.1.4 Reverse Isolation

Ideally, the RF signal in the LNA travels only from the input port to the output port, without any backward transmission. However, in real world the active devices incorporated in the LNA circuits are not unilateral and the excessive parasitic effects also introduce additional backward transmission paths for RF signal. Such backward transmission from the output port of the LNA to the input port brings about potential stability issues since the amplified signal finds its way to feed back to the input, especially when the gain is high. On the other hand, it is also possible that the local oscillator (LO) signal or other reflected signal at the LNA and next stage circuits interface leaks to the receiver antenna through the backward transmission and potentially pollutes the spectrum in the wireless medium.

Consequently, the reverse isolation needs to be examined in LNA designs. The backward transmission coefficient S_{12} defined in Figure 3.1 is employed to quantify the degree of isolation from the output port to the input. Typically, S_{12} of better than -30-dB is needed to make sure that the non-ideal backward transmission will not lead to any undesirable problem.

3.1.5 Noise Figure

The amount of signal-to-noise ratio degradation through the LNA reflects how much noise the LNA adds to the signal when amplifying it. Thus, the noise factor of a low-noise amplifier is defined by the ratio of signal-to-noise ratio (SNR) at the input port to the signal-to-noise ratio at the output port. The noise factor F is mathematically given by

$$F = \frac{S_i/N_i}{S_o/N_o} \quad (3.2)$$

where S_i and S_o are the signal power at the input and output port respectively and N_i and N_o are the noise powers at the input and output port respectively. The noise figure NF is defined as the logarithm of the noise factor, given by

$$NF = 10 \log_{10} F \quad (3.3)$$

Since S_i and S_o are related by

$$S_o = G * S_i \quad (3.4)$$

where G is the forward gain of the LNA, the noise factor F can be re-written by

$$F = \frac{S_i}{S_o} * \frac{N_o}{N_i} = \frac{N_o}{G * N_i} \quad (3.5)$$

Equation (3.5) reveals that the noise factor can also be interpreted as the ratio of total noise power at the output port to the output noise power due to the input noise.

Figure 3.4 shows the noise contribution of a receiver chain assuming ideal matching to standard characteristic impedance is achieved at all input and output ports. The LNA has a power gain of G_1 and the available output noise power of the LNA is N_1 when connected to the standard source impedance; the blocks following the LNA (including

the mixer, filters and etc) are considered as whole, whose overall gain is G_2 and overall available output noise power is N_2 .

Figure 3.4 Cascaded Receiver Chain Noise Analysis

As shown in the figure, N_S is the available noise power from the source, which can be expressed as

$$N_S = kTB \quad (3.6)$$

where k is the Boltzmann's constant, namely 1.38×10^{-23} J/K. T is the absolute operation temperature in Kelvin and B is the noise bandwidth in Hertz.

Hence the total available noise power at the LNA output is given by

$$N_{O1} = N_S * G_1 + N_1 \quad (3.7)$$

Similarly the total available noise power at the receiver chain output can be given by

$$\begin{aligned} N_{O2} &= N_{O1} * G_2 + N_2 \\ &= (N_S * G_1 + N_1) * G_2 + N_2 \end{aligned} \quad (3.8)$$

And the overall noise factor of the receiver can be calculated strictly according to its definition by

$$F = \frac{N_{o2}}{N_s * G_1 * G_2} = \frac{(N_s * G_1 + N_1) * G_2 + N_2}{N_s * G_1 * G_2} \quad (3.9)$$

$$= \frac{N_s * G_1 + N_1}{N_s * G_1} + \frac{N_2}{N_s * G_1 * G_2}$$

Since the noise factor of the LNA F_1 and the noise factor of the subsequent blocks F_2 are defined by

$$F_1 = \frac{N_s * G_1 + N_1}{N_s * G_1} = 1 + \frac{N_1}{N_s * G_1} \quad (3.10)$$

$$F_2 = \frac{N_s * G_2 + N_2}{N_s * G_2} = 1 + \frac{N_2}{N_s * G_2} \quad (3.11)$$

The overall noise factor expression can be re-arranged to be given by

$$F = F_1 + \frac{F_2 - 1}{G_1} \quad (3.12)$$

Equation (3.12) shows that the noise performance of the whole receiver is largely dependent on the noise performance of the LNA; the noise of the following stages contributes to the overall noise performance only indirectly and the contribution is inversely proportional to the gain of the LNA.

For low-noise amplifier design on standard CMOS process technology, the device's physical dimension and biasing point are the design freedoms to achieve low noise figure. Hence, it is important to examine the noise sources in the MOS transistor and their properties so as to discover the way to determine optimum device geometry and biasing point for noise performance. Since the NMOS is normally preferred as the active device in a CMOS LNA over PMOS due to its higher electron mobility and thus better performance, NMOS symbol is used in the following study. The noise source in long channel MOS transistors has been studied in detail [19]. Although the flicker

noise dominates the noise contribution of the MOS transistor in the low frequency range, the dominant noise sources at RF frequencies are the channel thermal noise and gate noise, as shown in the Figure 3.5.

Figure 3.5 Dominant Noise Sources at RF Frequencies in the NMOS Transistor

In Figure 3.5, C_{gs} , V_{gs} and g_m are the gate-to-source capacitance, the gate-to-source voltage and the transconductance of the NMOS transistor respectively. The channel thermal noise and the gate noise are modeled by two noise current sources i_{nd} and i_{ng} respectively.

The channel thermal noise arises from the thermal noise of the channel resistance and its spectral density is normally modeled as

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{d0} \quad (3.13)$$

where γ is the NMOS transistor's channel thermal noise coefficient and g_{d0} is its zero-biased drain conductance. The zero-biased drain conductance is related with g_m by a coefficient α as

$$g_{d0} = g_m / \alpha \quad (3.14)$$

The gate noise mainly comprises the noise of the physical gate resistance and the induced gate noise that stems from the capacitive coupling of the randomly fluctuating channel potential to the gate terminal. The former can be reduced to minimum by

adopting proper layout techniques such as the multi-finger structure while the later is an intrinsic noise source of the MOS transistor that needs to be taken into account during circuit design. The spectral density of the induced gate noise is normally modeled as

$$\frac{\overline{i_{ng}^2}}{\Delta f} = 4kT\delta g_g \quad (3.15)$$

where δ is the NMOS transistor's gate noise coefficient and g_g is the equivalent shunt gate conductance introduced by the non-quasi-static (NQS) effect, which can be given as

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (3.16)$$

Van der Ziel has shown that for long channel devices, α equals to 1, γ equals to 2/3 in saturation region and increases to 1 when V_{DS} approaches 0 and δ equals to 4/3 [19].

The induced gate noise is partially correlated with the channel thermal noise and their correlation coefficient is defined by

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \quad (3.17)$$

According to Van der Ziel [19], c equals to $-j0.395$ for long channel devices with the direction of the noise currents defined as in Figure 3.5.

Earlier research work on MOS transistor noise reported anomalous increase in both channel thermal noise and induced gate noise and attributes the increase to the hot electrons caused by the strong electric field in the short-channel devices [20][21]. However, recent research work showed that the anomalous increase of noise observed

in the previous work could be possibly brought by the noise contributed by other noise source, including the avalanche noise caused by improper biasing of device, underestimation of the physical gate resistance and etc [22][23][24]. A thorough measurement and modeling of the noise sources in MOS transistors was performed in [22] at the 0.18- μm CMOS technology node, and the result showed that the noise from the two intrinsic noise sources increased only moderately comparing with the long channel devices: the channel thermal noise coefficient γ was found to be about 1.1, the gate noise coefficient δ was found to be about 3.3, the correlation coefficient c was still pure imaginary but its magnitude was reduced to about 0.2, which was in line with the result of Chen's work [25].

3.1.6 1-dB Compression Point

The 1-dB compression point (CP1) is an important figure-of-merit in describing the linearity of a circuit, specifically, the capability to handle high input power. The low-noise amplifier faces linearity challenge when the input signal or interferer power level approaches its handling limit mainly due to the saturation of the active devices. The 1-dB compression point is defined to be the power level at which the signal gain is compressed by 1-dB comparing with its small signal gain. According to this definition, we have

$$OCP1 = ICP1 + G - 1dB \quad (3.18)$$

where G is the small signal gain of the LNA; $ICP1$ and $OCP1$ are the 1-dB compression point of the LNA referred at the input port and the output port respectively. This is clearly demonstrated in Figure 3.6, in which the input-output

power relationship of the LNA is plotted and gain compression can be observed at high input power levels.

Figure 3.6 Input-Referred and Output-Referred 1-dB Compression Point

The maximum allowed input power of the in-band signal and interferer need to be understood before determining the specification for CP1 of the LNA. In real applications, the maximum operable power level needs to have several dBs back-off from the 1-dB compression point to avoid substantial signal quality degradation due to compression.

3.1.7 3rd-Order Intercept Point

The 3rd-order intercept point (IP3) is another figure-of-merit in describing the linearity of a circuit. Inter-modulation between signals of different frequencies could result in generation of unwanted interfering signal at related frequencies. Moreover, the products of the 3rd-order inter-modulation usually fall well in-band and cannot be filtered or attenuated by the RF front-end circuits. Thus, the signal-to-noise ratio

degrades inevitably when strong 3rd-order inter-modulation exists. The 3rd-order inter-modulation products could result from both the in-band signals of the interested wireless systems that adopts multiple carriers and the out-band signals of the other wireless systems whose frequency spacing is close to the frequency spacing between the interested band and either of the out-band signal, as shown in Figure 3.7.

The 3rd-order intercept point is defined as the power level where the 3rd-order inter-modulation product reaches the same power level as the fundamental signal at the output. Similar to CP1, the IP3 can be referred at the input port (IIP3) or the output port (OIP3), related by

$$OIP3 = IIP3 + G \quad (3.19)$$

Figure 3.7 Interferers due to 3rd-Order Inter-Modulation
(a) Interferer Caused by In-band Signals (b) Interferer Caused by Out-band Signals

In [26], the mathematical relationship between the IP3 and CP1 are investigated assuming that the non-linear behavior of the circuit can be fully modeled by a polynomial with constant coefficients against different power levels. The ICP1 and IIP3 are found to be related by

$$IIP3 = ICP1 + 9.6dB \quad (3.20)$$

The IIP3 and ICP1 of real circuits differ around but not exactly 9.6-dB since the behaviors of real devices deviate from the assumption of derivation. A graphical illustration of the input-referred and output-referred IP3 as well as their measurement method can be found in Appendix C in details.

For wideband communication systems, the 2nd-order inter-modulation is also an important figure-of-merit in studying the non-linearity of the receiver since there is good chance that the 2nd-order inter-modulation product of the received signal falls in the operation band of the wideband system itself, thus desensitizing the wideband receiver. However, IIP2 for the UWB LNA is not of great concern due to two reasons. First of all, the band group arrangement of the WiMedia Alliance's UWB standard actually makes the wideband system a relatively narrow one since only one 528-MHz band is active at a time. Moreover, the mixer follows the LNA in the UWB receiver usually comes in a differential form, which automatically cancels the 2nd-order inter-modulation products as long as it is not large, which is normally true since the UWB signal power level is low.

3.1.8 Stability

Considering the unwanted feedback path introduced in the low-noise amplifier circuits due to the parasitic effects, the LNA circuit is subject to possible oscillation since it usually has all the elements needed to complete an oscillator, namely the active gain, LC tank and feedback. Hence, it is important to investigate the stability of the LNA design and eliminate possible oscillation.

The LNA is unconditionally stable only if the magnitude of both the input reflection coefficient Γ_{in} and output reflection coefficient Γ_{out} are smaller than unity for all passive source and load impedances [27], given by

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \quad (3.21a)$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \quad (3.21b)$$

where Γ_S and Γ_L are the reflection coefficients of the source and the load impedances respectively, defined by

$$\Gamma_S = \frac{Z_S - Z_O}{Z_S + Z_O} \quad (3.22a)$$

$$\Gamma_L = \frac{Z_L - Z_O}{Z_L + Z_O} \quad (3.22b)$$

The magnitude of both Γ_S and Γ_L are no larger than unity for all passive source and load impedances.

Stability of the LNA circuit is normally evaluated using the K- Δ test method, in which the parameters K and Δ are defined as follows.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (3.23)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (3.24)$$

For the LNA circuit to be unconditionally stable, K should be larger than unity and $|\Delta|$ should be smaller than unity at all frequencies, which are necessary and sufficient conditions [27]. For LNA circuits that cannot achieve unconditional stability, extra

care should be taken in the design of the input and output matching network to ensure that the circuit is well within conditional stable region.

3.1.9 Group Delay

While processing a signal with wide frequency spreading, it is naturally desirable that all the frequency components of the signal experience same delay in the time domain in one circuit block so as to preserve its original phase relationship among those components. Otherwise, the wideband signal will suffer from frequency dispersion in the processing and potentially contributes to the increase of bit-error-rate of the system [28]. Constant delay in time domain for difference frequency components of the signal indicates a phase delay that increases linearly with frequency. Hence the group delay $T_D(\omega)$ is defined as follows to depict the conformance of the LNA to the desired relationship.

$$T_D(\omega) = -\frac{d\phi}{d\omega} \quad (3.25)$$

where ϕ is the phase shift of the LNA at frequency ω .

Practically, constant group delay cannot be achieved using finite order network; however, it is desirable to keep the in band group design as low as possible. Similar to the 2nd-order inter-modulation case, constant group delay of the LNA in a UWB receiver is not very important since the real time signal bandwidth is only 528-MHz rather than the whole available UWB spectrum according to the WiMedia Alliance's standard.

3.2 Conventional Narrowband CMOS LNA Designs

Generally speaking, the design of the low-noise amplifier starts from the selection of the input matching architecture, which essentially determines the trade-off between minimum noise figure achievable, quality and bandwidth of input matching as well as power consumption. The conventional narrowband CMOS LNA architectures are reviewed in this section to understand their respective advantages and disadvantages and inspire the design innovations on wideband LNA architectures.

Figure 3.8 Resistive Termination Input Matching Architecture
(a) Schematic (b) Small-Signal Equivalent Circuit

Figure 3.8 shows the resistive termination input matching architecture, in which the input port of a LNA is directly terminated by a 50-Ohm resistor. Using the direct resistive termination, high quality matching to 50-Ohm source impedance can be achieved very easily; however, the noise performance of such LNA could be quite poor [29]. Assuming the termination resistor is well matched to $R_S=50\text{-Ohm}$ and the induced gate noise is negligible, the noise factor (F) of the input stage can be easily derived and given as

$$F = 2 + \frac{4\gamma}{\alpha g_{m1} R_S} \quad (3.26)$$

where g_{m1} is the transconductance of the input MOS transistor M_1 .

It can be calculated that the noise figure is almost 5-dB for a long-channel device biased at a transconductance of 50-mS. Even though, the calculation is still conservative since it does not take the induced gate noise and other parasitic noise sources into consideration. Moreover, the increase of γ and decrease of α in short channel devices are also neglected. Consequently, although perfect matching can be obtained using this architecture, its noise performance is too poor to qualify itself as a decent candidate for LNA input architecture, especially considering the stringent sensitivity requirement of the wireless communication standards nowadays. This observation is also verified by the reported work [30][31].

Figure 3.9 Common-Gate Input Matching Architecture
(a) Schematic (b) Small-Signal Equivalent Circuit

As shown in Figure 3.9, the common-gate input architecture is well-known as the $1/g_m$ termination, since the impedance looking into the source of the input MOS transistor is $1/g_m$ while neglecting its gate-to-source capacitance C_{gs} . At a given frequency, C_{gs} can be resonated out using an inductor connecting between the source and ground, leaving only the $1/g_m$ item. Consequently, perfect matching at this frequency can be obtained while biasing the device at a transconductance of 20-mS. The noise factor of the common-gate stage is given by

$$F = 1 + \frac{\gamma}{\alpha g_{m1} R_S} \quad (3.27)$$

Under a perfect matching condition, the noise figure of the common-gate input architecture is calculated to be approximately 2.2-dB while taking the coefficients γ and α under long channel condition. Although the other noise sources are not considered in the calculation, the 2.2-dB noise figure is moderately good for LNA integrated in modern wireless receivers. Furthermore, since perfect matching is generally not required at the LNA input port, the noise figure can be further improved by trading off perfect matching condition for higher g_{m1} . Theoretically, g_{m1} can be increased to about 38-mS while the return loss at the LNA input port is still better than 10-dB. Under this condition, the noise figure achievable is improved to 1.3-dB according to the above calculation.

Due to the relatively higher noise and lower gain comparing with the common-source stage, very few narrow band LNA designs adopted the common-gate architecture [32]. However, since the noise performance can be improved by trading off perfect matching and the input matching provided by the common-gate stage is intrinsically wideband, we will re-visit the common-gate architecture in Chapter 5 of this thesis.

Figure 3.10 Shunt-Series Feedback Architecture
(a) Schematic (b) Small-Signal Equivalent Circuit

As shown in Figure 3.10, the shunt-series feedback architecture uses a combination of series and shunt feedback techniques to create a real part in the input impedance. The input impedance looking in to the input port of the shunt-series feedback architecture can be derived and given by

$$Z_{in} = \frac{(R_2 + R_3)R_1 + (R_2 + R_3)(1 + R_1 g_{m1})Z_{gs}}{R_1 + R_2 + R_3 + (1 + R_1 g_{m1} + R_3 g_{m1})Z_{gs}} \quad (3.28)$$

where Z_{gs} is the impedance between the gate and source terminals and is normally dominated by the gate-to-source capacitance of the MOS transistor. At low frequencies, Z_{in} can be simplified into

$$Z_{in} = \frac{(R_2 + R_3)(1 + R_1 g_{m1})}{(1 + R_1 g_{m1} + R_3 g_{m1})} \quad (3.29)$$

By tuning the values for R_1 , R_2 and R_3 as well as the MOS device's geometric size and biasing point, adequate input matching can be obtained.

However, only a few narrowband LNAs reported in the literature adopted this architecture or its revised form [31][33]. This is probably because the noise performance of the shunt-series feedback architecture is directly trading with the matching quality, making it quite difficult to achieve good matching quality and noise performance simultaneously. On the other hand, this architecture is intrinsically broadband since it does not take advantage of the inductors and capacitors for gain peaking, and this makes the shunt-series feedback LNAs generally power hungry [29].

The source inductive degeneration architecture had been used extensively in LNA designs based on compound semiconductor technologies. In [34], this technique was first introduced in standard CMOS process technology. A detailed mathematical

treatment is demonstrated in [29], which has been referenced by most of the subsequent work utilizing the source inductive degeneration architecture.

Figure 3.11 Source Inductive Degeneration Architecture
(a) Schematic (b) Small-Signal Equivalent Circuit

Figure 3.11 shows the schematic of the source inductive degeneration architecture and its simplified small-signal equivalent circuit. Simple derivation shows that the input impedance of this architecture can be given by

$$\begin{aligned} Z_{in} &= j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s \\ &\approx j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \omega_T L_s \end{aligned} \quad (3.30)$$

At the frequency where the gate-to-source capacitance C_{gs} resonates out with the combination of the source degeneration inductor L_s and gate inductor L_g , only the real part $\omega_T L_s$ is left in Z_{in} . As such, by properly selecting the biasing point of the MOS transistor and the source degeneration inductor L_s , perfect matching can be obtained at the resonant frequency of the series input network ω_0 , given by

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s) C_{gs}}} \quad (3.31)$$

A detailed derivation on the noise factor of the source inductive degeneration architecture with 50-Ohm source impedance was given in [29] and its subsequent corrections [35][36], which showed that the overall noise factor including the effect of the induced gate noise can be given as

$$NF = 1 + \frac{\gamma R_s \omega_0^2 C_{gs}^2}{\alpha g_m} + \frac{\alpha \delta (1 + \omega_0^2 C_{gs}^2 R_s^2)}{5 g_m R_s} \quad (3.32)$$

It was proven that the source inductive degeneration architecture achieves the 50-Ohm impedance matching condition while the noise matching condition is near-optimum [29]. This demonstrated that the source inductive degeneration architecture beautifully solves the trade-off between noise performance and input impedance matching, at the only cost of a little gain degeneration [37][38].

A substantial number of narrow band LNA work published in the literature achieved impressive noise performance using the source inductive degeneration architecture on standard CMOS process technology [39][40][41]. It can be observed that the designs utilizing the bonding wires as the gate or source inductors generally exhibited better noise performance due to the lower series resistance of the bonding wires comparing with the low-Q on-chip spiral inductors [39]. With the down-scaling of the CMOS process technology, this architecture has been employed in LNA designs that hits even higher frequency into the tens of GHz region [42][43][44], demonstrating the validation of the source inductive degeneration technique for millimeter-wave low-noise amplifier design.

In [45], a modified architecture was proposed to match the common-source input MOS transistor to 50-Ohm while eliminating the use of a source degeneration inductor, as shown in Figure 3.12.

Figure 3.12 Input Matching Architecture Proposed in [45]
(a) Schematic (b) Equivalent Circuit of the Input Matching Network

This architecture replaces the combination of the source and gate inductors in the input matching network with a LC parallel network connected at the gate. The resonant frequency of the LC parallel network ω_{01} is set to slightly higher than the operation frequency of the LNA. So at the frequency of interest ω_0 , the network is equivalent to a series combination of an inductance L_{gs} and a resistance R_{p2} due to the parasitic resistor of the inductor used in the LC parallel network shown in Figure 3.12(b). L_{gs} and R_{p2} can be given by

$$L_{gs} \approx \frac{L_{g1}}{1 - (\omega/\omega_{01})^2} \quad (3.33)$$

$$R_{p2} \approx \frac{R_{p1}}{(1 - (\omega/\omega_{01})^2)^2} \quad (3.34)$$

where ω_{01} is simply given by $\omega_{01} = (L_{g1}C_g)^{-1/2}$.

Input matching is achieved when R_{p2} is close to 50-Ohm and L_{gs} resonates out with the C_{gs} of the input MOS transistor. This architecture achieves similar matching quality and noise performance comparing with the source inductive degeneration architecture without any power consumption increase or gain degradation [37][45]. However, as can be observed in the expression of L_{gs} and R_{p2} , both terms approaches the desired value only near the nominal operation frequency and deviates quickly from the desired value once the frequency offsets from the nominal operation frequency due to the ω/ω_{01} component in the denominator. This is different from the source inductive degeneration architecture, in which the real part of the input impedance, namely, $\omega_T L_s$ is constant to the first order throughout the frequencies. Consequently, it is reasonable to expect that this gate LC parallel network architecture possesses narrower bandwidth comparing with the source inductive degeneration architecture. And because of this, the quality of input matching for this architecture is quite sensitive to possible process variation and a little variation in the value of the L_g and C_g could lead to a substantial change in the input impedance and the optimum matching frequency [37].

3.3 CMOS UWB LNA Specifications and State-of-the-Art Architectures

Based on the understanding of the UWB signal characteristics introduced in the previous chapter and the LNA design considerations developed above, the target specifications for the UWB LNA are derived in this section, followed by a brief review on the state-of-the-art UWB LNA architectures.

3.3.1 CMOS UWB LNA Target Specifications

The WiMedia Alliance's UWB PHY standard ECMA-368 has explicitly assumed an overall noise figure of 6.6-dB for the whole receiver while operating in Band Group 1,

together with an implementation loss of 2.5-dB and a margin of 3-dB. An additional of 1-2-dB is allowed while operating in Band Group 2-6. This requirement puts definitive constraints on the noise figure and forward gain to be achieved by the LNA stage, which largely determines the overall noise performance of the whole receiver as shown by Equation (3.12).

Assuming the overall noise figure of the stages that follows the LNA is 14-dB, which already leaves substantial design freedom for the subsequent mixer and the follow stages[46][47], Figure 3.13 plots the required noise figure and gain of the LNA stage to achieve different overall receiver noise figures based on calculations using Equation (3.12).

Figure 3.13 Required LNA Gain and Noise Figure for Different Overall Noise Figure

Coherent to the earlier discussion, it can be easily seen that the noise contribution from the following stages diminishes when the gain of the low-noise amplifier increases, relaxing the requirement on the noise figure of the LNA itself. However, the gain of

the LNA cannot be arbitrarily large from at least two other considerations. In the CMOS process technology, the transconductance of an active device is proportional to only square root of its DC biasing current; moreover, the increase in current becomes less efficient when the gain of the amplifier is increased in high gain region near gain saturation. This indicates that a very high gain low-noise amplifier could be very power hungry. On the other hand, achieving a very high gain LNA generally involves the employment of multiple stages, which compromises its linearity performance. Furthermore, the high level signal and interferers delivered by the LNA also challenge the linearity requirement of the next stage. Consequently, the gain of the LNA stage should be selected to be high enough to suppress the noise contribution of the following stages, but never too high to give rise to power dissipation or linearity problems.

As can be observed in Figure 3.13, the relaxation of the maximum allowed LNA noise figure by gain increase becomes less effective when the LNA gain is higher than 16-dB. As such, we select 16-dB as the minimum target for the forward gain of the LNA. With 16-dB gain, the noise figure of the LNA should be better than 4.0-dB to achieve an overall noise figure of 5.0-dB, assuming the overall noise figure of the following stages is 14-dB. Consequently, we select 4.0-dB as our target of maximum noise figure in the frequency range of Band Group 1, leaving 1.6-dB margin for the insertion loss of the pre-select filter, which is possibly needed between the antenna and the LNA to mitigate the out-band interferers.

As calculated in Chapter 2, the maximum emission power of an OFDM symbol is -8.4-dBm and the maximum power of a subcarrier in the OFDM symbol is -29.2-dBm

according to the WiMedia Alliance's UWB standard. The free space propagation loss of 1-cm distance for Band Group 1 UWB signal can be approximately by the loss of a 4-GHz signal, which can be simply calculated as

$$L = 20 \log_{10} (4\pi D / \lambda) = 4.5 \text{ dB} \quad (3.35)$$

This indicates that the received subcarrier power is only about -33.7-dBm when the transmitter is radiating at its maximum power level with the receiver placed only 1-cm away, let alone the other possible losses such as the multipath fading.

With a sufficient 10-dB back-off for the input-referred 1-dB compression point to ensure the signal power is within the linear region, the required ICP1 is only -23.7-dBm. Assuming an excellent 40-dBc suppression between the fundamental tone and the 3rd-order tone at the output of the LNA, the required IIP3 is only (-33.7+40/2) = -13.7-dBm. Both the ICP1 and the IIP3 specifications are quite loose when only the UWB signal itself is concerned, as is consistent with the low emission power feature of the UWB system. However, those specifications should be re-examined when the high-power interferers from the other wireless systems exist in the wireless medium as in real cases. Those high power interferers could be located quite near the UWB transmission spectrum (IEEE 802.11b/g), or even within the UWB spectrum (IEEE802.11a, WiMAX).

The challenge on the receiver linearity is pushed to its extreme while the UWB receiver is located far away from the UWB transmitter, which requires the UWB receiver to be operating at its maximum gain step, while the transmitters of the interfering signals are located near the UWB receiver. Taking 10-meters as the

maximum transmission distance for a UWB transmission system operating in Band Group 1 for instance, the free space path loss is approximately 64.5-dB, making the total power of a received OFDM symbol only about -73-dBm. On the other hand, assuming the noise figure of the receiver is 6.6-dB, the total noise power in the 528-MHz bandwidth of an OFDM symbol is approximately -80.2-dBm. The receiver is assumed to be operating with 6-dB margin above sensitivity according to the interference criteria, making the maximum allowable in-band interferer level to be about -74-dBm under the extreme condition.

Assuming two narrowband jamming signals are transmitting at their maximum allowed power level, namely, +24-dBm from 20-cm away from the Band Group 1 UWB receiver. Neglecting the frequency difference of the two 5-GHz jamming signals, the path loss is calculated to be approximately 32.5-dB, resulting in two -8.5-dBm power interferers at the antenna of the UWB receiver. Assuming the UWB antenna and preselect filter together provides 20-dB attenuation to these out-band interferers, the actual jamming signals challenging the linearity of the LNA is on the power level of -28.5-dBm. Considering the -74-dBm input-referred in-band interferer power level, we arrived at the desirable IIP3, given by

$$IIP3 = -28.5 + (-28.5 + 74)/2 = -5.8dBm \quad (3.36)$$

The requirement for the input-referred 1-dB compression point can be derived by studying the power level of the in-band interferers. For the Band Group 1 UWB receiver, the interferers from the WiMAX transmitters are among the strongest in-band jammers. Assuming a WiMAX transmitter is emitting a narrowband tone with a power level of +22-dBm at 2-m away from the UWB receiver, the interferer level at

the antenna of the UWB receiver is found to be $+22-20\log_{10}(4\pi \cdot 2/0.1) = -26\text{-dBm}$. Adding another 10-dB back-off margin to ensure that the interferer does not cause gain compression, we arrive at the desirable ICP1 of -16-dBm. The derived design targets for the IIP3 and ICP1 agree well with the well known 9.6-dB difference [26], which somehow validates the derivation process.

The input port of the LNA is desirable to be matched to 50-Ohm using all on-chip components to simplify the process of system level integration; this also allows the direct observation of the input matching quality using on-wafer probing technique without having to mount the die on to the printed circuit board (PCB) with external matching network. Single-end input architecture is preferred over the differential counterpart since a high quality wideband balun covering the ultra-wide spectrum could be difficult to implement, and the insertion loss of the balun directly adds to the noise figure of the whole receiver. Moreover, the single-end input architecture also takes advantage in terms of power consumption over the differential input architecture, which doubles the current consumption most of the time.

As discussed earlier, the output port is matched to 50-Ohm only for on-wafer probing purpose. The insertion of a wide band output buffer stage will prevent the previous stage from directly loaded by 50-Ohm while providing wideband output matching. As a rule of thumb, a return loss of 10-dB is considered to be acceptable in terms of output matching quality.

The reverse isolation is considered together with the stability of the low-noise amplifier circuit. As the impedance connected to the input and output port of the LNA

in real application is unknown and subject to change in different systems, it is desirable to design the LNA as unconditionally stable to eliminate any possibility of oscillation. A typical reverse isolation of 30-dB is sufficient to get this stability condition together with other considerations; the 30-dB reserve isolation is also a feasible target for standard CMOS process technology considering the lack of advanced substrate isolation process steps.

As discussed earlier, the group delay is not important in the WiMedia Alliance's UWB standard to the first order since the division of the total spectrum into multiple narrower bands has automatically resulted in a smaller group delay variation in each band than in the whole available spectrum.

Finally, the power consumption of the LNA will be dependent on the realization of the other specifications. Typically, higher power consumption will be needed to achieve high gain, better noise figure or sometimes better linearity. It should be ensured that all those target specifications are achieved with just enough power consumption during the design process.

Table 3.1 summarizes the target specifications of the CMOS UWB LNA to be implemented in this work. To further verify the derived target specifications of the UWB LNA, the key specifications from the UWB receiver work reported in the literature is studied and summarized in Table 3.2. It can be observed that the derived target specifications of the LNA agree well with the specifications of the reported UWB receiver, which assures that the UWB LNA development according to these specifications could fit in the UWB receiver chain properly.

Table 3.1 Target Specifications of the Proposed CMOS UWB LNA

Frequency	3.1-10.6-GHz
Forward Gain (S_{21})	>16-dB
Input Matching (S_{11})	<-10-dB
Output Matching (S_{22})	<-10-dB
Reverse Isolation (S_{12})	<-30-dB
Noise Figure (NF)	<4.0-dB in Band Group 1-2-dB higher in other Band Groups
Input-referred 1-dB Compression Point (ICP1)	-16-dBm
Input-referred 3 rd -Order Intercept Point (IIP3)	-6-dBm
Stability	unconditionally stable

Table 3.2 Summary of Key Specifications in Reported UWB Receivers

Ref	Technology	Frequency (GHz)	NF (dB)	IIP3 (dBm)	ICP1 (dBm)	Power Consumption	Comments
[47]	0.18 μ m CMOS	3.1 ~ 8.0	5.0 ~ 6.6	-5.6 ~ -2.6	n/a	19.5mA@2.3V	LNA+Mixer
[48]	0.25 μ m SiGe BiCMOS	3.1 ~ 4.8	4.5	-6	n/a	47mA@2.5V	LNA+Mixer+BB Filter
[49]	0.18 μ m CMOS	3.1 ~ 4.8 6.3 ~ 8.0	5.2 ~ 7.7	-3.5 ~ 3.3	-12.5 ~ -8	10mA@1.8V	LNA+Mixer
[50]	0.18 μ m SiGe BiCMOS	3.1 ~ 10.6	3.3 ~ 5	n/a	-41	30mA@1.8V	LNA+Mixer+LO Amp
[51]	0.13 μ m CMOS	3.0 ~ 5.0	3.6 ~ 4.1	-22/+2*	n/a	34mA@1.5V	LNA+PGA+ Mixer+BB Filter
[52]	0.25 μ m SiGe BiCMOS	3.1 ~ 10.6	5.0 ~ 10.0	n/a	-25 ~ -18	34mA@2.5V	LNA+PGA+ Mixer+BB Filter
[53]	0.18 μ m CMOS	3.1 ~ 8.0	7.0 ~ 8.1	-3.6**	-22.6 ~ -20	101mA@1.8V	LNA+ 1st Mixer+ 2nd Mixer+ LPF +VGA

*: -22-dBm for high gain setting and +2-dBm for low gain setting.

**: at low gain setting.

3.3.2 UWB LNA State-of-the-Art Architectures

Several architectures have been proposed in the literature to achieve the demanding specifications of the UWB LNA, almost all of which indicated that the trade-off between the wideband matching and noise performance was generally the most difficult problem to be solved.

The distributed amplifier (DA) architecture is acknowledged to be capable of providing gain and matching over large bandwidth [54][55][56]. A typical three-stage DA, as shown in Figure 3.14 without DC biasing, extends its attainable bandwidth by absorbing the intrinsic bandwidth limiting capacitor of the active devices (C_{gs} and C_{gd}) into the artificial transmission lines. Using a 0.18- μm CMOS technology, the DA implemented in [54] shows 7.3 ± 0.8 -dB gain over the 0.6-22-GHz band, which is more than sufficient for the 3.1-10.6-GHz UWB application.

Figure 3.14 A Simplified Schematic of the Distributed Amplifier

Although the achievable bandwidth can be quite large using the DA architecture, several drawbacks limit its application in the fully integrated CMOS UWB receiver implementation. First of all, the multiple on-chip inductors needed in this architecture occupy a quite large die area, potentially increasing the cost of the UWB receiver. More importantly, the low quality of the on-chip inductors in bulk CMOS technology

leads to the excessive parasitic resistance in the signal path, directly degrading the noise performance of the DA [54][55]. As the DA incorporates multiple branches for signal amplification, its total power consumption could be very high [56]. However, the gain of each branch is inefficiently added rather than multiplied together to obtain the total gain, the overall gain of the DA is typically less than 10-dB despite of the high power consumption. The low gain and high noise figure nature of the distributed amplifier makes it very difficult to achieve the noise figure and gain requirement for UWB LNA as listed in Table 3.1, let alone its high power consumption.

The shunt-feedback and common-gate architecture are intrinsically wideband and hence not favorable in narrowband low-noise amplifier designs, however, both find their application in the ultra-wideband LNA design [57][58][59][60][61][62].

Figure 3.15 Shunt-Feedback Architecture Variations
(a) Resistive Shunt Feedback (b) Common-Drain Feedback
(c) Resistive Shunt Feedback with Source Inductive Degeneration

Figure 3.15 shows several shunt-feedback architecture variations. The resistive shunt feedback is a simplified form of the shunt-series feedback architecture discussed earlier – without source degeneration resistor. The wideband input matching is achieved solely by the feedback resistor, which pulls the impedance looking into the input port to a level close to 50-Ohm. This architecture has been utilized for UWB

low-noise amplifier implementation on SiGe BiCMOS process technology [63][64], taking advantage of its relatively low noise and high gain performance. However, as discussed earlier, while porting this architecture to CMOS process technology, much more stringent trade-off is faced between input matching quality and noise performance. Since the input matching is achieved solely by the feedback resistor, it is practically impossible to achieve the noise and matching performance listed in Table 3.1 simultaneously.

The common-drain feedback architecture provides an alternative using the active device [33][65]. The input impedance and noise factor of this architecture are given respectively by [66] as follows.

$$Z_{IN} = \frac{1}{g_{m2}} \cdot \frac{1}{1 + g_{m1}R_L} \quad (3.37)$$

$$F = 1 + \frac{2}{3} g_{m2}R_S + \left(\frac{1}{R_L} + \frac{2}{3} g_{m1} \right) \frac{(1 + g_{m2}R_S)^2}{g_{m1}^2 R_S} \quad (3.38)$$

As can be observed from Equations (3.37) and (3.38), the direct trade-off between input matching quality and noise performance still holds its position in this active feedback architecture. The transconductance of the common drain feedback MOS transistor is desirable to be small for a lower noise figure yet to be relatively large for optimum matching. In [65], a 90-nm CMOS wideband LNA employing the common-drain feedback architecture with additional parallel RC tank in the feedback is reported; wideband high quality input matching is achieved over 0.1 to 10-GHz spectrum but the noise figure is in the range of 3.4 to 5.8-dB, as a result of the optimization for input matching. It should be noted that the LNA designs based on the

resistive and common-drain shunt feedback architectures typically occupy very small die size since no inductors are involved. This makes both architectures attractive for low-cost but medium performance wireless receivers.

This direct trade-off between input matching and noise figure can be mitigated by introducing a degeneration inductor at the source of the input MOS transistor, as shown in Figure 3.15(c). As discussed earlier, the source degeneration inductor generates a resistive part in the impedance looking into the gate of the MOS transistor, which provides a degree of design freedom other than the feedback resistor to obtain good input matching without introducing additional noise sources to the first order. The feedback resistor does not need to be very small to ensure input matching quality with the assistance of the degeneration inductor; hence the noise performance can be improved over the interested spectrum. Several pieces of work have been reported to obtain good matching and noise performance employing this architecture [57][67][68].

The common-gate input architecture shown in Figure 3.8 is another architecture that attracts research interest since its simple but excellent wideband matching characteristic [61][62][69]. As discussed earlier, the noise performance of the common-gate architecture can be improved by trading off perfect input matching to an acceptable input return loss of 10-dB. Typically, only a single MOS transistor will be used in the input stage in this architecture for better noise performance; consequently, the input stage will exhibit relatively low gain and more stages are needed to boost up the amplifier's gain. It can be observed that most common-gate LNA designs employed multiple stages to hit the target gain specification [61][62][69]. The detailed

design strategies of the common-gate architecture will be discussed later in Chapter 5 and Chapter 6, in which UWB LNA designs using this architecture are demonstrated.

The LC-ladder input architecture based on the doubly-terminated filter theory, as shown in Figure 3.16, is introduced in the design of the UWB LNA to achieve wideband input matching [70][71][72][73].

Figure 3.16 LC-Ladder Input Architecture
(a) Schematic (b) Equivalent Circuit

The beauty of the design lies in the fact that with proper selection of the design parameters, the narrow band source inductive degeneration architecture can be extended to the LC-ladder form, in which all the values of the passive components conform to that of a bandpass doubly-terminated filter, making the input impedance automatically matched to 50-Ohm within the selected -3-dB bandwidth.

Figure 3.17 Doubly-Terminated Butterworth Bandpass Filter

A 3rd-order doubly-terminated bandpass filter is shown in Figure 3.17 as well as its component values for the maximum flatness Butterworth response with -3-dB bandwidth from 3.1 to 10.6-GHz. Comparing the filter structure in Figure 3.17 with the equivalent circuit of the LC-ladder input architecture shown in Figure 3.16 (b), it is easily observed that the inductors and capacitors are connected exactly in the same manner. Consequently, the wideband input matching and the corresponding filter response can be achieved with proper selection of the LC component values as well as the geometry and biasing point of the input MOS transistor. Better than 10-dB return loss has been achieved over the full UWB bandwidth in some reported works [70][71]. However, since this architecture focuses solely on achieving the matching requirement over the wideband width, noise optimization has not been implemented. The employment of multiple inductors in the input LC-ladder introduces much parasitic resistance in the input path and this directly degrades the noise performance of the amplifier. Due to this problem, although the work based on this architecture achieved quite good noise performance on low-noise high-gain SiGe BiCMOS [71], the noise figure in the CMOS implementation of this LC-ladder input architecture was higher than 4-dB in the 3.1-10.6-GHz UWB bandwidth with the highest in-band noise figure hitting 9-dB at the high-end of the band [70]. As such, noise optimization techniques on CMOS technology still need to be studied for this architecture to meet the noise figure target for the UWB receiver.

3.4 Summary

This chapter studies the key considerations and specifications of low-noise amplifier designs for wireless receivers. The design techniques for narrow-band CMOS low-

noise amplifiers are reviewed. Based on the understanding of the key design considerations of the LNA and the specifications of the UWB receiver, the target specifications for the UWB LNA design is derived and concluded. In the last section, the state-of-the-art design architectures for CMOS UWB LNAs are reviewed.

CHAPTER 4 A Source Degenerated Shunt Feedback UWB LNA

As discussed in the Chapter 3, the source inductive degeneration input architecture has been adopted extensively in narrowband LNA designs due to its capability of achieving optimum impedance matching and near-optimum noise matching simultaneously. However, since this input architecture is originally meant for a limited bandwidth LNA design, the techniques to extend the bandwidth of this architecture need to be investigated. In this chapter, the source inductive degeneration input architecture is re-visited with the focus on its matching quality and noise performance over a wide bandwidth. Based on the useful understanding from the analysis, a wideband LNA design employing a modified source inductive degeneration architecture is proposed.

4.1 Source Inductive Degeneration Architecture – A Closer Look

Excellent matching and noise performance have been achieved simultaneously on narrowband low-noise amplifier designs based on the source inductive degeneration architecture [37][38]. However, the matching bandwidth and the noise performance of this architecture need to be examined to determine whether it is suitable for wideband LNA designs. In Figure 4.1, the conventional source inductive degeneration architecture is shown with a cascode transistor; the small signal equivalent circuit for the first stage is also given.

Figure 4.1 Conventional Source Inductive Degeneration Amplifier
(a) Schematic (b) Small-Signal Equivalent Circuit

As shown in Figure 4.1 (a), an inductor L_s is connected between the source of the input MOS transistor and ground for degeneration purpose. The inductive degeneration introduces a real part in the impedance looking into the gate of the input transistor. The gate inductor L_g is employed to resonate with the reactive part of the impedance looking into the gate of the degenerated transistor, so as to achieve pure real impedance matching to 50-Ohm at the resonant frequency. The load at the output is normally an LC network, whose impedance is denoted as Z_L in Figure 4.1 (a). A cascode MOS transistor in common-gate configuration is connected at the drain node of the input transistor, which re-uses the DC biasing current with the input transistor. The cascode stage does not contribute to the overall gain of the LNA directly; however, introducing this device does improve the design in several aspects [29]. First of all, inserting the cascode device enhances the isolation between the output load network and the input matching network, making the tuning of the two networks relatively independent. Otherwise, the two networks can interact with each other

without the cascode device due to the existence of the gate-to-drain capacitance of the input MOS transistor. Due to the same reason, this common-gate stage enhances the attenuation of the signal travelling from the output port to the input port, thus reverse isolation is improved and the low-noise amplifier becomes more unilateral and stable. Moreover, due to the low input impedance of the common-gate stage, the voltage gain of the input stage is relatively low, relaxing the influence of the Miller effect of its gate-to-drain capacitance on the input impedance. The open-drain output resistance of the cascode stage is much higher than the finite output resistance of a single input MOS transistor, potentially increases the quality factor of the load network and thus the gain. Due to the above-mentioned reasons, the cascode stage is normally employed in low-noise amplifier designs when the voltage headroom is sufficient.

The input impedance of the source inductive degeneration stage including the effects of the input MOS transistor's gate-to-drain capacitance C_{gd} can be derived according to Figure 4.1 (b) by applying a small stimulus voltage at the gate of the input MOS transistor; the derivation progress is briefed as follows.

The small signal input voltage v_{in} is related to the gate-to-source voltage of the input MOS transistor v_{gs} by

$$v_{in} = v_{gs} + Z_{L_s} \left(v_{gs} / Z_{C_{gs}} + g_m v_{gs} \right) \quad (4.1)$$

The small signal current on the gate-to-drain capacitor C_{gd} in the direction indicated by Figure 4.1 (b) can be given by

$$i_{C_{gd}} = (v_o - v_{in}) / Z_{C_{gd}} \quad (4.2)$$

where v_o is the small signal output voltage that can be expressed by

$$v_o = -Z_{CG} (i_{C_{gd}} + g_m v_{gs}) \quad (4.3)$$

In the above equations, $Z_{C_{gs}}$, $Z_{C_{gd}}$ and Z_{L_s} denote the impedance of the gate-to-source capacitance C_{gs} , the gate-to-drain capacitance C_{gd} of the input MOS transistor and the impedance of the source generation inductor L_s respectively, and Z_{CG} is the input impedance of the cascode stage serving as the load of the first stage.

From Equation (4.1), the relationship between v_{in} and v_{gs} can be explicitly derived as

$$v_{gs} = v_{in} / \left(1 + Z_{L_s} / Z_{C_{gs}} + Z_{L_s} g_m \right) \quad (4.4)$$

The relationship between the small signal input voltage and output voltage, namely the small signal voltage gain of this stage is found by substituting $i_{C_{gd}}$ and v_{gs} from Equations (4.2) and (4.4) into Equation (4.3).

$$A_v = \frac{v_o}{v_{in}} = - \frac{\frac{g_m}{1 + Z_{L_s} / Z_{C_{gs}} + Z_{L_s} g_m} - \frac{1}{Z_{C_{gd}}}}{\frac{1}{Z_{CG}} + \frac{1}{Z_{C_{gd}}}} \quad (4.5)$$

Since Z_{CG} is mainly a low resistance, it is easily seen that the existence of C_{gd} degrades the gain by both diminishing the magnitude of the numerator and enlarging the magnitude of the denominator.

With Equations (4.4) and (4.5), the resulted small signal input current can be re-written in terms of v_{in} as follows.

$$i_{in} = \frac{v_{in} - v_o}{Z_{C_{gd}}} + \frac{v_{gs}}{Z_{C_{gs}}} = \frac{Z_{C_{gs}} + Z_{L_s} + Z_{C_{gd}} + g_m Z_{C_{gs}} (Z_{L_s} + Z_{CG})}{Z_{C_{gd}} (Z_{C_{gs}} + Z_{L_s} + Z_{L_s} Z_{C_{gs}} g_m)} v_{in} \quad (4.6)$$

Consequently, the overall input impedance of the source inductive degeneration input architecture can be given by

$$\begin{aligned}
 Z_{in} &= Z_{L_g} + \frac{Z_{C_{gd}}(Z_{C_{gs}} + Z_{L_s} + Z_{L_s}Z_{C_{gs}}g_m)}{Z_{C_{gs}} + Z_{L_s} + Z_{C_{gd}} + g_mZ_{C_{gs}}(Z_{L_s} + Z_{CG})} \\
 &= sL_g + \frac{s^2L_sC_{gs} + g_msL_s + 1}{s^3L_sC_{gs}C_{gd} + s^2g_mL_sC_{gd} + s(C_{gs} + C_{gd} + g_mC_{gd}Z_{CG})}
 \end{aligned} \quad (4.7)$$

where $s=j\omega$. Since C_{gd} is relatively small to C_{gs} in modern CMOS technology, the first two terms $s^3L_sC_{gs}C_{gd}$ and $s^2g_mL_sC_{gd}$ are negligible comparing with the last term, allowing us to simplify Equation (4.7) into

$$Z_{in} = s(L_g + L_{es}) + \frac{1}{sC_{egs}} + \frac{g_mL_s}{C_{gs} + C_{gd} + g_mC_{gd}Z_{CG}} \quad (4.8)$$

where the effective source inductor L_{es} and the effective gate-to-source capacitor C_{egs} are given by

$$L_{es} = L_s \frac{C_{gs}}{C_{gd} + C_{gs} + g_mC_{gd}Z_{CG}} \quad (4.8a)$$

$$C_{egs} = C_{gd} + C_{gs} + g_mC_{gd}Z_{CG} \quad (4.8b)$$

As can be observed in Equation (4.8), the first two terms cancels at a frequency ω_0 given by

$$\omega_0 = 1/\sqrt{L_g(C_{gs} + C_{gd} + g_mC_{gd}Z_{CG}) + L_sC_{gs}} \quad (4.9)$$

and only the third term is left at ω_0 , which is a real term that can be tuned to 50-Ohm for optimum input matching.

$$Z_{in}|_{\omega=\omega_0} = \frac{g_mL_s}{C_{gs} + C_{gd} + g_mC_{gd}Z_{CG}} \quad (4.10)$$

Comparing with the input impedance expression derived neglecting the influence of the gate-to-drain capacitance C_{gd} , it is shown that the input impedance at the resonant frequency is reduced due to the Miller effect of C_{gd} . From Equation (4.9), it can be

observed that the input series resonant frequency is also lowered in real case due to the extra capacitance introduced by Miller effect at the gate of the MOS transistor.

It would be beneficial to examine the input matching bandwidth of the source inductive degeneration architecture based on the above development. Assuming the real part of the input impedance is ideally matched to 50-Ohm, the input impedance of the source inductive degeneration architecture can be re-written as

$$Z_{in} = 50 + jI \quad (4.11)$$

where I is the imaginary part in the input impedance and can be expressed by

$$I = \omega(L_g + L_{es}) - \frac{1}{\omega C_{egs}} \quad (4.12)$$

Ideally, I is negative at frequencies below ω_0 and is positive at frequencies above ω_0 .

The voltage reflection coefficient at the input port can be given as

$$\Gamma_{in} = \frac{Z_{in} - 50}{Z_{in} + 50} = \frac{jI}{100 + jI} \quad (4.13)$$

Optimum input matching is obtained at the frequency of ω_0 ; while the frequency decreases or increases from ω_0 , the input return loss degrades. At the frequency points where the input return loss is degraded to 10-dB, we have

$$S_{11} = 20\log|\Gamma_{in}| = 20\log\left|\frac{jI}{100 + jI}\right| = -10 \quad (4.14)$$

Solving Equation (4.14), we can obtain two solutions for I as follows, where the negative I_1 is corresponding for the lower boundary of the matching bandwidth and the positive I_2 is corresponding for the upper boundary.

$$I_{1,2} = \pm 33.3 \text{ Ohm} \quad (4.15)$$

Thus, the exact lower frequency boundary ω_L and upper frequency boundary ω_H for -10-dB matching bandwidth can be found by solving Equation (4.15) with Equation (4.12) and the results are given in Equations (4.16a) and (4.16b).

$$\omega_L = \frac{-33.3 + \sqrt{33.3^2 + 4(L_g + L_{es})/C_{egs}}}{2(L_g + L_{es})} \quad (4.16a)$$

$$\omega_H = \frac{33.3 + \sqrt{33.3^2 + 4(L_g + L_{es})/C_{egs}}}{2(L_g + L_{es})} \quad (4.16b)$$

So we finally arrived at an explicit expression of the -10-dB matching bandwidth for the source inductive degeneration architecture, given by

$$BW|_{S_{11} \leq -10dB} = \omega_H - \omega_L = \frac{33.3 \text{ Ohm}}{L_g + L_{es}} \quad (4.17)$$

It is interesting to find out the simple fact that to achieve a wide matching bandwidth, the sum of the gate inductor L_g and the effective source degeneration inductor L_{es} needs to be kept as small as possible. For a total inductance of 1-nH, the matching bandwidth is calculated to be 5.3-GHz, which is quite wide comparing with the bandwidth of the narrowband receivers, most of which incorporate an LNA based on this architecture. It is a direct-forward observation that to employ the source inductive degeneration architecture for design of UWB LNAs, the maximum input matching bandwidth in the 3.1 to 10.6-GHz UWB band can only be achieved when the series resonant frequency ω_0 of the input network is located at the center of the interested spectrum. A small sum of the gate and source inductance normally requires a large effective gate-to-source capacitance for the proper position of ω_0 , indicating the use of

a large input MOS transistor; this is generally welcomed since a larger transistor will provide a higher gain at the same DC biasing current to the first order.

The noise performance of the source inductive degeneration architecture also needs to be checked for wideband application. The inductors are assumed to be lossless to the first order; consequently the major noise sources in this architecture are the channel thermal noise and induced gate noise of the input MOS transistor.

Figure 4.2 Major Noise Sources in the Source Inductive Degeneration Architecture

Figure 4.2 shows the small signal equivalent circuit with all the major noise sources that contribute to the output noise current of the first stage, including the source noise, channel thermal noise and induced gate noise. Without loss of generality, Z_{gs} is used to denote the gate-to-source impedance of the MOS transistor, taking the resistive item due to the NQS effect into account. The effect of the gate-to-drain capacitance of the transistor is neglected in interest of simplicity.

The output noise current density due to the 50-Ohm source impedance can be calculated according to Figure 4.3.

Figure 4.3 Calculation of SID Stage Output Noise Current Due to Source Noise

The output noise current due to the 50-Ohm source noise v_{ns} is denoted as i_{nos} , and it can be easily derived as

$$\overline{i_{nos}} = \frac{g_m Z_{gs}}{R_s + s(L_g + L_s) + Z_{gs} + s g_m Z_{gs} L_s} \overline{v_{ns}} \quad (4.18)$$

Consequently the spectral density of the output noise current due to source noise can be given by

$$S_{nos} = \frac{\overline{i_{nos}^2}}{\Delta f} = \frac{g_m^2 |Z_{gs}|^2}{|R_s + s(L_g + L_s) + Z_{gs} + s g_m Z_{gs} L_s|^2} \cdot \frac{\overline{v_{ns}^2}}{\Delta f} \quad (4.19)$$

The output noise current due to the channel thermal noise i_{nd} can be calculated based on the small signal equivalent circuit shown in Figure 4.4.

Figure 4.4 Calculation of SID Stage Output Noise Current Due to Channel Noise

The output noise current i_{nod} due to the channel thermal noise i_{nd} can be given by

$$\overline{i_{nod}} = \frac{R_s + s(L_g + L_s) + Z_{gs}}{R_s + s(L_g + L_s) + Z_{gs} + sg_m Z_{gs} L_s} \overline{i_{nd}} \quad (4.20)$$

So the spectral density of the output noise current due to the channel thermal noise is given by

$$S_{nod} = \frac{\overline{i_{nod}^2}}{\Delta f} = \frac{\left| R_s + s(L_g + L_s) + Z_{gs} \right|^2}{\left| R_s + s(L_g + L_s) + Z_{gs} + sg_m Z_{gs} L_s \right|^2} \cdot \frac{\overline{i_{nd}^2}}{\Delta f} \quad (4.21)$$

Similarly, the output noise current due to the induced gate noise i_{ng} can be calculated based on the small signal equivalent circuit shown in Figure 4.5.

Figure 4.5 Calculation of SID Stage Output Noise Current Due to Gate Noise

The output noise current i_{nog} due to the induced gate noise i_{ng} can be given by

$$\overline{i_{nog}} = \frac{g_m Z_{gs} (R_s + sL_g + sL_s)}{R_s + s(L_g + L_s) + Z_{gs} + sg_m Z_{gs} L_s} \overline{i_{ng}} \quad (4.22)$$

So the spectral density of the output noise current due to the induced gate noise is given by

$$S_{nog} = \frac{\overline{i_{nog}^2}}{\Delta f} = \frac{\left| g_m Z_{gs} (R_s + sL_g + sL_s) \right|^2}{\left| R_s + s(L_g + L_s) + Z_{gs} + sg_m Z_{gs} L_s \right|^2} \cdot \frac{\overline{i_{ng}^2}}{\Delta f} \quad (4.23)$$

Based on the above derivations, the noise factor of the source inductive degeneration architecture can be derived by comparing the overall output noise current with the part

contributed by the 50-Ohm source alone. However, one should be especially cautious while calculating the overall noise factor since the channel thermal noise i_{nd} and the induced gate noise i_{ng} are correlated as described in Chapter 3.

$$NF = 1 + \frac{|\overline{i_{nod}} + \overline{i_{nog}}|^2}{\overline{i_{nos}^2}} = 1 + \frac{\overline{i_{nod}^2} + \overline{i_{nog}^2}}{\overline{i_{nos}^2}} + \frac{\overline{i_{nod} i_{nog}^*} + \overline{i_{nod}^* i_{nog}}}{\overline{i_{nos}^2}} \quad (4.24)$$

The second item in Equation (4.24) can be calculated directly using the results of Equation (4.19), Equation (4.21) and Equation (4.23), while the derivation for the third item is a little more complex.

According to the definition of the correlation coefficient c between the induced gate noise and the channel thermal noise and the fact that c is pure imaginary, we have

$$\begin{aligned} \overline{i_{nd}^* i_{ng}} &= c \sqrt{\overline{i_{nd}^2} \overline{i_{ng}^2}} \\ &= c \sqrt{4kT\gamma g_{d0}\Delta f \cdot 4kT\delta g_g\Delta f} \quad (4.25a) \\ &= c4kT\omega C_{gs} \sqrt{\gamma\delta/5\Delta f} \end{aligned}$$

$$\overline{i_{nd} i_{ng}^*} = -c4kT\omega C_{gs} \sqrt{\gamma\delta/5\Delta f} \quad (4.25b)$$

So we can calculate the numerator of the third item in Equation (4.24) as

$$\begin{aligned} \overline{i_{nod} i_{nog}^*} + \overline{i_{nod}^* i_{nog}} &= \frac{|R_s + s(L_g + L_s)|^2 \operatorname{Re}(c \cdot Z_{gs})}{|R_s + s(L_g + L_s) + Z_{gs} + sg_m Z_{gs} L_s|^2} 8kT\omega C_{gs} g_m \sqrt{\gamma\delta/5\Delta f} \\ &\quad + \frac{|Z_{gs}|^2 (L_g + L_s) \operatorname{Re}(c \cdot s)}{|R_s + s(L_g + L_s) + Z_{gs} + sg_m Z_{gs} L_s|^2} 8kT\omega C_{gs} g_m \sqrt{\gamma\delta/5\Delta f} \end{aligned} \quad (4.26)$$

Finally, the overall noise factor expression is given as

$$NF = 1 + \frac{\gamma}{\alpha g_m R_s} \left| \frac{R_s + s(L_g + L_s)}{Z_{gs}} + 1 \right|^2 + \frac{\alpha \delta \omega^2 C_{gs}^2}{5 g_m R_s} |R_s + s(L_g + L_s)|^2 \quad (4.27)$$

$$\frac{2\omega C_{gs} \sqrt{\gamma \delta / 5}}{g_m R_s |Z_{gs}|^2} \left[|R_s + s(L_g + L_s)|^2 \operatorname{Re}(c \cdot Z_{gs}) + |Z_{gs}|^2 (L_g + L_s) \operatorname{Re}(c \cdot s) \right]$$

In Equation (4.27), the second term is contributed by the channel thermal noise; the third term is contributed by the induced gate noise while the last term arises due to the correlation of the two noise sources.

To acquire a direct-forward observation of Equation (4.27) derived above, the noise factor is studied at the series resonant frequency of the input network ω_0 , assuming Z_{gs} is dominated by the gate-to-source capacitor at the interested frequencies.

$$NF|_{\omega=\omega_0} = 1 + \frac{\gamma R_s \omega_0^2 C_{gs}^2}{\alpha g_m} + \frac{\alpha \delta (1 + \omega_0^2 C_{gs}^2 R_s^2)}{5 g_m R_s} - \frac{2|c| R_s \omega_0^2 C_{gs}^2 \sqrt{\gamma \delta / 5}}{g_m} \quad (4.28)$$

In Equation (4.28), the second term is due to the channel thermal noise and the third term is contributed by the induced gate noise; the fourth term can be viewed as a correction to the sum of the second and third terms since they are partially correlated. R_s is the standard 50-Ohm source impedance; α , γ , δ and c are process parameters beyond designer's control. As discussed in the previous section, ω_0 needs to be set to center of the interested spectrum for maximum matching bandwidth. This leaves the width and the biasing condition of the active device the only design freedom for optimum noise performance, since minimum available gate length is always used in RF LNA designs for best performance.

Since $C_{gs}=2C_{ox}WL/3$ and $g_m=(2\mu_nC_{ox}W/LI_D)^{1/2}$, Equation (4.28) can re-written as follows to reflect the dependence of the overall noise factor on the device gate width W and its biasing current I_D .

$$\begin{aligned} NF|_{\omega=\omega_0} &= 1 + \eta R_s \omega_0^2 \frac{C_{gs}^2}{g_m} + \frac{\alpha \delta}{5 g_m R_s} \\ &= 1 + \frac{2\sqrt{2}}{9} \eta R_s \omega_0^2 \mu_n^{-\frac{1}{2}} C_{ox}^{\frac{3}{2}} L^{\frac{5}{2}} I_D^{-\frac{1}{2}} W^{\frac{3}{2}} + \frac{\alpha \delta}{5\sqrt{2}R_s} \mu_n^{-\frac{1}{2}} C_{ox}^{\frac{1}{2}} L^{\frac{1}{2}} I_D^{-\frac{1}{2}} W^{-\frac{1}{2}} \end{aligned} \quad (4.29)$$

where the coefficient η is given by

$$\eta = \left(\frac{\gamma}{\alpha} + \frac{\alpha \delta}{5} - 2|c|\sqrt{\gamma \delta / 5} \right) \quad (4.30)$$

Using the long channel device parameters, namely $\alpha=1$, $\gamma=2/3$, $\delta=4/3$ and $c=-0.395j$, η is approximately 0.61; η will become larger in short channel devices where α and $|c|$ decrease while γ and δ increase [22][25].

A biasing independent optimum device width for minimum noise figure can be derived based on Equation (4.29) and the optimum W can be given by

$$W = \sqrt{\frac{3\alpha\delta}{20\eta}} \cdot \frac{1}{R_s \omega_0 C_{ox} L} \quad (4.31)$$

Equation (4.31) offers a direct way to estimate the device width for optimum noise figure at the series resonant frequency of the input network ω_0 . In real design practice, the optimum W needs to be adjusted according to simulation predictions. This is because in LNA designs with short channel devices, the process parameter α , γ , δ , c and hence η will deviate from the classical theoretical values of long channel devices due to various effects happening in the short channel regime, where the values are more process dependent and difficult to extract accurately [22]. However, it is

important to understand that a biasing-independent optimum device width does exist for minimum noise figure of the low-noise amplifier at the center of the interested frequency spectrum, which generally leads to a minimum average noise figure over the whole bandwidth.

4.2 Design of a Source Inductive Degenerated Shunt Feedback UWB LNA

Based on the understanding of the principles in applying the source inductive degeneration architecture for wideband low-noise amplifier design in the previous section, a UWB LNA design is proposed in this section.

The previous discussion has been focusing on the feasibility of adopting the source inductive degeneration architecture as the wideband matched low noise input stage, yet a wideband load has to be designed to ensure that relatively flat gain is achieved over the interested spectrum. Traditionally, a single inductor or a resistor is connected between the drain of the output transistor and the supply voltage, serving as the load of the low-noise amplifier, as shown in Figure 4.6. The parallel capacitance C_L represents the sum of the total parasitic capacitance of the active and passive components at the output transistor's drain node and a real shunt capacitor possibly employed in the design for frequency response tuning purpose.

Figure 4.6 Conventional Load Types for the LNA Output Stage

(a) Inductive Load (b) Resistive Load (c) Shunt Inductive Peaking

The impedance of the L_L and C_L parallel network can be easily given by

$$Z_{L1} = \frac{j\omega L_L}{1 - \omega^2 L_L C_L} \quad (4.32)$$

According to Equation (4.23), the load impedance approached infinity when the frequency approaches the parallel resonant frequency of the LC network $\omega_0 = (L_L C_L)^{-1/2}$. However, since the real inductors and capacitors have limited quality factors, the overall parallel network has a quality factor Q_p as given below, where Q_L and Q_C are the quality factors of L_L and C_L respectively.

$$Q_p^{-1} = Q_L^{-1} + Q_C^{-1} \quad (4.33)$$

Normally, the quality factor of the inductors in standard bulk CMOS falls below 15, making it dominant in the overall quality factor of the parallel LC network. Due to the limited quality of the parallel resonance, the impedance of the L_L and C_L parallel network is equivalent to a finite resistance R_p at ω_0 , which can be given by

$$R_p = Q_p \omega_0 L_L = \frac{Q_p}{\omega_0 C_L} \quad (4.34)$$

The two poles in Equation (4.32) limit the -3-dB bandwidth of the parallel resonant network to [27]

$$BW|_{-3dB} = \frac{1}{2\pi} \cdot \frac{\omega_0}{Q_p} \quad (4.35)$$

To get as wide bandwidth as possible for UWB application, the resonant frequency should be chosen to be located at center of the interested spectrum, namely, around 6.8-GHz, resulting in a -3-dB bandwidth of less than 1.4-GHz assuming the overall quality factor is 5. Obviously, the parallel LC resonant network utilized extensively in narrowband low-noise amplifier designs is incapable of accomplishing the bandwidth requirement of a UWB low-noise amplifier.

In Figure 4.6(b), the impedance of the parallel combination of R_L and C_L can be simply given as

$$Z_{L2} = \frac{R_L}{1 + j\omega R_L C_L} \quad (4.36)$$

It is obvious that the resistive load is an inherently wideband load, however, the existence of the parallel capacitance makes the load a low-pass one and limits the highest achievable bandwidth.

The low-pass corner frequency of the R_L and C_L parallel network can be given as

$$BW|_{-3dB} = \frac{1}{2\pi} \cdot \frac{1}{R_L C_L} \quad (4.37)$$

Assuming the total parallel capacitance is 500-fF at the drain of the output transistor, including the input capacitance of the next stage, and R_L is 50-Ohm, the -3-dB low-pass corner frequency is around 6.4-GHz, still several GHz short to hit the 10.6-GHz upper boundary for UWB application. It is easy to observe that the capacitance at the drain node is of great important to the achievable bandwidth for this type of load because the load resistor R_L has little room for decreasing as it directly relates to the gain of the amplifier. Hence, it is always desirable to use a small active device as the cascode stage and similarly, the dimension of the input MOS transistor of the next stage is desirable to be small to reduce the total shunt capacitance that limits the bandwidth.

Figure 4.6(c) shows the shunt-inductive peaking technique to extend the gain bandwidth. The impedance of the shunt-inductive peaking network can be given as

$$Z_{L3} = \frac{R_L + j\omega L_L}{1 - \omega^2 L_L C_L + j\omega R_L C_L} \quad (4.38)$$

It can be seen that the introduction of the peaking inductor introduces a zero in the impedance of the load network, which compensates the poles and peaks the gain at high frequencies. The location of the zero is generally determined by the inductance of L_L , since not much freedom is available for R_L considering the overall gain. As such, it now becomes clear that to achieve wide gain bandwidth, the overall shunt capacitance at the drain node of the output MOS transistor needs to be designed as small as possible to push the pole higher while the peaking inductance needs to be selected carefully to compensate the pole of the load as well as the intrinsic gain degradation of the active device for maximum bandwidth.

In this way, a wideband load is designed for the wideband low-noise amplifier, which has several advantages for integration with the modern CMOS process technology. First of all, to peak the load impedance at high frequencies, the inductance of L_L is relatively small. This makes it suitable to be implemented in CMOS technology, in which large inductance normally means large area consumption and low self resonant frequency. Moreover, the peaking inductor L_L needs to be connected in series with the load resistor R_L , which indicates that the quality factor required for the inductor is much relaxed comparing with the inductors required in the narrowband designs. This fits the technology capability of the CMOS process, in which the inductors have relatively low quality factor.

Based on the above discussion on the wideband input matching and output load design techniques, a wideband low-noise amplifier incorporating source inductive degeneration with feedback technique, shorted as the SIDFB UWB LNA, is proposed as shown in Figure 4.7. A source inductor L_s is employed to generate the desirable 50-Ohm real part in the input impedance and a gate inductor L_g is employed to tune the series resonant frequency ω_0 of the input network to be around the center of the wide frequency spectrum for maximum matching bandwidth and best average noise figure. The L_s and L_g should be chosen to be as small as possible to extend the matching bandwidth as concluded in the previous section; small inductance also ensures the noise contributed by the series parasitic resistance of the inductor is minimized.

Figure 4.7 Proposed SIDFB UWB LNA

A cascode device is introduced mainly to mitigate the Miller effect and enhance reverse isolation. To minimize the total capacitance at the output node, a smaller MOS transistor is chosen while ensuring the reduction in the width of the transistor does not jeopardize the gain and noise performance of the amplifier according to the prediction of the circuit simulator.

A center-tapped inductor is employed in series with a resistor to serve as the load. The combination of the inductor L_L and the resistor R_L , as well as the total capacitance at the drain of the cascode transistor, forms the shunt-inductive peaking wideband load network as discussed earlier. The gain bandwidth of the amplifier can be extended by carefully selecting the value of the load resistor, inductor and the cascode transistor.

A resistive feedback path is introduced to further improve the matching and gain bandwidth, with a series capacitor to block the DC level from tangling. Unlike the

conventional way to tap the feedback path directly from the output node, this design taps the feedback path from the center-tap of the inductor, the advantages of which are discussed as follows. The simplified small signal equivalent circuit of the proposed SIDFB low-noise amplifier design is shown in Figure 4.8. The gate-to-drain parasitic capacitance and the finite output resistance of the MOS transistor are neglected in favor of simplicity. The half inductance of the center-tapped inductor is denoted as L_h and the mutual inductance is denoted as $-M$.

Figure 4.8 Small Signal Equivalent Circuit of the Proposed LNA Design

Through complicated derivation, the voltage gain from the gate of the input device to the drain of the output device can be given as

$$A_v = \frac{(R_L + j\omega L_h) \left[1 - \omega^2 L_s C_{gs} + jg_{m1}\omega(L_s - L_h) - \frac{g_{m1}R_L - \omega^2 L_h C_{gs} + 2jg_{m1}\omega L_h + j\omega C_{gs} R_L}{R_L + j\omega L_h} Z_f \right]}{(R_L + Z_f + j\omega L_h)(1 - \omega^2 L_s C_{gs} + jg_{m1}\omega L_s)} \quad (4.39)$$

And the overall input impedance can be given as

$$Z_{in} = \frac{1}{\frac{g_{m1} + j\omega C_{gs}}{R_L + j\omega L_h} + \frac{1 - \omega^2 L_s C_{gs} + jg_{m1}\omega(L_s - L_h) - \frac{g_{m1}R_L - \omega^2 L_h C_{gs} + 2jg_{m1}\omega L_h + j\omega C_{gs}R_L}{R_L + j\omega L_h} Z_f}{1 - \omega^2 L_s C_{gs} + jg_{m1}\omega L_s} + j\omega L_g} \quad (4.40)$$

In Equations (4.39) and (4.40), Z_f is employed to denote the overall impedance of the resistor R_f , capacitor C_f and mutual inductance M in the shunt feedback path, which can be given as

$$Z_f = R_f - j \left(\frac{1}{\omega C_f} + \omega M \right) \quad (4.41)$$

It would be difficult to get insight of the merit of this feedback technique by observing these equations. However, intuitive analysis can be done based on observing the impedance of the feedback path. The overall impedance in the feedback loop is the series combination of L_h and Z_f ; according to Miller's theorem, it is equivalent to a shunt impedance of $(1-A_v)$ times larger at the input port, where A_v is the gain of the amplifier. While employing a small capacitance for C_f , this overall impedance is capacitive at lower frequency but is tuned out by the inductive portion toward higher frequency, leaving only the resistive part. This provides a leverage to improve the matching quality at low frequencies while keeping the matching quality at high frequencies relatively unaffected. It can be found that by introducing this feedback path, the input impedance can be better matched to 50-Ohm because of the equivalent shunt path due to the Miller effect. Since the feedback path is tapped only at center of the output load and the resistor is chosen to be relatively high, the overall gain of the low-noise amplifier is not much affected by the introduction of the feedback. As

simulation shows, the unconditional stability of the amplifier still stands. Overall, this center-tap feedback technique introduces an inductive part in the feedback path for reliable matching without consuming additional silicon area or DC power.

A source follower is introduced to serve as the output buffer, which isolates the 50-Ohm load of the measurement equipments from directly loading the LNA core stage. In an integrated receiver, normally the LNA core stage is directly followed by a mixer stage without any buffer to reduce the power consumption. The input impedance of the mixer stage is normally purely capacitive and this is well taken into account in the proposed design since the input capacitance of the source follower is loaded on to the core stage's output, exactly in the same way as the mixer in an integrated receiver. The input capacitance of the source follower is about 35-fF, which represents the driving capability of the core stage of the proposed SIDFB LNA design and dictates the total input capacitance tolerable for the mixer stage while dropping the LNA core stage into an integrated receiver.

Figure 4.9 Voltage Attenuation of the Output Buffer Stage in Schematic and Extracted Simulation

The source follower stage has some voltage attenuation as shown in Figure 4.9, where the attenuations in schematic and extracted simulations are plotted and compared. The output buffer has relatively flat voltage attenuation across the interested frequency spectrum as indicated by schematic simulation; however, with the effect of the parasitic resistance and capacitance extracted and included in the extracted simulation, the voltage attenuation tends to increase slightly toward higher frequency. This loss needs to be de-embedded from the gain obtained from measurement since the source follower stage is only for measurement purpose and is not included in the integrated solution.

In the schematic shown in Figure 4.7, all the three MOS transistors in the RF signal path, namely M_1 , M_2 and M_3 , adopt the minimum channel length available in the process technology for highest transit frequency possible. The width of transistor M_1 is selected to be relatively large so that the transistor has a high transconductance at a given biasing current to overcome the noise contributed by the following stages. L_s is selected so that the real part of the input impedance is around 50-Ohm, while L_g is selected to ensure that the optimum matching frequency is located at the center of the interested band. A moderate width is chosen for the cascode device since a large device will introduce excessive parasitic capacitance to the load while a small device will reduce the overall gain. Due to the same reason, M_3 in the output buffer adopts a moderate width and it is co-simulated with the dimension of transistor M_4 for acceptable output matching. The center-tapped load inductor of the cascode stage L_L has been co-simulated with the feedback network to obtain maximum gain and matching bandwidth over the interested spectrum. The serial resistor R_L in the load is

considered together with the parasitic resistance of the power traces so that the total resistance is just sufficient to achieve the desired bandwidth. Extensive simulation has been carried out to find out the optimum device values for the given architecture and their optimum biasing conditions based on the device models provided in the process design kit and Table 4.1 summarizes the final device values decided for the design.

Table 4.1 Device Values for the Proposed SIDFB UWB LNA

Designation	Value
M_1	240- μm /0.18- μm
M_2	96- μm /0.18- μm
M_3	72- μm /0.18- μm
M_4	60- μm /0.35- μm
L_g	1.16-nH
L_s	0.31-nH
L_L	1.91-nH
C_f	150-fF
R_f	0.98-KOhm
R_L	53-Ohm
R_{b1}, R_{b2}	20-KOhm
C_{b1}, C_{b2}	6.0-pF

The supply voltage for the low-noise amplifier is set to 1.8-V, which is standard for a 0.18- μm CMOS technology. The gate biasing voltage VB1 directly sets the biasing current for the first stage, which determines the overall noise figure, input matching and linearity of the proposed design. VB2 directly sets the biasing current of the output buffer stage. According to final simulation results, VB1 and VB2 are set to 0.62-V and 0.82-V respectively, which directly set the DC biasing current of the LNA core stage to 4.8-mA and that of the buffer stage to 4.2-mA.

The performance of the circuit constructed by devices listed in Table 4.1 under this biasing condition is described below. The input matching conditions with and without the feedback path are compared in Figure 4.10.

(a)

(b)

Figure 4.10 Simulated Input Matching Quality of the Source Inductive Degeneration Architecture with and without the Feedback Path
(a) S_{11} in Magnitude (a) S_{11} in Smith Chart

It can be seen that by choosing small L_g and L_s , the -10-dB matching bandwidth of the source inductive degeneration input architecture reaches more than 5-GHz while the input series network resonates around 7-GHz. This correlates well with the matching

bandwidth predicted by Equation (4.17). Introducing the feedback path further improves the matching quality at low frequencies while keeping the matching quality at high frequencies unaffected. As shown in Figure 4.10, the -10-dB matching bandwidth in schematic simulation extends from 3.6 to 10.6-GHz, covering almost the whole UWB spectrum. Although not meeting the -10-dB criterion, S_{11} is still better than -8.5-dB in the 3.1 to 3.6-GHz frequency range.

The gain of the proposed LNA design in schematic simulation is shown in Figure 4.11. The gain of the two-stage amplifier is around 10-dB at low frequencies and is peaked up to 12-dB by the load inductor at about 8-GHz. Given the 6.3-dB attenuation of the output buffer stage, the core stage has about 16.3-dB to 18.3-dB gain. The 3-dB bandwidth of the amplifier extends from 2 to 9.8-GHz as shown, covering 7800-MHz spectrum.

Figure 4.11 Simulated Forward Gain of the SIDFB UWB LNA

High quality output matching is easy to achieve due to the intrinsic wideband matching nature of the source follower. High biasing current is used in the output buffer stage to minimize its attenuation. At the same time, high biasing current improves the linearity of the buffer stage, so that the overall linearity of the LNA is not noticeably limited by the buffer stage and the measurement results truly indicate the linearity of the LNA core stage. Consequently, the biasing current is increased so that S_{22} is only slightly better than -10-dB over the interested spectrum. The quality of the output matching is shown in Figure 4.12.

Figure 4.12 Simulated Output Matching Quality of the SIDFB UWB LNA

Due to the adoption of the cascode stage and the output buffer, good reverse isolation is automatically achieved as shown in Figure 4.13.

Figure 4.13 Simulated Reverse Isolation of the SIDFB UWB LNA

Figure 4.14 shows the 50-Ohm noise figure of the proposed LNA design and the minimum achievable noise figure under noise optimum source impedance condition. It can be observed that the noise figure increases monotonically with frequency, as predicted by Equation (4.28). At the series resonant frequency ω_0 of the input network, the 50-Ohm noise figure is very close to the optimum noise figure and the discrepancy between the two increases as the frequency offset from ω_0 increases. In the schematic simulation, the noise figure of the proposed LNA is 2.25-dB at 2-GHz and increases to 5.3-dB at 10.6-GHz, whose average is about 3.7-dB over the interested spectrum.

Figure 4.14 Simulated 50-Ohm and Minimum Noise Figure of the SIDFB UWB LNA

The linearity of the proposed LNA is examined by simulating both the 1-dB compression point and the 3rd-order intercept point. The input-referred 1-dB compression point at 3.5-GHz is predicted to be -11.6-dBm as shown in Figure 4.15. The two tones for 3rd-order intercept point simulation are set to 3.2-GHz and 3.3-GHz so as to make sure the result can be compared with the experimental result since one of the available signal generators can only provide single tone output up to 3.2-GHz. As shown in Figure 4.16, the input-referred 3rd-order intercept point is -2.4-dBm.

Figure 4.15 Simulated ICP1 of the SIDFB UWB LNA

Figure 4.16 Simulated IIP3 of the SIDFB UWB LNA

The stability of the core stage is also examined in schematic simulation. As shown in Figure 4.17, the K factor is well above unity and $|\Delta|$ is well below unity according to schematic simulation on the core stage of the proposed LNA design, suggesting the design is unconditionally stable.

(a)

(b)

Figure 4.17 Simulated Stability of the SIDFB LNA
(a) K Factor (b) $|\Delta|$

The group delay of the proposed amplifier is also checked in schematic simulation, which reports the group delay falls in the 66 ± 20 -ps range in the 3.1-10.6-GHz band as shown in Figure 4.18. Since the WiMedia Alliance's UWB standard utilizes the UWB spectrum in a multi-band manner, the group delay variation is even less in each 528-

MHz band, ensuring that the signal distortion contributed by the group delay is minimum.

Figure 4.18 Simulated Group Delay of the SIDFB UWB LNA

4.3 Post-Layout Simulation and Experimental Results

The proposed ultra-wideband low-noise amplifier is designed on GLOBALFOUNDRIES 0.18- μm 1P6M RF CMOS process technology. While the schematic of the proposed SIDFB UWB LNA design has been completed, the layout of the design is drawn with the corresponding device layout patterns provided by the process design kit. The complete layout of the proposed SIDFB UWB LNA design is shown in Figure 4.19.

Figure 4.19 Layout of the Proposed SIDFB UWB LNA

The circuit components of the proposed LNA are laid out in a 0.5-mm*1.0-mm rectangle. Ground-Signal-Ground (GSG) pad for the RF input port is placed at the left guard ring while the GSG pad for the RF output port is placed at the right guard ring. In this way, the unwanted coupling between the input and output ports are minimized. The voltage supply is located in the middle of the lower guard ring and supply voltage is delivered to the active circuits located at the center with a wide top metal to minimize the voltage drop on the supply line. Decoupling capacitors have been added along the supply line to bypass all high frequency interferers to the supply. The ground pad is placed close to the ground connection of the degeneration inductor. This is because any resistance introduced by the trace between the inductor terminal and ground influences the degeneration in an undesirable way that could cause impedance mismatch as well as higher noise figure. The gate biasing pads are placed at the upper guard ring; VB1 can also be applied through the RF input port using a bias-tee network, providing certain flexibility in the measurement setup. Local guard ring is

placed surrounding the active area in the center of the layout, which isolates the transistors from the external noisy substrate for better noise performance.

The parasitic effects are extracted after the layout is drawn and simulation with these extracted parasitic effects has been performed to identify their influence on the key specifications of the design. After indentifying the dominant parasitic components, the layout is modified to minimize their influence and the circuit device values are adjusted when necessary. After several iterations until the extracted simulation results are satisfactory, the design is finalized and delivered for fabrication. Figure 4.20 shows the die micro-photo of the fabricated design with all the probes touching the corresponding pad for measurement.

Figure 4.20 Micro-Photo of the Fabricated SIDFB UWB LNA

The measurement of the fabricated circuit is performed on Cascade Microtech's probe station using Cascade GSG-100 probes to establish reliable contacts between the RF ports of the integrated circuit and the measurement equipments. Appendix B details the measurement setups to characterize the performance of the fabricated design. The

LNA is measured with a supply voltage of 1.8-V; due to parasitic resistances, the gate biasing voltages VB1 and VB2 are slightly higher than simulated to make sure that the LNA core stage consumes 4.8-mA current and the output buffer stage consumes 4.2-mA current as simulated. The experimental results of the fabricated circuit are described as follows and the results from the extracted simulation are compared with.

The measured forward gain of the proposed SIDFB UWB LNA design is shown in Figure 4.21, where the forward gain curve in the extracted simulation is also plotted.

Figure 4.21 Measured and Simulated Forward Gain of the SIDFB UWB LNA

It can be observed that the measured forward gain of the low-noise amplifier design agrees well with the extracted simulation result at low frequencies. However, the discrepancy between the extracted simulation and measurement results increases toward higher frequency. This phenomenon is mainly caused by the underestimation of the total parasitic capacitance at the drain node of the cascode device, which directly leads to the down-shift of the inductive peaking frequency. The forward gain of the LNA core stage, derived by de-embedding the attenuation of the output buffer

stage according to its extracted simulation result, is shown in Figure 4.22. The -3-dB bandwidth of the low-noise amplifier's core stage is 2.0 to 8.0-GHz.

Figure 4.22 Measured and De-Embedded Gain of the SIDFB UWB LNA

The measured input matching quality is compared with the extracted simulation result in Figure 4.23. As shown, although the measured S_{11} agrees quite well with the extracted simulation result at low frequencies, the down-shift of the inductive peaking frequency also drags down the upper limit of the input -10-dB matching bandwidth. According to the measurement result, the -10-dB matching bandwidth is between 3.6 to 8.4-GHz, covering almost 5-GHz. The matching quality degrades gradually outside this bandwidth; however, the degradation is still acceptable since the measured S_{11} is better than -8-dB at 3.1-GHz.

Figure 4.23 Measured and Simulated Input Matching of the SIDFB UWB LNA

The measured output matching quality and reverse isolation are compared with their respective extracted simulation results in Figure 4.24 and Figure 4.25. The measured S_{22} is better than -12-dB from 2 to 10-GHz and the measured S_{12} is better than -45-dB in the interested frequency band.

Figure 4.24 Measured and Simulated Output Matching of the SIDFB UWB LNA

Figure 4.25 Measured and Simulated Reserve Isolation of the SIDFB UWB LNA

The measured noise figure of the fabricated design is shown below in dots with the noise figure predicted in the extracted simulation for comparison in Figure 4.26.

Figure 4.26 Measured and Simulated Noise Figure of the SIDFB UWB LNA

It can be seen that the measured noise figure is only less than 2-dB below 3-GHz and it increases gradually with frequency. At high frequencies, the noise figure increases faster than simulated. This is because the output noise contributed by the induced gate

noise increases proportional to the 2nd order of frequency as indicated by Equation (4.27); nevertheless, the MOS transistor model employed in the process design kit is based on BSIM3V3 model, which does not explicitly model the induced gate noise. At the upper boundary of -3-dB gain bandwidth, i.e., 8.0-GHz, the noise figure is still better than 5-dB.

The 1-dB compression point and the 3rd-order intercept point are also measured to verify the linearity of the fabricated LNA. The measurement results are shown in Figure 4.27 and Figure 4.28.

Figure 4.27 Measured ICP1 of the SIDFB UWB LNA

Figure 4.28 Measured IIP3 of the SIDFB UWB LNA

The 1-dB compression point is measured at 3.5-GHz, which is in the Band Group 1 of the WiMedia Alliance's UWB standard. As shown in Figure 4.27, the input-referred 1-dB compression point is measured to be -12.7-dBm. The 3rd-order intercept point is measured by injecting two testing tones at frequencies of 3.2-GHz and 3.204125-GHz, where the 4.125-MHz spacing is determined according to the spacing of two subcarriers in the WiMedia Alliance's UWB OFDM symbol. The measured output power values of the fundamental signal and 3rd-order inter-modulation (IM3) product are plotted in Figure 4.28 and the extrapolated input-referred 3rd-order intercept point is -2.2-dBm at 3.2-GHz. Both the measured input-referred 1-dB compression point and 3rd-order intercept point of the fabricated design agree quite well with the simulation results.

4.4 Summary

This chapter proposes a CMOS ultra-wideband low-noise amplifier design based on the classical source inductive degeneration architecture. Novel techniques to extend the matching and gain bandwidth for the conventional architecture have been proposed. The noise performance of the amplifier over a wide bandwidth is also studied. The proposed design is fabricated and verified by on-wafer probing method. The measured specifications of the proposed design are summarized in Table 4.2. The measurement results validate this proposed architecture for application with ultra-wideband low-noise amplifier design.

Table 4.2 Summary of Measured Specifications of the Proposed SIDFB UWB LNA

Supply Voltage	1.8-V
Current Consumption	4.8-mA (excluding 4.2-mA for testing only)
Gain Bandwidth	2.0-GHz ~ 8.0-GHz
Forward Gain (S_{21})	14.5-dB ~ 17.5-dB
Input Matching (S_{11})	<-8-dB (<-10-dB in 3.6-GHz ~ 8.4-GHz)
Output Matching (S_{22})	<-12-dB
Reverse Isolation (S_{12})	<-45-dB
Noise Figure	1.8-dB ~ 4.7-dB
ICP1	-12.7-dBm
IIP3	-2.2-dBm

CHAPTER 5 Design of a Two-Stage Staggering-Tuning UWB LNA

The common-gate input architecture is widely known for its active $1/g_m$ impedance termination, which offers a good chance to achieve high quality wideband input matching without the introduction of other complicated passive networks. However, the common-gate input architecture is also found to be noisier than its common-source counterpart, limiting its application as the first stage of a low-noise amplifier. In this chapter, the conventional common-gate architecture is studied with emphasis on the trade-off between the matching bandwidth and the noise performance. A common-gate two-stage staggering-tuning UWB low-noise amplifier, shorted as the CG2SST UWB LNA, is proposed based on the analysis of this input architecture. Experimental results of the proposed design are reported and discussed.

5.1 Detailed Analysis on the Common-Gate Input Architecture

The common-gate input architecture has been adopted for low-noise amplifier design only in very limited narrowband wireless receiver cases [32]. This is generally because of its relatively poorer noise performance comparing with its common-source counterpart as discussed in Chapter 3, while the intrinsic wideband feature of the common-gate input architecture is not so favorable in narrowband LNA designs. However, since wideband matching becomes a key design consideration for an ultra-wideband low-noise amplifier, the common-gate input architecture needs to be re-examined for its capability of meeting the matching bandwidth as well as the other specifications of the UWB LNA.

Figure 5.1 shows the typical configuration of a common-gate input stage and its small-signal equivalent circuit. The gate of the input MOS transistor is directly connected to a biasing voltage, which determines its transconductance to the first order. The source terminal of the MOS transistor is connected to ground through an inductor, which provides a DC path but exhibits high impedance to the incoming signal at the operation frequency and avoids signal leakage to ground. Typically, only a single transistor is employed in the common-gate architecture since the additional noise sources brought by more active devices will degrade the noise performance of the input stage substantially due to the relatively low gain of the common-gate stage. The overall load of the common-gate stage, including the input impedance of the next stage, is denoted as Z_L in the schematic. Normally, inductive load is used for the common-gate stage due to noise consideration.

Figure 5.1 Typical Common-Gate Input Architecture
(a) Schematic (b) Small-Signal Equivalent Circuit

The input impedance of the common-gate input architecture considering the effect of the MOS transistor's finite output resistance R_o can be calculated based on its small-signal equivalent circuit shown in Figure 5.1(b). The gate-to-drain parasitic

capacitance of the MOS transistor is in parallel with the load of the stage and is thus absorbed in Z_L .

It is clear that the input impedance consists of the parallel combination of the source inductor L_s , gate-to-source capacitor C_{gs} and the total impedance looking toward the drain of the MOS transistor Z_d . While the impedance of L_s and C_{gs} can be written directly, Z_d can be calculated as follows.

Since $v_{gs} = -v_{in}$, we have

$$i_d = g_m v_{gs} = -g_m v_{in} \quad (5.1)$$

So the voltage at the output node v_o can be written as

$$v_o = -Z_L \left(-g_m v_{in} + \frac{v_o - v_{in}}{R_o} \right) \quad (5.2)$$

Solving Equation (5.2), the voltage gain of the common-gate stage is found to be

$$A_v = \frac{v_o}{v_{in}} = \frac{Z_L (g_m R_o + 1)}{Z_L + R_o} \quad (5.3)$$

Consequently, the impedance looking toward the drain of the MOS transistor can be expressed as

$$Z_d = \frac{v_{in}}{-i_d + (v_{in} - v_o)/R_o} = \frac{1}{g_m - \frac{Z_L g_m - 1}{Z_L + R_o}} \quad (5.4)$$

As can be observed in Equation (5.4), the effective transconductance of the transistor in common-gate configuration is reduced due to the finite output resistance of the MOS transistor.

So the input impedance and admittance of the common-gate input architecture can be given by

$$Z_{in} = sL_s \parallel \frac{1}{sC_{gs}} \parallel Z_d \quad (5.5a)$$

$$\begin{aligned} Y_{in} &= sC_{gs} + \frac{1}{sL_s} + \frac{1}{Z_d} \\ &= sC_{gs} + \frac{1}{sL_s} + g_m - \frac{Z_L g_m - 1}{Z_L + R_o} \end{aligned} \quad (5.5b)$$

It can be seen that the output load impedance affects the input admittance due to the finite output resistance of the MOS transistor. Assuming the MOS transistor's output resistance R_o is large comparing to the load Z_L , Equation (5.5b) can be simplified into

$$Y_{in} = sC_{gs} + \frac{1}{sL_s} + g_m \quad (5.6)$$

According to Equation (5.6), while the real term is 20-mS, optimum matching is achieved at the frequency ω_0 where the inductive and capacitive parts are tuned out.

$$Y_{in} \big|_{\omega=\omega_0} = g_m \quad (5.7)$$

As the frequencies deviate from this optimum matching frequency ω_0 , the matching quality degrades as the susceptance plays important roles in the overall admittance. It is beneficial to examine the matching bandwidth of the common-gate input architecture based on the above development. To simplify the analysis, it is assumed that the conductance in the input admittance is ideally matched to 20-mS. Thus the input admittance can be simply written as

$$Y_{in} = 0.02 + jB \quad (5.8)$$

where B is the overall susceptance in the input admittance of the common-gate input architecture. The voltage reflection coefficient at the input port can be given as

$$\Gamma_{in} = \frac{Z_{in} - 50}{Z_{in} + 50} = \frac{1 - 50Y_{in}}{1 + 50Y_{in}} = \frac{-j50B}{2 + j50B} \quad (5.9)$$

At the frequencies where the input return loss degrades to 10-dB, we have

$$S_{11} = 20\log|\Gamma_{in}| = 20\log\left|\frac{-j50B}{2 + j50B}\right| = -10dB \quad (5.10)$$

Solving Equation (5.10), the marginal susceptance at both ends of the matching bandwidth can be found to be

$$B_{1,2} = \pm 0.0133S \quad (5.11)$$

where a positive B is corresponding to the upper boundary of the matching bandwidth and a negative B is corresponding to the lower boundary of the matching bandwidth.

Ignoring the part of input susceptance contributed from the load of the common-gate stage, the gate inductor L_s and the gate-to-source capacitance C_{gs} determines the value of B . According to Equation (5.6), B can be expressed as follows based on the above simplification.

$$B = \omega C_{gs} - \frac{1}{\omega L_s} \quad (5.12)$$

Solving Equation (5.12) with the B values provided in Equation (5.11), the lower boundary of the matching bandwidth ω_L and upper boundary of the matching bandwidth ω_H are found to be as follows.

$$\omega_L = \frac{-0.0133 + \sqrt{0.0133^2 + 4C_{gs}/L_s}}{2C_{gs}} \quad (5.13a)$$

$$\omega_H = \frac{+0.0133 + \sqrt{0.0133^2 + 4C_{gs}/L_s}}{2C_{gs}} \quad (5.13b)$$

So the -10-dB matching bandwidth can be easily obtained as

$$BW|_{S_{11} \leq -10dB} = \omega_H - \omega_L = \frac{13.3 \text{ mS}}{C_{gs}} \quad (5.14)$$

Consequently, the -10-dB matching bandwidth of the common-gate input architecture is determined by the gate-to-source capacitance of the input MOS transistor to the first order. In other words, the gate width of the input transistor directly determines the input matching bandwidth of the low-noise amplifier since the minimum gate length available in the process is used almost all the time for the input MOS transistor of a LNA design and the unit area capacitance C_{ox} is fixed in a specific process.

Assuming the gate-to-source capacitance of the input MOS transistor in common-gate configuration is 150-fF, the calculated -10-dB matching bandwidth is approximately 14.1-GHz, manifesting the intrinsic wideband matching nature of the common-gate input architecture. Consequently, it is quite promising that the common-gate input architecture can satisfy the wideband input matching requirement for the ultra-wideband low-noise amplifier. To accomplish this goal, the width of the input MOS transistor is preferred to be small for extending the matching bandwidth. It can be concluded that the matching bandwidth of the common-gate input architecture is extended with the down-scaling of CMOS process technologies, where a small gate length automatically reduces the gate-to-source capacitance.

The noise performance of the common-gate input architecture needs to be investigated to understand the design guideline for optimum noise figure and the trade-offs between the noise figure and the other specifications.

Figure 5.2 Major Noise Sources in the Common-Gate Architecture

Figure 5.2 shows the major noise sources in the common-gate input architecture, including the source noise, channel thermal noise and induced gate noise. Without loss of generality, Z_{gs} is used to denote the gate-to-source impedance of the MOS transistor, taking the resistive item due to the NQS effect into account. The effect of the finite output resistance of the MOS transistor is neglected in favor of simplicity. To facilitate the derivation process, the current noise model is adopted for the 50-Ohm source noise instead of the voltage noise model adopted in Chapter 4.

Figure 5.3 Calculation of CG Stage Output Noise Current Due to Source Noise

The output noise current spectral density due to source can be calculated based on the small-signal equivalent circuit shown in Figure 5.3, where only the noise current of the 50-Ohm source impedance is taken into account. It can be derived that the drain output noise current i_{nos} solely induced by the source resistance noise i_{ns} can be given by

$$\overline{i_{nos}} = \frac{g_m Z_p}{1 + g_m Z_p} \overline{i_{ns}} \quad (5.15)$$

where impedance Z_p is the parallel combination of the source resistance R_s , source inductor L_s and gate-to-source impedance of the MOS transistor Z_{gs} , given by

$$Z_p = R_s \parallel sL_s \parallel Z_{gs} \quad (5.16)$$

Hence the spectral density of the output noise current due to source noise S_{nos} can be given by

$$S_{nos} = \frac{\overline{i_{nos}^2}}{\Delta f} = \frac{g_m^2 |Z_p|^2}{|1 + g_m Z_p|^2} \cdot \frac{\overline{i_{ns}^2}}{\Delta f} \quad (5.17)$$

The output noise current spectral density due to channel thermal noise can be calculated based on the small-signal equivalent circuit shown in Figure 5.4, where only the channel thermal noise of the MOS transistor in common-gate configuration is considered.

Figure 5.4 Calculation of CG Stage Output Noise Current Due to Channel Noise

The drain output noise current i_{nod} solely due to the channel thermal noise i_{nd} can be given by

$$\overline{i_{nod}} = \frac{1}{1 + g_m Z_p} \overline{i_{nd}} \quad (5.18)$$

Hence the spectral density of the output noise current due to channel thermal noise of the input MOS transistor S_{nod} can be given by

$$S_{nod} = \frac{\overline{i_{nod}^2}}{\Delta f} = \frac{1}{|1 + g_m Z_p|^2} \cdot \frac{\overline{i_{nd}^2}}{\Delta f} \quad (5.19)$$

The output noise current spectral density due to the induced gate noise can be calculated based on the small-signal equivalent circuit shown in Figure 5.5, where only the induced gate noise of the MOS transistor in common-gate configuration is considered.

Figure 5.5 Calculation of CG Stage Output Noise Current Due to Induced Gate Noise

The drain output noise current i_{nog} solely due to the induced gate noise i_{ng} can be given by

$$\overline{i_{nog}} = \frac{g_m Z_p}{1 + g_m Z_p} \overline{i_{ng}} \quad (5.20)$$

Similarly, the spectral density of the output noise current due to induced gate noise of the input MOS transistor S_{nog} can be given by

$$S_{nog} = \frac{\overline{i_{nog}^2}}{\Delta f} = \frac{g_m^2 |Z_p|^2}{|1 + g_m Z_p|^2} \cdot \frac{\overline{i_{ng}^2}}{\Delta f} \quad (5.21)$$

With the above development, the 50-Ohm noise factor can be calculated by comparing the total output noise current and the output noise current due to source only. Since the channel thermal noise and induced gate noise are partially correlated, so are their respectively induced output noise currents. Therefore, one must be cautious in the derivation of the overall noise factor expression, given by Equation (5.22).

$$NF = 1 + \frac{\overline{i_{nod}^2} + \overline{i_{nog}^2}}{\overline{i_{nos}^2}} + \frac{\overline{i_{nod} i_{nog}^*} + \overline{i_{nod}^* i_{nog}}}{\overline{i_{nos}^2}} \quad (5.22)$$

While the second item can be calculated easily using the results of Equation (5.17), Equation (5.19) and Equation (5.21), the third item needs to be calculated carefully.

$$\begin{aligned}
 \overline{i_{nod} i_{nog}^*} + \overline{i_{nod}^* i_{nog}} &= \frac{g_m}{|1 + g_m Z_p|^2} \left(Z_p^* \overline{i_{nd} i_{ng}^*} + Z_p \overline{i_{nd}^* i_{ng}} \right) \\
 &= \frac{g_m}{|1 + g_m Z_p|^2} \left(Z_p^* c^* 4kT\omega C_{gs} \sqrt{\gamma\delta/5\Delta f} + Z_p c 4kT\omega C_{gs} \sqrt{\gamma\delta/5\Delta f} \right) \\
 &= \frac{8kT\omega g_m C_{gs} \sqrt{\gamma\delta/5\Delta f}}{|1 + g_m Z_p|^2} \text{Re}[Z_p \cdot c]
 \end{aligned}
 \tag{5.23}$$

Consequently, the overall noise factor of the common-gate input architecture can be given by

$$NF = 1 + \frac{\gamma R_s}{\alpha g_m |Z_p|^2} + \frac{\alpha \delta R_s \omega^2 C_{gs}^2}{5 g_m} + \frac{2 R_s \omega C_{gs} \sqrt{\gamma\delta/5} \text{Re}[Z_p \cdot c]}{g_m |Z_p|^2}
 \tag{5.24}$$

In Equation (5.24), the second item is contributed by the channel thermal noise; while the gate to source impedance is dominated by the gate-to-source capacitance and is resonated out by the source inductance, Z_p is reduced to R_s and the item contributed by the channel thermal noise is simplified to be $\gamma/\alpha g_m R_s$, validating the expression of Equation (3.27). The third item in Equation (5.24) is introduced by the induced gate noise and the fourth item is introduced by the correlation of the two noise sources.

It is clearly seen that to achieve better noise figure, high transconductance is desired. This leads to a directly trade-off between the noise performance and the input matching, since the transconductance should be around 20-mS for optimum matching.

To simplify the analysis process toward the technique for optimum noise figure, assuming Z_{gs} is dominated by the gate-to-source capacitance at the frequencies of interest. At the frequency where the gate-to-source capacitance C_{gs} and the source inductance L_s tunes out, Z_p reaches its maximum value across the operation frequency

band and the minimum noise figure is achieved according to Equation (5.24). At this resonant frequency of the input network ω_0 , Z_p is reduced to R_s and the noise figure at this frequency is given by

$$NF|_{\omega=\omega_0} = 1 + \frac{\gamma}{\alpha g_m R_s} + \frac{\alpha \delta R_s \omega_0^2 C_{gs}^2}{5 g_m} \quad (5.25)$$

Since $C_{gs}=2C_{ox}WL/3$ and $g_m=(2\mu_n C_{ox}W/LI_D)^{1/2}$, Equation (5.25) can be re-written as follows to explicitly reflect the dependence of the overall noise factor on the gate width of the common-gate MOS transistor and its biasing current I_D .

$$NF|_{\omega=\omega_0} = 1 + \frac{1}{\sqrt{2}} \alpha^{-1} \gamma R_s^{-1} \mu_n^{-\frac{1}{2}} C_{ox}^{-\frac{1}{2}} L^{\frac{1}{2}} I_D^{-\frac{1}{2}} W^{-\frac{1}{2}} + \frac{2\sqrt{2}}{45} \alpha \delta R_s \mu_n^{-\frac{1}{2}} C_{ox}^{\frac{3}{2}} \omega_0^2 L^{\frac{5}{2}} I_D^{-\frac{1}{2}} W^{\frac{3}{2}} \quad (5.26)$$

Consequently, a bias-independent optimum device width exists for minimum noise figure. The condition for minimum noise figure at frequency ω_0 is given by

$$\frac{1}{3\sqrt{2}} \alpha^{-1} \gamma R_s^{-1} \mu_n^{-\frac{1}{2}} C_{ox}^{-\frac{1}{2}} L^{\frac{1}{2}} I_D^{-\frac{1}{2}} W^{-\frac{1}{2}} = \frac{2\sqrt{2}}{45} \alpha \delta R_s \mu_n^{-\frac{1}{2}} C_{ox}^{\frac{3}{2}} \omega_0^2 L^{\frac{5}{2}} I_D^{-\frac{1}{2}} W^{\frac{3}{2}} \quad (5.27)$$

Solving Equation (5.27), we can obtain the optimum device gate width W_{opt} as given below.

$$W_{opt} = \frac{1}{2\alpha C_{ox} \omega_0 L R_s} \sqrt{\frac{15\gamma}{\delta}} \quad (5.28)$$

Hence, the noise-optimum gate width W_{opt} of the common-gate architecture can be estimated by Equation (5.28); it is interesting to discover that same to the source inductive degeneration architecture, this noise-optimum gate width is independent of the biasing current. In real design practice, the decision on the device gate width is generally a trade-off between the input matching bandwidth and the noise performance.

While optimum gate width exists in terms of noise optimization, the gate width is desired to be small to maintain wideband input matching over the interested frequency band. This trade-off is even more stringent while the real part of the input admittance, namely the transconductance of the input MOS transistor, is set to be higher than 20-mS for better noise performance according to Equation (5.24). Hence, with a fixed current consumption budget, design iteration is required to find out the best balance between the noise performance and input matching quality, which are compromised in the common-gate input architecture.

5.2 Design of a Two-Stage Staggering-Tuning Common-Gate UWB LNA

Based on the theoretical development of the common-gate input architecture presented in the previous section, an ultra-wideband low-noise amplifier design is implemented and proposed in this section.

As discussed earlier, the common-gate stage generally exhibits lower gain and higher noise figure comparing with the common-source stage; consequently, an inductive load is normally adopted for the common-gate input stage as complex load network will substantially degrade the noise performance of the LNA. Therefore, the load Z_L in Figure 5.1 is formed by a parallel LC tank, where the inductor L_L is implemented as an on-chip spiral and the capacitor C_L comprises the total capacitance loaded at the drain of the common-gate MOS transistor, including the input capacitance of the next stage. While the LNA is implemented as a single common-gate stage, the gain bandwidth is mainly determined by the load network. In such case, maximum gain bandwidth is obtained only when the LC load network resonates at the center of the interested band. As discussed in Chapter 4, such arrangement could only achieve less than 1.4-GHz

bandwidth assuming the overall quality factor of the load network is about 5. This insufficient bandwidth problem, together with the fact that a single common-gate stage normally provides gain of less than 10-dB due to input matching constraints, lead to the construction of a two-stage design in which the gain is boosted comparing with a single stage and the bandwidth is extended by introducing a novel staggering-tuning technique. This staggering-tuning technique takes advantage of the two amplification stages available in the low-noise amplifier by designing the load of each stage so that the two LC load networks peak the gain at different frequencies within the interested band to extend the overall gain bandwidth of the proposed low-noise amplifier.

Figure 5.6 shows the schematic of the proposed common-gate two-stage staggering-tuning ultra-wideband low-noise amplifier. The input MOS transistor M_1 is in common-gate configuration, whose gate is biased by a DC voltage V_{B1} through a resistor R_{b1} with decoupling capacitor C_{b1} to bypass the possible noise coupled through the DC biasing voltage. A source inductor L_s is employed to avoid RF signal leakage to ground while establishing the DC current path. An inductor L_{L1} is used as the load of the common-gate stage, which resonates with the total capacitance at the drain of the common-gate stage to peak the gain at frequency ω_1 . The output of the common-gate input stage is AC coupled to the second stage through coupling capacitor C_c . The second amplification stage is a common-source stage with a cascode transistor to improve the gain and reverse isolation.

Figure 5.6 Proposed CG2SST UWB LNA

Similarly, the common-source MOS transistor in the second stage is biased by a DC voltage $VB2$ through a resistor R_{b2} with decoupling capacitor C_{b2} . An inductor L_{L2} is used as the load of the second stage, which resonates with the total capacitance at the drain of the cascode MOS transistor at another frequency ω_2 . Small metal film resistors are added in series with the inductive load of both stages to degrade the quality factor of respective gain peaks for flatter gain response across the interested spectrum. Similar to the circuit proposed in Chapter 4, a source follower is employed as the output buffer, which achieves wideband output matching while avoiding direct loading of the 50-Ohm impedance of the measurement equipments to the output of the

second amplification stage. The biasing current of the output buffer is determined by the DC biasing voltage V_{B3} , through a resistor R_{b3} with decoupling capacitor C_{b3} .

Conventional narrowband low-noise amplifier peaks the gain of each stage at the interested frequency to ensure that maximum gain is obtained. However, this will definitely result in a narrow bandwidth determined mainly by the quality factor of the LC resonant network. Hence, a different arrangement of the peaking frequency is chosen to extend the bandwidth of the two-stage amplifier. Maximum bandwidth of the proposed UWB LNA design can only be achieved by optimal selection of the gain peaking frequencies of the two amplification stages, namely, ω_1 and ω_2 .

Figure 5.7 Gain Bandwidth Extension Using the Staggering-Tuning Technique

As illustrated in Figure 5.7, the two resonant frequencies are chosen to be close to the lower and upper boundaries of the interested band so as to peak the gain at these points. The gain of the LNA at the center of the interested band is obtained by the multiplication of the gain curves of the two stages. It is clear that a valley can be expected around the center of the interested band between the two gain peaks. To

obtain maximum extended bandwidth, it is important to ensure that the valley floor is less than 3-dB lower comparing with each gain peak. It is very difficult to mathematically calculate the gain difference between the valley floor and the peak gain of the two stages, due to various frequency dependent effects of the devices in CMOS process technology. Consequently, the staggering-tuning technique is adopted in simulation to determine the optimal gain peaking frequencies to ensure maximum - 3-dB gain bandwidth. The frequencies of the gain peaks are adjusted mainly by the load inductors of the two stages and their shapes are adjusted by the metal thin film resistors. The load inductor and resistor create a zero in the impedance of the load network as explained in Chapter 4, which is beneficial for the extension of bandwidth. A feedback path formed by a series combination of R_f and C_f is introduced, which effectively further decreases the quality factor of the two load networks according to the Miller's Theorem, especially for the first stage. As will be shown shortly, this feedback reduces the maximum gain of the first gain peak and improves the overall gain flatness of the proposed design.

The MOS transistor M_4 in the output buffer needs to be small so that its related parasitic capacitance does not influence the peak frequency of the second gain stage significantly. Because of this, the attenuation of the source follower is relatively higher than the output buffer employed in Chapter 4, as shown in Figure 5.8. The input capacitance of the source follower is approximately 20-fF, which indicates the suitable input capacitance of the next-stage mixer in an integrated receiver.

Figure 5.8 Voltage Attenuation of the Output Buffer in Schematic and Extracted Simulation

In the schematic shown in Figure 5.6, all the MOS transistors adopt minimum channel length available in the process technology. A moderate width is selected for MOS transistor M_1 so that its gate-to-source capacitance can resonate with a relatively large inductor L_s , which minimizes the signal leakage at lower frequencies. A relatively large width is selected for MOS transistor M_2 in the second stage so as to boost the overall gain of the LNA; however, it could not be too large since its gate-to-source capacitance is directly in shunt with the load of the first stage and has a direct influence on the position of the peak corresponding to the first stage load. Similar to the SIDFB UWB LNA design, the cascode device M_3 uses moderate channel width so as not to influence the position of the peak corresponding to the second stage load. As discussed earlier, the size of the MOS transistor in the source follower is selected to be small, which is co-simulated with the resistor R_o and current sink M_5 for acceptable output matching over the interested spectrum. Since excessive series resistance would result in noticeable noise degradation, the small resistors R_{L1} and R_{L2} in both loads,

implemented as thin film metal resistors, are considered together with the parasitic resistance of the power traces so that their resistance is just sufficient to obtain the desirable gain flatness over the operation frequencies. The resistor R_f and capacitor C_f in the feedback path are optimized together with the loads of the two stages for better gain flatness. The device values are determined after careful tuning of the gain curve as well as other specifications in both schematic and extracted simulations and the final values are listed in Table 5.1.

Table 5.1 Device Values of the Proposed CG2SST UWB LNA

Designation	Value
M_1	120- μm /0.18- μm
M_2	160- μm /0.18- μm
M_3	80- μm /0.18- μm
M_4	30- μm /0.18- μm
M_5	120- μm /0.18- μm
L_s	5.10-nH
L_{L1}	2.70-nH
L_{L2}	1.77-nH
C_c	1.0-pF
C_f	70-fF
C_{b1}, C_{b2}, C_{b3}	22.0-pF
R_f	7.4-KOhm
R_o	140-Ohm
R_{L1}	6.0-Ohm
R_{L2}	7.0-Ohm
R_{b1}, R_{b2}, R_{b3}	8.0-KOhm

As can be observed from Table 5.1, MOS transistor M_1 is sized to be relatively small to extend the input matching bandwidth as indicated by Equation (5.14). The source inductor L_s is chosen to be resonant with the gate-to-source capacitance of M_1 at the

center of the 3.1-10.6-GHz UWB band to minimize the overall noise figure throughout the band as indicated in Equation (5.24). MOS transistor M_2 is chosen to be relatively big to provide sufficient gain for the second stage and M_3 is only half the size of M_2 so as not to influence the gain peak frequency of the second stage. The load inductors L_{L1} and L_{L2} are determined by staggering-tuning the gain peaking frequencies of the respectively stages and the series resistors R_{L1} and R_{L2} are determined by the gain difference between the peak gains and the valley floor.

The schematic simulation results are shown here to demonstrate the competence of the proposed circuit in achieving the target specifications of the UWB LNA. The proposed LNA design is supplied by a 1.8-V DC voltage, which is standard for a 0.18- μm CMOS process. The input matching quality in schematic simulation is shown in Figure 5.9. The transconductance of the input MOS transistor has been increased to improve the noise performance of the common-gate stage and 10-dB return loss at the input port has been set at the criterion for this trade-off. According to simulation, an optimum balance is found while the device is biasing at 2.5-mA with a transconductance of 32-mS.

Figure 5.9 Simulated Input Matching of the CG2SST UWB LNA

As can be seen in Figure 5.9, the input return loss is better than 10-dB from 3 to 9.6-GHz, with the optimum matching achieved at about 5.5-GHz. The S_{11} in 9.6 to 10.6-GHz range is still better than -9-dB. Hence, good matching of the whole UWB spectrum can be obtained easily using the common-gate input architecture, which is coherent with the previous analysis and estimation.

The forward gain of the proposed low-noise amplifier is shown in Figure 5.10, with a demonstration on the effect of the feedback path.

Figure 5.10 Simulated Forward Gain of the CG2STT UWB LNA with and without the Feedback Path

It is clearly shown that the introduction of the feedback path slightly adjusted the gain curve in that it reduces the maximum gain of the first gain peak to make both peaks have similar maximum gain, hereby improving the gain flatness over the whole bandwidth. With the help of the series resistors in both loads, the gain of the proposed LNA between the two gain peaks are less than 2.2-dB lower than the maximum gain (9.1 to 11.3-dB); the overall -3-dB gain bandwidth extends from 4.4 to 10.3-GHz, covering almost the whole UWB spectrum. The maximum gain in schematic simulation is 11.3-dB including the output buffer; this indicates the maximum gain of the first two stages is 21.3-dB, leaving us sufficient margin to counter for the non-ideal implementation losses, such as the parasitic effects and pad contact losses. The corresponding current consumption of the second stage is 3.1-mA; so the total current consumption of the proposed CG2SST UWB LNA design is 5.6-mA.

The wideband output matching is relatively easy to achieve using the source follower. As shown in Figure 5.11, schematic simulation shows that the output return loss of the proposed LNA design is better than 13-dB across the entire UWB spectrum.

Figure 5.11 Simulated Output Matching of the CG2SST UWB LNA

The overall reverse isolation is good since three stages are incorporated in the design, including the output buffer stage. As shown in Figure 5.12, the overall reverse isolation is better than -70-dB in schematic simulation.

The 50-Ohm noise figure and minimum noise figure at noise optimum source impedance condition are shown in Figure 5.13. It suggests that the difference between the two curves is very small across the 3.0 to 11.0-GHz spectrum, indicating that 50-Ohm source impedance is close to the noise optimum source impedance for this input architecture.

Figure 5.12 Simulated Reverse Isolation of the CG2SST UWB LNA

Figure 5.13 Simulated 50-Ohm and Minimum Noise Figure of the CG2SST UWB LNA

The 50-Ohm noise figure reaches its minimum of 2.55-dB in the 4.8 to 5.4-GHz range and the worst noise figure in the -3-dB gain bandwidth is 5.5-dB at 10.3-GHz. Hence, the noise figure of the common-gate input architecture in simulation is only slightly worse than the source-inductive degeneration architecture when optimum input matching is traded off for noise performance.

The input-referred 1-dB compression point and the input-referred 3rd-order intercept point are both simulated at 6-GHz to examine their compliance to the linearity requirement. The simulation results for the ICP1 and IIP3 are shown in Figure 5.14 and Figure 5.15 respectively.

Figure 5.14 Simulated ICP1 of the CG2SST UWB LNA

Figure 5.15 Simulated IIP3 of the CG2SST UWB LNA

As shown above, the ICP1 and IIP3 of the proposed common-gate two-stage staggering-tuning UWB LNA is -12.9-dBm and -4.7-dBm respectively, which meet the target specification with some reasonable margins.

The stability of the two stages of the proposed LNA has been examined respectively to ensure that the two are both unconditionally stable. Hence, when the two stages are cascaded, the unconditional stability is ensured since no inter-stage feedback is involved in the design. The K factor and $|\Delta|$ of the respective stages are shown in Figure 5.16, which shows that the K factor is larger than unity and $|\Delta|$ is smaller than unity for both stages and suggests that both stages are unconditionally stable.

(a)

(b)

Figure 5.16 Simulated Stability of the CG2SST UWB LNA
(a) K Factor (b) $|\Delta|$

The group delay of the proposed CG2SST UWB LNA design is also checked in schematic simulation and the result is plotted in Figure 5.17. It can be observed that the peaks of the group delay are correspondent with the peaks in the gain curve and the group delay of the proposed LNA in the -3-dB gain bandwidth is within 60 to 215-ps range, whose ripple is higher than the proposed SIDFB UWB LNA since the quality factor of the load for the common-gate stage is relatively high for better noise performance.

Figure 5.17 Simulated Group Delay of the CG2SST UWB LNA

5.3 Post-Layout Simulation and Experimental Results

Same to the LNA design proposed in Chapter 4, the common-gate two-stage staggering-tuning ultra-wideband low-noise amplifier is implemented based on GLOBALFOUNDRIES 0.18- μm 1P6M RF CMOS process technology. The layout of the proposed LNA design is performed based on the device layout patterns provided in the process design kit and the final layout delivered for fabrication is shown in Figure 5.18.

Figure 5.18 Layout of the Proposed CG2SST UWB LNA

All the devices of the proposed LNA circuit are placed within the guard ring that sets up the perimeter. The RF signal input and output are both single-ended and the GSG pad patterns are placed at the left and the right guard rings respectively to ensure that the unwanted coupling between the input and output probes are minimized. The DC pads for the gate biasing voltages are placed at three corners of the layout to ensure that the DC probes can easily touch those pads without any confliction with the GSG RF probes during measurement. The voltage supply VDD pad is located at the right side of the bottom guard ring, where it can be connected to the load inductors of the first two stages conveniently through the small series resistors implemented on a metal layer. The total area of the proposed LNA design is 0.72-mm*0.82-mm, including the pads and the guard ring.

The parasitic effects are extracted after the layout is drafted and extracted simulations have been run to identify the impact of those parasitic effects to the key specifications of the proposed LNA design. The layout has been optimized iteratively according to the understanding of the dominant parasitic components. Specifically for this design, the down-shift of the two gain peaks is an important concern since the gain flatness and bandwidth will be largely compromised no matter the two peaks are shifted further away or closer to each other. Although the down-shift of the two gain peaks is inevitable comparing with the schematic simulation due to the introduction of the parasitic capacitance, the layout has been adjusted so as to ensure the valley floor is still less than 3-dB lower comparing with the maximum gain. The parasitic resistances of the interconnecting traces in series with the load inductors are also carefully treated to ensure that the thin film metal resistors are just enough to guarantee the maximum bandwidth.

The final extracted simulation results are compared with the experimental results in the following section. The measurement setup for the fabricated common-gate two-stage staggering-tuning UWB LNA is same to the setup for the SIDFB UWB LNA design in Chapter 4 and is elaborated in Appendix B. The micro-photo of the fabricated design is shown in Figure 5.19.

The VDD pin is supplied with a 1.8-V DC supply voltage during the measurement and VB1 and VB2 are adjusted so that the first stage and the second stage draw 2.5-mA and 3.1-mA respectively, to be consistent with simulation. The output buffer stage is consuming 4.5-mA current, which is same as in simulation to make sure that the

extracted simulation provided a reasonable estimation of the voltage attenuation for this stage.

Figure 5.19 Micro-Photo of the Fabricated CG2SST UWB LNA

The measured forward gain of the fabricated design is shown in Figure 5.20, with the final extracted simulation result as a comparison.

Figure 5.20 Measured and Simulated Forward Gain of the CG2SST UWB LNA

As shown in Figure 5.20, although the measured forward gain of the fabricated design is roughly 1-dB lower than in extracted simulation, the extracted simulation predicts the peaking frequencies quite well, especially for the peak at lower frequencies. In extracted simulation, the maximum gain at the higher frequency peak is deliberately adjusted to be about 1-dB higher than the lower frequency peak, so as to account for all the uncounted IC implementation losses that are typically higher at higher frequencies. The measurement result perfectly justifies such arrangement. The gain peak at higher frequency is shifted-down more significantly than the lower peak; moreover, the loss of gain is generally increased at higher frequencies, which makes the maximum gain of the two gain peaks almost the same. The maximum gain is measured to be 9.3-dB. Given the 10.5-dB attenuation of the output buffer, the measured gain of the proposed design is in the range of 16.8-dB to 19.8-dB. The measured -3-dB gain bandwidth is from 4.0 to 9.2-GHz.

Figure 5.21 Measured and De-Embedded Gain of the CG2SST UWB LNA

Figure 5.21 shows the measured gain and the actual forward gain of the first two stages without the output buffer. The de-embedding operation utilizes the voltage attenuation data of the output buffer from the extracted simulation result as shown in Figure 5.8 since the output buffer has not been fabricated and characterized separately for de-embedding. The upper boundary of the -3-dB gain bandwidth is extended to 9.3-GHz after taking the frequency-dependent loss of the output buffer stage into account.

Figure 5.22 shows the comparison of the input matching quality between the extracted simulation and the experimental results.

Figure 5.22 Measured and Simulated Input Matching of the CG2SST UWB LNA

As shown in Figure 5.22, the resonant frequency of the input network is 400-MHz lower than in the extracted simulation. The down-shift in the resonant frequency improves the input matching quality at lower frequencies, but degrades it at higher frequencies. The measured input return loss is higher than 10-dB from 3.0 to 8.0-GHz; from 8.0-GHz to the upper bound of the gain bandwidth, namely 9.3-GHz, S_{11} is still

better than -9.8-dB. Hence, very good matching over the whole gain bandwidth is obtained.

Figure 5.23 shows the output matching quality of the fabricated design. Again, very good matching quality can be achieved while employing the source follower as the output buffer; the measured result shows the output return loss is high than 16-dB throughout the 3 to 10-GHz spectrum.

Figure 5.23 Measured and Simulated Output Matching of the CG2SST UWB LNA

The extracted simulation and measurement results of the reverse isolation for the proposed design are compared in Figure 5.24.

Figure 5.24 Measured and Simulated Reverse Isolation of the CG2STT UWB LNA

As shown in Figure 5.24, S_{12} increases with frequencies and the worst reverse isolation generally is located generally at the higher boundary of the interested frequency range, namely, 10-GHz. The worst reverse isolation is about -52-dB in extracted simulation, which degrades about 20-dB from the schematic simulation due to the insertion of the extracted parasitic effects. The measured result shows 10-dB more degradation, making the worse measured reverse isolation -40-dB. It is clear that the degradation of reverse isolation between extracted simulation and measurement is much higher in this design comparing with the design proposed in Chapter 4. Moreover, in this design three stages are cascaded between the input and output ports, hence the reverse isolation should be better than the two-stage SIDFB LNA design, as supported by both the schematic and extracted simulations. However, the comparison between the measured results of the two designs does not agree with this theory. The reasonable explanation for this phenomenon is that the limitation for reverse isolation is no longer lying in the circuit itself when its reverse isolation is better than -40-dB;

instead, the coupling between the output and input probes through the substrate and air during reverse isolation measurement is dominating the results. This also explains why the three-stage LNA is measured to have less reverse isolation than the two-stage LNA, because the probe distance for the former case is 0.65-mm while it is 0.93-mm for the latter case.

The measured noise figure of the fabricated design is shown in Figure 5.25, in comparison with the extracted simulation result. It is obvious that the measured noise figure is higher than the extracted simulation in the entire interested spectrum; however, in the -3-dB gain bandwidth of the design, the discrepancy is generally less than 1-dB. In the 4.0 to 9.3-GHz bandwidth, the minimum measured noise figure is 3.2-dB and the maximum noise figure is 6.6-dB.

Figure 5.25 Measured and Simulated Noise Figure of the CG2SST UWB LNA

The 1-dB compression point and the 3rd-order intercept point are also measured to verify the linearity of the fabricated design. The 1-dB compression point is measured

at 6-GHz by observing the output power while increasing the power of the input single tone linearly. The 3rd-order intercept point is measured with two single tones of same power injected at 6-GHz and 6.004125-GHz. The 4.125-MHz spacing is determined according to the spacing of two carriers defined by the OFDM symbol of the WiMedia Alliance's UWB standard. The measured input-referred 1-dB compression point and the measured input-referred 3rd-order intercept point are -15.0-dBm and -5.7-dBm respectively as shown in Figure 5.26 and Figure 5.27, which well agree with the simulation results.

Figure 5.26 Measured ICP1 of the CG2SST UWB LNA

Figure 5.27 Measured IIP3 of the CG2SST UWB LNA

5.4 Summary

This chapter describes an ultra-wideband low-noise amplifier design based on the common-gate input architecture, for wideband input matching. Two amplification stages are employed so as to overcome the relatively low gain of the single common-gate stage. To extend the overall gain bandwidth, the load networks of the two stages are tuned in a staggering manner to peak the gain at two different frequencies in the interested frequency band for wide gain bandwidth. The proposed design is fabricated and verified by the on-wafer probing method. The measured specifications of the proposed CG2SST UWB LNA design are summarized in Table 5.2. Comparing with the SIDFB UWB LNA proposed in Chapter 4, the CG2SST UWB LNA exhibits higher minimum noise figure since the common-gate input architecture is intrinsically noisier and the trade-off between input matching quality and noise performance for this architecture is quite stringent. On the other hand, due to the introduction of one

more amplification stage, the difficult trade-off between gain and bandwidth in the single stage SIDFB UWB LNA is eased in this CG2SST UWB LNA. The maximum forward gain of the CG2SST UWB LNA is more than 2-dB higher than the SIDFB UWB LNA. However, as a penalty, it consumes slightly higher current and exhibits slightly degraded linearity.

Table 5.2 Summary of Measured Specifications of the Proposed CG2SST UWB LNA

Supply Voltage	1.8-V
Current Consumption	5.6-mA (excluding 4.5-mA for testing only)
Gain Bandwidth	4.0-GHz ~ 9.3-GHz
Forward Gain (S_{21})	16.8-dB ~ 19.8-dB
Input Matching (S_{11})	<-9.8-dB (<-10-dB in 3.0-GHz ~ 8.0-GHz)
Output Matching (S_{22})	<-16-dB
Reverse Isolation (S_{12})	<-39-dB
Noise Figure	3.2-dB ~ 6.6-dB
ICP1	-15.0-dBm
IIP3	-5.7-dBm

CHAPTER 6 Design of a Three-Stage Staggering-Tuning UWB LNA

According to the simulation and measurement results, the LNA designs proposed in Chapter 4 and Chapter 5 do not cover the whole 7500-MHz UWB spectrum.

In an effort to achieve full UWB spectrum coverage, this chapter extends the design work described in Chapter 5 by introducing one more gain peak in the interested frequency band. This common-gate three-stage staggering-tuning ultra-wideband low-noise amplifier, shorted as the CG3SST UWB LNA, exhibits higher maximum gain due to the introduction of the additional stage. A variable gain mechanism with minimum influence to the other specifications is implemented to help improve the dynamic range of the UWB receiver.

6.1 Three-Stage LNA Circuit Design

The gain bandwidth extension technique based on staggering gain peak tuning has been introduced in Chapter 5. It is found that the gain bandwidth achieved by the two-stage staggering-tuning technique is insufficient to cover the 3.1 to 10.6-GHz full UWB spectrum. According to the measurement results shown in Chapter 5, although good input matching has been achieved over the full UWB spectrum, the -3-dB gain bandwidth is from 4.0 to 9.3-GHz. Hence, generally 1-GHz bandwidth shortage is observed at both the low and high boundary of the target bandwidth. The reason for this shortage is easy to understand: while the gain of the LNA at the frequencies between the two peaks is boosted by both stages, the gain at frequencies outside the two peaks rolls off quite fast since it is well out of the band of the further gain peak.

To resolve this bandwidth shortage problem, an additional gain peak can be introduced by another cascaded amplification stage as shown in Figure 6.1.

Figure 6.1 Three-Stage Staggering-Tuning for Full UWB Spectrum Coverage

By tuning the three gain peaks, it is believed that the gain bandwidth can be extended to cover the full UWB spectrum based on the fact that more than 5-GHz bandwidth is already achieved with two staggering gain peaks. On the other hand, higher gain loss is expected at higher frequencies as proven in the previous chapter. Thus the gain curve is preferable to be pre-distorted as increasing with frequency slightly so as to compensate for this frequency-dependent loss in real implementation, as shown in Figure 6.1.

The schematic of the proposed common-gate three-stage staggering-tuning UWB LNA is shown in Figure 6.2. Two cascode stages are cascaded after the common-gate

stage to implement the three gain peaking loads that can be staggeringly tuned to cover the full UWB spectrum.

Figure 6.2 Schematic of the CG3SST UWB LNA

The trade-off between the noise performance and the input matching bandwidth in the common-gate input architecture is still valid in this design. The transconductance of the common-gate device is increased to the maximum value at which the input return loss reaches 10-dB at both low and high boundary of the full UWB spectrum. As demonstrated in Chapter 5, the wideband input matching is relatively easy to achieve, although the optimal matching frequency may shift down a little in the measurement. In Figure 6.3, the trade-off between the transconductance of the input transistor and the matching quality is shown.

Figure 6.3 Trade-off between Transconductance and Matching Bandwidth for the Common-Gate Input Architecture

It is apparent that the matching quality and matching bandwidth are both improved when the transconductance of the input MOS transistor is close to the 20-mS. However, since the noise figure of the common-gate stage decreases with the increase of the transconductance, we set the transconductance to 32-mS for the 120- μ m input transistor for better noise performance, while the input return loss at both ends of the UWB spectrum is still better than 10-dB according to schematic simulation.

Due to the relative low gain of the common-gate stage, the noise contributed by the common-source stage that directly follows the common-gate stage may also influence the overall noise figure of the LNA. Hence, the noise figure calculation including the noise sources in the common-source stage is performed based on the small-signal

equivalent circuit shown in Figure 6.4. The small resistor R_{L1} in series with the load inductor L_{L1} is neglected in favor of simplicity.

Figure 6.4 Small Signal Equivalent Circuit of the First Two Stages for Noise Analysis

After extensive calculation it can be shown that the noise factor of the first two stages can be expressed by

$$NF = F_{CG} + \frac{S_{ngu2}}{S_{R_s}} + \frac{S_{ngdc2}}{S_{R_s}} \quad (6.1)$$

where F_{CG} is the noise factor of the single common-gate stage given by Equation (5.24), S_{R_s} is the output noise current spectral density induced by the 50-Ohm source impedance; S_{ngu2} is the output noise current spectral density induced by the part of the gate noise of the common-source transistor that is fully uncorrelated with its channel thermal noise; S_{ngdc2} is output current spectral density induced by the sum of the common-source transistor's channel thermal noise and its part of gate noise that is fully correlated with the channel thermal noise [69]. The expressions for S_{ngu2} and S_{ngdc2} are given as follows.

$$S_{ngu2} = \left\{ \frac{\alpha \delta (1 - |c|^2) \omega^2 C_{gs2}^2}{5 R_s g_{m2}} \cdot \left[\left(\frac{1}{g_{m1}} + R_s \right)^2 + \frac{R_s^2}{g_{m1}^2 |Z_s(\omega)|^2} \right] \right\} \cdot S_{R_s} \quad (6.2)$$

$$S_{ngdc2} = \left(\frac{\gamma}{\alpha R_s g_{m2} |Z_o(\omega)|^2} + \frac{\alpha \delta |c|^2 \omega^2 C_{gs2}^2}{5 R_s g_{m2}} + \frac{2c\omega C_{gs2} \sqrt{\gamma \delta / 5 Z_o(\omega)}}{j R_s g_{m2} |Z_o(\omega)|^2} \right) \cdot \left[\left(\frac{1}{g_{m1}} + R_s \right)^2 + \frac{R_s^2}{g_{m1}^2 |Z_s(\omega)|^2} \right] \cdot S_{R_s} \quad (6.3)$$

In Equation (6.2) and Equation (6.3), g_{m1} and g_{m2} are the transconductance of the common-gate and common-source transistors respectively; C_{gs2} is the gate-to-source capacitance of the common-source transistor; $Z_s(\omega)$ is the impedance of the input parallel resonant network comprises L_s and Z_{gs1} while $Z_o(\omega)$ is the impedance of the load parallel resonant network formed by L_{L1} and C_{gs2} .

Beside the guidelines to improve the noise performance of the common-gate stage discussed in Chapter 5, it can be observed from the above derivation that the impedance of the load network of the common-gate stage also plays a role in determined the shape of the noise figure curve over the whole bandwidth. At frequencies far away from the resonant frequency of the load network, $Z_o(\omega)$ is reduced and the noise contributed by the common-source stage becomes significant. Hence, the resonant frequency of the load network for the common-gate stage is preferred to be located at the center of the band, to increase the average magnitude of $Z_o(\omega)$ over the whole bandwidth. This indicates that the common-gate stage should be corresponding to the middle gain peak among the three gain peaks and it is preferable to be tuned to the center of the interested band.

The previous work takes advantage on the easy application of the source follower stage without investigating its output impedance in detail. Equation (6.4) gives the

expression for the output impedance of the common-drain output buffer, where $Z_3(\omega)$ is the impedance of the parallel LC tank formed by L_{L3} and the sum of gate-to-drain capacitance of M_5 and M_6 . C_{gs6} and g_{m6} are the gate-to-source capacitance and the transconductance of the MOS transistor M_6 respectively.

$$Z_{out}(\omega) = \frac{1 + j\omega Z_3(\omega) C_{gs6}}{g_{m6} + j\omega C_{gs6}} \quad (6.4)$$

While C_{gs6} is relatively small since small size transistor is chosen, the output impedance can be well approximated by $1/g_{m6}$ within the interested frequency band and good output matching can be easily achieved. However, if L_{L3} is relatively large and its self resonant frequency falls in the interested frequency band, this high quality output matching could be potentially deteriorated. Hence, L_{L3} is relatively small and consequently the load network of the third stage must be corresponding to the gain peak of highest frequency in the LNA's gain curve, near the high boundary of the UWB spectrum. Based on the above analysis, we now understand the underlying principles for arranging the sequence of the three gain peaks, which determine the selection of the load inductors as well as the transistor sizes.

The proposed LNA circuit is biasing using simple current mirrors. The common-gate stage and the source follower stage share one reference current and the second and third cascode stages share another reference current. The biasing current of the second and third cascode stages can be adjusted by tuning the resistor R_{b6} in the current reference, through which variable gain can be achieved. Since the common-gate stage determines the input impedance and the noise performance of the proposed LNA design to the first order, tuning the biasing current of the second and third stage will

not significantly influence the input matching quality and the noise figure of the LNA. The principles in selecting the values of the devices in the schematic shown in Figure 6.2 are similar to the principles adopted for the CG2SST UWB LNA. Since the proposed CG3SST UWB LNA has three gain peaks in the interested spectrum instead of only two, more simulation iterations can be expected for optimum gain flatness. After extensive simulations including the extracted parasitic effects, the device values for the proposed LNA design in maximum gain condition are determined and given in Table 6.1.

Table 6.1 Device Values for the CG3SST UWB LNA

Designation	Value
M ₁ , M ₂ , M ₃ , M ₄	120- μ m/0.18- μ m
M ₅	100- μ m/0.18- μ m
M ₆	30- μ m/0.18- μ m
M ₇ , M ₈ , M ₉	60- μ m/0.18- μ m
L _s	7.46-nH
L _{L1}	2.39-nH
L _{L2}	5.30-nH
L _{L3}	1.43-nH
C _f	106-fF
C _{c1} , C _{c2}	1.0-pF
C _{b1}	10-pF
R _f	7.4-kOhm
R _{L1}	6.0-Ohm
R _{L2}	4.0-Ohm
R _{L3}	7.2-Ohm
R _{b5}	1.1-kOhm
R _{b6}	400-Ohm
R _{b1} , R _{b2} , R _{b3} , R _{b4}	5.0-KOhm

6.2 Simulation Results

The design of the proposed common-gate three-stage staggering-tuning low-noise amplifier is also based on the GLOBALFOUNDRIES 0.18- μm 1P6M RF CMOS process technology. The layout of the LNA circuit is shown in Figure 6.5; the die size is 0.74-mm*0.67-mm including the I/O pads and guard rings.

Figure 6.5 Layout of the Proposed CG3SST UWB LNA

The parasitic capacitances and resistances associated with the layout are extracted and the schematic simulation and extracted simulation results are compared and discussed in the following section.

Figure 6.6 Pre-layout and Post-layout Simulated Maximum Forward Gain of the CG3SST UWB LNA

Figure 6.6 shows the comparison of forward gain of the LNA in both pre-layout and post-layout simulations. It can be observed that the 3.1 to 10.6-GHz UWB spectrum can be well covered by the gain curve with three gain peaks. As expected, the frequencies of each gain peak are shifted down a little in post-layout simulation due to the introduction of parasitic capacitance. Also, it shows that the gain loss due to the parasitic effects generally increases with frequency. Therefore, the pre-compensation technique is proven again: by adjusting the gain curve in the pre-layout simulation so that it increases slightly with frequency, a relatively flat gain curve can be obtained in the post-layout simulation. By adjusting the resistor R_{b6} in the current reference, variable gain is obtained with variable biasing currents of the second and third cascode stages. The noise figure, input matching quality and output matching quality are not significantly influenced by this variable gain mechanism since only the biasing currents of the two intermediate stages are changed. However, the linearity of the

LNA does change with its gain since the signal reaches largest swing at the output of the third cascode stage. Table 6.2 summarizes the resistance of R_{b6} , corresponding biasing current of the proposed LNA circuit, the overall gain and the input-referred 1-dB compression point at different gain settings.

Table 6.2 Comparison on Variable Gain Steps

R_{b6} (Ohm)	Forward Gain (dB)	DC Current (mA)	ICP1 (dBm)
400	15.9 ~ 17.5	15.2	-23.1
500	14.9 ~ 16.6	13.4	-22.3
600	13.8 ~ 15.6	12.1	-21.7
700	12.5 ~ 14.3	11.1	-21.1
800	11.3 ~ 13.0	10.4	-20.1
900	9.9 ~ 11.6	9.8	-19.1
1000	8.7 ~ 10.4	9.3	-17.5

Considering the 10.5-dB attenuation introduced by the output buffer stage, the forward gain is comparable with the result of the two-stage LNA design in Chapter 5 when R_{b6} is 1-KOhm. The overall power consumption of the amplification and buffer stages at this gain step is 16.7-mW under a 1.8-V voltage supply, excluding the power consumed by the current references.

The comparison of the input matching quality in pre-layout and post-layout simulation is shown in Figure 6.7.

S_{11} is better than -10-dB over the full UWB spectrum in pre-layout simulation, while in post-layout simulation the optimal matching frequency is shifted down due to the introduction of the parasitic capacitance; thus the matching quality at high frequencies is degraded. However, S_{11} is still better than -9-dB in the 3.1 to 10.6-GHz frequency band in post-layout simulation. Similar comparison has been observed between the simulation and measurement results reported in Chapter 5.

The output matching quality and the reverse isolation are shown in Figure 6.8. The output return loss is higher than 10-dB and the reverse isolation of the LNA in post-layout simulation is better than 70-dB across the UWB spectrum.

Figure 6.7 Pre-Layout and Post-Layout Simulated Input Matching Quality of the CG3SST UWB LNA

Figure 6.8 Pre-Layout and Post-Layout Simulated Output Matching Quality and Reverse Isolation of the CG3SST

The pre-layout and post-layout noise figure curves of the proposed common-gate three-stage staggering-tuning UWB LNA are compared in Figure 6.9.

Figure 6.9 Pre-Layout and Post-Layout Simulated Noise Figure of the CG3SST UWB LNA

The noise figure under maximum gain condition in pre-layout simulation is better than 4.0-dB almost across the whole UWB bandwidth and the minimum noise figure is 2.9-dB. With the parasitic effects added in, the noise figure under maximum gain condition is degraded by about 0.5-dB at center of the band and more degradation is observed toward both ends of the interested frequency range. While the minimum gain step is chosen, the noise figure is only less than 1.2-dB worse than under the maximum gain condition, as shown by the curve c in Figure 6.9.

The performance of the proposed common-gate three-stage staggering-tuning UWB LNA is summarized in Table 6.3. All the data are based on the minimum gain condition and the loss of the output buffer has been de-embedded. The minimum noise figure of the CG3SST UWB LNA is similar to the CG2SST UWB LNA proposed in

Chapter 5. The introduction of one more amplification stage in this CG3SST UWB LNA design improves its gain bandwidth as well as maximum forward gain at the cost of 2.4-mA more current consumption and slight degradation in linearity.

Table 6.3 Summary of Post-Layout Simulation Results of the Proposed CG3SST UWB LNA

Supply Voltage	1.8-V
Current Consumption	8.0-mA (excluding 1.3-mA for testing only)
Gain Bandwidth	3.1-GHz ~ 10.6-GHz
Forward Gain (S_{21})	19.2-dB ~ 20.9-dB
Input Matching (S_{11})	<-9-dB
Output Matching (S_{22})	<-13-dB
Reverse Isolation (S_{12})	<-70-dB
Noise Figure	3.5-dB ~ 6.9-dB
ICP1	-17.5-dBm

CHAPTER 7 Design of DC Generation and ESD Protection Circuits

The ultra-wideband low-noise amplifier designs proposed in Chapter 4 and Chapter 5 directly take the advantage of off-chip DC voltage sources to set up the gate biasing voltages. In the design reported in Chapter 6, simple current mirrors are used to set the DC biasing points for each stage. However, to complete the whole low-noise amplifier circuit, stable and high-efficiency DC generation circuits need to be implemented and integrated. Another important consideration in LNA design is its capability of surviving ESD events since the RF input port of the LNA is usually connected to the external antenna through an I/O pin. In this section, the DC biasing and ESD protection schemes will be proposed based on the GLOBALFOUNDRIES 0.18- μm RF CMOS process, on which the proposed LNA circuits are designed.

7.1 DC Biasing Generation Circuits Design

To gain a competitive status in the wireless product market, it is quite important for an integrated circuit to reduce its pin count since the cost of an IC product is heavily dependent on its final pin count. First of all, the cost of packaging the IC die increases proportionally with the number of pins to be bonded. Similarly, in the production testing phase, the complexity of the testing development and thus the cost also increase with the pin count of the IC product. Hence, it is generally desirable to integrate all the DC biasing generation circuits on the same die with the core circuits to reduce the pin count. Beside the pin count issue, the integrated biasing circuit offers another design advantage in that it is able to sense the same temperature change as the core circuits and make necessary compensation, since they are physically placed

together. Consequently, it is highly desirable to design the DC biasing generation circuits together with the proposed RF circuits.

A constant reference current or voltage is normally desirable to bias the RF circuits against operation condition variations due to the change of ambient temperature, supply voltage and etc. The constancy against temperature is especially important since the IC need to operate in different part of the world, across which the temperature changes significantly. Since no constant current or voltage reference against temperature is automatically available in the CMOS IC process technology, a temperature constant DC biasing voltage or current normally involves the summation of a component that is complementary to absolute temperature (CTAT) and another component that is proportional to absolute temperature (PTAT), leading to the introduction of the bandgap voltage reference circuit.

In this work, a bandgap voltage reference circuit is implemented based on the vertical NPN bipolar devices available in the process. This constant bandgap reference voltage serves as one input of an operational transconductance amplifier (OTA) and the other input of the OTA is tapped from a conventional voltage-to-current (V2I) conversion circuit. The error of the two inputs is amplified by the OTA and the output of the OTA is controlling the gate of a PMOS transistor in the V2I branch, forming a negative feedback loop. This ensures the error between the two inputs of the OTA is reduced to minimum, thereby well defines a constant voltage in the V2I branch. With a low temperature coefficient resistor, this constant voltage can be converted into constant current, which can be mirrored to accurately define the biasing current of each stage in

the low-noise amplifiers. Figure 7.1 shows the full schematic of the bandgap voltage reference circuit with start-up circuit as well as the conventional OTA and V2I circuits.

Figure 7.1 Proposed Bandgap, OTA and V2I Circuits

As showed in Figure 7.1, thanks to the available vertical NPN transistors in the process, the classic Brokaw bandgap circuit [74] can be implemented to generate a constant reference voltage, whose operation principles are briefed as follows.

According to [75], the base-emitter voltage V_{BE} of the bipolar transistor can be expressed as a function of collector current I_C and absolute temperature T by

$$V_{BE} = V_{G0} \left(1 - \frac{T}{T_0} \right) + V_{BE0} \frac{T}{T_0} + \frac{mkT}{q} \ln \left(\frac{T_0}{T} \right) + \frac{kT}{q} \ln \left(\frac{J_C}{J_{C0}} \right) \quad (7.1)$$

where V_{G0} is the bandgap voltage of silicon extrapolated to zero Kelvin, T is the temperature in Kelvin, k is Boltzmann's constant, J_C is the collector current density

and m is a temperature constant around 2.3. V_{BE0} , J_{C0} are the base-emitter voltage and collector current density at the reference temperature T_0 respectively. According to Equation (7.1), the base-emitter voltage V_{BE} is found to have -2-mV/K temperature coefficient around room temperature under the assumption of constant collector current. Hence, V_{BE} can be utilized as the CTAT component in the generation of the bandgap reference voltage.

On the other hand, the base-emitter voltage of a bipolar transistor can also be expressed as

$$V_{BE} = \frac{kT}{q} \ln \left(\frac{I_C}{I_S} \right) \quad (7.2)$$

So the difference of the base-emitter voltages of two bipolar transistors can be written as

$$\begin{aligned} \Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= \frac{kT}{q} \ln \left(\frac{I_{C1}}{I_{S1}} \right) - \frac{kT}{q} \ln \left(\frac{I_{C2}}{I_{S2}} \right) \quad (7.3) \\ &= \frac{kT}{q} \ln \left(\frac{I_{C1} \cdot I_{S2}}{I_{C2} \cdot I_{S1}} \right) \end{aligned}$$

where I_{C1} and I_{C2} are the collector currents of the two bipolar transistors respectively and I_{S1} and I_{S2} are the scale currents of the two transistors respectively. Since the scale current of a bipolar transistor is linearly proportional to its base-emitter junction area, we have

$$\frac{I_{S2}}{I_{S1}} = \frac{A_2}{A_1} \quad (7.4)$$

where A_1 and A_2 are the base-emitter junction area of the two bipolar transistors respectively. Assuming the collector currents of the two transistors are identical, Equation (7.3) can be reduced to

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln \left(\frac{A_2}{A_1} \right) \quad (7.5)$$

Equation (7.5) suggests that the difference of the base-emitter voltages of two bipolar transistors is linearly proportional to the absolute temperature, hence we obtained the PTAT term.

Specifically in Figure 7.1, the difference of the based-emitter voltages of the transistors T_3 and T_4 drops across the resistor R_4 . So the DC current flowing on resistor R_4 can be given by

$$I_{R_4} = \frac{V_{BE4} - V_{BE3}}{R_4} = \frac{kT}{R_4 q} \ln \left(\frac{A_3}{A_4} \right) \quad (7.6)$$

Identical currents flowing through the bipolar transistors T_3 and T_4 are ensured by the current mirror formed by transistors M_1 and M_2 , where long channel PMOS transistors have been adopted to minimize the influence of the channel length modulation effect on the accuracy of one-to-one current mirroring. Consequently, the DC voltage at the base and collector of the bipolar transistor T_4 can be given as

$$\begin{aligned} V_{bg} &= 2R_5 I_{R_4} + V_{BE4} \\ &= \frac{2R_5}{R_4} \cdot \frac{kT}{q} \ln \left(\frac{A_3}{A_4} \right) + V_{BE4} \end{aligned} \quad (7.7)$$

As shown in Equation (7.7), the PTAT and CTAT terms are both available in the expression of V_{bg} , indicating constant voltage can be obtained by tuning the ratio of

resistors R_4 and R_5 . Table 7.1 summarizes the device values adopted for the DC generation circuits after optimization using the circuit simulator.

Table 7.1 Device Values of the Proposed DC Generation Circuits

Designation	Value
R_1, R_2, R_3	40-KOhm
R_4	10-KOhm
R_5	42-KOhm
R_6	6.0-KOhm
R_7	2.1-KOhm
T_1, T_2, T_4	5- μm *5- μm *1
T_3	5- μm *5- μm *8
M_1, M_2	16- μm /2- μm
M_3, M_4	12- μm /1- μm
M_5, M_6	6- μm /2- μm
M_7	150- μm /0.18- μm
M_8	15- μm /0.18- μm
C_1	1.6-pF
C_2	4.0-pF

The layout and the micro-photo of the proposed DC generation circuits are shown in Figure 7.2.

Figure 7.2 Layout and Micro-Photo of the Proposed DC Generation Circuits

(a) Layout (b) Micro-Photo

Due to the limitation of the measurement equipment, the ambient temperature cannot be varied to observe the performance of the DC generation circuits against temperature changes. Figure 7.3 shows the extracted simulation result of the temperature dependence of the voltage V_{bg} . The bipolar transistors T_3 and T_4 are both biased with a collector current of $5\text{-}\mu\text{A}$. V_{bg} is relatively constant across the $-40\text{-}^{\circ}\text{C}$ to $+85\text{-}^{\circ}\text{C}$ operation temperature range. The voltage is approximately 1.096-V when approaching the lower and upper temperature limits; while at about $20\text{-}^{\circ}\text{C}$, V_{bg} reaches its maximum value of approximately 1.104-V . The 8-mV variation across $-40\text{-}^{\circ}\text{C}$ to $+85\text{-}^{\circ}\text{C}$ is corresponding to $\pm 60.6\text{-ppm}/^{\circ}\text{C}$ temperature coefficient for the constant reference voltage V_{bg} ; this is regarded as acceptable for the biasing of low-noise amplifier circuits.

Figure 7.3 Simulated V_{bg} and V_{st} Variation with Temperature

The temperature dependence of the start-up voltage V_{st} is also shown in Figure 7.3. The start-up circuit is indispensable in the design since the bandgap circuit has two stable operation points. Beside the desirable operation point, in which V_{bg} can be used as a constant reference voltage, the bandgap circuit can also be stuck in a status where the circuit fails to start up and no current flows through the bipolar transistors. The start-up circuit solves this problem nicely by turning on the start-up transistor T_2 and injecting current into the bandgap circuit during start-up, ensuring that the bandgap circuit is pulled out from the stuck condition. V_{st} of around 1.2-V is sufficient to fulfill this task and only very low accuracy is required on V_{st} . While the bandgap circuit is in normal operation, V_{st} is only slightly higher than V_{bg} ; hence the start-up transistor T_2 is turned off and the operation of the bandgap circuit is not influenced by the start-up circuit.

Figure 7.4 shows both the simulated and measured variations of V_{bg} against the supply voltage V_{DD} at room temperature. The simulation results agree well with the

measurement results; V_{bg} only increases by 26-mV while V_{DD} increases from 1.5-V to 2.2-V, which corresponds to a line regulation of $\pm 18.6\text{-mV/V}$.

Figure 7.4 Simulated and Measured V_{bg} Variation with Supply Voltage V_{DD}

The OTA circuit amplifies the error between the constant reference voltage V_{bg} and the source voltage V_s of the PMOS transistor M_7 in the V2I branch. The output of the OTA circuit is connected to the gate of the PMOS transistor M_7 , forming a negative feedback loop. While the loop gain is high enough, the error between V_{bg} and V_s is very small and the voltage V_s is actually fixed to V_{bg} . This allows the transformation from a constant voltage to a constant current by utilizing the low temperature coefficient poly resistor R_7 . The current in the V2I branch can be given by

$$I_{V2I} = \frac{V_{DD} - V_s}{R_7} = \frac{V_{DD} - V_{bg}}{R_7} \quad (7.8)$$

The desired constant reference current can be obtained by simply tuning the resistance of R_7 .

The capacitors C_1 and C_2 are introduced to enhance the stability of the negative feedback loop by improving its phase margin. As shown in Figure 7.5, the phase margin of this loop is almost 90 degrees, ensuring the stability of the loop in the existence of temperature and process variation.

Figure 7.5 Phase Margin of the Close-Loop OTA Circuit

The physical dimension of the MOS transistor M_8 can be sized properly so that the W/L ratio of M_8 to the mirror transistors in the low-noise amplifier stages fits the ratio of the current in the V2I branch to the desired biasing currents for the respective LNA stages. It has been confirmed in simulation that thanks to the bypass capacitors employed in the LNA designs, the introduction of the proposed biasing circuit has virtually no influence on the noise performance of the low-noise amplifiers.

Hence, the proposed CMOS UWB LNA designs can be biased using the proposed DC biasing generation circuit, whose bandgap core circuit provides a 1.1-V reference voltage with ± 60.6 -ppm/ $^{\circ}\text{C}$ temperature coefficient and ± 18.6 -mV/V line regulation while consuming 10-uA biasing current at 1.8-V supply voltage. Better results have been achieved and reported based on CMOS technologies [28][76][77]. The main

cause for the relatively large variation of V_{bg} against temperature lies in the low β value of the bipolar transistor available in the CMOS process. Although the vertical NPN transistor has the best β value among all bipolar devices in this process, its β is still lower than 30 under typical biasing conditions. This low β value indicates higher base current, which introduces substantial mismatch in the collector currents of transistors T_3 and T_4 and hence increases V_{bg} 's variation against temperature and supply voltage.

7.2 ESD Protection Circuits Design

When integrated into a packaged IC product, the low-noise amplifier block has several pins to be connected to the external world. The RF signal received by the external antenna needs to be delivered to the internal LNA input port through an I/O pin; the supply voltage and ground of the LNA may also be delivered externally; moreover, the output of the LNA may be routed out of the package for filtering by an external filter. Consequently, the ESD protection circuits are necessary to be considered in the design of the low-noise amplifier to avoid possible damage to the internal LNA circuit during ESD events.

Several ESD event models have been established, among which the Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) are the most prevalent ones in defining the IC's capability of surviving ESD stress. The HBM, MM and CDM ESD event models are shown in Figure 7.6.

In each ESD event model, the switch is thrown to the left in the initial status and the equivalent ESD capacitor C_{ESD} is charged up to the ESD voltage level V_{ESD} . When the

ESD event happens, the switch quickly turns to the right and the total charge stored on the ESD capacitor is injected into the device-under-test (DUT) through the equivalent series resistance R_{ESD} and the equivalent series inductance L_{ESD} in the discharge path. During an ESD event, the series resistance R_{ESD} generally determines the overshoot current flowing into the DUT, in which the series inductance L_{ESD} is not playing an important role. Hence, since the HBM model has a series resistance of about two orders of magnitude larger than the MM and CDM models, the peaking current in the HBM model is the lowest among the three models under similar ESD stress level.

Model	$C_{ESD}(\text{pF})$	$R_{ESD}(\Omega)$	$L_{ESD}(\mu\text{H})$
HBM	100	1500	7.5
MM	200	Few tens	1~2
CDM	6.8	Few tens	1~2

Figure 7.6 HBM, MM and CDM ESD Event Models

The high transient current makes the real ESD process heavily dependent on the transient conductivity of the metal as well as its change with transient temperature increase; moreover, the transient electro-magnetic field induced by this high current usually makes the transient ESD response quite sensitive to the bonding and packaging conditions. This makes the transient process of the MM model and CDM model ESD events very difficult to predict by conventional circuit simulators, leaving

the HBM model ESD events the most predictable with minimum error among the three models. Hence, due to the lack of access to the more accurate physical-level device simulators, this work takes the HBM model as the testing bench for the ESD protection level estimation of the proposed ESD protection circuits. Precaution has been taken to leave certain margin between the predicted maximum overshoot voltage and the maximum tolerable transient voltage.

The typical ESD protection scheme for one I/O pin is demonstrated in Figure 7.7. The general principle of the protection scheme is that a discharge path should be available between any two I/O pins when the ESD stress is imposed between these two pins, no matter positive or negative.

Figure 7.7 Typical ESD Protection Scheme for I/O Pin

As shown in Figure 7.7, the typical protection scheme comprises two ESD protection devices that are directly connected to the I/O pin and a supply clamp that clamps the voltage drop between the two supply rails. The two ESD protection devices and the

supply clamp are all in off status during the normal operation of the IC to minimize their influence on the performance of the core circuits. However, during an ESD event, some of those devices must be triggered on to conduct the high ESD current before it damages the core circuits. The ESD discharge currents in ESD events, during which the I/O pin experiences positive or negative ESD stress with respect to the VSS rail, are also shown in Figure 7.7 as P1 and P2 respectively. When a positive ESD stress is imposed on the I/O pin with reference to the VSS rail, the upper ESD protection device is turned on and the ESD current is directed toward the VDD rail through the low resistance ESD protection device in on status. This causes a sudden increase on the voltage of the VDD rail and the power supply clamp is triggered on. The power supply clamp in on status creates a low resistance path between the VDD and VSS rails and the ESD current is finally directed to the VSS rail. When a negative ESD stress is imposed on the I/O pin with reference to the VSS rail, the lower ESD protection device is turned on and the ESD current is conducted from VSS rail to the I/O pin directly through the lower ESD protection device before the ESD stress damages the core circuits. The circuit behaviors during ESD events in which the I/O pin experiences positive or negative ESD stress with reference to the VDD rail are largely similar to the cases described above, only that the upper device alone is conducting ESD current under positive ESD stress and the lower device and the supply clamp are conducting ESD current under negative ESD stress.

Between the two ESD discharge paths shown in Figure 7.7, the path P₁ is normally of more concern since two ESD devices are in the discharge path, causing higher series resistance comparing with the path P₂. This high series resistance in the ESD

discharge path directly converts to higher transient voltage overshoot resulted at the I/O pin, which challenges the survivability of the core circuits.

The most widely used ESD protection devices are the diodes, the grounded-gate NMOS (ggNMOS) and the silicon-controlled rectifiers (SCR). The protection mechanism of the diodes can be easily understood. The forward bias region of the diodes is utilized rather than the reverse break-down region. This is because in modern deep submicron CMOS processes the core circuits could have already been damaged when the reverse break-down of the diodes happens. The ggNMOS device is automatically available in CMOS process technology and a single ggNMOS is capable of providing bidirectional ESD protection. While the protection mechanism against negative ESD stress can be easily understood according to the operation principle of the NMOS transistor, the protection against the positive ESD stress involves the reverse break-down of the base-collector junction of the parasitic substrate NPN bipolar transistor in the NMOS transistor. Accurate modeling of the break-down voltage and current conducting capability of the substrate NPN transistor requires careful modeling with an advanced model for the NMOS transistor. The SCR device is basically a PNPN structure with a MOS transistor that can provide bidirectional ESD protection with high area efficiency. However, such structure normally requires careful modeling and characterization before dropping into application and it is also difficult to scale for different protection levels. The power supply clamp can be easily implemented using a large NMOS transistor with an RC timer that can keep the NMOS transistor in off status during normal operation and trigger it into on status transiently during ESD events.

Specifically in the GLOBALFOUNDRIES 0.18- μm RF CMOS process, no SCR devices have been characterized and available for application. Diodes are available; however, all the diodes come in rectangle form and are very area-inefficient. The parasitic capacitances associated with the diodes are also high. This leaves the ggNMOS the only viable option for the implementation of the ESD protection devices in this process. The schematic of the ESD protection circuits for one I/O pin is shown in Figure 7.8.

Figure 7.8 Schematic of the Proposed ESD Protection Circuits

As shown in Figure 7.8, a grounded-gate NMOS and a PMOS with VDD gate connection are used as the ESD protection devices at the I/O pin. Although the ggNMOS itself is a bidirectional ESD protection device that can protect the internal circuit against both positive and negative ESD stresses, the behavior of the ggNMOS during positive ESD stress with reference to ground is not well modeled since it is actually dependent on the behavior of the parasitic substrate NPN bipolar transistor. Hence, the PMOS with VDD gate connection is introduced to establish an explicit

discharge path for positive ESD stress. The supply clamp is composed of a large NMOS transistor M_t with capacitor C_t and resistor R_t to ensure the transient triggering as well as holding of M_t . During normal circuit operation, the gate voltage of M_t is set to 0-V by R_t , ensuring minimum leakage current. During an ESD event when a positive overshoot voltage exists on the VDD rail, the gate voltage of M_t is pulled high since C_t is connected between the two nodes. The time constant of R_t and C_t determines the total period that M_t is turned on and consequently determines the final holding voltage at the I/O pin when the ESD event is over. As simulated, the leakage current of the power supply clamp is less than 5-nA at room temperature.

Table 7.2 summarizes the device values adopted for the proposed ESD protection circuits design.

Table 7.2 Device Values of the Proposed ESD Protection Circuits

Designation	Value
M_P	PMOS, 100- μm /0.18- μm
M_N	NMOS, 100- μm /0.18- μm
M_t	NMOS, 400- μm /0.18- μm
R_{gp}	2.0-KOhm
R_{gn}	2.0-KOhm
R_t	150-KOhm
C_t	10-pF

The size of the NMOS transistor M_t is recommended by GLOBALFOUNDRIES 0.18- μm RF CMOS process design guide, which indicates that a power supply clamp built with 400- μm width transistor is able to pass 2-kV HBM model ESD testing. C_t and R_t are sized so that the RC time constant is about 1.5- μs ; this is to ensure the on period of M_t is long enough so that the residue charge at the I/O pin is not enough to maintain a

holding voltage of higher than 1.8-V, preventing possible latch-up. M_P and M_N are sized as a compromise of the ESD protection level and the parasitic capacitance. Roughly assuming the discharge current spread evenly across the width of the transistor, the 100- μm transistor pair is believed to offer better than 500-V HBM model ESD protection in both directions comparing with the test result of the power supply clamp. The total parasitic capacitance added to the I/O pin node is approximately 0.36-pF, which already brings about noticeable influence to the performance of the internal circuits as will be shown below. The 2-K Ω gate resistors are added to mitigate the transient voltage drop between the gate and the drain node of both MOS transistors, as recommended by the design guide.

Literature shows that for a typical 0.18- μm CMOS technology, the gate oxide, which is normally the most vulnerable part, breaks down at a transient overvoltage of approximately 9-V [78]. The HBM ESD event model has been reproduced in the circuit simulator to find out the maximum transient voltage at the I/O pin under both positive and negative ESD stresses. It is worth mentioning that the simulation results predicted by the circuit simulator are not accurate mainly because of two reasons. First, the current-voltage characteristics of the devices are all measured and modeled under continuous signal condition, which generally underestimate their transient current conducting capability. Moreover, the high ESD current always causes excessive heating along the discharge path, while the circuit simulator is unable to predict the transient response with varying temperature. However, since the actual performance of the ESD protection circuits can only be understood through real experiment and the circuit simulator is currently the only tool available to predict its performance, we will

rely on the result predicted by the circuit simulator to estimate the real protection level of the proposed ESD protection circuits.

Figure 7.9 Transient Response of the ESD Pad to HBM ± 1 -kV Strikes

Figure 7.9 shows the transient voltage response at the I/O pin of the proposed ESD protection circuits with no internal circuits connected. Transient voltage response to both the positive and negative 1-kV HBM ESD events happening at 0.6- μ s have been simulated and shown. Due to the different discharging paths for respective events as discussed earlier, the negative 1-kV ESD stress only induces less than -1-V peak voltage at the I/O pin, while the positive 1-kV ESD stress causes the voltage at the I/O to overshoot to about +6.8-V transiently. The final holding voltage of both positive and negative stress cases are within the ± 1.4 -V range, so the possibility of latch-up is minimized. Hence, the proposed ESD protection circuits are capable of handling ± 1 -kV HBM model ESD events with sufficient margin according to the simulation result.

To evaluate the influence of the ESD protection circuits on the proposed LNA designs, the proposed ESD protection circuits have been attached to each I/O pin of the

proposed LNA design in Chapter 5 and simulated with the parasitic effects extracted. The noise figure performance of the proposed CG2SST LNA with the effect of the proposed ESD circuits is shown in Figure 7.10. As can be observed, while the ESD protection circuits are attached, the 0.36-pF parasitic capacitance directly adds to the source node of the input common-gate stage and significantly lowers the resonant frequency of the input LC tank. Hence, the inductance of the source inductor L_s needs to be reduced to compensate for the additional capacitance. However, L_s cannot be reduced arbitrarily because smaller inductance connected to the source leads to higher signal leakage to ground and hence lowers the gain. Since the total parasitic capacitance brought about by the ESD protection circuits is twice as large as the gate-to-source capacitance of the input MOS transistor, its effect cannot be fully compensated by reducing the source inductance. Consequently, although the noise figure of the full circuit is the same or even better comparing with the noise figure of the proposed CG2SST LNA alone at low frequencies, it increases faster as the frequency increases, which can be understood easily while referring to Equation (5.24).

Due to the same reason, the input matching quality of the proposed CG2SST LNA design is also significantly degraded with the introduction of the ESD protection circuits, as shown in Figure 7.11. The matching quality is still good at low frequencies, however, the upper bound for the -10-dB input matching bandwidth is reduced to 7-GHz due to the additional capacitance introduced by the ESD protection circuits.

Figure 7.10 Simulated Noise Figure of the CG2SST UWB LNA with and without ESD Protection Circuits

Figure 7.11 Simulated Input Reflection Coefficient of the CG2SST UWB LNA with and without ESD Protection Circuits

Figure 7.12 shows the influence of the ESD pad on the forward gain of the proposed LNA design. It is clear that the forward gain degraded at high frequencies after adding the ESD protection circuits to the LNA. The parasitic capacitance at the input node is partially responsible for this change, while the parasitic capacitance at the output node further contributes to the gain degradation at high frequencies.

Figure 7.12 Simulated Forward Gain of the CG2SST UWB LNA with and without ESD Protection Circuits

It is obvious that the excessive parasitic capacitance brought by the ESD protection circuits has deteriorated the wideband nature of the proposed UWB LNA design as well as its noise performance. To mitigate this effect, the PMOS transistor serving as the upper ESD protection device can be removed after the behavior of the substrate NPN bipolar transistor in the ggNMOS transistor is well understood and modeled. Moreover, highly parasitic-economical ESD protection diodes can be designed by engineering its physical dimension and doping concentration [39][79].

Figure 7.13 shows the layout and the micro-photo of the proposed ESD protection pad. The proposed ESD protection pad has been employed in one project where the die needs to be bonded-out and packaged. It is verified through board-level testing that the circuits with the proposed ESD protection pads are working properly as expected. However, due to the limitation of ESD measurement equipment, the ESD protection level and the associated parasitic capacitance value cannot be measured.

Figure 7.13 Layout and Micro-Photo of the Proposed ESD Protection PAD
(a) Layout (b) Micro-Photo

7.3 Summary

The DC biasing generation circuits and the ESD protection circuits based on GLOBALFOUNDRIES 0.18- μm RF CMOS process technology are proposed in this chapter. It is found that DC biasing generation circuits can be directly integrated with the proposed LNA designs without any degradation on its performance. However, since ggNMOS is the only available ESD protection device in this process, the matching, forward gain and noise performance of the proposed UWB LNAs have to be compromised by the introduction of the ESD protection circuits.

CHAPTER 8 Conclusions and Recommendations

This chapter concludes the research work presented in this thesis and recommends the direction for future research work.

8.1 Conclusions

This thesis focuses on the design and implementation of the CMOS low-noise amplifiers for ultra-wideband applications. The investigated circuit topologies for the input stage of the LNA include the source inductive degeneration architecture and the common-gate architecture, both of which are demonstrated to be eligible for the design of a UWB LNA.

A new UWB LNA design based on the source inductive degeneration architecture is proposed. The relationship between the matching bandwidth and the source and gate inductance are discovered. The feedback technique for input matching bandwidth extension is introduced and analyzed. Noise factor expression for this architecture is derived, including the effect of the induced gate noise. The noise optimization techniques are proposed based on the noise factor expression. The measurement result shows the single stage LNA has a 6.0-GHz bandwidth with 17.5-dB maximum in-band gain and 1.8-dB minimum in-band noise figure, while only drawing 4.8-mA from a 1.8-V supply. This work clearly demonstrates that the source inductive degeneration architecture, which is commonly believed to be narrow-band design architecture, can be adopted in wideband LNA designs.

Another UWB LNA design based on the common-gate architecture is also proposed. The technique to improve matching bandwidth is discovered for this architecture. The noise factor expression for this architecture is derived, based on which the optimization techniques are proposed. The two-stage staggering-tuning technique is introduced to extend the bandwidth of the LNA design as well as increase the gain for the common-gate stage. The measurement result shows the two-stage LNA has 5.3-GHz bandwidth with 19.8-dB maximum in-band gain and 3.2-dB minimum in-band noise figure, while drawing total current of 5.6-mA from a 1.8-V supply. This work demonstrated that the common-gate input architecture, which is known to be quite noisy and thus not adopted as the input stage of conventional LNA designs, is capable of satisfying the UWB LNA specifications while adopting the new design techniques.

To further extend the bandwidth to cover the entire UWB operation frequencies, a three-stage common-gate LNA utilizing the staggering-tuning technique is reported. From the post-layout simulation result, the 3.1 to 10.6-GHz full UWB operation frequency can be covered. A variable gain technique is incorporated in the design to enhance the dynamic range of the UWB receiver employing this LNA design.

The proposed LNA designs are compared with the reported work in literature in Table 8.1, where a figure-of-merit (FOM) is proposed to evaluate the overall performance of the wideband low-noise amplifiers implemented using different process technologies. The FOM is devised as

$$FOM = \frac{S_{21, \max, abs} \times BW_{GHz}}{(F_{\min} - 1)I_{DC, mA}} \quad (8.1)$$

where $S_{21,\text{max,abs}}$ denotes the maximum absolute in-band forward gain, BW is the bandwidth of the LNA in GHz, F_{min} is the minimum in-band noise factor and $I_{\text{DC,MA}}$ is the DC current consumption of the LNA. This FOM includes only the most important performance parameters of a low-noise amplifier for a low-cost low-power UWB receiver. The DC current consumption is employed as the parameter to indicate the power consumption for a fair comparison; this is because the LNA designs using different technologies usually adopt different supply voltages required by their respective process technologies.

Of the three proposed CMOS UWB LNA designs, the SIDFB UWB LNA takes advantage of the low noise input matching architecture and exhibits the lowest noise figure among the three designs; it also consumes the lowest power since it only contain one amplification stage. However, it is quite difficult to obtain wider bandwidth or higher gain using this architecture due to the stringent trade-offs within a single stage. On the other hand, the CG2SST and CG3SST UWB LNAs exhibits a little higher noise figure due to the adoption of the common-gate input architecture; their power consumptions also increase since two and three stages are employed respectively. Nevertheless, both the achieved gain and bandwidth increase with the addition of amplification stages. It can also be observed that with the cascading of more amplification stages, the linearity of the UWB LNA degrades with increased overall gain. The silicon area of all the three designs are actually all limited by the inductors employed in the designs; since the three proposed CMOS UWB LNA designs all uses only three to four inductors, their required silicon area are similar and small. As shown in Table 8.1, the proposed SIDFB UWB LNA exhibits the best FOM

among the listed UWB LNA work; the CG2SST and CG3SST UWB LNAs possess similar FOMs and are both better than the listed UWB LNA works based on 0.18- μm CMOS process technologies.

The design of auxiliary circuits to the critical RF circuits in the low-noise amplifier designs, namely the DC biasing generation circuits and the ESD protection circuits, are also reported.

Finally, Appendix A summarize the UWB regulation status in the countries and areas other than the United States; Appendix B and Appendix C summarize the measurement setup and the technique to measure the 3rd-order intercept point for the LNA design, respectively.

Table 8.1 Comparison of the Proposed UWB LNA Designs with the Reported Work

Ref	Technology	Frequency (GHz)	NF (dB)	S11 (dB)	S21 (dB)	ICP1 (dBm)	IIP3 (dBm)	Power Consumption	Area (mm ²)	FOM (GHz/mA)
[58]	0.15 μ m pHEMT	3.1~10.6	3.4~4.0	<-8	12.0~13.0	n/a	n/a	4.3mA@3V	2.25	6.56
[63]	0.35 μ m SiGe BiCMOS	3.0~11.6	2.5~7.1	<-9	23.1~26.1	-26@5GHz	-17@5GHz	15.3mA@1.7V	0.22	14.58
[80]	0.25 μ m SiGe BiCMOS	3.1~10.6	2.8~4.7	<-12	18.5~20.0	n/a	-8@3.2GHz	11.1mA@2.7V	0.34	7.47
[71]	0.18 μ m SiGe BiCMOS	3.0~10.0	2.5~4.2	<-9	18~21	-11.8@3.4GHz	-5.5@3.4/3.6GHz	10mA@3V	1.8	10.10
[81] LNA1		3.0~10.0	3.4~4.7	<-11	16.4~18.0	n/a	n/a	9mA@2.5V	0.53	5.20
[81] LNA2		3.0~10.0	3.05~4.5	<-13	19.8~20.8	n/a	-11.7	17mA@2.5V	0.53	4.44
[64]		2.0~10.0	2.9~3.3	<-5	10.0~13.0	-17~-14	-7~-4	4mA@2.4V	0.88	9.40
[82]	0.18 μ m CMOS	2.4~5.4	2.85~4.5	<-10	20~23	-22.0@4GHz	-14.0@4GHz	13mA@1.8V	1.04	3.51
[83]		1.2~11.9	4.5~5.1	<-11	6.7~9.7	n/a	-6.2@6GHz	11.1@1.8V	0.59	1.62
[84]		3.4~11.0	3.1~6.0	<-8	13.5~16.0	n/a	-7@6GHz	6.6mA@1.8V	1.2	6.97
[61]		0.4~10.0	4.4~6.5	<-10	11.2~12.4	-15@6GHz	-6@6GHz	6.7mA@1.8V	0.42	3.41
[55]		2.7~9.1	3.8~6.9	<-10	6.3~9.3	n/a	1@4GHz	11.7mA@0.6V	1.57	1.14
[85]		3~5&6~10	4.0~7.8	<-10	14~20.3	n/a	-14.3~-12.1	13.3mA@1.8V	1.43	3.60
[86]		2.8~7.2	3.0~3.8	<-4	16.1~19.1	n/a	-1@6GHz	17.8mA@1.8V	1.63	2.24
[62]		3.1~10.6	3.8~4.0	<-10	13.0~16.0	n/a	n/a	5.3mA@1.8V	0.98	6.38
[68]		3.1~10.6	4.1~5.2	<-9.7	11.0~11.8	-7.9@6.4GHz	0.7@6.4GHz	8.2mA@1.9V +7.1mA@1V	0.45	1.21

[87]	0.13 μ m CMOS	2.0~5.2	4.7~5.7	<-9	15.5~16.5	-24	n/a	19mA@2V	0.24	0.58
[72]		3.1~4.8	3.5~5.3	<-10	12.5~15.5	-6@3.1GHz	-0.8@3.1GHz	11mA@1.5V	1.08	8.17
[59]		3.1~10.6	2.1~3.0	<-10	13.7~16.5	n/a	-8.5~-5.1	7.5mA@1.2V	0.87	10.74
[73]		6.0~10.0	3.5~4.8	<-8	26.6~28.1	n/a	n/a	11.7mA@1.2V	0.4	7.01
[60] LNA1	90 nm CMOS	0.5~7	2.3~2.9	<-5	19.0~22.0	n/a	-8.8@5.8GHz	10mA@1.2V	0.012	11.72
[60] LNA2		4~8	2~2.4	<-5	21.4~24.4	n/a	-7.7@5.5GHz	7.7mA@1.2V	0.022	14.74
[65]		0.1~8.0	3.4~5.8	<-10	13.0~16.0	n/a	-9dBm	12mA@1.2V+ 1mA@1.4V	0.034	3.68
[79]	65 nm CMOS	2.6~6.6	4.0~6.5	<-13	10.8~13.8	-17.6@4GHz	n/a	5.7mA@1.2V	1	2.27
SIDFB LNA*	0.18 μ m CMOS	2.0~8.0	1.8~4.8	<-8	14.5~17.5	-12.7@3.5GHz	-2.2@3.2GHz	4.8mA@1.8V	0.5	18.25
CG2SST LNA*		4.0~9.3	3.2~6.6	<-9.8	16.8~19.8	-15.0@6GHz	-5.7@6GHz	5.6mA@1.8V	0.59	8.65
CG3SST LNA*		3.1~10.6	3.5~6.9	<-9	19.2~20.9	-17.5@7GHz	n/a	8.0mA@1.8V	0.5	8.39

*: design in this work

8.2 Recommendations and Future Work

As reported in Chapter 4 and Chapter 5, both the source inductive degeneration and the common-gate input architectures are capable of achieving several GHz operation bandwidth with less than 10-mW power consumption. The measured noise figure is better in the LNA design based on the source inductive degeneration architecture. It is believed that the on-chip source and gate inductors degrade the overall noise performance since they are integrated on wafer and have relatively low quality factors. As discovered in Chapter 4, to achieve wideband matching bandwidth, the sum of the two inductors needs to be small. Consequently, it is desirable from the noise's perspective to implement the two small inductors using bonding wires available in the packages, which generally have higher quality factors. The load inductors can be integrated on wafer since they have relatively large inductance, while low quality factor is acceptable and even preferable considering the bandwidth.

As can be concluded from the measured noise figure plots, the induced gate noise plays an important role on the noise figure of the low-noise amplifiers at higher frequencies. To allow the accurate estimation of noise figure by the circuit simulator, the MOS transistor model is preferable to be upgraded to newer versions, in which the induced gate noise can be properly modeled. Verification of the noise factor derivations in this work with the simulation results that take the induced gate noise into consideration will be interesting.

Finally, improving the ESD protection solution on this RF CMOS process technology is necessary for commercializing the UWB receivers employing the proposed LNAs.

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- Y. Lu, K. S. Yeo, J. G. Ma, M. A. Do, and Z. Lu, "1.8-V 3.1-10.6-GHz CMOS Low-Noise Amplifier for Ultra-Wideband Applications", Microwave and Optical Technology Letters, Volume 44, Issue 3, Feb. 2005, Pages 299-302.
- Y. Lu, J. M. Gu, K. M. Lim, and K. S. Yeo, "A 4.0-9.3-GHz Wideband CMOS Low-Noise Amplifier Exploiting Staggering-Tuning Technique", submitted to IEEE Microwave and Wireless Components Letters
- Y. Lu, J. M. Gu, K. M. Lim, and K. S. Yeo, "Bandwidth Extension Techniques for CMOS Low-Noise Amplifiers", to be submitted to IEEE Transaction on Circuits and Systems-I: Regular Papers

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- Y. Lu, K. S. Yeo, J. G. Ma, M. A. Do, and Z. Lu, "A CMOS Low-Noise Amplifier For 3.1-10.6GHz Ultra-Wideband Applications", Asia Pacific Microwave Conference (APMC-2004), 15-18 Dec. 2004, Delhi, India.

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- J. N. Yan, K. X. Ma, K. S. Yeo, K. M. Lim, J. M. Gu, Y. Lu, W. M. Lim, and H. Yu, "A Wideband Active Gilbert-cell Ku-Band SiGe BiCMOS Up-Conversion Mixer with Low LO Drive Power", International Conference on High-Speed Circuits Design (HSCD'10), 25-26 Oct, 2010, Taichung, Taiwan

- B. K. Thangarasu, K. X. Ma, K. S. Yeo, S. X. Mou, N. Mahalingam, J. M. Gu, K. M. Lim, Y. Lu, and H. Yu, "A DC to 4 GHz Fully Differential Wideband digitally

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APPENDIX A Worldwide Regulation Status of UWB Operation

The regulation status of the world's major wireless markets is reviewed in this section, except that of the United States', which is introduced in detail in Chapter 2.

1. Japan

Japan started studying of UWB radio systems ever since September 2002; and in August 2006, the Ministry of Internal affairs and Communications (MIC) of Japan formally announced the approval of UWB operation in Japan under MIC's rulings [2].

According to MIC's first ruling and its subsequent revisions, the UWB signal is defined as any signal with its -10-dB bandwidth larger than 450-MHz and in-band average emission power spectral density below -41.3-dBm/MHz. In Japan, the allocated spectrum for UWB signal transmission comprises two separate bands, namely 3.4-4.8-GHz and 7.25-10.25-GHz.

Aside from the different operation spectrum comparing with the FCC's UWB regulation, some other differences are worth mentioning. First of all, MIC's regulation allows the UWB radio systems to operate indoors under the host-client network topology only. The host devices must be mains powered with the client devices allowed to be battery powered. The designated network topology does not contribute to critical implementation barrier; however, the MIC is showing its explicit intention to keep all UWB transmission indoors. Moreover, the MIC has also required the implementation of Detect-And-Avoid (DAA) mechanism should the UWB device work up to the maximum allowed transmission power spectral density in certain part

of its allocated spectrum as an interference-mitigation practice. The DAA mechanism requires the UWB device to be able to detect the presence of any wireless signal from incumbent wireless systems in the air before transmitting the UWB signal. If such signal is detected, the UWB device should avoid operation in the band of the existing signal to minimize possible interference. According to MIC's regulation, the DAA implementation is mandatory for the 3.4-4.2-GHz; and for 4.2-4.8-GHz, DAA will be mandatory after the year of 2010. If DAA is not implemented in a UWB device, the maximum allowed emission power spectral density is reduced to only -70-dBm/MHz, which will greatly reduce the transmission distance and data throughput. The 3-GHz UWB spectrum from 7.25-GHz to 10.25-GHz is not subject to the DAA requirement.

2. Korea

The Ministry of Information and Communication of Korea (now the Korea Communications Commission, KCC) announced distribution of UWB frequency channels in July 2006. Similar to Japan's UWB frequency planning, the Korean UWB frequency band is divided into one lower band (3.1-4.8-GHz) and one higher band (7.2-10.2-GHz).

However, the Korean UWB regulation supports both indoor and outdoor UWB system operation. DAA is also required to allow the device to transmit the maximum allowed power spectral density in certain part of the approved spectrum. It is immediately required for the 3.1-4.2-GHz band and for the 4.2-4.8-GHz band, DAA will be required after June 2010. Similarly, DAA is not required for UWB operation in the higher band. While operating in the frequencies that require DAA mechanism, a UWB

device without DAA implementation could either work in a low power mode or in a low duty cycle mode. The low power mode defines a maximum in-band emission level of -70-dBm/MHz, which is the same as in the Japanese UWB regulation. The low duty cycle mode allows device without DAA implementation to transmit under -41.3-dBm/MHz emission limit, but such transmission should last no more than 5-ms after a non-transmission period of no less than 1-s. Consequently, the data transmission distance and throughput are also greatly reduced without the implementation of the interference-mitigation mechanisms according the Korean UWB regulation.

3. European Union

On 21 February 2007, the Commission of the European Communities announced its decision to allow the use of UWB signal transmission in a harmonized manner in the community [3]. In the May of the same year, the Commission issued the first edition of the details of the operation regulations for UWB networking in Europe. The technical investigations have continued to be conducted afterwards to re-evaluate the interference-free UWB power emission limit and define certain mitigation mechanisms. According to the latest technical update decided by the Commission in April 2009 [4], a lower band of 3.1-4.8-GHz and a higher band of 6.0-9.0-GHz were approved for UWB operation with implementation of certain interference-mitigation mechanisms for some part of the approved spectrum. As defined in the Commission's regulations, the appropriate interference mitigation mechanisms include the Low-Duty-Cycle (LDC) technique and the Detect-And-Avoid (DAA) technique. The LDC technique restricts the UWB device to emit power up to a maximum average EIRP

density of -41.3-dBm/MHz with a maximum peak EIRP power of 0-dBm in 50-MHz by reducing to transmission duty cycle to less than 5 percent of the time in each second and less than 0.5 percent of the time in each hour with a maximum single transmission period of 5-ms. The DAA technique requires the UWB device to detect any other existing signal of other wireless systems in the operation bandwidth before transmitting; UWB transmission in the corresponding band can be carried out only if no wireless signals of other systems are detected [4].

The approved UWB spectrum allocation by the Commission is detailed as follows.

The 3.1-4.2-GHz band can be operable to maximum average emission power spectral density of -41.3-dBm/MHz with LDC or DAA implemented; otherwise, the maximum allow emission level is -80-dBm/MHz in 3.4-3.8-GHz and -70-dBm/MHz in 3.1-3.4-GHz and 3.8-4.2-GHz.

The 4.2-4.8-GHz band can operate up to -41.3-dBm/MHz without LDC and DAA implemented till the end of year 2010; after 2010, the device needs to operate with LDC or DAA mechanism to remain the same transmission power level, otherwise it can only operate up to -70-dBm/MHz power limit.

The 6.0-8.5-GHz band can operate up to -41.3-dBm/MHz with no interference mitigation mechanism implemented without deadline.

The 8.5-9.0-GHz band can operate up to -41.3-dBm/MHz only if DAA mechanism is implemented in the UWB device, otherwise the maximum power emission limit is reduced to -65-dBm/MHz.

The EC's UWB regulation does not only allow use of UWB system indoors, but also outdoors and in automotive and railway vehicles; however, the outdoor UWB system should not be operated at a fixed location or with a fixed antenna.

4. China

The Ministry of Industry and Information Technology (MIIT) of China allocated spectrum for UWB transmission in December, 2008 [5]. China's UWB regulation defines the UWB signal to be any signal with -10-dB bandwidth of no less than 500-MHz with certain power spectral density requirements. The allocated UWB spectrum is divided into a lower band (4.2-4.8-GHz) and a higher band (6.0-9.0-GHz). In the lower band, the UWB system can transmit up to -41-dBm/MHz without any mitigation mechanism until end of 2010; mitigation mechanism must be implemented to qualify for the same power emission level after 2010, otherwise the maximum emission power spectral density will be reduced to -70-dBm/MHz. The high band is not subject to any mandatory implementation of the interference-mitigation mechanisms. Both indoor and outdoor UWB system operation are supported by China's regulation, but operation on aircraft or within 1 kilometer of radio astronomical observatory is prohibited.

The summary of those regulations is shown in Figure A.1, where the UWB spectrum allocation and the portion imposed of implementation of interference-mitigation mechanisms can be compared, including the UWB regulation of the United States'.

Figure A.1 Comparison of the UWB Spectrum Allocation of World's Major Wireless Markets

APPENDIX B Measurement Setup for S-Parameters, Noise Figure, 1-dB Compression Point and 3rd-Order Intercept Point

This section describes the measurement setups to characterize the fabricated low-noise amplifier. The LNA is characterized in its die form and all the measurements are performed on Cascade Microtech's probe station with the LNA bare die hold in the micro-chamber. GSG RF microwave probes from Cascade Microtech are employed to establish low-resistance contacts between cables and the input and output pads of the LNA. The HP 11612B 45-MHz~50-GHz Bias Networks are used both at input and output of the LNA to implement DC blocking.

The key performance parameters measured are listed as follows.

1. S-parameters (input matching, output matching, forward gain, reverse isolation)
2. Noise figure
3. 1-dB compression point
4. 3rd-order intercept point

The measurement setups for those parameters will be discussed in detail one by one.

1. S-Parameters Measurement

The S-parameters are generally measured by the Vector Network Analyzer (VNA). In the measurement of the LNA, we use HP 8510C Network Analyzer to control the HP 8517B S-Parameter Test Set and the HP 83650B Synthesized Sweep Signal Generator.

The HP 8510C Network Analyzer also receives and analyzes the down-converted signal and subsequently calculates and displays the S-parameter measurement results. The measurement setup for S-parameters is briefly shown in Figure B.1, with DC biasing not shown.

Figure B.1 Equipment Setup for S-Parameter Measurement

The HP 8510C Network Analyzer and the HP 83650B Synthesized Sweep-Signal Generator share the same reference clock for clock synchronization. The HP 8510C also controls the sweeping action of the HP 83650B, whose output is fed into HP8517B S-Parameter Test Set as the incident signal. The HP8517B delivers the incident wave to the DUT through the GSG probe and monitors the reflected and transmitted signals, both of which are down-converted by HP8517B to 20-MHz IF

signal and delivered back to the HP 8510C for processing. The S-parameters are analyzed and calculated by the HP 8510C Network Analyzer and the calculated data is captured on the workstation by Agilent's IC-CAP software through the General Purpose Input Output (GPIO) port connection between the HP8510C and the workstation.

Since the on-wafer standard open-short-load structures are adopted in the calibration stage, the measured S-parameters shown in the IC-CAP are directly the S-parameters of the on-wafer LNA (including the effects of input and output pads). No extra de-embedding effort is needed regarding the cable or probe losses.

2. Noise Figure Measurement

The noise figure is generally measured using a noise figure meter. In the measurement of the LNA, we use the HP 8970B Noise Figure Meter to analyze the noise performance of the DUT and calculate the noise figure. Since the HP 8970B can only operate in the 10-1600-MHz frequency range, the HP 8971C Noise Figure Test Set is introduced, which extends the measurable limit to 26.5-GHz. An Agilent 346C Noise Generator is connected to the HP 8971C as the noise source. The noise signal generated by the Agilent 346C is fed into the 2-26.5-GHz ATN Remote Receive Module (RRM), which is controlled by the ATN NP5B Noise Parameter Test System. The RRM is a solid-state impedance tuner, which serves as the source impedance puller here to assist finding the noise-optimum source impedance. The noise signal after the ATN RRM is applied to the DUT and the output signal is delivered back to HP 8971C, which down-converts the output signal and delivers the IF signal to HP

8970B for further processing. The measurement setup for the noise figure is briefly shown in Figure B.2, with DC biasing not shown.

As shown in Figure B.2, the noise generated by the Agilent 346C noise generator is applied to the DUT through the ATN RRM to transform the source impedance; the output noise from the DUT is down-converted by the HP 8971C and delivered to HP 8970B for analysis and calculation. A workstation computer is controlling the measurement equipment throughout the measuring process through GPIO port connections and the noise figure measurement data can be obtained from the workstation. Again, since the standard on-wafer short structure is adopted in the calibration stage, the noise figure obtained is directly the noise figure of the on-wafer LNA (including the effects of input and output pads). No extra de-embedding effort is needed regarding the cable or probe losses.

Figure B.2 Equipment Setup for Noise Figure Measurement

3. 1-dB Compression Point Measurement

The 1-dB compression point is measured strictly according to its definition. A sinusoidal single tone at the desired frequency is applied to the DUT from a signal generator and the output signal at the same frequency is measured by a spectrum analyzer. The small signal gain is calculated by subtracting the output power (in dBm) with the input power (in dBm). While the power level of the input signal increases, the gain starts to be compressed. The input signal power level where the gain compressed exactly 1-dB comparing with the small signal gain is taken down as the input-referred 1-dB compression point. The RS SMF 100A Microwave Signal Generator and the HP 8563E Spectrum Analyzer are used in the measurement. The measurement setup for the 1-dB compression point is shown in the Figure B.3, with DC biasing not shown.

Figure B.3 Equipment Setup for 1-dB Compression Point Measurement

Under this circumstance, it is important to find the actual losses of the cables and probes at the input to de-embed those losses and find out the actual signal power level that is delivered into the DUT.

4. 3rd-Order Intercept Point Measurement

The 3rd-order intercept point measurement is performed according to the methodology described in Appendix C. Two independent signal generators are employed to generate two uncorrelated sinusoidal single tones, which are combined together by a signal combiner and delivered to the DUT, the 1st-order and 3rd-order tones are observed at the output of the DUT from the spectrum analyzer. The RS SMF 100A Microwave Signal Generator and the RS SMBV 100A Vector Signal Generator are used as two independent signal sources; the HP 8563E Spectrum Analyzer is utilized at the output to observe the fundamental signal and the IM3 signal levels. The measurement setup for the 3rd-order intercept point is shown in Figure B.4, with DC biasing not shown.

The two single tones are attenuated by 10-dB and combined by the ANAREN RF signal combiner; the combined signal is then applied to the input of the DUT and the output of the DUT under two-tone stimulus can be observed in the HP 8563E. The purpose of using the attenuators is to attenuate the interfering signals at the output of one signal generator, which may be coupled from the other signal generator during the

combining process. Such coupling interferers would cause inaccurate output signal level as well as additional IM3 components from the signal generator.

Figure B.4 Equipment Setup for 3rd-Order Intercept Point Measurement

Under this measurement setup, it is important to measure the combined two-tone signal before it is applied to the input of the DUT. By doing this, the losses of the cables, attenuators and the combiners are de-embedded, and the actual signal level applied to the input of the DUT can be understood. The signal generators can be adjusted slightly for the difference in cable and combiner losses to ensure the two tones delivered to the DUT have the same power level. The input-referred 3rd-order intercept point can be calculated easily after obtaining the actually input power level and the power level difference between the 1st-order and 3rd-order tones at the output according to the methodology described in Appendix C.

APPENDIX C 3rd-Order Intercept Point Measurement Method

The 3rd-order intercept point is an important figure of merit in describing the linearity of a RF circuit block, a RF sub-system or even a complete receiver/transmitter chain. The 3rd-order intercept point is defined as the point where the linear 1st-order signal power equals the linear 3rd-order signal power at the output of a non-linear circuit block. When the power is referred at the input port, it is input-referred 3rd-order intercept point (IIP3); when the power is referred at the output port, it is then output-referred 3rd-order intercept point (OIP3).

Obviously, IP3 cannot be acquired according to its definition in real experimental measurement. Since the IP3 is approximately -9.6-dB higher than the 1-dB compression point, the 1st-order signal power will also be substantially compressed at the linear intercept point. Consequently, the IP3 can only be acquired by extrapolation. Traditionally, multiple points of the 1st-order and 3rd-order signal powers are measured at relatively low-power levels; those points are then plotted on a X-Y coordinate system and extrapolation is done based on those points to find the IP3.

As a matter of fact, the IP3 can be measured by only taking one point in the low power range where the 1st-order and 3rd-order signal powers are mostly linear. Figure C.1 shows the relationship between the linear 1st-order signal power line (as well as a “bend” in real case where gain compresses at high input power), the linear 3rd-order signal power line, the input-referred IP3 and the output-referred IP3.

Figure C.1 IP3 Relationship and Measurement

In the X-Y coordinate system, the X axis denotes the input power level and the Y axis denotes the output power level, both in dBm. So the 1st-order linear signal power line can be expressed by

$$Y = X + G \quad (\text{B.1})$$

where X is the input test tone power, Y is the output test tone power and G is the small signal gain of the DUT.

The 3rd-order linear signal power line can be expressed by

$$Y = 3 * X + T \quad (\text{B.2})$$

where X is the input power of each test tone, Y is the output power of each 3rd-order inter-modulated tone and T is a fitting parameter. According to its definition, the IIP3

and OIP3 are solutions to X and Y when the two equations above are listed together as an equation set.

So we have

$$OIP3 = IIP3 + G \quad (B.3)$$

$$OIP3 = 3 * IIP3 + T \quad (B.4)$$

Solving the equation set for IIP3, we have

$$IIP3 = (G - T) / 2 \quad (B.5)$$

This suggests that we only need to know the difference between G and T before calculating the IIP3, rather than their absolute values.

As shown in Figure C.1, we take only one point test at input test tone level of X0, which is exactly within the DUT's linear input range. It is easy to read the power of the test tones (Y1) and the power of the IM3 component (Y3) at the output. According to Equation (B.1) and Equation (B.2), we have

$$Y1 = X0 + G \quad (B.6)$$

$$Y3 = 3 * X0 + T \quad (B.7)$$

Based on this, we can easily get

$$G - T = 2 * X0 + Y1 - Y3 \quad (B.8)$$

So we have

$$IIP3 = (G - T) / 2 = X0 + (Y1 - Y3) / 2 \quad (B.9)$$

This indicates that IIP3 can be calculated by testing at only one input power point. Two single tones at same small power level $X0$ dBm is applied at the DUT input and at its output, the power level at the either test tone frequency ($Y1$) is read as well as the power level at either of the two IM3 frequencies ($Y3$). The input-referred 3rd-order intercept point can be calculated just based on those input stimulus power level and output readings at one power level point. The output-referred 3rd-order intercept point can be calculated by simply adding small signal gain G to IIP3, which is just $Y1 - X0$.

For sure, certain rules need to be applied when utilizing this IP3 measurement technique to guarantee its accuracy. First, the input signal power level for the test tone needs to be exactly within the linear range where the point falls nicely on the 1st-order and 3rd-order lines in Figure C.1. This requires the measurement of input-referred 1-dB compression point in advance, which is relatively easy. With about 20-dB back-off from the input-referred 1-dB compression point, it is sure that the input test tone levels are well within the input linear range. Second, the 3rd-order inter-modulation components at the DUT output should be at least 20-dB higher than the spectrum analyzer's noise floor in order to get accurate power readings. Fortunately, the signal generators ensure that the frequencies of the test tones are very accurate and the frequencies of the output IM3 components can be accurately predicted to observe the signal in a narrow frequency span and low resolution bandwidth (RBW) for a low noise floor of the spectrum analyzer.