65 nm BEOL electro-copper plating gap fill capability study

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2011

Deng, F. (2011). 65 nm BEOL electro-copper plating gap fill capability study. Master' s
thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/43218>

<https://doi.org/10.32657/10356/43218>

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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ENGINEERING**

A thesis submitted to the Nanyang Technological University
In fulfillment of requirement for the degree of
Master of Engineering

2011

Acknowledgments

This is an UMC-EDB-NTU joint Master of Engineering program. I would like to express my heartfelt thanks and appreciation for the financial and facilities support received from United Microelectronics Corporation (Singapore Branch) (UMC), Singapore Economic Development Board (EDB) and Nanyang Technological University (NTU).

I express sincere gratitude to my NTU supervisor, A/P Zhang Dao Hua. I deeply appreciate all the academic guidance, encouragement, and advices received from him.

I would like to forward my appreciation to my UMC department manager Liao Hong, section manager Hu Hang, Rios Chen, mentor Wang Qin, Wang Xiao Guang, Zhang Ju Bao, and Zhang Yi Yi, who have been helpful in providing me the essential knowledge, enumerable assistance and great supports during doing this project in UMC. I am greatly benefited from their patient instructions and direction.

Finally, I thank UMC PEI (process engineering integration) and other module engineers who involved in this project, without their kindness and help, the project will not be so harmonic.

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Summary

The objectives of this project include reducing Cu void defects, prolonging metal electromigration (EM) lifetime and improving wafer yield. As a result of the project, the Ta/TaN/Ta tri-layer barrier in the advanced direct contact via (ADCV) structures, via bottom removal and 3-step Cu seed for dual damascene (DD) Cu metallization were studied and implemented successfully in 65 nm technology-node products.

The comparative study of the samples with the tri-layer and bi-layer barriers shows that the samples with tri-layer barrier have lower defective die percentage. Downstream EM test reveals that the samples with tri-layer barrier have downstream EM lifetime three times more than those of the samples with bi-layer barrier.

ADCV structures with three different via bottom removals were comparatively investigated. Median removal in the ADCV split is found to result in the lowest defective die percentage. Meanwhile, the highest activation energy and the longest downstream EM lifetime are achieved with this process. However, it exhibits median via contact resistance as the tradeoff to the longer EM lifetime.

The metal lines with 3-step Cu seed layer with ac deposition powers of 0:500:1000 W (time ratio of 1:1:1) show a smaller average metal line leakage current than those with 2-step Cu seed layer with ac deposition powers of 500:1000 W (time ratio of 1:2). The

metal line sheet resistances and metal via contact resistances are comparable for the two kinds of Cu seed. For the samples with 3-step Cu seed layer, the average defective die percentages is 3% lower and the average yield is 0.5% higher than those with 2-step Cu seed layer. TEM images show that the 3-step Cu seed can have better barrier continuity at the point film among the barrier layer, tetra-ethyl-ortho-silicate (TEOS) and low k (LK) dielectric layers, and the Cu seed step coverage is also improved at the kink location with slightly less overhang.

These observations are of great value for optimization of barrier and seed processes in multilevel interconnects of nanoscale integrated circuits.

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Chapter 1 Introduction

1.1 Motivation

The semiconductor industry always tends to develop more powerful integrated circuits (ICs). This approach mainly focuses in two directions. One is to increase the speed of individual transistors through a continual reduction in the minimum dimension size of device features. And the other is to develop increasingly complex interconnect systems which use multi-layer structures of metal wiring separated by an inter layer dielectric (ILD) or inter metal dielectric (IMD). Scaling down the feature sizes in microelectronic circuits has shown efficiency in improving circuit performance and increasing yield at lower cost per function on chip. Since early 1970s, by reducing the transistor gate size about 30% every technology node, the industry remarkably doubled the device speed roughly every two years. In the back end of line (BEOL), the reduction in transistor dimension has been accompanied by the scaled reduction in interconnect feature size. The reduction in conductor cross-sectional area results in increased wire resistance, while the reduction in inter-conductor distance induces increased line capacitance and power dissipation. The interconnect signal delay, characterized by the resistance capacitance (RC) time constant, was essentially required to keep at lower range. Therefore, good conductivity metal and multi-layer structure are likely to be few of the most efficient

solutions. Some of today's advanced logic devices have as many as seven to eight layers of interconnect with minimum wire width and space of about 90 nm or even below [1, 2].

In the past several years, aluminum and its alloys had been widely used for contacts and interconnections in ICs. As the downscaling of metal interconnect line width and increasing of the electrical current density results in large RC time delay along with enhanced electromigration (EM) and stress-introduced void failures [3-6], the aluminum metallurgy may become inadequate. To solve these functionality and reliability problems, copper (Cu) metallization is used to replace Al metallization for deep submicron ICs (i.e., $<0.18\ \mu\text{m}$) due to its higher conductivity and higher resistance to electromigration. Major Cu metallization processes are single damascene (SD), dual damascene (DD) formation process (i.e., dielectric layer deposition and etching), barrier deposition, Cu seed deposition, electro copper plating (ECP) and chemical mechanical planarization (CMP). The concern for Cu interconnects on Cu void defects and metal line electromigration has been increased, as IC technology is continuously scaling down. Therefore, optimizing these processes to achieve higher ECP gap filling capability (fewer Cu void defects) becomes a hot topic in recent years.

In last two years, although the conventional barrier, seed and ECP technology were applied to implement the wafer production, some of the products in company still suffered serious Cu void (or commonly known as missing metal [7]) defects at DD structure and the electromigration lifetime only marginally passed the target value.

The Cu void defects depend greatly on the barrier and seed properties and directly influence the performance of Cu metal EM [8]. For the Cu integration process, many kinds of barriers have been proposed and evaluated. It has been shown that the TaN/Ta bi-layer can maximize adhesion to the inter-metal dielectric and Cu layer, and give a good thermal stability and low sheet resistivity [9]. EM lifetime of high purity films is usually about three times longer than that of low purity films. An investigation [10] suggested that the microvoids appeared in low purity films would migrate and move along grain boundaries. Eventually, during the EM testing, they will accumulate and lead to earlier failure of the low purity films. Thus, obtaining a void free film in the barrier and seed process is very important for the EM lifetime. The process step of barrier and seed layer deposition has been a key challenge for most researchers because getting these layers to the via bottom as well as lining sidewalls of the trenches and vias has proven difficult as the aspect ratio increases [11].

In order to find out solutions for the defect problems and improve EM lifetime, some process optimization actions need to be studied and taken. Two main approaches to reduce Cu void defects and improve EM lifetime are optimization of deposition step (e.g., barrier and seed) and Cu plating step such as ECP. Therefore, a design of experiment (DOE) has been implemented on the barrier and seed process optimization. However, due to time and facility limitations, the ECP process optimization is not included in this project.

1.2 Objectives

Driven by the above motivations, the objectives of this project are shown below:

1. To characterize the Cu void defects in terms of the barrier and seed.
2. To optimize barrier and Cu seed processes to improve the gap filling capability (Cu void defect reduction) and thus enhance electromigration performance.

1.3 Major Contributions of the Thesis

Following achievements have been resulted from this research work:

1) A design of experiment (DOE) was implemented to investigate barrier and Cu seed processes, which was motivated by reducing the Cu void defects of Metal2 (M2) dual damascene (DD) structure and improving wafer yield. Best conditions were extracted from 4 factors of DOE, which include the tri-layer barrier with lower via bottom removal, pre-barrier cooling process, Cu seed deposition using 3-step deposition power and Cu seed thickness of 700Å.

2) The comparative studies of the samples with tri-layer and bi-layer barriers show that the samples with tri-layer barrier have the lower defective die percentage. Downstream EM test reveals that the samples with tri-layer barrier have a downstream EM lifetime three times more than that of the samples with bi-layer barrier.

3) ADCV structures with three different via bottom removals were comparatively investigated. Median removal in the ADCV split has the lowest defective die percentage, the highest activation energy and the longest downstream EM lifetime. However, it exhibits median via contact resistance as the tradeoff to the longer EM lifetime.

4) The metal lines with 3-step Cu seed with powers of 0:500:1000 W (time ratio of 1:1:1) shows a smaller metal line leakage current than those of 2-step Cu seed with

power of 500:1000 W (time ratio of 1:2). The metal line sheet resistance and metal via contact resistance are comparable for the two kinds of Cu seed. For the samples with 3-step Cu seed, the average defective die percentage is 3% lower and the average yield is 0.5% higher than those with 2-step Cu seed. Transmission electron microscope (TEM) images show that the 3-step Cu seed reduces the barrier discontinuity at the point film among the barrier layer, tetra-ethyl-ortho-silicate (TEOS) and low k (LK) dielectric layers, and the Cu seed step coverage is also improved at the kink location with slightly less overhang.

1.4 Organization of the Thesis

The whole report is divided into eight chapters:

Chapter 1 presents the general history of the metallization and the motivation of this work, followed by the objectives, contributions and organization of this research project.

Chapter 2 reviews the Cu single damascene and dual damascene technology, followed by barrier, copper seed, electro copper plating (ECP), and Cu void defects.

Chapter 3 outlines the experimental setup employed in this project. Different characterization methods or tools, such as wafer acceptance test (WAT), KLA2800 defect scanner, scanning electron microscope (SEM), transmission electron

microscopy (TEM), focused ion beam (FIB), yield tester and electromigration are also discussed.

Chapter 4 addresses the barrier & seed design of experiment (DOE) for Cu void reduction of dual damascene (DD) structure, which includes the factors of barrier type, barrier cooling, seed layer deposition power and Cu seed thickness.

Chapter 5 describes comparative studies between the samples with tri-layer and bi-layer barriers in terms of TEM images of via profiles, Cu void defects and downstream electromigration lifetimes.

Chapter 6 shows three ADCV structures with different via bottom removals. The TEM images of via profiles, via contact resistances, Cu void defects and downstream electromigration lifetimes are comparatively studied.

Chapter 7 states a comparative study on the 3-step and 2-step Cu seed layers. In this chapter, their electrical properties (such as metal line sheet resistance, metal line leakage current, and via contact resistance), and wafer level properties (such as Cu void defects, yield, and TEM images of the dual damascene structure profiles) are comparatively studied.

Chapter 8 concludes the report and shows some recommendations for the future research.

Chapter 2 Literature Review

2.1 Cu Single Damascene and Dual Damascene Technology

Cu metallization used for ultra deep sub-micron integrated circuits (ICs) is not a trouble-free process. In order to integrate Cu metallization successfully into ICs, some technical issues such as poor adhesion to most of the dielectric layers, lack of anisotropic etching, corrosion, and oxidation associated with the transition to Cu have yet to be resolved [12, 13]. It is especially not easy to etch Cu using plasma. In the early 1990s, IBM demonstrated that it could overcome the problems of Cu device integration using a single damascene (SD) or dual damascene (DD) structure, by incorporating physical vapor deposition (PVD) Ta (N) as a barrier layer against Cu diffusion, PVD Cu as a seed layer, electro-chemical plated Cu for via and trench filling, and finally chemical mechanical planarization (CMP). In 1998, by using Cu DD technology, IBM implemented high volume Cu chips interconnections [14]. Motorola also published a paper [15] on Cu interconnects by using Cu DD technology. In 2000, IBM announced six-level Cu wiring process as a feature of CMOS logic technology [16] and started full scale manufacturing at around 2003.

The damascene process consists of etching trench and via in the dielectric layer, filling up the trench and via with a Cu diffusion barrier and subsequent deposition of

the Cu seed layer as a nucleation center for ECP. There are two damascene processes:

single damascene and dual damascene, and they are illustrated in Fig. 2.1.

Fig. 2.1. Cu single damascene and dual damascene processes [17].

The SD process is a process in which interconnect lines (trench) and interconnect via footprints are fabricated separately by dielectric fill, metal etch deposition and final metal CMP. In a DD process, interconnect lines (trench) and via footprints are filled simultaneously, which make DD process a simpler and more cost-effective one. There

are two principle modes for DD process, trench first and via first. They are currently used as the mainstream in production [17].

2.2 Barrier

Cu has some problems to degrade device performance when it directly contacts to the dielectric acting as interconnects, such as: (a) easy to diffuse into the dielectric, silicon and salicide; (b) poor adhesion to the inter metal dielectric (IMD) or inter layer dielectric (ILD) layer; (c) easy to form Cu-Si compounds at temperature as low as 200°C [18, 19]; (d) easy to drift through oxide under field acceleration; (e) easy to be oxidized, etc. Therefore, in order to successfully integrate Cu metallization into ICs, suitable barrier materials have to be developed against Cu diffusion and preventing undesirable interactions between Cu, and Si, SiO₂, or other low K dielectric materials.

The choice of the material depends on barrier properties, the stress migration (SM) and electromigration (EM) performance, the ability of the deposition technique to obtain sufficient step coverage and uniformity of the trench and via sidewalls, and the maximum temperature that a barrier could sustain. The metal barrier films could be deposited in different microstructures such as polycrystalline, amorphous and amorphous-like states with free of grain boundaries depending on process. Therefore, high thermal stability of these barriers could be achieved. It is well known that barrier

failure is caused by diffusion of Cu along the grain boundaries or through weak spots generated at elevated temperatures in the barrier films that are relatively intact, or by the reactions between barrier films and Si, SiO₂ or other low K dielectric materials to form new compounds such as metal-rich silicides.

Considering these factors, several refractory materials and their binary nitrides as well as ternary material (X-silicon-nitrogen) compounds have been examined, which include Ta [20, 21], TaN [3, 22, 23], TaSiN [24, 25], W [26], Ti and TiN [19, 27]. An overview of several materials, which can be used as an effective barrier against Cu diffusion, is shown in table 2.1 below.

Table 2.1. Barrier materials, deposition process and performance [28]

Parameter/deposition Method	PVD (IMP)			CVD		
Material	Ta	TaN	TiN	Ta	TaN	TiN
Deposition temperature (°C)	<150	<150	<150	>400	>350	>400
Process maturity	Good	Good	Good	Low	Good	Adequate
Resistivity (μOhm cm)	150~200	200~250	50~150	~1000	125~400	200~250
Step coverage (%) (Aspect ratio = 3 @0.25 μm)	25~40	25~40	25~40	>80	>80	<50
Maximum temperature (°C) of annealing for 30 min.(10 nm thick barrier)	500	600	450	NA	550	600

Among these barrier materials, Ta-based compounds show superior barrier properties against Cu diffusion [28, 29]. Both Ta and TaN have high melt point temperatures of 3017°C and 3087°C, respectively. Ta-based compound are known to be

thermodynamically stable with respect to Cu. Hence Ta and TaN barrier are expected to be stable at a very high temperature [21].

Work done by Jiang et al. [30] shows some property comparison between Ta and TaN as listed in Table 2.2. It indicates that the crystallinity is strong for Ta, and weak for TaN. And Ta/Cu interface is rough while TaN/Cu interface has a transition layer. Therefore, Ta has a better interface than TaN with copper, which indicates that Ta has a better adhesion with Cu. Agglomeration of Cu seed layer for the different barrier materials after annealing has also been investigated. It shows that Cu seed layer tends to form larger islands on the TaN barrier, compared with smaller islands on the Ta barrier. Surface roughness of TaN is much larger than Ta. Besides, (111) texture of Cu line is stronger with Ta than with TaN. It suggests that a Ta/TaN/Ta tri-layer barrier could be used to promote interfacial bonding between the barrier and Cu layer as well as take the advantage of TaN as a barrier material. The properties of Ta and TaN sputtered on the blanket wafer are summarized in the table below.

Table 2.2. Summary of blanket wafer measurements [30]

Barrier	Ta	TaN
Crystallinity	Strong	Weak
Stress (MPa)	-2100	-2100
Sidewall Agglomeration	Small islands	Large islands
Surface Roughness RMS (Å)	35	400
(111) of Cu Film	Medium	Weak
(111) of Cu lines	Medium	Medium

Diffusion properties of the Cu into Ta and TaN barrier for MOS device have been studied by Loh et al. [23]. It used Fick's law of diffusion to model the Cu diffusion into Ta and TaN based barrier. From these matching, it has been observed that the Cu diffusion coefficient ($D=D_0 \exp(-E/KT)$) in Ta is larger than that in TaN at different annealing temperatures.

The structure and thermal stability of Ta, TaN, TaN/Ta and Ta/TaN/Ta barriers between Cu and SiO₂ have been investigated by Hübner et al. [31]. During thermal treatment, when temperature is above 500°C, Ta atoms can diffuse through the Cu to the sample surface. This Ta diffusion phenomenon was also observed by Yuan et al. [21]. N content in the Ta based barrier can reduce this diffusion process. Such Ta diffusion will alter the barrier layer thickness and may influence its thermal stability. In the Cu interconnect layer, the accumulation of the diffused Ta atoms also degrade its electrical properties. Beside Ta diffusion, the diffusion of N atoms [31] was found in the graded barrier of Ta/TaN, and Ta/TaN/Ta at the annealing temperature of 300°C. N atoms diffuse from the TaN layer into the adjacent Ta layers. At annealing temperature of 500°C, the hexagonal Ta₂N is formed, which can change the original barrier properties like electrical resistivity. Both Ta and N diffusion are disadvantageous and should be suppressed. Rapid thermal process (RTP) is used to do annealing and the temperature normally does not excess 500°C in the BEOL processes.

Several barrier metal deposition processes have been studied to achieve the contamination-free via bottom with low resistance and avoid via open and EM failure. Ar^+ preclean barrier process [32] was applied prior to the deposition of Cu diffusion-barrier metal with higher bias power and shorter time argon plasma to clean the via bottom and achieved lower via resistance. Conventional direct contact via (DCV) [33] used high bias power and time controlled argon resputtering etching to selectively remove the barrier at the via bottom after the barrier deposition, and then implemented an additional step called ‘soft’ clean process that includes a chemical clean, hydrogen-based gas and low-energy inductively coupled plasma to remove the particles. This barrier free DCV structure can have as much as 71% reduction on via contact resistance compared with conventional DD structure. However, this process ignores the damage to the sidewall or trench bottom of the barrier during plasma etching, which leads to scraggly surface and influence the step coverage and within-trench-via uniformity of the Cu seed layer. Thus it’s hard to achieve a further void free ECP processing for ultra deep submicron ICs. After that, advanced DCV (ADCV) [34, 35] solved this problem by depositing a very thin Ta layer after resputtering. This process highly improved EM performance and at the same time kept the via contact resistance low. The previous studies on the DCV were implemented together with barriers Ta [33], TaN/Ta [34] or TiSiN/Ta [35]. However, the ADCV with the tri-layer barrier is a new process that has not been reported yet.

As each technology node feature size gets smaller and smaller in the Cu metallization scheme, the trenches and via become narrow and deep in damascene structure in ultra deep submicron ICs. The extendibility of the conventional PVD technology is challenged. Step coverage extendibility of the trench or via in Cu damascene structure becomes the key concerns specifically. The step coverage of both barrier and Cu seed layer becomes a very critical key factor to control Cu gap filling performance and eventually control overall interconnect reliability. Currently, several PVD technologies are used as sources to deposit barrier and Cu seed, which include ionized metal plasma (IMP) [36], hollow cathode magnetron (HCM) [37], and self-Ionized plasma (SIP) [38]. Each of these methods has limitations in achieving sufficient step coverage of trench or via as the feature size shrinks, according to Ding et al. [39].

The fundamental issue of the PVD sputtering source is the ionization rate. Because the step coverage largely depends on the metal ion fraction during deposition, increasing the ionization rate of the sputtering system can improve the step coverage, and a PVD sputtering source based on a high power density concept has been developed [40]. However, this sputtering source consumes much higher power (40 - 60 kW) than other methods in order to achieve higher level step coverage. It's suitable for the institute or school research application but not suitable for the mass production in industry due to its high power consumption, tool complexity and ultimately high cost. Therefore, finding a better barrier and seed deposition method to achieve good step coverage and keep the comparable power consumption becomes a challenge.

Metal line and via resistances are other two key factors to choose the barrier and seed materials, deposition sources as well as their thickness for the Cu metallization damascene structure optimization. With atomic layer deposition (ALD) liners, its metal line and via resistances can be reduced by 15% and 40%, respectively, compared with that of PVD liner applied on the 90 nm process node [40]. However, due to the complexity of the deposition tool and long time of processing, it is very difficult to integrate ALD into mass production for the wafer manufacturing.

2.3 Cu Seed

The primary function of the seed layer is to provide a low resistance conduction path for the plating current that drives the electro-Cu plating process as well as provide a nucleation layer for the initiation of the electroplated Cu film growth.

The Cu seed is very critical for the ECP process at the following two directions:

1. On the wafer scale, the seed layer carries the current from the edge to the center of the wafer. The thickness of the seed layer must be sufficient such that the voltage drop from the wafer edge to center would not impact the within-wafer (WIW) uniformity of the plating process. The minimum calculated field thickness is about 50 nm to achieve < 5% WIW uniformity on 8" wafer [41].

2. On the feature scale, the seed layer carries current from the field level into the via bottom and trenches. Again, the thickness of the seed layer must be sufficient such that the voltage drop does not significantly retard the plating process at the via bottom or trench relative to the top. When the seed layer thickness is insufficient at the bottom, rapid plating at the top of the feature will close up the feature, producing a center void or bottom void. A minimum of 10 nm (typical value will be 20-30 nm) of unagglomerated Cu seed is needed within the feature for successful ECP [42].

Some requirements of a seed material used are low cost of ownership, good adhesion to barrier, deposition temperature ($<300\text{ }^{\circ}\text{C}$) compatible with low-K dielectric, smooth continuous surface with no agglomeration, minimum overhang, good step coverage and high uniformity of the seed layer. These are the main factors in assuring completely void free Cu gap filling. Some PVD deposition technologies of the Cu seed have been mentioned along with the barrier early. Besides, there are still CVD [28], and electro-less (EL) technologies used to deposit Cu seed [43, 44]. CVD Cu seed can provide good step coverage but suffers high cost of chemical and relatively poor adhesion. EL Cu Seed can achieve good step coverage with little overhang, low deposition temperature process. However, it produces higher resistivity and roughness of initial Cu seed layer [44], and electroless bath has much more unstable bath chemistry [45] and poor (111) texture than those of PVD seed [46]. Every technology

has its tradeoff based on the step coverage, adhesion performance to barrier, and process cost. A study on the different via profiles was conducted by Abhulimen et al. [11]. It investigated the step coverage of Cu seed layer performed on different via structures, such as straight sidewall via, sloped (tapered) sidewall via, and deeper depth via. Sloped sidewall via would be essential in achieving continuous coverage of sputtered Cu seed films.

2.4 Electro Copper Plating (ECP)

After barrier and Cu seed, ECP is used to deposit the rest of Cu into the metal SD or DD structure to form the metal line and vias. ECP is currently the most popular and promising Cu deposition method and it's much cheaper than other metallization techniques in the coating industry. Electroplating is also known as electro-deposition, electrochemical (ECD) or electro-fill. The wafer is immersed into a plating bath that has the solution of Cu ions, cathode (negative bias) clamped to the wafer edge, and another Cu electrode as anode (positive bias). Cu seed layer on the wafer provides a low resistance conduction path for the plating current. A potential is needed to apply in the ECP process to cause the dissociation of Cu from the Cu anode, and attract the Cu^{2+} from the solution to deposit on wafer. At the wafer (negatively biased) side, the following reduction (deposition) reaction occurs: $\text{Cu}^{2+} + 2\text{e}^- \rightarrow \text{Cu(s)}$.

Small amount of additive species such as accelerators, suppressors and levelers are required to achieve desirable metallic deposition layers as well as proper filling of aggressive feature. The chemical composition of the ECP solution is shown in Table 2.3.

Table 2.3. Chemical composition of ECP solution [14, 47]

Compound	Chemical	Purpose	Concentration
Hydrated Cu sulfate	$\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$	Cu source	17.5-60g/L
Sulfuric acid	H_2SO_4	Control electrolyte conductivity and improve wetting	45-325g/L
Accelerators	E.g. organic mercapto species	Provide nucleation sites → accelerate deposition	1-25ppm
Suppressors	Polymers, e.g. polyethylene glycol	Current-suppressing film to remove global roughness and smooth defects	200-2000ppm
Levelers	Proprietary	Super fill of cavities	Low ppm
Chlorides	HCl	Prevent anode passivation	30-100ppm

The accelerators (brighteners) are small organic molecules that enhance deposition rate in the trench and via. It can strongly eliminate the center voids in the filling experiment and has less ability to eliminate the bottom voids. Suppression polymers are used to remove the global roughness and smooth defects during plating. The levelers are large organic macromolecules which can retard deposition rate at open field corners. As concentration of the chloride ion is increased from zero, the filling acceleration in vias increases to a maximum value but then decreases as concentration

of the chloride is further increased. By control the concentration of the additives, a conformal bottom-up filling can be obtained. Illustration of adsorption behavior of additives during plating fills is shown in Fig. 2.2.

Fig. 2.2. Illustration of adsorption behavior of additives during plating fills [47]

ECP current is another important issue. In this work [47], an example of a two-step DC current plating process with three important features identified is illustrated and shown Fig. 2.3. The first feature is "zero current induction time", at which the wafer is exposed to the plating solution and is wetted before applying current to prevent Cu corrosion, cuprous oxide dissolution and Ostwald ripening. The second feature is indicated as "initiation current", the current is relatively small, the surface resistance is large, the rate of deposition is slow, and thus the deposition is conformal. During this time, the equivalent seed layer within the feature for next step plating will thicken. It can insure the Cu seed discontinuity of the seed layer. The last feature in the figure is the fill step, which typically lasts 20-40 seconds, depending on feature size and bath conditions. Smaller features tend to fill earlier because they are less accessible to the electrolyte and develop conditions necessary for bottom-up fill more rapidly.

Fig. 2.3. A two-step DC plating process with three key features identified [47]

2.5 Cu Void or Missing Metal Defects

In Cu metallization scheme, as the feature size decreases, the trenches and via become deep and narrow in damascene structure in ultra deep submicron ICs. Defects are easily formed at some critical or smallest feature size location. Those defects that scanned after meal cap layer (SiCN) are the most common defects at the back end of line (BEOL). They can be classified as void or missing metal, abnormal Cu growth, and particles. The most serious defect type is Cu void defects, which are formed due to the plated Cu failed to fill completely in the metal line and via gap [7, 11, 48, 49].

Company has defined three types of Cu void defects as shown in Fig. 2.4: dash metal defect, unfilled defect, and protrusion defect.

Dash metal defect is that void is formed on the top of the metal line or via and Cu is partially filled in the metal line or via. ECP process is the dominate factor to induce dash metal defect. It's due to the bottom up speed which is not fast enough to fill up the gap and overhang problem appear during the ECP process. This defect can be eliminated by tuning the concentration of ECP additives. It also can be reduced by enlarging the gap top opening or tuning thickness of the barrier and Cu seed to reduced overhang effect.

Unfilled defect is the defect that there is no Cu filled in the metal line or via, which leads to an unfilled gap. It is possibly due to the discontinuity of barrier or Cu seed on

the sidewall. Therefore, robust barrier and Cu seed process can reduce this kind of defect.

Protrusion defect is the defect with void formed at the bottom or sidewall of metal line or via and Cu protruded on the top. It's induced by the Cu oxidation after Cu plating. This Cu oxide stresses the metal line and causes Cu to migrate and protrude to the surface. It can be reduced by adding nitrogen purging after plating and isolate the metal from other environments.

These defects can lead to opens or voids in the Cu damascene circuitry after CMP, which degrade significantly the stress migration and electromigration of that metal layer, moreover, it can even be the kill reason of die functionality fail and thus impact yield.

Defect naming	Description	Defect Image		FIB image	
K_Dashmetal	Partial filled with Cu
K_Unfilled	No Cu filled based on SEMV review
K_Protrusion	Cu Partial Filled and Protrude

Fig. 2.4. Cu Void defects classification after Cu plating.

Causes of Cu void or missing metal defect include pre-existing contamination of the barrier or seed, the step coverage of the barrier or Cu seed after their deposition, highly variable of severe oxidation of the Cu seed which limits wetting, the speed of ECP during Cu plating, and the overhang at the metal trench opening (top of the metal). Void defects can be reduced by improving the cleaning efficiency during metal processes, controlling the queue time [50] of wafers to ambient air among barrier, seed, ECP, Annealing and CMP, choosing good Cu barrier and seed deposition source, and improving Cu gap filling efficiency [51] by varying additives structures and concentration. By using these actions, Cu void defects reduction is improved a lot. More optimized processes need to be developed to maximally reduce Cu void defects and improve wafer final yield..

Chapter 3 Characterization Experimental Setup

3.1 Wafer Acceptance Test (WAT): R_S , R_C & I_{BR}

3.1.1 WAT Introduction

Wafer acceptance test (WAT) is a test to extract electrical parameters with special test structures on wafer at room temperature. The most important three parameters for metal at back end of line (BEOL) are metal line sheet resistance (R_S), metal via contact resistance (R_C) and metal line bridge leakage current (I_{BR} or metal line leakage current). All of them can be obtained from WAT test. WAT can also get the front end of line (FEOL) parameters like effective poly resistance, device capacitance, source, drain, gate and substrate saturation current, threshold voltage, and etc. Because FEOL parameters are not related to Cu interconnects, they will not be introduced in this report.

WAT can monitor the process capability and stability. Statistical process control (SPC) is a typical tool to control WAT parameters. With inline WAT, it can reduce the failure impact or loss by early detecting the abnormality of process or machine before wafer yield test. WAT is one of the key sources to evaluate the process change or new machine. Agilent 4073 (tester) and test key UF3000 (probe) are used as the hardware of the WAT system, as shown in Fig. 3.1 and Fig. 3.2.

Fig. 3.1. Hardware of wafer acceptance test.

Fig. 3.2. Probe card and tips.

Tester contains ①Controller/CMU/PG/HP3458, ②Test head, and ③Spectrum analyzer. Probe has three parts, such as ④Main body, ⑤FOUP Loader, and ⑥ Hinge (link Test head). The probe tips (⑦) are probed on test key of the wafer as interface of wafer and tester.

All test structures of the metal line sheet resistance, via contact resistance and metal line leakage current are integrated as the WAT test keys on the scribe lines with aluminum pads as the contacts lying on the surface of the wafer, as shown in Fig. 3.3. They are fabricated together with production die under the same processing condition. It ensures the WAT test can exactly monitor the electrical performance of the metal interconnect. WAT takes 9-point measurement and uses the average of the 9 values to represent for whole wafer. 9 points are picked from 9 frames located in the wafer donut and center area, as shown in Fig. 3.3. The rectangular die contains the given functional circuit components such as static random access memory (SRAM), logic connections and input/output (IO) devices. All scribe lines lie around the dies, and will be cut away after wafer diced.

Fig. 3.3. WAT test key on scribe lines.

3.1.2 Metal Sheet Resistance (R_S) Measurement

Metal line resistance is V_F over I_M , which is in term of R_S multiply length and over its width. Then metal sheet resistance R_S can be calculated.

Measurement method is:

- (1) Force $V_F = 1\text{ V}$, sense I_M

$$(2) \text{ Calculate the } R: R = \frac{V_F}{I_M} = \frac{L \times \rho}{A} = \frac{L \times \rho}{W \times t} = \frac{L}{W} \times R_S \quad (3-1)$$

$$(3) R_S = \frac{W}{L} \times R = \frac{R}{(L/W)} = \frac{(V_F/I_M)}{(L/W)} (\Omega / \text{square}) \quad (3-2)$$

The test structures of line sheet resistance for all metal trench layers are kept the same.

Take Metal2 (M2) as example, its test structure is shown in Fig 3.4. The M2 R_S test structure has M2 trench only. Its two pads lie on the wafer surface layer. The test structure is fabricated together with other M2 layer using dual damascene process. During the via1 photolithograph process, R_S test structure area is blocked by the via1 (V1) mask and thus no V1 formed.

Fig. 3.4. Metal line continuity serpentine structure (R_S) as a test key.

3.1.3 Metal Via Contact Resistance (R_C) Measurement

Series via (contact) and metal line chains are used to monitor contact resistance, which are illustrated in Fig. 3.5 to Fig. 3.7. It tests the M2V2 (metal 2 and via 2) contact resistance. The total contact resistance is the remainder of total resistance deducting metal line resistances of upper and lower metal layers.

Measurement method is:

(1) Force $V_F = 1$ V, sense I_M ;

(2) Total metal resistance is:

$$\begin{aligned} R_M = \frac{V_F}{I_M} &= N \times R_C + \left(\frac{N}{2}\right) \times \frac{L_2}{W_2} \times R_{S2} + \left(\frac{N}{2}\right) \times \frac{L_3}{W_3} \times R_{S3} \\ &= N \times R_C + \left(\frac{N}{2}\right) \times SQR_2 \times R_{S2} + \left(\frac{N}{2}\right) \times SQR_3 \times R_{S3} \end{aligned} \quad (3-3)$$

(3) Then calculate the via contact resistance R_c :

$$R_C = \frac{(V_F / I_M)}{N} - \frac{(SQR_2 \times R_{S2} + SQR_3 \times R_{S3})}{2} (\Omega / via) \quad (3-4)$$

Where R_{S2} and R_{S3} are sheet resistances of M2 and M3, respectively. N is the total number of vias.

Test structure of via contact resistance (R_C) is formed by dual damascene process with both upper and low metal layer deposited. There are 6 contacts ($N=6$) in the Fig. 3.6.

Unit of R_C is ohm per via.

Fig. 3.5. Metal via contact resistance calculation method.

Fig. 3.6. Lateral view of the test key structure of the metal via contact resistance.

Fig. 3.7. Top view of the test key structure of the metal via contact resistance.

3.1.4 Metal Line Leakage Current (I_{BR}) Measurement

The objective of this measurement is to check the isolation between metal to metal lines in the same layer. The measurement method uses forcing voltage (V_{CC}), and then measure the bridge current (I_{BR}) or leakage current. Its test structure is shown in Fig 3.8. Same as the metal line R_s test structure, M2 I_{BR} test structure is fabricated with dual damascene process.

Fig. 3.8. Metal line bridging (I_{BR}) comb structure as a test key.

3.2 KLA2800 Defect Scanner

KLA2800 (Product of KLA-Tencor Corporation) is a full-spectrum DUV/UV/VIS patterned wafer inspection platform for sub-65 nm design rule development and production. Due to its multiple wavelengths, extendibility and ultimate sensitivity, KLA2800 is able to take the widest range defect capture for all process layers.

In this project, KLA2800 is used to scan the ECP Cu void defects after metal cap layer (SiCN). Conducting defect scanning at this step can avoid queue time concern against Cu oxidation. Defects are scanned for one half of the wafer and shown in term of defective die percentage (DD%), which is defined by the percentage of the number of defective dies scanned over the total number of dies scanned on one wafer.

3.3 SEM, TEM & FIB

Scanning electron microscope (SEM) and transmission electron microscopy (TEM) are the most popular microscopes used in the semiconductor and materials science fields for specific inspection analysis on the wafer.

SEM is a type of electron microscope that images the sample surface by scanning it with a high energy electron beam in a raster scan pattern. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography composition and other properties such as electrical conductivity.

TEM is a microscope technique in which an electron beam is transmitted through an ultra thin sample, interacting with the sample as it passes through. An image is formed from the interaction of the electrons transmitted through the sample. The TEM

requires very thin samples, typically about 100 nanometers. CMP or electro polishing are used to prepare such thin samples.

Focused ion beam (FIB) is a scientific instrument that resembles a SEM. However, FIB uses focused beam of ions to image the sample in the chamber, while SEM uses a focused beam of electrons instead. Most widespread FIB uses Gallium ion sources. FIB is also commonly used to prepare samples for the TEM. Nanometer-scale resolution of FIB allows it to choose the accurate thin region from samples. Normally, we need to scrap the whole wafer to do TEM. However, FIB can prepare very thin sample and only destroy one die of the wafer by using the gallium ion beams.

3.4 Yield

Wafer yield is the ratio of the number of functional dies over the total number of dies for each wafer in percentage form. Wafer yield is very important for wafer chip manufacturing companies because it evaluates the overall process performance of wafer foundry. The company tests the chips on the wafer with an electronic tester that presses tiny probes against the chip. The machine marks each bad chip with a drop of dye.

Wafer yield tester tests some major areas of dies based on different evaluation parameters, such as ICs functionality and defect related. Each test item is named with a failure bin number. Wafer yield tester will exam the most likely and frequently failure bin first, and then the second, and so on. If there is any die failed at any bin test, for example, Bin x, the yield test on this die will be stopped, and mark it failed with Bin x. Finally, all the dies without any bin failure will be marked as Bin1, and others marked with the bin it failed at. These data can be used to calculate the wafer yield by equation (3-5).

$$Yield = \frac{\text{Total No. of Bin1}}{\text{Total No. of dies}} = 1 - \frac{\text{Total No. of failure Bins}}{\text{Total No. of dies}} \quad (3-5)$$

It can also get the information for each of the failure bins, like how many dies failed due to Bin2, Bin3, and etc. Bin2 is found to be the most common failure bin in the baseline wafers. It tests ICs functionality and defects in the static random access memory (SRAM) area. A physical failure analysis (PFA) Pareto plot for Bin2 mechanisms is shown in Fig. 3.9. It shows that M1 & M2 Cu loss, poly pimple, shallow trench isolation (STI) rip out, and contact opening are the major failure mechanisms for Bin2.

Fig. 3.9. Bin 2 PFA Pareto Plot.

3.5 Electromigration

Electromigration is the transportation of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. The effect is important in applications where high direct current densities are used, such as in microelectronics and related structures. As the dimension of integrated circuits (ICs) decreases, the practical significance of this effect increases. The Black empirical equation [52, 53], which is a mathematical equation, is commonly used to predict the lifetime of interconnects in IC tested under "stress", that is external controlled heating and increased current density, and the model's results can be extrapolated to the device's expected lifetime under real conditions. Such testing is known as high temperature operating lifetime (HTOL) testing.

$$\text{Black equation: } MTTF = AJ^{-n} \exp[E_a/(kT)] \quad (3-6)$$

Where: A is a constant, depend on the material quality and the interconnect geometry;

J is the current density applied in $10^6 \text{ A}/\mu\text{m}^2$;

n is the current acceleration factor, which is 1.1 in this project;

E_a is the activation energy in eV;

K is the Boltzmann constant;

T is the absolute temperature in K.

The equations that are used to extrapolate EM lifetime from test condition to product operation condition are shown below.

$$TTF_{operation} = MTTF_{TEST} \left(\frac{J_{operation}}{J_{TEST}} \right)^{-n} \exp \left[\frac{E_a}{k} \left(\frac{1}{T_{operation}} - \frac{1}{T_{TEST}} \right) \right] \exp(-N\sigma) \quad (3-7)$$

$$\text{And } T_{0.1\% operation} = T_{0.1\% TEST} \left(\frac{J_{operation}}{J_{TEST}} \right)^{-n} \exp \left[\frac{E_a}{k} \left(\frac{1}{T_{operation}} - \frac{1}{T_{TEST}} \right) \right] \quad (3-8)$$

Where: Parameters such as MTTF, and E_a are determined from experiments;

σ is 1/slope of the TTF cumulative density function plot;

J_{test} and T_{test} are the accelerated test conditions;

$J_{operation}$ at 110°C is $0.379 \times 10^6 \text{ A}/\text{cm}^2$, $T_{operation} = 110^\circ\text{C}$;

N is a constant that relates MTTF with a TTF at another fail percent, $N_{0.1\%} =$ inverse of standard of normal cumulative distribution $(0.1/100) = 3.09$.

The current densities and temperatures at product operation condition and EM test condition (acceleration condition) are shown in Table 3.1.

Table 3.1. The parameters of product operation condition and EM test condition

Conditions	Current density	Temperature
product operation condition	$0.379 \times 10^{-6} \text{ A/cm}^2$	110 °C
Test condition (EM accelerated)	$2 \times 10^{-6} \text{ A/cm}^2$	275, 300, 325 °C

The EM test structure schematic is shown in Fig. 3.10. It is downstream wide Metal2 (M2) structure for evaluating downstream EM (downstream wide V2M2 EM) where the downstream electrons flow at M2 cathode. Via size are $0.1 \mu\text{m} \times 0.1 \mu\text{m}$ in width and length, and $0.2 \mu\text{m}$ in height. The width, height and length of M2 in the test structures are 0.3, 0.2, and $400 \mu\text{m}$, respectively. The wide feeder metal lines (M2) are used to minimize EM failure probability.

Fig. 3.10. Schematics of DD Cu interconnect structures for downstream EM tests

Chapter 4 Design of Experiment on Barrier and Cu Seed

4.1 Introduction

Since the Meta2 (M2) dot pattern has very small dimension at the static random access memory (SRAM) area, Cu voids are easily formed at the interface of Vial (V1) and M2, leading to Bin 2 failure and yield loss. In the past two years, although the conventional barrier, seed and ECP technology were applied to the wafer production, some of the 65 nm products suffered from Cu void defects.

To reduce the Cu void defects, four factors which are barrier type, cooling, seed layer deposition condition, and seed layer thickness are chosen to optimize the 65 nm node process. In the design of experiment (DOE) for these four factors, a total of $3^4 = 81$ runs are usually needed. However, to minimize the production costs and time, Taguchi's L9 orthogonal array is chosen. With this method, the number of experiments reduces from 81 experiments to 9.

4.2 Experiment Design

The goal of this experiment is to reduce dual damascene Cu void defects. The Taguchi robust design method (orthogonal arrays) was used as an analysis tool.

Response (or dependent) variables (Y) include:

- Y_A : Defective die percentage (The smaller the better)
- Y_B : Wafer yield (The larger the better)

Independent variables (factors) (X) include:

- X_A : Barrier type
- X_B : Cooling
- X_C : Seed layer deposition power
- X_D : Seed layer thickness

To find the optimized conditions, 3 condition levels are selected for each factor. For 4 factors with 3 level experiments, the degree of freedom (df) is $= 4 \times (3-1) = 8$, and the total number of the experiments needed is $(df) + 1 = 9$. Therefore, with L9 orthogonal array for analysis and design, 9 wafers are fabricated in this work. The wafer splitting table with different conditions is shown in Table 4.1.

All parameters used in this study were the ones whose values were close to industry standard operating conditions (baseline) or the values to which the company was able to supply for the test samples. For example, bi-layer with resputtering of 15 s and 650 W, condition of no cooling, two steps of Cu seed with 500:1000 W, and Cu seed of 570 Å are baseline operation conditions. Others conditions were chosen around the

baseline or the newly developed condition that the company could supply for the test samples.

Table 4.1. Wafers fabricated under different conditions for barrier and seed optimization to reduce Cu void defects.

Factor	Level	Condition	#5	#3	#8	#9	#6	#1	#4	#2	#7
X_A Barrier Type	Level-1	Bi-layer resputtering 15 s/650 W	V	V	V						
	Level-2	Tri-layer resputtering 10 s/1000 W				V	V	V			
	Level-3	Tri-layer resputtering 15 s/650 W							V	V	V
X_B Cooling	Level-1	No cooling	V			V			V		
	Level-2	Pre-barrier cooling		V			V			V	
	Level-3	Post-seed cooling			V			V			V
X_C Seed deposition power	Level-1	500:1000 W = 1:2 (time ratio)	V					V		V	
	Level-2	0:1000:200 W = 1:1:1		V		V					V
	Level-3	0: 500: 1000 W = 1:1:1			V		V		V		
X_D Seed Thickness	Level-1	570 Å	V				V				V
	Level-2	700 Å		V				V	V		
	Level-3	840 Å			V	V				V	

4.3 Results and Discussion

The DOE results in terms of defective die percentage (DD%) and wafer yield obtained from the 9 wafers (#1 to #9) are shown in Table 4.2. In the table, the 4 factors, barrier type, cooling, seed layer deposition power, and seed layer thickness,

are represented by X_A , X_B , X_C , and X_D , respectively. The three levels for each factor are represented by 1, 2 and 3, respectively. Y_A undergo larger swings may due to the lower killer ratio of defects for some wafers. Defect die means the die with defect. However, not every die with defect will suffer yield loss. Some wafers have higher DD% (eg. splits 1 & 4), but may be due to the defect sizes of some dies are not large enough, or some defects appear at non critical position, there is no much yield loss for these wafers.

Table 4.2. Defective die percentage and wafer yield result of DOE

Split No.	Factor (X)				Wafer ID	DD% (Y_A)	Yield (Y_B)
	X_A	X_B	X_C	X_D			
1	1	1	1	1	#5	29.30%	18.36 % ^{\$}
2	1	2	2	2	#3	1.00%	18.58 %
3	1	3	3	3	#8	2.14%	18.5 %
4	2	1	2	3	#9	19.04%	18.24 %
5	2	2	3	1	#6	2.24%	18.5 %
6	2	3	1	2	#1	6.85%	18.52 %
7	3	1	3	2	#4	1.54%	18.9 %
8	3	2	1	3	#2	7.02%	18.56 %
9	3	3	2	1	#7	4.39%	18.62 %

^{\$}Because of confidential information, yield parameters have been replaced with normalized values.

Based on the data in Table 4.2, by using Taguchi robust design method with L9 orthogonal array, the expected signal to noise ratio (S/N, or ETA) for the four factors are plotted in Fig. 4.1 and 4.2, respectively. In the Taguchi method, the term "signal" represents the desirable value and "noise" represents the undesirable value. The S/N

indicates the degree of the predictable performance of a product or process in the presence of noise factors. The process parameter settings with the highest S/N always yield the optimum quality with minimum variance. The S/N for each condition level is calculated by averaging the S/N values obtained at that condition level. The S/N values of DD% (Y_A) and yield (Y_B) are calculated using equation (4-1) and (4-2), respectively [54]. The mean squared deviation (MSD) expression combines variation around the given target and is consistent with Taguchi's quality objective.

$$S/N (ETA) = -10 \times \log_{10}(MSD) = -10 \times \log_{10} \left[(1/n) \sum_{i=1}^n Y_i^2 \right] \quad (4-1)$$

$$S/N (ETA) = -10 \times \log_{10}(MSD) = -10 \times \log_{10} \left[(1/n) \sum_{i=1}^n (1/Y_i^2) \right] \quad (4-2)$$

The optimum process corresponds to the highest signal to noise ratio. From defective die data shown in Fig 4.1, the best combination conditions are 3-2-3-2, which are tri-layer with resputtering 15 s/650 W, pre-barrier cooling, 3-step Cu seed with power ratio of 0:500:1000 W and time ratio of 1: 1: 1, and seed thickness of 700 Å.

From the yield data shown in Fig. 4.2, the best combination conditions are also 3-2-3-2, which is the same as the conditions extracted from the defective die data. However, the barrier type is the most dominant parameter on the yield followed by seed layer thickness, seed layer deposition power and cooling.

Fig. 4.1. Defective die ETA plots for wafers with different barriers, cooling conditions, seed types and thicknesses.

Fig. 4.2. Yield ETA plots for wafers with different barriers, cooling conditions, seed types and thicknesses.

As reported by Jiang et al. [30], Ta has a stronger crystallinity than TaN. The Ta/Cu interface is rough while the TaN/Cu interface has a transition layer. Therefore, Ta can form a better interface with Cu than TaN in terms of adhesion to Cu. In the Ta/TaN/Ta tri-layer barrier, the upper Ta layer can promote interfacial bonding with the Cu seed, the lower Ta layer contact Cu at the via bottom can reduce micro voids, and the TaN in the middle functions as a good barrier material to reduce Cu diffusion.

The via bottom removal depends on the power applied and time taken. The higher Ar^+ resputtering power induces a cone-shape via bottom, which has poor adhesion to the upper deposition layer (Cu seed) due to more bombardment damage at the via bottom.

Compared with the process without cooling, pre-barrier cooling process provides lower defective die percentage. It is because the pre-barrier cooling cools the wafer into a low temperature and gives a low and stable initial temperature for barrier deposition. The lower temperature can reduce surface diffusion and prevent Cu agglomeration. Therefore, the first barrier layer has a better step coverage and uniformity, and eventually induces fewer defects, better interfaces with the low k (LK) dielectric and lower metal layer.

For the 3-step Cu seed layer, the introduction of the zero AC bias step makes the Cu seed being deposited onto barrier with a proper deposition speed and thus less damage.

In next three chapters, the effects of the tri-layer barrier, via bottom removal and Cu seed layer on the performance of the 65 nm node technology will be investigated in detail.

4.4 Summary

By using Taguchi method, 9 wafers were fabricated and characterized. It is shown the best conditions for barrier and seed in terms of defective die percentage and yield are the tri-layer with lower removal, pre-barrier cooling, 3-step Cu seed with power ratio of 0:500:1000 W and time ratio of 1: 1: 1, and seed thickness of 700 Å.

Chapter 5 Comparative Study of Ta/TaN/Ta Tri-layer and Ta/TaN Bi-layer Barriers

5.1 Introduction

Copper (Cu) has been used to replace aluminum (Al) as interconnect material for deep submicron as well as nanoscale integrated circuits (ICs) due to its lower bulk resistivity, higher stress voiding and electromigration (EM) resistance [55]. Cu damascene and low-k dielectric were introduced to reduce the resistance capacitance (RC) delay and crosstalk of interconnection, which resulted in the increase of the circuit speed. As CMOS technology is continuously scaling down, the main concern for the dual damascene (DD) structure Cu/low-k interconnection is the long-term reliability. EM becomes the primary reliability key issue for Cu interconnects due to the rapid shrink of critical dimensions. Since Cu can diffuse or migrate easily into silicon and dielectric, which degrades interconnects EM. The EM performance of the Cu interconnects depends strongly on the chosen effective diffusion barrier, which is used to block Cu diffusion [24]. For the Cu metallization, several refractory materials and their binary nitrides as well as ternary compounds have been proposed and evaluated, including Ta [20, 21], TaN [22, 23], TaSiN [24, 25], W [26], Ti and TiN [27].

Among these barrier materials, it has been shown that the Ta/TaN bi-layer can obtain the best metallurgical and thermal stability [9, 56]. Li et al. [57] observed that the Cu film deposited on the Ta/TaN bi-layer showed the smallest stress among Ta-based barriers due to the relaxation of strain in the bi-layer barrier. In addition, the Ta/TaN bi-layer showed very low via contact resistance [9, 58]. These qualities can ensure Ta/TaN bi-layer barrier to obtain highly reliable and EM-redundant Cu interconnects [58]. Structure and thermal stability of the Ta/TaN bi-layer and the Ta/TaN/Ta tri-layer barriers were evaluated at the laboratory, both of them can maintain thermal stable below 500°C [31], which is much higher than the operating temperature 110°C of IC chip. Physical vapor deposited (PVD) Ta/atomic layer deposited (ALD) TaN/PVD-Ta tri-layer barrier structure was developed by Furuya et al. [59] with via contact resistance around 5 Ω /via, which had a significant reduction compared with that of ALD-TaN single-layer (around 10^7 Ω /via). However, this tri-layer was implemented only on the single damascene (SD).

Several barrier metal deposition processes have been studied to achieve the contamination-free via bottom with low resistance and avoid via open and EM failure. Ar⁺ preclean barrier process [32] was applied prior to the deposition of Cu diffusion-barrier metal with higher bias power and shorter time argon plasma to clean the via bottom and achieve lower via resistance. Conventional direct contact via (DCV) [33] used a high power Ar⁺ resputtering to selectively remove the barrier at the

via bottom after the barrier deposition and achieved a very low via contact resistance. However, conventional DCV obtained poor adhesion of the seed Cu, and EM degraded as there is no barrier to block the Cu atoms migrating at the via bottom. The ADCV [34, 35] solved this problem by depositing a very thin Ta layer after resputtering. This process highly improved EM performance and kept a low via contact resistance at the same time.

Although there was an interest in the Ta/TaN/Ta tri-layer barrier thermal stability with normal via process in the research laboratory [31] and a growing interest in the ADCV [34, 35], little is known about its EM performance when the tri-layer barrier is implemented together with this ADCV on the nanoscale technology node ICs in the industry. It is the goals of this work to study the EM performance of the ADCV structures with Ta/TaN/Ta tri-layer barrier in the 65 nm node ICs, and also make a comparison to that of the ADCV structures with Ta/TaN bi-layer barrier.

5.2 Experiment

5.2.1 Wafer Fabrication Processes

To investigate the EM performance of the laminated Ta/TaN/Ta tri-layer and Ta/TaN bi-layer barriers, 65 nm technology node based CMOS mass production wafers with a

diameter of 300 nm were used. Five-level Cu interconnects were embedded in the low-k dielectric. The Metal1 (M1) level was fabricated with SD Cu line. For the Metal2 (M2) to Metal4 (M4) levels, DD structures were fabricated using a “trench first” approach. The Metal5 (M5) level was implemented using dual damascene with a “via first” approach with the size of four times that of M2. The main Cu metallization processes include: a) self-ionized-plasma (SIP) with PVD tool for both diffusion barrier and Cu seed deposition, b) electro-copper plating (ECP) process for Cu filling, c) Cu chemical mechanical polishing (CMP) for planarization to remove excess Cu, and finally d) capped by SiCN layer to cover the dielectric and Cu. The organo-silicate glass (OSG) with a dielectric constant (k) of about 3.05 acts as the low-k inter-metal dielectric (IMD). The Cu metal line was surrounded by the diffusion barrier around its sides and bottom and a cap layer (SiCN) on top. The nominal thickness of each Ta and TaN layer was 3 nm for the Ta/TaN/Ta barrier. Meanwhile, for Ta/TaN barrier deposition, a 3 nm TaN layer was deposited onto the dielectric, followed by a 6 nm Ta layer. Therefore, the total thickness of both the Ta/TaN/Ta tri-layer and the Ta/TaN bi-layer barriers were the same. After DD structure formation process, in order to reduce the contact resistance at the via bottom interface, a degassing process was used to remove the condensed water or volatile contamination, and a high bias power Ar^+ preclean process was used before barrier deposition to clean the underlying metal line interface and there is one more high bias power Ar^+ resputtering (DCV) step after barrier deposition to selectively remove the

barrier at the via bottom. After resputtering, another 5 nm Ta layer was deposited to improve the adhesion of the seed Cu (ADCV structure).

With the ADCV structure, two split samples with bi-layer and tri-layer barriers are studied in this part and the detailed conditions are shown in Table 5.1.

Table 5.1. The splits of barrier type and ADCV conditions

Process split	Barrier type	Barrier thickness			Resputtering time	Resputtering power	Ta (re-deposit)
		Ta	TaN	Ta			
A	Bi-layer	-	3 nm	6 nm	15 s	650 W	5 nm
B	Tri-layer	3 nm	3 nm	3 nm	15 s	650 W	5 nm

5.2.2 EM Test Structure and EM Lifetime Testing

The test structure for the downstream EM was described in Fig. 3.10 of chapter 3. The width, height and length of M2 in the test structures were 0.3, 0.2 and 400 μm , respectively.

To achieve a better process evaluation and minimize EM failure probability, the wide feeder metal line (M2) was used. The package level EM tests were performed at a current density of $J = 2 \times 10^{-6} \text{ A/cm}^2$ and temperatures of 275 °C, 300 °C, and 325 °C. In this work, 25 samples, i.e. 25 frames (one frame contains 4×5 dies), were randomly chosen for each temperature. Therefore, for each process condition, there were 75

frames chosen from 2 wafers for three-temperature EM tests. The EM tests were conducted for 200 hours, and the EM failure criterion used in this work was 10% resistance increase from their initial value. Only the failed samples were counted in the calculation and evaluation.

The EM lifetimes were extracted from the fitting of the cumulative distribution function (CDF), and the Arrhenius plots for median time to failure (MTTF, also known as t_{50}) were used to evaluate the activation energy (E_a). Focused ion beam (FIB) and transmission electron microscope (TEM) were used to examine the tested structures.

5.3 Results and Discussion

5.3.1 Defective Die Percentage

Fig. 5.1 shows the average defective die percentages of the ADCV structures with bi-layer and tri-layer barriers. Defective die percentage is defined by the percentage of the number of defective dies scanned over the total number of dies scanned on one wafer. From Fig. 5.1, it is clearly seen that the defective die percentage in the ADCV structures with tri-layer barrier is about 0.9%, which is much lower than 1.3% of the ADCV structures with bi-layer barrier. This can be explained by better adhesion to

bottom Cu for tri-layer barrier (due to extra bottom Ta layer) than that for bi-layer barrier. Therefore, tri-layer barrier has more uniform barrier at the corner of via bottom, which benefits Cu seed as well as ECP ignition growth, and thus it has fewer Cu voids defects.

Fig. 5.1. Defective die percentages of the ADCV samples with bi-layer and tri-layer barriers, respectively.

5.3.2 EM Results of the Samples with Bi-layer and Tri-layer Barriers

During the EM test, Cu atoms in the EM test structure migrate along the electron flow and induce micro voids. The resistance of EM test structure can be monitored by the forced current and voltage. The resistance becomes larger when the voids are formed and become bigger. The sample is counted failure when the relative resistance of it is larger than 110%. Taking the condition of split B (in Table 5.1) with tri-layer barrier

tested under the temperature of 275 °C as example, its relative resistances vs. stress time are plotted in Fig. 5.2. As shown in the figure, two types of resistance degradation behavior, namely early and late failures, are observed.

Fig. 5.2. Relative resistances vs. time degradation plot for EM test. Two different modes of degradation behavior are indicated in the figure.

Fig. 5.3 shows the CDF plots of the EM time to failure (TTF) under the downstream electron flow with a current density of 2×10^6 A/cm² and temperatures of 275, 300, and 325 °C. Fig. 5.3 (a) and (b) are for the samples of splits A and B with bi-layer and tri-layer barriers, respectively. It is found that the TTF significantly increases as the stress temperature decreases. All distributions in the figures are not single log-normal,

as indicated by the poor fitting, and two clearly distinguishable branches in the CDF plots for each temperature are observed.

Fig. 5.3. CDF plots of time to failure at $T = 275, 300, 325\text{ }^{\circ}\text{C}$, and $J = 2 \times 10^{-6}\text{ A/cm}^2$

for the samples with bi-layer and tri-layer barriers, respectively.

The extensive failure analysis was carried out to explore the root causes. Fig. 5.4 shows the FIB images of failure analysis results of the samples with bi-layer and tri-layer barriers. It is observed that the void under via is the major cause for early failure (Fig. 5.4 (a) and (c)), while the void along the metal line is the predominant cause of late failure (Fig. 5.4 (b) and (d)), though via depletion is sometimes found in conjunction with metal line void. It is also seen that the samples with the bi-layer barrier have breakdown [circled in Fig. 5.4 (a) and 5.4 (b)] between the barrier and Cu

(M2), but the samples with the tri-layer barrier do not have, indicating the better performance of the tri-layer barrier.

Fig. 5.4. FIB images of EM test structures from PFA showing the downstream EM induced voids for the bi-layer of (a) early and (b) late failure, and the tri-layer of (c) early and (d) late failure. The dashed arrows indicate the direction of electron flow.

By using the physical bimodal fitting method [60], according to their failure mechanisms, the samples are divided into two failure categories: early failure and late failure. Taking all splits with $T = 300\text{ }^{\circ}\text{C}$ as examples, as shown in Fig. 5.5, the cumulative TTFs of early failure group (unfilled circles in the upper frame of the figure) and late failure group (unfilled squares in the lower frame) are plotted

together. The bi-layer and tri-layer samples of splits A and B are shown in Fig. 5.5 (a) and (b), respectively. The bimodal fitting plots with the late and early failures show better fittings than the plots in Fig. 5.3. The median time to failures (MTTF, t_{50}) and shape factors (σ , $1/\text{slope}$) can be extracted from Fig. 5.5 (a) and (b) for early and late failures of bi-layer and tri-layer barriers. All these data are summarized in Table 5.2.

Fig. 5.5. Bimodal fitting for samples of bi-layer tri-layer barriers at $T = 300\text{ }^{\circ}\text{C}$, respectively.

Fig. 5.6 shows the Arrhenius plots of MTTF as a function of temperature. By using exponential fitting, the activation energy (E_a) of each failure can be extracted from the exponential coefficient of Black equation [52]: $\text{MTTF} = AJ^{-n} \exp [E_a / (KT)]$, where A , J , n and k are constants in this project. Fig. 5.6 (a) shows the activation energies of late failure modes for split A samples with bi-layer barrier (0.761 eV) and split B

samples with tri-layer barrier (0.835 eV). While Fig. 5.6 (b) shows the activation energies of early failure modes for bi-layer barrier samples (0.798 eV) and tri-layer barrier samples (0.945 eV).

Compare Fig. 5.6 (a) and (b), the early failures of splits A and B show higher activation energies than the late failures. The discrepancy should be attributed to the different diffusion paths. The late failure has the cap SiCN/Cu interface as the predominant diffusion path which has a relatively low E_a [61]. The early failure, however, is due to the failure of the Cu/barrier interface which has a high E_a , as at via bottom, the Ta and Cu form metallic bonds with good thermal stability.

For the early failure related to via bottom depletion in Fig. 5.6 (b), the activation energy of tri-layer samples is 0.945 eV, which is higher than the 0.798 eV of the bi-layer samples. These differences are mainly related to the interfaces at the via bottom of the ADCV structures. The Ar^+ resputtering has very strong vertical selectivity and only removes the barrier and partial Cu layers from the via bottom, the bi-layer and tri-layer barrier structures at the sidewall of via are still remained. Therefore, the ADCV structures with tri-layer barrier have Ta/Cu interface at the via bottom, while the ADCV structures with bi-layer have Ta/Cu interface only at the right bottom of the via, and the TaN/Cu interface at the sidewall of the via.

Fig. 5.6. Arrhenius plots of the MTTF as a function of temperature for splits A and B.

Activation energies of both early and late failure modes are extracted.

All fitting results of MTTF, shape factor sigma (σ , 1/slope), P(A) (the probability of failure mode A), activation energy (E_a) and predicted EM lifetime from the physical

method for the samples of splits A and B with two failure modes are summarized in Table 5.2.

Table 5.2. Key parameters of splits A and B obtained by physical fitting methods.

Split	Barrier	T (°C)	MTTF (s)		Sigma		P (A) (%)		Ea (eV)		Lifetime	
			Early	Late	Early	Late	Early	Late	Early	Late	Early	Late
A	Bi-layer	275	1.8×10^5	8.7×10^5	0.69	0.34	44	56	0.80	0.76	$2.8 \cdot l^\#$	$33 \cdot l$
		300	9.1×10^4	4.7×10^5	0.78	0.28	44	56				
		325	4.3×10^4	2.2×10^5	0.72	0.33	44	56				
B	Tri-layer	275	2.3×10^5	9.7×10^5	0.57	0.31	24	76	0.94	0.83	$24 \cdot l$	$54 \cdot l$
		300	8.8×10^4	4.5×10^5	0.53	0.50	24	76				
		325	4.3×10^4	2.2×10^5	0.49	0.44	44	56				

[#]Due to the company's confidential policy, the EM lifetime (year) is presented in terms of the multiplication of l .

The predicted EM lifetime of the product in the product operation condition for each split was calculated by using Black's law (equation (5-1)) [52] with the data of MTTF, current density, E_a , N and σ in the EM test condition.

$$TTF_{operation} = MTTF_{TEST} \left(J_{operation} / J_{TEST} \right)^n \times \exp \left[E_a / k \left(1/T_{operation} - 1/T_{TEST} \right) \right] \times \exp(-N\sigma) \quad (5-1)$$

Where J is the current density, n is current exponent, k is Boltzmann's constant, T is the temperature and N is the inverse of the cumulative standardized normal distribution, σ is the lognormal deviation.

As shown in Table 5.2, the EM lifetime of the samples with tri-layer barrier is about 8 times of that of the samples with the bi-layer barrier. Since the bi-layer and tri-layer barrier patterns at the sidewall of the via bottom are mostly remained, the significantly enhanced EM lifetime is again mainly because the extra Ta layer in the tri-layer barrier can have a better interface due to the Ta-Cu metallic bond and better adhesion to M2 Cu than the TaN layer of the bi-layer barrier. This can be verified by the FIB images shown in Fig. 5.4.

5.4 Summary

The samples with tri-layer barrier in the 65 nm node technology show much lower defective die percentage and much longer EM lifetime than those with bi-layer barrier. This is because the extra Ta layer in the tri-layer barrier can have a better interface due to the Ta-Cu metallic bond and better adhesion to the Cu than the TaN layer of the bi-layer barrier.

Chapter 6 Effects of Via Bottom Removal on the Performance of the Advanced Direct Contact Via (ADCV) Structures

6.1 Introduction

Electromigration (EM) performance of Cu interconnects depends strongly on the effective diffusion barrier [24, 34]. For Cu dual damascene (DD) interconnects, in order to achieve the contamination-free via bottom with low via contact resistance, several structures like direct contact via (DCV) [33] and Advanced DCV (ADCV) [34, 35] have been studied. In the previous studies, the DCV structures were implemented together with Ta [33], TaN/Ta [34] or TiSiN/Ta [35] barrier. However, the ADCV with the tri-layer barrier is a new process that has not been reported yet. The goal of this chapter is to study the effects of via bottom removal on the electrical properties and electromigration performance of the ADCV structures with the Ta/TaN/Ta tri-layer barrier.

6.2 Experiment

65 nm technology node based 300 mm CMOS production wafers with advanced back end of line (BEOL) DD Cu and $k = 3.05$ organo-silicate glass (OSG) dielectrics were used to investigate the package level EM lifetime and activation energy. After the

stacked barrier layers were deposited with the self ionized plasma (SIP) technique, three Ar⁺ resputtering conditions, as shown in Table 6.1, were used to selectively remove the barrier at the via bottom. Then, another 5 nm Ta layer was deposited to improve the adhesion of the seed Cu (ADCV structure).

Table 6.1. Splits of ADCV structures with different via bottom removals.

Process split	Resputtering time	Resputtering bias power	Via bottom removal	Cu recess depth
A	10 s	650 W	Low	390 Å
B	15 s	650 W	Median	520 Å
C	10 s	1000 W	High	751 Å

Fig. 3.10 (in chapter 3) is the schematic of the test structure for the downstream EM where the electrons flow from M3/V2 to cathode M2. The width, height and length of M2 in the test structures were 0.3, 0.2 and 400 μm , respectively. To achieve a better process evaluation and minimize EM failure probability, the wide feeder metal line (M2) was used.

The EM tests were performed at a current density of 2×10^{-6} A/cm² and temperatures of 275 °C, 300 °C, and 325 °C. For each temperature, 25 samples or frames were randomly chosen and tested. Therefore, for each process condition at three temperatures, 75 frames were randomly chosen from 2 wafers for the EM tests. The time taken for the EM tests was 200 hours. The EM failure criterion used in this work

was 10% resistance increase from its initial value. Only the failed samples were used in the calculation and evaluation. The EM lifetimes were extracted by fitting the cumulative distribution function (CDF), and the Arrhenius plots for median time to failure (MTTF, also known as t_{50}) were used to derive the activation energy (E_a). FIB and TEM were employed to examine the tested structures.

6.3 Results and Discussion

6.3.1 Cu Recess Depth, Defective Die Percentage and Via Contact Resistance

As shown in Fig. 6.1, the TEM cross-section pictures of splits A to C illustrate via bottom volume enlarging and Cu recess increasing from 390 to 751 Å, as the removals increase from very low (split A) to high (split C). The barrier and Cu at the center of via bottom are resputtered onto the via sidewall by the argon bombardment. For the higher Ar^+ power 1000 W split, the Ar^+ has a larger accelerated speed when it reaches the via bottom; the bombardment occurs more acutely, and induces deeper Cu recess, specially at the center of via bottom and thus a cone-shape via bottom is obtained, as shown in Fig. 6.1 (c). However, because of the lower accelerated speed, the 650 W power split will obtain a better uniformed via bottom, thus an inverse trapezoidal shape is obtained with a flatter via bottom, as shown in Fig. 6.1 (b). The areas of the two shapes are almost equal to each other due to same total energy.

Fig. 6.1. TEM showing the Cu recess depths of the typical die for splits (a) A, (b) B, and (c) C with low, median and high removals, respectively.

Fig. 6.2 shows the wafer defective die percentages of the three splits. As shown in the figure, split B with median removal shows the lowest defective die percentage, followed by split C and split A. The higher defective die percentage of split C is possibly due to the poor adhesion to the upper deposition layer caused by high power argon bombardment damage at the sidewall and via bottom. Split A has the highest

risk of existing porous oxide and polymer residue at the bottom of the via due to the lower removal and it thus has the highest defective die percentage.

Fig. 6.2. Defective die percentages of three splits at M2 layer.

The via contact resistance was measured with the structure shown in Fig. 3.7 of chapter 3. Such structures were integrated on the scribe lines between every two dies. They were fabricated by dual damascene process together with the production dies under the same processing condition. Fig. 6.3 shows that the via contact resistances are 2.38, 1.77 and 1.65 ohm/via from splits A to C, respectively, decreasing significantly as the removal increases from low to high. It indicates that via geometry-size expansion is the main cause to the decrease of the via contact resistance.

Fig. 6.3. Via contact resistances of three splits at V2M2.

6.3.2 EM Results of the Samples with Three Different Via Bottom Removals

Fig. 6.4 shows the cumulative time to failure (TTF) plots of splits A to C for tri-layer barrier samples with low, median and high removals stressed under downstream electron flow with a current density of $2 \times 10^6 \text{ A/cm}^2$ (or $20 \times 10^3 \text{ A/}\mu\text{m}^2$) at temperatures of 275, 300 and 325 °C, respectively. The TTF significantly increases as the stress temperature decreases. All distributions in the figure are not single log-normal, as indicated by the poor fit, and two clearly distinguishable branches in the cumulative distribution function (CDF) plots for each temperature are observed.

Fig. 6.4. CDF plots of time to failure (TTF) for split A to split C at T = 275, 300, 325

°C and $J = 2 \times 10^6 \text{ A/cm}^2$.

Fig. 6.5 shows the focused ion beam (FIB) images of failure analysis results for three different Cu recess depth of ADCV samples. It is observed that the void under via is the major mechanism for the early failure, while the void along the metal line is the predominant mechanism of the late failure.

Fig. 6.5. FIB images of EM test structures from PFA showing the downstream EM induced voids for (a) early and (b) late failure.

By using the physical bimodal fitting method [60], according to their failure mechanisms, the samples are manually divided into two failure groups: early failure group and late failure group. For splits A to C at $T = 300\text{ }^{\circ}\text{C}$, as shown in Fig. 6.6, the cumulative TTFs of early failure group (unfilled circles in the upper frame of the figure) and late failure group (unfilled squares in the lower frame) are plotted together. Splits A to C with Low, median and high removals are shown in Fig. 6.6 (a) to (c), respectively. The bimodal plots with late and early failures show better fittings than the plots in Fig. 6.4. The median time to failures (MTTF, t_{50}) and shape factors (σ , $1/\text{slope}$) can be extracted from Fig. 6.6 (a) to (c) for early and late failures of tri-layer barrier with low, median and high removals at $T = 300\text{ }^{\circ}\text{C}$. They are the same for $T = 275$ and $325\text{ }^{\circ}\text{C}$. All these data are summarized in Table 6.2.

Fig. 6.6. Bimodal fitting using the physical method for splits A to C at $T = 300\text{ }^{\circ}\text{C}$.

Fig. 6.7 shows the Arrhenius plots of MTTF as a function of temperature for splits A to C. By using exponential fitting, the activation energy (E_a) of each failure can be extracted from the exponential coefficient of Black equation [52] introduced in section 3.5 of chapter 3: $MTTF = AJ^{-n} \exp[E_a/(kT)]$, where A, J, n and k are constants. Fig. 6.7 (a) and (b) show the activation energies (E_a) of late (0.80, 0.835,

and 0.789 eV) and early (0.89, 0.945, and 0.837 eV) failures for tri-layer barrier with low, median and high removals, respectively. The difference of E_a between early and late failures is mainly due to the different diffusion pathes. Because late failure results from line depletion, cap SiCN/Cu interface with a relatively low E_a become the predominant diffusion path. The higher E_a of early failure is then attributed to the Cu/barrier interface. From previous study [61], Cu_xN_y interlayer (ionic bond) is formed at the SiCN/Cu interface. At via bottom, the Ta and Cu forms a metallic bond with good thermal stability and interface[30, 62], which is of larger activation energy than the SiCN/Cu interface. For the early failure related to via bottom depletion in Fig. 6.7 (b), the activation energies are 0.89, 0.945, and 0.837 eV for tri-layer barrier with low, median and high removals, respectively. Split B is observed to have a highest E_a . Possible reasons on this will be discussed together with EM analysis later.

Fig. 6.7. Arrhenius plots of MTTF as a function of temperature for splits A to C.

All fitting results of MTTF, shape factor σ (1/slope), $P(A)$ (the probability of failure mode A), activation energy (E_a) and predicted EM lifetime from the physical method for splits A to C with two failure modes are summarized in Table 6.2. The predicted EM lifetime in the product operation condition for each split is calculated using Black's law [52]. For the early failure mode with via depletion, EM lifetime of split B is about four times of split A, and seven times of split C. It is believed that this better EM performance of split B is due to its better removal of contamination and polymer than the split A, and its less damage and less EM stress at the flat shape via bottom than the split C at the sharp cone shape via bottom.

Table 6.2. Key parameters of each split obtained by the physical fitting method.

Split	Removal	T (°C)	MTTF (seconds)		Sigma (σ)		P (A) (%)		Ea (eV)		Lifetime	
			Early	Late	Early	Late	Early	Late	Early	Late	Early	Late
A	Low	275	1.5×10^5	7.3×10^5	0.65	0.37	48	52	0.89	0.80	$1.8 \cdot m^*$	$10 \cdot m$
		300	5.9×10^4	3.9×10^5	0.67	0.49	52	48				
		325	3.1×10^4	1.7×10^5	0.69	0.32	64	36				
B	Median	275	2.3×10^5	9.7×10^5	0.57	0.31	24	76	0.94	0.83	$7 \cdot m$	$15 \cdot m$
		300	8.8×10^4	4.5×10^5	0.53	0.50	24	76				
		325	4.3×10^4	2.2×10^5	0.49	0.44	44	56				
C	High	275	1.3×10^5	7.6×10^5	0.53	0.36	32	68	0.84	0.79	m	$10 \cdot m$
		300	6.5×10^4	4.0×10^5	0.70	0.39	48	52				
		325	2.9×10^4	1.8×10^5	0.85	0.30	48	52				

* Due to the company's confidential policy, the EM lifetime (year) is presented in terms of the multiplication of m .

6.4 Summary

Median via bottom removal in the ADCV process with the tri-layer barrier is found to result in the lowest defective die percentage, highest activation energy and longest downstream EM lifetime. The better EM performance is due to its better removal of contamination and polymer by the proper removal, less damage and less EM stress at the flat via bottom because of its lower resputtering power. However, median via contact resistance is shown as the tradeoff to the long EM lifetime.

Chapter 7 A Novel 3-step Cu Seed Layer using Self-ionized Plasma (SIP) Technology

7.1 Introduction

The Cu seed layer provides a low resistance conduction path for the electro-copper plating (ECP) current that drives the ECP process and also acts as a nucleation layer for the initiation of the ECP Cu film growth. Conventional PVD technologies are the most widely used sources to deposit Cu seed layer, which include ionized metal plasma (IMP) [36], hollow cathode magnetron (HCM) [37], self-Ionized plasma (SIP) [38]. As each technology node feature size gets smaller and smaller, in the Cu metallization scheme, the trenches and via become narrower and deeper in the damascene structures. The extendibility of the conventional PVD technologies is challenged. The fundamental issue of the PVD sputtering source is ionization rate. Because the step coverage largely depends on the metal ion fraction during deposition, increasing the ionization rate of the sputtering system can improve the step coverage. A PVD sputtering source based on a high power density concept has been developed [40]. However, this sputtering source consumes much higher power (40-60 kW) than other methods in order to achieve higher level step coverage. It's not suitable for the mass production in the industry due to its high power consumption, tool complexity and ultimately high cost.

Every technology of Cu seed deposition method has its tradeoff to the step coverage, adhesion performance to barrier, or process cost. Therefore, it becomes a challenge nowadays to find a better Cu seed deposition method to achieve good step coverage and at the same time keep the comparable power consumption. This work shows an optimized 3-step ac power of Cu seed deposition method using self-Ionized plasma (SIP, one of PVD methods) technology. Its electrical properties, defects, yield and structure profiles are comparatively studied with those of the conventional 2-step Cu seed ac power deposition method.

7.2 Experiment

65 nm technology node based 300 mm CMOS production wafers, which were implemented with advanced back end of line (BEOL) dual damascene (DD) Cu interconnects and organo-silicate glass (OSG) dielectrics ($k = 3.05$), were used for the experiment.

After Ta/TaN/Ta tri-layer barrier deposited together with ADCV process, the Cu seed layer was deposited to provide a low resistance conduction path for the electro-copper plating (ECP) current and also act as a nucleation layer for the initiation of the electroplated Cu film growth. In this work, SIP technology is used for Cu seed layer deposition.

SIP is PVD technology that makes use of a dc magnetron sputtering source using sustained self-sputtering to deposit copper onto the wafers. The sputtered Cu atoms were ionized in the magnetron plasma, and some Cu ions were accelerated to sputter more Cu atoms out of the Cu target. The plasma in the process is sustained by the ionization of sputtered neutrals and secondary metal ions. No additional energetic particles, such as argon ions, are needed to maintain the plasma. A threshold power (dc magnetron power, 38 kW in my work) needs to be applied to maintain the operation and its value depends on the size of the magnetron.

Except the 38 kW dc power, there is another ac bias applied. The ac bias is mainly to enhance the vertical directionality of the ionized Cu. It reduces overhang at the top of the trench, and leads to a larger trench opening and thus benefits gap filling capability. For conventional SIP Cu seed deposition method, it used 2-step deposition ac powers of 500:1000 W and time ratio of 1:2. The new method of Cu seed deposition used 3-step ac powers of 0:500:1000 W and time ratio of 1:1:1. The difference was that the 3-step Cu seed used an extra zero ac bias at its initial deposition step. Fig. 7.1 illustrates the Cu seed deposition ac powers changing with deposition time for the two types of Cu seed deposition processes. Two pieces of wafers were used for each type of seed deposition.

Fig. 7.1. Deposition powers of the 2-step (solid line) and 3-step (dash line) Cu seed layers.

The wafer acceptance test (WAT) for BEOL mainly tests the electrical properties of Cu interconnect. These include metal line leakage current, metal line sheet resistance and metal via contact resistance. Their test structures are shown in Fig. 3.8, Fig. 3.4 and Fig. 3.7 of chapter 3, respectively. The test structures were integrated in the scribe lines, which lay between every two dies. They were fabricated by dual damascene process together with production dies under the same processing condition. Therefore, they had same electrical properties with the Cu interconnects in the dies.

The electrical properties, defective die percentages, yields, and defect failure related Bin2 of two splits were measured and collected to do comparative study. The transmission electron microscope (TEM) was used to evaluate the structure profiles.

7.3 Results and Discussion

7.3.1 Electrical Properties

As shown in Fig. 7.2 (a), the average metal line leakage current is 3.85 pA and 4 pA for the 3-step and 2-step Cu seed samples, respectively. The averages of metal line sheet resistances and via contact resistances are both comparable for those samples with 3-step and 2-step Cu seed, as shown in Fig. 7.2 (b) and Fig. 7.3, respectively. Their test structures have been introduced in the experiment part in section 7.2.

Fig. 7.2. (a) Leakage currents and (b) sheet resistances of the metal lines with 3-step and 2-step Cu seed layers.

Fig. 7.3. Contact resistances of the metal via with 3-step and 2-step Cu seed layers.

7.3.2 Defective Die Percentage, Yield and Bin2 (Defect Related Failure Bin)

Cu void defects (or missing metal defects) are scanned after M2 SiCN cap layer deposited and presented in term of defective die percentage defined as the ratio of the number of defective dies scanned (dots in the defect maps) over the total number of dies scanned (all dies in the white vertical lines area) on the wafer. Fig. 7.4 shows the defective die percentages and defect maps of the samples with 3-step and 2-step Cu seed layers. As shown in the figure, the 3-step Cu seed samples show fewer Cu void defects with about 3% lower in term of defective die percentage than the 2-step Cu seed samples. The Cu void defects at the areas of the wafer center and donut are obvious reduced for the 3-step Cu seed samples, as shown in the defect maps of wafer 21 and 25.

Fig. 7.4. Defective die percentages and defect maps of the samples with 3-step and 2-step Cu seed layers, respectively.

Fig. 7.5(a) and 7.5(b) show the yields and Bin2 (Defects at static random access memory (SRAM) area of the die induced failure Bin) of sample wafers with 3-step and 2-step Cu seed, respectively. The average yield of the wafers with 3-step Cu seed is 0.5% higher than that of the wafers with 2-step Cu seed. The higher yield is mainly contributed from 0.34% less of Bin2. The yield is the percentage of functional dies over all the dies on the wafer. Bin2 is the percentage of non functional dies due to the failure of Bin2 over all the dies. (The test procedures of yield test and more detail of Bin2 can be referred to section 3.4 of chapter 3.)

Fig. 7.5. (a) Yields and (b) Bin2 of the wafers with 3-step and 2-step Cu seed.

7.3.3 TEM Images of Structure Profiles

For the 2-step Cu seed deposition, the first step 500 W ac power is suspected to cause barrier damage and induce barrier discontinuity, which thus cause poor gap-fill capability. The 3-step Cu seed deposition introduces a zero ac bias power as its first step Cu seed deposition, as it is believed to protect the barrier during the deposition process. The detailed procedures for the two Cu seed deposition methods are illustrated in Fig. 7.6(a) and 7.6(b), respectively.

Fig. 7.6. Mechanism comparison of (a) the 3-step and (b) 2-step Cu seed processes.

The TEM measurements were done after Cu plating with cap layer remaining (TiN and TEOS). In Fig. 7.7, the TEM images show that the 2-step Cu seed causes discontinuity at the point film (circled in the figures) among the barrier layer, tetra-ethyl-ortho-silicate (TEOS) and low k (LK) dielectric layers, while the 3-step seed shows less discontinuity effect. The improvement with 3-step Cu seed is due to its initial zero bias deposition step with which the Cu seed is deposited onto barrier in a proper speed (magnetron dc power still exist to support deposition) and covered the barrier smoothly with less damage. As a result, it reduces the discontinuity of the barrier and pursues better step coverage, and thus fewer defects (better gap filling capability) and higher yield.

Fig. 7.7. TEM images showing the barrier discontinuity performance for the metal line with (a) 3-step and (b) 2-step Cu seed layers. Barrier/Cu seed/barrier/Cu seed stack layers were deposited to do Cu seed evaluation in figures.

Final bias power 1000 W is used for overhang reduction for both methods. Fig. 7.8 shows the overhang of the samples with 3-step and 2-step seed layers measured by TEM. As shown in the figure, the 3-step Cu seed slightly improves the Cu seed step coverage at the kink location with less overhang effect (a little bit better). This is again attributed to the introduction of the zero ac bias step which has less damage and favors the step coverage.

Fig. 7.8. TEM images show the overhang and step coverage at kink location for (a) the 3-step and (b) 2-step Cu seed methods. Barrier/Cu seed/barrier/Cu seed stack layers were deposited to do Cu seed evaluation in two figures.

7.4 Summary

The metal lines with 3-step and 2-step seed layers are comparatively investigated. The 3-step Cu seed with ac powers of 0:500:1000 W (time ratio of 1:1:1) results in a smaller metal line leakage current than the 2-step Cu seed with ac powers ratio of 500:1000 W (time ratio of 1:2). The metal line sheet resistance and metal via contact resistance are comparable for both types of Cu seed deposition methods. For the samples with 3-step Cu seed, the defective die percentage is 3% lower and the yield is 0.5% higher than those with 2-step Cu seed. TEM images show that the new 3-step Cu seed results less discontinuity at the point film among the barrier layer, TEOS and

LK dielectric layers. The Cu seed step coverage is also improved at the kink location with slightly smaller overhang. These are attributed to the introduction of the zero ac power step with which the Cu seed can be deposited on the barrier with a proper deposition speed and thus less damage caused.

Chapter 8 Conclusion and Recommendations

8.1 Conclusion

In this work, the Ta/TaN/Ta tri-layer barrier in the advanced direct contact via (ADCV) structures, via bottom removal and the 3-step Cu seed for dual damascene (DD) Cu metallization were studied and they were implemented successfully in 65 nm technology-node products.

The comparative studies of the samples with tri-layer and bi-layer barriers show that the samples with tri-layer barrier have lower defective die percentage. Downstream electromigration test reveals that the samples with tri-layer barrier have EM lifetime three times more than those of the samples with bi-layer barrier. This is because the lower Ta layer of the tri-layer barrier has a better interface as well as better adhesion with M2 Cu than the TaN layer of the bi-layer barrier.

ADCV structures with three different via bottom removals were comparatively examined. Median removal in the ADCV with the tri-layer barrier split is observed to have the lowest defective die percentage. Meanwhile, the highest activation energy and the longest downstream EM lifetime are also achieved with this process. It is believed that the better EM performance is due to the better removal of contamination and polymer, less damage and less EM stress at the via bottom because of the lower

resputtering power. However, median via contact resistance with this process is the tradeoff to the longer EM lifetime.

The metal lines with 3-step Cu seed layer with ac powers of 0:500:1000 W (time ratio of 1:1:1) show a smaller metal line leakage current than those with 2-step Cu seed with ac powers of 500:1000 W (time ratio of 1:2). The metal line sheet resistance and metal via contact resistance are comparable for the two Cu seed layers. The samples with 3-step Cu seed layer have 3% lower defective die percentage and 0.5% higher yield than those with 2-step Cu seed layer. TEM images show that the 3-step Cu seed can have better barrier continuity at the point film among the barrier layer, tetra-ethyl-ortho-silicate (TEOS) and low k (LK) dielectric layers, and the Cu seed step coverage is also improved at the kink location with slightly less overhang. With its initial zero ac bias power, it is very likely that the Cu seed can be deposited onto the barrier with a proper deposition rate resulting in less damage.

8.2 Recommendations for future research

8.2.1 For 65 nm Technology Node Products

- 1) Cu seed thickness can be further optimized to improve gap filling capability based on current BEOL technology. The Cu seed layer cannot be too thin. It should be

sufficient not to impact the wafer uniformity and not to cause the overhang as the thin seed may have poor step coverage within trench and via, which results poor uniformity and poor Cu fill. The Cu seed thickness cannot be too thick either, because increasing Cu seed thickness may increase the aspect ratio, which may induce overhang problem.

- 2) An optimization study on the electro-copper plating (ECP) current for gap filling and bulk filling can be conducted based on current BEOL technology. This practice can also improve gap filling capability and reduce the Cu void defects. Large ECP current can induce more Cu ions into the metal line and via to enhance Cu deposition. It can reduce the overhang problem and have large critical dimension (CD) at the via top, thus can have lower risk of closing the via top during ECP Cu gap filling. However, ECP current cannot be too large, as there is not sufficient time for Cu to grow well layer by layer which leads to very loose structures, and therefore, resulting in shorter electromigration lifetime.

8.2.2 For 45 nm and below technology node products

As the CMOS technology continues to scale down to 45 nm node and below, for BEOL interconnects, all the thickness, width, length of the LK as well as metal need to shrink accordingly to adapt the front end of line (FEOL) CMOS device dimension.

From the methodology point of view, the defect scanner needs to be upgraded in order to detect smaller size defects and particles. From the process point of view, the barrier and seed deposition processes as well as ECP gap filling process have to be further optimized. The layer thickness, step coverage and interface quality of the barrier and seed will become the major concerns to the electrical property, defects and EM performance. The ECP current, chemical composition and concentrations also need adjustment to ensure a void free and high quality Cu layer.

List of Publications

F. X. Deng, D. H. Zhang, H. Liao, and H. Hu, "Advanced Direct Contact Via (DCV) Process with Ta/TaN/Ta Tri-layer Barrier for Advanced BEOL Dual Damascene Cu Interconnects," presented at *17th IEEE International Symposium on the Physical & Failure Analysis of Integrated Circuits*, Singapore, 2010, pp. 87-90.

L. Y. Yang, D. H. Zhang, F. X. Deng, and C. Y. Li, "Electrical Properties and Thermal Stability of Ta/TaN/SiCN Tri-layer Barrier," in *17th IEEE International Symposium on the Physical & Failure Analysis of Integrated Circuits*, Singapore, 2010, pp. 155-157.

F. X. Deng, D. H. Zhang, H. Liao, and H. Hu, "Comparative Study of Ta/TaN/Ta Tri-layer and Ta/TaN Bi-layer Barriers," *IEEE Transactions on Device and Materials Reliability*, submitted for publication, 2010.

F. X. Deng, D. H. Zhang, H. Liao, and H. Hu, "A Novel 3-Step Cu Seed Layer using Self-ionized Plasma (SIP) Technology," *Thin solid film*, submitted for publication, 2010.

Bibliography

- [1] B. Zhao, "Advanced interconnect systems for ULSI technology," in *Proceedings of International Conference on Solid-State and Integrated Circuit Technology*, 1998, pp. 43-46.
- [2] Y. Ye, D. Ma, A. Zhao, P. Hsieh, W. Tu, X. Deng, G. Chu, C. Mu, J. Chow, P. Moon, and S. Sherman, "Development of Cu etch process for advanced Cu interconnects," in *Proceedings of the IEEE 1998 International Interconnect Technology Conference*, 1998, pp. 235-237.
- [3] M. T. Wang, Y. C. Lin, and M. C. Chen, "Barrier Properties of Very Thin Ta and TaN Layers Against Copper Diffusion," *Journal of the Electrochemical Society*, vol. 145, pp. 2538-2545, 1998.
- [4] S. Shingubara, Y. Nakasaki, and H. Kaneko, "Electromigration in a single crystalline submicron width aluminum interconnection," *Applied Physics Letters*, vol. 58, pp. 42-44, 1991.
- [5] T. Nitta, T. Ohmi, T. Hoshi, S. Sakai, K. Sakaibara, S. Imai, and T. Shibata, "Evaluating the Large Electromigration Resistance of Copper Interconnects Employing a Newly Developed Accelerated Life-Test Method," *Journal of the Electrochemical Society*, vol. 140, pp. 1131-1137, 1993.
- [6] P. L. Pai and C. H. Ting, "Selective electroless copper for VLSI interconnection," *Electron Device Letters*, IEEE, vol. 10, pp. 423-425, 1989.
- [7] Y. A. Wahab, A. F. Ahmad, and Z. Awang, "Comparison of Missing Metal Defect Formation on He In-Situ and Furnace Annealed Electroplated Copper Films," in *SCORed 2006. 4th Student Conference on Research and Development*, 2006, pp. 53-57.
- [8] C. K. Hu, L. Gignac, E. Liniger, and R. Rosenberg, "Electromigration in on-chip single/dual damascene Cu interconnections," *Journal of the Electrochemical Society*, vol. 149, pp. G408-G415, 2002.
- [9] L. Y. Yang, D. H. Zhang, C. Y. Li, and P. D. Foo, "Comparative study of Ta, TaN and Ta/TaN bi-layer barriers for Cu-ultra low-k porous polymer integration," *Thin Solid Films*, vol. 462-463, pp. 176-181, 2004.
- [10] G. B. Alers, X. Lu, J. H. Sukamto, S. K. Kailasam, J. Reid, and G. Harm, "Influence of copper purity on microstructure and electromigration," in

- Proceedings of the IEEE 2004 International Interconnect Technology Conference*, 2004, pp. 45-47.
- [11] I. U. Abbulimen, T. Lam, A. Kamto, S. Burkett, L. Schaper, and L. Cai, "Effect of via profile on copper seed layer deposition for electroplating," in *Region 5 Technical Conference*, 2007 IEEE, 2007, pp. 102-104.
- [12] S. Riedel, J. Rober, S. E. Schulz, and T. GeBner, "Stress in copper films for interconnects," *Microelectronic Engineering*, vol. 37-38, pp. 151-156, 1997.
- [13] E. Kondoh, "Material characterization of Cu(Ti)-polyimide thin film stacks," *Thin Solid Films*, vol. 359, pp. 255-260, 2000.
- [14] P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, "Damascene copper electroplating for chip interconnections," *IBM Journal of Research and Development*, vol. 42, pp. 567-574, 1998.
- [15] S. Venkatesan, A. V. Gelatos, S. Hisra, B. Smith, R. Islam, J. Cope, B. Wilson, D. Tuttle, R. Cardwell, S. Anderson, M. Angyal, R. Bajaj, C. Capasso, P. Crabtree, S. Das, J. Farkas, S. Filipiak, B. Fiordalice, M. Freeman, P. V. Gilbert, M. Herrick, A. Jain, H. Kawasaki, C. King, J. Klein, T. Lii, K. Reid, T. Saaranen, C. Simpson, T. Sparks, P. Tsui, R. Venkatraman, D. Watts, E. J. Weitzman, R. Woodruff, I. Yang, N. Bhat, G. Hamilton, and Y. Yu, "A high performance 1.8 V, 0.20 μm CMOS technology with copper metallization," in *Electron Devices Meeting, 1997. IEDM '97. Technical Digest., International*, 1997, pp. 769-772.
- [16] R. Rosenberg, D. C. Edelstein, C. K. Hu, and K. P. Rodbell, "Copper metallization for high performance silicon technology," *Annual Review of Materials Science*, vol. 30, pp. 229-262, 2000.
- [17] T. Gupta, "The Copper Damascene Process and Chemical Mechanical Polishing" in *Copper Interconnect Technology*: Springer New York, 2009, p. 267.
- [18] E. R. Weber, "Transition metals in silicon," *Applied Physics A: Materials Science & Processing*, vol. 30, pp. 1-22, 1983.
- [19] J. O. Olowolafe, J. Li, and J. W. Mayer, "Interactions of Cu with CoSi_2 , CrSi_2 and TiSi_2 with and without TiN_x barrier layers," *Journal of Applied Physics*, vol. 68, pp. 6207-6212, 1990.

- [20] Z. L. Yuan, D. H. Zhang, C. Y. Li, K. Prasad, C. M. Tan, and L. J. Tang, "A new method for deposition of cubic Ta diffusion barrier for Cu metallization," *Thin Solid Films*, vol. 434, pp. 126-129, 2003.
- [21] Z. L. Yuan, D. H. Zhang, C. Y. Li, K. Prasad, and C. M. Tan, "Thermal stability of Cu/a-Ta/SiO₂/Si structures," *Thin Solid Films*, vol. 462-463, pp. 284-287, 2004.
- [22] D. H. Zhang, S. W. Loh, C. Y. Li, R. Liu, and A. T. S. Wee, "Effect of a thin ionised-metal-plasma deposited Cu layer on the properties and thermal stability of Cu/TaN/SiO₂/Si structures," *IEEE Transactions on Device and Materials Reliability*, pp. 174-178, 2001.
- [23] S. W. Loh, D. H. Zhang, C. Y. Li, R. Liu, and A. T. S. Wee, "Study of copper diffusion into Ta and TaN barrier materials for MOS devices," *Thin Solid Films*, vol. 462-463, pp. 240-244, 2004.
- [24] H. Lee and S. D. Lopatin, "The influence of barrier types on the microstructure and electromigration characteristics of electroplated copper," *Thin Solid Films*, vol. 492, pp. 279-284, 2005.
- [25] E. Ivanov, "Evaluation of tantalum silicide sputtering target materials for amorphous Ta-Si-N diffusion barrier for Cu metallization," *Thin Solid Films*, vol. 332, pp. 325-328, 1998.
- [26] O. Adciello, S. Chevacaroenkul, M. S. Ameen, and J. Duarte, "Controlled ion beam sputter deposition of W-Cu-W layered films for microelectronic applications," *Journal of Vacuum Science & Technology A*, vol. 9, pp. 625-632, 1991.
- [27] J. O. Olowolafe, C. J. Mogab, R. B. Gregory, and M. Kottke, "Interdiffusions in Cu/reactive-ion-sputtered TiN, Cu/chemical-vapor-deposited TiN, Cu/TaN, and TaN/Cu/TaN thin-film structures: Low temperature diffusion analyses," *Journal of Applied Physics*, vol. 72, pp. 4099-4103, 1992.
- [28] S. Kordic, J. Torres, L. Liauzu, C. Verove, P. Vannier, R. Gonella, P. Gayet, E. V. d. Vegt, and J. M. Gilet, "Cu Dual Damascene Integration Issues," in *VLSI Multilevel Interconnection Conference*, 1999, pp. 53-62.
- [29] S.-Q. Wang, S. Suthar, C. Hoeflich, and B. J. Burrow, "Diffusion barrier properties of TiW between Si and Cu," *Journal of Applied Physics*, vol. 73, pp. 2301-2320, 1993.

- [30] Q.-T. Jiang, R. Faust, H. Lam, and J. Mucha, "Investigation of Ta, TaN and TaSiN barriers for copper interconnects," in *Proceedings of the IEEE 1999 International Interconnect Technology Conference*, 1999, pp. 125-127.
- [31] R. Hübner, M. Hecker, N. Mattern, V. Hoffmann, K. Wetzig, C. Wenger, H. J. Engelmann, C. Wenzel, E. Zschech, and J. W. Bartha, "Structure and thermal stability of graded Ta-TaN diffusion barriers between Cu and SiO₂," *Thin Solid Films*, vol. 437, pp. 248-256, 2003.
- [32] J. P. Wang, Y. K. Su, and J. F. Chen, "Effects of surface cleaning on stressvoiding and electromigration of Cu-damascene interconnection," *IEEE Transactions on Device and Materials Reliability*, vol. 8, pp. 210-215, 2008.
- [33] C. Y. Li, D. H. Zhang, J. J. Wu, D. X. Qi, S. S. Su, Y. Qian, Y. F. Chow, L. T. Koh, and P. D. Foo, "Barrier-free direct-contact-via (DCV) structures for copper interconnects," *Electronics Letters*, vol. 38, pp. 1026-1028, 2002.
- [34] S. J. Joo, H. C. Lee, I. C. Baek, C. Shim, J. H. Hong, J. W. Han, K. H. Kim, and Y. Kim, "Selectively Formed Metal Organic Chemical Vapor Deposition TiSiN and Ta Barrier Metal Using Direct Contact Via Process for Sub-65 nm Interconnects," *Japanese Journal of Applied Physics*, vol. 46, p. 1947, 2007.
- [35] M. H. Lee, H. C. Lee, C. H. Park, J. W. Han, and K. W. Paik, "Improvement of device performance by optimizing the advanced DCV process condition in dual-damascene Cu interconnects," *Journal of the Electrochemical Society*, vol. 156, pp. H644-H647, 2009.
- [36] B. Chin, P. Ding, B. Sun, T. Chiang, D. Angelo, I. Hashim, Z. Xu, S. Edelstein, and F. Chen, "Barrier and Seed Layer for Damascene Copper Metallization " in *Solid State Technology*, July, 1998, pp. 141-147.
- [37] K. A. Ashtiani, E. Klawuhn, D. Hayden, M. Ow, K. B. Levy, and M. Danek, "A new hollow-cathode magnetron source for 0.10 μ m copper applications," in *Proceedings of the IEEE 2000 International Interconnect Technology Conference*, 2000, pp. 37-39.
- [38] J. Fu, P. Ding, F. Dorleans, Z. Xu, and F. Chen, "Deposition of copper by using self-sputtering," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 17, pp. 2830-2834, 1999.
- [39] P. J. Ding, P. Gopalraja, J. M. Fu, J. Yu, Z. Xu, and F. S. Chen, "Advanced Cu barrier/seed development for 65nm technology and beyond," in *Proceedings of*

- 7th International Conference on Solid-State and Integrated Circuits Technology*, 2004, pp. 486-488 vol.1.
- [40] P. Gopalraja, S. Rengarajan, J. Forster, and X. Tang, "Advanced Engineering of PVD and ALD based Barriers for Sub-micron Device Generations in Dual Damascene Copper Interconnects," *Semiconduct Technology*, vol. 48, pp. 42-46, 2003.
- [41] L. Velo, A. Paranjpe, M. Moslehhi, G. H. Shang, T. Omstead, Z. M. Liu, R. Bubber, C. Davis, D. Campbell, and B. Reja, "Cluster tool technology for CVD Cu based Multilevel Metallization," in *VLSI Multilevel Interconnection Conference*, Santa Clara, CA, USA, 1998, pp. 16-18.
- [42] S. Wickramanayaka, H. Nagahama, E. Watanabe, T. Hayashi, M. Sato, Y. Nakagawa, S. Hasegawa, S. Mizuno, and Y. Numasawa, "Seed-layer Deposition for Sub 0.25 μm Cu Metallization Using a Line Cusp Magnetron Plasma Source," *Material Research Society proceeding*, vol. 612, p. D6.3, 2000.
- [43] Y. C. Ee, Z. Chen, L. Chan, A. K. H. See, S. B. Law, K. C. Tee, K. Y. Zeng, and L. Shen, "Effect of processing parameters on electroless Cu seed layer properties," *Thin Solid Films*, vol. 462-463, pp. 197-201, 2004.
- [44] W. L. Goh and K. T. Tan, "The use of electroless copper seed in electrochemical deposited copper interconnect," *Thin Solid Films*, vol. 462-463, pp. 275-278, 2004.
- [45] Y. Shacham-Diamand, V. Dubin, and M. Angyal, "Electroless copper deposition for ULSI," *Thin Solid Films*, vol. 262, pp. 93-103, 1995.
- [46] C. Y. Mak, S. Nakahara, Y. Okinaka, H. S. Trop, and J. A. Taylor, "Annealing Behavior of Fine-Grained Electroless Copper Deposits," *Journal of the Electrochemical Society*, vol. 140, pp. 2363-2369, 1993.
- [47] J. Reid, S. Mayer, E. Broadbent, E. Klawuhn, and K. Ashtiani, "Factors Influencing Damascene Feature Fill Using Copper PVD and Electroplating," *Solid State Technology*, vol. 43, pp. 86-103, July 2000.
- [48] R. Doering and Y. Nishi, "Damascene Copper Electroplating," in *Handbook of semiconductor manufacturing technology: Technology & Engineering*, 2007, p. 16.37.

- [49] S. Varadajaran, D. Kalakad, and T. Cacouris, "Understanding and Reducing Copper Defects," *Semiconduct International*, vol. 25, pp. 215-130, 2002.
- [50] Y. A. Wahab, A. F. Ahmad, and Z. Awang, "Queue Time Impact on Defectivity at Post Copper Barrier Seed, Electrochemical Plating, Anneals and Chemical Mechanical Polishing," in *ICSE '06. IEEE International Conference on Semiconductor Electronics*, 2006, pp. 938-943.
- [51] C. H. Shih, S. W. Chou, C. J. Lin, T. Ko, H. W. Su, C. M. Wu, M. H. Tsai, W. S. Shue, C. H. Yu, and M. S. Liang, "Design of ECP additive for 65 nm-node technology Cu BEOL reliability," in *Proceedings of IEEE 2005 International Interconnect Technology Conference*, 2005, pp. 102-104.
- [52] J. R. Black, "Electromigration--A brief survey and some recent results," *IEEE Transactions on Electron Devices*, vol. 16, pp. 338-347, 1969.
- [53] K.-D. Lee and P. S. Ho, "Statistical study for electromigration reliability in dual-damascene Cu interconnects," *IEEE Transactions on Device and Materials Reliability*, vol. 4, pp. 237-245, 2004.
- [54] I. Nutek, "SIGNAL TO NOISE RATIOS (S/N) FOR STATIC AND DYNAMIC SYSTEMS " in *Design of Experiments (DOE) and the Taguchi Approach*, available: www.nutek-us.com/wp-doe.html
- [55] C. Ryu, K.-W. Kwon, A. L. S. Loke, H. Lee, T. Nogami, V. M. Dubin, R. A. Kavari, G. W. Ray, and S. S. Wong, "Microstructure and reliability of copper interconnects," *IEEE Transactions on Electron Devices*, vol. 46, pp. 1113-1120, 1999.
- [56] C. Y. Li, D. H. Zhang, L. He, J. J. Wu, Y. Qian, L. T. Koh, B. Yu, P. D. Foo, and J. Xie, "Comparative study of ionized metal plasma Ta, TaN and multistacked Ta/TaN structure as diffusion barriers for Cu metallization," *Surface Review and Letters*, vol. 8, pp. 459-464, 2001.
- [57] C. Y. Li, D. H. Zhang, J. J. Wu, D. X. Qi, Y. Qian, W. H. Li, and P. D. Foo, "Effect of underlayers on the stress of Cu films prepared using ionized metal plasma," *International Journal of Modern Physics B*, vol. 16, pp. 189-196, 2002.
- [58] D. Edelstein, "A high performance liner for copper damascene interconnects," *Proceedings of IEEE International Interconnect Technology Conference*, pp. 9-11, 2001.

List of Publications

- [59] A. Furuya, N. Ohtsuka, N. Ohashi, S. Kondo, and S. Ogawa, "Low-resistivity atomic-layer-deposited- TaN with atomic-layer-deposited- TaN /physical-vapor-deposited-Ta multilayer structure for multilevel Cu damascene interconnect," *Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films*, vol. 24, pp. 103-105, 2006.
- [60] M. H. Lin, Y. L. Lin, K. P. Chang, K. C. Su, and T. Wang, "Copper interconnect electromigration behavior in various structures and precise bimodal fitting," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, vol. 45, pp. 700-709, 2006.
- [61] J. Noguchi, N. Ohashi, T. Jimbo, H. Yamaguchi, K. i. Takeda, and K. Hinode, "Effect of NH₃-plasma treatment and CMP modification on TDDB improvement in Cu metallization," *Electron Devices, IEEE Transactions on*, vol. 48, pp. 1340-1345, 2001.
- [62] Y. Zhao and G. Lu, "First-principles simulations of copper diffusion in tantalum and tantalum nitride," *Physical Review B*, vol. 79, p. 214104, 2009.