Negative-bias temperature instability (NBTI) characterization of MOSFETS employing decoupled-plasma-nitrided gate oxides

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

NBTI CHARACTERIZATION OF MOSFETS EMPLOYING DPN-NITRIDED
GATE OXIDES

**NEGATIVE-BIAS TEMPERATURE
INSTABILITY (NBTI)
CHARACTERIZATION OF MOSFETS
EMPLOYING DECOUPLED-PLASMA-
NITRIDED GATE OXIDES**

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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2011

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Abstract

The power-law time exponent n of negative-bias temperature instability (NBTI) is perceived to be able to explain the underlying physical mechanism. At present, molecular hydrogen is hypothesized as the diffusing specie, as it is able to reconcile the theoretical value of 0.167 with the experimentally obtained range of ~ 0.14 -0.17. Recent findings revealed the presence of deep-level hole traps (DLHTs) near the Si bandgap, which may not have been discounted in earlier deductions of n .

The purpose of this thesis is to establish correlations between those trap holes and measured time exponent, as well as to explore the change in oxide trap distribution away from the Si/SiO₂ interface, during NBTI stress. The former was achieved by use of static and bipolar stress, together with charge pumping. This isolated the distortion DLHTs had on the time exponent values due to interface states. The latter was determined using an in-house flicker noise ($1/f$) measurement system.

Results concluded that the presence of DLHTs led to an under-estimation of the time exponent values, to ~ 0.3 -0.5, and the values were attributed to interfacial trapped charge above the Si mid-gap. In addition, these trapped charges exhibited both acceptor-like and donor-like behaviours, and may be related to E' centres. $1/f$ noise data revealed that for thick gate devices, some neutral oxide traps were generated during NBTI.

Chapter 1: INTRODUCTION

1.1 Introduction to MOSFET

The invention of integrated circuits (ICs) marked a paradigm shift in the development of electronic applications [1]. Electronic circuits were greatly miniaturised to improve performance, and their mass production capabilities over semiconductor substrates reduced cost by allowing many circuit components to be built simultaneously via lithography. The most fundamental unit driving integrated circuits is the metal-oxide-semiconductor field effect transistor (MOSFET), which functions as a switch by varying voltage support at the gate terminal. The name MOSFETs was derived from the use of metal material for the gate, SiO₂ the gate dielectric and silicon as the substrate. In today's state-of-the-art wafer fabrication processes, nitrogen is added to SiO₂ to improve transistor performances. Nonetheless, the term MOSFET is still applicable for devices operating under the same principles as its predecessors. Since their inception into mass manufacturing of ICs in the 1970s, MOSFETs have been continually subjected to reduction in physical dimension in order to improve performance. The development, also known as scaling, is necessary in order to increase speed, lower power consumption and increase packing density of transistors. As a result, semiconductor products were able to offer more functional capabilities at increased speed and reduced physical size. This led to Moore's Law prediction that the number of components in a chip would double every year for the first decade, and subsequently double in density for every two years.

1.2 Critical Issues Related to Gate Oxide Scaling

Theoretically, if the scaling down of MOSFET physical dimensions is done at a constant α (<1), corresponding adjustment of supply voltage ($\times\alpha$) and doping conditions ($/\alpha$) would keep the vertical electric field across the gate dielectric invariant. Circuit speed would be improved by a factor of α and circuit density increased by α^2 . In practice, the supply voltage could not be scaled as much as linear dimensions [2], leading to a higher electric field across the gate dielectric during operations. Moreover, higher temperature density results from increased packing density of transistors per die. A combination of high electric field and high operating temperature aggravates failure mechanisms and causes reliability concerns, in particular, to the gate dielectric. This would be briefly discussed below.

As the channel width/length of MOSFETs shrinks, the oxide thickness would have scaled down proportionally to ensure the gate's ability to control the channel. For state-of-the-art technology, the oxide thickness has been scaled down to less than 20 Å, which is equivalent to a few atomic layers. For this ultra-thin gate oxide, quantum tunnelling occurs readily and the leakage current increases exponentially as the oxide thickness is reduced [3]. The side effect of higher leakage current would be excessive power consumption and time dependent (gate) dielectric breakdown (TDDB). To overcome leakage current related reliability issues, nitrided SiO₂ gate dielectric or high- κ gate dielectric materials are currently employed in the fabrication of MOSFETs. These materials increase the physical gate oxide thickness to sufficiently block leakage current, yet exhibit a small equivalent oxide thickness (EOT) for desirable gate control.

In addition to increased leakage current, another reliability concern with gate oxide scaling is higher boron penetration. It is common for today's CMOS fabrication process to create a p-type poly-silicon gate electrode with boron doping, replacing the n-type gate electrode. The p+ polysilicon gate results in a surface-channel p-MOSFET instead of a buried channel transistor using an n-type gate. This change is necessary so as to benefit from reduced short-channel effect and better turn-off properties [4]. However, thinner oxide gate dielectric resulted in higher boron penetration from the polysilicon gate through the gate oxide, increasing the threshold voltage of the p-MOSFET [5]. While adding nitrogen provided a solution to the boron penetration problem as well [6], the presence of nitrogen worsened the oxide quality when the device is operating at high electric fields and temperature, resulting in what is now known as Negative-Bias Temperature Instability.

1.3 Overview of Negative-Bias Temperature Instability

Negative-Bias Temperature Instability (NBTI) occurs when high gate voltage is applied to operate a p-MOSFET, under high temperature. This causes positive charges build up within the gate oxide, increasing the threshold voltage of the device. In turn, this lowers other electrical parameters such as drive current and transconductance, unfavourably affecting device and overall circuit performances and reliability, as schematically shown in Figures 1.1a and 1.1b. While NBTI studies have begun as early as 1966 [7], it was only in recent years that studies have become more intense. This increased attention was primarily driven by 1) the switch from buried channel to surface channel

structure for better device scalability, resulting in channel holes, the key reactant in inducing NBTI, being brought nearer to the Si/SiO₂ interface than before. 2) The higher oxide electric field as oxide thickness are reduced. The combination of these factors inevitably enhanced NBTI occurrence and severity in today's p-MOSFETs, and will have further impact on device reliability as scaling continues down to the 22nm node.

Figure 1.1(a) Schematic diagram of *p-type* MOSFET under NBTI stressing. + denotes positive trapped charge built up in the gate oxide near the Si-SiO₂ interface. (b) Increase in the threshold voltage magnitude V_T over the NBTI stress duration

While much work has been generated from recent NBTI studies, the exact mechanism is still not well understood. Most studies have shown a power-law time dependence for the threshold voltage degradation ($\Delta V_t \sim t^n$). The Reaction-Diffusion (R-D) model is widely used to explain NBTI generation [8-10]. In this model, hydrogen is released during the reaction phase, and subsequently diffuses from the interface into the oxide with time dependence t^n , in the generation of interface traps that are responsible for V_t degradation during NBTI. The R-D model relates the time exponent n to the diffusing species, which is the reaction rate-limiting process during NBTI degradation. Experimentally obtained values of n were then applied to the

model to deduce the diffusing species. The identification of the actual hydrogen nature had evolved over time. Initial studies showed that this value n was $\sim 1/4$, corresponding to neutral H atoms being the diffusion species [11]. Later works showed that the commonly used DC stress-measure-stress measurement method in was unable to fully characterise the entire NBTI degradation, particularly because the presence of recovery effects during the measurement process [12-13]. This raises questions that could not be sufficiently answered by the initial R-D model. Subsequent works using fast-measurement methods obtained a wide range of value for n , from approximately 0.05 to 0.167 [14-15]. Given this wide distribution of values for n , determining it accurately from experiment is paramount for building onto the existing understandings from the R-D model.

Yet, the hypothesis of stress-induced interface states was found to be insufficient in explaining trap generation mechanism in NBTI. Huard *et al.* [16-17] suggested that the presence of nitrogen atoms acted as hole traps were also responsible for the threshold voltage degradation. Moreover, the application of positive gate bias was found to have enhanced partial recovery [18], suggesting the presence of charges has contributed to NBTI. This recovery effect with positive bias was not well-understood in the R-D model, since neutral diffusing species have been assumed.

1.4 Motivation and Scope of the Project

The use of p-MOSFETs in today's electronic circuits has become more prevalent than before. Device scaling has been IC designers and foundry's

preferred approach in maximising circuit performances, so that more transistors may be packed within a die. As such, the study of NBTI to better understand its mechanisms and finding innovative ways to overcome it has become more paramount. Nonetheless, factors relating to NBTI are diverse, ranging from the impact of wafer processing have on the gate oxide quality to trap recovery mechanism. This project would focus on the characterization of the difficult constituents of traps generated.

Firstly, this project would ascertain the true value of the time exponent for the interface traps generated during NBTI. The reported presence of hole traps residing near the Si conduction band, which could only be discharged with positive gate bias [19], indicated that currently known values of the time exponent were the resultant of both interface states and hole traps. Determining the time exponent value accurately would allow the actual diffusing species, responsible for interface traps generation, to be identified. In addition, the nature of the interface states residing in different regions of the Si energy band diagram would be studied.

Secondly, this project attempts to identify the nature of oxide traps that might be generated within the gate oxide, at some distance away from Si/SiO₂ interface. The widely used charge pumping method [20] is only suitable for interface traps due to the high pulsing frequency used. On the other hand, flicker noise ($1/f$) measurements have been used to characterize oxide traps in MOS devices since 1968 [21], and the $1/f$ noise theories relating to MOSFETs were better understood. Based on the existing understandings of oxide traps from noise theories, pre/post NBTI noise measurements would be extracted to deduce the change in such oxide traps.

1.5 Major Contributions of this Thesis

In this work, the traps generated during NBTI were characterized in p-MOSFETs made from different gate oxide materials. Firstly, it was shown that the presence of deep-level hole traps significantly lowered the measured time exponent value in measured MOSFETs, ranging from 0.3 to 0.5. These large values were attributed to stress-induced interface states residing on the upper half of the Si bandgap, which could not be isolated via the commonly used charge-pumping method. This result has significant implication that the reported n values of 0.14-0.17, used to support molecular H_2 as the main diffusion species in the R-D model, may not be entirely accurate.

Secondly, the nature of interface traps above the Si mid-gap was investigated. Since NBTI measurements of p-MOSFETs covered the lower half of the Si mid-gap, n-MOSFETs, made from the same wafer processing steps as the p-MOSFETs, were subjected to comparable NBTI stress. It was found that, contrary to existing understanding of interface states at the upper half of the bandgap being acceptor-like (accepts electrons to become negatively charged), such interface states were found to have exhibited a bipolar nature, exhibiting both donor-like and acceptor-like properties. By comparing with other works [22-23], these stressed induced interface states demonstrated similar properties as E' centres, in which the two trivalent Si atoms could act as both hole traps and electron traps concurrently.

Thirdly, an in-house flicker noise measurement setup was developed to overcome disadvantages associated with existing setups. This $1/f$ noise

measurement setup was verified to follow closely to existing results and noise measurements related to NBTI were conducted. By comparing the values of the slope of the flicker noise spectrum before and after NBTI stress, it was found that oxide trap distribution had increased at some distance away from the Si/SiO₂ interface on thick gate p-MOSFETs. On the other hand, no conclusive result was found, contrary to what was reported [24]. It was suspected that this difference was due to flicker noise being better suited for characterizing thick gate devices than thinner gate ones.

1.6 Organization of this Thesis

There are seven chapters in this thesis and are organised as follows:

Chapter 1 introduces the background information of MOSFET devices and how device scaling worsens NBTI, as well as providing the motivation and scope of this research project.

Chapter 2 presents the literature review on NBTI mechanisms proposed thus far. The interface traps and hole traps generation mechanisms were discussed, as well as recent findings on how shortcomings of the charge pumping could be overcome. A background of the existing flicker noise theories was discussed as well.

Chapter 3 describes the equipment setup used to characterize NBTI, namely the stress-measure-stress method, and the use of charge pumping and subthreshold current to characterize interface traps density. In addition, the in-house $1/f$ noise measurement setup was discussed and the calculations used to extract noise data.

The results on how deep-level hole traps affect the time exponent value was presented in Chapter 4. Experiments were ran with different devices that were known to have different degrees of hole traps generated, and the new time exponent values were attributed to the interface states generated above the Si mid-gap.

Further investigations on these interface states were carried out and shown in Chapter 5. Existing theory on interface states stated that these traps at the upper half of the Si bandgap are acceptor-like, and NBTI experiments were carried out on n-MOSFETs to verify this.

In Chapter 6, measurements obtained from the in-house flicker noise setup were verified with known values. It was then used to determine how oxide traps further from the Si/SiO₂ interface vary before and after NBTI stress.

Chapter 7 provides the highlights of key results and recommends what may be explored for future works.

Chapter 2: LITERATURE REVIEW

2.1 Introduction

Before reviewing some of the NBTI degradation models, it is helpful to go through some basic MOSFET concepts such as threshold voltage, interface trapped charge and fixed oxide charge. The p-channel MOSFET threshold voltage (V_t) is given by

$$V_t = V_{FB} - 2\phi_f - |Q_B|/C_{ox} \quad (2.1)$$

where ϕ_f is the difference between the Fermi potential and the intrinsic Fermi level given as $(kT/q)\ln(N_D/n_i)$, $|Q_B|$ is the Si bulk charge density expressed as $(4qK_s\epsilon_0\phi_f N_D)^{1/2}$ and C_{ox} is the oxide capacitance per unit area. The flatband voltage V_{FB} is given by

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} \quad (2.2)$$

where Q_f is fixed oxide trap charge density and Q_{it} is interface trap charge density.

The only parameters that could affect the threshold voltage would be the interface trap density and fixed oxide trap density. The former in (2.2) is dependent on the surface potential ϕ_s because the occupancy of the interface trap is surface potential dependent. Positive increase in either of these trapped charge densities leads to a negative shift in the threshold voltage. Since negative V_t shift is observed after NBTI stress, either of both charge densities increased during NBTI. The following sections would describe the nature of these trap types in detail.

2.2 Interface Traps

Interface traps generated under NBTI stress are widely believed to be one of the dominant charges contributing to threshold voltage shift. In the silicon substrate below the SiO₂-Si interface, Si is tetrahedrally bonded with each Si atom bonded to 4 Si atoms in the wafer bulk. When the Si is oxidized, dangling bonds are formed at the SiO₂-Si interface due to lattice mismatch. The bonding configuration at the surface is shown in Figure 2.1, with most of the Si atoms bonded to oxygen at the surface. Some of the remaining Si atoms are bonded to hydrogen. An interface trapped charge, often called interface trap, is an interface trivalent Si atom with an unsaturated (unpaired) valence electron at the SiO₂-Si interface. It is usually denoted as

$$Si_3 \equiv Si \bullet$$

The $\equiv$ represents three complete bonds to other Si atoms and the $\bullet$ represents the forth, unpaired electron in a dangling orbital (dangling bond). Interface traps are also known as P_b centres [1]. The density of interface traps is designated as N_{it} (cm⁻²). The dangling bonds could be neutralized easily by forming Si-H bonds under low temperature annealing in a forming gas (N₂/H₂). These Si-H bonds could also break easily under NBTI stress and form interface trapped charges, or interface traps.

On (100) Si, the four tetrahedral Si-Si directions intersect the interface plane at the same angle. Two defects, named P_{b1} and P_{b0} , have been detected via electron spin resonance (ESR), as shown in Figure. 2.1. The P_{b1} centre was

originally thought to be a Si atom backbonded to two substrate Si atoms, with the third saturated bond attached to an oxygen atom, designated as $Si_2O \equiv Si \bullet$. This was later found to be inaccurate, as the calculated energy levels for this defect do not agree with experimental data [25]. Recent calculation suggests the P_{b1} centre to be an asymmetrically oxidized dimer, with no first neighbour oxygen atoms [26]. It was unambiguously established that both P_{b0} and P_{b1} are chemically identical to the P_b centre [27]. While P_{b0} centres are due strain relaxation taking place with a defect residing at (111) microfacets at the Si/SiO₂ interface, P_{b1} centres are formed when strain relief occurs with a defect at (100) Si/ SiO₂ interface regions. As P_{b0} centres are believed to be electrically active [27], such defects are considered to be directly responsible for interface traps creation in (100) silicon. It should also be noted that while recent ESR measurements show that P_{b1} centres to be electrically active with 2 definite narrow peaks near the midgap of the Si bandgap, these P_{b1} centres are often created at much lower densities relative to P_{b0} centres, hence diminishing their relative importance.

Figure 2.1 Defect P_{b0} and P_{b1} in (100) silicon [5]

Interface traps at the SiO_2/Si interface are acceptor-like in the upper half and donor-like in the lower half of the bandgap [6]. As shown in Figure. 2.2a, at flatband, the states in the lower half of the bandgap are neutral when electrons occupy states below the Fermi level (occupied donors are denoted as “0”). Those between mid-gap and the Fermi energy are negatively charged (occupied acceptors are marked as “-“), and those above the Fermi level (E_F) are unoccupied acceptors, hence neutral. For a p-MOSFET biased in inversion, as shown in Figure 2.2b, the interface traps residing between mid-gap and the Fermi level are now unoccupied donors, resulting in a positive interface trapped charge (marked by “+”). Therefore, during inversion, interface traps in p-channel devices are positively charged, leading to a negative threshold voltage shift, and applying more negative bias till stress level generates donor states in the lower half of the band gap [28].

The generation of additional interface states has been attributed to as the main mechanism for NBTI degradation. The Reaction-Diffusion (R-D) model is to-date the most prevalent [10, 29] model in relating the generation of interface states and threshold voltage degradation in the presence of high temperature and electric field. Since the year 2003, results from fast measurement methods have challenged the R-D model. Reconciliations are being made to allow the model to explain what has been observed. In the next sections below, the evolution of the R-D model before and after the year 2003, and the relevance of these changes will be discussed.

Figure 2.2(a) Energy band diagram of Si substrate for p-MOSFET illustrating interface states occupancy and charge polarities at flatband. Each horizontal line on the axis represents an interface trap, which is either occupied by a hole (unoccupied by an electron) an electron (solid circle) [30].

Figure 2.2(b) Energy band diagram of Si substrate for p-MOSFET illustrating interface states occupancy and charge polarities at inversion [30].

2.2.1 The Reaction-Diffusion Model of NBTI Degradation, Pre 2003

works

In the Reaction-Diffusion (R-D) model for NBTI [8, 31], the occurrence of threshold voltage degradation is assumed to be due to holes in the inversion layer interacting with Si-H bonds at the Si/SiO₂ interface. The resultant hole capture weakens Si-H bonds and at higher temperature, leads to the release of hydrogen during the reaction phase, and the generation of interface traps. The rate of trap generation is given by,

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_H(0) N_{IT} \quad (2.3)$$

where N_{IT} is the fraction of Si-H bonds broken at time t due to NBTI stress. N_0 is the initial number of Si-H bonds at the Si/SiO₂ interface. The dissociation rate constant k_F is proportional to the number of inversion layer holes trapped by the Si-H bonds. The two-electron Si-H covalent bond is weakened when a hole is captured and this bond (aided by the electric field) is easily broken at a relatively moderate temperature. The dissociated Si bond acts as a donor trap [32] and contributes to the threshold voltage shift and transconductance reduction. The R-D model assumes that N_{IT} generation is the primary cause of NBTI. Experiments conducted by various groups [31, 33] showed evidences that the formation of the interface state takes place at a much faster rate compared to the diffusion of the mobile hydrogen species, hence the R-D model exhibits the characteristic of a diffusion-limited system, i.e. the formation of the interface trap is dominated by the rate of out-diffusion of the diffusing species from the interface.

Early R-D model deduced that the H atoms released in the process would diffuse away from the interface, i.e.

$$\frac{dN_{IT}}{dt} = D_H \frac{d^2 N_H}{dx^2} + N_H \mu_H E_{ox} + \frac{\delta}{2} \frac{dN_H(0)}{dt} \quad (2.4)$$

The last term in (2.4) is negligible as the hydrogen diffusion is small at the initial fast reaction-dominated phase. The H atoms may diffuse with diffusion constant (D_H) if the atoms are neutral, or drift with mobility μ_H if they are charged. Since the rate of trap generation in (2.3) is usually small compared to

the dissociation and annealing rates and since $N_{IT} \ll N_0 \sim 5 \times 10^{12} \text{cm}^{-2}$, therefore

$$\left(\frac{k_F N_0}{k_R} \right) \approx N_H(0) N_{IT} \quad (2.5)$$

Also, (2.4) may be rewritten as a conservation equation which specifies that the number of broken Si-H bonds equal that of total H concentration in the gate dielectric, i.e.,

$$N_{IT}(t) = \int_{x=0}^{x(t)=f(D_H, \mu_H, t)} N_H(x, t) dx \quad (2.6)$$

In (2.5), $x = 0$ is the boundary condition for the Si/SiO₂ interface and $x(t)$ denotes the tip of the diffusion front. Consider the diffusion of neutral atomic H as shown in the centre diagram of Figure 2.3. The diffusion distance at a given time t is $x(t) \sim (D_H t)^{1/2}$, therefore the right hand side of (2.6) can be interpreted as the area under the triangle (sometimes referred to as ‘Triangle Method’) so that

$$N_{IT}(t) = \int_{x=0}^{\sqrt{D_H t}} N_H(x, t) dx = \frac{1}{2} N_H(0) \sqrt{D_H t} \quad (2.7)$$

Figure 2.3 Illustration of hole-assisted dissociation of Si-H bond at the Si/SiO₂ interface. The H may diffuse (middle) or drift (bottom) away from the interface depending on the charge state of the diffusing species.

Inserting this expression for N_{IT} into (2.3), we find

$$N_{IT}(t) = \sqrt{\frac{k_F N_0}{2k_R}} (D_H t)^{1/4} \quad (2.8)$$

The above derivation leads to the time exponent in the classical R-D model of $n=1/4$, which had been a key characteristic of NBTI degradation based on a diverse range of experimental results. The success of the R-D model in interpreting the NBTI exponent has led to a common understanding at that time that NBTI degradation is characterized by diffusion of atomic H in gate dielectrics.

On the other hand, the possibilities of other hydrogen-related species present during NBTI were hypothesized as well, although not supported by the empirical evidences. Consider the case if the released hydrogen species are protons, we must retain the drift term in (2.4), given the influence of the

vertical electric field across the gate oxide on charged species, then rewrite the conservation (2.6) (in analogy to the Triangle Method) as

$$N_{IT}(t) = \int_{x=0}^{x(t)=f(D_H, \mu_H, t)} N_H(x, t) dx = N_H(0) \mu_H E_{ox} t \quad (2.9)$$

Here, $\mu_H E_{ox}$ is the velocity with which the H⁺ drift-front moves away from the interface as shown in Figure 2.3 top diagram. Together with Equation 2.3, we find [8]

$$N_{IT}(t) = \sqrt{\frac{k_f N_0}{2k_R}} (\mu_H E_{ox})^{1/2} \quad (2.10)$$

Due to the additional drift term the H⁺ system shows a theoretical time exponent n of 1/2. However, this n=1/2 regime has never been seen in NBTI results, leading to the deduction that NBTI degradation through proton transport is unlikely. However, it should be noted that later works [34-35] have suggested that the involvement of protons was possible under the dispersive transport framework.

Experimental observations have shown that upon the removal of stress, some of the threshold voltage degradation could be recovered. This NBTI recovery effect could be explained by the back-diffusion of hydrogen species from the gate electrode to the SiO₂/Si interface, through the bulk gate oxide, and the Si dangling bonds are repassivated by the hydrogen species [36].

2.2.2 The Reaction-Diffusion Model of NBTI Degradation, Post 2003

Works

In 2003, a few authors reported that after DC voltage NBTI stress was removed, a significant recovery effect was observed [13, 37]. They inferred that NBTI degradation consists of 2 components – a permanent component responsible for permanent threshold voltage shift, and another that could be recoverable upon the removal of the stress voltage. The inability to characterize NBTI degradation fully was due to the measurement delay inherent to the DC stress-measure-stress measurement method, particularly due to the longer time needed to determine threshold voltage from I_d - V_g sweep (see Figure 3.2). As a result, the often quoted time exponent value of 0.25 was actually a resultant value coming from more than one trap generation component. The R-D model would need to be refined to justify this observation.

It was also discovered that interface trap generation (ΔN_{it}) during NBTI is not the only component responsible for the entire threshold voltage shift [16, 38]. Using the charge-pumping (CP) method to measure ΔN_{it} , Huard *et al.* [17] found that threshold voltage shift due to interface state generation measured by the CP method was only a fraction of the total V_t degradation during NBTI stress. The authors attributed this to hole trapping, resulting in additional charge build-up within the oxide, hence increasing the p-MOSFET threshold voltage negatively. In addition, experimental results from these work showed that the application of a positive bias enhanced the recovery of the degraded threshold voltage, which strongly suggested the presence of charges responsible for the recovery process. The inability of the DC stress-measure-

stress method to capture all the V_t degradation due to inherent time delay, together with NBTI V_t degradation not limited to interface trap generation, put doubt into the accuracy of 0.25 as the true time exponent value, and corresponding prediction by the R-D model that atomic H is the main diffusing specie driving interface state generation during NBTI stress.

The limitation with the DC measurement method has resulted in the development of pulsed I_d - V_g method, to extract V_t with minimum delay time between the removal of stress to the completion of measurement. Such fast measurement methods, with delay time from milliseconds [39] to microseconds [12], reported time exponent values from 0.18 to 0.1, which are noticeably smaller than the value 0.25 obtained from previous experiments. However, the exact value responsible for interface trap generation during NBTI stress, which hopefully could be used to reconcile with the R-D model, remained unknown.

To reconcile this wide range of exponent values observed by various studies, Lee [40] assumed that the threshold voltage shift contributed by hole trapping saturates rapidly in the initial stress duration, based on the hole trapping/detrapping model [41-42]. Hole traps were characterized as those that could only be captured by fast measurement methods, as they recover upon the removal of the stress gate bias. The interface trap density generated over the stress duration would be obtained by subtracting the constant V_t shift due to hole trapping from the total threshold voltage degradation measured. This separation method allowed the authors to correct the effects due to recovery and time delay in the different measurement systems. In addition, this method showed how time exponent value varied over the stress duration (Figure 2.4) – from $n=1$ within the first 10ms, to $n=1/3$ during the intermediate stress to $n=1/6$,

over longer term NBTI stress time. Lee *et al.* suggested that atomic H is released from the interface and is being converted to molecular H₂ when $n=1/3$ and molecular H₂ becomes the main diffusing specie when $n=1/6$ (~0.167), after a longer time into the NBTI reaction.

Figure 2.4 Evolution of the time exponent n over 3 stages during NBTI stress [40]. Dashed line represents ΔV_h , circle symbols denote ΔV_{it} , and square symbols denote $\Delta V_h + \Delta V_{it}$ at each instance in time measured.

Chakravarthi *et al.* utilized quantitative numerical simulations to deduce the underlying physics leading to NBTI degradations [31]. Probable hydrogen species (atomic H, molecular H₂, and proton H⁺) were computed into the numerical models. In the case of the molecular H₂, the results showed that the time exponent for molecular H₂ was ~0.165. This was in good agreement with the n derived from experimental data by Lee *et al.* Hence, Lee's work reconciled pre-2003 findings relating to atomic H, with results from post-2003 works on fast measurements and hole trapping, arriving to the current exponent

value n of 0.16. Subsequent works [43-44] have since supported this explanation in reconciliation with the R-D model.

While the use of fast measurement methods have allowed the hole traps component generated during NBTI to be characterized, as well as indirectly aiding to reconcile observed time exponent values with the R-D model, there are unresolved issues that could not complete the existing understanding of NBTI. Firstly, the nature of hole traps remained unclear. Studies by Ang *et al.* [19, 45] have consistently shown that there is a variant of hole traps (deep-level hole traps) that are continuously generated during the stress duration, contradictory to what Lee's work have suggested that hole traps should saturate within the first second of the stress duration. Secondly, the presence of positive gate bias enhanced NBTI recovery process, and could not be explained by the back-diffusion of hydrogen, as the presence of positive bias suggests charge presence / some form of charge removal in recovery, hence lowering the threshold voltage [9]. This is observed in conventional DC measurement setup, with which the dominant degradation mechanism would be interface trap generation, when applying positive gate bias increased V_t recovery. In this case, back-diffusion would not have increased with neutral molecular H_2 . The presence of a previously undetected NBTI induced component would have an implication that the time exponent of $1/6$ currently obtained may be contaminated as well. If so, it could not be concluded with certainty that molecular H_2 is the main diffusing species, as predicted by the R-D model. In the next section, observations about this new "deep-level hole traps", and how it provides a starting platform for this thesis, would be discussed in detailed.

2.3 Role of Oxide Traps and Hole Trapping

Huard *et al.* [17] provided experimental results showing that, in addition to interface traps generation during NBTI stress, hole trapping in the oxide has great influence on threshold voltage (V_t) degradation as well. This second component was believed to be due to either holes trapped onto oxide defects (such as nitrogen induced defects), traps pre-existent to NBTI stress (V_t degradation contributed by traps with lower activation energy than required in N_{it} generation), or slow states close to the interface [46]. It has also been suggested that hole traps may be generated by anode hot-hole injection mechanism during NBTI stress [38]. However, this remained controversial to this day. Another characteristic of hole trapping was that it had minimal temperature dependence, as mentioned in [47].

Ang *et al.* first re-examined [19] the method used to determine the contributions of oxide traps generation (ΔN_{ot}) and interface trap generation to the total stress-induced V_t shift. This was done by separately quantifying ΔN_{it} using the charge pumping (CP) method, and then comparing the experimental $\Delta V_t - \Delta N_{it}^{CP}$ curve to the theoretical $\Delta V_t - \Delta N_{it}^T$ curve, as shown in Figure 2.5(a). The interface trap density measured by the CP method, ΔN_{it}^{CP} , is determined from the change in measured charge pumping current ΔI_{cp} , the transistor's gate area (A) and pulse frequency (f), and is given by

$$\Delta N_{it}^{CP} = \Delta I_{cp} / qAf \quad (2.11)$$

The theoretical $\Delta V_t - \Delta N_{it}^T$ curve may be independently obtained if the oxide capacitance C_{ox} is known. C_{ox} may be determined from C-V simulators, taking into account quantum confinement and polysilicon depletion effect. From first order, ΔN_{ot} could then be obtained by subtracting $|\Delta V_{it}|$ from $|\Delta V_t|$. Unfortunately, this direct approach was made on two assumptions that were inaccurate: 1) Not all stress-induced interface traps are measured since the charge pumping method only probes a fraction of the silicon bandgap, implying that interface states generated at energy range above the CP measured window might not be captured. 2) The pulsing of the gate voltage could induce significant relaxation of interface states during CP measurement. As a result, the actual ΔN_{it}^{CP} measured would actually be underestimating the actual amount of interface states present, as illustrated in Figure 2.5(b). Moreover, before using the $\Delta V_t - \Delta N_{it}^{CP}$ plots to make meaningful comparisons about the stressed induced $|\Delta V_{it}|$ and $|\Delta V_{ot}|$, the limitations of the CP method need to be factored in as well.

Figure 2.5 (a) The difference in the threshold voltage shift between the CP measured ΔN_{it}^{CP} and the theoretical ΔN_{it}^T is expected to give V_t shift contributed by stress-induced oxide traps. (b) Possible under-estimation of the total stress-induced interface trap density, due to the limitations of the charge pumping method [19].

To resolve this possible limitation of CP measurement method, Ang *et al.* proposed the use of the subthreshold current to quantify interface states that are in the energy range comparable to that probed by the charge pumping method, ΔE_{CP} . This effective energy range, ΔE_{CP} , over which interface states contribute to the recombination current, is constrained by thermal emission of electrons to (from) the conduction (valence) band edge during gate pulse transition. From the results shown in [48], ΔE_{CP} may be expressed as

$$\Delta E_{cp} = -2kT \ln \left[n_i \cdot v_{th} \cdot \sqrt{\sigma_n \sigma_p} \cdot \left(\frac{V_{FB}^{CP} - V_t^{CP}}{\Delta V_G} \right) \cdot t_{rf} \right] \quad (2.12)$$

where V_{FB}^{CP} (approximately 0.8V) and V_t^{CP} (approximately -0.2V) are the CP flat band and threshold voltages respectively, k is Boltzman constant, T the temperature in Kelvin, n_i the intrinsic carrier concentration, v_{th} ($\sim 10^7$ cm/s) is the thermal velocity, ΔV_G the amplitude of the gate pulse, t_{rf} (=40ns) is gate pulse transistion time and σ_n (σ_p) the electron (hole) capture cross-section. At high temperatures used during NBTI stress, temperature $T = 373K$ (100°C), and the corresponding $n_i \sim 1.4 \times 10^{12} \text{ cm}^{-3}$. Assuming $\sqrt{\sigma_n \sigma_p} \sim 10^{-14} - 10^{-15} \text{ cm}^{-2}$, ΔE_{cp} is estimated to range from 0.37-0.52eV, which corresponds to 33-45% of the Si bandgap ($E_g = 1.12 \text{ eV}$). It should be highlighted that precise determination of ΔE_{cp} is generally not possible, since σ_n and σ_p their associated temperature dependencies are unknown.

A key feature of the subthreshold swing method is that when used in ultrathin gate oxide devices, the effective energy interval probed ΔE_{ss} varies closely with the change in gate voltage when measured within the subthreshold regime (weak inversion region), i.e. $\Delta E_{ss} \sim \Delta V_g$. This is because in the subthreshold region, when the voltage drop across the dielectric is small, the Si surface band bending ψ_s at a given V_g may be expressed as:

$$V_g - V_{FB} = \psi_s - \frac{\sqrt{2K_s \epsilon_0 q N_D \psi_s}}{C_{ox}} + V_{poly} \quad (2.13)$$

where K_s (=11.8) the relative permittivity of Si, ϵ_0 the permittivity of free space, N_D the doping concentration of the n-Si substrate, V_{poly} (~ 0 at the subthreshold region) is the polysilicon depletion voltage, and V_{FB} is the flatband voltage. V_{FB} may be taken to be independent of ψ_s in an unstressed device with low interface state density. The second term on the right hand side of (2.13) denotes the voltage drop across the gate oxide layer V_{ox} . For an ultrathin gate oxide (EOT = 1.6nm), $C_{ox} \sim 2.2 \times 10^{-6}$ F/cm². For N_D on the order of 10^{17} cm⁻³, $V_{ox} \sim 60$ mV at $\psi_s = 0.6$ V. From this first order analysis, it could be shown that a change in Si surface band bending $\Delta\psi_s$ closely follows the change in gate voltage ΔV_g in an ultrathin gate device (i.e. $\Delta\psi_s \sim \Delta V_g$) biased in weak inversion, since the voltage drop across the ultrathin gate dielectric is small. Therefore, by obtaining the subthreshold swing over a given ΔV_g range, it could be determined that ~ 0.33 - 0.34 eV of the Si bandgap is probed. This energy range closely resembles to the range probed using the charge pumping method as well. This implies that the ΔN_{it} obtained from the subthreshold swing method could be compared with measurements obtained from the CP method. Figure 2.6 shows the depletion region used to extract subthreshold

swing values (opened circles) and the corresponding energy range of the Si bandgap probed using the subthreshold swing method (see inset).

Figure 2.6 Use of subthreshold swing method in determining the threshold voltage degradation. Inset shows an energy band diagram of the p+ gate/SiON/ n-substrate Si structure in the regime where subthreshold swing method is probed, with the shaded energy interval (approximately 0.33eV)

After stress, an increased in oxide trapped charge and interface state density shift and distort the I_d - V_g curve. The increase in positive charges from stress induced interface states result in an increase of the subthreshold swing, and the resultant increase may be expressed as

$$\Delta S = \ln 10 \cdot \frac{kT}{q} \cdot \left(\frac{\Delta C_{it}}{C_{ox}} \right), \quad \Delta C_{it} = q \Delta \overline{D_{it}} \quad (2.14)$$

where ΔC_{it} is the average interface trap capacitance per unit area, and $\Delta \overline{D_{it}}$ is the average increase in the interface state density. During NBTI stress, the build up of interface states and oxide trapped charges could change V_{FB} . If the same $|\Delta V_g|=0.4V$ is used for both before and after stress measurements, the

referred ΔE_{ss} range in post stress would be different from the pre-stress energy window. By fixing the upper and lower limits of the drain current, the measured energy window by this method would not be affected by the change in the flatband voltage. Experimental results comparing the interface trap density measured from the charge pumping method and the subthreshold swing method showed that both results were of close resemblance, even though the latter was measured without the application of a positive gate bias (and hence additional recovery). While there has been a claim that charge pumping measurements are subjected to additional recovery of interface traps [18], comparable values obtained from CP measurement and subthreshold swing method put this claim in doubt. In addition to the lack of significant recovery effect during charge pumping, the results from the subthreshold swing add weight to the argument that interface traps are generated, during NBTI, over a wide energy range within the silicon bandgap, which is outside the energy range scanned by charge pumping or the subthreshold swing method. The larger than expected ratio of the effective positive trap density to interface trap density, if the traps were assumed to be of a uniform distribution, strongly suggests a high density of stress-induced traps, comprising both interface and hole traps, above the conduction band.

Ang *et al.* [19] proceeded to investigate whether a positive gate bias would increase the passivation of interface states. Classical R-D model expected partial recovery of the degraded threshold voltage to originate from the back-diffusion of the hydrogen atoms to the interface states [31, 49], on the removal of the stress voltage. However, some works had observed that changing the gate bias to a positive polarity and increasing its magnitude

reduce the overall threshold voltage degradation, compared to the case when the stress voltage was removed without further application of gate bias. This contradicts the explanation given by the R-D model, as the effect of an electric field on recovery suggests the involvement of positive trapped charge (or hole traps). Ang *et al.* did a detailed investigation of the effect of applying a positive gate bias on interface state recovery.

To investigate the possibility of interface state re-passivation by a positive gate voltage, a static NBTI stress was performed to induce interface trap generation, followed by charge pumping measurement to characterize the interface trap density. The results were compared against a bipolar NBTI stress followed by charge pumping. Bipolar stress involves applying a positive gate bias after each preceding cycle of negative bias at stress level. It aims to anneal hole traps generated, leaving behind interface states to be measured. If any of the interface states probed by charge pumping would recover in the presence of positive bias, it would show up in the ΔN_{it}^{CP} bipolar readings, when compared to ΔN_{it}^{CP} static results. However, results from both the charge pumping and subthreshold swing methods were found to yield comparable stress-induced interface trap density values. Hence, it could be concluded that there is no significant interface state relaxation under positive gate biasing. This implies that the traps recovered from NBTI recovery are most likely to come from hole traps.

In addition, recovery data shows distinct rate of recovery – one with a rapid and substantial decrease in the V_t degradation as gate voltage is biased from negative to positive; the other with a slower rate of decrease, i.e. the recovery of deep-level hole traps takes place at a much faster rate than the

interface states, in the presence of a positive gate bias. This difference shows that hydrogen interaction dynamics in the R-D model could not sufficiently explain NBTI phenomenon. One possible mechanism for hole traps could involve the loss of electronic charge from nitrogen donors to the Si conduction band or holes at the Si valance band edge, in the presence of negative-field, suggested in Chaiyasena *et al* [50]. This was observed by the distinct electron spin resonance (ESR) measured in nitrogen trap centres in nitrided oxide.

2.4 Summary of NBTI Literature

The literature review thus far has provided coverage on the NBTI trap generation mechanisms, showing how the use of the time exponent in the initial R-D model could correlate experimental results of $n = 0.25$. Subsequent use of fast measurement techniques and the inclusion of hole traps into NBTI generation led to reconciliations of the new $n = 0.16$ results into the R-D model. However, such reconciliations did not account for hole traps that cause partial V_t recovery when positive gate bias is applied. The presence of such hole traps in deep-level energy states (deep-level hole traps, DLHTs) could corrupt the true value of the time exponent, as they could be picked up during the conventional DC measurements. As such, the exponent value of 0.16 may not represent the true interface states generation mechanism. Therefore, this project aims to investigate quantitatively how DLHTs influence the true value of n for the stress-induced interface states. These NBTI-generated interface states include those measurable by the charge pumping method and those that reside at the upper half of the Si bandgap.

While interface trap generation due to the breaking of Si-H bonds were considered, the breaking of Si-O bonds during NBTI is likely to occur as well [8], though few studies gave consideration to such traps located some distance away from the interface. On the other hand, oxide traps located within the SiO₂ dielectric of MOS devices have been studied via flicker (1/f) noise measurements since 1957 [51]. 1/f noise was found to cause drain current fluctuations was due to the presence of oxide traps in the silicon dioxide dielectric, by affecting the number of inversion charges in the channel as well as mobility of these channel charges. Experimental results have shown that flicker noise could be used as a tool to probe oxide traps located near the conduction band edge of the silicon bandgap, as well as measuring oxide trap distribution in the Si dielectric [52]. Hence, this work would investigate in detail the impact of NBTI degradation on changes in flicker noise, and hopefully, further understand the changes in trap distribution during NBTI.

2.5 Flicker Noise and NBTI

2.5.1 Introduction

As described in the earlier section, the threshold voltage shift in NBTI is due to trap generation in the gate oxide. However, the actual nature or occurrence of such traps has yet to be well understood. It is believed that these traps might be tunnelled into and out of by the inversion charges (holes in p-MOSFETs), resulting in low frequency noise detected in DC current [52]. Specifically, it has been known since 1957 that the fluctuating response of the DC drain current, flicker noise (also known as $1/f$ noise), is the result of interactions between charge carriers in the MOSFET channel and oxide traps from the SiO_2 dielectric [51, 53-54].

The electrical current in a solid-state device is proportional to the charge carriers density (or numbers) N multiplied by the mobility of the carriers μ . While this relationship suggested that $N \times \mu$ should be considered together in identifying the main $1/f$ noise source, two schools of thought have tried to explain flicker noise separately, until as late as 1990. In the following sections, existing theories of flicker noise in MOSFET transistors would be examined, followed by a discussion on how flicker noise measurements could help identify trap distribution during NBTI.

2.5.2 Numbers fluctuations ΔN Model

The numbers fluctuation model (ΔN), or the McWhorter model, first hypothesized that the fluctuations observed in the drain current is the result of tunneling of channel charges at the semiconductor surface to traps located in the oxide near the dielectric-Si interface [55], as indicated in Figure 2.7. The resulting number fluctuation power spectral density is given by

$$S_N(f) = 4 \int_0^{x_i} dx N_{ot}(E) f_T (1 - f_T) \times \Delta E \Delta y \Delta z \frac{\tau_t}{1 + (2\pi f \tau_t)^2}, \quad (2.15)$$

in which it is assumed that the have a uniform distribution across energy level E and with a tunneling time constant τ_t , which varies with distance x from the interface, according to the following expression:

$$\tau_t = t_0 \exp(\alpha_t x) \quad (2.16)$$

The tunneling parameter is of the order of 10^8 cm^{-1} and the attempt time t_0 is approximately 10^{-10} s for the Si-SiO_2 interface. The oxide trap density $N_{ot}(E_F)$ is parallel to the plane of the interface. (2.15) is thus the summation of the contribution of a large number of independent traps. Each trap generates a Lorentzian Generation-Recombination (GR) spectrum given by

$$S_{GR}(f) = A_{GR} \frac{\tau_t}{1 + (2\pi f \tau_t)^2} \quad (2.17)$$

where A_{GR} is a constant amplitude pre-factor, proportional to the density of the underlying trap levels. The Fermi-Dirac function $f_T(E)$ gives the electron occupation probability of the trap with energy position E . Due to the near delta function behaviour of the product $f_T(1 - f_T)$, flicker noise comes only trap levels

within a few kT of the surface Fermi level E_F . This simplifies (2.15) into (2.19). As shown by McWhorter, the integral in (2.15) will reduce to a $1/f$ -like spectrum, for a sufficient spread in τ_t . The depth of the traps is directly related to the tunnelling time, hence traps further from the Si/SiO₂ interface are detected in the lower frequencies. Therefore, in the McWhorter model, flicker noise across measured frequency shows the distribution of tunnelling times, from the deduction of the tunnelling time (see Eq. (2.7)) with distance x in the oxide. For the frequency range of interest (≤ 10 kHz), only traps within a distance x_1 from the interface will contribute. For silicon, practical trap depths are expected to be deeper than 1.3 nm. Usually, a homogeneous oxide trap density $N_{ot}(E)$ with depth is assumed in the modelling, although depth dependent trap profiles will also lead to a $1/f^\gamma$ like spectrum, with $\gamma \approx 1$. In the case that $\gamma < 1$, more noise at higher frequency implies the presence of more ‘fast’ traps, and vice versa for $\gamma > 1$ [52]. Hence, for a profile whereby the trap density increases with the distance into the oxide, the tunnelling time will be larger, as emphasized in the low frequency transitions.

Figure 2.7 Energy band of Si substrate and oxide illustrating tunneling of channel carriers into oxide traps and released back into channel, causing flicker noise, according to McWhorter’s model. Illustration for n-MOSFET biased to inversion. The x-direction is from the Si/SiO₂ interface into the gate oxide, y-direction is along the channel length, while z-direction is along the channel width.

After deriving (2.15) based on MacWhorter's $1/f$ noise models, the equation could then be converted into a voltage (or current) noise spectral density of a MOSFET in the linear regime of device operation [21, 52, 56-57]. Assuming that the fluctuations are in the number (ΔN) or charge density in the homogeneous channel at small V_{DS} , one can express the drain current fluctuations in an elementary area $\Delta y \Delta z$ as

$$\Delta I_D = \frac{W\mu V_{DS}}{L} \frac{q\delta N \Delta y \Delta z}{WL} \quad (2.18)$$

In writing (2.18), a classical linear MOSFET model is assumed, for a device with area $W \times L$ and mobility μ . In this model, fluctuations in mobility are neglected, while δN is the fluctuation in the number of inversion charges in the elementary surface $\Delta y \Delta z$ and q is the elementary charge. The corresponding drain current noise power spectral density is then

$$S_{I_D} = \frac{I_D^2}{W^2 L^2 Q_N^2} q^2 S_N \quad (2.19)$$

such that,

$$Q_N = C_{ox} (V_{GS} - V_T) \quad (2.20)$$

C_{ox} refers to the gate oxide capacitance per cm^2 , V_{GS} the gate voltage, V_T the threshold voltage and I_D is the drain current. The resultant input (or gate) referred noise spectral density follows from (2.19)

$$S_{V_G} = S_{I_D} / G_m^2 \quad (2.21)$$

with G_m the transconductance ($=\partial I_D/\partial V_{GS}$). Combining with (2.15) and assuming that the trap density is uniform in energy and oxide depth, this results in the expression [52]

$$S_{V_G} = \frac{kTq^2}{8WLC_{ox}^2\alpha_t} \frac{N_{ot}(E_F)}{f} \text{ (in V}^2\text{/Hz)} \quad (2.22)$$

The oxide trap density term $N_{ot}(E_F)$ is based on the fact that the function $f_T(E)$ [$1 - f_T(E)$] is sharply peaked around the surface Fermi level E_F . As such, only oxide traps in an energy interval of $\pm kT$ around E_F contribute to the $1/f$ noise.

Equation (2.22) predicts that there is no direct relationship between applied gate bias and flicker noise magnitude in linear operation, for a standard MOSFET. In addition, based on (2.22), one can derive the density of interface traps, also sometimes called border traps [14, 15], from the $1/f$ noise magnitude, as demonstrated in the following publications, both for n- [52, 58-59] and p-MOSFETs [60]. However, while gate voltage independence has been observed in many occasions for longer channel n-MOSFETs [57, 60-61], this is not so for their p-type counterparts [6, 7, 17, 18]. This discrepancy can be explained using the ΔN framework, by assuming that N_{ot} (in $\text{cm}^{-3} \text{ eV}^{-1}$) shows a profile in energy or oxide depth or both [52, 60, 62-63]. In this way, a form of slow-interface-state 'spectroscopy' can be performed. Along the same line, the variation of the frequency exponent γ against gate bias can be explained by considering a non-uniform trap distribution [52, 62]. Equation (2.22) is strictly speaking only valid above threshold, i.e. for $V_{GS} > V_T$ (see (2.19)). A more generally valid expression, which is widely accepted in the ΔN framework, has been proposed by Reimbold [57] and covers the linear region from weak to

strong inversion. The resulting normalised drain current noise power spectral density is given by

$$\frac{S_{I_D}}{I_D^2} = \frac{q^4}{kT W L \alpha_t} \frac{1}{f^\gamma} \frac{N_{ot}}{(C_{ox} + C_d + C_{it} - \beta Q_n)^2} \quad (2.23)$$

with $\beta = q/kT$, C_d the depletion capacitance per unit of area, C_{it} the interface state capacitance per unit of area ($= q^2 N_{it}$, with N_{it} in $\text{cm}^{-2} \text{eV}^{-1}$) and Q_n the inversion layer charge density. For dimensional reasons, the frequency exponent in (2.23) should in fact be equal to 1. This relationship can more directly be derived from the flat-band voltage fluctuations concept, as shown by Ghibaudo *et al.* [64]. For weak inversion, corresponding to $|\beta Q_n| C_{ox} + C_d + C_{it}$, Equation (2.23) predicts a constant plateau for the normalised noise power at small I_D . A typical example is given in Figure 2.8(a) for a $20 \times 0.45 \mu\text{m}$ n-MOSFET, while the corresponding S_{V_g} is shown in Figure 2.8(b). The results in weak inversion are in full agreement with the ΔN model, which is one of the strong points in favour of the theory.

Figure 2.8(a) Normalised current noise spectral density and $(G_m/I_D)^2$ ratio versus the drain current for a $20 \times 0.45 \mu\text{m}$ n-MOSFET in linear operation, at $f=1\text{Hz}$. Parallel slopes of the 2 curves is in full agreement with the ΔN origin of $1/f$ noise (b) Input-referred noise spectral density S_{V_g} versus the gate overdrive $V_{GS}-V_T$ for a $20 \times 0.45 \mu\text{m}$ n-MOSFET in linear operation at $f=1\text{Hz}$. The constant noise level below the threshold voltage V_T is in line with the ΔN model [65]

Figure 2.9(a) Normalised current noise spectral density and $(G_m/I_D)^2$ ratio versus the drain current for a $20 \times 0.35 \mu\text{m}$ p-MOSFET in linear operation, at $f=1\text{Hz}$. Parallel slopes of the 2 curves in weak inversion is in full agreement with the ΔN origin of $1/f$ noise (b) Input-referred noise spectral density S_{V_g} versus the gate overdrive $V_{GS}-V_T$ for a $20 \times 0.35 \mu\text{m}$ p-MOSFET in linear operation at $f=1\text{Hz}$ [65].

On the other hand, $\Delta\mu$ models predict a strong increase of the noise in weak inversion [32]. Typical curves for a $20 \times 0.35 \mu\text{m}$ p-MOSFET are shown in Figure 2.9(a) and 2.9(b). Some clear differences compared to the n-

MOSFET case are reported in [65]. There is, for example, the parallelism in Figure 2.9(a) only holds true under small drain current but not in the large drain current, as opposed to Figure 2.8(a) for n-MOSFETs. This implies that the ΔN model holds true in weak inversion for p-MOSFET but not under inversion. Strong support for the ΔN model has been provided by the behaviour of RTS in submicrometer area MOSFETs [11, 12]. If one neglects for a moment the possible impact on the mobility, one can write for the relative amplitude of a drain current RTS in linear operation [66]

$$\frac{\Delta I_D}{I_D} = \frac{G_m}{I_D} \frac{q}{WLC_{ox}} \left(1 - \frac{d}{t_{ox}}\right) \quad (2.24)$$

Firstly, (2.24) suggests that the relative drain current amplitude is proportional to the relative change in the carrier number (or charge) $1/N$ ($qN = WLC_{ox}[V_{GS} - V_T]$) when one carrier disappears from the channel. Secondly, it proposes proportionality with the G_m/I_D ratio. It has been demonstrated that (2.24) is also applicable to describe the RTS amplitude in saturation (i.e. the V_{DS} dependence) [66]. In weak inversion, a constant value is predicted by (2.24), since G_m/I_D is constant for small I_D [11, 12, 21] and is equal to the subthreshold slope. This results in

$$\frac{\Delta I_D}{I_D} = \frac{1}{WL} \frac{q^2 / kT}{C_{ox} + c_d + C_{it}} \left(1 - \frac{d}{t_{ox}}\right) \quad (2.25)$$

for $V_{GS} < V_T$, which is the counterpart of (2.23) derived by Reimbold [57] for the 1/f noise in large area MOSFETs.

2.5.3 Mobility Fluctuations $\Delta\mu$ models

The $\Delta\mu$ model was deduced empirically and had first been proposed to explain the $1/f$ noise in homogeneous semiconductors [67], i.e. in resistors provided with low-noise ideal Ohmic contacts. Hooge [67] observed that the normalised current noise spectral density for a wide range of materials could be represented by the empirical relationship

$$\frac{S_I}{I^2} = \frac{\alpha_H}{Nf} \quad (2.26)$$

Equation (2.26) assumed that the device shows an ohmic(linear) I - V characteristic so that the spectral density scales with I^2 . N is the total number of carriers in the conductor, or more generally, the total number of fluctuators. It was originally thought that α_H was a fundamental constant for all materials, approximately 10^{-3} . Note that α_H is dimensionless only for a pure $1/f$ spectrum, i.e. with a frequency exponent γ exactly 1. At present, α_H is considered to be material dependent, which can vary over many decades, depending on the degree of crystalline of the material. Good material has a low α_H value and thus generate low $1/f$ noise and vice versa. For silicon, α_H has been observed to be in the range from 5×10^{-6} to 2×10^{-3} [68]. As such, the α_H parameter and flicker noise in general can thus be used to investigate the structural quality and processing induced defects in semiconductor technology. A major difficulty with noise studies is identifying the responsible source, since there are various fluctuation processes to be considered. Since α_H is not a constant but is subjected to the crystalline quality, the following refinement is necessary [69]:

$$\alpha_H = \alpha_{latt} \left(\frac{\mu}{\mu_{latt}} \right)^2 \quad (2.27)$$

where α_{latt} is a constant having an approximate value of 2×10^{-3} , μ is the carrier mobility and μ_{latt} is the mobility due to lattice scattering only. Here, it is assumed that scattering mechanisms are independent and acting in parallel, resulting in a total mobility that follows Matthiesen's rule and is smaller than μ . It follows from (2.27) that the lattice (phonon) scattering is the dominant $1/f$ noise generating process, while other types of scattering related to defects (Coulombic, neutral, scattering) suppress the $1/f$ noise at low frequencies [53]. Putting Hooge's rule in the context of a standard MOSFET in linear operation results in

$$S_{V_G}(f) = \frac{q}{C_{ox}} \frac{\alpha_H}{WLf} (V_{GS} - V_T) \quad (2.28)$$

Equation (2.28) is valid above threshold voltage and predicts a linear dependence of noise spectral density on the gate overdrive voltage ($V_{GS} - V_T$). Experimentally, there is evidence that p-channel devices are better described by (2.28) [18, 19] and thus show better correlation with mobility fluctuations. Physically, this has been explained that for p-channel devices fabricated with single n+ polysilicon gate material, they show a buried channel behaviour and thus can be considered as a 'bulk' device compared with an n-MOSFET, which has a more 'surface-like' nature. In other words, channel carriers in the semiconductor bulk induce flicker noise due to lattice scattering in the bulk rather than interaction with traps in the surface dielectric. Hence, the larger distance of the inversion layer from the interface and the oxide traps explains

the lower $1/f$ noise which is generally found for p-MOSFETs in the same CMOS technology [61].

One particular problem with the mobility theory is that during weak inversion, the noise spectral density should follow a $1/N$, or a $1/I_D$ relationship, according to (2.28). In other words, the normalised drain current noise should increase exponentially in the subthreshold regime [64]. In most cases far less than predicted by (2.29).

Another unsolved question is the theoretical explanation of α_H . Although several explanations have been proposed, none are generally accepted, and the Hooge parameter is still considered to be purely empirical and dependent on technological variables. One recent approach is the universal power spectral density representation introduced by Wolters *et al.* [25, 26]. In this approach, a universal $1/f$ noise plot is obtained for different solid-state systems, i.e. MOSFETs and metal interconnects, if the noise power density $S_P = S_{Id}/g_{ch}$ is plotted versus the power per charge P/Q , with $g_{ch} (= \partial I_D / \partial V_{DS})$ the channel conductance. The $1/f$ fluctuations are then just the natural power fluctuations of any power dissipating system. Both the $1/Q$ dependence predicted by Hooge's theory and the interface state dependence coming out of the McWhorter theory could be explained in this way. The physical basis of the proposed model is, however, questionable and needs further improvements.

It should be noted that a hybrid $\Delta\mu$ model has been formulated by Surya *et al.* [62], such that mobility fluctuations are thought to be caused by scattering at the interface traps N_{it} . The fluctuation in trap occupancy in turn induces a change in the scattering cross-sectional area and rate. The

corresponding mobility fluctuations are considered independent of possible number fluctuations. This model has been used to describe the flicker noise in p-channel devices, under various operating temperature [57].

Finally, previous works based on pre-submicron devices [55, 57, 70-71] concluded that ΔN is the major cause of flicker noise in n-MOSFET, while $\Delta\mu$ is responsible in the case of p-MOSFET. As mentioned earlier, the main reason is that the former is surface channel devices, hence the interaction of channel carriers and oxide traps would play a more significant role in generating $1/f$ noise, while the latter is buried channel devices, and fluctuations in channel charges depend more on the interactions with crystalline defects in the bulk. However, the use of p^+ polysilicon gate in building modern deep submicron p-MOSFET to overcome short channel effects has inevitably turned the p-MOSFET into surface channel device. Hence the role of non-fundamental $1/f$ noise sources is now as important in p-MOSFET as it had been for n-MOSFET, and hence the introduction of correlated models to account for the effects of carrier numbers and mobility fluctuations on flicker noise as they are brought together.

2.5.4 Linear operation: Correlated Mobility (ΔN - $\Delta\mu$) Model

While models described previously can be categorised as pure number or pure mobility theory, recent modelling efforts attempt to explain the two effects together in order to derive a universal $1/f$ noise theory for MOSFETs. One of the earliest works in this came from Mikoshiba *et al.*, who considered the sum of a ΔN and a $\Delta\mu$ term [55, 72]. Experiment shows that the two terms

are in fact correlated. The systematic study of RTS in small area MOSFET has greatly helped in understanding this effect [73-75], resulting in the development of what could be considered as a correlated mobility fluctuation theory [2, 16, 28, 30, 31].

Evidence from RTS studies on small-area devices has shown that mobility effects related to trap-scattering generate low frequency fluctuations [75]. This is especially so for signals at low temperatures, where the anomalously high amplitudes ΔI_D observed cannot be explained by a ΔN approach only, i.e. by the exchange of one carrier between trap and channel. In other cases, the variation of the RTS amplitude at high drain currents has been explained by considering interface and oxide trap scattering on the mobility, as shown in [76]. The resulting amplitude is given by

$$\frac{\Delta I_D}{I_D} = \frac{1}{WL} \left(\frac{1}{N} \pm \alpha_{sc} \mu \right) \quad (2.29)$$

where α_{sc} is a scattering parameter on the order of 2×10^{-15} Vs [76]. The sign depends on the charge of the trap: if the trap is neutral upon electron capture, it would be a minus-sign, since the mobility increases after carrier capture and, therefore, opposes the number reduction proportional to $1/N$. For a trap which is charged when occupied, Coulombic scattering will reduce the mobility, hence the plus-sign applies in (2.29).

The basic concept behind the correlated mobility fluctuations model is given in (2.29). Not only does it take into account that the oxide/interface traps interact with the channel through carrier capture and generation, but also indirectly through a change in scattering rate, when a trap becomes occupied or

emptied. This is generally accompanied by a change in the charge state of the scattering centre, which affects the fluctuation of mobility through a change in the scattering cross section from a charged centre to a neutral one or vice versa.

The drain current noise spectral density takes in this concept the form [28, 30]

$$SI_D(f) = \frac{kTI_D^2}{\alpha_t f WL} \left(\frac{1}{N} \pm \alpha_{sc} \mu \right)^2 N_{ot}(E_F) \quad (2.30)$$

and produces a good fit to experimental data of both n- and p-MOSFETs and in a broad temperature range [77]. According to (2.30), a quadratic dependence on $(V_{GS} - V_T)$ is expected [64]. The resulting input-referred noise spectral density becomes

$$S_{V_G} = S_{V_{fb}} [1 + \alpha_{sc} \mu C_{ox} (V_{GS} - V_T) / q]^2 \quad (2.31)$$

with $S_{V_{fb}}$ the flat-band voltage noise spectral density. The latter is defined by [64],

$$S_{V_{fb}} = \frac{S_{I_D}}{G_m^2} = \frac{q^2 k T N_t(E_f)}{\alpha_t W L C_{ox}^2 f^\gamma} \quad (2.32)$$

where use is made of the symmetric role played by the gate and the flat-band voltage. Note that this is only applicable at weak inversion, where the spectral density at flat-band voltage is weakly dependent on the gate bias. Otherwise, the equation becomes:

$$S_{V_G} = \frac{S_{I_D}}{G_m^2} \quad (2.33)$$

For small α_{sc} , i.e. mobility scattering that is insensitive to the insulator, the classical ΔN (2.32) is retrieved [78]. Note that if different types of oxide traps, i.e. donor- and acceptor-like are present, Eqs. (2.30-32) can produce a local minimum in the noise for a certain drain current or gate overdrive voltage in linear operation [64]. This is related to the + or - sign in the equations, or in other words, to the fact whether the trap induced mobility change assists or opposes the number reduction.

2.5.5 Application to this Work

In order to discriminate between the different $1/f$ noise sources, the following straightforward procedure has been recommended [64]. As a first step, the normalised drain current noise in linear operation should be plotted versus the drain current in a log-log plot and compared with the $(g_m/I_D)^2$ ratio, like in Figures 2.8a and 2.9a. If both curves run parallel, the number fluctuations dominate the overall flicker noise behaviour. Additionally, correlated mobility fluctuations will be present when the S_{VG} shows a quadratic increase with the gate overdrive voltage. Mobility fluctuations could be the origin of the $1/f$ noise if the normalised drain current noise varies according to $1/I_D$, especially in weak inversion. Additionally, the S_{Vg} will diverge in that case below threshold and follows a $1/I_D$ law [64].

After identifying the role of numbers and correlated mobility fluctuations in fresh devices, the unstressed DUT would be subjected to NBTI DC stress conditions. Since the objective would be to characterize the additional oxide traps generated during NBTI that are responsible for permanent NBTI degradation, DC stressing is sufficient. Post-stress noise measurements would then be carried out and compared with pre-stress data to determine the impact of NBTI on flicker noise, and consequently, the nature of oxide traps generated in the process.

Chapter 3 METHODOLOGY OF CHARACTERIZATION

3.1 Introduction

Negative-Bias Temperature Instability (NBTI) characterization techniques have generated much interest in recent years. This was mainly driven by the desire to obtain the most accurate time exponent value for correlation with the Reaction-Diffusion (R-D) model. Once DC measurement methods were found to have contributed significant time delay and unable to fully characterize fast recovery traps, various groups came up with different fast measurement methods, for example, On-the-Fly (OTF) [79-80] and Fast Switching (FS) [81], in hopes of identifying the true time exponent.

While these novel methods enable the fast recovery hole traps to be characterized, their uses are not without limitations. In particular, the OTF method cannot determine the “time-zero” reference value, and by measuring at stress conditions, additional degradations were introduced by the setup and does not reflect normal operating conditions. Moreover, these fast measurement setups came with arbitrary measurement delays, dependent on the circuits used in setting up the system. This means that experimental results based on different inherent measurement delays could not be compared easily. This hinders the progress in finding the true mechanisms responsible for NBTI threshold voltage degradation attributed to interface states.

In this project, the conventional DC stress-measure-stress method was utilized to characterize NBTI. Thus, fast traps were not monitored. In addition, flicker noise measurements could only be conducted by supplying a DC drain current. To ensure consistency and comparable results between flicker noise measurements and NBTI characterization, the DC setup was used. Since all the measurement systems used to-date (both fast and slow ones) have fixed delays anyway, the outcome from the setup is not affected by the longer measurement delays.

In the subsequent sections, the DC stress-measure-stress method would be described, together with the charge pumping and subthreshold current techniques that determine interface trap density. The static and bipolar stress methods would be described as well. Finally, the in-house flicker noise measurement setup and the measurement steps would be discussed.

3.2 DC Stress-Measure-Stress Method

The DC Measurement setup requires a probe station with 4 probe tips connected to the terminals of the device under test (DUT), which are in turn connected to the source-measure units (SMU). The SMU is responsible for measuring the voltage and current at the terminals probed.

The DC Method for NBTI characterization involves measuring the I_d - V_g characteristics of the DUT before it undergoes stressing. During the stressing phase, as shown in Figure 3.1, a voltage bias is applied at the gate terminal at the pre-defined stress voltage (V_g^s) and temperature at specific time

intervals. The stress voltage is released when each stress period has elapsed, and the I_d - V_g characteristic is measured (Figure 3.2), after which the DUT is stressed again. Hence this method follows the stress-measure-stress sequence.

Figure 3.1 Conventional DC Stress-Measure-Stress for NBTI characterization, showing V_g variations over the stress duration. Negative gate bias applied at stress level is interrupted and I_d - V_g sweep is carried out, hence the slope at measured section as drain current values were sampled at intervals of V_g . Gate bias is then resumed to stress level again, and this process is repeated throughout the stress cycle.

Figure 3.2 Extraction of threshold voltage shift before and after NBTI from the I_d - V_g measurements of a DPN p-MOSFET, $W/L = 10\mu\text{m}/0.18\mu\text{m}$, $t_{ox} = 20\text{ \AA}$, at drain bias = -0.1V . Device was subjected to NBTI stress of 10MV/cm electric field, at 100°C .

After the various I_d - V_g plots have been gathered to include the pre-stress and post-stress results, the next step involves extracting the increase in threshold voltage after stressing. From the $\log_{10}(I_d)$ - V_g plot, a constant current is selected such that the drain current remains in the subthreshold region in the pre- and post- stress $\log_{10}I_d$ - V_g curve. The difference across the corresponding gate voltage values will be the threshold voltage shift $|V_t|$.

3.3 The Charge Pumping Method

The charge pumping (CP) method is commonly used in measuring interface trap density (N_{it}). It is suitable for extracting N_{it} measurements in small dimension MOSFETs, compared to the Capacitance-Voltage (C-V)

measurement method, which is more suitable for larger geometry MOS capacitors.

The CP method is carried out by pulsing the gate voltage at regular time intervals, to alternate the surface channel between inversion and accumulation. The drain and source terminals may be tied together or grounded, and the charge pumping current is then extracted from the substrate terminal.

Figure 3.3 Illustration of the general CP setup – the gate terminal is pulsed while source and drain are grounded. Charge pumping current I_{cp} is extracted from the substrate terminal. (a) shows the surface channel at time t_1 ($|V_g| > |V_t|$), when the p-MOSFET is in inversion (with holes at the channel, denoted by filled circles); (b) shows the surface channel in accumulation at time t_2 ($|V_g| > |V_{fb}|$), with electrons (unfilled circles) in the channel. (c) The energy band diagram of the Si in p-MOSFET under inversion, with horizontal lines denoting interface traps, and filled circles represents holes on the interface traps. During accumulation, the holes are swept away and replaced by electrons (d) shows the energy band diagram for the n-MOSFET during inversion and accumulation (unfilled circles denote electron, filled circles denote holes)

As the device switches from inversion to accumulation (and vice versa), there is a finite transition period due to the rising and falling edges of the gate voltage pulse. Most of the holes in the inversion layer (for p-MOSFET, Figure 3.3(a)) drift to the drain and source during this short duration. However, holes that are on interface traps do not have enough time to be discharged and remained with the interface traps. Once the device is switched to accumulation (or inversion), the trapped holes recombine with some the electrons now brought to the surface, illustrated in Figure 3.3(b). The energy diagrams in 3.3(c) shows holes occupying the interface traps during inversion and electrons during accumulation. The same is true when the gate is pulsed to inversion. After each recombination in accumulation (inversion), there is less electrons/holes returning to the substrate terminal than before, and the difference in the charge pumping current, ΔI_{cp} , is proportional to the interface trap density ΔD_{it} (given as $\text{cm}^{-2} \text{ eV}^{-1}$). As ΔD_{it} and ΔN_{it} are related by $\Delta N_{it} = \Delta D_{it} \times \text{Gate area } A_G$, ΔI_{cp} , is directly proportional to the density of generated interface traps (ΔN_{it}) and the pulse frequency (f_{cp}), given by:

$$\Delta I_{cp} = qA_G f_{cp} \Delta N_{it} \quad (3.1)$$

Through this series of measurement and calculations, the CP method is able to determine the interface traps density. However, there had been reported studies regarding the limitations of the CP method. In particular, by pulsing the gate to positive bias, it could cause fractional passivation of the stress-induced interface traps [18], as well as probing only a limited portion of the Si bandgap [41]. As discussed in the lit review [Section 2.3], Ang *et al.* [19] has since showed how these limitations of charge pumping method may be

justified, by determining the change in the subthreshold swing and the resultant interface trap density. This method of using the subthreshold swing (subsequently referred to as the “subthreshold swing method”) would be used in the experiments, particularly in Chapter 5, to compare with CP results, and is discussed in the next section.

3.4 The Subthreshold Swing Method in MOSFET

The subthreshold swing method is another method to determine the interface states density. Unlike the charge pumping method, which gives the interface trap density as it is measured, the subthreshold swing method is a differential method to determine the *change* in the interface states density, for example, before and after a DUT is subjected to stress. The derivation of the subthreshold swing from the drain current would first be shown. The general equation for the relationship between the linear drain current I_d and gate bias V_g is given as follows:

$$I_D = I_{D0} \exp\left(\frac{q(V_{gs} - V_T)}{nkT}\right) \left(1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right) \quad (3.2)$$

where I_{D0} is a temperature, device dimension and substrate doping dependent parameter, $n = 1 + (C_b + C_{it})/C_{ox}$. Ideally, $n = 1$ but increased doping and interface charge capacitance per unit area would inevitably lead to increase in the value of n . Hence, equation 3.2 shows the dependence of the drain current on the interface charge capacitance, which is related to the interface traps density. The subthreshold plot of $\log_{10} I_d$ against V_g , for $V_{ds} \gg kT/q$, is then drawn.

After stress, an increase in the interface state density would distort the I_d - V_g curve. The subthreshold slope, given as $d\log_{10}I_d/dV_g$, would decrease, causing the corresponding subthreshold swing, SS ($SS = (d\log_{10}I_d/dV_g)^{-1}$), to increase. The increase in the subthreshold swing ΔS after stress is then given as:

$$\Delta S = SS_{after} - SS_{before} = \ln 10 \cdot \frac{kT}{q} \cdot \left(\frac{\Delta C_{it}}{C_{ox}} \right) \quad (3.3)$$

where ΔC_{it} ($= q\langle \Delta D_{it} \rangle$) is the capacitance of the interface trap per unit area, $\langle \Delta D_{it} \rangle$ is the average interface state density in $\text{cm}^{-2} \text{ eV}^{-1}$. Hence the stress-induced interface state density $\Delta N_{it} = \langle \Delta D_{it} \rangle \cdot \Delta E_{ss}$, where ΔE_{ss} is the effective energy window probed. As highlighted in [19], ΔE_{ss} is linked closely to the change in the gate voltage $|\Delta V_g|$, i.e. $\Delta E_{ss} \sim |\Delta V_g|$. Figure 3.4 shows a subthreshold $I_d - V_g$ curve of a typical p-channel MOSFET, with drain bias at -0.1V. In the subthreshold region, the Si surface band bending ψ_s at a given V_g is expressed by:

$$V_g - V_{FB} = \psi_s - \frac{\sqrt{2K_s \epsilon_0 q N_D \psi_s}}{C_{ox}} + V_{poly} \quad (3.4)$$

where K_s ($=11.8$) the relative permittivity of Si, ϵ_0 the permittivity of free space, N_D the doping concentration of the n-Si substrate, V_{poly} (~ 0 at the subthreshold region) is the polysilicon depletion voltage, and V_{FB} is the flatband voltage. V_{FB} may be taken to be independent of ψ_s in an unstressed device with low interface state density. This term denotes the voltage drop across the gate oxide layer V_{ox} . For an ultrathin gate oxide ($EOT = 1.6\text{nm}$), $C_{ox} \sim 2.2 \times 10^{-6} \text{ F/cm}^2$. For N_D on the order of 10^{17} cm^{-3} , $V_{ox} \sim 60\text{mV}$ at $\psi_s = 0.6\text{V}$. From first order analysis, it could be shown that the change in gate voltage ΔV_g is closely

followed by a change in Si surface band bending $\Delta\psi_s$ in an ultrathin gate device (i.e. $\Delta\psi_s \sim \Delta V_g$), since the voltage drop across the ultrathin gate dielectric is small. Therefore, by obtaining the subthreshold swing over a given V_g range, it could be determined that $\sim 0.33\text{-}0.34\text{eV}$ of the Si bandgap is probed. Figure 3.4 inset shows the energy range of the Si bandgap probed using the subthreshold swing method.

Figure 3.4 Subthreshold drain current against gate voltage of a fresh DPN device ($W/L = 10\mu\text{m} / 0.065\mu\text{m}$) at drain bias of -0.1V [19]. Selected region (unfilled circles) for extracting subthreshold hold is where ΔV_g closely varies with $\Delta\psi_s$ for first order analysis. Inset is the Si energy band diagram, with the shaded region being the energy window probed by the subthreshold swing method.

Ang *et al.* has showed that show that results of the generated interface traps obtained from charge pumping closely resemble those obtained independently using the subthreshold swing method [19]. As described in

Section 2.3, ΔE_{ss} is within the effective energy range probed using the CP method (ΔE_{cp}), even though the latter involves biasing the gate to positive voltage. On the other hand, the subthreshold method involved measuring from the subthreshold regime and does not enhance recovery in any way by the change in gate polarity. As the result shows that the recovery effects under CP measurements were minimal even with positive gate bias, it means that experimentally there would be no difference whether I_d - V_g sweep is done first before charge pumping, or vice-versa. In the following experiments, the procedure was kept consistent to conduct the I_d - V_g sweep first before the CP measurements.

The subthreshold swing method is not commonly used on the ultrathin gate p-MOSFETs primarily because this method is less sensitive to large C_{ox} . In general, ΔS of a modern thin gate device has an average ΔD_{it} value of $10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$. In addition, being a comparative technique, this method is susceptible to measurement fluctuations in the weak inversion region. This may be overcome by increasing the integration time in the SMU. This would lead to higher measurement time, but since the threshold voltage shift (via constant current method) and the subthreshold swing needed are extracted from the same subthreshold region, and measurements do not monitor fast recovery traps, the time increase is not of concern.

The CP and the subthreshold swing characterization techniques mentioned so far has assumed a discussion using static stress. However, static stress results exclude the impact of positive gate bias have on the recovery of deep-level hole traps. This makes separating the various constituents of threshold voltage degradation (interface and oxide traps) difficult by just using

static stress. The following section describes how bipolar stress could facilitate the identifications of the components causing different degrees of $|\Delta V_t|$.

3.5 Static and Bipolar NBTI Stress

Typically, NBTI stress involves applying the negative gate voltage to the p-MOSFET throughout the stress duration. This approach of applying a gate voltage with only one polarity is known as static stress. It was discovered [18, 82] that switching to positive gate bias would result in partial recovery of the threshold voltage degraded. However, it was uncertain whether interface or oxide traps were responsible for the recovery. Through the use of both static and bipolar stressing, Ang *et al.* [19] has shown that while the static $|\Delta V_t|$ shift is still significantly higher than that of the bipolar $|\Delta V_t|$, the interface trap density measured by the CP method for both static and bipolar stress remained comparable. It became apparent that the interface traps measured by the CP method did not contribute to recovery, and this increased recovery at the positive gate bias was attributed to deep-level hole traps (DLHTs). Hence, subjecting the device to bipolar stress allows the DLHTs to be accounted for in experimental results.

Figure 3.5 illustrates the difference between static and bipolar stress, in terms of the applied gate stress against stress duration. For a given stress duration t_0 used in static stress, a duration of $2t_0$ is used in bipolar stress, with half the time subjecting the device to a positive recovery gate voltage, V_g^r . The value of V_g^r was chosen to be higher than the positive gate bias used in CP measurements, and the net recovery period was much longer than the time

taken during CP measurements ($< 1\text{s}$). For bipolar stress, a 100 kHz trapezoidal voltage pulse switching between V_g^s and V_g^r . The pulse rise and fall times were 40ns and the duty cycle is 50%. The advantage for cycling the gate bias in this AC manner was to immediately recover some of the hole traps generated by the preceding cycle.

Figure 3.5 Illustration of the difference between static stress (left) and bipolar stress, in terms of V_g^s variations against stress duration.

The various measurement techniques discussed earlier aimed to distinguish $|\Delta V_t|$ due to interface states generation from those due to oxide traps (general classification of traps not formed near the interface). Ang *et al.* stated that the results may be presented using the $|\Delta V_t| - |\Delta N_{it}^{CP}|$ relationship, as shown in Figure 3.6. The theoretical plot based on charge pumping measurement had assumed the CP method to have covered all the interface states generated. Hence, by comparing solely the static stress against the theory plots (Figure 3.6 regions A and B), Huard [17] over-estimated $|\Delta V_t|$ contribution coming from oxide traps generation, since the CP method could not quantify the stress-induced interface traps from the upper half of the Si bandgap. In the $|\Delta V_t|$ -

$|\Delta N_{it}^{CP}|$ relationship curves used in this project, the theory curve still comes from CP measurements, but it is noted that the measured interface traps from the CP method were from a limited energy window only. With this understanding in mind, the difference in $|\Delta V_t|$ between the static stress and theory curve are due to deep-level hole traps and interface traps coming from the upper half of the band gap (Figure 3.6 regions A and B), while the $|\Delta V_t|$ coming from DLHTs came from region a (as the use of bipolar stress neutralised most of these hole traps). Thus region B consisted of interface traps that could not be probed by the CP method, as well as some of the deep-level hole traps with energy levels pinned by the Si/SiO₂ conduction band and could not be discharged by electron injection.

Figure 3.6 Graphical approach depicting how interface traps and DLHTs may be distinguished by the use of static and bipolar stress, and comparing them with the theory (measured by CP method) curve.

While static and bipolar stress with subsequent CP and the subthreshold swing characterization techniques strive to measure oxide traps close to the Si/SiO₂ interface, the high frequency used in the former and the fundamental limitation of the latter (equation 3.2 only included how interface traps might influence the drain current magnitude) did not consider oxide traps further

from the interface for measurements. To overcome this, flicker noise measurements through an in-house setup will be utilized to determine how the distribution of such oxide traps varies during NBTI.

3.6 Measurement and Characterization of Flicker Noise

3.6.1 Oxide Traps Measured by Flicker Noise

It was described in the earlier sections that the charge pumping and subthreshold swing methods are suitable for determining the interface trap density, albeit only traps near the Si/SiO₂ interface, and within a limited energy window. In particular, the high frequency pulse (~1 MHz) used in charge pumping means that there is insufficient time for deeper oxide traps to trap the channel charges, before the polarity of the gate pulse reverses. While NBTI studies have mainly focused on the stress-induced interface states, as described in the Reaction-Diffusion (R-D) model, oxide traps that may be generated during NBTI and are further from the Si/SiO₂ interface has not been given as much coverage. Before determining if flicker noise can be used as characterization tool for NBTI, the nature of oxide traps responsible for flicker (1/f) noise in MOSFETs should be understood first.

As defined in the numbers fluctuation and correlated mobility models (2.22) and (2.32), the implied oxide trap density at a given noise power spectral density (and hence at discrete gate voltage level) is with respect to the Fermi level. This is commonly denoted as $N_{ot}(E_F)$. The relationship shown in (2.32) for $N_{ot}(E_F)$ makes use of the fact that the function $f_T(E)$ [$1 - f_T(E)$] is sharply peaked around the surface Fermi level E_F . In other words, only oxide traps in an energy range within $E_F \pm kT$ contribute to 1/f noise. This is illustrated in Figure 3.7(i), when a p-MOSFET is bias to weak inversion regime. The band bending of the energy diagram occurs at the surface of the Si substrate, but

there is insufficient voltage to bend the energy band of the oxide. It could then be seen that holes from the inversion layer tunnel through a certain distance from the Si/SiO₂ interface before the trap-detrap mechanism occurs. The mean value is the E_F (denoted by the bold unbroken line), while the maximum-minimum come from the $\pm kT$ portion (denoted by the broken lines). The shaded region denotes the energy range scanned during weak inversion.

On the other hand, under strong inversion, band bending in the oxide occurs, as shown in Figure 3.7(ii). The band bending has an effect of pulling the energy level of the traps up, hence those traps captured during weak inversion move up (the shaded portion, the skewed shape a result of oxide band bending), while those traps that were previously nearer to the valence band had energy levels raised and could now be captured by flicker noise (the filled region). Therefore, by extracting flicker noise data over a range of gate voltages from weak and strong inversion, the distribution of the oxide traps could be deduced.

Figure 3.7 (i) shows the energy range of the oxide traps captured during weak inversion (no band bending at the oxide) (ii) shows the energy range of oxide traps scanned as the gate bias is gradually increased from weak inversion to strong inversion. Energy band diagram is shown for a p-MOSFET. Partially shaded region denotes the instantaneous energy level scanned by flicker noise measurement during weak inversion, while the grey area denotes the energy level of noise measured during strong inversion. The change in shape of the partially shaded region illustrates how the energy window changes with oxide band bending.

3.6.2 Conventional Flicker Noise Measurement Setup

The schematic diagram of a conventional setup for measuring flicker noise is shown in Figure 3.8. The MOSFET is biased to operate at inversion region with a DC gate and drain voltage bias. R_D is a resistor, typically with a large value of 100k Ω , and the preamplifier (preamp) is used to amplify the signal before passing the output signal to the signal analyzer. As noted in the

lit review (Section 2.5), the signal of a DC current is theoretically flat, but in reality, has fluctuation (or noise) within it. A large R_D is used so that these fluctuations could be magnified into the preamp. A key disadvantage of such as setup is the high amplitude of V_{DD} required. For example, if a drain current value of 1mA is used, and $R_D = 100\text{k}\Omega$, the V_{DD} required will be $\sim 100\text{V}$. Such high voltages could be difficult to set up and raise safety issues when used in common laboratories.

Figure 3.8 Schematics of Conventional Drain Current $1/f$ Noise Setup

3.6.3 The In-house $1/f$ Noise Setup

The need for high applied voltage required during noise measurement meant that another setup is required. Hence the schematic of the in-house setup was designed and used in this project, as shown in Figure 3.9. A key advantage of this new setup is the absence of high applied voltage. This could be achieved by connecting the drain terminal to the current preamp, as the

current preamp acts as a resistor with infinitely high resistance value. The other terminal of the preamp serves to close the loop in the circuit.

The following equipments required are – 1) Current and voltage pre-amplifiers 2) Signal analyzer. Preamplifiers from Stanford Research Systems SR560 (voltage) and SR570 (current), and signal analyzer HP35670A were designed and used in the in-house setup, but the setup is generic and could be implemented with hardware providing similar functions.

Figure 3.9 Schematic of the $1/f$ noise setup designed and used in this project. The drain and source terminals are connected to the same preamp to form a closed path for current flow. The gate is connected to another current preamp (not shown) for gate voltage supply. The drain and gate terminals are negatively biased while the source is grounded.

The current pre-amplifier has several functions. Firstly, the input terminal provides DC voltage bias to the connected device terminal, as well as measuring the resultant current (DC + noise) from the same terminal. The drain and source terminals are connected to the current preamp to form a closed loop for current flow, while the gate terminal receives supplied voltage

from another current preamp (not shown). Secondly, its bandpass filter allows the DC component of the current to be filtered off, leaving the fluctuation components to be passed off as the output signal. A 6dB bandpass filter is normally applied to the input signal, for the range of frequency 1 Hz to 10 kHz measured. Thirdly, the sensitivity of the pre-amplifier could be adjusted so that the input signal is sufficiently amplified, since the raw input could go as low as 10^{-9} A. The output signal from the current pre-amplifier is then sent to the input terminal of the voltage pre-amplifier for further amplification, before the resultant signal goes into the signal analyzer.

The signal analyzer is used to facilitate Fast Fourier Transform calculations to convert the measured time-domain signals into frequency-domain spectrums. This is necessary in order to compute the power spectral density (PSD), which refers to the power carried by the waveform (in this case, the time-domain fluctuation due to flicker noise). Only by computing the PSD of the drain current, which is also known as S_{Id} , could further analysis be done. Note that for the signal analyzer, the S_{Id} is measured in dBV, with respect to 1V, which means additional calculations are needed in order to determine S_{Id} in terms of A^2/Hz . Given that flicker noise source is random in nature, measured data are averaged to reduce the impact of nonlinearities.

From the measured S_{Id} (in dBV) at each frequency, the “measured” voltage fluctuation needs to be worked out first. $PSD \text{ in dBV} = 20 \log_{10} (V_{measured}/V_{reference})$, where $V_{measured}$ is the measured voltage fluctuation and $V_{reference} = 1V$. The $V_{measured}$ could be determined by subtracting the background noise in the system. In general, the background noise in the system consists of thermal and shot noise. The former is generation by equilibrium fluctuations

of electric current inside electric conductor (no applied voltage), due to the random thermal motion of charge carriers (electrons); random fluctuations of electric current in conductor, due to charge carriers, esp. when charge is not well-localised, hence non-equilibrium condition.

From $V_{measured}$, the actual current fluctuation measured for a particular frequency could then be found, since the conversion from current to voltage during data extraction was due to the signal passing through a current pre-amplifier and a voltage pre-amplifier sequentially. The mean drain current fluctuation $\overline{\Delta I_d}$ is then extracted for each frequency measured.

From $\overline{\Delta I_d}$, the power spectral density is then determined by squaring it and dividing by the equivalent noise bandwidth (ENBW) factor used by the signal analyzer. In this experiment, the Hanning window is used, which has a factor of 1.48. This window was chosen for its reduced signal leakage and improved amplitude accuracy. The downside is that a loss of frequency resolution is to be expected. However, since the key concern in this project is the trend the spectrum may show over the frequency range measured, as opposed to the magnitude at each discrete frequency, the Hanning window is hence chosen.

3.7 Summary

In this chapter, the various characterizations techniques used in the experiments were described. DC stress-measure-stress measurements are used to determine the $|V_t|$ due to static and bipolar stress. At the different stresses

used, charge pumping and subthreshold swing methods were utilized to characterize the stress-induced interface states. The various tools used allowed the different types of traps and relative contributions to $|V_t|$ to be identified. In addition, the in-house flicker noise measurement setup and how measurements are taken were discussed.

Chapter 4 IMPACT OF DEEP-LEVEL HOLE TRAPS ON THE POWER-LAW TIME EXPONENT

4.1 Introduction

The Reaction-Diffusion (R-D) model has always been used to explain the mechanism of NBTI interface states generation. It is widely used because it has been able to explain consistently the time exponent of 0.25 with respect to a physical framework. This model related the rate of interfacial trapped charge generation to the rate of diffusion of atomic hydrogen away from the Si/SiO₂ interface. The hydrogen diffusing species were believed to have come from the bond breaking of Si-H bonds by holes in the inversion layer. Currently, the experimentally obtained time exponent of 0.14-0.17 was attributed to the hydrogen molecule H₂ as the diffusing specie, since atomic H is unstable and could not exist long enough for diffusion.

Since then, various works had subjected oxynitride gate p-MOSFETs to NBTI stressing, and put the actual time exponent value into dispute. Fast measurement methods extracted time exponent values as low as ~0.05 [12, 15], challenging previous assumption that the value of 0.25 was a unique identification to NBTI mechanism. In fact, other studies have shown that measurement delay could lead to a wide range of the time exponent value, from 0.05 to 0.17, with obtained values dependent on the delay time. This dependency on the measurement delay meant that using arbitrarily obtained exponent values to explain interface states generation is no longer a reliable method.

Recent studies have revealed the generation of deep-level hole traps (DLHTs) over a broad gate stress voltage (-2.6V to -1.4V) [19, 83-84]. Findings showed that these DLHTs were generated near or above the conduction band edge (E_C) of Si, which, unlike hole traps that recover upon the removal of the stress gate bias, could remain positively charged for long durations after stress removal. As they do not recover quickly, they could be detected by conventional DC stress-measure-stress method. These DLHTs could recover only in the presence of positive gate bias, which caused electrons from the n-Si substrate to detrap these DLHTs when energy levels of the traps are lower to below E_C .

In this chapter, the focus will be on the relationship between such deep-level hole traps and the extracted time exponent value. Devices fabricated from two different gate oxide nitridation processes were used – the thermally nitrided oxide (TNO) and the decoupled-plasma-nitrided (DPN) processing. The key difference is that nitrogen concentration [N] is concentrated near the polysilicon-gate oxide interface for the DPN-gate, while [N] distribution is broader in the TNO-gate device. As the thermally nitrided-oxide (TNO)-gate p-MOSFETs were found to have generated significant amounts of DLHTs [84-86], it was the first device type chosen for investigation. The time exponent extracted using the dc measurement was less than 0.2. However, once the DLHTs were discharged, the extracted exponent value rose to about 0.3. Results from TNO-gate device were compared with SiO₂-gate devices as well. For decoupled-plasma-nitrided (DPN)-gate devices, a lower time exponent value due to the presence of DLHTs was observed, even as DPN-gate devices were expected to have less hole trapping. However, when similarly processed

DPN-gate n-MOSFET is subjected to NBTI stress (conditioned to yield similar interface states density as p-MOSFET), but measured at positive bias, the time exponent becomes about 0.5. As DLHTs were neutralized under positive gate bias, the higher exponent value in the n-MOSFET demonstrated that the impact of DLHTs is still significant in DPN-gate p-MOSFET. This result in turn suggested that experimentally obtained exponent value of 0.14-0.17, currently used to support molecular H_2 as the main diffusion-drive species in interface states generation, should be re-examined.

4.2 Experimental Setup

The devices under test (DUTs) were p+ polysilicon-gate p-MOSFETs with SiO_2 gate dielectric or ultrathin oxynitride. The oxynitrided samples were formed either using rapid thermal oxidation followed by NO anneal (TNO) or by DPN. Similar processing conditions were used for the n-channel devices tested (both the p-MOSFETs and n-MOSFETs DUTs came from the same wafer). Equivalent oxide thickness (EOT) for the TNO processed DUT was $\sim 20 \text{ \AA}$; EOT of DPN devices was $\sim 15 \text{ \AA}$. The nitrogen concentration in both TNO and DPN devices was $\sim 4\%$ atomic% at the Si/SiON interface and $\sim 6\text{-}13\%$ atomic% at the polysilicon gate/SiON interface. DC stress-measure-stress (SMS) method was used, and hence fast recovery was not monitored. This would not affect the conclusion, since the fast recovering hole traps do not contribute to interface states generation. At the same time, the deep-level hole traps of interest remained positively charged over long duration, and could be captured by the DC SMS method. The stress field was kept to $\sim 10\text{MV/cm}$ for

pMOSFETs and nMOSFETs after accounting for polysilicon gate depletion and work-function difference in the respective devices.

4.3 Time Exponent n in SiO_2 and TNO-gate Devices

The contribution of NBTI-induced DLHTs from p-channel devices was investigated using the relationship between the degraded threshold voltage ($|\Delta V_t|$) and the generated interface trap density measured by the charge pumping (CP) method ($|\Delta N_{it}^{CP}|$), by plotting the difference in $|\Delta V_t|$ between the static and bipolar stress, at a given increase in $|\Delta N_{it}^{CP}|$. This is shown in Figure 4.1. It has been shown that during bipolar stressing, when the gate voltage was pulsed to the positive polarity, DLHTs located near and/or above the conduction band (E_C) of Si are neutralized (hence the threshold voltage shift is lower), while the measured $|\Delta N_{it}^{CP}|$ remains unchanged [19]. Moreover, this difference in threshold voltage degradation increases between the static and bipolar stress, indicating that DLHTs are continuously generated during the stress cycle. This is contrary to reported study [18] which claimed that all hole trapping saturate within the first second of NBTI stress. By adding the theoretical relationship between $|\Delta V_t|$ and $|\Delta N_{it}^{CP}|$ into Figure 4.1, it could also be deduced that the difference between the bipolar stress and the theoretical/calculated plots would result in the interface traps density not measured by the CP method, representing generated interface states above the midgap of the Si energy band.

Figure 4.1 Threshold voltage shift $|\Delta V_t|$ (extracted at constant subthreshold current method) in terms of $|\Delta N_{it}^{CP}|$ (interface trap density generated and measured by the charge-pumping method). Solid line represents measurement taken after dc stress and then positive gate bias; dotted line is $|\Delta V_t|$ is calculated from the CP method

Having isolated the possible constituents of traps generated during NBTI stressing and measured using DC measurements – interface traps measured by CP method, interface traps above the Si midgap energy range and DLHTs – the time exponent in TNO and DPN devices would be determined next, and the impact of DLHTs have on the exponent is studied. In accordance with recent works [19, 45], TNO-gate pMOSFETs have been observed to generate higher ΔN_{it} and DLHTs compared to pure SiO₂ gate pMOSFETs. This observation was repeated in this experiment as well, as shown in Figure 4.2. From there, a correlation could be observed between the power-law exponent and DLHT as well, given that TNO devices, which generate more DLHTs during NBTI, exhibit a smaller overall n value than the SiO₂ p-MOSFETs ($n \sim 0.16$ in TNO devices compared to 0.26 in SiO₂ gate).

Having compared the two gate dielectrics, further experiments were carried out on the TNO p-MOSFET to determine the role of DLHT on the exponent. A unipolar stress was carried out on the TNO device before applying a positive gate voltage for approximately 5s, followed by post-stress I_d - V_g measurement (shown in Figure 4.1 as solid line). Applying a positive gate voltage neutralizes DLHTs without changing the interface trap density. In this case, the value of n increased to ~ 0.3 , which was comparable to the n measured for the SiO₂-gate device (Figure 4.2). This result confirms that the presence of DLHTs suppressed the value of the power-law time exponent. Earlier, it was observed that increased generation of DLHTs corresponds to a smaller exponent n in TNO devices. This relationship would next be investigated for DPN devices.

Figure 4.2 Power-law dependence of $|\Delta V_t|$: time exponent for TNO device is increased compared to that of SiO_2 device after application of positive gate bias, which detraps DLHTs

4.4 Role of DLHT in TNO-gate and DPN-gate Devices

It has been suggested that NBTI degradation in DPN-gate devices came predominantly from interface trap generation [8], and the contributions by hole traps would be minimal, hence the expected n would be higher. As shown in Figure 4.2, the time exponent of the DPN-gate devices is generally larger than that of TNO devices. This difference could be due to a smaller number of stress-generated DLHTs in DPN-gate p-MOSFETs. In DPN-gate devices, most of the nitrogen-induced DLHTs are located near the valence band of the p+ polysilicon gate, as shown in inset of Figure 4.3. As the probability of valence band electron tunneling to a DLHT is larger than the probability of electron tunneling out to the Si conduction band, this lowers the likelihood of

DLHTs being charged up. In addition, charges near the gate has a smaller effect on the threshold voltage shift compared to charges within the gate dielectric. Despite the larger n in DPN-gate devices, it is worth noting that increasing the nitrogen concentration increases DLHT, and correspondingly, decreases n . This is shown in Figure 4.4. The difference between static and bipolar stress represents $|\Delta V_t|$ due to the generation of DLHTs. At a given stress duration, DLHTs generated in the higher atomic % p-MOSFET is higher than that by the lower atomic % device, as denoted by arrows (a) and (b) respectively.

Figure 4.3 Power-law dependence of $|\Delta V_t|$ of DPN-gate p-MOSFET, showing smaller time exponent with increasing nitrogen concentration. Inset shows DLHTs situation at the p+ gate/SiON interface, which are readily neutralized by valence and electrons

Figure 4.4 DPN-gate p-MOSFET with higher nitrogen content still generates more interface traps and DLHTs compared to those with lower nitrogen. This suggests that DLHTs generation is still important in DPN devices. Arrows (a) and (b) denote the threshold voltage degradation due to DLHTs in the 13 atomic % and 6 atomic % devices respectively, both subjected to stress duration of 2×10^4 s.

4.5 Comparison of DPN-conditioned p-MOSFETs and n-MOSFETs

To confirm the dependency of the time exponent on DLHTs, n-MOSFETs with similar DPN process condition were subjected to NBTI stress, to yield comparable $|\Delta N_{it}^{CP}|$ with the p-MOSFET (inset of Figure 4.5). For the n-MOSFET, this was achieved at the same temperature but at higher magnitude of negative gate bias, in order to account for the difference in flatband voltage in the n-channel device. Post-stress I_d - V_g measurements were carried out with positive gate bias sweep in order to bring the device to inversion region, hence stress generated DHLTs would be neutralized, and the resultant threshold

voltage shift would be due to the sum of interface states measured by CP method and interface states not measurable by CP method.

Compared to p-channel device, ΔV_t in the n-MOSFET is positive, since those interface states probed by I_d - V_g measurement exhibit acceptor-like characteristics. As shown in Figure 4.5, the exponent n is relatively large for the n-channel case, at around 0.47, compared to the time exponent of 0.18 for p-channel device. As the ΔN_{it} for the p-MOSFET and n-MOSFET are both similar, the lower exponent for the former is due to rapid hole trapping at deep-level defect states. As the energy states for these DLHTs are located outside the energy window of electron tunneling, they remain present when the stress bias was removed, unlike shallow hole traps. Therefore, DLHTs are responsible for the additional threshold voltage degradation, hence decreasing the exponent value.

Figure 4.5 Power-law time dependence of NBTI induced threshold voltage shift of p- and n-MOSFET with DPN gate dielectric. Applied electric field stress was kept constant for both devices. The p-MOSFET was stressed at -2.2 V, 100 °C. The n-MOSFET was stressed at the same temperature but at a more negative gate voltage (-2.6 V) in order to achieve similar interface state generation as the p-MOSFET.

At this stage, the nature of these DLHTs remains relatively unknown. Simulation results have shown that H^+ near the Si interface could have introduced hole traps near/ or above the conduction band of Si [87], while Campbell and Lenahan's work suggested that NBTI stressing of oxynitrided devices created k_N centres (related to nitrogen trap precursors) which resulted in hole traps [88]. Through the use of electron spin resonance (ESR) and spin-dependent recombination (SDR), they noted that the k_N defect has density of states that differ greatly from the P_{b0}/P_{b1} defects in SiO_2 -based devices. While the SiO_2 -based P_{b0}/P_{b1} defects were found to have relatively constant density

of states, the k_N centre defects had a much narrower distribution in energy level. In addition, the authors found that NBTI preferentially generated k_N defects compared to P_{b0}/P_{b1} defects in DPN-gate devices. They suggested that the difference in bonding at the dielectric interface was due to the presence of nitrogen near the interface, hence favouring the formation of k_N defects over P_{b0}/P_{b1} defects.

In addition, DLHTs were known to be mostly found near the conduction band edge, as opposed to being distributed over a wide range in the energy bandgap. This is similar to the known energy distribution of k_N centres as well, as highlighted by Campbell. Moreover, DPN-gate n-MOSFETs showed a much larger increase in the time exponent upon the neutralization of DLHTs. With the removal of DLHTs causing increased ΔV_t from interface states (time exponent rose to 0.5) in the n-MOSFET, this also reinforced the point highlighted by Campbell that k_N centres were generated preferentially over the P_{b0}/P_{b1} defects responsible for interface traps.

4.6 Role of Interface States not Captured by Charge Pumping

Method

Another interesting observation should be noted in Figure 4.5. The exponent shown for ΔN_{it}^{CP} (and hence threshold voltage shift due to interface states, measurable by CP method, ΔV_{it}^{CP}) is approximately 0.27, which is higher than the exponent measured in the p-MOSFET $|\Delta V_t|$ (at 0.18). This could be explained by the recovery of DLHTs as the gate bias is subjected to alternate negative and positive polarity during charge pumping, after

performing I_d - V_g measurements. $\Delta V_{t,p-MOSFET}$ may be summarised by $\Delta V_{t,p-MOSFET} = \Delta V_{it}^{CP} + \Delta V_{it}^{>E_g/2} + \Delta V_t^{DLHT}$, where $\Delta V_{it}^{>E_g/2}$ is the threshold voltage shift from the interface face traps at the upper half of the Si bandgap.

However, this recovery explanation does not justify the observations in the n-MOSFET. In this case, the time exponent n obtained from n-MOSFET CP measurements was lower than that obtained from I_d - V_g measurements (0.27 versus 0.47). Positive gate bias was applied during I_d - V_g sweeps in the n-MOSFET, which means all the DLHTs would have recovered before doing CP measurements. The threshold voltage shift in the n-MOSFET may then be summarised as $\Delta V_{t,n-MOSFET} = \Delta V_{it}^{CP} + \Delta V_{it}^{>E_g/2}$ ($>E_g/2$ denotes upper half of the Si bandgap). In addition, in the absence of DLHTs, the total threshold voltage shift, contributed by both interface states measurable by the CP method and those outside the energy range probed by CP method, was actually lower than that of ΔV_{it}^{CP} for the n-MOSFET, during the first 10^3 s of the stress duration. On the other hand, after DLHTs are annealed in the p-MOSFET during CP measurements, ΔV_{it}^{CP} remains consistently lower than $\Delta V_{t,p-MOSFET}$ before using CP method, over the stress duration tested.

The discrepancies observed in the n-MOSFET may be explained in two ways. Firstly, while DLHTs are significantly reduced when positive gate bias was applied, some of the DLHTs reappeared after the positive gate bias was removed during charge pumping. It is possible that these DLHTs were electrically neutralized by electrons from the inversion layer during the positive gate biasing, and were discharged as CP current during the CP negative/positive gate cycling. Results from Lelis [89] had shown that an E' centre demonstrates some of the properties inferred for this type of DLHT. An

E' centre is formed when a strained Si-Si bond traps an external hole and becomes two trivalent Si atom, one of the Si atom holding the trapped hole, the other Si atom with an unpaired electron. In the presence of positive bias, the E' centre could take in an electron, together with a hole that it has taken in earlier, to become neutral. The taking in of electrons by DLHTs and rendering them inactive supports the results of a lower $|\Delta V_t|$ shift for the n-MOSFET, as no component is contributed by these neutralised DLHTs.

Secondly, it should be noted that the threshold voltage shift in the p-MOSFET is due to the build-up of positive charges in the gate oxide. In contrast, ΔV_t shift in the n-channel device is due to the build-up of negative charges. In this case, let's assume that all the DLHTs were discharged when a positive gate bias was applied, leaving only stress-induced interface traps responsible for the threshold voltage degradation. As Figure 4.5 inset shows that the ΔV_{it}^{CP} (as measured during charge pumping and plotted as ΔN_{it}^{CP} against time) increases over the stress duration, it suggests that the lower overall threshold voltage shift is due to interface traps from the upper half of the bandgap. A decrease in the physical quantity of the interface traps density would have put the ΔV_t shift in the n-MOSFET to be in line with the ΔV_{it}^{CP} plot, and lower than it. Hence, a more likely explanation is that these stress-induced interface traps from the upper half of the bandgap is positively charged, hence lowering the effective negative charge in the gate dielectric, causing the threshold voltage shift to appear lower.

Classical understanding was that these interfacial traps, which lie outside the energy window probed by the CP method ($\sim 0.35\text{eV}$ at 100°C), exhibits acceptor-like nature (accepts electrons and becomes negatively

charged). However, it may be inferred that these interfacial trapped charge is positively charged (hence donor-like properties), lowering the net threshold voltage shift during the early stress duration, before the overall gate oxide gained more negative charges subsequently. The nature of these interfacial traps that showed lower ΔV_t than ΔV_{it}^{CP} in n-MOSFET is still not well understood here. More discussions about these interfacial traps and their demonstration of both donor-like and acceptor-like (hence bipolar) characteristics would be made in Chapter 5.

4.7 Summary

Experimental results have presented that DLHT generation is significant in both TNO-gate and DPN-gate p-MOSFETs. By comparing data obtained from static NBTI with bipolar NBTI stress, the presence of DLHTs lowered the measured value of the power-law time exponent (0.16 with DLHTs; 0.3 with most of the DLHTs removed) on TNO-gate devices. While DPN-gate p-MOSFETs did not show as significant difference in the exponent value, DPN-gate n-MOSFETs registered a larger time exponent value (~0.4-0.5) was observed in this work after removing DLHTs components from stress-induced interface states. The results from both p-channel and n-channel devices has significant implication that reported n values of 0.14-0.17, used to support molecular H_2 as the main diffusion species in the R-D model, may not be entirely accurate. In addition, the nature of interfacial traps generated in the n-MOSFET, outside the energy range probed by the CP method, has not been well understood, and would be investigated next.

Chapter 5 BIPOLAR NATURE OF STRESS-INDUCED INTERFACE STATES IN UPPER HALF OF SI BANDGAP

5.1 Introduction

In the preceding chapter, the use of bipolar stress during Negative-Bias Temperature Instability (NBTI) on n-MOSFETs highlighted the impact of deep-level hole traps on the time exponent. It has also demonstrated on how interface states in the upper midgap of Si could be characterized. An issue raised earlier was the lowering of the overall threshold voltage shift by these upper Si bandgap interfacial trapped charges ($\Delta N_{it}^{>E_g/2}$), compared to the stress-induced interface trap density measured using charge pumping (CP), denoted as ΔN_{it}^{CP} . This suggested that $\Delta N_{it}^{>E_g/2}$ are donor-like (positively charged), so that it reduces the overall negative charge within the gate oxide. In contrast, classical theory attributed NBTI in p-MOSFET to the generation of donor-like interface states in the lower half of the bandgap (donate electrons and become positive trapped charges when pulled up above the Fermi level E_F in the presence of negative gate bias), and generation of acceptor-like interface states in upper half of the bandgap in n-MOSFET, according to studies done by Saminadayar [28] and Schroder [30].

In this chapter, further investigations were carried out to understand the nature of these stress induced interfacial states residing at the upper half of the bandgap. The threshold voltage degradation of the n-MOSFET (ΔV_t^n) and its subthreshold swing characteristic during NBTI were examined. Results

indicated that interfacial traps exhibited bipolar characteristics, i.e. these interface states are both acceptor-like and donor-like. Using subthreshold swing degradation to determine the change in the interfacial trapped charge, it was found that the interface states density measured by the subthreshold swing method (ΔN_{it}^{SS}) for the n-MOSFET is consistently doubled of that for the p-MOSFET. When comparing the ratio of ΔN_{it}^{SS} to that of the physical interfacial trap density measured in both devices (ΔN_{it}^{CP}), both methods measuring traps from the same energy range, the ratio is consistently 2 as well. This suggests the same type of traps having two charge state transitions, i.e. from positive to neutral, and from neutral to negative. Since the interface traps measured by charge pumping were kept nearly the same in both p-MOSFET and n-MOSFET, this means that the charge change would have to come from the interfacial trapped charge above the Si midgap. These traps exhibited bipolar nature, and the findings challenge previous understanding that stress induced interface states are donor-like only.

5.2 Experimental Setup

Several experimental parameters were carefully controlled to ensure a fair comparison. Firstly, n-MOSFETs and p-MOSFETs tested were from the same wafer, hence devices were made under the same processing conditions. This ensures identical interface trap properties. Secondly, the negative gate stress voltage applied (V_g^{stress}) on the n-MOSFET was adjusted to obtain comparable ΔN_{it}^{CP} for both types of devices. As the flat band and threshold voltages were comparable for both p- and n-MOSFETs, similar energy ranges

were probed during charge pumping (CP) measurements. As a result, the similar stress-induced ΔN_{it}^{CP} meant that the physical density of interfacial traps were comparable in both devices. Thirdly, the $\Delta V_t^p - \Delta N_{it}^{CP}$ relationship used in p-MOSFET, which was used as the reference for comparison with $\Delta V_t^n - \Delta N_{it}^{CP}$ in n-MOSFET, was carried out on bipolar stress. As stated in Section 4.4, the positive gate bias removes contributions from deep-level hole traps in the p-MOSFET, so that during the $I_d - V_g$ sweep in negative gate bias at the lower mid-gap, the threshold voltage shift from the upper mid-gap interfacial charges could then be characterized. On the other hand, the n-channel devices conduct $I_d - V_g$ measurements with positive gate voltage, sweeping the upper half of the bandgap. Hence this would ensure that both types of devices are measuring ΔV_t coming from interface states only, without the interference of DLHTs.

The experimental setup is given as follows. Dual-gate p-channel and n-channel MOSFET devices were used, with channel length and width at 65nm and 10 μ m respectively. The device's steam generated gate oxide has a thickness of 13 Å and is exposed to remote nitrogen plasma. Peak nitrogen concentration is approximately 13.5 atomic %, resulting in an equivalent oxide thickness (EOT) of 15 Å. NBTI stressing for both n-channel and p-channel devices were carried out at 100°C under comparable electric field strength. Interface states generated during NBTI stressing were determined using the subthreshold swing method (ΔSS method, extracted from the DC $I_d - V_g$ measurements) to obtain ΔN_{it}^{SS} , followed by the charge-pumping (CP) method to determine ΔN_{it}^{CP} . CP measurements were obtained using a 1 MHz, ± 1 V gate pulse with 40ns transistion time. DC $I_d - V_g$ measurements probe the lower / upper midgap of p-MOSFETs / n-MOSFETs respectively, and the ΔV_t

obtained was determined from a constant subthreshold drain current $I_{d,sub}$. As shown in [19], the energy range probed by both ΔSS and CP methods were within the same energy window ΔE , approximately 0.33eV at 100°C. This earlier paper has also demonstrated that doing I_d - V_g first before CP or vice-versa has no material impact to the results, hence providing a strong basis for adaptation into this work.

5.3 Positive and Negative Interfacial Charge Occurring

Concurrently

Measurements from the n-MOSFETs showed that the threshold voltage shift ΔV_t^n is positive, suggesting a negative interfacial trapped charge. This observation is expected, since it is widely-known that interface states above the mid-gap are acceptor-like. However, data extracted from the p-MOSFET earlier indicated that interfacial trapped charge was distributed over a wide energy range, extending into the upper mid-gap as well [30]. Hence the ability of these interfacial charges to become both positive and negative suggest that interface states in the upper half of the bandgap are bipolar in nature, i.e. they could be both acceptor-like and donor-like.

Figure 5.1 plots the relationship between the extracted ΔV_t and ΔN_{it}^{CP} , for both p-channel and n-channel devices (shown as ΔV_t^n , $\Delta N_{it}^{CP,n}$ and ΔV_t^p , $\Delta N_{it}^{CP,p}$ respectively). The increasing trend in ΔV_t^n is observed to be correlated to that of ΔV_t^p , suggesting that the negative and positive interfacial trapped charge is of the same physical origin. The next observation of importance is that for the n-MOSFET, by increasing the reference current during the ΔV_t

extraction (see constant current method, section 3.1), the $\Delta V_t^n - \Delta N_{it}^{CP}$ relationship would shift towards the one obtained for the p-MOSFET subjected to bipolar stress (shown as dashed line). This result means that for the same ΔN_{it}^{CP} measured in the n-MOSFET, the threshold voltage shift ΔV_t^n increased and became more positive at $I_{d,sub}$ of 100 μA than 10 μA , for the same stress condition. In contrast, the threshold voltage shift in the p-MOSFET, ΔV_t^p , was found to be comparable within the same range of $I_{d,sub}$ used, as shown by the near parallel shift of the $I_d - V_g$ curves at those current levels in Figure 5.3.

Figure 5.1 Variations of threshold voltage shift ΔV_t , obtained from different $I_{d,sub}$, to ΔN_{it}^{CP} ($= \Delta I_{cp}/qAf$), determined from charge pumping (CP) current measurement. The dashed line represents $|\Delta V_t^p|$ versus ΔN_{it}^{CP} characteristic of the p-MOSFET.

The explanation for why the $\Delta V_t^n - \Delta N_{it}^{CP}$ plot for p-MOSFET does not change with increasing subthreshold drain current but changes for n-MOSFET is as follows. For the p-MOSFET, when $I_{d,sub}$ of 10 μA is used, the energy band diagram is shown in Figure 5.2b(i). The shaded region indicates the interfacial states that could not be detected within the energy window of the $I_d - V_g$ sweep, and in turn, also not detectable from the subthreshold swing degradation. When a higher $I_{d,sub}$ (100 μA) is used, illustrated in Figure

5.2b(ii), the intrinsic Fermi level is pulled up such that the intrinsic Fermi level E_i is above the shaded region. However, these interfacial trapped charges are still above the Fermi level E_F , and hence still do not contribute to subthreshold swing degradation. In turn, the $\Delta V_t^p - \Delta N_{it}^{CP}$ relationship does not change much for the p-channel devices.

The increase in ΔV_t^n may be explained as follows. At a lower $I_{d,sub}$ used (Figure 5.2a(i)), only a fraction of the interface states in the upper midgap fall below the Fermi level E_F and are negatively charged. The remaining positive trap charge offsets part of the negative interfacial charge, causing the magnitude of ΔV_t^n to be less than that of ΔV_t^p . At higher $I_{d,sub}$ (Figure 5.2a(ii)), the Si surface band bending increased, pulling more interface trap states (denoted by grey area) to fall below E_F to become negatively charged. This leaves less positively charged interfacial trapped charge in the upper midgap, leading to higher ΔV_t^n (from higher overall negative charge) at a given ΔN_{it}^{CP} .

Figure 5.2(a)

Figure 5.2(b)

Figure 5.2 Energy band diagrams of the Si/SiO₂ interfacial region for (a) n-MOSFET and (b) p-MOSFET. For both devices, (i) schematics when $I_{d,sub} = 10 \mu A$ is used for constant current extraction, and shaded/grey region refers to interfacial states that were not detected by subthreshold swing degradation. (ii) band diagram when $I_{d,sub} = 100 \mu A$ is used for constant current extraction, E_i is pulled up compared to its previous level in (i), and shaded/grey region refers to interfacial states that is now detected by subthreshold swing degradation. For p-MOSFET, interfacial charge in shaded region does not change (remain donor-like) with higher $I_{d,sub}$, hence no change to subthreshold swing degradation; For n-MOSFET, interfacial charge changes from positive to negative with higher $I_{d,sub}$, hence observable subthreshold swing degradation.

5.4 Subthreshold I_d - V_g Characteristics in p-MOSFET and n-MOSFET

The significant difference of ΔV_t^n with respect to $I_{d,sub}$ warranted for an investigation to cover a wider range of the I_d - V_g subthreshold region, for both p- and n-channel devices. While stress conditions were ensured to give similar stress-induced interface trap density, the subthreshold swing degradations turned out to be very different, as shown in Figure 5.3. It should be noted that the CP method and subthreshold swing method measure interface traps within the same energy range, as shown in Section 3.4 and in [19]. For the p-MOSFET, the shift from the pre- to post-stress I_d - V_g curve is nearly parallel, resulting in relatively small subthreshold swing degradation, seen in Figure 5.3(a). On the other hand, for the n-MOSFET in Figure 5.3(b), the post stress I_d - V_g curve is clearly sheared from the pre stress curve towards the direction of the positive gate voltage, resulting in higher subthreshold swing degradation. From equation (3.3), this in turn results in a larger stress-induced interfacial trap density (ΔN_{it}^{SS}) in the n-channel device. This is in conflict from earlier inference that the same ΔN_{it}^{CP} should correspond to similar stress induced interface trap density.

Figure 5.3 Subthreshold I_d - V_g characteristics of (a) p-MOSFET and (b) n-MOSFET. Both devices were stressed to yield similar ΔN_{it}^{CP} (stress induced interface trap density measured by the charge pumping method).

To investigate this difference further, ΔN_{it}^{SS} extracted from the subthreshold swing degradation of the p- and n-MOSFETs were compared, as illustrated in Figure 5.4. It was observed that ΔN_{it}^{SS} for the n-MOSFETs were consistently doubled of that for the p-MOSFETs over the stress duration. In Figure 5.4(b), the ratios of $\Delta N_{it}^{SS}/\Delta N_{it}^{CP}$ for the n- and p-channel devices were compared over a broad range of stress gate voltage V_{gs} . According to (3.3), ΔN_{it}^{SS} is obtained from ΔC_{it} , which is due to the charging up of interface states during I_d - V_g sweep. In p-MOSFET, the stress-induced interface states across the whole energy range are expected to be donor-like (positively charged only), and hence associated +1 charge for every interface trap generated. As such, the ratio of $\Delta N_{it}^{SS}/\Delta N_{it}^{CP}$ is approximately 1. With every trap generated contributing to only one charge change, this shows that the interfacial trap states in the lower half of the bandgap is unipolar, i.e. only undergo single charge transition from neutral to positive.

Figure 5.4 (a) Comparison of stress generated interface trap density ΔN_{it}^{SS} (determined by subthreshold swing degradation) of the n- and p-MOSFET. (b) ΔN_{it}^{SS} of the n-MOSFET is consistently doubled that of the p-MOSFET. All devices were stressed to induce comparable ΔN_{it}^{CP} (interface trap density extracted by the charge pumping method).

On the other hand, the ratio obtained for the n-MOSFETs were from those interfacial trap states in the upper-midgap. If the interface states generated throughout the bandgap during NBTI stress were acceptor-like, the ratio of $\Delta N_{it}^{SS} / \Delta N_{it}^{CP}$ is expected to be one as well. However, the ratio of 2 was obtained experimentally. As the subthreshold swing degradation captures the change in the interfacial trapped charge within the given energy window during I_d - V_g sweep, this would mean that some of the interfacial trapped charge pulled down to below the Fermi level experienced two charge transitions – first from positive to neutral, and then neutral to negative. Hence, ΔN_{it}^{SS} would appear to be doubled that of the increase in physical trap density. This is consistent with the bipolar nature of the interfacial trap charge in the upper half of the bandgap. The constant ratio of 2 also implies that the same type of trap states is involved in the transition, and not due to the compensation of negative and positive

trapped charges from different sources. For unipolar trap states, they only involve one charge state transition (neutral to negative or neutral to positive).

5.5 E' Centres – Possible Source of Bipolar Nature

At this point, the difference in the electrical behaviour of the interfacial trapped states at the lower midgap and upper midgap is unclear. In Section 4.6, it was raised that some of the DLHTs reappearing after a change in the gate polarity might be responsible, but was also mentioned that since DLHTs should anneal in the presence of a positive gate bias, the remaining traps measured contributing to ΔV_t should be interface states only. This uncertainty in the nature of the interfacial trapped charge may be resolved if E' centres were responsible for the bipolar nature in these interfacial states. Figure 5.5 illustrates the trapping/detrapping process of an E' centre in the presence of a hole. It was observed by Lenahan and Dressendorfer [22] that oxygen vacancies near the Si/SiO₂ interface lead to strained Si-Si bonds. When a strained bond is attacked by a hole, it causes bond breaking and the hole to be trapped in one of the Si atoms, causing the Si atom to be positively charged. The other Si atom has one unpaired electron in its dangling orbital, but remains neutral. Thus, these two trivalent Si atoms form an E' centre.

Figure 5.5 Model of E' centre before Si-Si bond dissociation, and after it trapped a hole in one of the Si atoms, with an unpaired electron in another Si atom [23]. Shaded atoms denote oxygen atoms, while unshaded atoms represent silicon atoms.

During NBTI stressing of n-MOSFET, the negative gate bias puts the device into accumulation, attracting holes at the Si/SiO₂ interface. These holes were then able to attack strained Si-Si bonds, resulting in hole trapping and the formation of E' centres. While E' centres could also be described as hole traps, it may also be formed near the Si/SiO₂ interface as well, and these hole traps do not anneal/recover once the stress voltage is removed. These interfacial trapped charge hence exhibit some of the properties of DLHTs by not recovering on the removal of stress bias, and are located near the interface, hence referred to as the interfacial trapped charge. After the removal of stress, and I_d - V_g measurements were carried out by applying positive gate bias, electrons from the channel would have tunnelled back into the oxide, and resided with the Si atom that had gained a hole. This would cause the E' centre

to appear to be neutral, but in fact, had both the hole and electron with it. As more surface bending occurs further at higher $I_{d,sub}$, more of these E' centres were shifted from above the Fermi level E_F to below it. An additional electron is now able to attach to the 2nd Si atom's dangling orbital with the unpaired electron, hence the E' centre transits from neutral to negative. Ab-initio simulation shows that the negative state is stable, and could explain the bipolar nature of interfacial states observed [90].

This bipolar nature of interfacial trapped charge could now explain the observation in Figure 4.5, where threshold voltage degradation by the n-MOSFET (ΔV_t) was lower than that of the V_t shift from interface states, measured by the charge pumping method, when the stress duration was less than 10^3 seconds. During NBTI of the n-MOSFET, both donor-like and acceptor-like interfacial trapped charges were generated in the upper midgap, the former due to hole trapping during the formation of E' centres. The presence of both positive and negative charges for the interfacial trapped charges caused the overall threshold voltage to be less positive. As the stress duration increases, the E' centres took more electrons, first for dangling orbital and together with the trapped holes, appeared to be electrically neutral. Subsequently, they took more electrons and became negatively charged, causing the threshold voltage shift to increase positively. Hence, the preferential formation of E' centres (Section 4.6) over interface states with P_b centre (Section 2.1), could explain some of the observations not predicted by the Reaction-Diffusion model for NBTI in p-MOSFET, such as enhanced recovery on the application of positive gate bias.

5.6 Summary

The use of bipolar NBTI stress on p-MOSFETs indicated the presence of donor-like stress-induced interfacial trapped charge in the upper half of the bandgap. However, the use of static NBTI stress on n-MOSFETs, conditioned to give comparable physical density of interfacial traps in both devices, was expected to remove DLHTs during the subsequent positive gate bias for I_d - V_g sweep. Some of the stress-induced interfacial trapped charge was found to be donor-like, instead of acceptor-like as predicted by theory. This suggested that interfacial trapped charge could exhibit bipolar nature. Further analysis showed that the subthreshold swing degradation in n-MOSFETs is consistently doubled of that in the p-MOSFETs, and the $\Delta N_{it}^{SS}/\Delta N_{it}^{CP}$ ratios are approximately 2 and 1 respectively, over the range of gate stress voltage applied. The p-MOSFET results demonstrated that for an increase in the physical trap density during the applied NBTI stress (ΔN_{it}^{CP}), the trapped charge is increased at the same rate (ΔN_{it}^{SS}). This further proves that interfacial trapped charge at the lower midgap is donor-like only, with one charge transition from neutral to positive.

On the other hand, the n-MOSFET results illustrated that for the same physical trap density generated, the corresponding trapped charge is doubled. For these interfacial states in the upper midgap to do so, the physical traps would have to undergo two charge transitions during the positive gate I_d - V_g measurements – from positive to neutral, and then from neutral to negative. It was suggested that these transitions were possible if the interface states in

upper half of the bandgap consisted of E' centres. During NBTI stress, each centre consisted of two trivalent Si atoms, one of them with a trapped hole and the other with an unpaired electron in its dangling orbital. This hole trapping caused the trap to be donor-like. After the removal of the stress bias and positive gate bias was applied during measurement, the first Si atom accepted an electron together with its trapped hole, causing charge transition to neutral. When more surface bending led to some of the E' centres to be below E_F , the other Si atom accepts another electron to transit the charge from neutral to negative. This would result in the inferred interfacial trapped charge being doubled to the increase in physical trap density. The demonstration of hole-trap mechanism in this deep-level interfacial trapped charge could help explain some of the observations not predicted by the R-D model for a NBTI-stressed p-MOSFET.

Chapter 6 NBTI CHARACTERIZATION VIA FLICKER NOISE MEASUREMENTS

6.1 Introduction

The use of flicker noise measurement to characterize oxide traps in semiconductor physics have been carried out since 1957 [51]. However, few studies have used flicker noise to characterize oxide traps generated during NBTI. In this work, $1/f$ noise results taken before and after NBTI are presented. Apart from comparing different stress conditions on the same type of devices, fluorinated devices were compared with baseline counterparts to investigate the impact of reduced N_{it} component would have on flicker noise.

The results show that:

1. Variation in the slope of the noise spectrum:
 - a. It was observed that the slope of the measured noise spectrum consistently increased (in magnitude) for thick gate (Equivalent oxide thickness, $EOT = 45 \text{ \AA}$) devices, compared to the thin gate ($EOT = 20 \text{ \AA}$) devices. This implies that not only interface traps were responsible for NBTI, as suggested in the R-D model, but oxide traps are found in the gate dielectric, at some distance away from the gate oxide-substrate interface. This is also in contradiction with a study demonstrating that flicker noise slope in thin gate oxide of comparable thickness could be measured accurately.

- b. Investigation on the thick gate oxide over the stress duration showed that the magnitude of the slope gradient varies in a near logarithmic function. This suggested that the oxide traps probed by flicker noise contribute partly to the permanent degradation of the threshold voltage.
2. Oxide trap density derived from noise measurement:
- a. Trap density results derived from noise measurement was found to be higher than those measured from NBTI DC characterization. This was attributed to the possibility that neutral traps were generated during NBTI in the region scanned, but could not be observed from threshold voltage degradation.

6.2 Validation of In-house Noise Setup

As described in Section 3.6.2, one key advantage of the in-house noise measurement setup was the use of much lower voltage through the use of pre-amplifiers. In this section, key parameters formulating the current flicker noise theory would be measured by this setup, with comparisons made to existing works whenever possible, in order to validate its accuracy. It should be noted that the scope of the noise measurement is kept to the p-MOSFET operating in the linear region. This is to ensure consistency with the NBTI measurements, which were done using the DC method.

One of the key considerations in deciding for an accurate noise measurement setup would be its ability to minimize background noise while

flicker noise readings are captured. Figure 6.1 shows the magnitude of the measured drain current noise spectrum, measured in units of V^2/Hz , relative to the background noise. The background noise was measured by applying the same gate voltage ($V_g = -1.2\text{V}$ in this case), but kept the drain voltage V_d to 0V . When a potential difference is applied between the drain and the source terminals, the drain current noise spectrum could then be measured. Hence, it could be observed that within the range of frequencies used to capture flicker noise (1Hz to 10kHz), the background noise is about 5 to 8 orders lower than the measured spectrum. Hence, in future noise measurement readings, the background noise has taken into account and would have no material impact on the accuracy.

Figure 6.1 Comparison of measured noise spectrum relative to an ideal noise slope of -1 (represented by straight line), and the relative magnitude of the background noise

As shown in Figure 6.1, the slope of the measured noise spectrum is then compared with the ideal $1/f$ slope trend line. If oxide trap density is uniform, it would be exactly at -1, but in most case, any slope values that fall between -0.8 and -1.2 could be considered to be caused by flicker noise mechanisms as well.

The next step would be to reproduce the key findings from the flicker noise theory. It has been reported in some papers [91-92] that the p-MOSFET has different flicker noise mechanisms, depending on whether they are operating in weak or strong inversion regions. Under weak inversion, the drain current noise is expected to be ΔN -dominant, while it was shown to follow closely to the correlated $(\Delta N - \Delta \mu)$ model in the latter. Based on the widely accepted ΔN framework proposed by Reimbold [57], which covers the linear region, the resulting normalized drain current noise power spectral density is given by equation 2.19.

Under weak inversion, where $|\beta Q_n| < C_{ox} + C_d + C_{it}$, Eq. 2.19 predicts a near constant normalized noise power at small drain current I_D . The result obtained in this experiment was able to show this as well, as seen in Figure 6.2. As the pure mobility noise model predicted a strong increase in noise during weak inversion, this result is one of the supporting evidence for numbers fluctuation in the noise theory. As for the deviation in the relationship using high drain current (in linear region), this would be investigated using Hung's $\Delta N - \Delta \mu$ model.

Figure 6.2 Comparison of slopes of (S_{Id} / I_D^2) with $(G_m / I_D)^2$ with a fresh device, to confirm numbers fluctuation dominance under weak inversion before NBTI ($f = 20$ Hz)

Under strong inversion, the correlated mobility model predicts a quadratic relations between the gate referred input noise S_{V_g} ($S_{V_g} = S_{Id} / G_m^2$) and the gate overdrive $|V_{gs} - V_{th}|$, as shown in equation 2.27. The results obtained in figure shown a good quadratic fit of the noise-gate voltage plot, and the values are found to be within the same orders as results obtained by [24], another of the few works covering flicker noise with NBTI. Notice that as the gate voltage applied becomes closer to the threshold voltage, i.e. $|V_{gs} - V_{th}| \rightarrow 0+$, S_{V_g} flattens out to a near-constant plateau. In the correlated noise model, it is expected to attain a constant value known as flat-band voltage noise spectral density, as shown in Eq. 2.28. This value would play an important role in determining the oxide trap density in the next section.

Figure 6.3 Consistency of input referred noise to the correlated mobility model ($f = 20$ Hz), as seen from quadratic relationship under strong inversion

6.3 Flicker Noise Results Before and After NBTI Stress

In this section, flicker noise results of the NBTI-stressed DUTs would be discussed. Unless otherwise stated, the nominal NBTI stress conditions used on the devices under test (DUTs) are gate oxide field stress of 8 MV/cm, at 100°C temperature over stress duration of 7000 seconds. The magnitude of the threshold voltage degradation was measured using the stress-measure-stress method described in Section 3.2. Flicker noise measurements are taken from the fresh and stressed device samples, and then quantitatively resolved into key components – variations in the slope of the noise spectrum, and the implied oxide trap density.

6.3.1 Variation in the slope of the noise spectrum

Figure 6.4 shows the pre- and post- stress input referred noise (S_{Vg}) against the gate overdrive ($|V_{gs}-V_{th}|$) at a given frequency. S_{Vg} increases with $|V_{gs}-V_{th}|$ indicate trap generated during NBTI that were picked up by the flicker noise readings, via the mechanisms described in the correlated mobility model.

Figure 6.4 Input referred noise against gate overdrive before and after stress. Noise measurement was carried out at low frequency region ($f = 20$ Hz). The gate oxide field stress applied was 8 MV/cm, at 100°C temperature over stress duration of 7000 seconds.

The above gate referred noise was converted to the normalised drain current noise power spectral density and were plotted against frequency, as shown in Figure 6.5. The drain current noise power was used so that the change in drain current magnitude during NBTI would be taken into account.

It is shown that there is a distinct increase in the drain current noise after NBTI stressing.

Figure 6.5 Normalised drain current spectral density versus frequency before and after stress, at strong inversion. Measurements were taken from a thin gate oxide device (20 Å).

Figure 6.6(a) shows the range of values obtained for the spectrum slopes, for the thin gate oxide (TN) and thick gate oxide devices (TK) used. The range is defined by a maximum and minimum value of the slope measured for the DUTs, and the median value is taken as reference. TN has an EOT of ~ 20 Å while TK has an EOT of ~ 45 Å. Measurements were extracted from four TN-gate and four TK-gate devices, built on the same wafer and from similar fabrication process, and the maxima, minima and average values were presented to illustrate the distribute of the values obtained. It was observed from the data that TK-gate devices consistently show an increase in the slope magnitude when measurements were taken after NBTI. However, the

spectrum slope on TN-gate devices showed little change when measured before and after NBTI.

It was suspected that the stress might be insufficient for distinct trap distribution to be observed in the TN-gate device. Hence, a higher electric field stress (12 MV/cm) was applied across the gate oxide to increase the threshold voltage degradation, so as to increase the number of traps in the oxide. The temperature and stress duration remained at 100°C and 7000 seconds respectively. As shown in Figure 6.6(b), the TK-gate devices continued to show consistent increase in slope magnitude after NBTI, while the flicker noise slopes on TN-gate devices did not show any appreciable difference.

Figure 6.6(a) Spectrum slope of thick and thin gate devices (45 Å versus 20 Å) before and after NBTI stress. Gate voltage was adjusted to produce similar oxide field stress at 8MV/cm. Slope distribution shown from 7 similarly processed p-MOSFETs. Slope median was found to have increased after NBTI for TK gate, but not TN gate.

Figure 6.6(b) Spectrum slope of thick and thin gate devices (45 Å versus 20 Å) before and after NBTI stress. A higher oxide field stress was applied (12MV/cm) compared to 6.6(a) to investigate if higher electric field would affect the trap distribution in thin gate devices.

As the flicker noise gradients measured from TK-gate devices were found to respond consistently to NBTI stress, the next step was to investigate how the noise slope varies over the NBTI stress duration. To determine this, an additional step was carried out at the stress-measure-stress method described in Section 3.2. After the I_d - V_g sweep, flicker noise measurement was carried out to obtain spectral information at this point in time of the stress duration. Following this, stress is resumed and would be followed by stress interruption, I_d - V_g sweep and then flicker noise measurement again. Since the DUT remains at negative-bias during the extraction of the noise readings, the threshold voltage degradation responsible for causing permanent degradation is not expected to recover significantly with this additional step.

Figure 6.7 shows that the magnitude of the spectrum gradient increased over the duration of the NBTI stress. An increase in the slope value indicates an increase in the oxide trap distribution further from the gate oxide/substrate boundary. Hence it could be inferred that during NBTI, oxide traps are also generated near the valence band region at some distance from the interface, which corresponds to the energy window that could be probed by flicker noise measurement. These traps do not recover upon the stress interruption, allowing the gradient magnitude to increase gradually over the stress period.

Figure 6.7 Spectrum slope of thick gate devices measured over NBTI stress duration of 7000 seconds, at applied electric field of 12MV/cm. As slope magnitude increases, this also means more oxide traps generated at some distance away from the interface.

As discussed in the literature review (Section 2.4.5), the noise slope could be used as a parameter for determining trap distribution [52]. A slope magnitude, $|\gamma|$, of 1 represents an uniform trap distribution within the gate oxide. When there are more oxide traps closer to the interface, channel charges would be able to be trapped and detrapped through these traps at shorter time,

i.e. the trap-detrap process occurs at higher frequencies. This would correspond to a higher spectral noise power at the higher frequency range during flicker noise measurements relative to the lower frequency region. Therefore, the slope of the spectrum would be less steep, or the slope magnitude is less than 1. Conversely, higher trap distribution further away from the gate dielectric/substrate interface would increase the slope magnitude, i.e. $|\gamma| > 1$.

The results obtained in Figures 6.6(a) and (b) contradict the findings made by Kepila *et al.*, which also used devices with gate oxide thickness of $\sim 20 \text{ \AA}$ as well, but were able to obtain unambiguous difference in the slope magnitude before and after NBTI. On the other hand, the experiments carried out in this work did not show such distinct differences at this oxide thickness. With reference to equation 2.16, the extraction frequency was at around 15 Hz, which would correspond to approximately $20 \text{ \AA}$. For the oxide thickness of $20 \text{ \AA}$ used, this is extremely close to the polysilicon-gate oxide interface. Given that the variations around this boundary is just atomic lengths apart, it is very likely that the noise measured probed in the TN-gate devices for this work is actually some region into the polysilicon itself, hence the oxide trap distribution could not be determined. On the other hand, for the TK-gate devices, a mean of $20 \text{ \AA}$ in a device with oxide thickness of around $45 \text{ \AA}$, there is more likelihood for the inversion charges to still trap-detrap within the gate oxide. Hence, when oxide traps are generated during NBTI and lie in the energy range probed by flicker noise, the slope change is consistently reproduced.

6.3.2 Oxide Trap Density Derived from Noise Measurement

From the previous section, the use of the flicker noise spectrum gradient could be used to characterize trap distribution in the gate oxide of the p-MOSFET. In this section, this work would like to extend this finding further and attempt to extract the oxide trap density measured from flicker noise. The calculation of the oxide trap density would be based on Hung's correlated mobility model, shown in equations 2.31 and 2.32. The values would then be compared that obtained from NBTI measurements, via the subthreshold swing method. The subthreshold swing method was chosen because the energy range considered is similar to that in flicker noise measurement, near the valence band edge.

Accordingly the correlated mobility model, as the gate overdrive tends towards the weak inversion region, the gate referred noise would converge to a near constant, known as flat-band voltage noise spectral density S_{Vfb} . This is consistent with the saturating of the normalised drain current noise power at weak inversion, shown in Figure 6.2. Figure 6.8 shows the gate referred input noise measured for a fresh device and after it had undergone NBTI stress. Notice that at the weak inversion region, the gate referred noise is saturated to a near constant value as well.

Figure 6.8 Gate referred noise against gate overdrive before and after stress. Circled points are magnified in Figure 6.9 ($f = 20$ Hz)

Figure 6.9 Magnified S_{vg} values in weak inversion region. Dash lines denote the average values for the pre-stress (bottom) and post-stress S_{vg} values.

Figure 6.9 shows a zoom-in scale of the gate referred noise at the weak inversion region. The pre- and post- S_{VFB} values were then calculated by taking a simple average of the five values plotted. Based on equation 2.32, the oxide trap density values are obtained:

	Fresh Device	After NBTI
Average S_{VFB}	$2.57 \times 10^{-11} \text{ V}^2/\text{Hz}$	$2.95 \times 10^{-11} \text{ V}^2/\text{Hz}$
$N_t(E_F)$, 20Hz	$4.23 \times 10^{21} \text{ cm}^{-3} \text{ eV}^{-1}$	$6.38 \times 10^{21} \text{ cm}^{-3} \text{ eV}^{-1}$

The rise in the calculated oxide trap density is expected because ΔV_{th} is caused by increased trap generation in the oxide, and some of those are detected by flicker noise exist within the energy range $E_F \pm kT$, via numbers fluctuations.

On the other hand, the increase in the number of interface traps after stress using the subthreshold swing method, ΔN_{it}^{ss} , is equal to $3.71 \times 10^{10} \text{ cm}^{-2}$, while the oxide trap suggested by flicker noise is $6.37 \times 10^{13} \text{ cm}^{-2}$ for the fresh device and $7.38 \times 10^{13} \text{ cm}^{-2}$ for the stressed device. Chew *et al.* [93] showed that for devices with similar channel dimensions, the trap density is in the $10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$ range, while scattering parameter is in the order of 10^{-15} Vs , even after accounting for the 70Å thick gate oxide used. Other papers [94-95] with similar device dimensions have reported results within that range as well. The much larger values recorded in the experiments indicates that some of the oxide traps already existed in the fresh device before NBTI. It is suspected that

the difference could not be accounted for because NBTI measurements only consider the positively charged traps that induce threshold voltage degradation. However, it may be possible that neutral traps are also generated in the process, and flicker noise measurements were able to capture them.

6.4 Summary

The raw data obtained from the in-house flicker noise measurement system were found to be comparable with other flicker noise related studies. By comparing flicker noise slopes in thick and thin gate p-MOSFETs, it was found that the thick gate devices show consistent increase in the gradient magnitude after NBTI. This was attributed to oxide traps generated during NBTI which were spatially further from the gate dielectric-substrate interface. On the other hand, oxide trap density calculated based on the correlated mobility model was found to be much larger than expected. This could be due to the generation of neutral traps during NBTI which could not be captured from the threshold voltage degradation.

Chapter 7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

A detailed study of negative bias temperature instability (NBTI) characterization is presented in this report. This thesis re-examines the accuracy of the NBTI power-law exponent value, investigate the bipolar nature of interface states near the conduction band, as well as providing an insight to how flicker noise may be used in NBTI characterization.

For experimental setup, the DC stress-measure-stress technique is used to characterize NBTI, together with the use of the charge pumping and subthreshold swing method to determine the interface traps density generated during stress. For flicker noise extraction, an in-house noise measurement setup was designed, implemented and utilized in this work. NBTI trap characterization takes place between pre and post stress noise measurement of the device under test (DUT).

In Chapter 4, the role of hole traps from deep-level energy states on the power-law time exponent of NBTI-induced threshold voltage degradation was investigated. The removal of such deep-level hole traps through the application of a positive gate bias caused the time exponent for interface trap generation to become much larger, at approximately 0.4-0.5. This challenges existing understanding that exponents of ~ 0.14 - 0.17 , obtained experimentally, imply interface-state generation to be H_2 diffusion-driven process.

In Chapter 5, it was shown that interface traps generated during NBTI stress in the upper half region of the bandgap exhibit bipolar (i.e. both acceptor and donor-

like) property. In other words, in p-MOSFET, the trap states in the upper-half of the Si energy bandgap are positively charged when empty, showing a near-parallel shift in the device's I_d - V_g curve. However, for n-MOSFET, these positive trap states changed from positive to neutral, and then to negative, during I_d - V_g sweep in the presence of a positive gate bias. This resulted in significant change in the subthreshold swing of the device. The bipolar nature of the interfacial trapped charge was attributed to E' centre, and it showed hole trapping characteristics at deep-level energy states.

Chapter 6 reported the use of flicker noise as a supplement to NBTI characterization. Comparisons of the slope gradient before and after stress indicated a shift in the trap distribution after NBTI, with the increase coming from oxide traps deep inside the gate oxide dielectric. This observation was more prominent in thick gate p-MOSFETs than thin gate devices. Further noise measurements carried out during the stress duration showed that the flicker noise slope increase progressive over the stress period, suggesting that these oxide traps were generated over time, rather than saturating quickly after applying the initial stress.

7.2 Recommendations for Future Work

Given that device scaling would continue to play an important role in increasing the device performance of MOSFETs, further studies in NBTI would help in better understanding the trap generation mechanisms, and hopefully new ways are derived in minimising NBTI impact on device reliability. Therefore, current models may be questioned and refined to better

explain new observations. Some areas of interest that could be worth further investigation include:

- 1) The use of high-K gate dielectric as replacement for the SiO₂ gate oxide is gaining popularity as device scaling strives to further reduce the EOT. As described in Chapter 5, the interfacial trapped charge identified exhibited both DLHT and interface states properties. It would be useful to characterize the impact of introducing this new gate dielectric on this interfacial trapped charge, as such traps are not easily annealed even in the presence of a positive gate bias. This could impact the reliability and performances of circuits that run on AC currents.

- 2) Flicker noise studies carried out by Dutta and Horn [96] identified that besides spatial trap distribution within the oxide, a distribution of oxide trap activation energies could lead to flicker noise as well. For example, flicker noise measurements as a function of temperature may be carried out to deduce the density of the fluctuations with respect to the energy. As NBTI degradation requires high temperature, this approach may help to monitor the change in trap distribution across the various energy levels before and after NBTI.

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