Development and characterization of GaN high electron mobility transistors for low noise applications

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**DEVELOPMENT AND CHARACTERIZATION
OF GAN HIGH ELECTRON MOBILITY TRANSISTORS
FOR LOW NOISE APPLICATIONS**

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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FOR LOW NOISE APPLICATIONS**

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School of Electrical and Electronic Engineering

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other university or institution.

Date

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Abstract

This thesis presents the fabrication, detailed characterization and analysis of AlGaIn/GaN high electron mobility transistors (HEMTs) and metal-insulator-semiconductor HEMTs (MISHEMTs) for microwave low-noise applications. The major contributions of this thesis are given below:

(1) Fabrication processes for conventional Schottky-gate GaN HEMTs and MISHEMTs were developed particularly for low-noise applications.

(2) The physical mechanisms of the OFF-state breakdown characteristics were comprehensively studied for GaN HEMTs on Si.

(3) The surface passivation effects on the bias-dependent microwave small signal characteristics and noise characteristics have been comprehensively studied for AlGaIn/GaN HEMTs on Si. The effects of SiN surface passivation on the bias-dependent small signal equivalent circuit elements have been investigated in detail.

(4) The temperature dependent noise performance was characterized for GaN HEMT on high-resistivity Si substrate over a wide temperature range from -50 °C to 200 °C. An analytical model for the temperature dependent microwave noise parameters has been proposed for the GaN HEMTs.

(5) A 0.25- μm Atomic-Layer-Deposited (ALD) $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISHEMT on high-resistivity Si with excellent noise performance was demonstrated. A state-of-the-art minimum noise figure ($NF_{\min}$) value of 1.0 dB at 10 GHz was achieved for a 0.25 μm ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISHEMT on Si for the first time. The 2-dimensional-electron-gas (2DEG) density and transport properties in the ALD- $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISHEMTs have been studied.

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Chapter 1

Introduction

1.1 Motivations

(A) *Unique material properties of GaN based semiconductors*

As wideband semiconductor materials, GaN based compound semiconductors have attracted enormous interests in microwave applications. GaN has many excellent properties for microwave applications in high power amplifiers (HPAs), and more recently low noise amplifiers (LNAs). For comparison purpose, Table 1.1 gives a summary of some key intrinsic properties for major semiconductor materials [1].

Table 1.1 Some key intrinsic properties for major semiconductor materials.

Material	Si	GaAs	InP	4H-SiC	GaN	AlN
E_g (eV)	1.1	1.42	1.34	3.26	3.42	6.2
n_i (cm ⁻³)	1.5×10^{10}	2.1×10^6	1.3×10^7	8.2×10^{-9}	1.9×10^{-10}	$\sim 10^{-31}$
ϵ_r	11.8	12.9	12.5	10	9.0	8.4
μ_n (cm ² /Vs)	1350	8500	5400	700	900	1100
E_C (10 ⁶ V/cm)	0.3	0.4	0.5	3	3.3	11.7
v_{sat} (10 ⁷ cm/s)	1.0	1.2	0.9	2.0	2.5	1.8
Θ_K (Wcm ⁻¹ K ⁻¹)	1.5	0.54	0.68	4.5	1.3	2.5
JM ($E_C^2 v_{sat}^2 / 4\pi^2$)	1	2.7	2.25	400	760	4930

From Table 1.1, it can be seen that GaN based materials have several important advantages over other semiconductors such as Si, GaAs and InP as described below:

(1) Owing to its wider band-gap, GaN has a much higher critical electrical field (E_C) up to about one order of magnitude than Si, GaAs or InP. High E_C of GaN means that the GaN based high electron mobility transistor (HEMT) can have an extremely high breakdown voltage, which is necessary for a device to obtain high output power, since the ideal power output provided by an HEMT at class-A operation can be estimated as [2]:

$$P_{out} = \frac{I_{dmax}(BV_{OFF} - V_{knee})}{8} \quad (1.1)$$

where I_{dmax} is the maximum drain current, BV_{off} is the off-state breakdown voltage and V_{knee} is the knee voltage. In addition, the high breakdown voltage improves the GaN based circuit's robustness and survivability.

(2) There exists strong spontaneous and piezoelectric polarization in wurtzite III-nitride crystals. In a typical Ga-face AlGa_N/Ga_N HEMT, there exists a large spontaneous polarization difference between the barrier layer (AlGa_N) and the channel (Ga_N). Furthermore, there is also a strong piezoelectric polarization inside the AlGa_N barrier due to the strain. The polarization effect induces a high two-dimensional electron gas (2DEG) density (typically $n_s > 1 \times 10^{13} \text{ cm}^{-2}$) at the interface between the barrier and the channel, even without high-doping in the barrier layer. The AlGa_N/Ga_N heterostructure typically has a value of n_s ($\sim 10^{13} \text{ cm}^{-2}$) which is about one order of magnitude higher than that of the GaAs and InP heterostructure. Higher n_s can lead to a higher channel current in GaN HEMTs than other material HEMTs.

(3) GaN has a very high electron saturation velocity (v_{sat}) up to 2.5×10^7 cm/s, which is about three times more than that in GaAs or InP, as shown in Fig. 1.1 [3, 4]. This is due to the fact that GaN crystal has a direct bandgap with a large energy splitting between the lowest (Γ) and upper ($M-L$) conduction valleys (1.5 -2.0 eV) [5]. High electron velocity in GaN means that GaN HEMTs can be expected to have a high drain current density and high operating frequency as indicated in the following expressions:

$$I_{d\max} \approx qn_s v_{sat} W_g \quad (1.2)$$

$$f_T \approx \frac{v_{sat}}{2\pi L_g} \quad (1.3)$$

where $I_{d\max}$ is the maximum drain current, f_T is the cut-off frequency, q is the electron charge quantity, W_g is the gate width, L_g is the gate length.

Fig. 1.1 Electron drift velocity versus electric field for various semiconductors.

(4) GaN has a high thermal conductivity which is more than two times that of GaAs and InP. High thermal conductivity can help with the heat dissipation and suppress the self-heating effect which is critical for high power applications.

(5) In Table 1.1, JM is the Johnson's figure of merit (FOM) for high frequency and high power applications. The JM values in the table are normalized with respect to that of Si. GaN has a value of JM which is one order of magnitude larger than that for Si, GaAs and InP, indicating the great potential of GaN to be applied in high frequency and high power applications.

(B) Potential of GaN HEMTs for low noise applications

Low noise amplifier (LNA) is an important component in the transmit/receiver (T/R) module for microwave communication systems, and it determines the overall system noise figure. Presently, GaAs or InP based HEMTs have been widely used with great success in LNAs by virtue of their broad-band low noise figures and high gains at high frequencies. However, GaAs based and InP based HEMTs feature a low breakdown voltage due to their narrow band gaps. So a limiter is generally needed on the receive frontend to protect the GaAs or InP

Fig. 1.2 Schematics of (a) a classical GaAs front end and (b) a robust GaN front end.

LNA against high input power, as shown in Fig. 1.2 (a) (dashed line). This limiter is usually realized with discrete and expensive components, such as PIN diodes. Such limitation circuit degrades the noise performance and the dynamic range of the front end part, and it also increases the complexity of the system design and raises the cost of the whole T/R module.

Due to the high electron saturation velocity in 2DEG, GaN HEMTs have a great potential to obtain high microwave and noise performance in spite of the relatively low mobility compared to GaAs and InP. As for low noise applications, GaN HEMTs have a predominant advantage over GaAs or InP HEMTs, namely the extremely large breakdown voltage due to the wide bandgap of the III-nitride material. Therefore the GaN LNAs can be expected to feature higher robustness and survivability, that is, the ability in sustaining higher level of input power

Fig. 1.3 State-of-art reported results of $NF_{\min}$ for various semiconductor HEMTs.

without degradation, as compared to the GaAs and InP LNAs. The T/R module with GaN LNAs can eliminate the need for input limitation/protection circuit, like that shown in Fig. 1.2 (b), and hence reduce the system complexity and lower the cost.

To date great progress has been achieved in the development of GaN HEMTs for high-frequency and low noise applications. High f_T up to 190 GHz [6], maximum oscillation frequency (f_{max}) up to 300 GHz [7], and low minimum noise figure (NF_{min}) up to 1.5 dB at K band [8] have been reported for GaN HEMTs. Fig. 1.3 shows the state-of-art results of noise performance for various semiconductor HEMTs. Until now GaN HEMTs have already shown comparable values as GaAs HEMTs. Fig. 1.4 shows a picture of wireless communication application spectrum for promising semiconductor technologies, presented in the 2008 International

Fig. 1.4 Promising technology for wireless communication application spectrum (published in ITRS public conference [9]).

Technology Roadmap for Semiconductors (ITRS) [9]. GaN HEMTs have been expected to have a wide application spectrum up to Ka-band. Although GaN HEMTs have been mainly developed for high-power applications in the past, their great potential for low-noise applications has only received more attention in recent years. Hence, it is expected that with much effort to improve their noise performance, GaN HEMTs could become an important contender for a wide range of low-noise applications in the near future.

(C) Advantages of GaN HEMTs on high-resistive Si substrate

Currently there are mainly three types of substrates employed in the epi-layer growth for GaN HEMT, namely SiC, sapphire and Si. Table 1.2 lists the comparison of some important properties between these three substrates. SiC has the highest thermal conductivity and lowest lattice mismatch to GaN. Until now the GaN HEMTs fabricated on SiC have demonstrated best power and noise performance with high output power density up to 41.4 W/mm at 4 GHz [10] and low minimum noise figure ($NF_{\min}$) of 1 dB at 20 GHz [11]. But SiC substrate has the highest cost. Sapphire substrate is more cost-effective than SiC; in addition, the lattice mismatch between GaN and sapphire is still moderate though much higher than that of SiC, and hence the GaN HEMTs grown on sapphire have also attracted great interest as a substitute for SiC [12]. Unfortunately the thermal conductivity of sapphire is the poorest among the three types of materials, which limits the maximum output power density which can be achieved for the GaN HEMT grown on it. To date the output power density for GaN HEMTs on sapphire has been reported to only be 12 W/mm at 4 GHz [13] and the $NF_{\min}$ has been reported to be 1.1 dB at 20 GHz [14].

Table 1.2 Comparison of three substrates for GaN HEMT epi-layer growth.

Substrate	Lattice Mismatch (%)	k (Wcm ⁻¹ K ⁻¹)	Cost	Integration Ability
SiC	3.6	4.9	High	Difficult
Sapphire	13.8	0.4	Moderate	Difficult
Si	17	1.3	Low	Easy

Si substrate is the most cost effective one when compared with sapphire and SiC. Furthermore, compared to sapphire, Si has a higher thermal conductivity. Si substrate can also provide the ability to integrate the GaN HEMTs with Si CMOS components using the mature Si process technologies.

However, conductive silicon substrate causes a noticeable parallel conduction and large parasitic pad capacitance, which leads to extra signal loss and time delay and thus are not suitable for RF or microwave circuit applications. To overcome these shortcomings, high-resistivity Si substrate is typically used [15].

The main difficulty faced in the GaN HEMT on Si is the growth of high quality crack-free GaN epilayers on Si substrate since the lattice mismatch between GaN and Si is large. After the optimization of growth conditions for seedling and transition layers, great progress has been achieved in the quality of GaN HEMT epilayers grown on Si substrates. High output power density up to 12.9 W/mm at 2.14 GHz [16] and 7 W/mm at 10 GHz have been reported for GaN HEMTs on Si [17]. As for noise performance, low $NF_{\min}$ of 0.65 dB at 10 GHz and 1.0 dB at 20 GHz have been reported [18]. The state-of-art reported minimum noise figures ($NF_{\min}$) at microwave frequencies for GaN HEMTs on different substrates at 10 GHz are shown in Fig. 1.5. It can be clearly seen that excellent noise performance for GaN HEMTs on Si substrate has been demonstrated close to that on sapphire and SiC substrates, at least at X band. The GaN HEMT on Si substrate

shows its strong competence over that on sapphire and SiC substrate in low noise applications.

Fig. 1.5 State-of-art reported results of $NF_{\min}$ at 10 GHz for GaN HEMTs on SiC, sapphire and Si.

(D) Motivation for the work in this thesis

In spite of the great progress that has been achieved, GaN HEMTs are still much more costly and technically less mature than GaAs HEMTs. For GaN HEMTs, there are still some process issues required to be solved and some characteristic behaviors required to be further investigated to understand the inside physical mechanisms before they can be widely applied into commercial systems, especially for those grown on Si substrates. For instance, low ohmic contact resistance is one of the key factors to obtain high frequency and low noise performance; however, there are still very limited reports on the study of the electron transport properties in ohmic contact and the characteristics at various

temperatures. Large breakdown voltage is one of the important advantages for GaN HEMTs in low noise application over GaAs or InP HEMTs, but until now the comprehensive study reported on the physical mechanisms of breakdown voltage is still lacking.

To comprehensively study the physics of the microwave and noise performance as well as to extract the noise model, the techniques of small signal equivalent circuit parameter (ECP) extraction and noise de-embedding are indispensable. Surface passivation has been widely used in GaN HEMTs to reduce the surface states and suppress the current collapse and frequency dispersion, however, the comprehensive characterization and investigation on the effect of passivation on the microwave small-signal equivalent circuit elements and internal noise sources have not been carried out. Furthermore, for GaN HEMTs to be used in harsh environments, it is necessary to evaluate its small signal and noise performance at elevated temperatures. And the thermal modeling for noise characteristics is also important to predict the device performance at various temperatures and frequencies so as to help to the system design. However, there are only limited temperature dependent studies on the noise characteristic and empirical modeling for GaN HEMTs on SiC or sapphire.

In addition, the conventional GaN HEMT with Schottky gate generally suffers from high gate current, which degrades their noise performance, as the mean square of the gate shot noise is proportional to the gate current:

$$\overline{I_{ngsh}^2} = 2qI_g \quad (1.4)$$

The intrinsic $NF_{\min}$ of the GaN HEMTs can be approximately expressed as [19]:

$$NF_{\min} = 1 + \frac{2\sqrt{i_{nd}^2(i_{ngi}^2 + i_{ngsh}^2)}}{g_m} \sqrt{1 - |C|^2} \quad (1.5)$$

The metal-insulator-semiconductor HEMTs (MISHEMTs) with a thin dielectric as gate insulator is a promising solution to this issue and can be predicted to further improve the noise performance.

In short, all the work in this thesis was motivated by the desire to develop and understand GaN HEMTs on high-resistivity Si substrates for low noise applications.

1.2 Objectives

The objectives of this work are to develop fabrication processes, characterize and analyze AlGaIn/GaN HEMTs for microwave low-noise applications. Novel GaN MISHEMTs with Atomic-Layer-deposited (ALD) Al₂O₃ as gate insulator is to be developed and demonstrated for improved noise performance.

1.3 Major Contributions of the Thesis

The major contributions of the thesis are summarized as below:

- (1) A set of fabrication processes have been developed for low-noise GaN HEMTs on silicon based on the facilities in our cleanroom.
- (2) The electron transport properties in the ohmic contact for AlGaIn/GaN HEMTs have been studied by means of temperature-dependent ohmic contact characterization and analysis.
- (3) The physical mechanisms of the OFF-state breakdown characteristics were comprehensively studied for GaN HEMTs on Si. By means of the drain

current injection and side-gate techniques, the off-state channel breakdown voltage and gate-drain breakdown voltage for the GaN HEMTs were extracted at varying temperatures. In combination with the analysis on the behavior of the gate current at high and low temperatures with varying gate-drain field, the physical mechanisms inside the different breakdown behaviors were determined.

(4) Procedures are successfully developed to extract the small-signal equivalent circuit elements and to de-embed the internal noise sources in GaN HEMTs from the measured S parameters and noise parameters, for the purpose of device physics study and microwave and noise modeling.

(5) Surface passivation effects on the bias-dependent microwave small signal characteristics and noise characteristics have been comprehensively studied for AlGaIn/GaN HEMTs on Si. The physics of the effects of SiN surface passivation on the bias-dependent small signal equivalent circuit elements have been investigated in detail. The noise performance was found to be improved by the surface passivation, and the main factor responsible for this improvement has been found to be due to the increased transconductance. The channel noise was found to be enhanced by the passivation and the physical mechanisms behind it have been identified.

(6) The temperature dependent noise characterization was carried out for a GaN HEMT on high-resistivity Si substrate over a wide temperature range from -50 °C to 200 °C. The degradation rates of the noise parameters with the increase of the temperature for the GaN HEMT on Si substrate were found to be comparable to those GaN HEMTs on SiC and sapphire substrates, and also comparable to the GaAs and InP HEMTs. The results demonstrated the great potential of GaN HEMTs for high-temperature applications.

(7) An analytical model for the temperature-dependent microwave noise parameters has been proposed for GaN HEMTs. It is found that the C_{gd} is necessary to be included in order to accurately modeling all the noise parameters over temperature.

(8) The technique of Al_2O_3 growth by ALD was optimized and successfully employed into the fabrication of GaN MISHEMTs. The 2DEG properties in ALD- Al_2O_3 /AlGaIn/GaN MIS heterostructures have been studied. It was found that the ALD Al_2O_3 thin film has improved the electron drift mobility and electron saturation velocity of 2DEG electrons, which is believed to result from the reduction of the remote Coulomb scattering from the surface states.

(9) A 0.25- μm ALD Al_2O_3 /AlGaIn/GaN MISHEMT on high-resistivity Si with excellent microwave small-signal and noise performance was demonstrated. The MISHEMT has also shown improved linearity in DC, microwave small signal and especially noise characteristics compared to the conventional GaN HEMT with Schottky gate.

1.4 Organization of the Thesis

This thesis is divided into 8 chapters and organized as follows. This chapter provides a brief introduction to this work. Chapter 2 describes the details of the key fabrication processes developed for conventional GaN HEMTs with Schottky-gate and GaN MISHEMTs with ALD Al_2O_3 gate insulator. The study of the current transport properties in ohmic contact is also described here. In Chapter 3, the physical mechanisms of the off-state breakdown characteristics are thoroughly studied. Chapter 4 presents the extraction procedures for small signal ECPs and the de-embedding procedures for internal noise sources, which provides necessary and

basic techniques to study the device characteristics and model the results in the later chapters. In Chapter 5, the surface passivation effects are comprehensively studied on the DC, small signal and noise characteristics. In Chapter 6, the temperature dependent noise performance for GaN HEMTs on Si is measured and compared with other devices. An analytical model for the temperature-dependent microwave noise parameters is also proposed and evaluated. To solve the issue of high gate leakage current and further improve the noise performance in conventional GaN HEMTs with Schottky gate, high quality Al_2O_3 grown by ALD technique is developed and employed into the GaN MISHEMT on Si. In Chapter 7, the 2DEG properties in ALD- $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ heterostructure is studied and then a $0.25\ \mu\text{m}$ ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISHEMT on Si with excellent noise performance is demonstrated. Finally, the conclusions of this work together with some recommendations for future work are given in Chapter 8.

Chapter 2

Fabrication Process for GaN HEMTs and MISHEMTs

In this chapter a set of processes for GaN HEMT and MISHEMT fabrication were developed based on our cleanroom facilities. The whole process for conventional HEMTs with Schottky gate includes mainly five steps, namely mesa isolation, ohmic contact formation, gate formation, pad and interconnection metallization and surface passivation. For MISHEMTs, an additional step of Al_2O_3 deposition using Atomic Layer Deposition (ALD) system was included before gate formation.

This chapter is divided into two parts. The first part will describe the typical device structure and key processes such as mesa isolation, ohmic contact formation and gate fabrication etc. for conventional HEMTs. In the second part, the detailed Al_2O_3 film deposition using the ALD system is described, followed by the C-V characterization technique to evaluate the quality of the gate insulator. Some key electrical characteristics of ALD grown Al_2O_3 are given at last.

2.1 Conventional GaN HEMT Fabrication

2.1.1 Typical device structure for conventional GaN HEMTs

A typical GaN HEMT structure and its band diagram are shown in Fig. 2.1. The basic structure of a typical GaN HEMT comprises of a cap layer, an AlGaN barrier layer, a spacer layer, a GaN buffer and a transition/seedling layer. A quasi-triangular potential well is formed at the heterointerface between the wide bandgap spacer layer and the small bandgap buffer layer. A high density two-dimensional electron gas (2DEG) is confined in this well due to the large polarization

difference and the big conduction band difference ΔE_C between the barrier/spacer and the buffer. The gate bias modulates the 2DEG concentration, so that the conductive current travelling in the channel is controlled by the gate bias. The function of each layer in the structure is listed as below:

Fig. 2.1 (a) The schematic of the cross section and (b) energy band diagram of a typical GaN HEMT.

(a) Cap layer

In GaN HEMTs, the cap layer could be either undoped or n^+ doped. For undoped GaN cap structure, due to the sufficiently large Schottky barrier height (>1.0 eV), the gate can be directly formed on this layer without the need for additional recess to remove this layer. This will ease the device fabrication and avoid device non-uniformity across the wafer caused by gate recess. In view of this, all the GaN HEMTs reported in this work have adopted the undoped GaN cap layer.

(b) Barrier layer

Barrier layer needs to have a larger bandgap than the channel and typically AlGa_N is used for this purpose. Besides AlGa_N, AlIn_N barrier has also been used in view of its advantages such as low lattice mismatch with the Ga_N and higher ΔE_C (1.31 eV for In_{0.17}Al_{0.83}N versus 0.4 eV for Al_{0.2}Ga_{0.8}N) between the barrier and the channel [20]. The barrier layer is typically undoped. However, it can be doped with n-type impurities to provide more electrons for the channel 2DEG. Typically, high Al composition is needed to provide a high ΔE_C , which can induce more electrons into the 2DEG and block the hot electrons spilling over into the barrier. The maximum composition of Al in AlGa_N barrier is typically <30% due to the critical thickness limit as a result of the crystal strain arising from the lattice mismatch between the barrier and the buffer.

(c) Spacer Layer

A wide bandgap undoped spacer layer can be inserted between the channel layer and the barrier layer to further increase the ΔE_C thus 2DEG sheet density and to reduce the remote coulomb scattering of the channel electrons thus increase the electron mobility. For this purpose, a very thin AlN layer (~1 nm) is recently tried to be used as the spacer layer. It has been observed the AlN spacer can increase the 2DEG density by ~10% and the mobility by ~50% [21].

(d) Channel Layer

In AlGa_N/Ga_N HEMTs, part of the Ga_N buffer close to the barrier/spacer serves as the channel layer at the same time. The channel layer has a thinner bandgap compared with the barrier and a quasi-triangular quantum well is formed close to the heterojunction, in which electrons are confined and form the 2DEG. Due to the large polarization difference between the barrier and the channel, a very high density 2DEG can be formed in Ga_N HEMTs. As a result, it is unnecessary to

have extra doping in the channel to realize high density 2DEG. Besides GaN, channels with even smaller bandgap such as InGaN and InN have also been investigated to be inserted between the barrier/spacer layer and the GaN buffer layer to further increase the 2DEG sheet concentration and electron mobility.

(d) Buffer

GaN is generally used in nitride HEMTs as the buffer. Insulated buffer is needed to reduce the parallel leakage current and the parasitic capacitive coupling effect. Intentional dopants such as Iron (Fe) have been used to compensate the background unintentional dopants in the buffer to reduce the buffer leakage current. However, such compensation doping will induce more carrier traps which will give rise to serious adverse effects on the device performance, such as DC to RF dispersion, current collapse etc. Thus it is of great importance to optimize the growth of the buffer layer.

(e) Transition/Seedling layer

Due to the lack of the large-area and good-quality GaN substrates, typically the III-Nitride semiconductor epilayers are grown on a different material substrate with relatively large lattice-mismatch to GaN such as SiC (mismatch $\sim 3.6\%$), sapphire (mismatch $\sim 13.8\%$) or silicon (mismatch $\sim 17\%$). The design and growth of the transition/seedling layer are the key to realize high-quality III-nitride epilayers. The transition/seedling layer is supposed to effectively block the dislocation and/or defects spreading into the buffer.

(f) Substrate

Typically three types of substrates are used to grow III-nitride epilayers for HEMT applications, that is, SiC, sapphire and Si. The details of the comparison between the three substrates have been thoroughly described in Chapter 1. In this

work, we use the high-resistivity Si as the substrate in view of its lowest cost and moderate thermal conductivity.

2.1.2 Key processes for conventional GaN HEMTs

The fabrication process flow for the conventional GaN HEMTs with sub-micron gate is shown as Fig. 2.2.

Fig. 2.2 Fabrication process flow for the conventional GaN HEMT with sub-micron gate.

The whole process can be divided into mainly five steps, that is, mesa isolation, ohmic contact metallization, gate formation, pad and interconnection metallization, and surface passivation.

2.1.2.1 Mesa Isolation

The pads of the devices must be isolated from each other to prevent short-circuit. Isolation can be realized by ion implantation or mesa (trench) etching. The former can offer a planar process but requires an ion-implanter. The mesa etching usually can be wet-etching or dry-etching; however, the commonly-used acid in clean room is difficult to etch GaN based semiconductor materials under normal conditions. Extra treatment is required for the successful etching such as heating or Ultra-Violet (UV) lighting [22]. Thus dry etching such as Reactive-Ion-Etching (RIE) or Inductively-Coupled-Plasma (ICP) is typically used in the GaN HEMT fabrication for mesa isolation.

ICP system has the advantages of high plasma density, low ion and electron energy (and thus low damage) while maintaining fast etch rates. The ICP etching recipe developed in this work is targeted to be optimized for low surface damage while keeping an acceptable etch rate. At the start, a layer of photoresist AZ1518 was coated and patterned using a UV-light (320 nm) contact mask aligner. The photoresist residue after development was descummed using O₂ plasma followed by a hard bake. Then the wafer was loaded into the ICP chamber. The etching was carried out with 10/20 sccm Cl₂/BCl₃ gases, 50/100 W RF/ICP power and at 10 mTorr chamber pressure to give a low etch rate of around 13 nm/min. The successful mesa isolation was ensured by etching down to the GaN buffer (~200 nm).

The isolation current is one of the key parameters used to evaluate the effectiveness of the mesa etching. High isolation current can result in high leakage between the electrodes and influence the device performance such as causing poor pinch-off. The isolation current also depends on the GaN buffer quality which is determined by the material growth. A typical current-voltage (I-V) curve for isolation leakage measurement is shown as Fig. 2.3. Typically the isolation leakage current is less than 10^{-6} A/mm at 20 V.

Fig. 2.3 (a) Layout of the pattern for isolation leakage measurement. (b) Typical current-voltage characteristics for mesa isolation in a GaN HEMT.

2.1.2.2 Ohmic Contact Formation

Low source and drain ohmic contact resistances are important for the GaN HEMT to achieve high drain current, high speed and low noise. The device structure, material quality, doping concentration in barrier, surface treatment before metal deposition, metal selection and thickness and post metallization annealing all influence the fabricated ohmic contact resistances.

The ohmic contact formation started from the pattern definition using the image reversal process of photoresist AZ5214. AZ 5214 was used to eliminate the chlorobenzene which can cause rough edges and non-uniform critical dimensions (here mainly source-to-drain distances) over the whole wafer. At first a layer of AZ5214 with thickness of $\sim 1.4 \mu\text{m}$ was coated on the wafer. After dehydration bake, the wafer was exposed by 320 nm UV light using a contact mask aligner. Then a second hard bake was used and followed by flood exposure. The patterns were developed using CD 26 developer. After appropriate surface treatment, a four-layer metal Ti/Al/Ni/Au was deposited using an electron beam evaporator and then followed by lift-off using Acetone and AZ 300T photoresist stripper. Finally, the wafer with ohmic metal was annealed to form ohmic contact between the source/drain metal electrode and the AlGaIn/GaN heterostructure.

Appropriate surface treatment before metal deposition can reduce the ohmic contact resistance and improve long-term reliability by removal of the residual photoresist, native oxide and foreign contamination. A clean, oxide-free surface is critical for the metal adhesion and low specific contact resistance. Before metallization, short-time oxygen plasma RIE was used to remove the residual photoresist brought during the previous lithography processes. Acid treatment using HCl:H₂O (1:1) solution for 1 minute was followed to remove the native oxide and contaminations.

The selection of the metal for ohmic contact needs to consider several metal characteristics including work function, resistivity, thermal expansion coefficient, thermal conductivity and adhesion to the III-nitride surface etc. The characteristics of some commonly used metals for ohmic contact process in semiconductor devices are listed in Table 2.1[23]. Generally speaking, low workfunction, low

resistivity, good thermal conductivity, similar thermal expansion coefficient to GaN materials and good adhesion to the semiconductor surface are required for the ohmic metal scheme in GaN HEMT.

Table 2.1 Workfunction, resistivity, coefficient of linear thermal expansion, and thermal conductivity for commonly used metals.

Metal	Workfunction (eV)	Resistivity (at 273 K) ($10^{-6} \Omega\text{cm}$)	Thermal Expansion Coefficient (at 298 K) (10^{-6}K^{-1})	Thermal Conductivity ($\text{Wcm}^{-1}\text{K}^{-1}$)
Pt	5.65	9.60	8.8	0.716
Ni	5.15	6.16	13.4	0.907
Pd	5.12	9.78	11.8	0.718
Au	5.10	2.05	14.2	3.170
W	4.55	4.82	4.5	1.740
Cr	4.50	11.80	4.9	0.937
Ti	4.33	39.00	8.6	0.219
Al	4.28	2.42	23.1	2.370
Ta	4.25	12.20	6.3	0.575
Mg	3.66	4.05	24.8	1.560

Ti/Al/Ni/Au multilayer metal scheme is a common metal scheme for ohmic contact in GaN HEMTs and is used in this work. The combination of Ti/Al is widely used to successfully form a low resistance ohmic contact for GaN HEMTs with Al acting as the “dopant species”. After post metallization annealing, the Al attracts the nitrogen from the AlGaN layer below (including GaN cap layer if available) and formed AlN [24]. Then a large amount of N-vacancies are formed in the barrier. These N-vacancies will work as high concentration n-dopants and provide free electrons, leading to a conductive barrier layer under the ohmic electrode. The AlN formed is very thin and electrons can easily tunnel through. Ti

is also necessary since it works as the catalyst for the reaction between Al and GaN/AlGa_N. And Ti itself also reactivates with GaN/AlGa_N to form TiN and leave N vacancies in the barrier. At the same time, Ti works as a thin “wetting agent” layer to promote the adhesion of Al to the semiconductor. At the top of the ohmic metal, Au is included to avoid the oxidation of Ti/Al, and to be as the bonding and interconnecting metal owing to its low electric resistivity and good chemical stability. To prevent the interdiffusion between the Au and Ti/Al during the high temperature annealing and/or long time working, Ni is inserted between the Au and Ti/Al as a blocking layer. As comparison to Ti, Ni can also improve the smoothness of the metal surface after annealing.

The thickness of each layer in the metal scheme is also important to get low contact resistance and smooth surface. After optimization, a thickness scheme of 20/120/40/50 nm for Ti/Al/Ni/Au was selected for the GaN HEMTs in this work. These metals were deposited using an electron beam evaporation system.

Post metallization annealing is required for the reaction of Ti/Al with the GaN/AlGa_N and formation of high concentration N-vacancies in the barrier. The annealing temperature and time are two key parameters to determine the result of the ohmic contact resistance. Compared to the furnace annealing, rapid thermal annealing (RTA) has much higher heating and cooling rates (30~500 °C/sec), which can further suppress the formation of the unwanted metal phase, because only a very short time is available at a certain temperature for the undesirable process or phase formation. In addition, RTA can reduce the thermal budget, that is, *anneal temperature* × *anneal time*.

The value of ohmic contact resistance (R_c) can be measured using a transmission line method (TLM) technique. For a pattern with two ohmic metal

pads fabricated on a mesa of AlGaIn/GaN heterostructure, as shown in the Fig. 2.4 (a), the total resistance between the two metal pads can be expressed as:

$$R_t = 2R_C' + R_{sh} \frac{L}{W} \quad (2.1)$$

where R_C' is the non-normalized ohmic contact resistance, R_{sh} is the sheet resistance of the AlGaIn/GaN heterostructure between the two ohmic metal pads, L/W are the gap length/width. For a group of such patterns with different gap lengths, as shown in Fig. 2.4 (b), the measured R_t versus L can be plotted as a line from which R_C and R_{sh} can be extracted:

$$R_C = \frac{\text{intercept}}{2} \cdot W \quad (2.2)$$

$$\text{And } R_{sh} = \text{slope} \cdot W \quad (2.3)$$

The specific contact resistivity ρ_c is calculated by:

$$\rho_C = \frac{R_C^2}{R_{sh}} \quad (2.4)$$

Fig. 2.5 shows the R_t versus L line measured from a TLM pattern with $L = 5, 10, 20, 40, 80 \mu\text{m}$ and $W = 100 \mu\text{m}$. The ohmic contact was formed by Ti/Al/Ni/Au (20/120/40/50 nm) deposited on AlGaIn/GaN surface and followed by RTA at 850 °C for 30 s in N_2 atmosphere. The calculated values of R_{sh} , R_C and ρ_c are 493 $\Omega/\square$, 0.31 $\Omega \cdot \text{mm}$ and $2 \times 10^{-6} \Omega \cdot \text{cm}^2$ respectively. Fig. 2.6 shows the measured values of R_C and ρ_c annealed at different temperatures. After annealing at 850 °C and 875 °C, ρ_c reaches the minimum, but the metal surface is obviously rougher at 875 °C than that of at 850 °C. Rough surface can blur the pattern edge definition and results in inaccurate critical-dimension (CD) values, as well as increase the risk of the short between the gate and source electrodes, since the gate-source distance is generally very small in the GaN HEMT in order to obtain a low source access resistance.

Hence the annealing temperature of the ohmic contact with Ti/Al/Ni/Au (20/120/40/50 nm) at 850 °C for 30 s at N₂ atmosphere using RTA was used considering both the requirements for low contact resistance and smooth surface.

Fig. 2.4 (a) Schematic of the cross section of a TLM pattern and its equivalent circuit. (b) A typical layout of TLM pattern with difference gap lengths.

Fig. 2.5 $R_t \sim L$ line measured for the TLM pattern with Ti/Al/Ni/Au (20/120/40/50 nm) on AlGaIn/GaN heterostructure after RTA annealing at 850 °C for 30 s in N₂ atmosphere.

Fig. 2.6 Measured R_c and ρ_c for the Ti/Al/Ni/Au (20/120/40/50 nm) on AlGaIn/GaN heterostructure annealed at different temperatures.

2.1.2.3 Gate Fabrication

Gate formation is a crucial step to realize a device with high performance. The gate electrode needs to form a Schottky contact with the III-nitride semiconductors. High workfunction metal is needed for the gate metal to form a Schottky contact with high barrier height and then low leakage current. Contact mask aligner can be used to pattern a gate with $\geq 1\mu\text{m}$ length. To fabricate a sub-micron gate length device, electron beam lithography (EBL) is one of the typically used techniques.

To achieve excellent microwave performance, short gate length is essential due to the fact that the transit time of electrons across the channel is proportional to the gate length, and hence the shorter the gate length, the shorter the transit time

and the higher the device speed. However, on the other side, shorter gate length will increase the gate resistance (R_g). R_g of a single gate can be expressed as :

$$R_g \approx \rho_g \frac{W_g}{L_g h_g} \quad (2.5)$$

where ρ_g is the gate metal resistivity, W_g is the gate width and h_g is the gate metal thickness. High R_g will degrade the microwave signal power gain and noise performance. To realize a short-length gate while maintaining small R_g at the same time, a T-shape gate (or mushroom-shape gate, with a short foot length and long head length) is a good solution.

Until now, various technologies have been developed to realize sub-micron gate patterning, such as tri-layer resist process [25], electron beam lithography (EBL) [26], x-ray lithography [27] and deep UV Phase Shifting Mask Lithography [28] etc. In this work, EBL system was employed together with the bi-layer electron beam resist to form the T-shape gate patterns for subsequent gate metal deposition and liftoff.

(A) EBL mark formation

JEOL JBX 5500FS EBL system was used in this work for sub-micron pattern definition. The alignment mark for the EBL writing should be fabricated at the same layer as the ohmic patterns in order to minimize the influence of the misalignment brought by the contact mask aligner during the optical lithography for other layers. However, different from the GaAs or InP device fabrication, where the RTA annealing for ohmic contact is accomplished at low temperatures (<450 °C) and the metal surface was normally smooth enough to be detected by the EBL systems, the RTA annealing in GaN HEMT fabrication are carried out at a high temperature (850 °C) and the metal surface became very rough after annealing

and cannot be detected by the EBL system. To solve this issue, additional steps were involved before the annealing as shown in Fig. 2.7:

Fig. 2.7 Process flow for EBL mark formation.

The main idea of the special treatment for the EBL alignment mark is to avoid the use of the rough ohmic metal as the EBL alignment mark and instead to utilize the mesa for EBL detection. After the ohmic metal formation, a layer of photoresist was coated on the whole wafer and a small window enclosing the EBL alignment mark was opened by photolithography using contact mask aligner. Then the wafer was etched down by Cl_2/BCl_3 plasmas using ICP to a depth of around 500 nm. During the etching, the ohmic metal will serve as a self-aligned mask to allow the formation of the 500 nm deep mesa. The four-layer ohmic metal was removed by the acid of aqua regia ($\text{HCl}:\text{HNO}_3=3:1$) and buffered oxide etchant (BOE, $\text{HF}:\text{NH}_4\text{HF}=1:6.5$). Then the protection photoresist was stripped and the EBL mark with smooth semiconductor surface was realized. Finally the entire wafer was subject to RTA for good ohmic contacts. The ICP etched depth is needed to be deep enough to provide a good contrast for the subsequent EBL detection. However too much of a depth needs a longer etch time and the ICP chamber temperature will become very high. This in turn can harden the photoresist and make it difficult to be stripped off. In our process, an optimized etch depth of 500 nm was adopted.

(B) T-shape gate fabrication

Fig. 2.8 shows the process flow for the fabrication of sub-micron T-shape gate.

Fig. 2.8 The process flow used to fabricate submicron T-shape gate.

After EBL mark formation and ohmic metal annealing, a bi-layer of polymethylmethacrylate (PMMA) (dissolved in chlorobenzene, 2wt%) and MMA-PMMA co-polymer (dissolved in ethyl lactate, 11wt%) was coated. A JEOL JBS 5500FS EBL system was then used to directly write the submicron T-gate pattern. The sensitivity to the electron beam of the top MMA-PMMA is higher than that of the bottom PMMA, so the exposure length on top was larger than that at the bottom, and thereby a T-shape is formed. After exposure, the sample was developed using a Methyl Iso-Butyl Ketone (MIBK): Isopropanol (IPA) =1:3 solution at room temperature. The developed gate pattern was descumed using O₂ plasma to remove the resist residue, and treated by HCl (1:1) for 1 min to remove the native oxide and other contaminations. Then Ni/Au bi-layer metals were deposited using an electron beam evaporation system. Ni was selected due to its large work function (See Table 2.1) and good adhesion to the semiconductor surface. Finally after normal lift-off process, the T-shape gate was formed.

Fig. 2.9 and Fig. 2.10 show some Scanning Electron Microscope (SEM) pictures of the fabricated T-shape gates. Fig. 2.9 (a) shows a typical cross section of the PMMA/MMA bi-layer photoresist after EBL exposure and development; (b) shows the cross section of the T-shape gate metal; Fig. 2.10 shows the top view of the fabricated Π -type two-finger transistor. The gate shown in the figure has a foot length ~ 250 nm and head length ~ 800 nm.

Fig. 2.9 SEM pictures of the T-shape gate fabricated using the bi-layer photoresist and EBL techniques. (a) Cross section of the PMMA/MMA bi-layer photoresist after EBL exposure and development. (b) Cross section of the T-shape gate metal.

Fig. 2.10 SEM pictures of the T-shape gate fabricated using the bi-layer photoresist and EBL techniques. Top view of the fabricated Π -type two-finger transistor.

2.1.2.4 Surface Passivation

Generally there exists a large amount of surface states at the surface of the III-nitride semiconductor. Some fabrication processes also damage the surface and bring forth more states. These surface states maybe come from the dangling bonds of the surface atoms, or the dislocations/defects at the surface as grown and generated by the damage during the processes, or the foreign contaminations etc. These surface states will work as carrier traps and seriously deteriorate the device performance. The negative charge induced by the electrons trapped at the surface will work as a virtual gate and lead to depletion to the channel electrons, thereby decrease the channel 2DEG density. The trapped charges at the surface also contribute to the remote Coulomb scattering to the channel electrons and decrease

the 2DEG mobility and velocity. In actual application, large surface states have brought serious effects such as current collapse and DC-to-RF dispersion.

Passivation using some dielectrics has been proven to successfully suppress the effects of surface states, such as Si₃N₄, SiO₂, Al₂O₃ and etc. In this work a layer of 120 nm SiN grown by plasma enhanced chemical vapor deposition (PECVD) is used as the surface passivation. The SiN was deposited at 300 °C using SiH₄, NH₃ and N₂ plasma under a chamber pressure of 1000 mTorr and at the RF power of 20 W. The deposition rate is around 0.9 nm/s. After the 120 nm SiN film was deposited on the whole wafer, the probing pad area was opened after patterning by normal photolithography and CF₄ plasma etch.

2.1.3 Study on the electron transport characteristics in ohmic contact for GaN HEMTs

Low ohmic contact resistance is one of the key factors for FETs to obtain high frequency and low noise performance. The extrinsic transconductance ($g_{m,ext}$) of an FET can be expressed as:

$$g_{m,ext} = \frac{g_{m,int}}{1 + g_{m,int} R_s + g_{m,int} \frac{R_s + R_d}{R_{ds}}} \quad (2.6)$$

where $g_{m,int}$ is the intrinsic transconductance, R_s is the source access resistance, R_d is the drain access resistance and R_{ds} is the output resistance. The ohmic contact resistance R_C is one important part for R_s , R_d or R_{ds} . The knowledge of the electron transport mechanisms in ohmic contact is one of the fundamental concerns in optimizing the device performance. However, very limited reports were available on the study of the electron transport properties in ohmic contact and the characteristics at various temperatures [29].

In this section we investigated the current transport mechanisms in ohmic contact formed by a commonly-used Ti/Al/Ni/Au metal scheme in AlGa_N/Ga_N HEMTs by means of characterizing its contact properties over a wide range of temperature from -50 to 200 °C. The variations of the 2DEG sheet resistance (R_{sh}) and the specific contact resistivity (ρ_c) and the contact resistance (R_c) with the temperature are reported and the relative physical mechanisms are discussed. The specific contact resistivity (ρ_c) decreased with the temperature and it was observed to be determined by the electron thermionic field emission (TFE) from the lowered conduction band-edge in the modified AlGa_N region with high-density N-vacancies to the quantum well at the AlGa_N/Ga_N heterojunction with two dimensional electron gas (2DEG).

In this work two samples were investigated. Sample #1 was grown on high resistivity (>10,000 Ω-cm) Si(111) substrate by metalorganic chemical vapor deposition (MOCVD), and its active structure consists of a 2 nm-thick undoped Ga_N cap layer, a 17.5 nm-thick un-doped Al_{0.26}Ga_{0.74}N barrier layer and an undoped Ga_N buffer layer. Sample #2 has the same active structure as Sample #1 but was grown on sapphire substrate.

The ohmic contact process is same as the description in the last section. The ohmic contact was measured by means of the TLM technique using a HP4142 semiconductor device analyzer. The temperature dependence measurements were carried out from -50 °C to 200 °C with step of 25 °C on Cascade Summit 1000 probe station with a Temptronic thermo chuck. The current-voltage (I-V) curves showed ohmic-like behaviors at all temperatures for both the samples. The values of R_{sh} , R_c and ρ_c are acquired from the Eqns. (2.2)-(2.4).

The values of R_{sh} of the two samples are shown in Fig. 2.11. It is known that R_{sh} is determined by the 2DEG density (n_s) and the mobility (μ) according to the formula:

$$R_{sh} = \frac{1}{qn_s\mu} \quad (2.7)$$

We have observed a very slow increase of the n_s with the temperature for AlGaIn/GaN heterostructure on Si from Hall measurement at the temperature range from -190 °C to 120 °C as shown in the inset of Fig. 2.11. Recent studies have also shown that the temperature has very little influence on the n_s in AlGaIn/GaN heterostructure in the temperature range similar to our work [29, 30]. Therefore the temperature dependence of R_{sh} is mainly determined by μ . This conclusion also agrees with the observation that the temperature dependence of R_{sh} can be fitted well using a power-law relation, since the electron 2DEG mobility over the temperature typically shows the power-law relation at $T > \sim 200$ K due to the predominant optical phonon scattering [31, 32]. That is,

$$R_{sh} = R_{sh0} \left(\frac{T_0}{T} \right)^\gamma = \frac{1}{qn_s} \left(\mu_0 \left(\frac{T}{T_0} \right)^\gamma \right)^{-1} \quad (2.8)$$

where R_{sh0} and μ_0 are the values of R_{sh} and μ at $T=300$ K, and γ is the power index. The fitted curves and the fitted values of R_{sh0} and γ for the two samples are shown in Fig. 2.11 (a). The obtained γ values ($\gamma=-2.7$ and $\gamma=-2.3$) are consistent with the one ($\gamma=-2.5$) obtained from our Hall measured R_{sh} and μ (See Fig. 2.11 (b)), and these values are also consistent with those reported values in the range between -2.18 and -3.42 [33, 34, 35].

Fig. 2.11 (a) Measured (symbols) and fitted (lines) 2DEG sheet resistances R_{sh} as a function of temperature from -50 to 200 $^{\circ}\text{C}$ for Sample #1 (on Si) and #2 (on sapphire). (b) Normalized Hall measurement data for AlGaIn/GaN heterostructure on Si at the temperature from -190 to 120 $^{\circ}\text{C}$.

The measured ρ_c versus temperature for the two samples are plotted in Fig. 2.12. Both ρ_c values for the two samples decreased at higher temperatures, and similar behavior was reported for the ohmic contact of AlGaIn/GaN

heterostructures [29], n-type GaN [36], p-type GaN [37] and other materials [38, 39], while opposite behavior has also been reported for n-GaN [38] and other materials [39]. It is well known that in the metal-semiconductor contacts there exist mainly three current transport mechanisms: field emission (FE) (or direct tunneling), thermionic field emission (TFE) (or thermally enhanced tunneling) and thermionic emission (TE) [40]. The ρ_c under the mechanism of FE with triangle potential approximation can be expressed as:

$$\rho_c = \frac{k_B T}{q A_{ri}} \exp\left(\frac{\phi_B}{k_B T}\right) \quad (2.9)$$

The ρ_c under the mechanism of TE can be expressed as:

$$\rho_c = \left[\frac{A^* T \pi q}{k_B \sin(\pi c_1 k_B T)} \exp\left(-\frac{\phi_B}{E_{00}}\right) - \frac{A^* c_1 q}{(c_1 k_B)^2} \exp\left(-\frac{\phi_B}{E_{00}} - c_1 E_n\right) \right]^{-1} \quad (2.10)$$

$$\text{where} \quad c_1 = \frac{1}{2E_{00}} \ln\left(\frac{4\phi_B}{E_n}\right) \quad (2.11)$$

$$\text{and} \quad E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N_D}{m_n^* \epsilon}} \quad (2.12)$$

And the ρ_c under the mechanism of TFE can be expressed as:

$$\rho_c = \left(\frac{1}{q A_{ri}} \right) \frac{k_B^2}{\sqrt{\pi(\phi_B + E_n) E_{00}}} \cosh\left(\frac{E_{00}}{k_B T}\right) \sqrt{\coth\left(\frac{E_{00}}{k_B T}\right)} \times \exp\left(\frac{\phi_B + E_n}{E_0} - \frac{E_n}{k_B T}\right) \quad (2.13)$$

$$\text{where } E_0 = E_{00} \coth\left(\frac{E_{00}}{k_B T}\right) \quad (2.14)$$

A_{ri} is the Richardson constant and is expressed as

$$A_{ri} = 4\pi m_n^* q k_B^2 / h^3 \quad (2.15)$$

m_n^* is the effective mass of tunneling electron and here $m_n^*=0.226m_e$ with m_e the electron rest mass. The dielectric constant is $\varepsilon=8.9\varepsilon_0$. ϕ_B is the barrier height during the carrier transport and E_n is the energy difference between the conduction-band edge and the Fermi level. k_B is the Boltzmann constant. All other parameters have their usual meanings.

After the evaluation of three models by fitting the measured data, we found that the TFE model is suitable for our measured ρ_c for both the two samples. The fitted curves and the fitted values of ϕ_B , N_D and E_n are shown in Fig. 2.12.

Fig. 2.12 Measured (symbols) and modeled (lines) specific contact resistance ρ_c as a function of temperature for Sample #1 (on Si) and #2 (on sapphire).

The current transport in ohmic contact of HEMTs is actually much more complicated and needs to be accurately described using an equivalent network including distributed components with different specific contact resistivities and sheet resistances for the metal and each semiconductor layer [38]. However, we

can make a simple assumption that the total ohmic contact only involves two barriers in series (as shown in Fig. 2.13): the first barrier (Region I) with ρ_{C1} formed between the metal and the modified GaN/AlGaN; the second barrier (Region III) with ρ_{C2} formed between the modified AlGaN and the 2DEG, and the total specific contact resistivity $\rho_C = \rho_{C1} + \rho_{C2}$. Here the “modified GaN/AlGaN” (Region II) means that the material properties of the original GaN/AlGaN nearby the surface were altered by the reaction between the ohmic metal alloy (mainly Ti and Al) and GaN/AlGaN during high temperature annealing and as a result, high-density donor-like N-vacancies were formed. These N-vacancies manifest themselves as high-concentration n-dopants [41] which pull the local electron conduction band well below the Fermi level and leave a very thin Schottky barrier at the interface. Since electrons can tunnel through such a thin barrier with very high probability, ρ_{C1} should be very small and negligible for the total ρ_C . This is

Fig. 2.13 The energy band schematic of the ohmic metal and AlGaN/GaN. The carrier transport is divided into three regions: Region I, the barrier between the ohmic metal to modified GaN/AlGaN; Region II, modified GaN/AlGaN; Region III, the barrier between the modified AlGaN and 2DEG.

consistent with our modeling results that the TFE with a single barrier can fit the ρ_C versus temperature well. It also agrees with ref [29], where the authors directly took the modified GaN/AlGaN region as the extension of the ohmic metal and no barrier was considered at the metal-AlGaN interface.

It is interesting to find that similar values of ϕ_B (0.52 eV and 0.48 eV) were obtained from the fitting of the temperature dependent ρ_C for the two different samples. Since the barrier height between the ohmic metal (Ti and/or TiN/TiAl) and the GaN/AlGaN is around 1.0 eV (estimated from Ref. [42, 43]), the extracted ϕ_B here should not be the barrier height between the metal to the modified GaN/AlGaN but the barrier height between the modified AlGaN and the 2DEG. This further verifies the previous analysis that the metal modified GaN/AlGaN barrier does not play a key role in the total ρ_C . Besides our results, other researchers have also obtained similar ϕ_B of 0.42 eV for ohmic contact of AlGaN/GaN HEMT [31]. This is despite the different barrier doping condition and ohmic contact processes in their device, and the fact that FE was found to be dominant in their ohmic transport behavior. The similar values of ϕ_B show that this parameter is relatively less sensitive to the barrier doping condition and the ohmic process. However, for n-GaN, much different values of ϕ_B around 0.81-1.21 eV were obtained [36]. The reason for the difference is because in ohmic contact on n-GaN, the responsible barrier for carrier transport is the Schottky barrier from ohmic metal to the modified bulk GaN, while in AlGaN/GaN HEMT, the responsible barrier is that from the modified AlGaN to 2DEG.

In the TFE model another important parameter is E_n , which represents the energy difference between the effective conduction-band edge and the Fermi level in the quantum well at AlGaN/GaN interface. Taking quantum effects into

Fig. 2.14 Numerically simulated (a) energy band diagram (b) electron distribution at the tri-angle quantum well at the AlGaIn/GaN interface. The simulation is accomplished by solving the Poisson Equation and Schrödinger Equation self-consistently using ATLAS software.

consideration, we used the 2-D numerical simulation tool ATLAS to solve the Poisson Equation and Schrödinger Equation self-consistently at the triangle-like quantum well. The results are shown in Fig. 2.14. The two electron subband levels were found to be $E_1 = E_F - 0.137$ eV and $E_2 = E_F - 0.007$ eV. Since the number of

electrons occupying E_1 and E_2 take 82.7% and 13.0% of the total electron numbers respectively, the effective conduction band energy $E_{c,eff}$ can be estimated as $E_{c,eff} \approx E_F - 82.7\%*(E_F - E_1) - 13.0\%*(E_F - E_2) = 0.114$ eV. It is clear that our experimentally fitted values of E_n (see Table 2.2) agree well with the result from the 2-D simulation.

The parameter N_D in the TFE model approximately represents the 2DEG concentration and the orders of magnitude for the fitted N_D agree well with that of the 2DEG concentration (10^{19} cm^{-3}). However, the comparison of N_D for the two samples is inconsistent with E_n (that is, $E_{n,\#1} < E_{n,\#2}$, but $N_{D,\#1} > N_{D,\#2}$), which suffers from the fact that the expression of E_{00} in the TFE model is also affected by other variables such as the shape and width of the barrier and/or traps etc., whereas the employed relation between E_{00} and N_D in the N_D calculation is simplified under triangle potential approximation.

Fig. 2.15 shows the measured R_C for the two samples. Because of

$$R_c = \sqrt{\rho_c \cdot R_{sh}} \quad (2.16)$$

R_C is affected by both ρ_C and R_{sh} . Since ρ_C and R_{sh} are inversely proportional to the temperature in opposite ways, the temperature dependence of R_C showed a non-monotone behavior and had a local maximum around 50°C. In other reports, the R_C values have been observed to show various dependencies on temperature such as increase [44], or decrease [31] or non-monotone behavior similar to ours [45]. The various R_C dependencies are due to the different ratios of increase/decrease of ρ_C and R_{sh} over temperature in the different findings. In our case, the R_C versus temperature for both samples can be divided into two linear sections separated at 50°C, and each section can be modeled using linear approximation $R_C(T)=R_C(T_0)(1+B(T-T_0))$, where $T_0=300$ K and B is the

temperature coefficient. The fitted values of B_1 ($\sim 4 \times 10^{-3} / ^\circ\text{C}$, from -50°C to 50°C) and B_2 ($\sim -3.5 \times 10^{-3} / ^\circ\text{C}$, from 50°C to 200°C) are listed in Table 2.2 and not much difference exist between the two samples.

The values of R_C for the GaN HEMTs used in this study are relatively higher compared to the typical value nowadays of $<0.5 \Omega\cdot\text{mm}$. Some groups have realized very low R_C of around $0.2 \Omega\cdot\text{mm}$ [46]. However, it can be predicted that the proposed TFE model (Eqns 2.13-2.15 and Fig. 2.13) is still suitable when R_C is lowered down by process optimization. After further optimization, Region II in Fig. 2.13 will be enlarged and the width of Region III will become thinner. This will enhance the electron direct tunneling through the barrier in Region III, and then reduce the decrease rate of ρ_C with the increase of temperature. According to Eqn. 2.16, the peak of the R_C curve versus temperature (See Fig. 2.15) will shift to a higher temperature point.

Fig. 2.15 Measured (symbols) and fitted (lines) contact resistance R_C as a function of temperature for Sample #1 (on Si) and #2 (on sapphire).

Table 2.2 Fitted values of R_{sh0} , γ , ϕ_B , E_n , N_D , B_1 , B_2 for Sample #1 (on Si) and #2 (on sapphire).

	R_{sh0} ($\Omega/\square$)	γ	ϕ_B (eV)	E_n (eV)	N_D ($\times 10^{19} \text{cm}^{-3}$)	B_1 ($\times 10^{-3} / ^\circ\text{C}$)	B_2 ($\times 10^{-3} / ^\circ\text{C}$)
Sample #1	554.4	-2.7	0.52	0.08	1.09	3.81	-3.38
Sample #2	860.9	-2.3	0.48	0.11	0.85	4.18	-3.76

In conclusion, the electron transport properties in the Ti/Al/Ni/Au ohmic contact in AlGaIn/GaN HEMTs on Si substrate and sapphire were investigated. Over a temperature range of -50°C to 200°C , the two samples exhibited increase of R_{sh} , decrease of ρ_c and non-monotone behavior of R_c with the temperature. The R_{sh} increase with temperature is mainly due to the decrease of mobility according to the power-law equation with the power indices of around -2.3 to -2.7. The electron TFE from the modified AlGaIn with high-density N-vacancies to the 2DEG was found to be the dominant transport mechanism in the AlGaIn/GaN heterostructures ohmic contact. The experimentally fitted ϕ_B , E_n and N_D agree well with the calculation and the 2-D numerical simulation. The opposite behavior of R_{sh} and ρ_c leads to the observed non-monotone behavior of R_c with temperature.

2.2 GaN MISHEMTs Fabrication

Typically the conventional GaN HEMTs with Schottky metal gate have suffered an issue of high gate leakage current [47, 48, 49]. The high gate leakage limit the highest positive voltage which can be biased on the gate, then limit the maximum drain current and available output power. The microwave noise

performance will be also affected by the high gate shot noise induced by the high gate leakage current as Eqns. (1.4, 1.5) shows and reported in [49, 50, 51, 52].

The MISHEMT, that is, like Si MOSFET with a thin dielectric layer between the metal gate and the epilayer, is a good solution to the issue of high gate leakage current. The criteria to choose the insulator material includes its band gap, dielectric constant, breakdown field, etc. Wide band gap is necessary for gate insulator to keep a low leakage current. High dielectric constant can reduce the equivalent oxide thickness (EOT) of the gate insulator and enable the device to hold a low gate leakage current while high gate capacitance, and the high gate capacitance is needed for high modulation efficiency for the channel carrier concentration. High breakdown field of the gate insulator is required for the reliability of the device. In addition, low trap density and low fixed/mobile charge density are also required.

GaN MISHEMTs with various dielectric materials, such as SiO₂ [53], SiN [54], Al₂O₃ [55, 56, 57], HfO₂ [58], Ga₂O₃ [59], Sc₂O₃ [60], etc. have been demonstrated. Among these materials, Al₂O₃ have attracted great interest due to its excellent physics properties including wide band gap, high dielectric constant and high breakdown field. Excellent DC and small signal performance of the GaN MISHEMTs with Al₂O₃ gate insulator have been reported [55, 56, 57].

There are various techniques to deposit Al₂O₃ thin film on a GaN wafer, including electron beam evaporation, sputtering, MOCVD, Al metal oxidization, atomic layer deposition (ALD) etc. Among these techniques, ALD has the advantages of good film quality, high uniformity and nano-scale controllability etc. The details of the MISHEMT device structure and ALD technique are described as follow.

2.2.1 Typical device structure for GaN MISHEMTs

Fig. 2.16 shows the schematic of the cross section for a typical GaN MISHEMT. As compared to the conventional GaN HEMT, as shown in Fig. 2.1, the only difference is that GaN MISHEMT involves an extra dielectric layer between the metal gate and the III-Nitride semiconductor surface. This gate insulator can effectively reduce the gate leakage current. At the same time, it also works as a passivation layer and can effectively reduce the surface states. In fabrication, this gate insulator layer is usually deposited before gate process and after ohmic annealing.

Fig. 2.16 Schematic of the cross section of a typical GaN MISHEMT.

2.2.2 Atomic Layer Deposition (ALD) of Al_2O_3

ALD is a method of depositing thin films on the substrate with atomic scale precision. The difference between ALD and chemical vapor deposition (CVD) exists in that, ALD reaction breaks the CVD reaction into two parts, and keeps the precursor materials separate during the reaction. The first precursor gas is

introduced alone into the process chamber and produces a monolayer of gas on the wafer surface. Then the chamber and the pipe line are pumped. Then the second precursor of gas is released and introduced into the chamber and reacts with the first precursor on the wafer surface. A monolayer of film is thus formed.

There are two fundamental mechanisms during the growth: the chemisorption saturation process and the sequential surface chemical reaction process. Since each pair of gas pulses, that is, one cycle, produces exactly one monolayer of film, the thickness of the resulting film can be precisely controlled by the number of the deposition cycle. During the growth, the precursors are kept separate all the time, so that the thin film layer thickness can be obtained as fine as atomic/molecular scale per monolayer.

The ALD growth procedure of Al_2O_3 is shown in Fig. 2.17 - Fig. 2.23, step 1 -7 [61].

Fig. 2.17 ALD growth procedure step 1.

Step 1: After placing the sample in the reactor and pumping the chamber to a low enough pressure, trimethylaluminum (TMA) is pulsed into the reaction chamber.

Fig. 2.18 ALD growth procedure step 2.

Step 2: The TMA reacts with the absorbed hydroxyl groups, producing methane as the reaction product: $\text{Al}(\text{CH}_3)_3 + \text{Ga-O-H} \rightarrow \text{Ga-O-Al}(\text{CH}_3)_2 + \text{CH}_4$.

Fig. 2.19 ALD growth procedure step 3.

Step 3: The TMA reacts with the absorbed hydroxyl groups, until the surface is passivated. TMA does not react with itself, termination the reaction to one layer. This causes the perfect uniformity of ALD. The excess TMA is pumped away together with the methane reaction product.

Fig. 2.20 ALD growth procedure step 4.

Step 4: After the TMA and methane reaction product is pumped away, water vapor (H_2O) is pulsed into the reaction chamber.

Fig. 2.21 ALD growth procedure step 5.

Step 5: H_2O reacts with the dangling methyl groups on the new surface forming aluminum oxygen (Al-O) bridges and hydroxyl surface groups, waiting for a new TMA pulse. Again methane is the reaction product: $2\text{H}_2\text{O} + \text{Ga-O-Al}(\text{CH}_3)_2 \rightarrow \text{Ga-O-Al}(\text{OH})_2 + 2\text{CH}_4$.

Fig. 2.22 ALD growth procedure step 6.

Step 6: The reaction product methane is pumped away. Excess H_2O vapor does not react with the hydroxyl surface groups, again causing perfect passivation to one atomic layer.

Fig. 2.23 ALD growth procedure step 7.

Step 7: One TMA and one H_2O vapor pulse form one cycle. Here three cycles are shown, with approximately 1 Angstrom per cycle. Each cycle including pulsing and pumping takes e. g. 3 sec. Two reaction steps in each cycle:

The ALD has the following advantages over other deposition techniques for high-k dielectric thin film:

- Stoichiometric films.
- Perfect step coverage and 3D conformability. Typically the thin film by ALD has an over aspect ratio as high as 60:1. The bottoms and sidewalls of the mesa/trenches are covered uniformly.
- High large-area uniformity.
- High thin film quality, low leakage and high reliability.
- Precise thickness control. The thickness of the film is determined simply by the number of deposition cycles.
- Low temperature deposition possibility (from room temperature to 400 °C)

2.2.3 C-V characterization technique for gate dielectric

The quality of the gate insulator and the interface between it and the semiconductor wafer is crucial for the MISHEMT to achieve excellent and reliable performance. Until now many characterization techniques have been developed to evaluate the gate insulator quality, including optical metrology, such as AFM, TEM etc, and electrical metrology, such as current-voltage (I-V), capacitance-voltage (C-V); temperature accelerated test, etc. Among these techniques, C-V measurement is the most commonly used as it is simple and reliable to evaluate the thin film quality both qualitatively and quantitatively.

2.2.3.1 Basic theory of the MIS heterostructure capacitance

The schematic and the equivalent circuit for a MIS diode with AlGaN/GaN heterostructure are shown in Fig. 2.24. Fig. 2.24 (a) shows the top view of the layout for a typical circular MIS diode; (b) shows its cross section and equivalent

Fig. 2.24 The schematic and equivalent circuit of a MIS diode; (a) the top view of the layout for a typical circular MIS diode; (b) the cross section and equivalent circuit element distribution; (c) the equivalent circuit topology.

circuit element distribution; (c) shows its equivalent circuit topology. The traps located at those places other than interface are ignored. The resistance R_s accounts for the series resistance from the ohmic contact to the channel below gate through the access region between the source and gate electrodes. The resistance R_t accounts for the effect of gate leakage current. C_{IN} accounts for the capacitance of the gate insulator. C_b accounts for the capacitance of the barrier layer (here the term “barrier” includes the possible spacer layer and cap layer). C_d accounts for the capacitance of the channel depletion region. The C_{it} and R_{it} in series describe the capacitance effect of the traps located at the interface between the gate insulator

and III-nitride barrier. When the gate bias changes, the number of trapped electrons in the interface states also varies, so that an effective capacitor is formed. The R_{it} together with C_{it} describes the time delay (τ) required for the electrons trapped at the interface to form an equilibrium with those in the channel, and C_{it} is related to the trap density (D_{it}) as the following expression shows: [62]

$$\begin{cases} \tau = R_{it} C_{it} \\ D_{it} = \frac{C_{it}}{qA} \end{cases} \quad (2.17)$$

where A is the area of the gate.

2.2.3.2 Thickness/Permittivity measurement of the gate insulator by C-V technique

Considering the circuit in Fig. 2.24 (c), if (1) the leakage current of the diode is negligible, that is, R_t is very large; (2) the gate bias is oscillating at such a high frequency that the emission and capture of the trapped electrons cannot catch up

Fig. 2.25 Simplified circuit of (a) a MIS diode (b) Schottky diode and (c) measurement.

with the change of the gate bias, therefore the effect of C_{it} and R_{it} is negligible; (3) the device is working in accumulation region, then the circuit can be simplified

into Fig. 2.25 (a). The equivalent circuit for the corresponding conventional Schottky diode (without gate insulator) is simplified into Fig. 2.25 (b). The circuit of the C-V measurement is assumed to Fig. 2.25 (c) by the equipment.

The C_m and G_m in Fig. 2.25 (c) are the values of capacitance and conductance directly measured. The R_s effect on the measured capacitance can be subtracted by:

$$C_{m'} = \frac{C_m}{(1 + R_s G_m)^2 + (\omega R_s C_m)^2} \quad (2.18)$$

Then for conventional HEMT ($C_m' = C_{HEMT}$):

$$C_{HEMT} = C_b \quad (2.19)$$

For MIS diode ($C_m' = C_{MISHEMT}$):

$$\frac{1}{C_{MISHEMT}} = \frac{1}{C_{IN}} + \frac{1}{C_b} \quad (2.20)$$

Afterward C_{IN} can be calculated from the measured overall capacitance for the corresponding MIS diode ($C_{MISHEMT}$) and conventional Schottky diode (C_{HEMT}):

$$C_{IN} = \frac{1}{\left(\frac{1}{C_{MISHEMT}} - \frac{1}{C_{HEMT}} \right)} \quad (2.21)$$

C_{IN} is determined by the dielectric constant ε and the thickness of the gate insulator d by the expression:

$$C_{IN} = \frac{A\varepsilon}{d} \quad (2.22)$$

where A is the area of the diode gate. Thus if anyone between ε or d is known by other means, the value of the other one can also be determined.

2.2.3.3 Interface quality evaluation for $Al_2O_3/AlGaIn/GaN$ by C-V technique

Like the Si MOS diode, the large amount of interface states in $Al_2O_3/AlGaIn/GaN$ MIS diode will broaden the transition region from the

depletion to the accumulation. For a trap-free depletion-mode MIS diode, when the gate bias is zero, the channel is open and the diode is working in the accumulation region with $C_{MISHEMT} = 1 / \left(\frac{1}{C_{IN}} + \frac{1}{C_b} \right)$. When the gate voltage is ramped down from zero until the threshold voltage V_{th} , the device is still working in the accumulation region and $C_{MISHEMT}$ remains nearly constant. When V_g reaches and goes below V_{th} , the channel is turned off and $C_{MISHEMT}$ is sharply lowered to a small value close to zero.

When a large amount of interface states exist at the interface between the gate insulator and the III-nitride semiconductor, the traps will capture or release electrons when gate bias changes. The net charge change will cause the threshold voltage V_{th} changed. Displayed on the C-V curve, this trap effect will lead to a wider transition from the depletion the accumulation region. Thus the degree of the sharpness for this transition in the C-V curve can be used to roughly judge how the quality of the gate insulator is.

Fig. 2.26 shows two C-V curves for two ALD $Al_2O_3/AlGaN/GaN$ MIS structures with different Al_2O_3 quality measured at high frequency (1 MHz). The curve in Fig. 2.26 (a) was measured for the Al_2O_3 deposited earlier with poor quality, and (b) is for the Al_2O_3 whose quality is much improved. It can be clearly seen that the transition region from depletion to accumulation in the C-V curve is much sharper for $Al_2O_3/AlGaN/GaN$ MIS diode with high quality Al_2O_3 (with small amounts of traps inside the oxide and/or at the interface) than that one with poor quality Al_2O_3 (with large amounts of traps).

Fig. 2.26 High frequency (at 1 MHz) C-V characteristics of the ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS structure on Si with different Al_2O_3 quality. (a) For the early deposited Al_2O_3 with poor quality; (b) For the Al_2O_3 with improved quality.

Fig. 2.27 C-V characteristics for the ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS structure on Si with different Al_2O_3 quality at high frequency (1 MHz) and low frequency (10 KHz). (a) For the Al_2O_3 deposited early with poor quality; (b) for the Al_2O_3 with improved quality.

Another simple technique to directly evaluate the quality of the thin film is the low-frequency C-V measurement. At low enough frequency, the numbers of the electrons at the interface states have enough time to reach equilibrium through electron exchange with the electrons at the conduction band in the channel, and hence C_{it} will add to the measured overall capacitance C_m , as the circuit in Fig. 2.24 (c) shows. As a result, the measured overall capacitance at low frequency will be larger than that measured at high frequency, and their difference varies with the electrical potential at the interface which depends on the gate bias. Fig. 2.27 shows two groups of C-V curves for ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS structure with different Al_2O_3 quality measured at both high frequency (1 MHz) and low frequency (10 KHz). The curve shown in Fig. 2.27 (a) is for the Al_2O_3 deposited early with poor quality, and (b) is for the Al_2O_3 whose deposition condition has been much improved. It can be seen that in the case of the gate insulator with poor quality, its C-V curve at low frequency shows much difference from that at high frequency. The big hump comes from the capacitance of the interface states with a peak density at the energy level corresponding to that gate bias. For the Al_2O_3 with good quality, the gap of the two curves at high and low frequencies is very small.

The techniques described above can be employed for the purpose of qualitatively evaluating the quality of the deposited Al_2O_3 thin film. To quantitatively determine the interface trap density, more calculations and other techniques are needed. A simple method to measure the interface trap density is the so-called “*hi-lo* frequency” method [63, 64]. As described in the last paragraph, the difference between the measured overall capacitances at high and low frequencies includes the information of trap effects. But to work out the trap density (D_{it}), the values of R_t and R_s are required to be determined first by other measurement. Then

Fig. 2.24 (c) will be simplified into Fig. 2.28 (a). The interface state density can be calculated by [64]:

$$D_{it} = \frac{C_{it}}{q} = \frac{C_{LF} - C_{HF}}{q \left(1 - \frac{C_{LF}}{C_{IN}} \right) \left(1 - \frac{C_{HF}}{C_{IN}} \right)} \quad (2.23)$$

where C_{LF} and C_{HF} are the measured capacitance values (C_m) at low and high frequencies, as shown in Fig. 2.28 (b).

Fig. 2.28 Simplified equivalent circuit of a MIS diode for interface state density calculation by “*hi-lo* frequency” method.

Another widely-used and reliable method to measure the interface trap densities is the AC conductance technique [65]. To further simplify the analysis, the C_{IN} in the circuit of Fig. 2.29 (a) can be subtracted and the part inside the dashed frame can be de-embedded. The C_b and C_d in series can be combined as one element C_d' . After Thevenin transformation, the circuit of Fig. 2.29 (b) can be described as Fig. 2.29 (c), that is, a conductance G_p in parallel with a capacitance C_p . The frequency dependent values of G_p can be used to calculate the interface trap densities.

Fig. 2.29 Simplified equivalent circuit for a MIS diode.

If the traps have a single energy level, the value of $\frac{G_p}{\omega}$ can be expressed as:

$$\frac{G_p}{\omega} = \frac{q^2 N_{it}}{kT} \left(\frac{\omega \tau}{1 + \omega^2 \tau^2} \right) \quad (2.24)$$

where N_{it} is the trap density, k is the Boltzmann constant and ω is the angular

frequency. $\frac{G_p}{\omega}$ reaches its peak at $\omega \tau = 1$:

$$\left(\frac{G_p}{\omega} \right)_{\max} = \frac{q^2 N_{it}}{kT} \quad (2.25)$$

If the traps have an energy level continuum, $\frac{G_p}{\omega}$ can be expressed as:

$$\frac{G_p}{\omega} = qD_{it} \left(\frac{\ln(1 + \omega^2 \tau^2)}{2\omega \tau} \right) \quad (2.26)$$

It will reach its peak at $\omega \tau = 1.95$:

$$\left(\frac{G_p}{\omega} \right)_{\max} = 0.403 qD_{it} \quad (2.27)$$

If the MIS diode has a large gate area and the fluctuation of surface potential (u_s) is needed to be considered, the statistical model is needed to be adopted under the assumption of random fluctuation for u_s :

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2} (2\pi\sigma_s^2)^{-\frac{1}{2}} \int_{-\infty}^{\infty} \exp\left(-\frac{(u_s - \overline{u_s})^2}{2\sigma_s^2}\right) \cdot \frac{1}{\omega\tau} \cdot \ln(1 + \omega^2\tau^2) du_s \quad (2.28)$$

where $\overline{u_s}$ and σ are the mean value and standard deviation of u_s in units of kT/q ,

that is, $u_s = \frac{\Psi_s}{kT/q}$ and $\overline{u_s} = \frac{\overline{\Psi_s}}{kT/q}$. The values of D_{it} and τ can be obtained by fitting

the curve of $G_p/\omega \sim \omega$ using the above equation.

Fig. 2.30 shows the measured interface trap density using different techniques for ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS structure, where (a) shows the results measured by the “*hi-lo* frequency” method and (b) shows those measured by AC conductance method. E_T is the trap energy level from the conduction band bottom and calculated by:

$$E_T = -k_B T \ln(\tau\sigma_T N_C v_t) \quad (2.29)$$

where k_B is the Boltzmann constant, T is the temperature and here $T=300\text{K}$, σ_T is the capture cross section of the traps, N_C is the effective density of states at the bottom of the conduction band, v_t is the average thermal velocity of the electrons. It is assumed that $\sigma_T=3.4\times 10^{-15} \text{ cm}^2$, $N_C=4.3 \times 10^{14} \times T^{3/2} \text{ cm}^{-3}$, and $v_t=2.6 \times 10^7 \text{ cm/s}$ [66].

As shown in Fig. 2.30 (b), regarding the AC conductance method with different models, the results by the multilevel model and single level model are consistent with those by the statistical model, indicating that the surface potential

Fig. 2.30 Measured interface trap density using different techniques for ALD $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ MIS structure: (a) by *hi-lo* frequency method; (b) by AC conductance method.

fluctuation can be ignored in the fabricated MIS diode even with a large gate area up to 300 μm diameter. This reveals the good uniformity of ALD deposited thin dielectric film. On the other hand, the trap density measured by “*hi-lo*” method is lower than that from the AC conductance, which is believed to be from the inaccuracy of the “*hi-lo* frequency” method. This is partially due to the slight difference in the values of the threshold voltage at the high-frequency and low-frequency measurements [67]. However, it turned out that the magnitudes of the interface state density measured by two methods are similar, indicating that the “*hi-lo* frequency” method is still valuable for quick and rough estimation of the dielectric interface quality.

2.2.4 Characteristics of the ALD grown Al_2O_3 film

At the early stage of this work, the quality of the ALD grown Al_2O_3 was bad due to the un-optimized growth conditions. Their typical C-V characteristics are like those shown in Fig. 2.26 (a) and Fig. 2.27 (a). After optimization of the ALD system setup and growth conditions (including introducing a more powerful pump for better purging purpose and increase the purge time), the quality of the grown Al_2O_3 was greatly improved, with typical C-V characteristics as shown in Fig. 2.26 (b) and Fig. 2.27 (b). The main physical and electrical characteristics of the improved ALD- Al_2O_3 are listed in Table 2.3 and shown in Fig. 2.31.

Table 2.3 The main physical and electrical characteristics of the improved ALD-
Al₂O₃.

Characteristics	Value
Growth rate (nm/cycle)	~0.1
Thickness uniformity	<1.7% for 3 inch wafer
Refractory index	1.64 at $\lambda=630$ nm
Dielectric Constant	8.6 (Fig. 2.31(a))
Breakdown field (MV/cm)	4.7 (Fig. 2.31 (b))
Interface trap density (cm ⁻² eV ⁻¹)	<2x10 ¹² (Fig. 2.30)

Fig. 2.31 Measured (a) capacitances versus frequency (b) I - V characteristics for a metal-insulator-metal (MIM) structure with size of $200 \times 200 \mu\text{m}^2$. ALD Al₂O₃ with thickness of 10 nm was used as the insulator.

Chapter 3

Studies on the Off-State Breakdown Mechanisms in AlGaIn/GaN HEMTs

3.1 Introduction

As described in the first chapter, one of the most important advantages of GaN HEMTs for microwave low noise applications over other types of microwave transistors such as GaAs FETs and HEMTs is the high breakdown voltage. The high breakdown voltage enables the LNAs based on GaN HEMTs to eliminate the need for extra RF limiters, as illustrated by Fig. 1.2, and hence improves the overall noise performance and the dynamic range of the front end. The off-state breakdown voltage directly determines the upper limit of the ideal output power for a GaN HEMT at class-A operations [2], as Eqn. (1.1) shows. The ability of high output power together with low noise is also a favorite feature for GaN HEMTs to be applied in LNAs [68].

To further improve the breakdown characteristics in GaN HEMTs through device structure and fabrication process optimization, it is essential to understand their physical breakdown mechanisms. However, until now there are still very limited publications on the study of breakdown mechanisms in GaN HEMTs [69, 70, 71]. A systematical study on the mechanisms of channel breakdown and gate-drain breakdown in GaN HEMTs is still not available.

In this chapter we have carried out a systematic study of the three-terminal off-state breakdown mechanism in AlGaIn/GaN HEMTs on silicon substrate. Temperature dependent drain current injection (DCI) and side-gate techniques

were used to investigate the off-state channel breakdown and gate-drain breakdown behaviors for different device structures. Through this analysis on the behavior of the gate current at high and low temperatures with varying gate-drain field, the physical mechanisms for the different breakdown behaviors were discussed.

3.2 Experiments

Two samples of AlGaN/GaN HEMT were used for the study in this work as shown in Fig. 3.1: (a) Sample A, from top to bottom, comprises of a 2 nm GaN cap layer, a 25 nm undoped $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier layer, a 1.2 nm AlN spacer layer, a 2 μm undoped GaN buffer, and a transition/nucleation layer; (b) Sample B, from top to bottom, comprises of a 2 nm GaN cap layer, a 17.5 nm undoped $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier layer, a 1.5 μm undoped GaN buffer, and a transition/nucleation layer. Both samples are grown on high-resistivity Si (111) substrates using MOCVD.

The fabrication processes were the same as those described in Chapter 2. For both samples, additional probe pads so-called “side gate” were intentionally fabricated to collect the holes generated by channel impact ionization as stated in [72]. The side gates were realized by the combination of ICP etching into the buffer layer and ohmic contact formation.

Fig. 3.1 Schematics of the AlGaN/GaN HEMTs: (a) Sample A, its surface was un-passivated and the device was with a 1 μm gate; (b) Sample B, its surface was passivated by 120 nm SiN and the device was with a 0.25 μm gate.

The measured device on Sample A has a gate-to-source distance $L_{gs}=2.0\ \mu\text{m}$, a gate-to-drain distance $L_{gd}=3\ \mu\text{m}$ and a gate width $W_g=50\ \mu\text{m}$, while the measured device on Sample B has a gate-to-source distance $L_{gs}=1.0\ \mu\text{m}$, a gate-to-drain distance $L_{gd}=2\ \mu\text{m}$ and a gate width $W_g=50\ \mu\text{m}$. During the DCI measurement, the side gate was biased at -20 V. The DC measurements were carried out using an HP 4156B semiconductor parameter analyzer.

3.3 Results and Discussion

(A) *Three-terminal off-state breakdown characteristics measured by DCI technique*

When the gate of a HEMT device is biased below the pinch-off voltage, the channel conduction is closed and the device breakdown characteristic is called the “off-state” breakdown. One common technique used to measure the drain-source off-state breakdown voltage BV_{DS} is by ramping up the drain voltage from a low value until it reaches a critical point when the drain current increases sharply [73]. This is a destructive method and will easily cause the device to burn out.

A more stable and repeatable breakdown measurement technique, called “drain-current injection technique”, has been developed by S. R. Bahl et al. for FETs [74]. The schematic diagram of the DCI measurement is shown in Fig. 3.2. During the measurement, the source was grounded and the drain was being injected with a fixed current $I_d=1$ mA/mm for Sample A and $I_d=4$ mA/mm for Sample B. The higher drain current for Sample B is due to the relatively higher

Fig. 3.2 Schematic of circuit diagram during the off-state breakdown characterization using the drain current injection technique.

Schottky gate current in Sample B. Since our purpose in this work is to understand qualitatively the breakdown behaviors and not to compare their absolute values, hence the different drain currents used in the DCI characterization would not affect the findings. The gate bias V_g was ramped down from $V_g=0$ V when the channel was open to $V_g = -10$ V when the channel was pinched off. The gate current I_g , side gate current I_{sg} , and the drain voltage with respect to the source V_{ds} were monitored. The drain voltage with respect to the gate V_{gd} was calculated using $V_{gd}=V_{ds}-V_g$.

Fig. 3.3 shows the typical DCI characteristics at room temperature for Sample A. The DCI characteristics of Sample B are similar to those of Sample A and also those of GaAs and InP HEMTs [74]. When the gate bias is ramped down from zero to highly negative values, the drain voltage and gate current enter four distinct regions sequentially: ohmic (Region I), sub-threshold (Region II), channel breakdown (Region III) and gate-drain breakdown (Region IV).

Around the starting point at $V_g=0$, the device is on and the channel conductance is high, and thus, only a small V_{ds} close to zero is needed to meet the drain current $I_d=1$ mA/mm. V_{dg} is also very small, slowly increasing with the decrease of V_g . I_g is very low due to the small V_{dg} . This region is called the ohmic region (Region I). Then V_g is further ramped down to below threshold voltage V_{th} , causing the channel to shut off the channel is shut off quickly. V_{ds} is needed to increase sharply to accommodate the constant I_d being injected into the drain. The device is then driven into channel breakdown, and enters the channel breakdown region (Region III). Between the channel breakdown and the ohmic region there exists a narrow sub-threshold region (Region II), which is due to the soft pinch-off characteristics of the HEMT caused by the short-channel effect. At the start of Region III, it can be confirmed that the channel breakdown rather than gate-drain

Fig. 3.3 Typical drain-current injection characteristics for Sample A.

breakdown occurs, for the reason that here I_g is still much smaller than I_d , and most of the current flows out of the source. At the same time I_{sg} starts to rise, which indicates that the holes generated by the impact ionization in the channel are collected by the side-gate. Thus, I_{sg} is an effective indicator of the channel impact ionization. The off-state channel breakdown voltage BV_{CH}^{OFF} is then defined as the V_{ds} at the start of Region III, or when I_g or I_{sg} shows a significant rise.

In Region III, with V_g becomes more negative, the depletion of the channel electrons is enhanced, thus higher V_{ds} , and thereby higher impact ionization, are needed to keep the impact ionization current constant. Correspondingly, more holes are generated by the increasing V_{ds} and collected by the side gate. At the same time, V_{dg} is also increased, which increases the gate-drain electrical field and leads to the further increase of gate current, and more holes are collected by the gate. As a result of the combination of these two opposite mechanisms, I_{sg} rises up to a peak value and then ramps down.

When $I_g=I_d$ and $I_s=0$, all the current injected from the drain flows out of the gate and $I_{sg}\sim 0$ (the reverse-biased source gate diode current is negligible). This configuration is equivalent to a two-terminal drain-gate measurement with source floating. The gate-drain breakdown voltage BV_{GD}^{OFF} is then defined as the V_{dg} at this point. Beyond that point, namely, in Region IV, the gate-drain breakdown is dominant and I_d is dependent on V_{dg} . Because the drain current is kept constant, V_{dg} is also needed to remain constant and does not change with the decrease of V_g . Since $V_{ds}=V_{dg}+V_g$, the locus of V_{ds} shows a peak and then decreases linearly with V_{gs} with a slope of one.

(B) Temperature dependent breakdown measurement

To investigate the physical mechanism of the off-state channel breakdown and gate-drain breakdown in the AlGaIn/GaN HEMT, temperature dependent DCI measurement was carried out from 25 °C to 150 °C at a step of 25 °C. Fig. 3.4 and Fig. 3.5 show the temperature dependent DCI behaviors for Sample A and Sample B, respectively. The BV_{CH}^{OFF} values were read with the assistance of the I_{SG} bell shape curve. For Sample A, at temperature >100 °C, the V_{ds} versus V_g curve shows an abnormal curve and the BV_{CH}^{OFF} is difficult to be accurately extracted. More experiments are needed to explore the physical mechanics of these two temperature points. However, the trends of the BV_{CH}^{OFF} and BV_{GD}^{OFF} with the increase of temperature can still be clearly obtained.

Fig. 3.4 Temperature dependent three-terminal off-state breakdown characteristics measured by DCI technique for Sample A from 25 to 150 °C at the step of 25 °C.

Fig. 3.5 Temperature dependent three-terminal off-state breakdown characteristics measured by DCI technique for Sample B from 25 to 150 °C at the step of 25 °C.

Fig. 3.6 summarizes the temperature dependence of the BV_{CH}^{OFF} and BV_{GD}^{OFF} for Sample A and B. The BV_{CH}^{OFF} is found to have negative temperature coefficients for both samples. The shape of the DCI curves and SG current curves confirm that this breakdown happens in the GaN channel due to the impact ionization, not due to the current transport at the gate-drain surface or in the gate-drain barrier layer. The negative temperature coefficient indicates that the impact ionization in GaN channel is enhanced by high temperatures.

Fig. 3.6 Summarized temperature dependence of channel breakdown voltages BV_{CH}^{OFF} and gate-drain breakdown BV_{GD}^{OFF} for Sample A and Sample B.

The impact ionization induced current can be expressed as [75]:

$$I_{II} = \alpha_n (E_{\max}) \Delta L I_{ds} \quad (3.1)$$

where $\alpha_n(E_{\max})$ is the impact ionization coefficient for electrons as a function of maximum electrical field $E_{\max}$, ΔL is the effective length of $E_{\max}$ region. According to the Wolff model [76], α_n can be expressed as:

$$\alpha_n(E_{\max}) = \frac{qE_{\max}}{E_i} \exp\left(-\frac{3E_p E_i}{(qE\lambda)^2}\right) \quad (3.2)$$

where E_i is the threshold voltage for electron-hole pair generation, E_p is the effective energy of the phonons involved in the scattering process, λ is the phonon scattering mean free path, and q is the electron charge. E_i is proportional to the bandgap E_g . For GaN it can be expressed as [77]

$$E_i = E_g \left(1 + \frac{m_c^*}{m_c^* + m_v^*}\right) \quad (3.3)$$

where m_c^* and m_v^* are the effective electron mass and hole mass respectively. The temperature dependence of the impact ionization is determined mainly by two physical phenomena. The first mechanism is the shrinkage of the band-gap E_g (Eqn. (4)), described by the following equation [78]:

$$E(T) = E(0) - \frac{\alpha T^2}{\beta + T} \quad (3.4)$$

where α and β are two coefficients and their values can be found in literature. The second mechanism is due to the enhanced scattering, as a result of the enhanced crystal lattice vibration at higher temperature (determining the λ in Eqn. (3.2)). The former mechanism enhances the impact ionization, while the latter weakens it.

Due to the wide band-gap of GaN, generally the band-gap shrinkage at high temperatures cannot be the dominant mechanism to determine the temperature dependence of the impact ionization in GaN HEMTs. Some groups have observed that the impact ionization in GaN HEMTs on SiC and sapphire substrates is reduced at high temperatures [69, 71]. Therefore, the enhancement of the GaN channel impact ionization by the high temperatures observed in our experiment should be related to the effect of the defects in the buffer. People have found that the defects in the SiC diode can result in the increasing impact ionization coefficient with the increase of the temperature [79].

As for the gate-drain breakdown, it is found that in Sample A, BV_{GD}^{OFF} has a positive temperature coefficient, while in Sample B it shows a negative temperature coefficient. The physical mechanisms possibly responsible for the off-state gate-drain breakdown are much more complicated than the channel breakdown. These include surface hopping transport [70, 80], impact ionization [81] and the carrier transport through AlGaIn barrier such as conventional thermal emission / thermionic field emission / field emission (TE/TFE/FE) [81, 82], thin-surface-barrier (TSB) enhanced TFE/FE [83], trap assistant tunneling (TAT) [84, 85]. Among these mechanisms, the impact ionization can have either a negative temperature coefficient or positive temperature coefficient, depending on whether the shrinkage of band gap or enhancement of the lattice scattering is dominant at higher temperatures, as Eqn. (3.1)-(3.4) shows. As a result, the BV_{GD}^{OFF} determined by impact ionization can also have either a positive or negative temperature coefficient. However, all the carrier transport mechanisms have a positive temperature coefficient, which leads to a negative temperature coefficient of BV_{GD}^{OFF} . Hence the positive temperature-coefficient BV_{GD}^{OFF} in Sample A is believed to arise from the impact ionization; but for the case in Sample B, the BV_{GD}^{OFF} has a negative temperature coefficient and it is difficult to distinguish which physical mechanism is the predominant. To determine which one is the dominate mechanism responsible for the gate-drain breakdown, extra experiment and analysis are required. In the next part, the study of the gate current behavior at high drain-gate biases and at high temperatures is further carried out.

(C) Temperature dependent reverse gate leakage current

For the off-state gate drain breakdown, as M. H. Somerville et. al. has proposed, mainly two different possible mechanisms are involved: the carrier

transport of TFE/tunneling and the impact ionization [81]. They can be differentiated through the analysis of the temperature dependent and bias dependent gate current. Under different mechanisms, the trends of the ratio of high-temperature gate current ($I_{g,HT}$) to low-temperature gate current ($I_{g,LT}$) varied with the gate-drain field are different. For the TFE/tunneling limited breakdown, the $I_{g,HT}$ and $I_{g,LT}$ should converge and their ratio decreases to 1 at higher biases. For the breakdown limited by impact ionization with negative temperature coefficient, the $I_{g,HT}$ and $I_{g,LT}$ should display a “twist” (See Fig. 2 in [81]) and their ratio decreases to below 1 at higher biases. And for the breakdown limited by impact ionization with positive temperature coefficient, the $I_{g,HT}$ and $I_{g,LT}$ should diverge and their ratio is more than unity and increases with temperature.

The gate current in Sample A at different temperature as a function of drain-gate bias, together with the ratio of $I_{g,HT}$ to $I_{g,LT}$ (in this work 25 °C was taken as the low temperature), are plotted in Fig. 3.7 and Fig. 3.8, respectively. The gate current curves at different temperatures show a twist at $V_{dg} \approx 15$ V. Before the twist, the gate current increases with temperature at the same V_{dg} . This indicates that the TFE/TT dominates in the gate current. After the twist, especially at high V_{dg} , The value of $I_{g,HT}/I_{g,LT}$ decreases to below 1 (for Temperature > 50 °C) at high gate drain field. This indicates that in Sample A, the gate-drain breakdown is dominated by the impact ionization in gate-drain region with a negative temperature coefficient. The carrier scattering by the phonons at high temperatures is responsible for this negative temperature coefficient. This gate-drain breakdown is most likely related to the impact ionization near the surface layers, because there exists a stronger electrical field due to the large density of surface states compared to the AlGaN bulk (See Fig. 3.11).

Fig. 3.7 Gate-drain leakage current at different temperatures as a function of gate-drain bias for Sample A. The two small figures above are zoomed pictures for the special parts before and after the twist.

Fig. 3.8 The ratio of gate-drain current at high temperature $I_{g, HT}$ to that at low temperature (25 °C) $I_{g, LT}$ for Sample A.

However, for Sample B, as shown in Fig. 3.9 and Fig. 3.10, the gate currents at different temperatures diverge at high gate-drain field and the value of $I_{g, HT}/I_{g, LT}$ shows a minimum then increases again when gate-drain field increases. This suggests that the impact ionization with a positive temperature coefficient determines the gate-drain breakdown in sample B, and the impact ionization occurs at the channel. The dominant physical mechanism of the impact ionization is related to the defects in the buffer.

The cause of the different physical scenario in gate-drain breakdown between Sample A and B is not very clear. One possible reason is related to the lack of AlN spacer and a thinner AlGaIn barrier in Sample B. In sample B, the electrons are

easier to transport through AlGaN barrier from gate to channel, and the holes are also easier to transport from channel to gate, compared to that in sample A. This is due to the lack of barrier height enhancement by AlN spacer, and also contributed from the stronger electrical field caused by the thinner AlGaN layer. So the impact ionization in the channel is dominant in the gate-drain breakdown in Sample B, but not in Sample A. Another possible reason is related to the surface passivation in Sample B, which reduces the surface charge density and enhances the electrical field peak in the channel. However, more experiments on samples with different structures are needed to be carried out to determine the exact cause.

Fig. 3.9 Gate-drain leakage current at different temperatures as a function of gate-drain bias for Sample B.

Fig. 3.10 The ratio of gate-drain current at high temperature $I_{g,HT}$ to that at low temperature (25 °C) $I_{g,LT}$ for Sample B.

3.4 Conclusion

In conclusion, the three-terminal off-state breakdown mechanisms in AlGaIn/GaN HEMTs on Si substrate were comprehensively investigated through the temperature dependent DCI and side-gate techniques. Negative temperature coefficients for channel breakdown, as well as both positive and negative temperature coefficients for gate-drain breakdown, were observed for the AlGaIn/GaN HEMTs with different device structures. It is found that the impact ionization in GaN channel is enhanced at high temperatures. Two impact ionization mechanisms with different temperature coefficients were believed to be responsible for the gate-drain breakdown.

Fig. 3.11 Schematic band diagrams illustrating the possible locations of impact ionization responsible for the gate-drain breakdown for Sample A and Sample B.

Chapter 4

Extraction and De-embedding Procedure Developed For Microwave Small-Signal and Noise Modeling

4.1 Introduction

A circuit model of a microwave device is necessary for circuit designers to design and predict the system performance under various conditions, such as at various frequencies, or biases, or temperatures etc. The equivalent circuit parameters (ECPs) form the basis of a microwave small signal model and noise model. The values of the small signal ECPs at a wide range of biases are also used to derive the large signal model in the bottom-up modeling technique. Furthermore, in many cases ECPs are helpful to analyze and understand the physical mechanisms of various figures-of-merits for microwave and low noise applications, such as f_T , f_{max} , NF_{min} , stability factor etc., and hence they can be used as a guide to design the device structure and/or processes to improve the device performance.

When integrated in the actual monolithic microwave integrated circuit (MMIC) LNA systems, the layout of the electrodes of the transistors are different from the discrete devices as additional large probe pads are required for microwave measurement. Thus the intrinsic noise parameters are required to be de-embedded from the measured extrinsic data, in order to extract the intrinsic device characteristics for circuit design. In addition, the different noise sources need to be distinguished to comprehensively study the physics behind the behaviors of the high-frequency noise characteristics which are affected by many parameters such as structure design, processes, temperature and biasing.

For GaAs and InP HEMTs, the procedures in extracting the small signal ECPs and de-embedding the noise sources have been well developed [86, 87, 88, 89]. However, for GaN HEMTs, some special considerations such as the relatively high ohmic contact resistances have to be taken into account when extracting the model [90, 91]. In this chapter we have successfully developed procedures to extract the values of the small signal equivalent circuit elements and to de-embed the internal noise sources for GaN HEMT modeling. The procedure is also suitable for GaN MISHEMT.

Our developed extraction and de-embedding approach has the following advantages over those reported in the literatures [90, 91, 92, 93, 94, 95].

1) A distributed small-signal model with 22 elements [91] is adopted. This model separates the parasitic capacitive effects of the interelectrode and crossover from those effects from the pads, and thus can be used widely and is suitable for the large gate-periphery devices. It also includes the elements to account for the large gate leakage current, which is typically observed in the conventional HEMT with Schottky metal gate.

2) A separate test structure, namely a dummy “OPEN” structure, is used to determine the parasitic capacitances from the pads. By this means the complex process of the bi-directional optimization based on the initial value estimation through empirical and algebraic assumption, as used in [91], can be avoided.

3) A zero gate bias is used in the cold FET method to extract the parasitic inductances and resistances, rather than a high forward gate bias traditionally used in GaN HEMTs to shunt the effect of gate capacitance [89, 93]. This can avoid the potential damage to the device due to the high forward gate voltage. And this

method also makes the extraction approach suitable for a MISHEMT, in which a high gate bias will permanently fail the gate dielectric.

4) When to determine the element values from the measured data over a series of frequencies, linear regression is tried to be used, rather than a simple averaging. This can avoid many errors arising from the simplification of the model. The actual circuit is more complex than the model and some residue terms have been neglected in the simplified analytical expression. The method of linear regression can significantly reduce the errors from such residue terms.

5) The whole small signal extraction and noise de-embedding procedure is easy to be programmed using a generally-used scientific computation tool, e. g., MATLAB, and thus, is suitable for the microwave CAD applications.

This chapter is organized as follows. The first section gives a brief introduction. In the 2nd section, the small signal ECP extraction procedures are described, including techniques of dummy OPEN test structure, cold pinched-off and cold channel-on for parasitic element determination, linear regression of re-defined parameter for intrinsic element determination, and the final optimization. The noise de-embedding procedure is described in 3rd section. Based on the noise theory of a linear two-port network and by means of noise correlation matrix technique, the influences of the extrinsic circuit are subtracted and the intrinsic noise parameters and noise source currents are obtained. The extraction procedure is verified in the last section by comparing with the measured data.

4.2 Small Signal Model and Extraction Procedure for Equivalent Circuit Parameters (ECPs)

Fig. 4.1 The schematic of the cross section and the physical origins of the small-signal ECPs for a GaN HEMT.

The small signal equivalent circuit for a GaN HEMT with 22 elements is shown in Fig. 4.1 and Fig. 4.2. Fig. 4.2 shows the schematic of the cross-section and physical origins of the circuit elements, and Fig. 4.2 (a) and (b) show its intrinsic and extrinsic equivalent circuits, respectively. Among these circuit elements, the resistances R_{fs} and R_{gd} account for the gate-source and gate-drain leakage current. C_{gs} and C_{gs} are the capacitances between the gate and source side of the channel and that between the gate and the drain side of the channel respectively. R_{gs} is the channel charging resistance and it is included to account for the time delay of the charge at the source side of the channel in response to the gate signal. Its physical origin is complex and some people treat it as the physical resistance of the input part of the channel [96]. Similar to R_{gs} , R_{gd} is the gate-drain charging resistance reflecting the time delay between the charge at the drain side of the channel and the gate signal. g_m is the transconductance, and τ accounts for the

time delay between the channel current and the gate voltage. C_{ds} is the channel capacitance between the drain and source. R_{ds} is the output resistance.

Fig. 4.2 (a) Equivalent intrinsic circuit and (b) the extrinsic elements accounting for the parasitic electrode effect and access resistances for a GaN HEMTs.

The parasitic elements include the parasitic capacitances C_{pgo} , C_{pdo} , C_{pgdo} , C_{pgi} , C_{pdi} , C_{pds} , parasitic inductances L_G , L_D , and L_S , and access resistances R_g , R_d and R_s . C_{pgo} and C_{pdo} account for the pad-to-buffer/substrate capacitances and the pad-to-ground/source capacitances for gate and drain, respectively. The C_{pgdo} reflects the

capacitance between the gate and drain pads. The parasitic capacitances due to the measurement equipments, probes and probe tip-to-device contact transitions have been de-embedded before the measurement by the line-reflect-reflect-match (LRRM) calibration method [97]. C_{pgi} , C_{pdi} , and C_{pgdi} account for the capacitances between the interconnect metals of gate, drain and source. L_g , L_s and L_d account for the parasitic inductances of the pad, interconnect and electrode metal. R_g accounts for the distributed gate resistances arising from the gate metal at microwave frequencies. R_s and R_d comes from the ohmic contact resistance in series with the AlGaIn/GaN wafer resistance at the gate to source region and gate to drain region, respectively.

The flow chart of the extraction procedure is shown in Fig. 4.3. The small signal ECP extraction procedure includes mainly five steps: 1) With the aid of a dummy test structure fabricated together with the actual devices at the same wafer, the extrinsic capacitances of C_{pgo} , C_{pdo} and C_{pgdo} are extracted; 2) The device is measured at cold pinched-off condition, that is, at the biases of $V_d=0$ and $V_g < V_{th}$, and the extrinsic capacitances of C_{pgi} , C_{pdi} and C_{pgdi} are extracted from the measured S parameters and the results from the first step; 3) The device is measured at cold channel-on condition at the biases of $V_d=0$ and $V_g=0$, and the parasitic inductances and access resistances are extracted from the measured S parameters and the results from the previous two steps; 4) The extrinsic elements which have been obtained from the previous steps are subtracted from the measured S parameters for the whole device at the same bias. The intrinsic Y parameters are then obtained and the intrinsic circuit elements are extracted. 5) The optimal parameter values are finally obtained by an optimization program based on those values already obtained in the above four steps.

Fig. 4.3 Flow chart of the small signal ECP extraction procedure.

Step 1. “OPEN” test structure

The first step is to determine the values of C_{pgo} , C_{pdo} and C_{pgdo} with the aid of a separate test structure intentionally fabricated on the same wafer using the same process. This structure has the metal pads with same size as the actual device but no active region. Fig. 4.4 (a) shows the layout of this “open” test structure and (b) shows its equivalent circuit.

Fig. 4.4 (a) Layout of the OPEN test structure fabricated on the same wafer with the GaN HEMTs and (b) its equivalent circuit

The Y parameter of the “open” pattern as shown in Fig. 4.4 is:

$$[Y_{ts_op}] = \begin{bmatrix} Y_{11O} & Y_{12O} \\ Y_{21O} & Y_{22O} \end{bmatrix} \quad (4.1)$$

And the following expressions can be obtained:

$$\begin{cases} \text{Im}[Y_{11O}] = \omega(C_{pgo} + C_{pgdo}) \\ \text{Im}[Y_{12O}] = \text{Im}[Y_{21O}] = -\omega C_{pgdo} \\ \text{Im}[Y_{22O}] = \omega(C_{pdo} + C_{pgdo}) \end{cases} \quad (4.2)$$

Then the C_{pgo} , C_{pdo} and C_{pgdo} can be calculated by:

$$\begin{cases} C_{pgo} = \frac{1}{\omega} \left(\text{Im}[Y_{11O}] + \frac{\text{Im}[Y_{12O}] + \text{Im}[Y_{21O}]}{2} \right) \\ C_{pdo} = \frac{1}{\omega} \left(\text{Im}[Y_{22O}] + \frac{\text{Im}[Y_{12O}] + \text{Im}[Y_{21O}]}{2} \right) \\ C_{pgdo} = -\frac{1}{\omega} \left(\frac{\text{Im}[Y_{12O}] + \text{Im}[Y_{21O}]}{2} \right) \end{cases} \quad (4.3)$$

Step 2. Measurement under cold pinched-off condition ($V_d=0$, $V_g < V_{th}$)

Under the condition of pinched-off and $V_d=0$, the circuit in Fig. 4.2 can be simplified as Fig. 4.5. Under this condition, the channel is turned off and there is no current flow, so $g_m=0$ and $R_{ds}=\infty$. The source and drain side of the channel are symmetric and $C_{gso}=C_{gdo}$. The influences of the parasitic inductances L_g , L_d and L_s and the access resistances on the Y-parameters are very small. So the circuit can be simplified into the one shown in Fig. 4.5. The values of C_{pgo} , C_{pdo} and C_{pgdo} have been obtained in the first step and can be easily subtracted by calculation. The imaginary part of the Y-parameters for the elements defined by the dashed frame can be expressed as:

Fig. 4.5 The equivalent circuit of GaN HEMTs under cold pinched-off conditions ($V_d=0$, $V_g < V_{th}$).

$$\begin{cases} \text{Im}[Y_{11}] = \omega(C_{pgi} + C_{pgdi}) + \omega(C_{gso} + C_{gdo}) \\ \text{Im}[Y_{12}] = \text{Im}[Y_{21}] = -\omega C_{pgdi} - \omega C_{gdo} \\ \text{Im}[Y_{22}] = \omega(C_{pdi} + C_{pgdi}) + \omega(C_{dso} + C_{gdo}) \end{cases} \quad (4.4)$$

There are five unknowns in the above equations, thus it is necessary to provide more assumptions to get the solution. One is $C_{pgdi}=0$, in view of the fact that the value of C_{pgdi} is much smaller than the others. The other is as for C_{dso} , and at the first run of calculation it has to be set to zero. Its optimal value will be determined by an optimization procedure at the last step. The procedure for this step is summarized as below:

- (1) Measure the S parameters for the device biased at $V_d=0$ and $V_g < V_{th}$;
- (2) Convert the measured S parameter into Y parameter: $[S_{ColdPO}] \rightarrow [Y_{ColdPO}]$.
- (3) De-embed the Y parameters of the circuit elements inside the dashed box in Fig. 4.5 using:

$$\begin{aligned} [Y] &= [Y_{ColdPO}] - [Y_{po}], \\ [Y_{po}] &= [Y_{ts_op}] \approx \begin{bmatrix} j\omega(C_{pgo} + C_{pgdo}) & -j\omega C_{pgdo} \\ -j\omega C_{pgdo} & j\omega(C_{pdo} + C_{pgdo}) \end{bmatrix} \end{aligned} \quad (4.5)$$

- (4). From Eqn. 4.4, one can solve the values of C_{pgi} and C_{pdi} .

Step 3. Measurement under “Cold Channel-open” condition ($V_d=0$, $V_g=0$)

To extract the values of parasitic inductance and access resistances, a standard method has been widely used for the GaAs and InP MESFETs and HEMTs, that is, by biasing the gate at a strong forward voltage with $V_{ds}=0$ [88]. In such an operation, the gate current will be very high and the gate capacitance is shunt, and not only the g_m but also the capacitances inside the intrinsic circuit are ignored with only parasitic elements left. The inductances and access resistances can be

easily calculated after subtracting the parasitic capacitances. However, this method is difficult to be applied into the GaN HEMT and especially not possible for MISHEMT because a strong forward gate bias can easily deteriorate the devices. Furthermore, the gate turn-on voltage for MISHEMT is too large due to the existence of the gate insulator.

Thus a method similar to that generally applied in Si MOSFETs is suitable for GaN HEMTs to extract the extrinsic inductances and resistances, by which the gate is biased at zero instead of a strong forward value. At $V_d=0$ and $V_g=0$, zero g_m and negligible R_{ds} can be assumed and the equivalent circuit can be simplified into Fig. 4.6 [98]. The Z parameters for the circuit inside the dashed frame can be expressed as [99, 100]:

$$\begin{cases} \omega^2 \text{Re}[Z_{11}] = \omega^2 (R_g + R_s) + \Delta R_{11} \\ \omega^2 \text{Re}[Z_{22}] = \omega^2 (R_d + R_s) + \Delta R_{22} \\ \omega^2 \text{Re}[Z_{12}] = \omega^2 R_s + \Delta R_{12} \end{cases} \quad (4.6)$$

$$\begin{cases} \omega \text{Im}[Z_{11}] = \omega^2 (L_g + L_s) - \left(\frac{1}{C_g} + \frac{1}{C_s} \right) \\ \omega \text{Im}[Z_{22}] = \omega^2 (L_d + L_s) - \left(\frac{1}{C_d} + \frac{1}{C_s} \right) \\ \omega \text{Im}[Z_{12}] = \omega^2 L_s - \frac{1}{C_s} \end{cases} \quad (4.7)$$

The error term ΔR_{11} , ΔR_{22} and ΔR_{12} in Eqn. (3.6) account for the contribution of C_g , C_d and C_s to the real part of the measured Z parameters.

Fig. 4.6 The equivalent circuit of GaN HEMTs under cold channel-open conditions ($V_d=0$, $V_g=0$).

The values of R_g , R_s , R_d can then be calculated by fitting $\omega^2 \text{Re}[Z]$ versus ω^2 based on the above Eqn. (4.6), and the values of L_g , L_s and L_d can be calculated by fitting $\omega \text{Im}[Z]$ versus ω^2 based on the above Eqn. (4.7). The procedure at this step is summarized as below:

- (1) Measure the S parameters for the device biased at $V_d=0$ and $V_g=0$;
- (2) Convert the measured S parameter into Y parameter: $[S_{ColdCO}] \rightarrow [Y_{ColdCO}]$.
- (3) De-embed the Y parameters of the circuit elements inside the dashed box in Fig. 4.5 using:

$$[Y] = [Y_{ColdCO}] - [Y_{po}] - [Y_{pi}],$$

$$[Y_{pi}] = \begin{bmatrix} j\omega(C_{pgi} + C_{pgdi}) & -j\omega C_{pgdi} \\ -j\omega C_{pgdi} & j\omega(C_{pdo} + C_{pgdi}) \end{bmatrix} \quad (4.8)$$

- (4) Convert the obtained Y parameter into Z parameter: $[Y] \rightarrow [Z]$.

(5) Calculate the values of L_g , L_d , L_s and R_g , R_d , R_s by linear regression for $\omega^2 \text{Re}[Z]$ versus ω^2 and $\omega \text{Im}[Z]$ versus ω^2 based on the Eqn. (3.6) and (3.7).

Step 4. Directly extract the Intrinsic ECPs

After all the extrinsic ECPs have been obtained, the Y parameters of the intrinsic circuit $[Y_{\text{int}}]$ shown in Fig. 4.2 (b) can be easily extracted by subtracting the parasitic ECPs from the measured S parameter for the overall device. The $[Y_{\text{int}}]$ can be expressed by:

$$[Y_{\text{int}}] = \begin{bmatrix} Y_{11i} & Y_{12i} \\ Y_{21i} & Y_{22i} \end{bmatrix}$$

$$\left\{ \begin{array}{l} Y_{11i} = \frac{1}{R_{fs}} + \frac{1}{R_{fd}} + \frac{\omega^2 R_t C_{gs}^2}{D_1} + \frac{\omega^2 R_{gd} C_{gd}^2}{D_2} + j\omega \left(\frac{C_{gs}}{D_1} + \frac{C_{gd}}{D_2} \right) \\ Y_{12i} = -\frac{1}{R_{fd}} - \frac{\omega^2 R_{gd} C_{gd}^2}{D_2} - j\omega \frac{C_{gd}}{D_2} \\ Y_{21i} = -\frac{1}{R_{fd}} + \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_t C_{gs}} - j \frac{\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \\ Y_{22i} = \frac{1}{R_{fd}} + \frac{1}{R_{ds}} + \frac{\omega^2 R_{gd} C_{gd}^2}{D_2} + j\omega \left(C_{ds} + \frac{C_{gd}}{D_2} \right) \\ D_1 = 1 + \omega^2 R_{gs}^2 C_{gs}^2 \\ D_2 = 1 + \omega^2 R_{gd}^2 C_{gd}^2 \end{array} \right. \quad (4.9)$$

R_{fs} and R_{fd} can be obtained from the DC measurement. The other intrinsic ECPs can be directly solved as described in [101]. However, in the actual operation, to directly solve the ECPs generally produces significant errors for some elements, due to the unavoidable measurement uncertainties and the inaccuracies during the extraction of parasitic elements. The accuracy of the extracted intrinsic

ECPs can be improved by linear aggression for a series of new-defined variables, as proposed by Jarndal etc. in [91]. The detailed operations are described as follow.

The admittance of the intrinsic gate to source branch Y_{gs} is:

$$Y_{gs} = Y_{11i} + Y_{12i} = \frac{1/R_{fs} + j\omega C_{gs}}{1 + R_{gs}/R_{fs} + j\omega R_{gs}C_{gs}} \quad (4.10)$$

A new variable D_{Cgs} can be defined as:

$$D_{Cgs} = \omega \frac{|Y_{gs}|^2}{\text{Im}(Y_{gs})} = \frac{1/R_{fs}^2}{C_{gs}} + \omega^2 C_{gs} \quad (4.11)$$

Then the value of C_{gs} can be obtained by fitting the slope of D_{Cgs} versus ω^2 .

And a new variable D_{Rgs} can be defined as:

$$D_{Rgs} = \omega \frac{Y_{gs}}{\text{Im}(Y_{gs})} = \frac{1/R_{fs}^2 (1 + R_{gs}/R_{fs})}{C_{gs}} + \omega^2 R_{gs} C_{gs} - j \quad (4.12)$$

The value of R_{gs} can be obtained after fitting the slope of D_{Rgs} versus ω^2 and the slope is divided by C_{gs} . The admittance of the intrinsic gate to drain branch Y_{gd} is:

$$Y_{gd} = -Y_{12i} = \frac{1/R_{fd} + j\omega C_{gd}}{1 + R_{gd}/R_{fd} + j\omega R_{gd}C_{gd}} \quad (4.13)$$

A new variable D_{Cgd} can be defined as:

$$D_{Cgd} = \omega \frac{|Y_{gd}|^2}{\text{Im}(Y_{gd})} = \frac{1/R_{fd}^2}{C_{gd}} + \omega^2 C_{gd} \quad (4.14)$$

The value of C_{gd} can be obtained by fitting the slope of D_{Cgd} versus ω^2 . And a new variable D_{Rgd} can be defined as:

$$D_{Rgd} = \omega \frac{Y_{gd}}{\text{Im}(Y_{gd})} = \frac{1/R_{fd}^2 (1 + R_{gd}/R_{fd})}{C_{gd}} + \omega^2 R_{gd} C_{gd} - j \quad (4.15)$$

The value of R_{gd} can be obtained after fitting the slope of D_{Rgd} versus ω^2 and the slope is divided by C_{gd} . The admittance of the intrinsic transconductance branch Y_{gm} is:

$$Y_{gm} = Y_{21i} - Y_{12i} = \frac{g_m e^{-j\omega\tau}}{1 + R_{gs}/R_{fs} + j\omega R_{gs} C_{gs}} \quad (4.16)$$

A new variable D_{gm} can be defined as:

$$D_{gm} = \left| \frac{Y_{gs}}{Y_{gm}} \right|^2 = \left(\frac{1}{g_m R_{fs}} \right)^2 + \omega^2 \left(\frac{C_{gs}}{g_m} \right)^2 \quad (4.17)$$

The value of g_m can then be obtained by fitting the slope of D_{gm} versus ω^2 and then $g_m = \frac{C_{gs}}{\sqrt{\text{Slope}}}$. A new variable D_τ can be defined as:

$$D_\tau = \Phi \left[\left(\frac{Y_{gm}}{Y_{gs}} \right) \left(1/R_{fs} + j\omega C_{gs} \right) \right] = \Phi(g_m e^{-j\omega\tau}) = \omega\tau \quad (4.18)$$

The value of τ can then be obtained by fitting the slope of D_τ versus ω . The admittance of the intrinsic drain-to-source branch Y_{ds} is:

$$Y_{ds} = Y_{22i} + Y_{12i} = g_{ds} + j\omega C_{ds} \quad (4.19)$$

The value of g_{ds} can be obtained by fitting the slope of $\omega \text{Re}(Y_{ds})$ versus ω . And a new variable D_{Cds} can be defined as:

$$D_{Cds} = \text{Im}(Y_{ds}) = \omega C_{ds} \quad (4.20)$$

The value of C_{ds} can be obtained by fitting the slope of D_{Cds} versus ω .

The whole procedure to extract the intrinsic ECPs is summarized as below.

(1) Convert the measured S parameter of the whole device into Y parameter:

$$[S_{DUT}] \rightarrow [Y_{DUT}]$$

(2) Subtract the elements of the C_{pgo} , C_{pdo} and C_{pgdo} from the S parameters obtained at last step:

$$[Y_{DUT1}] = [Y_{DUT}] - [Y_{po}]$$

(3) Convert the obtained Y parameter into Z parameter:

$$[Y_{DUT1}] \rightarrow [Z_{DUT1}]$$

(4) Subtract the elements of the parasitic inductances L_g , L_d and L_s from the Z parameters obtained at last step:

$$[Z_{DUT2}] = [Z_{DUT1}] - [Z_L], [Z_L] = \begin{bmatrix} j\omega(L_g + L_s) & j\omega L_s \\ j\omega L_s & j\omega(L_d + L_s) \end{bmatrix}$$

(5) Convert the obtained Z parameter into Y parameter:

$$[Z_{DUT2}] \rightarrow [Y_{DUT2}]$$

(6) Subtract the elements of the parasitic capacitances C_{pgi} , C_{pdi} , C_{pgdi} from the Y parameters obtained at last step:

$$[Y_{DUT3}] = [Y_{DUT2}] - [Y_{pi}]$$

(7) Convert the obtained Y parameter into Z parameter:

$$[Y_{DUT3}] \rightarrow [Z_{DUT3}]$$

(8) Subtract the elements of the access resistances R_g , R_d and R_s from the Z parameters obtained at the last step:

$$[Z_{INT}] = [Z_{DUT3}] - [Z_R], [Z_R] = \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_g + R_s \end{bmatrix}$$

(9) Convert the obtained intrinsic Z parameter into Y parameter:

$$[Z_{INT}] \rightarrow [Y_{INT}], [Y_{INT}] = \begin{bmatrix} Y_{11i} & Y_{12i} \\ Y_{21i} & Y_{22i} \end{bmatrix}$$

(10) Calculate the various intrinsic ECPs by linear regression described at this step (Eqn. (4.10)-(4.20)).

Step 5. Optimization

The extracted values of small signal ECPs using the above procedures are still not accurate enough due to several factors: (A) During the determination of extrinsic capacitances in step 2, some assumptions on the values of a few elements have been made, for example, C_{ds} is assumed to be zero at $V_g < V_{th}$ and $V_d = 0$; (B) The extracted values for some elements are sensitive to the uncertainties of other elements, such as R_{gs} , which is sensitive to the value of R_g and R_s ; (C) There exist some errors in the measurement arising from the inaccuracies of the system calibration, machine resolution, contact between the microwave probe and the metal pad on wafer etc. So it is necessary to further fine tune the values for all the circuit elements. This optimization can be performed using commercial softwares like Agilent ADS or ICCAP, or using scientific computation tools such as MATLAB with self-written program codes etc.

The optimization criteria are generated as follows. After the initial direct extraction, the device's S parameters can be simulated using the obtained ECPs following the inverse procedure at step 4. The extraction error for the four elements of S parameters $\varepsilon_{ij}(S)$ can be calculated as:

$$\varepsilon_{ij}(S) = \frac{1}{N} \sum_{n=1}^N \frac{|S_{ij_sim_n} - S_{ij_mea_n}|}{|S_{ij_mea_n}|} \quad (i, j = 1, 2) \quad (4.21)$$

where $S_{ij_sim_n}$ and $S_{ij_mea_n}$ are the simulated and measured values of the S parameter element at the nth frequency point, respectively. Then the total error of the S parameters $\varepsilon_{mean}(S)$ can be taken as the mean value of those for four elements:

$$\varepsilon_{mean}(S) = \frac{1}{4} \sum_{i,j=1}^2 \varepsilon_{ij}(S) \quad (4.22)$$

The standard deviation of the errors for four elements $\varepsilon_\sigma(S)$ is also needed to be considered:

$$\varepsilon_\sigma(S) = \sqrt{\frac{1}{4} \sum_{i,j=1}^2 (\varepsilon_{ij}(S) - \varepsilon_{mean}(S))^2} \quad (4.23)$$

Then the optimization process is carried out repeatedly in order to minimize ε_{mean} and ε_σ through searching for the optimal values for those elements with some initially assumed values during the extraction procedure and for those elements which are of high uncertainties, such as C_{ds} , R_{gs} etc. Finally all small signal ECPs are determined.

4.3 Noise Model and De-embedding Procedure for Internal Noise Sources

The equivalent circuit for noise modeling employed in this thesis is shown in Fig. 4.7 including (a) extrinsic circuit and (b) its intrinsic circuit. The physical meanings of the elements have been described in the last section. The extrinsic elements of the equivalent circuit are considered to only generate Johnson noise through the three access resistances R_g , R_s and R_d as expressed by the Nyquist formula:

$$\begin{cases} \overline{i_{nR_g}^2} = 4kT_0\Delta f / R_g \\ \overline{i_{nR_s}^2} = 4kT_0\Delta f / R_s \\ \overline{i_{nR_d}^2} = 4kT_0\Delta f / R_d \end{cases} \quad (4.24)$$

where T_0 is the reference temperature and $T_0=290$ K, Δf is the frequency band, k is the Boltzmann constant.

To calculate the intrinsic drain noise source current and gate noise source current, the intrinsic noise parameters in Fig. 4.7 (b) are needed to be de-embedded first. The development of the de-embedding procedure is based on the theory for noisy linear two-port networks [102] and using the noise correlation matrices for calculation. The basic idea of the de-embedding procedure is to mathematically subtract the effect of the extrinsic elements on the overall noise parameters so that the intrinsic values are then obtained. Before the de-embedding procedure is described, the theory of noise correlation matrix is briefly described as below [102].

According to the theory of noisy linear two-port network, any noisy two-port network can be treated as a noise circuit comprising of a noiseless part and two additional noise sources [103]. Three basic representations for such an equivalent noise circuit are listed in Table 4.1 including their correlation matrices and electrical matrices.

Table 4.1 Basic representations for the equivalent noise circuit and their correlation matrices and electrical matrices.

	admittance	impedance	chain
equivalent noise circuit
correlation matrix	$[C_Y] = \begin{bmatrix} C_{i_1 i_1^*} & C_{i_1 i_2^*} \\ C_{i_2 i_1^*} & C_{i_2 i_2^*} \end{bmatrix}$	$[C_Z] = \begin{bmatrix} C_{u_1 u_1^*} & C_{u_1 u_2^*} \\ C_{u_2 u_1^*} & C_{u_2 u_2^*} \end{bmatrix}$	$[C_A] = \begin{bmatrix} C_{uu^*} & C_{ui^*} \\ C_{iu^*} & C_{ii^*} \end{bmatrix}$
electrical matrix	$[Y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$	$[Z] = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$	$[A] = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}$

The correlation matrix can be transformed from one representation to another using the following equations:

$$[C]' = [T][C][T]^+ \quad (4.25)$$

where $[C]$ is the original correlation matrix, $[C]'$ is the resulting correlation matrix, $[T]$ is the transformation matrix and $[T]^+$ is its conjugate transpose. The values of $[T]$ for various transformations are given in Table 4.2.

For multiple two-ports in series, in parallel or in cascade, as long as these two-ports are uncorrelated, the resulting matrices can be calculated as:

$$[C_Y] = [C_{Y_1}] + [C_{Y_2}] \quad (\text{in parallel}) \quad (4.26)$$

$$[C_Z] = [C_{Z_1}] + [C_{Z_2}] \quad (\text{in series}) \quad (4.27)$$

$$[C_A] = [C_{A_1}] + [A_1][C_{A_2}][A_1]^+ \quad (\text{in cascade}) \quad (4.28)$$

Table 4.2 Transformation matrices between various correlation matrices.

		original representation		
		admittance	impedance	chain
resulting representation	admittance	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$	$\begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}$
	impedance	$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -z_{11} \\ 0 & -z_{21} \end{bmatrix}$
	chain	$\begin{bmatrix} 0 & a_{12} \\ 1 & a_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -a_{11} \\ 0 & -a_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

where the subscripts 1 and 2 denote the two-port network to be connected and the left correlation matrix in each equation denotes the resulting correlation matrix.

For a passive network, the correlation matrix can be calculated from their electrical matrix based on the theory of Johnson noise (thermal noise):

$$[C_Z] = 2k_B T_0 \operatorname{Re}[Z] \text{ (impedance representation)} \quad (4.29)$$

$$[C_Y] = 2k_B T_0 \operatorname{Re}[Y] \text{ (admittance representation)} \quad (4.30)$$

The chain representation of correlation matrix $[C_A]$ and noise parameters (minimum noise figure $NF_{\min}$, equivalent noise resistance R_n and optimal source admittance Y_{opt}) can be derived from each other. The correlation matrix can be calculated from the noise parameters by [104]:

$$[C_A] = 2k_B T_0 \begin{bmatrix} R_n & \frac{NF_{\min} - 1}{2} - R_n Y_{\text{opt}}^* \\ \frac{NF_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} \quad (4.31)$$

The noise parameters can be calculated from the correlation matrix by:

$$\begin{cases} NF_{\min} = 1 + \frac{1}{k_B T_0} \left(\operatorname{Re}[C_{A12}] + \sqrt{C_{A11} C_{A22} - (\operatorname{Im}[C_{A12}])^2} \right) \\ Y_{\text{opt}} = \frac{\sqrt{C_{A11} C_{A22} - (\operatorname{Im}[C_{A12}])^2} + j \operatorname{Im}[C_{A12}]}{C_{A11}} \\ R_n = \frac{C_{A11}}{2k_B T_0} \end{cases} \quad (4.32)$$

The procedure to de-embed the internal noise sources from the measured noise parameters and S parameters can be developed based on the noisy linear two-port theory and by means of the noise correlation matrix method. The flowchart of the procedure is shown in Fig. 4.8 and the detailed steps are described as follows.

Fig. 4.8 (to be continued in next page)

Fig. 4.8 Flow chart of the de-embedding procedure for the intrinsic noise sources.

$$\textbf{Step (1)} \quad [S_{DUT}] \rightarrow [Y_{DUT}]; NF_{\min_DUT}, R_{n_DUT}, \Gamma_{opt_DUT} \rightarrow [C_{A_DUT}]$$

Convert the measured S parameters into Y parameters for the overall Device-Under-Test (DUT); Convert the measured noise parameters $NF_{\min}$, R_n and Γ_{opt} for DUT to the chain representation of noise correlation matrix $[C_{A_DUT}]$.

$$\textbf{Step (2)} \quad [Y_{TRAN1}] = [Y_{DUT}] - [Y_{Cpo}]; [C_{Y_TRAN1}] = [C_{Y_DUT}] - [C_{Y_Cpo}]$$

Subtract the effect of C_{pgo} , C_{pdo} , and C_{pgdo} .

$$\textbf{Step (3)} \quad [Y_{TRAN1}] \rightarrow [A_{TRAN1}]; [C_{Y_TRAN1}] \rightarrow [C_{A_TRAN1}]$$

Convert the Y parameters obtained at last step into A parameters; Convert the admittance representation of noise correlation matrix obtained at last step into the chain representation.

$$\textbf{Step (4)} \quad [A_{TRAN2}] = [A_{Lg}]^{-1} [A_{TRAN1}];$$

$$[C_{A_TRAN2}] = [A_{Lg}]^{-1} ([C_{A_TRAN1}] - [C_{A_Lg}]) ([A_{Lg}]^+)^{-1}$$

Subtract the effect of L_g .

$$\textbf{Step (5)} \quad [A_{TRAN3}] = [A_{TRAN2}] [A_{Ld}]^{-1};$$

$$[C_{A_TRAN3}] = [C_{A_TRAN2}] - [A_{TRAN3}] [C_{A_Ld}] [A_{TRAN3}]^+$$

Subtract the effect of L_d .

$$\textbf{Step (6)} \quad [A_{TRAN3}] \rightarrow [Y_{TRAN3}]; [C_{A_TRAN3}] \rightarrow [C_{Y_TRAN3}]$$

Convert the A parameters obtained at last step into Y parameters; Convert the chain representation of noise correlation matrix obtained at last step into the admittance representation.

$$\textbf{Step (7)} \quad [Y_{TRAN4}] = [Y_{TRAN3}] - [Y_{Cpi}]; [C_{Y_TRAN4}] = [Y_{TRAN3}] - [C_{Y_Cpi}]$$

Subtract the effect of C_{pgi} , C_{pdi} , C_{pgdi} .

$$\text{Step (8)} \quad [Y_{TRAN4}] \rightarrow [A_{TRAN4}]; [C_{Y_TRAN4}] \rightarrow [C_{A_TRAN4}]$$

Convert the Y parameters obtained at last step into A parameters; Convert the admittance representation of noise correlation matrix obtained at last step into the chain representation.

$$\text{Step (9)} \quad [A_{TRAN5}] = [A_{Rg}]^{-1} [A_{TRAN4}];$$

$$[C_{A_TRAN5}] = [A_{Rg}]^{-1} ([C_{A_TRAN4}] - [C_{A_Rg}]) ([A_{Rg}]^+)^{-1}$$

Subtract the effect of R_g .

$$\text{Step (10)} \quad [A_{TRAN6}] = [A_{TRAN5}] [A_{Rd}]^{-1};$$

$$[C_{A_TRAN6}] = [C_{A_TRAN5}] - [A_{TRAN5}] [C_{A_Rd}] [A_{TRAN5}]^+$$

Subtract the effect of R_d .

$$\text{Step (11)} \quad [A_{TRAN6}] \rightarrow [Z_{TRAN6}]; [C_{A_TRAN6}] \rightarrow [C_{Z_TRAN6}]$$

Convert the A parameters obtained at last step into Z parameters; Convert the chain representation of the noise correlation matrix obtained at last step into the impedance representation.

$$\text{Step (12)} \quad [Z_{INT}] = [Z_{TRAN6}] - [Z_{Rs}]; [C_{Z_TRAN6}] = [C_{Z_INT}] - [C_{Z_Rs}]$$

Subtract the effect of R_s .

$$\text{Step (13)} \quad [Z_{INT}] \rightarrow [Y_{INT}]; [C_{Z_INT}] \rightarrow [C_{A_INT}]$$

Convert the Z parameters obtained at last step into Y parameters; Convert the impedance representation of the noise correlation matrix obtained at last step into the chain representation.

$$\text{Step (14)} \quad [C_{A_INT}] \rightarrow NF_{\min_INT}, R_{n_INT}, Y_{opt_INT}$$

Convert the noise correlation matrix $[C_{A_int}]$ of the intrinsic circuit into the noise parameters NF_{min_INT} , R_{n_INT} and Y_{opt_INT} .

Step (15) NF_{min_INT} , R_{n_INT} , Y_{opt_INT} and $[Y_{INT}] \rightarrow \overline{i_{ng}^2}, \overline{i_{nd}^2}, \overline{i_{ng}i_{nd}^*}$

Calculate the internal noise source currents from the noise parameters and Y parameters of the intrinsic circuit using the following equations [105]:

$$\left\{ \begin{array}{l} \overline{i_{nd}^2} = 4k_B T_0 \Delta f \cdot R_{n_INT} |Y_{21i}|^2 \\ \overline{i_{ng}^2} = 4k_B T_0 \Delta f \cdot R_{n_INT} \left\{ |Y_{opt_INT}|^2 - |Y_{11i}|^2 + 2 \operatorname{Re} \left[(Y_{11i} - Y_c) Y_{11i}^* \right] \right\} \\ \overline{i_{ng}i_{nd}^*} = 4k_B T_0 \Delta f \cdot R_{n_INT} Y_{21i}^* (Y_{11i} - Y_c) \\ Y_c = \frac{NF_{min_INT} - 1}{2R_{n_INT}} - Y_{opt_INT} \end{array} \right. \quad (4.33)$$

The above de-embedding procedure for noise sources can be easily carried out by means of the hand-written programs in widely-used scientific computation language such as MATLAB.

4.4 Verification of the Models and the Developed Extraction / De-embedding Procedure

To verify the validity of the above models and the small signal extraction / noise de-embedding procedure, comparison was carried out between the simulated results and the measured data. The simulation for the small signal S-parameters of the device is done through the calculation based on the RF circuit theory, inversely following the procedure described in step 4 of section 4.2. The Y-parameters of the intrinsic circuit in Fig. 4.2 (b) is firstly calculated using Eqn. (4.9), then the extrinsic elements are added from inside to outside: adding R_g , R_d , $R_s \rightarrow$ adding C_{pgi} ,

C_{pdi} , C_{pgdi} → adding L_g , L_d , L_s → adding C_{pgo} , C_{pdo} , C_{pgdo} . Finally the overall S parameter of the whole circuit is obtained.

A GaN HEMT on high-resistivity Si substrate was used for the verification. The S parameters and noise were measured at $V_g = -2.5$ V and $V_d = 6$ V from 2 to 20 GHz. The extracted values of the small signal ECPs are listed in Table 4.3. The measured and simulated S parameters are compared and shown in Fig. 4.9. It can be seen that the simulated curves agree well with the measurement. The errors of the simulation calculated according to Eqn. (3.21) are as low as 0.7%, 1.5%, 2.1% and 0.6% respectively for S_{11} , S_{12} , S_{21} and S_{22} . The mean error of the simulation for S parameters defined by Eqn. (4.22) is 1.2% and the standard deviation among the four elements is 0.7%. The small errors indicate the validity of the small-signal model and developed ECP extraction procedure for GaN HEMTs.

Table 4.3 Values of the extracted equivalent circuit parameters (in Fig. 4.2).

Parameter	$C_{pgo}(\text{fF})$	$C_{pdo}(\text{fF})$	$C_{pgdo}(\text{fF})$	$C_{pgi}(\text{fF})$	$C_{pdi}(\text{fF})$	$C_{pgdi}(\text{fF})$
Extracted Values	15.8	15.6	0	5.15	8.54	0.8
Parameter	$L_g(\text{pH})$	$L_d(\text{pH})$	$L_s(\text{pH})$	$R_g(\Omega)$	$R_d(\Omega)$	$R_s(\Omega)$
Extracted Values	62.9	57.2	0	7.2	26.2	8.2
Parameter	$g_{m0}(\text{mS})$	$C_{gs}(\text{fF})$	$C_{gd}(\text{fF})$	$C_{ds}(\text{fF})$	$R_{gd}(\Omega)$	$R_{ds}(\Omega)$
Extracted Values	36.2	108.1	17.4	13.2	47.9	480.0
Parameter	$R_{gs}(\Omega)$	$\tau(\text{fs})$	$R_{fs}(\Omega)$	$R_{fd}(\Omega)$		
Extracted Values	4.86	460	∞	∞

Fig. 4.9 (a)-(h): Comparison of the simulated S parameters and measurement data for a GaN HEMT on high resistivity Si using the model in Fig. 4.2 and developed procedure in this chapter.

To confirm the validity of the noise equivalent circuit (Fig. 4.7) and the developed noise de-embedding procedure, we calculated the device noise parameters based on the noisy linear 2-port network theory [103] and the extracted noise source currents and small signal ECPs. The de-embedded noise source currents and their correlation are shown in Fig. 4.10. The de-embedded noise current curves have been smoothed, as the originally measured data are remarkably scattered due to the limit of measurement system. The simulated noise parameters for the whole device are compared with the measured data in Fig. 4.11 and good agreement is achieved, and thus, the noise model and the de-embedding procedure is validated.

Fig. 4.10 De-embedded noise source currents and their correlation for GaN HEMTs on Si using the developed procedure.

Fig. 4.11 (a)-(d): Comparison of the simulated noise parameters and the measurement data for a GaN HEMT using the model and developed procedure.

Chapter 5

Comprehensive Study on the Effect of Surface Passivation on Microwave Small Signal and Noise Characteristics

5.1 Introduction

Generally a large amount of surface states exist on the surface of GaN HEMTs. These surface states are possibly caused by the dangling bonds and/or the defects/dislocations and foreign contaminations. They are working as carrier traps and seriously deteriorate the device performance, typically causing trapping effects of current collapse and DC-to-RF dispersion. Surface passivation using some dielectrics such as Si_3N_4 , SiO_2 has been proven to be able to effectively reduce the density of surface states, and hence suppress the surface trap effects and improve the microwave power output [106, 107].

The effects of surface passivation on the DC, microwave small signal and power performance have been widely reported by other groups [106, 108, 109, 110]. However, for the small signal equivalent circuit elements, which are of great importance in device modeling and in providing a better understanding of their physical origins, there is still no comprehensive study of the surface passivation effects. Furthermore, the effect of passivation on the microwave noise characteristics has not been well investigated, in particular for GaN HEMTs on high-resistivity silicon substrates.

In this chapter, we comprehensively study the effects of Plasma Enhanced Chemical Vapor Deposited (PECVD) SiN passivation on the DC, small signal and especially microwave noise characteristics of AlGaIn/GaN HEMTs on high

resistivity Si. The passivation effects on the various small signal ECPs are discussed. The noise performance of the device is found to be improved after passivation and it is believed to be due to the increase of 2DEG density and mobility by the reduction of surface states. The physical mechanism of the channel noise increase after passivation is investigated.

The organization of this chapter is shown as follows. In the first section, a brief introduction is given. Then the experimental details are described in Section 2. The DC performance and small signal characteristics before and after passivation are measured and presented in Section 3 and Section 4. The bias dependent small signal ECPs are extracted and their behaviors due to surface passivation are comprehensively studied in Section 5. The passivation effects on the noise performance are given in Section 6 and the physical mechanisms of the channel noise after passivation are discussed in Section 7. In the last section, some key conclusions are drawn.

5.2 Experiments

The AlGaIn/GaN HEMT in this work was grown on high-resistivity ($>10,000 \Omega\cdot\text{cm}$) Si substrate by metalorganic chemical vapor deposition (MOCVD). Fig. 5.1 shows the schematic of its structure. The epi-layer comprises of a 2-nm un-doped GaN cap layer, a 17.5-nm un-doped $\text{Al}_{0.26}\text{Ga}_{0.74}$ barrier layer, a 1.5- μm undoped GaN buffer and a transition/seedling layer. Hall measurement showed a 2-D-electron-gas (2DEG) sheet carrier density of $0.7 \times 10^{13} \text{ cm}^{-2}$ and electron mobility of $1300 \text{ cm}^2/\text{V}\cdot\text{s}$ at room temperature.

The fabrication details are same as those described in Chapter 2. Before the last step surface passivation, the DC, small signal and microwave noise

performance were measured. After surface passivation, they were measured again. Then the characteristics before and after passivation were compared and studied.

In this chapter, the devices with gate length $L_g = 0.3 \mu\text{m}$ and $W_g = 2 \times 100 \mu\text{m}$ were used for the characterization. DC characterization was performed using Agilent 4156B semiconductor parameter analyzer, and the microwave small signal characteristics were measured using HP8510C Vector Network Analyzer. The microwave noise performance was measured using ATN NP5 noise test set, with HP8970B noise figure meter and HP8510C Vector Network Analyzer.

Fig. 5.1 Schematic of the device structure utilized in this chapter.

5.3 DC Performance Improved by Passivation

The DC output (I_d - V_d) and transfer (I_d - V_g) characteristics of the AlGaIn/GaN HEMT before and after surface passivation are plotted in Fig. 5.2 (a) and (b). Table 5.1 summarizes the DC characteristics affected by the SiN surface passivation. After passivation, the maximum drain current I_{dmax} significantly increased by ~70% from 300 mA/mm to 490 mA/mm (at $V_g = +1 \text{ V}$). The channel

resistance in linear region (R_{on}) decreased by 29% from 9.3 $\Omega \cdot \text{mm}$ to 6.6 $\Omega \cdot \text{mm}$ and the maximum extrinsic transconductance $g_{m\text{max}}$ increased by 30% from 120 mS/mm to 160 mS/mm). A slightly negative shift in the threshold voltage ($\Delta V_{th} \sim -0.15$ V) was observed after passivation. The gate voltage swing (GVS) of the transconductance g_m , defined as the gate voltage range in that the values of g_m are $\geq 90\%$ of $g_{m\text{max}}$, increased from 1.05 V to 1.60 V. The higher GVS for g_m enables the device to have a higher output power and a better linearity [111]. The improved DC characteristics by SiN surface passivation is consistent with other published reports [106, 107, 110], which is believed to be due to the increased sheet carrier density (n_s) and electron mobility (μ) of the 2DEG by the SiN thin film deposited at the source-to-gate and drain-to-gate region. We have confirmed the increase of n_s after SiN passivation through Hall measurement [112].

Table 5.1 Summary of the DC characteristics affected by the SiN surface passivation.

Parameters	Before Passivation	After Passivation
$n_s(\text{cm}^{-2})$	0.83×10^{12}	1.37×10^{13}
$I_{d\text{max}}(\text{mA/mm})$	298	489
$R_{on}(\Omega \cdot \text{mm})$	9.3	6.6
$g_{m\text{max}}(\text{mS/mm})$	120	156
$V_{th}(\text{V})$	-2.39	-2.55

Fig. 5.2 DC characteristics of (a) output $I_d - V_d$ and (b) transfer $I_d - V_g$ before and after passivation for AlGaIn/GaN HEMT on high-resistivity Si substrate.

5.4 Passivation Effect on Microwave Small Signal Characteristics

Fig. 5.3 shows the microwave small-signal gain characteristics measured from the AlGaIn/GaN HEMT on Si before and after passivation at $V_d=12$ V and $V_g=-1.5$ V. The values of the short-circuit current gain $|H_{21}|$, maximum available gain/maximum stable gain (MAG/MSG) and the unilateral power gain (G_u) as a function of frequency are shown in the figure. The device's current-gain cut-off frequency f_T determined by the extrapolation of $|H_{21}|$ using a -20dB/dec slope was found to have increased from 18 GHz to 23 GHz after passivation. The device's maximum oscillation frequency f_{max} determined by extrapolation of MAG/MSG at a slope of -20 dB/dec and by G_u were found to increase from 35 GHz to 65 GHz and 26 GHz to 44 GHz separately after passivation. Table 5.2 summarizes the small signal characteristics influenced by the SiN surface passivation. It is clearly

Fig. 5.3 Microwave small-signal gain characteristics of the AlGaIn/GaN HEMT on high-resistivity Si before and after passivation.

shown that the SiN surface passivation has improved the microwave performance for AlGaIn/GaN HEMTs on Si.

Table 5.2 Summary of the small signal characteristics before and after the SiN surface passivation.

Parameters	Before Passivation	After Passivation
f_T (GHz)	18	23
f_{max} (MAG/MSG) (GHz)	35	65
$f_{max}(G_u)$ (GHz)	26	44

Fig. 5.4 shows the measured bias-dependent f_T and f_{max} values of the AlGaIn/GaN HEMT before and after passivation as a function of (a) gate bias V_g at $V_d=12$ V and (b) drain bias V_d at $V_g = -1.5$ V. From Fig. 5.4 (a), it can be seen that both the f_T and f_{max} have increased over the whole measured V_g range after passivation. After passivation, the linearity of f_T and f_{max} was obviously improved. At $V_g = -2$ V, the values of f_T and f_{max} decreased by only 4.6% and 2.3% from the peak respectively after passivation, while they decreased by 44.4% and 17.8% from the peak respectively before passivation. At $V_g = +1$ V, the values of f_T and f_{max} decreased by 31.8% and 35% from the peak, while they decreased by 68.0% and 71.2% before passivation respectively.

The f_T and f_{max} also increased over the whole drain bias range after passivation, as shown in Fig. 5.4 (b). The curves of f_T and f_{max} versus V_d became flatter after passivation. The f_T and f_{max} values are decreased obviously at high drain biases, but this droop was suppressed after surface passivation.

Fig. 5.4 Measured f_T and f_{max} values of the AlGaIn/GaN HEMT on high-resistivity Si before and after passivation versus (a) V_g at $V_d = 12$ V (b) V_d at $V_g = -1.5$ V.

5.5 Passivation Effect on the Bias-dependent Small Signal ECPs

In order to comprehensively understand the physical mechanisms of the passivation effect on the bias-dependent microwave small signal characteristics, the values of ECPs at all measured bias points both before and after passivation were extracted using the developed procedure that have been described in Chapter 4. The behaviors of these bias-dependent ECPs after SiN surface passivation are described and discussed in detail in this section.

Table 5.3 lists the extracted values for access resistances R_s and R_d before and after passivation. The source and drain access resistances can be expressed as:

$$\begin{cases} R_s = R_c' + R_{sh} L_{gs} / W_g \\ R_d = R_c' + R_{sh} L_{gd} / W_g \end{cases} \quad (5.1)$$

where R_c' is the ohmic contact resistance (with the unit of Ω), R_{sh} is the wafer sheet resistance, L_{gs} and L_{gd} are the distances from gate to source and from gate to drain respectively. R_c' depends on the fabrication process of the ohmic contact which is hardly affected by the surface condition changes. From Eqn. (5.1), we can get:

$$R_d - R_s = R_{sh} (L_{gd} - L_{gs}) / W_g \quad (5.2)$$

Then the R_{sh} change due to passivation can be calculated from the change of the difference between R_d and R_s . R_{sh} was found to decrease by 29% after passivation. Since R_{sh} can be expressed as:

$$R_{sh} = \frac{1}{qn_s \mu} \quad (5.3)$$

The decrease of R_{sh} indicates that the SiN surface passivation has improved the 2DEG transport property namely $n_s \mu$.

Table 5.3 Values of the access resistances R_s and R_d before and after passivation.

	Before passivation	After passivation
$R_s (\Omega \cdot \text{mm})$	1.4	1.0
$R_d (\Omega \cdot \text{mm})$	7.6	5.4

The small-signal intrinsic transconductance $g_{m,\text{int}}$ versus gate bias at a fixed drain voltage of 12 V is shown in Fig. 5.5 (a). After passivation, the value of $g_{m,\text{int}}$ was improved over the whole measured gate bias range from -2 to +1 V. The $g_{m,\text{int}}$ improvement is mainly due to the increase of the effective velocity v_{eff} by the reduction of surface traps after passivation. The linearity of the intrinsic g_m was also slightly improved.

Fig. 5.5 (b) shows the extracted $g_{m,\text{int}}$ versus drain bias at a fixed gate voltage of -1.5 V. The values of the $g_{m,\text{int}}$ have also increased over the whole V_d range after passivation. Before passivation, the $g_{m,\text{int}}$ decreased greatly at high drain voltage (around $V_d=20$ V), possibly as a result of the hot electrons captured by the surface traps and depleting the channel. After SiN surface passivation, that hot electron effect is suppressed.

Fig. 5.5 Extracted intrinsic transconductance $g_{m,\text{int}}$ versus (a) gate bias and (b) drain bias before and after SiN surface passivation for the AlGaIn/GaN HEMT on Si.

The extracted gate-source capacitance C_{gs} versus the gate bias before and after passivation is shown in Fig. 5.6 (a). The C_{gs} increases with the gate voltage from pinch-off and reaches a peak close to the location where the peak $g_{m,int}$ occurs. Then C_{gs} slightly drops at higher gate voltage. After passivation, this trend has not changed.

The C_{gs} arises from two parts: C_{gs}^{2DEG} and C_f :

$$C_{gs} = C_{gs}^{2DEG} + C_f \quad (5.4)$$

where C_{gs}^{2DEG} is the capacitance component from the channel 2DEG under the gate at the source side and C_f is the fringing capacitance. In contrast to the typical GaAs HEMT [113], the barrier for GaN HEMT in this work is undoped. Thus, there are no components from the neutralized donor capacitance. C_f can be expressed as: [96]

$$C_f = \frac{\epsilon W_g}{\pi} \quad (5.5)$$

After passivation the C_f is increased due to the higher dielectric constant of the induced SiN layer ($\epsilon \sim 7.0$, measured by a separate metal-insulator-metal (MIM) capacitor using the SiN as insulator) as compared to that of air ($\epsilon = 1$). This is reflected from the observation that at those gate biases close to the pinch-off voltage, the C_{gs} values have obviously increased after passivation. This is because that, at such gate bias conditions, the electrons in the channel are greatly depleted and the channel capacitance was very small, so the C_f change is more pronounced in the total C_{gs} . However, when V_g is increased beyond a certain point, the difference of the C_{gs} values before and after passivation becomes insignificant and negligible. This can be explained by the electrical field distribution change therefore resulting in the vertical extension of the depletion region after passivation

[114], which decreases C_{gs} and cancels the effect of increased dielectric constant by the deposited SiN layer.

Fig. 5.6 Extracted gate-source capacitance C_{gs} versus (a) gate bias and (b) drain bias before and after SiN surface passivation for the AlGaIn/GaN HEMT on Si.

As for the drain bias dependence, the C_{gs} is less affected by drain bias than by gate bias. At high drain bias e.g. $V_d=20$ V, the C_{gs} is slightly increased before passivation but it decreased after passivation. The low C_{gs} value at high drain voltage is believed to be due to the enhanced peak electrical field at the drain side of the gate as a result of the suppressed surface depletion after passivation.

The extracted gate-drain capacitance C_{gd} versus the gate bias and drain bias in the AlGaIn/GaN HEMT before and after passivation is shown in Fig. 5.7. The values of C_{gd} were observed to increase with the gate bias and decrease with the drain bias both before and after passivation. After passivation, the rate of increase with gate bias was reduced and the rate of decrease with the drain bias was enhanced.

Similar to C_{gs} , C_{gd} is also composed of two parts, the channel 2DEG capacitance C_{gd}^{2DEG} and the fringing capacitance C_f :

Fig. 5.7 Extracted gate-drain capacitance C_{gd} versus (a) gate bias and (b) drain bias before and after SiN surface passivation for the AlGaIn/GaN HEMT on Si.

$$C_{gd} = C_{gd}^{2DEG} + C_f \quad (5.6)$$

At low gate bias near pinch-off, C_{gd} is observed to increase after passivation due to the increase in the fringing capacitance C_f which is similar to the case of C_{gs} . But different from C_{gs} , the C_{gd}^{2DEG} is determined not only by the variation of the drain part of the space charge region but also by the accumulation of carriers at the drain side of the gate from inter-valley transitions [115]. The latter leads to a positive increment of the charge with negative increment of V_{ds} . In general, the value of C_{gd} is much smaller than C_{gs} , and C_f plays a key role in the total C_{gd} . Thus, the increase of C_{gd} after passivation is more pronounced than C_{gs} at most biases. In addition, the bias dependence of C_{gd} has a much different behavior from that of C_{gs} . When V_{ds} increases, or V_g increases (the channel current increases), the inter-valley transition becomes more pronounced hence C_{gd} is reduced. After passivation, the reduction of the surface charge changed the electric field profile and made its peak larger and sharper at high drain bias [114]. So the inter-valley transition became

more effective and this made C_{gd} less dependent on the bias change. In other words, the C_{gd} increases slower with V_g and decreases faster with V_d after passivation.

From another point of view, the C_{gd} at the saturation region can be roughly expressed as [116]

$$C_{gd} \approx \frac{\epsilon W_g (d + \Delta d)}{L_{gd,eff}} \quad (5.7)$$

where d is the distance from the gate to the channel heterojunction. Δd is the effective distance from the channel heterojunction to the 2DEG electron cloud, that is, the effective depletion depth at the drain side of the gate. $L_{gd,eff}$ is the effective width of the space charge region (or depletion region) at the drain side of the gate. At high V_{ds} the depletion region at the drain side of the gate extends towards the drain side, so C_{gd} decreases with V_{ds} . The V_{ds} dependence of C_{gd} in the AlGaIn/GaN HEMT is similar to those observed in other types of HEMTs [113]. After passivation, the negative charge density due to the surface electron traps located at the gate-drain region was reduced, and thereby the depletion effect from the surface charge was weakened. This made the shape of the depletion region, especially at the drain side of the gate, more determined by the drain bias. Thus C_{gd} decreases faster with V_{ds} . For the similar reason, C_{gd} increases with V_{gs} due to the shortened $L_{gd,eff}$ at high V_{gs} , and the increase rate becomes lower after passivation. Thus the increase of C_{gd} with V_{gs} became slower after passivation.

The values of C_{ds} were found to be increased over both gate bias and drain bias ranges after passivation, as Fig. 5.8 shows. The C_{ds} can be expressed as [117]:

$$C_{ds} = \frac{2\pi\epsilon_{GaIn} h(V_{gs}, V_{ds}) W}{L_{dep,eff}} \quad (5.8)$$

Fig. 5.8 Extracted drain-source capacitance C_{ds} versus (a) gate bias and (b) drain bias before and after SiN surface passivation for the AlGaIn/GaN HEMT on Si.

where $h(V_{gs}, V_{ds})$ is the effective depletion height in the channel and it is a function of gate and drain bias. $L_{dep,eff}$ is the effective depletion length in the channel.

C_{ds} increases after passivation as shown in Fig. 5.8. This is believed to arise from two factors. First, due to the electrical field profile change under the gate after reduction of the charged surface states, the electrical peak is enhanced at the drain side of the gate. The increased high field pushes more carriers into the buffer and increases the value of effective depletion height h . Second, the suppression of the surface depletion reduces the lateral space charge length $L_{dep,eff}$, which also contributes to the C_{ds} increase.

Before passivation, as a result of the relatively lower gate field at the drain side of the gate, the electrons are more confined in the channel and h is sensitive to the gate bias compared with after passivation. When the gate voltage increases, the electrons are closer to the heterojunction and the effective depletion height h becomes smaller, so the C_{ds} is decreased obviously when V_g increases, as shown in Fig. 5.8(a). When the drain voltage increases, both the effective depletion height h

and length $L_{\text{dep,eff}}$ are enhanced and the resulted C_{ds} almost does not vary at relatively low drain voltage range, as shown in Fig. 8(b). At high drain voltage range, the increase of the effective depletion length $L_{\text{dep,eff}}$ is more than that of the effective depletion height, so C_{ds} decreases. After passivation the trend of C_{ds} versus V_{ds} has not been changed, but only the values of C_{gs} are increased.

The values of R_{ds} versus gate bias and drain bias before and passivation are plotted in Fig. 5.9. It was observed that, at low drain bias or the gate bias near pinch-off, the R_{ds} values were reduced by the passivation. At high drain bias, the R_{ds} values were increased. The R_{ds} decrease is similar to the due to the R_{sh} . After SiN passivation the density of surface states was decreased and thus the depletion and remote Coulomb scattering of the channel electrons were also suppressed. This resulted in the improved n_s and mobility/saturation velocity hence decreased R_{ds} and R_{sh} . At high drain voltage, because of the enhanced depletion under the gate after passivation, the values of R_{ds} are increased.

Fig. 5.9 Extracted output resistance R_{ds} versus (a) gate bias and (b) drain bias before and after SiN surface passivation for the AlGaIn/GaN HEMT on Si.

Fig. 5.10 Extracted R_{gs} and R_{gd} versus (a) gate bias and (b) drain bias before and after SiN surface passivation for the AlGaIn/GaN HEMT on Si.

The values of R_{gs} and R_{gd} versus gate and drain bias before and passivation are shown in Fig. 5.10. It is well known that their values are difficult to be accurately extracted and their physical source is still unclear [118]. However, some trends can still be clearly seen from the figure in terms of the change in their behaviors due to surface passivation. After passivation, the values of R_{gs} and R_{gd} both decreased over the measured gate-bias range and drain-bias range. This is

most likely associated with the increased mobility and saturation velocity by the reduced surface charges after passivation.

Fig. 5.11 plots the bias dependent τ which is also affected by surface passivation. Similar to R_{gs} and R_{gd} , the accurate extraction of τ is also difficult. τ decreases with the increasing gate bias and increases with the increasing drain bias. After passivation, the values of τ increased at high V_{ds} (>8 V). This is possibly due to the enhanced depletion at the drain side of the gate. However, more work need to be done in order to clearly understand the details of the behavior for R_{gs} , R_{gd} and τ versus biases affected by the surface passivation.

Fig. 5.11 Extracted gate-source capacitance τ versus (a) gate bias and (b) drain bias before and after SiN surface passivation for the AlGaIn/GaN HEMT on Si.

5.6 Passivation Effect on Microwave Noise Performance

Fig. 5.12 and Fig. 5.13 show the microwave noise characteristics of the AlGaIn/GaN HEMTs before and after passivation measured at a frequency range from 2 to 18 GHz and at fixed biases of $V_g = -1.5$ V and $V_d = 12$ V. Both the values of NF_{min} and R_n were reduced and G_a increased over the whole frequency range

after passivation. At 10 GHz, the value of the $NF_{\min}$ and G_a was reduced by 21.1% (0.55 dB, from 2.6 dB to 2.05 dB) and increased by 27.2% (2.5 dB, from 9.2 dB to 11.7 dB) respectively. The R_n decreased by 11.5% (3.8Ω from 33.1Ω to 29.3Ω), which means that the output noise figure becomes less dependent on the deviation of source impedance from the optimal state. The optimal source impedances Z_{opt} also had changed slightly as shown in Fig. 5.13 (b). Both the values of $NF_{\min}$ and G_a also show less dependent with the frequency after passivation. Our observed microwave noise improvement after passivation is opposite to the other report of AlGaIn/GaN HEMT on sapphire substrate [108], in which an increase of $NF_{\min}$ was observed due to the higher increase of C_{gs} over only a slight increase of g_m .

Fig. 5.12 Measured $NF_{\min}$ and G_a as a function of frequency (from 2GHz to 18GHz) at $V_d=12$ V and $V_g=-1.5$ V for AlGaIn/GaN HEMT on high-resistivity Si before and after passivation.

Fig. 5.13 Measured (a) R_n and (b) Z_{opt} as a function of frequency (from 2 GHz to 18 GHz) at $V_d=12$ V and $V_g=-1.5$ V for AlGaIn/GaN HEMT on high-resistivity Si before and after passivation.

In the actual LNA application, the device is generally biased at a fixed output current instead of voltage. So it is more meaningful to compare the noise performance before and after passivation at a fixed drain current. Fig. 5.14 and Fig. 5.15 show the microwave noise characteristics of the AlGaIn/GaN HEMTs before and after passivation measured at fixed biases of $I_d=120$ mA/mm and $V_d=12$ V. Improvement of the noise parameters also have been measured. Both the values of $NF_{\min}$ and R_n were reduced and G_a increased over the whole frequency range after passivation. At 10 GHz, the values of the $NF_{\min}$ and G_a were reduced by 38.3% (1.27 dB, from 3.32 dB to 2.05 dB) and increased by 22.8% (1.8 dB, from 7.9 dB to 11.7 dB), respectively. The R_n decreased by 25.3% (9.9 Ω from 39.2 Ω to 29.3 Ω). The optimal source impedances Z_{opt} has changed slightly as shown in Fig. 5.15 (b). It has been observed that the noise parameters $NF_{\min}$, G_a and R_n have

Fig. 5.14 Measured $NF_{\min}$ and G_a as a function of frequency (from 2 GHz to 18 GHz) at $V_d=12$ V and $I_d=120$ mA/mm for the AlGaIn/GaN HEMT on high-resistivity Si before and after passivation.

Fig. 5.15 Measured (a) R_n and (b) Z_{opt} as a function of frequency (from 2 GHz to 18 GHz) at $V_d = 12$ V and $I_d = 120$ mA/mm for of AlGaIn/GaN HEMT on high-resistivity Si before and after passivation.

been improved more when they are compared at the same drain current than when they are compared at the same gate bias before and after passivation. This is because that the passivation effect increases the drain current at the same gate bias. Both values of $NF_{\min}$ and G_a show less dependence with the drain current.

Fig. 5.16 shows the bias dependent noise characteristics including $NF_{\min}$, G_a and R_n at 10 GHz for the AlGaN/GaN HEMT on high-resistivity Si substrate before and after passivation. The improvement of all the three parameters has been observed over the whole bias range ($NF_{\min}$ and R_n were decreased and G_a was increased) especially at high drain currents (or, gate voltages) and low drain voltages. The linearity of the noise parameters is obviously improved after passivation, that is, there is a wider drain current range for low $NF_{\min}$, low R_n and high G_a . For example, if we define a figure-of-merit called drain current swing (DCS) as the drain current range in which the parameter has its values no more than 150% (~ 1.8 dB) of its minimum point, the parameter $NF_{\min}$ has a DCS value of 46 mA after passivation, which is 64% higher than the 28 mA before passivation.

The improvement of the noise parameters is believed to be mainly due to the increase of g_m after passivation. The $NF_{\min}$, R_n and G_a are greatly dependent on g_m as the following expressions show [119, 120]:

$$\left\{ \begin{array}{l} NF_{\min} = 1 + \frac{2}{T_0} \frac{\omega(C_{gs} + C_{gd})}{g_m} \sqrt{\frac{R_{gs}}{R_{ds}}} T_g T_d \\ R_n = \frac{1}{T_0} \left(R_{gs} T_g + \frac{T_d}{R_{ds}} \frac{1}{g_m^2} \right) \\ G_a = \frac{2T_d}{T_0 (NF_{\min} - 1)} \end{array} \right. \quad (5.9)$$

Fig. 5.16 Measured values of $NF_{\min}$, G_a and R_n at 10 GHz as a function of (a) drain current I_d (b) drain voltage V_d for the AlGaN/GaN HEMT on high-resistivity Si before and after passivation.

where T_g and T_d are variables associated with the internal noise sources, T_0 is the noise standard temperature and $T_0=290$ K, and other symbols hold their normal meanings. The improvement of g_m can be seen in Fig. 5.5. Since C_{gs} is almost not changed by the passivation at high current and C_{ds} is much smaller than C_{gs} at most biases (as Fig. 5.6 shows), the term $C_{gs}+C_{gd}$ has not been changed significantly after passivation and the significant increase of g_m leads to the decrease of NF_{min} and R_n and the increase of G_a . Except the circuit elements, the internal noise sources have also been changed by the surface passivation and their effects on the measured noise parameters will be discussed in next section.

5.7 Physical Mechanism of the Increased Channel Noise after Passivation

It is interesting to understand the physical mechanisms of the passivation effects on the internal noise sources. For this device the gate leakage current is relatively low and its magnitude is smaller than $\sim\mu A$. Since the gate shot noise $\overline{i_{ngsh}^2}$ generated by the gate leakage current is determined by:

$$\overline{i_{ngsh}^2} = 2qI_g \Delta f \quad (5.10)$$

where q is the electron charge quantity, the mean square gate shot-noise current is calculated to be no larger than $\sim 10^{-25} A^2$, which is much smaller than the typical value of the mean square induced gate noise current with a magnitude of $\sim 10^{-23} A^2$ at frequencies > 5 GHz. Therefore, the gate shot noise is ignored in the following discussion, and the overall gate noise is dominated by the induced gate noise by the capacitive effect of the Schottky gate. It is interested to understand how the channel noise changes after SiN passivation.

Fig. 5.17 shows the extracted mean square of channel noise voltage over the frequency range from 2 to 18 GHz for the AlGaIn/GaN HEMT on Si substrate before and after passivation. The bias was kept at $V_d=12$ V and $I_d=120$ mA/mm during the measurements both before and after passivation. It can be seen that the mean square of channel noise voltage is enlarged about 3 times uniformly over all the measured frequencies after passivation. The purpose of selecting the mean square of channel noise voltage $\overline{v_{nd}^2}$ instead of the channel noise current $\overline{i_{nd}^2}$ nor the channel noise coefficient P for the comparison is to exclude the influence of the g_m and small signal output conductance g_{ds} , since both the values of g_m and g_{ds} are influenced by the passivation [121]. The $\overline{i_{nd}^2}$ and P can be expressed as: [122]

$$\overline{i_{nd}^2} = \overline{v_{nd}^2} \times g_{ds}^2 \quad (5.11)$$

$$\text{And } P = \frac{\overline{v_{nd}^2} \times g_{ds}^2}{4kT_0 \Delta f g_m} \quad (5.12)$$

where T_0 (=290 K) is the reference temperature and Δf is the frequency band.

Fig. 5.17 The mean square channel noise voltage for the AlGaIn/GaN HEMT on Si substrate before and after SiN surface passivation.

The channel noise source can be divided into two components as described in a widely-accepted physical based model on high-frequency noise originally proposed by Pucel et al. for MESFETs [122] and later modified by Anwar et al. to suit HEMTs [123]. The mean square noise voltage from the linear region $\overline{v_{nd1}^2}$ and that from the velocity-saturation region $\overline{v_{nd2}^2}$ can be expressed as [123]:

$$\left\{ \begin{array}{l} \overline{v_{nd1}^2} = \frac{4kT_0\Delta f}{I_d} \cdot \cosh^2\left(\frac{\pi L_2}{2d_{eff}}\right) [f_1(V_g, V_d) + \delta f_2(V_g, V_d)] \end{array} \right. \quad (5.13)$$

$$\left\{ \begin{array}{l} \overline{v_{nd2}^2} = \frac{64qI_d d_{eff}^3 \Delta f}{\pi^5 \epsilon^2 v_{sat}^3 W_g^2 \Delta d^2} \cdot \sinh^2\left(\frac{\pi \Delta d}{2d_{eff}}\right) [D_h \cdot f_3(\lambda) + \mu_0 f_4(\lambda)] \end{array} \right. \quad (5.14)$$

where f_1 and f_2 are both weak functions of the bias V_g and V_d ; $f_3, f_4 \sim \lambda^2$ and $\lambda = \exp\left(\frac{\pi L_2}{2d_{eff}}\right)$. $d_{eff} = d_{bar} + \Delta d$, and d_{bar} is the thickness of the GaN top layer and AlGaIn barrier layer, Δd is the effective channel width. Here Δd is assumed to be a constant value over the whole channel. The meanings of $L_1, L_2, d_{eff}, d_{bar}$ and Δd are shown in Fig. 5.18. Other symbols have the same meanings as those in Ref. [123].

Fig. 5.18 Schematic of the channel noise model for AlGaIn/GaN HEMTs.

It can be seen from the above two equations that both the channel noise components $\overline{v_{nd1}^2}$ and $\overline{v_{nd2}^2}$ are dependent on the drain current, but their dependences are opposite to each other. In Fig. 5.17 we compare the mean square channel noise voltage before and after passivation not at the same gate bias but at the same drain current, so that the drain current influence can be excluded and the analysis is simplified. Furthermore, other researchers have observed that the μ_0 slightly decreased after passivation because n_s increased in AlGaIn/GaN HEMTs [112,124]. As for the v_{sat} , although few people have discussed its behavior after passivation, we believe that it is supposed to increase or at least not greatly decrease since the surface state scattering is reduced. Thus the observed channel noise increase is not due to the μ_0 or v_{sat} change.

On the other hand, the quality of the SiN dielectric layer and the interface between SiN/semiconductor was verified by the pulsed I-V measurement and there are not many charge defects induced by the passivation process itself [112]. We have reported that the PECVD SiN passivation reduces the net negative charge induced by the trapped electrons at the surface, thereby increases the n_s , g_m , maximum drain current I_{dmax} , and reduces the overall noise figure NF_{min} [107, 121]. It is well known that the negative surface charge at the gate-drain region can work as a “virtual gate” which changes the surface potential and the lateral electrical field profile in the channel then suppresses the peak of the lateral electrical field at the gate edge close to the drain at large drain voltage [125]. Such lateral electrical field profile change caused by the surface trapped charge has also been observed in AlGaAs/GaAs HEMTs as the phenomenon of gate-drain breakdown voltage “walk out” [125]. In fact, at the bias point for the noise measurement in AlGaIn/GaN HEMT, the gate leakage current was measured to increase from 4.5×10^{-7} to 1.4×10^{-7}

⁵ A/mm after passivation. We have reported the gate leakage current increase and gate-drain 2-terminal breakdown voltage decrease after SiN surface passivation for AlGaIn/GaN HEMTs on Si in [112]. Other groups have also observed the 3-terminal off-state breakdown voltage decreased after SiN surface passivation for AlGaIn/GaN HEMTs on sapphire substrate [43]. The fact that the gate leakage increases and breakdown voltage decreases after passivation shows that the peak value of the lateral electrical field underneath the gate is enlarged.

The increased peak of the lateral electrical field after passivation can reduce the value of D_h , but enlarges the length of the saturation region L_2 at the same time. Fig. 5.19 shows the simulated electron density in the triangle-like quantum well close to the interface between AlGaIn barrier and GaN channel before and after passivation by self-consistently solving the 2-dimensional Poisson equation and current continuity equation using ATLAS software. During simulation all the materials' parameters used the software's default values. The simulation clearly shows the trend of L_2 increase after passivation. d_{eff} is the distance from the gate to the 2DEG at source side, so it is almost not affected by the electrical field profile change due to the surface passivation, which is also verified by the simulation (Fig. 5.19). From the expressions of $\overline{v_{nd1}^2}$ and $\overline{v_{nd2}^2}$ (Eqn. (5.13) and (5.14)), it can be seen that the mean square of the channel noise voltage approximately increases exponentially with the value of L_2/d_{eff} . Thus the channel noise is much sensitive to the length of the saturation region L_2 and finally the channel noise is increased after the surface passivation through the increasing of L_2 .

Fig. 5.19 Numerical simulation of 2DEG density in the channel before and after surface passivation.

The increase of L_2 after passivation can be verified by the comparison of another internal noise coefficient – i. e., the correlation coefficient between drain and gate noise (C) – before and after passivation. This is based on the fact that the correlation between the channel diffusion noise (in Region II) and its induced gate noise is unity; while the correlation between the channel thermal noise (in Region I) and its caused gate noise is smaller than unity, thus the value of the C is dependent on the ratio of L_2 to L_g [122]. If the value of L_2 increases, the measured value of C should be closer to unity. Fig. 5.20 shows the measured values of C before and after passivation. It is evident that after passivation, the value of C increased and became closer to unity, which verified the above analysis that the value of L_2 has increased.

Fig. 5.20 The correlation coefficient between the channel noise and the gate noise for the AlGaIn/GaN HEMT on high-resistivity Si substrate before and after SiN surface passivation.

5.8 Conclusion

In conclusion, the effects of PECVD SiN surface passivation on DC, small signal and microwave noise characteristics have been comprehensively studied for 0.3 μm gate-length AlGaIn/GaN HEMTs on Si substrate in this chapter. The main findings are summarized as below:

DC characteristics including I_{Dmax} , g_{mmax} were found to be improved after passivation.

Bias dependent microwave small signal characteristics were measured and the SiN surface passivation has been found to improve the microwave performance including f_{T} , f_{max} etc. over all the biases.

The bias dependent small signal ECPs were extracted before and after passivation and the influence of the SiN surface passivation were comprehensively studied. After passivation, the surface state density in the device was reduced and hence the depletion and remote Coulomb scattering of the 2DEG channel electrons are suppressed, which leads to an increase of the channel electron density and velocity. The electrical field distribution in the channel varying at different gate and drain bias is also changed by passivation. The combination of the above factors results in the different behaviors of the bias-dependent the small signal ECPs before and after surface passivation.

After passivation, the device showed improved noise performance with decreased $NF_{\min}$, R_n and increased G_a . The $NF_{\min}$ and G_a of passivated device became less dependent on frequency and drain currents. The improved microwave noise performance is proven to be mainly due to the increase of intrinsic g_m , which is due to the increase of 2DEG sheet carrier density and mobility by the suppression of surface trap depletion and remote Coulomb scattering.

The physical mechanism of high-frequency channel noise behavior due to passivation is investigated. It is observed that the channel noise was increased after the surface passivation. This increase is believed to be due to the lateral electrical field profile modification caused by the reduction of surface charge.

Chapter 6

Temperature Dependent Microwave noise

Characterization and Modeling in GaN HEMTs

6.1 Introduction

To provide a reliable GaN HEMT for low noise applications in various environments, it is necessary to evaluate its performance at elevated temperatures. There are a few reports published on the temperature dependent microwave noise characterization for AlGaIn/GaN HEMTs on SiC [14, 126, 127, 128] and sapphire substrates [129]. However, until now still very limited reports on the microwave noise characteristics over various temperatures for GaN HEMTs are available, particularly for GaN HEMTs on Si.

In addition, to design and realize reliable LNAs based on GaN HEMTs for applications in various environments, it is necessary to predict the performance of GaN HEMT not only at various frequencies but also at various temperatures. Thorsell et al. has made an empirical thermal modeling for the microwave noise based on fitted bias coefficients for AlGaIn/GaN HEMTs on SiC [130]. Such empirical models have their inherent limitations in that their temperature coefficients have not much physical meaning, and hence it will be difficult to correlate the temperature variance with the physical mechanisms. On the other hand, analytical models can provide more information about the device physical mechanism and can be helpful for the optimization of the device structure and/or processes to improve the microwave noise performance. However, still very few

reports on the analytical high-frequency noise modeling including temperature dependence for GaN HEMTs are available.

In this chapter, we carried out the temperature dependent characterization and analytical modeling of the microwave noise performance for AlGaIn/GaN HEMTs on high resistivity Si substrate over a wide temperature range from -50 to 200 °C. The contents will be organized as follows. In the first section, a brief introduction is given. Then Section 2 describes the experimental details. In Section 3, the microwave S-parameters and typical noise parameters including $NF_{\min}$, R_n , Γ_{opt} and G_a at different temperatures were measured and their temperature dependent characteristics are modeled using a simple linear or quadratic approximation. In Section 4, the physical mechanisms of the behavior of the overall noise figure and internal noise sources varied with temperature are discussed. In Section 5, comparison was made on the degradation rates of the noise characteristics over temperature between the AlGaIn/GaN HEMT on Si and those on other substrates and GaAs and InP HEMTs. In Section 6 the small signal ECPs and internal noise source coefficients (P , R , and C) were extracted at each measurement temperature and their temperature coefficients were obtained. In Section 7, an analytical thermal model of the overall noise parameters is proposed and based on the Pucel's PRC theory evaluated based on the measured data. In the last section, some key conclusions are drawn.

6.2 Experiments

The AlGaIn/GaN HEMT used in this work was grown on a high-resistivity Si substrate ($>10,000 \Omega\text{-cm}$) by metal-organic chemical vapor deposition (MOCVD).

Its structure details are same as the Fig. 5.1 shows in Chapter 5. The fabrication process is same as that for conventional HEMT described in Chapter 2.

The device with $L_g=0.25 \mu\text{m}$, $W_g=2 \times 75 \mu\text{m}$ and $L_{sd}=2.6 \mu\text{m}$ was studied. The small signal and noise measurement at microwave frequencies from 2 to 20 GHz were performed using ATN NP5 microwave noise test set with HP8510C Vector Network Analyzer (VNA) and HP8970B noise figure meter. The device bias was fixed at $V_d=8 \text{ V}$ and $I_d=250 \text{ mA/mm}$ during the measurement. The temperature dependent measurement was carried out using a Cascade Summit 1000 on-wafer probe station with a Temptronic thermo chuck and the temperature was increased from -50 to 200°C at a step of 25°C .

To explore the physical mechanism inside the temperature dependence of the noise parameters and internal noise sources, the noise source currents $\overline{i_{nd}^2}$, $\overline{i_{ng}^2}$ and their correlations $\overline{i_{nd}i_{ng}^*}$ at each temperature points were extracted using the procedure described in Chapter 4. The channel noise coefficient P , drain noise coefficient R , and their correlation coefficient C were extracted using the following expressions: [122]

$$P = \frac{\overline{i_{nd}^2}}{4kT_0\Delta f|Y_{21}|}, \quad R = \frac{\overline{i_{ng}^2}|Y_{21}|}{4kT_0\Delta f|Y_{11}|^2}, \quad C = \frac{\text{Im}[\overline{i_{nd}i_{ng}^*}]}{\sqrt{\overline{i_{nd}^2}\overline{i_{ng}^2}}} \quad (6.1)$$

The temperature coefficients (TCs) of the noise parameters in AlGaN/GaN HEMTs can be extracted by fitting the measured parameter values using a linear or quadratic equation, as proposed in [131]:

$$\text{Linear:} \quad P(T) = P(T_r)(1 + B(T - T_r)) \quad (6.2)$$

$$\text{Quadratic:} \quad P(T) = P(T_r)(1 + B_1(T - T_r) + B_2(T - T_r)^2) \quad (6.3)$$

where $P(T)$ is the value of the parameter at the temperature of interest, $P(T_r)$ is the value of the parameter at the reference temperature (in this work $T_r=25$ °C), B or B_1 is the linear coefficient and B_2 is the quadratic term coefficient.

The flow chart of the overall modeling procedure in this work is shown in Fig. 6.1. The extraction and de-embedding procedures were repetitively performed at each measurement temperature, so that the temperature dependent small signal ECPs and internal noise source coefficients were obtained. The quadratic approximation as Eqn. 6.3 shows was utilized to depict the temperature dependence of extracted small signal ECPs and internal noise source coefficients. Then these temperature dependent ECPs and noise source coefficients were substituted into the analytical equations and the overall noise parameters including $NF_{\min}$, R_n , R_{opt} and X_{opt} were calculated and compared with the measurement.

6.3 Temperature Dependent Microwave Noise Characteristics

The noise parameters including $NF_{\min}$, R_n , Γ_{opt} and associate gain (G_a) of AlGaIn/GaN HEMT on Si substrate were measured as a function of frequency from 2 to 20 GHz at the base temperature range of -50 to 200 °C in step of 25 °C. Their characteristics are shown in Fig. 6.2 and Fig. 6.3. It was observed that the microwave noise performance of the GaN HEMT on silicon degraded at high temperatures over all the frequencies, similar to the other microwave HEMTs. The increase of the values of $NF_{\min}$ with frequency is faster at higher temperature. At very high temperatures, e.g. 200 °C, the values of $NF_{\min}$ in low frequency region (<10 GHz) show a trend obviously deviating from a linear variation with frequency, which reveals that the gate shot noise generated by the gate leakage current ($I_{g,\text{leak}}$)

Fig. 6.1 Flow chart of the analytically thermal modeling procedure.

becomes more remarkable and plays an more obvious role in the overall noise at high temperatures [52]. However, for the other parameters, such as R_n , Γ_{opt} and G_a , the effect of $I_{g,\text{leak}}$ is not obvious over the measurement frequency range even at high temperatures. The frequency dependences of R_n and Γ_{opt} are less affected by the high temperatures. The value variance of Γ_{opt} with the temperature is very

small. The decrease rate of the G_a values with the frequency gets faster at higher temperature.

Fig. 6.2 Measured noise parameters (a) NF_{min} and (b) R_n as a function of frequency from 2 to 20 GHz at the temperature range of -50 to 200 °C for AlGaIn/GaN HEMT on high-resistivity Si substrate. The device biases were fixed at $V_d=8$ V and $I_d= 250$ mA/mm.

Fig. 6.3 Measured noise parameters (a) Γ_{opt} and (b) G_a as a function of frequency from 2 to 20 GHz at the temperature range of -50 to 200 °C for AlGaIn/GaN HEMT on high-resistivity Si substrate. The device biases were fixed at $V_d=8$ V and $I_d= 250$ mA/mm.

Fig. 6.4 shows the measured noise parameters $NF_{\min}$, R_n , Γ_{opt} (including its magnitude $|\Gamma_{\text{opt}}|$ and angle $\angle \Gamma_{\text{opt}}$), G_a and their normalized values with respect to room temperature at 10 GHz for the AlGaIn/GaN HEMT on high-resistivity Si as a function of temperature from -50 to 200 °C. With the aid of the normalized parameter plot, the variation rates over temperature between different parameters can be easily compared. In the whole measurement temperature range from -50 to 200 °C, all the noise parameters showed non-linear temperature dependency especially at high temperatures. This non-linear temperature dependency can be simulated using simple quadratic approximation (Eqn. (6.3)). The fitted curves are shown in Fig. 6.4. The linear and quadratic terms of TCs for the noise parameters are listed in Table 6.1. There is a small difference between the TCs of $NF_{\min}$ and R_n . As compared to $NF_{\min}$ and R_n , the decrease rate of G_a , $|\Gamma_{\text{opt}}|$ and $\angle \Gamma_{\text{opt}}$ with temperature are much smaller, especially for the $|\Gamma_{\text{opt}}|$, which is almost independent of temperature.

Table 6.1 The measured noise parameters at room temperature $P(T_r)$ and their TCs (B_1 and B_2 in Eqn. (6.3)) (at 10 GHz).

	$NF_{\min}$	G_a	R_n	$ \Gamma_{\text{opt}} $	$\angle \Gamma_{\text{opt}}$
$P(T_r)$	1.59 dB	12.65 dB	46.1 Ω	0.713	39.4°
B_1 ($\times 10^{-3}$ /°C)	3.19	-0.56	4.61	-0.1	-1.11
B_2 ($\times 10^{-6}$ /°C ²)	13.6	-3.4	6.0	-1.3	3.67

Fig. 6.4 Measured (symbols) and modeled (lines) noise parameters of (a) $NF_{\min}$, R_n , G_a and (b) $|\Gamma_{\text{opt}}|$, $\angle \Gamma_{\text{opt}}$ at various temperature from -50 to 200 $^{\circ}\text{C}$ at the frequency of 10 GHz and at the bias of $V_d=8$ V and $I_d=250$ mA/mm.

6.4 Discussion on the Physical Mechanisms in the Temperature Dependence of Noise Figure

It is well known that the minimum noise figure greatly depends on the intrinsic current-gain cut off frequency $f_{T,\text{int}}$. The $NF_{\min}$ can be expressed using the following equation (high order frequency terms are neglected): [122]

$$NF_{\min} \approx 1 + 2 \frac{f}{f_{T,\text{int}}} \sqrt{K_g \left(K_r + g_m (R_s + R_g) \right)} \quad (6.4)$$

where K_g and K_r are the functions of the three internal noise source coefficients (P , R , and C) as defined in the following equations:

$$K_g = P + R - 2C\sqrt{PR}, \quad K_r = \frac{PR(1-C^2)}{P + R - 2C\sqrt{PR}} \quad (6.5)$$

However, $f_{T,int}$ does not decrease much as the temperature increases, as shown in Fig. 6.5. This means that the temperature behavior of $f_{T,int}$ is not the dominant factor in the temperature dependence of the NF_{min} . The $f_{T,int}$ values in the plot were calculated by $f_{T,int} = g_m / 2\pi(C_{gs} + C_{gd})$ and the small signal ECPs (g_m , C_{gs} , C_{gd} etc.) were extracted using the procedure described elsewhere [121].

Fig. 6.5 Intrinsic current-gain cut off frequency $f_{T,int}$ at various temperature and their normalized values to the values at room temperature.

In Eqn. (6.4), the first term K_r inside the square root results from the internal noise sources, and the second term $g_m(R_s + R_g)$ results from the thermal noise generated by the extrinsic access resistance R_g and R_s . The temperature dependent values of g_m , R_s , R_g and their normalized values with respect to the values at room temperature are shown in Fig. 6.6. The high increase rate of R_s over temperatures is due to the high degradation rate of the electron mobility at high temperature [132]. The increase of R_g at high temperature comes from the metal resistivity properties.

In Fig. 6.6 (b) the normalized value of the term $g_m(R_s+R_g)$ is also plotted. It can be seen that, due to the degradation of the g_m with the increasing temperature, the thermal coefficient of the term $g_m(R_s+R_g)$ is smaller compared to that of the extrinsic access resistance R_s+R_g .

Fig. 6.6 (a) Measured (symbols) and modeled (lines) g_m , R_g and R_s and (b) their normalized values to the values at room temperature at various temperatures from -50 to 200 $^{\circ}\text{C}$ at the bias of $V_d=8$ V and $I_d=250$ mA/mm.

In this work, because the value of $g_m(R_s+R_g)$ is only around 50% of the value of K_r at the measurement gate and drain biases, the temperature behavior of the internal noise sources plays an important role in the temperature dependence of the overall $NF_{\min}$. The absolute and normalized values of internal noise source coefficients P , R and C obtained from the extraction procedure described in [121] as a function of temperature from -50 to 200 $^{\circ}\text{C}$ are shown in Fig. 6.7. The fitted curves using the quadratic approximation (Eqn. (6.3)) are also plotted in Fig. 6.7. The fitted values of linear term and quadratic term for P , R and C versus temperature are listed in Table 6.2. It is observed that the values of P and R increase with temperature whereas the values of C decrease with temperature. As a

result, this leads to a degradation of the overall noise performance of the HEMTs. This is because P and R are both proportional to the drain and gate noise current while C works as a cancellation factor between the gate noise current and drain noise current [122]. The temperature variations of P and C are shown to be linear and that of R shows a strong non-linearity in the whole measurement temperature range. R increases much faster with temperature as compared to P and C .

Fig. 6.7 (a) Temperature dependent internal noise source coefficients P , R , C (symbols: measured; lines: modeled) and (b) their normalized values to the values at room temperature from -50 to 200 °C.

Table 6.2 The values of the internal source coefficients P , R and C at room temperature ($P(T_r)$) and their TCs (B_1 and B_2 , in Eqn. (6.3)).

	P	R	C
$P(T_r)$	1.36	0.47	0.55
B_1 ($\times 10^{-3}$ /°C)	3.82	3.44	-0.67
B_2 ($\times 10^{-6}$ /°C ²)	0	26.8	0

According to the microwave-noise source theory by Pucel et al. [122] and Y. Ando et al. [133], the channel noise coefficient P is comprised of two parts:

$P=P_1+P_2$, where P_1 denotes the contribution from the thermal noise in the ohmic region of the channel (Region I, with the length L_1), and P_2 demotes the contribution from the diffusion noise in the saturated velocity region (Region II, with the length L_2). The calculated temperature-dependent normalized values with respect to the values at room temperature for P_1 and P_2 based on the equations in [133] are plotted in Fig. 6.8 (a).

Fig. 6.8 Calculated temperature-dependent normalized values to the values at room temperature for P_1 and P_2 .

It is obvious that P_1 increases much faster than P_2 with the increase of the temperature. P_2 even decreases slightly with temperature. One physical factor responsible for the much higher thermal coefficient of P_1 than P_2 is that the thermal noise (or Johnson noise) generated in Region I has the expression of Nyquist equation and is proportional to the temperature; while the diffusion noise from the dipole layer formation and drift in Region II has the expression of shot noise, and is not related the temperature [122]. In addition, the length of Region II L_2 becomes shorter at higher temperatures. This is due to the fact that the degradation rate of the electron low-field mobility μ with temperature is much higher than the degradation rate of the saturated velocity v_{sat} [132, 134]. The

intrinsic voltage across the channel region beneath the gate (V_{dsi}) decreases at high temperatures, which slightly contributes to the above-mentioned L_2 shortening. The decrease of V_{dsi} at high temperatures can be explained using the following equation:

$$V_{dsi} = V_d - I_{ds} (R_s + R_d) \quad (6.6)$$

During the measurement, the drain current I_{ds} was kept fixed but the access resistances R_s and R_d both increase with the temperature.

More noise contribution from Region I at higher temperatures is also reflected in the temperature behavior of the correlation coefficient C . Since the correlation coefficient between the diffusion noise in Region II and its induced gate noise is unity, and the correlation coefficient between the thermal noise in Region I and its induced gate noise is smaller than unity, the L_2 reduction should lead to the C reduction. As shown in Fig. 6.7 (a) and (b), the noise correlation coefficient C shows a negative temperature coefficient.

For the similar reason, the gate induced noise coefficient by thermal noise in Region I (R_1) also increases much faster than the gate induced noise coefficient by diffusion noise in Region II (R_2), as Fig. 6.8 (b) shows.

6.5 Comparison with Other Types of HEMTs

Table 6.3 summarizes the linear TCs (B) (Eqn. (6.2)) of the three main noise parameters (NF_{min} , R_n , and G_a) at a relatively small temperature range from room temperature (RT) to around 150 °C for various types of HEMTs calculated from this work and published reports. The absolute values of the noise parameters at reference temperature $P(T_r)$ are also shown in the table. All the noise parameters were measured at 10 GHz except ref. [127] (3 GHz), ref. [128] (9 GHz) and ref.

[135] (12 GHz). From the table it can be seen that the degradations of the noise parameters $NF_{\min}$, R_n and G_a at high temperatures for our GaN HEMTs on Si are comparable to the reported GaN HEMTs on SiC or sapphire substrates. As for the degradation rate of $NF_{\min}$ and G_a with increasing temperature, the GaN HEMTs are also found to be comparable to the GaAs and InP based HEMTs. The shortcoming of the GaN HEMTs is the relatively higher absolute value of R_n , which is believed to be mainly due to the lower g_m and higher extrinsic R_s caused by the relatively lower low-field electron mobility μ_0 in AlGaIn/GaN 2DEG channel (typically $\mu_0=8000, 10000, 1400 \text{ cm}^2/\text{V}\cdot\text{s}$ respectively for the 2DEG channel in AlGaAs/GaAs, InAlAs/InGaAs and AlGaIn/GaN heterostructures [136]). However, as far as the thermal coefficient of R_n is concerned, the AlGaIn/GaN HEMT in our work shows similar values to GaAs HEMTs.

The comparison of the linear TCs of P , R , and C (in Eqn. (6.2)) at a temperature range from room temperature to around 150 °C between GaN HEMTs and GaAs pHEMTs (currently only GaAs pHEMT was available from reports) are shown in Table 6.4. It can be seen that the absolute values of P and C for our GaN HEMT at room temperature are comparable with the reported GaAs pHEMTs. But the value of R for our GaN HEMT is larger, which leads to the higher absolute values of measured $NF_{\min}$ and R_n . For the GaN HEMT the increase of P with the temperature is slightly faster but the increase of R and the decrease of C is slower compared with the GaAs pHEMT. Thus the resulting degradation of the overall noise performance with temperature is similar between GaN HEMTs and GaAs HEMTs.

Table 6.3 Measured noise parameters ($NF_{\min}$, R_n and G_a) at reference temperature $P(T_r)$ (linear TCs B , 10^{-3} /°C) for various HEMTs.

Material	$NF_{\min}$ (dB)	R_n ($\Omega \square$ mm)	G_a (dB)	REF.
GaAs HEMT	1.1(6.06)	N.A.	N.A.	[137]
GaAs pHEMT	0.64(11.5)	N.A.	N.A.	[138]
GaAs pHEMT	1.07(5.61)	2.47(4.5)	N.A.	[139]
GaAs pHEMT	0.83(5.83)	3(4.93)	N.A.	[131]
GaAs pHEMT	0.46(9.52)	N.A.	13(-0.95)	[140]
InP HEMT	0.79(5.67)	N.A.	N.A.	[141]
InP HEMT	0.5(8.02)	N.A.	N.A.	[142]
AlGaIn/GaN HEMT on SiC	1.13(6.95)	N.A.	4.58(-0.83)	[127]
AlGaIn/GaN HEMT on SiC	1.13(8.17)	N.A.	11.9(-1.14)	[129]
AlGaIn/GaN HEMT on SiC	1.07(7.2)	8.05(8.01)	18.1(-0.73)	[143]
AlGaIn/GaN HEMT on SiC	0.74(9.85)	N.A.	10.6(-0.74)	[14]
AlGaIn/GaN HEMT on SiC	1.13(4.54)	4(6.5)	11.6(-1.59)	[128]
AlGaIn/GaN HEMT on sapphire	0.54(23.9)	N.A.	11.4(-1.31)	[14]
AlGaIn/GaN HEMT on Si	1.59(4.84)	6.92(5.34)	12.65(-0.97)	This work

Table 6.4 The values of intrinsic noise coefficients (P , R , and C) at reference temperature $P(T_r)$ (linear TCs B , 10^{-3} /°C) for various HEMTs.

Material	P	R	C	REF
GaAs pHEMT	0.69(3.5)	0.13(38.6)	0.82(-8.5)	[131]
GaAs pHEMT	1.34(3.18)	0.29(6.31)	0.24(-1.41)	[135]
AlGaIn/GaN on Si	1.36(3.82)	0.47(5.09)	0.55(-0.67)	This Work

6.6 Temperature Dependence of the Internal Noise Source Coefficients and Small Signal ECPs

Fig. 6.9 (a)-(e) show the values of P , R and C and small signal ECPs (as defined in the equivalent circuit of Fig.3.1 in Chapter 3) in the AlGaIn/GaN HEMTs on Si substrate extracted from the measured small signal S-parameters and noise parameters as a function of temperature from -50 to 200 °C. Here the frequency variances of P , R , C were not involved and their values were obtained from the means of the data at the flat region in the plots of $P(R,C)$ versus frequency. The influence of their frequency variances will be discussed later. The fitted curves are also plotted in Fig. 6.9 using the quadratic approximation (Eqn. (6.4)). The fitted values of linear and quadratic terms (B_1 and B_2) for P , R and C and small signal ECPs versus temperature are listed in Table 6.5.

Table 6.5 P , R , C and small signal ECPs at room temperature ($P(T_r)$) and their thermal coefficients (B_1 and B_2 in Eqn. (6.4), B_1 : 10^{-3} /°C, B_2 : 10^{-6} /°C²).

	R_g	R_s	R_d	g_m	C_{gs}	C_{gd}	C_{ds}
$P(T_r)$	4.1 Ω	4.8 Ω	8.3 Ω	33.4 mS	108.9 fF	14.8 fF	5.0 fF
B_1	4.74	7.1	6.6	-0.81	-0.44	1.1	2.48
B_2	-10.5	13.3	10.65	3.4	3.1	0	0
	R_{ds}	R_{gd}	R_{gs}	τ	P	R	C
$P(T_r)$	329 Ω	44.7 Ω	1.7 Ω	0.22 ps	1.36	0.47	0.55
B_1	0.62	-5.24	4.85	-2.1	3.82	3.44	-0.67
B_2	-13.4	22.5	-40	30.9	0	26.8	0

Fig. 6.9 (a)-(e). Temperature dependent noise source coefficients (P , R , C) and small signal ECPs (symbols: measured; lines: modeled) in AlGaIn/GaN HEMTs on Si from -50 to 200 °C.

6.7 Analytical Modeling and Discussion

Although the measured four microwave noise parameters $NF_{\min}$, R_n , $|I_{\text{opt}}|$ and $\angle I_{\text{opt}}$ of the AlGaIn/GaN HEMT at various temperatures can be modeled well using a simple empirical quadratic model, it cannot provide insight into the physical mechanisms. An analytical models can be helpful for the optimization of the device structure and/or processes to improve the microwave noise performance. The widely-used analytical models for high-frequency noise include the Fukui model [144], the PRC model proposed by Pucel et al. [122], and the resistor temperature noise model proposed by Pospieszalski [145]. The Fukui model is expressed as:

$$NF_{\min} = 1 + 2\pi K_f f C_{gs} \sqrt{\frac{R_g + R_s}{g_m}} \quad (6.7)$$

where the coefficient K_f is a semi-empirical parameter. The validity of the model depends on the assumptions that the induced gate noise and the quadratic term of the frequency are negligible as well as the correlation coefficient between gate and drain noise is unity [146], thus this model is not suitable for our GaN HEMT since its induced gate noise and correlation coefficient do not agree on the above assumptions (See the values of R and C in Fig. 6.9 (a) and Table 6.5).

In [122] Pucel et al. defined another three parameters K_g , K_r and K_c as the functions of the internal noise source coefficients P , R , and C :

$$K_g = P + R - 2C\sqrt{PR}, \quad K_r = \frac{PR(1-C^2)}{P + R - 2C\sqrt{PR}}, \quad K_c = \frac{P - C\sqrt{PR}}{P + R - 2C\sqrt{PR}} \quad (6.8)$$

The intrinsic microwave noise parameters are calculated by:

$$\left\{ \begin{array}{l} g_n = K_g \frac{\omega^2 C_{gs}^2}{g_m}, r_n = K_r \left(1 + \frac{\omega^2 C_{gs}^2 R_i^2}{g_m} \right), \\ Z_c = R_c + jX_c = K_c \left(R_i - \frac{j}{\omega C_{gs}} \right) \\ NF_{\min} = 1 + 2g_n \left(R_c + \sqrt{R_c^2 + \frac{r_n}{g_n}} \right) \\ R_n = r_n + g_n |Z_c|^2, \\ R_{opt} = \sqrt{\frac{r_n}{g_n} + R_c^2}, X_{opt} = -X_c \end{array} \right. \quad (6.9)$$

It should be noted that the above model does not take into account the feedback capacitance C_{gd} . In addition, the relationships between the $NF_{\min}$, R_n and Z_{opt} and the small signal ECPs are complicated and not direct as three median variances r_n , g_n and Z_c are required. We simplify the above formulas, include the effects of C_{gd} and then get the following expressions:

$$\left\{ \begin{array}{l} NF_{\min} = 1 + 2 \frac{\omega(C_{gs} + C_{gd})}{g_m} \sqrt{K_g K_r} + 2 \frac{\omega^2(C_{gs} + C_{gd})^2}{g_m} K_g K_c R_i \\ R_n = \frac{P}{g_m} + \frac{\omega^2(C_{gs} + C_{gd})^2 (K_g K_c^2 + K_r^2) R_i^2}{g_m} \\ R_{opt} = \sqrt{\frac{K_r}{K_g \omega^2 (C_{gs} + C_{gd})^2} + K_c^2 R_i^2} \\ X_{opt} = \frac{K_c}{\omega C_{gs}} \end{array} \right. \quad (6.10)$$

Another widely-used analytical model in the low noise devices and circuits is the resistor temperature model described by Pospieszalski in [145]. This model assigns two uncorrelated equivalent noise temperature T_g , T_d to the input resistor R_{gs} and output resistor R_{ds} , respectively. The original mode in [145] neglected the

effects of the C_{gd} . After including the C_{gd} , the intrinsic noise parameters are expressed as:

$$\left\{ \begin{array}{l} NF_{\min} = 1 + \frac{2}{T_0} \frac{\omega(C_{gs} + C_{gd})}{g_m} \sqrt{\frac{T_g T_d R_i}{R_{ds}} + \left(\frac{\omega(C_{gs} + C_{gd})}{g_m} \right)^2 \frac{T_d^2 R_i^2}{R_{ds}^2}} \\ \quad + \frac{2}{T_0} \left(\frac{\omega(C_{gs} + C_{gd})}{g_m} \right)^2 \frac{T_d R_i}{R_{ds}} \\ R_n = \frac{T_g}{T_0} R_i + \frac{T_d}{T_0} \frac{1 + \omega^2 C_{gs}^2 R_i^2}{R_{ds} g_m^2} \\ R_{opt} = \sqrt{\left(\frac{g_m}{\omega(C_{gs} + C_{gd})} \right)^2 \frac{T_g}{T_d} R_i R_{ds} + R_i^2} \\ X_{opt} = \frac{1}{\omega C_{gs}} \end{array} \right. \quad (6.11)$$

where T_g , T_d are related to K_g and K_r (K_g and K_r are defined in Eqn. (6.8)):

$$T_d = T_o K_g g_m R_{ds}, \quad T_g = \frac{T_o K_r}{g_m R_{ds}} \quad (6.12)$$

As presented in the previous section, the internal noise source coefficients P , R , C and the small signal ECPs are all varying with the temperature and the relations can be expressed as a quadratic function (Eqn. (6.4)) as shown in Fig. 6.9 with the temperature coefficients listed in Table 6.5. These temperature-dependent P , R , C and the small signal ECPs can be substituted into the above three models Eqns. (6.9), (6.10) and (6.11), and then the modeled noise parameters at various temperatures were obtained. Fig. 6.10 (a)-(d) plots the results of the measured (extracted from the measured overall parameters) and modeled noise intrinsic parameters $NF_{\min}$, R_n , R_{opt} and X_{opt} at 10 GHz at the temperature range from -50 to 200 °C.

Fig. 6.10 The measured (extracted from the measured overall parameters) and modeled noise intrinsic parameters (a) $NF_{\min}$, (b) R_n , (c) R_{opt} (d) X_{opt} at 10 GHz at the temperature range from -50 to 200 $^{\circ}\text{C}$.

From Fig. 6.10, it can be seen that the results of our modified model (Eqn. (6.10)) agree with the measurement very well over the whole temperature range. The feedback capacitance C_{gd} plays an obvious role in the intrinsic noise parameters $NF_{\min}$ and R_{opt} , but has little contribution to the values of R_n and X_{opt} , although the values of C_{gd} are around 10 - 20% of C_{gs} (See Fig. 6.9 (b) and (c)). This point can be easily understood from Eqn. (6.10). C_{gd} contributes to the total gate-to-channel coupling capacitor ($C_g = C_{\text{gs}} + C_{\text{gd}}$), and this coupling capacitor is one of the key factors determining the gate noise induced by the channel noise. As

for R_n , C_{gd} only exists in the second term $(\frac{\omega^2 (C_{gs} + C_{gd})^2 (K_g K_c^2 + K_r^2) R_i^2}{g_m})$, which

gives a minor contribution to R_n , so C_{gd} plays a minor role. The results of the modeling using the resistor temperature noise model including the C_{gd} (Eqn. (6.11)) agree well with the measurement for NF_{min} and R_{opt} but not for R_n and X_{opt} , especially at high temperatures.

The deviation of the value of modeled X_{opt} from measurement for the resistor temperature model is due to the assumption $K_c=1$ or $C=\sqrt{R/P}$ [13], which is not true in the GaN HEMT especially at high temperatures. If we use the actual K_c values for calculation, the expression of X_{opt} in Eqn. (6.11) will be the same as that in Eqn. (6.10), and the modeled X_{opt} values will be same as the original PRC model Eqn. (6.9) and our modified model Eqn. (6.10).

In addition, in the actual application of low noise MMIC, the HEMT is generally embedded in the circuit and the values of the parasitic capacitances and inductances in the equivalent circuit Fig. 3.1 in Chapter 3 will be different from the discrete devices as used for our characterization, but the access resistances R_g , R_s and R_d will still remain the same. The access resistances, mainly the input access resistance R_g and R_s , will generate Johnson noise (or thermal noise, Eqn. (4.24)) and contribute to the overall noise figure obviously. So from the perspective of low noise circuit designing, it will be more useful to provide the whole model including the effect of access resistances. However, with regard to the resistor temperature noise model, it is difficult to involve R_s and R_g directly into the expression (Eqn. (6.11)) and get a simple expression. For the PRC model, the involvement of R_s and R_g is rather straightforward as described in [147]. But in

[147], the effect of C_{gd} is still excluded. For our modified model Eqn. (6.10), after including the access resistances, the expressions become:

$$\left\{ \begin{array}{l} NF_{\min} = 1 + 2 \frac{\omega(C_{gs} + C_{gd})}{g_m} \sqrt{K_g (K_r + g_m (R_s + R_g))} \\ \quad + 2 \frac{\omega^2 (C_{gs} + C_{gd})^2}{g_m} K_g (R_s + R_g + K_c R_i) \\ R_n = R_g + R_s + \frac{P}{g_m} + \frac{\omega^2 (C_{gs} + C_{gd})^2 (K_g (R_g + R_s + K_c R_i)^2 + K_r^2 R_i^2)}{g_m} \\ R_{opt} = \sqrt{\frac{K_r + g_m (R_g + R_s)}{K_g \omega^2 (C_{gs} + C_{gd})^2} + (R_g + R_s + K_c R_i)^2}, \quad X_{opt} = \frac{K_c}{\omega C_{gs}} \end{array} \right. \quad (6.13)$$

Fig. 6.11 (a)-(d) shows the measured and modeled results of noise parameters (a) $NF_{\min}$, (b) R_n (c) R_{opt} (d) X_{opt} for the intrinsic circuit together with R_g , R_s and R_d for AlGaIn/GaN HEMT on high-resistivity Si substrate at 10 GHz as a function of ambient temperature. The modeled results include our modified model Eqn. (6.13) and that by V. Guru et al.[147]:

$$\left\{ \begin{array}{l} g_n = K_g \frac{\omega^2 C_{gs}^2}{g_m}, r_n = R_s + R_g + K_r \left(\frac{1 + \omega^2 C_{gs}^2 R_i^2}{g_m} \right), \\ Z_c = R_c + jX_c = R_s + R_g + K_c \left(R_i - \frac{j}{\omega C_{gs}} \right) \\ NF_{\min} = 1 + 2g_n \left(R_c + \sqrt{R_c^2 + \frac{r_n}{g_n}} \right) \\ R_n = r_n + g_n |Z_c|^2, \\ R_{opt} = \sqrt{\frac{r_n}{g_n} + R_c^2}, \quad X_{opt} = -X_c \end{array} \right. \quad (6.14)$$

Fig. 6.11 The measured and modeled results of noise parameters (a) $NF_{\min}$, (b) R_n (c) R_{opt} (d) X_{opt} for the intrinsic circuit together with R_g , R_s and R_d for AlGaIn/GaN HEMT on high-resistivity Si substrate at 10 GHz as a function of ambient temperature.

The above Eqn. has taken R_s and R_g but not C_{gd} into consideration, so its modeled results of $NF_{\min}$, R_{opt} do not match well with the extracted data, similar to the case of intrinsic circuit (Fig. 6.10). The results of our modified model including the access resistances match well with the measurement data once again, indicating the aforementioned importance of the feedback capacitance C_{gd} for the temperature dependent high frequency noise modeling.

The above evaluations for the proposed models (Eqn. (6.10)) have adopted the mean values of the P (or R, C) over frequency, as mentioned in Section III. In

other words, it has been assumed that the P (R, C) are frequency independent. In fact, this assumption is true at most frequencies and temperature points except those at very high temperatures and low frequencies, as Fig. 6.12 shows. As seen from the figure, P is frequency independent at almost all frequencies and all temperatures at the measurement range. R shows an obvious decrease with frequency when $T > 150$ °C and at relatively low frequency region (< 8 GHz). And C also shows an increase with frequency at these points. The frequency dependence of R and C leads to significant errors for the proposed model at these high

Fig. 6.12 Extracted P , R , C at whole frequency range from 2-20 GHz and at various temperatures. Scatter: directly extracted data; line: mean values over the flat region; dashed line: modeled values involving the frequency dependence.

temperature and low frequency points. Fig. 6.13 (a) shows the frequency-dependent $NF_{\min}$ from 50 to 200 °C measured (scatters) and simulated (lines) with the proposed model (Eqn. (6.10) and frequency independent R and C . It can be seen that at high temperatures (especially at 200 °C), large gap exists between the simulated results and the measured data at low frequency region.

To expand the application range of the proposed model to cover the high temperature and low frequency region, the frequency dependence of R and C can be involved. It is believed that the frequency dependence of R and C for the GaN HEMT in this work mainly ascribes to the gate shot noise caused by the gate leakage current. So R can be expressed as:

$$R = R_{ind} + \frac{2}{\omega^2} \frac{g_m}{C_{gs}^2} q I_g \quad (6.15)$$

where R_{ind} accounts for the induced gate noise, I_g is the gate leakage current and its values can be obtained by fitting the measured R versus frequency at each temperature. I_g exponentially increases with temperature when the temperature is not too low (>25 °C in this work):

$$I_g = A_{I_g} \exp(B_{I_g} T) \quad (6.16)$$

where A_{I_g} and B_{I_g} are two coefficients, and their values can be obtained by fitting the values of I_g with temperature using above equation.

C can be expressed as:

$$C = \frac{1}{C_1 + \frac{C_2}{\omega}} \quad (6.17)$$

C_1 , C_2 can be obtained by fitting the values of C versus frequency at each temperature. The temperature dependence of C_1 and C_2 are considered to follow the quadratic approximation (Eqn. 6.3).

By this means the frequency dependence of R and C are modeled. The simulated R and C at 150 °C and 200 °C are plotted in Fig. 6.12 (c) and (d) (dashed

line). The simulated frequency-dependent $NF_{\min}$ are shown in Fig. 6.13 (b). It can be seen that, the accuracy of the models in the region of low frequencies and high temperatures is greatly improved after including the frequency dependent model of R and C (Eqns. (6.15)-(6.17)).

Fig. 6.13 Measured and modeled results of $NF_{\min}$ using frequency independent P , R , C (a) and frequency dependent P , R , C (Eqn. (12)-(14)) (b). Scatter: measured data; line: modeled results.

6.8 Conclusion

In this chapter the temperature dependent microwave noise characteristics of AlGaIn/GaN HEMT on Si were investigated and analytically modeled over a wide temperature range from -50 to 200 °C. The physical mechanisms of the thermal behavior of the microwave noise are discussed. It was found that the degradation rates of noise parameters with temperature including $NF_{\min}$, R_n , $|F_{\text{opt}}|$ and $\angle F_{\text{opt}}$, together with G_a for the GaN HEMT on Si is comparable to those of reported GaN HEMTs on SiC and sapphire substrates and also comparable to the GaAs and InP low noise HEMTs. The temperature variances of the internal noise source coefficients P , R and C were also found to be comparable to those of GaAs HEMT. This indicates the excellent potential of the GaN HEMT on Si for low noise application at high temperatures.

The thermal dependence of the microwave noise was analytically modeled. The small signal ECPs and internal noise source coefficients were extracted at each temperature and their thermal variations was fitted using a quadratic equation. Two commonly used analytical models, namely the original Pucel's PRC model and the Pospiesalski's resistor temperature noise model are compared with our proposed model. It is found that in order to improve the accuracy of the analytical model for all the noise parameters over temperature, it is important to include C_{gd} in the model. Frequency dependent R and C are needed to be included, considering the effect of the gate leakage current, to accurately simulate the noise at high temperature and low frequency regions.

Chapter 7

GaN MISHEMT on Silicon with ALD Grown Al_2O_3 as Gate Insulator

7.1 Introduction

Although GaN HEMTs with Schottky metal gate have demonstrated excellent performance in high frequency [148], high power [149] and more recently low microwave noise [14, 150] applications, they typically suffer from high gate leakage current, which degrades their noise performance due to the high gate shot noise based on the Eqn. (1.4) and (1.5) [49].

GaN MISHEMTs with a thin dielectric film as gate insulator is one of the effective solutions to reduce the high gate leakage current. Higher RF output power can be achieved in MISHEMTs owing to the higher positive gate voltage swing and thereby higher maximum drain current arising from the lowered gate leakage current [151]. Higher microwave noise performance can also be expected in MISHEMTs due to the low gate leakage current thereby resulting in low gate shot noise [49]. M. Yanagihara has presented an AlGaIn/GaN MISHEMT on sapphire substrate with 2-nm *in situ* SiN as gate insulator showing a low noise figure of 1.4 dB at 28 GHz [8]. However, to our best knowledge, no reports on the microwave noise characteristics of GaN MISHEMT on Si substrate are available.

Different dielectric materials have been investigated as the gate insulator materials for GaN MISHEMTs, such as Si_3N_4 [152, 153], SiO_2 [154], Al_2O_3 [47, 155, 156, 157], Ga_2O_3 [158], HfO_2 [159], Sc_2O_3 [160] etc. Among these materials, Al_2O_3 is one of the most attractive materials due to its high band-gap, high

dielectric constant and high breakdown field. As compared with the preparation methods like RF sputtering, Al metal oxidizing etc, the atomic layer deposition (ALD) has the advantages of nanometer scalability, high uniformity and low defect density etc. The ALD- Al_2O_3 /AlGaIn/GaN MISHEMTs with good DC performance have been reported [155, 156, 157]. However, there are still few reports available on the comprehensive study of the effects of ALD- Al_2O_3 gate insulator on the 2DEG in Al_2O_3 /AlGaIn/GaN MISHEMTs.

In addition to low noise figure, high linearity is also critical for many low-noise communication applications [161]. Conventional GaN HEMTs have demonstrated excellent linearity performance for high power and low noise applications [162, 163, 164]. For MISHEMT, it generally has a broader transconductance (g_m) versus gate bias characteristics than the conventional HEMT [152], [165]. Hence, it is expected that the MISHEMT based LNAs will have a better linearity performance, such as higher output third-order intercept point (OIP3), than the conventional HEMT. High linearity has been reported in the GaN MIS double-heterojunction FETs (MISDHFETs) on SiC with SiO_2 as gate dielectric [165]. However, to our best knowledge, there are still few publications on the linearity characteristics in low noise GaN MISHEMTs on Si.

In this chapter, GaN MISHEMTs on high-resistivity Si substrate with ALD grown Al_2O_3 as the gate insulator have been developed and characterized. The effects of ALD Al_2O_3 gate insulator on the 2DEG properties in the MISHEMTs were investigated. We demonstrate for the first time a 0.25- μm gate-length ALD- Al_2O_3 /AlGaIn/GaN MISHEMT on high-resistivity silicon substrate with excellent microwave small signal and noise performance at X-band. Bias dependent DC, microwave and noise characteristics were measured in the 0.25- μm AlGaIn/GaN

MISHEMT using ALD Al₂O₃ as gate insulator. The improved device linearity shows that the ALD Al₂O₃/AlGa_{0.3}N/GaN MISHEMT on high-resistivity silicon substrate is promising for high-linearity LNA applications.

A comparative study on the characteristics of the conventional HEMTs with Schottky metal gate and the MISHEMTs with ALD Al₂O₃ as gate dielectric has been carried out. The two types of devices were fabricated using the same processes on the same batch of wafers (with the same epitaxial structure). For the comparison, at least five devices for each characteristic were tested. Although there exist some variations in the measured results, we can still observe some typical values with clear trends between the two types of devices.

7.2 Study on the 2DEG Properties in ALD Al₂O₃/AlGa_{0.3}N/GaN MISHEMT

In this section the GaN MISHEMT was grown on a high-resistivity silicon substrate (>6000 Ω·cm) by MOCVD with its epilayer including a 2.5-nm GaN cap layer, a 20 nm Si-doped AlGa_{0.3}N barrier, a 1.2 nm AlN spacer and an un-doped

Fig. 7.1 Schematic of the structure for the ALD Al₂O₃ AlGa_{0.3}N/GaN MISHEMT on high resistivity silicon substrate used in this chapter.

GaN buffer. The structure details are shown in Fig. 7.1.

The fabrication processes for the ALD Al₂O₃/AlGaN/GaN MISHEMT were the same as those described in Chapter 2. The conventional Schottky-gate AlGaN/GaN HEMT for comparison has the same device structure and fabrication process as the MISHEMT except that a 10 nm Al₂O₃ was deposited by ALD as the gate dielectric for the MISHEMT. Both devices were without any additional surface passivation. A 1.0 μm gate was fabricated by normal photolithography process using contact mask aligner and Ni/Au deposition/lift-off, instead of the sub-micron gate using EBL system. The C-V and I-V measurements for the diodes were carried out using an Agilent B1500A semiconductor parameter analyzer. The dynamic DC measurement was carried out using an Accent D265 dynamic IV analyzer (Diva).

The dielectric constant of the ALD-Al₂O₃ ϵ_{ox} is determined to be 8.6 through the metal-insulator-metal (MIM) structures ($\epsilon_{\text{ox}} = C * d / (A \epsilon_0)$, where d is the thickness of the Al₂O₃ insulator in MIM measured by an ellipsometer, A is the area, and ϵ_0 is the vacuum permittivity). This value is in agreement with the reported 8.5 for the Al₂O₃ grown by MOCVD [166] and 9.0 for the Al₂O₃ deposited by PE-ALD [155]. Fig. 7.2 (a) shows the measured C-V curves (at frequency of 1 MHz) for conventional AlGaN/GaN Schottky diode and Al₂O₃/AlGaN/GaN MIS diode (diameter=300 μm). The C-V curves show a sharp transition from the deep depletion to accumulation and a small hysteresis (≈ 0.16 V), indicating the good quality of the Al₂O₃ dielectric film and the low trap density at the interface between Al₂O₃ and III-Nitride semiconductor. The thickness of Al₂O₃ gate insulator in MISHEMT is extracted to be around 10 nm from the C-V curve, using the equations in accumulation region:

Fig. 7.2 (a) C-V characteristics of the Al₂O₃/AlGa_{0.3}N/GaN MIS diode and the conventional AlGa_{0.3}N/GaN diode. (b) The extracted 2DEG n_s versus the gate bias.

$$\frac{1}{C_{\text{MISHEMT}}} = \frac{1}{C_{\text{HEMT}}} + \frac{1}{C_{\text{ox}}} \quad (7.1)$$

where

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}} \epsilon_0 A}{d} \quad (7.2)$$

The values of C_{MISHEMT} and C_{HEMT} are read from the plateau region of the C-V curves for MISHEMT and HEMT respectively.

Fig. 7.2 (b) plots the 2DEG sheet density (n_s) as a function of gate voltage (V_g) calculated from the C-V results by:

$$n_s = \int_{V_{\text{th}}}^{V_g} \frac{C(V_g)}{qA} dV_g \quad (7.3)$$

where V_{th} is the threshold voltage. At $V_g=0$ V, the MIS diode shows a slightly smaller n_s value ($7.2 \times 10^{12} \text{ cm}^{-2}$) compared with the conventional Schottky diode ($8.4 \times 10^{12} \text{ cm}^{-2}$). N. Maeda et al. has reported that the n_s was increased by around 58% in Al₂O₃/AlGaIn/GaN MIS-heterostructure with the Al₂O₃ deposited by electron cyclotron resonance (ECR). [167] However, no obvious increase in n_s was observed for ALD-Al₂O₃/AlGaIn/GaN MIS-heterostructure in our work, which shows that there does not exist any evident additional positive charge inside the ALD-Al₂O₃ dielectric or at the interface. From the measurements conducted on the on-wafer Van de Pauw patterns, the Al₂O₃/AlGaIn/GaN structure shows a lower sheet resistance (R_{sh}) ($355 \text{ } \Omega/\square$) compared with the conventional AlGaIn/GaN heterostructure ($390 \text{ } \Omega/\square$), indicating that the electron mobility μ in 2DEG is increased due to the Al₂O₃ passivation effect because of

$$R_{\text{sh}} = \frac{1}{qn_s \mu} \quad (7.4)$$

The mobility increase is re-confirmed by the FATHMT technique that will be described later.

The apparent electron concentration (N_a) versus the corresponding depth (d) in Al₂O₃/AlGa_{0.3}N/GaN MIS heterostructure ($d > t_{\text{cap}}$) can be extracted from the C-V measurements by [168]:

$$N_a = -\frac{2}{qA^2 \epsilon_r \epsilon_0} \frac{dV_g}{d(1/C(V_g)^2)} \quad (7.5)$$

where

$$\epsilon_r = \begin{cases} \epsilon_{\text{AlGa}N}, & d \leq t_{\text{ox}} + t_{\text{cap}} + t_{\text{bar}} \\ \epsilon_{\text{Ga}N}, & d > t_{\text{ox}} + t_{\text{cap}} + t_{\text{bar}} \end{cases}$$

$$d = \begin{cases} \frac{\epsilon_{\text{AlGa}N} \epsilon_0 A}{C(V_g)} + \left(1 - \frac{\epsilon_{\text{AlGa}N}}{\epsilon_{\text{ox}}}\right) t_{\text{ox}} + \left(1 - \frac{\epsilon_{\text{AlGa}N}}{\epsilon_{\text{Ga}N}}\right) t_{\text{cap}} & d \leq t_{\text{ox}} + t_{\text{cap}} + t_{\text{bar}} \\ \frac{\epsilon_{\text{Ga}N} \epsilon_0 A}{C(V_g)} + \left(1 - \frac{\epsilon_{\text{Ga}N}}{\epsilon_{\text{ox}}}\right) t_{\text{ox}} + \left(1 - \frac{\epsilon_{\text{Ga}N}}{\epsilon_{\text{AlGa}N}}\right) t_{\text{bar}} & d > t_{\text{ox}} + t_{\text{cap}} + t_{\text{bar}} \end{cases}$$

where t_{ox} , t_{cap} , t_{bar} are the thickness of Al₂O₃ gate insulator, GaN cap layer, AlGa_{0.3}N barrier layer respectively; $\epsilon_{\text{AlGa}N}=9.3$, $\epsilon_{\text{Ga}N}=9.5$; $C(V_g)$ is the overall capacitance as a function of gate bias. The capacitance of the ultrathin AlN space was neglected. For conventional AlGa_{0.3}N/GaN heterostructure, similar equations with $t_{\text{ox}}=0$ were employed. The N_a - d curves are shown in Fig. 7.3. The distance between the two peaks agrees well on the Al₂O₃ film thickness measured by the ellipsometer (10 nm). The inset of Fig. 7.3 shows the zoomed-in N_a shapes at the two peaks. It can be seen that the electron distribution inside the triangle quantum well in Al₂O₃/AlGa_{0.3}N/GaN MIS-heterostructure is slightly different from the conventional AlGa_{0.3}N/GaN heterostructure and spreads towards the AlGa_{0.3}N barrier, which possibly results from the surface passivation effect of the Al₂O₃ dielectric. The Al₂O₃ gate insulator reduces the surface states at the interface between the dielectric and top GaN layer (shown in Fig. 7.1) and suppresses its depletion of the electrons inside the channel.

Fig. 7.3 Extracted apparent electron concentration N_a as a function of depth d . The inset shows the zoomed-in regions at the two peaks.

The FATHEMT technique was utilized to measure the drift mobility of the 2DEG in MISHEMT and conventional HEMT. The FATHEMT patterns were designed to have much shorter source-to-gate distance L_{sg} and drain-to-gate distance L_{dg} of 3 μm compared to the wide gate length (L) of 150 μm , so as to reduce the influence of the access resistance on the mobility calculation. The width of the gate (W) was 50 μm . The DC transfer (I_d - V_g) and C-V characteristics were measured and the drift mobility μ_d was calculated from:

$$\mu_d = \frac{L}{W} \frac{I_d}{V_d Q_i} \quad (7.6)$$

$$\text{and } Q_i(V_g) = \int_{V_{th}}^{V_g} C_g(V_g) dV_g \quad (7.7)$$

During the measurement V_d was fixed at 1 V to ensure that the device was working in linear region and the electrons traveled across the channel with a

uniform mobility. Fig. 7.4 shows the measured μ_d versus n_s in MISHEMT and conventional HEMT. It was found that the GaN MISHEMT with Al₂O₃ gate insulator has a higher electron drift mobility compared with the conventional HEMT. At $n_s=8 \times 10^{12} \text{ cm}^{-2}$, the electron drift mobility in 2DEG increases from $1500 \text{ cm}^2/\text{Vs}$ in conventional AlGaIn/GaN HEMT to $1670 \text{ cm}^2/\text{Vs}$ in Al₂O₃/AlGaIn/GaN MISHEMT. The peak drift mobility of Al₂O₃ MISHEMT is high up to $1780 \text{ cm}^2/\text{Vs}$, which is 19% larger than that of $1500 \text{ cm}^2/\text{Vs}$ for conventional HEMT structure. The main characteristics of the Al₂O₃/AlGaIn/GaN MIS structure and AlGaIn/GaN structure are listed in Table 7.1. The increased mobility has ever been observed in the AlGaIn/GaN MISHEMT using Al₂O₃ grown by MOCVD [157], but has not been reported for the Al₂O₃ grown by ALD. The channel mobility increase can be explained by the reduction of remote Coulomb scattering of the 2DEG electrons due to the reduced trapped charge at the interface between the dielectric and top GaN layer. Such surface passivation effect has been reported by T. Hashizume et al. [47]. We have also confirmed this passivation effect by pulsed DC measurement for a conventional HEMT with 10 nm ALD Al₂O₃ as surface passivation. After passivation, the drain current and transconductance droops under gate quiescent voltage $V_{gq} < V_{th}$ and drain quiescent voltage $V_{dq}=0$ compared to those values under $V_{gq}=0$ and $V_{dq}=0$ have obviously been suppressed. This indicates the reduction of the surface trap density in the gate-source region and gate-drain region due to the Al₂O₃ passivation [169].

The reduced remote scattering center density can be estimated to be around $8 \times 10^{11} \text{ cm}^{-2}$ at $n_s=8 \times 10^{12} \text{ cm}^{-2}$ using [170]

$$\Delta n_d = A n_s^{1.5} \left(\frac{1}{\mu_{MOSHEMT}} - \frac{1}{\mu_{HEMT}} \right) \quad (7.8)$$

where the coefficient A is calculated using the GaN material parameters listed in [171] and the structure dimensions of this work.

Fig. 7.4 Drift mobility μ_d versus n_s in ALD-Al₂O₃/AlGa_N/Ga_N MISHEMT and conventional AlGa_N/Ga_N HEMT.

The DC dynamic characterization can reduce the influence of surface states and the self-heating effect, thus can be utilized to accurately investigate and compare the transport characteristics of the 2DEG between the ALD-Al₂O₃/AlGa_N/Ga_N MISHEMTs and conventional AlGa_N/Ga_N HEMT. During the measurement, the width of the pulse was set to 200 ns and the duty cycle was set to 0.02%. The quiescent biases for the gate and drain were both set to 0 V. Fig. 7.5 shows the dynamic DC output characteristics of the Al₂O₃ MISHEMT and conventional HEMT (with gate length $L_g=1 \text{ }\mu\text{m}$ and gate width $W_g=2\times 100 \text{ }\mu\text{m}$). The relatively high ohmic contact resistances ($R_c \sim 0.8 \text{ }\Omega\cdot\text{mm}$) for the conventional

Fig. 7.5 Dynamic drain current of the ALD-Al₂O₃/AlGaN/GaN MISHEMT and the conventional AlGaN/GaN HEMT.

HEMT and MISHEMT lead to a small difference between their output resistance values at the linear region. Compared with the conventional HEMT, the saturation drain current $I_{d,sat}$ of the MISHEMT at $V_g = 0$ V increased by 36% (from 655 mA/mm to 890 mA/mm) and the calculated electron velocity v_{sat} increased by 59% ($I_{d,sat} \approx qWn_s v_{sat}$). Due to the reduced gate leakage current, much higher gate bias can be applied for the Al₂O₃ MISHEMT than the conventional HEMT. If $I_g = 1$ mA/mm is taken as the upper limit of the positive gate bias, the highest V_g can be set to +5 V for Al₂O₃ MISHEMT while it can only be +1 V for the conventional HEMT. Thus the available $I_{d,max}$ of MISHEMT can be as high as 1.3 A/mm (at $V_g = +5$ V), which is 55% higher than the 840 mA/mm obtained for conventional HEMT (at $V_g = +1$ V).

Table 7.1 Typical characteristics of the ALD-Al₂O₃/AlGa_{0.3}N/GaN MISHEMT and conventional AlGa_{0.3}N/GaN HEMT on high-resistivity Si.

Parameter	Conventional AlGa _{0.3} N/GaN HEMT	ALD-Al ₂ O ₃ AlGa _{0.3} N/GaN MISHEMT
R_{sh} ($\Omega/\square$)	390	355
C_g (pF) ($V_g = 0$ V)	264	180
n_s (10^{12} cm ⁻²) (at $V_g=0$)	8.4	7.2
μ_d (cm ² /Vs) (at $n_s=8 \times 10^{12}$ cm ⁻²)	1500	1670
$\mu_{d,max}$ (cm ² /Vs)	1500	1780
$I_{d,dy}$ (mA/mm)(at $V_g=0$)	655	890
v_{sat} (10^6 cm/s)(at $V_g=0$)	4.9	7.8

7.3 Demonstration of 0.25- μ m gate-length ALD

Al₂O₃/AlGa_{0.3}N/GaN MISHEMTs on Si with Excellent Microwave and Noise Performance

In this section the structure of the GaN MISHEMT is shown as Fig. 7.6. Hall measurement shows a 2DEG sheet carrier density of 0.7×10^{13} cm⁻² and electron mobility of 1300 cm²/Vs at 300K for the AlGa_{0.3}N/GaN heterostructure. The fabrication processes were the same as those described in Chapter 2.

The C-V and I-V characteristics of the diodes were measured using an Agilent B1500A semiconductor parameter analyzer. The DC characteristics of the MISHEMTs were measured using a HP 4142 semiconductor parameter analyzer. The microwave small signal (from 6 to 40 GHz) and noise (from 2 to 20 GHz) measurements were carried out using HP 8510C vector network analyzer (VNA), HP 8970B noise figure meter and ATN NP5 noise test set.

Fig. 7.6 Schematic diagram of the AlGaN/GaN MISHEMT with ALD-Al₂O₃ as gate insulator on high-resistivity Si (111) substrate.

For MISHEMT an 8-nm Al₂O₃ film was deposited at 300 °C as the gate insulator using an Oxford Instrument OpAL ALD system. The dimensions of the measured devices are: gate length $L_g=0.25\ \mu\text{m}$, gate width $W_g=2\times 100\ \mu\text{m}$, gate-to-source distance $L_{gs}\sim 0.9\ \mu\text{m}$, and gate-to-drain distance $L_{gd}\sim 3.9\ \mu\text{m}$.

The DC, microwave small signal and noise performance were measured over a wide range of drain currents at a fixed drain voltage for both the MISHEMT and conventional HEMT. In this work, to quantitatively compare the linearity performance for various parameters of the MISHEMT and conventional HEMT, we adopt the figure-of-merits namely Drain voltage Swing (DCS) and Gate Voltage Swing (GVS) which are defined as the range of the drain current and range of gate voltage respectively where the device parameter remains $\geq 80\%$ of its maximum value or $\leq 120\%$ of its minimum value.

Fig. 7.7 shows the typical (a) C-V and (b) I-V characteristics of the Al₂O₃/AlGaN/GaN MIS diode and conventional AlGaN/GaN Schottky diode

Fig. 7.7 (a) $C-V$ and (b) $I-V$ characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS diode and conventional AlGaIn/GaN Schottky diode on high-resistivity Si substrate. The diode diameter is 50 μm .

fabricated on the same wafer as the MISHEMTs. The C-V curves were measured at 1 MHz. The C-V curve of the MIS diode shows a sharp transition from deep depletion to accumulation, which verifies the good quality of the ALD-Al₂O₃ dielectric and the low trap density at the interface between the Al₂O₃ and III-Nitride semiconductor. The threshold voltage shift $\Delta V_{th} = -0.67$ V of the MIS diode compared with the conventional Schottky diode is consistent with the estimation from the n_s values and the barrier/oxide capacitances. It can be seen from Fig. 7.7 (b) that the Al₂O₃ gate insulator greatly reduces the gate leakage current at both positive and negative biases by more than 4 orders of magnitude. The lower gate leakage current at positive bias for Al₂O₃/AlGaIn/GaN MIS structure enables the gate to be biased at up to +4 V whereas for conventional AlGaIn/GaN heterostructure, the gate can only be biased at < +1 V.

The DC output and transfer characteristics of the Al₂O₃/AlGaIn/GaN MISHEMT are plotted in Fig. 7.8 (a) and (b). The device has gate-to-source distance (L_{gs}) of 0.9 μm , gate-to drain distance (L_{gd}) of 3.9 μm and gate width (W_g) of 2x100 μm . High maximum drain current (I_{dmax}) of around 1.0 A/mm is achieved at $V_g = +4$ V. At $V_d = 6$ V, the device has a maximum extrinsic transconductance (g_{mmax}) of 180 mS/mm. This is lower as compared to the typical value of ~250 mS/mm in the conventional AlGaIn/GaN HEMT as a result of the increased gate-to-channel distance. The device shows a threshold voltage shift under high drain bias ($> \sim 10$ V) and kinks in the I-V curves. This is believed to be due to the existence of buffer traps, which can be improved by further optimization of the buffer quality [107].

Fig. 7.8 DC (a) output and (b) transfer characteristics of the Al₂O₃/AlGaN/GaN MISHEMT on high-resistivity Si substrate. The device is with $L_{gs}=0.9$ μm , $L_g=0.25$ μm , $L_{gd}=3.9$ μm and $W_g=2 \times 100$ μm .

Fig. 7.9 shows the small signal gain versus frequency for the Al₂O₃ MISHEMT with $L_{gs}=0.9\ \mu\text{m}$, $L_{gd}=2.9\ \mu\text{m}$ and $W_g=2\times 50\ \mu\text{m}$ at $V_g=-2.0\ \text{V}$ and $V_d=6\ \text{V}$. High current gain cutoff frequency f_T up to 43 GHz was extrapolated from the $|H_{21}|$ curve. The maximum oscillation frequencies f_{max} of 76 GHz and 98 GHz were extrapolated from the unilateral power gain (G_u) and the maximum available gain / maximum stable gain (MAG/MSG) at -20 dB/dec respectively.

Fig. 7.9 Small signal characteristics of the Al₂O₃/AlGaIn/GaN MISHEMT. The device is with dimensions of $L_{sg}=0.9\ \mu\text{m}$, $L_{gd}=2.9\ \mu\text{m}$, $W_g=2\times 50\ \mu\text{m}$ and biased at $V_d=6\ \text{V}$, $V_g=-2\ \text{V}$.

Fig. 7.10 shows the values of current-gain cutoff frequency (f_T) as a function of various gate and drain biases for (a) Al₂O₃ MISHEMT and (b) conventional HEMT with $L_{gs}=0.9\ \mu\text{m}$, $L_{gd}=2.9\ \mu\text{m}$ and $W_g=2\times 50\ \mu\text{m}$. It can be clearly seen from the figure that a larger bias window is obtained for the MISHEMT to maintain high f_T values, for example, $>35\ \text{GHz}$, than the conventional HEMT.

Fig. 7.10 Values of f_T as a function of various gate and drain biases for (a) Al₂O₃ MISHEMT and (b) conventional HEMT.

Fig. 7.11 shows the minimum noise figure ($NF_{\min}$), associate gain (G_a) and noise equivalent resistance (R_n) of the Al₂O₃/AlGaIn/GaN MISHEMT with $L_{gs}=0.9$ μm , $L_{gd}=3.9$ μm and $W_g=2\times 100$ μm . At 10GHz, a low $NF_{\min}$ of 1.0 dB together with high G_a of 10.5 dB and low R_n of 29.2 Ω were obtained at $V_d=6$ V and $I_d=300$ mA/mm. The noise performance of our 0.25 μm MISHEMT at 10 GHz is comparable with the reported state-of-the-art conventional 0.25 μm GaN HEMTs on SiC substrate (~ 0.8 dB) [172] and on sapphire substrate (~ 1.0 dB) [127]. At 20 GHz, the device shows the $NF_{\min}$ of 2.1 dB, G_a of 7.5 dB and R_n of 23.8 Ω , which are comparable to the reported results of conventional GaN HEMT on Si with 0.17 μm gate length [173]. The excellent noise performance in our MISHEMT is believed to benefit from the low gate leakage current due to the Al₂O₃ gate insulator [49].

Fig. 7.11 Microwave noise characteristics of the Al₂O₃/AlGaIn/GaN MISHEMT on high-resistivity Si substrate. The device is with dimensions of $L_{gs}=0.9$ μm , $L_g=0.25$ μm , $L_{gd}=3.9$ μm , $W_g=2\times 100$ μm and biased at $V_d=6$ V and $I_d=300$ mA/mm.

For a microwave noise transistor, the noise figure (NF) at a certain source termination reflection coefficient (Γ_{in}) is dependent on all the three parameters: NF_{min} , R_n and Γ_{opt} according to the following expression [174]:

$$NF = NF_{min} + 4 \frac{R_n}{50} \frac{|\Gamma_{in} - \Gamma_{opt}|}{|1 + \Gamma_{opt}|^2 (1 - |\Gamma_{in}|^2)} \quad (7.9)$$

Based on the above expression, the noise circles for the Al₂O₃ MISHEMT and the conventional HEMT are plotted in Fig. 7.12. It can be seen that GaN MISHEMT has less sensitivity to the deviation of the source termination reflection coefficient from its optimal values, which can enhance its feasibility for low noise applications.

7.4 Improved Linearity for Low Noise Applications in ALD

Al₂O₃/AlGaN/GaN MISHEMTs

The device structure measured in this section is same as that in the last section (as shown in Fig. 7.6). The typical DC transfer characteristics for the Al₂O₃/AlGaN/GaN MISHEMT and conventional AlGaN/GaN HEMT on high-resistivity silicon are plotted in Fig. 7.13. The drain current (I_d) is higher for the MISHEMT compared with the conventional HEMT. At the same biases with $V_d=6$ V and $V_g=+1$ V, the I_d for the MISHEMT is as high as 900 mA/mm, which is ~29% higher than the 700 mA/mm for the conventional HEMT. The increase in the output current is due to the improved 2DEG transport characteristics by the passivation effect of the ALD Al₂O₃ thin film [175].

Fig. 7.12 Noise circles of the Al₂O₃/AlGaIn/GaN MISHEMT and conventional HEMT on high-resistivity Si substrate.

Fig. 7.13 Typical transfer characteristics as a function of drain current at $V_d=6$ V in the ALD Al₂O₃/AlGaN/GaN MISHEMT and the conventional AlGaN/GaN HEMT on high-resistivity Si substrate.

It was observed that DCS for g_m in the MISHEMT is clearly wider than that in the conventional HEMT. The DCS is about 540 mA/mm for the MISHEMT which is 26% higher than the 430 mA/mm for the conventional HEMT. The corresponding GVS is 3.2 V for the MISHEMT versus 1.8 V for the conventional HEMT.

Fig. 7.14 shows the small-signal current-gain cutoff frequency (f_T) as a function of drain current measured for the ALD Al₂O₃ MISHEMT and conventional HEMT. The DCS for f_T in the MISHEMT is 480 mA/mm which is 52% higher than the 315 mA/mm for the conventional HEMT. The corresponding GVS of the MISHEMT shows a value of 3.7 V (from -5.4 to -1.7 V), nearly 3 times of the 1.3 V (from -2.5 to -1.2 V) for the conventional HEMT. The improved linearity

for f_T in MISHEMT is believed to be associated with the higher-linearity for both g_m and gate-source capacitance C_{gs} .

Fig. 7.14 Current-gain cut-off frequency (f_T) as a function of drain current in the ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISHEMT and conventional $\text{AlGaIn}/\text{GaIn}$ HEMT on high-resistivity Si substrate.

The minimum noise figure ($NF_{\min}$) of a HEMT can be expressed as: [122]

$$NF_{\min} = 1 + 2 \frac{f}{f_T} \sqrt{K_g \left(K_r + g_m (R_s + R_g) \right)} \quad (7.10)$$

where K_g and K_r are two parameters associated with the internal noise sources; R_s and R_g are the gate and source access resistances. It can be seen that the microwave noise characteristics are greatly dependent on the f_T and g_m , thus the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISHEMT with high-linearity f_T and g_m can be expected to have a high-linearity noise performance. Actually at all the measured frequency points (2-20 GHz) the MISHEMT was found to have a wider bias range for low $NF_{\min}$ compared with the conventional HEMT. The values of $NF_{\min}$ at 10 GHz versus drain current in the ALD Al_2O_3 $\text{AlGaIn}/\text{GaIn}$ MISHEMT and conventional

AlGa_N/Ga_N HEMT are plotted in Fig. 7.15. From the values of $NF_{\min}$ (a.u.), it can be seen that the MISHEMT has a DCS of 540 mA/mm, which is $\sim 23\%$ higher than the 430 mA/mm in the conventional HEMT. The corresponding GVS in the MISHEMT and conventional HEMT are 3.8 V (from -5.5 to -1.7 V) and 1.6 V (from -2.5 to -0.9 V) respectively.

Fig. 7.15 Minimum noise figure ($NF_{\min}$) at 10 GHz as a function of drain current in the ALD Al_2O_3 /AlGa_N/Ga_N MISHEMT and conventional AlGa_N/Ga_N HEMT on high-resistivity Si substrate.

The increased noise linearity performance in the MISHEMT can be ascribed to two facts related to the Al_2O_3 gate insulator. One is that the MISHEMT structure suppresses the 2DEG electron spillover into the AlGa_N barrier, so that suppresses the mobility drop at high gate voltage in conventional HEMT [176]. The other is that the gate insulator reduces the gate shot noise induced by the gate leakage current [49].

Fig. 7.16 plots the associated gain (G_a) at 10 GHz for the ALD Al_2O_3 AlGa_N/Ga_N MISHEMT and the conventional AlGa_N/Ga_N HEMT. The DCS /

GVS for G_a at 10 GHz in MISHEMT was found to be 600 mA/mm/4.2 V (from -5.5 to -1.3 V), whereas it was only 400 mA/mm /1.6 V (from -2.5 to -0.9 V) for the conventional HEMT. The MISHEMT also has a wider bias range for high G_a over the whole measured frequency range (2-20 GHz).

Fig. 7.16 Associated gain (G_a) at $V_d=6$ V and $f=10$ GHz as a function of drain current in the ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISHEMT and conventional $\text{AlGaIn}/\text{GaIn}$ HEMT on high-resistivity Si substrate.

Equivalent noise resistance (R_n) is another important parameter for low noise amplifier design since it reflects the sensitivity of the noise figure (NF) to the departure of the input termination reflection coefficient (Γ_{in}) from the optimal value (Γ_{opt}), as the Eqn. (7.9) shows.

Fig. 7.17 shows the values of R_n versus drain current at 10 GHz for the ALD Al_2O_3 $\text{AlGaIn}/\text{GaIn}$ MISHEMT and the conventional $\text{AlGaIn}/\text{GaIn}$ HEMT. The DCS for R_n is 340 mA/mm in the MISHEMT and 26% higher than the value of 270 mA/mm in the conventional HEMT. The corresponding GVS values are 2.4 V

(from -4.2 to -1.8 V) and 1.2 V (from -2.4 to -1.2 V) for the MISHEMT and conventional HEMT respectively. The wider DCS for R_n in the MISHEMT can enhance the feasibility of matching circuit design at a wider bias range for LNA applications.

Fig. 7.17 Equivalent noise resistance R_n as a function of drain current at $V_d=6$ V in the ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISHEMT and conventional $\text{AlGaIn}/\text{GaIn}$ HEMT on high-resistivity Si substrate.

Measurement of two-tone intermodulation characteristics was carried out at $V_{ds}=6$ V, $I_{ds}=300$ mA/mm and $f=10$ GHz with an offset frequency of 10 MHz and $Z_{in}, Z_{out}=50$ Ω for both of the MISHEMT and conventional HEMT. The bias condition was selected to be consistent with that for previous low-noise measurement. Fig. 7.18 shows the measured third order intermodulation (IM3) and carrier to IM3 ratio (C/IM3) versus the output power at linear region. At output power of -3 dBm, the MISHEMT shows a C/IM3 value of -54 dBc, which is about 5 dB lower than that of the conventional HEMT. The output third-order intercept (OIP3) value for the MISHEMT is 23 dBm, which is 3 dB larger than that of 20

dBm for the conventional HEMT. These values are comparable to the reports for GaN HEMTs at similar biases [163, 164]. The increased IP₃ values clearly demonstrated the improvement of linearity in ALD Al₂O₃ AlGa_{0.5}N/GaN MISHEMT compared with the AlGa_{0.5}N/GaN conventional HEMT. It is to be noted that the impedance matching conditions for the conventional HEMT and MISHEMT are different. At $Z_{out}=50\ \Omega$, the conventional HEMT is better matched than the MISHEMT. As a result, it can be expected that for MISHEMT under optimal load matching conditions, it will give rise to better linearity than the conventional HEMT.

Fig. 7.18 Intermodulation characteristics at 10 GHz for the ALD Al₂O₃/AlGa_{0.5}N/GaN MISHEMT and conventional AlGa_{0.5}N/GaN HEMT on Si substrate. Both devices were biased at $V_d=6$ V and $I_d=300$ mA/mm.

7.5 Conclusion

In summary, conclusions can be drawn and divided into three catalogues:

(1) The characteristics of 2DEG were investigated in the Al₂O₃/AlGa_{0.3}N/GaN MISHEMT with ALD-Al₂O₃ as gate insulator on a high-resistivity Si substrate. Slight change of the electron lateral distribution in the channel was observed in the MISHEMTs. The sheet resistance R_{sh} of the Al₂O₃/AlGa_{0.3}N/GaN heterostructure is smaller than that of the conventional AlGa_{0.3}N/GaN heterostructure. The electron drift mobility μ_d of the Al₂O₃/AlGa_{0.3}N/GaN MISHEMTs is increased because of the passivation effect of the inserted Al₂O₃ thin layer. Due to the higher 2DEG saturation velocity v_{sat} and the allowed higher positive gate voltage, a 55% higher dynamic drain current can be obtained for the Al₂O₃/AlGa_{0.3}N/GaN MISHEMTs. The improved transport properties in the ALD-Al₂O₃/AlGa_{0.3}N/GaN MISHEMT are promising for the development of high power devices.

(2) We have demonstrated a 0.25- μ m gate-length AlGa_{0.3}N/GaN MISHEMT on high-resistivity Si substrate using ALD-Al₂O₃ as gate insulator with excellent microwave and noise performance. High f_T of 43 GHz and f_{max} of 76 GHz were achieved. Low NF_{min} of 1.0 dB together with high G_a of 10.5 dB and low R_n of 29.2 Ω were measured at 10 GHz benefitting from the low gate leakage current. These results are comparable to the reported conventional AlGa_{0.3}N/GaN HEMT on high-resistivity Si with the same or even shorter gate length, and thus demonstrate the good potential of ALD-Al₂O₃/AlGa_{0.3}N/GaN MISHEMT for microwave low noise applications.

(3) Improved linearity for low noise applications is demonstrated in a 0.25- μ m AlGa_{0.3}N/GaN MISHEMT on high-resistivity silicon substrate using ALD Al₂O₃ as gate insulator. Compared to the conventional AlGa_{0.3}N/GaN HEMT, the ALD

Al₂O₃/AlGaIn/GaN MISHEMT has a wider gate-voltage swing and drain-current swing for g_m , f_T and all the three noise parameters $NF_{\min}$, G_a and R_n . Higher IP3 value was obtained for the MISHEMT from the two-tone intermodulation measurement. These results show the great potential of the ALD Al₂O₃/AlGaIn/GaN MISHEMTs for high linearity GaN MMIC LNAs.

Chapter 8

Conclusions and Recommendations for Future Work

8.1 Conclusions

In this work, low-noise AlGaIn/GaN HEMTs and ALD Al₂O₃/AlGaIn/GaN MISHEMTs on high-resistivity Si substrate have been successfully developed and demonstrated excellent performance. $NF_{\min}$ of 1.0 dB at 10 GHz was achieved for the 0.25 μm gate-length ALD Al₂O₃ AlGaIn/GaN MISHEMT on Si, while that of 1.2 dB was achieved in the conventional GaN HEMTs with same gate-length Schottky metal gate. The fabrication process and characterization techniques, together with a full procedure to determine the microwave small-signal ECPs and noise sources were developed.

Some critical issues related to the optimization of the device structure and fabrication processes and to the applications at elevated temperatures have been studied in details. The main achievements in this work are summarized as below:

(1) The electron transport properties in the ohmic contact of AlGaIn/GaN HEMTs have been studied by the temperature dependent ohmic contact characterization over a temperature range of -50 °C to 200 °C. The Ti/Al/Ni/Au ohmic contact in AlGaIn/GaN HEMTs exhibited increase of R_{sh} , decrease of ρ_c and non-monotone behavior of R_c over temperature. Electron TFE from the modified AlGaIn region with high-density N-vacancies to the 2DEG was found to be the dominant transport mechanism in the AlGaIn/GaN heterostructures' ohmic contact.

(2) The three-terminal off-state breakdown mechanisms in AlGaIn/GaN HEMTs on Si substrate were comprehensively investigated by means of the

temperature dependent DCI and side-gate techniques. As for the channel breakdown voltage, negative temperature coefficient was found for both two different samples; whereas for the gate-drain breakdown, positive and negative temperature coefficients were found for two samples separately. Through the analysis on the behavior of the gate current at high and low temperatures with varying gate drain field, the physical mechanisms related to the different breakdown behaviors were determined.

(3) The effects of PECVD SiN surface passivation on DC, bias-dependent microwave small signal and noise characteristics were comprehensively studied for AlGaIn/GaN HEMTs on Si substrate. The SiN surface passivation was also found to improve the microwave and noise parameters including f_T , f_{max} , NF_{min} , R_n and increased G_a etc. over the entire bias range carried out in this work. The bias dependent small signal ECPs were extracted before and after passivation and the influence of the SiN surface passivation on the bias dependence of the various ECPs were comprehensively studied. The improved microwave noise performance is determined to be mainly due to the increase of intrinsic g_m , which is due to the increase of channel electron mobility by the suppression of surface trappint effects. The channel noise was observed to have increased after surface passivation, which is believed to result from the lateral electrical field profile modification by the reduction of surface charge.

(4) Temperature dependent microwave noise characteristics of AlGaIn/GaN HEMT on Si were investigated over a wide temperature range from -50 to 200 °C. The physical mechanisms of the thermal behavior of the microwave noise are discussed. The degradation rates of the noise parameters and internal noise source coefficients were comparable to those reported GaN HEMTs on SiC and sapphire

substrates and also comparable to the GaAs and InP low noise HEMTs. This indicates the excellent potential of the GaN HEMT on Si for low noise application at high temperature. Analytical modeling was carried out for the high-frequency noise including temperature effects in AlGaIn/GaN high electron mobility transistors (HEMTs) on high-resistivity Si substrate over a wide temperature range from -50 to 200 °C. The feedback capacitance C_{gd} was found to be important to accurately simulate all the measured noise parameters over temperature. Frequency dependent R and C are needed to be included, considering the effect of the gate leakage current, to accurately simulate the noise at high temperature and low frequency regions.

(5) The characteristics of 2DEG were investigated in the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISHEMTs with ALD- Al_2O_3 as gate insulator on high-resistivity Si substrate. The electron drift mobility μ_d and saturation velocity v_{sat} of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS heterostructure have increased because of the passivation effect of the inserted Al_2O_3 thin layer.

(6) We have also demonstrated for the first time a 0.25- μm gate-length ALD- $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISHEMT on high-resistivity silicon substrate with excellent microwave small signal and noise performance at X-band. f_T of 40 GHz, f_{max} of 76 GHz and NF_{min} of 1.0 dB, G_a of 10.5 dB, R_n of 29.2 Ω at 10 GHz were achieved. The device exhibits improved noise performance compared to the conventional Schottky gate HEMT. The DC transconductance, microwave small signal and noise performance of the MISHEMT have less dependence on the drain current as compared to conventional Schottky-gate AlGaIn/GaN HEMT. The improved device linearity shows that the ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISHEMT on high-resistivity silicon substrate is promising for high-linearity LNA applications.

8.2 Recommendations for Future Work

Although the excellent noise performance at the X-band has been achieved in the conventional Schottky gate GaN HEMTs and further improved by the ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ HEMT on high-resistivity silicon substrate, there is still much room for improvement. The device performance can be expected to be further improved considering the following aspects.

(1) The ohmic contact resistance is still relatively high for the GaN HEMTs in this work. The microwave and noise performance can be significantly improved by lowering the ohmic contact resistance through optimization of the process recipes, such as surface treatment, metal scheme and annealing temperature etc. Plasma treatment before metal deposition [177] and ohmic recess technique [178, 179], that is, thinning the barrier through plasma etch, are promising methods to reduce the high contact resistance brought by the AlN insertion as the spacer layer.

(2) More optimization is needed to further improve the quality of the ALD Al_2O_3 , such as lower fixed charge density and lower interface state density. Additional surface treatment, including plasma treatment, can be included and optimized before deposition.

(3) The access resistances can be further reduced by adopting self aligned gate (SAG) technique [180]. For SAG, a key point is how to realize compatible gate-first fabrication process. There are two ways to realize this, one is trying to lower the annealing temperature of the ohmic metal to around 500 °C by selecting a compatible metal scheme; the other is to increase the reliability of the gate metal during high temperature annealing around 850 °C, such as adopting gate metals with high reliability like W, Mo etc, or adopting MIS structure. Another issue to be

resolved for SAG is the optimization of the T-shape or Γ -shape gate to reduce the associated parasitic coupling capacitances, and to increase the breakdown voltage.

(4) A gate recess MISHEMT has been demonstrated [181]. Short gate-to-channel distance is needed to reduce the short channel effect when the gate-length is further scaled down for high frequency performance. The depth of the recess and the thickness of gate insulator are needed to be optimized to realize the trade-off of high transconductance and low leakage current and therefore to realize the best noise performance.

List of Publications

Journal Papers:

- 1 Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, and H. Zhou, "Temperature-dependent forward gate current transport in atomic-layer-deposited $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ metal-insulator-semiconductor high electron mobility transistor," *Applied Physics Letters*, vol. 98, no. 16, pp. 163501-1-163501-3, Apr. 2011.
- 2 Z. H. Liu, G. I. Ng, H. Zhou, S. Arulkumaran, and Y. K. T. Maung, "Reduced surface leakage current and trapping effects in $\text{AlGaIn}/\text{GaIn}$ high electron mobility transistors on silicon with $\text{SiN}/\text{Al}_2\text{O}_3$ passivation," *Applied Physics Letters*, vol. 98, no. 11, pp. 113506-1-113506-3, Mar. 2011.
- 3 Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and S. Vicknesh, "Temperature dependent microwave noise characteristics in ALD $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISHEMTs on silicon substrate," *IEEE Electron Device Letter*, vol. 32, no. 3, pp. 318-320, Mar. 2011.
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