CMOS VLSI subsystems for low-voltage low-power applications

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**CMOS VLSI Subsystems
For
Low-Voltage Low-Power Applications**

Kong Zhi Hui

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

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Summary

Low-voltage and low-power circuit design has become vitally indispensable with the emergence and increasing popularity of off-the-shelf handheld electronic devices. Indeed, portable appliances are stimulating and dominating the System-on-a-Chip (SoC) mass consumer market at a tremendously high pace. As a result, it is essential to continue venturing into higher-end approaches and realizing more refined solutions to achieve further low-voltage/low-power design while sustaining high-speed performance and small-area consumption. In this dissertation, we present several innovative CMOS VLSI subsystem designs for use in low-voltage low-power environments.

We introduce a new design of a high-performance adder based on the conventional square root Carry-Select Adder (CSL) scheme and a modified add-one circuit. It is a plausible evolution of its existing counterparts in the sense that it successfully addresses and eradicates the weak point of the antecedent add-one CSL circuits. Extensive simulation results using the 1.8 V/0.18 μm CMOS process from Chartered Semiconductor Manufacturing Pte. Ltd. (CHRT) have verified that the new adder architecture improved significantly in terms of computation speed and power consumption while promising an attractive small-area footprint. This is achieved by legitimate and appropriate usage of logic structure and circuit technique.

An area-efficient current-mode comparator, which is based on the conventional CMOS current comparator, is proposed to meet the increasing requirement for customized circuits that suit varying operating environments and specifications. Extensive circuit simulations using the 0.25 μm , 0.18 μm , and 0.13 μm CMOS technology from CHRT verify that the proposed design acts as an ideal complement to the conventional current comparator while operating at low threshold current (I_{th}) levels. A low I_{th} is generally more favorable than a higher I_{th} as it often translates to lower static power dissipation. A more encouraging and promising fact is that the area advantage becomes more pronounced when the feature size/technology is scaled. This attribute blends well with today's further minimization of the minimum feature size. To confirm its performance feasibility, the proposed current comparator has been integrated into a Positive-Digit Adder (PDA) using the Current-Mode Multiple-Valued Logic (CMMVL)

approach with 1.8 V/0.18 μm CMOS technology. The PDA utilizing the new current comparator exhibits a significantly smaller silicon area than those of the conventional and contemporary circuits, while offering apparent power-delay product improvement.

In addition, as for the memory subsystem, a low-voltage low-power current conveyor amplifier for high-speed SRAM implementations is presented. Simulation results showed that the new circuit offers substantial improvement over the conventional circuit with respect to speed and power-delay product, regardless of the variations in bit-line and data-line capacitances.

A high-performance current sense amplifier employing a cross-coupled current-mirror configuration is also presented. The circuit is designed for low-voltage low-power SRAM applications. Its sensing speed is independent of the bit-line capacitances and is also insensitive to the data-line capacitances. Simulation results have shown that the new sense amplifier gives performance leverage over the conventional sense amplifier circuits with respect to speed and power.

Another competitive current sense amplifier, namely the micro-power current sense amplifier employing a cross-coupled current-mirror configuration, is introduced. Similar to the previous designs, this circuit is designed for low-voltage low-power SRAM applications. Its sensing speed is independent of the bit-line capacitances and is almost insensitive to the data-line capacitances. Extensive simulation results based on a 1.8 V/0.18 μm CMOS technology from CHRT verifies that the new sense amplifier promises a much sought-after power-efficient advantage and note-worthy power-delay product superiority over the conventional and recently reported sense amplifier circuits. These attributes of the proposed sense amplifier make it especially appropriate for use in the contemporary high-complexity SoC, which requires low-power characteristics.

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List of Abbreviations

ADP	Area-Delay Product
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
ASIC	Application-Specific Integrated Circuit
BL	Bit-Line
CC	Current Comparator
CHRT	Chartered Semiconductor Manufacturing Pte. Ltd.
CM	Current-Mode
CMi	Current Mirror
CMMVL	Current-Mode Multiple-Valued Logic
CMOS	Complementary Metal Oxide Semiconductor
CLA	Carry Lookahead Adder
CLG	Carry Generator Block
COS	Conditional Sum Adder
CPA	Carry Propagate Adder
CPL	Complementary Pass-transistor Logic
CPU	Central Processing Unit
CS	Column-Select
CSA	Carry Save Adder
CSL	Carry Select Adder
CSK	Carry Skip Adder
DL	Data-Line
DRAM	Dynamic Random-Access Memory
DSP	Digital Signal Processing
FA	Full Adder
GSI	Giga Scale Integration
HA	Half Adder
IC	Integrated Circuit
IP	Intellectual Property
IT	Information Technology
ITRS	International Technology Roadmap for Semiconductors
LSB	Least Significant Bit
MC	Memory Cell
MCC	Manchester Carry Chain
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MPU	Microprocessor
MSB	Most Significant Bit
MVL	Multiple-Valued Logic
MUX	Multiplexer
nMOS	n-channel Metal Oxide Semiconductor
PC	Personal Computer
PD	Positive-Digit

PDA	Positive-Digit Adder
PDN	Pull-Down Network
PDP	Power-Delay Product
PE	Processing Element
PDA	Positive-Digit Adder
pMOS	p-channel Metal Oxide Semiconductor
PUN	Pull-Up Network
RAM	Random-Access Memory
RCA	Ripple Carry Adder
ROM	Read-Only Memory
RS	Row-Select
R/W	Read/Write
SDDA	Single-Digit Decimal Adder
SG	Sum Generator
SoC	System-on-a-Chip
SRAM	Static Random-Access Memory
TFA	Transmission Function Adder
VLSI	Very Large Scale Integration
VSCS	Voltage Switched Current Source
WL	Word-Line
XOR	Exclusive OR
XNOR	Exclusive NOR

Chapter 1

Introduction

1.1 Motivation

The semiconductor industry has witnessed a phenomenal growth that has evolved into one of the critical economic foundations, which has immense impact to the global economy. For the last two decades, most of the worldwide output of the semiconductor industry has been used in the Personal Computer (PC) sector. However, in today's mass consumer's market, the mobile electronic appliances sector has surpassed the PC sector in terms of semiconductor revenue [1, 2]. Portable electronic products, ranging from small handheld personal communication devices, such as pagers and cellular phones, to larger and more sophisticated multimedia-based applications, such as laptop and notebook computers, have enjoyed remarkable success.

The huge market demand for portable devices has motivated the trend of System-on-a-Chip (SoC) integration. The move to SoC is further fueled by the rapid progress in silicon process technology that increasingly allows an entire system to be designed into a single integrated device, while garnering the advantages of cost, space and power reductions, and enhanced chip performance [3]. The SoC often consists of mixed-technology designs, including such diverse combinations as embedded DRAM, high-performance or low-power logic, analog, Radio Frequency (RF), Micro-electro Mechanical Systems (MEMS) and optical input/output [4]. Typical SoC Intellectual Property (IP) cores include microprocessors, microcontrollers, digital signal processors, encoders/decoders, bus interfaces, and many other common peripherals [5].

However, the industry has significant challenges, and these challenges must be addressed if we are to continue and prolong the historic growth pattern. The challenges include process and Very Large Scale Integration (VLSI) design issues especially as we move into the regime where conventional technologies will no longer work.

The concern for power dissipation in design has traditionally been of secondary importance to other design constraints, such as operating speed and area. However, with the advent of portable electronics and high-performance SoC chips that threaten to exceed power dissipation limits, power management has emerged as a prerogative and vital metric in the design of integrated circuits. With high power dissipation leading to the generation of high temperatures on the chip, the reliability of the chip will be very much degraded. This will tend to exacerbate several silicon failure mechanisms such as package-related failure, electromigration and gate oxide degradation. Consequently, such high-speed products would inevitably demand expensive packaging and cooling techniques to effectively reduce the heat associated with the product. Therefore, the developments of low-power devices, circuits, algorithms and architectures are imperative for the successful realization of SoC for wireless communications and portable computing applications [6].

In our technology savvy mass market, the relentless drive for high-speed and real-time operation is commonly seen. However, high-level of sophistication comes with a price in increased complexity, in particular, a sacrifice or even an upsurge in power and area consumption. In most cases, a high operating speed is often achieved at the cost of an increase in power consumption and/or silicon area. Power dissipation is placed on an equal footing with performance because of the emergence and increasing popularity for smaller and more durable mobile computing and communication systems. Portability imposes a stringent limitation on power dissipation while still demanding high computational speeds as necessitated by real-time tasks. In view of that, it is imperative to strike a balance between the two often-conflicting power and delay entities [7-9]. Therefore, the Power-Delay Product (PDP) is also used as a prerogative metric of performance in this research.

There is a need, therefore, to invest more time and effort in designing low-power chips without sacrificing high performance while requiring only a reasonable amount of the silicon real estate. Furthermore, with the relentless drive for deep submicron VLSI/ULSI technology, where device sizes continue to shrink into submicron dimensions at increasingly higher speed, the requirement for low-power consumption in a single chip becomes increasingly prominent.

It is evident that power has become a major consideration that endangers portability, reliability, cost-effectiveness and environmental-friendliness in the leading edge VLSI and Giga Scale Integration (GSI) engineering. In this context, the Complementary Metal Oxide Semiconductor (CMOS) technology [10], with low power dissipation and high packing density, has proven to be a workhorse for off-the-shelf portable applications as well as non-portable products. The major characteristics of CMOS technology such as cost efficiency, performance improvement, and ease of integration for high-performance digital/analog circuits, compounded by innovative circuit design techniques have further accentuated its dominance as the favored solution for realizing high-end handheld devices [11].

Based on the above-mentioned issues, it is important to explore well-engineered technologies that meet the essential criteria of low-power and high-speed integrated chips. In this research, the design of CMOS subsystems, which is particularly accustomed to the portable electronic products where speed, area and power are of utmost importance, will be attended to. Subsystems are the integral part of the SoC. The CMOS subsystems that consume excessive power will be identified and we will in turn tackle the power consumption issue in a SoC environment.

Our research embraces critical elements coexisting in the SoC that perform fundamental and crucial operations such as adders, comparators, and memories. Adders are elements that demand for careful and assiduous research in circuit design. This is because addition is an obligatory and indispensable function in most fundamental arithmetic operations. It is used extensively in many VLSI design paradigms and is by far the most frequently used operation in a general-purpose system and an application specific processor. It is a very critical operation because it involves a carry propagation step, where the propagation of carry signal from each bit to all higher bit positions is necessary. Subsequently, this results in a substantial circuit delay and hence the adder that lies in the critical delay path determines the overall speed of the system. Given the potential versatility of adders in the contemporary research field, it is worth devoting an entire chapter in this thesis to describing adders designed for low-voltage and low-power environment.

The revitalization and increasing popularity of current-mode signal processing techniques have accentuated the importance of a small area and low power-delay product current comparator as it is one of the main building blocks of current-mode design. An extensive literature survey has been carried out on the existing current comparators. However, it is found that most of these circuits produce a two-level output voltage in response to the polarity of the input currents, rather than performing a current detection based on a pre-defined value of the threshold current. In other words, the input current of these circuits is often considered as the subtraction or difference between a threshold current and an actual input current signal. The circuit structure that realizes such subtraction is not illustrated. In view of that, there is an absence of adequate circuit design consideration for the required current subtraction segment that drives these circuits. There is an immediate need, therefore, to design a competitive current comparator that incorporates the current subtraction circuit.

The memory subsystem is a requisite attribute in the age of Information Technology (IT) [12]. It is the vital enabling technology in the SoC era whereby a myriad of value-added products can be realized. However, one critical underlying problem is the widening gap between the speed performances of the faster processor and the slower DRAM-based main memory. Further advances on the processor speed yield limited performance improvement due to the memory bottleneck [13]. In an effort to circumvent this issue, cache memory is a widely used technique for traversing this gap. SRAM is often used in the implementation of the cache memory due to the requirements for high speed performance and ease in applications. Operating at a much higher speed, an SRAM-based cache memory temporarily stores a portion of the frequently accessed data content of the main memory. The memory circuits, e.g. the cache memory, are a significant component of the total power consumption of a single chip due to its extensive use [14, 15]. Hence, circuit design techniques are often ventured and employed to minimize power dissipation. As a matter of fact, the most effective means of minimizing the power consumption in today's research is by lowering the operating power supply voltage. Nevertheless, this is the root of some critical problems, particularly in memory circuits where the time delay to sense the signals from the memory cells rises immensely. On top of that, reducing the supply voltage causes degradation of the readout voltage

amplitude on the bit-lines. Thus, designing a sense amplifier with high sensitivity for SRAM applications is one of the prime concerns of this project. Detailed description of the design of low-power high-performance CMOS subsystems will be presented in the following chapters.

1.2 Objectives

With the presently accelerating semiconductor industry, the consumer electronics market niche is marching towards high-performance access through the deployment of wireless portable appliances. It is therefore evident that there are many opportunities for research and studies on more efficient and sophisticated low-power, high-speed and small-area design. The research presented in this dissertation continues with this philosophy and proposes techniques to realize subsystems with the lowest possible power dissipation at a better or at least equal speed, or, best possible speed at a lower or at least equal power dissipation, while minimizing the silicon area cost. In other words, the goal is to improve the PDP of a particular subsystem.

The objective of this project is to address the above-mentioned challenges. Its fundamental goals are to stimulate new and concrete ideas that develop the forefront of VLSI low-voltage/low-power subsystem designs by integrating the CMOS technology in the deep submicron era, while sustaining a high-speed performance and small silicon area consumption. The scope of this project also covers a profound analysis on the state-of-the-art development of the CMOS subsystems for the low-voltage, low-power SoC environment.

1.3 Major Contributions of the Thesis

The specific contributions of this research work are outlined below:

- 1) A low-power high-performance Carry-Select Adder (CSL) is proposed. It addresses and eliminates the weak point of the existing add-one CSL circuits. A 64-bit addition implementation in a realistic simulation environment has demonstrated the performance feasibility of the proposed circuit as compared to the conventional and contemporary designs.

- 2) An area-efficient current-mode comparator with low PDP is introduced. It acts as a perfect complement to the conventional current comparator for low threshold current (I_{th}) levels. An especially promising property is that the area advantage becomes more significant with reducing feature size/technology. This attribute blends well with the further miniaturization of contemporary and ongoing process technology.
- 3) A new high-speed current conveyor amplifier for low-voltage low-power SRAM applications is developed. The performance evaluation has shown that the new circuit offers substantial improvement over the conventional circuit in terms of speed and power-delay product for approximately the same Integrated Circuit (IC) layout area. The sensing delay of the new circuit remains comparatively low regardless of variations in bit-line and data-line capacitances.
- 4) Another current sense amplifier that employs a cross-coupled current-mirror configuration is designed, which offers high-speed performance and low-power consumption. It is also appropriate for use in low-voltage low-power SRAM applications. Its sensing speed is independent of the bit-line capacitances and is relatively insensitive to the data-line capacitances. Simulation results have shown that the new sense amplifier has performance advantages over the conventional sense amplifier circuits in terms of speed, power and sensing delay sensitivity.
- 5) A novel micro-power current sense amplifier, which is an evolution of the previous two designs, is presented. Its sensing speed is independent of the bit-line capacitances and is relatively insensitive to the data-line capacitances. Post-layout simulation results have verified that the new sense amplifier promises a much sought-after power-efficient advantage and note-worthy power-delay product superiority over the conventional and other recently reported sense amplifier circuits.

1.4 Organization of the Thesis

The remainder of this thesis is organized as follows: Chapter 2 provides an overview of the CMOS technology and accentuates its continued dominance in the information technology industry. Also, the past, present and future trends in CMOS technology development and power supply voltage scaling are illustrated. Following that,

the sources of power dissipation and various techniques to achieve low-power dissipation ranging from the process level to the system level are reviewed.

Chapter 3 presents the low-power high-performance CMOS adder. The chapter provides a comprehensive literature review of the standard adder cells, i.e. the half adder and full adder. The full adder serves as a basis for different architectures of adder types, such as the Ripple Carry Adder (RCA), the Carry Select Adder (CSL), and Carry Skip Adder (CSK), which will also be individually addressed. Then, Current-Mode Multiple-Valued Logic (CMMVL) adders are introduced as an alternative methodology for designing competitive adder blocks. We then report the design and implementation of a proposed 64-bit square-root CSL by incorporating the hybrid combination of CSK and a modified add-one circuit. This adder has been extensively simulated and analytically compared with the conventional CSL and three other existing add-one architectures. The simulation results show that the proposed adder outperformed the other adders in comparison in terms of power dissipation, worst-case delay, and also PDP with relatively low hardware cost. In view of that, it is intuitively a viable contender to replace the conventional CSL and contemporary add-one CSL circuits.

Chapter 4 gives a detailed description of the continuous-time CMOS current-mode comparators. It begins with the literature review of the existing current comparator designs without the integration of a current subtraction circuit. Subsequently, the current comparators with the current subtraction segment are reported. The chapter also proposes an area-efficient CMOS current-mode comparator circuit design for low current applications, which is a variation of the conventional current-mode comparator. The justification for the emphasis on the research of the proposed area-efficient current-mode comparator for low current operation is supported by providing adequate referenced applications where such a design can be of specific merit without unduly sacrificing the critical power-delay characteristics. An accompanying benefit of reducing the effective area utilization of the proposed CMOS multiple-valued current comparator is a reduction of PDP, particularly in the advanced submicron regime, as manifested in the simulation results. In addition, the implementation of a single-stage Positive-Digit Adder (PDA), using the proposed current comparator has reflected an increased novelty and performance merits of our proposed design.

Another important CMOS subsystem is the memory, which is the focus of Chapter 5 of this dissertation. The demand for higher capacity electronic devices with high-performance and low-power dissipation has made it necessary to create improved memory designs to facilitate new system implementations. We first present an overview of semiconductor memory, which includes the Read-Only Memory (ROM), Static Random Access Memory (SRAM), and Dynamic Random Access Memory (DRAM), followed by a more thorough coverage of SRAM. Among the building blocks of the SRAM architecture, the sense amplifier is the key to achieving high-speed and low-power SRAM designs. Therefore, in this chapter, it becomes our primary goal to design high sensitivity sense amplifiers, without compromising the power and area properties. It has been demonstrated that current-mode sensing techniques offer greater advantages than their voltage-mode counterparts. We have therefore developed three current sense amplifier designs, which satisfy the crucial criteria of retaining a low PDP. The underlying tenet of our sense amplifier designs is to amplify the bit-line differential current signals to ensure a swift response time.

Chapter 6 summarizes the conclusions of this dissertation and outlines several constructive recommendations for future research.

Chapter 2

Low-Power Digital CMOS Circuit Design

2.1 Overview of CMOS Technology

To set the scene for this dissertation, it is useful to present a discussion on the CMOS technology. CMOS, short for Complementary Metal-Oxide Semiconductor technology, employs both n-type and p-type transistors to realize logic functions. Today, CMOS technology has carved out a niche for itself as the dominant semiconductor VLSI technology for microprocessors, memories and Application-Specific Integrated Circuits (ASICs) as diverse as DVD players, mobile phones and automotive engine management that require highly complex circuits to be integrated in very small silicon chips. Very often, CMOS turns out to be the top choice for digital-logic design, particularly in portable, low-cost, and low-frequency applications.

The most prevalent description of the advancement of CMOS technology is none other than the Moore's Law, introduced by Gordon Moore in 1965 [16]. In his observation, Moore presciently envisioned an exponential growth in the number of transistors that could be integrated on a single die and he predicted that this trend would continue. More precisely, he anticipated a doubling in the transistor density per integrated circuit every couple of years. This prediction has proven to be remarkably true for the subsequent few decades. This exponential growth and ever-shrinking transistor size result in increased performance and decreased cost. This is the amazing characteristic of transistors that fuels the rapid growth of the semiconductor industry and the information technology age: their speed increases and their cost decreases as their size is reduced [17].

CMOS technology provides performance superior to n-channel Metal Oxide Semiconductor (nMOS) and bipolar technologies with respect to power dissipation, noise margins, packing density, and the ability to integrate large complex functions with high yields. Even though the MOS field-effect transistor has been traditionally recognized as

an inherently slower switching component than its bipolar counterpart, the incessant accelerated scaling of the feature size has contributed to eliminate the roadblocks preempting its widespread applications [11]. Despite the speed advantage of the bipolar transistor, its power dissipation does not decrease as rapidly as its CMOS counterpart at smaller sizes, and hence the bipolar devices have lower achievable packing density than the CMOS devices. As a result, CMOS technology is able to attain greater system-level performance at high integration levels. Apart from that, there is a significant decrease in the number of parts and interconnections in CMOS technology, and fewer components translate to fewer failures. Consequently, this results in better speed and power performance, while lowering the cost of computing in a granular and scalable fashion.

2.2 Trends of Technology and Power Supply Voltage

Significant progress has been made towards producing devices with ever-decreasing miniaturized scale. It is anticipated that nanometer-scale devices will continue this trend. Figure 2.1 depicts the projected trend of technology of the Microprocessor (MPU) printed gate length and power supply voltage scaling from the year 2003 to 2018. This information was obtained from the 2004 update of International Technology Roadmap for Semiconductors (ITRS) [18]. In 2003, the MPU printed gate length was 65 nm and it is currently at 45 nm in 2005. It is conceivable that the gate length will reach 10 nm in 2018 once the problem in manufacturing yield is overcome. As for the power supply voltage, it was at 1 V in 2003, entered the sub-1 V regime in 2004, and is expected to experience a “ladder-like” reduction to 0.5 V in 2018 due to portability and reliability issues.

Figure 2.1 ITRS trends of technology and power supply voltage.

2.3 Sources of Power Dissipation in Digital CMOS

The primary advantage of CMOS over nMOS and bipolar technologies is the much lower power dissipation. Unlike nMOS or bipolar circuits, a CMOS circuit has significantly lower static power dissipation for technologies preceding $0.18\ \mu\text{m}$ [19, 20] and power is mainly dissipated when the circuit actually switches. Hence, the CMOS is inherently a low-power logic family. Basically, there are two important mechanisms of power consumption in digital CMOS circuits, namely, the dynamic power dissipation and static power dissipation. Dynamic power dissipation (P_{dyn}) is further categorized into two components: switching power (P_{switch}) and short-circuit power (P_{sc}), whereas the static power dissipation (P_{stat}) has another two constituents: leakage power (P_{leak}) and DC power (P_{DC}) [21-23]. Therefore, the average power dissipation (P_{avg}) in digital CMOS circuits can be expressed by:

$$\begin{aligned}
 P_{\text{avg}} &= P_{\text{dyn}} + P_{\text{stat}} \\
 &= P_{\text{switch}} + P_{\text{sc}} + P_{\text{leak}} + P_{\text{DC}}
 \end{aligned}
 \tag{2.1}$$

2.3.1 Dynamic Power Dissipation

Dynamic power consumption is typically the dominant entity accounting for at least 84% [24] of the total power dissipation at 0.18 μm CMOS technology. As mentioned earlier, there are two elements of dynamic power, i.e., the switching power and short-circuit power. Consider the CMOS inverter depicted in Figure 2.2, which is the most fundamental and hence important CMOS gate.

Figure 2.2 A CMOS inverter model for switching power computation.

The switching power component stems from the transient behavior of the CMOS circuit while charging and discharging the parasitic capacitive nodes, which are made up of gate, diffusion and interconnect capacitances. The cumulative effect of these capacitances is lumped at the output as capacitor C_L . For this explanation, we assume a step input, i.e., zero rise and fall times such that neither the pMOS and nMOS devices are conducting simultaneously. During a falling transition at the input, the pMOS transistor turns on and the nMOS transistor turns off. At this time, a certain amount of energy (E_{VDD}) is drawn from the power supply to charge the capacitor C_L from 0 to V_{swing} through the pMOS device, where V_{swing} denotes the voltage swing. The value of E_{VDD} can be calculated by integrating the instantaneous power over the period of interest as shown below:

$$E_{VDD} = \int_0^{\infty} i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^{\infty} C_L \frac{dv_{\text{out}}}{dt} dt = C_L V_{DD} \int_0^{V_{\text{swing}}} dv_{\text{out}} = C_L V_{DD} V_{\text{swing}} \quad (2.2)$$

In most cases, a full rail-to-rail swing is often observed. However, for some logic styles, such as the single-gate pass transistor implementations, the voltage swing on some internal nodes may be slightly less than V_{DD} [25, 26]. Considering a full swing at the output node for our CMOS inverter example, the voltage swing is equivalent to the power supply voltage, hence $V_{\text{swing}} = V_{DD}$. In view of that, Equation (2.2) becomes:

$$E_{V_{DD}} = C_L V_{DD}^2 \quad (2.3)$$

Part of this energy is dissipated in the pMOS network while the remainder is stored in C_L . The energy stored in C_L (E_c) can be derived as:

$$\begin{aligned} E_c &= \int_0^\infty i_{V_{DD}}(t) v_{\text{out}} dt = \int_0^\infty C_L \frac{dv_{\text{out}}}{dt} v_{\text{out}} dt \\ &= C_L \int_0^{V_{\text{swing}}} v_{\text{out}} dv_{\text{out}} = C_L \int_0^{V_{DD}} v_{\text{out}} dv_{\text{out}} = \frac{C_L V_{DD}^2}{2} \end{aligned} \quad (2.4)$$

Judging from Equations (2.3) and (2.4), it is observed that literally only half of the energy supplied by V_{DD} is used to charge C_L whilst the other half has been wasted by the pMOS device. During a rising transition at the input, the pMOS transistor turns off and the nMOS transistor turns on, following which the capacitor C_L is discharged and its stored charge is dissipated in the nMOS network. As a result, each full switching cycle (transition of 0-to- V_{DD} followed by V_{DD} -to-0) requires a fixed amount of energy, which is $C_L V_{DD}^2$. As for the computation of power dissipation, it depends on how frequently the gate is switched. If the gate is switched on and off at a frequency f , the switching power dissipation is:

$$P_{\text{switch}} = C_L V_{DD}^2 f \quad (2.5)$$

One thing to note is that in a logic network, not all gates switch at a full rate of f . The activity is considerably lower. This phenomenon can be accommodated in this context by introducing the switching activity, α , which is the fraction of times the output node experiences switching (0-to- V_{DD} -to-0) in a given clock cycle. Equation (2.5) now becomes:

$$P_{\text{switch}} = \alpha C_L V_{DD}^2 f \quad (2.6)$$

The previous assumption that the input waveform has zero rise and fall times is of course an oversimplification. In reality, the finite rise and fall times imply the momentary

existence of a direct current path from V_{DD} to ground during switching. Thus, short-circuit current flows whenever there is a transition in static CMOS circuits. This leads to another class of dynamic power dissipation, which is less substantial than its switching counterpart: the short-circuit power. It has been reported in the literature that the short-circuit power is about 10% of the total dynamic dissipation if V_{th}/V_{DD} is kept constant [27]. Considering the CMOS inverter pictured in Figure 2.2, this happens for a short period of time when both nMOS and pMOS devices are conducting (a short-circuit condition). Assume that the CMOS inverter in question is symmetrical, with gain factors, $k = k_p = k_n$ and threshold voltage, $V_{th} = |V_{thp}| = V_{thn}$ for the pMOS and nMOS transistors, respectively. If the inverter is driven by an input voltage waveform with equal rise and fall time ($\tau = t_{rise} = t_{fall}$) and with zero load capacitance, the average short-circuit current is given by [28]:

$$I_{sc} = \frac{k\tau f}{12V_{DD}}(V_{DD} - 2V_{th})^3 \quad (2.7)$$

The short-circuit power dissipation is then:

$$P_{sc} = V_{DD} \times I_{sc} = \frac{k\tau f}{12}(V_{DD} - 2V_{th})^3 \quad (2.8)$$

The short-circuit component of power dissipation is insignificant when the rise/fall time of the input waveform is small, and/or when the output load capacitance is large (output rise/fall time larger than the input rise/fall time). In this case, the short-circuit path between V_{DD} and ground will only be active for a relatively short period of time.

2.3.2 Static Power Dissipation

Static power is the power consumed during the intervals when the logic states remain constant. Ideally, this class of power dissipation is completely absent in a static CMOS logic gate because the pMOS and nMOS transistors are never on concurrently in steady-state mode. Yet, in reality, since the MOS transistor is not a perfect switch, there is still a minimal contribution of the static component to the total amount of dissipation. There are potentially two main classes of static power, namely the leakage power and the DC power.

The basic CMOS model for the leakage power calculation is portrayed in Figure 2.3. This is a source of power that is common to all CMOS-based logic families. Apparently there are two types of leakage currents flowing, viz. the reverse-bias current, I_{rev} , and the subthreshold current, I_{sub} . The reverse-bias current is caused by the parasitic diode junctions located between the source or drain and the substrate of the transistors. This occurs when a transistor is turned off, while the other conducting transistor charges/discharges the drain of the former transistor with respect to its substrate potential. The reverse-bias current is expressed by the ideal diode equation:

$$I_{\text{rev}} = I_s \left(\exp \frac{V_d}{V_T} - 1 \right) \quad (2.9)$$

where $I_s = A_D J_s$ denotes the reverse saturation current, A_D is the area of drain diffusion and J_s is the reverse saturation current density. Meanwhile, V_d is the diode biasing voltage, $V_T = KT/q$ denotes the thermal voltage, where q is electronic charge, K is the Boltzmann constant, and T is the absolute temperature.

Figure 2.3 A CMOS inverter model for leakage power computation.

Very often, the reverse-bias diode leakage power is a negligible fraction of the overall power consumption. However, it may become substantial for a system application that spends most of its time in standby mode since this power is being dissipated even when there is no switching activity.

A more significant source of leakage current is the subthreshold current of the transistors. It is caused by the carrier diffusion between the source and the drain when the

gate-source voltage, V_{gs} , is within the weak inversion operating region lying below the threshold voltage, V_{th} , where carrier drift mechanism is dominant. The current in the subthreshold region is given by:

$$I_{sub} = K e^{\frac{V_{gs} - V_{th}}{nV_T}} \left(1 - e^{-\frac{V_{ds}}{V_T}} \right) \quad (2.10)$$

where K is a function of the technology, V_{ds} is the drain-source voltage, and V_T is the thermal voltage. Also, $n = 1 + \Omega t_{ox}/D$, with t_{ox} being the gate oxide thickness, D being the channel depletion layer width and $\Omega = \epsilon_{si}/\epsilon_{ox}$, where ϵ_{si} and ϵ_{ox} are the Si and SiO₂ permittivity, respectively. For $V_{ds} \gg V_T$, the value of $(1 - e^{-V_{ds}/V_T}) \approx 1$, which means that the drain-to-source leakage current is independent V_{ds} , for V_{ds} approximately larger than 0.1 V. For both sources of leakage, the resulting static power dissipation is given by:

$$\begin{aligned} P_{stat} &= I_{leak} V_{DD} \\ &= (I_{rev} + I_{sub}) V_{DD} \end{aligned} \quad (2.11)$$

Another source of static power dissipation, the DC power, originates from two scenarios: degraded (non full-swing) voltage levels feeding into complementary static gates, and the pseudo nMOS circuit family. A typical example for the first scenario is depicted in Figure 2.4. It shows an nMOS pass transistor driving a CMOS inverter.

Figure 2.4 An example illustrating the DC power caused by reduced voltage levels.

This circuit structure experiences a degenerated potential at node X , which is only $V_{DD} - V_{thn}$, as the nMOS transistor passes a poor V_{DD} . This voltage is not high enough to fully turn off the pMOS transistor and hence at this point, the pMOS device will enter the weak conduction state since $|V_{gs} - V_{thp}|$ is close to zero. As a result, a DC current, I_{DC} , will flow from V_{DD} to ground.

As in the pseudo-nMOS logic style [23], a single pMOS device with grounded gate forms the pull-up network while a complex block of nMOS devices implements the pull-down network. In view of this circuit style, there always exists a direct path from V_{DD} to ground, as the pMOS transistor is conducting at all times. As compared to the CMOS logic, this logic family can minimize power consumption only for applications in which the complex logic switches at high operating frequencies. If the circuit is idle most of the time, then the DC power will tend to contribute substantially to the total power consumption.

2.4 Low-Power Design Techniques

As mentioned earlier, low-power technology enables mobile products to run longer or to host more features. Power optimization can be realized at different levels of the circuit design hierarchy, starting from the elementary device/process level, physical/layout level, circuit level, logic level, architecture level, algorithm level, all the way up to the system level [22, 29, 30]. An important point that deserves careful consideration is to assess the effect of power optimization approaches on other parametric criteria such as speed performance and area requirement, which are also the important figure of merits determining a system's overall performance.

2.4.1 Device/Process Level Power Optimization

Equation (2.6) in Section 2.3.1 suggested that the switching power is proportional to V_{DD}^2 . Since the switching power accounts for the largest fraction of the total power dissipation, it is therefore a seemingly attractive method to reduce the supply voltage for a significant quadratic reduction in the power consumption of CMOS logic. Unfortunately, the scaling of the supply voltage imposes speed degradation. One possible

solution at the device/process level is to commensurately decrease the V_{th} to allow V_{DD} to be scaled down (hence lowering the switching power) and avoid the speed penalty. However, at some point, the power advantage obtained from the reduction of V_{th} and V_{DD} is offset by an increase in the subthreshold leakage currents, resulting in significant static power dissipation. Following that, an optimal V_{th} , which must compromise between the enhancement of the current drive at low- V_{DD} operation and the control of subthreshold leakage, is required for a given level of logic complexity. Besides, the value of the optimal V_{th} is also affected by the necessity to attain adequate noise margins. Apart from that, processes with dual (or multi) V_{th} have also been developed to address the excess power caused by subthreshold leakage [31, 32]. The basic principle is to make use of low- V_{th} transistors with low V_{DD} in the switching mode to retain high speed, whereas in the standby mode, devices with high V_{th} are utilized to ensure ultra low leakage power.

2.4.2 Physical/Layout Level Power Optimization

The advances in semiconductor technology and the advent of the system-on-chip era have caused the effects of interconnect parasitic capacitance on the latency, power consumption and VLSI area to become increasingly non-trivial [33, 34]. As a result, reducing the parasitic capacitance has emerged as a key design premise for the reduction of dynamic power dissipation. The parasitic capacitance can be reduced by incorporating power-conscious layout schemes where fewer and smaller devices as well as fewer and shorter interconnects are used at the physical/layout level. The physical place and route should be optimized such that signals that have high switching activity (such as clocks) should be assigned short wires and signals with lower switching activity can be allowed to use relatively longer wires.

2.4.3 Circuit Level Power Optimization

As for the circuit level, optimized transistor sizing plays an indispensable role in achieving minimized power dissipation regardless of the choice of logic family or topology. The choice of transistor dimensions has always a major impact on the area, performance and power dissipation of a circuit [35-37]. To realize low power and also

high speed circuit design, it is crucial to optimize and equalize all delay paths so that a single critical path does not unnecessarily limit the performance of the entire circuit [29]. The basic idea of this method is to optimize the transistor sizes and make proper connections to a particular circuit so that the discrepancies of the delay throughout each interconnection path are minimized.

Another efficient means of power dissipation optimization is by the proper choice of logic style. In a nutshell, the CMOS circuits can be categorized into static logic and dynamic logic. The static CMOS logic family is further divided into complementary CMOS logic and pass-transistor logic.

The complementary static CMOS gate is composed of a combination of dual networks, i.e. the pMOS Pull-Up Network (PUN) and the nMOS Pull-Down Network (PDN) controlled by the identical set of inputs feeding to the gates of the pMOS/nMOS pairs. A representative complementary static CMOS gate is given by the CMOS inverter depicted in Figure 2.2 of the previous section. The PUN and PDN provide a conditional/potential connection between the gate output and the power lines, V_{DD} and V_{SS} , respectively. The plus points of the static CMOS include robustness against noise, voltage scaling and transistor sizing, hence offering a great reliability at low voltages and arbitrary transistor sizes [25]. In addition, the CMOS circuit offers straightforward and efficient layout due to the complementary transistor pairs. One significant drawback of the static CMOS circuit is its relatively weak output current drivability due to the series connection of transistors at the output. This can be compensated by inserting additional buffers/inverters at the output stage. Nevertheless, the CMOS family's driving capability is still superior to that of the pass-transistor logic family, which will be discussed below.

The pass-transistor logic family makes use of only a single nMOS (or pMOS) network to implement a logic function, rather than a full complementary transistor to reduce the number of transistor. A distinctive feature that differentiates the pass-transistor logic from complementary CMOS is that the source terminal of a transistor is connected to the input signals instead of V_{DD} or V_{SS} [25]. It is feasible to implement logic functions and at the same time alleviating the node capacitance. Nonetheless, there exists an inherent threshold drop issue in pass-transistor logic, resulting in reduced current drive capability and hence deteriorated speed at scaled power supply voltages. Other than that,

direct-path static power could constitute a noteworthy proportion of the total power dissipation of this logic family since the “high” input voltage level at the regenerative inverters/logic gates is slightly lower than V_{DD} , causing the pMOS device to be incompletely turned off. To overcome this problem, a level restoration circuit is often incorporated at the gate output to eliminate the static currents at the subsequent stage. However, the pass-transistor circuits with level restoration are less robust than the complementary CMOS as they are more vulnerable to voltage scaling and transistor sizing, hence requiring careful transistor optimization to ensure correct gate functionality [38]. From the layout viewpoint, the pass-transistor circuit is not as straightforward as it requires implicit routing to accommodate the overhead of the complementary signals and the rather irregular transistor arrangements, which require higher wiring complexity. The most efficient pass-transistor style is the Complementary Pass-transistor Logic (CPL). An example of a two-input multiplexer (MUX) implemented in CPL is portrayed in Figure 2.5. The two nMOS networks (one for each signal rail) implements the logic function, the two weak pMOS transistors form the level restoration circuit for the reduced swing passed by the nMOS transistors, while the inverters are used as buffers for the complementary output signals.

Figure 2.5 The CPL implementation of a two-input MUX.

A variation of CPL that successfully overcomes the voltage drop problem is the transmission gate logic circuit. It is a special kind of pass-transistor logic circuit in which

a pMOS transistor and an nMOS transistor are connected in a parallel arrangement, which is individually controlled by a pair of complementary control signals. The transmission gate acts as a bidirectional switch and when both pMOS and nMOS are turned on simultaneously, the input signal will be propagated to the output without any potential loss. As a result, no level restoration circuitry is required in this logic style. The main shortcoming of the transmission gate logic is that it requires twice the number of transistors or more transistors than the standard pass-transistor logic to implement the same circuit, hence increasing the node capacitance.

Contrary to static logic, the operation of dynamic circuit proceeds in two phases, viz. the precharge and the evaluation phase [21, 22, 25, 29, 30, 39]. Its logic function is implemented by a single pMOS PUN or an nMOS PDN, hence resulting in substantially smaller area, reduced parasitic input capacitance, and higher speed as compared to its static CMOS counterpart. Also, short-circuit power and glitching power are intrinsically absent in dynamic circuit operation. However, notwithstanding its advantages mentioned earlier, the dynamic logic exhibits large clock loads and high switching activity due to the precharge mechanism, hence consuming an excessively high power. Moreover, the dynamic logic is less robust with regards to noise. This is aggravated by the fact that this logic style has a number of inherent deficiencies such as charge leakage and charge sharing that must be dealt with to guarantee functional operation. Due to this noise susceptibility, the operating margin of the dynamic circuit narrows rapidly with the scaling down of V_{DD} .

Having presented some of the available logic families with their own distinct characteristics, it is apparent that circuit designers must select from a wide variety of logic styles to minimize power, delay, and/or area. The factors determining the choice of a certain technique is therefore application-dependent and some trade-offs have to be made to achieve their intended goals. However, judging from several studies reported recently, static CMOS fits all applications and is the style of choice for robust, low-voltage amenable and low-power designs [25, 40].

2.4.4 Logic Level Power Optimization

Power optimization at the logic level can be realized by a number of different techniques, some of which are technology mapping, retiming, and logic level power down. Technology mapping refers to the process of selecting library gates to implement a design that has been structurally optimized, with the aim to reduce switching activity [41]. Besides, positioning registers or flip-flops in sequential circuits via retiming is also a potential method of minimizing power consumption [42, 43]. This is done by first identifying the circuit nodes with high glitching activity or high parasitic capacitance and then placing a flip-flop at the particular node to filter out unwanted transitions. Other than that, logic modules may be switching and dissipating power even when they are not performing useful tasks. Therefore, another efficient topology to reduce the switching activity is to power down the execution units as and when they are not required [29, 30]. This can be realized by using gated clocks to disable the clock inputs to these modules [44].

2.4.5 Architecture, Algorithm, and System Level Power Optimization

There are a myriad of design methodologies in optimizing architectures for low-power applications [22, 23, 29]. These techniques include architecture driven voltage scaling using parallelism and pipelining, switching activity reduction by the choice of number representation, the exploitation of signal correlations, glitching activity minimization, and power shutting down of the unused blocks. For instance, parallelism plays an important role in power reduction since reductions in V_{DD} produce a quadratic decrease on dynamic power dissipation without any speed penalty [23, 45].

At the algorithm level, power consumption is minimized by decreasing the number of operations required to execute a particular task so as to effectively reduce the overall switching activity [23]. Besides, the exploitation of concurrency is also a good candidate to reduce V_{DD} and power [29]. Hence, the ability for an algorithm to be parallelized is crucial. A good algorithm also makes the hardware design straightforward and regular.

Finally, for system-level optimization, it is feasible that the clocks used system wide to be tuned to a low frequency, while the on-chip phase locked loop provides the circuit with the required higher frequency rate [45]. High-level integration of off-chip peripheral integrated circuits into one single chip is also a viable alternative using, for example, the SoC paradigm.

Chapter 3

Low-Power High-Performance Adder

3.1 Introduction

Addition is an obligatory and crucial function in the fundamental arithmetic operations [46, 47]. It is used extensively in many VLSI design paradigms and is by far the most copiously used operation in general-purpose systems and application-specific processors. Addition is a fundamental part of the arithmetic unit because the mathematical operations, such as subtraction, multiplication, division, and address calculation, usually rely on it. For example, the exploitation of a two-operand addition is inevitable in the final stage of a Wallace tree multiplication process. Its essentiality is accentuated by the fact that a fast Carry Propagate Adder (CPA) contributes a typical 25% to 35% of the total multiplier delay [48]. Hence, the adder is dubbed the heart of any microprocessor, DSP architecture, and data processing system.

In the addition process, each of the resulting bits relies on all input bits of equal or lower magnitude [49]. It is a very critical operation because it usually involves a carry ripple step, where the propagation of carry signal from each bit to its higher bit position is necessary [50]. This results in a substantial impediment in circuit delay and hence, the adder that lies in the critical delay path determines the overall speed of the system [51]. On the other hand, reducing the power consumption of the designed adder has emerged as an area of prime concern for VLSI system designers. This can be attributed to the emergence and increasing popularity of smaller and more durable mobile computing and communication systems. Low-power dissipation allows portable systems to operate longer with the same battery. Therefore, designing a low-power adder with high-speed performance is unquestionably an important research theme.

Given the potential versatility of adders in the contemporary research field, this chapter is devoted solely to describing the existing adders designed for low-voltage and low-power environment. The chapter begins with the literature review of adders in

Section 3.2. This section encompasses the half adder and full adder cells, which serve as the basis for different adder architectures. An overview of a range of representative architectures of the adder families is presented in Section 3.3.

This chapter also includes a new adder design based on the carry-select and an existing add-one concept in Section 3.4. The proposed adder has been extensively simulated and analytically compared with four other architectures. The circuits being evaluated are simulated for power, delay and power-delay product and the results are analyzed and compared. Section 3.5 summarizes and concludes the work presented in this chapter.

3.2 Half Adders and Full Adders

The Half Adder (HA) is the simplest and the most fundamental type of adder [52]. It takes two single-bit binary input operands and produces a two-bit binary result. The lower order bit of the result is called the *Sum*, whereas the higher order bit is called the C_{out} . The logic gate of the half adder is shown in Figure 3.1 and the truth table representing its operation is depicted in Table 3.1 [53].

Figure 3.1 Logic gate of a half adder.

Table 3.1 Truth table of a half adder.

<i>A</i>	<i>B</i>	<i>Sum</i>	C_{out}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the truth table, the logic functions for the *Sum* and C_{out} are generalized as:

$$Sum = A \oplus B \tag{3.1}$$

$$C_{out} = A \cdot B \tag{3.2}$$

The half adder can only be used for the addition of two single-bit binary numbers because it does not permit a carry-in. To add operands of more than one bit, the adder needs to have three inputs instead of two, in order to take the carry-in into consideration. An adder with a carry-in is called a Full Adder (FA).

The structure of the conventional CMOS full adder is shown in Figure 3.2. It is constructed using two half adders and an OR gate. There are a total of three inputs for the full adder, two for the input numbers *A* and *B*, and one for the carry-in, C_{in} . The outputs are the *Sum* and carry-out, C_{out} . The truth table for the full adder logic circuit is shown in Table 3.2.

Figure 3.2 Logic circuit of the conventional CMOS full adder.

Table 3.2 Truth table of a full adder.

C_{in}	<i>A</i>	<i>B</i>	<i>Sum</i>	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From Table 3.2, the corresponding logic functions for the *Sum* and C_{out} are:

$$Sum = A \oplus B \oplus C_{in} \tag{3.3}$$

$$C_{out} = (A + B) \cdot C_{in} + A \cdot B \tag{3.4}$$

The logic symbol for the full adder is given in Figure 3.3 and it will be used in the following subsections.

Figure 3.3 Logic symbol of a full adder.

The schematic diagram for the direct implementation of Equations 3.3 and 3.4 is portrayed in Figure 3.4 [54]. A 3-input Exclusive OR (XOR) gate is used to compute the *Sum*. This implementation makes use of 32 transistors.

Figure 3.4 The conventional CMOS full adder.

An alternative implementation of the full adder cell that does not need the XOR gates requires only 28 transistors, as shown in Figure 3.5 [54]. The implementation of this full adder is realized by reusing the C_{out} term in the Sum term as a common sub-expression. The logic functions for this implementation are:

$$\begin{aligned}
 Sum &= A \bullet B \bullet C_{in} + (A + B + C_{in}) \bullet \overline{C_{out}} \\
 &= A \bullet B \bullet C_{in} + (A + B + C_{in}) \bullet \overline{(A \bullet B + C_{in} \bullet (A + B))} \tag{3.5}
 \end{aligned}$$

Figure 3.5 Full adder without XOR gates (a) Logic diagram. (b) Transistor diagram.

A modified version of the conventional full adder based on CMOS transmission gates and inverters uses only 20 transistors [55]. The schematic diagram is shown in Figure 3.6 and is logically equivalent to the circuit depicted in Figure 3.4.

Figure 3.6 The modified conventional CMOS full adder.

Although the modified conventional CMOS full adder configuration has been widely accepted and utilized in numerous applications, it often exhibits a critical delay and thus in effect limiting the total system performance. The speed is increasingly diminished when two or more of these full adders are cascaded together for multiple-bit addition. As a result, a fast full adder is designed to ensure better speed performance, the logic realization of which is illustrated in Figure 3.7.

Figure 3.7 Logic structure of a fast full adder.

To further simplify the full adder, a CMOS full adder that exploits the transmission function theory [56-58], namely the Transmission Function Adder (TFA) was developed [59]. Its schematic diagram is illustrated in Figure 3.8. The TFA consists of 16 transistors and dissipates less power as compared to the conventional CMOS full adders reported so far.

Figure 3.8 The Transmission Function Adder (TFA).

Another schematic configuration of the full adder, which ensures both low-power and high-speed performance, is shown in Figure 3.9 [60]. It is a combination of an XOR gate and transmission gates. It has 14 transistors and occupies 30% and 20% less area than the modified conventional CMOS full adder and the TFA, respectively.

Figure 3.9 The 14-transistor full adder.

Next, a low-power CMOS full adder cell using 17 transistors is described [55]. It is based on the XOR and Exclusive NOR (XNOR) gates [61], and the pass-transistors. Comparative analysis showed that it consumes 10% to 15% less power than the TFA and the 14-transistor full adder. This is due to the fact that this cell has no short circuit power and lower dynamic power relative to the other two cells. The transistor schematic of this implementation is portrayed in Figure 3.10.

Figure 3.10 The 17-transistor full adder.

Another promising full adder prototype is the 10-Transistor low-power high-speed Full Adder cell (10-T FA), which employs an XOR gate, an inverter and a pass transistor in its critical path [50]. The schematic diagram is shown in Figure 3.11.

Figure 3.11 The 10-transistor full adder (10-T FA).

This full adder configuration has been compared with the TFA reported earlier. At a power supply voltage of 3.3 V using a 0.6 μm CMOS technology, the 10-transistor FA shows 0.086 ns while the TFA exhibits 0.12 ns for the critical path delay. Also, with the same supply voltage at a clock frequency of 1 GHz, the 10-transistor FA has an average power dissipation of 81 μW , whereas the TFA dissipates about 170 μW of power.

With the array of 1-bit full adders reported so far, the addition of two binary numbers of any number of bits can be computed. An n -bit adder can be built by cascading n 1-bit full adders together. This arrangement results in a Ripple Carry Adder, which will be discussed in the next section.

3.3 CMOS Adder Architectures

In this section, several important families of CMOS adder architectures are studied, each of which offering specific tradeoffs in terms of area requirement, speed performance, and power consumption.

3.3.1 Ripple Carry Adders (RCA)

The basic unit of a Ripple Carry Adder (RCA) is the full adder. It can be extended indefinitely to any number by connecting the carry-out of the previous 1-bit full adder to the carry-in of the next 1-bit full adder. An n -bit RCA consisting of n single-bit full adders is described in Figure 3.12 [45]. The figure clearly shows that the carry bit ripples through the chain of the cascaded full adders, from a lower bit to the next higher order full adder [62, 63].

Figure 3.12 The Ripple Carry Adder (RCA).

The RCA offers good performance for random input data [64] and occupies the smallest area among all other adder architectures. Nonetheless, its delay characteristics depend heavily on the length of the carry propagation path, hence causing it a relatively unfavorable choice for circuits with non-random input operands. Since all the full adders in the RCA are connected together by the carry chain, the worst-case addition will require the carry to ripple from the least significant bit position to the most significant bit position. The worst-case delay increases linearly with the length of the carry propagation path, which is dependent on the number of bits of the operands, n . Similarly, the area of the adder is also proportional to n [63]. Therefore, in situations when speed is a critical

factor and a minimum amount of hardware is not vital, using an RCA in the arithmetic operation will be detrimental. In spite of this, the carry propagation can be enhanced by exploiting faster logic circuit technologies and faster full adder design.

The RCA is subjected to glitching problem [45]. To further illustrate this issue, a 4-bit RCA and its static simulation are depicted in Figure 3.13. Here, we make an assumption that the inputs A_i are set to zero, whereas B_i and C_{in} rise from 0 to 1. Ideally, the outputs S_i should remain at zero. Nonetheless, owing to the delay characteristic of the carry signal along the chain of cascaded full adders, the outputs display spurious transitions, as shown in Figure 3.13(b). This is known as the glitching phenomenon. These dynamic transitions cause extra power dissipation and can contribute to an important portion of the total power. However, this setback can be minimized through careful circuit design and optimization.

Figure 3.13 (a) The 4-bit RCA. (b) Static simulation of the 4-bit RCA.

3.3.2 Carry Look-Ahead Adders (CLA)

The linear increase of carry-ripple delay with the size of the input operand for the RCA can be improved by generating carries of each stage in a parallel circuit [54, 65]. For example, in the Carry Look-ahead Adder (CLA), carries are generated concurrently by means of a look-ahead logic. It is an adder with $O(\log n)$ time and $O(n \log n)$ area. The delay time of the CLA architecture increases logarithmically with the size of the adder, hence allowing the propagation delay of the carry signal to be minimized [66].

The limitation of the sequential method of forming carries in the RCA arises from the fact that it is necessary to specify C_{i+1} as a specific function of C_i . In the CLA, a carry does not depend explicitly on the preceding one, but can be expressed as a function of the relevant propagate and generate signals, P_i and G_i , as well as the initial carry-in, C_{in} . As a result, the CLA comes in handy for better delay performance. However, it is not advantageous for adders of length less than or equal to four because a four-stage RCA is almost as fast and requires less hardware. In addition, the CLA consumes more area and power because of its large number of logic gates.

For a particular combination of inputs A_i and B_i , the propagate signal P_i determines whether the carry-in to the i -th block would propagate to the output, whereas the generate signal G_i determines if a carry-out would be set from inside the block independently from the inputs [62, 67]. The expressions for G_i and P_i with two input binary operands, A_i and B_i are:

$$G_i = A_i \bullet B_i \quad (3.6)$$

$$P_i = A_i \oplus B_i \quad (3.7)$$

Carry generation occurs when $A_i = B_i$. When $A_i = B_i = 1$, a carry of 1 is produced at the i -th position, while for $A_i = B_i = 0$, a carry of 0 is generated instead. On the other hand, carry propagation happens when $A_i \neq B_i$. When the carry-in (C_{in}) is 1 and $A_i \neq B_i$ for some $i = 0, 1, 2, 3, 4, 5$, then C_{in} is said to propagate to the fifth bit position. Figure 3.14 illustrates an example, which shows that carry propagation occurs when $A_i \neq B_i$ and carry generation happens at the 3rd and 11th bits when $A_i = B_i$.

Figure 3.15 Logic schematic of the 4-bit carry generator.

Figure 3.16 Block diagram of the 4-bit CLA.

3.3.3 Carry Select Adders (CSL)

The basic idea of the Carry-Select Adder (CSL) is an anticipatory parallel computation, which can be further categorized as either a linear or square root configuration depending on the block length partitioning. In a linear CSL, the n -bit numbers to be added are divided into several adder stages with equal length. In each of the adder stages, additions are executed in parallel for two different scenarios: one assuming that the carry-in, C_{in} is a zero and another anticipating a one. The results for both possibilities are evaluated conditionally in advance and once the actual value of C_{in} is known, it is used to select the correct result by using a final MUX stage [21]. However, the propagation delay of this adder is linearly proportional to n , viz. the worst-case propagation delay $t_{adder} = O(n)$, which is undesirable.

A better design that successfully gets over this linear dependency is the square root CSL architecture that is portrayed in Figure 3.17 [21]. The input signal, $C_{in,0}$, is the incoming carry, and C_o is the outgoing carry. Meanwhile, S_i^0 and S_i^1 are the sums of the dual RCAs with $C_{in} = 0$ and $C_{in} = 1$, respectively, whereas S_i denotes the actual sum bits, for i bit positions. Unlike the equal-length adder blocks in the linear CSL, the particular block size in the square root CSL is determined according to the arrival times of the S_i^0 , S_i^1 , and the carry-select signal at the MUX. The adder blocks in the square root CSL are made progressively longer from the lower to the higher stage so that the discrepancy of the delay path between the sum and carry-select signals can be diminished. This simple trick enhances the delay characteristics of the CSL to $t_{adder} = O(\sqrt{n})$, which delivers a major benefit in improving the speed performance of parallel adders.

Figure 3.17 The square root carry-select adder.

3.3.4 Carry Save Adders (CSA)

As described in Section 3.3.1, the RCA makes use of a row of cascaded binary FAs to compute the sum of two operands. In fact, with only a slight modification, this row of FAs can also be viewed as a mechanism to reduce three binary numbers into two binary numbers in multi-operand (three or more operands) addition [66]. This method is used in the Carry Save Adder (CSA) where it is indeed a RCA with its carries saved rather than propagated. Therefore, the CSA operator is often called a (3:2) counter.

Unlike the RCA, CLA and CSL adders, the CSA realizes concurrent addition of multiple operands, which is the basic requirement of multiplication. Instead of using the 2-operand adders that necessitate the time-consuming carry propagation to repeat several times depending on the number of operands, the CSA is capable of improving timing with little increase or even reduced area [68].

A CSA tree consists of CSA operators and one adder at the root of the tree. The CSA operators are used to transform an arbitrary number of operands in the addition process to produce two adding operands, and subsequently, the adder at the root of the

CSA tree computes the final sum [69]. Figure 3.18 shows the addition of three 1-bit binary numbers, A , B and C , implemented without and with the CSA operator.

Figure 3.18 The addition process (a) without CSA operation. (b) with CSA operation.

The 1-bit multi-operand addition mentioned earlier can be extended to an n -bit multi-operand addition by cascading the CSA operators. An n -bit CSA consists of n disjoint FAs operating in parallel. Each FA has three i -th bit inputs and generates two outputs, namely the i -th bit partial sum, S_i , and an i -th bit carry, C_i . As for the addition of more than three operands, there is a second or more levels of the CSA operators. They receive the S_i and C_i from the previous CSA operator level, together with another input operand, and produce a set of new S_i and C_i [62]. The levels with CSA operators contain no carry propagation. The carries propagate only in the last step. Consequently, as compared to the RCA's propagation delay of n FAs, the CSA has the same propagation delay as only one FA, and it remains constant for any value of n [68-70].

Figure 3.19 shows a CSA for the addition of four 4-bit binary numbers A , B , C and D , with an initial carry-in, C_0 [62]. The upper two levels of the FA or (3:2) counters form the 4-bit CSA, while the third level is the 4-bit CPA. The CPA used in this case is a RCA, but a CLA or any other fast adders can substitute it. Each CSA operator takes three bits of the same significance and computes the sum of the same significance and the carry for the bit of a higher significance [71].

Figure 3.19 A 4-operand CSA.

3.3.5 Manchester Carry Chain (MCC) and Manchester Adder

The Manchester Carry Chain (MCC) is a carry propagation network that is characterized by the well-known carry generate, G_i , carry propagate, P_i , and carry annihilate (absorb), AN_i , functions. The expressions for G_i and P_i have been introduced in Section 3.3.2 and they will not be repeated here to avoid redundancy. As for the carry annihilate signal, it can be defined as:

$$AN_i = \overline{A_i} \bullet \overline{B_i} = \overline{A_i + B_i} \quad (3.10)$$

The Manchester Adder uses the MCC as its carry network. The carry recurrence function in Equation (3.9) serves as the basis for the MCC. The conceptual representation and CMOS realization of a one-stage MCC are depicted in Figure 3.20 [62]. Referring to Figure 3.20(a), a one-stage MCC can be conceptually analyzed as having three switches, each manipulated by the controlling signals, G_i , P_i and AN_i . It is clear that at any time, only one of the three signals G_i , P_i and AN_i is at logic 1. The carry-out signal, C_{i+1} , is connected to 0 if AN_i is high, to 1 if G_i is high and to the incoming carry, C_{in} , if P_i is high. In other words, if $G_i = 1$, an outgoing carry ($C_{i+1} = 1$) is generated regardless of the C_{in} . If $AN_i = 1$, any incoming carry is annihilated and its propagation is truncated. However, if $P_i = 1$, the C_{in} is allowed to propagate [54].

Figure 3.20 (a) Conceptual representation. (b) CMOS realization of the one-stage MCC.

The CMOS implementation of the MCC is illustrated in Figure 3.20(b) [2]. Once a carry is generated, it quickly propagates along the carry chain composed of transmission gates, until it is finally absorbed. A multiple-bit MCC adder can be constructed by concatenating the circuit in Figure 3.20(b). Buffers are usually inserted between them to partition the n bits into separate groups in order to reduce the delay and strengthen the carry signal.

3.3.6 Carry Skip Adders (CSK)

A Carry Skip Adder (CSK) applies a similar concept as the MCC adder, which is to reduce the carry propagation time by skipping over groups of successive adder stages [62]. A 16-bit RCA divided into four 4-bit blocks is portrayed in Figure 3.21(a) [51]. Each block has four stages ranging from $4k$ to $4k+3$, where k is the number of the block, from 0 to 3. In the meantime, each stage consists of a 1-bit FA with two input binary numbers, A_i and B_i . The Boolean definitions for G_i , P_i , S_i and C_{i+1} are the same as those of the CLA, which have been presented in Equations (3.6) to (3.9), respectively [72].

The time-consuming carry-ripple phenomenon in the RCA can be improved by establishing bypasses or skip paths around the 4-bit blocks, as depicted in Figure 3.21(b). The carry can skip any consecutive stages if the corresponding bits in the two operands are not equal ($A_i \neq B_i$ or $P_i = 1$). Meanwhile, every block computes a block carry

propagate signal, $P_{[4k, 4k+3]}$, which is equal to one if all stages within the block satisfy $P_i = 1$ [62]. Here, the block carry propagate signal is denoted as:

$$P_{[4k, 4k+3]} = P_{4k} \cdot P_{4k+1} \cdot P_{4k+2} \cdot P_{4k+3} \quad (3.11)$$

With this signal, a carry-in into a block k can bypass all the internal stages and straightaway produce a block carry-out. This block carry-out signal will then become the carry-in for the next block. As shown in Figure 3.21(b), the skip logic consists of a 5-input AND gate and a 2-input OR gate with the following Boolean expression for the block carry-out, C_B :

$$C_{B(k+1)} = C_{4k+4} + P_{[4k, 4k+3]} \cdot C_{B(k)} \quad (3.12)$$

where block $k = 0, 1, 2, 3$, denotes the particular group taken into consideration.

Figure 3.21 (a) A 16-bit RCA. (b) A 16-bit CSK with 4-bit skip blocks.

For an n -bit CSK with fixed block size K , the worst-case carry propagation occurs when a carry is generated in stage 0 of block 0 and then ripples through stages 1, 2, $(K-1)$ within the first block, skips blocks 1, 2, $(\frac{n}{K} - 2)$, and propagates through the last block $(\frac{n}{K} - 1)$. In general, with the assumption that the delay of the skip logic is equal to the carry propagation delay from one stage to another (in the first and the last block), the overall time of this carry propagation chain is [51]:

$$\begin{aligned}
T_{\text{carry}} &= \underset{\text{first block}}{(K-1)} + \underset{\text{skips}}{\left(\frac{n}{K}-2\right)} + \underset{\text{last block}}{(K-1)} \text{ stages} \\
&= \left(2K + \frac{n}{K} - 4\right) \text{ stages}
\end{aligned} \tag{3.13}$$

Assuming that a straightforward 2-gate level implementation is used for both the RCA stage and skip block, then one stage will have $2\Delta_G$ gate delays. Equation 3.13 becomes

$$T_{\text{carry}} = \left(2K + \frac{n}{K} - 4\right) \cdot 2\Delta_G \tag{3.14}$$

Differentiating Equation 3.14 with respect to K and equating the resulting first derivative to 0 results in an optimal fixed block width of:

$$\frac{dT_{\text{carry}}}{dK} = \left(2 - \frac{n}{K^2}\right) \cdot 2\Delta_G = 0 \tag{3.15}$$

$$K_{\text{opt}} = \sqrt{\frac{n}{2}} \tag{3.16}$$

Therefore, for a 32-bit CSK, the best design will be eight blocks of width $K_{\text{opt}} = \sqrt{\frac{32}{2}} = 4$. This leads to a worst-case carry propagation of $24\Delta_G$ instead of $32 \times 2\Delta_G = 64\Delta_G$ for the 32-bit RCA. The fixed block-width CSK can be modified to a variable block-width CSK with multiple levels of skip logic associated with it to create an even faster circuit [38].

3.3.7 Conditional Sum Adders (COS)

The Conditional Sum Adder (COS) is a fast adder implementation with logarithmic speed-up [62, 73, 74]. The underlying principle of this architecture is the parallel computation of two sets of conditional sums and conditional carries for every bit position. To minimize the overall computation time, the given n bits are divided into smaller groups so that the serial carry propagation within the groups can be carried out in parallel. The COS approach is very similar to that of the CSL. The major difference is that in COS, the division of the n bits into sub-blocks continues until the extreme of having only single-bit adders if n is an integer power of 2. The COS scheme can still be

implemented even if n is not a power of 2 because sub-blocks of equal sizes are not compulsory. The operation of the COS can be further illustrated with the aid of the 4-bit COS depicted in Figure 3.22 [45, 75].

Figure 3.22 Schematic diagram of a 4-bit COS.

Figure 3.22 shows that the 4-bit COS makes use of two types of cells, namely the conditional cells and the MUXs. Each conditional cell consecutively generates two sums and two carries. One set of the results, S^0 and C^0 , assumes that the carry-in is a “0”, while the other set, S^1 and C^1 , is based on the assumption that the carry-in is a “1” [74]. Therefore, the block results will be ready for both carry conditions. The real sums are selected by the initial carry-in (C_0) and the carry-outs from the previous cells, which act as the control signals for the MUXs. One possible logic realization of the conditional cell is shown in Figure 3.23 [51].

Figure 3.23 Logic realization of the conditional cell.

3.4 A Proposed Low-Power High-Performance Carry-Select Adder

The CLA has long been the adder architecture of choice for time-critical high performance designs because of its logarithmic delay time. The logarithmic-depth parallel prefix CLA renders a superior speed performance but incurs an increase in area consumption [65]. On the other hand, the RCA provides a compact design but in the meantime suffers from a long delay time. In an effort to address the two contradictory factors, the CSL provides an attractive compromise between the CLA and RCA in terms of area usage and speed performance in CPA design. Therefore, the CSL has been deemed to be the appropriate candidate for incorporation in many high-end applications where speed, power, and area are of utmost importance. The square root CSL scheme as discussed in Section 3.3.3 is chosen in our adder design to achieve an optimized worst-case delay.

3.4.1 Existing Add-One Circuits based on Square Root CSL

As shown earlier in Figure 3.17, a typical square root carry-select adder consists of dual RCAs, one for $C_{in} = 0$ and the other for $C_{in} = 1$. It consumes more power due to the doubled amount of circuitry required to do the speculative addition where half of the replicated computation is redundant. On top of that, the extensive use of the ripple-carry method throughout the adder architecture seriously deteriorates the overall speed performance of the addition process. Henceforth, there is still ample room for improvement and an adder scheme that is able to overcome the area, power, and speed drawback is reasonable to expect. Several variants of the square root CSL based on an add-one concept have been reported in the literature, namely the Chang's CSL [76], Kim's CSL [77, 78], and Rawat's CSL [79].

The underlying principle of the add-one circuit is a complement scheme, which can be conceptualized as follows [76]. Suppose that $S^0 = (S^0_{n-1}, S^0_{n-2}, \dots, S^0_0)$ and $S^1 = (S^1_{n-1}, S^1_{n-2}, \dots, S^1_0)$ are the respective results of two RCAs with $C_{in} = 0$ and $C_{in} = 1$. Instead of using dual RCAs, which is inferior in terms of area and power efficiency, the

addition process based on the CSL scheme can be made simple by making use of the generated S^0 to further generate S^1 . By simply adding one to S^0 , the result will be S^1 .

It has been verified through careful observation that the S^1 can be generated based on the add-one concept, which is just inverting each S^0 bit starting from the least significant bit until the first zero is detected. Two examples for the lemma are shown in Figure 3.24. Before the first zero-bit is detected, all the less significant bits will be inverted (including the first zero bit itself). The inversion will be disrupted once the first zero is found, following which the remaining bits will be selected as it is. The 4-bit block representations of the Chang’s CSL, Kim’s CSL, and Rawat’s CSL using the add-one principle are shown in Figures 3.25, 3.26, 3.27, respectively. S denotes the sum, whereas i signifies the bit position of an operand. Meanwhile, C_{in} and C_o denote the carry-in and carry-out signals, respectively.

Figure 3.24 Examples showing the add-one principle.

Figure 3.25 Chang’s CSL architecture [76].

Figure 3.26 Kim’s CSL architecture [77, 78].

Figure 3.27 Rawat’s CSL architecture [79].

Even though the add-one adder architectures proposed in [76-78] successfully reduced the transistor count as compared to the conventional square root CSL, no effort has been made to significantly improve their power and speed performance. On the other hand, the circuit reported in [79] is superior to the conventional CSL from the power consumption point of view but is inferior in terms of area and speed performance. In view of the above scarcity, in this thesis, we propose a viable contender to its predecessors, which is an enhanced add-one adder architecture offering much better area-time-power efficiency.

3.4.2 Design of the Proposed Adder Architecture

This section proposes an enhancement of the conventional square root carry-select adder architecture and the aforementioned contemporary add-one circuits. This design offers significantly accelerated worst-case speed performance and minimized power dissipation with a relatively low hardware cost.

In contrast to the add-one circuits reported in [76-79], the RCA blocks with $C_{in} = 0$ in the new circuit are replaced by a variable block width Carry-Skip Adder (CSK) [21]

for bigger block size, typically 4 bits and above. This is because of the overhead of bypass structure in the CSK that makes it somewhat unattractive for lower-bit adders. A 4-bit block representation is singled out and displayed in Figure 3.28 to better illustrate its operation. The propagate signal is denoted as $P = A \oplus B$, where A and B are the single-bit operand to be added.

Figure 3.28 The proposed CSL architecture.

The CSK structure used in the new architecture is slightly different as compared to the traditionally known CSK [21]. Since the CSK resides individually in each of the blocks, any carry generated will terminate within the block and hence does not propagate to the next more significant blocks. In this way, the issue on the first and last block delay of typical CSK structure, which imposes additional delay penalty on the adder architecture if not properly optimized, is readily eliminated [80]. The skip logic of the CSK is composed of a select logic (2-to-1 MUX with inverted select) and its control element, which is a NAND gate. The incorporation of this 2-to-1 MUX with inverted select input removes an inverter delay for each block as compared to the common CSK design. The addition at the LSB is performed by a half adder instead of a full adder as the

C_{in} is a permanent zero. Furthermore, the propagate signal for the LSB, does not contribute to the select logic of the MUX and hence saving a few more transistors. In view of the above, the resource overhead of the bypass structure has been substantially minimized as compared to the conventional CSK design. The replacement of CSK for larger bits blocks exhibits worst-case delay performance superiority as compared to its ripple-carry counterpart.

Besides, all the RCA blocks with $C_{in} = 1$ are substituted by an add-one circuit, which is an efficient and modified design of the existing add-one circuit reported in [77, 78]. With this enhancement, the power consumption and silicon area requirement of the carry-select adder are considerably minimized. In the simulation process, it is observed that the schematic diagram given in [77, 78] contains an obscure error at the C_{out} selection for each block resulting in an incorrect operation. This error has been rectified to justify correct functionality.

As indicated clearly in Figure 3.35, the add-one circuit for each bit is implemented by the first zero finding circuit, viz. a pair of pMOS-nMOS devices. Since the FA14T full adders [60] used generates only a single sum output to the add-one circuit, the original add-one circuits (Kim's and Rawat's) require an inverter at each bit to generate the complement of the sum, $\bar{S}$. In the new design, however, $\bar{S}$ is produced intrinsically from the internal nodes of the pMOS-nMOS chains. This eliminates the use of an inverter for each sum bit and mitigates the number of fan-out from the full adders. It can be noticed that prior to detecting the first zero-bit, each pMOS-nMOS pair actually serves as an inverter. Thus, the complements of all bits before the first zero-bit including the first zero-bit itself, can be readily generated without the aid of any additional circuitry. The pMOS-nMOS chains no longer act as inverters after the first zero-bit is found. Nonetheless, this does not affect the sum bits after the first zero-bit in the add-one circuit because these sum bits no longer need to be inverted.

Buffers are added in every two FA cells for the purpose of speed optimization and logic level restoration. Another inverter delay is omitted for the LSB of each block by switching the V_{DD} and the GND on the first zero finding circuit of the add-one circuit reported in [77, 78]. Eventually, a chain of MUXs is placed at the bottom to select the actual sum, be it from the CSK ($C_{in} = 0$) or the add-one circuit ($C_{in} = 1$). The select logic

of each of these MUXs is composed by a NAND gate and an inverter. Meanwhile, the design structure of the proposed add-one circuit is implemented in a 64-bit adder architecture. The optimized block size configuration of the 64-bit realization is depicted in Table 3.3.

Table 3.3 Block size configuration of the proposed 64-bit square root CSL.

Block no.	10	9	8	7	6	5	4	3	2	1
Block size	12	11	9	8	7	6	4	3	2	2

3.4.3 Simulations and Performance Comparison

Extensive circuit simulations have been carried out to verify the circuit operation and characterize its performance in the vital aspects of power consumption, speed performance, transistor (xtrs) count, and silicon area requirement. The proposed 64-bit CSL architecture has been simulated together with both its driver and load, e.g. a pair of inverters at each of its inputs and outputs. This is a simulation environment, which is realistic to the actual circuit operational condition. The simulation results are obtained using the 0.18 μm CMOS technology from Chartered Semiconductor Manufacturing Pte. Ltd. (CHRT) at a power supply voltage of 1.8 V and an operating frequency of 50 MHz. The speed performance is gauged based on the worst-case delay, whereas the power dissipation is simulated based on 1024 combinations of randomly generated input data.

The proposed 64-bit square root carry-select adder is comparatively evaluated with four other types of adders, namely the conventional square root CSL, Chang’s CSL, Kim’s CSL, and Rawat’s CSL, in identical simulation conditions. Transistor size optimization for all architectures was carried out using an impartial and consistent strategy. Also, to ensure fair comparison, we have made use of the FA14T full adder as reported in [60] to build the core of all the aforementioned 64-bit adder architectures. The simulation results are tabulated in Table 3.4.

Table 3.4 Performance comparison of the various 64-bit square root CSL architectures using a 1.8 V/0.18 μm CMOS technology at 50 MHz.

64-bit CSL	Conv. CSL	Chang's CSL	Kim's CSL	Rawat's CSL	Proposed CSL (using FA14T)	Proposed CSL (using new FA14T)
Power, mW	1.056	0.934	0.920	0.979	0.781	0.635
Worst-case delay, ns	2.251	2.902	2.293	2.654	1.891	1.920
PDP, pJ	2.377	2.710	2.109	2.598	1.477	1.219
No. of xtrs	2216	1928	1968	2332	2110	2090
Area (normalized wrt Conv. CSL)	1	0.692	0.785	0.867	0.799	0.629

Based on Table 3.4, it is clear that the performance of the proposed CSL is superior to that of the preceding designs. The proposed circuit has the best power efficiency among all the circuits in comparison, rendering a 26%, 16.38%, 15.1%, and 20.22% enhancement as compared to the conventional, Chang's, Kim's, and Rawat's CSL circuits, respectively. On top of that, while the other existing add-one circuits display deteriorated worst-case delay relative to the conventional CSL, the worst-case speed performance is yet another noteworthy plus point offered by the new adder. To be more precise, it is 16% faster than the conventional CSL and 34.84%, 17.53%, and 28.75% faster than its other three contemporary counterparts, respectively. This speed advantage can be attributed to the exploitation of the CSK configuration in the CSL architecture. As for hardware requirement, the modified circuit requires slightly more silicon area as compared to Chang's and Kim's circuits. However, this drawback of the new circuit is overshadowed by its tremendous improvement in power efficiency, worst-case delay and PDP performances.

To further reduce the power dissipation, we have developed a full adder, which is almost identical to the FA14T [60] yet having an apparent decrease in power consumption while maintaining a fast worst-case delay measure. The new FA14T cell simply replaces the XOR in the original FA14T with an XNOR [61] of equivalent number of transistors and the interconnections are then modified accordingly. It has been verified that this amendment is favorable when we integrate the new FA14T into the new CSL architecture. It offers a power reduction to a greater extent without compromising the speed performance. The proposed square root CSL circuit with the new FA14T

alleviates the power consumption of the conventional, Chang's, Kim's, and Rawat's designs by a drastic 39.87%, 32.01%, 30.98%, and 35.14%, correspondingly. In the meantime, its speed performance remains the best among all the circuits in comparison. Its worst-case delay is only 85.3%, 66.16%, 83.73%, and 72.34% of those of the conventional, Chang's, Kim's, and Rawat's architectures, respectively. Moreover, despite having the same transistor count as the original FA14T, the new CSL configuration using the new FA14T promises a most substantial reduction in hardware cost, occupying only 62.9% of the silicon area of the conventional CSL. The layout of proposed CSL using the new FA14T has been drawn based on the 0.18 μm 6M1P n-well p-substrate CMOS design rules from CHRT and is shown in Figure 3.29. Also, the modified adder promises an impressive PDP, with an improvement of 48.72%, 62.73%, 42.2%, and 53.08% relative to the conventional and recent architectures, respectively.

3.5 Summary

This chapter provided a comprehensive and wide-ranging review of the development of the low-voltage low-power adder circuits. A myriad of eminent architectures of adder family, including the Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), and Carry Select Adder (CSL), to name a few, have been covered. Each of these adder architectures offers explicit compromises and tradeoffs in terms of area requirement, speed performance, and power consumption. For example, the RCA is particularly useful for applications where the area is of prime concern and the importance of high-speed is downplayed. On the other hand, the CLA offers a fast addition calculation at the expense of an overhead in hardware consumption. In applications where both silicon area and speed are the main design criterions, the CSL is an appropriate design choice, since it can be very fast while sustaining a considerably low area usage.

A high-performance low-power 64-bit square root CSL based on an add-one concept is proposed in this chapter. It substitutes the dual ripple-carry adders in the conventional CSL with variable block size carry-skip adders for zero carry-ins, and modified add-one circuits for one carry-ins. The proposed adder has been extensively

simulated and analytically compared with four other architectures, namely the conventional CSL, Chang's CSL, Kim's CSL, and Rawat's CSL using a 1.8 V/0.18 μm CMOS process from CHRT. The simulation results show that the proposed adder outperformed the other adders in comparison in terms of power dissipation, worst-case delay, and also Power-Delay Product (PDP) with relatively low hardware cost. For example, it promises an improved 48.72%, 62.73%, 42.2%, and 53.08% PDP when compared to the conventional square root carry-select adder, Chang's CSL, Kim's CSL, and Rawat's CSL, respectively. These salient attributes of the proposed square root CSL are attractive for use in today's DSP systems, which are required to perform complex and computationally intensive signal processing tasks at speeds suitable for real-time operation with the lowest possible power consumption. In view of that, it is a viable contender to replace the conventional CSL and contemporary add-one CSL circuits.

Figure 3.29 Layout of the proposed CSL.

Chapter 4

Low-Power Continuous-Time CMOS Current Comparator

4.1 Introduction

In today's state-of-the-art VLSI technology, the common approach used in the design of arithmetic circuits is the voltage-mode operation for both digital and analog parts of the chip. However, due to the emerging challenge of realizing efficient VLSI CMOS high-end integrations, such as advanced handheld gadgetry, photo sensors and artificial neural networks, there has been rekindled interest in reducing the area complexity of the processing elements, where Current-Mode Multiple-Valued Logic (CMMVL) circuits can be exploited to manage the complex interconnections in these applications [81-85]. Apart from that, the switch to current-mode approach is further motivated by higher speed performance, larger bandwidth and lower voltage requirements when compared to its voltage-mode counterpart [86].

It is well known that the binary number system is a logical and dominant choice for conventional voltage-mode design of digital computers. However, there are also significant drawbacks of binary numbers in traditional system implementations. For instance, in a typical VLSI circuit, about 70% of the chip area is occupied by interconnection, 20% by insulation and the remaining 10% is devoted to the devices [82]. Interconnection occupies a large portion of the physical area even when it is not in use. Thus, the interconnection would be used more efficiently if several levels of logic were to be injected into a single wire, as in the Multiple-Valued Logic (MVL). MVL requires more than two discrete levels of logic signals that are better represented in Current Mode (CM) by specific current values, hence resulting in the birth of the Current-Mode Multiple-Valued Logic (CMMVL) [87, 88]. The exploitation of this design technique with the proper choice of numerical representation of numbers and current levels will

inevitably lead to a low-power and high-speed VLSI circuit with increased packing density. The beauty of CMMVL design is that it can add two currents by simply wiring them into a common node.

Another difficulty encountered by the conventional VLSI design method is the pin-out problem, which is interconnection outside the chip. Here, metal pins are required to transport information. Due to strength and reliability issues, there is a minimum dimension for the metal pins. This, in turn, imposes limitations on the structure to support the pin, and hence places restrictions on the number of pins available. This is another implementation where the CMMVL approach is advantageous since the CMMVL requires less number of external pins due to a lower number of data wires.

A typical example of the CMMVL system is depicted in Figure 4.1 [81, 83]. The MVL arithmetic operation can be performed in a simple way by interconnecting some CM basic blocks. The chip level embraces CM blocks such as memories, CMMVL multipliers and neural networks, while each CM chip consists of functional blocks such as the CMMVL adder. At the basic level of the hierarchical structure, there are four elementary blocks, namely, Current Comparator (CC), Current Mirror (CMi), Current Source (CS), and Voltage Switched Current Source (VSCS).

Figure 4.1 Hierarchy of the CMMVL system.

Before we proceed to describe the current comparators used in CMMVL, we discuss one of the important functional blocks of the CMMVL system, namely, the adder.

One of the adders described in this section will incorporate the proposed design of the area-efficient current comparator circuit. To ensure efficient and competent design of adders in CMMVL, the main criteria to be considered are the numerical representation of numbers and unit current step per logic level [81, 83]. A 4-digit decimal adder that can be used to perform addition operation for two 4-digit decimal numbers, A and B , where $A = \{A_0, A_1, A_2, A_3\}$ and $B = \{B_0, B_1, B_2, B_3\}$, is shown in Figure 4.2 [83]. Each digit of the decimal 10-digit set (0, 1, ..., 8, 9) is represented by one of the ten possible current levels, 0 μA , 1 μA , ..., 8 μA , or 9 μA , with a unit current step of 1 μA . To facilitate the illustration of this circuit, the current levels of A and B are denoted by $\{a_0, a_1, a_2, a_3\}$ and $\{b_0, b_1, b_2, b_3\}$, respectively.

The 4-digit decimal adder comprises four Single-Digit Decimal Adders (SDDAs). It can be further extended to an n -digit decimal adder by using n SDDAs in the implementation. There is an inherent carry propagation path from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). However, a simple wiring connection with the inputs of the subsequent SDDA performs the addition of C_{out} to its adjacent digit, which is an extra feature of the CM circuits.

Figure 4.2 Block diagram of a 4-digit decimal adder.

The SDDA structure is illustrated in Figure 4.3. The input current I_{in} to the SDDA cell is the sum of a_i , b_i and carry-out, C_{out} , with i ranging from 0 to 3. C_{out} is either 0 μA or 1 μA , representing a decimal 0 or 1, respectively. As a result, I_{in} is in the range from 0 μA to 19 μA , with a unit current step of 1 μA . This suggests that the SDDA cell has a resolution of 20 levels to distinguish 20 different levels of the input current I_{in} . The SDDA implements the partial sum, S_{out} , and carry-out, C_{out} , as described by Equations 3.18 and 3.19, respectively:

$$S_{out} = \begin{cases} I_{in} & ; (I_{in} \leq 9) \\ I_{in} - 10 & ; (I_{in} \geq 10) \end{cases} \quad (4.1)$$

$$C_{out} = \begin{cases} 0 & ; (I_{in} \leq 9) \\ 1 & ; (I_{in} \geq 10) \end{cases} \quad (4.2)$$

Figure 4.3 The structure of the SDDA cell.

The SDDA cell consists of a Current Comparator (CC) and five current mirrors. Two of the current mirrors are of the super MOS transistor type (n-type ST_n and p-type ST_p), whereas the other three are high-swing cascoded current mirrors (n-type HS_n and p-type HS_p). The schematic diagrams of the n-type ST current mirror, together with its super nMOS transistor, are depicted in Figure 4.4, while Figure 4.5 depicts the n-type high-swing cascoded current mirror.

Figure 4.4 (a) Current mirror with super nMOS transistor.
(b) Super nMOS transistor.

Figure 4.5 The n-type high-swing current mirror.

By referring to Figure 4.3, the addition of the two decimal numbers, A and B , is first carried out by wiring the currents of the respective digits into the common node, I_{in} , which then passes through ST_n and hence two identical duplications of I_{in} are generated. One copy propagates to the node X , while another copy goes to the CC. Here, I_{in} will be compared with the reference current ($I_{ref} = 9.5 \mu A$), previously set by HS_n . If I_{in} is lower than I_{ref} , switches $sw1$ and $sw2$ will stay open. Consequently, the output signals $S_{out} = I_{in}$ and $C_{out} = 0$. On the other hand, if I_{in} is higher than I_{ref} , both of the switches will be turned on, hence connecting the $10 \mu A$ constant current source to node X and the $1 \mu A$

constant current source to C_{out} via HS_{p1} and ST_p , respectively. As a result, the output signals will be $S_{out} = I_{in} - 10 \mu A$ and $C_{out} = 1 \mu A$.

Another implementation of the CMMVL adder is a Positive-Digit Adder (PDA), which uses the redundant Positive-Digit (PD) number representation. This number system has the potential to lead to high-speed parallel computer arithmetic due to the fact that the carry-ripple effect does not exist in the scheme, which implies that the time required for the arithmetic operations is independent of the word length. This is because different arrangements of digits correspond to the same value, resulting in the term “redundant” number [82]. Generally, the basic CM circuits may require longer execution time to perform a single-bit operation as compared to the conventional voltage-mode circuits. Nonetheless, by exploiting the attractive feature of the PD number system, it can result in equal or even faster execution time of the multiple-bit addition, multiplication and other arithmetic algorithms.

The PD number scheme makes use of three prominent steps [82] to eliminate the carry propagation chain. We consider the addition of two operands $A = \{A_{n-1}, A_{n-2}, \dots, A_2, A_1, A_0\}$ and $B = \{B_{n-1}, B_{n-2}, \dots, B_2, B_1, B_0\}$ using the radix-2 PD number algorithm. Here, A_i is in the range of 0 to 3, and the same goes for B_i .

Step 1: Generate a linear sum, Z_i , by adding up A_i and B_i linearly.

$$Z_i = A_i + B_i \quad (4.3)$$

where $Z_i \in \{0, 1, \dots, 5, 6\}$.

Step 2: Generate two carry values, C_i^1 , C_i^2 , and another intermediate sum, W_i , from Z_i , that satisfy the following equation:

$$4 \bullet C_i^2 + 2 \bullet C_i^1 + W_i = Z_i \quad (4.4)$$

where C_i^1 , C_i^2 and $W_i \in \{0, 1\}$.

C_i^1 , C_i^2 and W_i are the 3-bit standard binary number representation of Z_i , with W_i being the LSB and C_i^2 the MSB. C_i^1 and C_i^2 , respectively, will go to the next higher digit positions, while W_i will be added with the C_{i-1}^1 and C_{i-2}^2 from the lower digit positions. In other words, these three bits are arranged in such a way that they are extending diagonally up and to the right.

Step 3: Generate the final sum by the following equation:

$$S_i = C_{i-2}^2 + C_{i-1}^1 + W_i \tag{4.5}$$

Assuming the initial $C_{in} = 0$, an example of the PD two-operand addition is tabulated in Table 4.1.

Table 4.1 The addition procedure for a two-operand PD number system.

Augend A			2	1	0	3	2	1	Decimal $A = 97$
Augend B			1	0	2	3	3	1	Decimal $B = 67$
Z_i			3	1	2	6	5	2	
W_i			1	1	0	0	1	0	
C_i^1		1	0	1	1	0	1	0	
C_i^2	0	0	0	1	1	0	0	0	
S_i	0	1	1	3	2	0	2	0	Decimal $S_i = 164$

Define a_i as the current representation of A_i , and the same goes for b_i , z_i , c_i^2 , c_i^1 , w_i and s_i . The block diagram of the PDA operation based on the radix-2 PD number representation is depicted in Figure 4.6 [81, 82, 89]. Steps 1 and 3 are easily performed by wiring the current signals to the common nodes, while step 2 is executed in block labeled “PDA”. The PDA cell that integrates an operational block with a unit current step of 11 μA , which is capable of distinguishing seven levels of input signals corresponding to the seven possible values of Z_i , has been designed and fabricated using CMOS 0.8 μm technology. The schematic configuration of the PDA cell is portrayed in Figure 4.7 [81, 83]. The PDA cell actually serves as a binary number converter. As described in Equation 4.4, the cell converts z_i to c_i^1 , c_i^2 and w_i , represented by either 0 μA or 12 μA .

Figure 4.6 Block diagram of PDA using the radix-2 PD number representation.

Figure 4.7 The CMMVL PDA cell.

Lying at the heart of a CMMVL circuitry is the current-mode comparator. It serves as a current threshold detector to discriminate various input current levels [84]. The current-mode comparator receives an input signal, in the form of a current, and compares it with its own threshold current. The result of the comparison is in the form of an output voltage.

A myriad of CMOS current-mode comparators have been proposed in the literature to-date [87, 90-97]. However, most of these circuits [90-95] have made a straightforward assumption, where the input current is often considered as the subtraction or discrepancy between a threshold current and an actual input current signal. They produce a two-level output voltage in response to the polarity of the input currents, rather than performing current detection based on a pre-defined value of the threshold current. Moreover, the circuit structure that realizes such current subtraction, which is an imperative entity of the current comparator, is not illustrated in these designs. We denote the actual input current as I_{in0} and the difference between I_{th} and I_{in0} as I_{in} throughout the remainder of this chapter. We will first discuss the existing designs of the current comparators without current subtraction entity, followed by the current comparator designs with the incorporation of current subtraction feature. Most importantly, in an effort to address the absence of a competent current subtraction component in the literature, we will propose a low-power area-efficient current comparator design towards the end of this chapter.

4.2 Current Comparators without Current Subtraction

4.2.1 Traff's Current Comparator

Traff's current comparator, as shown in Figure 4.8, has a source follower input buffer (M1 and M2) with low input impedance of approximately $\frac{1}{g_m}$ and an output CMOS inverter stage (M3 and M4) [90]. The input current I_{in} denotes the result of the subtraction of a threshold current from the signal current. When I_{in} is positive, node X is pulled high and node Y pulled low, thus turning M1 off and M2 on. At this point of time, node X is in low impedance state, since I_{in} is supplied by M2. When I_{in} changes its

polarity, there is an inadequacy in the gate drivability for the buffer to supply I_{in} , hence rendering node X a temporarily high impedance node. When I_{in} is negative, node X is low and node Y is high, turning M1 on and M2 off. This again causes node X to have low impedance.

The source follower structure provides the ability to apply positive voltage feedback to the gates. The feedback effect from the output CMOS inverter stage is then exploited to attain sufficient gain for amplifying the small voltage variation at the input node. The low input impedance feature of this structure allows simpler current mirrors to be incorporated to provide current subtraction to the input node. Additional stages of CMOS inverters are cascaded at the output stage to ensure rail-to-rail swing. Graphs showing the waveforms of the input, output and the second additional CMOS stage voltage signals and input current signal are depicted in Figure 4.9. One disadvantage of Traff's current comparator is that the input voltage of the CMOS output inverter does not exhibit rail-to-rail swing, thus causing neither M3 nor M4 to be completely off. Consequently, the quiescent current flowing through the output stage will cause a nonzero DC power dissipation. Besides, this approach shows the existence of a deadband region during input transition period where the input impedance is relatively high, thereby slowing the speed of operation. This effect is particularly significant when the input current is scaled down.

Figure 4.8 The Traff's current comparator.

Figure 4.9 (a) The voltage signals at the input, output and second additional CMOS stage. (b) Input current.

4.2.2 Deadband-Alleviated Current Comparator

As discussed earlier, Traff's current comparator experiences a deadband region due to the high input impedance during an input transition. The size of the deadband region is determined by the threshold voltages, V_{th} of M1 and M2. A lower V_{th} is preferable to achieve faster response times. To circumvent the deadband region issue, M1 and M2 can be biased in class AB configuration, with their gate-source voltages denoted as V_{b1} and V_{b2} , respectively, as presented in the deadband-alleviated current comparator [91]. The deadband of the buffer reduces correspondingly when V_{b1} and V_{b2} are increased towards V_{th1} and V_{th2} , respectively. This phenomenon results in smaller voltage fluctuations at nodes X and Y, thus causing an improved performance.

The absolute magnitude of V_{th} is not a well-determined parameter in process technology. Following that, the circuit is designed in such a way that V_{b1} and V_{b2} are set by the threshold voltages from other MOS devices, namely Mb1 and Mb2, as illustrated in Figure 4.10. Since the body-source voltages of Mb1 and Mb2 are less than those of M1 and M2, their threshold voltages are also lower due to the body effect. At this stage, there is still a small amount of deadband in the transfer characteristic of the buffer. Further adjustment can be made by carefully setting the current sources I_{b1a} , I_{b1b} to bias Mb1

and I_{b2a} , I_{b2b} to bias M_{b2} . Due to the fact that node Y has a reduced voltage swing, three inverting stages (instead of two as in Traff's circuit) are concatenated at the output to provide sufficient voltage gain. A significant plus point of this design is that its speed-to-power ratio is increased at low input currents. However, this is achieved at the expense of an increased complexity and higher power dissipation as compared to Traff's current comparator. Process variations impose immense impact on the comparator because its performance is closely related to the values of the four current sources. Other than that, a twin-well CMOS technology is necessitated for this design since the body of the biasing transistors, M_{b1} and M_{b2} is connected to the source, rather than connected to ground or V_{DD} .

Figure 4.10 The deadband-alleviated current comparator.

The deadband-alleviated and Traff's current comparators have been simulated based on a 5 V/1.6 μm CMOS technology [91]. Figure 4.11 portrays the speed comparison for a range of input currents. The speed enhancement is most noteworthy for low input currents. As for high input currents, the speed performance is determined primarily by the propagation delay of the MOS transistors rather than the time taken for nodes X and Y to swing through the deadband region.

Figure 4.11 The speed performance of the deadband-alleviated current comparator and the Traff's current comparator [91].

4.2.3 Simple Current Comparator

In view of the high-complexity solution of the deadband-alleviated current comparator to the shortcoming of the Traff's circuit, a current comparator with a substantially simpler topology has been proposed as an alternative contender offering comparable performance [92]. The schematic diagram of the simple structure is shown in Figure 4.12. Two additional devices operating in diode configuration, M5 and M6, have been incorporated to the original Traff's circuitry to shift up the gate voltage of M1 and shift down the gate voltage of M2 relative to the output voltage, V_{out} . By carefully sizing M5 and M6, input transistors M1 and M2 can at most reach the limit of the off-state threshold, which is the optimal operating condition, without entering the deep sub-threshold region. In this way, the input buffer will instantaneously follow any variations of the input current, hence improving the speed of the current comparator. However, because there is an inevitable deterioration in the output signal, four inverting stages are required to attain rail-to-rail output voltage swing.

Figure 4.12 The simple CMOS current comparator.

Together with the Traff's and the deadband-alleviated current comparator, the simple current comparator has been simulated using 5 V/2 μm CMOS technology to validate and evaluate their performance [92]. The average response time of the three designs with respect to a range of square-wave input current is pictured in Figure 4.13.

Figure 4.13 The speed performance of the simple, deadband-alleviated and Traff's current comparators [92].

As can be seen, the performance of the simple topology is comparable to that of the deadband-alleviated circuit and much faster than the Traff's design at low input currents. Nonetheless, this speed advantage does not persist for higher input current. This is because the enhanced voltage swing due to the increased current magnitude completely turns off M1 and M2. This recurrence of the Traff's problem can be overcome by simply reducing the aspect ratios of M5 and M6 for higher input currents.

4.2.4 Current Comparator using Resistive Feedback

The circuitry of the current comparator based on a resistive feedback network is shown in Figure 4.14 [93]. It comprises a three-stage current-source inverting amplifier and a CMOS inverter as the output stage. In contrast to the deadband-alleviated current comparator, this design exhibits good process immunity. The bias current I_{bias} and the input resistance are well-controlled parameters. The resistive feedback element MR is introduced in the first stage current-source inverting amplifier to circumvent the problem of high output resistance inherent in current-source inverting amplifiers, without which this large output resistance limits its use for high-speed environments, especially for capacitive loads. Other than reducing the output resistance, transistor MR is also included to reduce the input resistance. The decreased input and output resistances cause small voltage fluctuations at nodes X and Y , and hence faster response times in the subsequent inverting amplifiers.

Figure 4.14 The current comparator using resistive feedback network.

The current comparator using the resistive feedback configuration has an intrinsic auto-zeroing feature that does not require any offset compensation techniques. This is because the DC operating points of the inverting amplifiers can be set to the same value by using the same nMOS and pMOS devices, hence resulting in negligible offset with zero input current level.

The resistive feedback and Traff's current comparator were simulated using a 0.35 μm CMOS technology at $V_{DD} = 3\text{ V}$ and $I_{bias} = 50\text{ }\mu\text{A}$ for square-wave input current ranging from $\pm 0.01\text{ }\mu\text{A}$ to $\pm 10\text{ }\mu\text{A}$ [93]. Their respective speed performance is graphically illustrated in Figure 4.15. For current levels $< 10\text{ }\mu\text{A}$, the response time increases when the input current reduces. For high input current levels, the response time no longer depends on the time taken for nodes X and Y to apply negative feedback to the gate of the common-source MOS transistor of the first inverting amplifier. Rather, it is determined mainly by the propagation delay of the subsequent stages of current-source inverting amplifiers. An increased I_{bias} tremendously enhances the speed performance of the resistive feedback current comparator, owing to the increased output current of the current-source inverting amplifier, which can provide sufficient charging current required to meet the transient response specifications. A large I_{bias} is also necessary for high-resolution applications, with an unavoidable increase in power consumption.

Figure 4.15 The speed performance of the resistive feedback and Traff's current comparators [93].

4.2.5 Robust Current Comparator

A robust current comparator with enhanced speed-to-power ratio as compared to the previously reported designs is presented in this section [94]. Its schematic diagram is shown in Figure 4.16. It makes use of one CMOS complementary amplifier, M1 and M2, two resistive-load amplifiers, M6-M9 and two pairs of CMOS inverters, M10-M13. M3 and M4 are included to reduce the operating current since both M1 and M2 work in the saturation region. The device M5, which establishes a negative feedback effect of the input CMOS complementary amplifier, operates in triode region. The small input and output resistances of this design reduce the voltage fluctuations at nodes *X* and *Y*, rendering a greatly decreased response time. Following that, two resistive-load amplifiers are cascaded to supply additional gains to amplify the small voltage variation at node *Y*. Finally, the two CMOS inverters provide a rail-to-rail voltage at the output node. Process variation immunity of this current comparator is improved since there is no incorporation of any external biasing currents and voltages.

Figure 4.16 The robust current comparator.

Performance evaluation and comparison based on a 3 V/1.2 μm CMOS technology have been carried out on the robust current comparator and its other counterparts discussed in the previous sections [94]. Figure 4.17 displays the average speed performance of each of the designs with square-wave input currents ranging from $\pm 0.01 \mu\text{A}$ to $\pm 10 \mu\text{A}$. For low input current levels, the robust current comparator is the fastest among all other design techniques. Its response time is very much lower than that of the Traff's circuit and slightly better than the deadband-alleviated and resistive feedback circuits. When the input current is increased to $10 \mu\text{A}$, the four response times converge to practically the same value because the delay time is predominated by the propagation delay of the amplifier stages, instead of the time required for the signal to propagate through the negative feedback network.

Figure 4.17 The speed performance of the various designs of current comparator [94].

Even though the response time of the robust current comparator is comparable to those of the deadband-alleviated and resistive feedback circuits, it promises a certain reduction of power dissipation. Figure 4.18 shows the power dissipation of the four current comparators with respect to the range of square-wave input current levels. It can be observed that the Traff's comparator dissipates the least amount of power. However, this is attained at the cost of a much higher delay time for small input current levels due to its much larger voltage swing. As for the other three comparators, their power consumption are almost identical when the input current is $0.01 \mu\text{A}$. When the input current goes higher, the power dissipation of the resistive feedback circuit remains at almost the same value, since its bias current stays constant even with the change in input current because of the use of the current-source inverting amplifiers. Meanwhile, the power dissipation of the deadband-alleviated and the robust current comparators experience a steep decrease with the increase in input current level. When the input current is $1 \mu\text{A}$, the speed-to-power ratio of the robust current comparator is 127% and 177% over those of the deadband-alleviated and the resistive feedback current comparators, respectively.

Figure 4.18 The power consumption of the various designs of current comparator [94].

4.2.6 Low-Input Current Comparator

The CMOS current comparator introduced in this section addresses the scarcity in speed performance degradation suffered by the earlier discussed current comparators when operating at very low input current, i.e. below 1 μA . Figure 4.19 depicts the circuit structure of the low-input current comparator [95]. Instead of using two diode-connected MOS devices as in the simple current comparator reported in Section 4.2.3, this comparator design makes use of one such device to supply for the voltage drop between the gates of M1 and M2. Because M4 always works in the saturation region, its $(V_{\text{gs}} - V_{\text{th}})$ value is proportional to the square root of the current flowing through M3, M4 and M5. Since I_{in} is very small, the variations of current and $(V_{\text{gs}} - V_{\text{th}})$ of M4 are also considerably small. Therefore, the input resistance is approximately $\frac{1}{g_{m1} + g_{m2}}$, which is substantially smaller than that of the conventional Traff current comparator. The purpose of connecting the drain and the source of M4 to the gates of M7 and M6, respectively, is to more rapidly discharge and charge the gates of M8 and M9. Transistors M8-M11 are cascaded to realize full voltage swing at the output. Individually manipulated by constant

voltages V_p and V_n , MP and MN are integrated to adjust the threshold voltage of the inverter M8-M9 to ensure that the comparator is feasible at all process corners.

Figure 4.19 The low-input current comparator.

The low-input current comparator has been simulated together with the Traff's and the resistive feedback current comparator based on a $0.35\ \mu\text{m}$ CMOS technology at $V_{DD} = 3\ \text{V}$ with square-wave input current levels varying from $\pm 0.001\ \mu\text{A}$ to $\pm 10\ \mu\text{A}$ [95]. Figure 4.20 and Figure 4.21 show graphically the response time and the average power dissipation versus the input current levels of the circuits in comparison, respectively. It can be seen that the low-input comparator exhibits the fastest speed performance for input current $< 1\ \mu\text{A}$. However, it is inferior to the Traff's comparator in terms of power computation. A further performance evaluation using the PDP shown in Figure 4.22 suggests that it is the most promising for low input current levels.

Figure 4.20 The speed performance of the various designs of current comparator [95].

Figure 4.21 The average power dissipation of the various designs of current comparator [95].

Figure 4.22 The PDP comparison of the various designs of current comparator [95].

4.3 Current Comparators with Current Subtraction

4.3.1 Conventional CMOS Current Comparator

Figure 4.23 shows the conventional CMOS current-mode comparator [87]. It includes the threshold current (I_{th}) generation circuit, which is made up of transistors MP1 and MN1, the mirror pMOS MP2 that produces a replica of I_{th} , the input nMOS MN2 in a diode-connected configuration, and its mirror transistor MN3. The discrepancy between I_{th} and the input current, I_{in0} , either becomes the charging current for the output capacitive load, C_L , if the former is greater than the latter, or the discharging current, if the opposite is true. As a result, the output voltage, V_{out} , will rise to a ‘high’ logic level if I_{in0} is less than I_{th} , and vice versa.

Figure 4.23 The schematic diagram of the conventional CMOS current-mode comparator.

The expression for I_{th} is derived as follows. By equating the saturation currents of MP1 and MN1, their gate potential, V_G , is given by Equation (4.6a).

$$V_G = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{K_{MN1}}{K_{MP1}}} V_{tn}}{1 + \sqrt{\frac{K_{MN1}}{K_{MP1}}}} \quad (4.6a)$$

where V_{DD} denotes the power supply voltage, while $|V_{tp}|$ and V_{tn} stand for the pMOS and nMOS threshold voltage, respectively. K is the device parameter defined by

$$K_{MN1} = \frac{1}{2} \mu_n C_{ox} \frac{W_{MN1}}{L_{MN1}} \quad (4.6b)$$

$$K_{MP1} = \frac{1}{2} \mu_p C_{ox} \frac{W_{MP1}}{L_{MP1}} \quad (4.6c)$$

where μ_n represents the electron mobility in the induced n channel, μ_p symbolizes the mobility of holes in the induced p channel, C_{ox} (oxide capacitance) is the capacitance per unit area of the gate-to-body capacitor for which the oxide layer serves as the dielectric [98], L is the channel length, and W is the channel width for the respective MOSFETs.

In general, I_{th} (for a long-channel device) is represented by

$$I_{th} = K(V_{GS} - V_{th})^2 \quad (4.7)$$

where V_{GS} is the gate-source voltage, and V_{th} is the threshold voltage of the transistor. More specifically, by substituting Equation (4.6a) into Equation (4.7), I_{th} is related to the dimensions of MP1 and MN1, and V_{DD} , by

$$I_{th} = I_{DMN1} = K_{MN1} \left(\frac{V_{DD} - |V_{tp}| + \sqrt{\frac{K_{MN1}}{K_{MP1}}} V_{tn}}{1 + \sqrt{\frac{K_{MN1}}{K_{MP1}}}} - V_m \right)^2 \quad (4.8)$$

$$= \frac{K_{MN1}}{\left(1 + \sqrt{\frac{K_{MN1}}{K_{MP1}}}\right)^2} (V_{DD} - |V_{tp}| - V_{tn})^2$$

This conventional current comparator has a major drawback, which is its inability to offer a small-area feature when I_{th} is low due to the constraint of the minimum channel width. When I_{th} is low, the area of the comparator is necessarily large, since the aspect ratio will be less than 1 as shown by the Cadence Spectre simulation for low I_{th} . This implies that in order to achieve a low I_{th} , the channel length has to be scaled up proportionately. This will inevitably increase the area consumption of the circuit. As area is one of the most fundamental and critical design parameters to ensure optimum performance, the new current-mode comparator will be a plausible solution to this problem.

4.3.2 Chunyan's CMOS Current Comparator

The schematic diagram of Chunyan's current comparator is depicted in Figure 4.24 [96]. This circuit requires gated control for an additional step, which is implemented by switch K for I_{th} set-up. This is in contrast to our proposed comparator, which realizes an efficient current-to-voltage conversion based on I_{in0} and I_{th} comparison in merely one step. Our proposed comparator design will be presented in Section 4.4 of this chapter. The operation of Chunyan's current comparator commences with the setting up of I_{th} . The input current, I_{in0} is mirrored to I_2 with a certain gain coefficient. The initially closed switch K causes I_2 to be equal to I_3 when equilibrium is reached. The output voltage, V_{out} is set to a virtual value of half- V_{DD} . After I_{th} is attained, switch K is opened and the

established gate voltage of MP1 is retained. At this stage, normal current comparison between I_{in0} and I_{th} , as explained in Section 4.3.1 on the conventional current comparator is carried out. The transistors MP4 and MN1, individually controlled by constant voltages V_p and V_n , are integrated to set the operating points of MP1 and MN3 at equilibrium, without which a substantially small $|I_{in0} - I_{th}|$ may cause V_{out} to end up in an indiscernible level. This indispensable inclusion of MP4 and MN1 for proper functionality will undoubtedly add to the intricacy and complexity of the design, not to mention area consumption.

Figure 4.24 Schematic diagram of Chunyan’s current-mode comparator.

4.3.3 Low-Input Impedance Current Comparator

This section reports on the design of a low-input impedance current comparator with a complete circuitry, which performs current subtraction between I_{th} and I_{in0} , and also voltage amplification at the output to achieve rail-to-rail swing. Its schematic diagram is shown in Figure 4.25 [97]. The utilization of an enhanced Wilson current mirror, M1-M4 in this circuit is two-fold: firstly to carry out a current subtraction

between I_{th} and I_{in0} , and secondly to reduce the input impedance of the circuit by applying negative feedback within the current mirror itself. The device M5 is a diode-connected load, whereas transistors M6-M11 form the three resistive-load common-source amplifiers for voltage amplification at node Y and transistors M12-M15 are two CMOS inverters used to attain rail-to-rail voltage swing at the output node. This design of the current comparator has low input impedance due to the effect of negative feedback in the modified Wilson current mirror.

When I_{th} flows to M1, the drain current of M2 and M4 will be the same if their aspect ratios are identical. The output current, I_{out} (or I_{in} as reported in other literatures), is the result of the subtraction between I_{th} and I_{in0} . If the value of I_{in0} is increased and larger than I_{th} , I_{out} will be reduced hence pulling up the voltage at node Y . On the other hand, if I_{in0} is reduced and smaller than I_{th} , the resultant I_{out} increases and pulls down the voltage at node Y .

Figure 4.25 The low-input impedance current comparator.

Circuit simulations based on a 3 V/0.5 μm CMOS technology have been performed on the low-input impedance current comparator, and also the robust, resistive feedback and Traff's current comparators that have been discussed in the preceding sections [97]. Figure 4.26 shows the response time versus an input current range from $\pm 0.01 \mu\text{A}$ to $\pm 10 \mu\text{A}$ for the comparators. The speed performance of the low-input

impedance current comparator is much superior than the circuit proposed by Traff and is comparable to its other counterparts. However, something worth-mentioning here is that the delay time of the robust, the resistive feedback and the Traff's circuit does not include the delay contributed by the current subtraction circuit, which is an indispensable entity of a complete current comparator. Likewise for the power dissipation comparison as depicted in Figure 4.27, the average power computation of the robust, the resistive feedback and the Traff's circuit ignored the current subtraction part, which, needless to say, contributes a certain amount of additional power consumption. In this case, the low-input impedance comparator dissipates a power comparable to that of the robust circuit, and much higher than the other two circuits in comparison. The graph on the input impedance with respect to the input current is shown in Figure 4.28. As its name suggests, it can be observed that the input impedance of the low-input impedance comparator is the lowest among all other designs from $\pm 0.01 \mu\text{A}$ to $\pm 10 \mu\text{A}$.

Figure 4.26 The comparison on speed performance of different current comparators [97].

Figure 4.27 The comparison on power dissipation of different current comparators [97].

Figure 4.28 The input impedance comparison of different current comparators [97].

4.4 A Proposed Area-Efficient CMOS Multiple-Valued Current Comparator Circuit

4.4.1 Overview

In the present state-of-the-art VLSI technology, the need to develop customized circuits to suit varying operating environments and specifications is escalating. An area-efficient current-mode comparator, which is based on the modifications of the conventional CMOS current comparator, is proposed. It has been verified by circuit simulations using the 0.25 μm , 0.18 μm , and 0.13 μm CMOS technology from Chartered Semiconductor Manufacturing Pte. Ltd (CHRT) that the proposed design acts as a viable contender in replacing the conventional current comparator for low threshold current (I_{th}) levels. A low I_{th} is generally more favorable than a higher I_{th} as it tends to dissipate low static power. A more assuring and promising fact is that the area advantage becomes more significant with reducing feature size/technology. This attribute blends well with the contemporary and ongoing process technology miniaturization.

The proposed small-area low current comparator can be utilized in applications using current-mode approach such as the Analog-to-Digital (A/D) converters, arithmetic-intensive circuitry and VLSI neural network [83, 89, 99, 100]. In addition, it can also be incorporated to detect weak current signals in temperature sensors and photo sensors generating very small current. These applications are characterized by massively interconnected homogeneous Processing Elements (PEs), where CMMVL can be exploited to efficiently manage the complex interconnections and circumvent the limited pin-out problem. Lowering the area of the current comparator of the CMMVL circuit leads to compact PEs and a significant area reduction of the overall die size for these applications.

A number of CMOS current comparators have been reported in the preceding sections. However, as discussed earlier, most of these circuits produce a two-level output voltage in response to the polarity of the input currents, which is in contrast to the actual behaviour of a current comparator, which performs current detection based on a pre-defined value of the threshold current. In other words, the input current of these circuits is often considered as the subtraction or difference between a threshold current and an

actual input current signal. The circuit structure that realizes such subtraction is not illustrated. In view of that, we have designed a proficient current subtraction circuit to overcome the aforesaid deficiency. The proposed design has been compared with its closest counterparts in relation to the current detection scheme, namely the conventional circuit and Chunyan's circuit in terms of area, power and delay. On top of that, to provide a more coherent and lucid circuit evaluation, each current-mode comparator design has been implemented into a one-stage Positive-Digit Adder (PDA), which is an illustrative example of the CMMVL circuits at 1.8 V/0.18 μm CMOS technology. The PDA utilizing the new current comparator occupies a silicon area of only 40.2 μm^2 , which is only 77.2% and 22.6% of those of the conventional and contemporary circuits, with a power-delay product improvement of 7.3% and 70.4%, respectively.

4.4.2 Design of the New Current-Mode Comparator

From Equation (4.7) of Section 4.3.1, it is observed that the threshold current can be reduced substantially by decreasing the V_{GS} . This intuitive observation is translated into practice by introducing the new current-mode comparator, which incorporates an nMOS in series with, or beneath the original threshold generation circuit. Figure 4.29 portrays the modified circuit with an additional nMOS device, MN4. The insertion of MN4 aids in reducing the V_{GS} , and hence attaining a smaller I_{th} . In actual case, more than one nMOS devices can be inserted for even smaller values of I_{th} .

Figure 4.29 The schematic diagram of the proposed area-efficient current comparator.

By examining the threshold current generating circuit, one can observe

$$V_{DD} = |V_{tp}| + nV_{tn} \quad (4.9)$$

Rearranging Equation (4.9) yields

$$n = \frac{V_{DD} - |V_{tp}|}{V_{tn}} \quad (4.10)$$

where n denotes the maximum number of nMOS that can be coupled into the threshold generation circuit before any of the devices in the threshold generation circuit leaves the saturation mode.

The expression for I_{th} is derived as follows. By equating the saturation currents of MN1 and MN4, the source potential of MN1, V_{SMN1} , is given by

$$V_{SMN1} = \frac{V_{G1} - V_{th} + \sqrt{\frac{K_{MN4}}{K_{MN1}}} V_{tn}}{1 + \sqrt{\frac{K_{MN4}}{K_{MN1}}}} \quad (4.11)$$

Equating the saturation currents of MP1 and MN1 yields

$$K_{MP1} (V_{SGMP1} - |V_{tp}|)^2 = K_{MN1} (V_{GSMN1} - V_{tn})^2 \quad (4.12)$$

Substituting Equation (4.11) into Equation (4.12), V_{G1} is expressed as

$$V_{G1} = \frac{(V_{DD} - |V_{tp}|) \left(1 + \sqrt{\frac{K_{MN4}}{K_{MN1}}} \right) + 2 \left(\sqrt{\frac{K_{MN4}}{K_{MP1}}} V_{tn} \right)}{1 + \sqrt{\frac{K_{MN4}}{K_{MN1}}} + \sqrt{\frac{K_{MN4}}{K_{MP1}}}} \quad (4.13)$$

Hence,

$$I_{th} = I_{DMP1} = \frac{K_{MN4} (V_{DD} - |V_{tp}| - 2V_{tn})^2}{\left(1 + \sqrt{\frac{K_{MN4}}{K_{MN1}}} + \sqrt{\frac{K_{MN4}}{K_{MP1}}} \right)^2} \quad (4.14)$$

For the conventional and modified current-mode comparators, the smallest possible gate area for the transistors in the threshold current generation circuit will tend to yield an optimized $I_{th(opt)}$. At $I_{th(opt)}$, the W and L of a transistor are the minimum dimensions that can be realized in a layout. It has been corroborated by our simulations that the $I_{th(opt)}$ of the conventional current comparator is higher than that of the new comparator for the same CMOS technology and power supply voltage. In view of the fact that to obtain an I_{th} , which is lower than the $I_{th(opt)}$, will require the channel length to be increased since the channel width has reached its minimum boundary, the utilization of the proposed comparator is more desirable for low I_{th} applications.

4.4.3 Simulations and Performance Comparison

Extensive simulations have been carried out on the conventional, Chunyan's and the proposed current-mode comparator based on three different technologies, namely, the 0.25 μm , 0.18 μm , and 0.13 μm CMOS technology from CHRT. Various technologies were utilized to figure out the dominant operating environment for each circuit.

By using each of the above-mentioned technology, the minimum gate area requirement of the circuits was established for two distinct I_{th} , i.e., 1 μA and 0.5 μA , for

varying values of V_{DD} . Low values of I_{th} are used as test bed due to the incessantly escalating demand for low-power devices [101, 102]. The input current level I_{in0} of $I_{th} = 0.5 \mu A$ swings between $0.2 \mu A$ to $0.8 \mu A$, whereas that of $I_{th} = 1 \mu A$ steps between $0.7 \mu A$ and $1.3 \mu A$. In order to make a fair comparison, identical sets of W and L values for MN2 and MN3 for all circuits in evaluation were employed throughout a particular technology. According to the simulated and optimized gate area of the three circuits, the most compact and area-optimum layouts are drawn based on the respective CHRT $0.25 \mu m$ 5M2P, $0.18 \mu m$ 6M1P and $0.13 \mu m$ 8M1P n-well p-substrate CMOS design rules for comparison on their layout area consumption.

A comprehensive performance perusal and discussion on the simulation results of different parameters in comparison of the three current comparators is illustrated in the following paragraphs. Figures 4.30 and 4.31 show the savings on layout area (represented in percentage) of the new current-mode comparator with respect to those of the conventional and Chunyan's circuits at different power supply voltage, V_{DD} . It gives a clear graphical illustration on the operating environment at which each current comparator should be used to bring forth minimum area consumption. The modified comparator promises an impressive across-the-board gate area reduction for both the test I_{th} . An example of the layout drawing of the proposed comparator based on the $0.18 \mu m$ technology at $I_{th} = 0.5 \mu A$ and $V_{DD} = 2.5 V$ is shown in Figure 4.32. It occupies an area of $29.67 \mu m^2$, which is 49.53% and 56.35% less than those of the conventional circuit ($58.79 \mu m^2$) and Chunyan's circuit ($67.97 \mu m^2$), respectively.

(a)

(b)

Figure 4.30 Area reduction of the new current comparator with respect to the conventional comparator at varying technology and I_{th}
(a) $V_{DD} = 3.3$ V. (b) $V_{DD} = 2.5$ V. (c) $V_{DD} = 1.8$ V.

Figure 4.31 Area reduction of the new current comparator with respect to Chunyan's comparator at varying technology and I_{th}
(a) $V_{DD} = 3.3$ V. (b) $V_{DD} = 2.5$ V. (c) $V_{DD} = 1.8$ V.

Figure 4.32 Layout of the modified current comparator at $I_{th} = 0.5 \mu\text{A}$ based on 2.5 V/0.18 μm CMOS technology.

A most desirable trait of this new circuit is that the area efficiency becomes more prominent with the scaling down of the process technology. In other words, the proposed circuit has the greatest area advantage when the smallest technology is used, which is the 0.13 μm technology. For instance, at $V_{DD} = 1.8 \text{ V}$ and $I_{th} = 0.5 \mu\text{A}$, the area enhancement over the conventional circuit at 0.25 μm and 0.18 μm technology is 27.91% and 35.83%, respectively, while that of 0.13 μm is further elevated to 58.18%. The comparison with Chunyan's circuit shows similar trend. This characteristic is the main attraction of the proposed design as it parallels the drive towards ever shrinking technology.

The new current-mode comparator offers a significantly enhanced reduction in layout area without compromising its power consumption and propagation delay performance. The Area-Delay Product (ADP) and Power-Delay Product (PDP) are used as performance indicators for the circuits in comparison. Figure 4.33 illustrates the ADP with respect to I_{th} for all three circuits at 1.8 V/0.13 μm CMOS technology. It can be seen that the modified circuit exhibits performance leverage over the other two circuits by offering a drastically reduced ADP. For example, at $I_{th} = 0.5 \mu\text{A}$, the proposed current comparator offers a significant 58.18% and 89.23% reduction in ADP when compared to the conventional and Chunyan's circuit, correspondingly.

Figure 4.33 Area-Delay Product (ADP) for 1.8 V/0.13 μm CMOS technology at $C_L = 100$ fF.

The simulation result of the PDP relative to I_{th} is shown in Figure 4.34. The proposed current comparator promises a significantly lower PDP at $I_{th} = 1 \mu\text{A}$, with an improvement of 10.55% and 60.34% as compared to the conventional and Chunyan's circuit. As for $I_{th} = 0.5 \mu\text{A}$, the modified circuit exhibits a marginally higher PDP as compared to its conventional counterpart. However, this trivial drawback of the new circuit at a higher I_{th} can readily be compensated by the vast improvement in its remarkably reduced layout area.

Figure 4.34 PDP for 1.8 V/0.13 μm CMOS technology at $C_L = 100$ fF.

4.4.4 Design and Implementation of PDA

The current comparators assessed in the preceding sections have been incorporated into the CMMVL PDA to confirm their functionality. The PDA, as reported in Section 4.1, is realized based on the redundant Positive-Digit (PD) number representation [103]. The PDA cell actually serves as a binary number converter, converting z_i to c_i^2 , c_i^1 , and w_i , denoted by either a '0' or '1' value. Each signal level is represented by a multiple of a unit current step, I_0 . Basically, three stages are required to compute the binary values of c_i^2 , c_i^1 , and w_i .

In this proposal, we design a single-stage PDA cell that realizes the computation of c_i^2 . This implementation is sufficient to gauge and compare the practicality and performance of our proposed current comparator with the other two designs. The full implementation incorporating the generation of c_i^1 and w_i can then be easily deduced [96]. The simplified circuit configuration of the single-stage PDA cell is shown in Figure 4.35. It consists of a current-mode comparator and a Voltage-Switched Current Source (VSCS).

The current comparator is made up of current source I_{ref} and a pair of current mirrors, while the VSCS comprises current source, I_0 , which represents the value of the unit current step and a switch. The current mirror duplicates an identical replica of the input current, z_i and compares it with the reference current, I_{ref} . The difference of these two current values decides the potential of node X, which will be used to open or close the switch of VSCS. When the switch is closed, c_i^2 will take the value of I_0 , while an opened switch turns c_i^2 to a '0' value.

Figure 4.35 A single-stage PDA implementing c_i^2 .

The conventional, Chunyan's and the new current comparator have been integrated in the single-stage PDA to verify their functionality and compare their performance, in terms of layout area and PDP. The PDA has been designed with an I_{th} of $1 \mu\text{A}$ and a load resistance, R_L of 50Ω based on a $1.8 \text{ V}/0.18 \mu\text{m}$ CMOS technology from CHRT. It uses an I_0 of $1 \mu\text{A}$, and is capable of distinguishing seven levels of input signals corresponding to the seven possible discrete values of z_i (0 to $6 \mu\text{A}$). In conjunction to that, I_{ref} for this design is set to $3.5 \mu\text{A}$ as c_i^2 is the MSB of a three-digit binary number. The value of c_i^2 is either 0 or $1 \mu\text{A}$. The transient response of the single-stage PDA encompassing the proposed current comparator is shown in Figure 4.36.

Figure 4.36 Transient response of the single-stage PDA incorporating the proposed current comparator.

The simulation results comparison of three single-stage PDAs, each using different types of current comparators is tabulated in Table 4.2. The PDA using the new current comparator requires a silicon area of only $40.2 \mu\text{m}^2$ (layout drawing shown in Figure 4.37), which is 22.8% and 77.4% less than those of its conventional ($52.07 \mu\text{m}^2$) and Chunyan's ($177.94 \mu\text{m}^2$) counterparts. Apart from that, a prominent performance improvement over other designs in comparison has been observed when the proposed current comparator is integrated into the PDA. Thus, the contribution of the novelty arising from the proposed circuit has been non-trivial and has gone beyond the simplicity of area reduction, as demonstrated from the 7.3% and 70.4% power-delay product improvement of the PDA with the proposed current comparator over that of the conventional and contemporary contender circuits.

Table 4.2 Simulation results comparison of three single-stage PDAs, each using different types of current comparators in comparison.

	Single-stage PDA using:		
	Conventional current comparator	Chunyan's current comparator	Proposed current comparator
Layout Area, μm^2	52.07	177.94	40.2
Delay, ns	16.27	44.71	14.91
Power consumption, μW	9.18	10.47	9.29
Power-delay product, pJ	0.1494	0.468	0.1385

Figure 4.37 Layout of the single-stage PDA implementation using the proposed current comparator.

4.5 Summary

In this chapter, the conventional and the contemporary work on current comparators have been reported. We have highlighted the various current detection circuits of existing publications and the lack of adequate circuit design consideration for the imperative current subtraction segment that drives these circuits. The chapter has been divided in such a way that it first covers the current comparators without the inclusion of a current subtraction entity and subsequently followed by the complete current comparators with current subtraction. This chapter also presents a CMOS current-mode comparator circuit that evolves from the conventional current-mode comparator. The justification for the emphasis on the research of the proposed area-efficient current-mode comparator for low current operation has also been added by providing adequate referenced applications where such design can be of specific merits without unduly sacrificing the critical power-delay characteristics.

The modified current-mode comparator is proposed as a viable contender for the conventional comparator at low I_{th} . Extensive simulations and evaluative comparison have been carried out among the conventional, Chunyan's and the proposed current comparator. It has been verified that for low I_{th} , the modified current comparator offers a convincing small-area feature without compromising the power dissipation and speed performance. A small I_{th} , which implies a low static power consumption, is preferable in today's advanced ULSI technology that highlights the essentiality of low-power design. Furthermore, this area advantage becomes even more pronounced when the process technology is scaled down, from 27.91% area reduction at 0.25 μm technology to 58.18% for 0.13 μm CMOS technology as compared to the conventional circuit. This characteristic of the proposed circuit, which offers increasingly attractive area reduction with the scaling down of the feature size, is a prominent advantage, since it is in line with today's continuous miniaturization of the process technology. A further design and implementation of PDA, is included to give a judicious and lucid coverage regarding the concept, realization and comparison of the single-stage PDA using the current comparators in comparison. The end result is a promising enhancement of our proposed design, featuring an impressive improvement in layout area and PDP computation.

Chapter 5

Low-Power High-Performance Static Random-Access Memory

5.1 Introduction

A review of power requirement in individual building blocks of processors has shown that memory devices constitute the highest proportion of the overall power consumption [104-106]. The availability of semiconductor memory is a salient prerequisite for data and program instruction storage in almost all fields of applications in the information technology age [12]. In fact, it has even been forecast that embedded memory will dominate up to 90% of the total chip area in SoC integration by 2013 [107, 108].

Semiconductor memory is usually of the random-access type, where the time required for storing and retrieving data is independent of the physical location in which the data is stored [98]. Hence, the average access time for the semiconductor memory is normally shorter than that of mass-storage memory, which is often associated with serial or sequential memory such as hard disks, floppy disks, CD-ROM and tape backup systems, from which information is accessible only in the same sequence as it was originally stored. Semiconductor memory can be classified into Read-Only Memory (ROM) and Read/Write Random-Access Memory (RAM). An overview of the classification of semiconductor memory types is shown in Figure 5.1.

Figure 5.1 Overview of semiconductor memory.

As its name implies, ROM only allows the retrieval of prerecorded data, but precludes write operation, as it does not permit modifications of the stored information. It is a nonvolatile memory that stores information in a fixed pattern [98]. In the digital circuit jargon, nonvolatile denotes that the contents are always preserved even with the removal of power supply. This is the crucial property that distinguishes ROM from RAM, in which constant flow of electricity is required to retain its contents.

5.2 SRAM and DRAM

RAM has seen an outstanding and tremendous advancement in power reduction over the years. Many circuit techniques have been devised to target reduced active and standby power in both static and dynamic RAMs [109-112]. This trend is attributed to the advent of high-density and low-power electronic applications such as hand-held terminals, mobile phones and laptops.

As mentioned earlier, RAM is Read/Write (R/W) memory. This denotes that the data bit stored in its memory cells can be altered to a new data bit easily and quickly [113]. The time required for a RAM to store (write) information and to retrieve (read) information is independent of the physical location (within the memory) in which the information is stored. It is organized and controlled in a way that enables data to be stored and retrieved directly to a specific location. Indeed, data can be stored and retrieved at comparable speeds in R/W memory [98]. Furthermore, RAM is a volatile

memory. It retains its memory patterns as long as power is being supplied. Conversely, its contents are lost once the power is removed.

R/W Random-Access Memories can be classified into two categories according to their memory cell architectures:

- * Static RAM (SRAM)
- * Dynamic RAM (DRAM)

The major difference between SRAM and DRAM is that SRAM does not need power refresh operations, while DRAM warrants cyclical refreshing of the stored charge [114]. SRAM utilizes static latches, which operate in a flip-flop mechanism, as the memory cells. The electrical feedback ensures that voltage levels are sustained and data is retained indefinitely as long as the power supply remains. On the other hand, the term ‘dynamic’ is used for DRAM because the inherent leakage phenomenon necessitates the capacitor to be periodically refreshed for the purpose of data retention, without which will inevitably leads to gradual charge leakage and depletion. A closer inspection on the two RAM structures reveals that the SRAM cell is less power hungry than DRAM since it always operates in stable state [115]. Even though DRAM is more cost-efficient and provides much higher density (usually four times) than its SRAM counterpart by virtue of its smaller memory cell size, it is achieved at the expense of more intricate overhead peripheral circuitry [98]. Moreover, unlike the DRAM, which depends on capacitive element for data storage, SRAM offers extremely fast access time (approximately four times faster than DRAM) as it operates with differential-mode of bit-lines pairs [98].

Both SRAM and DRAM have their respective niche markets given their distinctive features and benefits. SRAM is used when power and speed is essential while silicon area is not critical and vice versa for DRAM. For example, the SRAM-based cache memory hierarchies have become ubiquitous in the design of modern microprocessors for bridging the widening divergence in the performance of the Central Processing Unit (CPU) and the DRAM-based main memory [116]. To juggle between the often-conflicting constraints of performance and cost, many embedded systems include a small block of SRAM along a critical data path or in on-chip cache memory and a much larger block of DRAM for the main memory. On top of that, the SRAM is a required memory class in SoC designs due to its compatibility to standard CMOS processes. In

contrast to most other memory types, SRAM can be integrated in the conventional CMOS processes without any additional fabrication cost [117].

The remainder of this thesis addresses only SRAM. The ultimate concerns on power consumption and speed performance are the key motivators driving us to select SRAM instead of DRAM as our main focus in this research. In addition, embedded SRAM macros are important dissipation sources in many VLSI devices as they contain high-capacitance buses and they are frequently accessed [118]. This power consumption is predicted to rise because of the escalating transistor budget allocated to cache and the increasing operating frequency. In view of that, there is invariably an apparent urgency to reduce the power dissipation and to further enhance the performance of SRAM to cater to the tremendous surge of interest in high-durability and small-sized handheld personal communication devices and other more sophisticated multimedia-based applications.

5.3 SRAM Basic Architecture

The block diagram of a typical SRAM architecture is depicted in Figure 5.2 [98]. SRAM chips consist mainly of address buffers, row/column decoders, memory cell matrix, sense amplifiers and input/output buffers. The conditioning circuit executes the pre-charging of the bit-lines to an equalized potential prior to the read operation. Meanwhile, the array of memory chip contains the cells in which data bits are stored (read operation) or to be stored (write operation). Each cell is connected to one of the multiple word-lines and bit-lines. The word-lines shared by the memory cells in each row run horizontally throughout the memory matrix, while pairs of bit-lines extend vertically and are shared by the memory cells in each individual column. In a read or write operation, a particular cell is selected by triggering its word-line and bit-line. This task is performed by the row decoder and the column decoder driven by the address buffers. The addressed cell is positioned at the point of intersection between the activated word-line and bit-line. A column sense amplifier will then detect the contents of the selected cell in the form of small voltage variations via the memory cell complementary bit-lines. The detection must occur as speedily as possible to achieve minimal access time.

Figure 5.2 Typical SRAM architecture.

The access time is defined as the time required to locate and produce a single piece of information, from the start of the valid input address until the appearance of a valid output signal. It is typified by the critical path from the address input to the data output as shown in Figure 5.3. The word-line decoding and bit-line sensing delay times are critical delay components. In view of this, a small swing at the bit-lines and a sense amplifier with high sensitivity is greatly desirable to reduce the sensing delay during a read operation. Also, from the viewpoint of power consumption, the bit-line and sense amplifier power components are found to be the dominant factors in on-chip caches, together contributing 80-90% to the total cache power.

Figure 5.3 Typical path for read access in SRAM.

5.4 Read and Write Operation

The SRAM promises fast and robust read and write operations. As seen in Figure 5.2, the commonly used control signals in an SRAM are the Write-Enable ($\overline{WE}$), Chip-Select ($\overline{CS}$) and Output-Enable ($\overline{OE}$). The $\overline{WE}$ signal decides between the read and write modes. For the read operation, the bit-line signals are transported to the output, whilst for the write operation, the bit-lines are driven from the input. In a memory system where a myriad of SRAMs are pooled together, the SRAMs are connected to common address and data buses. Only one memory out of the memory bank may be selected at a given time to place information on the data bus. In this case, the $\overline{CS}$ signal aids in the selection of a single SRAM from the memory bank. Meanwhile, $\overline{OE}$ serves as the enabling signal for the output buffer.

The timing diagram of a read operation is shown in Figure 5.4(a). During this time the datum stored in a specific SRAM location (defined by the address) is read out. The read cycle time, t_{RC} , is specified as the time needed to complete one read cycle from one memory address to another. The address access time, t_{AA} , is the amount of time it takes to produce the data required, from the time the address becomes valid until the time when the output data is available for use.

Figure 5.4(b) shows the write operation, which permits changes to the information within an SRAM. Similar to t_{RC} , the write cycle time, t_{WC} is defined as the time required to complete a write cycle between subsequent memory accesses. Meanwhile, the time necessary to recover from the write cycle to the next state after the $\overline{WE}$ signal is deactivated is called the write recovery time, t_{WR} . It is an important timing component in

high-speed SRAMs because the shorter the delay is, the earlier the next operation can be initiated.

Figure 5.4 Typical timing of an SRAM (a) read cycle. (b) write cycle.

The Memory Cell (MC) is a fundamental element in the design of low-power and high-density SRAMs because a hefty portion of the memory size is dominated by the cell area. The memory cell implementation in its most commonly used and simplest form is shown in Figure 5.5, namely the 6-T memory cell [45]. The cell is made up of two pass-transistors (MN3 and MN4) and a flip-flop formed by two cross-coupled inverters (MP1, MN1 and MP2, MN2). The access transistors, which are connected to the two complementary bit-lines BL and $\overline{BL}$, are governed by the signal RS (Row-Select). They act as transmission gates providing bi-directional access between the flip-flop and the bit-lines [98]. The structure of the cell represents an inherent latch operation, whereby only two stable states can occur at any point of time. It offers the characteristics of low power property (almost zero static power), high-speed performance and high stability. In addition, it features a low process complexity and a good compatibility with logic processes. Various other static storage cells have been reported in the literature [45, 119-123]. However, most of these storage cells compromise on the power and speed criterions in favor of reduced transistor count.

Figure 5.5 The 6-T CMOS memory cell.

The SRAM memory cells are usually optimized to be small and compact, resulting in very small cell currents and hence a slow bit-line charge/discharge rate. The speed performance deteriorates further if the bit-line capacitances are large, as is common in the SoC era, which hastens the development and realization of excessively high-complexity electronic appliances. Subsequently, a sense amplifier with high sensitivity is often desirable to amplify the small bit-line signals to get, at the end, a full-swing well-defined signal.

Before the read operation, the voltages at both bit-lines are pre-charged to an equalized potential. Consider a stored logic ‘1’ at node A and a complementary logic ‘0’ at node B . When this particular memory cell is selected by asserting the WL, $\overline{BL}$ will be discharged to ground via MN4 and MN2. Concurrently, current flows from V_{DD} to BL through MP1 and MN3, causing an increase in its voltage. During a read operation, a small voltage swing variation on the bit-line is pragmatic to ensure high-speed sensing, as it would require a substantial amount of time to charge/discharge the voltages of the bit-lines all the way to V_{DD}/Gnd by the SRAM memory cell especially when C_{BL} is high. This small swing will be detected and amplified by a current-mode sense amplifier, which will be covered in detail in the subsequent section.

As for the write operation, the data bit to be written and its complement are transferred to the BL and $\overline{BL}$ lines, respectively. For instance, if the value to be written is ‘1’, the BL line is raised to ‘1’ and the $\overline{BL}$ line is lowered to ‘0’. When the cell is

selected by WL, the access transistors will write a '1' at node A and conversely, a '0' will appear at node B . The cross-coupled inverter pair has a high gain to cause the nodes A and B to switch to opposite voltages. This state, which corresponds to a stored 1, will be maintained indefinitely unless it is altered by another write operation.

5.5 Sense Amplifier

As mentioned earlier, power-efficient SRAM is the heartland of our technology savvy mass market, which serves as a viable contender for cache memories [124-126]. Its memory capacities have been quadrupling from one generation to another almost every three-yearly [107]. Each of these generations of CMOS SRAMs has been advanced by reducing the memory cell size by about one-third and increasing the chip size by roughly 1.5 times. However, with the advent of the SoC technology, the density of SRAMs in embedded applications has multiplied significantly in recent years. This has inevitably resulted in a rise in both bit-line and data-line capacitances, and hence constituting a major design constraint in achieving low power consumption and high sensing speed in memory systems. The most efficient way of reducing power dissipation is by scaling down the power supply voltage. However, reducing the supply voltage causes degradation, or in other words, a reduction of the readout voltage amplitude on the bit-lines. The important entity that plays a key role in attaining power and speed efficiency of the SRAM architecture is none other than the sense amplifier. It consumes the largest amount of power and constitutes 30-40% of the total read access time [45, 127]. In view of the above issues, designing a sense amplifier with high sensitivity, low power, and small area is of ultimate importance.

The sense amplifier is one of the most prominent building blocks of SRAM as it enables differentiation between a logic '0' or a logic '1' stored in the memory cell. Also, due to the increasingly large bit-line and data-line capacitances, coupled with the restricted current drivability of the small memory cell, a rail-to-rail excursion over the bit-lines is undesirable due to speed and power considerations. The sense amplifier is therefore required to detect a small signal appearing at the two bit-lines, and then amplify it to provide full-swing signals at the output of the sense amplifier for interaction with

other peripheral circuitries. In other words, the availability of the sense amplifier allows for a reduced voltage swing on the bit-lines, which is an essential feature in enhancing both the power and speed performances.

The SRAM sense amplifier can be implemented either in differential or non-differential (single-ended) column architectures [117]. An important characteristic of the differential approach over its non-differential counterpart is the common-mode rejection [21, 128]. For differential structures, only the difference between its inputs is amplified, while the signals common to both inputs (such as noise sources or any unwanted input signals) are suppressed at the output of the amplifier. This feature is exceedingly imperative for SRAM memory designs where the amplitude of the signal to be sensed is generally small. In view of the above issues, we concentrate mainly on the differential-type sense amplifier in our discussion.

5.5.1 Voltage Sensing versus Current Sensing

The differential sense amplifier to be discussed in this chapter is categorized into voltage-mode and current-mode. We will first discuss the concepts of the respective sensing methods, followed by the contemporary sense amplifiers adopting the voltage sense and current sense techniques.

The voltage sensing mechanism is displayed in Figure 5.6(a) [117]. Prior to sensing, BL and $\overline{\text{BL}}$ are equalized to a potential of V_{BL} , which is usually close to V_{DD} , and the bit-line load is deactivated during sensing. The bit-line MUX (column MUX) is placed between the memory cell and the sense amplifier such that a single sense amplifier can be shared among multiple columns for area saving and potentially, power reduction. When a “0” is stored in one side of a selected memory cell, a current is drawn into that side of the particular cell. Consequently, this current, i_{cell} , will discharge the bit-line capacitance resulting in a voltage pull-down, ΔV_{BL} at the bit-line. On the contrary, a stored “1” in the other side of the cell will not draw any current since V_{BL} is close to V_{DD} . Hence, this complementary bit-line signal acts as a reference for sensing. The voltage sense amplifier, which essentially is a voltage comparator, generates a CMOS level output signal. Unfortunately, the voltage sensing approach has one principle drawback: it

needs an intolerably long delay time to discharge the large bit-line capacitance presented by the long interconnect lines and the increasing memory capacity, thus constituting a major bottleneck in achieving a high sensing speed.

Figure 5.6 (a) Voltage sensing mechanism. (b) Current sensing mechanism.

An apparent solution to the above-mentioned sensing speed degradation is to make use of the current sensing technique instead of the conventional voltage sensing methodology. The current sensing mechanism is portrayed in Figure 5.6(b), where an additional current conveyor for the purpose of current sensing is included before the current-to-voltage converter. The current conveyor and current-to-voltage converter jointly form a current sense amplifier. This current conveyor is a buffer stage with no gain that decouples the current-to-voltage converter from the highly capacitive bit-lines. The current-to-voltage conversion circuitry can be the voltage sense amplifier used in the voltage sensing mechanism, or, it can also be a current-sensitive circuitry.

A distinct advantage of the current sense amplifier is that it exhibits a low input resistance characteristic, which significantly reduces the bit-line voltage swing and sensing delay. Due to the integration of the current sensing stage, the differential current signal from the memory cell propagates almost instantaneously and produces an output voltage, which is proportional to i_{MC} , to the voltage sense amplifier. In other words, the sensing delay is virtually unaffected by the bit-line capacitance since differential capacitor discharging is not required to sense the cell datum. These attributes in turn translate to lower power consumption and higher speed performance.

An equivalent model of the sensing circuit is depicted in Figure 5.7 [129]. It includes the memory cell, the distributed RC bit-line and the sense amplifier equivalents. The memory cell is modeled by a current source i_{MC} and a source resistance, R_{MC} . This source resistance is actually the bit-line load in parallel with the drain terminal resistance of the access transistor, which is the output device of the memory cell. The distributed network with arbitrary number of resistance load R and capacitance load C , represents the infinite-length bit-line. This model can well be utilized to represent both the voltage and current-mode sensing circuits, depending on the way the transmission line is terminated. In general, the line is terminated by the sense amplifier's input resistance, R_s , which is infinity for voltage sensing with an open-circuit signal v_s , and approaches zero for current sensing with a short-circuit signal i_s .

Figure 5.7 An equivalent model of the sensing circuit.

The propagation delay of a continuous ramp signal is represented by

$$t = \frac{R_{BL} C_{BL}}{2} \left(\frac{R_{MC} + \frac{R_{BL}}{3} + R_s}{R_{MC} + R_{BL} + R_s} \right) + R_{MC} C_{BL} \left(\frac{R_s}{R_{MC} + R_{BL} + R_s} \right) \quad (5.1)$$

where R_{BL} and C_{BL} denote the total bit-line resistance and capacitance, respectively.

Equation (5.1) can be simplified for the voltage-mode and current-mode sensing by inserting their respective R_s values and with the assumption that $R_{MC} > R_{BL}$, as is always the case for CMOS circuits. The propagation delay for voltage sensing with infinite R_s is denoted by

$$t_v = C_{BL} \left(\frac{R_{BL}}{2} + R_{MC} \right) = R_{MC} C_{BL} \quad (5.2)$$

It can be observed that the sensing delay of the voltage amplifier is substantially longer than the intrinsic line delay. Meanwhile, the propagation delay for current sensing with low (ideally zero) input resistance is given by

$$t_i = \frac{R_{BL} C_{BL}}{2} \left(\frac{R_{MC} + \frac{R_{BL}}{3}}{R_{MC} + R_{BL}} \right) = \frac{R_{BL} C_{BL}}{2} \quad (5.3)$$

which is close to the intrinsic line delay. As long as the approximation $R_{MC} > R_{BL}$ holds true, it can be deduced that the sensing delay of the current-mode approach is much shorter than that achievable by voltage-mode technique. The effect of the bit-line self-inductance on the sensing delay is neglected in this context as it is negligible as compared to the resistance load, R_{BL} . Having explained the voltage and current sensing methodologies, it is now appropriate to include the conventional and some of the contemporary designs of voltage and current sense amplifiers, which have been reported in the literature.

5.5.2 Voltage Sense Amplifier

Figure 5.8 shows a simplified conventional voltage sense amplifier with an active current-mirror [45]. It has two differential inputs, DL and $\overline{DL}$. The differential approach has the advantage that only the difference between its input signals is amplified. However, the signals common to both inputs are suppressed at the output of the amplifier by a ratio called the Common-Mode Rejection Ratio (CMRR). This sense amplifier has a large DC current component when it is energized. In view of that, the transistor MN_s , which serves as a current source, is activated by the signal ϕ_{SA} only during read operation

to cut off the static current. Before ϕ_{SA} is asserted, the data-lines DL and $\overline{DL}$ are high. Likewise for all the nodes A , B , and C . When the data stored in the memory cell is logic '1', the voltage at DL is higher than that at $\overline{DL}$. Both nMOS transistors will turn on and since the potential at DL is higher, more current flows through it. Eventually, transistor $MN2$ will turn off and the output at node C will be at logic '1' and vice versa for a logic '0' stored in the memory cell. A drawback of this current-mirror sense amplifier is its single-ended output.

Figure 5.8 Current-mirror voltage sense amplifier with single-ended output.

The differential voltage sense amplifier with double-ended output is used to achieve larger voltage gain, better output voltage stability, and faster data transfer during read operation [21]. A simplified double-ended sense amplifier is illustrated in Figure 5.9. The delay time of this amplifier generally depends on the gate widths of MN_n and MN_s or the amplifier current. Its operation is the same as that of the single-ended sense amplifier except that it has two outputs. Nonetheless, for memories with high-density, this type of sense amplifier may result in high-power dissipation even with a pulsed current source [45].

Figure 5.9 Current-mirror voltage sense amplifier with double-ended output.

Another type of voltage sense amplifier, which is based on positive feedback operation, is formed by cross-coupling two CMOS inverters, as shown in Figure 5.10 [98]. Transistors MN1 and MP1 function as switches that connect the sense amplifier to ground and V_{DD} only when data-sensing action is required. Otherwise, SE is low and the sense amplifier is turned off, which helps to conserve power.

Figure 5.10 Cross-coupled CMOS inverter latch used as sense amplifier.

For a read access, if the cell had stored a '1', then a small positive difference will develop between the two bit-lines with V_{BL} higher than $V_{\overline{BL}}$. The amplifier will cause V_{BL} to further rise to V_{DD} and $V_{\overline{BL}}$ to fall to 0 V. This logic '1' output will be directed to the I/O pin by the column decoder. On the contrary, if a '0' is stored in the cell, a negative voltage difference will develop between the bit-lines with V_{BL} lower than $V_{\overline{BL}}$. The

amplifier will cause V_{BL} to rise to V_{DD} and V_{BL} to fall to 0 V. This indicates that a ‘0’ is being stored in the cell.

A sense amplifier, which is suitable for low-voltage power supply is depicted in Figure 5.11 [130]. $CSeI$ denotes the Chip-Select signal. This circuit is employed when the bit-lines are near V_{DD} , where the gain of a conventional current mirror amplifier is poor. The V_{DD} -close input voltages are essential to guarantee a stable low-voltage operation of SRAMs. A level-shift circuit and a two-stage conventional current mirror amplifier are incorporated to form the sense amplifier.

The level shifter makes use of two low-threshold nMOSFETs to shift the voltage at the common data-lines from 1 V to almost half of it (around 0.6 V to 0.7 V) to ensure that the current mirror amplifier is sensitive to this voltage level.

Figure 5.11 Low-voltage sense amplifier [130].

5.5.3 Current Sense Amplifier

The current sense amplifier is used to detect the current difference between the data-lines to determine whether a ‘1’ or a ‘0’ is stored in the memory cell. It directly measures the cell read current and transfers it to the output circuits. This approach can overcome the restriction of gain reduction of voltage-mode sense amplifiers at low-power supply voltage. The simplest structure of the current sense amplifier is the conventional current sense amplifier, which basically consists of four equal-sized pMOS transistors as shown in Figure 5.12 [129]. It features a current sensing characteristic since it represents a virtual short circuit to the bit-lines, transferring the cell current directly to the output circuits.

Figure 5.12 The conventional current sense amplifier.

Suppose the cell is accessed and if it is storing a logic ‘0’ in the cell, it draws a current I . Transistors MP1 and MP3 will have equal gate-source voltage since their currents and sizes are equal, and both transistors operate in saturation. This voltage is represented by $V1$. The same principle applies to MP2 and MP4. Their gate-source

voltages are represented by V_2 . Following that, since the column-select CS is grounded, the potentials of both BL and $\overline{BL}$ will be equal to $V_1 + V_2$ independent of current distribution. This means that there exists a virtual short circuit across the bit-lines. Since the bit-line voltages are identical, the bit-line load currents will also be identical. Since the memory cell draws current I , the right leg of the sense amplifier must pass more current than the left leg. The drain currents of MP3 and MP4 are passed through the current conveyor to the current transporting data-lines. The differential data-line current is therefore equal to the cell current. If a logic '1' is stored in the cell, a current would flow out of the cell instead and causes the left leg to pass more current than the right leg. This difference in current implies that a logic '1' is being stored in the cell.

Owing to an intrinsic pre-charge property, current consumption for the current sense amplifier decreases and sensing speed has improved. The virtual short circuit character across the bit-lines ensures equal bit-line potentials, thus eliminating the need for bit-line equalization during a read access. The sensing delay is insensitive to bit-line capacitance since no capacitor discharging is required to sense the cell data. Therefore, current sense amplifier has better performance than voltage sense amplifier in terms of smaller delay and less current consumption.

A high-speed current sense amplifier coupled with a pre-output buffer is portrayed in Figure 5.13 [131]. This design successfully tackles the gain reduction problem of the conventional voltage sense amplifier as it offers a large voltage gain for bit-line voltages close to V_{DD} . The control signal Φ_{eq} is the equalization signal for both the bit-lines and data-lines, whereas EQ represents the equalization signal for the terminals $S1$ and $S2$. Meanwhile, SAC denotes the sense amplifier control signal.

Figure 5.13 Sensing circuitry of a 7 ns 140 mW CMOS SRAM with current sense amplifier.

When RS is not chosen, the memory cell is not selected and the current I_0 that flows from both bit-lines (BL1 and BL2) to the sense amplifier is the same. Thus, a same current $I_0/2$ flows through the pMOS devices MP1, MP2, MP3 and MP4 in the amplifier. On the other hand, if RS is asserted, the memory cell is selected and a small quantity of cell current ΔI flows from one of the bit-lines to the cell. For instance, if a logic '0' is stored in the cell, ΔI will flow from BL1 to the cell, and hence the current flowing from BL1 to the amplifier is reduced to $(I_0 - \Delta I)$, while the current flowing from BL2 to the amplifier stays at I_0 . As a result, the current that flows through MP1 and MP3 is reduced to $(I_0 - \Delta I)/2$, meanwhile the current that flows through MP2 and MP4 remains at $(I_0/2)$. The current, which flows through MN1, is $I_0/2$ because the current flowing through MP2

and MN2 is the same, and MN1 is the current mirror of MN2. Therefore, the load capacitance $C1$ is discharged by MN1, which draws more current than MP1 provides. Similarly, the load capacitance $C2$ is charged up by MP4, which provides more current than MN4 draws. As a consequence, the potential of terminal $S1$ drops while the voltage of terminal $S2$ rises, and a voltage swing is obtained between $S1$ and $S2$.

The current sense amplifier (Figure 5.13) has been simulated and compared with the conventional double-ended voltage sense amplifier (Figure 5.9) with a 1.1 mA amplifier current at a 3.3 V power supply voltage [131]. The simulated voltage gain for both circuits in comparison is depicted in Figure 5.14 and it shows that the current sense amplifier has almost three times the gain of the voltage sense amplifier over a wide range of supply voltages.

Figure 5.14 Simulated voltage gain [131].

Figure 5.15 shows the sensing delays for the current sense amplifier and voltage sense amplifier [131]. Sensing delay denotes the time interval from the crossing point of the input voltages to the time when the output voltage swing reaches 0.1 V. The current sense amplifier shows a 30% improvement in delay time as compared to the voltage sense amplifier.

Figure 5.15 Sensing delay of the current and voltage sense amplifier [131].

A hybrid sense amplifier, which makes use of current-transporting sensing techniques at both the bit-lines and data-lines, is shown in Figure 5.16 [132]. It adopts the conventional current sense amplifier topology, as illustrated in Figure 5.12 for column sensing, and a regenerative CMOS cross-coupled latch as the current-to-voltage converter. This cross-coupled latch has been designed in such a way that it is current-sensitive, hence detecting the differential current at the data-lines and amplifying them to well-defined voltage levels. In the meantime, the always-conducting MN1 and MN2 devices present a low input resistance to the input nodes of the cross-coupled latch at the source terminals of MN3 and MN4. Therefore, not only is the sensing speed of this circuit insensitive to the parasitic bit-line capacitances, it is also insensitive to the parasitic data-line capacitances.

Figure 5.16 The hybrid current-mode sense amplifier.

An improved current-mode sense amplifier with a modified current conveyor was developed, as shown in Figure 5.17 [133]. It closely resembles the hybrid sense amplifier presented earlier, with just an additional pMOS transistor MP7 in the modified current conveyor. The circuit shows performance leverage over the conventional sense amplifier by resolving the problem associated with pattern dependency, which limits the scaling of the operating voltage. Without MP7, the nodes RXP and RXN get floated after each read operation and there exists a residual differential voltage between nodes RXP and RXN. When the same logic value is being read out from the same column for several times consecutively, the residual differential voltage will be amplified further. If the new data to be read is the same as the previous one, the amplified voltage strengthens the signal development. However, if the new data is different from the previous one, the amplified voltage will obstruct the normal read operation and hence, the pattern dependency problem occurs. In some cases, a read-out error may be caused if the differential data current is not sufficient to override the amplified voltage. By adding the equalization

transistor MP7, which will be turned on after every read cycle, nodes RXP and RXN are equalized and thus eliminating any residual differential voltage between them.

Figure 5.17 An improved current-mode sense amplifier with a modified current conveyor.

Another current sense amplifier for low-power and high-speed CMOS SRAMs is depicted in Figure 5.18 [134]. It has the ability to transform itself into a latch soon after a differential current signal appears at nodes A and B . Assume that the accessed memory cell stores a logic “0”. Differential current will flow across the bit-lines with BL passing less current than its $\overline{\text{BL}}$ counterpart. Sufficient time delay is provided by the inverter, INV, so that the differential current can appear at nodes A and B before turning off transistors MP6 and MP7. Immediately after MP6 and MP7 are cut off, the conveyor transforms into a latch. The regenerative effect of the flip-flop action is swift, and causes the potential at node B to rise more rapidly than that at node A . Following that, the transistor MP3 turns off and hence the BL current will be truncated, leaving only $\overline{\text{BL}}$ to flow through the conveyor. As a result, a large differential voltage is developed over the

data-lines, thereby significantly reducing the sensing delay of the sense amplifier. In the meantime, low-power consumption is achieved since only one branch of current is allowed to flow through the conveyor. As for the current-to-voltage conversion stage, it uses the conventional differential current-mirror sense amplifier with a single-ended output.

Figure 5.18 The low-power current sense amplifier.

5.6 Proposed Designs of Low-Power High-Performance Current Sense Amplifier

Sensing current instead of voltage presents an alternative solution to signaling on the lengthening wires that are increasingly limiting the performance of CMOS as it scales into the deep sub-micrometer regime. In this section, we present three competitive designs of current sense amplifiers for use in low-power and high-performance applications.

5.6.1 Current Conveyor Amplifier for Low-Voltage High-Speed Applications

The proposed current sense amplifier together with a simplified read-cycle-only memory system is shown in Figure 5.19. It consists of eight pMOSFETs (P21, P22, P23, P24, P31, P32, P33 and P34) and four nMOSFETs (N5, N6, N7 and N8). It can be seen that transistors P31, P32, P33 and P34 forms a conventional current conveyor, which has been reported earlier in Section 5.5.3. Therefore, the new circuit is also insensitive to the bit-line capacitance. It is designed to improve the poor sensing speed of the conventional current conveyor with the basic idea of amplifying the bit-line currents in order to increase the sensing speed. C_{BL} and C_{DL} signify the bit-line and data-line capacitances, respectively, whereas RS and CS denote the row- and column-select.

In order to increase the sensing speed, the current signals to the data-lines should be large so that the charging time of the data-line capacitances is greatly reduced. Consider both the $RS1$ and $CS1$ lines being activated during a read cycle. The differential current signals that appear at the common bit-lines then propagate to current mirrors (N5, N6 and N7, N8). The two pairs of current mirrors have the same aspect ratio to avoid amplification. The currents are not amplified yet to save power. However, the currents involved are sinking currents, and not sourced currents. To change the current direction, two pMOS current mirrors (P21, P22 and P23, P24) are used. These two pMOS current mirrors are also used as current amplifiers. The current signals appearing at the input of the differential amplifier will be amplified and available at the output, V_o .

Figure 5.19 The proposed current conveyor amplifier and a simplified read-cycle-only memory system.

Two representative current sense amplifiers reported in the previous section, namely the conventional current sense amplifier [129] with zero input resistance while sensing, and the low-power sense amplifier [134], which has the ability to transform into a latch, were also simulated together with the proposed current conveyor amplifier based on a simplified read-cycle-only memory system. For ease of explanation, the former current sense amplifier will hereafter be referred to as the conventional circuit, while the low-power sense amplifier will be named the low-power circuit.

In an effort to gauge the actual behavior and performance of the circuits in comparison, extensive simulations have been carried out on a complete and identical set of four memory cells together with their different methods of data sensing. This simulation approach is sufficient for testing and verifying the reliability and functionality of all the sense amplifiers. Each memory cell is alternatively activated using $RS1$ or $RS2$, and $CS1$ or $CS2$, and hence the stored data, be it a one or a zero is detected by the sense amplifier. The graph showing the waveforms of the output V_o , along with their corresponding RS and CS signals are depicted in Figure 5.20. The simulation is realized using Cadence's Affirma Spectre circuit simulator [135], with the 1.8 V/0.18 μm CMOS technology from CHRT.

The IC layout compaction and optimization of all the circuits have been implemented according to CHRT's 0.18 μm 6M1P n-well p-substrate CMOS design rules. In the meantime, transistor matching requirements have been considered while drawing the layout. For example, the multi-gate finger layout structure has been incorporated where the differential transistor pairs have been matched by sharing the same source/drain terminal. The three sense amplifier topologies are comparatively evaluated based on approximately the same area, in terms of the propagation delay and average power dissipation with different bit- and data-line capacitances. The active chip areas for the conventional, the low-power, and the proposed (with layout shown in Figure 5.21) sense amplifiers are 615.18 μm^2 , 658.68 μm^2 , and 632.91 μm^2 , respectively.

Figure 5.20 Transient waveform of the output voltage V_o for the proposed current conveyor amplifier with the RS and CS signals for 1.8 V/0.18 μ m technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF and $C_{DL} = 1.0$ pF.

Figure 5.21 Layout of the proposed current conveyor amplifier.

The effect of bit-line capacitances on both propagation delay and average power consumption is shown in Figure 5.22. All the three circuits are insensitive to the bit-line capacitances. The new circuit has the lowest propagation delay (i.e. fastest sensing speed), However, it has the highest power consumption as compared to the other two circuits. The power consumption for the new circuit is below 1.5 mW, which is still sufficiently low for portable applications. For the case where C_L has a capacitive load of 0.1 pF with $C_{BL} = 5$ pF, $C_{DL} = 1$ pF, the speed of the new circuit is 49.6% and 18.7% faster than the conventional circuit and the low-power circuit, respectively.

Figure 5.22 Sensing delay and average power dissipation against bit-line capacitances for 1.8 V/0.18 μ m technology, $C_L = 1.0$ pF, $C_{DL} = 1.0$ pF.

The sensing delay with respect to the data-line capacitances for the 1.8 V/0.18 μm technology is illustrated in Figure 5.23. Unlike the conventional circuit, the sensing delay of the proposed current conveyor amplifier is less sensitive to changes in the data-line capacitances. More specifically, its sensing delay sensitivity with respect to the data-line capacitances is only 224 ps/pF as compared to 373 ps/pF for the conventional circuit. The improvement in speed for the new circuit is even more significant for higher data-line capacitances. For the case which C_L has a capacitive load of 0.1 pF with $C_{BL} = 1$ pF, $C_{DL} = 5$ pF, the speed of the new circuit is 56.5% and 13.2% faster than the conventional circuit and the low-power circuit, respectively. Hence the proposed current conveyor amplifier is very suitable for use in high density SRAMs.

Figure 5.23 Sensing delay and average power dissipation against data-line capacitances for 1.8 V/0.18 μm technology, $C_L = 1.0$ pF, $C_{BL} = 1.0$ pF.

Table 5.1 shows the simulation results of the various circuits in comparison for $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF, $C_{DL} = 5.0$ pF at 1.8 V/0.18 μ m technology and 50 MHz operating frequency.

Table 5.1 Comparison of the proposed current conveyor amplifier with its various contemporary counterparts for $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF, $C_{DL} = 5.0$ pF at 1.8 V/0.18 μ m technology and 50 MHz operating frequency.

Current sense amplifiers	Conventional circuit	Hybrid circuit	Low-power circuit	Proposed current conveyor amplifier
Layout area, μm^2	615.18	569.83	658.68	632.91
Sensing delay, ns	3.09	1.10	2.24	1.98
Power dissipation, mW	1.13	1.46	0.67	1.28
Power-delay product, pJ	3.48	1.60	1.50	2.54

The proposed current conveyor amplifier has successfully tackled the disadvantage of slow speed performance of the conventional and low-power circuit. However, as can be seen from Figure 5.23, its sensing delay is still quite sensitive to variations in data-line capacitances. This is because of the usage of the conventional differential current-mirror amplifier as its current-to-voltage converter stage, which is apparently operating in voltage mode. In addition, despite its speed advantage, there is still much room for improvement in terms of power dissipation. This gives birth to the high-performance low-power current sense amplifier using a cross-coupled current-mirror configuration as detailed in Section 5.6.2.

5.6.2 High-Performance Low-Power Current Sense Amplifier using a Cross-Coupled Current-Mirror Configuration

The second proposed current sense amplifier, which is shown in Figure 5.24, achieves a fast sensing speed without compromising its power dissipation. Similar to the first design, its fundamental concept is to strengthen and amplify the differential current

signals across the bit-lines in order to enhance the sensing speed. Meanwhile, the new design has extracted the gist of the conventional current sense amplifier by including the transistors P41, P42, P43 and P44 forming a conventional current conveyor. As a result, the new circuit is bit-line capacitance insensitive. Figure 5.24 also includes a CMOS amplifier (N15, N16, P45, P46 and P47) and a data-line equalization circuit. This proposed circuit will, thereafter be referred to as the high-speed circuit.

During the read cycle, when $RS2$ and $CS1$ are activated, the memory cell at the left column and lower row will be selected, resulting in a higher current flow through BL than that at $\overline{BL}$. These differential current signals that appear at the bit-lines will propagate to two pairs of current mirror (N11, N12 and N13, N14). The current mirrors increase the current transmitted from the bit-lines by the same amplification ratio. After current intensification, the bit-line currents are considered sufficiently large to greatly enhance the sensing speed. In spite of this, the current mirrors act as current sink instead of current source. Hence, the conventional differential current-mirror voltage sense amplifier (Figure 5.8) is not compatible with this novel circuit. The new current-mode amplifier (N15, N16, P45, P46 and P47) is therefore designed to use the current sink. Since the current through N12 is larger than at N13, node E is discharged to a potential lower than node F ($V_E < V_F$). The aspect ratios for N12 and N15 must be carefully designed to sink the current from node C . Coupled with the fact that the gates of N15 and N16 are initially clamped at a same potential by the signal EQ , the magnitude of the gate to source voltage of N15 ($V_{GS(N15)}$) is higher than that of the $V_{GS(N16)}$. To ensure efficient operation of the circuit, the EQ signal can only be released after the current from the bit-lines resides at the data-lines. Owing to the sinking transistor N15 rendering higher V_{GS} than N16, the voltage at node C is lower than the voltage at node D . Furthermore, the amplifier with cross-coupled configuration implies that the source to gate voltage of P45 ($V_{SG(P45)}$) is less than the $V_{SG(P46)}$. The current flowing towards node D will therefore be much higher than node C . The voltage at node D then increases further and the voltage at node C decreases. This process will continue until the output V_o reaches V_{DD} . Figure 5.25 shows the voltages at different nodes during a read cycle.

Figure 5.24 The proposed high-speed circuit using a cross-coupled current-mirror configuration with a simplified read-cycle-only memory system.

Figure 5.25

Transient voltage waveforms for various nodes of the proposed high-speed circuit for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF and $C_{DL} = 1.0$ pF.

Extensive circuit simulations have been carried out by using the identical simulation environment based on the four memory cells as detailed in Section 5.6.1 to verify the operation of the proposed high-speed sense amplifier and characterize its performance. The graph showing the waveforms of the outputs V_o and $\overline{V}_o$, along with their corresponding RS and CS signals are depicted in Figure 5.26. It has also been compared with the conventional circuit, the low-power circuit and the hybrid current sense amplifier [132], which has bit-line and data-line capacitances independent (ideally) sensing speed. Besides, the current conveyor amplifier proposed in the previous section is also included for comparison. All the five circuits are simulated together with a simplified read-cycle-only memory system. They are comparatively evaluated in terms of the propagation delay and average power dissipation with different bit- and data-line capacitances. The layout of the proposed high-speed current sense amplifier is shown in Figure 5.27, with an active chip area of $659.12 \mu\text{m}^2$. Meanwhile, the conventional, hybrid, low-power, current conveyor amplifier circuits occupy an area of $615.18 \mu\text{m}^2$, $569.83 \mu\text{m}^2$, $658.68 \mu\text{m}^2$, and $632.91 \mu\text{m}^2$, respectively. The layouts are drawn according to CHRT's $0.18 \mu\text{m}$ 6M1P n-well p-substrate CMOS design rules.

Figure 5.26 Transient waveform of the output voltages V_o and $\overline{V_o}$ for the proposed high-speed circuit with the RS and CS signals for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF and $C_{DL} = 1.0$ pF.

Figure 5.27 Layout of the proposed high-speed circuit.

The effects of bit-line capacitances on propagation delay is shown in Figure 5.28. All the five circuits are insensitive to the bit-line capacitances. The new circuit has the lowest propagation delay (i.e. fastest sensing speed). For the case which C_L has a capacitive load of 0.1 pF with $C_{BL} = C_{DL} = 1$ pF, the speed of the new circuit is 68.5%, 10.5%, 34.4%, and 13.7% faster than the conventional, the hybrid, the low-power, and the current conveyor amplifier circuits, respectively.

Figure 5.28 Sensing delay against bit-line capacitances for 1.8 V/0.18 μ m technology, $C_L = 0.1$ pF, $C_{DL} = 1.0$ pF.

The sensing delay with respect to the data-line capacitances is illustrated in Figure 5.29. Unlike the conventional circuit, the low-power circuit, and the current conveyor amplifier, the sensing delay of the proposed high-speed circuit is almost insensitive to the data-line capacitance. Its sensitivity is only a trivial 22 ps/pF as compared to 373 ps/pF, 240 ps/pF, and 224 ps/pF for the conventional, the low-power, and current conveyor amplifier circuits, respectively. The improvement in speed for the new circuit is even more pronounced at higher data-line capacitances. For the case which C_L has a capacitive load of 0.1 pF with $C_{BL} = 1$ pF, $C_{DL} = 5$ pF, the speed of the new circuit is 198.2%, 6%, 115.7%, and 90.6% faster than the conventional, the hybrid, the low-power, and the current conveyor amplifier circuits, respectively. Hence the proposed high-speed circuit is very suitable for use in high-speed low-power SRAMs.

Figure 5.29 Sensing delay against data-line capacitances for 1.8 V/0.18 μ m technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF.

The average power consumption with respect to bit-line capacitance for all circuits in comparison is depicted in Figure 5.30. The power efficiency of the proposed high-speed current sense amplifier is much greater as compared to the conventional, the hybrid, and current conveyor amplifier circuits. Although its power consumption is higher than the low-power circuit, it will be shown in due course that the proposed high-speed circuit exhibits an enhanced PDP as compared to its conventional and contemporary counterparts.

Figure 5.30 Average power dissipation against bit-line capacitances for 1.8 V/0.18 μ m technology, $C_L = 0.1$ pF, $C_{DL} = 1.0$ pF.

The PDP performance with respect to the variations in bit-line and data-line capacitances is illustrated in Figures 5.31 and 5.32, respectively. It can be observed that the proposed high-speed current sense amplifier offers the lowest PDP when compared to all other circuits in comparison. For instance, at $C_L = 0.1$ pF, $C_{BL} = 5$ pF, and $C_{DL} = 1$ pF, the PDP of the high-speed circuit is only 0.78 pJ, which is 106.8%, 94%, 12.7%, and 103.48% lower than those of the conventional, hybrid, low-power, and current conveyor amplifier circuits.

Figure 5.31 Power-Delay Product (PDP) against bit-line capacitances for 1.8 V/0.18 μ m technology, $C_L = 0.1$ pF, $C_{DL} = 1.0$ pF.

Figure 5.32 Power-Delay Product (PDP) against data-line capacitances for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{DL} = 1.0$ pF.

A comparison of the various current sense amplifiers simulated at 1.8 V/0.18 μm technology and 50 MHz operating frequency for $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF, $C_{DL} = 5.0$ pF is tabulated in Table 5.2.

Table 5.2 Comparison of the proposed high-speed circuit with its various contemporary counterparts for $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF, $C_{DL} = 5.0$ pF at 1.8 V/0.18 μm technology and 50 MHz operating frequency.

Current sense amplifiers	Conventional circuit	Hybrid circuit	Low-power circuit	Current conveyor amplifier	Proposed high-speed circuit
Layout area, μm^2	615.18	569.83	658.68	632.91	659.12
Sensing delay, ns	3.09	1.10	2.24	1.98	1.04
Power dissipation, mW	1.13	1.46	0.67	1.28	1.04
Power-delay product, pJ	3.48	1.60	1.50	2.54	1.07

It is noted that even though the sensing delay and the PDP of the proposed high-speed circuit is the best among the circuits compared, its power dissipation is still inferior to the low-power circuit. In view of that, a new ultra low-power circuit was designed to remedy this shortcoming with the intention to further reduce the PDP.

5.6.3 An Ultra Low-Power Current Sense Amplifier

In this section, we propose a novel current-mode sense amplifier, which has sub-mW order power dissipation and enhanced PDP, while maintaining high-speed sensing and small area required in SRAM application. The performance of this current sense amplifier is also compared with four other sense amplifiers reported to-date. Addressing them individually, they are the conventional circuit, the hybrid circuit, the low-power circuit, and our previous designs as presented in Section 5.6.1 and Section 5.6.2, namely, the current conveyor amplifier and the high-speed current sense amplifier employing current-mirror configuration.

The proposed ultra low-power current sense amplifier, coupled with a simplified read-cycle-only memory system, is portrayed in Figure 5.33. It has integrated the gist of the conventional current sense amplifier by including the transistors P31, P32, P33 and

P34 operating in saturation. Owing to the assimilation of this current conveyor, the new circuit is intrinsically bit-line capacitance insensitive since it has (ideally) zero input resistance during sensing. It also incorporates a current amplifier, made up of two pairs of current mirrors at each bit-lines, which aims to amplify the bit-line current and thus enhancing the sensing speed. Following that, Figure 5.33 embraces a cross-coupled CMOS amplifier (N15, N16, P45, P46 and N47) for global sensing. The complementary signals of the CMOS amplifier will feed their respective output sections, which are inverter stages, each cascoded with an additional nMOS transistor. This supposedly minor tweak will aid in minimizing a major proportion of the unnecessary power dissipation. Data-line equalization is not compulsory in this circuit due to the inherent equalizing action of transistor N47.

Consider both $RS1$ and $CS1$ being activated during a read operation. The memory cell at the upper row and left column will be selected, resulting in a smaller current flow through BL than that at $\overline{BL}$. These differential current signals that appear at the common bit-lines will then propagate to two pairs of nMOS current mirrors (N5, N6 and N7, N8). In view of the fact that P31, P32, P33 and P34 have to be in saturation mode to ensure a bit-line capacitance insensitive sensing delay, the drains of P33 and P34 are pulled to a low voltage with the aid of the relatively large-sized N5 and N8. Meanwhile, the widths of N6 and N7 are appropriately sized to a smaller dimension to avoid non-essential power wastage. However, the current mirrors at this stage act as current sinks instead of current sources. Two pMOS current mirrors (P21, P22 and P23, P24) are therefore included to change the current direction to comply with our novel design of the power saving cross-coupled CMOS latch. These two pMOS current mirrors also double up as current amplifiers, which serve the purpose of increasing the current transmitted from the bit-lines by the same amplification ratio. After current intensification, the bit-line currents are considered adequately large to enhance the sensing speed.

Prior to the read cycle, nodes C and D are clamped at the same potential by the pre-equalizing signal, EQ . This voltage-clamping signal can only be released after the differential current from the bit-lines resides at the data-lines to establish a correct data output. Since the current through P22 is smaller than its P23 counterpart, node E is charged to a potential lower than node F ($V_E < V_F$). Coupled with the fact that the gates of

P45 and P46 are initially clamped at an equal potential, the magnitude of the source to gate voltage of P45 ($V_{SG(P45)}$) is smaller than that of the $V_{SG(P46)}$. As a result, the voltage at node *C* is lower than the voltage at node *D*. Moreover, the CMOS amplifier, which is arranged in a cross-coupled configuration, causes the gate to source voltage of N15 ($V_{GS(N15)}$) to be higher than $V_{GS(N16)}$. Due to the regenerative effect of this positive feedback structure, the current sinking from node *D* will therefore be much lower than node *C*. The voltage at node *D* then increases further and the voltage at node *C* decreases. This process will continue until the output V_o discharges to V_{SS} .

The new current sense amplifier is capable of achieving an ultra low-power dissipation due to the existence of the nMOS devices (N3 and N4) connected in cascode with the output inverters. The control signal, $Q1$, is unasserted during the standby mode, hence keeping the nMOS transistors in cut-off. The inactive nMOS device inhibits the possibility of a DC current path flowing through V_{DD} and V_{SS} . Following that, a hefty portion of the unnecessary power dissipation is conserved. Figure 5.34 illustrates graphically the voltages at different nodes during a read cycle.

Figure 5.34 Transient voltage waveforms for various nodes of the proposed ultra low-power circuit at 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF and $C_{DL} = 5.0$ pF.

Extensive circuit simulations have been carried out by using the identical simulation environment based on the four memory cells, as detailed in Section 5.6.1, to verify the operation of the proposed ultra low-power sense amplifier and characterize its performance. The graph showing the waveforms of the outputs V_o and $\overline{V}_o$, along with their corresponding RS and CS signals are depicted in Figure 5.35. All the six circuits are simulated together with a simplified read-cycle-only memory system.

The transistor sizes of the respective designs of sense amplifiers have been fully optimized to achieve minimum PDP, based on similar silicon area consumption. Although the proposed ultra low-power sense amplifier involves a seemingly larger number of transistors, the optimized sizes of the devices are actually smaller and thus, do not deteriorate its overall small-area advantage. The layout drawing of the new sense amplifier is shown in Figure 5.36. Its active chip area is $579.94 \mu\text{m}^2$, whereas those of the conventional, hybrid, low-power, current conveyor amplifier, and high-speed sense amplifiers are $615.18 \mu\text{m}^2$, $569.83 \mu\text{m}^2$, $658.68 \mu\text{m}^2$, $632.91 \mu\text{m}^2$, and $659.12 \mu\text{m}^2$, respectively.

In addition, to test the robustness of the circuit against process variations, the proposed ultra low-power sense amplifier circuit has been simulated at the typical as well as the extreme process corners, namely the slow-slow and fast-fast MOS models. The circuit has been proven to be functioning perfectly well for all three environments, without the need to re-optimize the transistor dimensions or re-adjusting the control signals. The results and graphs presented in this dissertation are obtained from the typical model file simulations. For the slow-slow model, its sensing delay is 1.861 ns, power dissipation is 0.3786 mW, whereas the PDP is computed as 0.7046 pJ. As for the fast-fast model, its sensing delay is 1.419 ns, power dissipation is 0.7528 mW, while the PDP is 1.068 pJ.

Figure 5.35 Transient waveform of the output voltages V_o and $\overline{V}_o$ for the ultra low-power circuit with the RS and CS signals for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF and $C_{DL} = 1.0$ pF.

Figure 5.36 Layout of the ultra low-power current sense amplifier.

All the sense amplifiers in comparison (the conventional, hybrid, low-power, current conveyor amplifier, high-speed, and the proposed ultra low-power circuit) are simulated together with a simplified read-cycle-only memory system. They are comparatively evaluated in terms of the propagation delay and average power dissipation with different bit- and data-line capacitances. Meanwhile, PDP is used as the key performance indicator. The average power dissipation with respect to the bit-line and data-line capacitances is illustrated in Figure 5.37 and Figure 5.38, respectively. The new circuit offers the lowest power consumption as compared to the other five sense amplifiers. For a load capacitance, C_L , of 0.1 pF and $C_{BL} = C_{DL} = 1$ pF, the power of the new circuit is 94.1%, 169.5%, 30.3%, 179.4%, and 55.3% lower than the conventional, hybrid, low-power, current conveyor amplifier, and high-speed circuits, respectively.

The sensing delays of all the circuits are insensitive to the bit-line capacitances, as appeared in Figure 5.39. The effect of data-line capacitances on propagation delay is shown in Figure 5.40. Unlike the conventional circuit, the low-power circuit, and the current conveyor amplifier, the sensing delay of the proposed ultra low-power circuit is only slightly sensitive to the data-line capacitances, which is only 50 ps/pF. Its speed performance is intermediate among the circuits compared. It is faster than the conventional circuit and the low-power circuit especially at high data-line capacitances. Even though its speed is slower than its hybrid and high-speed counterparts, this inadequacy can easily be offset by its impressive power advantage. This phenomenon is further corroborated by the PDP computation, which serves as an intuitive and commendable performance metric in ULSI circuit design environment. The PDP comparisons with regard to the bit-line and data-line capacitances are displayed in Figure 5.41 and Figure 5.42, respectively. For both cases, the proposed ultra low-power current sense amplifier exhibits the most pronounced PDP leverage over all other circuits. For example, at $C_L = 0.1$ pF, $C_{BL} = 1$ pF and $C_{DL} = 5$ pF, the new circuit improves the PDP by 314% as compared to the conventional circuit, and 91%, 79%, 202%, and 28% when comparison is made with the hybrid, low-power, current conveyor amplifier, and high-speed sense amplifiers, respectively. The comparison summary for all the sense amplifier designs is tabulated in Table 5.3.

Figure 5.37 Average power dissipation with respect to the changes in bit-line capacitances for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{DL} = 1.0$ pF.

Figure 5.38 Average power dissipation with respect to the changes in data-line capacitances for 1.8 V/0.18 μ m technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF.

Figure 5.39 Sensing delay against bit-line capacitances for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF.

Figure 5.40 Sensing delay against data-line capacitances for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF.

Figure 5.41 Power-Delay Product (PDP) against bit-line capacitances for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{DL} = 1.0$ pF.

Figure 5.42 Power-Delay Product (PDP) against data-line capacitances for 1.8 V/0.18 μm technology, $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF.

Table 5.3 Comparison summary of various circuits for $C_L = 0.1$ pF, $C_{BL} = 1.0$ pF, $C_{DL} = 5.0$ pF at 1.8 V/0.18 μm technology and 50 MHz operating frequency.

Current sense amplifiers	Conventional circuit	Hybrid circuit	Low-power circuit	Current conveyor amplifier	High-speed circuit	Proposed ultra low-power circuit
Layout area, μm^2	615.18	569.83	658.68	632.91	659.12	579.94
Sensing delay, ns	3.09	1.10	2.24	1.98	1.04	1.47
Power dissipation, mW	1.13	1.46	0.67	1.28	1.04	0.57
Power-delay product, pJ	3.48	1.60	1.50	2.54	1.07	0.84

5.7 Summary

This chapter has explored the application of current sensing techniques in memory subsystems using CMOS technology. As a start, a short introduction on the semiconductor memory is included. Following that, an explicit discussion on the SRAM is presented because of its increasing prominence in the SoC era. Due to the potential of the integrated circuit technology to becoming one of the fastest growing segments in semiconductor industry, the density of SRAMs in embedded applications has been multiplied dramatically. This has resulted in a rapid increase in both bit- and data-line capacitances, thereby leading to a major design limitation in achieving higher sensing speed in memory systems. With regard to that, a sense amplifier with quick response time is an essential element in memory design. It is crucial to ensure a robust and reliable read access with a feasible performance, given the weak signaling characteristics of the memory cells. As illustrated in this chapter, the current-mode sense amplifier has gradually replaced the traditional voltage-mode approach for sensing and amplification purposes since current-mode sense amplifier facilitates low-voltage and high-speed operation by providing a very low bit-line and data-line voltage swings. A literature

review embracing the development and evolution of both the voltage- and current-mode SRAM sense amplifiers based on multiple conference and journal papers presenting the conventional and contemporary exploratory approaches on sense amplifier designs have been covered.

Acknowledging the importance of the role of sense amplifier in achieving high-speed sensing, we have proposed three current sense amplifier designs in this chapter. A novel current conveyor amplifier, which is appropriate for high sensing speed and low-voltage operation, has first been proposed. It is evaluated and compared with some existing current sense amplifiers. The static behaviour of the new circuit is analysed and by using Cadence's Affirma Spectre circuit simulator, it is well proven that it exhibits performance superiority over the conventional conveyor. With almost the same chip area, the new circuit gives much higher sensing speed and relatively low power-delay product based on the 1.8 V/0.18 μm CMOS technology. At capacitances $C_L = 0.1$ pF, $C_{BL} = 1$ pF and $C_{DL} = 5$ pF, the proposed design with a chip area of 632.91 μm^2 operates at a pace higher than the conventional circuit and the low-power circuit by 56.5% and 13.2%, correspondingly. In addition, the proposed current conveyor amplifier shows lower sensing delay sensitivity with respect to the data-line capacitances, i.e. 224 ps/pF as compared to 373 ps/pF for the conventional circuit.

Subsequently, a high-performance current sense amplifier with a fast sensing speed is illustrated. The new circuit is appropriate for applications in low-voltage low-power environment. It has been simulated to confirm its superiority over existing current sense amplifier circuits. With almost equivalent chip area, the new circuit promises a much lower sensing delay and permits low power consumption based on the 1.8 V/0.18 μm CMOS technology. At capacitances $C_L = 0.1$ pF, $C_{BL} = 1$ pF and $C_{DL} = 5$ pF, the proposed high-speed circuit improves the sensing speed by 198.2% as compared to the conventional current sense amplifier, and 6% and 115.7% when comparison is made with the hybrid and low-power circuits, respectively. Also, the proposed high-speed circuit exhibits a significant decrease in sensing delay sensitivity with respect to the data-line capacitances, i.e. only a relatively small 22 ps/pF as compared to 373 ps/pF and 240 ps/pF for the conventional and low-power circuits, respectively.

A novel CMOS current-mode sense amplifier with ultra-low power dissipation has also been presented. It is feasible for the state-of-the-art high-density ULSI environment, which highlights the essentiality of low-power, high-speed and small area design. Post-layout simulations using Spectre have confirmed its superiority over a representative set of existing sense amplifiers, namely the conventional, hybrid, low-power, and high-speed designs. With almost equivalent chip area, the new circuit promises significantly reduced power dissipation without compromising its speed performance based on the 1.8 V/0.18 μm CMOS technology. For the case in which C_L has a capacitive load of 0.1 pF with $C_{BL} = C_{DL} = 1$ pF, the power consumption of the new circuit is 94.1%, 169.5%, 30.3% and 55.3% lower than the conventional, hybrid, low-power and high-speed circuits, respectively. Moreover, the sensing speed of the new circuit is independent of the variations in bit-line capacitances. Its sensing delay sensitivity with respect to the data-line capacitances is only a modest 50 ps/pF as compared to 373 ps/pF and 240 ps/pF for the conventional circuit and the low-power circuit, respectively, and is comparable to those of the hybrid and high-speed current sense amplifiers. A further performance comparison based on the PDP shows that the proposed ultra low-power circuit is the candidate of choice when power and speed are of equal design priority.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

Recently, there has been a tremendous surge of interest in high-durability and small-sized handheld personal communication devices and other more sophisticated multimedia-based applications. Consequently, on the road to the embarkation of the System-on-Chip (SoC) era, which hastens the development and realization of high-complexity electronic appliances, the concern over low-power consumption is particularly important. Indeed, it is fast becoming a crucial backbone criterion in circuit design methodology for the leading edge Ultra-Large-Scale-Integration (ULSI) engineering. More importantly, with the demand for deep sub-micrometer, or even the sub-nanometer region VLSI/ULSI technology, where device sizes continue to shrink into miniaturized dimensions at apparently higher speed, the requirement for low-power consumption becomes increasingly prominent. Indeed, the demand for low-power consumption has been at the forefront of active development for digital integrated circuits.

Scaling down the power supply voltage has been a common way of reducing power dissipation. However, this simple strategy comes at a heavy price: significant degradation in speed performance and noise immunity. Downscaling of the power supply voltage entails reduction in the drive current, which in turn, leads to speed degradation. This issue will be exacerbated by the increase in packing density: more interconnects that come with higher packing density to bring about more RC delay. On top of that, reducing the supply voltage reduces the readout voltage amplitude on the bit-lines (as in SRAM), which will reduce noise immunity. Hence, innovative circuit design techniques, which circumvent the pitfalls of degradation in power consumption and speed performance, are often explored for low-power high-performance signal processing.

This dissertation focuses on the design methodologies to improve the performance of CMOS subsystems, which encompass critical elements that execute elementary and

crucial operations in SoCs. We have identified the building blocks that consume excessive power and in turn addressed the power consumption issue, namely adders, comparators, and memories. These are the fundamental and essential blocks that coexist in a SoC. We have outlined in this dissertation several techniques for designing CMOS subsystems, which are feasible for achieving power saving and speed efficiency, while attaining a small-area attribute.

The addition operation is a most frequently used operation in general-purpose systems and application-specific processors. Due to the carry propagation step that comes with the addition operation, substantial circuit delay will be introduced if proper circuit design techniques were not implemented. This is especially true since the adders lie in the critical delay path. As far as time-critical high-performance designs are concerned, the Carry Look-Ahead (CLA) has been the most preferred choice due to its logarithmic delay time. However, this high-speed advantage comes at the expense of an increase in area consumption. On the other hand, the Ripple Carry Adder (RCA) complements the CLA by offering the most compact design but suffers from a long delay deficiency. In an effort to merge the advantages of the CLA and RCA, the Carry Select Adder (CSL) serves as a valuable compromise in terms of area usage and speed performance in Carry Propagate Adder (CPA) design. Therefore, the CSL has been identified as the contender for incorporation in many high-end applications where speed, area, and power are of paramount importance. In conjunction with that, a high-performance adder based on the conventional square root CSL scheme and a modified add-one circuit has been proposed. The new proposed circuit successfully overcame the weaknesses of the preceding add-one CSL circuits. It improved significantly in terms of computation speed and power consumption while promising an attractive small-area feature, as verified by the extensive simulation results using the 1.8 V/0.18 μm CMOS process from Chartered Semiconductor Manufacturing Pte. Ltd. (CHRT). For a 64-bit addition, our proposed CSL is 14.7% faster and consumes 39.87% less power than the conventional CSL.

Historically, the design of both the digital and analog parts of arithmetic circuits has been dominated by the voltage-mode approach. However, the increasing need to develop more advanced circuits using reduced wiring complexity and lower device counts per function has weakened its dominance, resulting in the revitalization of the

interest in current-mode design methods. Consequently, Multiple-Valued Logic (MVL), which successfully addresses the issue of excessive interconnect in the conventional binary voltage-mode design, has become increasingly important. MVL requires more than two discrete levels of logic signals, which are better represented in Current Mode (CM) by specific current values, hence resulting in the birth of the Current-Mode Multiple-Valued Logic (CMMVL). Lying at the heart of a CMMVL circuitry is the current-mode comparator. Most of the CMOS current-mode comparators assume that the input current is the difference between a threshold current and an actual input current signal. They produce a two-level output voltage in response to the polarity of the input currents, rather than performing current detection based on a pre-defined value of the threshold current. Moreover, the circuit structure that realizes such current subtraction, which is an imperative entity of the current comparator, is not illustrated in these designs. A simple area-efficient CMOS low current comparator attending to the above-mentioned scarcity has been proposed. It offers tremendous superiority in terms of area consumption, without sacrificing power and speed performance. More importantly, the area advantage becomes more significant with reducing feature size. This feature blends well with the contemporary and ongoing process technology miniaturization. Besides, to provide a more complete and eloquent circuit evaluation, the proposed current-mode comparator has been implemented into a one-stage Positive-Digit Adder (PDA), which is an illustrative example of the CMMVL circuits.

The ever-increasing gap in speed performance between the faster processor and the slower DRAM-based main memory has imposed a serious bottleneck on data access time. Further advances on the processor speed yield limited performance merits due to this bottleneck. The SRAM-based cache memory is used to circumvent this issue. However, due to the need to access the data frequently, power consumption in the cache constitutes a major portion of the total chip power consumption. As mentioned earlier, one of the most frequently employed methods to minimize power consumption is to reduce the power supply voltage. Nonetheless, this gives rise to some critical problems, especially in memory circuits where the time-delay to sense the signals from the memory cells increases drastically, as well as degradation of the readout voltage amplitude on the bit-lines. Due to the immensity of this issue, designing a sense amplifier with high

sensitivity for SRAM applications is one of the prime concerns of this research. Altogether, a total of three circuits adopting the current-mode approach have been proposed in this dissertation. These circuits have shown significant Power-Delay Product (PDP) enhancement as compared to the contemporary designs.

6.2 Recommendations for Future Research

The author has reviewed her own work extensively, and proposes the following for potential future research:

- 1) Due to the greatly increased data processing loads of future applications, the proposed 64-bit CSL design can be extended to realize an addition scheme with higher number of data bits as necessary. On top of that, the proposed adder can be integrated into the multiplier and datapath of any processor to enhance the overall speed performance and power consumption of the system. This serves as another test vehicle to verify the capability of the proposed adder to sustain its performance advantages at higher system levels.
- 2) Further work should investigate other applications that could benefit from the area-efficiency of the proposed current comparator. The proposed current comparator can be implemented into applications, where it is extensively used, such as the Analog-to-Digital Converter (ADC), arithmetic-intensive circuitry and VLSI neural network. Moreover, it is also commonly used in temperature sensors and photo sensors to detect weak current signals. Lowering the area of the current comparator of the CMMVL circuit leads to compact Processing Elements (PEs) and a noteworthy area saving of the overall die size for these applications.
- 3) All the proposed circuits in the dissertation should be fabricated to evaluate their performance and practicality in an actual chip environment. This will include testing, measurement and comparison. Moreover, the fabricated chip should be subjected to stress tests, such as extreme temperatures. Other than that, sensitivity analysis with regard to the device and process parametric variations should be performed. This is particularly

important in deep sub-micrometer, where the changes in the key physical parameters of MOSFETs will have a profound impact on their characteristics and performance. These changes in the process parameters may significantly affect one or more device parameters, which may in turn affect the overall circuit performance, i.e. speed and power sensitivity.

Author's Publications

Journal:

- [1] K. S. Yeo, W. L. Goh, Z. H. Kong, Q. X. Zhang, and W. G. Yeo, "A high-performance low-power current sense amplifier using a cross-coupled current-mirror configuration," *IEE Proc. Circuits, Devices, Sysys*, vol. 149, no. 5, pp. 308-314, Oct./Dec. 2002.
- [2] K. S. Yeo, and Z. H. Kong, "ESD robust and area-efficient circle-type layout design for CMOS output buffers," *Journal of Electrostatics*, vol. 61, issue 3-4, pp. 189-196, 2004.
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- [5] Z. H. Kong and K. S. Yeo, "Design of a low-power high-performance 64-bit carry-select adder," submitted to *IEE Proc. Circuits, Devices, Sysys*.
- [6] K. S. Yeo and Z. H. Kong, "SPICESoft: Automated tool for sensitivity analysis, performance analysis and inverse performance analysis of digital circuits," submitted to *Journal of Circuits, Syst., Computers*, pending second revision.

Conference:

- [1] K.S. Yeo, Z.H. Kong, W.L. Goh, Q.X. Zhang, and W.G. Yeo, "A new current conveyor amplifier for low-voltage high-speed application," in *International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA)*, Oct. 2003, pp. 235-238.

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