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HIGH FREQUENCY NOISE IN DEEP-SUBMICROMETER SILICON MOSFETS

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2011

Acknowledgement

Approaching the destination of my postgraduate study, I retrospect the past three years – an exploration in a scientific domain, an understanding of a profession, and a process of building up a philosophy. There are many people who have helped in shaping my intellectual and personal growth. The completion of this thesis would not have been successful without the generous help from them.

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Summary

The continuous downscaling of device feature size makes CMOS technology an attractive alternative for RF circuits because of its low cost, low power, and high integration capability. However, when working at high frequencies, the noise generated within CMOS device itself plays an increasingly important role in the overall noise performance of analog circuits. In this work, different aspects of high frequency noise characteristics of deep sub-micrometer MOSFETs are investigated.

We analyzed the hot carrier induced interface damage and its spatial location (either at source- or drain-side) on high frequency noise in 0.18 μm NMOSFET. It was found that device noise degraded more significantly if the damage is localized at source than that at drain side. The difference is caused by larger impendence field presents near the source junction. This experimental results provide direct evidence that source side plays a more dominant role in determining the overall noise performance in short-channel MOSFETs.

We investigated the role of shallow Si/SiO_2 interface states on NMOSFET channel noise. A new physical mechanism of channel noise generation by capture and emission of channel carriers at shallow interface states was proposed. Interface states with activation energy as small as 0.03eV was experimentally verified to be responsible for the channel noise increment at high frequencies.

To extend the study of Si/SiO_2 interface states on high frequency noise, NMOSFET noise performance under different types of hot carrier stresses were presented and compared. The results show that the degradation of noise parameters strongly depend on the defect types (interface states or oxide traps) generated during stress. Much larger noise increment was observed on device with high interface states

generation (maximum substrate current $I_{B,max}$ stress and hot hole injection) than that with high oxide traps generation (hot electron injection).

Furthermore, RF noise in both N- and P-MOSFETs under forward body bias were characterized and analyzed in detail. Experimental results show that the high frequency noise is increased with the body bias, and can be qualitatively explained by nonequilibrium channel noise and substrate resistance noise. The increase in high frequency noise in PMOS was found to be predominately caused by the increase in substrate resistance noise, whereas noise increment in NMOS was attributed to a combinational effect of substrate resistance noise and nonequilibrium channel noise.

Table of Contents

List of Acronyms

AC	Alternative Current
CMOS	Complementary MOS
DC	Direct Current
DUT	Device Under Test
FBB	Forward Body Biasing
GHz	Giga Hertz
GPS	Global Positioning System
HC	Hot Carrier
HCI	Hot Carrier Injection
HBT	Hetero-junction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IFM	Impedance Field Method
LNA	Low Noise Amplifier
MOSFET	Metal-Oxide-Semiconductor-Field-Effect Transistor
NBTI	Negative Bias Temperature Instability
NMOSFET	*n*-type MOS Transistor
PAN	Personal Area Networks
PMOSFET	*p*-type MOS Transistor
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuits
WLANs	Wireless Local Area Neworks
ZBB	Zero Body Bias

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Why CMOS for RFIC Applications?

In the last decade, there is substantial growth in the market of wireless communication systems, including cellular phones, cellular base station amplifiers, Global Positioning System (GPS), wireless local area networks (WLANs), wireless personal area networks (PAN) and Gigabit wireless networks [1]. The speed is an important parameter in evaluating the performance of wireless communications, therefore it is necessary to increase the carrier frequency and spectral efficiency to expand the metric of wireless communication systems [2].

Traditionally, the majority of radio frequency integrated circuits (RFICs) are implemented by III-V compound or silicon bipolar technologies. However, with aggressive scaling in device feature size and development in fabrication technology, operating frequency of CMOS devices has been dramatically improved [3-10]. For example, cut-off frequency (f_T) of 300 GHz and 230 GHz for NMOS and PMOS has been demonstrated for transistors with a gate length of 35 nm by 45-*n*m standard CMOS technology [11]. Figure 1.1 shows a comparison of competing technologies in f_T for SiGe hetero-junction bipolar transistor (HBT), InP HBT, GaAs high-electron mobility transistor (HEMT) and CMOS transistors. It clearly suggests that MOSFET today is already a challenging alternative for high speed applications. Furthermore, CMOS platform is superior to other technology platform because it is most cost

effective and provides great integration density and power savings for large-scale integrated chips. All of these advantages have made CMOS become today's mainstream for wireless and personal electronic systems.

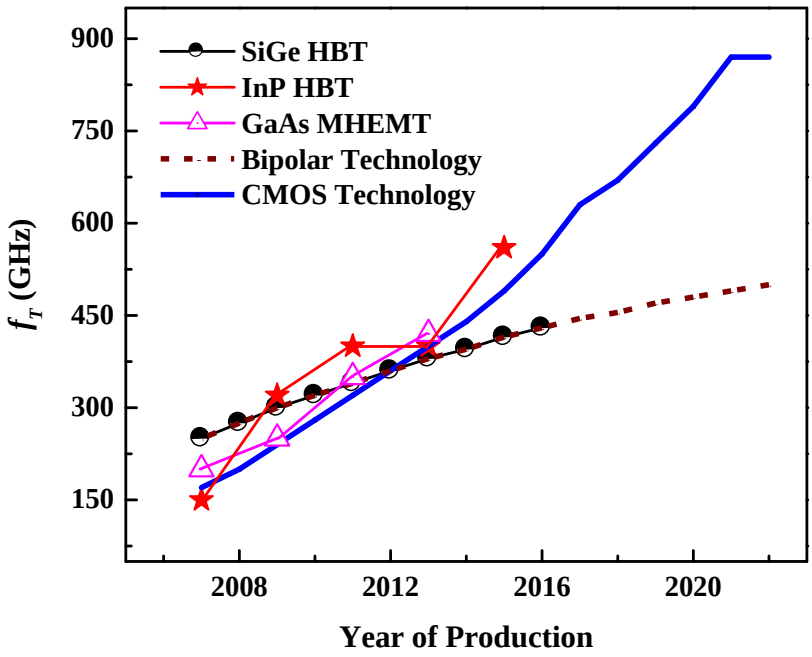


Figure 1.1: Cutoff frequency f_T versus year of production for different process technologies from 2009 ITRS Roadmap Update [2].

1.2 The Importance of High Frequency Noise in RFICs

Understanding noise in electronics is extremely important in wireless communications. The performance of many of communication systems is affected by noise in various ways. For example, electrical noise is one of the key factors which determine the maximum possible communication speed; it also determines the number of users sharing the same transmission media. In high precision measurement systems, electrical noise limits the maximum achievable precision level. Because of all these practical considerations, there is an enormous growth in interest in low-noise RF circuits design. Noise of devices or systems needs to be reliably quantified so that

RFIC designers can save development time and cost by eliminating trial and error. However, as the operating frequency of the signal increases, lots of parasitic components (gate resistance, substrate resistance, drain/source to body capacitance, etc.) need to be considered, which made high frequency noise behaviours more difficult to predict and understand [12-13].

During the past few years, the noise performance of Si RF MOSFETs has been improved considerably. NF_{min} at f = 5 GHz as a function of gate length is shown in Figure 1.2. We can clearly see that about 0.2 dB or lower is required for sub-45nm MOSFETs according to ITRS roadmap. However, with MOSFETs scaling down, f_T keeps increasing but the minimum noise figure (NF_{min}) is difficult to scale down due to the increase of gate resistance. So far, for applications where extremely low noise figures at high operating frequencies are required, SiGe HBTs and III–V HEMTs are still preferred to Si MOSFETs.

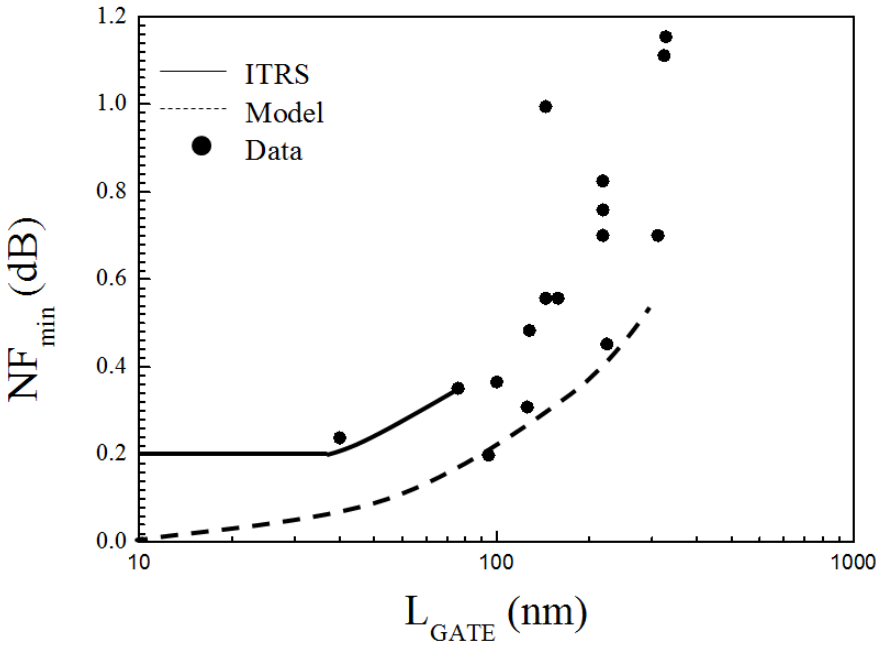


Figure 1.2: Projected NF_{min} (decibels) (at f = 5GHz) versus gate length of MOSFETs in future [14].

1.3 Objectives

Accurate noise modeling is critical in the design of RF circuits, especially for LNA (low noise amplifier) blocks. Since it is indispensable to understand the physical phenomena of high frequency noise and to incorporate this information into the models, lack of understanding of MOSFET noise presents a substantial barrier to the implementation of CMOS in RF circuits. The purpose of this work is to have an in-depth investigation on the high frequency noise in deep submicron MOSFETs in various aspects.

Although the noise parameters in short channel MOSFETs are reported to increase as the channel length scales down, the amount and origin of the increased noise is still debatable. The first objective of this research is to study the spatial origin of the channel noise by comparing the device noise performance with hot carrier damage located at either the source or drain side of the channel.

Several authors have studied the hot carrier effects on RF CMOS noise performance. However, it was still unclear how hot carrier stress can influence the channel noise in deep submicron MOSFETs. Therefore, the second objective of this research is to discuss the physical mechanism of the excess channel noise caused by hot carrier induced Si/SiO_2 interface states at high frequencies.

Based on the magnitude of applied gate voltage in relation to the drain voltage, three different hot carrier degradation modes in NMOSFETs were distinguished. They are low-V_g ($V_{th}<V_g<V_d/2$), mid-V_g ($V_g = V_d/2$), and high-V_g ($V_d/2<V_g<V_d$) modes. It has been reported that the interface states generation is strongly depended on the gate voltage and injected charges. Therefore, the third objective is to compare noise performance of device under three different modes of hot carrier stresses.

Lastly, forward body biasing is used to improve device performance, and studies revealed that 1/*f* noise could also be improved. Therefore, the noise performance of both N- and P-MOSFETs under FBB and the underlying physics is the fourth objective of this research.

1.4 Thesis Outline

The work described in this thesis was motivated by the desire to understand the mechanism of MOSFET high frequency noise and the impact of device degradation on RF noise characteristics. The main results of this study are presented in following chapters.

Chapter 2 gives an introduction to the definition and classification of device noise. Then different kinds of noise sources in MOSFETs and high frequency noise measurement system are described. In Chapter 3, the devices used in the research and test structure layout are introduced. Pad de-embedding method and noise extraction procedure are discussed later.

Chapter 4 investigates hot carrier induced damage and its spatial location on deep-submicron NMOSFET noise performance. It is shown that degradation of noise performance is much greater if the hot carrier induced interface damage is near the source side than the one located at drain side. This is due to larger additional channel noise is generated by the interface damage when they located near source junction. This result provides direct experimental evidence to support the recent theoretical simulation that the localized noise component at source side plays a more important role in determining the overall channel noise in short channel MOSFETs.

Chapter 5 studies the correlation of channel noise degradation and HC induced shallow Si/SiO_2 interface states. A new noise model based on capture and emission at

interface states is proposed, the activation energy and characteristic time constant are also extracted experimentally to verify the new channel noise generation mechanism.

Chapter 6 presents high frequency noise degradation under different modes of hot carrier stresses. Defect types induced by stress are found to be critical on the noise performance. Experimental results show the channel noise is increased significantly if interface states are generated during stress. However, the impact of oxide traps on channel noise at high frequencies is minimal.

Chapter 7 discusses the forward body bias effect on high frequency noise in both N- and P-MOSFETs. It is observed that noise performance is degraded with the increase in body bias. The noise increase can be qualitatively explained by secondary effects such as the nonequilibrium channel noise and substrate resistance noise. Different noise degradation mechanisms in N- and P-MOSFETs are also discussed in this chapter.

Finally, Chapter 8 summarizes the main results and contributions of this thesis and gives suggestions for future work.

Chapter 2

Noise and RF Measurement

2.1 Definition of Noise

In general, the word “noise” is used to describe any unwanted signal. In electronics, noise is defined as any unwanted disturbance that obscures with a desired signal, different kinds of noise sources interfering during the signal transmission are shown in Figure 2.1. The noise sources include power line, signal cross-talk, electromagnetic waves, and so on. This type of noise is classified as artificial noise, which can be reduced by strengthen the signal power, or using a good noise shielding scheme to improve the signal to noise ratio.

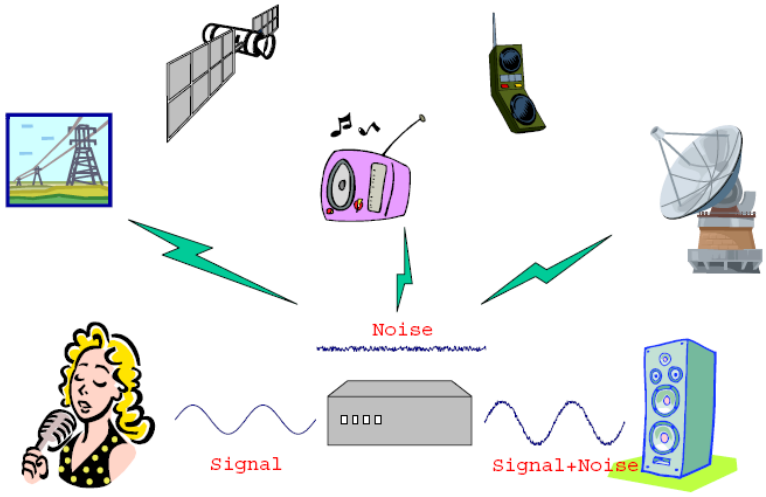


Figure 2.1: Different types of artificial noise [15].

The second category of noise, "fundamental noise", is irreducible since it is inherent in the system or device itself. The fundamental noise defines the lowest limit of a signal that can be detected. Since noise is random in nature, we need to use statistical approaches for its characterization. Generally, noise is expressed by power spectral density per unit frequency, which represents the average of noise power over one hertz bandwidth at any given frequency.

2.2 Intrinsic Noise Sources in MOSFETs

As noise generated within MOSFETs plays an increasing important role in circuit design and performance evaluation, it is crucial to understand the noise physical mechanisms in deep submicron MOSFETs. The most important intrinsic noise sources in MOS transistors are thermal noise, shot noise, and flicker noise.

In order to have a better understanding of the device noise behavior, a MOSFET is often modeled as an equivalent circuit with different resistive, capacitive, and active components. Figure 2.2 shows a simple equivalent noise model of an intrinsic MOSFET for high frequency application. The capacitor C_{gs} is composed of the gate-channel capacitance and the gate-source overlap capacitance, whereas C_{gd} is mainly due to the gate-drain overlap. The gate resistance R_g models the distributed effect at the gate of the MOSFET at high frequencies. The source and drain resistances R_s and R_d are due to the resistance of the lightly doped extensions of the source and drain diffusions, and the elements C_{db}, R_{db}, C_{gb}, and C_{sb} model various high frequency effects. In the noise model, it has taken into account the following noise sources: channel noise ($\overline{i_d^2}$), noise due to the gate resistance ($\overline{i_G^2}$), induced gate noise ($\overline{i_g^2}$), the resistance between the drain and bulk ($\overline{i_{DB}^2}$), and the thermal noise in the source ($\overline{i_S^2}$) and drain ($\overline{i_D^2}$) parasitic resistances.

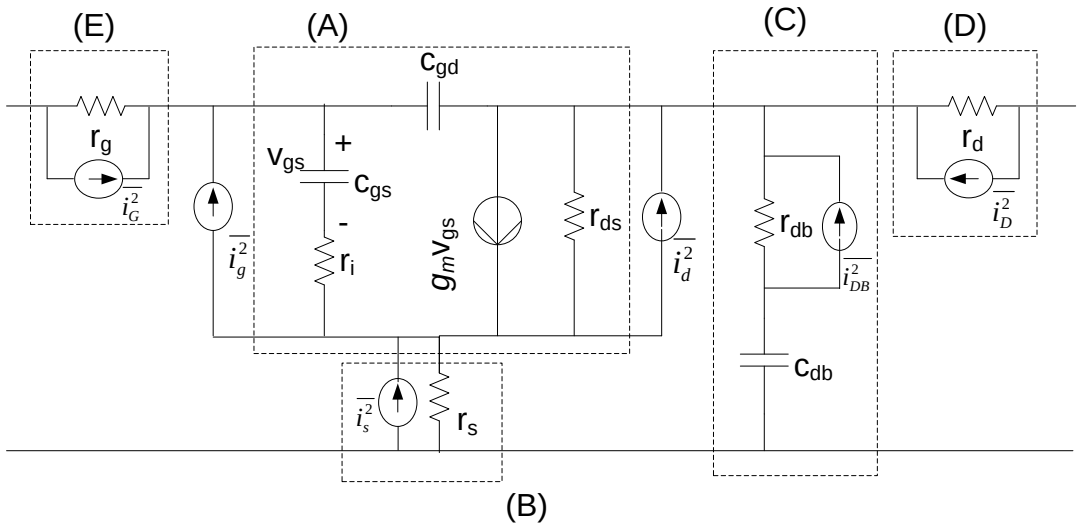


Figure 2.2: Small signal equivalent noise circuit of substrate grounded MOSFET with five sub-networks: (A) the intrinsic part of the transistor; (B) the source resistance; (C) the substrate network; (D) the drain resistance; and (E) the gate resistance network [16].

2.2.1 Thermal Noise of MOSFETs

Thermal noise, also known as Nyquist-Johnson noise, is caused by collisions of the charged carries with the lattice due to random thermal motion of the carrier [17-18]. Thermal noise is often considered as "white noise", because its power spectral density is almost frequency independent at high frequencies. In general, the power spectral density of short-circuit current fluctuation $S_{I,T}$, in A^2/Hz, can be expressed as

$$S_{I,T} = 4k_B T / R \tag{2.1}$$

where k_B is the Boltzman constant, T is the absolute temperature of the semiconductor device , and R is the resistance of the sample.

In the following, we will discuss three most important thermal noise sources in the high frequency range, including drain current noise $\overline{i_d^2}$, induced gate noise $\overline{i_g^2}$, and

thermal noise from parasitic resistances $\overline{i_D^2}$, $\overline{i_S^2}$, $\overline{i_G^2}$. The noise from parasitic resistors can be modeled using Equation (2.1) with the corresponding resistance values. It is noted that the noise from the channel and from the resistors are quite different, which will be discussed in detail later.

- ***Drain Current Noise***

Drain current noise, also referred as "channel thermal noise", is the most dominant and important noise source for MOSFETs. It originates from the random thermal motions of carriers in the channel of the device as shown in Figure 2.3. A classical channel thermal noise model, which has been widely used in many MOS SPICE model, is expressed as

$$S_{I_d} = 4k_B T g_{d0} \gamma \tag{2.2}$$

where g_{d0} is the output conductance at V_{ds} = 0, and γ is bias dependent noise factor. The value of γ is 1 and 2/3 in the triode and saturation regions for long-channel MOSFETs, respectively.

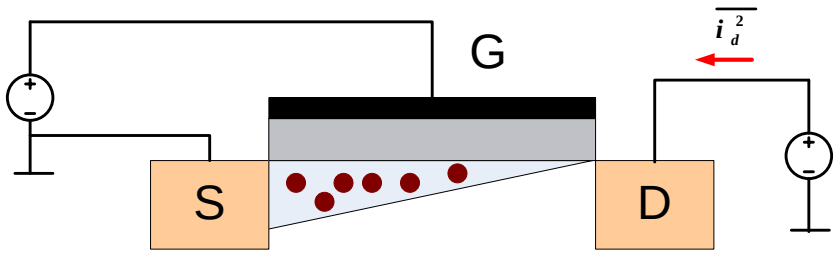


Figure 2.3: Drain current noise of MOSFET.

Two decades ago, Jindal firstly reported the excess channel noise in short channel MOSFETs [19]. He found that the long channel noise model failed to predict the channel noise of the MOSFET when L_{eff} < 0.42 μm. Since then, physical

mechanism of the excess channel noise in short channel MOSFETs has been a focus of intense activity in the MOSFET noise modeling over the past 20 years. It was found that factor γ for short channel device was much larger than that for long channel device in the saturation regime. Different noise factors γ versus channel length reported in recent years has been summarized by Jindal in [20].

On the increase in noise factor in short channel MOSFETs, a number of theories have been developed to explain the physical origin of the excess noise. Klein [21] and Knoblinger [22] suggested that the excess channel noise was caused by the carrier heating in the pinch-off region. Hence, they developed a new model that sums up the channel noise from both linear and saturation region (Figure 2.4). This model was implemented in standard BSIM3v3 SPICE model, and had been widely used in RF-CMOS design [23]. Over the past few years, several analytical noise models which attributed the excess noise in saturation region to either hot carriers, or mobility degradation were developed [21-22, 24-26].

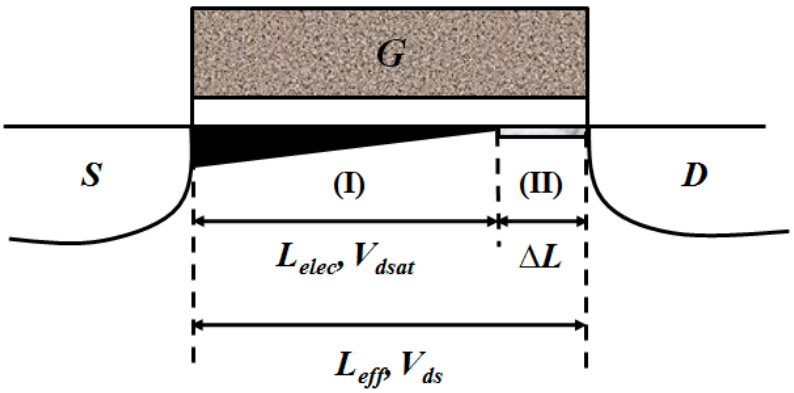


Figure 2.4: Cross section of the channel of a MOSFET, divided into two regions: (I) linear and (II) velocity saturation regions. L_{elec} is the point in the channel where the channel field $E(x)$ is equal to the critical field E_c, and the velocity of carriers is equal to their saturation velocity v_{sat}. ΔL is the length of the pinch-off or velocity saturated region [27].

On the other hand, by using channel length modulation (CLM) effect, Chen and Deen showed that the noise contribution from the velocity saturation region is negligible and hot carriers in pinch-off region does not produce significant noise [27]. This argument was also supported by the experimental data in [28] , which suggested that high frequency noise is irrelevant to the increase in channel hot electrons population under explored bias conditions. More recently, theoretical studies using the hydrodynamic (HD) and full Langevin Boltzmann equation (LBE) noise models, demonstrated that the channel noise could be dominated by the source side contribution rather than the drain side due to higher impedance field near the source junction [29-31]. As such, the device simulators have to keep track of the noise modeling progress because CLM effect, mobility degradation and carrier heating together are not able to explain excess noise observed in sub-100 nanometer regime irrespective the transport model used. Additional effects for modeling noise behaviors in nanoscale MOSFETs should be considered.

- ***Induced Gate Noise***

At high frequencies, the MOSFET must be considered as an RF distribution network, such that channel thermal noise is coupled to the gate through the gate capacitance and causes induced gate noise [32]. As shown in Figure 2.5, the thermal fluctuations originating in the channel induce a gate current outwards from the gate electrode. Induced gate noise is fully correlated to channel thermal noise, and can be expressed as

$$S_{Ig} = 4k_B T g_g \delta \tag{2.3}$$

Where g_g is the real part of the gate-to-source admittance, δ are bias dependent noise factor, and normally is 4/3 for MOSFETs. Generally, induced gate noise can be

implemented as a current source in parallel with C_{gs} in a noise model as shown in Figure 2.2. Induced gate noise is proportional to f^2, owing to ωC the dependence. Therefore, it dominates noise performance of MOSFETs at high frequencies.

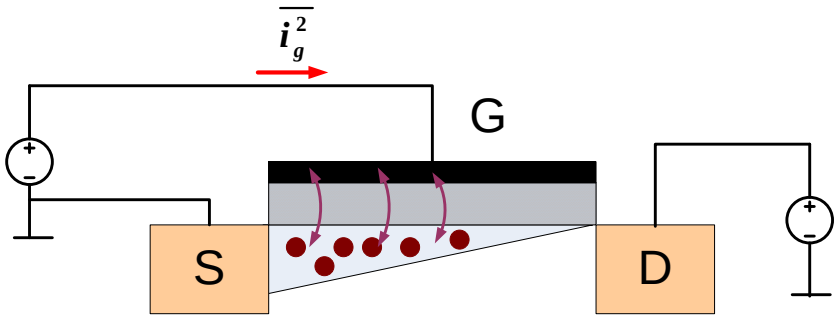


Figure 2.5: Induced gate noise effect of MOSFETs

- ***Thermal Noise from Characteristic Resistance***

In short-channel MOSFETs, there are several types of parasitic resistance, the major extrinsic elements are source resistance R_S, drain resistance R_D and gate resistance R_G. Source and drain resistance (R_S and R_D) degrade the drive current of the device while R_G has a strong impact on the maximum oscillation frequency. The role of thermal noise from parasitic resistance has gain more attention and is taken into account in the noise modeling as shown in Figure 2.2. It is important to minimize these noise sources by advanced process techniques especially for short-channel MOSFETs. For instance, gate resistance is reduced by using "multi-finger" layout. In general, the power densities of these noise sources can be expressed as

$$S_{I_{R_s}} = 4kT / R_s \quad (\text{drain noise}) \tag{2.4}$$

$$S_{I_{R_D}} = 4kT / R_D \quad (\text{source noise}) \tag{2.5}$$

$$S_{I_{R_G}} = 4kT / R_G \quad (\text{gate noise}) \tag{2.6}$$

2.2.2 Shot Noise of MOSFETs

Shot noise, generally is defined as electronic noise that occurs when finite number of carriers (electrons or hole) cross potential barriers. This type of noise is mainly present in diodes and bipolar transistors. In MOSFETs, shot noise arises mainly due to gate leakage current, which is a current flow from quantum-mechanical tunneling of carriers through the gate oxide. Traditionally, gate shot noise is neglected in MOSFET noise modeling (Figure 2.2). However, as gate oxide gets thinner than 2 *n*m, significant direct tunneling gate current is observed. Researchers have found that for sub 90 *n*m MOSFET, gate shot noise becomes very crucial for accurate noise modeling and should be considered carefully [33]. The gate shot noise is also important if gate oxide breakdown happens (either SBD or HBD), and even becomes the most dominant noise source in the MOSFETs under such circumstance [34]. Since the gate current is caused by carriers randomly crossing a potential barrier, the power spectral density of the gate shot noise (A^2/Hz) is given by the formula

$$S_{I_{g,shot}} = 2qI_G \tag{2.7}$$

where q is the electronic charge (1.6×10^{-19}C) and I_G is the gate current. Gate shot noise is ideally white, and has amplitude that possesses a Gaussian distribution.

2.2.3 Flicker Noise of MOSFETs

Flicker noise is also known as 1/*f* noise because its spectral density is inversely proportionally to frequency. In principle, flicker noise is dominant at low frequencies and can be ignored in high frequency regime. However, in some RF circuits, such as mixers and oscillators, flicker noise should be considered as low frequency noise could be up-converted to high frequency and deteriorate the noise performance of the circuits [35]. Flicker noise is the most widely studied and debated phenomena in the

history of noise [36-40], and it is considered to be a surface phenomenon which related to oxide-semiconductor interface. There are two conflicting theories on flicker noise mechanisms although the exact physical mechanism is not clear yet.

The first one is called the number fluctuation (ΔN) model. Experimental results showed that flicker noise had a strong correlation with the density of interface traps (N_{it}) or near oxide traps (N_{ot}). There are strong indications that the flicker noise is mainly caused by conductance variations due to the random capture and release of charges by the traps as shown in Figure 2.6. The resulting number fluctuation power spectral density is

$$S_{VG,1/f} = \frac{S_{i_d}}{g_m^2} = \frac{kTq^2}{8WLC_{ox}^2\alpha_t}\frac{N_{ot}(E_f)}{f} \tag{2.8}$$

where α_t is the tunneling parameter and N_{ot} is the oxide trap density.

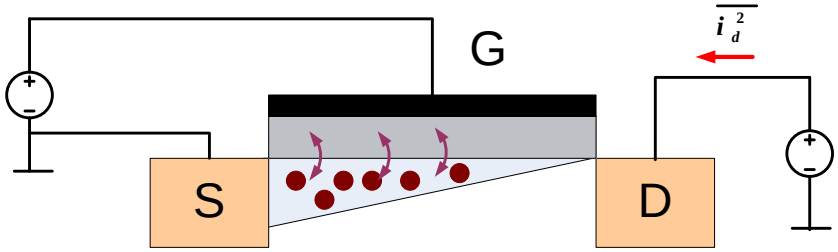


Figure 2.6: Flicker noise in MOSFET.

Opposite to ΔN model is mobility fluctuation ($\Delta\mu$) model, which considers flicker noise is a result of carrier mobility fluctuations. The flicker noise for this model is expressed as

$$S_{VG,1/f} = \frac{q}{WLC_{ox}}\frac{\alpha_H(V_{gs}-V_{th})}{f} \tag{2.9}$$

$$\alpha_H = 2\times10^{-3}\left(\frac{\mu}{\mu_{latt}}\right) \tag{2.10}$$

where α_H is a material parameter, μ is the carrier mobility and μ_{latt} is the mobility due to lattice scattering only. This model is purely empirical, and assumes that the bulk mobility fluctuation is introduced by the lattice (phonon) scattering.

Recently, unified models which combined both carrier number and mobility fluctuations have been proposed [40]. The basic concept of the unified model is that the oxide/interface traps not only interact with the channel through carrier capture and generation, but also affect carrier mobility through change in scattering rate indirectly, when traps are occupied and emptied.

2.3 Calculation of Noise Parameters

2.3.1 Four Noise Parameters

In noise model derivation and circuit simulation, the noise power spectral density is used as a measure of noise output in the device as shown in Figure 2.2. However, in measurements, the high frequency noise is usually characterized by some other parameters, such as minimum noise figure, equivalent noise resistance, and optimum source admittance. Noise Figure in a two-port network is defined as the signal-to-noise ratio at the input port divided by the signal-to-noise ratio at the output port. It is widely used to evaluate the noise performance of a noisy two-port network and is normally expressed in decibels (dB). Noise Figure (NF) is generally affected by two factors, source impedance and noise sources in the two-port network.

In general, the noise figure of a two-port network can be given by the following equivalent equations:

$$\mathrm{NF} = \mathrm{NF}_{\min} + \frac{R_n \left| Y_s - Y_{opt} \right|^2}{G_s} \quad , \qquad \text{or} \tag{2.11}$$

$$\mathrm{NF} = \mathrm{NF}_{\min} + \frac{4R_n}{Z_0} \bullet \frac{\left|\Gamma_{opt} - \Gamma_s\right|^2}{\left|1+\Gamma_{opt}\right|^2 \left(1-\left|\Gamma_s\right|^2\right)} , \tag{2.12}$$

$$\Gamma_{opt} = \frac{1 - Z_0 Y_{opt}}{1 + Z_0 Y_{opt}} , \tag{2.13}$$

where Y_s is the source admittance, Z_0 is the characteristic impedance (50Ω), $\mathrm{NF}_{\min}$ is the minimum noise factor when the network can achieve with the optimum source admittance condition $Y_s = Y_{opt} = G_{opt} + jB_{opt}$, and R_n is the equivalent noise resistance which determines the sensitivity of the noise figure when Y_s differs from Y_{opt}. They are often referred as "four noise parameters". This representation is widely used in RF circuit design because it offers an intuitive way to deal with noise prosperities.

$\mathrm{NF}_{\min}$ is a function of biases (device current) and frequency. Each $\mathrm{NF}_{\min}$ is associated with one value of Γ_{opt}. By re-arranging Equation (2.12), we have

$$\left|\Gamma_s - \frac{\Gamma_{opt}}{(1+N_i)}\right|^2 = \left|\frac{1}{1+N_i}\sqrt{N_i^2 + N_i(1-\sqrt{1-\left|\Gamma_{opt}\right|^2}}\right|^2 , \tag{2.14}$$

where

$$N_i = \frac{(NF - NF_{\min})\left|1+\Gamma_{opt}\right|^2}{4R_n} \tag{2.15}$$

When source reflection coefficients Γ_s is plotted on a Smith chart for a set of constant noise factors NF, it will result in a set of "noise circles" in the Γ_s plane (Figure 2.7). Noise circles are convenient to display the complex relation between source impedance and noise figure.

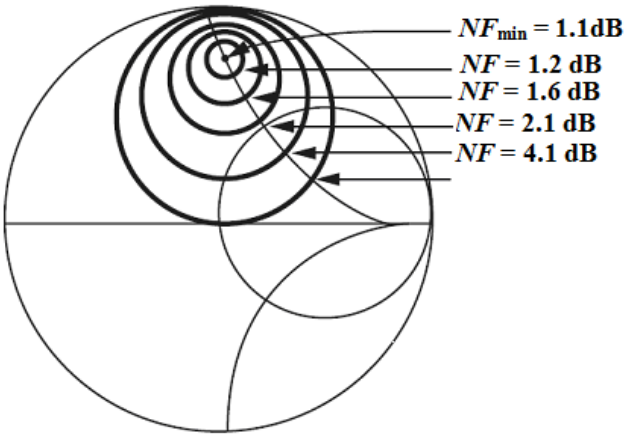


Figure 2.7: Noise figure circles of a typical transistor. The noise circles are used to display the complex relation between source impedance and noise figure.

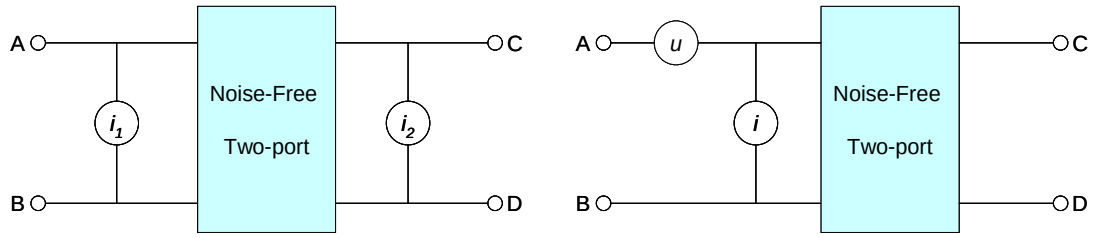
2.3.2 Noise Theory of Two-Port Network

As mentioned above, circuit designers prefer to use parameters related to a two-port network to describe the noise performance of a device and a circuit. Universal noise models have been developed for two-port networks. A noisy two-port may be represented by a noise-free two port with two noise current sources (i_1, i_2), at both the input and the output as shown in Figure 2.8 (a) (i_1, i_2 are correlated with each other). It can also be represented by a noise current source (i) with a noise voltage source (u) both at the input port as shown in Figure 2.8 (b). The current i and voltage u in Figure 2.8 (b) is correlated by factor Y_{cor} as

$$i = i_{un} + uY_{cor} \ , \tag{2.16}$$

$$\overline{iu^*} = Y_{cor}\overline{|u|^2} , \tag{2.17}$$

where i_{un} is the component that is not correlated to u, and uY_{cor} is the part fully determined by u. According to the two-port network give in Figure 2.8 (b), u and Y_{cor} can be calculated as



(a) (b)

Figure 2.8: Different representations of a noisy two-port network.

$$u = -\frac{1}{Y_{21}} i_2 \ , \ i = i_1 - \frac{Y_{11}}{Y_{21}} i_2 \ , \tag{2.18}$$

$$Y_{cor} = Y_{11} - Y_{21} \frac{\overline{i_1 i_2^*}}{\overline{|i_2|^2}} = G_{cor} + jB_{cor} \ , \tag{2.19}$$

the noise power of *i* and *u* then is

$$\overline{|u|^2} = \frac{\overline{|i_2|^2}}{|Y_{21}|^2} = 4kT\Delta f R_u \ , \tag{2.20}$$

$$\overline{|i|^2} = \overline{|i_1|^2} + \overline{|i_2|^2} \left| \frac{Y_{11}}{Y_{21}} \right|^2 - 2\,\mathrm{Re}\left\{ \overline{i_1 i_2^*} \cdot \frac{Y_{11}^*}{Y_{21}^*} \right\} = 4kT\Delta f G_i \ , \tag{2.21}$$

On the basis of the above relationships, the four noise parameters can be written as

$$R_n = R_u \ , \tag{2.22}$$

$$G_{opt} = \sqrt{\frac{G_i}{R_n} - B_{cor}^2} \ , \tag{2.23}$$

$$B_{opt} = -B_{cor} \ , \tag{2.24}$$

$$\mathrm{NF}_{\min} = 1 + 2R_n (G_{cor} + G_{opt}) , \tag{2.25}$$

2.3.3 Analytical Calculation of Noise Parameter for Intrinsic MOSFETs

Figure 2.2 illustrates all the noise sources in a MOSFET. However, it is sometimes too complex to calculate each of them. A simpler equivalent small signal model of an intrinsic MOSFET is shown in Figure 2.9.

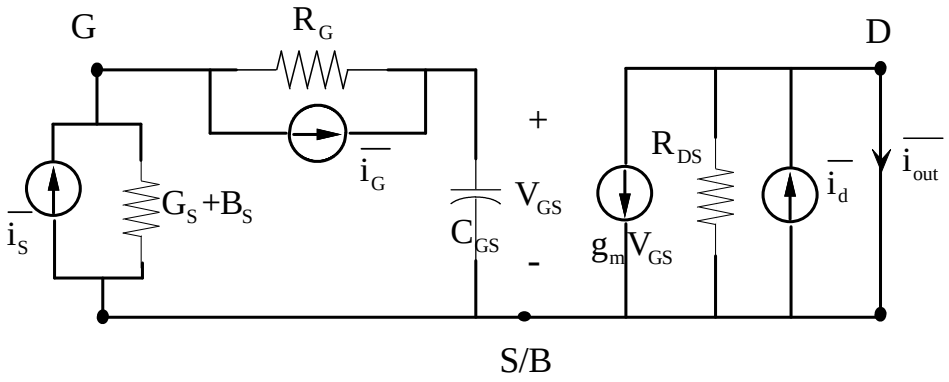


Figure 2.9: Simplified equivalent circuit model of intrinsic MOSFETs for analytical calculation of noise parameters [16].

Based on analytical calculation method, the noise figure (NF) is calculated by dividing the total noise power of the short-circuit noise current i_{out} at the output port from each noise source by the noise power at the output port from source impedance. The equivalent noise resistance (R_n) can be calculated by dividing the total noise power of the short-circuit noise current i_{out} at the output port from each noise source by the square of the magnitude of the small-signal current gain. Therefore, the four noise parameters can be expressed as

$$\mathrm{NF}_{\min} = 1 + \frac{1}{2} R_G \omega C_{GS} i_d \cdot \frac{\omega C_{GS} i_d + \sqrt{\omega^2 C_{GS}^2 i_d^2 + i_G^2 g_m^2}}{g_m^2 kT}, \tag{2.26}$$

$$R_n = \frac{1}{4kT} \cdot \left(\frac{1 + \omega^2 C_{GS}^2 R_G^2}{g_m^2} \cdot i_d^2 + R_G^2 i_G^2 \right), \tag{2.27}$$

$$G_{opt} = \frac{\omega C_{GS} R_G i_d \cdot \sqrt{\omega^2 C_{GS}^2 i_d^2 + i_G^2 g_m^2}}{i_d^2 + \omega^2 C_{GS}^2 R_G^2 i_d^2 + R_G^2 i_G^2 g_m^2} \quad , \tag{2.28}$$

$$B_{opt} = -\frac{\omega C_{GS} i_d}{i_d^2 + \omega^2 C_{GS}^2 R_G^2 i_d^2 + R_G^2 i_G^2 g_m^2} \tag{2.29}$$

2.4 Scattering and Noise Parameter Measurements

2.4.1 Concepts of NP5 Noise Measurement System

The complete S-parameter and noise parameter measurement system for high frequency noise and S-parameter measurement is shown in Figure 2.10. The system is consisted of an ATN NP5 wafer prober test set, a S-parameter measurement system, and a noise parameter measurement system. The NP5 mainframe works as a switch for switching between HP8510B for S-parameter measurements and the HP8970 for noise measurement.

The wafer prober is comprised with a mainframe controller and two remote modules. The input module, called Mismatch Noise Source (MNS), contains a solid state electronic tuner with a built-in bias tee and switching circuitry. The output module, Remote Receiver Module (RRM), contains a bias tee, switching circuitry, and a low noise amplifier. The switch box is used to pass the RF signal from the HP8341B frequency synthesizer to either S-parameter or noise measurement system if there is only one frequency synthesizer available for different measurement mode.

The S-parameter measurement systems contains HP8510B vector network analyzer (VNA) and HP8514A S-parameter test set to measure the scattering and gain parameters of linear two port networks. In S-parameter measurement mode, HP8510B controls RF source (H8341B) and two kinds of measurement are made – reflection and transmission.

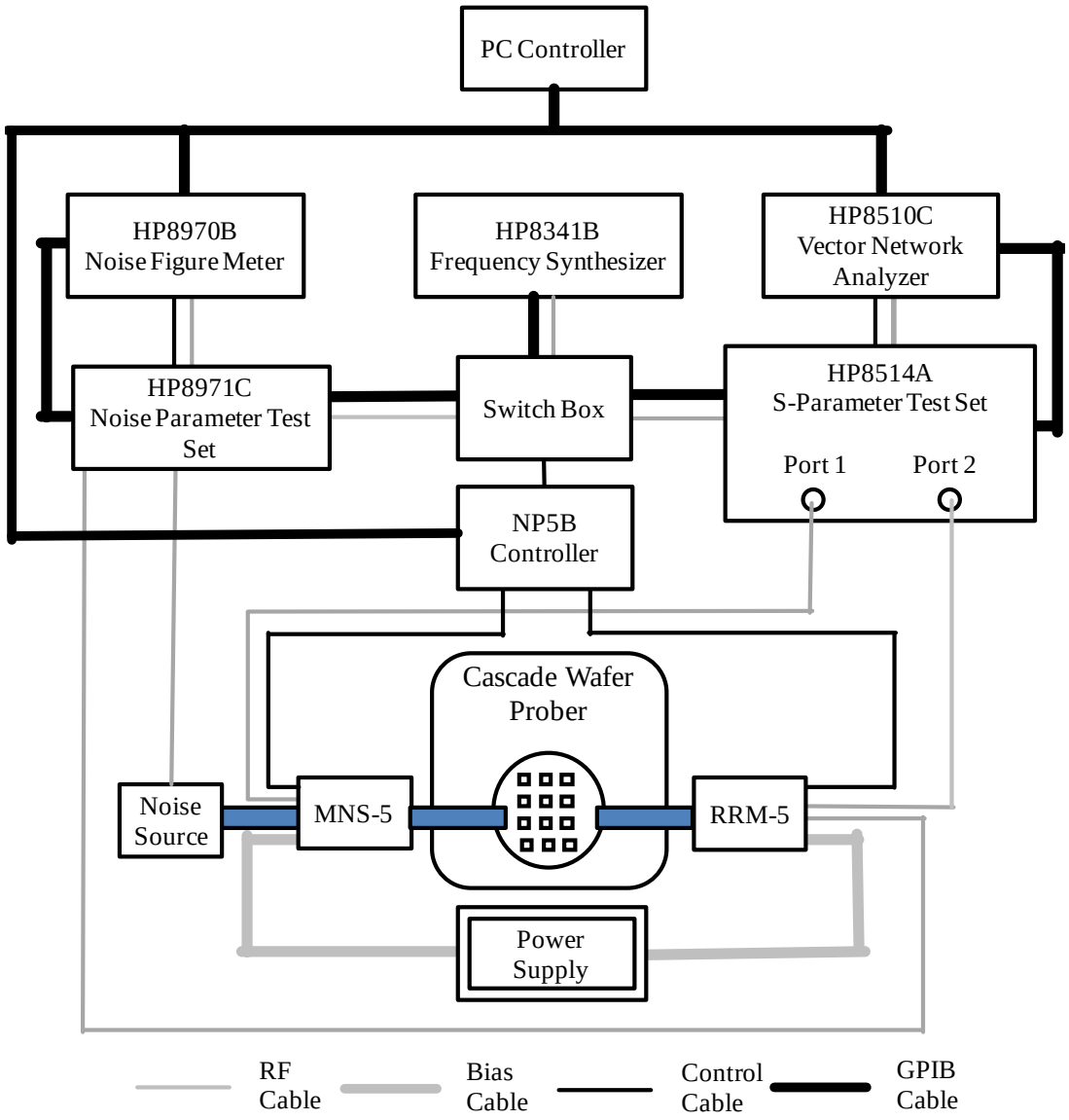


Figure 2.10: ATN NP5 measurement system for S-parameter and noise parameter measurement [41].

The noise measurement systems contains HP8970B noise figure meter and HP8971C noise parameters test set to measure the noise parameter and gain of the device under test (DUT).

2.4.2 Calibration of NP5 Noise Measurement System

All NP5 measurements require prior calibration of the system. This enables the placing of the calibration reference planes directly at the DUT without explicit

knowledge of the test fixture or test probe S-parameters. Figure 2.11 shows simplified diagrams of NP5 calibration and DUT reference planes. These reference planes are suitable for performing a coaxial S-parameter calibration. RP1 and RP2 are the reference planes for the DUT evaluation. RP2 is the reference plane where the coaxial calibration standards (Short/Open/Load or S/O/L) and the coaxial power meter interface are connected.

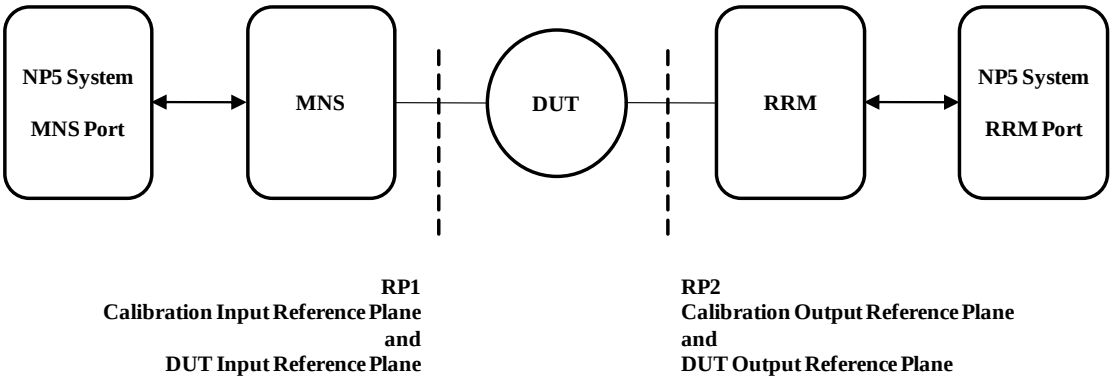


Figure 2.11: Simplified diagrams of NP5 system calibration and device-under-test (DUT) reference planes [42].

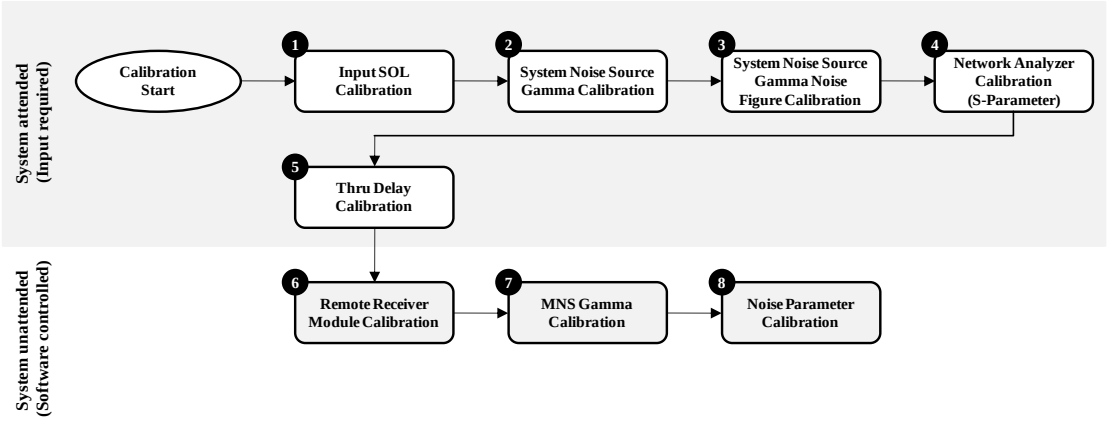


Figure 2.12: Schematic of NP5 system calibration procedure steps [42].

Noise system calibration is comprised of several individual steps which can be group into two distinct phases, system attended (user input required) and system unattended (software controlled). The sequential calibration steps are (Figure 2.12) [42]:

1) Input SOL Calibration : With a thru of known delay as the DUT, the NP5 system makes raw S_{22} measurements with a short, open, and load in the place of the noise source. This raw data will be combined with the data taken during the full 2 port calibration (at the device plane) to determine the S-parameters of the MNS.
2) System Noise Source Gamma Calibration : With the same thru as in the SOL calibration and having established a reference plan at the noise source from the SOL calibration, the NP5 system makes raw S_{22} measurement with the noise source on and off and calculates the corresponding reflection coefficients for the noise source. The NP5 system then proceeds to make hot and cold power measurements with the noise figure meter. The data is used to correct for the mismatch of the noise diode.
3) System Noise Source Noise Figure Calibration: This step is to determinate the system noise figure from the noise diode back into the system. The same four low –loss states that used in SOL calibration are used here. ENR (excess noise ratio) values listed are those associated with the noise source. YIG peaking is always recommended, though it may be skipped if it has been recently done.
4) Network Analyzer Calibration (S-parameter): This is a standard S-parameter calibration by any of the standard acceptable methods – Short-Open-Load-Thru (SOLT), Line-Reflect-Match (LRM), Thru-Reflect-Line (TRL), or Line-Reflect-Line (LRL). It is noted that the S-parameter reference plans are the noise parameter reference planes in the NP5 software.

5) Thru Delay Calibration: With the same thru as in the SOL and NS1 calibrations as the DUT, the corrected S-parameters are measured and the thru delay is calculated and displayed for confirmation. If the thru delay value is within the range of $1 \pm 0.1ps$, this step of calibration is passed.
6) Remote Receiver Module (RRM) Gamma Calibration: With the same thru as before, S_{11} measurements are made to determinate the input reflection coefficient of the post receiver. This information is referred to the S-parameter port 2 (output) reference plane and stored.
7) Mismatch Noise Source (MNS) Gamma Calibration: With the same thru as before, S_{22} measurements are made for the 88 impedance states of the solid state tuner. These impedances are referred to S-parameter port 1 (input) reference plane.
8) Noise Parameter Calibration: With the same thru as before, noise power versus source impedance is measured and the receiver noise parameters are calculated and stored at S-parameter port 2 reference plane.

After calibration is finished, users are advised to do a check with a known DUT. For example, S-parameters and noise parameters of a thru is measured to check the system performance. If loss (S_{11}) is not within 0.1 dB of the expected loss of the thru there is an error in the calibration and it should be redone. If NF_{min} is not within plus or minus 0.2 dB, there is a problem with the noise calibration and it should be redone.

2.5 Summary

In this chapter, fundamentals of noise are introduced, followed by a detailed review on different kinds of noise sources in MOSFETs, including thermal noise, shot noise and flicker noise. The physical origins of channel noise are studied and their

manifestations in MOSFETs are presented with equations to describe their behaviors. A general noise theory for a noisy two-port network and four noise parameters are described in detail. Finally, noise and s-parameter measurement system and its calibration procedures are described.

Chapter 3

Experiments

3.1 Devices

The devices used for the tests in this work are N and PMOS fabricated by standard 0.18-μm twin-well CMOS process flow. The gate oxide was 29 Å thick containing ~1% nitrogen, grown via rapid thermal oxidation in an N_2O ambient. After the formation of 2000 Å thick polysilicon gate electrodes, moderately doped source/drain extensions were formed by low-energy arsenic (NMOS) or boron (PMOS) implantation. Following the nitride spacer formation, a high-dose arsenic or boron implantation was applied to form N+ or P+ source/drain.

MOS transistors used in S-parameter measurements are using the multi-gate finger approach (also called folded layout). A general principle of multi-finger gate MOS transistors is given in Figure 3.1, the device is very compact. The minimization of parasitic capacitance due to shared drain/source regions provides the best RF performance such as cut-off frequency f_T enhancement [43-44]. Moreover, as gate fingers are contacted from both sides to minimize the gate resistance, better high frequency noise behavior can be achieved. A compact RF CMOS model taking gate resistance R_g into account can be found in reference [45].

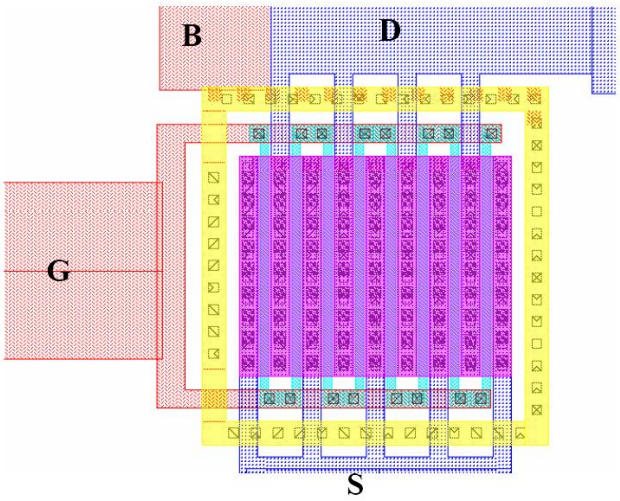


Figure 3.1: Layout of a multi finger RF MOS transistor. The transistor is embedded in a Ground-Signal-Ground (GSG) pad frame with grounded source. (B: Body, D: Drain, G: Ground, S: Source)

3.2 Pad De-Embedding

3.2.1 Test Device Layout for HF Noise Measurement

For S-parameter and high frequency noise measurements, a good grounding is essential, and ground loops must be avoided. Therefore, the Bulk and Substrate contacts are reliably connected to the ground when GSG (Ground-Signal-Ground) are connected to the test device. Figure 3.2 shows the layouts of the device under test, and their corresponding dummy structures used in de-embedding, including “Open”, “Short” and “Thru”. All test pads are ground-signal-ground (GSG) mode with 150 *u*m

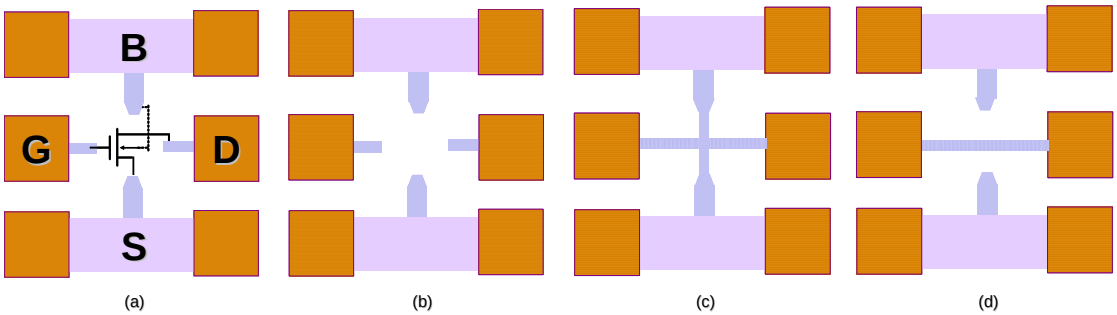


Figure 3.2: Layout of the DUTs and corresponding dummy structures, (a) MOSFET (b) Open (c) Through (d) Short.

pitch (the distance between the centers of the pads) fabricated by standard 0.18 μm CMOS technology. The dimensions of the signal pads are 100 μm × 100 μm.

3.2.2 Pad De-embedding Techniques

After network analyzer calibration, the calibration plane is located at the ends of NWA cables. The device itself, however, needs to be connected to the calibration plane. In the case of packaged devices, S-parameter measurements would now include test fixture, package and the intrinsic DUT. In order to get the DUT response from measurement, the parasitics of the pad must be removed. The layout patterns, with one including the DUT while the other (dummy) excluding it, are fabricated on the same wafer as shown in Figure 3.2. The correction of measurement results for pad parasitics is often called “pad de-embedding”.

The simplest de-embedding method is de-embedding from an OPEN device. The prerequisite for this method is that all the circuit components of the OPEN dummy structure can be represented exclusively by lumped circuit components, and they are altogether in parallel with the DUT. Figure 3.3 shows the topology of the pads parasitics with the intrinsic transistor in a parallel configuration.

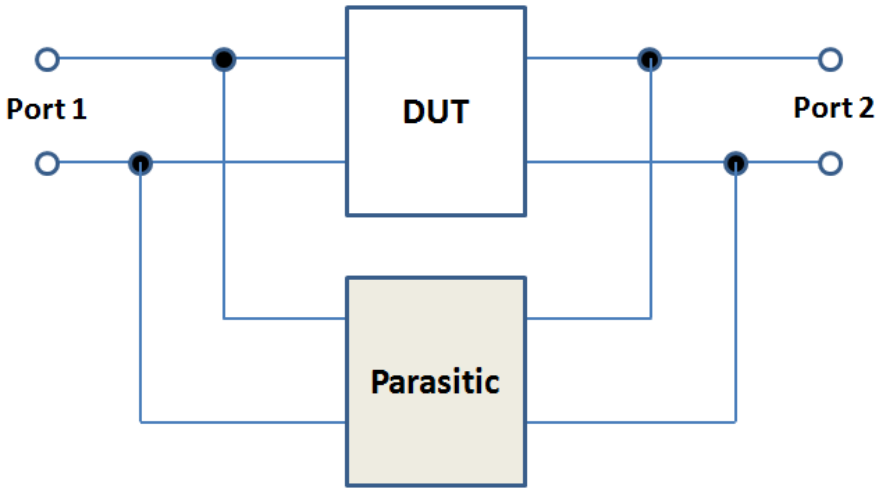


Figure 3.3: Topology of the pads parasitic with the intrinsic transistor.

From the S-parameter measurement of the device and the pads, we define the two-port extrinsic S-parameter matrix as

$$S_E = \begin{pmatrix} S11_E & S12_E \\ S21_E & S22_E \end{pmatrix} \tag{3.1}$$

The pads parasitic S-parameter matrix is defined as

$$S_P = \begin{pmatrix} S11_P & S12_P \\ S21_P & S22_P \end{pmatrix} \tag{3.2}$$

Both S_E and S_p matrix can be transformed to the *Y*-parameters. Using the equivalent circuit transformations from ABCD to *Y* format, we extract the admittance matrix of the intrinsic device by

$$Y_I = Y_E - Y_P \tag{3.3}$$

Finally, we use the equivalent circuit transformations from the *Y* back to the *S* format to calculate the intrinsic S-parameter.

A more accurate de-embedding procedure, based on cascade configuration for on-wafer RF measurements of MOSFETs is presented in detail by Chen and Deen in

reference [46]. This method is not easy to implement since the parasitic elements in equivalent circuit model are both technology and design dependent.

3.3 Procedures of Noise Extraction in Deep Submicron MOSFETs

For the application of modern CMOS technologies in low-noise RF circuits, accurate modeling of device noise is required. A crucial procedure in noise analysis is to extract channel and induced gate noise currents directly from RF noise measurements. Several noise models and extraction methods have been presented [22, 47-48].

The channel noise, induced gate noise, and their correlation in MOSFETs can be extracted by using the following 15 steps from measured noise parameters (NF_{min}, R_n, and G_{opt}) [49]. This method has been used in the following chapters to extract different noise parameters.

1) Measure the scattering parameters S_{DUT}, S_{OPEN} of the device-under-test (DUT), and OPEN dummy structures, respectively.
2) Measure the noise parameters $NF_{min,DUT}$, $Y_{opt,DUT}$, and $R_{n,DUT}$.
3) Perform a parameter de-embedding to get the intrinsic scattering ($Y_{opt,DUT}$) and noise parameters ($NF_{min,dev}$, $Y_{opt,dev}$, and $R_{n,dev}$).
4) Perform a parameter extraction [50] based on and other measured data to get all the element values (e.g., g_m, C_{GS}, C_{GD}, etc.,) in the RF noise model (Figure 2.2).
5) Calculate the correlation matrix $\boldsymbol{C}_{Adev}$ of the intrinsic device from measured noise parameters of the device

$$C_{Adev} = \begin{bmatrix} R_{n,dev} & \frac{NF_{\min,dev}-1}{2} - R_{n,dev}(Y_{opt,dev})^* \\ \frac{NF_{\min,dev}-1}{2} - R_{n,dev}(Y_{opt,dev}) & R_{n,dev}\left|Y_{opt,dev}\right|^2 \end{bmatrix} \quad (3.4)$$

6) Calculate the four-port admittance matrix $\boldsymbol{Y}_{extr}$ of the extrinsic part in the RF transistor model by excluding C_{GS}, C_{GD}, g_m, R_{DS}, and R_i

$$Y_{extr} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \quad (3.5)$$

where the submatrixes $\boldsymbol{Y}_{ee}$, $\boldsymbol{Y}_{ei}$, $\boldsymbol{Y}_{ie}$, and $\boldsymbol{Y}_{ii}$ are 2×2 matrixes.

7) Calculate the two-port admittance $\boldsymbol{Y}_{intr}$ of the intrinsic part in the RF transistor model.

8) Calculate a matrix $\boldsymbol{D}$ as follows:

$$D = -Y_{ei}(Y_{ii} + Y_{intr})^{-1} \quad (3.6)$$

9) Convert the noise correlation matrix $\boldsymbol{C}_{\boldsymbol{A}dev}$ to its admittance form $\boldsymbol{C}_{\boldsymbol{Y}dev}$ by using

$$C_{Ydev} = T_Y C_{Adev} T_Y^{\dagger} \quad (3.7)$$

where the † in $T_Y^{\dagger}$ denotes Hermitian conjugation (transpose and complex conjugate) and the transformation matrix $\boldsymbol{T}_{\boldsymbol{Y}}$ is given by

$$T_Y = \begin{bmatrix} -Y_{11,dev} & 1 \\ -Y_{21,dev} & 0 \end{bmatrix} \quad (3.8)$$

10) Calculate the admittance noise correlation matrix $\boldsymbol{C}_{\boldsymbol{Y}extr}$ of the extrinsic part by

$$C_{Yextr} = kT(Y_{extr} + Y_{extr}^{\dagger})$$

$$\text{or} \quad C_{Yextr} = 2kT\Re(Y_{extr}), \quad (3.9)$$

where T is the device temperature, $\Re()$ denotes for the real part of the matrix elements and partition $\boldsymbol{C}_{\boldsymbol{Y}extr}$ as

$$C_{Yextr} = \begin{bmatrix} C_{ee} & C_{ei} \\ C_{ie} & C_{ii} \end{bmatrix} \quad (3.10)$$

where the submatrixes $\boldsymbol{C}_{ee}$, $\boldsymbol{C}_{ei}$, $\boldsymbol{C}_{ie}$, and $\boldsymbol{C}_{ii}$ are 2×2 matrixes.

11) Calculate the admittance correlation matrix $\boldsymbol{C}_{\boldsymbol{Y}intr}$ of the intrinsic part in the RF transistor model from

$$C_{Y\mathrm{int}r} = D_i (C_{Ydev} - C_{ee}) D_i^{\dagger} - C_{ie} D_i^{\dagger} - D_i C_{ei} - C_{ii} \tag{3.11}$$

where $D_i = D^{-1}$.

12) Convert $\boldsymbol{Y}_{intr}$ to its chain representation $\boldsymbol{A}_{intr}$ using the conversion formula:

$$A_{\mathrm{int}r} = \frac{-1}{Y_{21,\mathrm{int}r}} \begin{bmatrix} Y_{22,\mathrm{int}r} & 1 \\ Y_{11,\mathrm{int}r} Y_{22,\mathrm{int}r} - Y_{12,\mathrm{int}r} Y_{21,\mathrm{int}r} & Y_{11,\mathrm{int}r} \end{bmatrix} \tag{3.12}$$

13) Convert $\boldsymbol{C}_{\boldsymbol{Y}intr}$ to its chain matrix form $\boldsymbol{C}_{\boldsymbol{A}intr}$ by using

$$C_{A\mathrm{int}r} = T_A C_{Y\mathrm{int}r} T_A^{\dagger} \tag{3.13}$$

where T_A is given by

$$T_A = \begin{bmatrix} 0 & A_{12,\mathrm{int}r} \\ 1 & A_{22,\mathrm{int}r} \end{bmatrix} \tag{3.14}$$

14) Calculate the noise parameters NF_{min}, Y_{opt}, and R_n of the intrinsic part in the RF transistor model from the noise correlation matrix $\boldsymbol{C}_{\boldsymbol{A}intr}$ by using (3.26), where $\Im()$ stands for the imaginary part of elements and j is the imaginary unit

$$NF_{\min} = 1 + \frac{1}{kT_0} (\Re(C_{12A,\mathrm{int}r} + \sqrt{C_{11A,\mathrm{int}r} C_{22A,\mathrm{int}r} - (\Im(C_{12A,\mathrm{int}r}))^2}) \tag{3.15}$$

$$Y_{opt} = \frac{\sqrt{C_{11A,\mathrm{int}r} C_{22A,\mathrm{int}r} - (\Im(C_{12A,\mathrm{int}r}))^2} + j\Im(C_{12A,\mathrm{int}r})}{C_{11A,\mathrm{int}r}} \tag{3.16}$$

$$R_n = \frac{C_{11A,\mathrm{int}r}}{2kT_0} \tag{3.17}$$

15) Calculate the power spectral density of the channel noise $\overline{i_d^2}$, induced gate noise $\overline{i_g^2}$, and their correlation $\overline{i_g i_d^*}$ from

$$\frac{\overline{|i_d|^2}}{\Delta f} = 4kT_0R_n\left|Y_{21,intr}\right|^2 \tag{3.18}$$

$$\frac{\overline{|i_g|^2}}{\Delta f} = 4kT_0R_n \times \left\{\left|Y_{opt}\right|^2 - \left|Y_{11,intr}\right|^2 + 2\Re\left[(Y_{11,intr} - Y_{cor})Y_{11,intr}^*\right]\right\} \tag{3.19}$$

$$\frac{\overline{i_g i_d^*}}{\Delta f} = 4kT_0(Y_{11,intr} - Y_{cor})R_nY_{21,intr}^* \tag{3.20}$$

where Y_{cor} is given by

$$Y_{cor} = \frac{NF_{\min} - 1}{2R_n} - Y_{cor} \tag{3.21}$$

where $\omega=2\pi f$ and f is frequency, i_d is channel noise and i_G is gate resistance noise.

Formulas (3.4) to (3.21) have been widely used in RF noise issues analysis. The extracted channel noise and induced gated noise can be used to verify different kinds of physics-based noise models of deep sub-micrometer MOSFETs.

3.4 Summary

In this chapter, devices used in our research work and the test structure layouts are introduced, followed by a discussion on pad de-embedding method. In addition, procedure for extraction of channel and induced gate noise on RF MOSFET has been presented, which will be used in following chapters for noise analysis.

Chapter 4

Hot-Carrier-Induced Damage and Its Spatial Location on MOSFETs High Frequency Noise

4.1 Introduction

The continuous downscaling of device feature size makes CMOS technology a viable choice for RF circuits because of its low cost, low power and high integration capability [3]. Based on the characterization, modeling, and analysis of RF noise in MOSFETs, a lot of efforts have been made to understand the physical origin of the excess channel noise in short-channel MOSFETs. As we discussed in Chapter 2, Knoblinger and Klein believe that excess noise are mainly due to the increase in lateral electrical field [21-22]; however, Chen and Deen, based on channel length modulation (CLM), showed that the noise contribution from the velocity saturation region is negligible [27]. Furthermore, recent theoretical studies using the hydrodynamic (HD) and full Langevin–Boltzmann equation (LBE) noise models, demonstrated that the channel noise is dominated by the source-side contribution due to higher impedance field near the source junction [29, 51]. Hence, whether the channel noise is dominant by the source or drain side is still controversial.

On the other hand, as device aggressively scales down, hot carrier (HC) induced degradation emerges as one of the most serious reliability issues in MOSFETs [52-56]. A clear understanding of hot-carrier effects in actual circuit environment is essential to ensure product reliability in the early stage of process optimization. In the past few years, hot carrier effects of MOSFETs have been studied thoroughly but mainly in DC and low frequency region. In view of the increasingly importance of CMOS technology for high frequency low noise applications, the impact of hot carrier effect on RF noise performance of MOSFETs has gained some attentions. It was found that the hot carrier stress induces substantial degradation on device noise characteristics such as NF_{min} and R_n [57-62]. The variation of RF noise performance due to the hot carrier induced damage was qualitatively explained by the degradation of transconductance (g_m) or reduction of the inversion charge density in the channel (Q_{inv}) for a fixed biasing point [57, 60]. However, from the microscopic point of view, noise is caused by local random fluctuation of the carriers. Therefore, it is important to know whether the current fluctuation induced by the exchange of charges between the hot-carrier-induced interface states and the channel will result in additional channel noise.

In this chapter, a comprehensive experimental study of the impact of hot carrier induced damage and its spatial location (source and drain) on the high frequency noise in 0.18-μm NMOSFETs will be given. The primary emphasis of this chapter is to provide a direct experimental verification on the spatial origin of the channel noise by characterizing the RF noise of different devices with the interface damages at different locations (drain- or source-side) in the channel region. The result also provides a better insight to hot carrier induced damage on RF noise performance in scaled MOSFETs.

4.2 Experiments

The devices under test are *n*-MOSFETs with multiple gate layout (16 gate fingers) with a drawn channel dimensions of L/W = 0.18 μm/5μm fabricated by standard 0.18-μm CMOS process flow (Chapter 3). An HP4156B semiconductor parameter analyzer was used for DC measurement and HC stress. For a Drain Avalanche Hot Carrier (DAHC) stress, the device was stressed at peak substrate current condition ($I_{b,max}$) with the drain bias V_{ds} = 3 V and gate bias voltage V_{gs} = 1.5 V for 3000 s. The source and substrate were shorted to ground during the stress. The stress results in interface states spatially distributed in a region near the drain side as shown in Figure 4.1(a). Two groups of devices were stressed for RF noise characterization. The devices in the first group (group 1) were undergone a normal DAHC stress resulting in drain side interface damage. The second group was subjected to the reverse DAHC stress where source and drain were swapped so that the HC-induced interface damage could be confined in a region near the source junction [Figure 4.1(b)]. The same biasing voltages and stress duration were used to ensure similar interface damage being created. During the hot carrier stress, shift of threshold voltage (ΔV_{th}), change of saturation current ($\Delta I_{d,sat}$) and transconductance (Δg_m) were carefully monitored, so that the devices with similar amount of interface states (ΔN_{it}) can be selected for RF noise characterization.

Device RF noise characterizations were carried out using a semi-auto Cascade probe station. The S-parameters were measured with a HP8510B network analyzer. Measurements of noise parameters were conducted by using ATN NP5 Noise and S-parameter Measurement Systems in the frequency range of 2 to 10 GHz. All of the parasitic effects from probing pads and interconnections were de-embedded following the approach proposed by Deen and Chen [46].

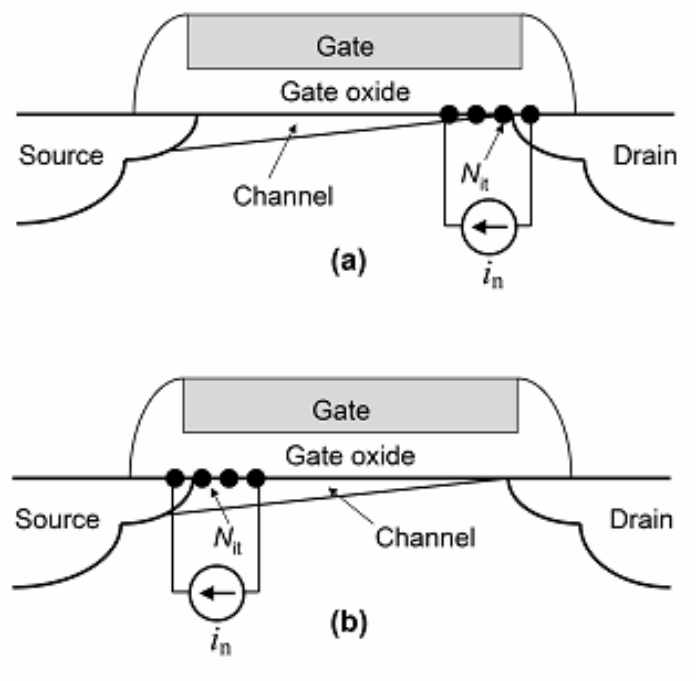


Figure 4.1: Interface states distribution in the MOSFET channel after DAHC stress: (a) Interface states at drain side induced by normal stress; (b) Interface states at source side induced by reverse DAHC stress.

4.3 Effects of Hot Carrier Stress on DC Characteristics

Figure 4.2 compares the I_{ds}-V_{ds} characteristics of *n*-MOSFETs with different HC induced damage locations. Presence of similar amount of hot carrier induced interface states N_{it} at source side results in slightly larger degradation of drain current compared to the one with drain side damage. This can be virtually found from the normalized drain current degradation ($\Delta I_{ds}/I_{ds0}$). The change of drain current at V_{ds}=1.8 V is ~12% if the damage region induced by hot carriers is at the source side. Whereas, there is only ~6% degradation of the drain current at the same bias condition when same amount of interface states are presented at drain side. Less drain current degradation observed from the devices with drain-side interface damage is due to

partial screening of the interface states in the channel pinch-off region as shown in Figure 4.1. On the other hand, the devices with source side damage, interface states contribute fully to the degradation of the carrier transport in the inversion channel, resulting in a relatively larger decrease in I_{ds}. Detailed modeling of the forward mode and reverse mode hot carrier stress was studied in [63].

Figure 4.3 shows the transfer characteristics of the devices with different damage locations. In general, hot carrier stress causes a large shift of V_{th}. It is also found that the change in V_{th} of the device with hot carrier damage at source side is larger than the one with drain-side damage. The percentage change of saturation threshold voltage $V_{th,sat}$ is 27.1% for the device with source-side damage. However, there is only about 11.1% variation in $V_{th,sat}$ if the damage is at the drain side.

The degradation of saturation transconductance (g_m) after hot carrier stress is shown in Figure 4.4. g_m is plotted against V_{gs}-V_{th} to exclude the effect of shift in V_{th} after hot carrier stress. The normalized transconductance degradation ($-\Delta g_m/g_m$) is shown in the inset of Figure 4.4. The maximum degradation of g_m are presented at V_{gs}-$V_{th} \approx 0.2$ V. The degradation of transconductance is much smaller compared to that of saturation current and V_{th}. Table 4.1 summarizes the changes of $I_{d,sat}$, V_{th} and g_m due to hot carrier stress. It can be seen that, for a given bias condition (i.e., fixed V_{ds} and V_{gs}), the degradation of drain current is mainly due to the shift of threshold voltage (i.e., the charge density in the inversion layer) rather than the reduction of carrier mobility and g_m. This serves as a useful implication for noise analysis in the following sections.

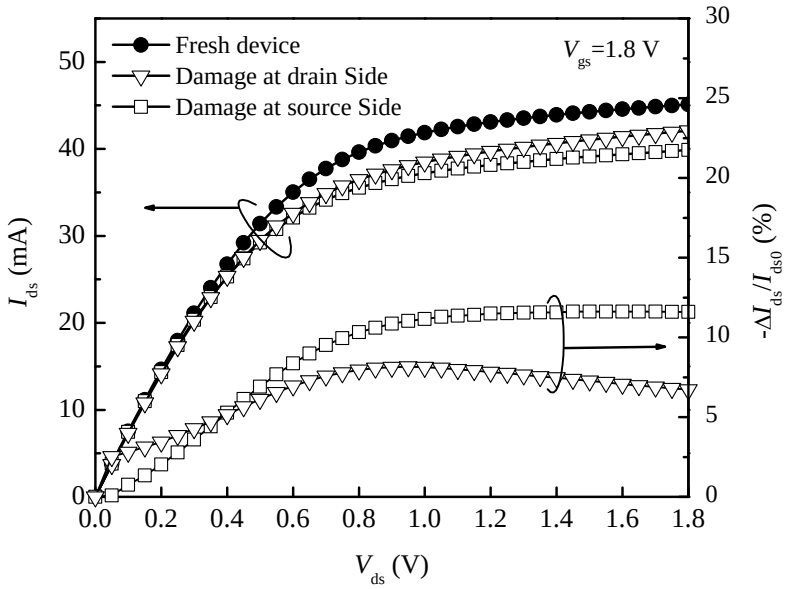


Figure 4.2: I_{ds} versus V_{ds} at V_{gs}=1.8 V for the devices before and after hot carrier stress. Normalized drain current degradation ($\Delta I_{ds}/I_{ds0}$) for the devices with source and drain side damage is also plotted for comparison. The transistors were subjected to the normal and reverse mode hot carrier stress with V_{ds}=3 V and V_{gs}=1.5 V.

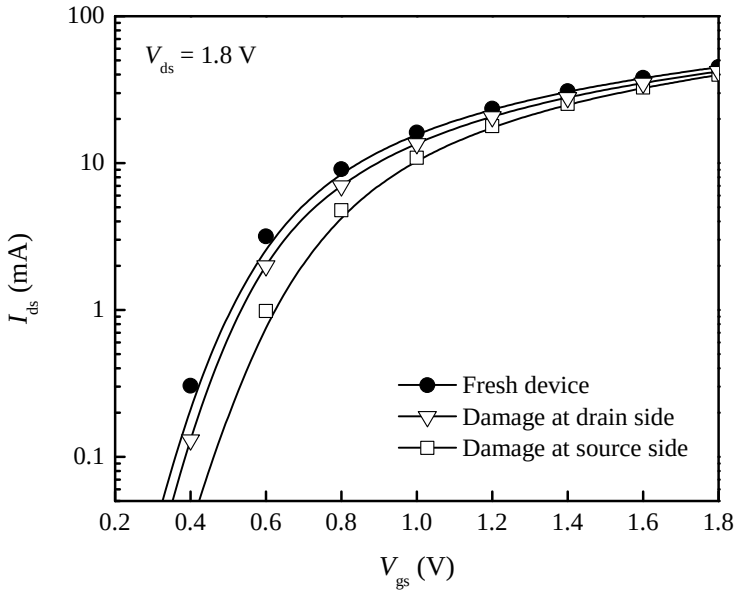


Figure 4.3: Typical I_{ds}-V_{gs} characteristics (V_{ds}=1.8 V) of the transistors before and after hot carrier stress. The transistors were subjected to the normal and reverse mode hot carrier stress with V_{ds}=3 V and V_{gs}=1.5 V.

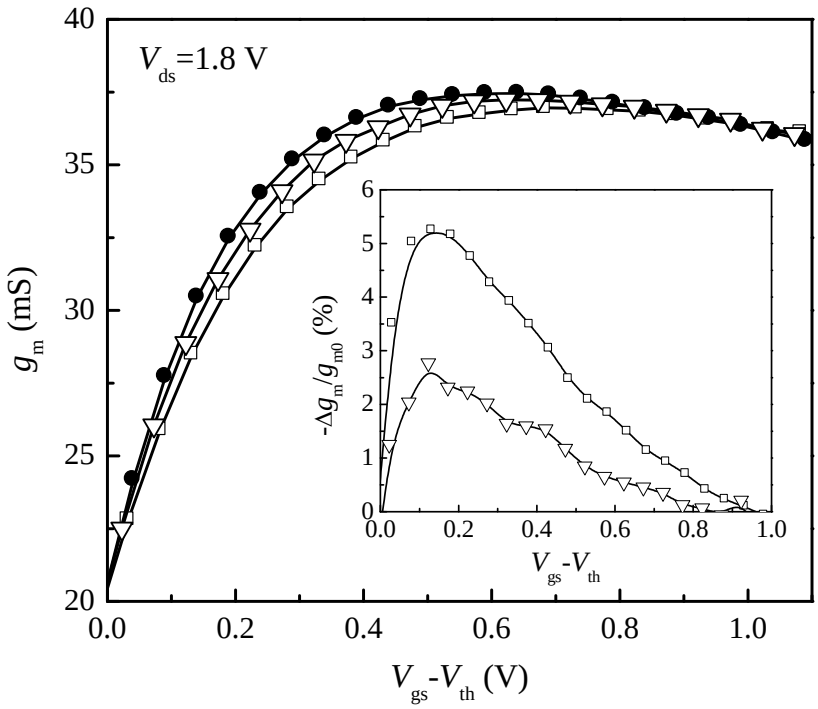


Figure 4.4: Saturation g_m as a function of V_{gs} - V_{th} before and after hot carrier stress. ● Fresh device; ▽ Damage at drain side; □ Damage at source side. Inset: Normalized transconductance degradation ($\Delta g_m/g_{m0}$).

Table 4.1: Normalized degradation percentage of $I_{d,sat}$, $V_{th,sat}$ and g_m due to hot carrier induced damage at both source and drain side.

Parameters	Damage Location	
	Source side	Drain side
$-\Delta I_{d,sat}/I_{d,sat0}$	12%	6%
$\Delta V_{th,sat}/V_{th,sat0}$	27.10%	11.10%
$-\Delta g_m/g_{m0}$	5.20%	2.80%

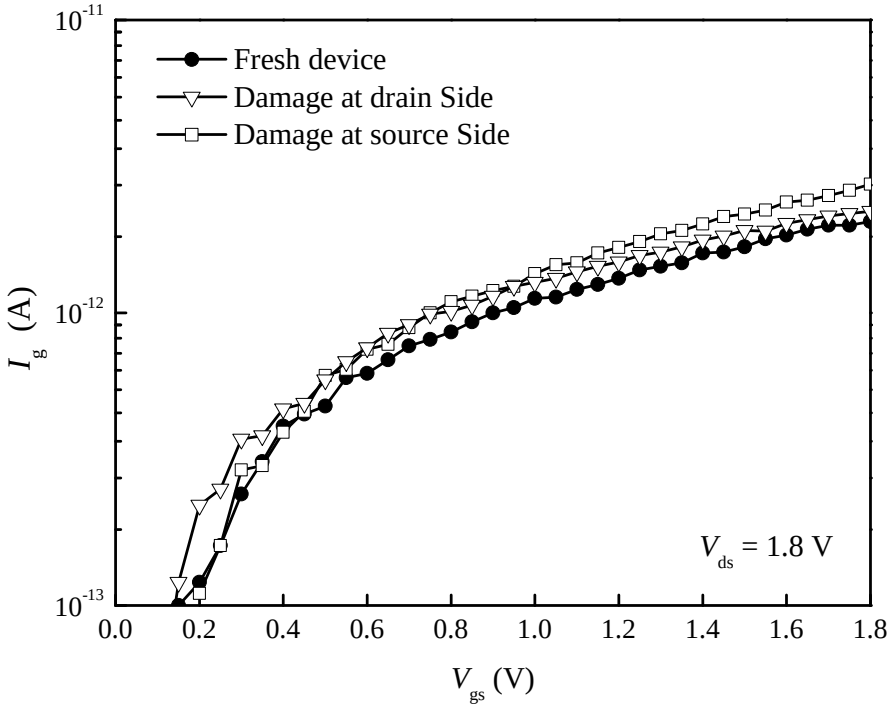


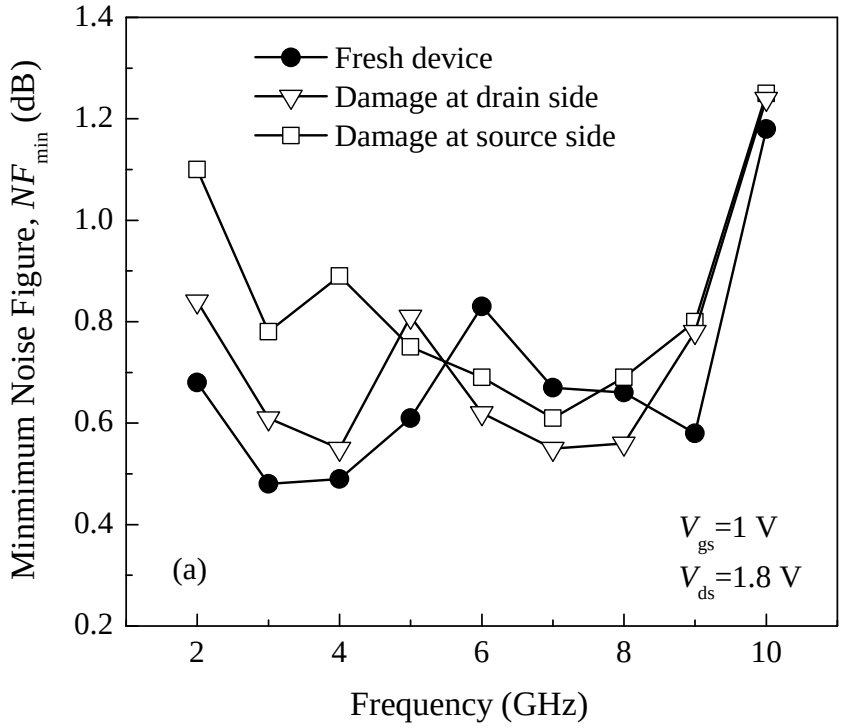
Figure 4.5: Gate leakage current I_g before and after hot carrier stress.

Finally, the impact of hot carrier stress on gate oxide leakage current was assessed and shown in Figure 4.5. The gate leakage current only shows a negligible increase regardless of damage location, and the current I_g is less than 3×10^{-12} A in the whole bias range. This small stress induced leakage current (SILC) suggests that the hot carrier damage to the bulk gate oxide is insignificant. Hence, Si/SiO_2 interface damage by hot carrier stress should be the dominant factor causing the device DC performance degradation.

4.4 Effects of Hot Carrier Stress on High Frequency Noise Characteristics

The effect of HC stress and its damaged location on minimum noise figure NF_{min} and noise resistance R_n are shown in Figure 4.6. The frequency dependence of NF_{min} shown in Figure 4.6 (a) indicates a general trend of increase on NF_{min} in the

frequency range of 2 to 10 GHz. As compared with the drain side damaged device, a larger increase in NF_{min} in the device with interface states near source-side can be seen. Although the effect of HC stress on NF_{min} at high frequency region is not obvious, the increase in R_n after HC stress can be clearly observed in both devices with drain- and source-side damages in the whole frequency range from 2 to 10 GHz. Again, device with source-side damage presents a larger increase in R_n. In the past, the deterioration of RF noise performance of MOSFETs after hot carrier stress was mainly attributed to the degradation of the charge density in the inversion layer of the channel (i.e., the channel conductance) and transconductance [57-58]. Therefore, if the change of the charge density in the inversion layer dominates the degradation of NF_{min} and R_n after hot carrier stress, by plotting NF_{min} and R_n against I_{ds} to exclude the influence of inversion layer charge density and mobility variations, negligible difference of NF_{min} and R_n between the fresh and stressed devices would be expected. However, as shown in Figure 4.7 (a), it is not the case. Hot carrier stress results in a dramatic increase in NF_{min}, and it can be seen even more clearly in Figure 4.7(b) by plotting R_n as a function of I_{ds}. Hot carrier stress significantly increases R_n in the whole bias range. Notably, in low I_{ds} region, the presence of interface damage at source side shows much greater impact on the degradation of NF_{min} and R_n. The experimental results suggest that, additional noise source could be involved in the post-stress MOSFETs besides the variation of inversion charge density. One of the possible mechanisms is the additional channel carrier fluctuation induced by capture and emission of charges at the hot carrier-induced interface states. Modeling of device RF noise to extract different noise components such as channel noise and induced gate noise is necessary to quantify this postulation, and will be discussed in the next section.



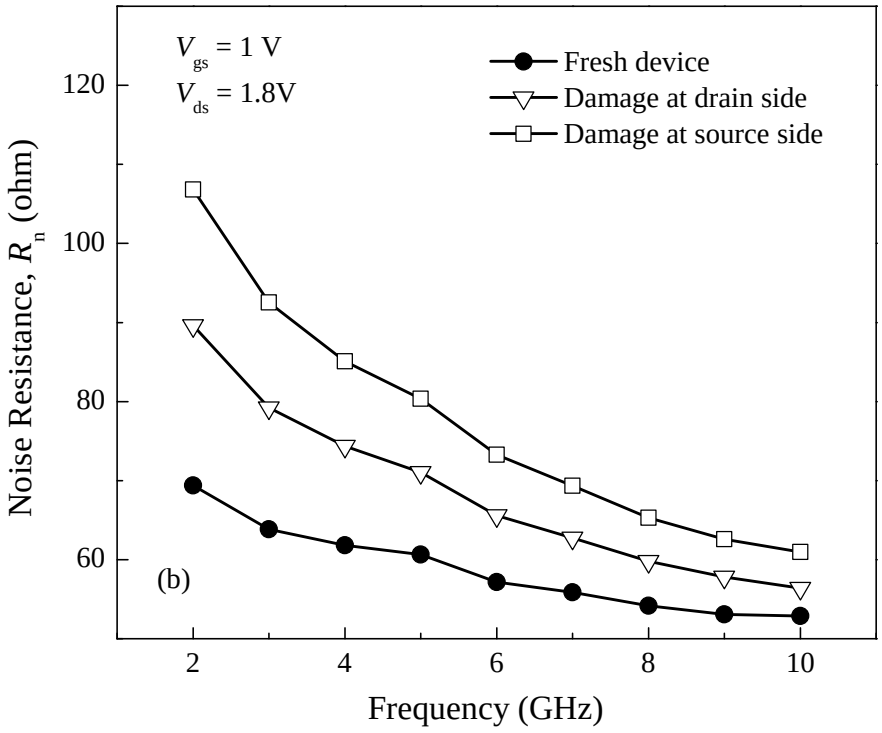


Figure 4.6: (a) Minimum noise figure NF_{min} and (b) equivalent noise resistance R_n as a function of frequency for the devices before and after hot carrier stress.

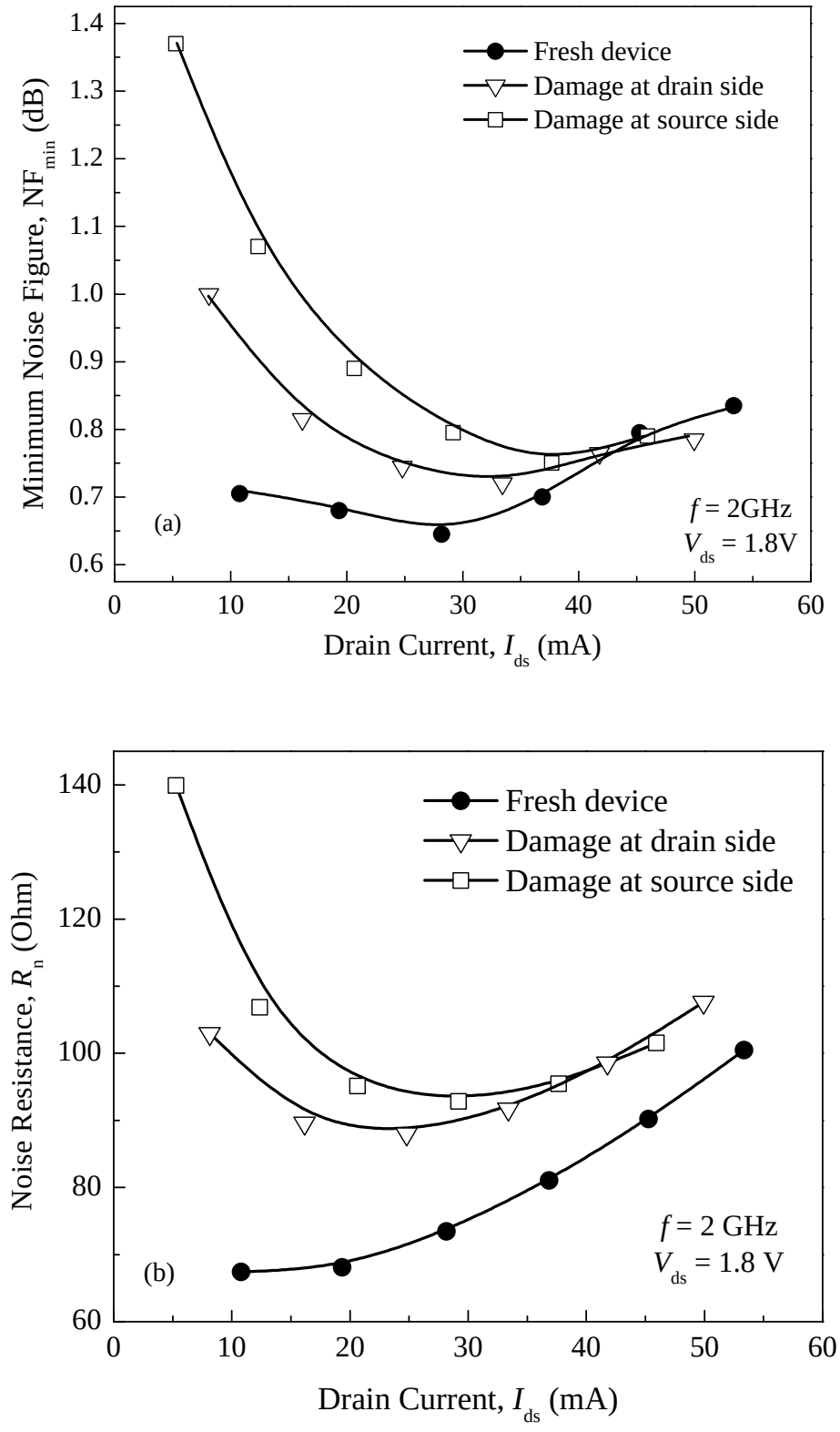


Figure 4.7: (a) Minimum noise figure NF_{min} and (b) equivalent noise resistance R_n as a function of drain current I_{ds} before and after hot carrier stress.

4.5 Additional Channel Noise due to Hot Carrier Stresses

Many different noise sources in MOSFETs might be important to the overall device noise [41, 47, 50], including channel thermal noise ($\overline{i_d^2}$), induced gate noise ($\overline{i_g^2}$), gate shot noise ($\overline{i_{g\_shot}^2}$), gate resistance noise ($\overline{i_G^2}$) and substrate noise ($\overline{i_b^2}$). Considering that the gate resistance and substrate noise are hardly affected by hot carrier stress, we will focus the analysis on the noise components such as $\overline{i_d^2}$, $\overline{i_g^2}$ and $\overline{i_{g\_shot}^2}$ which are directly associated with gate oxide and channel properties and potentially can be affected by the hot carrier stress. Since the gate leakage current in both fresh and stressed devices under investigation did not exceed a few picoamperes (pA) in the device operation region (see Figure 4.5) and was nine orders of magnitude smaller than the drain current, the gate leakage current should not contribute much to the overall output noise in the stressed devices. Normally, gate shot noise could be roughly estimated by [41]

$$\overline{i_{g\_shot}^2} = 2qI_g \ (\mathrm{A}^2/\mathrm{Hz}) \tag{4.1}$$

where I_g is the gate leakage current and q is the electron charge. As can be seen in Figure 4.5, in both fresh and stressed devices, we would see a gate shot noise $\overline{i_{g\_shot}^2}$ in the order of 10^{-31} A^2/Hz, which is quite small.

In order to determine the channel noise and induced gate noise, RF noise characteristics were modeled. The channel noise and induced gate noise were extracted by using the procedure developed by Chen *et al*. [49] , which was based on the scattering and RF noise parameters measured from the *n*-MOSFETs and other necessary “open” and “through” structures. The extracted channel noise and induced gate noise at 2 GHz as a function of drain current are shown in Figure 4.8. It can be

seen that the major impact of hot carrier stress is on the channel noise. The effect of hot carrier stress on the induced gate noise is also insignificant.

During the hot carrier stress, the defects will be created at or near the Si/SiO_2 interface which cause degradation of electron mobility μ and the inversion charge Q_{inv} along the channel. If the thermal noise in the channel is the major contributor to the overall channel noise, the channel noise can be expressed as [27]

$$S_{i_d} = 4kT\frac{\mu}{L^2}(-Q_{inv}) \propto I_d \tag{4.2}$$

where L is the channel length. According to Equation (4.2), the channel noise is proportional to the drain current. Therefore, plotting the extracted channel noise versus drain current can rule out any possible contribution from the variations of Q_{inv} and μ induced by hot carrier stress. Furthermore, if the change of Q_{inv} and μ in post hot carrier stress devices is the main mechanism for the variation of channel noise, plotting the channel noise against drain current should give a unified trend regardless of the stress condition or damage location. However, the dependences of the extracted channel noise on the drain current for different devices shown in Figure 4.8 do not support this postulation. Significant increase in channel noise can be seen from the devices after hot carrier stress for the whole bias range. Moreover, the device with source–side damage shows a larger increase in channel noise compared to the one with interface damage near the drain. The results shown here clearly suggest that, besides the channel thermal noise variation due to the changes of Q_{inv} and μ after hot carrier stress, additional noise source related to the hot carrier induced interface damage could play an important role. In other words, hot carrier stress does not only cause variations in Q_{inv} and μ, consequently, the channel thermal noise, but also adds a local noise source (i_n) to the device as illustrated in Figure 4.1. Depending on how the stress was performed, the additional noise source i_n may be presented at source

side or the drain side. The additional channel noise $\Delta\overline{i_d^2}$ due to the propagation of the i_n to the drain terminal is illustrated in Figure 4.9. One possible explanation for the additional noise source could be carrier fluctuation due to the exchange of charges between the channel and defects at and near the Si/SiO_2 interface. In order to contribute to the noise in GHz regime, the defect traps should be very close to or just at the interface so that tunneling can be very effective. In fact, studies on stress induced leakage current decay in ultra-thin gate oxide has revealed a minimum tunneling time constant of ~ 10^{-13} s. With this time constant, exchange of charge with the channel at GHz frequency is possible if the hot carrier induced traps are within several angstroms of the distance from the Si/SiO_2 interface [64]. The additional noise source is not necessary to be of thermal nature, a more specific discussion on the additional noise will be presented in Chapter 5.

Moreover, the presence of local noise i_n induced by hot carrier stress provides an effective approach to verify the spatial origin of the channel noise predicted by the theoretical simulation. In order to have a clearer picture of the spatial location of i_n on the additional channel noise measured at drain terminal, $\Delta\overline{i_d^2}$ were extracted by subtracting the channel noise of the fresh devices as illustrated in Figure 4.8 (a). Figure 4.9 shows $\Delta\overline{i_d^2}$ as a function of drain current I_{ds} for the devices with interface damages at source and drain side. Indeed, device with source-side damage (*i. e.*, a noise source introduced near to the source junction) shows a higher $\Delta\overline{i_d^2}$ at low and medium current region compared to the one with drain-side damage. This is consistent with the recent theoretical studies using the hydrodynamic (HD) and full Langevin Boltzmann equation (LBE) noise models, which suggested that the local noise at the source side plays a more important role in determining the overall channel noise.

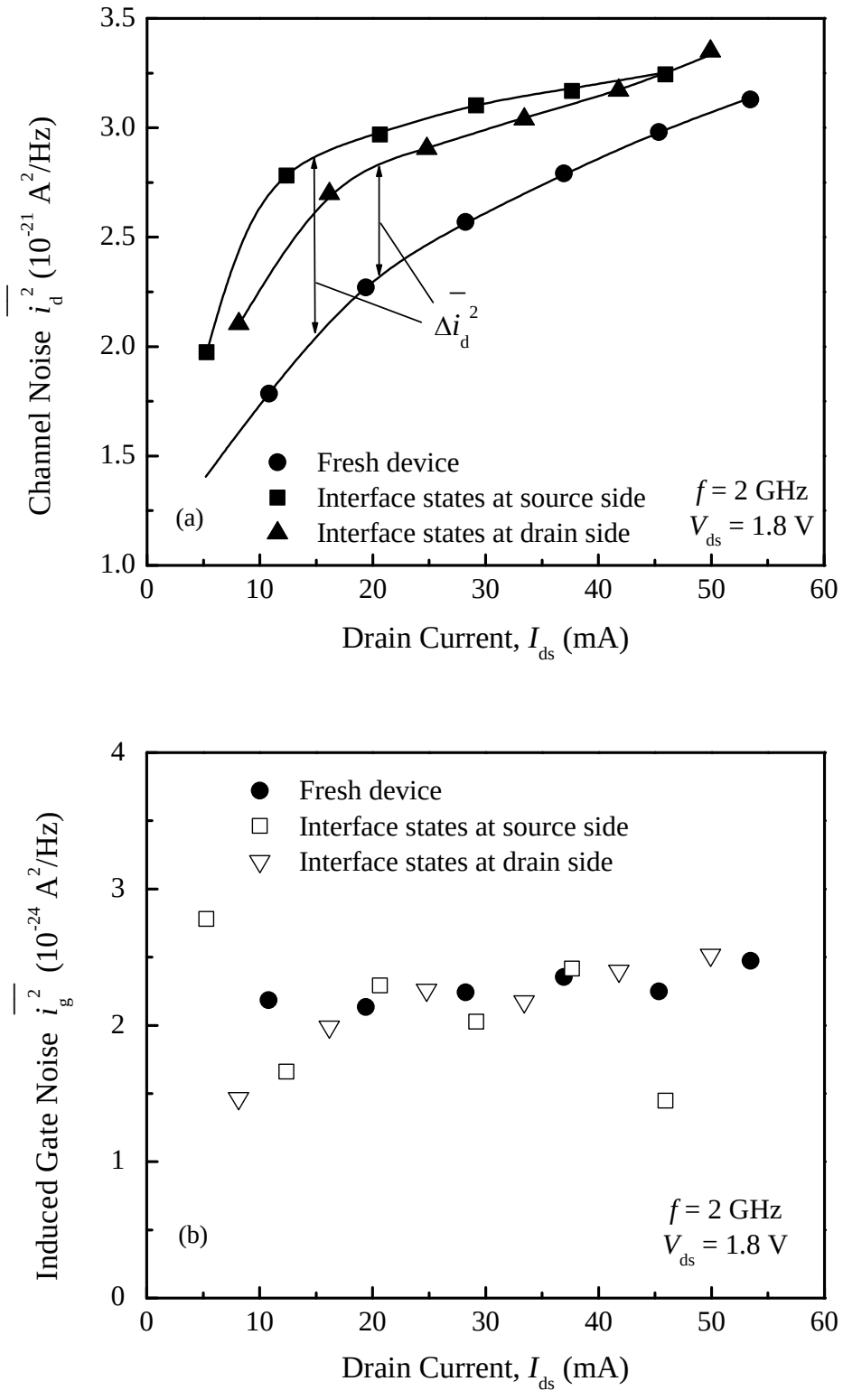


Figure 4.8: Extracted channel noise $\overline{i_d^2}$ (a) and induced gate noise $\overline{i_g^2}$ (b) as a function of drain current I_{ds} for *n*-MOSFETs before and after hot carrier stress.

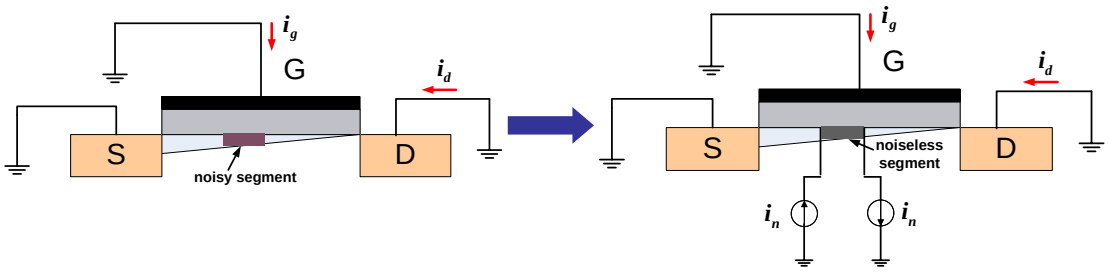


Figure 4.9: Basic concept of impedance field method. Left: Original device representation with a noisy segment; Right: Modified device representation adopting the impedance field method.

In the framework of the impedance field representation [31], channel noise at drain terminal is determined by two independent factors: local fluctuations, which can be considered as the local noise source i_n induced by hot carrier stress in our case, and their propagation to the drain electrodes. The basic concept of IFM is illustrated in Figure 4.9. The noisy segment of the MOSFET in the channel can be modeled as a noiseless segment with a current source. Therefore, the additional current noise power at drain terminal due to the presence of the local noise source induced by hot carrier damage can be calculated by

$$\Delta\overline{i_d^2} = |\Delta A_d|^2 \overline{i_n^2} \tag{4.3}$$

where ΔA_d is the impendence field, and can be expressed by the following approximation:

$$\Delta A_d \approx r_{oL} g_{mD} \tag{4.4}$$

r_{oL} is the local ac resistance of the damaged region, g_{mD} is the segmental transconductance for the channel segment between the hot carrier damaged region and the drain electrode.

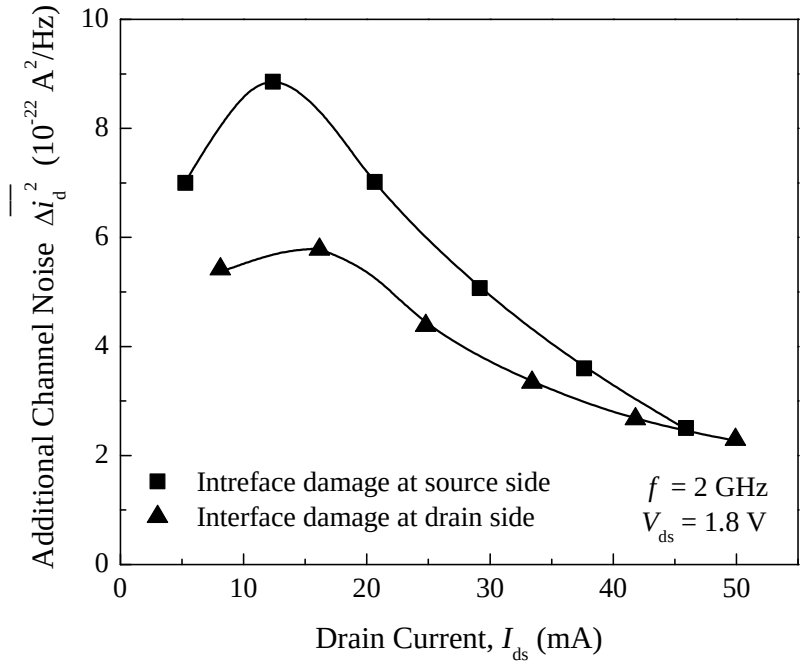


Figure 4.10: Additional channel noise components $\Delta\overline{i_d^2}$ as a function of drain current I_{ds} for the device with different damage locations.

The higher local ac resistance r_{oL} near the source junction is primarily responsible for the higher $\Delta\overline{i_d^2}$ observed in the MOSFET with source-side damage [29]. It is inversely proportional to the derivative of the carrier velocity with respect to the electric field in the channel. Generally, the electric field change near the source is quite small, which results in a higher local ac resistance and larger impedance filed. Figure 4.10 also suggests a strong gate bias dependence of the impedance field. For a fixed V_{ds}, at low gate voltage, the variation of the electric field near the drain junction is quite abrupt and much higher than the source junction. However, as the gate voltage becomes larger, the channel enters into strong inversion region, the electric field in the channel becomes more uniform and the field variation at the drain side is significantly decreased. As a result, difference in impedance field between drain and source end is

also greatly decreased. Thus smaller discrepancy of $\Delta\overline{i_d^2}$ for the devices with different damage locations is observed at high I_{ds}.

4.6 Summary

In summary, the impact of hot carrier induced interface damage on high frequency noise in deep sub-micrometer *n*-MOSFETs has been investigated. The increase in device noise parameters such as NF_{min}, R_n after hot carrier stress can be explained by the additional channel noise caused by the fluctuation due to the hot carrier induced interface damage. By using normal and reverse modes of drain avalanche hot carrier stress as an effective means to create local noise source in the channel near the drain or source junctions, the spatial origin of channel noise in submicron *n*-MOSFETs was experimentally examined. It is confirmed that the presence of interface damage at source side results in a larger increase in channel noise as compared to the devices with drain-side damage. This is consistent with the theoretical simulation using the hydrodynamic (HD) and full Langevin Boltzmann equation (LBE) noise models based on impedance field method (IFM) representation. The results provide direct experimental verification that the local noise at the source side plays a more important role in determining the overall channel noise.

Chapter 5

Role of Shallow Si/SiO$_2$ Interface States on High Frequency Channel Noise in *n*-MOSFETs

5.1 Introduction

As shown in Chapter 4, channel noise shows a significant dependence on the location of the HC damage at source or drain, however it remains unconcluded how the localized defect will contribute to the channel noise at gigahertz frequency. The physical mechanism of the excess noise due to HC induced interface damage will be presented in this chapter. In MOSFETs, channel noise is often referred as "white noise" and considered to be of sole thermal origin at high frequencies [65], the exact physical origin is still controversial in the literature. For instance, it is observed that channel noise of a virgin MOSFET exhibits weak frequency dependent behavior in gigahertz frequency region showing a higher noise value at lower frequencies. Ou *et al.* [66] attributed the slightly larger channel thermal noise at lower frequencies to the inaccuracy of the noise measurement system. Scholten *et al*. [47] suggested that the excess noise in lower frequency region came from gate or bulk parasitics. Goo *et al*. [67] lately demonstrated that the frequency dependent noise behavior can be partially explained by the additive noise contribution from the substrate resistance.

Furthermore, Pantisano and Cheung [68] suggested that flicker noise due to defect-induced fluctuation rather than thermal noise could be more favorable to explain the noise behavior of the MOSFETs in gigahertz range. On the other hand, in the past few decades, the impact of hot carrier (HC) stress on low frequency noise of MOSFETs has been extensively investigated [37, 69]. It is generally believed that low frequency noise of MOSFETs originates from capture/release of charge carriers by oxide traps which have relatively deep energy levels and long time constants [70]. Sah and Jie [71] recently suggested that with the presence of the oxide traps or interface states at energy levels close to conduction or valence band edges, gigahertz noise could be generated from carrier transitions between these interface traps/states and the conduction or valence bands. A similar point was also addressed by Pantisano and Cheung [68]. However, no experimental confirmations have been made so far.

In this chapter, the effects of interface states generated during HC stress on HF channel noise in *n*-MOSFETs were investigated. We found that the presence of Si/SiO$_2$ interface states result in a frequency dependent excess channel noise in the gigahertz range. The excess channel noise can be well predicted by using van der Ziel's current fluctuation model with a characteristic time constant on the order of 10^{-11} s. This could be explained by carrier capture and emission mechanisms associated with the shallow Si/SiO$_2$ interface states. An activation energy E_a of ~0.033 eV for the excess channel noise is determined by temperature dependent noise measurement which further supports our conclusion.

5.2 Experiment

The device under test is *n*-MOSFET same as those used in Chapter 4, and is stressed under maximum substrate current condition ($V_{gs} \approx 1/2\ V_{ds}$ = 1.5 V) for 3000 s. As shown in Figure 5.1, an U-shape distribution of interface states is believed to be

generated inside the forbidden bandgap when MOSFETs are subjected to hot carrier stress [72-73], resulting in a high density of shallow interface states near the conduction or valence band edge. The different energy levels of interface states are determined by the different released energy, which are related to the carrier energy obtained from the stress electrical field. Therefore, shallow-level interface states are mainly due to carriers with smaller released energy, while deeper-level traps might be created by a small portion of the carriers with higher energies due to fewer collisions before recombination.

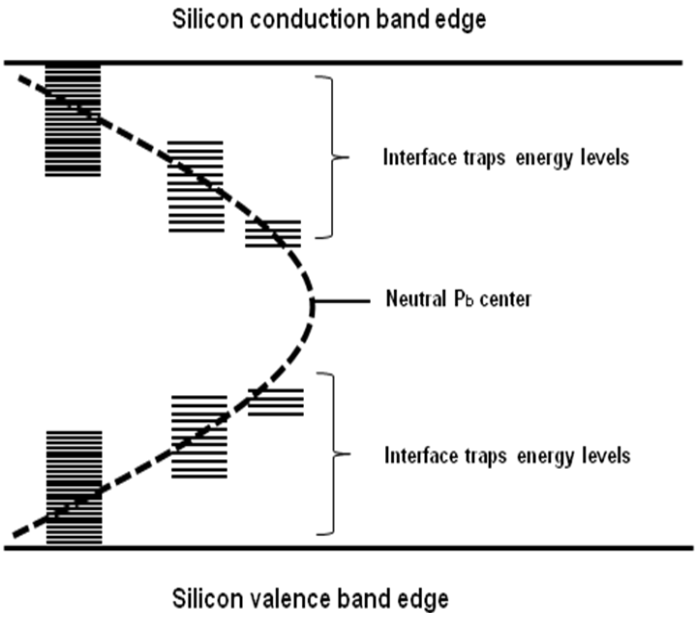


Figure 5.1: Illustration of the shallow interface states/traps energy levels in the silicon band gap. The energy of a neutral P_b denotes the silicon midgap [72].

5.3 Shallow Si/SiO$_2$ Interface States on MOSFET High Frequency Noise Performance

Figure 5.2 shows the measured minimum noise figure NF_{min} at a fixed drain current I_{ds} = 35 mA as a function of frequency. NF_{min} increase in the frequency range below 10 GHz is clearly observed after hot carrier stress. The impact of hot carrier

stress on MOSFET high frequency (HF) noise performance has previously been studied by different research groups. The increase in NF_{min} (or R_n) were explained by the reduction of the transconductance g_m [57] or the increase in the parasitic series resistances [74]. In Chapter 4, we have demonstrated that the hot carrier stress induced additional channel noise but not discuss the details on the physical origin of this additive noise source. In order to assess the effect of hot carrier stress on channel noise directly, the channel noise $\overline{i_d^2}$ was extracted following the method described in [49] for both virgin and stressed devices. Figure 5.3 compares the change of $\overline{i_d^2}$ due to hot carrier stress, and the data is plotted in both linear and log scale in Figure 5.3 for clarity. If the channel noise is considered as thermal type, it can be expressed by inversion layer charge density Q_I and electrical channel length L_{ele} as [27]

$$\overline{i_d^2} = 4kT\mu(-Q_I)/L_{ele}^2 \qquad (5.1)$$

we can see that channel noise is proportional to the magnitude of the drain current (I_{ds}). Therefore, we would expect a negligible change or small reduction of $\overline{i_d^2}$ after hot carrier stress (due to mobility μ reduction) if the channel noise $\overline{i_d^2}$ is plotted at a fixed I_{ds}. However, as shown in Figure 5.3, after hot carrier stress, $\overline{i_d^2}$ at I_{ds} = 35mA exhibits a noticeable increase in the frequency range of 2 to 10 GHz. The frequency dependent behavior of $\overline{i_d^2}$ strongly suggests that the excess channel noise induced by hot carrier stress may not be attributed to the inherent thermal noise. A non-thermal type of noise which associated with stress induced interface states/traps may play an important role.

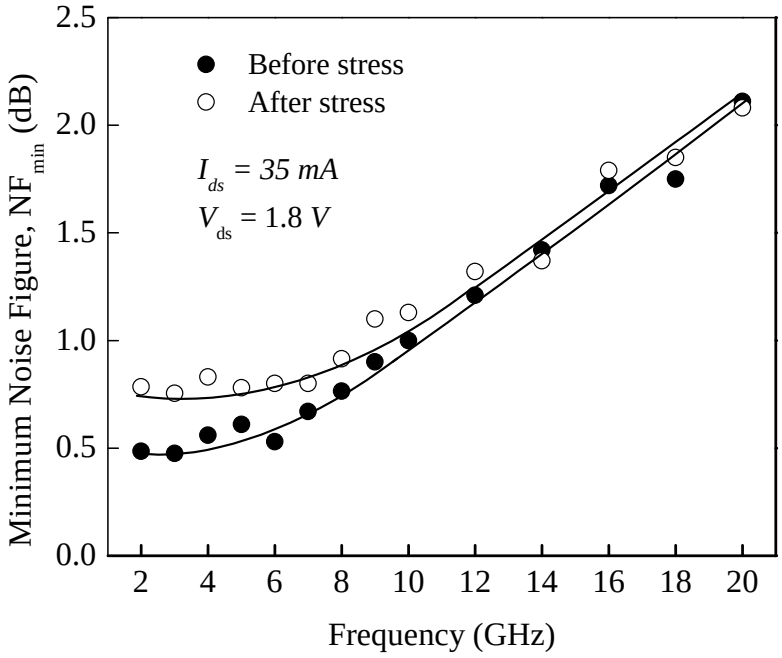


Figure 5.2: Minimum noise figure NF_{min} as a function of frequency for device before and after hot carrier stress.

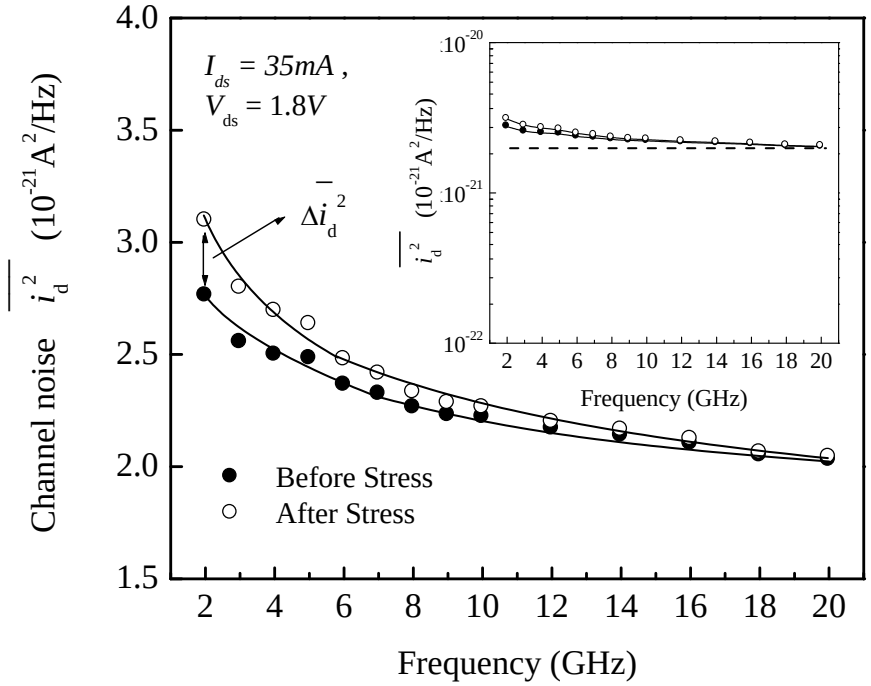


Figure 5.3: Extracted channel noise $\overline{i_d^2}$ as a function of frequency for device before and after hot carrier stress. Inset: Replot the channel noise $\overline{i_d^2}$ versus frequency in log-scale.

5.4 Physical Origin of Excess Channel Noise due to Shallow Si/SiO$_2$ Interface States

In this section, we will further investigate the physical origin behind the excess channel noise. The additional channel noise component $\Delta\overline{i_d^2}$ induced by HC stress which is the difference of channel noise between the stressed and fresh devices ($\overline{i_{d,\text{stressed}}^2} - \overline{i_{d,\text{fresh}}^2}$) is plotted in Figure 5.4. The $\Delta\overline{i_d^2}$ shows a strong frequency dependent behavior and it decreases with the increase of frequency. If the carrier density fluctuation is due to the presence of defect related transitions, such as exchange of carriers between the interface states and the channel, the power spectral density of $\Delta\overline{i_d^2}$ can be predicted by van der Ziel's channel current fluctuation model in the form of [75]

$$S_{i_d} = \frac{A\tau}{1+(2\pi f)^2\tau^2}, \tag{5.2}$$

where τ is the characteristic time constant associated with the mechanism causing the current fluctuation. As can be seen in Figure 5.4, by assuming that only one physical mechanism contributes to the excess noise due to HC stress, the experimental data can be well fitted by a single characteristic time constant of 45.9 *p*s using Equation (5.2). The small time constant obtained here may allow us to link the excess channel noise to the carrier transitions between the shallow interface states and conduction band in an *n*-MOSFET, which is illustrated in the inset of Figure 5.4. The charge capturing and releasing at the shallow Si/SiO$_2$ interface states may substantially cause carrier fluctuation in the channel and results in additional channel noise. If the carrier transitions are dominated by the shallow interface states at the Si/SiO$_2$ interface, the

transition time can be significantly small so that carrier fluctuation (noise) at gigahertz frequencies could happen [76].

Above postulation can be supported by measuring and extracting the excess channel noise at different temperatures. Arrhenius plot of $\Delta\overline{i_d^2}$ at 2 GHz shown in Figure 5.5 reveals an activation energy E_a of 0.033 eV. This indicates that the Si/SiO$_2$ interface states responsible for the excess channel noise in post stressed *n*-MOSFETs in gigahertz region lie quite close to the silicon conduction band. The characteristic time constant of the current fluctuation, which is representative of electron trapping and detrapping processes at the shallow interface states, can be approximately estimated by [76]

$$\tau = 2\exp[(E_c - E_{it})/kT]/(N_c\sigma_{it}\upsilon_{th}), \tag{5.3}$$

where E_c and E_{it} are the energy levels of the conduction band and shallow interface states/traps, N_c is the effective density of states in the conduction band, σ_{it} is the electron capture cross section at the interface states/traps, and υ_{th} is the electron thermal velocity. Using $E_c - E_{it} \cong 0.033$ eV, $\upsilon_{th} \cong 10^7$ cm/s, and $\sigma_{it} \cong 10^{-15}$ cm^2 [76], we would expect a characteristic time constant of 25.3 *p*s, which is in a good agreement with the value extracted in Figure 5.4. If the individual characteristic time constant is related to activation energy E_a via the expected $\tau = \tau_0 \exp(E_a/kT)$, based on the experimental results of τ = 45.9 ps and E_a = 0.033 eV, we can obtain an "attempt to escape frequency" τ_0 of 13 *p*s. The value is much higher than the reported τ_0 of 1.8×10^{-15} s associated with oxide border traps (O vacancy-related defects in SiO$_2$) that contribute to 1/*f* noise [77]. This suggests that the high frequency channel noise associated with the shallow interface states may not share the same microscopic mechanism responsible for the 1/*f* noise, which warrants follow-up study.

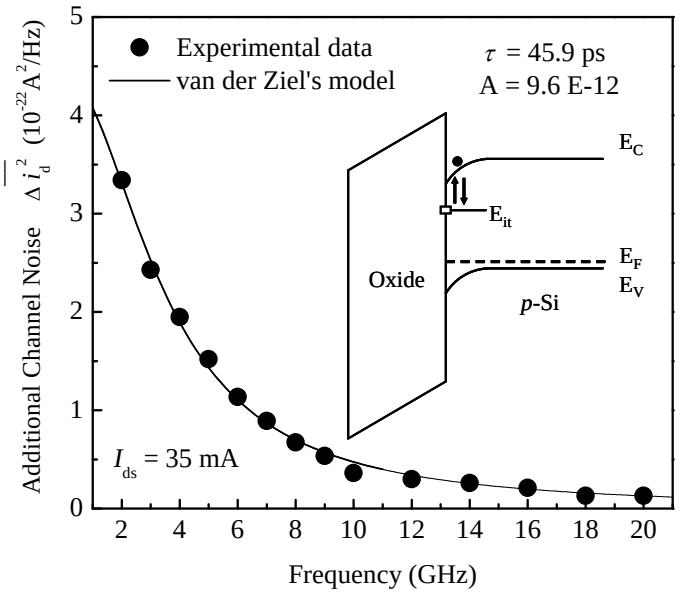


Figure 5.4: Excess channel noise $\Delta\overline{i_d^2}$ induced by hot carrier stress as a function of frequency. The schematic diagram illustrates possible capture and emission of electrons between the shallow interface states energy level and the silicon conduction band is shown at the inset.

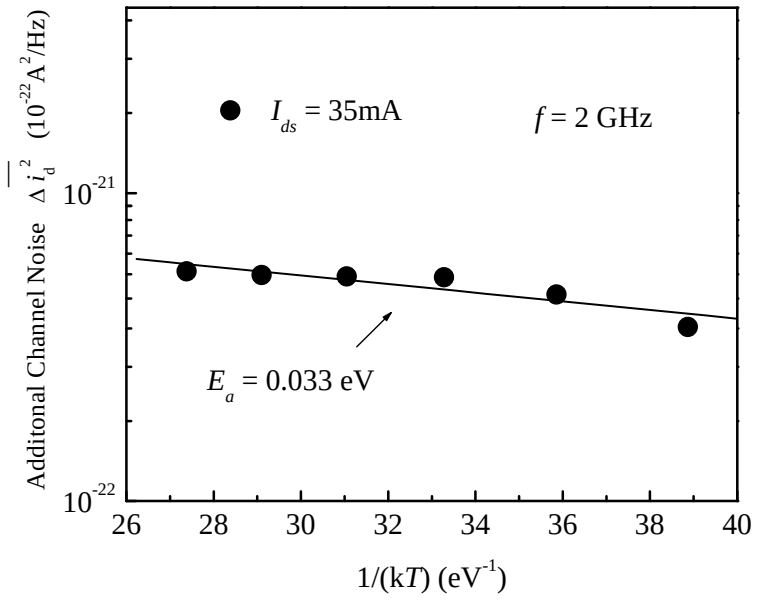


Figure 5.5: Excess noise $\Delta\overline{i_d^2}$ as a function of $(kT)^{-1}$. Activation energy of 0.033 eV is extracted.

5.5 Summary

In summary, the channel noise of *n*-MOSFETs has been characterized and analyzed to gain a fundamental understanding of the physical origin of the excess channel noise induced by HC stress. The experimental results obtained in this chapter reveal a strong correlation between the excess channel noise component and carrier transitions associated with shallow Si/SiO_2 interface states. This suggests that the shallow Si/SiO_2 interface states in MOSFETs play an important role in determining the channel noise in gigahertz frequency range.

Chapter 6

High Frequency Noise Degradation in *n*-MOSFETs under Different Hot Carrier Stresses

6.1 Introduction

In Chapter 5, we have analyzed frequency dependent excess channel noise (GHz) generated by hot carrier stress. The excess noise was explained by carrier capture and emission with HC induced shallow interface states, and is strongly supported by characteristic time and activation energy extracted from measurement data. On the other hand, it has been well established that 1/*f* noise originates from oxide traps, and the degradation is found to be proportional to the oxide trap density [53, 55, 69]. Therefore, device noise (GHz) performance dependency on HC induced defects (interface states and oxide traps) should be further investigated.

In this chapter, high frequency noise performances under different types of hot carrier stresses were studied. It is found that high frequency noise degradation is strongly dependent on the stress conditions. Noise parameters NF_{min} and R_n show much larger increase if device is stressed under maximum substrate current ($I_{B,max}$) or hot hole (H_{inj}) injection than under hot electron (E_{inj}). Possible mechanism is the significant differences in the channel noise increment from interface states/traps and

oxide traps. The presence of interface states/traps generated by $I_{B,max}$ stress and hot hole injection (H_{inj}) caused substantial channel noise increase through capture and emission of electrons at HC induced interface states/traps. On the other hand, the effects of oxide traps generated by hot electron injection on channel noise are insignificant because they fluctuate too slowly to be detected as RF noise.

6.2 Different Types of Hot Carrier Stresses

The hot-carrier induced degradation processes are initiated by the injection of high-energy carriers from the channel of the device into the gate oxide. The physical mechanisms which are involved in the device degradation are strongly dependent on the relative concentration of electrons and holes injected at any given location along the channel. This section provides a qualitative analysis of the dependence of electron and hole injection currents on the gate bias of a conventional *n*-channel MOSFET. As shown in Figure 6.1, at relatively low gate biases, the transverse electric field and the barrier lowering favor the injection of holes over electrons. The oxide field under this condition also favors the transport of the injected holes to the gate terminal resulting in a gate current comprised primarily of holes. As the gate bias increases, the barrier lowering effect for holes levels off while the electron injection current continues to increase due to a relatively smaller barrier height for electrons. However, as long as a repulsive field is present in the oxide, the injected electrons are scattered back to the interface. Therefore, the gate current under these gate biases is negligible compared to the electron injection current. At higher gate biases, the repulsive oxide field decreases and a larger proportion of injected electrons contribute to the gate current resulting in a peak gate current around $V_{gs} = V_{ds}$. For $V_{gs} > V_{ds}$, the lateral electric field close to the drain decreases with increasing gate bias and hence the electron injection current also decreases.

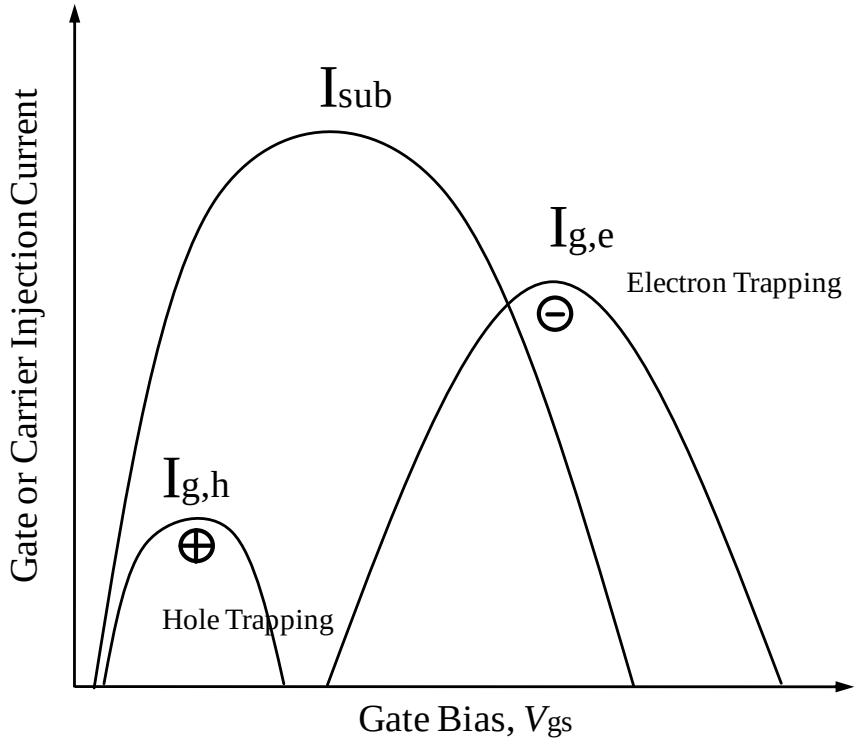


Figure 6.1: The dependence of carrier injection and gate current on the gate bias in a conventional n-channel MOSFET [78].

Table 6.1: Dependence of injection and degradation modes on the gate bias in n-channel MOSFETs.

Stress Condition	Injected Carrier		Degradation Process		
	electron	hole	ΔN_{it}	Δn_{trap}	Δp_{trap}
$I_{B,max}$ $(V_{gs} \approx V_{ds}/2)$	y	y	y	n	n
E_{inj} $(V_{gs} \approx V_{ds})$	y	n	n	y	n
H_{inj} $(V_{gs} \leq V_{ds}/4)$	n	y	y	n	y

With different gate bias condition, the expected degradation modes under each of the three injection conditions along with the type of carriers injected are listed in the Table 6.1. In the earlier studies of n-channel devices, it was observed that the degradation in *n*-MOSFETs is predominant due to the increase in interface state density at the gate bias which resulted in the maximum substrate current. However recent works show that hole injection under low gate-biases and electron injection under high gate biases can also result in significant device degradation under circuit operation. Mistry *et al.* identified three dominant degradation modes in *n*-channel MOSFETs and incorporated their effects into an AC lifetime model [79-81]. According to their study, the device degradation is dominated by the increase in interface states at mid-gate biases ($V_{gs} \approx V_{ds}/2$), close to $I_{B,max}$ condition. At the same time, interface states/traps and oxide traps are generated at low gate biases ($V_{gs} \leq V_{ds}/4$) under hot hole injection (H_{inj}) while the device degradation is dominated by carrier trapping during hot electron injection (E_{inj}) at high gate biases ($V_{gs} \approx V_{ds}$) along with a small increase in interface state density. For the case of channel hot-carrier injection in *n*-MOSFETs, it is difficult to separate the role of electrons and holes in the interface states generation because both types of carriers are injected into the gate oxide during stresses. Although the mechanism of interface states generation remains controversial, hot hole injection is reported to be more efficient than electrons at interface state generation, and the trapping rate of hole are also much higher than electrons [82-84].

6.3 Experiments

Same *n*-MOSFETs as those in Chapter 4 and 5 are used here for experiments. In order to monitor the device behavior under each of these degradation modes, we

performed three different sets of DC stressing experiments. Hot carrier stresses with drain avalanche hot carrier stress ($I_{B,max}$: V_{gs} = 1.5 V, V_{ds} = 3 V), channel hot electron stress (E_{inj} : V_{gs} = 3 V, V_{ds} = 3 V) and hot hole injection (H_{inj} : V_{gs} = 0.6V, V_{ds} = 3 V) were carried out respectively to investigate the high frequency noise degradation mechanisms. In order to achieve same percentage of I_{ds} degradation, device was stressed 3,000s for $I_{B,max}$, 4,600s for hot electron injection (E_{inj}), and 17,500s for hot hole injection (Figure 6.2). The source and substrate were shorted to the ground. During the HC stress, the shift of threshold voltage (V_{th}), change of saturation current (I_{ds}), and transconductance (g_m) were carefully monitored.

6.4 The Impact of Different Hot Carrier Stresses on *n*-MOSFETs DC Performance

Hot carrier degradation has attracted tremendous studies in the past few decades. Normally, device parametric shifts (saturation current I_{ds}, threshold V_{th}, transconductance g_m), arise from three categories of degradation mechanisms: the generation of interface states/traps ΔD_{it}, positive oxide traps ΔN_{ot}^{+} and negative oxide traps ΔN_{ot}^{-}. As shown in section 6.2, for short-channel *n*-MOSFETs: 1) at maximum substrate current stress ($V_{gs} \approx V_{ds}/2$), the dominant degradation mechanism is attributed to interface states/traps ΔD_{it}; 2) at low V_{gs} stress ($V_{gs} \leq V_{ds}/4$), device degradation is attributed to hole trapping ΔN_{ot}^{+} as well as interface states/traps; 3) at the condition of a high gate bias ($V_{gs} \approx V_{ds}$), hot electron dominates and results in electron trapping ΔN_{ot}^{-} [85] (Figure 6.1).

In this study, saturation drain current I_{ds} percentage decrease ($\%\Delta I_{ds}$) is used as the monitor of the device degradation, and it is shown in Figure 6.2. It is clearly seen that the worst-case degradation occurs at the condition of maximum substrate current

$I_{B,max}$, followed by electron injection (E_{inj}) and then hole injection (H_{inj}). The time power factor n is 0.42, 0.49, 0.35 for $I_{B,max}$, E_{inj} and H_{inj} stress conditions, respectively. The fractional increase of V_{th} in linear operation mode (V_{ds} = 0.1 V) is shown in Figure 6.3. The shift of V_{th} for $I_{B,max}$ stress and hot electron injection are similar, at ~20%, while the shift of V_{th} is less at ~15% for hot hole injection.

Figure 6.4 shows the percentage decrease of linear transconductance (% Δg_m) (V_{ds} = 0.1 V). It shows that power-law slope is n = 0.51 at $I_{B,max}$ stress condition, while the slope is 0.34 and 0.77 for hot electron injections and hot hole injection, respectively. Similar power slope values are also reported in previous studies [57, 59], indicating different underlying degradation mechanisms for three hot carrier stress conditions. The g_m degradation are examined in Figure 6.5 in both linear and saturation mode. At V_{ds} = 0.1 V, peak g_m reduces by 19 % after $I_{B,max}$ stress, followed by 14 % for hot electron injection (E_{inj}) and 12 % for hot hole injection (H_{inj}). On the other hand, the decrease on saturation peak g_m is only about 3%, and the degradation is comparable under three different hot carrier stress conditions. The much less degradation of $g_{m,sat}$ than $g_{m,lin}$ is mainly attributed to the well known screening effect, because HC induced damages are mainly localized near the drain side, such that it is masked by the pinch-off region [63].

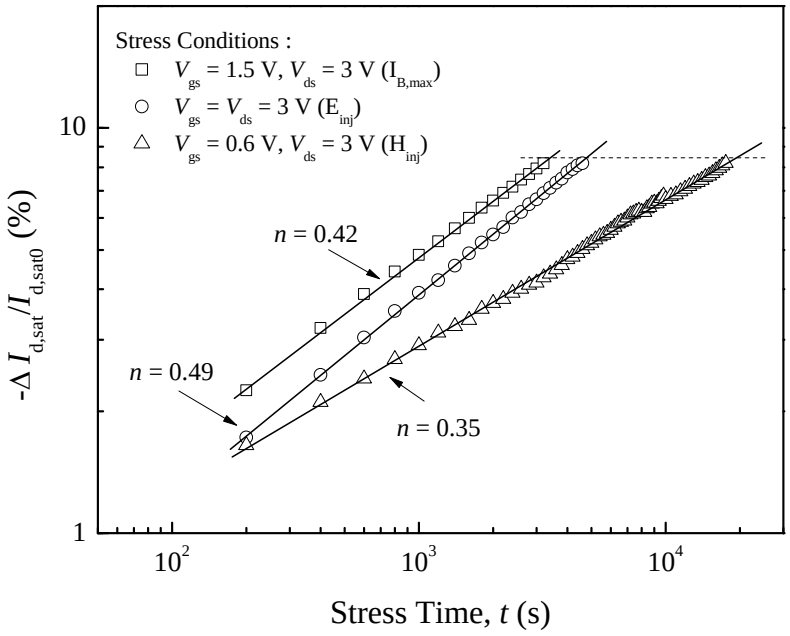


Figure 6.2: Fractional decrease in drain current $\Delta I_{d,sat}/I_{d,sat0}$ under different hot carrier stresses as a function of stress time *t*.

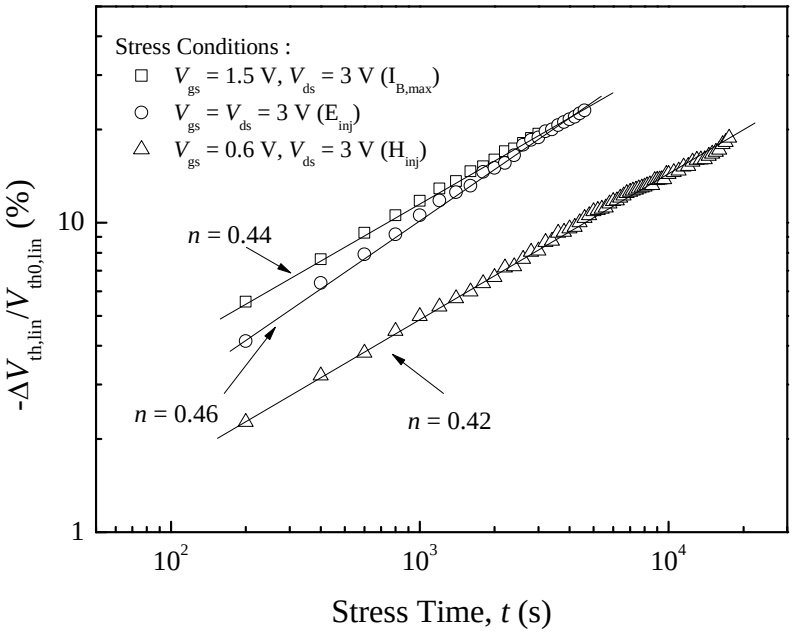


Figure 6.3: Fractional increase in threshold voltage in linear region $\Delta V_{th,lin}/V_{th,lin}$ under different hot carrier stresses as a function of stress time *t*.

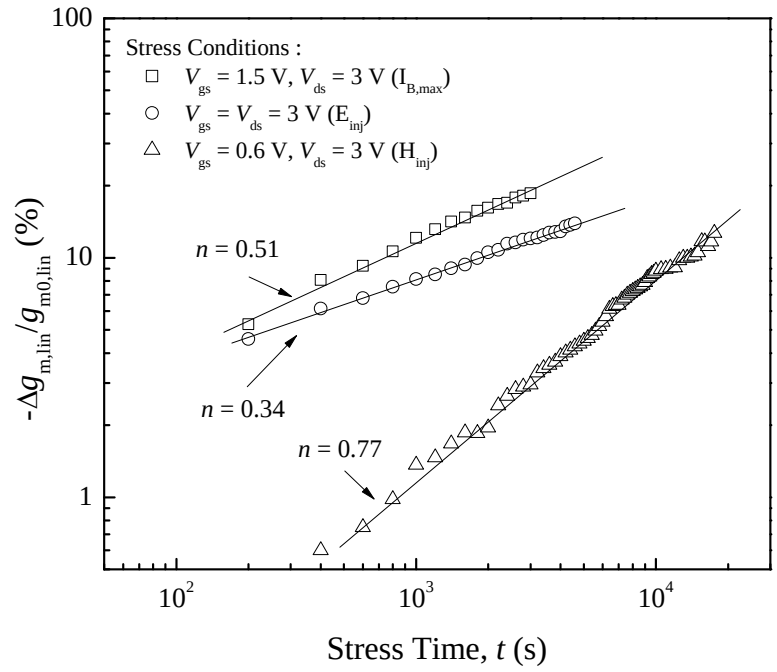


Figure 6.4: Fractional degradation of transconductance g_m under different hot carrier stresses as a function of stress time *t*.

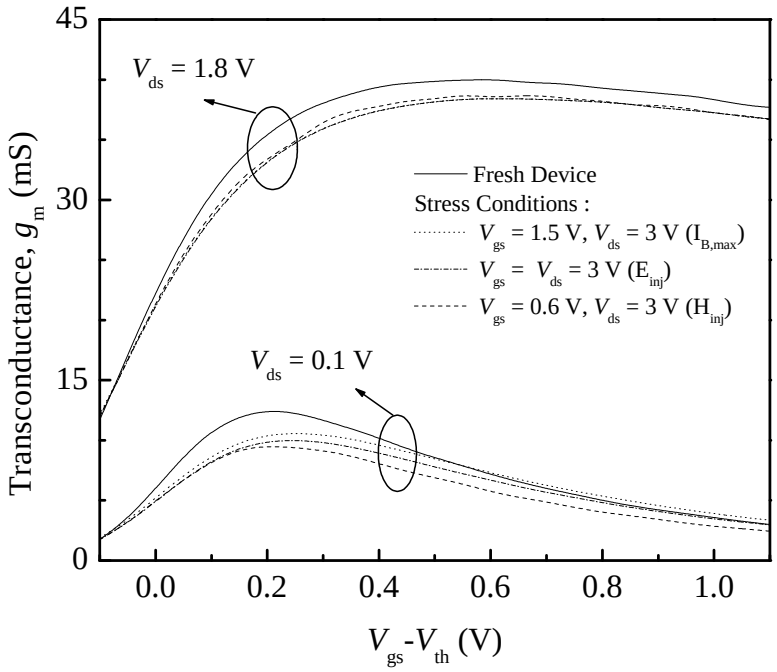


Figure 6.5: Transconductance g_m degradation before and after hot carrier stress as a function of V_{gs}-V_{th}.

6.5 *n*-MOSFET RF Performance Degradation under Different Hot Carrier Stresses

The cut-off frequency (f_T) is one of the most important figure of merits (FOM) to the characterization of device RF performance, and has been determined as the frequency where the current gain is 0 dB. Figure 6.6 shows a plot of the cutoff frequency (f_T) versus drain current (I_{ds}) before and after hot carrier stresses. Generally, the analytical expression of f_T for MOSFET is given by [59]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{6.1}$$

where g_m is the transconductance, C_{gs} and C_{gd} are gate-source and gate-drain capacitances, respectively. The peak cutoff frequency f_T (saturation region, V_{ds} = 1.8V) decreases by about 5 % and it is observed that three post-stressed f_T curves are nearly indistinctive, which matches well with the saturation g_m curves shown in Figure 6.5. It has been demonstrated recently that the reduction of f_T is primarily due to the decrease in g_m and increase in C_{gs}, while C_{gd} is hardly changed after hot carrier stress [57]. Moreover, it is reported that, f_T degradation ($\Delta f_T/f_T$) is found to be proportional to drain current degradation ($\Delta I_{ds}/I_{ds}$) regardless of stress conditions, and the ratio is about 0.6 in both linear and saturation region [59]. This well explained the negligible difference in f_T degradation observed between different hot carrier stresses, because I_{ds} degradation are purposely made to be same in our experiment (Figure 6.2). The relation of peak f_T degradation and I_{ds} degradation is about 0.65 in this study. It is noted that the degradation of f_T will give a great impact on CMOS RF circuits such as LNA (low noise amplifier), mixer and power amplifiers [61, 86].

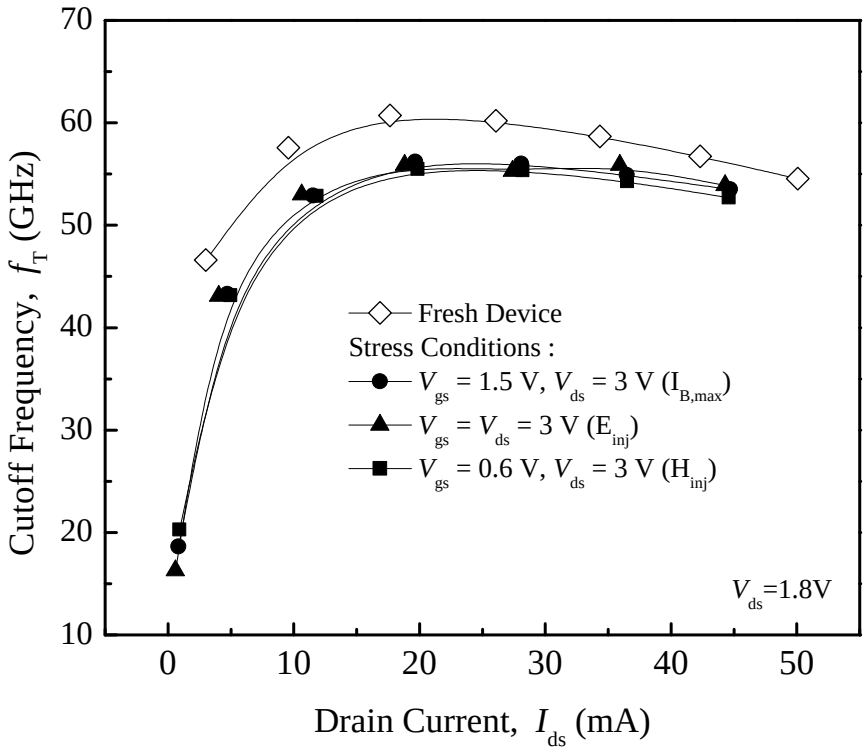


Figure 6.6: Cutoff frequency f_T before and after different hot carrier stress as a function of drain current I_{ds}.

6.6 *n*-MOSFET Noise Performance (GHz) Degradation under Different Hot Carrier Stresses

The effects of HC stress on minimum noise figure NF_{min} and equivalent noise resistance R_n at f = 2 GHz as a function of drain current I_{ds} are shown in Figure 6.7. It is observed that device noise degraded dramatically if the device was subjected to $I_{B,max}$ stress or hot hole injection (H_{inj}). However, the noise degradation was insignificant if it was subjected to hot electron injection (E_{inj}). Take I_{ds} = 25 *m*A as an example, NF_{min} increased ~5% when device was under electron injection (E_{inj}), whereas more than 25% noise increase was observed if *n*-MOSFET underwent $I_{B,max}$ stress or hot hole injection (H_{inj}). Since noise degradation behaviors are highly

dependent on the stress conditions, it is strongly suggested that high frequency noise of *n*-MOSFETs could be degraded via different physical mechanisms under three different stress modes.

Based on high frequency noise modeling of MOSETS, if we consider the channel noise and induced gate noise as the major noise sources, the noise parameters NF_{min} and R_n of the MOSFET can be obtained as [41]

$$NF_{min} \approx 1 + \frac{R_g S_{i_g}}{2kT} + [(\frac{f}{f_{t0}})^2 + \frac{1}{R_g r_T g_m^2}]\frac{R_g S_{i_d}}{2kT} + 2R_n G_{opt} \tag{6.2}$$

$$R_n \approx R_g + R_g^2 \frac{S_{i_g}}{4kT} + \frac{1}{g_m^2} \cdot \frac{S_{i_d}}{4kT} \tag{6.3}$$

where S_{id} and S_{ig} are channel noise and induced gate noise, respectively. Considering R_g~3.7 Ω (extracted based small signal S-parameters) and g_m~40 mS under biasing condition (V_{ds} = 1.8V) used for the high frequency noise measurement, we would expect a much larger contribution from the channel noise (the 3rd term in Equation (6.3)) as compared to the induced gate noise (the 2nd term in Equation (6.3)) due to ~45 times larger of $(1/g_m)^2$ compared to R_g^2. This is particularly true for the device in low frequency region where the gate induced noise is small (f = 2 GHz, $f / f_T < 10$). As a result, R_n may serve as a direct indicator to the variation of channel noise, since R_g is hardly affected by the HC stress. In Figure 6.7, NF_{min} and R_n are plotted against I_{ds} instead of V_{gs} to exclude the possible impact of charge density variation in the inversion layer due to different HC stresses. Higher NF_{min} and R_n might be explained by Equation (6.3) as device g_m decreases after hot carrier stress. However, the g_m reduction is only ~3% such that it is impossible to have such large impact in noise parameters NF_{min} and R_n. Moreover, the g_m reduction cannot explain why device with $I_{B,max}$ stress or hot hole injection (H_{inj}) has much larger increase in NF_{min} and R_n than

hot electron injection (E_{inj}). Because when device moves into saturation region saturation, g_m reduction is nearly the same among three post-stress devices (Figure 6.3). Therefore, it is believed that channel noise S_{id} rather than transconductance g_m plays a dominant role in different noise performance degradation under three hot carrier stress modes.

Based on channel length modulation (CLM) effect, the channel noise of deep submicron MOSFETs could be expressed as [27]

$$S_{i_d} = \frac{4kT\mu_{eff}}{L_{elec}^2} Q_{inv} \propto I_{ds} \tag{6.4}$$

where μ_{eff} is effective carrier mobility, L_{elec} is the electrical gate length, and Q_{inv} is the inversion charge in the channel. Channel noise before and after hot carrier stress is compared as a function of I_{ds} in Figure 6.8. Similar to minimum noise figure NF_{min} and noise resistance R_n, the channel noise (f = 2 GHz) exhibits large degradation under $I_{B,max}$ stress, followed by hot hole injection (H_{inj}) and then hot electron injection (E_{inj}). The observation of different post-stress channel noise behaviors tends to suggest that additional channel noise is generated via different physical mechanism. The additional channel noise ΔS_{id}, which is the channel noise difference before and after different hot carrier stresses, is plotted in Figure 6.9. We can clearly see that with $I_{B,max}$ stress, channel noise degradation is most significant, which is nearly 5 times larger than that with hot electron injection (E_{inj}).

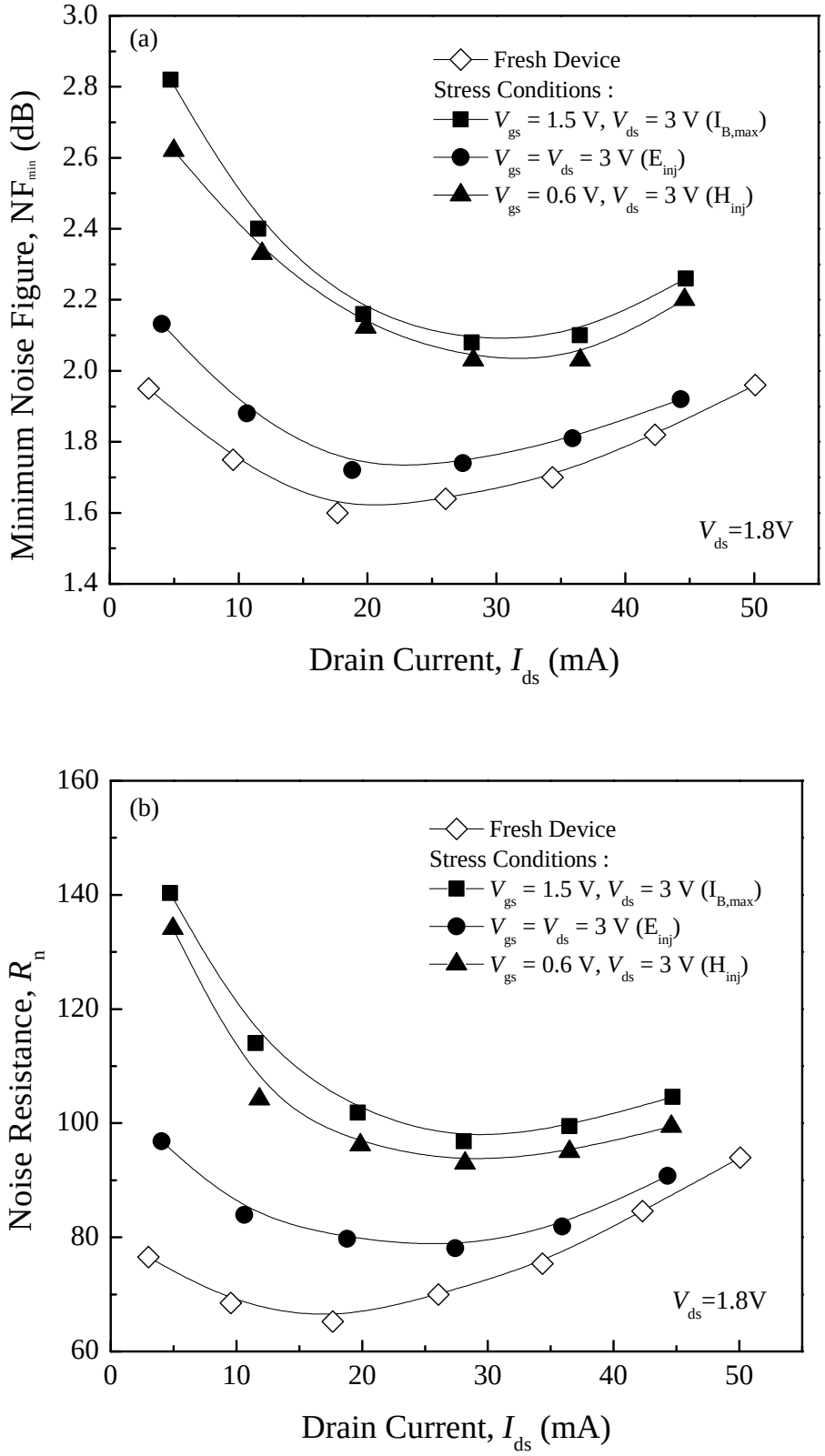


Figure 6.7: (a) NF_{min} and (b) R_n before and after different hot carrier stress as a function of drain current I_{ds}.

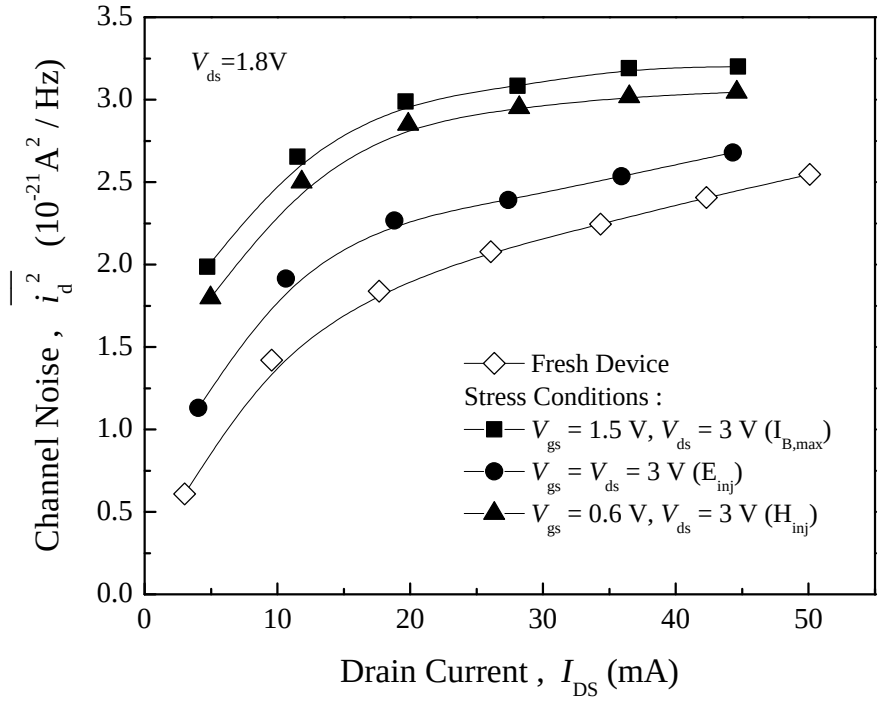


Figure 6.8: Channel noise $\overline{i_d^2}$ before and after different hot carrier stress as a function of drain current I_{ds}.

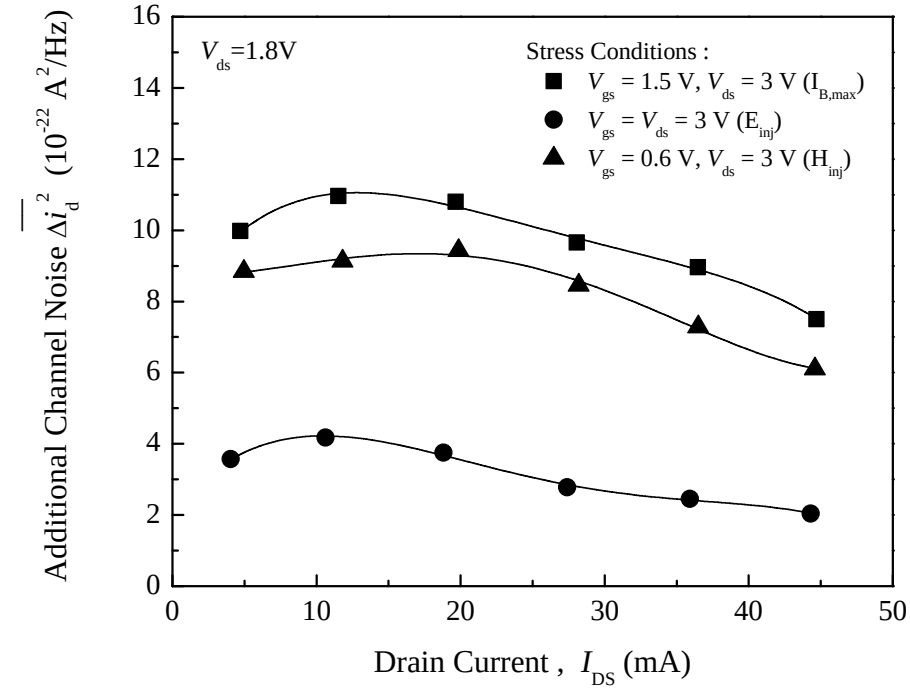


Figure 6.9: Additional channel noise $\Delta\overline{i_d^2}$ with different hot carrier stress as a function of drain current I_{ds}.

In our experiment, although I_{ds} degradation were purposely made to be similar, the interface state density, especially those at shallow energy level just below conduction band could be quite different. It is known that $I_{B,max}$ stress owes the highest interface states generation efficiency, and a number of interface states are also expected to be generated with long time hot hole injection (H_{inj}). However for hot electron injection (E_{inj}), electron trapping in the gate oxide is known as the dominant degradation mechanism, the interface states generation is relatively lower [80-81, 85, 87]. Channel noise after hot carrier stressing therefore reveals a strong dependence on the interface state density, largest noise increase was seen under maximum substrate current stress, followed by hot hole injection, whereas the noise increase is minimal under hot electron injection.

In Chapter 5, it was found that carrier fluctuations could arise from random emission and capture of electrons at the shallow interface states/traps with characteristic noise frequency in GHz regime. An activation energy E_a of ~0.033 eV for the excess channel noise was determined by temperature dependent noise measurement. This additional noise component could not be thermal type, but is considered as the major source of channel noise increment after hot carrier stress. Here, we would like to discuss further on the different noise generation mechanisms associated with interface states/traps and oxide traps. As shown in Figure 6.10 and Figure 6.11, the carrier transition between the conduction band state and the shallow interface states/trap does not produce a location change (in the *x*-direction), therefore the transition time is significantly reduced, resulting in a large fluctuation (noise) frequency. On the other hand, oxide traps are lying so deeply in the gate oxide such that their fluctuations are too slow to be detected as RF noise. Instead, $1/f$ noise is induced in this case, which has been widely studied in the past few years. It is

proposed that the high frequency noise degradation is strongly correlated to the density of shallow Si/SiO_2 interface states generated during hot carrier stresses, while low frequency noise is more correlated to the traps in the oxide. The location of the defect generated during stress is the key to distinguish them on the device noise properties. Therefore, in view of high frequency noise performance of *n*-MOSFETs, hot electron injection (E_{inj}) is a less concern than $I_{B,max}$ stress and hot hole injection (H_{inj}). In addition, it should be noted that $1/f$ noise also increases under $I_{B,max}$ stress and hot electron injection (E_{inj}), this is because charged interface traps could give rise to Coulomb scattering to carriers in the channel due to their closeness to the conduction channel, and affect the mobility of the carriers [69].

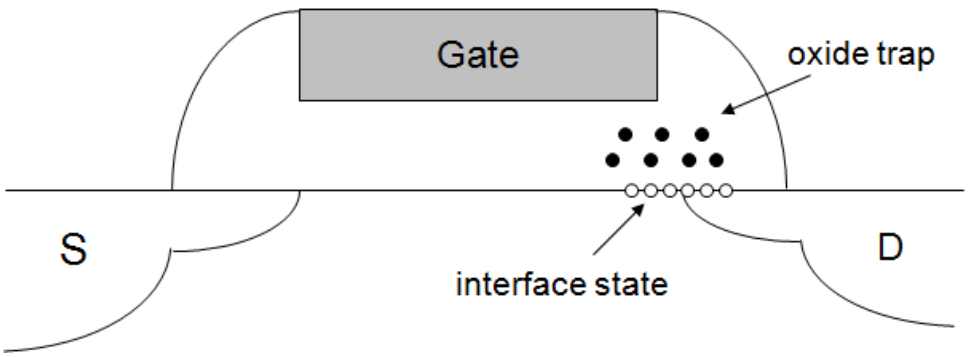


Figure 6.10: Schematic diagram of interface states (○) and oxide traps (●) spatial location in the *n*-MOSFET generated during hot carrier stresses.

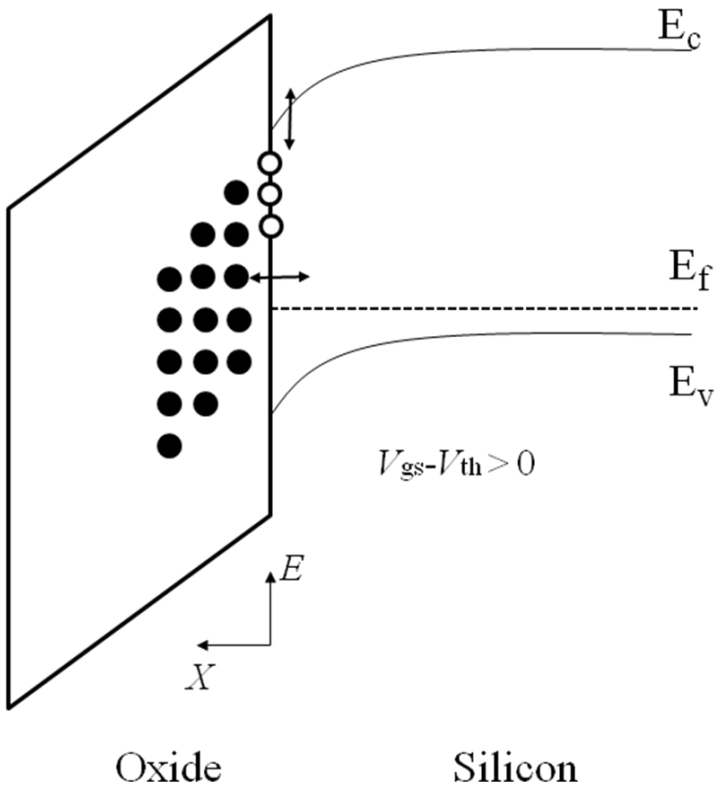


Figure 6.11: Schematic diagram of interface states (○) and oxide traps (●) detectable as RF or 1/*f* noise in (*x*, *E*) space. (*E* is the energy level of interface states or oxide traps)

6.7 RF CMOS Hot Carrier Reliability

Through Chapter 4 to 6, we have investigated different aspects of high frequency noise in *n*-MOSFETs subjected to hot carrier stress. In this section, we would like to discuss the correlation among the DC, RF and noise performance degradation due to different hot carrier stresses. Traditionally, device hot carrier lifetime estimation is based on DC parameters degradation, either by threshold voltage V_{th}, drain current I_{ds}, or transconductance g_m. Recent studies on RF performance after hot carrier stress have demonstrated that the f_T (RF parameter) HCI

lifetime could be well predicted using traditional HCI lifetime model (eg. Substrate Current Lifetime Model) [59, 62].

In Table 6.2, device DC, RF and high frequency noise parameters degradation after different hot carrier stresses are listed, 10% decrease in I_{ds} is chosen as a reference level. It is observed that the degradation of RF parameter f_T is proportional to drain current degradation $\left(\Delta I_{ds} / I_{ds}\right)$ with the same ratio R_1 at approximately 0.6 regardless of hot carrier stress conditions [59]. On the other hand, channel noise degradation $\left(\Delta \overline{i_d^2} / \overline{i_d^2}\right)$ is greater than I_{ds} degradation, and the ratio (R_2, R_3, R_4) varies for different hot carrier stresses. $I_{B,max}$ stress results in greatest channel noise degradation, followed by hot hole injection (H_{inj}), and then hot electron injection (E_{inj}).

Table 6.2: DC, RF and noise parameters (GHz) comparison under different hot carrier stresses.

Hot Carrier Stress	Failure Mechanism	DC	RF	Noise (GHz)
		$\left(\Delta I_{ds} / I_{ds}\right)$	$\left(\Delta f_T / f_T\right)$ ($R_1 \approx 0.6$) [59]	$\left(\Delta \overline{i_d^2} / \overline{i_d^2}\right)$ ($R_2 > R_4 > R_3 > 1$)
$I_{B,max}$ ($V_{gs} \approx V_{ds}/2$)	Interface States	10%	10%×R_1	10%* R_2
E_{inj} ($V_{gs} \approx V_{ds}$)	Oxide Traps	10%	10%× R_1	10%* R_3
H_{inj} ($V_{gs} \leq V_{ds}/4$)	Interface States + Oxide Traps	10%	10%× R_1	10%* R_4

Based on the RF measurement data of the *n*-MOSFETs under different hot carrier stresses, it is acceptable to predict device RF HCI performance by simply charactering the DC HCI performance. This is because the origin of the changes of f_T (or f_{max}) are the changes of g_m (DC parameter) and are independent of hot carrier injection modes [86]. However, it is not accurate enough to implement the same method for device high frequency noise performance prediction. The mechanisms of channel noise degradation under different hot carrier stress are physically different. The channel noise degradation is mainly due to additional noise component arises from carrier capture and emission mechanisms associated with the HC induced shallow Si/SiO_2 interface states, it is not directly correlated to DC parameters degradation but the density and location of the defect generated during stress. The study has demonstrated that higher density of shallow Si/SiO_2 interface states generated during the hot carrier stress (such as $I_{B,max}$ stressing) leads to worse high frequency noise performance on MOSFETs even if DC or RF parameter degradation are similar. As a result, measurement is still necessary for assess noise performance after hot carrier stress to determining the noise HCI lifetime of RF transistors.

6.8 Summary

In this Chapter, we found that the degradation of high frequency noise in deep submicron *n*-MOSFETs under different hot carrier stress conditions is different. With high V_{gs} stress (E_{inj}), where oxide traps are the dominant mechanism of device degradation, the increase in device RF noise was much smaller than that under maximum substrate current ($I_{B,max}$) stress and high V_{gs} stress (H_{inj}). Our results strongly suggest that high frequency noise degradation is dependent on hot carrier stress modes and directly related to stress induced interface states. This is because

additional channel noise is generated due to carrier capture and emission between the interface states and the channel, while oxide traps can hardly change the channel noise at high frequencies. The study on the impact of stress conditions in high frequency noise provides some new insight and better understanding on the nature of channel noise in short channel MOSFETs. Finally we discussed the correlation of device DC, RF and noise performance degradation under different hot carrier stresses. It is suggested that traditional HCI lifetime model can be used to predict the RF HCI lifetime, whereas it is not accurate for noise HCI prediction, because noise degradation strongly depends on the defect type generated during hot carrier stress (interface states or oxide traps).

Chapter 7

Effects of Forward Body Bias on CMOS High Frequency Noise

7.1 Introduction

The forward body bias (FBB) scheme has been proposed as an effective method to improve the device performance in MOSFETs [88-93]. Forward biasing the substrate-to-source of a MOSFET reduces the threshold voltage (V_{th}), increases the unit current gain frequency (f_T) and circuit operating speed. Benefits of FBB on device and circuits have been extensively studied in the literatures. Hokazono *et al.* [88] reported that, by reducing the electric field in the drain region through FBB, MOSFET hot carrier lifetime could be significantly improved. FBB has also been considered as a promising solution to extend bulk-Si CMOS scaling limit, since short channel behavior of MOSFET could be greatly improved under FBB [90, 93]. Moreover, Terauch [94] investigated the impact of forward substrate bias on the threshold voltage fluctuation in MOSFETs. He demonstrated that the threshold voltage fluctuation could be suppressed up to 20% in sub-100-nm devices by applying a forward substrate voltage of 0.3 V.

Considering the high frequency noise performance, accurate noise modeling is a prerequisite for low noise RF circuits design. Significant efforts have been made to understand the physical origin of RF noise in MOSFETs [41, 47, 50, 95]. However,

most of these studies were carried out under zero body bias (ZBB). There is lack of studies on the effect of the body bias on the high frequency noise performance.

In this chapter, the effects of forward body bias on high frequency noise in 0.18-μm CMOS transistors were investigated. Although low frequency noise (1/*f* noise) in MOSFET could be improved when applying a forward body bias [96], significant increase in high frequency noise was observed in the devices under forward substrate bias. This could be due to superposition of the increased channel noise and substrate resistance noise under forward body bias. Our results indicate that, for analog circuit applications, forward body bias is not favorable if high frequency noise is a concern.

7.2 Experiments

In this experiment, we used a four-terminal N and PMOS fabricated by standard 0.18-μm CMOS process flow (as shown in Figure 7.1). The devices under test had a multiple gate layout with four gate fingers. The devices are based on twin-well CMOS technology. Contacts to *p*-Si or *n*-Si well allow for adjustment of the body bias to vary the electric field between the channel and substrate. During the measurements, the body-to-source voltage V_{bs} is varied from 0 V to 0.6 V and 0 V to -0.45 V for NMOS and PMOS, respectively. Substrate bias of -0.60 V is excluded for PMOS because source-substrate junction starts to turn on at this voltage.

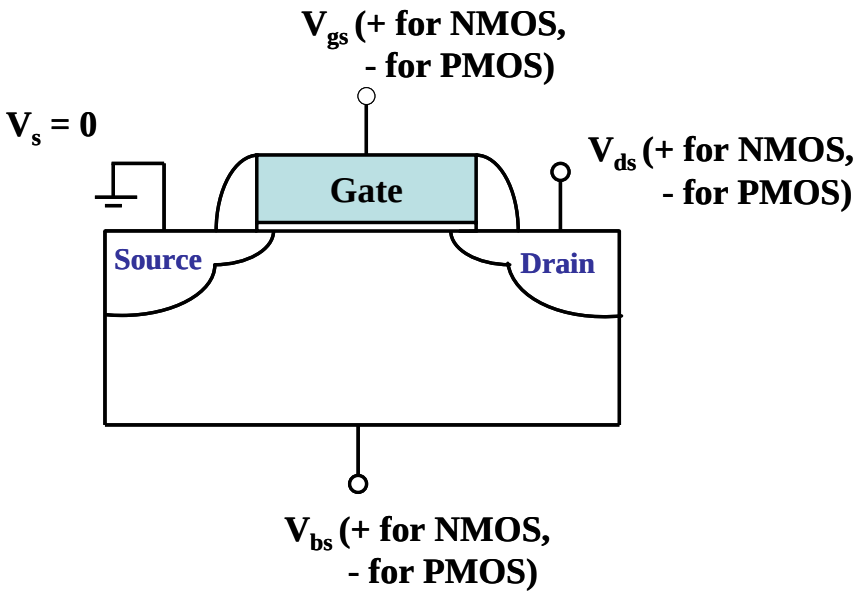


Figure 7.1: Schematic representation of a NMOS or PMOS under forward body bias used in this study.

7.3 Effects of Forward Body Bias on DC Performance

By using bulk terminal as an active electrode, body biasing strategy was introduced in the design of dynamic threshold voltage MOSFET (DTMOS). The substrate bias was used to adjust threshold voltage [89]. In active mode, by forward biasing the source-body junction, transverse electrical field in the channel can be reduced, which improves the carrier mobility and the transistor operation. On the other hand, in stand-by mode, reverse body bias is applied to reduce the off-state leakage current [90]. In this study, we will focus our investigation on the effects of forward body bias on DC and high frequency noise performance of N- and P-MOSFETs.

Figure 7.2 shows the I_{ds}-V_{gs} characteristics at room temperature as a function of substrate bias at $|V_{ds}|$ =1.8 V. Both N- and P-MOSFET transfer curves shift to the left under FBB. As expected, higher current drive is observed with increasing $|V_{BS}|$

because of higher channel carrier mobility and larger inversion charge. On the other hand, forward body bias leads to an enhancement in the off-state current I_{off} (at V_{gs} = 0). Furthermore, the subthreshold swings become larger due to the reduction in the gate depletion layer width when forward body bias is applied [90].

Figure 7.3 illustrates the variations of V_{th} with forward $|V_{bs}|$. The reduction on threshold voltage is often regarded as one of the most impressive advantages of FBB. With a forward biased substrate-source junction, the potential barrier at the Si-SiO_2 interface is lowered thus a smaller threshold voltage is expected. Generally, the threshold voltage can be expressed as [97]

$$V_{th}(V_{bs}) = V_{th,0} + \gamma\left(\sqrt{\phi_b - V_{bs}} - \sqrt{\phi_b}\right) \tag{7.1}$$

where $V_{th,0}$ is the threshold voltage evaluated at V_{bs} = 0, γ is the body effect parameter, and ϕ_b is the total surface bending. As can be seen in the figure, both linear ($|V_{ds}|$ = 0.1V) and saturation V_{th} ($|V_{ds}|$ = 1.8V) were severely reduced when $|V_{bs}|$ moving to the forward direction. When forward body bias increased from 0 to 0.45 V, linear V_{th} decreased from 529 to 396 mV for NMOS and from 490 to 374 mV for PMOS. Both devices show about 25% reduction of V_{th}. On the other hand, degradation of saturation V_{th} is larger in NMOS than that in PMOS. The decrease in V_{th} are 17.5 % (586 to 483 mV) for NMOS and 11.3 % (658 to 584 mV) for PMOS when 0.45 V $|V_{bs}|$ is applied. The body effect factor γ, which is defined as the ratio of change in threshold voltage (ΔV_{th}) over change in body voltage (ΔV_{bs}), is around 0.23 and 0.16 for N and PMOS, respectively. This indicates that NMOS is more sensitive to body bias. The detail information on the modeling of threshold voltage with forward body bias could be found in [97].

In order to evaluate the effect of FBB on the impact ionization process, substrate currents I_{sub} as a function of $|V_{gs} - V_{th}|$ at V_{ds} = ± 1.8 V were plotted at

different body bias (see Figure 7.4). For the NMOS devices, higher impact ionization current I_{sub} is observed as V_{bs} increases. At $|V_{gs} - V_{th}| \approx 0.4$ V, peak I_{sub} increased about 15 %. However, the impact ionization rate, defined by I_{sub}/I_{ds}, only increases slightly and becomes nearly identical at high V_{gs}. For the PMOS transistors, I_{sub} increases slightly at low $|V_{gs} - V_{th}|$, and decreases at high $|V_{gs} - V_{th}|$ under FBB. The impact ionization rate I_{sub}/I_{ds} is insensitive to the substrate bias. It is believed that the average energy of the carriers under FBB is lowered, since the maximum electric field along the channel is reduced by forward substrate bias.

Finally, variations of transconductance (g_m) as a function of substrate bias were assessed and shown in Figure 7.5. Transconductance for both N- and P-MOSFET devices show a weak dependence on V_{bs}. The trivial impact of body bias on g_m can be explained by the channel quasi-Fermi potential gradient effect in scaled devices. In long-channel MOSFETs, g_m is expected to increase with forward body bias; but in short-channel MOSFETs, g_m improvement through the mobility enhancement under forward body bias is compensated by the decrease of channel quasi-Fermi potential gradient [92, 98]. Moreover, the influences of body bias on output conductance g_{d0}, which are illustrated in the insets of Figure 7.5, are also negligible. Therefore, the possible impact of g_m and g_{d0} on the device noise performance subjected to substrate bias could be ignored as both of them are insensitive to the substrate bias.

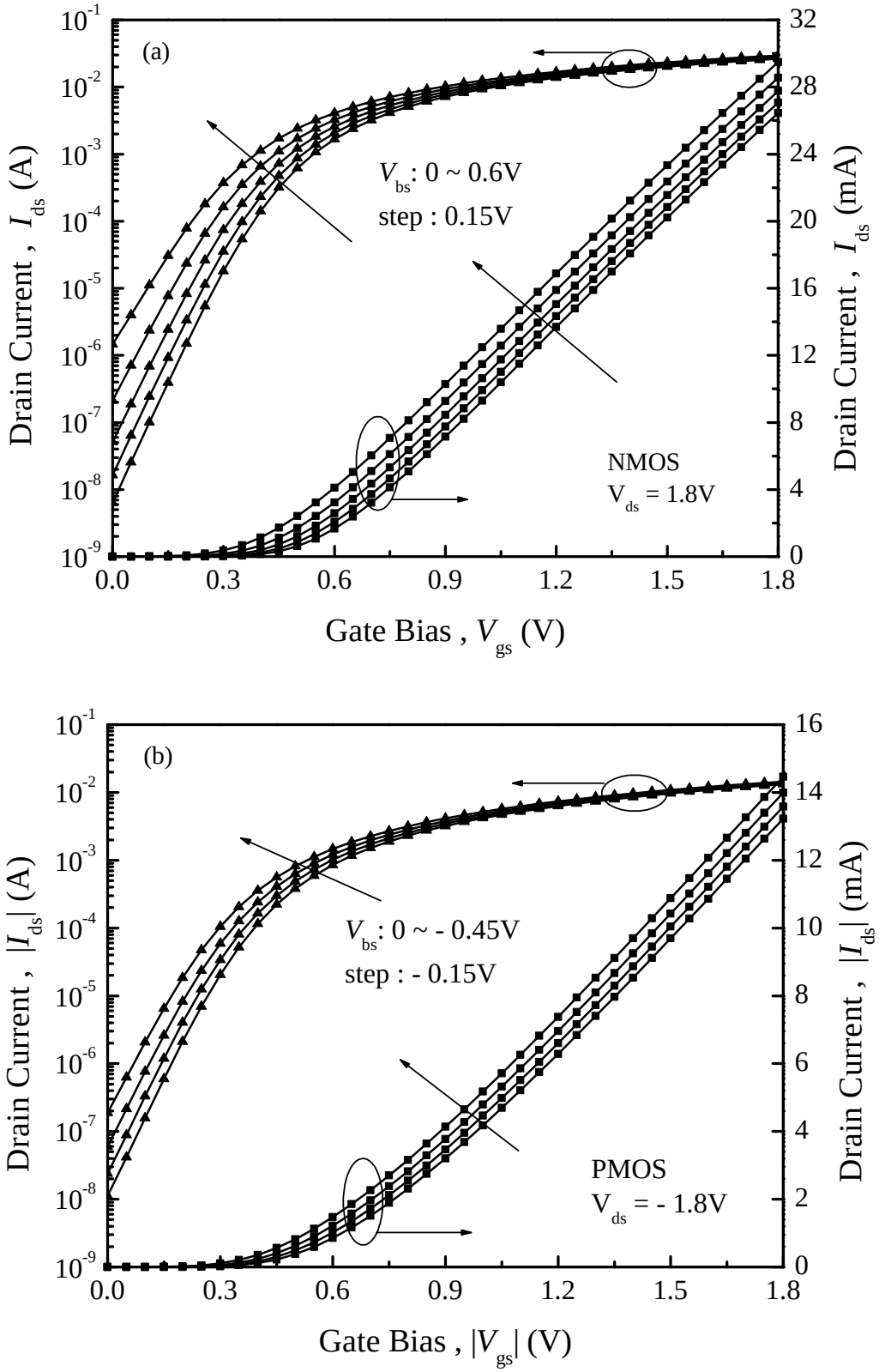


Figure 7.2: Drain current I_{ds} against gate bias V_{gs} as a function of body bias V_{bs}. (a) NMOS ; (b) PMOS.

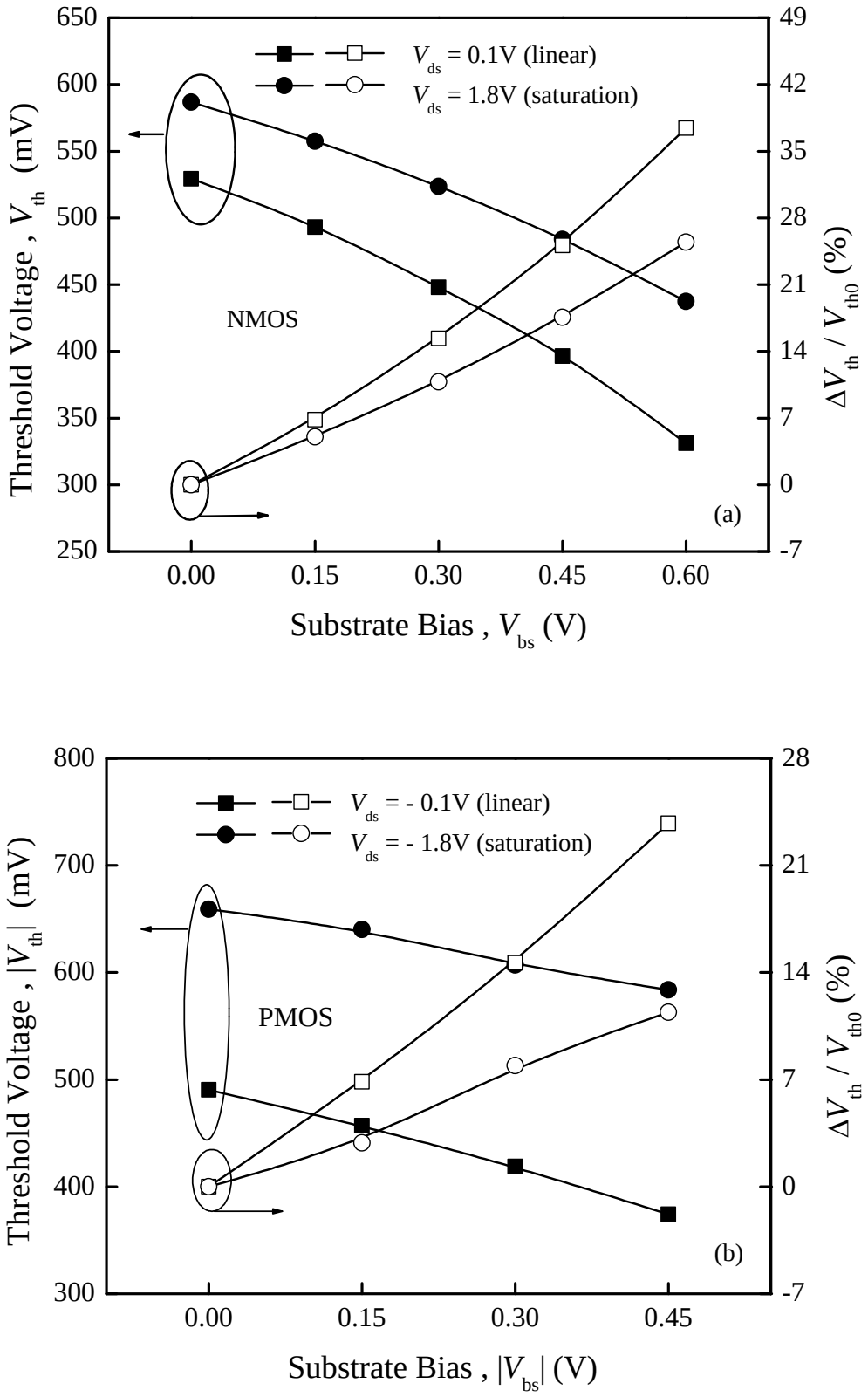


Figure 7.3: Threshold voltage V_{th} and variations of V_{th} as a function of body bias V_{bs}. (a) NMOS; (b) PMOS.

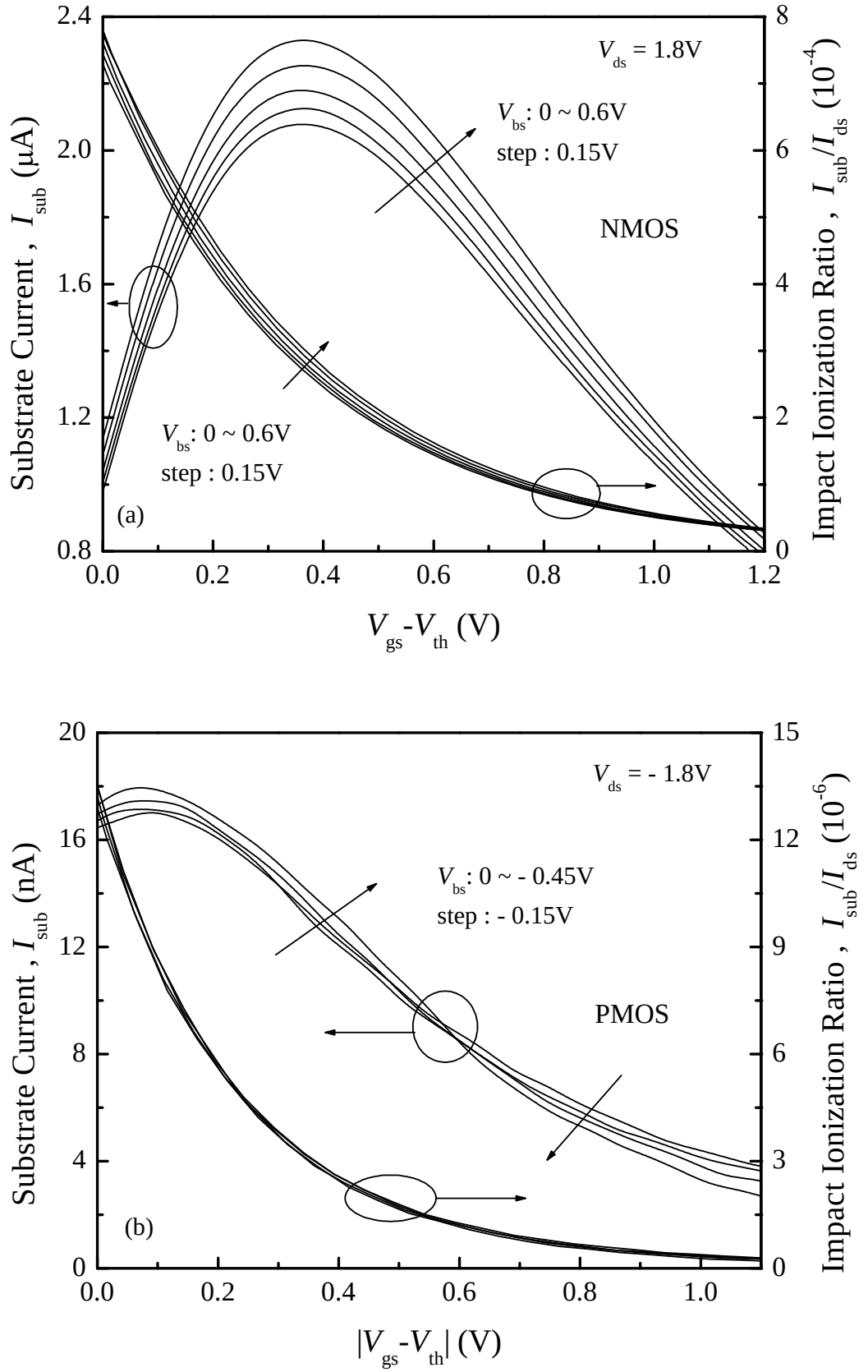


Figure 7.4: Substrate current against V_{gs}-V_{th} as a function of body bias V_{bs}. (a) NMOS; (b) PMOS.

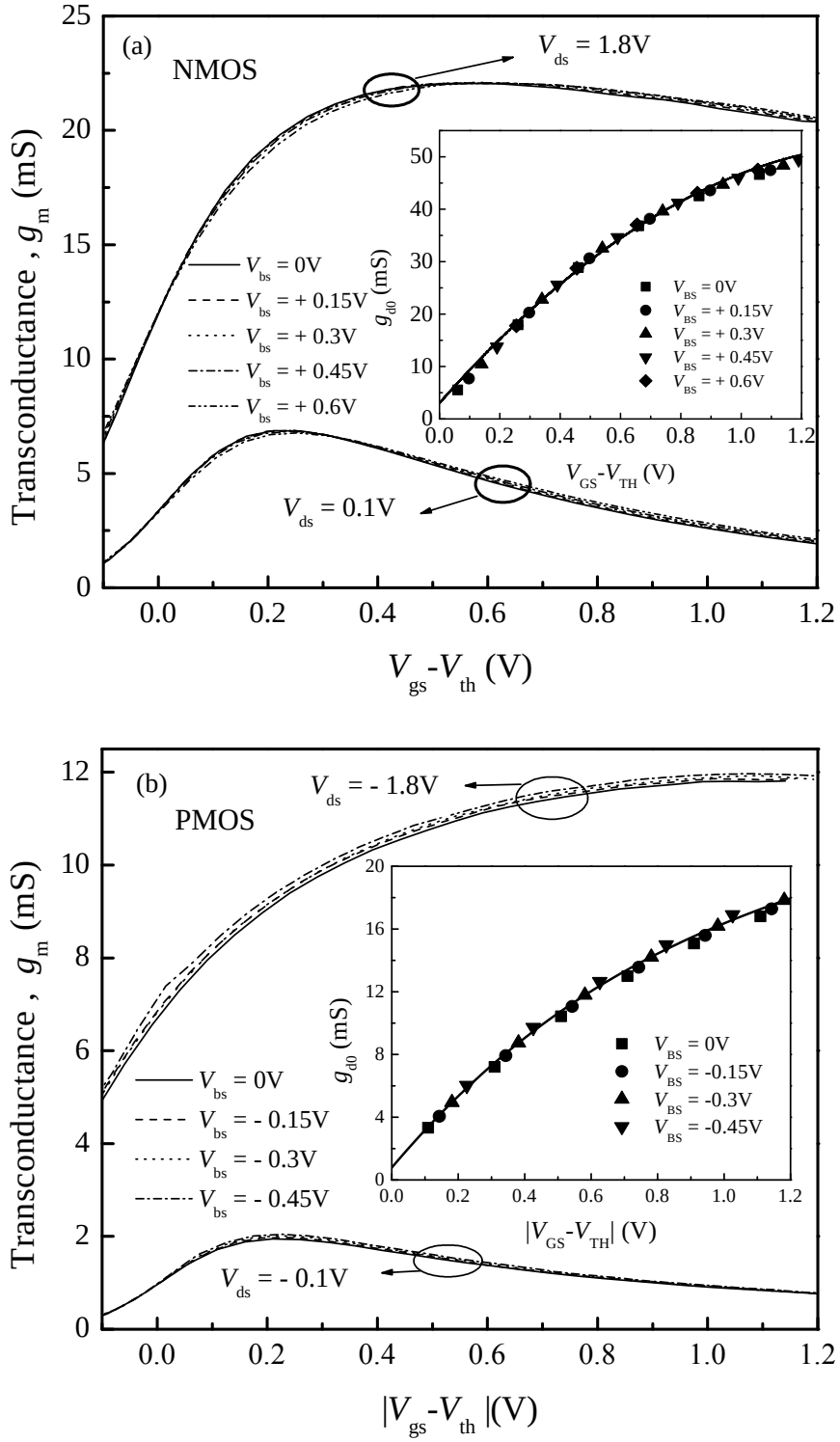


Figure 7.5: Saturation and linear transconductance (g_m) as a function of V_{gs}-V_{th} with different body bias. Inset: Output conductance at zero drain bias (g_{d0}) as a function of V_{gs}-V_{th} with different body bias. (a) NMOS; (b) PMOS.

7.4 Effects of Forward Body Bias on High Frequency Noise Performance

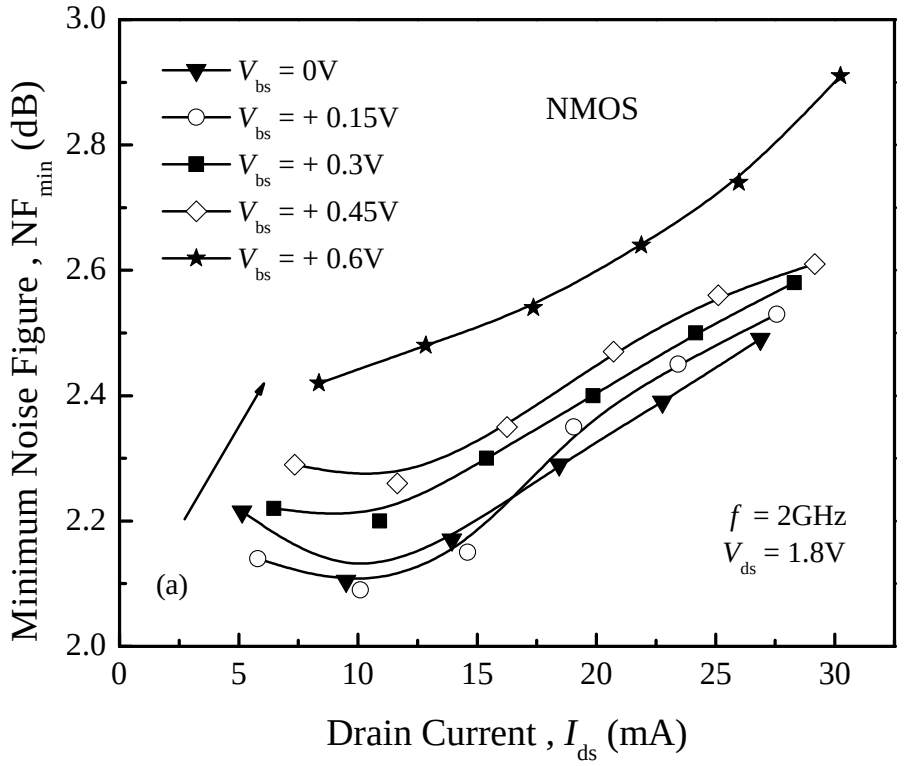
The impact of forward body bias on the MOSFET minimum noise figure NF_{min} and noise resistance R_n at 2 GHz are shown in Figure 7.6 and Figure 7.7. Both parameters are plotted against drain current $|I_{ds}|$ in order to exclude the body effect. Although the increase of NF_{min} is small at low forward substrate bias, it becomes significant when $|V_{bs}|$ raises to 0.45 V or 0.6 V. The dependence of R_n on the body bias also shows an increase trend as body bias increases. For example, R_n increased from 140 to 158 Ω (NMOS, I_{ds} = 15 mA) and 145 to 155 Ω (PMOS, $|I_{ds}|$ = 8mA) as forward body bias varied from 0 to 0.45V. Thus, in moderate inversion mode under the same $|V_{bs}|$, R_n increased 12.8 % in NMOS compared to 6.8 % in PMOS. The degradation of noise performance is severer in NMOS than PMOS. It is worth noting that the deterioration of high frequency noise performance under FBB would limit its application in low-noise circuit design although forward body bias is preferred in optimizing device DC performance.

For the high frequency noise characterization of MOSFET transistors, the noise Figure (NF) is not only affected by NF_{min} and R_n but also by the source impendence at the input port. Generally, the noise performance of any noisy two-port network can be represented by

$$NF = NF_{min} + \frac{4(R_n / Z_o)\cdot\left|\Gamma_s - \Gamma_{opt}\right|^2}{\left(1-\left|\Gamma_s\right|^2\right)\cdot\left|1+\Gamma_{opt}\right|^2} \tag{7.2}$$

where NF_{min} is the minimum noise figure, R_n is the equivalent noise resistance, Z_0 is the characteristic impedance, Γ_s is the source reflection coefficient, and Γ_{opt} is the optimum source reflection coefficient that results in NF_{min}. In a noisy two-port

network, NF_{min}, R_n, $|\Gamma_{opt}|$ and $\angle\Gamma_{opt}$ are often referred as four noise parameters. The dependence of body bias on MOSFET optimum source reflection coefficient Γ_{opt} is shown in Figure 7.8. Unlike NF_{min} and R_n, both the magnitude and phase of Γ_{opt} are insensitive to the body bias. This weak dependence of body bias on Γ_{opt} indicates that the associated noise matching networks in the device equivalent-circuit is scarcely changed when device body is forward biased.



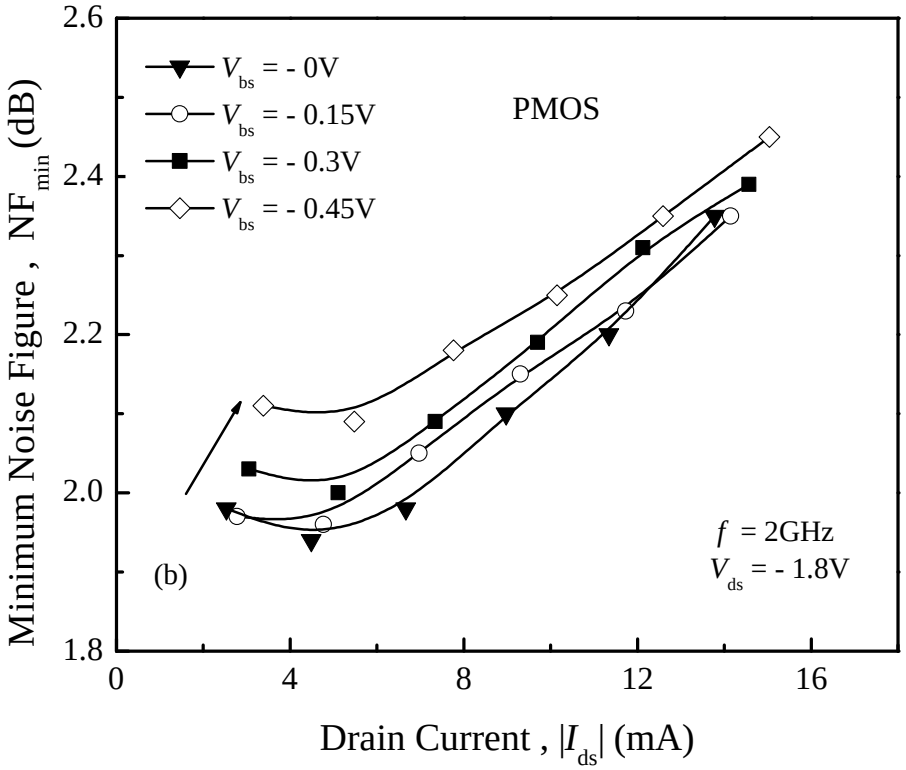


Figure 7.6: Minimum noise figure NF_{min} against drain current I_{ds} as a function of body bias V_{bs}. (a) NMOS; (b) PMOS.

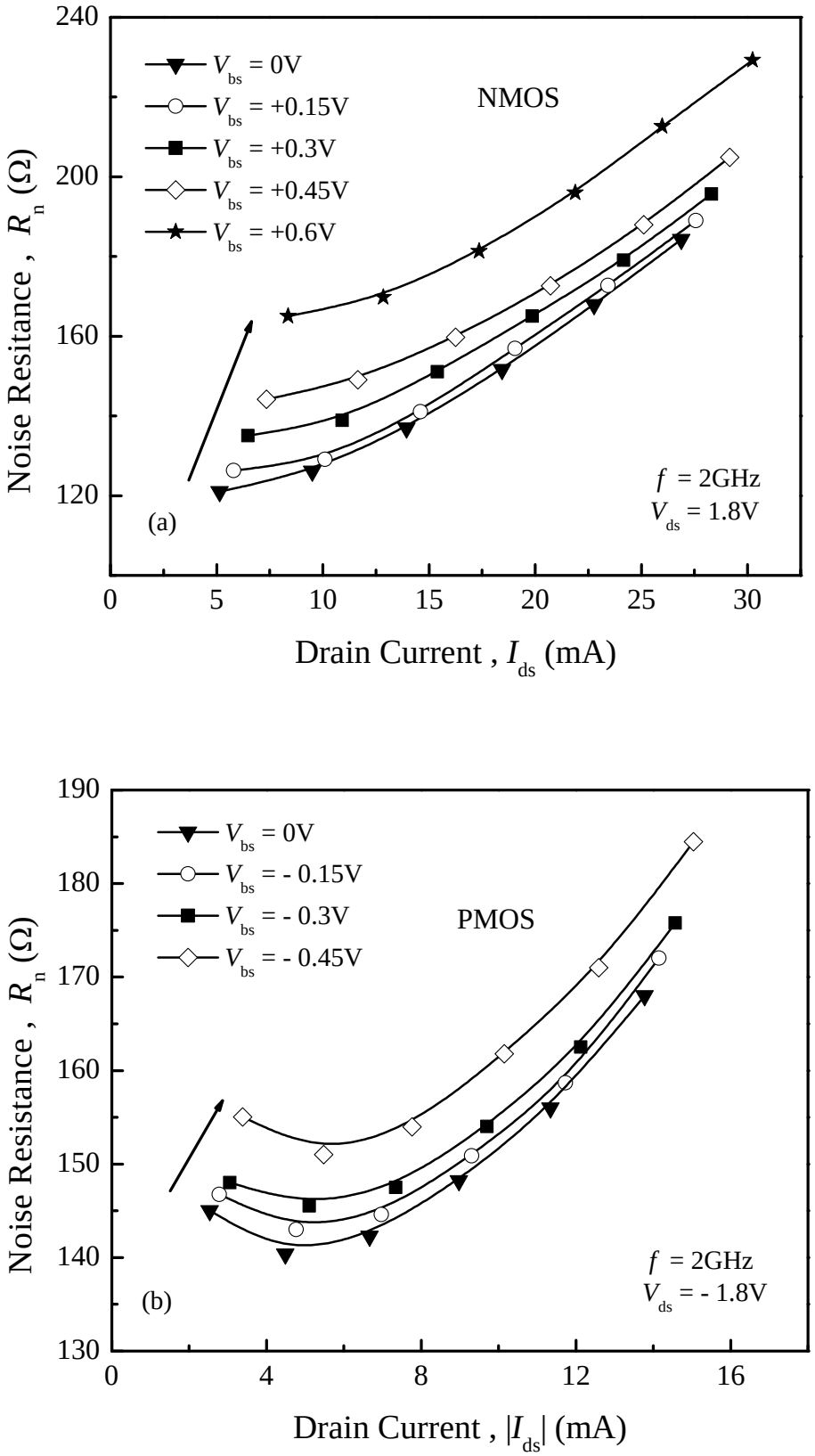
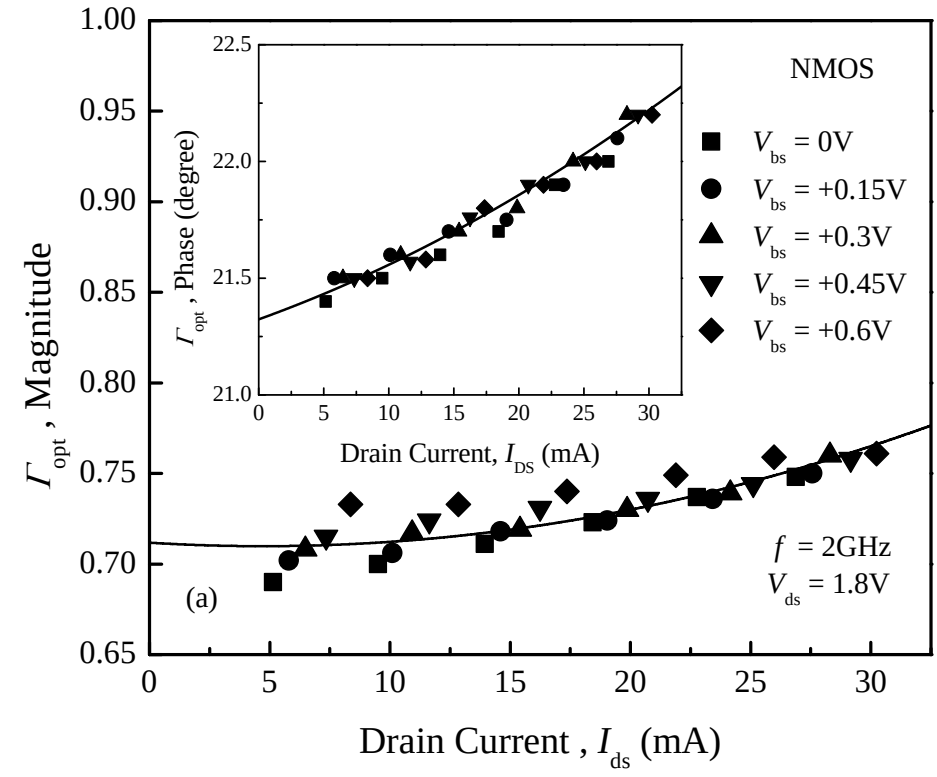


Figure 7.7: Equivalent noise resistance R_n against drain current I_{ds} as a function of body bias V_{bs}. (a) NMOS; (b) PMOS.



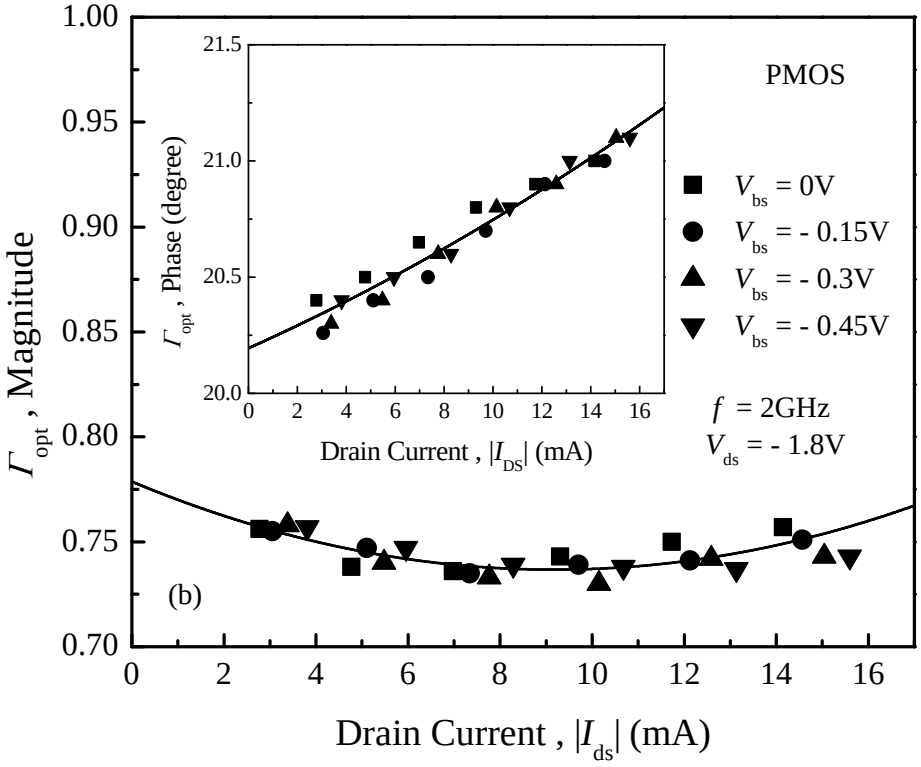


Figure 7.8: Magnitude and phase of reflection coefficient Γ_{opt} against drain current I_{ds} as a function of body bias V_{bs}. (a) NMOS; (b) PMOS.

7.5 Further Analysis on Different Noise Sources

As discussed in the literature review, there are a number of noise sources might be important to the overall noise performance, including channel thermal noise ($\overline{i_d^2}$), induced gate noise ($\overline{i_g^2}$), gate shot noise ($\overline{i_{g\_shot}^2}$), gate resistance noise ($\overline{i_G^2}$) and substrate resistance noise ($\overline{i_b^2}$). The increase in NF_{min} and R_n under forward body bias could be caused by one noise source or a combination of several noise sources. Channel thermal noise, which has been considered as a dominant noise source in MOSFET was extensively investigated during the past few years [21-22, 27, 29, 31, 51, 99-100]. At high frequencies, the channel thermal noise is coupled to the gate through oxide capacitance and causes an induced gate noise. In this study, an intermediate frequency is chosen (f = 2GHz, and $f / f_T < 0.1$), so that the influence of induced gate noise can be minimized. Gate shot noise normally is not considered unless gate oxide breakdown happens. The gate and substrate terminals contribute to the overall noise as well because thermal voltage fluctuations are produced across the gate and substrate resistance [47]. Because gate resistance is hardly affected by body bias, gate resistance noise can be treated as constant during the variation of body bias. However, the substrate resistance noise has a strong dependence on the body bias, and will be examined later.

Although substrate resistance noise is often regarded as a second-order noise, it was found that NF_{min} and R_n could be strongly affected by this noise source [50, 95]. So the substrate resistance noise should be carefully accounted when doing noise calculation and optimization. Normally it is given by [67]

$$\overline{i_b^2} = \frac{4k_B T R_{sub} g_{mb}^2 \Delta f}{1+(\omega R_{sub} C_{sub})^2} \tag{7.3}$$

where k_B is Boltzmann's constant, T is the absolute temperature, ω is the frequency,

g_{mb} is bulk transconductance, R_{sub} and C_{sub} are the substrate resistance and capacitance. As shown in Figure 7.9, body bias significantly influences the magnitude of the bulk transconductance. Twice increase in g_{mb} was observed in both devices when $|V_{bs}|$ is increased to 0.45V. The analytical expression of the equivalent noise resistance R_n could be estimated as [50]

$$R_n = \frac{\gamma}{\alpha g_m} + R_g + \frac{R_{sub}}{g_m^2} g_{mb}^2 \tag{7.4}$$

where R_g is the gate resistance, $\alpha = g_m / g_{do}$, γ is channel noise factor, which is about 2/3 for long-channel device and will be increased to more than unity as channel length reduced [27]. As shown in Figure 7.5, both g_m and g_{do} are insensitive to body bias, so does parameter α. Noise factor γ is generally determined by MOSFETs inherent design for a fixed drain current I_{ds}. So it can also be treated as body bias independent parameter. From Equations (7.3) and (7.4), a parabolic behavior of R_n on g_{mb} is expected provided that substrate resistance noise is dominant in the variation of R_n under FBB. In Figure 7.10, R_n is plotted against g_{mb} for NMOS and PMOS at various body biases. In NMOS, noise resistance R_n does not follow the parabolic dependence on g_{mb}, especially at high $|V_{bs}|$. On the other hand, in PMOS, the data matches well with the parabola described by Equation (7.4). This observation suggests that, in NMOS, noise increase could not be fully accounted by the substrate resistance noise; while in PMOS transistors, the noise increase under forward body bias could be mainly attributed to the increase in substrate resistance noise. Furthermore, based on the coefficients of the fitting curve (NMOS: $R_n = 130.8 + 0.6 \times 10^6 g_{mb}^2$ and PMOS: $R_n = 135.2 + 1.9 \times 10^6 g_{mb}^2$), the noise factor can be extracted using (6.4). Noise factor γ are found to be ~ 1.6 for NMOS and ~ 1.5 for PMOS, which are in agreement with previously reported values for 0.18-μm MOSFETs [20].

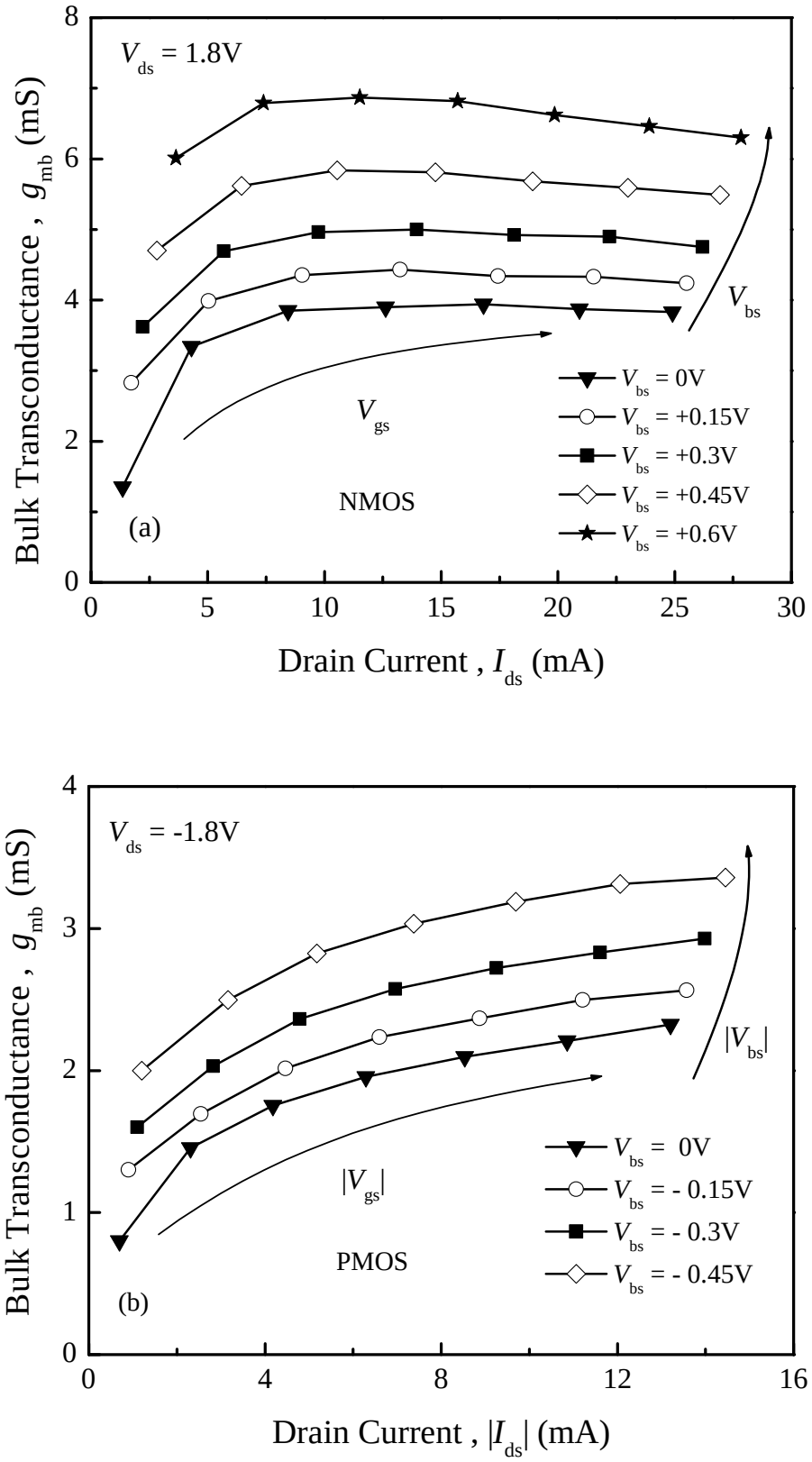


Figure 7.9: Bulk transconductance (g_{mb}) as a function of drain current I_{ds} for different V_{bs}. (a) NMOS; (b) PMOS.

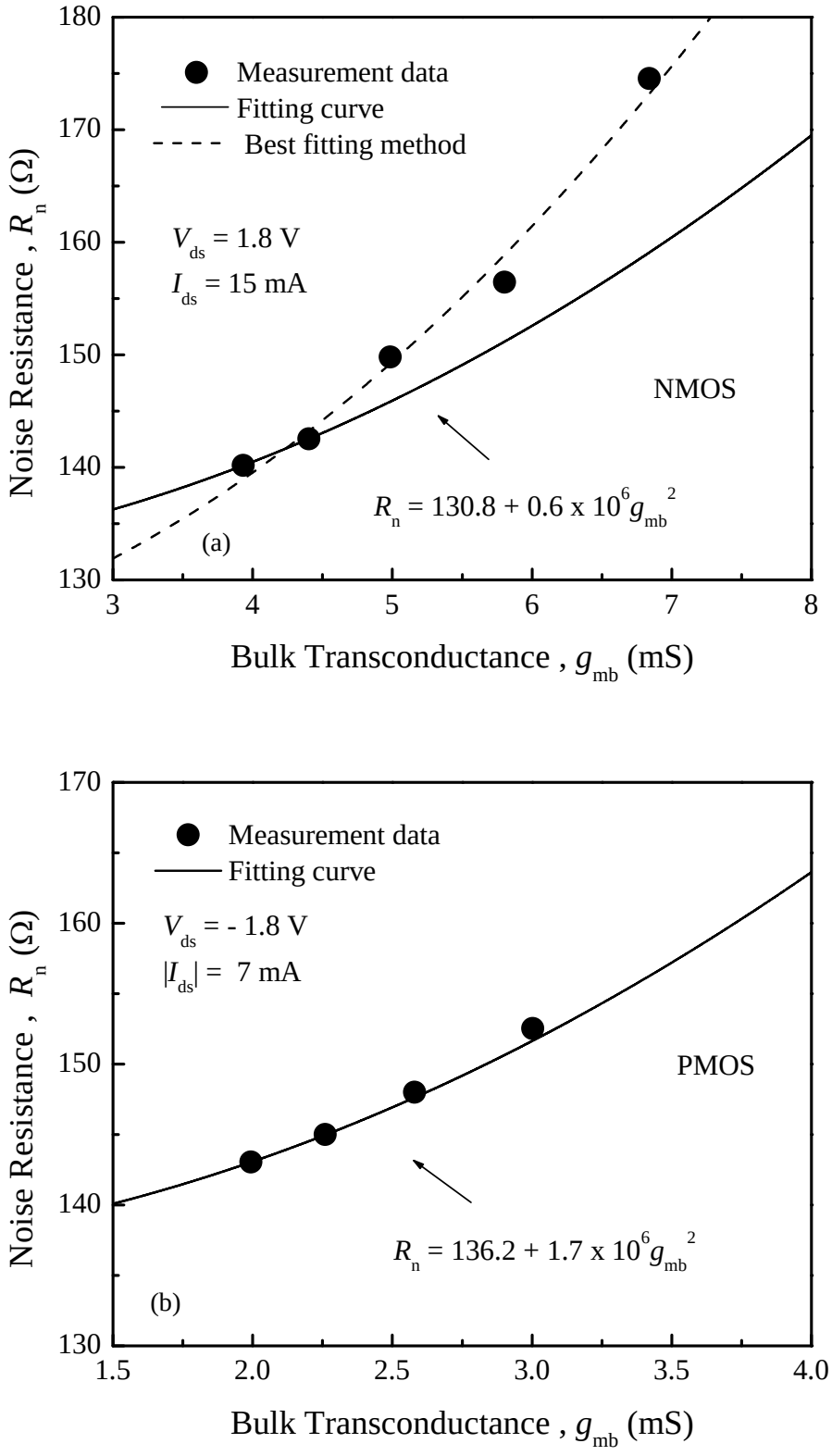


Figure 7.10: Noise resistance R_n versus g_{mb}. The values R_n and g_{mb} were extracted from Figure 7.7 and Figure 7.9. (a) NMOS at I_{ds} = 15 mA; (b) PMOS at $|I_{ds}|$= 7 mA.

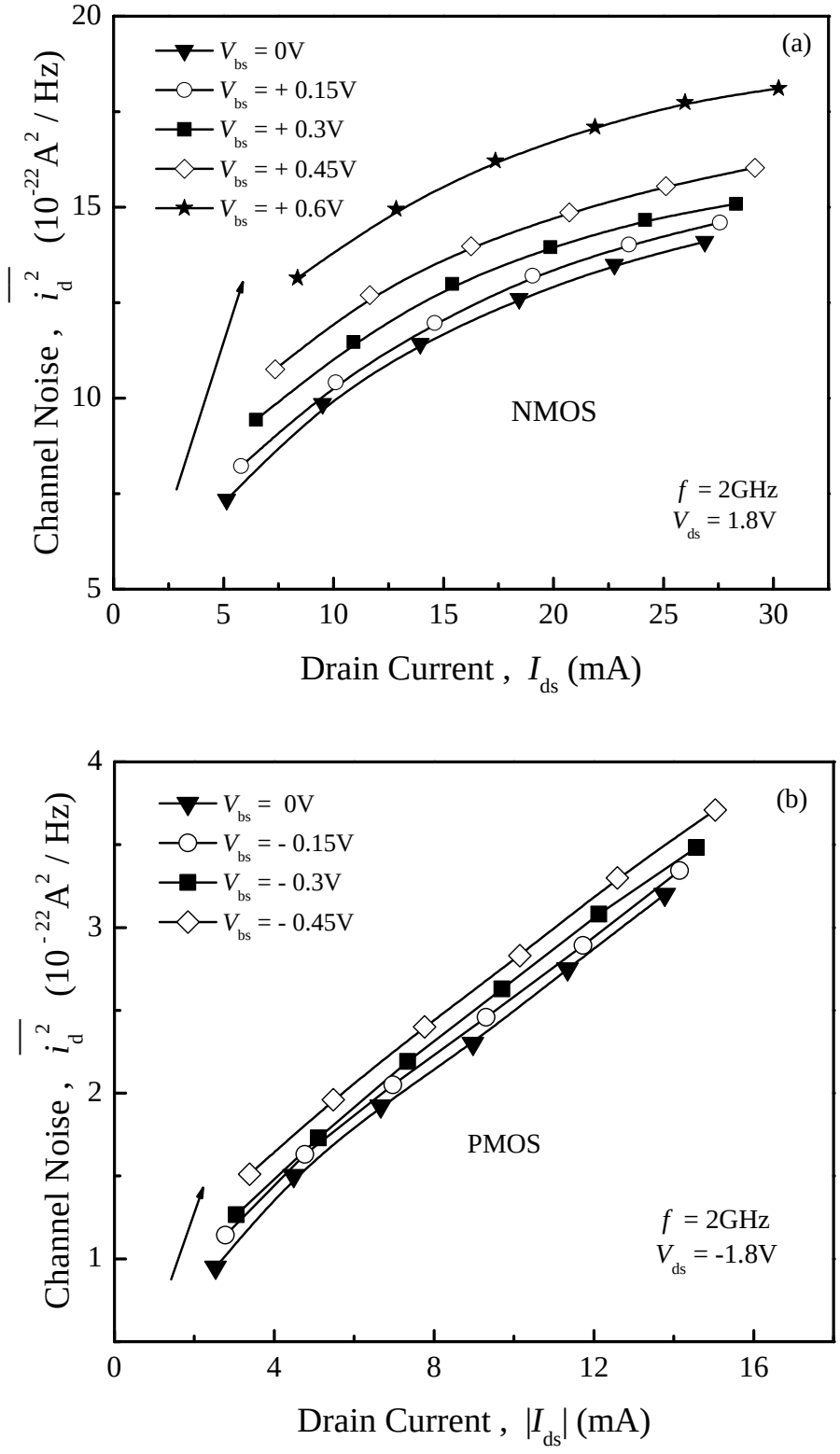


Figure 7.11: Channel noise $\overline{i_d^2}$ against drain current I_{ds} as a function of body bias V_{bs}. (a) NMOS; (b) PMOS.

The difference in R_n-g_m relationship between N- and P-MOSFET could be well explained by taking the channel noise into consideration. Figure 7.11 compares the extracted channel noise against drain current I_{ds} for N and PMOS at different substrate biases. A significant increase in channel noise is observed in NMOS when body is forward biased, whereas the increase is not obvious in PMOS. Therefore, in NMOS, besides substrate resistance noise, channel noise is responsible for the device noise degradation as well, so it leads to failure on fitting R_n by Equation (7.4) when substrate bias is larger than 0.3V. However, the impact of forward body bias on PMOS channel noise is insignificant. This explains why the measurement data of PMOS in Figure 10(b) fits well with the calculation by considering the substrate effect only.

Moreover, we found that the different channel noise behaviors between N and PMOS under FBB can be strongly supported in the light of nonequilibrium noise theory proposed by Navid and Dutton [101]. Considering the carrier nonequilibrium transport, in deep-submicrometer MOSFETs, the channel noise should include not only the usual thermal noise component, but also a partially suppressed shot noise term associated with the limited number of inelastic scattering events in the channel. Simulation studies indicated that the nonequilibrium noise is negligible when scattering is high. However, it should be accounted if the scattering is low. Mathematically, the drain noise can be expressed as

$$S_{I_d} = S_{I_d}^{\mathrm{Eq}} + C(V_{gs}, V_{ds}, V_{bs}) \cdot 2qI_d \tag{7.5}$$

where $S_{I_d}^{\mathrm{Eq}}$ is the equilibrium noise term, and the coefficient, C(V_{gs}, V_{ds}, V_{bs}) is a function of device bias condition determined by the scattering processes in the channel. According to the recent paper by Navid *et al*. [102], the dominant noise mechanism would shift from classical thermal fluctuation to shot noise as MOSFETs

scales into ballistic regime. Their hypothesis was strongly supported by the different simulation results of channel noise between long and short-channel MOSFETs when temperature or bias changes.

The number of inelastic scattering events in MOSFET channel can be approximately estimated by comparing the mean free path of carrier and the channel length. The relationship of carrier mobility and mean-free-path is given by:

$$\mu = \frac{e \times l_m}{m \times \upsilon_{th}} \tag{7.6}$$

where e is electron or hole charge, l_{m} is mean-free-path, m is the electron or hole mass, v_{th} is the thermal velocity, and μ is the carrier mobility. Following the mobility extraction method introduced in [103], we can estimate that the electron mobility μ_{n} is ~580 cm^2/V-sec (in NMOS), and hole mobility μ_{h} is ~140 cm^2/ V-sec (in PMOS) when devices operate at saturation mode. Using 2×10^5 m/s and 1.6×10^5 m/s for electron and hole thermal velocities, 1.08 m_0 and 0.56 m_0 for electron and hole effective mass (m_0 is the free electron mass), the mean-free-path for electron and hole are estimated to be 50 *n*m and 6 *n*m, respectively. Therefore, in 0.18-μm gate length devices, the order of scattering in NMOS is only about 4. This is much lower than the value ~30 in PMOS. In NMOS, the nonequilibrium noise, i.e. the 2^{nd} term in Equation (7.5) could be quite significant because of limited number of scattering events. The nonequilibrium noise thus may contribute a larger portion to overall channel noise as compared to PMOS. The reduction of electrical field and the surface scattering in the channel due to forward body bias may provide a further enhancement of channel noise, i.e., increase in C(V_{gs}, V_{ds}, V_{bs}) in Equation (7.5). In PMOS, because of the high scattering order, the nonequilibrium noise is greatly suppressed to a negligible level which is insensitive to body bias. The substrate resistance noise consequently

becomes the only important factor affecting the device noise performance when the body bias is applied.

It should be pointed out that generation-recombination (G-R) noise could also be induced via auger recombination if holes (electrons) are injected back to the channel when a forward substrate bias is applied [104]. This additional GR noise could also contribute to the channel noise. However, for NMOS, the substrate (hole) current is only about 2 μA, while drain current is around 20 mA. The ratio of I_{sub}/I_{ds} is in the order of 10^{-4}. Therefore, the contribution of GR noise to the drain current noise could be negligibly small. For PMOS, ratio of I_{sub}/I_{ds} is in the order of 10^{-6}, the effect of G-R noise is even smaller.

Through the investigation on the degradation of device noise performance under FBB, one of the important points we would like to highlight is that the contribution of the substrate resistance noise and its sensitivity to the substrate bias in RF MOSFET noise modeling cannot be underestimated. This is particularly true for the circuits in which the devices may be under forward substrate bias.

7.6 Summary

In summary, the effects of forward body bias on the high frequency noise in 0.18-μm MOS transistors have been investigated. Although MOSFETs DC performance could be improved when substrate is forward biased, significant degradation of high frequency noise was observed in both N- and PMOSFET devices. The increase in high frequency noise with $|V_{bs}|$ was qualitatively explained by considering the contributions of nonequilibrium channel noise and substrate resistance noise. The increase in high frequency noise in PMOS noise was found strongly correlated to the substrate resistance noise, while increase in RF noise in NMOS was attributed to a combinational effect of substrate resistance noise and channel noise.

Our experimental results in this study suggest that, if high frequency noise is an important concern for the RF circuit applications, forward body biasing scheme is not favorable.

Chapter 8

Conclusion and Future Work

8.1 Conclusion

High frequency noise characteristics of modern MOSFETs have emerged as an important issue in high frequency circuits design. This dissertation has explored various high frequency noise behaviors of MOSFETs, including channel noise spatial origin, physical origin of excess noise of Si/SiO_2 due to shallow interface states, body biasing effects on device noise performance, etc. To conclude, this chapter briefly summarizes the key contributions presented in the thesis.

The effects of HC induced damage and its spatial location on the high frequency noise of *n*-MOSFETs was investigated. It was observed that noise parameters NF_{min} and R_n degraded more when interface damage located at source side rather than that on drain side. The difference in noise performance with the same amount of HC damage at source and drain side is mainly attributed to the difference in channel noise increment. Considering additional channel noise i_n induced by hot carrier damage to be the same, through propagation, channel noise will increases more if noise source i_n is located at the source side. Our results provide direct experimental verification that the local noise at the source side plays a more important role in determining the overall channel noise, which has been controversial in recent compact noise modeling.

The role of shallow Si/SiO_2 interface states on high frequency channel noise in *n*-MOSFETs has been carefully investigated. It was found that the presence of shallow Si/SiO_2 interface states result in a frequency dependent excess channel noise in the gigahertz range. A new noise generation mechanism was proposed. It is suggested that carrier capture and emission associated with the shallow Si/SiO_2 interface states to be physical origin of the excess channel noise. The excess channel noise was found to be non-thermal type and could be well predicted by using van der Ziel's current fluctuation model with a characteristic time constant in the order of 10^{-11} s. An activation energy E_a of ~0.033 eV for the excess channel noise was determined by temperature dependent noise measurement, and it defines the energy levels of the shallow Si/SiO_2 interface states affecting high frequency channel noise.

The high frequency noise degradation under different types of hot carrier stresses has also been studied. Noise performance degradation was found to be dependent on the hot carrier stress biasing conditions, and strongly correlated to density of interface states generated during HC stress. It was observed that high frequency noise degradation in device is much smaller for high V_{gs} stress than that for maximum substrate current ($I_{B,max}$) stress or low V_{gs} stress. This is because oxide traps are known to be the dominant mechanism of device degradation under high V_{gs} stress (hot electron injection), while for $I_{B,max}$ stress and low V_{gs} (hot hole injection), high density of interface states are generated. When device is operating in GHz regime, excess channel noise is induced through the transition of channel carriers between shallow Si/SiO_2 interface states and the silicon conduction or valence band. On the other hand, trapping/detrapping of channel carriers associated with oxide traps are only responsible for the noise at low frequency, because they lie deeply in the gate oxide, and are difficult to be detected at high frequency. The study of the impact of

HC stress biasing conditions on high frequency noise provides a better insight into the nature of channel noise, and it highlights the importance of transition time of channel carriers associated with interface states or oxide traps on device noise performance in different frequency regime.

High frequency noise performance of CMOS under forward body biasing is investigated. Although forward body biasing has been proposed to improve device and circuit performance, significant increase in high frequency noise was observed when devices are under forward substrate biasing. This could be due to increased channel noise and substrate resistance noise under forward body bias. The increase of high frequency noise in PMOS noise was found to be strongly correlated to the substrate resistance noise, while noise increase of NMOS was attributed to a combinational effect of substrate resistance noise and channel noise. This is because the nonequilibrium noise component of overall channel noise in NMOS increases with smaller electrical field and less surface scattering under forward body bias. However in PMOS, due to the high scattering order, the nonequilibrium noise is greatly suppressed to a negligible level, so that its channel noise can hardly be affected by forward body biasing. In conclusion, for analog circuit applications, forward body biasing is not favorable if high frequency noise is a concern [105].

8.2 Recommendations for Future Work

There are various challenging issues that await exploration in future research. Noise characterization is one area that needs more work as device moving into nano-scale regime.

In this work, we have a detailed study on the hot carrier effects on the *n*-MOSFETs high frequency noise. As CMOS technology advances, the thickness of gate oxide decreases. For thinner gate oxide, gate leakage becomes an important

source of MOSFET degradation. Therefore, for future work in the study of hot carrier effects on MOSFETs high frequency noise, gate shot noise should be carefully considered as it may dominate over channel thermal noise for high frequency noise performance degradation.

Apart from hot carrier effects, as gate oxide continues scaling down, NBTI effect has becoming a major concern when realizing highly reliable integrated CMOS devices. As shown in Figure 8.1, the V_{th} shift of the PMOS due to NBTI has become a limiting factor for MOSFET further scaling [106-108]. Although NBTI has been extensively studied over years, there is still lack of research on its impact on MOSFET high frequency noise performance [109]. Better insights into HF noise due to NBTI stress will be helpful in developing accurate noise models for prediction of system behaviors in high temperature application.

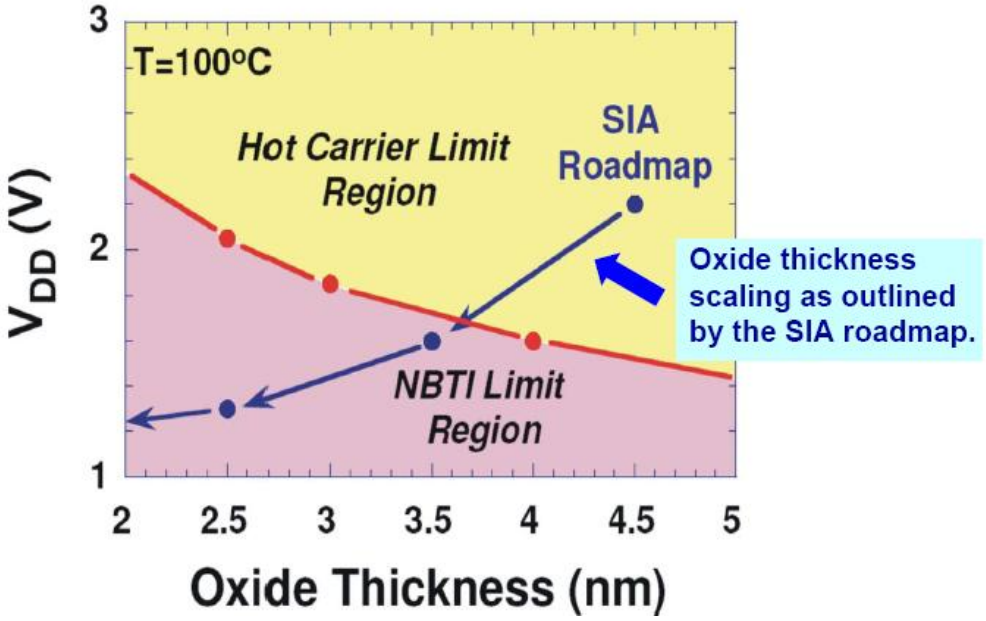


Figure 8.1: The transition of lifetime limitation mechanisms as a function of gate oxide thickness [107].

Moreover, the correlation of excess channel noise and HC induced interface states has been well studied from the device physics perspective. To make the experimental results more useful for the RF circuit designers, modeling of noise degradation due to hot carrier injection is another extension of this work.

Author's Publications

The publications are sorted in chronological order, starting with the latest one.

Journal publications

1. Hao Su, Hong Wang, Hong Liao, and Hang Hu, "High Frequency Noise Degradation in n-MOSFETs under Different Hot Carrier Stresses," (submitted to *IEEE Transactions on Electron Devices*)

2. ***Hao Su***, Hong Wang, Tao Xu, and Rong Zeng, "Role of shallow Si/Si_{O2} interface states on high frequency channel noise in n-channel metal-oxide-semiconductor field effect transistors," *Applied Physics Letter*, vol.95, pp.123508(1)-123508(3), Sep. 2009.
3. ***Hao Su***, Hong Wang and Tao Xu, "Effects of Forward Body Biasing on High Frequency Noise in 0.18-μm CMOS Transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol.57, no.4, pp.972-979, Apr.2009.
4. ***Hao Su***, Hong Wang and Tao Xu, "Hot Carrier Induced Damage and its Spatial Location on Radio Frequency (RF) Noise in Deep Submicron NMOSFETS," *IEEE Transactions on Microwave Theory and Techniques*, vol.56, no.5, pp.1295-1300, May. 2008.

Conference publications

5. Hao Su, Hong Wang "High frequency noise in deep-submicrometer nMOSFETs under different hot carrier stresses," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA USA, pp. 601-604, 2009.

6. ***Hao Su***, Hong Wang and Tao Xu, "Temperature Dependence of High Frequency

Noise Performance of Deep Submicron NMOSFETs,*" IEEE Asia Pacific Microwave Conference (APMC),* Hong Kong, China, 2008 (accepted).

7. ***Hao Su***, Hong Wang "Effects of forward body biasing on the high frequency noise in deep submicron nMOSFETs," in *2008 IEEE RFIC Symposium,* Atlanta, GA USA, pp. 567-570, 2008.
8. ***Hao Su***, Hong Wang "Experimental study on the role of hot carrier induced damage on high frequency noise in deep submicron nMOSFETs," in *2007 IEEE RFIC Symposium*, Honolulu, HI, USA, pp. 163-166, 2007.

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