A signal-conditioning chip for accelerometer applications

Lee, Wing Foon

2006

Lee, W. F. (2006). A signal-conditioning chip for accelerometer applications. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/4587>

<https://doi.org/10.32657/10356/4587>

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A Signal-Conditioning Chip for Accelerometer Applications

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2006

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Acknowledgments

It has been a great privilege to be a graduate student in School of Electrical & Electronic Engineering at Nanyang Technological University. My experience here is full of opportunities to learn from a faculty and people with a wide and deep expertise in engineering. Therefore, I would like to directly thank those people who were particularly instrumental in contributing to my experience at NTU.

First and foremost, I would like to thank my advisor, Associate Professor Chan Pak Kwong, for his invaluable guidance throughout my long journey as a graduate student. His wealth of knowledge and experiences in the integrated circuit designs have assisted me in identifying the critical and interesting issues of research. His attitude towards work and professionalism has also inspired me to continuously challenge myself to reach new levels. I look up to him not only as an excellent research advisor, but also a great person who has the highest degree of professionalism and integrity. It has certainly been a unique privilege to be under his supervision, which is the key factor in the success of this research.

In the endeavor of this research, the implementation of the accelerometer system, in particular, could definitely not have been completed without significant input from industrial and commercial world. I would like to express my deepest gratitude to Mr. Chew Chim Lai for sharing his expertise and industrial experiences in the field of my research. His invaluable inputs on real-life, practical problems encountered in the accelerometer industry have greatly contributed to the success of the project.

One of the best things about NTU has been the knowledgeable and friendly people that I have had privilege to work and become friends with. Many thanks to Associate Professor Siek Liter for sharing his interesting stories on those big names and his knowledge in the IC design industry that has widen my scope of the global IC market, as well as those countless supports that he has given me throughout my student life in the University. A special thanks to Associate Professor Ng Lian Soon and Associate Professor Jong Ching Chuen for their wise analysis of the IC job market that has help me to identify some relevant potential job opportunities. I am also grateful to Associate Professor Au Yeung Tin Cheung for sharing interest topics on Quantum Theory. I would like to thank my good friend, Qasem Mohammad Hindi Alramandan. His perseverance on BioMEMS research has pushed my research interest to a higher level and has increased my appreciation on microsystem technology. Our discussions on wide variety of topics, especially on Physics and BioMEMS, have been very enriching and enjoyable. I would also like to say thanks to another of my good friends, Tan Meng Tong. He has been my usual lunch partner, whom I have enjoyed chitchatting with. I cannot continue without acknowledging my postgraduate friends, Alper Cabuk, Cai Hong, Chow Fong Ling, Du Yuanyuan, Fan Xianping, Jia Lin, Li Jing, Ng Wil Lie, Shangguan Wangzuo, Sin Tze Yee, Wong Hon Hin, Yang Wei and Zhang Hongliang.

The research work would not have been possible without the help of the lab support team. I greatly appreciate the help from Ms. Guee Geok Lian, Ms. Tan Min Lim, Mr. Richard Tsoi, Ms. Gan Siew Kim, Ms. Hau Wai Ping, Ms. Chan Nai Hong, Ms. Koh Piak Yok, Ms. Katherine Kwek, Ms. Lim Siew Peng, Ms. Tung Wang Why, Ms. Wong Li Eng, Ms. Adelene Yong, Mr. Tay Boo Thong, Ms. Lim Huey Pin, Ms. Joanne Lim, Mr. York Ching Fong and Mr. Thomas Lee. They were always there for me when I needed logistic supports.

I would like to thank all my friends who have help me in one way or another especially those more important ones here, who had encouraged me throughout my Ph.D. career. Yap Hui Boon has been an exceptional friend and a very understanding girl that deserves more thanks than I can express here. I treasure all the happy moments that we were together very much. I would like to extend my special thanks to my best friends, Tan Ming Siew, Esther Oon, Carey Wan, Jiame Tan and David Lim; my former colleagues, Crystal Oh, Joanne Lee, Jocelyn Chua and Tan Li Lin; my marathon and biathlon jogging mates, Lee Yee Hui and Chan Chong Wei; and not forgetting those kind-hearted friends in Chen Su Lan Methodist Children Home, Mr See Choon Wai, Nancy Lau and Lim Puay Leng.

Last but not least, my acknowledgment would not be complete without expressing my deepest gratitude towards my family, which has supported me throughout the years. I am greatly indebted to my mother who has taken good care of me in all aspects especially cooking delicious meals.

I would like to acknowledge Academic Research Fund (AcRF) for supporting this project and NTU for funding the patent. Great thanks to Ms. Fu Dong from Innovation and Technology Transfer Office for administrating the patent application and filing.

Summary

This thesis presents a low-cost, high-performance, fully-integrated interface and signal-conditioning ASIC (Application-Specific Integrated Circuits) for capacitive-based automotive accelerometers. The ASIC is a mixed-signal system, which comprises a switched-capacitor (SC) sense amplifier, a two-stage (SC and continuous-time) filter, a scaling output stage and a clocking module, with on-chip calibration capability. The design foundation is based on a new "injection-nulling switch" (INS). The INS has been experimentally verified to exhibit error less than 25 μV in sample-and-hold (S/H) circuit and demonstrated to be insensitive to variation of process parameters. For the ASIC design, the INS allows for simplified topology of SC front-end sense amplifier and subsequent SC building blocks without jeopardizing the performance via counteracting the impact of charge injection and clock feedthrough effects on sensitivity, resolution and offset. This has resulted in reducing power consumption of system IC significantly. The clocking module is a new programmable low-frequency clock generator based on the Miller ring oscillator that offers wide-tuning range whilst using small capacitance values, with jitter less than 300 ps at $\pm 10\%$ variation in 5 V supply. A new orthogonal fusible link structure design is incorporated in the calibration circuits to improve its reliability. The development of the ASIC is based on a new sensor model, which takes into account of sensor parasitic effects. The ASIC was fabricated using a standard 0.6 μm CMOS technology with a die size of 2.8 mm by 2.3 mm. The accelerometer was implemented in a two-chip integrated 16-pin DIL IC, where the ASIC was bonded to a $\pm 50\text{ g}$ sensing element. The IC has been experimentally tested. It has achieved a low power consumption of 10 mW (2 mA at 5 V), maximum noise root spectral density of 11.87 $\mu\text{V}/\sqrt{\text{Hz}}$ (rms noise root spectral density of 0.187 mg/ $\sqrt{\text{Hz}}$) at 15.63 Hz, a signal-to-noise dynamic range of 77 dB for 500 Hz bandwidth and 74 dB for 1 kHz bandwidth, and maximum clock noise of 1.562 mV.

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CHAPTER 1

Introduction

1.1 Motivation

With the advancement in integrated circuit (IC) and microsystem technologies [Menz-2001], [Madou-2002], silicon sensor technology [Petersen 1982] has emerged pre-eminently in the area of transducer applications, leading to a huge variety of silicon sensors being actualized [Middelhoek-1989], [Sze-1994], [Göpel-1995], [Baxter-1997]. Accelerometers belong to a class of mechanical sensors [Malvicino 1996] that measure accelerations of moving bodies and convert them into electrical signals. Through the years, capacitive acceleration sensing elements have received much attention [Petersen 1982], [Rudolf 1983], [Rudolf 1987], [Wilner 1988], [Seidel 1990], [Burbaum 1991], [Cole 1991], [Peeters 1992], [Ristic 1992], [Puers 1993], [Lee 1996], [Baxter-1997], [Drieënhuizen 1997], [Yazdi 1998], [Weigold 2001]. This is because they exhibit high sensitivity, low drift, low temperature sensitivity, low cost, simplicity in structure and compatible with CMOS process [Zimmermann 1995], [Yazdi 1998]. These characteristics are important when applied to automotive accelerometers. Accelerometers such as those for seat-belt and air-bag systems, which are capable of sensing up to 50 g of acceleration (where 1 g is the acceleration due to the average force of gravity occurred at the Earth's surface approximately equal to 9.807 m/s^2), have become popular ever since the safety requirement for the automobile has risen [Goodenough 1991]. This has led to a high demand for low-cost and small-size accelerometers. Thus, integrated capacitive-based accelerometers, which meet the requirements, are well received [Petersen 1982a], [Henrion 1990], [Leuthold 1990], [Rudolf 1990], [Yun 1992], [Kuehnel 1994], [Smith

1994], [Lu 1995], [Wenk 1995], [Zimmermann 1995], [AD 1996], [Boser 1996], [Chau 1996], [Hierold 1996], [Matsumoto 1996], [Spangler 1996], [Ahmad 1997], [Lötters 1997], [Motorola 1997], [AD 1998], [Puers 1998], [Selvakumar 1998], [Lemkin 1999], [Takao 1999], [Motorola 2000], [Yazdi 2000], [Motorola 2001], [Motorola 2001a], [Luo 2002],

The implementations of these accelerometers can be classified into two types, namely fully integrated approach and two-chip approach. A fully-integrated capacitive accelerometers, whereby the electromechanical sensing element and the electrical ASIC (application-specific integrated circuit that comprises interface and signal-conditioning circuits) are fabricated on a single monolithic IC, offer ease of packaging and reduced parasitic effects on connections between the sensor and the ASIC. However, as micromachining processes are still complicated and failure prone [Kajita 2000], the yield of the overall integrated system can be a serious problem. Consequently, the cost of the final product will increase. In contrast, a sensing element and ASIC that are manufactured separately and bonded together during packaging on a two-chip approach, can achieve higher yield [Kajita 2000] especially on the ASIC, which is fabricated on a more stable IC manufacturing process. This approach can also add flexibility to the designers whereby stand-alone sensing elements can be employed if micromachining facility is not available. Nevertheless, it presents a potential problem on higher parasitic effects.

Much as the capacitive accelerometers are well received, high-performance ASICs that exhibit low-power and high-resolution characteristics are required to interface with the capacitive sensing element. This has imposed a design challenge on the ASIC designers. Low-power requirement is important especially in air-bag applications, where there will be a potential low supply of power during crashing environment. One of the crucial factors

that determine the power consumption is most often dictated by front end sensing interface. This is because the interface circuit is heavily responsible for reducing the circuit inherent DC (direct-current) offset and low frequency noise in order to achieve high resolution in the context of small changes of sensing capacitance. Sensing interfaces [Kuehnel 1994], [Lötters 1999], [Wu 2002] making use of the chopper stabilization technique are popular. However, the chopper stabilization scheme requires the operational amplifier (opamp) to operate at high frequency so as to perform modulation and demodulation functions. It is well understood that for some gain requirements, an opamp that is designed to operate at high frequency drains more power than low-frequency based designs. Alternatively, other well-known front-end capacitive interfaces [Kung 1988], [Schnatz 1992], [Yamada 1992], [Kemp 1995], [Zimmermann 1995], [Ahmad 1997], [Kraft 1998], [Lemkin 1999], [Yazdi 1999], [Ogawa 2001] using a switched-capacitor (SC) approach were proposed. Although the simple interface [Ahmad 1997] minimizes the power consumption, it often suffers from switch injection errors caused by charge injection (CI) and clock feedthrough (CF) effects when using MOS (metal-oxide semiconductor) based switches [Unbehauen-1989], [Martin-1997]. This greatly limits the resolution as well as the stability due to the offset drift with temperature and time. Thus, complicated front-end interface circuits [Schnatz 1992], [Lemkin 1999], [Yazdi 1999], [Wu 2002] have been proposed to compensate these switch errors. In these sophisticated topologies, fully differential opamps in association with complicated switch arrangement and capacitor pairs are commonly used but they will increase the power dissipation and switching noise. As reported, a fully differential (FD) opamp consumes 40 to 70 percent more power [Unbehauen-1989] and requires more silicon area than its single-ended counterpart [Martin-1997]. Furthermore, a common-mode feedback (CMFB) circuit is needed to stabilize the common-mode output voltage in FD opamp.

The conventional method for tackling the problem of switch injection errors is to use a dummy switch topology [Eichenberger 1990], [Unbehauen-1989], [Martin-1997]. It offers effective compensation of switch errors but it is more sensitive to variation of process parameters. This is due to the main switch and the half-size dummy switch being different sizes, which makes them difficult to match each other under different process parameters. Thus, this gives the motivation to investigate a new effective compensation switch, which is not sensitive to variations in process parameters, and yet is simple in design and implementation for circuits to avoid high-power circuit topology in front-end interface.

Another important requirement for the front-end interface is that of the safety standard as demanded by automotive regulation. Hence, the accelerometer should provide self-testing function, which imposes a design issue on the sense amplifier. The open-loop structure is preferred because closed-loop structures using force-balanced technique, dependent upon applications [Lemkin 1999], [Yazdi 1999], might have difficulties in implementing the self-test feature on the basis of topology, complexity, stability and performance tradeoffs. This project is focused on the design of an accelerometer with self-test capability.

Another problem inherent in the micromachining fabrication process when dealing with acceleration sensors is the large deviation in their device parameters [Göpel-1995], [Menz-2001], [Madou-2002] which can be as much as plus or minus 50 percent. As the accuracy of the accelerometer can be affected significantly, on-chip calibration must be provided for post-adjustment of the system. Commonly-use techniques such as continuous type laser trimming [Brokaw 1996], [Deluca 2002] method can provide good results, but it is expensive. As cost is an important issue in automotive applications, discrete-type trimming techniques such as floating gate [Säckinger 1988], Zener-zapping [Erdi 1975] and fusible link [Schroeder 1977], [Mok 1995] methods can offer the alternative solutions.

However, when considering the implementation perspective, the floating gate method suffers from leakage problem [Manabe 1999], the Zener-zapping method requires a bipolar process. In contrast, fusible link method avoids these shortcomings and allows ease of implementation in a standard CMOS process. However, it is subject to the possible regrowth of blown fuses under environmental temperature effect. This raises the motivation for investigation of a reliable calibration circuit technique.

1.2 Objectives

The main objective of the thesis is to investigate circuit techniques for the design and realization of a low-cost, high-performance, fully-integrated capacitive-based accelerometer for automotive applications. The scope of the research project can be stated as follows:

1. To investigate modeling approaches for sensing elements so as to facilitate the entire mixed-signal system simulation using the Spice circuit simulator.
2. To research new methods for solving a fundamental problem that limits the performance of switched-capacitor-based sensing networks and to design a low cost capacitive sensing interface with self-test capability for accelerometer.
3. To research strategies for designing cost-effective analog signal-conditioning building blocks.
4. To investigate low-cost techniques for on-chip calibration of the accelerometer system.

Table 1.2.1: Design specifications

Specification	Typical Automotive Industrial Requirement for 50 g	Design Specification for 50 g
Operating Power	Low	10 mW
Output Noise	< 1 g (at 1 kHz)	0.5 g (at 1 kHz)
Resolution	500 mg (at 1 kHz)	500 mg (at 1 kHz)
Non-Linearity	1 %	1 %
Power Supply	5 V	5 V
Frequency Range	DC to 1 kHz	DC to 1 kHz
Operating Temperature Range	-40 °C to +85 °C	-40 °C to +85 °C
Shock Survival	2000 g	2000 g
Load	Buffered	10kΩ, 100 pF
Sensitivity	-----	40 mV/g
Output	-----	0.25 to 4.75 V
ASIC Technology	-----	0.6 μm CMOS
ASIC Die Size	-----	3 mm by 3 mm
Integration	-----	Two-chip
External Supporting Circuitry Needed	-----	No

Based on the typical automotive industrial requirements for 50g accelerometer, the design specifications for the accelerometer are given in Table 1.2.1. Operating power of an accelerometer integrated circuit is often a major concern in automotive-based applications because the power supply during a car crash can be very low. Hence, low supply power is highly desirable and this turns out that the supply current should be made as small as possible. An operating current of 2 mA at a 5 V supply would be appropriate. However, this is translated to a challenge in the accelerometer system design. In addition, the design should address small area of die size as it helps the reduction of production cost. In this specification, the estimated maximum die size of 3 mm by 3 mm is suitable for housing the entire signal-conditioning circuit together with a sensor in a common 16-pin DIP (Dual-in-line package). Finally, with the employment of a standard CMOS process, not only does it benefit from low cost, it facilitates the system integration with the ultimate goal of no external supporting circuitry.

1.3 Major Contributions of the Thesis

The major contributions of this dissertation can be summarized as:

1. A low-cost, high-performance ± 50 g accelerometer has been successfully designed and realized. The performance of the accelerometer has shown significant improvement over that of the present commercialized products [AD 1998], [Motorola 2001]. The key performance can be summarized as follows:
 - Power consumption of 10 mW (2 mA at 5 V supply) without the need of external circuitry.
 - Low-noise with maximum noise root spectral density of $11.87 \mu\text{V}_{\text{pk}}/\sqrt{\text{Hz}}$ (equivalent to rms noise root spectral density of $0.187 \text{ mg}/\sqrt{\text{Hz}}$) at 15.63 Hz.
 - High resolution with root-mean-squared (rms) noise level of $0.314 \text{ mV}_{\text{rms}}$ or equivalent of 7 mg for 1 kHz bandwidth.
 - High signal-to-noise dynamic range of 74 dB for 1 kHz bandwidth, 77 dB for 500 Hz bandwidth, and 84 dB for 100 Hz bandwidth.
 - Maximum clock noise of 1.562 mV.
 - Programmable filter bandwidth of 500 Hz or 1 kHz.
 - Self-test function with high self-test output voltage.

2. A new "injection-nulling switch" (INS) switch that offers effective compensation of charge injection and clock feed-through errors has been invented. It has improved performance over the dummy switch topology. It is easy to be implemented into switched-capacitor circuits. It does not need a fully differential opamp configuration, hence simplifying the front-end sense amplifier and subsequent switched-capacitor modules and achieving low power consumption for the overall system. In addition, it is insensitive to variation of process parameters. The INS technique has been filed in a patent.
3. A small area and low-jitter ring oscillator has been designed. For identical values of integrated components in implementation, the proposed ring oscillator reduces the oscillation frequency by 5 times over the conventional ring oscillator, and 3 times over the conventional current-starved inverter ring oscillator. Benefits include a relaxation of the PSRR requirement and a reduction of substrate noise coupling in mixed-signal circuits. A programming range of 56 kHz to 1.042 MHz has been achieved using discrete-step tuning on small capacitor values from 0.375 pF to 5.625 pF together with frequency division by four divider stages, whilst the jitter is less than 300 ps at $\pm 10\%$ variation in a 5 V supply in the entire tuning range.
4. A low cost, CMOS compatible fusible link technique with improved reliability has been successfully designed, and realized as part of an on-chip calibration circuit. The proposed orthogonal fusible link trimming circuit, making use of a redundancy technique, adds extra protection to the programmed data and lowers the possibility of regrowth of blown fuses. As a result, it improves the reliability of the calibrated accelerometer system.

1.4 Organization of the Thesis

Following this introduction, the subsequent chapters are organized in the following manner.

Chapter 2 covers the review of accelerometer system and circuit design. First, it reviews accelerometer system architectures concerning with different implementations that include sensing element and ASIC. Next, there follows a discussion on system configurations in terms of closed-loop and open-loop system approaches. Then, literature surveys on the circuit topology of each building block in the ASIC are presented.

Chapter 3 discusses the modeling of the acceleration sensing element. This includes the development of a sensor model in Spice. The model takes into account non-ideal effects such as leakage, stray resistances and parasitic capacitances.

Chapter 4 presents the proposed injection-nulling switch (INS), which is the key building element for designing the switched-capacitor circuits employed in the accelerometer system. The theory of the INS is first explained. A description of the INS implementation using a simple sample hold circuit for verification of its performance is then provided. The experimental results are given for comparing with other switch topologies.

Chapter 5 presents the overall proposed accelerometer system architecture. It describes the proposed techniques to be used in implementing the respective building blocks for the system as introduced in Chapter 2.

Chapter 6 presents the implementation of the front-end sense amplifier and signal-conditioning block, which includes a gain stage, a filter stage and an output stage. The employment of INS in the SC circuits has demonstrated that the circuit topologies can be simplified and the power consumption can be reduced without sacrificing the performance.

Chapter 7 describes the clock generator together with its on-chip calibration technique. The programmable low-frequency Miller ring oscillator clock and the orthogonal fusible link structure are proposed. Their circuit operation principles are detailed. The measurement results of the work are discussed.

Chapter 8 discusses the complete measured results on the realized accelerometer, with emphasis on comparing the key parameters of the proposed work with that of state-of-the-art commercial products and previous works.

Chapter 9 summarizes the work presented in this dissertation. It gives the conclusions as well as the recommendations for future research.

CHAPTER 2

Review of Accelerometer System and Circuit Design

2.1 Introduction

The challenge in building accelerometer systems involves the design of a high quality electromechanical sensing element and high-performance electrical ASIC as well as interfacing between these two entities in a complete system. As mentioned in the previous chapter, integration of the sensing element and the ASIC can be in fully-integrated or two-chip approach. Table 2.1.1 summarizes the differences between these two approaches, relating to important issues that affect the overall system performance.

Table 2.1.1: Summary of fully-integrated and two-chip approach [Kajita 2000]

	Fully-integrated Approach	Two-chip Approach
Yield of the product	<i>Poor</i> Micromachining processes are failure-prone.	<i>Good</i> Micromachining process and IC process can be optimized individually and IC process is more stable in general.
Performance of ASIC and overall product	<i>Moderate</i> Limitation on ASIC performance as micromachining process uses older IC process for fabrication of ASIC.	<i>High</i> Standard IC process can be used for fabrication of higher performance ASIC.
Choice of sensing element	<i>Rigid</i> It is fixed to a particular micromachining process.	<i>Flexible</i> Stand-alone, high quality sensing elements can be employed if no access to micromachining process.
Parasitic effects	<i>Low</i> On-chip connections reduce the parasitic effects.	<i>High</i> Parasitic effects arise from bonding pads and bonding wires.
Ease of packaging	<i>Good</i> Only one monolithic IC is considered.	<i>Moderate</i> Positioning of the two-chips is considered.

The comparison has shown that the two-chip approach is favorable for designing low-cost, high performance accelerometers. In view of those demerits, whilst the present fast growing packaging technology can deal with the packaging problem, the parasitic effects can be alleviated by circuit techniques. Thus, a realistic acceleration sensing element model that encompasses parasitic effects is important for use in design and simulation phase.

The criteria for designing high-performance ASIC are identified as low noise, low power consumption, high resolution, cost-effective design and simplicity in implementation. Therefore, they must be addressed during system architecture and circuit building blocks design.

This chapter first describes conventional accelerometer system architectures. The state-of-the-art commercial accelerometer system architectures are then discussed. This is followed by a review of circuit design techniques for individual building block. The review of sensor modeling is covered in the next chapter.

2.2 Review of Accelerometer System Architectures

Capacitive accelerometer systems can be classified into two main categories, closed-loop configuration (Figure 2.2.1) and open-loop configuration (Figure 2.2.2).

Figure 2.2.1: Simplified block diagram of a closed-loop accelerometer system configuration

Figure 2.2.2: Simplified block diagram of an open-loop accelerometer system configuration

During the sensing process, the closed-loop configuration (also known as force-balanced configuration) feeds back a signal to control the proof mass of capacitive acceleration sensor by electrostatic force so as to balance it at a neutral position in stable manner. The acceleration readout will usually be measured according to the amplitude of electrostatic force that maintains the proof mass at that position. Various schemes were employed to implement the feedback approach. These include phase-locked loop (PLL) [Matsumoto 1993], pulse width modulation [Suzuki 1990], gain feedback [Paemel 1989], [Boxenhorn 1990], [Leuthold 1990], [Kampen 1994], [Kuehnel 1994], [Krömer 1995], [Zimmermann 1995], [Burstein 1996], [Chau 1996], and sigma-delta modulators [Henrion 1990], [Yun 1992], [Smith 1994], [Lu 1995], [Boser 1996], [Spangler 1996], [Wuestling 1997], [Kraft 1998], [Kraft 1998a], [Lemkin 1999], [Yazdi 1999], [Kulah 2000].

Although closed-loop operation can improve linearity, dynamic range and bandwidth, there are some key issues to be addressed. First, it is important to have an accurate acceleration sensor model to facilitate the design of feedback control. However, it is often onerous to obtain an accurate model because the sensor parameters are subject to variation of process parameters [Göpel-1995], [Menz-2001], [Madou-2002], which are random in nature. These variations could cause the parameters, for instance the sensing capacitance, to deviate about $\pm 50\%$ from nominal value. The outcome is that the loop stability is difficult to maintain. This makes a significant impact on the production yield of closed-loop accelerometers leading to increase of production cost. Second, depending on topology, high sampling rate systems, such as sigma-delta modulators and PLL schemes, can consume significant power. It is common to observe that high-order sigma-delta modulators or high-frequency-based PLL circuits consume more power than those of the open-loop counterparts that employ low sampling rate circuits. Third, sensor self-test capability is not often demonstrated in closed-loop configurations on the basis of the difficulty in including self-

test circuitry into the feedback loop, for example in peculiar topology of sensor interface [Lemkin 1999]. This is because the sensing element does not provide built-in mechanical self-test structure like comb-drive capability [Kuehnel 1994], [Zimmermann 1995], [Chau 1996], [Lee 1996], [Yazdi 1998], [Lemkin 1999], [Weigold 2001]. The reason for the absence of mechanical self-test structure in sensing element is to avoid decreasing of yield, as more fabrication steps are needed. To allow self-test function in such a sensing element, the common way is to inject a reference voltage signal into the feedback loop during self-testing mode [Kuehnel 1994], [Chau 1996], [AD 1996]. In summary, the closed-loop configuration is less attractive in terms of product cost (which is related to yield and test cost), power consumption and inclusion of self-test function, which are essential attributes for industrial automobile accelerometers.

In contrast, open-loop configurations are simple and inherently stable. Due to tolerance on variation of process parameters, the yield of the open-loop accelerometers can be better than the closed-loop counterparts. Furthermore, in view of the ease in adding self-test circuit, the open-loop accelerometers have been demonstrated successfully in the design trend of current commercial products [Motorola 1997], [AD 1998], [AD 1999], [Motorola 2001], [Motorola 2001a].

The basic structure of a conventional open-loop capacitive accelerometer system (Figure 2.2.2) comprises a front-end interface block, a signal-conditioning block, a clock generator and trimming circuits. The front-end interface block contains a sense amplifier that converts change in capacitance into electrical signal. As the change in capacitance is small, DC offset and noise problems become the major concerns because they determine the accuracy as well as the resolution of the acceleration measurement. The signal-conditioning block can include a gain stage, a filter stage and an output stage. The gain stage amplifies

the electrical signal from the sense amplifier to the required scale before the signal enters the filter stage. The filter stage can be a low-pass filter that removes out-of-band noise especially the switching and clock noises if switched-capacitor circuits are used. It also defines the operating bandwidth of accelerometer so as to avoid hitting the resonant frequency of the sensing element. The output stage is designed to drive external load and to perform scaling of output signal to required specification. The clocking circuit is used mainly to provide clocking sequence to analog switches and digital control circuits for the system. In order to provide control on the accuracy of readout circuit, trimming circuits are incorporated into the system.

2.2.1 Review of Closed-loop Structures

The accelerometer that has been reviewed in literature is the Analog Devices ADXL50 [AD 1996]. It was the first commercially available ± 50 g accelerometer that employed fully-integrated approach [Goodenough 1991]. The initial cost of the product was high. This could be due to the yield problem, which led to high production cost.

The front-end interface is configured as a closed-loop (force-balanced) system, which consists of a sensor, a demodulator and a preamplifier. The sensing scheme applies chopper stabilization technique (to be discussed in the section 2.3.2) for compensating the offset error of the amplifier and reducing low frequency noise. The on-chip oscillator modulates the change in the sensor capacitance to high-frequency electrical signal. It also drives the synchronous demodulator that demodulates the modulated high-frequency signal back to baseband, hence eliminating the offset error. The baseband signal is fed back through a $3\text{ M}\Omega$ resistor to electrically force the center sensor plate back to its neutral position. As the modulation and demodulation are operated at high frequency, the bandwidth of the opamp has to be larger for signal integrity. This causes the power consumption of the opamp to be comparatively higher than those of low-bandwidth type. It becomes the major contributor to the high power dissipation in the chip, which is specified typically at 50 mW (10 mA at 5 V). In addition, there exists a feedback stability problem of closed-loop system if there are large changes in sensor parameters due to variation of process parameters. This further deteriorates the yield of the product. The preamplifier provides a full-scale output range of 0.85 V to 2.75 V for ± 50 g.

The front-end interface circuit also incorporates a self-test function. Due to the closed-loop configuration, an additional reference voltage has to be injected into the feedback loop during self-testing mode [Chau 1996].

The output circuit, comprising an uncommitted buffer amplifier, is separated from the interface circuit. Therefore, for a complete accelerometer system with full-scale output range of 0.25 V to 4.75 V, an external resistor network is required to configure the buffer amplifier. Although the approach offers flexibility in configuring for different sensitivity, it is not favorable for some applications with highly integrated objective. The ADXL150 [AD 1998] is an improved version of ADXL50. It is an open-loop system that offers reduced power consumption of 9 mW (1.8 mA at 5 V supply). The built-in buffer amplifier provides a full-scale output range of 0.6 V to 4.4 V. When a true DC (gravity) response with full-scale output range of 0.25 V to 4.75 V is specified, an external amplifier with resistor network is required.

2.2.2 Review of Open-loop Structures

Motorola MMA2202D ± 50 g accelerometer [Motorola 2001] is one of the commercially products that utilizes open-loop structure. The MMA2202D has adopted the two-chip approach. The surface-micromachined capacitive sensing cell (G-Cell sensor) and CMOS (complementary metal-oxide semiconductor) signal-conditioning ASIC are fabricated separately using different processes (one is MEMS-based, the other is CMOS-based). They are bonded together during packaging and are housed in a single package.

The accelerometer system is configured in open-loop structure whereby the front-end interface circuit (as being labeled "INTEGRATOR" block [Motorola 2001]) is directly connected to a gain stage, which is followed by a filter stage. Such an arrangement is inherently stable and easy for incorporating self-test circuit that activates the built-in mechanical sensor self-test structure in the G-Cell. Nevertheless, the use of built-in mechanical self-test structure can reduce the yield of the sensing element. Besides, owing to extra processing steps combined with the increase of complexity in mechanical sensor, the front-end interface circuit employs switched-capacitor technique, which is insensitive to sensor parasitics and compensates both amplifier offset error and low-frequency noise. However, this technique suffers from switch injection errors, arising from charge injection and clock-feedthrough errors when MOS-based switch is turned off. These errors greatly limit the accuracy and the resolution of acceleration readout.

The gain and filter stages are both realized using switched-capacitor technique. The filter stage is of low-pass Bessel-filter type. The advantage of using the Bessel-type is that it preserves the pulse shape integrity, as its phase response is linear against frequency. The trade-off is that the filter roll-off rate is low (lower than that of Butterworth filter type).

This is the reason for implementing a 4th order Bessel filter in order to achieve the required roll-off sharpness. However, this increases the power consumption because the number of opamps required for the filter stage is high. The typical value of power consumption for the chip is specified at 25 mW (5 mA at 5 V). An internal clock generator, which is driven by an on-chip oscillator, provides clock signals to the analog switches in the SC circuits. As the filter is of SC type, the clock signals would appear as high frequency clock noises at the output. Therefore, an external continuous-time filter is required to filter these clock noises (as recommended in the data sheet).

The control logic provides the overall control of the accelerometer system while the EPROM (electrically-programmable read-only-memory) trimming circuit calibrates the gain stage and the output stage ("TEMP COMP" module) to required output specification. The use of EPROM in the trimming circuits, however, will inflict some implementation and reliability issue on trimming settings. First, most standard CMOS process does not support fabrication of EPROMs. The implementation of EPROMs would result in increasing of production cost. Second, there is also a potential leakage problem in EPROMs due to the stored charges being leaked away over a long period of time. Consequently, some of the trimming data may be lost, resulting in malfunction of the accelerometer.

2.3 Review of Front-End Interface Circuits

2.3.1 Preliminary

The front-end interface circuit (or sense amplifier) is essentially a capacitance-to-voltage converter. It senses the change in capacitance of sensing element resulted from the change in acceleration and then converts it to the change of voltage at its output. In order to establish the relationship between acceleration, the capacitance and the output sensing voltage, the transduction of acceleration to capacitance is first discussed.

Figure 2.3.1.1: Mechanical lumped model of an acceleration sensor

Figure 2.3.1.1 shows the lumped mechanical model of an acceleration sensor. The electrodes are connected to the conductive proof mass and fixed frame that exists a capacitance between them. The dynamic response of acceleration sensor can be modeled as a second-order system, in which the mechanical transfer function (detailed derivation of the function is covered in sensor modeling chapter) in s-domain can be expressed as

$$H(s) = \frac{X(s)}{A(s)} = \frac{m}{k_s} \frac{\frac{k_s}{m}}{s^2 + \frac{b}{m}s + \frac{k_s}{m}} = K \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2.3.1.1)$$

From Equation (2.3.1.1), the transfer function of proof mass displacement x , over the external acceleration a , has a natural resonant frequency of $\omega_n = \sqrt{\frac{k_s}{m}}$, a damping factor of

$\xi = \frac{1}{2}b\sqrt{\frac{1}{mk_s}}$, and a sensitivity of $K = \frac{m}{k_s}$. Therefore, the static response ($s = 0$) of the

change of proof mass displacement Δx_{static} , under external acceleration can be denoted by

$$\frac{\Delta x_{static}}{a} = \frac{m}{k_s} \quad (2.3.1.2)$$

The capacitance between the proof mass electrode and the fixed frame electrode C , having an effective capacitive area S , and a cavity distance x_d , between them is defined by the function

$$C = \frac{\epsilon_o \epsilon_r S}{x_d} \quad (2.3.1.3)$$

The product of the permittivity of free space ϵ_o , and the relative permittivity ϵ_r , gives the permittivity of the dielectric material in the cavity between the mass and the fixed frame. If the cavity is filled with air, which is in most cases, the permittivity can be approximated to that of free space ϵ_o , where the relative permittivity of air is about one [Madou-2002]. Since the capacitance is reciprocal to the cavity distance, the displacement of the proof mass is often limited to $\pm 10\%$ of the nominal cavity distance in order to ensure good linearity. Hence, for small change of displacement (δx) from its nominal distance (x_o), the small change of capacitance (δC) can be approximated to the product of the gradient of the capacitance function at x_o , and the small change of displacement δx . This can be written as

$$\delta C \approx \left. \frac{dC}{dx_d} \right|_{x_d=x_o} \delta x = -\frac{\epsilon_o \epsilon_r S}{x_o^2} \delta x = -\frac{C_o}{x_o} \delta x \quad (2.3.1.4)$$

The capacitance $C_o = \frac{\epsilon_o \epsilon_r S}{x_o}$ is the nominal capacitance when the cavity distance between the proof mass electrode and the fixed frame electrode is x_o . Therefore, the static sensitivity of change of capacitance under external acceleration (according to the direction of displacement in Figure 2.3.1.1) can be expressed as

$$\frac{\Delta C_s}{a} = -\frac{C_o}{x_o} \frac{\Delta x_{static}}{a} = -\frac{C_o}{x_o} \frac{m}{k_s} \quad (2.3.1.5)$$

Note that a linear relationship between ΔC_s and a , is established.

Figure 2.3.1.2: Equivalence of the sensing element to differential sensing capacitors, C_{S1} and C_{S2}

Figure 2.3.1.2 shows the equivalence of sensing element in the form of differential sensing capacitors, top plate capacitor C_{S1} and bottom plate capacitor C_{S2} . Under the displacement (x) of middle movable plate, the capacitance of differential sensing capacitors can be calculated by

$$C_{S1} = C_o + \Delta C_s \quad (2.3.1.6)$$

$$C_{S2} = C_o - \Delta C_s \quad (2.3.1.7)$$

Note that the nominal capacitance C_o and the change of capacitance ΔC_s can be obtained from Equation (2.3.1.3) and Equation (2.3.1.5) respectively. From the above two equations, the capacitance values of C_{S1} and C_{S2} reflect the change of external acceleration translated by sensing element. In brief, the physical acceleration parameter can be indirectly measured by converting the change of capacitance to useful electrical signal via the capacitance-to-voltage sense amplifier.

2.3.2 Front-End Sense Amplifier

The objectives of designing sense amplifier are to achieve high resolution, low power dissipation by circuit topology and simplicity of incorporating self-test function. These issues are discussed as follows.

The first issue is related to sensing resolution. Since resolution depends on the minimum detectable change in sensing capacitance, the strength of electrical signal at the minimum detectable value is small. The adverse effects of amplifier offset, device and circuit noise, and switch injection errors (for sampling circuit) become significant. The main causes of amplifier offset are improper device dimensions, bias conditions and layout of designed devices, and mismatch of ideally symmetrical device due to variation of process parameters. For an untrimmed monolithic MOS opamp, the offset can range from 1 mV to 20 mV [Gray-2001]. The amplifier offset is considered a deterministic constant DC voltage, which can be removed easily by offset zeroing, trimming or subtraction method. The circuit and device noise, on the other hand, is more difficult to be eliminated as they are time varying and random in nature. In general, the noise sources are flicker noise (or $1/f$ noise) and thermal noise. There are several causes of flicker noise [Tsividis-1999] but the well-known phenomenon is the random trapping and releasing of energy state as charge carriers move along the interface between the gate oxide and the silicon substrate. This is due to the "dangling" bonds existing at the interface that gives rise to extra energy states as illustrated in [Razavi-2001]. The trapping and releasing phenomenon generates noise, of which the spectral density is inversely proportional to the frequency with the constant being process technology dependent. Since the energy of the noise concentrates more in the DC as well as the low frequency region, $1/f$ noise is considered as low frequency noise. On the other hand, thermal noise is a wideband noise with a spectral density fairly constant across

the whole frequency range (white noise) but proportional to the absolute temperature. It originates from the time varying random fluctuations of voltage across a conductor, which is mainly caused by the random motion of electrons in the conductor. Due to the time varying and random nature, noise cannot simply be solved by the offset method.

The two most promising methods to overcome amplifier offset and $1/f$ noise problems are chopper stabilization (CHS) and autozero (AZ) techniques. The solution to $1/f$ noise problem strongly depends on how well the noise reduction techniques can shape or transpose the noise out of the frequency of interest and how strong is the correlation function between the noise sample and the instantaneous noise value from which the sample is subtracted. Correlated double sampling (CDS) technique, a particular case of AZ technique, is also very effective case. Sigma-delta technique is another method, which is employed to increase resolution and to provide digital output. Brief descriptions of these techniques are as follows.

Figure 2.3.2.1: Operation principle of chopper stabilization technique

Figure 2.3.2.1 shows the basic conceptual principle of CHS operation, which was first developed by E. A. Goldberg in 1948 [Williams 1985]. The CHS technique uses a square-wave carrier V_o to modulate the change of capacitance into high frequency electrical signal. A wideband amplifier will then amplify the modulated signal V_x to the signal V_y . At the same time, the error at baseband, where there exists the amplifier dc offset error and circuit noise, are also amplified (see spectrum of V_y). The removals of the dc offset and low frequency noise are achieved by going through a demodulator (see spectrum of V_z) and a low-pass filter (see spectrum of V_{out}). At the output of the demodulator stage (V_z), the baseband error and the modulated signal are swapped in frequency domain; that is the error in the baseband is transposed to high frequency while the modulated signal is demodulated back to baseband. The error that has been transposed to high frequency is filtered in the low-pass filter and the required signal V_{out} , which reflects the change of capacitance at the input, is recovered at the output of the filter.

One of the drawbacks of the CHS technique is the operation of opamp in high frequency. The chopper amplifier has to operate at high frequency in order to amplify the modulated signal. The bandwidth is thus made high. Consequently, the complexity and the power consumption will increase while the effective gain of the amplifier will usually be lower than that of the amplifier employed in the AZ technique, which is designed to operate at low-frequency baseband. In addition, chopping frequency determines the requirements for low-pass filter (LPF), which filters the offset and the low frequency noise that have been transposed. For design consideration, there is a trade-off in terms of power consumption and chopping frequency because high chopping frequency reduces the order of filter but increasing power consumption of the chopper amplifier, whilst low chopping frequency relaxes the amplifier bandwidth but increasing the order of the LPF. For continuous-time signal amplification, the CHS technique is usually preferable.

Figure 2.3.2.2: Operation principle of autozero technique with offset and noise stored as analog form

Figure 2.3.2.3: Operation principle of autozero technique with offset and noise stored as digital form

Alternatively, the AZ technique is essentially a sampling technique, in which the input signal is not amplified to the output at some instance of time. The AZ process is split into two phases. These two phases are the sampling phase (ϕ_1) and the signal-processing phase (ϕ_2) (refer to Figure 2.3.2.2). During the sampling phase, the amplifier inputs are short-circuited and set to an appropriate common-mode voltage; in most cases, it is set to analog ground or sampling reference voltage of the sampling system. The amplifier offset (V_{os}) and noise (V_N) are then sampled and can be either stored in analog form, for example in

sample-and-hold (S/H) circuit (Figure 2.3.2.2) or digital form, for instance in successive approximation register (SAR) (Figure 2.3.2.3). It can be seen that the circuit is performing an autozero function on the offset and noise in this phase. During the signal-processing phase, the stored value in S/H or SAR is converted to an appropriate voltage to null the offset and noise, through an auxiliary nulling input port N of the amplifier. Thus, the input signal, which is now connected to the amplifier, can be amplified to the output (V_{out}) by the amplifier that is ideally free of offset and lower in noise level (within the frequency band of interest).

Nevertheless, the AZ technique suffers from two major drawbacks. The first drawback is the power consumption. The storing of offset voltage into the storage element (S/H or SAR) needs an amplifier (A_2). This is to prevent excessive loading to the output of the main amplifier. Therefore, many autozero configurations, like the "multistage offset cancellation", "offset cancellation using an additional offset nulling input", "continuous-time AZ amplifier" [Enz 1996] etc., require additional amplifiers. In similar context, digital-to-analog converter (DAC block) must be included to convert the digital data in SAR back to analog signal for offset cancellation. Consequently, with these additional amplifier and converter, the power consumption will be higher than that using just one amplifier (as discussed in the CDS technique). The second drawback is the switch injection errors. As the AZ techniques are based on switched-capacitor topology, MOS-based transistors are used to realize the switches. The major problem associated with MOS-based transistors is the switch injection errors, which are caused by charge injection and clock feedthrough errors when they are turned off. This is the most fundamental problem in switched-capacitor circuit that limits the accuracy of the circuit output. This is addressed later.

Figure 2.3.2.4: Operation principle of CDS technique (Phase 1)

Figure 2.3.2.5: Operation principle of CDS technique (Phase 2)

Similar to the AZ technique, the CDS technique is another alternative for solving offset and low frequency noise problem. The origin of the CDS technique was from [White 1974] and [Brodersen 1976] where it was developed to reduce the noise produced in charge-coupled devices. Due to its implementation effectiveness and versatility, CDS circuits are widely used in sampled-data systems [Enz 1996]. The CDS technique also operates in two phases. The phase 1 (ϕ_1) (Figure 2.3.2.4) is essentially an autozero operation. The amplifier is configured as unity-gain buffer while being disconnected from the signal path. The capacitor C is then charged up to the offset voltage V_{os} by the high gain amplifier in unity-gain configuration. As a result, amplifier offset and noise are sampled and stored in the

capacitor C . During phase 2 (ϕ_2) (Figure 2.3.2.5), the signal is reconnected to the input of the amplifier, through the capacitor, where it is amplified to the output V_{out} . The subtraction of the previously stored offset and noise in the capacitor with those during the amplification will make the output to be ideally free of error in ideal case.

In comparison, there are two main differences between the CDS and the AZ technique. First, offset and noise errors in the CDS technique are stored in capacitor instead of S/H or SAR. Second, the CDS essentially converts the output into a S/H configuration and the cancellation of errors is performed by the capacitor rather than nulling the error through auxiliary nulling input port of the amplifier. The later difference has made the CDS technique very versatile in sampled-data system implementation. One practical issue concerning CDS is the requirement for high slew-rate and fast settle amplifier because the output signal is slewed back and forth between the amplified input signal and the sampling reference voltage. However, by using an improved CDS topology, this can be solved. It is noted that the effect of CDS on errors is very similar to the AZ technique [Enz 1996], of which both have the similar noise shaping response. The following is a comparison of the noise shaping property of chopper stabilization and AZ / CDS technique.

Figure 2.3.2.6: Comparison of noise shaping property [Hsieh 1981]
 (a) Generic equivalent noise model for both CHS and CDS,
 (b) CHS noise shaping of equivalent input noise spectrum,
 (c) CDS noise shaping of equivalent input noise spectrum

Figure 2.3.2.6(a) shows the generic equivalent noise model for both CHS and CDS (or AZ technique). The noise source $\overline{V_{neq}^2}$ represents the equivalent input noise model for each of the CHS and CDS technique while the amplifier is noiseless with gain of a . Figure 2.3.2.6(b) displays the equivalent input noise spectrum of the CHS technique. The $1/f$ noise component is transposed to odd harmonic frequencies of the chopping waveform [Hsieh 1981]. However, there exists some "fold-back" noise from the transposed $1/f$ noise harmonics at low frequencies. In order to reduce this "fold-back" noise, the chopping frequency has been made higher than the signal bandwidth. Figure 2.3.2.6(c) shows the

equivalent input noise spectrum of the CDS and the AZ technique. In contrast to the CHS technique, the efficiency of the CDS (or AZ) technique for the low-frequency noise reduction depends greatly on the autocorrelation between the noise sample and the instantaneous noise value from which it is subtracted. It is noted that the technique is more efficient for the $1/f$ noise than the wideband thermal noise as the autocorrelation between two samples of $1/f$ noise is better [Enz 1996]. Nevertheless, the technique is very effective in low frequency region of the spectrum because it imposes a zero at the origin of the spectrum [Krummenacher 1982] to eliminate any noise appearing at frequency 0 Hz, which cancels amplifier offset, and reduces noise at low frequency. The detailed analysis of CHS and CDS noise cancellation properties can be referred to [Kansy 1980], [Hsieh 1981], [Krummenacher 1982], [Wey 1986] and [Enz 1996]. It can be concluded that the improved CDS is attractive for applications that require high resolution without substantially increasing the power consumption.

Another technique that has noise shaping capability is sigma-delta ($\Sigma\Delta$) modulator [Norsworthy 1989], [Aziz 1996]. Sigma-delta analog-to-digital converter (ADC) is employed in the form of closed-loop system. They are mainly used to increase the resolution as well as to provide digital output. The basic working principle (Figure 2.3.2.7) [Norsworthy 1989] is to oversample the analog input signal at a rate (f_s) many times greater than the signal Nyquist rate (f_N) in the analog noise-shaping modulator. In this way, the analog signal is pulse density modulated into a digital 1-bit stream, that is, the density of the output pulses over a given period is approximately equal to the mean value of the analog input over the same period. Inherently to its modulator structure, it is able to shape the quantization wideband noise power, which is injected by its own quantizer (Figure 2.3.2.8) [Aziz 1996], over a bandwidth much larger than the signal band. The 1-bit output stream is subsequently low-pass filtered digitally to remove out-of-band noise.

Figure 2.3.2.7: Basic working principle of a sigma-delta ADC

Figure 2.3.2.8: Basic working principle of a first-order sigma-delta ADC

Figure 2.3.2.8 shows the basic structure of a simple 1-bit sigma-delta ADC. It comprises an integrator, a quantizer and a digital-to-analog converter (DAC). The integrator integrates the difference between the sampled analog signal $x[n]$ and the quantized analog signal $y_a[n]$. Operating on the same oversampling frequency, the quantizer converts the integrated difference into a digital bit stream output that represents a pulse density modulated signal. The digital bit is then fed back to the input in analog form through a DAC. The major issue in designing the sigma-delta ADC for sensor interface is the stability problem [Hein 1993], [Baird 1994], caused mainly by process variation. It is also common to observe that this type of ADC exhibits higher power consumption [Lemkin 1999] and demands complicated digital compensation circuit [Yazdi 1999].

The noise shaping properties of sigma-delta ADC depends on three main design parameters, oversampling rate, order of modulator and bit-order of quantizer. The performance of the noise shaping response will improve by increasing any of the three design parameters, or a combination of them. This will lead to an increase of the signal-to-noise (SNR) of the system. The noise transfer function of the 1-bit first-order sigma-delta modulator is essentially a first-order differentiation function in discrete-time domain (Z -

domain). The noise response of this first-order differentiation operation in frequency domain is a linearly increasing function with respect to the increase of frequency. This is generally not effective to shape most of the in-band noise [Boser 1988], [Candy 1981] out of the signal bandwidth. Therefore, better performance of sigma-delta ADC is required. However, increasing oversampling rate will push operating frequency of the integrator amplifier higher, whilst increasing the order of the modulation will add more integrator stages, which increases the number of integrator amplifiers. Although the performance can be improved through increasing the bit-order of the quantizer to multi-bit quantizer, the complexity of the DAC will increase. Furthermore, decimator and digital filter are required to filter out-of-band noise. Therefore, increasing any of the design parameters and the need for digital filter will lead to increase of power consumption.

Although the CDS technique can minimize the offset and noise with low power consumption, it suffers from the switch injection errors, which greatly limit the resolution. These non-ideal switch errors, namely charge injection error and clock feed-through error, are inherent in all switched-capacitor networks and sampled-data circuits. The causes for their existence are the dumping of stored channel charges and the coupling of clock voltage into the high impedance node, for instance the input of opamp, at the moment when the switches are closed. These errors are very difficult to eliminate simultaneously in signal-ended structure. Nevertheless, there are very few methods to counteract them.

The popular methods are classified as CMOS (complementary metal-oxide semiconductor) switch topology [Eichenberger 1991], half-size dummy switch topology [Eichenberger 1990] and fully differential switch structure [Enz 1996]. For CMOS switch topology, it is not so effective because the matching characteristic between NMOS (n-type MOS) and PMOS (p-type MOS) transistors is poor. Although dummy switch topology is more effective than CMOS switch, it greatly depends on matching degree between the half-size dummy transistor and the main transistor in layout. As their sizes are different, the matching performance tends to be poor and they are most often sensitive to variation of process parameters. On the other hand, the fully differential structure is effective, conceptually, to reject the errors in the form of common-mode signal cancellation. However, it depends on the symmetry of differential structure and requires fully differential opamp to perform the cancellation. This gives the price of increasing complexity of circuit, power consumption and matching degree among component pairs in layout.

The second issue is that of the power dissipation by the circuit devices, which has been stressed extensively in the first issue. A simple circuit with fewer components normally consumes relatively lesser power than that of complicated circuit topologies. It is common to observe that a fully differential opamp demands higher power than a single-ended opamp. Therefore, sensing schemes, such as chopper stabilization technique that requires high-bandwidth opamp, sigma-delta technique that requires high-speed opamp, and fully differential switch technique that requires differential opamp, are not suitable for implementation of low-power front-end sense amplifier.

The third issue is the simplicity of incorporating self-test function. Self-test operation is related to the functional check on the accelerometer system in automotive application. Therefore, the ease of inserting self-test feature without affecting the normal operation of the accelerometer is important for designing the sense amplifier. Depending on how the sensor and the sense amplifier are being configured, some topologies do not allow the insertion of self-test (has been discussed in previous chapter). This is especially common in the closed-loop force-balanced topologies. Therefore, an open-loop configuration is focused in this project for implementing the self-test function.

Based on the three issues, comparison of previous works on sensor interface is shown in Table 2.2.2.1. In the case of [Kuehnel 1994], [AD 1996], [Chau 1996], [Wu 2004], higher power is consumed using the CHS technique as compared to the CDS technique in [Kulah 2000], [Motorola 2001]. Of particular interest, the expected high power consumption stems from the BiCMOS circuitries employed in [Kuehnel 1994], [AD 1996], [Chau 1996]. As in the case of sigma-delta modulator, a 2nd-order modulator [Lemkin 1999] dissipates more power than a 1st-order modulator [Kulah 2000]. Moreover, these sigma-delta modulator structures do not provide self-test function. Therefore, the goal of the thesis is to realize a low-power sense amplifier whilst meeting multiple design objectives. These include effective minimization of opamp offset, low frequency noise and switch injection errors and incorporation of on-chip economical self-test circuit.

Table 2.3.2.1: Comparison of sensor interfaces

Reference	Technique	Output Noise Root Spectral Density	Area and Technology	Power Dissipation	Self-test Function
[Kuehnel 1994]	Fully-integrated, Closed-loop, CHS using high bandwidth fully differential amplifier	98 $\mu\text{V}/\sqrt{\text{Hz}}$	3 x 3 mm ² (3 μm BiCMOS process for circuitry)	50 mW (10 mA at 5 V)	Yes
[AD 1996] ADXL50	Fully-integrated, Closed-loop, CHS using high bandwidth fully differential amplifier	125 $\mu\text{V}/\sqrt{\text{Hz}}$	—	50 mW (10 mA at 5 V)	Yes
[Chau 1996]	Fully-integrated, Closed-loop, CHS using high bandwidth fully differential amplifier	120 $\mu\text{V}/\sqrt{\text{Hz}}$	3 x 3 mm ² (3 μm BiCMOS process for circuitry)	40 mW (8 mA at 5 V)	Yes
[AD 1998] ADXL150	Fully-integrated, Open-loop, CHS using high bandwidth fully differential amplifier	38 $\mu\text{V}/\sqrt{\text{Hz}}$	—	9 mW (1.8 mA at 5 V)	Yes
[Lemkin 1999]	Fully-integrated, Closed-loop, 1-bit 2 nd -order $\Sigma\Delta$ modulator, charge integrator using fully differential amplifier	4.4 $\mu\text{V}/\sqrt{\text{Hz}}$ (x-axis) 6.4 $\mu\text{V}/\sqrt{\text{Hz}}$ (y-axis) 39.6 $\mu\text{V}/\sqrt{\text{Hz}}$ (z-axis)	4 x 4 mm ² (2 μm CMOS MEMS process)	135 mW (27 mA at 5 V for 3 axes) 45 mW (9 mA at 5 V for 1 axes) excluding digital filter	No
[Kulah 2000]	Two-chip, Closed-loop, 1-bit 1 st -order $\Sigma\Delta$ modulator, CDS front-end charge integrator	110 $\mu\text{V}/\sqrt{\text{Hz}}$	3.4 x 3.6 mm ² (3 μm CMOS process)	7.2 mW (1.44 mA at 5 V) excluding digital filter	No
[Motorola 2001] MMA2202D	Two-chip, Open-loop, CDS	110 $\mu\text{V}/\sqrt{\text{Hz}}$	—	25 mW (5 mA at 5 V)	Yes
[Wu 2004]	Fully-integrated, Open-loop, CHS using high bandwidth amplifier	6.5 $\mu\text{V}/\sqrt{\text{Hz}}$	3.5 x 2.5 mm ² (0.5 μm CMOS MEMS process)	30 mW (6 mA at 5 V) excluding differential-to-single-ended amplifier and off-chip components	No

2.4 Review of Signal-Conditioning Circuits

2.4.1 Gain Stage

The acceleration sensor parameters are highly sensitive to random process variations. As a result, capacitance between sensing plates and sensitivity of moveable plate of a differential-capacitive sensing element can vary over a wide range of values after fabrication. Ideally under zero acceleration, the middle moveable plate is nominal at mid-way between the two fixed plates. However, the variation of sensor parameters will cause the middle plate to deviate from the nominal position as well as the nominal sensitivity. This will create a constant difference in capacitance value between C_{S1} and C_{S2} (from Equation (2.3.1.6) and Equation (2.3.1.7)), which can be denoted as a systematic offset, and a change in sensitivity parameter. They can be represented as follows:

$$C_{S1} = (1 + \alpha)C_o + (1 - \beta)\Delta C_s \quad (2.4.1.1)$$

$$C_{S2} = (1 - \alpha)C_o - (1 - \beta)\Delta C_s \quad (2.4.1.2)$$

where α is the offset error and β is the gain error.

Therefore, the important role of the gain stage is to correct these anomalies before the signal goes into the filter stage. The most convenient way is to incorporate trimming circuits, for both gain and offset. Since the gain stage gets its input from the output of the front-end sense amplifier, the major concern is the small input voltage, whose amplitude is usually below 0.5 V. As a result, opamp offset and low-frequency noise become the dominant factors that determine the performance of gain circuit when inserting trimming circuits.

Several techniques for gain circuit have been reported. The active-RC gain circuit [Martin-1997] in Figure 2.4.1.1 is an example of continuous-time gain stage. The gain factor K can be adjusted via the ratio of component values. However, it may not be an appropriate choice because it has no provision to reduce the opamp offset voltage and $1/f$ noise, instead it amplifies them. On the other hand, in terms of compatibility to the switched-capacitor sense amplifier, a switched-capacitor gain stage is often preferred. One of the earliest SC gain circuits, as shown in Figure 2.4.1.2 [Foxall 1980], utilizes SC approach, where the two resistors in Figure 2.4.1.1 have been replaced by their SC equivalents. The advantages are that it does not incur large slew-rate requirement on the opamp and its output is a quasi-analog waveform. However, this approach will amplify offset and noise to the output. As already discussed in the previous section, these shortcomings can be overcome by CDS technique. The conventional gain circuit using CDS technique is depicted in Figure 2.4.1.3 [Gregorian 1981]. The operation of the circuit is briefly described as follows. During the clock phase T_2 , the inverting input of the opamp is connected to the output voltage V_{out} and to one end of capacitors C_1 and C_2 . The other ends of the capacitors are connected to ground. Therefore, the voltages of V_{out} across the capacitors are equal to the opamp offset voltage at the end of the phase. During T_1 , input V_{in} is connected to C_1 whilst V_{out} is connected to C_2 . In this configuration, by conservation of charges, it can be shown [Martin-1997] that at the end of phase T_1 , the output voltage is independent of the opamp offset voltage. In addition, due to CDS structure, the $1/f$ noise can also be reduced. The major drawback of this scheme is that the output voltage is reset to ground voltage on T_2 . It has to slew between the ground during T_2 and the amplified output during T_1 . The opamp is demanded with large slew-rate values and fast settling time. Another drawback is that of the switch injection errors created during turning MOS-based switch S_1 off. This limits the accuracy of the output.

Figure 2.4.1.1: Continuous-time active-RC gain circuit

Figure 2.4.1.2: Switched-capacitor active-RC gain circuit [Foxall 1980]

Figure 2.4.1.3: Conventional switched-capacitor gain circuit [Gregorian 1981]

Figure 2.4.1.4: Conventional switched-capacitor capacitive-reset gain circuit [Haug 1984]

In order to solve the high slew-rate problem, the capacitive-reset gain circuit shown in Figure 2.4.1.4 was proposed [Haug 1984]. The feedback reset switch S_1 is replaced by a S/H circuit, consisting of holding capacitor C_3 , switches S_2 and S_3 . The capacitor C_3 eliminates the output voltage from resetting to ground and to ensure that the output voltage changes as little as possible between clock phases, in every clock period. In addition, the structure also reduces the finite gain error of opamp. Hence, this relaxes the opamp specifications on slew-rate parameter, settling time and open-loop gain. Another advantage is its simplicity in design. The circuit can be easily configured as a summing amplifier. This benefits the addition of offset trimming circuit, in which the offset trimming network can be connected to the inverting input of the opamp. Although the switch injection errors

are still the major problems, an improved differential-to-single-ended structure in Figure 2.4.1.5 was reported [Martin 1987] for reducing these errors. The capacitors and switches that are connected to the non-inverting input of the opamp are correspondently identical to those connected to the inverting input. The idea is to subtract the switch errors, which are in the form of common-mode components similar to differential scheme. However, this circuit increases the area utilization, potential switching noise and the matching requirement on capacitor pairs. Moreover, when offset trimming circuit is added, the compensation will not be effective, as the impedances would be disturbed further. Based on these observations, the design objective is to devise a gain circuit that is simple, low power and small area, but yet effective in minimization of switch injection errors.

Figure 2.4.1.5: Differential-input switched-capacitor capacitive-reset gain circuit [Martin 1987]

2.4.2 Filter Stage

The main purpose of the low-pass filter (LPF) stage is to remove out-of-band noise. The filter stage also defines the bandwidth of the accelerometer system. Since the response of the mechanical sensor is of low frequency, the bandwidth of the accelerometer is designed low, popularly at 1kHz in many implementations. However, the low system bandwidth imposes a practical implementation problem on the integrated filter design. That is, the component values tend to be large because the cutoff frequency is reciprocal to RC time constant (the product of resistance R and capacitance C value). For example, the time constant for 1 kHz cutoff frequency is about 0.16 ms in a first-order filter, which requires the resistance value of mega-ohms and capacitance of hundreds of pico-farads. Hence, it is impractical and not cost-effective to integrate such large values of the resistance and capacitance because they can occupy, for instance a few hundreds of square micrometers of silicon area in a standard 0.6 μm CMOS process. Moreover, the thermal noise generated by resistors of more than mega-ohms range has significant effect on the noise performance of circuit.

To solve the large time constant problem, a promising approach is to utilize switched-capacitor filter [Gregorian 1983]. This is because analog switches combined with small capacitors (in SC filter) can replace the resistors of large values (in continuous-time filter) to realize very low cutoff frequency without consuming large area. The equivalent resistance value is the reciprocal of the product of sampling frequency and capacitance value, that is, $R_{eq} = \frac{1}{f_s C}$. For fixed sampling frequency, the higher the resistance value to be realized, the smaller is the capacitance. This improves the area efficiency but the trade-off is higher mean-squared value of capacitor noise, KT/C [Castello 1985]. To reduce the

noise impact, the gain stage preceding the filter should have as high gain as possible on the signal.

Another consideration is to keep the signal integrity so that the filter will not degrade the acceleration response. This is particularly important for automotive air-bag application to accurately pinpoint on crash situation. To achieve that, the filter is preferred to have linear-phase characteristic. This is because when all frequency components are delayed equally, the signal will be delayed without distortion, resulting in magnitude being constant [Valkenburg-1982].

Among the popular analog filter approximation to the ideal rectangular low-pass filter (LPF) response, Bessel-Thomson polynomial approximation is preferred over that of Butterworth and Chebyshev [Leib 1992] as it is considered as a linear-phase filter [Valkenburg-1982], [Allemandou 1966]. Another distinguish merit of the Bessel-Thomson (or simply Bessel) filter is its absence of overshoot property [Valkenburg-1982]. Under a time-step response, unlike other filter approximations, Bessel filter does not exhibit any overshoot, which displays a good settling behavior. The overshoot is not desirable in the air-bag application because it may cause system false triggering. In addition, Bessel filter has been identified to be more robust against sampling clock jitter on sampling system implementation than Butterworth and Chebyshev approximations [Leib 1992].

The drawback of Bessel filter is that it has lower roll-off rate in the stop band as compared to that of Butterworth-type. This requires the increase of filter order. For this reason, power consumption becomes another important issue for the filter stage. The higher the order of active filter, the more number of filtering stages are to be designed. This is translated to more number of opamps required. Besides, Gaussian-type approximation filter is excluded. It may not be suitable for integrated implementation because it demands huge number of

components for realizing the infinite delay property [Klapper 1959], despite having linear-phase property.

The final issue is concerned with filter topology. Power consumption has great impact on the choice of appropriate topology. Popular filter topologies can be found in [Schaumann-1981], [Valkenburg-1982], [Moschytz-1984], [Franco-1998]. In particular, biquad [Lee 1971], [Lee 1971a] and Sallen-Key [Balabanian 1963], [Moschytz 1967], [Moschytz 1972], [Moschytz 1973] topologies are commonly used. The advantage of using biquad is that each opamp is connected in inverting configuration (Figure 2.4.2.1). Although it avoids common-mode design issue, the number of opamps per filter stage becomes comparatively larger. Hence, this thesis focuses on the topology that has the least number of opamps required to realize high-order filter for low-power and area-efficient implementation. Sallen-Key filter is identified as the potential topology because it needs only one opamp (Figure 2.4.2.2) to realize a second-order or third-order filter. Despite its power and area efficiency, it may suffer from common-mode input range problem on the basis of non-inverting configuration. This problem can be resolved via appropriate signal scaling for each building block in the system.

Figure 2.4.2.1: Basic second-order biquad filter

Figure 2.4.2.2: Basic second-order Salley-Key filter

2.4.3 Output Stage

The signal after the filter stage is trimmed by the output stage to give a maximum acceleration range. The output stage aims at scaling the output voltage to the required specification and driving external loads. Therefore, it has to provide calibration for both gain and offset. Moreover, it is required that the output to be in continuous form to maintain signal fidelity and integrity. For this reason, the output stage often employs continuous-time amplifier with ratio-metric resistor network. The opamp offset and low frequency noise are not major concern here since the input signal is large.

The design of scaling amplifier has the following two issues. First, it must provide a rail-to-rail output voltage swing without degrading linearity of output signal. The aim of maximizing the output voltage swing is to maximize the sensing dynamic range. However, the saturation voltage requirement of output transistors limits the maximum possible voltage range. In addition, there is degradation of linearity in the amplification when the output swing is close to the supply and ground constraints.

Second, the integrated scaling resistors should be of good matching whilst not occupying large silicon area. To get an accurate resistance value with good matching, the layout of the resistor using polysilicon with broad width is employed. However, the unit resistance of polysilicon (resistance per square) is small, usually about 30 to 50 ohms/square $\pm 10\%$ to 20% . Due to wide trimming range, spread of resistance values is wide. This imposes some integration problems. For large resistors to be realized using polysilicon, the area occupation will be very large and hence not cost-effective. For small resistors, on-resistance of trimming analog switches may have significant effect on their accuracy. This is due to the analog switches being connected in series with them in the trimming circuit

for simplicity purpose. As a result, the on-resistances of the switches are added to the corresponding trimming resistance values. This may be a serious problem if the switch resistance is comparable or higher than the trimming resistance value with the switches being designed to be of minimum size for minimizing area utility. Thus, with compromising area, the sizes of the switches have to be increased until its on-resistance is within the tolerable range. Taking into consideration of the above issues, the design of the output stage will focus on area-efficient, rail-to-rail amplifier output stage design combined with gain and offset trimming circuits for continuous-time signal processing.

2.5 Review of Clock Generator Circuits

To achieve the fidelity in switching between phases in SC circuits, the clock generator plays a very important role. It is responsible for the clocking and synchronization of all switches in the SC circuits. It also ensures that there is no cross switching. In this way, switches of different phases will not be turned on at the same instant of time. Otherwise, momentary shorting of power supply terminals may occur, which can draw large surge current from supply to ground. This is hazardous to both the circuit and external devices. Therefore, there is a need for generating non-overlapping clock signals [Martin-1997] to provide multiple switching phases. This adds constraints to the clock generator design. The on-chip clock generator with incorporated oscillator is preferred over the off-chip counterpart for most sensor applications. Although the off-chip solution can provide the flexibility in implementation, it consumes higher power and requires longer distribution distance [Nilsson 1996] on printed-circuit-board (PCB). In addition, external components and circuitries are required, which defeat the purpose of integrated ASIC. In contrast, the integrated clock generator has the advantage of localized connection that minimizes the total loading capacitance for all the clock signals. However, on-chip integration of clock generator encounters many issues. The first issue is jitter [Weigandt 1994], [McNeill 1997], [Hajimiri 1999], [Herzel 1999] and phase noise [Razavi 1996], [Hajimiri 1998], [Lee 2000], [Dai 2002] in oscillator. Jitter in oscillator is defined as the deviation of signal period to its mean period while phase noise can be quantified by the bandwidth of offset frequencies with respect to its ideal oscillation frequency. The two parameters are distinguishable by different domains, as the jitter is treated in time domain while the phase noise is determined in frequency domain. However, the two sources are often indistinguishable as they are both caused by supply noise, substrate noise and circuit noise. Nevertheless, both of them have significant effects on sampled-data systems [Shinagawa

1990], [Leib 1992], especially on switched-capacitor circuits [Beex 1992], because they will increase the output noise level. The second issue is area consumption. For practical sensor application, the sampling frequencies of SC circuits are often chosen between few tens of kilohertz to few megahertz in order to prevent capacitive leakage from allowable low frequency, and to relax the amplifier from high slew-rate and fast settling time based on the maximum frequency constraint. With this range of clock frequencies, the design of oscillator will require large values of components, especially those of capacitances. This imposes limitation on silicon area utilization. The third issue is that of power dissipation [Chandrakasan 1992]. Therefore, the constraints on jitter and phase noise, with reference to area and power dissipation, pose a challenge on the design of small-area and low-power oscillator.

There are mainly two design methodologies for clock generator, the analog and the digital design methodologies. Phase-locked loops (PLL) [Jeong 1987], [Young 1992], [Alvarez 1995] and delay-locked loops (DLL) [Welti 1994], [Christiansen 1996] belong to the analog type. They are very popular in telecommunication systems for designing clock-recovering circuits and frequency synthesizers. The reason is that they can provide low-jitter and low-phase noise solution to high frequency or high-speed circuit applications. However, they are not suitable for low frequency sensor applications for the following reasons. First, integrating PLL and DLL in sampled-data system or digital system are expensive. As operated in mixed-signal nature, PLL and DLL techniques are very susceptible to switching noise [Young 1992], [Mu 1999] and process variations [Nilsson 1996]. Other methods utilize quartz reference voltage-controlled oscillators on PLL for better frequency stability [Giebel 1989] but they are not suitable for integration in CMOS process. Secondly, PLL and DLL feedback loops are more complicated in design since they involve many sub-modular circuits. The power consumption of the PLL or DLL technique

becomes much higher than that of the digital counterpart. Furthermore, the development time for the analog techniques is longer, which will lead to higher cost of products. In contrast, the digital techniques are simple, robust and more suitable for both low-cost and low-power clock generations. The conventional digital method is to employ a ring oscillator. The method offers a design that is simple and robust. However, it has problems in jitter and phase noise since it is subject to power supply variation. Moreover, for low frequency generation, the capacitance values tend to be large, imposing additional problem on area utilization and cost. More importantly, the rising and falling edges of clock signals are not sharp due to sinusoidal nature of node voltages in ring oscillator. This is critical for proper digital operation because long rising and falling clock transition time will increase short-circuit current, and hence, the dynamic power dissipation in digital circuits [Chandrakasan-1996]. Based on these observations, another goal of this project is to devise a low-cost, low-jitter and small-area oscillator for use in integrated sensor applications.

2.6 Review of Trimming Circuits

On-chip calibration circuit is important for post-installation adjustments of accelerometer system. The reasons for the need of post adjustment is firstly to compensate device parameters deviations caused by variation in process parameters, secondly to adjust accelerometer system parameters for normal operation, and thirdly to provide flexibility of programming the system to suit different user requirements. In a wider perspective, it increases the yield of the product. However, this comes at the expense of increased area, power consumption and price of product. Most importantly, the reliability of the trimming technique has great impact on the success of final product.

The popular types of trimming techniques are laser trimming [Brokaw 1996], [Deluca 2002] floating-gate trimming [Säckinger 1988], [Carley 1989], [Tschan 1995], Zener-zap trimming [Price 1965], [Erdi 1975] and fusible link trimming [Schroeder 1977], [Mok 1995], [Kokkonen 1981], [Metzger 1983]. Laser trimming technique has the advantage of trimming component parameters accurately as it applies active trimming (feedback trimming method) in which an output is continually monitored while trimming is performed and stopped as soon as the output reaches a certain level. In other words, ideally it can precisely scale the size of components, which are mainly thin or thick film resistors, to their exact required values because of continuous nature of the process. In addition, it does not need any extra trimming circuitry added onto the chip, thus saving area and power. However, the technique suffers from localized heating, caused by prolonged heating-effect of laser, that not only affects stability of trimmed resistors but also neighbor sensitive circuitries [Price 1976]. This localized heating changes the characteristics of the resistors, such as sheet resistance and temperature coefficient, and worst of all, degrades the aging [Bulger 1975], [Angulo 1987], [Angulo 1988]. Therefore, the product may suffer

from serious reliability problem. Moreover, the technique is expensive as it relies heavily on accuracy, precision and stability of the laser equipments. In addition, extra cost is required to deposit film resistors on standard analog CMOS process. Hence, this incurs higher cost on the products.

Floating-gate trimming technique employs floating-gate elements to store appropriate charges so as to obtain the required trimming conditions. It can achieve continuous trimming value by controlling the amount of charge stored on the floating-gates. The floating-gate structure can also be applied to electrically erasable programmable read-only memory (EEPROM) for storing digital trim data [Tarui 1972], [Harrison 2001]. Although the technique has advantages of re-programmability and achieving precise trim values, it has its own drawbacks. Firstly, floating-gate element belongs to the class of programmable nonvolatile semiconductor memory, which requires special fabrication steps for producing the floating-gate structure. This is usually not included in standard analog CMOS process. Thus, additional requirement has to be made to include fabrication of the floating-gate elements that will result in increase of production cost. Secondly, the programming of charges on the floating-gate is accomplished by applying high supply voltage across the gates, which often exceeds ten volts [Säckinger 1988]. For this reason, protective circuitry must be included on the chip to prevent the high voltage injection from damaging other parts of the system during programming. This may take up significant amount of silicon area. Thirdly, as the floating-gate is capacitive in nature, it suffers from leakage problem [Manabe 1999], especially for those that demand precision charges to be stored. Charges that are programmed into the gate will leak away through time. Such leakage problem may reduce the product reliability.

The Zener-zapping is a process of shorting diodes to achieve short-circuited condition between terminals of diodes. During the process, a large reverse current is supplied into the diode to attained Zener avalanche-mode that makes the diodes break down. The method was first proposed in [Price 1965] and later extended to bipolar transistors [Erdi 1975]. It was popular in the early stage during which bipolar and bipolar-FET processes were proliferating [Erdi 1979], [Menniti 1984], [Pease 1984], [Gariboldi 1987].

Zener-zap trimming technique is essentially a discrete-type, rather than continuous-type trimming method, which either connects or shorts the components that are connected in parallel to the diodes. Although the technique requires some silicon area for the implementation of diodes or bipolar transistors, the advantages are that it does not require extra fabrication process steps for bipolar process, and selective short-circuiting procedure of diodes can be performed at the wafer test phase. This technique offers a lower cost solution than the two preceding techniques. However, the technique is considered a bipolar version of one-time programmable read-only memory [Ichikawa 1996], hence, it is not suitable for standard CMOS process. Moreover, for low-cost and low-power solution, the direction is to move towards using standard CMOS circuits rather than the more expensive and higher power consumption type such as bipolar or bipolar-CMOS circuits. Furthermore, the zapping voltage that is required to achieve thermal breakdown of diodes is high, usually more than ten volts. Therefore, careful considerations on the diode connections have to be taken in order not to affect other parts of the circuit during programming. Another important weak point for Zener-zap technique is that the trimming is carried out during wafer fabrication stage by using wafer probes to access individual zapping points. For off-wafer trimming (trimming is to be done after the chip has been fabricated), it is very difficult because the zapping diodes or transistors are in parallel connection [Erdi 1975]. Therefore, more package pins have to be dedicated for trimming to

access the zapping points, see Figure 2.6.1. As number of pins is limited by the package perimeter, which grows as the square root of die area [Harrison 2001], it is not feasible and is also costly to pull all the zapping access point out to pins. Consequently, this technique is not suitable for one-chip calibration solution where trimming is to be executed off-wafer.

Figure 2.6.1: Zener-zap circuit in [Erdi 1975] showing parallel connection of base-emitter diodes and zapping access points

In contrast to Zener-zapping, the mechanism of trimming fusible link (or simply, fuse) is to drive a sufficiently large current so to blow the link. The blown link presents an open-circuited connection cutting-off any current passing through the link. Hence, fusible links are mainly serial-connected and the technique is considered a discrete-type trimming method [Kim 1998] (see Figure 2.6.2).

Figure 2.6.2: Unit trimming circuit in [Kim 1998] showing serial connection of fuse

Fusible link technique is a promising method for on-chip calibration circuit because of several reasons. Firstly, it is a small-area implementation. The area occupied by a single fuse is often the minimal as the width must be made narrow for ease of blowing in order to reduce programming time as well as programming current. Secondly, it offers a lower-cost and lower-power trimming solution [Fuller 1994] than the bipolar Zener-zap technique because it is fully compatible to standard CMOS process. Thirdly, it provides flexibility for different implementation of fusible link elements to suit required applications. For instance, other than typical polysilicon, elements can be of Arsenic-doped polysilicon to

reduce the programming voltage and current [Tanimoto 1982], or of Nichrome material for radiation hardening in space application [Fuller 1994], or of aluminum material for power devices [Venkatraman 1996], [Venkatraman 1996a]. Fourthly, it is well suited for off-wafer trimming. The serial-connection property of the fusible links makes it easy to implement fuse branches that can be blown individually. It is also the reason for popularity of fuse trimming technique in digital implementation [Schroeder 1977], [Kokkonen 1981], [Metzger 1983], [Mok 1995]. However, the major problem is the regrowth of fuse due to electromigration and thermal expansion under environmental temperature effect after the fuse has been blown [Erdi 1975]. This gives a problem on reliability of the product. In addition, as the fusing current is large, the programming voltage can be high, which can cause the same adverse effect as mentioned in the Zener-zap technique. Arising from this survey, this thesis is focused on investigating a reliable trimming method for use in the accelerometer system IC.

CHAPTER 3

Accelerometer Sensor Modeling

3.1 Overview

Sensor modeling is an important step prior to performing any simulation. A good model will bring the designer closer to the real-world situation. This is especially important in the accelerometer design because a good acceleration sensor model will command a higher rate of success and shorten the time-to-revenue of the final products. Analog circuit designers prefer electrical sensor model because the results generated by electrical simulator, like Spice, are widely accepted. Moreover, the cost of utilizing the electrical simulator is much lower than those mixed-signal simulators having mechanical and electrical simulation capabilities.

This section first covers the background of acceleration sensor structure and the problems involving modeling of practical acceleration sensors. It gives a brief introduction of the prior-art works of acceleration sensor modeling. A new electrical sensor model, which encompassed the practical acceleration sensor parameters, is then proposed. A comparison between the prior-art works and the proposed model is summarized. Lastly, the use of model to predict leakage issue in a practical acceleration sensor is presented.

3.2 Review of Acceleration Sensor Modeling Methods

3.2.1 Background of Acceleration Sensor Structure

Figure 3.2.1.1 shows the plan view of a typical micromachined capacitive acceleration sensor while Figure 3.2.1.2 shows the cross-section view of the sensing element structure for one finger. From Figure 3.2.1.2, the movable conductive plate is held in between two fixed conductive plates, top plate and bottom plate, forming two capacitors, one between the moving plate and top plate (C_1) pair and the other between the moving plate and bottom plate (C_2) pair. The movable conductive plate and the fixed conductive plates are fabricated using polysilicon. These polysilicon plates are fabricated on top of silicon dioxide with silicon substrate as base material. Typically, the total number of fingers' pair in the sensor structure is 58 and the length of the fingers L_f is 250 μm . See Appendix A for more details on the typical dimensions of the sensor structure. An equivalent electrical model of the sensor structure is shown in Figure 3.2.1.3. C_{S1} is the capacitance sum of all the fingers' capacitor C_1 in the sensor structure while C_{S2} is the capacitance sum of all the fingers' capacitor C_2 . Under the influence of acceleration, the moving plate, which is anchored at the tether on both ends, will move left or right in a spring manner depending on the direction of the acceleration. It will then alter the distance between the pairs of plates and produce a differential change in the sensing capacitance of C_{S1} and C_{S2} . This means that if C_{S1} is increased by an amount of capacitance, C_{S2} will be decreased by the same amount, and vice versa. As can be represented in Figure 3.2.1.3, the top and bottom plates together with the movable plate form a differential sensing capacitor. Through detecting this difference in capacitances, the acceleration can be obtained.

Figure 3.2.1.1: Plan view of capacitive micromachined acceleration sensor

Figure 3.2.1.2: Cross-sectional view of capacitive sensing element in one finger

Figure 3.2.1.3: Simplified equivalent differential sensing capacitance

3.2.2 Background of Acceleration Sensor Modeling

Figure 3.2.2.1: Conceptual diagram of an acceleration sensor

Figure 3.2.2.1 shows the conceptual diagram of an acceleration sensor that describes the mechanical movement of proof mass¹ m , having a mechanical damping factor b , and a spring constant k_s . The displacement of the mass, x , that resulted from an external force, F_x , can be expressed using the differential equation as follows:

$$F_x = m \frac{d^2x}{dt^2} + b \frac{dx}{dt} + k_s x \quad (3.2.2.1)$$

Assuming m , b , k_s do not change with time, hence, the transfer function of the displacement to force can be transformed to s-domain as

$$\frac{X(s)}{F_x(s)} = \frac{1}{m s^2 + b s + k_s} \quad (3.2.2.2)$$

¹ **Proof mass:** A predetermined test mass in a measuring device or machine, such as in acceleration measurement equipment that serves as the reference mass for the quantity to be measured.

Since force is equal to the product of mass m , and acceleration a , the sensitivity function can be described as a second-order system function as follows.

$$H(s) = \frac{X(s)}{A(s)} = \frac{m}{k_s} \frac{\frac{k_s}{m}}{s^2 + \frac{b}{m}s + \frac{k_s}{m}} = K \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (3.2.2.3)$$

The second-order transfer function of the proof mass displacement x , over the external acceleration a , has a natural resonance frequency of $\omega_n = \sqrt{\frac{k_s}{m}}$, a damping factor of

$$\xi = \frac{1}{2}b\sqrt{\frac{1}{mk_s}}, \text{ and a sensitivity of } K = \frac{m}{k_s}.$$

Capacitance to Displacement Relationship

Referring to Figure 3.2.1.3, the equation for the differential capacitance C_{S1} and C_{S2} with small change of distance x (when the moving plate of the sensor is displaced) can be expressed as

$$C_{S1,S2} = \frac{\varepsilon A}{d \pm x} \quad (3.2.2.4)$$

where ε is the permittivity of the dielectric, A is the effective area and d is the nominal cavity distance. The sign $\pm$ means that when the plate C_{S1} displaces $+x$ value, the plate C_{S2} displaces $-x$ or vice versa, depending on the direction of the middle plate movement.

The following points summarize the problems associated with electrical modeling of acceleration sensor.

- A prominent problem to circuit designers when designing interface circuits is the handling of device parasitics. In sensor modeling, it needs to understand the mechanism of the parasitics in order to model them appropriately (see Figure 3.2.2.2 on r_{leak} and C_p).

Figure 3.2.2.2: Cross-sectional view of capacitive micromachined acceleration sensor showing the sensor parasitics

- Not only does the mechanical acceleration force cause the middle plate of acceleration sensor to move, the electrostatic force applied on the plates can also move it. The electrostatic force is necessary in force-balanced configuration. For this reason, the modeling process has to bring in both of these forces. However, as both the forces are of different nature, there are some difficulties to include both the mechanical actuation and the electrostatic actuation into the model.

- As the model is originated from an equation that relates capacitance to required parameters, the concern for electrical modeling is the conversion of this equation into the equivalence electrical representation. This can be complicated when modeling the second-order effect of acceleration sensor (see Equation 3.2.2.3) relating to the change of capacitance.

3.2.3 Review of Sensor Modeling Methods

This section discusses modeling methods for the acceleration sensor. The section begins with a review of the reported modeling methods. Then, comparisons of these methods are summarized. It is noted that the notations for parameters such as acceleration a , displacement x , mass m , damping ratio b and spring constant k_s are consistent with those in Figure 3.2.2.1.

Conventional Differential Capacitance Model

Figure 3.2.3.1 shows the conventional differential capacitance model [Baxter-1997] with and without parasitic capacitance. With this model, the values of C_1 and C_2 have to be set manually. Parasitic capacitance can be added as C_p . It is very simple to implement and can give a quick answer to circuit designers.

Figure 3.2.3.1: Conventional acceleration sensor models

Mathematical Model of Mechanical Movement

Figure 3.2.3.2 shows a mathematical model of an acceleration sensor that describes the second-order mechanical movement. The mathematical model is presented as a signal flow block diagram. The signal flow diagram, which includes integration blocks ($\int$), is used in simulator like Matlab for obtaining the dynamic response of the acceleration sensor [Kraft 1998], [Wuestling 1997]. However, conversion to electrical block diagram for Spice simulation would be difficult and cumbersome.

Figure 3.2.3.2: Signal flow block diagram showing mathematical model of mechanical movement

Parallel-LCR Sensor Model of Mechanical Movement

Figure 3.2.3.3 shows the modeling method using parallel-LCR sensor model of mechanical movement [Kampen 1998]. This model accounts for the second-order effects of acceleration sensor by direct translation of mechanical parameters into electrical representations. For example, the change of displacement Δx is translated to the product of current I , and inductance L . The simulation is easily done in Spice. However, the electrical representation values converted are very small, which need some scaling.

Figure 3.2.3.3: Parallel-LCR sensor model using direct translation method

Series-LCR Sensor Model of Mechanical Movement

To solve the scaling problem, an improvement to the parallel-LCR method (discussed in the previous section) is shown on the left of Figure 3.2.3.4. This approach uses the scaling factor A (typically 10^6 in surface micromachined) to scale all the components appropriately [Fedder 1996]. The force F_x is converted into voltage v_x in a series-LCR model and is then transformed into v_o using voltage-dependent voltage source. In this way, a time-varying capacitor model in Spice can be designed that gives a voltage output for any change in sensing capacitance (see the right diagram of Figure 3.2.3.4). This method, however, does not give a direct change in capacitance.

Figure 3.2.3.4: Series-LCR sensor model using direct translation method and Spice time-varying capacitor

Gas-film Accelerometer Sensor Model

A recent development of sensor model is gas-film acceleration sensor model [Veijola-1999]. The sensor model is depicted in Figure 3.2.3.5. Gas-film is employed for damping of the sensor. There is a direct translation of mechanical parameters to electrical representation. The electrostatic actuation is realized by a current source. It uses gyrators for converting acceleration to capacitance outputs. This method is quite complicated to implement.

Figure 3.2.3.5: A gas-film acceleration sensor model using gyrator

3.2.4 Comparison of Reviewed Accelerometer Sensor Model

Table 3.2.4.1 summarizes the strength and weakness for the above-mentioned methods.

Table 3.2.4.1: Summary of strength and weakness of acceleration sensor modeling methods

Methods	Strength	Weakness
Conventional Differential Capacitance Model with/without Parasitic [Baxter-1997]	<ul style="list-style-type: none">✧ Simple and easy to implement✧ Spice compatible	<ul style="list-style-type: none">⇒ Capacitance fixed at a value during simulation⇒ Cannot be used for electrostatic force actuation
Mathematical Model of Mechanical Movement [Kraft 1998] [Wuestling 1997]	<ul style="list-style-type: none">✧ Full description of mechanical movement✧ Second-order effect of the sensor is modeled	<ul style="list-style-type: none">⇒ More cumbersome to implement in Spice⇒ Electrostatic force actuation is not modeled
Parallel-LCR Sensor Model of Mechanical Movement [Kampen 1998]	<ul style="list-style-type: none">✧ Direct translation of mechanical parameters to electrical representation✧ Second-order effect is modeled✧ Spice compatible	<ul style="list-style-type: none">⇒ Difficult to implement⇒ Need value scaling⇒ Electrostatic force actuation is not modeled
Series-LCR Sensor Model of Mechanical Movement [Fedder 1996]	<ul style="list-style-type: none">✧ Direct translation of mechanical parameters to electrical representation with scaling✧ Parasitics are modeled✧ Second-order effect is modeled✧ Spice compatible	<ul style="list-style-type: none">⇒ Output in terms of voltage and current and is not reflecting the change of capacitance directly⇒ Electrostatic force actuation is not considered
Gas-film Accelerometer Sensor Model [Veijola-1999]	<ul style="list-style-type: none">✧ Direct translation of mechanical parameters to electrical representation✧ Electrostatic force actuation is realized as current source✧ Gas-film damping is easily added	<ul style="list-style-type: none">⇒ Implementation is more complex

3.3 Proposed Acceleration Sensor Model

3.3.1 Initial Proposed Acceleration Sensor Model

In order to combine the mechanical actuation parameters and the electrostatic actuation equation together, a behavioral acceleration sensor model as shown in Figure 3.3.1.1 is proposed². This model is implemented in HSpice. This behavioral model can also be used in standard Spice or Spice-compatible simulators.

Figure 3.3.1.1: The proposed behavioral accelerometer sensor model

² This approach has been published in the paper [Lee 1999a].

The sensing capacitances C_{S1} and C_{S2} are functions of acceleration (in term of voltage, 1g per volt sensitivity) at the input terminal N_a as well as the voltage differences between terminal N_{ot} and N_{om} (i.e. V_{S1}) and voltage difference between terminal N_{ob} and N_{om} (i.e. V_{S2}) respectively. The mismatch factor (mmf) and the temperature effect (T_{diff} and TC) are added components to model sensor mismatch and temperature dependency. The model is flexible enough to cater for the preceding two parameters, which can be neglected by setting them to zero if they are not known during the application of the model. The relationship between acceleration and capacitance, taking into account of mechanical and electrostatic actuation, is as follows (See Appendix A for derivation).

$$C_{S1} = (1 + mmf)(1 + T_{diff} * TC) \frac{\epsilon S}{x_o - (x_a + x_e)} \quad (3.3.1.1)$$

$$C_{S2} = (1 - mmf)(1 + T_{diff} * TC) \frac{\epsilon S}{x_o + (x_a + x_e)} \quad (3.3.1.2)$$

where $x_a = \frac{ma}{k_s}$ - mechanical actuated distance

$x_e = \frac{\epsilon S}{2k_s x_o^2} (V_{S1}^2 - V_{S2}^2)$ - electrostatic actuated distance

mmf - sensor mismatch factor

T_{diff} - temperature difference

TC - temperature coefficient

The variables are defined as the proof mass m , the external acceleration a , the spring constant k_s , the permittivity of dielectric material filling the cavity between the mass and the fixed frame ϵ , the effective capacitive area S , the nominal cavity distance x_o , the top-middle plate terminal voltage V_{S1} and the bottom-middle plate terminal voltage V_{S2} .

With sensing capacitance being modeled behaviorally, the parasitic components in Figure 3.2.2.2 can be easily modeled and combined with the sensing capacitances to give a complete acceleration sensor model as shown in Figure 3.3.1.1. A description of each of the parasitic components is elaborated below.

Firstly, Figure 3.3.1.2 shows the parasitic capacitance (C_{p1} , C_{p2} and C_{p3}) on the conductive plates. Since the substrate thickness d_{Si} (typically 700 μm) is much larger than the silicon dioxide thickness d_{ox} (typically 2 μm), the contribution of the parasitic capacitance due to the substrate is negligible when compared silicon dioxide. Thus, the parasitic capacitance C_{px} ($x = 1,2,3$) can be lumped as (see Appendix A for illustration of some typical values):

$$C_{px} = \frac{\epsilon_o \epsilon_{SiO2} S_{px}}{x_{px}} \quad (3.3.1.3)$$

where ϵ_o is the permittivity of free space, ϵ_{SiO2} is the relative permittivity of silicon dioxide, S_{px} is the effective capacitive area and x_{px} is the cavity distance. Note that C_{px} is for one finger. Hence, the sum of the individual C_{px} for all the fingers will give the stray parasitic capacitance of C_{pt} , C_{pm} , and C_{pb} respectively.

Figure 3.3.1.2: Stray parasitic capacitances of the acceleration sensor

Secondly, since the requirement is a two-chip approach, bonding pad capacitances are also one of the contributing factors for parasitic effects. Figure 3.3.1.3 shows the bonding pads between the sensor and the ASIC. A typical value for the bonding pad capacitance is around 3 pF. The C_b of the top plate, the middle plate and the bottom plate bonding pads will determine the values of C_{bt} , C_{bm} and C_{bb} respectively.

Figure 3.3.1.3: Bonding pad capacitances of the acceleration sensor for a two-chip approach

Thirdly, Figure 3.3.1.4 shows the distribution of lead resistances along the sensor structure (tethers, polysilicon plates, conductive leads). All these stray resistances can be lumped to a resistor R_{tp} , R_{mp} and R_{bp} for each of the plates shown in Figure 3.3.1.1.

Figure 3.3.1.4: Stray lead resistances along the acceleration sensor

Lastly, Figure 3.3.1.5 shows the resistance between the plates and the substrate. These resistances may be voltage dependent and can be considered as leakage from the plates to ground because sensor substrate if not being biased, is normally grounded. Hence, they are modeled as voltage-controlled-current sources G_{it} , G_{im} and G_{ib} for the top, the middle and the bottom plate respectively. The leakage resistance r_{Leak} sets the control ratio of voltage-to-current conversion, for an example, $1\text{ G}\Omega$ will be set to 1 nA per volt.

Figure 3.3.1.5: Leakage resistances from the acceleration sensor to ground

An example of Spice model description on the proposed acceleration sensor model is listed at the end of Appendix A. This model, however, does not include the second-order effects of mechanical movement. An improved version of the acceleration sensor model is discussed in the next subsection.

3.3.2 Improved Proposed Acceleration Sensor Model

Figure 3.3.2.1 shows the improved acceleration sensor model over the one previously described. The second-order effect of mechanical movement has been implemented in the model as series LCR circuit. The mechanical actuation of external acceleration is implemented using inductance L_a , capacitance C_a and resistance R_a , while the electrostatic actuation is implemented using inductance L_e , capacitance C_e and resistance R_e . E_e is a voltage-controlled-voltage source that directly converts the voltage at node N_{om} (V_{om}) to node N_{cmp} (terminal voltage of E_e). Since the goal is to incorporate the second-order effect of capacitive plate movement into the calculation of the change in sensing capacitance C_{S1} and C_{S2} , the LCR circuit is not to be connected physically into the model. Hence, E_e is implemented to isolate the node N_{om} from the LCR circuit. After the LCR circuits have been included, the electrostatic actuated distance of the model equations (Equation 3.3.1.1 and Equation 3.3.1.2) have been changed to

$$x_e = \frac{\epsilon S}{2k_s x_o^2} (V_{tom}^2 - V_{hom}^2) \quad (3.3.2.1)$$

V_{tom} is the potential difference between node N_{ot} and node N_{omp} , while V_{hom} is the potential difference between node N_{ob} and node N_{omp} . Note that the LCR model is added only to the middle plate because only the middle plate can move. The top and the bottom plate are fixed and hence exhibiting no mechanical movement. This second-order mechanical movement is essential for stimulating the dynamic and delay response of the proof mass. The series LCR circuit has been employed for modeling the delay response of proof mass movement in the simulation of self-test circuit³. Correlation of the series-LCR with the mechanical movement is presented in Appendix B.

³ This model is used in the paper [Lee 1999b] to simulate delay effect for self-test circuitry.

Figure 3.3.2.1: Improved acceleration sensor model with inclusion of second-order effect

The advantages of using the proposed sensor model are summarized in Table 3.3.2.1 with reference to the weaknesses of previous methods.

Table 3.3.2.1: Summary of the proposed sensor model with previous methods

Methods	Weakness	Proposed Sensor Model
Conventional Differential Capacitance Model with/without Parasitic [Baxter-1997]	<ul style="list-style-type: none">⇒ Capacitance fixed at a value during simulation⇒ Change capacitance manually	<ul style="list-style-type: none">✧ Capacitance change by acceleration and electrostatic force automatically
Mathematical Model of Mechanical Movement [Kraft 1998] [Wuestling 1997]	<ul style="list-style-type: none">⇒ More cumbersome to implement in Spice	<ul style="list-style-type: none">✧ Easy for Spice modeling
Parallel-LCR Sensor Model of Mechanical Movement [Kampen 1998]	<ul style="list-style-type: none">⇒ Difficult to implement⇒ Need value scaling⇒ Electrostatic force actuation not considered	<ul style="list-style-type: none">✧ Direct implementation in HSpice, behavioral description✧ Electrostatic force actuation built into sensor model
Series-LCR Sensor Model of Mechanical Movement [Fedder 1996]	<ul style="list-style-type: none">⇒ Output in terms of voltage and current, not reflecting the change of capacitance directly⇒ Electrostatic force actuation not considered	<ul style="list-style-type: none">✧ Direct conversion of acceleration and electrostatic force into change of capacitance✧ Electrostatic force actuation built into sensor model
Gas-film Acceleration Sensor Model [Veijola-1999]	<ul style="list-style-type: none">⇒ Implementation more complex	<ul style="list-style-type: none">✧ Implementation simpler - behavioral description

3.4 Simulation Results and Discussions

This section is to demonstrate the importance of modeling leakage current. The results will show the effect of the leakage current on the sensing interface circuit. Figure 3.4.1 shows the design of the sense amplifier, which is simply a switched-capacitor gain circuit in the first stage and a correlated double sampling circuit in the second stage. Simulation was based on the acceleration sensor model in Figure 3.3.1.1. Simulation conditions were single supply of 5 V, V_{ref} of 2.5 V, acceleration input V_a of 50 V (i.e. equivalent of 50 g in modeling) and sampling frequency of 256 kHz.

Figure 3.4.1: Sensing circuit to demonstrate the importance of including the leakage current model

Figure 3.4.2 and Figure 3.4.3 show the simulation results of sensing output V_{out1} , V_{out2} and V_{out3} , without and with leakage current model included in the sensor model respectively. It can be seen that with the leakage current model included, problems appeared in the first stage, V_{out1} and V_{out2} of being charged up at steady state (see circled portion). Due to the balanced circuit topology, the output V_{out3} is able to correct these problems. However, if the sensor model does not include the leakage current model, the charging effect becomes the hidden phenomenon.

Figure 3.4.2: Simulation result of sensing outputs using sensor model without leakage current model

Figure 3.4.3: Simulation result of sensing outputs using sensor model with leakage current model

CHAPTER 4

An Injection-Nulling Switch for Switched-Capacitor Circuits

4.1 Introduction

Switched-capacitor circuits have been widely used for decades. Not only are they being employed in both integrated circuits (IC) [Martin-1997], [Ogawa 1993], [Horie 1995], [Unbehauen-1989] and discrete component implementations [Franco-1998] but also play a very important role in instrumentation such as in sensor interfaces [Ogawa 2001], [Li 2001] and capacitance sensing circuits [Huang 1988], [Rudolf 1990], [Yun 1992], [Kuehnel 1994], [Zimmermann 1995], [Boser 1996], [Chau 1996], [Ahmad 1997], [Puers 1998], [Lemkin 1999], [Yazdi 2000]. Although they possess many advantages over the conventional resistive circuits, for example low power consumption and better temperature invariance, they have their own fundamental problems, that is, the charge injection and the clock feedthrough errors. These non-ideal switch errors, which originate from MOS switches, greatly limit the performance of precision measurement. Hence, it is important to minimize these errors so that the accuracy and the resolution can be improved.

To reduce these errors, the use of either a CMOS switch [Eichenberger 1991] or a dummy switch (DS) [Eichenberger 1990], [Martin-1997] is common. The CMOS switch technique aims to cancel out the charge injection error of a NMOS transistor by using that of a PMOS transistor, and vice versa. However, in a typical CMOS switch, the vast difference in their threshold voltages causes the two transistors to turn off at different time instances, which results in an unavoidable charge injection (CI) error. In addition, the presence of large

parasitic capacitance mismatch also makes the compensation of the clock feedthrough (CKFT) error ineffective. In many SC circuits, the DS is more desirable. It employs a main MOS transistor either in series with a dummy MOS transistor or sandwiched between two. As the DS is half of the size, upon turning off of the main transistor, the dummy transistors are assumed to absorb half of the channel charge. However, in practice, it is difficult for the two transistors to establish an exact half-ratio proportion on all their characteristics, especially on the parasitic capacitance. Therefore, it is normal to observe the existence of some residual switch errors.

This chapter presents an approach using the new injection-nulling switch (INS) [Lee 2005a], [Lee 2005b] to circumvent the above-mentioned problems. A considerable improvement in the reduction of the switch errors will be shown using two identically designed MOS transistors and a capacitor. The mechanisms of both the charge injection error and the clock feedthrough error are illustrated in Section 4.2. Section 4.3 proposes the INS technique in conjunction with the derivation of its error. Then a comparison with the conventional switch methods implemented on the sample-and-hold (S/H) circuit is discussed in Section 4.4.

4.2 Charge Injection and Clock Feedthrough

Figure 4.2.1: Charge injection and clock feedthrough mechanisms of a single MOS transistor

This section illustrates the mechanism of the CI error and the CKFT error using a single MOS transistor switch in a simple S/H circuit (Figure 4.2.1). When the NMOS transistor M_1 driven by a clock signal ϕ is turned on (i.e. gate-to-source voltage V_{GS} larger than threshold voltage V_T), it operates in the triode region with approximately zero voltage-drop across the drain and source terminals. The channel of M_1 is then inverted, and the amount of accumulated channel charge is given by [Martin-1997]

$$Q_{ch} = -WLC_{ox}(V_{GS} - V_T) \quad \text{for } V_{GS} > V_T \quad (4.2.1)$$

where L and W are the effective channel length and width of M_1 , respectively, and C_{ox} is the gate capacitance per unit area. Note that the accumulation of electrons in the channel accounts for the negative sign.

Subsequently, when M_1 is turned off, due to the fact that there is no longer an electrical force attracting the channel charge, the charge starts to flow to both the drain and the source terminals. The fraction (α) of it that is eventually stored in the holding capacitor C_h gives rise to the CI error voltage V_{CI} , which is written as

$$V_{CI} = \frac{\alpha Q_{ch}}{C_h} = -\frac{\alpha WLC_{ox}(V_{GS} - V_T)}{C_h} \quad \text{for } V_{GS} > V_T \quad (4.2.2)$$

This will cause some non-linear distortion in the input signal [Martin-1997] because of the signal-dependent parameters α , V_{GS} and V_T . Incidentally, α depends on the transition rate of the driving clock [Shieh 1987]. If the rate is high (in fast switching condition), owing to the lack of time for charge distribution that results in an equal spreading on both terminals, α can be approximated to 50 per cent. But, if the rate is slow enough to allow a charge distribution such that a higher proportion of the charge goes to the side with lower impedance, α will take a different value. Despite the possibility that a slow transition rate can minimize α for reducing the CI error, because of the increase in the power dissipation due to the long rise and fall time of the clock edges, it is often not considered. This makes the high clock rate popular in most applications.

In contrast, CKFT error does not cause any distortion as it relies only on the ratio of capacitances and the difference in clocking voltages. Basically, through the parasitic capacitance C_p between the gate and either of the terminals, the abrupt transition change in the clocking voltages causes a sudden flow of charge towards the holding capacitor C_h . This produces the CKFT error voltage V_{CKFT} , which is given by

$$V_{CKFT} = -\frac{(V_{DD} - V_{SS})C_p}{C_h + C_p} \quad (4.2.3)$$

where V_{DD} and V_{SS} are high and low voltage levels of the clock signal, respectively, and C_p is the parasitic capacitance seen by C_h . Note that the negative voltage step, due to the falling-edge of the clock, gives the result of the negative sign.

More generally, the total error voltage is expressed by

$$V_E = V_{CI} + V_{CKFT} \quad (4.2.4)$$

4.3 Injection-Nulling Switch (INS)

Figure 4.3.1: General structure and clocking scheme of injection-nulling switch (INS)

As mentioned earlier, the INS [Lee 2005a], [Lee 2005b] comprises two identically designed NMOS transistors and a capacitor. Figure 4.3.1 shows how these components (M_i , M_n and C_n in the dotted box) are connected in a S/H circuit together with the clocking scheme. In particular, terminal H is joined to the high-impedance MOS-gated opamp input, which is prone to switch errors. Although the clock signal ϕ_n (switching M_n) is a phase-shifted signal of ϕ_i (switching M_i), ϕ_n and ϕ_i are of the same frequency and can be easily

realized using digital clock dividers. Based on this clocking scheme and the principle of charge distribution, the mechanism of the INS technique is described as follows.

Figure 4.3.2: Operation of INS during time interval τ_1

The operation starts from τ_1 , the interval when both M_i and M_n are turned on (Figure 4.3.2). During this time, the two capacitors C_{hold} and C_n are directly connected to the input signal with voltage $V_i(nT - T + \tau_1^-)$, where nT represents the n^{th} sampling instance of the clock period T , and τ_1^- signifies the interval from the beginning to the end of τ_1 just before going into τ_2 . By definition, when the voltage across a capacitor, with capacitance C , changes from 0 to V , the amount of charges Q stored in the capacitor is expressed as $Q = \int_0^V C dv = CV$. Accordingly, given that the clocking period has been designed to ensure sufficient settling time for the charge transfer, the charge stored in C_{hold} and C_n are given by

$$Q_{hold}(nT - T + \tau_1^-) = V_i(nT - T + \tau_1^-)C_{hold} \quad (4.3.1)$$

$$Q_n(nT - T + \tau_1^-) = V_i(nT - T + \tau_1^-)C_n \quad (4.3.2)$$

where $Q_{hold}(nT - T + \tau_1^-)$ are charges stored in the holding capacitor during

time interval τ_1^- ;

$Q_n(nT - T + \tau_1^-)$ are charges stored in the nulling capacitor during

time interval τ_1^- ;

$V_i(nT - T + \tau_1^-)$ is the input voltage sampled into the circuit during

time interval τ_1^- .

where $\alpha_{n_{\tau_2}}$ is the fraction of M_n 's channel charge stored in C_n during τ_2 , and $[V_{DD} - V_i(nT - T + \tau_1)]$ is the V_{GS} of M_n before it is switched off. Note that, in Equation (4.3.4), the quantity of charge in the second term

$\left\{ -\alpha_{n_{\tau_2}} WLC_{OX} [V_{DD} - V_i(nT - T + \tau_1) - V_T] \right\}$ is caused by the charge injection error. The

negative sign indicates that the electrons flowed into the nulling capacitor since the channel charges stored in NMOS transistor M_n were electrons. The third term

$\left\{ \frac{-(V_{DD} - V_{SS})C_p}{C_n + C_p} C_n \right\}$ is caused by the clock feedthrough error and the negative sign

indicates the negative transition of clock signal from V_{DD} (ON) to V_{SS} (OFF).

Figure 4.3.4: Operation of INS during time interval τ_3 (injection phase)

Nonetheless, the source of errors in the output arises when M_i is being switched off by ϕ_i (Figure 4.3.4) during τ_3 (the injection phase). At this point, due to the off-state M_n , instead of flowing to C_n , the error charges are either stored in C_{hold} or absorbed by the input source. This results in the following charge distributions:

$$\begin{aligned} Q_n(nT - T + \tau_1 + \tau_2 + \tau_3^-) &= V_i(nT - T + \tau_1)C_n \\ &\quad - \alpha_{n-\tau_2} WLC_{OX} [V_{DD} - V_i(nT - T + \tau_1) - V_T] - \frac{(V_{DD} - V_{SS})C_p}{C_n + C_p} C_n \end{aligned} \quad (4.3.5)$$

$$\begin{aligned} Q_{hold}(nT - T + \tau_1 + \tau_2 + \tau_3^-) &= V_i(nT - T + \tau_1)C_{hold} \\ &\quad - \alpha_{i-\tau_3} WLC_{OX} (V_{GSi-\tau_3} - V_T) - \frac{(V_{DD} - V_{SS})C_p}{C_{hold} + C_p} C_{hold} \end{aligned}$$

which leads to

$$Q_{hold}(nT - T + \tau_1 + \tau_2 + \tau_3^-) = V_i(nT - T + \tau_1)C_{hold} + \varepsilon_{switch} C_{hold} \quad (4.3.6)$$

Here, $\alpha_{i_{\tau 3}}$ is the fraction of M_i 's channel charge stored in C_{hold} during τ_3 , and similarly, $[V_{DD} - V_i(nT - T + \tau_1)]$ is the V_{GS} of M_i before it is turned off. The switch error voltage ε_{switch} due to the error charges is expressed as

$$\varepsilon_{switch} = \frac{-\alpha_{i_{\tau 3}} WLC_{OX}}{C_{hold}} [V_{DD} - V_i(nT - T + \tau_1) - V_T] - \frac{(V_{DD} - V_{SS})C_p}{C_{hold} + C_p} \quad (4.3.7)$$

Figure 4.3.5: Operation of INS during time interval τ_4 (nulling phase)

The final phase τ_4 (the nulling phase) is the main emphasis of the whole operation because it is when the errors are minimized while generating an almost precise replica of the input signal to the output. The uniqueness of this phase lies in the turning-on of M_n . This produces the error-compensating CI and CKFT charges in view of the fact that electrons from C_{hold} and C_n are drawn into M_n to form the inverted channel (Figure 4.3.5), whilst CKFT charges are generated in the reverse polarity (on both sides of M_n) by the positive transition of ϕ_n (from V_{SS} to V_{DD}). These two error-compensating charges counteract those

error charges produced in τ_2 and τ_3 . In other words, the charge distributions on the two capacitors at the end of the nulling phase are as follows:

$$\begin{aligned} Q_{hold}(nT - T + \tau_1 + \tau_2 + \tau_3 + \tau_4^-) &= V_i(nT - T + \tau_1)C_{hold} \\ &\quad - \alpha_{i_{\tau 3}} WLC_{OX} [V_{DD} - V_i(nT - T + \tau_1) - V_T] - \frac{(V_{DD} - V_{SS})C_p}{C_{hold} + C_p} C_{hold} \\ &\quad + \alpha_{n_{\tau 4}} WLC_{OX} (V_{GS_{n_{\tau 4}}} - V_T) + \frac{(V_{DD} - V_{SS})C_p}{C_{hold} + C_p} C_{hold} \end{aligned}$$

$$\begin{aligned} Q_n(nT - T + \tau_1 + \tau_2 + \tau_3 + \tau_4^-) &= V_i(nT - T + \tau_1)C_n \\ &\quad - \alpha_{n_{\tau 2}} WLC_{OX} [V_{DD} - V_i(nT - T + \tau_1) - V_T] - \frac{(V_{DD} - V_{SS})C_p}{C_n + C_p} C_n \\ &\quad + (1 - \alpha_{n_{\tau 4}}) WLC_{OX} (V_{GS_{n_{\tau 4}}} - V_T) + \frac{(V_{DD} - V_{SS})C_p}{C_n + C_p} C_n \end{aligned}$$

where $\alpha_{n_{\tau 4}}$ is the fraction of M_n 's channel charges that has been drawn from C_{hold} during τ_4 , and $\{V_{DD} - [V_i(nT - T + \tau_1) + \varepsilon_{switch}]\}$ is the V_{GS} of M_n at the juncture when M_n is switched on. After further simplification, it yields

$$\begin{aligned} Q_{hold}(nT^-) &= V_i(nT - T + \tau_1)C_{hold} - \alpha_{i_{\tau 3}} WLC_{OX} [V_{DD} - V_i(nT - T + \tau_1) - V_T] \\ &\quad + \alpha_{n_{\tau 4}} WLC_{OX} \{V_{DD} - [V_i(nT - T + \tau_1) + \varepsilon_{switch}] - V_T\} \end{aligned} \quad (4.3.8)$$

$$\begin{aligned} Q_n(nT^-) &= V_i(nT - T + \tau_1)C_n - \alpha_{n_{\tau 2}} WLC_{OX} [V_{DD} - V_i(nT - T + \tau_1) - V_T] \\ &\quad + (1 - \alpha_{n_{\tau 4}}) WLC_{OX} \{V_{DD} - [V_i(nT - T + \tau_1) + \varepsilon_{switch}] - V_T\} \end{aligned} \quad (4.3.9)$$

The time symbol nT^- signifies the point of time just before going to the next sampling period. Therefore, by law of conservation of charge, the charges stored in C_{hold} (Equation 4.3.9) and charges stored in C_n (Equation 4.3.8) being summed at node A are

$$Q_T(nT^-) = Q_{hold}(nT^-) + Q_n(nT^-)$$

$$\begin{aligned} \text{or } Q_T(nT^-) &= V_i(nT - T + \tau_1)(C_{hold} + C_n) \\ &\quad + [1 - (\alpha_{n_{\tau 2}} + \alpha_{i_{\tau 3}})] WLC_{OX} [V_{DD} - V_i(nT - T + \tau_1) - V_T] - WLC_{OX} \varepsilon_{switch} \end{aligned} \quad (4.3.10)$$

Finally, by dividing Equation (4.3.10) with $(C_{hold} + C_n)$, the output voltage can be expressed in the form of

$$V_{out}(nT^-) = V_i(nT - T + \tau_1) + \varepsilon_{INS} \quad (4.3.11)$$

where ε_{INS} is error voltage of the INS, which is given by

$$\varepsilon_{INS} = \left[1 - (\alpha_{n,\tau_2} + \alpha_{i,\tau_3}) \right] \frac{WLC_{OX}}{C_{hold} + C_n} [V_{DD} - V_i(nT - T + \tau_1) - V_T] - \frac{WLC_{OX}}{C_{hold} + C_n} \varepsilon_{switch} \quad (4.3.12)$$

Substituting Equation (4.3.7) into Equation (4.3.12), the general expression that defines the INS error is

$$\begin{aligned} \varepsilon_{INS} = & \frac{WLC_{OX}}{C_{hold} + C_n} \left(\frac{(V_{DD} - V_{SS})C_p}{C_{hold} + C_p} \right) \\ & + \left[1 - (\alpha_{n,\tau_2} + \alpha_{i,\tau_3}) + \alpha_{i,\tau_3} \frac{WLC_{OX}}{C_{hold}} \right] \frac{WLC_{OX}}{C_{hold} + C_n} [V_{DD} - V_i(nT - T + \tau_1) - V_T] \end{aligned} \quad (4.3.13)$$

where $\left(\frac{WLC_{OX}}{C_{hold} + C_n} \right) \ll 1$, $\left(\alpha_{i,\tau_3} \frac{WLC_{OX}}{C_{hold}} \right) \ll 1$ and $(\alpha_{n,\tau_2} + \alpha_{i,\tau_3}) \approx 1$ for fast clock transition.

Equation (4.3.13) reveals that the fundamental uncompensated switch error voltage ε_{switch} (Equation (4.3.7)), arising from the injection phase, has been significantly reduced to ε_{INS} .

In this connection, observing the first term, the uncompensated CKFT error voltage

$\frac{(V_{DD} - V_{SS})C_p}{C_{hold} + C_p}$ is made very much smaller by the factor $\left(\frac{WLC_{OX}}{C_{hold} + C_n} \right)$; for the typical

values of $WL = 1 \mu\text{m}^2$, $C_{OX} = 2 \text{ fF}/\mu\text{m}^2$, $C_{hold} = 2 \text{ pF}$, $C_p = 1 \text{ fF}$ and $(V_{DD} - V_{SS}) = 5 \text{ V}$, the uncompensated error voltage of 2.5 mV has now reduced to $1.25 \mu\text{V}$ by the factor of 5×10^{-4} . Similarly, shown in the second term, the CI error is greatly minimized since

$[1 - (\alpha_{n_{\tau 2}} + \alpha_{i_{\tau 3}})]$ has value that approaches zero and $\left[\alpha_{i_{\tau 3}} \left(\frac{WLC_{OX}}{C_{hold}} \right) \left(\frac{WLC_{OX}}{C_{hold} + C_n} \right) \right]$ is

very small. It is worth mentioning that the benefit of having matching transistor characteristics, by utilizing two identically designed transistors, has resulted in this significant reduction of the switch errors. Incidentally, the INS error has a direct relationship with the area (WL) of the transistor. This means that the increase in the area will lead to a larger INS error. Therefore, it is desirable to choose a small switch.

4.4 Experimental Results and Performance Comparison

To verify the effectiveness of the proposed technique, a comparison with the conventional switch topologies, the single NMOS switch (SS) and the DS, was performed using the basic S/H circuit implementation. Shown in Figure 4.4.1 (SS), Figure 4.4.2 (DS) and Figure 4.4.3 (INS), each circuit consists of a holding capacitor C_{hold} , a folded-cascode non-inverting opamp with high-swing current mirrors, and its own switch element. The driving clock signal for the switches are also displayed. With the following values: $C_n = C_{hold} = 2$ pF, W/L ratio of $M_d = 1.4 \mu\text{m} / 0.6 \mu\text{m}$, and that of M_l , M_m , M_i and $M_n = 2.8 \mu\text{m} / 0.6 \mu\text{m}$, all three circuits were fabricated on the same test chip using AMS (Austria Mikro Systeme International AG) $0.6 \mu\text{m}$ n-well CMOS process. The microphotograph is shown in Figure 4.4.4.

Figure 4.4.1: S/H circuit using SS as switch

Figure 4.4.2: S/H circuit using DS approach

Figure 4.4.3: S/H circuit using INS approach

Figure 4.4.4: Microphotograph of the S/H circuits using SS, DS and INS

Two types of measurement were taken on the chip. These are the time domain for comparing the effectiveness of switch error minimization, and the frequency domain to support the former on the reduction of signal-dependent CI error since high CI error can lead to the existence of some higher-order harmonics. The respective measurement instruments being employed were an oscilloscope (HP 54645D MegaZoom Mixed-Signal oscilloscope) with a cursor measurement resolution of $25\ \mu\text{V}$ and an analyzer (Stanford Research Systems Model SR770 FFT Network Analyzer) with a low distortion output source. A DC input voltage calibrated to compensate for the opamp's offset was used for the time domain measurement to produce an output voltage (V_{out}) of 2.8 V. This value is chosen to prevent any voltage swing or common-mode issues arising from the non-inverting opamp. As for the frequency domain measurement, the input was a 1 kHz, 1 V_{pk} AC signal coming from the analyzer output source. The circuits were operating on a 5 V supply and the clock signals were running on 125 kHz from an on-chip 1 MHz-divided digital ring oscillator. A discussion for each measurement is as follows.

Figure 4.4.5, Figure 4.4.6 and Figure 4.4.7 show the time domain V_{out} waveforms and the clock signals of Figure 4.4.1, Figure 4.4.2 and Figure 4.4.3, respectively. Note that although some spikes may appear along the V_{out} waveform due to the switching noise originating from the multi-stage divider circuits, their effects are not of concern because from observation, the output voltage was able to recover from them within a short time. The error voltage of SS (Figure 4.4.5) and DS (Figure 4.4.6) are highlighted in the circle. Basically, SS presents the common switch error voltage, which is 5.312 mV, whilst 3.75 mV error in DS was caused by the mismatch transistor characteristics between the main and dummy transistors. Unlike the two, the actual INS error in Figure 4.4.7 should be read from the nulling phase instead of the "error voltage" in the injection phase. Displaying the same waveform but with the addition of the clocking signals, Figure 4.4.8 presents a

finer illustration of the INS technique. In particular, when M_n is turned on again in the nulling phase, the -4.375 mV switch error (in the injection phase) was substantially reduced, resulting in an output voltage that appeared to be the same as the required 2.8 V in τ_1 . Table 4.4.1 summarizes the above-mentioned error magnitude. In brief, it shows that the INS technique does have a definite edge over its counterparts in terms of minimization of switch errors.

Table 4.4.1: Error voltage results of the three S/H circuits

Compensation Method	From Figure	Error Voltage Magnitude
Single NMOS switch	4.4.5	5.312 mV
Dummy switch	4.4.6	3.75 mV
Injection-nulling switch	4.4.7 & 4.4.8	Less than 25 μV (Cursor resolution limit)

Figure 4.4.5: Measured time domain response of S/H circuit using SS

Figure 4.4.6: Measured time domain response of S/H circuit using DS

Figure 4.4.7: Measured time domain response of S/H circuit using INS

Figure 4.4.8: Measured time domain response of Figure 4.4.7 with detailed clock sequence

Figure 4.4.9, Figure 4.4.10 and Figure 4.4.11 show the respective frequency spectrum of V_{out} . For the case of SS (Figure 4.4.9), the third harmonic component was 70.37 dB below the fundamental component and the THD was measured at 68 dB. For DS (Figure 4.4.10), it was 74.23 dB and 74 dB respectively. For INS (Figure 4.4.11), however, the respective results of 85.55 dB and 85 dB were obtained. All these are summarized in Table 4.4.2. The results have again supported the fact that INS performs better in the reduction of charge injection error.

Table 4.4.2: Comparison of THD of the compensation methods on S/H circuits

Compensation Method	Technology	Sampling Frequency	THD
Single NMOS switch	0.6 μm	125 kHz	68 dB
Dummy switch	0.6 μm	125 kHz	74 dB
Injection-nulling switch	0.6 μm	125 kHz	85 dB

Figure 4.4.9: Measured spectral harmonic distortion of the S/H circuit in Figure 4.4.1 using SS

Figure 4.4.10: Measured spectral harmonic distortion of the S/H circuit in Figure 4.4.2 using DS

Figure 4.4.11: Measured spectral harmonic distortion of the S/H circuit in Figure 4.4.3 using INS

CHAPTER 5

Accelerometer System Design

5.1 Proposed Accelerometer System Architecture

Figure 5.1.1: Proposed accelerometer system block diagram showing the connections between building blocks and modules

The proposed accelerometer system architecture and its respective building blocks are illustrated in Figure 5.1.1. The ASIC comprises a sense amplifier, a gain stage, a filter stage, an output stage, an oscillator, a clock generator, trimming and control logic circuits (on-chip calibration circuits) and a serial-to-parallel register. The self-test selection and the filter bandwidth selection are externally specified by the self-test input and the filter bandwidth input respectively. The programming data is serially shifted into the serial-to-parallel registers, which provides calibration data for the trimming and control logic circuits. The circuits will subsequently calibrate the gain stage, the output stage as well as

the oscillator. After the required output has been calibrated, the finalized settings are to be programmed. It is ultimately fixed by the programming of polysilicon fuses in the trimming circuits.

The overall accelerometer chip requires only a single 5 V supply. The accelerometer employs two-chip integration approach. As the sensor and the ASIC are fabricated individually using their own process technology, fabrication complexity has been reduced and better manufacturing control and flexibility are achieved. This approach is chosen to improve the yield [Kajita 2000] and to lower the cost per device.

The following sections describe the proposed solutions to the design and the implementation of each building block in the system, which aim to solve the problems that have been discussed in Chapter 2.

5.2 Proposed Solution for Front-End Interface Circuit

In view of the three issues (high resolution, low power, simplicity of incorporating self-test) discussed in Chapter 2, the thesis has proposed the CDS technique together with the employment of INS implementing in an open-loop system that incorporate self-test capability. As the conventional CDS gain amplifier [Gregorian 1983] suffers from high slew-rate and fast settling time requirements, a capacitive-reset gain circuit [Enz 1996], [Martin-1997], is employed on the basis of reduced the slew-rate and the settling time requirements in the amplifier. There is also an improvement on the gain error, due to the finite open loop gain (A_0) of the opamp, from the usual $1/A_0$ to $1/A_0^2$ [Unbehauen-1989], [Enz 1996]. The operation range of the sense amplifier output is maintained between ± 0.1 V from the midway of supply voltage (2.5 V) for the $\pm 10\%$ limits of sensor capacitance change. The complete implementation of the sensing interface circuit is covered in Chapter 6.

5.3 Proposed Solution for Gain Stage

Practical considerations of the gain stage have been discussed in Chapter 2. In addition, the practical range of the trimming array values and the effect of trimming circuit on the gain stage must be taken into account. Therefore, the thesis proposes a single-stage capacitive-reset gain topology with INS switch approach, incorporating the trimming arrays of gain and offset. The advantages of using such topology are as follows. Firstly, it reduces the amplifier offset error and the low-frequency noise. Secondly, the employment of INS switch minimizes the switch injection errors and simplifies the circuit, which is able to achieve lower power consumption. Thirdly, the topology permits the trimming of gain and offset simultaneously with a single opamp stage using calibration circuit.

The gain stage is responsible for amplifying the amplitude of the signal from sense amplifier, which is of order ± 0.1 V, by a gain factor of four times to a range of ± 0.4 V center at 2.5 V. This is to limit the signal amplitude so as to facilitate the design of subsequent filter stage. The circuit implementation is described in Chapter 6.

5.4 Proposed Solution for Filter Stage

For the design of filter stage, the thesis proposes the LPF to be split into two stages. The first stage is a switched-capacitor filter with low cutoff frequency, selectable between 500 Hz and 1 kHz. The low cutoff frequency is designed for filtering the out-of-band noise as well as the sampling clock signal. The selectable cutoff frequency option gives user the flexibility to configure the bandwidth of accelerometer system. The second stage is a continuous-time LPF that will filter the sampling clock signal and other remaining noise. The cutoff frequency for this LPF is 5 kHz. The main reason for the division of the filter stage into two parts is to alleviate the time constant problem. Since the continuous-time LPF is impractical to be realized for frequency of 500 Hz, switched-capacitor filter is the appropriate choice. Both the LPFs are of Bessel filter-type. In order to minimize power dissipation, they are implemented using Sallen-Key filter topology, which requires only one opamp for each stage. To alleviate the common-mode voltage problem, the gain stage prior to the filter stage keeps the amplitude of filter input voltage small, within a maximum of 0.4 V (as mentioned in the previous section), and the filter is designed with unity gain so as to avoid the increase of offset and noise arising from the active filter. The circuit implementation of the two-stage LPF is described in Chapter 6.

5.5 Proposed Solution for Output Stage

By careful consideration, the thesis proposes the output stage to be a continuous-time inverting gain amplifier with offset trimming circuit added to the inverting input of opamp. To solve the rail-to-rail and the linearity problem, a low-power rail-to-rail class AB opamp with added cascode biasing was designed. In addition, the output of the system is scaled within 0.25 V to 4.75 V to prevent linearity degradation near 5 V supply voltage and ground. Furthermore, to solve the resistance range problems, the high-resistive polysilicon fabrication process is recommended. The high-resistive polysilicon, which is part of the standard process, is able to realize resistors of high resistance value with accuracy comparable to polysilicon layer but using much lesser area. Its unit resistance is 1 k Ω per square of tolerance $\pm 20\%$. In addition, the control switches are realized with CMOS structure to reduce the switch resistances within the operating voltage range. This is to limit the on-resistances within the tolerable range so as not to have significant effect on the trimming resistances. The circuit is described in more detail in Chapter 6.

5.6 Proposed Solution for Oscillator and Clock Generator

Judging from the review in Chapter 2, with the objectives for achieving low-jitter and for utilizing small capacitor values, the thesis proposes a clock generator using a new Miller current-starved inverter based ring oscillator. Current-starved inverter ring oscillator is simple to implement. It consumes lower power and has lower phase noise when compared to the differential type on the basis of given power dissipation in less noisy environment [Hajimiri 1999]. To tackle the large capacitance values, the design employs the Miller capacitor technique, which makes use of the gain of every inverter stage of the ring oscillator. The Miller capacitor configuration can reduce the capacitance value significantly. Last but not least, it employs zero hysteresis Schmitt trigger technique [Popov 1998] to sharpen the edge of the clock edges for minimizing power consumption. The clock generator circuit is covered in Chapter 7.

5.7 Proposed Solution for Trimming and Control Logic Circuits

In consideration of the trimming techniques, the thesis proposes to adopt the fusible link trimming technique and uses standard polysilicon to realize the fuse elements. Polysilicon is easier to blow than other materials because the polysilicon layer is encapsulated with passivated silicon dioxide that is of lower heat conductivity than silicon substrate [Kim 1998]. Hence, thermal energy confines better between the passivated silicon dioxide, which is able to heat the polysilicon elements to its fusing temperature easier and faster. Thus, the programming time is reduced. More importantly, prolong heating of the die during programming is avoided. In addition, it is the basic material found in standard CMOS process, which offers low-cost solution without additional process step. The thesis also proposes an improved method using two orthogonal-positioned fusible link structure for one trim data so to minimize the possible fuse regrowth. It aims at increasing the reliability of the trimmed data. To lower the programming voltage and to prevent excessive power dissipation, fuse circuits are built so as to ensure that not only the programming voltage is minimized to the required fuse-blowing power but also the power dissipation for each branch of the fuse is to its minimal. In addition, protective circuitries are also included so as to isolate the possible affected area during fusing of the links. Finally, to make the calibration more flexible, a testing phase is designed to affirm the accuracy of the calibration data before blowing the fuses. The trimming circuit techniques are described together with the clock generator circuit in Chapter 7.

CHAPTER 6

Front-End Interface and Signal-Conditioning Circuits

6.1 Overview

In this chapter, the design techniques pertaining to the front-end interface circuit (sense amplifier) and the signal-conditioning circuit of the ASIC are presented. The ASIC employs injection-nulling switch for the design of low-power front-end sense amplifier so as to alleviate the switch charge injection problem. Not only does it simplify the front-end sense amplifier through using comparatively fewer switches, a single-ended opamp can be used for precise operation without resorting to the fully differential techniques. Despite single-ended topology, it is effective in improving the resolution and reduces the potential noise of the readout circuit. Furthermore, in the context of the switch error compensation, the effectiveness of the INS to minimize the switch injection errors allows a large time-constant single-ended SC filter to be implemented economically. Thus, this reduces the complexity and power consumption significantly without sacrificing the performance. Due to the fact that the front-end interface circuit is an open-loop system, it also eases the design of self-test function with minimal circuitry.

The following sections cover the design and implementation of the front-end interface circuit and the signal-conditioning circuits. The employment of INS and the implementation of self-test function in the sense amplifier are presented. The design and implementation of the signal-conditioning circuits that comprise of a gain stage, a filter stage and an output stage, are described later. The results and discussions sections detail the finding results and concluding remarks of the INS in sense amplifier design.

6.2 Front-End Interface Circuit

Figure 6.2.1: Conventional front-end sense amplifier using SC capacitive-reset gain circuit

Fig. 6.2.1 shows the conventional front-end sense amplifier using capacitive-reset gain circuit [Martin-1997] that incorporates correlated double sampling (CDS) technique to reduce both the offset and the low frequency noise of the amplifier [Kansy 1980]. It is essentially a capacitance-to-voltage converter that converts the change of capacitance value of capacitive sensing element into voltage. In response to the change of capacitance in differential capacitive sensor, the extra feedback loop, realized by using holding capacitor C_h and associated switches, is to ensure that the output voltage V_{sense_out} changes as little as possible between the clock phases T_1 and T_2 in each switching period. The structure also reduces DC error of the realized gain by a factor of $1/A_0^2$ [Martin-1997], where A_0 is the finite open-loop gain of the opamp. As a result, the circuit relaxes the opamp performance parameters in the context of slew-rate, settling time and open-loop gain issues. These are favorable characteristics for low-power opamp implementation as far as the worst-case slew-rate specification has been met.

The output voltage $V_{\text{sense_out}}$ at steady-state is given as

$$V_{\text{sense_out}} = \frac{(C_{S1} - C_{S2})}{C_f} (V_{\text{REF}} - V_{\text{AG}}) + V_{\text{AG}} \quad (6.2.1)$$

where C_{S1} is the capacitance between the top and middle plate, defined by $C_{S1} = C_0 + \Delta C_S$, and C_{S2} is the capacitance between the bottom and middle plate, defined by $C_{S2} = C_0 - \Delta C_S$. Note that C_0 is nominal capacitance under zero acceleration when the middle sensing plate is at the mid-way between the two-fixed plates whilst ΔC_S is the change of capacitance when the middle plate is displaced by external acceleration. The two sensing capacitors are switching between the reference voltage V_{REF} and the analog ground voltage V_{AG} . Hence, the change of output voltage V_{out} with reference to nominal analog ground potential (V_{AG}) can be expressed as

$$V_{\text{out}} = V_{\text{sense_out}} - V_{\text{AG}} = \frac{2(V_{\text{REF}} - V_{\text{AG}})}{C_f} \Delta C_S \quad (6.2.2)$$

The major drawback of the circuit is the switch charge injection error and the clock feedthrough error [Martin-1997] at the inverting node of opamp that limit the circuit performance in terms of precision and stability. The shortcomings of the conventional sense amplifier are alleviated via the use of the INS [Lee 2005a] (dotted box) in Figure 6.2.2 as replacement of a conventional switch (S_i) in Figure 6.2.1. The INS is realized by a switch $S_{\text{INS}i}$, a switch $S_{\text{INS}n}$ and a capacitor $C_{\text{INS}n}$, connecting to the input of the opamp as illustrated in Figure 6.2.2. With the employment of INS, the circuit can resolve a much precise value, thus increasing the capacitance sensing resolution. It can be shown that the equations for $V_{\text{sense_out}}$ and V_{out} of Figure 6.2.2 are identical to that of Figure 6.2.1 in Equation (6.2.1) and Equation (6.2.2) respectively, hence they will not be repeated here. The switch $S_{\text{INS}i}$ and $S_{\text{INS}n}$ are implemented using single MOS transistor of identical size. The operation of the INS can be explained using the clocking sequence shown in Figure 6.2.3. It is noted that T_1 and T_2 are biphasic clock signals.

During the time period of τ_1 when both switches are turned on (clock T_2 and T_n are high), the output signal $V_{\text{sense_out}}$ is sampled into C_{INSn} and node Y (Figure 6.2.2) through C_h . On entering into τ_2 , S_{INSi} remains on but S_{INSn} is turned off. When the clock transits from high supply voltage V_{DD} (ON) to low supply voltage V_{SS} (OFF), S_{INSn} will have its channel charge injection and clock feedthrough errors stored into C_{INSn} and node Y. Unlike switch errors stored in C_{INSn} , the switch errors that are injected into node Y will be absorbed by the output signal as S_{INSi} is still in the on state.

At the beginning of τ_3 (also called the injection phase), S_{INSn} remains off while S_{INSi} is switched off. The switching off of S_{INSi} will create the main source of switch errors to the output because the transistor S_{INSi} will inject its switch errors into the input (node Y) of the opamp. It is also noted that there is no change in the charges stored in C_{INSn} because transistor S_{INSn} is still in the off state. The operation of the circuit during time interval τ_4 (nulling phase) is the most crucial phase of the operation when a precise replica of the sampled signal is to be passed to the output. Hence, the switch errors at node Y that were injected during τ_3 must be eliminated. At the start of the nulling phase τ_4 , S_{INSi} remains off while S_{INSn} is switched on again. Electrons from C_{INSn} and node Y are drawn into S_{INSn} when forming the inverted channel, whilst clock feedthrough errors are generated in reverse polarity due to positive transition of the clock signal from V_{SS} (OFF) to V_{DD} (ON) on both sides of S_{INSn} . The flow of these two error-compensating charges is in complete reverse directions to the flow of error charges created by the switching off action of S_{INSn} in τ_2 and switching off action of S_{INSi} in τ_3 previously. As the switches are identical to each other, the switch errors can be reduced significantly by this reverse directional canceling action.

The self-test feature for the sensor is easily incorporated into the gain circuit design. It requires only two additional control switches S_3 and S_6 , which are controlled by a digital control bit B_{st} as shown in Figure 6.2.2. To activate self-test operation, B_{st} is simply set to high (digital '1'). Note that B_{st} is low (digital '0') during normal sensing operation. When B_{st} is high, the sensor bottom plate is connected to V_{AG} while the sensor top plate is switching between the supply voltage V_{dd} (5 V) and analog ground voltage V_{AG} (2.5 V). With the bottom plate held at analog ground, the switching of the top plate establishes an electric field between the top and middle plate. This electric field will produce a net electrostatic force that displaces the movable middle plate a distance from its equilibrium position. Thus, this will create a difference in the sensing capacitance, which produces a self-test voltage being displayed at the output V_{sense_out} . However, if the sensor is faulty, the middle plate will fail to move under the influence of the electrostatic force. Then the self-test voltage will not be sensed at the V_{sense_out} .

It is well known that cascode opamps with slew-rate enhancement circuit have the advantages of high PSRR (power supply rejection ratio), fast settling property and low power consumption. Figure 6.2.4 shows the slew-rate enhanced [Martin-1997] folded-cascode opamp for use in the sense amplifier. As can be seen, the input transistors M_{p1} and M_{p2} are PMOS transistors because they have lower flicker noise than that of the NMOS transistors. In addition, they are biased by the cascode current source transistors M_{p3} and M_{p4} , which aim to achieve high CMRR (common mode rejection ratio). Transistors M_{p5} , M_{p6} , M_{p7} and M_{p8} realize a high-swing cascode current mirror to obtain high open-loop gain. Transistors M_{p9} and M_{p10} are added to improve the slew-rate parameter of the opamp. The current sources (M_{n3} and M_{n4}) in conjunction with the active loads (M_{p5} and M_{p6}) are optimized in dimensions to achieve minimum noise according to [Chan 1999]. The current consumption of the opamp is 180 μA at 5 V supply.

Figure 6.2.4: Simplified folded-cascode opamp circuit with improved slew-rate

6.3 Signal-Conditioning Circuits

6.3.1 Gain Stage

Figure 6.3.1.1 shows the SC gain stage with programmable capacitors for gain and offset adjustment on the input signal $V_{\text{sense_out}}$ from the output of the sense amplifier. This calibration is essential because it compensates the parameter variations arising from the fabrication of acceleration capacitive sensor and limits the signal amplitude within 0.4 V before entering the filter stage for signal-conditioning. Similar to the sense amplifier, the gain stage utilizes capacitive-reset topology together with the employment of INS (dotted box) to minimize the switch injection errors. The digital control bit B_{pol} provides the flexibility of changing the polarity of the offset voltage correction. The calibration procedure and trimming circuits are explained in chapter 7.

Figure 6.3.1.1: Programmable SC gain stage with gain and offset calibration

6.3.2 Filter Stage

The first filter stage as shown in Figure 6.3.2.1 is a second-order SCF using Sallen-Key topology [Franco-1998]. The objectives of the filter design are (1) to employ the INS to ensure that the filter can operate at large capacitor ratios for a minimum of 500 Hz system bandwidth but not jeopardizing the conditioning signal quality from potential charge injection effect impacting the small capacitors and (2) to provide economic implementation without resorting to fully differential structure. Besides, SCF has the advantage of realizing very large resistance value with small value of capacitor as far as it is within the acceptable KT/C noise level. This is due to the fact that the equivalent resistance value is inversely proportional to the clocking frequency and the capacitor value.

The equivalent resistor connected to the input V_{ic_out} is realized by the switches S_{11} , S_{12} , S_{13} , S_{14} , and the capacitor C_{r1} while the resistor being connected to the non-inverting input of the opamp is realized by the switches S_{21} , S_{22} , S_{23} , S_{INSi} and the capacitor C_{r2} . The injection-nulling switch (dotted box) consists of the switch S_{INSi} , the switch S_{INSn} and the capacitor C_{INS} . The function to minimize the switch errors has been described before and hence it is not repeated here. The cutoff frequency can be selected to be either 1 kHz or 500 Hz through programming the digital bit B_{capsel} . The component values are calculated according to the Bessel response transfer function given in [Valkenburg-1982]. The capacitances C_{r1} and C_{r2} are equal and are calculated from the equivalent resistance of

$$C_{r1} = C_{r2} = \frac{1}{f_{clk} R_{eq}}.$$

Figure 6.3.2.1: Programmable SC Sallen-Key low-pass filter stage

Figure 6.3.2.2: Continuous-time Sallen-Key low-pass filter stage

The second filter stage as shown in Figure 6.3.2.2 is a third-order CTF. It is realized using a passive first-order LPF cascaded to a second-order low-pass Sallen-Key filter. Based on the clock frequency of 100 kHz and the practical values of integrated resistors and capacitors, a cutoff frequency of 5 kHz is chosen. This structure requires only one opamp to implement a third-order LPF. For matching consideration and ease of design, the resistors R_1 , R_2 and R_3 are designed to have the same value. The values of the other components are selected according to a third-order Bessel filter response [Valkenburg-1982].

6.3.3 Output Stage

The output stage is a scaling amplifier using a low-power class-AB opamp topology [Gregorian-1999] combined with trimming circuits to calibrate the output signal based on a full scale of 4.5 V (0.25 V to 4.75 V), which is equivalent to 100 g peak-to-peak value, with a 5 V supply. The implementation of the output stage is shown in Figure 6.3.3.1. The inverting summing amplifier is employed where the offset trimming circuits are added to the inverting input of the opamp. The non-inverting input of the opamp is driven at analog ground potential (V_{AG}) 2.5 V. The digital control bit B_{pol} provides the flexibility of changing the polarity of the offset voltage correction. As mentioned in the previous chapter, the trimming resistors are implemented using high-resistive poly. The output stage gives the final output (V_{OUT}) of the accelerometer system. The calibration procedure and trimming circuits are explained in chapter 7.

Figure 6.3.3.1: Implementation of output stage with gain and offset trimming

The implementation of the class-AB opamp is shown in Figure 6.3.3.2. The input stage of the opamp is a folded-cascode configuration, which is similar to that of the Figure 6.2.4 and hence it will not be repeated here. The output stage of the opamp is a rail-to-rail class-AB push-pull stage with common-gate level shifters [Gregorian-1999]. The push-pull output stage is formed by transistors M_{p16} and M_{n10} . The common-gate transistors M_{p15} and M_{n9} fix the voltage drop between the gates of M_{p16} and M_{n10} in a form of a class-AB bias circuit. The gate voltage of M_{p15} is defined by the drain potential of diode-connected transistors M_{p11} . Similarly the drain potential M_{n9} is defined by diode-connected transistors M_{n6} . The diode-connected transistors are biased by their respective cascode current sources, (M_{n5} and M_{n7}) and (M_{p12} and M_{p14}). Standard Miller compensation resistor and capacitor pairs R_{c1} and C_{c1} , and R_{c2} and C_{c2} are used to keep the opamp stable. The current consumption of the complete opamp is 150 μA at 5 V supply.

Figure 6.3.3.2: Simplified folded-cascode amplifier with class-AB output stage

6.4 Results and Discussions

To verify the effectiveness of INS on minimizing switch errors, the sense amplifier in Figure 6.2.1 using different switch topologies are simulated and compared. Except with S_i , all the switches in Figure 6.2.1 were implemented using CMOS switches. The sense amplifier was simulated with four cases of switch S_i . Case 1 is an ideal switch, which will not exhibit any switch injection error. Case 2 is a single MOS switch topology (the switch is an NMOS transistor). Case 3 is a dummy switch topology [Martin-1997] formed by a main NMOS transistor connected to a half-size dummy switch (NMOS transistor with half size of that of the main NMOS transistor), of which drain and source are being tied together. The drain and source of the half-size dummy switch is connected to the inverting input of the opamp and it is switched by a clock signal complementary to that of the main transistor, while the main NMOS transistor is connected to C_h (Figure 6.2.1). Case 4 is the INS topology. The connection of the INS can be referred to the dotted box in Figure 6.2.2 and each of the switches S_{INSi} and S_{INSn} was implemented using a single NMOS transistor.

To have a fair comparison, the NMOS transistor in case 2, the main NMOS transistor in case 3 and the two NMOS switches in case 4 were identical. In addition, the dummy transistor switch in case 3 was half-sized with that of the main transistor switch. For $V_{REF} = 3.5$ V, $V_{AG} = 2.5$ V, $(C_{S1}-C_{S2})/C_f = 0.1$, the sense amplifier was designed such that the output voltage V_{sense_out} would have an ideal voltage of 2.6 V according to Equation (6.2.1). These circuits were simulated under typical, worst-power and worst-speed cases using level 49 transistor models in AMS 0.6 μ m CMOS technology.

Figure 6.4.1 and Figure 6.4.2 depict the simulation results based on 4 types of switch topology under typical condition. The INS operation on nulling the switch errors in the nulling phase is also highlighted. Figure 6.4.2 gives the expanded view of the dotted box in Figure 6.4.1, indicating the actual value of the output voltage $V_{\text{sense_out}}$. Table 6.4.1 summarizes the simulation results without mismatch under 3 conditions. The absolute errors in Table 6.4.1, calculated by taking ideal switch topology results, form the benchmark. The simulation results have shown that the switch errors in INS are smaller than the other two topologies and the output voltage at the end of nulling phase is equivalent to that of an ideal switch.

Figure 6.4.1: Simulation results of the sense amplifier with 4 types of switch topologies at typical conditions

Figure 6.4.2: Expanded view of the simulation results in Figure 6.4.1

Table 6.4.1: Comparison of output simulation results of the sense amplifier using different switch topologies at 3 different operating conditions

	Typical Condition (Typical transistor model, V_{dd} @ 5 V, V_{REF} @ 3.5 V, temp @ 25 °C)		Worst-Power Condition (Worst-power transistor model, V_{dd} @ 5.5 V, V_{REF} @ 3.5 V, temp @ -40 °C)		Worst-Speed Condition (Worst-speed transistor model, V_{dd} @ 4.5 V, V_{REF} @ 3.5 V, temp @ 90 °C)	
Case	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)
1. Ideal Switch	2.599984	-----	2.599994	-----	2.599946	-----
2. Single MOS Switch	2.606437	6.453	2.606564	6.57	2.607523	7.577
3. Dummy Switch	2.600152	0.168	2.596963	3.031	2.603509	3.563
4. INS	2.599984	0	2.599998	0.004	2.599951	0.005

Figure 6.4.3, Figure 6.4.4 and Figure 6.4.5 illustrate the simulation results of the circuits with intentional mismatches (3 %, 5 % and 8 %) in the dummy switch (DS) topology and the INS topology at typical, worst-power and worst-speed condition respectively. It can be observed that under the mismatch effects and the process parameters variation, the respective outputs will deviate from its original value (0%).

Figure 6.4.3: Simulation results of dummy switch (DS) and INS topology with intentional mismatches at typical condition

Figure 6.4.4: Simulation results of dummy switch (DS) and INS topology with intentional mismatches at worst-power condition

Figure 6.4.5: Simulation results of dummy switch (DS) and INS topology with intentional mismatches at worst-speed condition

These results are summarized in Table 6.4.2. Consider a typical 5 % of mismatched factor (that is a lumped mismatch factor contributed by mismatches on gate oxide thickness, charges mobility, threshold voltage and dimension), the improvement on the compensation of switch errors is 2.35 times under typical condition, 5.55 times under worst-power condition and 7.9 times under worst-speed condition. At 8 % mismatch and worst-case condition, the maximum error voltage is 0.9 mV for INS topology and 5.35 mV for DS topology. Therefore, the results have revealed that INS is effective in minimizing the switch errors and is insensitive to variation of process parameters. In comparison, the dummy switch topology is less effective than INS because the main NMOS transistor is difficult to match the half-sized NMOS transistor. Hence, the compensation of switch errors becomes more sensitive to variation of process and environmental parameters.

Table 6.4.2: Comparison of output simulation results of the sense amplifier using dummy switch (DS) and INS topologies with intentional mismatches at 3 different operating conditions

	Typical Condition (Typical transistor model, V_{dd} @ 5 V, V_{REF} @ 3.5 V, temp @ 25 °C)		Worst-Power Condition (Worst-power transistor model, V_{dd} @ 5.5 V, V_{REF} @ 3.5 V, temp @ -40 °C)		Worst-Speed Condition (Worst-speed transistor model, V_{dd} @ 4.5 V, V_{REF} @ 3.5 V, temp @ 90 °C)	
Case	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)
Ideal Switch	2.599984	-----	2.599994	-----	2.599946	-----
DS (0 % mismatch)	2.600152	0.168	2.596963	3.031	2.603509	3.563
(3 % mismatch)	2.600618	0.634	2.597363	2.631	2.604105	4.159
(5 % mismatch)	2.601084	1.1	2.597763	2.231	2.60470	4.754
(8 % mismatch)	2.60155	1.566	2.598163	1.831	2.605296	5.35
INS (0 % mismatch)	2.599984	0	2.599998	0.004	2.599951	0.005
(3 % mismatch)	2.600219	0.235	2.600198	0.204	2.60025	0.304
(5 % mismatch)	2.600453	0.469	2.600396	0.402	2.600548	0.602
(8 % mismatch)	2.600687	0.703	2.600595	0.601	2.600846	0.9

CHAPTER 7

Clock Generator and Trimming Circuits

7.1 Overview

Switched-capacitor circuits have broad applications in integrated circuits [Martin-1997], [Lahiji 2000], [Schemmel 2002], [Unbehauen-1989]. They play a very important role in analog signal processing block such as sensor interface [Ogawa 2001], [Amendola 2001], switched-capacitor integrator [Lahiji 2000], summing amplifier, voltage comparator [Unbehauen-1989] and so forth. In some applications such as gain circuits, they often do not demand precise sampling frequency on their driving clocks as far as the time constant is defined by capacitor ratio and the amplifiers meet the settling time specification. Thus, ring-oscillator-based clock generator is suitable for switched-capacitor circuits because it is simple and consumes lower power when compared to those of the relaxation oscillators and phase-lock loops (PLL). In the oscillator design consideration, the substrate noise coupling is the major problem for switched-capacitor circuits in mixed-signal environment [Su 1993], [Costa 1999], [Secareanu 1999], [Singh 2001]. The amount of substrate noise coupling depends strongly on the frequency of the oscillator [Singh 2001] since the higher the frequency, the greater number of switching transitions. Hence, reducing the frequency of the oscillator is advantageous in lowering the possibility of substrate noise coupling and relaxing the requirement of the power-supply-rejection ratio (PSRR) [Peteghem 1988]. Low-frequency ring oscillator also encounters large time constant problem, which leads to the area efficiency issue. Conventional methods for obtaining low-frequency clocks are to use weak inverter stage (i.e. inverter implemented using long channel length transistors), or

to employ high frequency ring oscillator going through many stages of digital clock dividers. However, the first approach results in higher sensitivity of the oscillator jitter to the variation of environmental parameters such as supply voltage variation and substrate noise [Herzel 1999], whilst the latter approach leads to substantial increase of substrate noise coupling [Singh 2001]. Therefore, the first motivation is to investigate circuit techniques that are able to reduce the oscillator frequency with small capacitor values in ring oscillator.

Although a programmable clock generator is useful for broad range of switched-capacitor circuits, it requires trimming. For applications that do not require precise sampling frequency, a discrete-type trimming method is sufficient. This is because continuous-type trimming method like laser trimming [Deluca 2002] is expensive. However, conventional discrete-type trimming methods like the floating gate method [Säckinger 1988], Zener-zapping method [Erdi 1975], external component trimming method and fusible link method [Schroeder 1977], [Mok 1995] have their own shortcomings. From the implementation perspective, floating-gate method suffers from leakage problem [Manabe 1999] whilst Zener-zapping method requires bipolar process [Ichikawa 1996]. On the contrary, fusible link method avoids these shortcomings, which offers a total integrated solution in standard CMOS technology. However, it is subject to possible regrowth of blown fuse under environmental temperature effect. This raises the second motivation to devise a circuit and layout technique to alleviate the problem.

In this chapter, two techniques for designing a reliable low-cost programmable clock generator for low-frequency switched-capacitor applications are described. The first technique is concerned with proposed ring oscillator. Not only does it reduce the frequency of the oscillator to relax the PSRR requirement, small capacitor values can be used to enhance the area utilization. Moreover, it eliminates the use of weak inverter stages, which will result in low clock jitter performance. The second technique deals with the proposed orthogonal-fusible-link trimming circuit that adds extra protection to the programmed data and lowers the possibility of regrowth of blown fuse. Therefore, it improves the reliability of programmed clock signals.

The clock generator system [Lee 2006], which consists of clock generator circuit and the trimming circuit, is presented in Section 7.2. The implementation of clock generator circuit and the trimming circuit is described in Section 7.3 and Section 7.4 respectively. The experimental results are discussed in Section 7.5.

7.2 Clock Generator System

The system block diagram of the clock generator is illustrated in Figure 7.2.1. The clock generator system consists of the clock generator circuit and the trimming circuit.

Figure 7.2.1: Block diagram of clock generator system

The clock generator circuit is made up of an oscillator circuit and a timing generator. The oscillator circuit generates an oscillating signal using an improved ring oscillator with smaller delay capacitors. The delay capacitors are programmable by means of setting the digital trimming bits B_0 to B_{n-1} (n is the total number of trimming bits) that discretely program the period of the oscillation signal. The programmed oscillating signal drives the timing generator to generate the non-overlapping clock signals required by the switched-capacitor circuits.

The trimming circuit consists of fuse cells and SIPO (serial-in-parallel-out) register. Each of the fuse cells comprises of a fusible link trimming circuit with a digital output bit B_{out} to define the trimming bit. The number of trimming bits required by the oscillator circuit determines the number of fuse cells. The external control bits B_{test} and B_{prog} are connected to every fuse cell internally. The B_{test} is to switch between tuning mode and normal operation mode. In the tuning mode, the output bit B_{out} is adjusted by the data from SIPO register while in the normal operation mode, B_{out} is set by the programmed fuse data. The B_{prog} is responsible for blowing the fusible link. The SIPO register, on the other hand, provides all the trimming data that are required by the fuse cells. The data is serially shifted into the register so as to keep a small number of external pins, which are required to trim the overall clock generator.

7.3 Implementation of Clock Generator Circuit

Figure 7.3.1 shows the schematic diagram of a conventional 3-stage ring oscillator. It consists of three inverter stages and their respective delay capacitors. The oscillation frequency [Kang-1999] is given as

$$f_{osc} = \frac{1}{6R_d C_d} = \frac{1}{6t_d} \quad (7.3.1)$$

where t_d is the time delay for each stage defined as the product of the load resistance R_d and the effective output load capacitance C_d , as seen from the output of each stage. For low-frequency oscillation, the large time delay is achieved through the increase of load resistance and/or increase of capacitance. To increase load resistance, PMOS and NMOS transistors in weak inversion are designed with long channel length at the price of increased jitter effect [Herzel 1999]. On the other hand, the increase of load capacitance will increase the silicon area and the cost of product.

Figure 7.3.1: Schematic diagram of conventional ring oscillator

Figure 7.3.2: Schematic diagram of proposed programmable oscillator circuit

Figure 7.3.2 shows the schematic diagram of the proposed oscillator circuit in n-well CMOS technology. It consists of a ring oscillator, a transition-sharpening inverter and an Schmitt trigger. The proposed oscillator (left dashed box) comprises three-stage current-starved inverter with their respective Miller capacitors in a ring arrangement. The improvement for low-frequency oscillation comes from the Miller capacitors, C_1 , C_2 and C_3 (note that the arrows indicate that the capacitors are programmable). The purpose of these Miller capacitors is to increase the effective capacitance at the input of each inverter stage.

Figure 7.3.3: First stage of ring oscillator and its equivalence for illustration of Miller effect

Figure 7.3.3 illustrates the first stage of the ring oscillator together with its equivalence. Referring to the diagram on the right side, the input equivalent capacitance C_{lieq} as seen from the input of the current-starved inverter is increased by a factor of $(1+|A|)$ over that of C_1 , while the output equivalent capacitance $C_{loe q}$ from the output is slightly increased by a factor of $\left(1 + \frac{1}{|A|}\right)$. Note that the input equivalent capacitance will be treated as an output capacitance by the preceding inverter stage. During transition of the signal around the linear operating point of the inverter, that is around the midway between the supply voltage and ground, the voltage gain A which is the transconductance of the inverting amplifier multiply by the effective load of the inverter can be derived using small-signal analysis as

$$A = - \left[\frac{g_{mp2}g_{dp1}(g_{dn1} + g_{dn2} + g_{mn2} + g_{bn2}) + g_{mn2}g_{dn1}(g_{dp1} + g_{dp2} + g_{mp2} + g_{bp2})}{g_{dp1}g_{dp2}(g_{dn1} + g_{dn2} + g_{mn2} + g_{bn2}) + g_{dn1}g_{dn2}(g_{dp1} + g_{dp2} + g_{mp2} + g_{bp2})} \right] \quad (7.3.2)$$

where g_{dp1} , g_{dp2} , g_{dn1} and g_{dn2} are the output conductance of transistor M_{p1} , M_{p2} , M_{n1} , M_{n2} , respectively, g_{mp2} is the transconductance, g_{bp2} is the bulk transconductance of M_{p2} , g_{mn2} is the transconductance and g_{bn2} is the bulk transconductance of M_{n2} . Assuming that $(g_{mn2} + g_{bn2}) \gg (g_{dn1} + g_{dn2})$, $(g_{mp2} + g_{bp2}) \gg (g_{dp1} + g_{dp2})$ and neglecting the body effect $(g_{mp2} \gg g_{bp2} \quad , \quad g_{mn2} \gg g_{bn2})$, the gain can be approximated as

$$A \cong - \left[\frac{g_{mp2}g_{mn2}(g_{dp1} + g_{dn2})}{g_{mp2}g_{dn1}g_{dn2} + g_{mn2}g_{dp1}g_{dp2}} \right] \quad (7.3.3)$$

Equation (7.3.3) shows that the gain factor $(1+|A|)$ of the input equivalent capacitance can achieve in order of 10 in principle. For operation range that is out of the linear range, the gain is reduced due to the decrease of g_m in non-linear range. However, there is still a substantial reduction on the size of capacitors. This improvement is important because large integrated capacitors are not area efficiency.

In addition, the current-starved inverter stages of the ring oscillator is configured such that the gate voltages of the current sources M_{p1} , M_{p3} and M_{p5} are kept at ground (0 V) while the gate voltages of M_{n1} , M_{n3} and M_{n5} is biased at V_{dd} . This configuration has been proven to be effective in reduction of clock jitter [Hajimiri 1999].

Since the output of the ring oscillator (V_{osc}) is a sinusoidal waveform, it has to go through an inverter (Figure 7.3.2) to sharpen its transition edges before entering the zero hysteresis Schmitt trigger. The zero hysteresis Schmitt trigger technique [Popov 1998] is used to ensure the clock signal to have a 50 percent duty cycle. This symmetrical clock signal in association with the timing generator devices derives all the timing clock signals.

Figure 7.3.4: Schematic diagram of the timing generator

Refer to Figure 7.3.4 for illustration of the operation of the timing circuit, the frequency of the oscillator output V_{osc} is divided by the clock divider, which comprises of small number of toggle flip-flops (FF) on the basis of utilizing the Miller-based current-starved inverter. The number of FFs required in the clock divider is dependent on the size of the Miller capacitors and the frequency step-down ratio. The divided clock signal is then toggled through a JK FF to derive a complementary clock signal that is required by the non-

overlapping timing generator. In the non-overlapping timing generator (dashed box), the feedback connection of T_{1b} to the input of the upper NOR gate and T_{2b} to the input of the lower NOR gate, produces the non-overlapping time delay region between the switching off of timing clock T_1 and the switching on of T_2 , and vice versa. The width of the non-overlapping region is adjustable by the delay capacitors C_{d1} , C_{d2} , C_{d3} and C_{d4} . Note that the output of timing generator are the timing clock signals T_1 , T_2 , T_{1a} and T_{2a} that are required by most of the switched-capacitor circuits where T_{1a} and T_{2a} are the advanced clock signal of T_1 and T_2 respectively. The complementary clocks T_{1b} , T_{2b} , T_{1ab} and T_{2ab} are also available from the clock generator circuit. The clock signal T_n for the INS is produced using a FF and two inverters as shown.

7.4 Implementation of Trimming Circuit

The trimming circuit, consisting of the fuse cells and the SIPO (serial-in-parallel-out) register (Figure 7.2.1), enables the frequency of the timing clock signals to be programmable through digital data bits b_0 to b_{n-1} (n is the total number of bits). These data bits are used to trim the capacitance of the Miller capacitors, which are implemented in the form of arrays; refer to Figure 7.4.1 for illustration of the programmable Miller capacitor array implementation. Each of these data bits controls an analog switch on every of the inverter stage in the ring oscillator (Figure 7.4.1). When the switch is turned on, it will connect the respective capacitor between the input and output of each inverter stage. Thus, the main objective is to program the data bits to attain the required clock period, hence the clock frequency, by adjusting the capacitance of the Miller capacitor array in each inverter stage.

Figure 7.4.1: Programmable Miller current-starved inverter ring oscillator

The data bits are programmed using fusible link technique. Figure 7.4.2 shows one of the fuse cell module. Each fuse cell module comprises two fusible links, F_1 and F_2 . The fusible links, when not blown, serve as pull-up resistors to pull fuse data bit B_{fdata} to logical value '1'. Note that B_{fdata} provides the programmed data for the output B_{out} of the fuse cell during normal operation. The proposed dual-fusible-link design is more reliable in preventing the programmed data from changing against the regrowth of the blown fuse than the conventional design of using one fusible link for the following reasons. Firstly, the logic of the dual-fusible-link design is designed in such a way that if one of the blown fuses grows back, the programmed data is still unaffected. This can be achieved by the AND gate in the trimming circuit because since the blown fuse presents a logic '0', any one of the fuse grows back will not cause the output of the AND gate to change. Secondly, the two fusible links are arranged orthogonal to each other in layout. This minimizes the possibility of the regrowth of both the blown fuses when electromigration and thermal expansion act only in a fixed direction [Erdi 1975]. Thus, for these reasons, it will improve the reliability of programmed data.

Although the dual fuse logic circuit increases the trimming circuit area by about 30 % to 40 % and causes a longer programming time, for area aspect, this can be acceptable. Firstly, the area increase for one fuse is less than 5 % of the area of the main clock generator circuit. Secondly, for programming time aspect, if the programmed data is logic '1', the fusible link needs not to be blown, hence counteracting the increase of programming time in volume production.

Figure 7.4.2: Schematic diagram of a fuse cell module

Referring to Figure 7.4.2, the programming procedure of the fusible links is described as follows. The programming of the fusible links goes through two phases of operation, testing phase and programming phase. During testing phase, the programming bit B_{prog} , which is connected to all the fuse cell modules, is set low (digital '0') whilst the test bit B_{test} , which is connected to the multiplexer (MUX) of all the fuse cell modules, is asserted (digital '1'). When B_{test} is '1', the value of the input program data bit B_{pdata} of the respective module will be the value of the MUX output bit B_{out} in each module, where each B_{out} is connected to one of the data bits B_0 to B_{n-1} of the ring oscillator shown in Figure 7.2.1. The program data bits (B_{pdata}) will then be adjusted to their finalized values after the desired clock period has been attained. These finalized values will be used as fuse data in the programming phase for deciding whether the fusible links are to be blown so as to ensure the fuse data bit B_{fdata} to be the same as that of B_{pdata} (refer to the inputs of the MUX in Figure 7.4.2).

The main operation in the programming phase is to blow the two fusible links F_1 and F_2 successively, one after another, for each fuse cell module. It is important to note that when the fusible links are not blown, fuse data bit B_{fdata} is at '1'. This is because the fusible links, which are biased by NMOS current sources M_{nfb1} and M_{nfb2} respectively, pulls the input voltages of the AND gate to high, which gives a '1' to B_{fdata} . For this reason, if those fuse cell modules that have finalized data bits (B_{pdata}) as digital '1', the programming phase is omitted. On the contrary, when the finalized B_{pdata} is '0', the operation will go into the programming phase. During programming phase, since fuse F_1 is the first fusible link to be blown, the fuse select bits B_{fs1} is first pulled high to turn on the programming switch M_{pfp1} . The programming bit B_{prog} is then enabled to switch on the large-sized NMOS transistor M_{nfl1} (by setting to '1') to drive huge current through it so as to blow the fusible link F_1 . When the blowing of F_1 is completed, B_{prog} is set back to '0' to facilitate the setting up of data for programming the second fusible link F_2 and to prevent false-blowing of other fusible links. After that, the cycle is repeated again for the second fusible link. It is noted that the PMOS transistors at the input of the AND gate are switched off when B_{prog} is '1'. This is to prevent the huge fuse-blowing current from damaging the inputs of the AND gate. It is also noted that pull-down resistors R_{pd1} and R_{pd2} switch off the large-sized NMOS transistors M_{nfl1} and M_{nfl2} respectively during normal operation (B_{prog} is '0') in order to prevent the possibility of false-blowing the corresponding fusible links.

For the above operation, all the settings of the digital bits are provided by the SIPO register, with the objective to minimize the number of external pins required for programming based on the serial data input. The register is implemented using cascaded shift registers that convert the serial data input (serial data in) into parallel data bits, which are presented at the output of the shift registers. Thus, the parallel data are then used to set all the corresponding digital bits during the programming of the fusible links.

The same trimming procedure is employed for calibrating the gain and offset in the gain stage as well as the scaling output amplifier.

7.5 Results and Discussions

The clock generator is implemented using 4-bit trimming, B_0 to B_3 . Therefore, only four branches of Miller capacitors paths and four fuse cell modules are required. The circuit has been fabricated using AMS (Austria Mikro Systeme International AG) $0.6\text{ }\mu\text{m}$ n-well CMOS process. The sizes of the Miller capacitors and the transistors that implement the ring oscillator are listed in Table 7.5.1. All the transistors in the ring oscillator are in minimum channel length of $0.6\text{ }\mu\text{m}$ and the capacitance of the Miller capacitor array are digitally trimmed in steps of 0.375 pF . The channel widths of the large-sized NMOS transistors M_{nfl1} and M_{nfl2} , which are responsible to blow the fusible links, are selected to ensure the driving current is large enough to blow the fusible link. The fusible links are implemented using standard poly resistor with the size of $1.1\text{ }\mu\text{m}$ by $0.6\text{ }\mu\text{m}$. The clock divider combined with the JK toggle flip-flop gives a total division factor of 16. The clock generator circuit occupies an area of $590 \times 150\text{ }\mu\text{m}^2$ while each of the fuse cell modules occupies an area of $250 \times 36\text{ }\mu\text{m}^2$. The microphotograph for the clock generator (excluding the fuse cell module) and the orthogonal fusible link layout are shown in Figure 7.5.1 and Figure 7.5.2, respectively.

Table 7.5.1: Dimensions of devices in the proposed programmable Miller current-starved inverter ring oscillator

Stage 1		Stage 2		Stage 3	
M_{p1}	$W/L = 2.2\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{p3}	$W/L = 2.2\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{p5}	$W/L = 2.2\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$
M_{p2}	$W/L = 2.2\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{p4}	$W/L = 2.2\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{p6}	$W/L = 2.2\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$
C_{1b3}	3 pF	C_{2b3}	3 pF	C_{3b3}	3 pF
C_{1b2}	1.5 pF	C_{2b2}	1.5 pF	C_{3b2}	1.5 pF
C_{1b1}	0.75 pF	C_{2b1}	0.75 pF	C_{3b1}	0.75 pF
C_{1b0}	0.375 pF	C_{2b0}	0.375 pF	C_{3b0}	0.375 pF
M_{n2}	$W/L = 1.4\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{n4}	$W/L = 1.4\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{n6}	$W/L = 1.4\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$
M_{n1}	$W/L = 1.4\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{n3}	$W/L = 1.4\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$	M_{n5}	$W/L = 1.4\text{ }\mu\text{m}/0.6\text{ }\mu\text{m}$

Figure 7.5.1: Layout (top) and Microphotograph (bottom) of the clock generator circuit

Figure 7.5.2: Layout (left) and Microphotograph (right) of the orthogonal fusible link layout

Figure 7.5.3 shows the timing clock signals T_{1a} , T_1 , T_{2a} , T_2 and T_n at 106.8 kHz with only 3 pF Miller capacitor. It was measured using Hewlett Packard 54645D 100 MHz Mixed Signal Oscilloscope. The period of the non-overlapping region was measured to be 10 ns. It is highlighted using the dash-circles and the arrows.

Figure 7.5.3: Experimental results of clock generator outputs showing timing clock signals T_{1a} , T_1 , T_{2a} , T_2 and T_n

To evaluate the jitter performance, Tektronix TDS350 200 MHz oscilloscope was employed. It has functions that can detect the change in supply voltages and the jitter of clock signals. Figure 7.5.4 and Figure 7.5.5 were plotted to show the jitter of clock signal with changes in supply voltage of +/- 10 %.

Figure 7.5.4: Experimental results of T_1 rising edge jitter

Figure 7.5.5: Experimental results of T_1 falling edge jitter

Figure 7.5.4 shows the result of the jitter of the rising edge of T_1 while Figure 7.5.5 shows the jitter of the falling edge. The two figures have illustrated that the jitter of the output clock T_1 , which is subject to $\pm 0.5\text{ V}$ ($\pm 10\%$) variation of the power supply, is less than 300 ps. Note that the measurement was taken using cursor measurement mode (dashed circle), which could only resolve the time difference down to 100 ps (minimum step). The same jitter value was obtained for all other clock periods. A plot of the tunable clock periods against capacitance values in a step of 0.375 pF is shown in Figure 7.5.6. The plot has indicated a linear relationship between the clock period and the value of Miller capacitor. The corresponding measured frequencies of the tunable periods were translated in Table 7.5.2. It can be seen that the clock frequency obtained from four divider stages, is tunable from 56 kHz to 1.024 MHz for value of Miller capacitor ranging from 0.375 pF to 5.625 pF. This frequency range is suitable for most of the low-frequency based switched-capacitor circuit applications.

Figure 7.5.6: Experimental results showing the clock period versus the value of Miller capacitor

Table 7.5.2: Experimental results of measured tunable clock periods and clock frequencies

B ₃	B ₂	B ₁	B ₀	Total Capacitance of Miller Capacitors [pF]	Clock Period [μs]	Jitter Error (300ps / Clock Period) [ppm]	Clock Frequency [kHz]
0	0	0	1	0.375	0.96	313	1042
0	0	1	0	0.75	2.19	137	457
0	0	1	1	1.125	3.38	89	296
0	1	0	0	1.5	4.6	65	217
0	1	0	1	1.875	5.74	52	174
0	1	1	0	2.25	6.98	43	143
0	1	1	1	2.625	8.18	37	122
1	0	0	0	3	9.42	32	106
1	0	0	1	3.375	10.45	29	96
1	0	1	0	3.75	11.7	26	85
1	0	1	1	4.125	12.9	23	78
1	1	0	0	4.5	14.2	21	70
1	1	0	1	4.875	15.35	20	65
1	1	1	0	5.25	16.6	18	60
1	1	1	1	5.625	17.8	17	56

Table 7.5.3 summarizes the first stage capacitance values required for the conventional three-stage ring oscillator (Figure 7.3.1), conventional current-starved inverter ring oscillator [Hajimiri 1999] and the proposed Miller current-starved inverter ring oscillator. The capacitance values are compared based on identical tuning range and identical inverter size. Note that C_{dr1b0} , C_{dr1b1} , C_{dr1b2} and C_{dr1b3} represent the tunable delay capacitors of which one end is connected to ground. As can be seen from the table, the total capacitance required for proposed method is 16.875 pF, whereas for the conventional ring oscillator is 81 pF and for the conventional current-starved inverter ring oscillator is 49.5 pF. Therefore, a total reduction of capacitance over conventional ring oscillator is 64.125 pF (about five times) and over the latter one is 32.625 pF (about three times). This has confirmed that a substantial reduction of area is achieved in the proposed method.

Table 7.5.4 shows the results of the output frequency of the three ring oscillators using identical capacitor values of 4.875 pF. The result has shown that the proposed method has a reduction of 5 times the oscillation frequency over the conventional ring oscillator and 3 times over the conventional current-starved inverter ring oscillator. Hence, this leads to the relaxation of PSRR requirement of the analog circuits in mixed-signal environment.

Table 7.5.3: Comparison of the capacitance values requirement for three types of ring oscillators (only one stage listed)

Conventional Ring Oscillator (Figure 7.3.1)		Conventional Current-starved Inverter Ring Oscillator [Hajimiri 1999]		Proposed Miller Current-starved Inverter Ring Oscillator	
M_{pr1}	$W/L = 2.2 \mu\text{m}/0.6 \mu\text{m}$	M_{p1}	$W/L = 2.2 \mu\text{m}/0.6 \mu\text{m}$	M_{p1}	$W/L = 2.2 \mu\text{m}/0.6 \mu\text{m}$
		M_{p2}	$W/L = 2.2 \mu\text{m}/0.6 \mu\text{m}$	M_{p2}	$W/L = 2.2 \mu\text{m}/0.6 \mu\text{m}$
C_{dr1b3}	14.4 pF	C_{dr1b3}	8.8 pF	C_{1b3}	3 pF
C_{dr1b2}	7.2 pF	C_{dr1b2}	4.4 pF	C_{1b2}	1.5 pF
C_{dr1b1}	3.6 pF	C_{dr1b1}	2.2 pF	C_{1b1}	0.75 pF
C_{dr1b0}	1.8 pF	C_{dr1b0}	1.1 pF	C_{1b0}	0.375 pF
		M_{n2}	$W/L = 1.4 \mu\text{m}/0.6 \mu\text{m}$	M_{n2}	$W/L = 1.4 \mu\text{m}/0.6 \mu\text{m}$
M_{nr1}	$W/L = 1.4 \mu\text{m}/0.6 \mu\text{m}$	M_{n1}	$W/L = 1.4 \mu\text{m}/0.6 \mu\text{m}$	M_{n1}	$W/L = 1.4 \mu\text{m}/0.6 \mu\text{m}$

Table 7.5.4: Comparison of the output frequency of three types of ring oscillators using identical capacitor value

	Conventional Ring Oscillator (Figure 7.3.1)	Conventional Current-starved Inverter Ring Oscillator [Hajimiri 1999]	Proposed Miller Current-starved Inverter Ring Oscillator
Oscillator frequency (Values of all capacitor = 4.875 pF)	5 MHz	3 MHz	1 MHz
Normalized oscillation frequency with reference to the proposed work	5	3	1

CHAPTER 8

Results and Discussions

8.1 Overview

The entire ASIC, including the interface circuit, the signal-conditioning circuits, the clock generator and calibration circuits, is fabricated using AMS (Austria Mikro Systeme International AG) 0.6 μm n-well CMOS process. The design and layout procedures are described in Appendix C. The current consumption for the ASIC is designed to be 2 mA in typical condition. The die size of the ASIC is 2.8 mm by 2.3 mm. The ASIC is bonded to a ± 50 g commercial sensing element in a 16-pin DIL package. The microphotograph of the entire accelerometer system IC is shown in Figure 8.1.1.

Figure 8.1.1: Microphotograph of the accelerometer system IC in a 16-pin DIL package

A series of measurements for the ± 50 g accelerometer IC were taken. The time-domain measurement results were plotted using an oscilloscope (HP 54645D MegaZoom Mixed-Signal oscilloscope) whereas the spectral plots were obtained using a network analyzer (Stanford Research Systems Model SR770 FFT Network Analyzer). The acceleration excitation to the accelerometer IC was performed using a vibration shaker (Ling Dynamic Systems LDS V406) together with a sinusoidal function generator.

8.2 Results and Discussions

The measured output spectrum in Figure 8.2.1 shows the fundamental, its harmonic contents together with the noise floor of the output voltage for ± 50 g excitation at 500 Hz. The odd harmonics of the signal are due to the non-linearity of the differential capacitive sensor [Baxter-1997] whilst the even harmonics are arising from the mismatched between the two sensing capacitors, C_{S1} and C_{S2} .

Figure 8.2.1: Measured output spectrum of the ASIC for full-scale ± 50 g excitation at 500 Hz

The output noise power spectral density plot is shown in Figure 8.2.2. A maximum output noise root spectral density of $11.87 \mu\text{Vpk}/\sqrt{\text{Hz}}$, equivalent to rms (root-mean-square) noise root spectral density of $0.187 \text{ mg}/\sqrt{\text{Hz}}$, at frequency of 15.63 Hz is obtained. This corresponds to a dynamic range of 77 dB for 500 Hz bandwidth and 74 dB for 1 kHz bandwidth based on a 2-pole filter bandwidth using bandwidth scaling factor of 1.4 [AD 1999] for a 50 g input with sensitivity of 45 mV/g . The ASIC contributes lower noise root spectral density value than the well-known accelerometers. For applications with bandwidth of 100 Hz , the accelerometer IC can attain a dynamic range of 84 dB .

Figure 8.2.2: Measured noise root spectral density

The time-domain clock noise at the ASIC output is shown in Figure 8.2.3. It has demonstrated the filtering stage is effective in reducing the clock noise to 1.562 mVpp. The results are better than that of the commercial products [AD 1998], [Motorola 2001], confirming that effectiveness of the proposed INS switch that can improve the resolution and noise performance of the readout circuit on the basis of circuit simplification.

Figure 8.2.3: Measured time domain clock noise

Furthermore, Figure 8.2.4 shows the measured time domain response of ± 50 g excitation at 500 Hz. The excitation of ± 50 g caused the output voltage to swing with a full-scale magnitude of 4.5 Vpp. Figure 8.2.5 shows the peak-to-peak output voltage plot for the range of acceleration excitation from 0 to ± 50 g. The measured data points are plotted together with the best-fit line. It can be observed that the transfer function is quite linear. Figure 8.2.6 shows the plot of the percentage linearity error against acceleration excitation. The percentage linearity error is calculated from the following expression:

$$\left(\frac{\text{Measured Output} - \text{Actual Fitted Output}}{\text{Actual Fitted Output}} \times 100\% \right)$$

From the plot, a maximum linearity error of 0.71% is obtained. It is within 1% of the non-linearity specification stated in Table 1.2.1. The linearity error is still acceptable for automobile air-bag applications.

Figure 8.2.4: Measured time domain output voltage of the ASIC for full-scale ± 50 g excitation at 500 Hz

Figure 8.2.5: Measured peak-to-peak AC output voltage against acceleration excitation at 500 Hz

Figure 8.2.6: Measured percentage linearity error against acceleration excitation at 500 Hz

Finally, Figure 8.2.7 shows the measured self-test response. The transient response of the mechanical sensor under self-test condition has shown that it is a 2nd order system response as described by Equation (3.2.2.3) in Chapter 3. This correlates well with the proposed sensor model with the inclusion of 2nd order effect. An output voltage of 1.547 V, equivalent to 34.4 g, under self-test mode is obtained. It is large enough for easy detection. This relaxes the resolution of the comparator design for indicating fault in the sensing element.

Figure 8.2.7: Measured output response under self-test mode

The experimental results of fabricated chip have met all the specifications listed in Table 1.2.1. In order to evaluate the entire performance of proposed accelerometer system IC, the measured results on the basis of key parameters are compared with that of the commercial products [AD 1996], [AD 1998] and [Motorola 2001] in Table 8.2.1.

Table 8.2.1: Comparison of performance with popular commercial accelerometers

Specification	Analog Devices ADXL50 [AD 1996]	Analog Devices ADXL150 [AD 1998]	Motorola MMA2202D [Motorola 2001]	This Work
Supply Current	10 mA	1.8 mA	5 mA	2 mA
Operating Power at 5 V	50 mW	9 mW	25 mW	10 mW
Output Noise Root Spectral Density in peak value (in V _{pk} /√Hz)	-----	-----	110 μV _{pk} /√Hz	11.87 μV _{pk} /√Hz at 15.63 Hz
RMS Noise Level (in V _{rms})	-----	-----	2.8 mV _{rms} (1 kHz BW)	0.314 mV _{rms} (1 kHz BW)
Output Noise Root Spectral Density in rms value (in g/√Hz)	6.6 mg/√Hz	1 mg/√Hz	-----	0.187 mg/√Hz at 15.63 Hz
RMS Noise Level (in g rms)	----- ----- 66 mg (100 Hz BW) ----- -----	32 mg (1 kHz BW) ----- ----- 10 mg (100 Hz BW)	----- ----- ----- ----- -----	7 mg (1 kHz BW) 5 mg (500 Hz BW) 2.2 mg (100 Hz BW)
Clock Noise	----- -----	5 mV _{pp} -----	----- 2 mV _{pk}	1.562 mV _{pp} 0.781 mV _{pk}
Self Test Output Change	1 V -----	0.4 V -----	----- 12 g	1.547 V 34.4 g
-3 dB Bandwidth	dc to 1.3 kHz	dc to 1 kHz	dc to 400 Hz	dc to 1 kHz
Sensitivity	19 mV/g	38 mV/g	40 mV/g	45 mV/g
Acceleration Range	±50 g	±50 g	±47 g	±50 g
Full-scale Output Voltage Range for ±50 g	0.85 V to 2.75 V *	0.6 V to 4.4 V **	0.62 V to 4.38 V	0.25 V to 4.75 V
Power Supply	5 V	5 V	5 V	5 V
Non-Linearity	0.2 %	0.2 %	1 %	1 %
Integration Approach	Fully-integrated	Fully-integrated	Two-chip	Two-chip

* For full 5 V swing (0.25 V to 4.75 V), external resistor network is needed.

** For full 5 V swing (0.25 V to 4.75 V), external amplifier and resistor network are needed.

The measured power consumption of the proposed system IC is comparable with ADXL150 and is lower than others. As in the case of ADXL150, external amplifier and resistor network are needed for maximum output range of 0.25 V to 4.75 V, whereas the proposed work eliminates external active circuit completely.

Here are some comments on the measurement results. The low noise spectral density is due to the simple CDS structure of the front-end interface. In addition, benefited from the INS-based design, lesser switching components reduce the fundamental KT/C noise and the potential switching noise in the SC system. The high self-test output voltage is attained due to a better implementation of the test strategy and the test structure of the front-end interface circuit. The low clock noise is the combined result of the reduced complexity of the clock generator, the INS large time-constant SCF and 3rd-order CTF filtering stage. The non-linearity of one percent is acceptable because the open-loop system is adopted.

Table 8.2.2 gives the comparison of the reported works from Table 2.3.2.1 and the recent reported works with that of the proposed work. In order to evaluate the performance of different sensing interface circuits, a figure of merit (FOM) is introduced. It is defined as the product of spectral noise and power, i.e.

$$\text{FOM} = (\text{rms output noise root spectral density}) \times (\text{power dissipation}).$$

The lower the FOM, the better is the tradeoff in terms of power and noise. Note that the unit for FOM is $\text{W-V}/\sqrt{\text{Hz}}$.

Table 8.2.2: Comparison of reported works (Table 2.3.2.1) with this work

Reference and Techniques	RMS Output Noise Root Spectral Density	Power Dissipation	FOM	Area and Technology	Self-test Function
[Kuehnel 1994] Fully-integrated, Closed-loop, CHS using high BW FD amplifier	98 $\mu\text{V}/\sqrt{\text{Hz}}$	50 mW (10 mA at 5 V)	4.9 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3 x 3 mm ² (3 μm BiCMOS process)	Yes
[AD 1996] ADXL50 Fully-integrated, Closed-loop, CHS using high BW FD amplifier	125 $\mu\text{V}/\sqrt{\text{Hz}}$	50 mW (10 mA at 5 V)	6.25 $\mu\text{W-V}/\sqrt{\text{Hz}}$	-----	Yes
[Chau 1996] Fully-integrated, Closed-loop, CHS using high BW FD amplifier	120 $\mu\text{V}/\sqrt{\text{Hz}}$	40 mW (8 mA at 5 V)	4.8 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3 x 3 mm ² (3 μm BiCMOS process)	Yes
[AD 1998] ADXL150 Fully-integrated, Open-loop, CHS using high BW FD amplifier	38 $\mu\text{V}/\sqrt{\text{Hz}}$	9 mW (1.8 mA at 5 V)	0.342 $\mu\text{W-V}/\sqrt{\text{Hz}}$	-----	Yes
[Lemkin 1999] Fully-integrated, Closed-loop, 1-bit 2 nd -order $\Sigma\Delta$ modulator, charge integrator using FD amplifier	4.4 $\mu\text{V}/\sqrt{\text{Hz}}$ (x-axis)	45mW (9 mA at 5 V) (x-axis) excluding digital filter	0.198 $\mu\text{W-V}/\sqrt{\text{Hz}}$ (x-axis)	4 x 4 mm ² (2 μm CMOS MEMS process)	No
[Kulah 2000] Two-chip approach, Closed-loop, 1-bit 1 st -order $\Sigma\Delta$ modulator, CDS front-end charge integrator	110 $\mu\text{V}/\sqrt{\text{Hz}}$	7.2 mW (1.44 mA at 5 V) excluding digital filter	0.792 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3.4 x 3.6 mm ² (3 μm CMOS process)	No
[Motorola 2001] MMA2202D Two-chip approach, Open-loop, CDS	110 $\mu\text{V}/\sqrt{\text{Hz}}$	25 mW (5 mA at 5 V)	2.75 $\mu\text{W-V}/\sqrt{\text{Hz}}$	-----	Yes
[Baschiroto 2003] Two-Chip approach, Open-loop, CDS using FD amplifier	26.1 $\mu\text{V}/\sqrt{\text{Hz}}$	22.5 mW (4.5 mA at 5 V)	0.58725 $\mu\text{W-V}/\sqrt{\text{Hz}}$	2.60 x 2.84 mm ² (0.5 μm CMOS process)	Yes
[Wu 2004] Sensor-integrated, Open-loop, CHS using high BW amplifier	6.5 $\mu\text{V}/\sqrt{\text{Hz}}$	30 mW (6 mA at 5 V) excluding differential-to-single- ended amplifier and off-chip components	0.195 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3.5 x 2.5 mm ² (0.5 μm CMOS MEMS process)	No
[Amini 2004] Two-Chip approach, Open-loop, 1 st -order $\Sigma\Delta$ modulator	55 $\mu\text{V}/\sqrt{\text{Hz}}$	6 mW (2.4 mA at 2.5V)	0.33 $\mu\text{W-V}/\sqrt{\text{Hz}}$	2 x 2 mm ² (0.25 μm CMOS process)	No

Reference and Techniques	RMS Output Noise Root Spectral Density	Power Dissipation	FOM	Area and Technology	Self-test Function
[Petkov 2005] Two-Chip approach, Open-loop, 4 th -order $\Sigma\Delta$ modulator	13.5 $\mu\text{V}/\sqrt{\text{Hz}}$	18 mW (3.6 mA at 5V)	0.243 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	2.3 x 2.3 mm ² (0.5 μm CMOS process)	No
[This work] Two-chip approach, Open-loop, CDS using single- ended amplifier with INS	8.4 $\mu\text{V}/\sqrt{\text{Hz}}$	10 mW (2 mA at 5 V)	0.084 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	2.8 x 2.3 mm ² (0.6 μm CMOS process)	Yes

Figure 8.2.8: Comparison of the reported works with this work using FOM

Figure 8.2.8 plots the comparison of the previous reported works with this work using FOM. It can be seen from the plot that the result of this work has exhibited the best FOM value among the reported works. In summary, it has verified that the proposed accelerometer IC in conjunction with its design methodologies is promising for obtaining the optimum tradeoff in realization of low-power, low-noise accelerometer systems.

CHAPTER 9

Conclusions and Recommendations

9.1 Conclusions

A direct and convenient electrical modeling method for acceleration capacitive sensor has been presented. The behavior of the model reflects direct change of capacitance due to external acceleration and electrostatic actuation force. Equations have been derived for both cases and the parasitic effects in the MEMS acceleration sensor have been considered. The model is easy to implement in common Spice program. Simulation results have confirmed that the effects of the parasitic, such as leakage current, are important parameters to be modeled in order for the successful implementation of the accelerometer system. This electrical modeling method can be applied to other related type of capacitive sensors.

A circuit technique using the injection-nulling switch to minimize the charge injection and clock feedthrough errors in switched-capacitor circuits had been presented. The INS was implemented in a sample-and-hold circuit for comparison. The experimental results of the INS technique was compared to those of conventional switch element methods using single MOS transistor and dummy switch approach. The experimental evidences have shown that there is an improvement on the reduction of the channel charge injection error and the clock feedthrough error over the conventional switch techniques. The main reason is that the INS employs identical switches, which enables more effective compensation of switch errors. In addition, the implementation and matching of the switch are simpler and easier. This also favors the application of INS on discrete switched-capacitor applications. Besides, the INS can also be modified to have both terminals (terminal L and H) to include a nulling

switch and a nulling capacitor if compensation is needed on both terminals. Hence, this will make INS attractive for a broad range of switched-capacitor applications with minimum effort in design.

The circuit techniques for designing a low-cost programmable clock generator for low-frequency switched-capacitor applications have been presented. The proposed low-frequency ring oscillator offers implementation advantages of low oscillation frequency with small capacitor values and eliminating the use of weak inverter that affects the jitter performance. Incorporating the fusible link technique, it allows frequencies to be digitally tuned for more than a decade. The experimental results have verified that the clock generator has achieved a wide frequency tuning range and displayed low jitter. The proposed techniques are useful in implementing on-chip clock generator for switched-capacitor circuit applications. The reduction of oscillation frequency from that of the conventional methods is substantial and has the potential to decrease further if area requirement permits. This benefits the reduction of switching noise in the overall system.

The orthogonal fusible link structure employed in the trimming circuit has been presented. The technique adds extra protection to the programmed data and lowers the possibility of regrowth of blown fuse. Hence, it improves the reliability of programmed clock signals as well as the calibrated output signal of the accelerometer. In addition, it is low-cost and is readily implemented in standard CMOS process. This technique has a good potential in calibration circuits that operate in an environment having fuse regrowth problem, or that requires higher reliability on the programmed data.

A low-power interface and signal-conditioning ASIC for automotive accelerometers in standard CMOS technology has been presented. The design of SC modules in the

accelerometer system using INS has several benefits. Firstly, the design of the front-end sense amplifier using INS has shown that the circuit is insensitive to variation of process parameters and provides precision improvement over that of the dummy switch topology. This is because the switch structure utilizes an identical auxiliary switch design to compensate the errors arising from the main operating switch. Hence, this robustness against the variation of process parameters will result in the increase of yield in the final product. Secondly, the enhancement on the circuit simplicity in the sense amplifier offers ease of self-test design without the need of complicated structure. Thirdly, the reduction of the power consumption on the opamps in the sense amplifier and filter stage has decreased power dissipation of the overall system IC significantly. This is a favorable property for automotive application, especially in the air-bag system. Fourthly, the decrease in complexity of the SC circuit has yielded a low-noise system, which increases the dynamic range of the accelerometer.

The experimental evidences have confirmed that the proposed INS based accelerometer ASIC design leads to a high dynamic range system whilst maintaining simplicity that improves the performance significantly in terms of power consumption, noise, accuracy, resolution and integrated capability. The performance results were compared and have indicated a significant improvement over those of the well-known commercial products and reported prior-art works. More importantly, this gives an attractive low-cost, fully-integrated solution for automotive accelerometers.

In summary, the project has investigated numerous circuit techniques for the design of a low-power, high-performance capacitive-based automobile accelerometer. The proposed techniques, being applied to the implementation of an accelerometer system, have met the objectives of the overall project.

9.2 Recommendations for further research

During the beginning stage, there was a dilemma of whether to choose in-chip trimming or off-chip trimming. The in-chip trimming method making use of fusible-link technique was proposed on the basis of simplicity. Nevertheless, due to the increased processing power of the automobile IC controller, an off-chip trimming seems to be a promising approach because it offers better calibration in view of the potential drift problem of the accelerometer sensor IC.

Further research will focus on finding algorithms for converting the untrimmed output from the accelerometer into the actual acceleration readout. An initial mechanical and/or electrical static testing method will also be devised to collect the typical calibration data of the newly-fabricated accelerometers. The proposed system block diagram is illustrated in Figure 9.2.1. These default calibration data will serve as the setup data for the initial calibration phase. The data will be re-adjusted through the feedback logic formed by the DSP and the accelerometer IC. The advantage of using this DSP method is that the trimming process is versatile. It can solve the inaccuracy of the trimming data due to a change in condition or aging of the accelerometer IC because the trimming procedure can be performed whenever it is necessary. Not only does it reduce the cost of the ASIC, it also increases the system flexibility.

Figure 9.2.1: Mechanical and/or electrical testing for collection of calibration data

The employment of INS has demonstrated a promising way to implement low-power, low-noise, high resolution ± 50 g accelerometer ASIC for automotive air-bag system. The use of the INS on low-g accelerometer can also be explored for implementing a low-cost earthquake early-warning home-alarm system. This system has great potential because it is important for the safety of people that live in earthquake-prone countries. The low acceleration property of the earthquake has also raised a challenge on the design of low-noise high-resolution low-g accelerometer, where the INS can be adopted.

The low-power, low switch error switched-capacitor interfacing technique can also be extended to a variety of capacitive sensors such as pressure sensors and biologically sensors. Thus, it is worthwhile to investigate the possibility of generalizing low-power interface topologies for various types of sensor structures. Generalized interface topologies can yield a versatile sensor interface solution that will reduce the development time and hence minimizing the time-to-revenue for ASIC circuit designers.

The concepts of error minimization using INS are also applicable to other switched-capacitor circuits as well. These include ADC, DAC, switched-opamps and switched-current circuits. Ultimately, these circuits will offer improved resolution and enhanced system performance.

Author's Publications

Patent

- [Lee 2005a] W. F. Lee and P. K. Chan, "A method for nulling charge injection in switched networks", *Patent No. US 6,850,098 B2, February 1, 2005.*

Publications

- [Lee 1999a] W. F. Lee, P. K. Chan, L. Siek, "Electrical modeling of MEMS sensor for integrated accelerometer applications", *Proceedings 1999 IEEE Hong Kong Electron Devices Meeting*, pp.88-91, June 1999.
- [Lee 1999b] W. F. Lee, P. K. Chan, L. Siek, M.C.Yeo, S.Y.Chui, "An ASM-based ASIC for automobile accelerometer applications", *The First IEEE Asia Pacific Conference on ASICs*, pp.127-130, August 1999.
- [Lee 2005b] W. F. Lee and P. K. Chan, "An injection-nulling switch for switched-capacitor circuit applications", *IEEE Transactions on Instrumentation and Measurement*, vol.54, no.6, pp.2416-2426, December 2005. (Regular Paper)
- [Lee 2006] W. F. Lee and P. K. Chan, "A low-cost programmable clock generator for switched-capacitor circuit applications", *accepted by Analog Integrated Circuits and Signal Processing*, to be appeared in 2006. (Regular Paper)

Papers in Reviewing Process

- [Lee 2004] W. F. Lee and P. K. Chan, "A low-power low-noise ASIC for capacitive-based automotive accelerometers", *Paper has been submitted as regular paper. It is in the reviewing process.*

Bibliography

Research Papers and Articles

- [AD 1996] Analog Devices Inc., Norwood, USA, "ADXL50 - Monolithic accelerometer with signal conditioning", data sheet, rev. B, 1996.
- [AD 1998] Analog Devices Inc., Norwood, USA, "ADXL150 / ADXL250 - $\pm 5g$ to $\pm 50g$, low noise, low power, single / dual axis iMEMS accelerometers", data sheet, rev. 0, 1998.
- [AD 1999] Analog Devices Inc., "ADXL105 - High accuracy $\pm 1g$ to $\pm 5g$ single axis iMEMS accelerometer with analog input", data sheet, rev. A, 1999.
- [Ahmad 1997] Haidar Ahmad, Asim J. Al-Khalili, Les M. Landsberger and Mojtaba Kahrizi, "A two-dimensional micromachined accelerometer", *IEEE Transactions on Instrumentation and Measurement*, vol.46, no.1, pp.18-26, February 1997.
- [Allemandou 1966] P. Allemandou, "Low-pass filters approximating-in modulus and phase-the exponential function", *IEEE Transactions on Circuit Theory*, vol.CT-13, no.2, pp.298-301, September 1966.
- [Alvarez 1995] Jose Alvarez, Hector Sanchez, Gianfranco Gerosa and Roger Countryman, "A wide-bandwidth low-voltage PLL for PowerPCTM microprocessors", *IEEE Journal of Solid-State Circuits*, vol.30, no.4, pp.383-391, April 1995.
- [Amendola 2001] Gilles Amendola, Guo-Neng Lu and Lionel Babadjian, "Signal-processing electronics for a capacitive micro-sensor", *Analog Integrated Circuits and Signal Processing*, vol.29, no.1-2, pp. 105-113, October-November 2001.
- [Amini 2004] Babak Vakili Amini and Farrokh Ayazi, "A 2.5-V 14-bit $\Sigma\Delta$ CMOS SOI capacitive accelerometer", *IEEE Journal of Solid-State Circuits*, vol.39, no.12, pp.2467-2476, December 2004.
- [Angulo 1987] Jaime Ramírez-Angulo, Randall L. Geiger and Edgar Sánchez-Sinencio, "Characterization, evaluation, and comparison of laser-trimmed film resistors", *IEEE Journal of Solid-State Circuits*, vol.SC-22, no.6, pp.1177-1189, December 1987.
- [Angulo 1988] Jaime Ramírez-Angulo and Randall L. Geiger, "New laser-trimmed film resistor structures for very high stability requirements", *IEEE Transactions on Electron Devices*, vol.35, no.4, pp.516-518, April 1988.

- [Aziz 1996] Pervez M. Aziz, Henrik V. Sorensen and Jan Van Der Spiegel, "An overview of sigma-delta converters", *IEEE Signal Processing Magazine*, pp.61-84, January 1996.
- [Baird 1994] Rex T. Baird and Terri S. Fiez, "Stability analysis of high-order delta-sigma modulation for ADC's", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol.41, no.1, pp.59-62, January 1994.
- [Balabanian 1963] N. Balabanian and B. Patel, "Active realization of complex zeros", *IEEE Transactions on Circuit Theory (Correspondence)*, vol.CT-10, pp.299-300, July 1963.
- [Baschiroto 2003] Andrea Baschiroto, A. Gola, E. Chiesa, E. Lasalandra, F. Pasolini, M. Tronconi and T. Ungaretti, "A ± 1 -g dual-axis linear accelerometer in a standard 0.5- μ m CMOS technology for high-sensitivity applications", *IEEE Journal of Solid-State Circuits*, vol.38, no.7, pp.1292-1297, July 2003.
- [Beex 1992] A.A. (Louis) Beex and Monique P. Fargues, "Analysis of clock jitter in switched-capacitor systems", *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol.39, no.7, pp.506-519, July 1992.
- [Boser 1988] Bernhard E. Boser and Bruce A. Wooley, "The design of sigma-delta modulation analog-to-digital converters", *IEEE Journal of Solid-State Circuits*, vol.23, no.6, pp.1298-1308, December 1988.
- [Boser 1996] Bernhard E. Boser and Roger T. Howe, "Surface micromachined accelerometer", *IEEE Journal of Solid-State Circuits*, vol.31, no.3, pp.366-375, March 1996.
- [Boxenhorn 1990] Burton Boxenhorn and Paul Greiff, "Monolithic silicon accelerometer", *Sensors and Actuators A: Physical*, vol.A21-A23, pp.273-277, 1990.
- [Brodersen 1976] Robert W. Brodersen and Stephen P. Emmons, "Noise in buried channel charge-coupled devices", *IEEE Journal of Solid-State Circuits*, vol.SC-11, no.1, pp.147-155, December 1976.
- [Brokaw 1996] A. Paul Brokaw, "A temperature sensor with single resistor set-point programming", *IEEE Journal of Solid-State Circuits*, vol.31, no.12, pp.1908-1915, December 1996.
- [Bulger 1975] Gray A. Bulger, "Stability analysis of laser trimmed thin film resistors", *IEEE Transactions on Parts, Hybrids, and Packaging*, vol.PHP-11, no.3, pp.172-177, September 1975.
- [Burbaum 1991] C. Burbaum, J. Mohr and P. Bley, "Fabrication of capacitive acceleration sensors by the LIGA technique", *Sensors and Actuators A: Physical*, vol.A25-A27, pp.559-563, 1991.

- [Burstein 1996] Amit Burstein and William J. Kaiser, "Mixed analog-digital highly sensitive sensor interface circuit for low-cost microsensors", *Sensors and Actuators A: Physical*, vol.A52, pp.193-197, 1996.
- [Candy 1981] James C. Candy and Oconnell J. Benjamin, "The structure of quantization noise from sigma-delta modulation", *IEEE Transactions on Instrumentation and Measurement*, vol.COM-29, no.9, pp.1316-1323, September 1981.
- [Carley 1989] L. Richard Carley, "Trimming analog circuits using floating-gate analog MOS memory", *IEEE Journal of Solid-State Circuits*, vol.24, no.6, pp.1569-1575, December 1989.
- [Castello 1985] Rinaldo Castello and Paul R. Gray, "Performance limitations in switched-capacitor filters", *IEEE Transactions on Circuits and Systems*, vol.CAS-32, no.9, pp.865-876, September 1985.
- [Chan 1999] P.K. Chan, L.S. Ng, L.Siek, B.L. Tan and C.L. Ang, "Flicker noise optimization for CMOS operational amplifiers", *The 15th International Conference on Noise in Physical Systems and I/F Fluctuations (ICNF)*, Hong Kong, pp.413-416, August, 1999.
- [Chandrakasan 1992] Anantha P. Chandrakasan, Samuel Sheng and Robert W. Brodersen, "Low-power CMOS digital design", *IEEE Journal of Solid-State Circuits*, vol.27, no.4, pp.473-484, April 1992.
- [Chau 1996] K.H.-L. Chau, S.R. Lewis, Y. Zhao, R.T. Howe, S.F. Bart and R.G. Marcheselli, "An integrated force-balanced capacitive accelerometer for low-g applications", *Sensors and Actuators A: Physical*, vol.A54, pp.472-476, 1996.
- [Christiansen 1996] Jørgen Christiansen, "An integrated high resolution CMOS timing generator based on an array of delay locked loops", *IEEE Journal of Solid-State Circuits*, vol.31, no.7, pp.952-957, July 1996.
- [Cole 1991] John C. Cole, "A new sense element technology for accelerometer subsystems", *The 6th International Conference on Solid-State Sensors and Actuators (Transducers '91)*, San Francisco, USA, pp.93-96, June 1991.
- [Costa 1999] João Paulo Costa, Mike Chou and Luís Miguel Silveira, "Efficient techniques for accurate modeling and simulation of substrate coupling in mixed-signal IC's", *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems*, vol.18, no.5, pp.597-607, May 1999.
- [Dai 2002] Liang Dai and Ramesh Harjani, "Design of low-phase-noise CMOS ring oscillators", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol.49, no.5, pp.328-338, May 2002.

- [Dauderstädt 1996] U.A. Dauderstädt, P.H.S. de Vries, R. Hiratsuka, J.G. Korvink, P.M. Sarro, H. Baltes and S. Middelhoek, "Simulation aspects of a thermal accelerometer", *Sensors and Actuators A: Physical*, vol.A55, pp.3-6, 1996.
- [Deluca 2002] Phil Deluca, "A review of thirty-five years of laser trimming with a look to the future", *Proceedings of the IEEE*, vol.90, no.10, pp.1614-1619, October 2002.
- [Drieënhuizen 1997] B.P. van Drieënhuizen, N.I. Maluf, I.E. Opris and G.T.A. Kovacs, "Force-balanced accelerometer with mg resolution, fabricated using silicon fusion bonding and deep reactive ion etching", *The 9th International Conference on Solid-State Sensors and Actuators (Transducers '97)*, Chicago, USA, pp.1229-1230, June 1997.
- [Eichenberger 1990] Christoph Eichenberger and Walter Guggenbuhl, "On charge injection in analog MOS switches and dummy switch compensation techniques", *IEEE Transactions on Circuits and Systems*, vol.37, no.2, pp.256-264, February 1990.
- [Eichenberger 1991] C. Eichenberger and W. Guggenbuhl, "Charge Injection of Analogue CMOS Switches", *IEE Proceedings-G*, vol. 138, no. 2, pp. 155-159, April 1991.
- [Enz 1996] Christian C. Enz and Gabor C. Temes, "Circuit techniques for reducing the effects op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization", *Proceedings of the IEEE*, vol.84, no.11, pp.1584-1614, November 1996.
- [Erdi 1975] George Erdi, "A precision trim technique for monolithic analog circuits", *IEEE Journal of Solid-State Circuits*, vol.SC-10, no.6, pp.412-416, December 1975.
- [Erdi 1979] George Erdi, "A 300 V/ μ s monolithic voltage follower", *IEEE Journal of Solid-State Circuits*, vol.SC-14, no.6, pp.1059-1065, December 1979.
- [Fedder 1996] Gary K. Fedder and Roger T. Howe, "Multimode digital control of a suspended polysilicon microstructure", *Journal of Microelectromechanical Systems*, vol.5, no.4, pp.283-297, December 1996.
- [Foxall 1980] T. Foxall, R. Whitebread, L. Sellars, A. Aitken and J. Morris, "A switched-capacitor bandsplit filter using double polysilicon oxide-isolated CMOS", *1980 Digest of Technical Papers*, pp.90-91, February 1980.
- [Fuller 1994] Robert Fuller and Warren Newman, "Development of a radiation hardened NPN bipolar transistors for a 64K CMOS fusible-link PROM", *IEEE Transactions on Nuclear Science*, vol.41, no.6, pp.2474-2480, December 1994.

- [Gariboldi 1987] Roberto Gariboldi and Marco Morelli, "Very-low-drop voltage regulator with a fully complementary power process", *IEEE Journal of Solid-State Circuits*, vol.SC-22, no.3, pp.447-450, June 1987.
- [Giebel 1989] Burkhard Giebel, Jürgen Lutz and Paul L. O'Leary, "Digitally controlled oscillator", *IEEE Journal of Solid-State Circuits*, vol.24, no.6, pp.640-645, June 1989.
- [Goodenough 1991] Frank Goodenough, "Airbags boom when IC accelerometer sees 50g", *Electronic Design*, vol.39, no.15, pp.45-56, August 1991.
- [Gregorian 1981] Roubik Gregorian, "High-resolution switched-capacitor D/A converter", *Microelectronics Journal*, vol.12, no.2, pp.10-13, March/April 1981.
- [Gregorian 1983] Roubik Gregorian, Kenneth W. Martin and Gabor C. Temes, "Switched-capacitor circuit design", *Proceedings of the IEEE*, vol.71, no.8, pp.941-966, August 1983.
- [Hajimiri 1998] Ali Hajimiri and Thomas H. Lee, "A general theory of phase noise in electrical oscillators", *IEEE Journal of Solid-State Circuits*, vol.33, no.2, pp.179-194, February 1998.
- [Hajimiri 1999] Ali Hajimiri, Sotirios Limotyrakis and Thomas H. Lee, "Jitter and phase noise in ring oscillators", *IEEE Journal of Solid-State Circuits*, vol.34, no.6, pp.790-804, June 1999.
- [Harrison 2001] Reid R. Harrison, Julian A. Bragg, Paul Hasler, Bradley A. Minch and Stephen P. Deweerth, "A CMOS programmable analog memory-cell array using floating-gate circuits", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol.48, no.1, pp.4-11, January 2001.
- [Haug 1984] K. Haug, G. C. Temes and K. Martin, "Improved offset-compensation schemes for SC circuits", *Proceedings of the 1984 IEEE International Symposium in Circuits and Systems (ISCAS '84)*, Montreal, Quebec, vol.I, pp.1054-1057, May 1984.
- [Hein 1993] Søren Hein and Avidesh Zakhor, "On the stability of sigma-delta modulators", *IEEE Journal of Solid-State Circuits*, vol.41, no.7, pp.2322-2348, July 1993.
- [Henrion 1990] Widge Henrion, Len DiSanza, Matthew Lp, Stephen Terry and Hal Jerman, "Wide dynamic range direct digital accelerometer", *The 4th Solid-State Sensor and Actuator Workshop*, Hilton Head Island, USA, pp.153-157, June 1990.
- [Herzel 1999] Frank Herzel and Behzad Razavi, "A study of oscillator jitter due to supply and substrate noise", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol.46, no.1, pp.56-62, January 1999.

- [Hierold 1996] Christofer Hierold, Andreas Hildebrandt, Ulrich Näher, Thomas Scheiter, Bernd Mensching, Max Steger and Reinhard Tielert, "A pure CMOS surface-micromachined integrated accelerometer", *Sensors and Actuators A: Physical*, vol.A57, pp.111-116, 1996.
- [Horie 1995] Yuuji Horie, Admed A. A. Youssef, Tomoyuki Miyazaki and Taisuke Takeishi, "Ultralow-frequency design of the Wien bridge oscillator using switched capacitors", *IEEE Transactions on Instrumentation and Measurement*, vol. 44, no. 2, pp. 184-187, April 1995.
- [Hsieh 1981] Kuo-Chiang Hsieh, Paul R. Gray, Daniel Senderowicz and David G. Messerschmitt, "A low-noise chopper-stabilized differential switched-capacitor filtering technique", *IEEE Journal of Solid-State Circuits*, vol.SC-16, no.6, pp.708-715, December 1981.
- [Huang 1988] Songming Huang, Robert G. Green, Andrzej Plaskowski and Maurice S. Beck, "A high frequency stray-immune capacitance transducer based on the charge transfer principle", *IEEE Transactions on Instrumentation and Measurement*, vol. 37, no. 3, pp. 368-373, September 1988.
- [Ichikawa 1996] Yuichi Ichikawa, Toshimasa Sadakata, Fukuji Anzai, Yoshiyuki Fukuda, Kiyoshi Nakaya, Shinichi Matsubara, Taturu Saitoh and Takao Araki, "Development of VCR video/audio signal processing LSI chip", *IEEE Transactions on Consumer Electronics*, vol.42, no.3, pp.832-840, August 1996.
- [Jeong 1987] Deog-Kyoon Jeong, Gaetano Borriello, David A. Hodges and Randy H. Katz, "Design of PLL-based clock generation circuits", *IEEE Journal of Solid-State Circuits*, vol.SC-22, no.2, pp.225-261, April 1987.
- [Kajita 2000] Tetsuya Kajita, Un-Ku Moon and Gabor C. Temes, "A noise-shaping accelerometer interface circuit for two-chip implementation", *IEEE International Symposium on Circuits and Systems*, Geneva, Switzerland, vol.IV, pp.337-340, May 2000.
- [Kampen 1994] R.P. van Kampen, M.J. Vellekoop, P.M. Sarro and R.F. Wolffenbuttel, "Application of electrostatic feedback to critical damping of an integrated silicon capacitive accelerometer", *Sensors and Actuators A: Physical*, vol.A43, pp.100-106, 1994.
- [Kampen 1998] R.P. van Kampen and R.F. Wolffenbuttel, "Modeling the mechanical behavior of bulk-micromachined silicon accelerometers", *Sensors and Actuators A: Physical*, vol.A64, pp.137-150, 1998.
- [Kansy 1980] Robert J. Kansy, "Response of a correlated double sampling circuit to $1/f$ noise", *IEEE Journal of Solid-State Circuits*, vol.SC-15, no.3, pp.373-375, June 1980.

- [Kemp 1995] Christopher J. Kemp, "An accelerometer interface circuit", *Proceedings of the IEEE 1995 Custom Integrated Circuits Conference*, Santa Clara, USA, pp.345-348, May 1995.
- [Kim 1998] O. Kim, C.J. Oh and K.S. Kim, "CMOS trimming circuit based on polysilicon fusing", *Electronics Letters*, vol.34, no.4, pp.355-356, February 1998.
- [Klapper 1959] J. Klapper and C.M. Harris, "On the response and approximation of Gaussian filter", *IRE Transactions on Audio*, vol.7, no.3, pp.80-87, May 1959.
- [Kokkonen 1981] Kim Kokkonen, P. Owen Sharp, Roland Albers, J. Patrick Dishaw, Frank Louie and Ron J. Smith, "Redundancy techniques for fast static RAMs", *IEEE International Solid-State Circuits Conference (ISSCC '81)*, pp.80-81, February 1981.
- [Kraft 1998] Michael Kraft, Christopher Lewis, Thomas Hesketh and Stefan Szymkowiak, "A novel micromachined accelerometer capacitive interface", *Sensors and Actuators A: Physical*, vol.A68, pp.466-473, 1998.
- [Kraft 1998a] M. Kraft, C.P. Lewis and T.G. Hesketh, "Closed-loop silicon accelerometers", *IEE Proceedings - Circuits, Devices and Systems*, vol.145, no.5, pp.325-331, October 1998.
- [Krömer 1995] O. Krömer, O. Fromhein, H. Gemmeke, T. Kühner, J. Mohr and M. Strohrmann, "High-precision readout circuit for LIGA acceleration sensors", *Sensors and Actuators A: Physical*, vol.A46-A47, pp.196-200, 1995.
- [Krummenacher 1982] François Krummenacher, "Micropower switched capacitor biquadratic cell", *IEEE Journal of Solid-State Circuits*, vol.SC-17, no.3, pp.507-512, June 1982.
- [Kuehnel 1994] Wolfgang Kuehnel and Steven Sherman, "A surface micromachined silicon accelerometer with on-chip detection circuitry", *Sensors and Actuators A: Physical*, vol.A45, pp.7-16, 1994.
- [Kulah 2000] Haluk Kulah, Navid Yazdi and Khalil Najafi, "A CMOS switched-capacitor interface circuit for an integrated accelerometer", *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, Lansing, USA, pp.244-247, August 2000.
- [Kung 1988] Joseph T. Kung, Hae-Seung Lee and Roger T. Howe, "A digital readout technique for capacitive sensor applications", *IEEE Journal of Solid-State Circuits*, vol.23, no.4, pp.972-977, August 1988.

- [Lahiji 2000] G. Roientan Lahiji and M. Atri Ebrahimpour, "A continuous time auto-zero offset compensated switched capacitor integrator", *Analog Integrated Circuits and Signal Processing*, vol.24, no.3, pp. 269-272, September 2000.
- [Lee 1971] C. Thomson Lee, "The biquad: part I - some practical design considerations", *IEEE Transactions on Circuit Theory*, vol.CT-18, no.3, pp.350-357, May 1971.
- [Lee 1971a] C. Thomson Lee, "The biquad: part II - a multipurpose active filtering system", *IEEE Transactions on Circuit Theory*, vol.CT-18, no.3, pp.358-361, May 1971.
- [Lee 1996] C.I. Lee, A.H. Johnston, W.C. Tang and C.E. Barnes, "Total dose effects on microelectromechanical systems (MEMS): accelerometers", *IEEE Transactions on Nuclear Science*, vol.43, no.6, pp.3127-3132, December 1996.
- [Lee 2000] Thomas H. Lee and Ali Hajimiri, "Oscillator phase noise: a tutorial", *IEEE Journal of Solid-State Circuits*, vol.35, no.3, pp.326-336, March 2000.
- [Leib 1992] Harry Leib and Subbarayan Pasupathy, "Digital transmission performance of standard analog filter", *IEEE Transactions on Communications*, vol.40, no.1, pp.42-50, January 1992.
- [Lemkin 1999] Mark Lemkin and Bernhard E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics", *IEEE Journal of Solid-State Circuits*, vol.34, no.4, pp.456-468, April 1999.
- [Leuthold 1990] H. Leuthold and F. Rudolf, "An ASIC for high-resolution capacitive microaccelerometer", *Sensors and Actuators A: Physical*, vol.A21-A23, pp.278-281, 1990.
- [Li 2001] Xiujun Li and Gerard C. M. Meijer, "A capacitive-sensor interface circuit based on a first-order charge-balanced SC-oscillator", *IEEE Transactions on Instrumentation and Measurement Technology Conference*, Budapest, Hungary, pp. 282-285, May 2001.
- [Lötters 1997] J.C. Lötters, W. Olthuis, P.H. Veltink and P. Bergveld, "Design, realization and characterization of a symmetrical triaxial capacitive accelerometer for medical applications", *Sensors and Actuators A: Physical*, vol.A61, pp.303-308, 1997.
- [Lötters 1999] Joost C. Lötters, Wouter Olthuis, Peter H. Veltink and Piet Bergveld, "A sensitive differential capacitance to voltage converter for sensor applications", *IEEE Transactions on Instrumentation and Measurement*, vol.48, no.1, pp.89-96, February 1999.

- [Lu 1995] Crist Lu, Mark Lemkin and Bernhard E. Boser, "A monolithic surface micromachined accelerometer with digital output", *IEEE Journal of Solid-State Circuits*, vol.30, no.12, pp.1367-1373, December 1995.
- [Luo 2002] Hao Luo, Gang Zhang, L. Richard Carley and Gary K. Fedder, "A post-CMOS micromachined lateral accelerometer", *Journal of Microelectromechanical Systems*, vol.11, no.3, pp.188-195, June 2002.
- [Malvicino 1996] C. Malvicino, "Sensors in automotive applications", *Proceedings of the 1st Italian Conference on Sensors and Microsystems*, Rome, Italy, pp.223-227, February 1996.
- [Manabe 1999] Yukiko Manabe, Kousuke Okuyama, Katsuhiko Kubota, Atsushi Nozoe, Tetsuji Karashima, Kazuaki Ujiie, Hiroyuki Kanno, Moriyoshi Nakashima and Natsuo Ajika, "Detailed observation of small leak current in flash memories with thin tunnel oxides", *IEEE Transactions on Semiconductor manufacturing*, vol.12, no.2, pp.170-174, May 1999.
- [Martin 1987] Ken Martin, Levent Ozcolak, Y. S. Lee and Gabor C. Temes, "A differential switched-capacitor amplifier", *IEEE Journal of Solid-State Circuits*, vol.SC-22, no.1, pp.104-106, February 1987.
- [Matsumoto 1993] Y. Matsumoto and M. Esashi, "Integrated silicon capacitive accelerometer with PLL servo technique", *Sensors and Actuators A: Physical*, vol.A39, pp.209-217, 1993.
- [Matsumoto 1996] Yoshinori Matsumoto, Moritaka Iwakiri, Hidekazu Tanaka, Makoto Ishida and The late Tetsuro Nakamura, "A capacitive accelerometer using SDB-SOI structure", *Sensors and Actuators A: Physical*, vol.A53, pp.267-272, 1996.
- [McNeill 1997] John A. McNeill, "Jitter in ring oscillators", *IEEE Journal of Solid-State Circuits*, vol.32, no.6, pp.870-879, June 1997.
- [Menniti 1984] Pietro Menniti and Sandro Storti, "Low drop regulator with overvoltage protection and reset function for automotive environment", *IEEE Journal of Solid-State Circuits*, vol.SC-19, no.3, pp.442-448, June 1984.
- [Metzger 1983] Larry R. Metzger, "A 16K CMOS PROM with polysilicon fusible links", *IEEE Journal of Solid-State Circuits*, vol.18, no.5, pp.562-567, October 1983.
- [Mok 1995] Do-Sang Mok, Soon-Yang Hong, Myoung-Chun Hwang and Kyu-Soo Chung, "An adjustment-free LSI for the video signal processing system", *IEEE Transactions on Consumer Electronics*, vol.41, no.3, pp.414-420, August 1995.

- [Moschytz 1967] George S. Moschytz, "Sallen and Key filter networks with amplifier gain larger than or equal to unity", *IEEE Journal of Solid-State Circuits (Correspondence)*, vol.SC-2, pp.114-116, September 1967.
- [Moschytz 1972] George S. Moschytz, "A general all-pass network based on the Sallen-Key circuit", *IEEE Transactions on Circuit Theory*, vol.CT-19, no.4, pp.392-394, July 1972.
- [Moschytz 1973] George S. Moschytz, "A universal low-q active-filter building block suitable for hybrid-integrated circuit implementation", *IEEE Transactions on Circuit Theory*, vol.CT-20, no.1, pp.37-47, January 1973.
- [Motorola 1997] Motorola Inc., Schaumburg, USA, "MMAS40G10D - Micromachined accelerometer", data sheet, 1997.
- [Motorola 2000] Motorola Inc., Schaumburg, USA, "MMA2201D - Surface mount micromachined accelerometer", data sheet, 2000.
- [Motorola 2001] Motorola Inc., Schaumburg, USA, "MMA2202D - Surface mount micromachined accelerometer", data sheet, 2001.
- [Motorola 2001a] Motorola Inc., Schaumburg, USA, "MMA1220D - Low G micromachined accelerometer", data sheet, 2001.
- [Mu 1999] Fenghao Mu, Anders Edman and Christer Svensson, "Digital multiphase clock/pattern generator", *IEEE Journal of Solid-State Circuits*, vol.34, no.2, pp.182-191, February 1999.
- [Nilsson 1996] Peter Nilsson and Mats Torkelson, "A monolithic digital clock-generator for on-chip clocking of custom DSP's", *IEEE Journal of Solid-State Circuits*, vol.31, no.5, pp.700-706, May 1996.
- [Norsworthy 1989] Steven R. Norsworthy, Irving G. Post and H. Scott Fetterman, "A 14-bit 80-kHz sigma-delta A/D converter: modeling, design, and performance evaluation", *IEEE Journal of Solid-State Circuits*, vol.24, no.2, pp.256-266, April 1989.
- [Ogawa 1993] Satomi Ogawa and Kenzo Watanabe, "A switched-capacitor successive-approximation A/D converter", *IEEE Transactions on Instrumentation and Measurement*, vol. 42, no. 4, pp. 847-853, August 1993.
- [Ogawa 2001] Satomi Ogawa, Yutaka Oisugi, Kouji Mochizuki and Kenzo Watanabe, "A switched-capacitor interface for differential capacitance transducers", *IEEE Transactions on Instrumentation and Measurement*, vol. 50, no. 5, pp. 1296-1301, October 2001.
- [Paemel 1989] Mark van Paemel, "Interface circuit for capacitive accelerometer", *Sensors and Actuators A: Physical*, vol.A17, pp.629-637, 1989.

- [Pease 1984] Robert A. Pease, "A new Fahrenheit temperature sensor", *IEEE Journal of Solid-State Circuits*, vol.SC-19, no.6, pp.971-977, December 1984.
- [Peeters 1992] Eric Peeters, Stef Vergote, Bob Puers and Willy Sansen, "A highly symmetrical capacitive micro-accelerometer with single degree-of-freedom response", *Journal of Micromechanics and Microengineering*, vol.2, pp.104-112, 1992.
- [Peteghem 1988] Peter M. Van Peterghem, "On the relationship between PSRR and clock feedthrough in SC filters", *IEEE Journal of Solid-State Circuits*, vol.23, no.4, pp.997-1004, August 1988.
- [Petersen 1982] Kurt E. Petersen, "Silicon as a mechanical material", *Proceedings of the Institute of Electrical and Electronics Engineers (IEEE)*, vol.70, no.5, May 1982.
- [Petersen 1982a] Kurt E. Petersen, Anne Shartel and Norman F. Raley, "Micromechanical accelerometer integrated with MOS detection circuitry", *IEEE Transactions on Electron Devices*, vol.ED-29, no.1, pp.23-27, January 1982.
- [Petkov 2005] Vladimir P. Petkov and Bernhard E. Boser, "A fourth-order $\Sigma\Delta$ interface for micromachined inertial sensors", *IEEE Journal of Solid-State Circuits*, vol.40, no.8, pp.1602-1609, August 2005.
- [Popov 1998] Anguel N. Popov and Valentin S. Mollov, "CMOS Schmitt trigger with zero hysteresis", *IEEE Melecon '98 - 9th Mediterranean Electrotechnical Conference*, Tel-Aviv, Isreal, vol.2, no.1, pp.464-468, May 1998.
- [Price 1965] John E. Price, "Programmable circuit", *U.S. Patent 3191151*, June 22, 1965
- [Price 1976] John J. Price, "A passive laser-trimming technique to improve the linearity of a 10-bit D/A converter", *IEEE Journal of Solid-State Circuits*, vol.SC-11, no.6, pp.789-794, December 1976.
- [Puers 1993] Robert Puers, "Capacitive sensors: when and how to use them", *Sensors and Actuators A: Physical*, vol.A37-A38, pp.93-105, 1993.
- [Puers 1998] R. Puers and S. Reyntjens, "Design and processing experiments of a new miniaturized capacitive triaxial accelerometer", *Sensors and Actuators A: Physical*, vol.A68, pp.324-328, 1998.
- [Razavi 1996] Behzad Razavi, "A study of phase noise in CMOS oscillators", *IEEE Journal of Solid-State Circuits*, vol.31, no.3, pp.331-343, March 1996.

- [Ristic 1992] Lj. Ristic, R. Gutteridge, B. Dunn, D. Mietus and P. Bennett, "Surface micromachined polysilicon accelerometer", *The 5th Solid-State Sensor and Actuator Workshop*, Hilton Head Island, USA, pp.118-121, June 1992.
- [Rudolf 1983] F. Rudolf, "A micromechanical capacitive accelerometer with a two-point inertial-mass suspension", *Sensors and Actuators A: Physical*, vol.4, pp.191-198, 1983.
- [Rudolf 1987] Félix. Rudolf, Alain Jornod and Philip Bencze, "Silicon microaccelerometer", *The 4th International Conference on Solid-State Sensors and Actuators (Transducers '87)*, Tokyo, Japan, pp.376-379, June 1987.
- [Rudolf 1990] F. Rudolf, A. Jornod, J. Bergqvist and H. Leuthold, "Precision accelerometers with μg resolution", *Sensors and Actuators A: Physical*, vol.A21-A23, pp.297-302, 1990.
- [Säckinger 1988] Eduard Säckinger and Walter Guggenbühl, "An analog trimming circuit based on a floating-gate device", *IEEE Journal of Solid-State Circuits*, vol.23, no.6, pp.1437-1440, December 1988.
- [Schemmel 2002] Johannes Schemmel, Karlheinz Meier and Markus Loose, "A scalable switched capacitor realization of the resistive fuse network", *Analog Integrated Circuits and Signal Processing*, vol.32, no.2, pp. 135-148, August 2002.
- [Schnatz 1992] F.V. Schnatz, U. Schöneberg, W. Brockherde, P. Kopystynski, T. Mehlhorn, E. Obermeier and H. Benzel, "Smart CMOS capacitive pressure transducer with on-chip calibration capability", *Sensors and Actuators A: Physical*, vol.A34, pp.77-83, 1992.
- [Schroeder 1977] James E. Schroeder and Richard L. Goslin, "A 1024-bit, fused-link CMOS PROM", *IEEE International Solid-State Circuits Conference (ISSCC '77)*, pp.190-191, February 1977.
- [Secareanu 1999] Radu M. Secareanu, Ivan S. Kourtev and Juan Becerra, "The behavior of digital circuits under substrate noise in a mixed-signal smart-power environment", *Proceedings of the 11 IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD '99)*, Toronto, Canada, pp.253-256, May 1999.
- [Seidel 1990] H. Seidel, H. Riedel, R. Kolbeck, G. Mück, W. Kupke and M. Königer, "Capacitive silicon accelerometer with highly symmetrical design", *Sensors and Actuators A: Physical*, vol.A21-A23, pp.312-315, 1990.
- [Selvakumar 1998] Arjun Selvakumar and Khalil Najafi, "A high-sensitivity z-axis capacitive silicon microaccelerometer with a torsional suspension", *Journal of Microelectromechanical Systems*, vol.7, no.2, pp.192-200, June 1998.

- [Shieh 1987] Je-Hurn. Shieh, Mahesh Patil, and Bing J. Sheu, "Measurement and Analysis of Charge Injection in MOS Analog Switches", *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 2, pp. 277-281, April 1987.
- [Shinagawa 1990] Mitsuru Shinagawa, Yukio Akazawa and Tsutomu Wakimoto, "Jitter analysis of high-speed sampling systems", *IEEE Journal of Solid-State Circuits*, vol.25, no.1, pp.220-224, February 1990.
- [Singh 2001] R. Singh, S. Sali and W. L. Woo, "Efficient methods for modeling substrate coupling in mixed-signal integrated circuits", *Journal of Electronics & Communication Engineering*, vol.13, no.6, pp.237-248, December 2001.
- [Smith 1994] Ted Smith, Olivier Nys, Michel Chevroulet, Yves DeCoulon and Marc Degrauwe, "A 15b electromechanical sigma-delta converter for acceleration measurements", *IEEE International Solid-State Circuits Conference (ISSCC '94)*, San Francisco, USA, pp.160-161, February 1994.
- [Spangler 1996] Leland 'Chip' Spangler and Christopher J. Kemp, "ISAAC: integrated silicon automotive accelerometer", *Sensors and Actuators A: Physical*, vol.A54, pp.523-529, 1996.
- [Su 1993] David K. Su, Marc J. Loinaz, Shoichi Masui and Bruce A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits", *IEEE Journal of Solid-State Circuits*, vol.28, no.4, pp.420-430, April 1993.
- [Suzuki 1990] S. Suzuki and S. Tuchtani, "Semiconductor capacitance-type accelerometer with PWM electrostatic servo technique", *Sensors and Actuators A: Physical*, vol.A21-A23, pp.316-319, 1990.
- [Takao 1999] Hidekuni Takao, Yoshinori Matsumoto and Makoto Ishida, "A monolithically integrated three-axis accelerometer using CMOS compatible stress-sensitive differential amplifiers", *IEEE Transactions on Electron Devices*, vol.46, no.1, pp.109-116, January 1999.
- [Tanimoto 1982] Masafumi Tanimoto, Junichi Murota, Masato Wada, Takashi Watanabe, Kenji Miura and Nobuaki Ieda, "A novel 14 V programmable 4 kbit MOS PROM using a poly-Si resistor applicable to on-chip programmable devices", *IEEE Journal of Solid-State Circuits*, vol.SC-17, no.1, pp.62-68, February 1982.
- [Tarui 1972] Y. Tarui, Y. Hayashi and K. Nagai, "Electrically reprogrammable nonvolatile semiconductor memory", *IEEE Journal of Solid-State Circuits*, vol.SC-7, no.5, pp.369-375, October 1972.

- [Tschan 1995] Thomas Tschan, Wolfram Urbanek, Mel Lim, Henry Allen and James Knutti, "A high-performance, low cost capacitive accelerometer trimmed using nonvolatile potentiometers (EEPT's)", *The 8th International Conference on Solid-State Sensors and Actuators (Transducers '95)*, Stockholm, Sweden, pp.601-603, June 1995.
- [Venkatraman 1996] Prasad Venkatraman and B. Jayant Baliga, "Large area MOS-gated power devices using high-current fusible links", *IEEE Transactions on Electron Devices*, vol.ED-43, no.1, pp.172-174, January 1996.
- [Venkatraman 1996a] Prasad Venkatraman and B. Jayant Baliga, "Large area MOS-gated power devices using fusible link technology", *IEEE Transactions on Electron Devices*, vol.ED-43, no.2, pp.347-351, February 1996.
- [Weigandt 1994] Todd C. Weigandt, Beomsup Kim and Paul R. Gray, "Analysis of timing jitter in CMOS ring oscillators", *1994 IEEE International Symposium on Circuits and Systems (ISCAS '94)*, London, UK, vol.4, pp.27-30, May 1994.
- [Weigold 2001] Jason W. Weigold, Khalil Najafi and Stella W. Pang, "Design and fabrication of submicrometer, single crystal Si accelerometer", *Journal of Microelectromechanical Systems*, vol.10, no.4, pp.518-524, December 2001.
- [Welti 1994] A.L. Welti and B.Z. Bobrovsky, "Mean time to lose lock for Langevin-type delay-locked loop", *IEEE Journal of Solid-State Circuits*, vol.42, no.8, pp.2526-2530, August 1994.
- [Wenk 1995] B. Wenk, J. Ramos-Martos, M. Fehrenbach, P. Lange, M. Offenberger and W. Riethmüller, "Thick polysilicon based surface micromachined capacitive accelerometer with force feedback operation", *Proceedings of the International Society of Optical Engineering (SPIE) Micromachined Devices and Components*, Austin, USA, vol.2642, pp.84-94, 1995.
- [Wey 1986] H.M. Wey and W. Guggenbühl, "Noise transfer characteristics of a correlated double sampling circuit", *IEEE Transactions on Circuits and Systems*, vol.CAS-33, no.10, pp.1028-1030, October 1986.
- [White 1974] Marvin H. White, Donald R. Lampe, Franklyn C. Blaha and Ingham A. Mack, "Characterization of surface channel CCD image arrays at low light levels", *IEEE Journal of Solid-State Circuits*, vol.SC-9, no.1, pp.1-13, February 1974.
- [Williams 1985] Jim Williams, "Application Consideration and Circuits for a New Chopper-Stabilized Op Amp, Linear Technology online publications", Linear Technology Application Notes, March, 1985, http://www.linear-tech.com/pub/document.html?pub_type=app&document=16

- [Wilner 1988] L. Bruce Wilner, "A high performance, variable capacitive accelerometer", *IEEE Transactions on Instrumentation and Measurement*, vol.37, no.4, pp.569-571, December 1988.
- [Wu 2004] Jiangfeng Wu, Gary K. Feeder and L. Richard Carley, "A low-noise low-offset capacitive sensing amplifier for a 50- $\mu\text{g}/\sqrt{\text{Hz}}$ monolithic CMOS MEMS accelerometer", *IEEE Journal of Solid-State Circuits*, vol.39, no.5, pp.722-730, May 2004.
- [Wuestling 1997] S. Wuestling, O. Fromhein, H. Gemmeke, M. Tschuch and O. Wollersheim, "Planar-assembly triaxial microaccelerometer with electromechanical sigma-delta ADCs", *Sensors and Actuators A: Physical*, vol.A61, pp.436-440, 1997.
- [Yamada 1992] Mitsuhiro Yamada, Takashi Takebayashi, Shun-Ichi Notoyama and Kenzo Watanabe, "A switched-capacitor interface for capacitive pressure sensors", *IEEE Transactions on Instrumentation and Measurement*, vol.41, no.1, pp.81-86, February 1992.
- [Yazdi 1998] David Yazdi, Farrokh Ayazi and Khalil Najafi, "Micromachined inertial sensors", *Proceedings of the IEEE*, vol.86, no.8, pp.1640-1659, August 1998.
- [Yazdi 1999] David Yazdi and Khalil Najafi, "An interface IC for capacitive silicon μg accelerometer", *IEEE International Solid-State Circuits Conference (ISSCC '99)*, San Francisco, USA, pp.132-133, February 1999.
- [Yazdi 2000] David Yazdi and Khalil Najafi, "An all-silicon single-wafer micro-g accelerometer with a combined surface and bulk micromachining process", *Journal of Microelectromechanical Systems*, vol.9, no.4, pp.544-550, December 2000.
- [Young 1992] Ian A. Young, Jeffrey K. Greason and Keng L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessor", *IEEE Journal of Solid-State Circuits*, vol.27, no.11, pp.1599-1607, November 1992.
- [Yun 1992] Weijie Yun, Roger T. Howe and Paul R. Gray, "Surface micromachined, digitally force-balanced accelerometer with integrated CMOS detection circuitry", *The 5th Solid-State Sensor and Actuator Workshop*, Hilton Head Island, USA, pp.126-131, June 1992.
- [Zimmermann 1995] L. Zimmermann, J.Ph. Ebershol, F.Le Hung, J.P. Berry, F. Baillieu, P. Rey, B. Diem, S. Renard and P. Caillat, "Airbag application: a microsystem including a silicon capacitive accelerometer, CMOS switched capacitor electronics and true self-test capability", *Sensors and Actuators A: Physical*, vol.A46-A47, pp.190-195, 1995.

Books

- [Baxter-1997] Larry K. Baxter, *"Capacitive Sensors: Design and Applications"*, IEEE Press, 1997.
- [Chandrakasan-1996] Anantha P. Chandrakasan, *"Low Power Digital CMOS Design"*, Ph.D. Thesis, University of California, Berkeley, UMI, Michigan, USA, 1996.
- [Franco-1998] Sergio Franco, *"Design with Operational Amplifiers and Analog Integrated Circuits"*, Second Edition, McGraw-Hill Inc., 1998.
- [Göpel-1995] W. Göpel, J. Hesse and Jay N. Zemel, *"Sensors: A Comprehensive Survey"*, Volume 1 to 8, VCH, 1989 to 1995.
- [Gray-2001] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, *"Analysis and Design of Analog Integrated Circuits"*, Fourth Edition, John Wiley & Sons Inc., 2001.
- [Gregorian-1999] Roubik Gregorian, *"Introduction to CMOS Op-amps and Comparators"*, John Wiley & Sons Inc., 1999.
- [Kang-1999] Sung-Mo Kang and Yusuk Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, Second Edition, McGraw-Hill, Singapore, 1999.
- [Madou-2002] Marc J. Madou, *"Fundamentals of Microfabrication The Science of Miniaturization"*, Second Edition, CRC Press, 2002.
- [Martin-1997] Ken Martin and David Johns, *"Analog Integrated Circuit Design"*, John Wiley & Sons Inc., 1997.
- [Menz-2001] Wolfgang Menz, Jürgen Mohr and Oliver Paul, *"Microsystem Technology"*, WILEY-VCH, 2001.
- [Middelhoek-1989] S. Middelhoek S. and S.A. Audet, *"Silicon Sensors"*, Academic Press, London, 1989.
- [Moschytz-1984] George S. Moschytz, *"MOS Switched-Capacitor Filter: Analysis and Design"*, IEEE Press, New York, 1984.
- [Razavi-2001] Behzad Razavi, *"Design of Analog CMOS Integrated Circuits"*, McGraw-Hill Inc., 2001.
- [Schaumann-1981] Rolf Schaumann, Michael A. Soderstrand and Kenneth R. Laker, *"Modern Active Filter Design"*, IEEE Press, New York, 1981.

- [Sze-1994] S.M. Sze, "*Semiconductor Sensors*", A Wiley-Interscience Publication, John Wiley & Sons Inc., 1994.
- [Tsividis-1999] Y. Tsividis, "*Operation and Modeling of the MOS transistor*", Second Edition, McGraw-Hill Inc., 1999.
- [Unbehauen-1989] Rolf Unbehauen and Andrzej Cichoki, "*MOS Switched-Capacitor and Continuous-Time Integrated Circuits and Systems*", Springer-Verlag, Germany, 1989.
- [Valkenburg-1982] M.E. Van Valkenburg, "*Analog Filter Design*", CBS College Publishing, USA, 1982.
- [Veijola-1999] Timo Veijola, "*Equivalent Circuit Models for Micromechined Inertial Sensors*", Ph.D. Thesis, Helsinki University of Technology, Espoo, Finland, 1999.

APPENDICES

A. Derivation of Model Equations

In the section, the derivation of Equation 3.3.1.1 and Equation 3.3.1.2 are presented. Note that the mismatch factor and temperature effect are merely added components and are not included in the final equation. The derivation assumes the following:

- ✱ The acceleration sensor is not under any stress, therefore, the mass m , the damping coefficient b , and spring constant k_s , remain constant.
- ✱ The maximum deflection of the movable plate is less than 10 % of the nominal distance between each movable plate and fixed plate pair. Hence, non-linearity effect of capacitance to small change of distance can be neglected.

Refer to Figure 3.2.1.1 and Figure 3.2.1.2, which show the plan view and cross-sectional view of the basic acceleration sensor structure respectively and the symbol of complete sensing capacitance C_{s1} and C_{s2} in Figure 3.2.1.3, the capacitance of the two pairs of parallel conductive plates are given by

$$C_{s1} = \frac{\epsilon S}{x_o + x} \quad , \quad C_{s2} = \frac{\epsilon S}{x_o - x} \quad (\text{A.1})$$

where S = cross-sectional area of the conductive plate,

x_o = nominal capacitance gap under static condition.

The deflection x of the moveable conductive plate (towards top fixed plate as positive direction) can be changed by two types of forces. The first type is the external mechanical force due to acceleration asserting on the movable plate and the other is the electrostatic

force applying to the fixed and moveable plates. Let the displacement moved by the external mechanical force be x_a while the one affected by the electrostatic force be x_e .

Displacement by x_a

Following Newton 2nd Law of motion, the differential equation for the displacement, x , as a function of external force, F_{ext} , is given by

$$F_{ext} = ma = m \frac{d^2 x_a}{dt^2} + b \frac{dx_a}{dt} + k_s x_a \quad (A.2)$$

It can be shown that the resonant frequency and the quality factor are given by $\omega_r = \sqrt{k_s / m}$ and $Q = \omega_r m / b$ respectively. Since the working range of the sensor is small, we can assume a linear relationship in Equation A.2 as

$$x_a = \frac{ma}{k_s} \quad (A.3)$$

Displacement by x_e

The electrostatic force, F_{ele} , between the two parallel conductive plates under constant voltage condition can be obtained from gradient of the change of electrostatic potential energy, W_e , with respect to the displacement in the same direction [Kampen 1994], [Wenk 1995], as follows:

$$F_{ele} = -\frac{\partial W_e}{\partial x} = -\frac{\partial}{\partial x} \left(\frac{1}{2} C(x) V_x^2 \right) = \frac{\varepsilon S V_x^2}{2X^2}$$

Note that $X = x_o + x_e$ (for C_{S1}), $X = x_o - x_e$ (for C_{S2}), V_x ($x=1,2$) is the voltage difference applied between the parallel plates. Since the electrostatic force $F_{ele} = k_s x$, is applied in force-balanced condition (moveable plate almost at center), we can assume that $x_o \gg x_e$, and hence the above equation can be simplified to

$$x_1 = \frac{\varepsilon S V_1^2}{2k_s x_o^2}, \quad x_2 = \frac{\varepsilon S V_2^2}{2k_s x_o^2}$$

Note that V_1 is the voltage applied between the top fixed plate and the moveable plate resulted in the displacement x_1 while V_2 is the voltage applied between the bottom fixed and the moveable plates resulted in the displacement x_2 . The resulting displacement of $x_e = x_1 - x_2$ is given by

$$x_e = \frac{\varepsilon S}{2k_s x_o^2} (V_1^2 - V_2^2) \quad (\text{A.4})$$

Final Model Equations

From Equation A.3 and Equation A.4, the final model equations for the capacitances of the two pairs of parallel plates (sensing capacitors C_{S1} , C_{S2}) are

$$C_{S1} = \frac{\varepsilon S}{x_o + (x_a + x_e)} \quad , \quad C_{S2} = \frac{\varepsilon S}{x_o - (x_a + x_e)} \quad (\text{A.5})$$

It is interesting to note the convenience of applying Equation A.4 in force-balanced structure that the balanced condition to a given acceleration a can be designed using the equation $V_2^2 - V_1^2 = K_{fb} a$ where $K_{fb} = \frac{2m x_o^2}{\varepsilon S}$.

Calculations of effective capacitive area S and spring constant k_s

This subsection covers the calculation of the effective capacitive area S and the spring constant k_s of a surface micromachined acceleration sensor shown in Figure 3.2.1.1 as well as the definitions of all the related terms. Note that the bracketed value at the end of each term serves as an example. Cross-sectional area of the conductive plate is defined as

$$S = L_f h_f N_f \quad (\text{A.6})$$

where N_f - total number of pairs of fingers on both sides (58 pairs)

h_f - thickness (2 μm)

L_f - length of fingers (250 μm)

The effective spring constant is defined as [Wenk 1995]:

(Note: another factor k_3 , stiffness due to beam elongation, can be ignored.)

$$k_s = k_1 + k_2 \quad (\text{A.7})$$

where k_1 = stiffness due to beam bending, k_2 = stiffness due to residual stress

$$k_1 = \frac{4 E h_f W_t^3}{L_t^3}, \quad k_2 = \frac{4 h_f W_t \sigma_R}{L_t} \quad (\text{A.8})$$

E = Young Modulus of elasticity (190 MPa)

h_f = thickness (2 μm)

W_t = width of tether (2.5 μm)

L_t = length of tether (250 μm)

σ_R = tensile stress (20 MPa)

An example of calculating the typical parasitic capacitance value

As an illustration, the typical parasitic capacitance C_{pt} , C_{pm} and C_{pb} (Figure 3.3.1.2) are calculated as follows.

$$C_{pt} = C_{pb} = \frac{\epsilon_o \epsilon_{SiO_2} S_{t,b}}{x_o} = \frac{\epsilon_o (3.9)(5u \times 434u \times 58)}{2u} = 2.17 \text{ pF}$$

$$C_{pm} = \frac{\epsilon_o \epsilon_{SiO_2} S_m}{x_o} = \frac{\epsilon_o (3.9)(9u \times 260u \times 58)}{2u} = 2.34 \text{ pF}$$

An example of a SPICE model description on the proposed acceleration sensor model

```
.SUBCKT accel Na Not Nom Nob
+ pf=6p pm=12p pr=200 A=29n d=2u mass=520p
+ k=1.697 mmf=0 ilk=2E-9 Tdiff=0 TC=0 pb=3p
Rnv Na 0 10T
Cs1 Ntp Nmp C='(1+mmf)*(1+Tdiff*TC)*8.8542e-12*A
/(d-(4.427e-12*A*(v(Ntp,Nmp)*v(Ntp,Nmp)-
v(Nbp,Nmp)*v(Nbp,Nmp)))/(k*d*d)+mass*v(Na)*9.81
/k))' CTYPE=0
Cs2 Nbp Nmp C='(1+mmf)*(1+Tdiff*TC)*8.8542e-12*A
/(d+(4.427e-12*A*(v(Ntp,Nmp)*v(Ntp,Nmp)-
v(Nbp,Nmp)*v(Nbp,Nmp)))/(k*d*d)+mass*v(Na)*9.81
/k))' CTYPE=0
Cpt Ntp 0 pf
Cpm Nmp 0 pm
Cpb Nbp 0 pf
Cbt Not 0 pb
Cbm Nom 0 pb
Cbb Nob 0 pb
Git Ntp 0 VCCS Not 0 ilk
Gim Nmp 0 VCCS Nom 0 ilk
Gib Nbp 0 VCCS Nob 0 ilk
Rtp Ntp Not pr
Rmp Nmp Nom pr
Rbp Nbp Nob pr
.ENDS accel
```


B. Correlation of Electrical and Mechanical Model

This section documents the correlation of series-LCR circuit response with the mechanical motion response. This is to demonstrate that series-LCR circuit can be used to represent the second-order response of mechanical movement. In deriving the equation of the LCR circuit output, the following assumptions were made:

- ✧ The resistor, the inductor and the capacitor used in the series-LCR circuit are ideal. Therefore, the losses of the inductor and the capacitor are neglected.
- ✧ The temperature effects on all the components are excluded as the components are used for the purpose of obtaining the second-order response only.

LCR Model Equation

Figure B.1: Series-LCR Model

Take Figure B.1 as reference, the transfer function of the LCR model in s-domain can be described as

$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \quad (\text{B.1})$$

$$\frac{V_o(s)}{V_i(s)} = \frac{\omega_{ne}^2}{s^2 + 2\zeta_e \omega_{ne}s + \omega_{ne}^2} \quad (\text{B.2})$$

Comparing Equation B.1 and Equation B.2, the natural frequency is given by $\omega_{ne} = \frac{1}{\sqrt{LC}}$

and damping factor is given by $\zeta_e = \frac{1}{2} R \sqrt{\frac{C}{L}}$.

It can be shown that by taking the inverse Laplace transform, the time domain solution can be obtained as

$$V_o(t) = \frac{\omega_{ne}}{\sqrt{1-\zeta_e^2}} e^{-\zeta_e \omega_{ne} t} \sin \omega_{ne} \sqrt{1-\zeta_e^2} t \quad (\text{B.3})$$

Here, we have the usual second-order behavior with the oscillation described by $\sin \omega_{ne} \sqrt{1-\zeta_e^2} t$, the decay is expressed by $e^{-\zeta_e \omega_{ne} t}$ with time constant of $-\frac{R}{2L}$ and the

gain is given by $\frac{\omega_{ne}}{\sqrt{1-\zeta_e^2}}$.

The selection of inductance, capacitance and resistance values can be very flexible. They can be calculated by just using only the given sensor resonant frequency and damping factor or can perform a direct conversion from the mechanical parameters. For instance, for a given sensor resonant frequency and the damping factor, the selection of inductance, capacitance and resistance values can be designed as followed.

Set $L = 1 \text{ mH}$, then $C = \frac{1}{\omega_{ne}^2 L}$ and $R = 2\zeta_e \omega_{ne} L$.

For example, for $f_o = 10 \text{ kHz}$, $\zeta_e = 0.7071$, then

$C = 253.3 \text{ nF}$ and $R = 88.8568 \text{ } \Omega$ for $L = 1 \text{ mH}$.

Correlation of series LCR model to second-order mechanical model

From the sensitivity function in Equation 3.2.2.3 (repeated here for convenience),

$$H(s) = \frac{X(s)}{A(s)} = \frac{m}{k_s} \frac{\frac{k_s}{m}}{s^2 + \frac{b}{m}s + \frac{k_s}{m}} = K \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

the displacement $X(s)$ can be described as the product of sensitivity constant $K = \frac{m}{k_s}$ and

second-order acceleration response $A(s) \left(\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right)$; refer to Equation B.4 below.

Note also that Equation B.4 looks similar to $x_a = \frac{m}{k} a$ that is used in the sensor model

equation but with the inclusion of the second-order response $\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$.

$$X(s) = \frac{m}{k_s} A(s) \left(\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right) \quad (\text{B.4})$$

Therefore, replacing the term $\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$ with Equation B.2 and then multiplying

the result with the sensitivity constant K , the second-order mechanical movement response can be represented by the series LCR electrical model.

C. Design Procedures

This section describes the design procedures of the ASIC that were taken to achieve the final research prototype. Figure C.1 outlines the design procedures in the form of flow chart.

The designing procedures began with the system design to define the design specifications and requirements of all the circuit building blocks. After that, the circuits were designed and drawn using Cadence Electronic Design Automation (EDA) schematic drawing tools to obtain the schematic diagrams, which were then be converted into HSpice simulation description files. Using these description files plus the foundry technology files, the HSpice circuit simulator was able to verify the performance of circuits. The results of the simulation were then used to determine whether a re-design of the circuits was necessary. When the iterative designs and the simulation results had met all the specifications, the next phase was to perform the system layout of the chip. The floor plan of the chip is shown in Figure C.2.

Since the system made use of mainly analog circuits, a full custom layout approach was carried out using Cadence EDA layout tools. The complete system layout was done manually. Although the automated place-and-route tools can shorten the layout time, it is more suitable for large-scaled digital system than for mixed-signal system. This is because the mixed-signal system layout requires careful isolation between the analog and digital circuits in order to minimize the coupling noise between the different types of circuits, and also needs to provide the matching of critical cells. Therefore, the handcrafted full-custom layout approach is still a better solution. In addition, it offers better optimization of the chip area and better control on the placement of the critical components. More attention can also

be placed on reducing substrate noise, coupling noise, and so forth. The verification of the layout was performed using design rule check (DRC) and layout versus schematic (LVS) check. The DRC was to check whether the layout had violated any design rule, which would be prohibited during the fabrication process. The LVS check ensured the correctness of the layout according to the connection in the schematic. After going through these steps, the layout was ready for fabrication.

Nevertheless, a final check of the parasitics effects on the circuits was still necessary. It was carried out using the parasitic extraction program to extract the parasitic capacitances and resistances of the layout. The circuits with the parasitic capacitances and resistance were simulated. If the post-layout simulation results failed to meet the specifications, a re-design or re-layout task would be needed in the iterative process. This ASIC was sent to Austria Mikro Systeme International AG (AMS) for fabrication. When this was completed, the final test phase would be engaged to get all the required experimental results.

Figure C.1: Flow chart of the design procedures

Figure C.2: Layout floor plan of the ASIC