CMOS quadrature voltage-controlled oscillators and generators for wideband and multi-band transceivers

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CMOS Quadrature Voltage-Controlled Oscillators and Generators for Wideband and Multi-band Transceivers

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A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
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STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

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ABSTRACT

This thesis aims to provide a comprehensive study on the topic of CMOS quadrature voltage controlled oscillators and generators for wideband and multi-band transceivers, which pertains to the investigation, analysis, and design of different quadrature oscillators and generators.

The quadrature oscillators and generators play important roles in the modern direct-conversion and low-IF transceivers. Various methods for generating quadrature signals have been explored. One way to produce quadrature signals is to use the RC polyphase network. The transfer functions of the 1st-, 2nd- and 3rd-order RC polyphase networks used for quadrature signal generation have been re-derived based on very basic principles. The new approach removed the need for the complex phasor and matrix analysis; and it was simple and comprehensive. The output signals' matching behavior has also been explored. A quadrature generator consisting of a Voltage Controlled Oscillator (VCO), a 2nd-order RC polyphase network and output buffers has been designed and fabricated. In the presence of 15% component variation, it still achieved less than 0.5dB mismatch in amplitude and much less than 0.5° phase error. The quadrature generator had a frequency tuning range from 2.18GHz to 2.48GHz and it consumed 3.9mA current.

Quadrature signals can be produced by cross-coupling two VCOs as well. The operation principle of the Series Quadrature VCO (Series QVCO) has been presented based on circuit analysis. It has been shown that by putting the coupling transistors in series with switching transistors, the quadrature signals could be generated intrinsically.

A low power Series QVCO has been designed and fabricated. The Series QVCO removed the tail current of the coupling transistors, and by using the current-use technique, a low power design has been achieved. The measurement results showed that the Series QVCO produced 240mV output amplitude with only 1.5mA current consumed, which is very low-power consuming compared to other state-of-the-art designs.

Due to the increasing demand for low power dual-band transceivers, the design of low power dual-band quadrature VCOs becomes more important but yet remains challenging. A low-power low-phase noise eight-phase/quadrature VCO that operates in 2.4GHz and 5.0GHz frequency bands has been finally presented in this thesis. The dual-band VCO uses the frequency doubling method to generate the higher band signals from the lower band signals, and it shows improved phase noise performance compared to other works. The VCO has been implemented in 0.18 μ m CMOS technology, and it shows a frequency from 2.23GHz—2.68GHz and 4.46GHz—5.36GHz. The measured phase difference between the I/Q signals is 90°/89° for the two frequency bands respectively. The phase noise figure-of-merit is -189.4dB and -185.1dB for the two frequency bands, while draining 2mA/5.8mA from 1.5V power supply.

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LIST OF SYMBOLS

I	In-phase (0°) signal
Q	Quadrature-phase (90°) signal
$X(S)$	Input to a system in Laplace domain
$Y(S)$	Output from a system in Laplace domain
$H(S)$	Transfer function
ω	Angular frequency
ω_C	Center frequency
f_{REF}	Reference frequency
N	Frequency divider division ratio
f_{OUT}	Output frequency
ω_{FR}	VCO free running frequency
ω_{OUT}	VCO output frequency
K_{VCO}	VCO gain
V_{ctrl}	VCO control voltage
$\Delta \omega$	Offset frequency
Q	Quality factor
L	Inductance
C	Capacitance
R	Resistance

gnd	Ground
V_{dd}	Supply voltage
V	Voltage
I	Current
g_m	Transconductance
f_{res}	Resonant frequency
M	Coupling coefficient of QVCO
$Z(j\omega)$	Impedance
W	Transistor width
L	Transistor length
I_{ds}	Transistor drain-source DC current
V_{th}	Threshold voltage

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CHAPTER 1

Introduction

1.1 Motivation

The recent advancement of deep submicron CMOS technology has made it a preferred choice for the implementation of both the RF transceiver front end and the baseband signal processor on a single-chip. From the system level consideration, an architecture that is suitable for full integration is desired. The traditional superheterodyne architecture is not suitable for System-on-Chip (SoC) implementations, because high quality filters are required for the image-rejection and the channel selection, and unfortunately, fully-integrated high performance filters are essentially not practical. To circumvent this problem, architectures such as Direct-Conversion-Receiver (DCR) and Low-IF architectures have often been chosen for the receiver, and the architectures employing direct up-conversion and two-step techniques have been devised for the transmitter [1]-[2]. The direct conversion and image reject architectures have become increasingly popular as they remove the requirements of the off-chip image reject filters. The SoC solution has, however, faced difficulties as both of these architectures require precision quadrature local oscillators. The BER of the transceiver is greatly affected by the accuracies in gain and phase shift of the quadrature signals, which cannot be maintained over wideband or multi-band standards [3]. Therefore a local oscillator that can provide accurate quadrature signals over wideband is desired.

Over the last decade, the tremendous growth of the telecommunication market has created an increasing demand for high-performance Radio Frequency (RF) circuits in low-cost technologies, including smaller size, lower power consumption hence longer battery life. Low-power design gains more and more designers' attention, and minimizing the overall power dissipation in a system has become a high priority. One of the most important reasons for this trend is the advent of portable systems. As the "on the move with anyone, anytime, and anywhere" era becomes a reality, portability becomes an essential feature of the electronic systems, emphasizing efficient use of energy as a major design objective. To extend the battery life, the low-power circuit designs become more and more important, and it is also one of the focuses of this research project.

1.2 Choice of Technologies

In order to meet these growing demands of low-cost, small area and low power, it is desirable to implement the transceiver in a single chip, i.e. monolithically. The standard CMOS process is more attractive than other processes, for example BJT and GaAs processes, because of the possibility to offer the lowest cost and the highest integration.

Although the MOS devices are considered generally to be slow and noisy, the dimension scaling has improved the speed of MOSFETs continually, increasing the intrinsic speed of MOS transistors more than three orders of magnitude in the past 30 years, and becoming comparable with that of bipolar devices. Generally RF CMOS communication ICs have the advantages of low voltage, low power, high integration, and low cost. The lower fabrication cost and possibility of placing both analog and digital circuits on the same chip so as to improve the overall performance and to reduce the cost of packaging make CMOS technology attractive [4].

Compared to GaAs, silicon suffers from a lossy substrate and hence a lower quality of on-chip passive components. However, the strong market pressure toward low price and highly integrated consumer RFICs still makes Silicon CMOS the prime technology for RF blocks.

1.3 Objectives

The goal of this research is to explore, investigate, design and compare different quadrature generators/oscillators. The quadrature generator can be implemented in many ways such as using RC-CR phase shifter [5], using RC polyphase network [6], incorporating cross-coupled quadrature voltage-controlled-oscillator [7] and so on. This research is focused on the RC polyphase network approach and the coupled quadrature voltage-controlled-oscillator (QVCO) approach. A low-power low-phase-noise dual-band quadrature oscillator is also explored.

The design of quadrature generators/oscillators presents a considerable challenge because of its simultaneous requirements for well matched in-phase signal (I) and quadrature-phase signal (Q), low phase noise, stable output amplitude and low power consumption. The lack of high quality passive components and the inadequate modeling of the transistors for their RF behavior further complicate the design.

1.4 Major contribution of the thesis

In this research, the RC polyphase network, cross-coupled quadrature voltage-controlled oscillator, and dual-band quadrature oscillators have been investigated, designed and fabricated.

The transfer functions of the 1st-, 2nd- and 3rd-order RC polyphase networks used for quadrature signal generation have been re-derived based on very basic principles. The new approach removes the need for the complex phasor and matrix analysis; and it is simple and comprehensive. The output signals' matching behavior has also been explored. A quadrature generator consisting of a VCO, a 2nd-order RC polyphase network and output buffers has been designed and fabricated. In the presence of 15% component variation, it still achieves less than 0.5dB mismatch in amplitude and much less than 0.5° phase error. The quadrature generator has a frequency tuning range from 2.18GHz to 2.48GHz and provided more than 200mV output swing. It consumed total 3.9mA current from 1.8V supply.

Besides the RC polyphase network approach, quadrature signals can be produced by cross-coupling two VCOs as well. The operation principles of the Parallel-QVCO and Series-QVCO have been presented based on circuit analysis. It has been shown that by putting the coupling transistors in parallel or in series with switching transistors, the quadrature signals can be generated intrinsically. A Parallel-QVCO and a low power Series-QVCO have been designed and fabricated. The parallel incorporates both varactor tuning and coupling coefficient tuning, thus it achieves a wider frequency

tuning range than the Series-QVCO. The Series-QVCO removes the tail current of the coupling transistors, and by using the current-reuse technique, low power consumption can be achieved. The measurement results show that the Parallel-QVCO's output frequency tuning range is 16.42% with maximum 6.12mW power consumed. The Series-QVCO has a frequency tuning range of 10.53%, and it provides more than 241mV output amplitude with only 1.5mA current consumed, which is low-power consuming compared to other state-of-the-art designs.

The design of a low-power low-phase noise eight-phase/quadrature VCO that operates in 2.4GHz and 5.0GHz frequency bands has also been presented. The dual-band VCO uses the frequency doubling method to generate the higher band signals from the lower band signals, and it shows improved phase noise performance compared to other works. The VCO has been implemented in 0.18 μ m CMOS technology, and its output frequency ranges from 2.23GH to 2.68GHz and 4.46GH to 5.36GHz. The measured phase differences between the I/Q signals are 90.0° and 88.9° for the two frequency bands respectively. The phase noise figure-of-merit is -189.4dB and -185.1dB for the two frequency bands, while draining 2mA/5.8mA from 1.5V power supply.

1.5 Organization of the Thesis

This thesis is organized into six chapters.

Chapter 1 provides the background to the design of quadrature oscillators/generators. The motivation for wideband low-power quadrature generator design is discussed. The choice of technologies, the objectives of this project, the major contribution of the research and an outline of the thesis are also presented.

Chapter 2 provides an overview of quadrature generator designs. The design considerations of quadrature generators are firstly presented; and it is followed by a general discussion of the VCO designs. Several types of oscillators such as Colpitts LC oscillators, cross-coupled oscillators and ring oscillators will be presented. Recent works on the VCO, the phase shifter and the QVCO designs will be highlighted.

In Chapter 3, the RC polyphase network working as a phase shifter will be studied. Its transfer functions will be re-derived using a simple and novel approach. Subsequently, a quadrature generator design utilizing the RC polyphase network will be presented and its performance will be shown.

Chapter 4 takes a look at the design of Parallel QVCO and Series QVCO. This chapter explains how are the quadrature signals generated from the Parallel- and Series- cross coupled topologies. After that the designs of Parallel QVCO and Series QVCO are discussed in detail. Finally the measurement results of the Parallel QVCO and Series QVCO are presented and compared with the quadrature generator using RC polyphase

network approach. A cascode QVCO design is also introduced in this chapter. Its simulation results are shown and its limitation will be discussed as well.

Chapter 5 discusses the design of low-power low-phase-noise dual-band quadrature oscillator. The circuit operation is analyzed and its performance will be presented and compared with other state-of-the-art designs.

Finally, Chapter 6 concludes the report with a summary of results and a list of key research areas for further investigation. Future work is also recommended.

CHAPTER 2

Overview of Quadrature Generator Design

2.1 Design Considerations of Quadrature Generator

There are some parameters that researchers need to consider when designing a quadrature generator. These parameters include frequency tuning range, phase noise, I/Q matching, power consumption and so on. This section will present some discussions on these design considerations.

2.1.1 Frequency Tuning Range

The frequency tuning range is an important parameter of the quadrature generator. In the channel frequency synthesizer, the local oscillator must be able to track all the channels. A VCO/QVCO can be modeled by a frequency generator whose frequency is a linear function of a control voltage, V_{ctrl} :

$$\omega_{out} = \omega_{FR} + K_{VCO} \cdot V_{ctrl} \quad (2.1)$$

where ω_{FR} is the free-running frequency and K_{VCO} is the frequency-to-control voltage gain of the VCO/QVCO specified in $rad/s/V$ [8]. From the above equation, we can see the frequency tuning range of the VCO/QVCO depends on the available varying range of the control voltage and the gain of the VCO/QVCO.

2.1.2 Phase Noise

Figure 2.1 Output spectrum of oscillators

(a) without phase noise (b) with non-zero phase noise

As other analog circuits, oscillators are susceptible to noise. Noise of an oscillator can be divided into two types, the amplitude noise and the phase noise. Amplitude noise, the disturbance in the amplitude of the oscillator output signal, is usually less important and negligible compared to phase noise. Phase noise creates errors or random deviations of the frequency of the oscillator output signal. In ideal case without phase noise, the spectrum of an oscillator working at the frequency of ω_c is a single line as an

impulse. However, for an actual oscillator with non-zero phase noise, the spectrum exhibits “skirts” around the oscillating frequency as shown in Figure 2.1. The definition of the phase noise is the noise power in a unit bandwidth at an offset of $\Delta\omega$ from the center frequency ω_c , divided by the carrier power. The output noise can be mathematically expressed in Leeson’s Equation [9]:

$$\left| \frac{Y}{X}(j\omega) \right|^2 = \frac{1}{4Q^2} \left(\frac{\omega_c}{\Delta\omega} \right)^2 \quad (2.2)$$

where $\left| \frac{Y}{X}(j\omega) \right|$ is the transfer function of the noise appeared in the VCO loop, Q is the quality factor of the oscillator, ω_c is the oscillating frequency and $\Delta\omega$ is the offset frequency.

Phase noise in oscillators has been extensively analyzed in [10]-[14]. The main sources of phase noise in CMOS oscillators are the noise of the LC tank, $1/f$ noise of the active devices [9][15], the noise from the tail transistors and the noise coming from the supply and the substrate [16]. Generally, the phase noise of a VCO comes from two paths: the signal path and the control path. While the thermal noise in the signal path determines the noise floor of the VCO output, the low-frequency flicker noise in the control path actually modulates the carrier frequency and is up-converted into the close-in phase noise [11][17]-[18], making the $1/f$ noise in the control path particularly detrimental [8].

The finite phase noise may corrupt the wanted signal due to the “reciprocal mixing” as illustrated in Figure 2.2. Besides the wanted signal, the possible adjacent interferer is

also down-converted during the mixing process. Consequently the down-converted band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to the tail of the interferer [19].

Figure 2.2. Reciprocal mixing with non-ideal oscillator

2.1.3 I/Q Matching

The quadrature generator is to provide well-matched 0° -phase (I) and 90° -phase (Q) signals. The matching behavior of I/Q signals can be described in terms of amplitude matching and phase matching. In the ideal case, the I/Q signals have the same amplitude with 90° phase difference. However, in the real practice, the I/Q signals are not perfectly matched. The mismatch between I/Q signals may be due to components mismatch and/or asymmetrical layouts in I/Q paths. In an image reject down converter, the mismatch between I/Q signals will degrade the image rejection. In a direct conversion receiver, the mismatch will increase the BER.

The following analysis shows how does the I/Q matching affect the image rejection performance:

A typical directly conversion transceiver's up-conversion stage can be configured as in Figure 2.3 (a) or (b). In both configurations, the output signal consists of lower side band and upper side band. In Figure 2.3 (a), the signals from the two paths are added together, and the lower side band is the desired signal to be transmitted, and the upper side band is the unwanted signal, in another word, the "image". Figure 2.3 (b) is in the other way round: the signals from the two paths are in subtraction, and the upper side band is the wanted signal and lower side band is the image.

Figure 2.3 Up-conversion stage of the direct conversion transceiver
(a) in addition configuration (b) in subtraction configuration

The IF quadrature input signals are assumed to be perfectly matched, and they can be expressed as $A_{IF} \sin(\omega_{IF}t + \Delta)$ and $A_{IF} \cos(\omega_{IF}t + \Delta)$ respectively, where A_{IF} is the amplitude of the IF signal, ω_{IF} is the IF frequency, and Δ denotes the phase of the IF input signal with respect to the local oscillator signal. Taking into consideration of the mismatch in amplitude and phase, the local quadrature signals can be expressed as $A_{LO1} \cos(\omega_{LO}t)$ and $A_{LO2} \cos(\omega_{LO}t + \theta)$ respectively, where A_{LO1} and A_{LO2} are the amplitudes of the local quadrature signals, which may not be the same; ω_{LO} is the local oscillator's frequency; and θ is the phase error of the local quadrature signals. The output signal V_{out} in Figure 2.3 (a) can be calculated as:

$$\begin{aligned}
 V_{out} &= A_{IF} \cos(\omega_{IF}t + \Delta) A_{LO1} \cos(\omega_{LO}t) + A_{IF} \sin(\omega_{IF}t + \Delta) A_{LO2} \sin(\omega_{LO}t + \theta) \\
 &= \frac{1}{2} A_{IF} A_{LO1} \{ \cos[(\omega_{IF} + \omega_{LO})t + \Delta] + \cos[(\omega_{LO} - \omega_{IF})t - \Delta] \} - \\
 &\quad \frac{1}{2} A_{IF} A_{LO2} \{ \cos[(\omega_{IF} + \omega_{LO})t + \Delta + \theta] - \cos[(\omega_{LO} - \omega_{IF})t - \Delta + \theta] \} \quad (2.3) \\
 &= \frac{1}{2} A_{IF} A_{LO1} \cos[(\omega_{LO} - \omega_{IF})t - \Delta] + \frac{1}{2} A_{IF} A_{LO2} \cos[(\omega_{LO} - \omega_{IF})t - \Delta + \theta] \\
 &\quad + \frac{1}{2} A_{IF} A_{LO1} \cos[(\omega_{IF} + \omega_{LO})t + \Delta] - \frac{1}{2} A_{IF} A_{LO2} \cos[(\omega_{IF} + \omega_{LO})t + \Delta + \theta]
 \end{aligned}$$

The expressions of the lower side band (LSB) signal and the upper side band (USB) signal can be further calculated as:

$$\begin{aligned}
 V_{out}(LSB) &= \frac{1}{2} A_{IF} A_{LO1} \cos[(\omega_{LO} - \omega_{IF})t - \Delta] + \frac{1}{2} A_{IF} A_{LO2} \cos[(\omega_{LO} - \omega_{IF})t - \Delta + \theta] \\
 &= \frac{1}{2} A_{IF} A_{LO1} \cos[(\omega_{LO} - \omega_{IF})t - \Delta] + \frac{1}{2} A_{IF} A_{LO2} \{ \cos[(\omega_{LO} - \omega_{IF})t - \Delta] \cos \theta - \sin[(\omega_{LO} - \omega_{IF})t - \Delta] \sin \theta \} \\
 &= \left(\frac{1}{2} A_{IF} A_{LO1} + \frac{1}{2} A_{IF} A_{LO2} \cos \theta \right) \cos[(\omega_{LO} - \omega_{IF})t - \Delta] - \frac{1}{2} A_{IF} A_{LO2} \sin \theta \sin[(\omega_{LO} - \omega_{IF})t - \Delta] \quad (2.4)
 \end{aligned}$$

Letting $A = \frac{1}{2} A_{IF} A_{LO1} + \frac{1}{2} A_{IF} A_{LO2} \cos \theta$, and $B = \frac{1}{2} A_{IF} A_{LO2} \sin \theta$, we can get:

$$\begin{aligned} V_{out}(LSB) &= A \cos[(\omega_{LO} - \omega_{IF})t - \Delta] - B \sin[(\omega_{LO} - \omega_{IF})t - \Delta] \\ &= \sqrt{A^2 + B^2} \left\{ \frac{A}{\sqrt{A^2 + B^2}} \cos[(\omega_{LO} - \omega_{IF})t - \Delta] - \frac{B}{\sqrt{A^2 + B^2}} \sin[(\omega_{LO} - \omega_{IF})t - \Delta] \right\} \end{aligned} \quad (2.5)$$

Letting $\cos \varphi = \frac{A}{\sqrt{A^2 + B^2}}$ and $\sin \varphi = \frac{B}{\sqrt{A^2 + B^2}}$, we obtain:

$$\begin{aligned} V_{out}(LSB) &= \sqrt{A^2 + B^2} \{ \cos \varphi \cos[(\omega_{LO} - \omega_{IF})t - \Delta] - \sin \varphi \sin[(\omega_{LO} - \omega_{IF})t - \Delta] \} \\ &= \sqrt{A^2 + B^2} \cos[(\omega_{LO} - \omega_{IF})t - \Delta + \varphi] \end{aligned} \quad (2.6)$$

where $\varphi = \tan^{-1} \frac{B}{A}$. Therefore, substituting A and B into equation (2.6), we can obtain

the amplitude of the lower side band signal:

$$\begin{aligned} |V_{out}(LSB)| &= \sqrt{A^2 + B^2} \\ &= \sqrt{\frac{1}{4} A_{IF}^2 A_{LO1}^2 + \frac{1}{4} A_{IF}^2 A_{LO2}^2 \cos^2 \theta + \frac{1}{2} A_{IF}^2 A_{LO1} A_{LO2} \cos \theta + \frac{1}{4} A_{IF}^2 A_{LO2}^2 \sin^2 \theta} \\ &= \sqrt{\frac{1}{4} A_{IF}^2 A_{LO1}^2 + \frac{1}{4} A_{IF}^2 A_{LO2}^2 + \frac{1}{2} A_{IF}^2 A_{LO1} A_{LO2} \cos \theta} \end{aligned} \quad (2.7)$$

By using the same manipulation method, we can get the amplitude of the upper side band signal:

$$\begin{aligned} |V_{out}(USB)| &= \sqrt{\frac{1}{4} A_{IF}^2 A_{LO1}^2 + \frac{1}{4} A_{IF}^2 A_{LO2}^2 \cos^2 \theta - \frac{1}{2} A_{IF}^2 A_{LO1} A_{LO2} \cos \theta + \frac{1}{4} A_{IF}^2 A_{LO2}^2 \sin^2 \theta} \\ &= \sqrt{\frac{1}{4} A_{IF}^2 A_{LO1}^2 + \frac{1}{4} A_{IF}^2 A_{LO2}^2 - \frac{1}{2} A_{IF}^2 A_{LO1} A_{LO2} \cos \theta} \end{aligned} \quad (2.8)$$

The image rejection ratio can be calculated from equation (2.7) and equation (2.8):

$$\begin{aligned}
 IRR = \frac{USB}{LSB} &= \sqrt{\frac{\frac{1}{4}A_{IF}^2 A_{LO1}^2 + \frac{1}{4}A_{IF}^2 A_{LO2}^2 - \frac{1}{2}A_{IF}^2 A_{LO1} A_{LO2} \cos \theta}{\frac{1}{4}A_{IF}^2 A_{LO1}^2 + \frac{1}{4}A_{IF}^2 A_{LO2}^2 + \frac{1}{2}A_{IF}^2 A_{LO1} A_{LO2} \cos \theta}} \\
 &= \sqrt{\frac{A_{LO1}^2 + A_{LO2}^2 - 2A_{LO1} A_{LO2} \cos \theta}{A_{LO1}^2 + A_{LO2}^2 + 2A_{LO1} A_{LO2} \cos \theta}} \quad (2.9)
 \end{aligned}$$

For the direct-conversion transceiver configured in Figure 2.3(b), it can be proved in the similar with that:

$$|V_{out}(LSB)| = \sqrt{\frac{1}{4}A_{IF}^2 A_{LO1}^2 + \frac{1}{4}A_{IF}^2 A_{LO2}^2 - \frac{1}{2}A_{IF}^2 A_{LO1} A_{LO2} \cos \theta} \quad (2.10)$$

$$|V_{out}(USB)| = \sqrt{\frac{1}{4}A_{IF}^2 A_{LO1}^2 + \frac{1}{4}A_{IF}^2 A_{LO2}^2 + \frac{1}{2}A_{IF}^2 A_{LO1} A_{LO2} \cos \theta} \quad (2.11)$$

$$IRR = \frac{LSB}{USB} = \sqrt{\frac{A_{LO1}^2 + A_{LO2}^2 - 2A_{LO1} A_{LO2} \cos \theta}{A_{LO1}^2 + A_{LO2}^2 + 2A_{LO1} A_{LO2} \cos \theta}} \quad (2.12)$$

Both configurations have the same expression for the image reject ration. If the local oscillator's I/Q amplitude is well matched, that is, $A_{LO1} = A_{LO2} = A_{LO}$, the image rejection ratio can be simplified to:

$$IRR' = \sqrt{\frac{A_{LO}^2 + A_{LO}^2 - 2A_{LO}^2 \cos \theta}{A_{LO}^2 + A_{LO}^2 + 2A_{LO}^2 \cos \theta}} = \sqrt{\frac{1 - \cos \theta}{1 + \cos \theta}} \quad (2.13)$$

Figure 2.4 shows the relationship between the image rejection ration and the I/Q mismatch based on equation (2.9) and (2.13). It is clear that the image rejection

performance can get better with smaller I/Q amplitude mismatch and smaller I/Q phase error. For the practical designs reported in literature, the image rejection ratio can achieve less than -40dB, which corresponds to less than 1.15° degree phase error assuming that there is no amplitude mismatch [20]-[24].

Figure 2.4 Image rejection ratio versus phase error and amplitude mismatch

2.1.4 Other Parameters

Besides the frequency tuning range, phase noise and I/Q matching, there are still other parameters that the designers should consider when designing the quadrature generator, such as output amplitude, power consumption and silicon area. The output amplitude of the quadrature generator will affect the noise performance of the mixer significantly

[8]. The output amplitude is required to be high enough to ensure the differential pairs in a double-balanced Gilbert cell mixer function like a switch. The power consumption of the quadrature generator needs to be kept as low as possible and a small silicon area is also desired.

2.2 VCO Design

The quadrature generator can be implemented by using RC polyphase network approach or QVCO approach. For both approaches, the voltage-controlled-oscillator (VCO) is the key element.

An Oscillator is a self-sustaining frequency generator with a closed feedback loop. The circuit sustains the output without an input, which means that the circuit uses the positive feedback and amplifies its own noise at some specific frequency ω_c . Figure 2.5 shows a typical oscillator topology:

Figure 2.5 Typical oscillator topology

Its transfer function is:

$$\frac{Y(S)}{X(S)} = \frac{H(S)}{1 - H(S)} \quad (2.14)$$

where $Y(S)$ is the output, $X(S)$ is the input, and $H(S)$ is the open-loop gain.

In order to start and maintain a stable oscillation, the oscillator is required to satisfy the Barkhausen's Criteria: The loop gain must be higher than or equal to unity, i.e.

$|H(S)| \geq 1$, and the total phase shift of the loop must be equal to 360° , that is,

$$\angle H(S) = 360^\circ.$$

In an environment with the existence of all frequency noises, the Barkhausen's Criteria is satisfied only with the noise at a specific frequency ω_c . When the oscillation is properly started, the noise signal at frequency ω_c is amplified and increased until the amplifying devices are saturated; hence the stable oscillation is maintained.

In RF circuit design, to achieve high oscillation frequency and low phase noise, LC oscillators with high quality factor (Q) are preferred to the other topologies [25]. A brief description of these topologies is given below.

2.2.1 Colpitts and Hartley LC VCOs

Figure 2.6 (a) Colpitts LC oscillator (b) Hartley LC oscillator

Colpitts and Hartley are two types of LC oscillators, with different methods of impedance transformation. The Colpitts LC oscillator utilizes a capacitance divider to supply the high enough loop gain while forming the positive feedback as shown in Figure 2.6(a), while an inductance divider is employed in the Hartley LC structure as

shown in Figure 2.6(b). Although theoretically both are feasible, in reality the Colpitts structure is more popularly used because it requires less inductors.

2.2.2 Cross-Coupled LC VCO

Figure 2.7 The cross-coupled Colpitts VCO

In order to drive a mixer, the local oscillator is usually required to have differential outputs because the commonly used mixer in RF systems are the balanced passive mixer [26] and Gilbert-Cell mixer [27] which require differential RF inputs. A differential implementation of the Colpitts LC VCO, also called the cross-coupled structure is shown Figure 2.7.

The cross-coupled transistors pair in Figure 2.4 can be shown to have negative impedance of $-2/g_m$ [8]. Hence, with enough negative impedance, the cross-coupled pair can compensate for the loss of the LC tank and maintain the stable oscillation. Consequently, the cross-coupled LC oscillator is also called the negative-Gm oscillator.

The variable capacitors C_1 and C_2 are used to tune the resonant frequency of the LC tank or the oscillating frequency of the circuit, that is:

$$f_{out} = f_{res} = \frac{1}{2\pi\sqrt{LC_{tank}}} \quad (2.15)$$

The two LC tanks in Figure 2.7 are assumed to be identical, hence $L_1 = L_2 = L$ and $C_1 = C_2 = C$. L and C_{tank} in equation (2.15) denote the inductance and the total capacitance of each LC tank, respectively. For example, as shown in Figure 2.7, C_{tank} includes the variable capacitance, i.e. varactor, the parasitic capacitance of the inductors if they are implemented on chip, and the parasitic capacitance at the gate and drain of the MOSFETs M_1 and M_2 . The resonant frequency can be tuned by varying the varactor through a control voltage, but the tuning range is restricted by two factors. One is the limited variable range of the control voltage for maintaining the reverse biasing requirement of the varactor. The other factor is the contribution of varactors to the overall capacitance. Since there are parasitic capacitances in the MOSFET and on-chip inductors, the varactors usually constitute only a portion of the total tank capacitance. Therefore the maximum variable capacitance is quite limited.

2.2.3 Ring Oscillator

Figure 2.8 A three-stage ring oscillator

Ring oscillators usually employ three or more stages in a loop configuration [28]-[31]. Figure 2.8 is an example of three-stage ring oscillators, where the gain stage can be either common-source stage, CMOS inverting stage, or differential stages. In order to maintain an oscillation at a certain frequency, like LC oscillators, the Barkhausen Criteria must be satisfied. Therefore, the number of the inversion stages in the loop must be odd so that the circuit can oscillate, rather than latch up [4]. If the cross-coupling topology is used as shown in Figure 2.9, even number of differential inverters can be used too [32]. Because the cross-coupling structure can be considered as another inverting stage, so the total number of the inverting stages is still odd.

Figure 2.9 A four-stage differential ring oscillator

If there is even number of inverting stages in the loop, the overall DC phase shift around the loop is 0° . As a result the positive feedback at DC will finally drive the transistors to be either turned off or with a very high biasing current. For an odd number of inverting stages, the total phase shift of the loop is dependent on the frequency. Therefore the 360° phase condition of the Barkhausen's Criteria is satisfied at only a specific frequency.

The oscillation frequency of ring oscillators is determined by either the 3-dB bandwidth of each stage or the time delay of each stage, depending on whether the circuit is

working in a small signal condition with an output resistance or in a large signal case with the rail-to-rail swing [4]. Hence, the oscillation frequency of an N-stage ring oscillator can be tuned by varying the large signal delay of each stage [30].

In the absence of a frequency selective network such as the LC resonator, the ring oscillator is easy to implement with the current integration technology, but it suffers from a relatively high phase noise, compared to the LC oscillator [28]. In addition, the multiple stages also make contributions to the noise level, making the ring oscillator unpopular in RF systems.

2.2.4 Literature Survey on Oscillators

2.2.4.1 Wideband VCO with Active Inductors

To overcome the limitations imposed on the tuning range, the concept of the frequency tuning by active inductors has been introduced [33]-[34]. Owing to the wide inductance range provided by the tunable active inductors, a frequency tuning range up to 120% has been reported for a single-ended VCO at multi-gigahertz frequencies [35]. In 2006, L. L. Liu, Y. T. Liao and H. H. Hsieh proposed a new circuit topology to further improve the performance of the wide-tuning-range VCOs with active inductors as shown in Figure 2.10 [36]. The active inductor was realized by six transistors, and it could achieve a high quality factor and occupy a small silicon area. The LC-tank was formed by the tunable active inductor and a varactor for frequency control, and the negative conductance was employed to compensate for the loss from the LC-tank.

Figure 2.10 VCO with active inductor

Since the equivalent inductance of an active inductor can be tuned over a wide range, it was employed as the mechanism for coarse frequency tuning or band selection. In addition, varactors were included in the LC-tank for fine tuning, maintaining a relatively low tuning sensitivity to ensure the frequency stability.

By utilizing the differential active inductor and varactor for the LC-tank, the circuit exhibited a very wide frequency tuning range from 500MHz to 3.0GHz. The circuit performance was also enhanced in terms of phase noise, which was -101dBc/Hz at 1MHz offset.

2.2.4.2 Low-Phase-Noise VCO

A low voltage low phase noise multiband all-PMOS VCO was reported by Z. B. Li and K. O. Kenneth [37]. By using a combination of inductor and capacitor switching, a four band (2.4GHz, 2.5GHz, 4.7GHz and 5GHz) operation was realized. In this design, PMOS was used instead of NMOS. As PMOS transistors have 10dB lower $1/f$ noise compared to that for NMOS transistors in 0.18 μ m CMOS process; PMOS VCOs can achieve better phase noise performance than NMOS VCOs. As a result, The VCO with a 1-V power supply had a phase noise of -126 dBc/Hz at 1-MHz offset from a 4.7GHz carrier and -134 dBc/Hz from a 2.4GHz carrier.

The good phase noise performance came with the price of lower frequency tuning range. For a given current, PMOS transistors have larger size than NMOS transistors to achieve the same g_m . Because of this, the VCO core using PMOS transistors has larger parasitic capacitance, achieving a smaller tuning range than its NMOS counterpart.

2.2.4.3 Low-Power/Low-Voltage VCO

The continuous growth of personal wireless communications demands low power solutions in the design of wireless systems. Wireless transceivers for many standards such as GSM, Bluetooth and WLAN and so on require low-power design techniques to enhance their battery lifetime and to improve their portability [38]. Being a crucial part in wireless transceivers, the designs of low-power/low-voltage VCO attracts researchers' attention.

The bottleneck of low-power/low-voltage VCO is the limited output swing, which in turn limits the phase noise. K. Kwok and Howard C. Luong presented two high performance ultra-low-voltage VCOs using transformer feedback in 2005 [39]. Dual signal swings concept has been proposed in [39], which enabled the output signals to swing above the supply voltage and below the ground potential to increase the output amplitude and to lower the phase noise. The transformer feedback also improved the oscillator's loaded quality factor thus enhance the phase noise performance. The two proposed designs achieved -128.6dBc/Hz phase noise at 1MHz offset with 1.46mW power consumption, and -119dBc/Hz at 1MHz offset with 0.57mW power consumption respectively.

[40] proposed another low-power VCO by using a large value of parallel capacitor, an additional harmonic-suppressed capacitor, and an appropriate bulk bias voltage of transistor. The proposed design consumed 1.9mW power and achieved -119dBc/Hz at 1MHz offset.

2.3 Phase Shifter Design

The outputs from a conventional VCO are usually differential, thus a phase shifter is needed to shift the signals to be quadrature. The phase Shifter can be realized by a simple RC-CR network or a polyphase network. The RC-CR network shifter can shift the phase by 90° at a single frequency, but it is not suitable for wideband applications. The polyphase network may be implemented in passive or active form. At a certain frequency, the outputs from the polyphase network will have a 90° phase difference from each other.

2.3.1 Passive Polyphase Network

Figure 2.11 Schematic of passive RC polyphase network

The schematic of the passive polyphase network is shown in Figure 2.11. It consists of only resistors and capacitors. Its transfer function is obtained through a frequency translation of the high pass filter transfer function [41]. While a high pass filter will have a notch at DC (0 Hz), the passive polyphase network has the notch at the unwanted frequency.

One stage polyphase network has one pole at $1/(2\pi RC)$, where R is the resistance and C is the capacitance used in the network. By cascading several stages, the bandwidth is extended. The number of stages required in the cascade depends on the frequency band requirements. N -stage polyphase network have N poles at $1/(2\pi R_n C_n)$ respectively. Hence the resistor and capacitor value for each stage can be calculated if the locations of poles are known.

Although passive polyphase filter is extensively used, it still has its own limitation. Signal will be attenuated by 3dB for every stage. So there is a trade off between bandwidth and signal strength. To achieve a larger bandwidth, more stages will be used, which lead to larger attenuation. To compensate the signal loss, common source differential amplifier is usually inserted, which causes extra power consumption.

2.3.2 Active Polyphase Network

The schematic of an active polyphase network is shown in Figure 2.12 [42]. It utilizes active devices to provide gain. Unlike the passive implementation, the active polyphase network transfer function is obtained by applying a frequency translation to the low pass filter transfer function. Similar to the passive polyphase network, the active implementation may only pass one direction phasor signal while rejecting the other.

Figure 2.12 Schematic of active polyphase network

2.3.3 Comparison between passive and active polyphase networks

To generate quadrature signals, the method of using a differential VCO followed by a polyphase network is easy to implement. Compared to the passive polyphase network, the active polyphase network is able to provide gain to the signal. This, of course, comes with the price of higher power consumption. The increasing number of cascaded stages gives a better image rejection and wider operating bandwidth. However, there is a problem when the network is to be used for wideband operation. More polyphase networks are to be cascaded for higher rejection and wider bandwidth requirements. As

more stages are required, the network will introduce more noise and the phase accuracy deteriorates. The passive polyphase network is more suitable for wideband application; because it can provide a more accurate 90° phase shift over a wide bandwidth [43]. As the passive polyphase network has low input impedance, it cannot be driven directly by VCO. Therefore, an input buffer is usually added between VCO and the passive polyphase network. Similarly, an output buffer is also necessary for driving the next stage. Moreover, these buffers also add in parasitic effects which may deteriorate the phase accuracy of the quadrature signals.

2.4 Design of QVCO

2.4.1 Conventional QVCO

In 1996, Rofougaram [21] firstly proposed an oscillator with the coupled architecture in order to produce quadrature outputs without using the complex quadrature generator or phase shifter. With two differential frequency-fixed oscillators coupled through some transistors, the ultimate frequency of the overall oscillator was different from that of the original oscillators and was decided by both the original frequency and the coupling coefficients. This new topology of quadrature oscillator attracted attention of many researchers.

Figure 2.13 Block diagram of the QVCO

In 1999, a QVCO architecture was proposed using the same principle [44]. Because the frequency of the QVCO can be easily tuned by the coupling coefficients, without using any varactors, the limitation of the varactor tuning range does not exist any longer. Figure 2.13 shows the block diagram of the proposed QVCO. G_1 and G_2 are two identical fixed frequency oscillators. The output of one oscillator is coupled to the input

of the other oscillator with the coupling coefficients M_1 and M_2 . If in a steady state, the two oscillators synchronize to a single oscillation frequency ω . The output of each oscillator must satisfy the following equations:

$$(X + M_2 Y)G_1(j\omega) = X \quad (2.16)$$

$$(Y + M_1 X)G_2(j\omega) = Y \quad (2.17)$$

Since the oscillators are identical, $G_1 = G_2 = G$ and $M_1 = M_2 = M$ can be satisfied. Then it can be obtained from equations (2.16) and (2.17) that $X^2 + Y^2 = 0$ and thus $X = \pm jY$, which means that the phase of signal X is 90° different from signal Y . Therefore quadrature signals are produced.

In 2003, a novel dual-band QVCO design was presented in [45]. It combined both the varactor tuning technique and the coupling coefficient tuning technique to achieve dual-band operation. In this design, the fixed capacitors used in [46] were replaced by the varactors, and two control voltages were used to get a dualband QVCO. The first control voltage, which controlled the capacitance of the varactor, was used as the switching voltage to select one of two independent bands. The second control voltage, which was to control the coupling coefficient, was used to tune the frequency between two extreme ends of each band. A low harmonic technique was also employed in the design. This was done by a compensation circuit, which was actually an inverting voltage-current converter. Through this technique, the biasing voltages of the varactors were kept at a relatively constant value, hence improving the harmonic performance.

However, this design had a large current consumption, which was not suitable for low power applications.

2.4.2 Low-Phase-Noise QVCO

Conventional QVCOs [21], [44] operate away from the resonant frequency to create the required phase shift, which penalizes their Figure of Merit (FOM). Super-harmonic-coupled (SHC) QVCOs [46]-[47] do not have this problem, but they are not particularly effective in reducing phase noise. The phase noise can be reduced by combining two copies of differential VCOs together at NMOS and PMOS tail nodes by separate LC tanks [48]. The cross-coupled pairs acted as bi-directional gateways converting the oscillation frequency f_0 to $2f_0$ and $2f_0$ to f_0 and allowed energy to circulate among the main and tail tanks. Through this topology, the effective capacitance was made larger than the actual capacitance. Thus thermal noise was attenuated by the larger effective capacitance. Moreover, when the switching transistors entered the deep triode region, its resistance was approximately 30 times lower than the impedance of the LC tanks combined together at f_0 and $2f_0$. Therefore only a fraction of the available noise power from a triode-region transistor can be injected into the system due to the impedance mismatch. Although this design had a good performance on phase noise, its power consumption was 27.7mW and it was not suitable for low power applications [48].

2.4.3. Current Mode Oscillator

Implementing quadrature oscillators in current-mode attracts designers' attentions because of their ultra-low power feature. Current-mode oscillators utilizing current conveyors have been presented in [49]-[51]. The oscillators provided sinusoid waves with less than 1mA current consumption. However, due to the limitations of the current conveyors, those circuits only operate at Megahertz range, and they are not suitable for RF application. Moreover, the current conveyors use the bipolar junction transistors (BJTs) have higher cost compared to CMOS process.

A current-mode low-power quadrature oscillator through the use of only current mirrors with all NMOS transistors was discussed in [52]. Figure 2.14 show the small-signal block diagram and the circuit configuration of the quadrature generator. The low pass filters F_1 - F_4 consist of current mirrors, and they are connected in the closed loop. By adjusting the transistors sizes in the current mirrors properly, the circuit can provide quadrature signals at around 2.8GHz with a current consumption of 150uA. However, there are still some limitations on this circuit. First, the frequency tuning is achieved by varying the bias current I , but the bias current cannot go beyond a certain range as the transistor in the current source must be maintained in the saturation region. Second, the output quadrature signals are in the form of current, therefore an extra current-to-voltage converter may be needed when integrating this quadrature oscillator with other RF front-end blocks. Last, the phase noise performance degrades for the current-mode oscillator. In this design, the simulated phase noise is -71dBc/Hz at 1MHz offset, which is very high compared to the phase noise of a voltage-mode oscillator. Therefore, this

current-mode quadrature oscillator is suitable for the systems with less stringent requirements on phase noise and frequency tuning range, but ultra-low power consumption is required.

Figure 2.14 Small signal block diagram of the current-mode quadrature oscillator

2.5 Summary

In this chapter, an overview of the quadrature generators was presented. The design considerations such as frequency tuning range, phase noise and power consumption and so on are firstly presented. The VCO is the key element in a quadrature generator. The design of VCO has been studied, and various research work done on the VCO has also been explored. The designs of phase shifters were introduced subsequently, which include RC-CR phase shifter, passive RC polyphase network and active polyphase network. Lastly, the QVCO design was discussed, and the low phase noise QVCO and low power QVCO designs reported in literature have also been highlighted.

CHAPTER 3

Analysis and Design of Quadrature Generator Using RC Polyphase Network Approach

As discussed in previous chapters, the quadrature signals are needed in most transmitters and receivers for either vector modulation and demodulation or image rejection or both. There are several ways to generate quadrature signals. One popular method is to use a differential VCO that oscillates at twice a desired frequency, and then to obtain quadrature waveforms via frequency division [53]. However, a higher oscillation frequency and the frequency division result in increased power consumption. For narrow band applications, the simplest way is to use a RC-CR phase-shift network, which can shift the outputs by $\pm 45^\circ$ with respect to one another [54]. Another way is to use gm-C networks [55] to generate quadrature signals. The fourth way is to use RC polyphase network; and the last method is to use a quadrature voltage controlled oscillator (QVCO) [21][44]-[56] to generate quadrature signals directly. The RC-CR phase shifter and gm-C approaches have their limitations on bandwidth, phase accuracy or I/Q matching. Hence currently, the QVCO and RC polyphase network are still the popular approaches used for quadrature signal generation. This chapter will describe the analysis and design of broadband quadrature generator using RC polyphase network approach, and next chapter will focus on the QVCO design.

The RC polyphase network can provide an efficient solution for two main bottlenecks in the design of RF integrated transceivers [57]. The first is the generation of highly matched wide-band quadrature signals which are insensitive to components mismatch. The second is the suppression of the image signals without the need for highly selective RF networks and without employing image-reject techniques. The RC polyphase network can be configured in different ways by giving different input combination, and the different configurations will provide different characteristics to the RC polyphase networks. Therefore the designers can use one proper configuration to suit the design purpose. There is a lot of research work done on RC polyphase networks used for image rejection [41][57]-[59]. However, little work have focused on the other functions of the RC polyphase network – for quadrature signal generation, so this section will give a detailed analysis of RC polyphase network used as a quadrature generator.

3.1 Derivation of Transfer Functions for RC Polyphase Networks

The transfer functions for RC polyphase networks have been derived in [41] and [60]. However, the analysis was based on a concept of complex signal and circulant matrix properties in [60]; and phasor decomposition and matrix analysis in [41]. Both methods are complicated. For an RC polyphase network used as a quadrature signal generator, the consideration of phase sequence is not important anymore. Therefore the following analysis does not include any complex phasor or matrix analysis compared to previous works; and it re-derives the transfer functions for first-, second- and third-order RC polyphase networks by using some fundamental principles such as Ohm's Law and linear superposition. It is believed that the new approach is more explicit and comprehensive, which allows the characteristics of a RC polyphase network used as a quadrature generator to be easily understood. The transfer functions of higher-order RC polyphase networks can be obtained with the same approach. In the following sections, the amplitude and phase response of the 1st-, 2nd- and 3rd order RC polyphase networks configured as quadrature generators is plotted to give a better illustration of the characteristics of the network, which has not been shown in the previous works using circulant matrix or phasor approaches.

3.1.1 First-order RC Polyphase Network

The basic building block of a RC polyphase network is shown in Figure 3.1. Since all components are passive, and the system is linear, the linear superposition applies.

Therefore each output can be found as the sum of output signals contributed by individual input signal. For example, by breaking the RC chain and redrawing the polyphase network in another way as shown in Figure 3.2, the four outputs I_{out+} , I_{out-} , Q_{out+} and Q_{out-} can be calculated easily. Here we denote I_{in+} and I_{in-} as the input in-phase differential signals; Q_{in+} and Q_{in-} as the input quadrature-phase differential signals; I_{out+} and I_{out-} as the output in-phase differential signals; and Q_{out+} and Q_{out-} are the output quadrature-phase differential signals.

Figure 3.1 RC polyphase building block

Figure 3.2 Output signals contributed by:

(a) I_{in+} alone (b) Q_{in+} alone (c) I_{in-} alone (d) Q_{in-} alone

Therefore, by applying superposition principle, we can get:

$$\begin{aligned}
 I_{out+} &= I_{out+,a} + I_{out+,b} + I_{out+,c} + I_{out+,d} \\
 &= \frac{1}{1+sRC} I_{in+} + 0 + 0 + \frac{sRC}{1+sRC} Q_{in-}
 \end{aligned} \tag{3.1}$$

The other three outputs can be found in the same way:

$$Q_{out+} = \frac{1}{1+sRC} Q_{in+} + \frac{sRC}{1+sRC} I_{in+} \tag{3.2}$$

$$I_{out-} = \frac{1}{1+sRC} I_{in-} + \frac{sRC}{1+sRC} Q_{in+} \tag{3.3}$$

$$Q_{out-} = \frac{1}{1+sRC} Q_{in-} + \frac{sRC}{1+sRC} I_{in-} \tag{3.4}$$

Figure 3.3 1st-order RC polyphase network

When RC polyphase network works as a quadrature signal generator, the input does not include the quadrature components, i.e. the Q inputs are shorted to ground, i.e. $Q_{in+}=Q_{in-}=0$. Thus, the network becomes a 1st-order RC polyphase network as shown in Figure 3.3, and equations (3.1)-(3.4) can be rewritten as:

$$I_{out1+} = \frac{1}{1 + sRC} I_{in+} \quad (3.5)$$

$$Q_{out+} = \frac{sRC}{1 + sRC} I_{in+} \quad (3.6)$$

$$I_{out-} = \frac{1}{1 + sRC} I_{in-} \quad (3.7)$$

$$Q_{out-} = \frac{sRC}{1 + sRC} I_{in-} \quad (3.8)$$

Define $I_{out} = \frac{1}{2}(I_{out+} - I_{out-})$, $Q_{out} = \frac{1}{2}(Q_{out+} - Q_{out-})$ and $I_{in} = \frac{1}{2}(I_{in+} - I_{in-})$, where

$I_{in-} = -I_{in+}$, we can have:

$$I_{out} = \frac{1}{1 + sRC} I_{in} \quad (3.9)$$

$$Q_{out} = \frac{sRC}{1 + sRC} I_{in} \quad (3.10)$$

$$\frac{Q_{out}}{I_{out}} = sRC = j\omega RC \quad (3.11)$$

From equations (3.9)-(3.11), it is clear that at frequency $\omega = \frac{1}{RC}$, the 0°-phase (I) and

90°-phase (Q) output signals have the same amplitudes of $\frac{|I_{in}|}{\sqrt{2}}$; and the Q output signal

always has a 90° phase lead with respect to the I output signal. Based on equations (3.9)-(3.10), the magnitude frequency response of the first-order polyphase network can be plotted as shown in Figure 3.4(a). Here the operating frequency f_0 is set to be

2.45GHz, and the value of RC can be calculated from $\frac{1}{RC} = 2\pi f_0$, where $f_0=2.45\text{GHz}$.

The mismatch between in-phase and quadrature signals' amplitudes is also plotted in Figure 3.4 (b).

(a)

(b)

Figure 3.4 1st-order polyphase network frequency response.

(a) I Q gain. (b) I Q amplitude mismatch.

3.1.2 Second-Order RC Polyphase Network

Figure 3.5 2nd-order RC polyphase network.

(a) Schematic (b) Block diagram

Figure 3.5(a) shows the schematic for the second-order polyphase network. When the second stage loads the first stage without buffering, the resulting voltage at output node of the first stage drops due to the voltage divider formed by the output impedance Z_{out1}

of the first stage and the input impedance Z_{in2} of the second stage, where

$$Z_{out1} = R_1 // \frac{1}{j\omega C_1} \text{ and } Z_{in2} = \frac{1}{2} \left(R_2 + \frac{1}{j\omega C_2} \right).$$

Hence the voltage division ratio can be written as

$$\frac{Z_{in2}}{Z_{in2} + Z_{out1}} = \frac{(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)}{(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2) + 2j\omega R_1 C_2} \quad (3.12)$$

This division ratio is strongly frequency dependent. At very low or very high frequencies, the ratio approaches unity. When the frequency is near the vicinity of the

operating band, that is, $\omega \approx \frac{1}{R_1 C_1}$ or $\omega \approx \frac{1}{R_2 C_2}$, and if these two frequencies $\frac{1}{R_1 C_1}$ and

$\frac{1}{R_2 C_2}$ are not very far apart, this ratio is around $1/2$. Here in order to simplify the

derivation, it is assumed that the voltage division ratio is $1/2$ around the operation band.

In a practical design, multiple stages are cascaded in the manner of increasing resistance in order to reduce the loading effect and to broaden the bandwidth; therefore the actual division ratio is slightly larger than $1/2$.

It should be pointed out that the deviation of $1/2$ from the actual voltage division ratio will not affect I/Q matching in terms of amplitude and phase. Only the gain of every branch is slightly affected.

Therefore, from equations (3.1)-(3.8) and (3.12), the transfer functions of second-order polyphase network can be found to be:

$$\frac{I_{out2+}}{I_{in+}} = \frac{I_{out2-}}{I_{in-}} = \begin{cases} 1 & (\omega \rightarrow 0 \text{ or } \omega \rightarrow \infty) \\ \frac{1 + \omega^2 R_1 C_1 R_2 C_2}{2(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)} & (\omega \approx \frac{1}{R_1 C_1} \text{ or } \omega \approx \frac{1}{R_2 C_2}) \end{cases} \quad (3.13)$$

$$\frac{Q_{out2+}}{I_{in+}} = \frac{Q_{out2-}}{I_{in-}} = \begin{cases} 0 & (\omega \rightarrow 0 \text{ or } \omega \rightarrow \infty) \\ \frac{j\omega(R_1 C_1 + R_2 C_2)}{2(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)} & (\omega \approx \frac{1}{R_1 C_1} \text{ or } \omega \approx \frac{1}{R_2 C_2}) \end{cases} \quad (3.14)$$

Define $I_{out2} = \frac{1}{2}(I_{out2+} - I_{out2-})$ and $Q_{out2} = \frac{1}{2}(Q_{out2+} - Q_{out2-})$, then

$$\frac{I_{out2}}{I_{in}} = \begin{cases} 1 & (\omega \rightarrow 0 \text{ or } \omega \rightarrow \infty) \\ \frac{1 + \omega^2 R_1 C_1 R_2 C_2}{2(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)} & (\omega \approx \frac{1}{R_1 C_1} \text{ or } \omega \approx \frac{1}{R_2 C_2}) \end{cases} \quad (3.15)$$

$$\frac{Q_{out2}}{I_{in}} = \begin{cases} 0 & (\omega \rightarrow 0 \text{ or } \omega \rightarrow \infty) \\ \frac{j\omega(R_1 C_1 + R_2 C_2)}{2(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)} & (\omega \approx \frac{1}{R_1 C_1} \text{ or } \omega \approx \frac{1}{R_2 C_2}) \end{cases} \quad (3.16)$$

$$\frac{Q_{out2}}{I_{out2}} = j \frac{\omega(R_1 C_1 + R_2 C_2)}{1 + \omega^2 R_1 C_1 R_2 C_2} \quad (3.17)$$

From equation (3.17), it is clear that the Q signal always has a phase lead of 90° with

respect to the I signal regardless of the frequency. When $\omega = \frac{1}{R_1 C_1}$ or $\omega = \frac{1}{R_2 C_2}$,

$\left| \frac{Q_{out2}}{I_{out2}} \right| = 1$, i.e. the I/Q signals are matched in amplitude. In practical designs, knowing

the operating frequency band (e.g. from ω_1 to ω_2), then the $R_1 C_1$ and $R_2 C_2$ values can

be selected from $\frac{1}{R_1 C_1} = \omega_1$ and $\frac{1}{R_2 C_2} = \omega_2$.

For a second-order RC polyphase generator operating at 2.45GHz with a 300MHz bandwidth, Figure 3.6 shows the I/Q signals' amplitude responses, as well as I/Q

mismatch in terms of $\left| \frac{Q_{out2}}{I_{out2}} \right|$.

(a)

(b)

Figure 3.6 Second-order RC polyphase network frequency response.

(a) I/Q gain (b) zoomed-in view of (a) (c) I/Q amplitude mismatch

It is noticeable that within the band $\frac{1}{R_1 C_1} < \omega < \frac{1}{R_2 C_2}$, the I/Q amplitude mismatch is

very small, and there is a peak mismatch occurring inside the band. The peak can be

found by equating the derivative of $\left| \frac{Q_{out2}}{I_{out2}} \right|$ to zero:

$$\frac{\partial}{\partial \omega} \left| \frac{Q_{out2}}{I_{out2}} \right| = \frac{\partial}{\partial \omega} \frac{\omega(R_1 C_1 + R_2 C_2)}{1 + \omega^2 R_1 C_1 R_2 C_2} = 0$$

$$\Rightarrow \omega = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \quad (3.18)$$

By substituting equation (3.18) into equation (3.17), the maximum mismatch in the band can be found to be:

$$\left| \frac{Q_{out2}}{I_{out2}} \right|_{\max} = \frac{R_1 C_1 + R_2 C_2}{2\sqrt{R_1 C_1 R_2 C_2}} \quad (3.19)$$

This value is actually the ratio of the arithmetic mean to the geometric mean of $R_1 C_1$ and $R_2 C_2$, which is close to unity. This is verified by Figure 3.6 (c) that from 2.3GHz to 2.6GHz, the I/Q amplitude mismatch is less than 0.1dB. Thus it can be concluded that within the band $\frac{1}{R_1 C_1} < \omega < \frac{1}{R_2 C_2}$, the I/Q signals have a good matching.

3.1.3 Third-Order RC Polyphase Network

Figure 3.7 Third-order RC polyphase network

Figure 3.7 shows the schematic for the third-order polyphase network. The analysis of third-order polyphase network is similar to that of second-order polyphase network. By using the same approach, the transfer functions of a third order polyphase network can be found to be:

$$\frac{I_{out3}}{I_{in}} = \begin{cases} 1 & (\omega \rightarrow 0) \\ 0 & (\omega \rightarrow \infty) \\ \frac{1 + \omega^2 (R_1 C_1 R_2 C_2 + R_1 C_1 R_3 C_3 + R_2 C_2 R_3 C_3)}{4(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)(1 + j\omega R_3 C_3)} & (\omega \approx \frac{1}{R_1 C_1} \text{ or } \omega \approx \frac{1}{R_2 C_2} \text{ or } \omega \approx \frac{1}{R_3 C_3}) \end{cases} \quad (3.20)$$

$$\frac{Q_{out3}}{I_{in}} = \begin{cases} 0 & (\omega \rightarrow 0) \\ 1 & (\omega \rightarrow \infty) \\ \frac{j\omega(R_1 C_1 + R_2 C_2) + (1 + \omega^2 R_1 C_1 R_2 C_2)j\omega R_3 C_3}{4(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)(1 + j\omega R_3 C_3)} & (\omega \approx \frac{1}{R_1 C_1} \text{ or } \omega \approx \frac{1}{R_2 C_2} \text{ or } \omega \approx \frac{1}{R_3 C_3}) \end{cases} \quad (3.21)$$

$$\frac{Q_{out3}}{I_{out3}} = j \frac{\omega(R_1 C_1 + R_2 C_2) + \omega R_3 C_3 (1 + \omega^2 R_1 C_1 R_2 C_2)}{1 + \omega^2 (R_1 C_1 R_2 C_2 + R_1 C_1 R_3 C_3 + R_2 C_2 R_3 C_3)} \quad (3.22)$$

From equation (3.22), it is clear that the Q signal always has a 90° phase lead with respect to I signal regardless of the frequency. When $\omega = \frac{1}{R_1 C_1}$ or $\omega = \frac{1}{R_2 C_2}$

or $\omega = \frac{1}{R_3 C_3}$, $\left| \frac{Q_{out3}}{I_{out3}} \right| = 1$, which means the I/Q signals are matched in amplitude. Figure

3.8 shows the I/Q amplitude response, as well as the their mismatch in terms of $\left| \frac{Q_{out3}}{I_{out3}} \right|$.

It is still assumed that the frequency band is from 2.3GHz to 2.6GHz. It is noticed from Figure 3.8 (c) that from a mismatch less than 0.25dB is maintained through a 2GHz bandwidth. Therefore it can be concluded that a third-order polyphase generator can

provide good matching between in-phase and quadrature signals' amplitudes through a very wide band.

(a)

(b)

Figure 3.8 Third-order RC polyphase network frequency response.
 (a) I/Q gain (b) zoomed-in view of (a) (c) I/Q amplitude mismatch

3.1.4 Amplitude-matched RC polyphase network

The previous analysis reveals that if the first stage of the polyphase network is connected in the way as shown in Figure 3.3, i.e., with alternative inputs shorted to ground, then the phase difference between the I/Q outputs is always 90° for all frequencies; but the bandwidth for amplitude matching is limited depending on the number of stages used. The RC polyphase network can be connected in another way as shown in Figure 3.9, the following analysis will show that with this configuration, the polyphase network can achieve good amplitude matching for all frequencies, but scarifying the phase matching. In order to differentiate the two kinds of polyphase networks, we name the one shown in Figure 3.3 as “phase-matched polyphase

network”, and the one shown in Figure 3.9 is named as “amplitude-matched polyphase network”.

Figure 3.9 Schematic of amplitude-matched RC polyphase network

By substituting $Q_{in+}=I_{in+}$ and $Q_{in-}=I_{in-}$ into equations (3.1)-(3.4), the output expression for the 1st-order amplitude-matched polyphase network can be found as shown in equations(3.23)-(3.26). Here we use I'_{out1+} , I'_{out1-} , Q'_{out1+} and Q'_{out1-} to denote the four outputs of the 1st-order amplitude-matched polyphase network:

$$I'_{out1+} = \frac{1 - sR_1C_1}{1 + sR_1C_1} I_{in+} \quad (3.23)$$

$$Q'_{out1+} = \frac{1 + sR_1C_1}{1 + sR_1C_1} I_{in+} \quad (3.24)$$

$$I'_{out1-} = \frac{1 - sR_1C_1}{1 + sR_1C_1} I_{in-} \quad (3.25)$$

$$Q'_{out1-} = \frac{1 + sR_1C_1}{1 + sR_1C_1} I_{in-} \quad (3.26)$$

The expressions can be condensed to :

$$I'_{out1} = \frac{I'_{out1+} - I'_{out1-}}{2} = \frac{1 - sR_1C_1}{1 + sR_1C_1} I_{in} \quad (3.27)$$

$$Q'_{out1} = \frac{Q'_{out1+} - Q'_{out1-}}{2} = \frac{1 + sR_1C_1}{1 + sR_1C_1} I_{in} \quad (3.28)$$

$$\frac{Q'_{out1}}{I'_{out1}} = \frac{1 + sR_1C_1}{1 - sR_1C_1} = \frac{1 + j\omega R_1C_1}{1 - j\omega R_1C_1} \quad (3.29)$$

From the above equations, it can be seen that I_{out1} and Q_{out1} have the same amplitude of $|I_{in}|$ for all frequencies, but the phase difference is 90° at a single frequency $\omega = \frac{1}{R_1C_1}$.

From equation (3.29), the relationship between the I/Q phase error and frequency is illustrated in Figure 3.10.

Figure 3.10 Phase error for 1st-order amplitude-matched RC polyphase network

Using the same approach discussed in Section 3.1.2 and 3.1.3, we can derive the transfer functions for the 2nd- and 3rd- order amplitude-matched polyphase networks.

Here we use I'_{out2} , Q'_{out2} to denote the outputs of the 2nd-order amplitude-matched polyphase network, and I'_{out3} , Q'_{out3} to denote the outputs of the 3rd-order amplitude-matched polyphase network.

$$\frac{I'_{out2+}}{I_{in+}} = \frac{I'_{out2-}}{I_{in-}} = \begin{cases} 1 & (\omega \rightarrow 0 \text{ or } \omega \rightarrow \infty) \\ \frac{(1 + \omega^2 R_1 C_1 R_2 C_2) - j\omega(R_1 C_1 + R_2 C_2)}{2[(1 - \omega^2 R_1 C_1 R_2 C_2) + j\omega(R_1 C_1 + R_2 C_2)]} & \left(\omega \approx \frac{1}{R_1 C_1} \text{ or } \frac{1}{R_2 C_2} \right) \end{cases} \quad (3.30)$$

$$\frac{Q'_{out2+}}{I_{in+}} = \frac{Q'_{out2-}}{I_{in-}} = \begin{cases} 0 & (\omega \rightarrow 0 \text{ or } \omega \rightarrow \infty) \\ \frac{(1 + \omega^2 R_1 C_1 R_2 C_2) + j\omega(R_1 C_1 + R_2 C_2)}{2[(1 - \omega^2 R_1 C_1 R_2 C_2) + j\omega(R_1 C_1 + R_2 C_2)]} & \left(\omega \approx \frac{1}{R_1 C_1} \text{ or } \frac{1}{R_2 C_2} \right) \end{cases} \quad (3.31)$$

$$\frac{Q'_{out2}}{I'_{out2}} = \frac{(1 + \omega^2 R_1 C_1 R_2 C_2) + j\omega(R_1 C_1 + R_2 C_2)}{(1 + \omega^2 R_1 C_1 R_2 C_2) - j\omega(R_1 C_1 + R_2 C_2)} \quad (3.32)$$

3rd order:

$$\frac{I'_{out3}}{I_{in}} = \begin{cases} 1 & (\omega \rightarrow 0) \\ 0 & (\omega \rightarrow \infty) \\ \frac{1 + \omega^2(R_1 C_1 R_2 C_2 + R_1 C_1 R_3 C_3 + R_2 C_2 R_3 C_3) - j[\omega(R_1 C_1 + R_2 C_2 + R_3 C_3) + \omega^3 R_1 C_1 R_2 C_2 R_3 C_3]}{4(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)(1 + j\omega R_3 C_3)} & \left(\omega \approx \frac{1}{R_1 C_1} \text{ or } \frac{1}{R_2 C_2} \text{ or } \frac{1}{R_3 C_3} \right) \end{cases} \quad (3.33)$$

$$\frac{Q'_{out3}}{I_{in}} = \begin{cases} 1 & (\omega \rightarrow 0) \\ 0 & (\omega \rightarrow \infty) \\ \frac{1 + \omega^2(R_1C_1R_2C_2 + R_1C_1R_3C_3 + R_2C_2R_3C_3) + j[\omega(R_1C_1 + R_2C_2 + R_3C_3) + \omega^3R_1C_1R_2C_2R_3C_3]}{4(1 + j\omega R_1C_1)(1 + j\omega R_2C_2)(1 + j\omega R_3C_3)} & \left(\omega \approx \frac{1}{R_1C_1} \text{ or } \frac{1}{R_2C_2} \text{ or } \frac{1}{R_3C_3} \right) \end{cases} \quad (3.34)$$

$$\frac{Q'_{out3}}{I'_{out3}} = \frac{1 + \omega^2(R_1C_1R_2C_2 + R_1C_1R_3C_3 + R_2C_2R_3C_3) + j[\omega(R_1C_1 + R_2C_2 + R_3C_3) + \omega^3R_1C_1R_2C_2R_3C_3]}{1 + \omega^2(R_1C_1R_2C_2 + R_1C_1R_3C_3 + R_2C_2R_3C_3) - j[\omega(R_1C_1 + R_2C_2 + R_3C_3) + \omega^3R_1C_1R_2C_2R_3C_3]} \quad (3.35)$$

The following two graphs show the I/Q phase error with respect to frequency for 2nd- and 3rd- order amplitude-matched polyphase network respectively. The amplitude-matched polyphase network can provide constant output amplitude over frequencies and the I/Q amplitude are always matched.

Figure 3.11 Phase error for 2nd-order amplitude-matched RC polyphase network

Figure 3.12 Phase error for 3rd-order amplitude-matched RC polyphase network

3.1.5 Conclusion on RC Polyphase Networks

From the above analysis, it can be seen that depending on the circuit configuration, the RC polyphase networks can produce either phase-matched signal or amplitude-matched signals for all frequencies ideally regardless of its order. For the phase-matched RC polyphase network, the phase difference between I/Q signals is always 90° for all frequencies. Its amplitude matching behavior depends on the number of stages used. As the number of cascade stages increases, the bandwidth for the amplitude matching becomes wider and wider, but at the expense of a higher attenuation. On the other hand, the amplitude-matched RC polyphase network behaves in another way round. The I/Q signals' amplitude is well-matched for all frequencies regardless of its order. The I/Q phase can be matched for a certain frequency range, and the bandwidth will increase with the number of cascade stages.

Depending on different applications, one can choose either phase-matched RC polyphase network or amplitude-matched RC polyphase network. In most of the modern designs, the accurate I/Q phase of 90° is more desired, as it directly relates to the image-rejection performance for the direct conversion/low-IF transceiver architecture. Thus in the following section, the design of quadrature generator using the phase-matched RC polyphase network will be discussed. As analyzed in the previous sections, for the phase-matched RC polyphase network, there is a tradeoff between bandwidth and signal gain. From the transfer functions derived and plotted, it is clear that each stage will introduce 3dB loss to the signal. A two-stage RC polyphase network can provide the necessary bandwidth by choosing R_1C_1 and R_2C_2 properly, and its loss is 6dB, which is acceptable. A quadrature generator using a second-order RC polyphase network has been designed and tested, as it is described in the next section.

3.2 Design of Quadrature Signal Generator for the 2.4GHz ISM band

Figure 3.13 Block diagram of RF front-end

Figure 3.13 shows the typical configuration of the modern RF transceiver front-end for zero- or low-IF conversion. The quadrature Local Oscillator (LO) is used to provide the signals for the up- and down-conversion. It consists of a Voltage-Controlled-Oscillator (VCO), a two-stage RC polyphase network and output buffers as shown in Figure 3.14.

3.2.1 Design of VCO

This section will investigate the VCO design. First, both the amplitude-frequency and the phase-frequency characteristics of an LC tank will be described in order to understand its frequency selection behavior and the oscillating process. Subsequently,

the design and analysis of the LC VCO will be presented. Finally, the simulation and measurement results of this VCO will be shown.

Figure 3.14 Block diagram of the quadrature generator

3.2.1.1 Characteristics of an LC Tank

Figure 3.15 (a) Series LC resonator (b) Parallel LC resonator

An inductor in series or parallel with a capacitor forms a series or parallel resonator respectively as shown in Figure 3.15. With the parasitic series resistance shown as R in the figure, the effective impedances of the series and parallel resonators are:

$$|Z_s| = \left| R + j \left(\omega L - \frac{1}{\omega C} \right) \right| = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C} \right)^2} \quad (3.36)$$

$$|Z_p| = 1 / \left(\frac{CR}{L} + j \left(\omega L - \frac{1}{\omega C} \right) \right) = 1 / \sqrt{\left(\frac{CR}{L} \right)^2 + \left(\omega C - \frac{1}{\omega L} \right)^2} \quad (3.37)$$

Figure 3.16 The resonant characteristic of

(a) series LC resonator (b) parallel LC resonator

It is shown in the above equations that the impedance of the series resonator has its minimum value R at a specific frequency $\omega_s = \frac{1}{\sqrt{LC}}$. For the parallel resonators, the

impedance reaches its maximum value $R_p = \frac{L}{RC}$ at the resonant

frequency $\omega_p = \frac{1}{\sqrt{LC}}$. The resonant characteristics are illustrated in Figure 3.16. It is

also noticeable from Figure 3.16 that the sharper the magnitude-frequency characteristic is, the more precise the frequency selection is, which is expressed in

terms of the quality factor Q . For series and parallel cases, their quality factors are expressed as equations (3.38) and (3.39) respectively.

$$Q_s = \frac{\omega_s L}{R} = \frac{1}{\omega_s CR} = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (3.38)$$

$$Q_p = \frac{R_p}{\omega_p L} = \frac{L}{CR\omega_p L} = \frac{1}{CR\omega_p} = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (3.39)$$

3.2.1.2 LC Differential VCO Design

In this section, the design of an LC CMOS cross-coupled VCO tuned by varactors will be presented. The designed VCO is operating with 1.8V supply voltage and working at 2.4GHz ISM band, and it have been fabricated using Global Foundry 0.18 μ m CMOS process.

A. Description of the Circuit

Figure 3.17 Schematic of VCO

Figure 3.17 shows a LC VCO with Fixed Biasing (FB) topology. The VCO has a cross-coupled structure made up of a pair of N type MOSFETs, forming a positive feedback loop with LC resonators in the loop to select the operating frequency. The control voltage is utilized to tune the varactor's capacitance value and hence the operating frequency of the VCO. The biasing portion of the VCO consists of a current mirror, and the bias condition of the VCO is determined by the sizes of $NM3$, $NM4$ and R . To circumvent the asymmetry problem introduced by a single inductor, the inductor used in the VCO is split into two identical ones, and one is the mirror image of the other; thus the two output nodes are made symmetrical.

The small-signal voltage gain of the amplifier $NM1$ - $NM2$ is calculated by $A_v = g_m Z_p$. From this equation, we can deduce that the Barkhausen's Criteria is probably satisfied only at the resonant frequency, because the magnitude of the gain is maximized and its phase is equal to zero when the LC tank is resonating. Therefore, if the transconductance of the amplifying transistor is designed to be large enough to ensure its gain is larger than or equal to unity at the resonant frequency, the oscillation will be maintained. With the noise at any other frequency suppressed, the noise component at the resonant frequency is amplified, passed into the positive feedback loop and further amplified till the transistor enters the saturation region so that the oscillation amplitude is maintained.

Since $A_v = g_m Z_p$, at resonant frequency ω_o , the gain is:

$$|A_v| = g_m |Z_p| \propto \sqrt{\frac{W}{L}} \cdot I_{ds} \cdot Q \omega_o L \quad (3.40)$$

It needs to be pointed out that the Q in the above equation is the loaded Q , which takes into account all the parasitic effects at the oscillation node.

In the design of an LC VCO, considerations should be given for such parameters as the aspect ratio of the amplifying transistor, the biasing drain-source current of the amplifying transistor, and the Q and the inductance value (or the capacitance value) of the LC tank. Table 3-1 is a summary of the dimensions of the devices shown in Figure 3.17, and we will discuss these aspects in details in the following sections.

Table 3-1 Dimension and values of components in VCO

L	3.23nH
$NM1-NM2$	30 μ m/0.18 μ m
$PM1-PM2$	60 μ m/0.18 μ m
<i>Varactor</i>	Tunable from 0.5pF
$NM3$	128 μ m/0.35 μ m
$NM4$	32 μ m/0.35 μ m
R	6.9KOhm

B. Design of LC Tank

For the LC tank, the inductance and capacitance should be selected according to the intended operating frequency of the VCO and the availability of fabrication. As stated

above, the resonant impedance is determined by the value of R_p ($R_p = Q\omega_p L$), which indicates that increasing either Q or L of the inductor will result in increased resonant impedance R_p .

It is important to note that as Q or L increases, besides the improved phase noise according to the Leeson's equation discussed in Chapter 2, the needed gain of the amplifier decreases, resulting in decreased power dissipation. In other words, larger oscillation amplitude is obtained with the same gain. However, the on-chip inductors cannot have as high Q values as off-chip inductors, mainly due to their parasitic series resistance and the substrate loss. The implementation of a large inductor is also restricted by the chip area and the consideration for its Q value. Therefore, for the intended operating frequency, the inductance of the LC tank is chosen as 3.23nH in this VCO design; and the loaded Q value is simulated and plotted as shown in Figure 3.18:

Figure 3.18 Quality factor of 3.23nH inductor

In the above graph, x-axis denotes the frequency in Hz, and y-axis is the quality factor of inductor with inductance of 3.23nH. It is clear that the loaded Q is about 8 around 2.4GHz.

In Figure 3.17 the LC tank in the VCO incorporates a PN varactor. The output frequency of the VCO is determined by:

$$f_{out} = f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (3.41)$$

In the above equation, C refers to the capacitance of the varactors and parasitic capacitance, and it can be calculated from the known resonant frequency and the inductance value.

There are two types of commonly used varactors: PN varactor and MOS varactor. The PN varactor is made of a reversely biased PN junction. When a PN junction is under reverse bias, the depletion layer widens and its capacitance changes according to

$$C_d = \frac{\epsilon_s}{W_d}, \text{ where } \epsilon_s \text{ is the dielectric constant, and } W_d \text{ is the width of the depletion}$$

region, which is increases with the reverse bias voltage. Figure 3.19 shows the energy band diagrams of a PN junction in the equilibrium state and with reverse bias, where E_V , E_F and E_C represent the valence band energy level, the Fermi level and the conduction band energy level respectively.

Figure 3.19 Energy band diagram for PN junction (a) in equilibrium (b) with reverse bias

For a MOS device with source, drain and bulk connected together, it can be treated as a two-terminal device and it behaves like a capacitor [2]. The negative potential on the gate attracts the holes in the substrate to the oxide interface, and the MOSFET operates in the “accumulation” region. The two-terminal device can be viewed as a capacitor having a unit-area capacitance of C_{ox} , which is the gate oxide capacitance per unit area.

As V_{GS} rises, the density of holes at the interface falls, a depletion region begins to form under the oxide, and the device enters weak inversion. In this mode, the capacitance consists of the series combination of C_{ox} and C_{dep} . Finally, as V_{GS} exceeds V_{TH} , the oxide-silicon interface sustains a channel and the unit-area capacitance returns to C_{ox} . Fig. 3.20 plots the behavior, and the energy band diagrams are illustrated in Figure 3.21.

Figure 3.20 Capacitance-voltage characteristic of an NMOS device

Figure 3.21 Energy band diagrams of MOS varactor in

(a) accumulation region (b) strong inversion region

In general, the tuning characteristic of the diode varactor has a gradual change in slope; while for the MOS varactor, the C-V curve is the steepest in the linear region. Thus, a small change in the control voltage will cause a large deviation of the capacitance, hence the oscillation frequency. Noise introduced into the control voltage will result in a large phase noise due to the large K_{vco} **Error! Reference source not found..** Therefore PN varactor is used in this design.

The Capacitance-Voltage (C-V) curve of a 0.5pF PN varactor is shown below in Figure 3.22:

Figure 3.22 The C-V curve of the PN varactor

The x-axis is the reverse-bias voltage, and y-axis denotes the variable capacitance of the varactor. As shown in the graph, when the reverse-bias voltage changes from -0.5V to 1.3V, the capacitance of the varactor decreases from around 0.98pF to 0.60pF. When the reverse-bias voltage further increases, the capacitance will keep on

decreasing, resulting in an increasing frequency. However, the reverse-bias voltage cannot be increased infinitely, and it is limited by the real circuit implementation. As the P-junction of the varactor is connected to the VCO output node, the N-junction is biased by the control voltage V_{ctrl} . When the VCO is working, its output node remains at a DC level around 1V. As the control voltage cannot go beyond the supply voltage V_{dd} , which is 1.8V in practice, so the maximum reverse-bias voltage of the varactor is $1.8-1=0.8V$. Therefore, the resulted capacitance can be only changed from 0.62pF to 0.98pF, which limits the frequency tuning range. However, as this design is target for the 2.4GHz ZigBee standard, which specifies the frequency range as from 2.42GHz to 2.48GHz. Therefore, as long as the VCO can cover the required frequency range, the design is acceptable.

C. Amplifier Design

The cross-coupled amplifier is designed to provide enough gain to start and maintain the steady oscillation based on the Barkhausen's Criteria. According to equation (3.40), the biasing current I_{ds} and the size of transistors W/L are the variables that we can control. But it also indicates that there is a trade-off between the power consumption and the frequency range. If very low power consumption is needed, the biasing current I_{ds} must be kept low. In order to keep the transconductance constant and hence the gain constant in equation (3.40), larger W/L for NM_1 - NM_2 will be required, which increases the fixed parasitic capacitance to the LC tank. Since the parasitic capacitance cannot be controlled, the overall variable capacitance will be limited and the tuning range of the VCO will be restricted. Furthermore, as the fixed capacitance exceeds a certain value,

in order to maintain the frequency, the inductance need to be decreased, resulting in decrease in the gain. Therefore, for the 0.18 μm CMOS process, the size of the NMOS pair is optimized to 30 $\mu\text{m}/0.18\mu\text{m}$ to provide a good compromise between both the frequency range and the power consumption. To ensure a symmetric rise and fall time of sinusoidal wave, the cross-coupled PMOS has to be about twice the size of cross-coupled NMOS. Therefore, the PMOS size is optimized to 60 $\mu\text{m}/0.18\mu\text{m}$.

D. Biasing Circuit Design

Figure 3.23 Schematic of current mirror

The biasing circuit is a current mirror consists of two NMOS transistors $NM3$ and $NM4$ and one resistor R as shown in Figure 3.23. The current mirror provides bias current for the VCO to operate in the optimum condition. It should be noted that if the drain voltages of $NM3$ and $NM4$ are different, the channel length modulation effect will degrade the accuracy of current copying. To solve this problem, the cascode structure as shown in Figure 3.24 (a) can be used, where the cascode transistors ensure that $V_X = V_Y = V_N - V_{GS5}$, thus eliminating the channel length modulation effect. However, the cascode structure consumes extra voltage headroom, and the voltage at the output of the current mirror equals to $V_Y + V_{DS6} = V_{GS4} + V_{DS6}$. The low-voltage cascode structure

shown in Figure 3.24(b) helps to relax the voltage headroom, while still maintaining $V_X = V_Y = V_N - V_{GS5}$. For the low-voltage cascode structure, if we apply a voltage of $V_{DS4} + V_{GS5}$ at node V_N , the voltage at the output node equals to $V_{DS3} + V_{DS6}$ which is smaller than that of the circuit shown in Figure 3.24(a). As the low-voltage cascode structure requires one more accurate biasing voltage at node V_N , the design is less preferred. Moreover, in the VCO design, the requirement on accurate current coping is not stringent. Instead, the voltage headroom is crucial as it may limit the output signal swing, which is related to phase noise performance. Therefore, the simple current mirror shown in Figure 3.23 has been adopted in the design.

Figure 3.24 (a) cascode current mirror (b) low-voltage cascode current mirror

The $1/f$ flicker noise from the tail current is one of the contributors to the overall VCO phase noise. The flicker noise in MOSFET can be expressed by $K/(C_{ox} \cdot W L f)$, where K is the process-dependent constant, C_{ox} is the oxide capacitance, W and L are channel width and length respectively and f is the frequency. Therefore, using relatively large W and L for $NM3$ can help to reduce the VCO phase noise. Furthermore, the output

resistance of the current source is $R_{o3} = \frac{1/\lambda + V_{DS3}}{I_{D3}}$, where λ is the channel length modulation parameter and V_{DS3} is the drain-source voltage of NM3 and I_{D3} is the current in NM3. The channel length modulation parameter λ is inversely proportional to the channel length L_3 . Therefore, L_3 needs to be large to get a large output resistance. However, L_3 and W_3 cannot be too large due to the area constraint. Simulations have been done to find proper aspect ratio W_3/L_3 to be $128\mu\text{m}/0.35\mu\text{m}$, which gives good phase noise performance with reasonably large size. The current transfer ratio is designed to be 4, thus the NM4 size is $32\mu\text{m}/0.35\mu\text{m}$. The resistor is selected to be $6.9\text{K}\Omega$ to give a proper reference current, such that the output current is 0.7mA and the VCO is working properly under this bias current.

3.2.2 RC Polyphase Network Design

Figure 3.25 Schematic of 2nd-order RC polyphase network

The schematic of the 2nd-order RC polyphase network is shown in Figure 3.25. Since the RC polyphase network has a low input impedance at radio-frequency, a source follower is usually used as an input buffer to drive the RC polyphase networks. In order

to save power consumption and area, and to avoid signal distortion introduced by the source follower, the VCO is connected to the RC polyphase network directly. By doing so, the fixed capacitance at the VCO oscillating node is increased, which leads to a smaller tuning range from 2.32GHz to 2.65GHz according to the simulation. This, however, is still more than sufficient to cover the ISM band for ZigBee standard. Therefore the direct connection of the VCO and the polyphase network is acceptable. As the RC polyphase network loads VCO directly, the signal will drop due to the loading effect. In order to minimize this effect, the input impedance of the polyphase network needs to be maximized. As the input impedance is proportional to the resistance R and the reciprocal of the capacitance C , the capacitance needs to be minimized, and the resistance needs to be maximized. The smallest capacitor available from the Foundry is 109.5fF. However, the use of minimum size capacitor is usually avoided, because the percentage of component variation will be very large after fabrication. Therefore, as a compromise, the capacitance is chosen to 150fF. As discussed before, in order to provide well-matched I/Q signals over a wideband without much attenuation, the 2nd-order RC polyphase network is used in this design, and the two poles are selected at 2.3GHz and 2.6GHz. With the known capacitance, the resistors R_1 and R_2 can be then calculated from $2\pi f_1 = \frac{1}{R_1 C_1}$ and $2\pi f_2 = \frac{1}{R_2 C_2}$, where $f_1=2.6\text{GHz}$, $f_2=2.3\text{GHz}$, and $C_1=C_2=150\text{fF}$.

In a summary, the dimensions of the components used in the polyphase network are listed below in Table 3-2.

Table 3-2 Dimensions of components in polyphase network

$R1$	393 Ohm
$R2$	442 Ohm
$C1$	150 fF
$C2$	150 fF

3.2.3 Output Buffer Design

To compensate the 6dB loss introduced by the second-order polyphase network, output buffer shown in Figure 3.26 is employed to amplify the signal. A simple common source differential amplifier is used as the output buffer to provide the necessary output swing which is required by the mixer. The open drain transistors are connected as the dummy input transistors of the mixer, which load the buffer.

Figure 3.26 Output buffer

At radio-frequency, the gate-source capacitance of the mixer input transistor loads the buffer heavily. Therefore, the tail current has to be large enough to provide sufficient gain. In order to lower the power consumption, replacing the resistive load by an inductive load as shown in Figure 3.27 is an alternative solution. The inductor and the gate-source capacitor of the load transistor form a parallel resonator. By selecting a proper size of inductor, the resonator will resonate at the desired frequency, i.e. 2.4GHz in this case. As discussed before, at the resonant frequency, the impedance of the parallel LC tank is equal to R_p which is large. Hence bias current can be reduced. The designed value of the bias current is 1.6mA which is enough to provide 200mV output amplitude. The size of the input transistors of the buffer are carefully selected such that it does not load the RC polyphase network heavily and at the same time it can provide sufficient gain too. In summary, the dimensions of the components used in output buffer are listed below in Table 3-3.

Figure 3.27 Output buffer with inductive load

Table 3-3 Dimensions of components in the output buffer

<i>NM5-NM6</i>	30 μ m /0.18 μ m
<i>L</i>	7.81 nH
<i>NM7</i>	120 μ m/0.35 μ m
<i>NM8</i>	20 μ m/0.35 μ m
<i>Rref</i>	4.9KOhm

3.2.4 Layout Issue

Process variations during fabrication may limit accuracy and desired performance of analog circuits. Matching between components in layout of analog circuits is an important issue in many designs, such as current mirrors, differential pairs and so on. In this design the matching of the components in the RC polyphase network is crucial. Inter-digitization and common centroid are the most basic techniques to match components in layouts [62]. The inter-digitization technique is to place components alternately, and the common centroid technique is to place the components that both components have the same centroid. Figure 3.28(a) and (b) illustrate the concepts of inter-digitization and common centroid layout technique respectively.

Figure 3.28 (a) Inter-digitization layout technique (b) Common centroid layout technique

As discussed in the previous section, the resistances needed in this design are 393 Ohm and 442 Ohm. N-poly type resistor is chosen with the consideration of area and process variation. When the resistor's size reduces, the effect of process imperfection becomes

more severe. Therefore it is desirable to use relatively large size resistors. In this design, four 1572 Ohm resistors are connected in parallel to implement the 393 Ohm resistor, and four 1768 Ohm resistors are connected in parallel to implement the 442 Ohm resistor. This implementation has another advantage. As the number of resistors increases, it is easier to match the devices better. The inter-digitization method is used in this design, and the following figure illustrates the layout of the resistors of the 1st stage of the RC polyphase network. Each resistor is 1572 Ohm.

Figure 3.29 Layout of resistors in the 1st stage of RC polyphase network

The resistors for the 2nd stage are layout using the same method as the 1st stage. The capacitors are symmetrically distributed around the resistors, and the common centroid technique is implemented for capacitors.

The complete layout for the 2nd-order RC polyphase network is shown in Figure 3.30 below. It occupies $0.05 \times 0.05 = 0.0025 \text{ mm}^2$ silicon area.

Figure 3.30 Layout of 2nd-order RC polyphase network

3.3 Simulation and Measurement Results

A: (2.29401G -6.11505) delta: (299.216M -26.5692m)
 B: (2.59323G -6.14162) slope: -88.796p
 (a)

(b)

Figure 3.31 Simulated frequency response of 2nd-order RC polyphase network.

(a) Amplitude response. (b) Phase response.

Figure 3.31 shows the post-layout simulation result of the frequency response for the designed 2nd-order RC polyphase network. To illustrate the robustness of the RC polyphase network, all the resistance and capacitance in the network are purposely adjusted to be 15% higher than the calculated values. The new outputs responses with 15% components variation are shown in Figure 3.32. It is evident from Figure 3.32 that even with 15% components variations, the worst case I/Q amplitude mismatch within the frequency band is still less than 0.5dB and the phase error is much less than 0.5° .

(a)

(b)

Figure 3.32 Simulated frequency response of 2nd-order RC polyphase network with 15% components variation.

(a) Amplitude response. (b) Phase response.

Figure 3.33 shows the bench setup for measuring the quadrature generator.

Figure 3.33 Bench setup

It should be pointed out that based the output expressions derived in Section 3.1, it is possible that the variation from device to device will affect the I/Q matching. Let's take equation (3.17) for example:

$$\frac{Q_{out2}}{I_{out2}} = j \frac{\omega(R_1 C_1 + R_2 C_2)}{1 + \omega^2 R_1 C_1 R_2 C_2} \quad (3.17)$$

This equation has been derived with the assumption that all the resistance and capacitance in the 1st stage have the same values of R_1 and C_1 , and all the resistance and capacitance in the 2nd stage have the same values of R_2 and C_2 . If this assumption is not valid, equation (3.17) needs to be re-written in a much complicated form, and the I/Q phase difference of 90° cannot be assured. Therefore, careful measures need to be carried out during the circuit layout to minimize the device mismatch. As discussed in the previous section, techniques such as inter-digitization and common-centroid have been incorporated in this design to optimize the devices' matching behavior, therefore the variation from device to device is minimum and negligible.

The die photograph the quadrature generator is shown in Figure 3.34; its area is 1.25mm² including pads.

Figure 3.34 Die photograph of the quadrature generator

Figure 3.35 Frequency tuning of the quadrature generator

Figure 3.35 shows the frequency tuning ranges obtained from post-layout simulation and measurement. When the control voltage changes from 0.6V to 1.8V, the frequency can be tuned from 2.32GHz to 2.65GHz in the post-layout simulation, while the measured frequency varies from 2.18GHz to 2.48GHz. Due to the component variation and parasitic effect during fabrication, the measured output frequency is lower than the post-layout simulation result by around 200MHz. This problem can be solved by reducing the fixed-capacitance at the oscillation node of VCO.

Figure 3.36 Measured output waveform of the quadrature generator

Figure 3.36 shows the final output I/Q waveforms of the quadrature generator measured by the digital oscilloscope Lecory 8600A. There is advance DSP function built in the measurement equipment, and the phase difference measured between I/Q

signals can be measured directly, which is 89.99° as shown in Figure 3.36. The output amplitudes for the I/Q signals are 235.1mV and 250.3mV respectively, and the mismatch in amplitude is 0.29dB which may be caused by process variation in R and C of the RC polyphase network. The phase noise at 1MHz offset from 2.48GHz carrier is -125.1 dBc/Hz as shown in Figure 3.37. The VCO and the output buffers consume 3.9mA current in total.

Figure 3.37 Measured phase noise of the quadrature generator

A widely used figure-of-merit (FOM) for the VCO is defined as [63]:

$$FOM = L\{f_{offset}\} - 20 \log\left(\frac{f_o}{f_{offset}}\right) + 10 \log\left(\frac{P_{DC}}{1mW}\right) \quad (3.42)$$

Where f_{offset} is the offset frequency where the phase noise is measured, f_o is the carrier frequency and P_{DC} is the DC power consumption of the VCO. Therefore, the phase noise FOM of the designed quadrature generator can be calculated to be -184.5dB.

Table 3-4 summarizes the performance of the quadrature generator using RC polyphase network, and also compares it with other published RC polyphase networks.

Table 3-4 Performance comparison of the RC polyphase networks

	This Work	[64]	[65]
Technology	0.18 μ m CMOS	0.13 μ m CMOS	0.13 μ m CMOS
Number of Stages	2-stage	1-stage	2-stage
Output frequency(GHz)	2.18-2.48	4.6-6.4	2.4
Phase Noise @1MHz offset	-125.1dBc/Hz	--	--
Phase Noise FOM (dB)	-184.53	--	--
I/Q Phase error	<0.1°	<0.5°	-39dB ¹
I/Q amplitude mismatch (dB)	0.5dB	0.26dB	--
Output level	-2dBm	--	-9dBm
Total power consumption (mW)	7.02	0.25 ²	--

¹ -39dB is equivalent to 1.29° phase error according to equation (2.10)

² This power consumption is for auxiliary circuits only

3.4 Summary

In this chapter, the transfer functions of the 1st-, 2nd- and 3rd-order RC polyphase networks operating as quadrature generators have been re-derived based on very basic principles. The new approach removes the need for complex phasor and matrix analysis; and it is simple and comprehensive. The output signals' matching behavior is also described in details in the chapter. Besides the phase-matched RC polyphase network, the amplitude-matched RC polyphase network is also investigated. A quadrature generator consisting of a VCO, a 2nd-order phase-matched RC polyphase network and output buffers has been designed and fabricated. In the presence of 15% component variation, it still achieved less than 0.5dB mismatch in amplitude and much less than 0.5° phase error. The quadrature generator has been fabricated using Chartered 0.18 μ m process. It had a frequency tuning range from 2.18GHz to 2.48GHz and provided well matched I/Q with 89.99° phase difference. The phase noise at 1MHz offset from 2.48GHz carrier is -125.1 dBc/Hz with totally 3.9mA current consumed.

CHAPTER 4

Analysis and Design of Quadrature Generator Using QVCO Approach

The theory and practice of monolithic quadrature voltage-controlled-oscillator (QVCO) design has made significant progresses. The QVCO shown in Figure 4.1 is based on the cross-coupling of two differential LC-tank VCOs, with the coupling transistors placed in parallel with the switch transistors. It was known to have a trade-off between phase noise and I/Q mismatch. This QVCO design is referred to as the Parallel QVCO.

Figure 4. 1 Parallel QVCO

Two modifications of the Parallel QVCO have appeared in the literature. In the first case, phase shifters have been introduced between cascaded LC-resonators [66], allowing each resonator to be optimally driven at zero-degree phase shift [67]. The

second approach is cross-coupling the two differential VCOs in the QVCO by placing the coupling transistors in series with the switching transistors as shown in Figure 4.2 [68] rather than in parallel. This choice is motivated by the fact that the coupling transistors in the Parallel QVCO are responsible for a large contribution to the phase noise, and connecting the coupling transistors in series with the switching transistors, in a cascode-like fashion, should greatly reduce the noise from the cascode device. Since in this case the coupling transistors are placed in series with switching transistors, we will refer to this design as the Series QVCO.

Figure 4. 2 Series QVCO

4.1 Analysis of Parallel QVCO

In the Parallel QVCO topology shown in Figure 4.1, $M1$ - $M2$ and $M5$ - $M6$ are identical switching transistors with the same transconductance g_m ; and $M3$ - $M4$ and $M7$ - $M8$ form the coupling circuit and determine M , the coupling coefficients between the oscillator cores.

If the signal voltages at nodes A , B , C , D are denoted as V_A , V_B , V_C , and V_D , the drain-source current of M_1 and M_3 are $I_{ds1} = V_B g_{m1}$ and $I_{ds3} = V_D g_{m3}$, respectively. The total current flowing through the LC tank at node A is:

$$I_{\text{tank}} = I_{ds1} + I_{ds3} = V_B g_{m1} + V_D g_{m3} \quad (4.1)$$

Since the voltage at node A is:

$$V_A = V_{dd} - I_{\text{tank}} Z(j\omega) \quad (4.2)$$

substituting equation (4.1) in equation (4.2) results that:

$$V_A = V_{dd} - (V_B g_{m1} + V_D g_{m3}) Z(j\omega) \quad (4.3)$$

Suppose only AC signal is considered, then $v_a = -(v_b g_{m1} + v_d g_{m3}) Z(j\omega)$. Moreover,

because $v_b = -v_a$, v_a can be expressed as:

$$v_a = (v_a g_{m1} - v_d g_{m3}) Z(j\omega) = (v_a - g_{m3} / g_{m1} \cdot v_d) g_{m1} Z(j\omega) \quad (4.4)$$

$$\text{i.e. } v_a = (v_a - M_1 v_d) G_1(j\omega) \quad (4.5)$$

where $M_1 = g_{m3} / g_{m1}$, and $G_1(j\omega) = g_{m1} Z(j\omega)$.

Using the same procedures, it can be obtained that:

$$v_d = (v_d gm_6 - v_b gm_8)Z(j\omega) = (v_d - gm_8 / gm_6 \cdot v_b)gm_6 Z(j\omega).$$

From $v_b = -v_a$, we get $v_d = (v_d + gm_8 / gm_6 \cdot v_a)gm_6 Z(j\omega)$.

It can be rewritten as

$$v_d = (v_d + M_2 v_a)G_2(j\omega) \quad (4.6)$$

where $M_2 = gm_8 / gm_6$ and $G_2(j\omega) = gm_6 Z(j\omega)$. This means if these two oscillators synchronize to a single oscillation frequency ω , the output at nodes A and D must satisfy these equations:

$$v_a = (v_a - M_1 v_d)G_1(j\omega) \quad (4.7)$$

$$v_d = (v_d + M_2 v_a)G_2(j\omega) \quad (4.8)$$

If the circuit is symmetrical, oscillators G_1 and G_2 are identical, $G_1(j\omega) = G_2(j\omega) = G(j\omega)$ and $M_1 = -M_2 = M$, it can be obtained from equation (4.7) and (4.8) that $v_a^2 + v_d^2 = 0$ hence $v_a = \pm jv_d$. Nodes B and C can be proven to satisfy $v_b = \pm jv_c$ through the same procedures. Thus the oscillator provides quadrature outputs at A , B , C , and D . The new oscillation frequency ω can be found by substituting $v_a = \pm jv_d$ into equation (4.7) or (4.8):

$$(1 \pm jM)G(j\omega) = 1 \quad (4.9)$$

where $G(j\omega) = gmZ(j\omega)$ is the amplifier gain, which is proportional to the tank

impedance $Z(j\omega)$. For a resonator with a lossy inductor, the magnitude of its impedance peaks at a frequency higher than the resonant frequency:

$$\omega_0 = \frac{1}{2\pi\sqrt{LC}} \sqrt{1 - \frac{CR_s^2}{L}} \quad (4.10)$$

where R_s is the series resistance in the lossy inductor.

From equation (4.9), there are two possible frequencies which can satisfy the oscillation condition:

$$\phi(Z(j\omega_1)) = -\tan^{-1} M \quad \text{or} \quad \phi(Z(j\omega_2)) = +\tan^{-1} M \quad (4.11)$$

As illustrated in Figure 4.3, for ω_1 with $\phi(Z(j\omega_1)) = \tan^{-1} M$, the impedance magnitude is so small that the loop gain is less than one. Hence no oscillation occurs at ω_1 . Oscillation is sustainable when ω satisfies $\phi(Z(j\omega_2)) = -\tan^{-1} M$. The oscillation frequency can be tuned from ω_0 to ω_2 when a control voltage varies the coupling coefficient 0 to M .

Figure 4.3 Magnitude and phase responses of the LC resonator

4.2 Analysis of Series QVCO

The structure of Series QVCO is similar to that of Parallel QVCO, and it is shown in Figure 4.2. $M1-M2$ and $M5-M6$ are identical switching transistors operating in the saturation region with the same transconductance g_m ; and $M3-M4$ and $M7-M8$ are identical coupling transistors operating in the triode region. In this case the coupling transistors are placed in series of the switching transistors, and the following analysis shows that the quadrature signals can be generated through this structure³.

Considering the $M1-M3$ branch of the bottom series QVCO, the current flowing through $M3$ is:

$$\begin{aligned} I &= \mu_n C_{ox} (W/L)_3 [(V_{GS3} - V_{th})V_{DS3} - (1/2)V_{DS3}^2] \\ &\approx \mu_n C_{ox} (W/L)_3 [(V_{GS3} - V_{th})V_{DS3}] \\ &= K_3 [(V_{GS3} - V_{th})V_{DS3}] \end{aligned} \quad (4.12)$$

where I , V_{GS3} and V_{DS3} consist of both DC and AC components: $I = I_{DC} + i$, $V_{GS3} = V_{GS3,DC} + v_{gs3}$ and $V_{DS3} = V_{DS3,DC} + v_{ds3}$, where I_{DC} , $V_{GS3,DC}$ and $V_{DS3,DC}$ are the DC components, and i , v_{gs3} and v_{ds3} are the AC components. So equation (4.12) becomes:

$$I_{DC} + i = K_3 (V_{GS3,DC} + v_{gs3} - V_{th})(V_{DS3,DC} + v_{ds3}) \quad (4.13)$$

Since v_{gs3} and v_{ds3} are the AC signals at node D and S respectively, replacing them by v_d and v_s , and expanding the right-hand-side of equation (4.13), we can get:

³ To simply the analysis, the small-signal transistor model is applied, and 2nd-order effects are not considered in the derivation.

$$I_{DC} + i = K_3 (V_{GS3,DC} - V_{th}) V_{DS3,DC} + K_3 v_d V_{DS3,DC} + K_3 (V_{GS3,DC} - V_{th} + v_d) v_s \quad (4.14)$$

It is clear that the DC current is the first term of the right hand side of the equation:

$$I_{DC} = K_3 (V_{GS3,DC} - V_{th}) V_{DS3,DC} \quad (4.15)$$

and the AC current is:

$$\begin{aligned} i &= K_3 v_d V_{DS3,DC} + K_3 (V_{GS3,DC} - V_{th} + v_d) v_s \\ &\approx K_3 v_d V_{DS3,DC} + K_3 (V_{GS3,DC} - V_{th}) v_s \end{aligned} \quad (4.16)$$

(v_d is assumed small compared to the gate over-drive voltage $V_{GS3,DC} - V_{th}$.)

On the other hand, the AC current flowing through M1 is:

$$i = g_m v_{gs1} = g_m (v_b - v_s) \quad (4.17)$$

where v_b is the AC signal at node B.

From equations (4.16) and (4.17), we can get:

$$K_3 v_d V_{DS3,DC} + K_3 (V_{GS3,DC} - V_{th}) v_s = g_m (v_b - v_s) \quad (4.18)$$

Rearranging the above equation, we get:

$$v_s = \frac{g_m v_b - K_3 v_d V_{DS3,DC}}{K_3 (V_{GS3,DC} - V_{th}) + g_m} \quad (4.19)$$

Substituting equation (4.19) back into (4.17), we obtain:

$$i = g_m \left[v_b - \frac{g_m v_b - K_3 v_d V_{DS3,DC}}{K_3 (V_{GS3,DC} - V_{th}) + g_m} \right] \quad (4.20)$$

Rearranging it, we get:

$$i = \frac{g_m K_3 (V_{GS3,DC} - V_{th})}{K_3 (V_{GS3,DC} - V_{th}) + g_m} \left(v_b + \frac{V_{DS3,DC}}{V_{GS3,DC} - V_{th}} v_d \right) \quad (4.21)$$

Let $Z(j\omega)$ be the LC tank impedance, then we can obtain the AC signal at node A:

$$v_a = -i \times Z(j\omega) = -\frac{g_m K_3 (V_{GS3,DC} - V_{th}) Z(j\omega)}{K_3 (V_{GS3,DC} - V_{th}) + g_m} \left(v_b + \frac{V_{DS3,DC}}{V_{GS3,DC} - V_{th}} v_d \right) \quad (4.22)$$

Since v_a and v_b are differential signals, we can replace v_b by $-v_a$ in equation (4.22),

then we obtain:

$$v_a = \frac{g_m K_3 (V_{GS3,DC} - V_{th}) Z(j\omega)}{K_3 (V_{GS3,DC} - V_{th}) + g_m} \left(v_a - \frac{V_{DS3,DC}}{V_{GS3,DC} - V_{th}} v_d \right) \quad (4.23)$$

Repeating all the steps for $M6$ - $M8$ branch, we can get a similar expression for v_d :

$$v_d = \frac{g_m K_8 (V_{GS8,DC} - V_{th}) Z(j\omega)}{K_8 (V_{GS8,DC} - V_{th}) + g_m} \left(v_d + \frac{V_{DS8,DC}}{V_{GS8,DC} - V_{th}} v_a \right) \quad (4.24)$$

Since the two VCOs are identical, we can set:

$$M = \frac{V_{DS3,DC}}{V_{GS3,DC} - V_{th}} = \frac{V_{DS8,DC}}{V_{GS8,DC} - V_{th}}, \quad (4.25)$$

$$G(j\omega) = \frac{g_m K_3 (V_{GS3,DC} - V_{th}) Z(j\omega)}{K_3 (V_{GS3,DC} - V_{th}) + g_m} = \frac{g_m K_8 (V_{GS8,DC} - V_{th}) Z(j\omega)}{K_8 (V_{GS8,DC} - V_{th}) + g_m}, \quad (4.26)$$

and $X = v_a$, $Y = v_d$, then equation (4.23) and (4.24) can be represented as:

$$X = (X - MY)G(j\omega) \quad (4.27)$$

$$Y = (Y + MX)G(j\omega) \quad (4.28)$$

Using equation (4.28) to divide equation (4.27), we can get:

$$\frac{X}{Y} = \frac{X - MY}{Y + MX}$$

$$\Rightarrow M(X^2 + Y^2) = 0 \quad (4.29)$$

From equation (4.29), it is clear that when M is not equal to 0, the only condition for equation (4.29) to be valid is $X = \pm jY$, i.e. $v_a = \pm jv_d$. Therefore, it is proved that the Series QVCO can generate quadrature signals.

The oscillation frequency ω can be found by substituting $X = \pm jY$ into equation (4.27) or (4.28), then we can obtain:

$$(1 + jM)G(j\omega) = 1 \quad (4.30)$$

For equation (4.30), there are two possible conditions that the oscillation may occur:

$\phi(Z(j\omega_1)) = +\tan^{-1} M$ or $\phi(Z(j\omega_2)) = -\tan^{-1} M$. From the previous analysis, it will be known that the oscillation will occur when ω satisfies $\phi(Z(j\omega_2)) = -\tan^{-1} M$.

4.3 Design of Low Power Series QVCO

4.3.1 Description of the Circuit

Figure 4.4 Schematic of low-power Series QVCO

Compare to the Parallel QVCO, the coupling transistors $M3$ - $M4$ and $M7$ - $M8$ are in series with the switching transistors $M1$ - $M2$ and $M5$ - $M6$. Hence the bias current flowing through the switching transistors can be reused for the coupling transistors; therefore the Series QVCO consumes less power than Parallel QVCO. Furthermore, by adding cross-coupled PMOS transistors on top of the cross-coupled NMOS transistors, the current-reuse technique is used to further reduce the current consumption of S-QVCO. The open-drain transistors are added to the output nodes of the S-QVCO to represent the dummy input transistors of the mixer stage. Table 4-1 is a summary of the

dimensions of the devices shown in Figure 4.4, and we will discuss these aspects in details in the following sections.

Table 4-1 Series QVCO components dimensions

$NM1-NM2, NM5-NM6$	$30\mu\text{m}/0.18\mu\text{m}$
$PM1-PM4$	$60\mu\text{m}/0.18\mu\text{m}$
$NM3-NM4, NM7-NM8$	$60\mu\text{m}/0.18\mu\text{m}$
$L1=L2=L3=L4=L$	2.77nH
<i>Varactor</i>	Tunable from 0.5pF

4.3.2 Design of the LC Tank

The design procedure of LC tank for the Series QVCO is similar to what has been presented in Chapter 3. In [69] it is shown that the power consumption decreases quadratically with respect to the increment of the tank inductance. Furthermore, in [70] it is found that although the inductance L and the series resistance R are scaled proportionally, the equivalent parallel resistance R_p still increases linearly with L . However, [95] pointed out that as the increased L enters the voltage-limited regime, the overall performance degrades. Moreover, large inductor will give large parasitic capacitance, which limits the frequency tuning range. Therefore the oscillator usually suffers from a trade-off between the power consumption, output power, phase noise

performance and the tuning range. This Series QVCO is specially designed for the 2.4GHz ISM band to meet the ZigBee standard which covers 2.42-2.48GHz, so the requirement on the frequency tuning range is not so stringent. The varactors provided by the foundry have limited number of selections with discrete values, and 0.5pF varactor was selected for this design.

The formula $f = \frac{1}{2\pi\sqrt{LC}}$ is used to calculate the inductor value. From the C - V curve of the 0.5pF varactor shown in Figure 3.25, the capacitance varies from 0.6pF to 0.98pF, so we can select the average value of 0.8pF for calculation. With $f=2.4\text{GHz}$ and $C_{var}=0.8\text{pF}$, L can be calculated to be 5.4nH. However, the parasitic capacitances contributed by the switching and coupling transistors have not been counted in, and the loading effect from mixer stage also needs to be considered. The parasitic capacitances and the loading from mixer contribute another large capacitance at the oscillation nodes. Taking into consideration the parasitic effect, the inductor is expected to be much smaller than the theoretical value of 5.4nH. Simulation has been done to find a proper inductor size which gives the desired frequency range, and finally the inductor is selected to be 2.77nH.

4.3.3 Design of the Amplifier

As derived in Section 4.2, the coupling coefficient of these two VCOs can be expressed as:

$$M = \frac{V_{DS3,DC}}{V_{GS3,DC} - V_{th}} = \frac{V_{DS8,DC}}{V_{GS8,DC} - V_{th}}$$

where $V_{DS3,DC}$ and $V_{DS8,DC}$ are the drain-source DC voltages of the coupling transistors, $V_{GS3,DC}$ and $V_{GS8,DC}$ are the gate-source DC voltages of the coupling transistors, and V_{th} is the threshold voltage. In [71], it is shown that as the coupling coefficient increases, the design is less sensitive to component variation, and well matched I/Q signals with accurate 90° phase difference can be generated even there is mismatch in the components. As the drain-source voltage $V_{DS,DC}$ is difficult to be controlled, we can decrease the gate-source voltage $V_{GS,DC}$ of the coupling transistors to increase the coupling coefficient. Since the coupling transistor's source is at AC ground, only its gate voltage needs to be decreased to get a small $V_{GS,DC}$. It is clear from Figure 4.2 that the gate voltage of the coupling transistor is same as gate voltage of the cross-coupled PMOS, because their gates are connected together at the oscillation nodes. If we consider the PMOS, since $I_{DS} \propto (W/L)_p (V_{SG} - V_{th,p})^2$, the aspect ratio (W/L) of the PMOS has to be small to get a low gate voltage. Therefore, in order to increase the coupling coefficient M , the aspect ratio of the cross-coupled PMOS need to be small. However, to make sure that the output sine wave has symmetrical rise time and fall time, the PMOS size is usually chosen as twice of the size of the switching NMOS transistor. If the PMOS size is too small, the NMOS will be even smaller, and it may be

too small to provide enough gain to sustain oscillation. Finally, as a compromise, the size of the cross-couple PMOS is selected as $60\mu\text{m}/0.18\mu\text{m}$, and the size of the cross-coupled NMOS is selected as $30\mu\text{m}/0.18\mu\text{m}$.

4.3.4 Design of the Coupling Transistors

According to [72], the coupling transistors need to be much larger than the switching transistors for minimum phase noise contribution. However, as the coupling transistors' size increases, its parasitic effect becomes and more significant which introduce large loading to the resonate tank. In order to maintain the desired oscillation frequency, the size of coupling transistor needs to be limited. Finally its size is chosen as $60\mu\text{m}/0.18\mu\text{m}$.

4.4 Design of Parallel QVCO

Figure 4.5 Schematic of Parallel QVCO

A Parallel QVCO has been designed and fabricated in order to compare its performance with Series QVCO. The schematic of Parallel QVCO is shown in Figure 4.5. The structure is very similar to Series QVCO, except that the coupling transistors $NM3$ - $NM4$ and $NM7$ - $NM8$ are in parallel with the switching transistors $NM1$ - $NM2$ and $NM5$ - $NM6$, and extra bias transistors $NM9$ and $NM10$ have been added to control the current flowing through the coupling transistors. The design concept is similar to that of series QVCO, and for comparison purpose, the device parameters have been chosen to be the same as series QVCO. Table 4-2 shows the dimensions of the components used in Figure 4.5.

Table 5-2 Parallel QVCO components dimensions

<i>NM1-NM2, NM5-NM6</i>	30/0.18 μ m
<i>PM1-PM4</i>	60/0.18 μ m
<i>NM3-NM4, NM7-NM8</i>	60/0.18 μ m
<i>L1=L2=L3=L4=L</i>	2.77nH μ m
<i>Varactor</i>	Tunable from 0.5pF
<i>NM9-NM10</i>	72/0.35 μ m

As analyzed in section 4.1, the oscillation frequency of Parallel QVCO can be controlled by both LC tank and the coupling coefficient M , where $M=gm_3/gm_1$. In Figure 4.5, V_{ctrl1} is used to control the varactor's capacitance, and V_{ctrl2} is used to control the bias current of the coupling transistors, and thus the coupling coefficient M .

For the Series QVCO, the coupling coefficient is $M = \frac{V_{DS3,DC}}{V_{GS3,DC} - V_{th}} = \frac{V_{DS8,DC}}{V_{GS8,DC} - V_{th}}$,

which cannot be tuned easily, so the output frequency for the Series QVCO can only be controlled through the varactor. Because there are two mechanisms to vary the output frequency, so it is expected that the Parallel QVCO has wider frequency tuning range than Series QVCO.

4.5 Layout Consideration

For both Parallel QVCO and Series QVCO, the symmetrical layout is crucial to ensure well matched I/Q signals. The components those need to be matched include the switching transistors ($NM1$ - $NM2$, $NM5$ - $NM6$ and $PM1$ - $PM4$), coupling transistors ($NM3$ - $NM4$, $NM7$ - $NM8$), inductors ($L1$ - $L4$), varactors ($C1$ - $C4$) and the biasing transistors ($NM9$ - $NM10$).

The common centroid technique is applied to the switching transistors, coupling transistors and the varactors. Figure 4.6 shows the position of the mentioned components.

Figure 4.6 Layout of switching transistors, coupling transistors and varactors

The matching between the biasing transistors $NM9$ and $NM10$ is also important. The drains of $NM9$ and $NM10$ are connected to different VCOs and their sources are shorted

together to ground. To get a better matching behavior, each transistor is sub-divided into 4 fingers. As the bias transistors have multiple fingers, the inter-digitization technique has been applied here and the layout is shown in Figure 4.7. G9 and G10 represent the gates of NM9 and NM10 respectively, D9 and D10 denotes the drains, and S is the source.

Figure 4.7 Layout of bias transistors NM9 and NM10

The differential inductors are used in this design to achieve better matching between the differential signals. A differential inductor is formed from branch coils that are staggered with respect to one another rather than concentrically coiled within one another. Each coil is formed from conductive strips. The inductor used in this design has 4 turn and its die photograph is shown in Figure 4.8.

Figure 4.8 Die photograph of differential inductor

4.6 Circuit Performance

4.6.1 Measurement Results of Series QVCO

Figure 4.9 Die photo of Series QVCO

The Series QVCO has been designed and fabricated using Chartered 0.18 μ m process. Its total area is 0.59mm² including pads, and its die photo is shown in Figure 4.9. Its output frequency can be tuned from 2.330GHz to 2.589GHz by varying Vctrl from 0.6V to 1.8V, which corresponds to 10.53% tuning range. The output waveform of the Series-QVCO is captured by Lecory digital oscilloscope in Figure 4.10. The measured amplitude of the S-QVCO was 241.4mV and 246.4mV for I and Q signals respectively. The phase difference between I/Q signals is measured directly by the digital oscilloscope, which is 90.13°. The phase noise at 1Mhz offset from 2.58GHz carrier is -128.0dBc/Hz as shown in Figure 4.11. The total current consumption of the S-QVCO

was only 1.5mA current, which was very low compared to other state-of-the-art designs.

The phase noise FOM is -191.95dB based on equation (3.42).

Figure 4.10 Measured output waveform of Series QVCO

Figure 4.11 Measured phase noise of series QVCO

4.6.2 Measurement Results of Parallel QVCO

Figure 4.12 Die photo of Parallel QVCO

In order to compare the performance with Series QVCO, the Parallel QVCO has also been fabricated using Chartered 0.18 μm process. Its total area is 0.59mm² including pads, and its die photo is shown in Figure 4.12. As discussed in Section 4.2, there are two frequency tuning mechanisms for Parallel QVCO. One is by changing the varactance, and another is by varying the coupling coefficient which can be controlled by the bias current of the coupling transistor.

Figure 4.13 shows the output frequency of Parallel QVCO for different coupling coefficients M , and also the output frequency of Series QVCO. By varying both V_{ctrl} and M , the output frequency of Parallel QVCO can be tuned from 2.247GHz to 2.649GHz, which corresponds to 16.42% tuning range. It is clear that the parallel QVCO has larger frequency tuning than series QVCO due to the additional frequency tuning mechanism.

Figure 4.13 Measured frequency tuning range of Parallel QVCO and Series QVCO

The output waveform of the Parallel QVCO is depicted in Figure 4.14. The measured phase difference between I/Q signals of the parallel QVCO is 90.1° . The output amplitudes for the I/Q signals are 239.1mV and 243.4mV. The phase noise at 1MHz offset from 2.59GHz carrier is -125.8dBc/Hz as shown in Figure 4.15. The total current consumption for the Parallel QVCO was 2.25mA for M=1 and 3.4mA for M=2.5, which is higher than series QVCO. The phase noise FOM of the Parallel QVCO is -186.2dB based on equation (3.42).

Figure 4.14 Measured output waveform of Parallel QVCO

Figure 4.15 Measured phase Noise of parallel QVCO

4.6.3 Performance comparison

The Series QVCO and Parallel QVCO have been analyzed and their performances have been discussed. The quadrature generator using RC polyphase network approach has also been investigated in Chapter 3. The three designs have their own advantages and disadvantages. In general, the quadrature generator with RC polyphase network can provide well-matched I/Q signals over a wide bandwidth, but due the attenuation caused by the passive components R and C, power-hungry amplifiers are usually required to obtain a suitable output power level. Its phase noise and frequency tuning

range mainly depends on the VCO stage. The series QVCO has the advantage of low power consumption and good phase noise performance. Nevertheless, because of the large parasitic capacitor loading at the oscillation nodes, its frequency tuning range is limited. By incorporating dual-tuning mechanism, that is, by varying both the varactor's capacitance and the coupling coefficient, the parallel QVCO can achieve relatively wide frequency tuning range, but its phase noise performance and power consumption are not as good as series QVCO. Table 4-3 summarizes the performances of the three designs, and also compares the performances with the state-of-the-art design. One can select the suitable design approach based on the targeted application.

Table 4-3 Performances of the quadrature generators

	RC polyphase network	SQVCO	PQVCO	[73]
Output frequency(GHz)	2.18-2.48	2.33-2.589	2.25-2.65	5.09-6.15
Frequency tuning range	12.88%	10.53%	16.42%	18.9%
Phase Noise @1MHz offset (dBc/Hz)	-125.1	-128.0	-125.8	-119.39
Phase Noise FOM (dB)	-184.53	-191.95	-186.20	-188.21
I/Q Phase difference	89.99°	90.13°	90.11°	--
Output amplitude (mV)	235/250	241/246	239/243	--
Power consumption (mW)	7.02	2.7	4.05~6.12	4.9

Table 4-3 (cont'd) Performances of the quadrature generators

	[74]	[75]	[76]	[77]
Output frequency (GHz)	0.4	5.3	2.17-2.52	4.94-5.22
Frequency tuning range	--	10.1%	14.5%	5.5%
Phase Noise @1MHz offset (dBc/Hz)	-140	-119.3	-126	-124.58
Phase Noise FOM (dB)	-187	-183	-186	-189.42
I/Q Phase difference	--	95°	96°	90.65°
Output level	--	-7 dBm	--	2.35dBm
Power consumption (mW)	3.1	11.2	4.9	8.7

4.7 Design of Low-Power Cascode Quadrature VCO

4.7.1 Circuit Description

Figure 4.16 Schematic of Cascode QVCO

The proposed Cascode QVCO is constructed by stacking one VCO onto another VCO, and cross-coupling them through the coupling transistors as shown in Figure 4.16. Transistors $M1$ - $M4$ are the switching transistors which provide the negative resistance to initiate and maintain the oscillation; while transistors $M5$ - $M8$ are the coupling transistors which help to produce the quadrature signals. As one VCO is stacked onto

the other, they are at different DC levels. Therefore the coupling capacitors C_c and the bias resistors R_{bias} are necessary to ensure that the coupling and switching transistors in one VCO have the same DC bias condition; otherwise the circuit cannot work properly. For the Cascode QVCO, the coupling mechanism between these two VCOs is exactly the same as that for conventional Parallel QVCO. The only difference is that the two VCOs are in cascode, so almost half of the current can be saved.

4.7.2 Circuit Performance

It is clear that the current consumption of the proposed Cascode QVCO drops by almost half compared to the conventional Parallel QVCO. However, the headroom for each VCO also drops by almost half compared to that for the Parallel QVCO. As a result, the output signal swing of the Cascode QVCO is limited by the reduced headroom. If the output swing requirement is not stringent, Series QVCO structure presented in Chapter 4 can be used in the Cascode QVCO as well to further reduce the current consumption, but with the price of reduced frequency tuning range and phase noise performance. The main problem associated with this Cascode QVCO is the unbalance between the two VCOs. Ideally we want the voltages across the two VCOs to be identical, i.e. $V_{dd}-V_N=V_N-V_O$, where V_N and V_O are the DC voltage at node N and node O in Figure 4.16 respectively. However, due to the body effect of the transistors, the voltage at the centre node V_N is greater than $\frac{1}{2}(V_{dd}-V_O)$, i.e. the voltage is not equally divided between the two VCOs. As a result, I/Q mismatch is introduced.

Simulation results show that the I/Q phase error was 5° , and their amplitudes were also mismatched. The output waveforms are displayed in Figure 4.17.

Figure 4.17 Simulated output waveform of Cascode QVCO

The frequency tuning range of the Cascode QVCO was from 2.38GHz to 2.55GHz, and the phase noise was -114dBc/Hz at 1MHz offset as shown in Figure 4.18. Its current consumption was only 1mA for output amplitude of 100mV. Because of the poor I/Q matching, the application of this cascode QVCO is very limited. Future works can be done on balancing the two VCOs and solving the I/Q matching problem.

Figure 4.18 Simulated phase noise of Cascode QVCO

4.8 Summary

This chapter discussed different types of QVCOs: Parallel QVCO, Series QVCO and Cascode QVCO. It explains how are the quadrature signals generated from the parallel and series cross coupled topologies. After that the designs of Parallel QVCO and Series QVCO were discussed in detail. Finally the measurement results of the Parallel QVCO and Series QVCO were presented and compared with the quadrature generator using RC polyphase network approach. A cascode QVCO design was also proposed in this chapter. It has the advantage of low power consumption, but its performance such as frequency tuning range, I/Q matching needs to be improved.

CHAPTER 5

Low Power Low Phase Noise Eight-phase/ Quadrature VCO

5.1 Introduction

Due to the increasing demand for low power multi-band transceivers, the design of low power multi-band quadrature VCOs becomes more important but yet remains challenging. The most commonly adopted method was to use switched inductor or capacitor [78]-[79], but the parasitic of the switched elements inevitably degraded the quality factor of the LC tank. [80] showed a dual-band quadrature VCO realized by using frequency dividers, mixers and notch filters, but the increased circuitry complexity made this design unattractive.

In general, the operation in the higher frequency band imposes more challenges on the tuning range and phase noise performance than in the lower band due to the low loaded quality factor of the LC tank at high frequency. [81] introduced a method for realizing dual-band VCO by using frequency doublers, but the design was limited to differential/signal-ended mode operations. [82] discussed a 15/30-GHz dual-band multiphase VCO using the similar design concept. However, due to the signal loss along the coplanar strip line in the rotary traveling-wave oscillator, the circuit required a large power to start-up and sustain the VCO oscillation.

This chapter presents a dual-band eight-phase/quadrature VCO that can cover the most popular industrial, scientific and medical (ISM) frequency bands, such as Blue Tooth (2.40GHz—2.48GHz), IEEE 802.11_{b,g} (2.40GHz—2.48GHz for Europe and USA), IEEE 802.11_a (5.15GHz-5.25GHz/5.25GHz—5.35GHz) and HiperLAN (5.15GHz—5.30GHz). Because the targeted higher band frequency is almost twice of the lower band frequency, the higher band signal can be generated by multiplying the lower band frequency by 2. The series cross-coupled VCOs are implemented for the 2.4GHz band operation. Since the signals are coupled actively, and because of the series-coupling topology, the low-power operation can be achieved. The frequency doublers are adopted to provide signals at 5GHz band. Power-down scheme is implemented in the frequency doublers, which shuts off the supply to the frequency doubler when the system is working in the lower-band frequency. Therefore the overall power consumption can be further reduced. In this proposed design, the same LC tank is used for both bands operations, thus eliminating the disadvantages brought by the use of small size inductor/capacitor for higher band operation. Furthermore, compared to the conventional dualband QVCO designs in [78]-[79], the proposed design can provide eight-phase signals rather than four-phase signal in the lower band. This makes the circuit suitable for more applications, such as to be used in the clock and data recovery (CDR) circuits with quarter-rate sampling [83] or 1/8-rate sampling [84] topology.

5.2 Architecture

The architecture of the dual-band eight-phase/quadrature VCO is illustrated in Figure 5.1. It consists of an eight-phase VCO and four frequency doublers. PMOS-NMOS paired transistors with their drains and sources connected together are used as the switches for band selection. The eight-phase VCO oscillates in the 2.5GHz band, and the frequency doublers convert the signals from the 2.5GHz band to the higher 5.0GHz frequency band. In such a way, the frequency tuning range and the phase noise performance in the higher band can be maintained comparable as that in the lower band; while in other reported designs, the frequency tuning range and phase noise usually degrade in the higher band.

Figure 5.1 Architecture of proposed dual-band VCO

5.3 Lower Band Operation

5.3.1 Selection of topology

As discussed in Chapter 3 and Chapter 4, the RC polyphase network and the cross-coupled VCOs are the two major approaches to generate quadrature signals. In fact, besides quadrature signals, they can be used to produce eight-phase signals by using the same design concept with some modification to the circuits.

5.3.1.1 RC polyphase network

There was no RC polyphase network used for eight-phase signal generation presented in literature. Nevertheless, it is intuitive to believe that the below structure which is expanded from the structure in Figure 3.1 can suit for this purpose:

Figure 5.2 Proposed RC polyphase network for eight-phase signal generation

Figure 5.2 shows the basic structure of the proposed RC polyphase network used to generate eight-phase signals. The input signals are differential, and the output signals will have 45° phase difference with each other. We use v_{in} and $-v_{in}$ to denote the input differential signals. The eight inputs in_1 - in_8 can be v_{in} or $-v_{in}$ or at ground level, consequently there are a lot of combinations for the input sequence. Not all the combinations can produce eight-phase output signals; therefore it is a matter to determine a suitable input combination for generating eight-phase output signals. By using the linear superposition principle, the output signals in Figure 5.2 can be expressed as:

$$out_1 = \frac{1}{1+sRC}in_1 + \frac{sRC}{1+sRC}in_8 \quad (5.1)$$

$$out_2 = \frac{1}{1+sRC}in_2 + \frac{sRC}{1+sRC}in_1 \quad (5.2)$$

$$out_3 = \frac{1}{1+sRC}in_3 + \frac{sRC}{1+sRC}in_2 \quad (5.3)$$

$$out_4 = \frac{1}{1+sRC}in_4 + \frac{sRC}{1+sRC}in_3 \quad (5.4)$$

$$out_5 = \frac{1}{1+sRC}in_5 + \frac{sRC}{1+sRC}in_4 \quad (5.5)$$

$$out_6 = \frac{1}{1+sRC}in_6 + \frac{sRC}{1+sRC}in_5 \quad (5.6)$$

$$out_7 = \frac{1}{1+sRC}in_7 + \frac{sRC}{1+sRC}in_6 \quad (5.7)$$

$$out_8 = \frac{1}{1+sRC}in_8 + \frac{sRC}{1+sRC}in_7 \quad (5.8)$$

Through careful observation and by using the method of successive substitution, it can be found that the following input sequence can be one of the possible combinations to get eight-phase outputs: $in_1=v_{in}$, $in_2=0$, $in_3=-v_{in}$, $in_4=v_{in}$, $in_5=v_{in}$, $in_6=-v_{in}$, $in_7=-v_{in}$, $in_8=0$. The corresponding outputs are:

$$out_1 = \frac{1}{1+sRC}v_{in} \quad (5.9)$$

$$out_2 = \frac{sRC}{1+sRC}v_{in} \quad (5.10)$$

$$out_3 = -\frac{1}{1+sRC}v_{in} \quad (5.11)$$

$$out_4 = \frac{1-sRC}{1+sRC}v_{in} \quad (5.12)$$

$$out_5 = \frac{1+sRC}{1+sRC}v_{in} \quad (5.13)$$

$$out_6 = \frac{sRC-1}{1+sRC}v_{in} \quad (5.14)$$

$$out_7 = -\frac{1+sRC}{1+sRC}v_{in} \quad (5.15)$$

$$out_8 = -\frac{sRC}{1+sRC}v_{in} \quad (5.16)$$

Let out_1 be the 0° reference, the phases of the other 7 outputs are: $\angle out_2 = 90^\circ$, $\angle out_3 = 180^\circ$, $\angle out_4 = -45^\circ$, $\angle out_5 = 45^\circ$, $\angle out_6 = 135^\circ$, $\angle out_7 = 215^\circ$, $\angle out_8 = -90^\circ$. The schematic is shown in Figure 5.3.

Figure 5.3 1st-order RC eight-phase network

From equations (5.9)-(5.16), it can be seen that the 45° phase difference between the output signals is maintained for all frequencies, but the output signals' amplitudes only match at $\omega_o = \frac{1}{RC}$. When the frequency deviates from $\omega_o = \frac{1}{RC}$, the error in amplitude matching increases. In order to improve the amplitude matching, more stages can be cascaded together. The behavior of the RC eight-phase network is exactly the

same of the RC quadrature-phase network except the phase difference. Therefore the analysis for the 2nd-order and 3rd-order RC polyphase networks in Chapter 3 can be applied here. Therefore it will be known that as the number of stages increases, the output signals' amplitude can be matched for a very wide bandwidth, but the drawback is the high signal attenuation.

5.3.1.2 Eight-phase cross-coupled VCO

Figure 5.4 Structure of eight-phase VCO

Figure 5.4 shows the architecture of the eight-phase VCO by using the cross-coupled VCOs approach. It is composed of four differential VCOs connected in a loop. The positive and negative outputs from VCO1 are fed into VCO2 in phase. The same connection applies to VCO2 and VCO3. For VCO4, its positive output v_{out4+} is connected to the negative input of VCO1, and its negative output v_{out4-} is connected to the positive input of VCO1. As a consequence of this cross-coupling structure, the total phase shift in the loop is 180°, so the output signals from any two adjacent VCOs will have 45° phase difference. If we take the phase of v_{out1+} as the 0° reference, then we can obtain the phases of v_{out2+} , v_{out3+} and v_{out4+} as 45°, 90°, 135° respectively, and the phases of v_{out1-} , v_{out2-} , v_{out3-} and v_{out4-} as 180°, 215°, 270°, 315° respectively.

5.3.1.3 Other eight-phase oscillator topologies

The same design concepts of the current-mode quadrature oscillator [52] and Cascode QVCO can be used to implement the eight-phase oscillator. Both the current-mode oscillator and the Cascode VCO have the advantage of super low power consumption, but their performance is limited by frequency tuning range, phase noise, signal matching and so on.

5.3.1.4 Selection of the eight-phase techniques

The RC polyphase network can provide well-matched eight-phase signals for a wide bandwidth by using at least two cascaded stages. However, due to the signal attenuation along the passive resistors and capacitors, amplifiers are generally required to magnify the signals to a certain level to drive the subsequent mixer stage. Because such amplifiers are power-hungry, therefore the RC polyphase network approach is not suitable for low power requirement. The current-mode oscillator consumes very low power, but its performance is limited by the frequency tuning range and phase noise. The Cascode QVCO structure also consumes low current, but its output signals cannot be well-matched. For the series-coupled VCOs, the phase noise performance does not link to the phase accuracy, thus the phase noise can be optimized by reducing the coupling strength without sacrificing the phase accuracy [85]. The performance comparison shown in Chapter 4 Table 4-3 also proves that the Series VCO is more suitable for low power low phase noise application. Therefore it is selected in this design.

5.3.2 Circuit Description

The series-coupling topology shown in Figure 5.5 is adopted in this design. By placing the coupling transistors in series with the switching transistors, the need for extra bias current for the coupling transistors is eliminated, thus the low-power operation is achieved. Cross-coupled PMOS transistors are used to boost the gain, which in turns reduce the power consumption for the same output power.

Figure 5.5 Series-coupled eight-phase VCO

The following analysis shows how is the eight-phase signals generated from the series-coupling structure from the circuit point of view, and it also derives the expression for the oscillation frequency.

By using the similar approach as in chapter 4 for the series-coupled quadrature VCO, we can arrive at the follow expressions:

$$v_{out1+} = G(j\omega)(v_{out1+} + Mv_{out4+}) \quad (5.17)$$

$$v_{out2+} = G(j\omega)(v_{out2+} - Mv_{out1+}) \quad (5.18)$$

$$v_{out3+} = G(j\omega)(v_{out3+} - Mv_{out2+}) \quad (5.19)$$

$$v_{out4+} = G(j\omega)(v_{out4+} - Mv_{out3+}) \quad (5.20)$$

where $M = \frac{V_{AB}}{V_{GS,DC} - V_{th}}$ and $G(j\omega) = \frac{g_m Z(j\omega)}{2}$. By dividing equation (5.17) by

(5.18), (5.18) by (5.19), (5.19) by (5.20) and (5.20) by (5.17), we can get the following expressions:

$$\frac{v_{out1+}}{v_{out2+}} = \frac{v_{out1+} + Mv_{out4+}}{v_{out2+} - Mv_{out1+}} \Rightarrow -Mv_{out1+}^2 = Mv_{out2+}v_{out4+} \quad (5.21)$$

$$\frac{v_{out3+}}{v_{out4+}} = \frac{v_{out3+} - Mv_{out2+}}{v_{out4+} - Mv_{out3+}} \Rightarrow Mv_{out3+}^2 = Mv_{out2+}v_{out4+} \quad (5.22)$$

$$\frac{v_{out2+}}{v_{out3+}} = \frac{v_{out2+} - Mv_{out1+}}{v_{out3+} - Mv_{out2+}} \Rightarrow Mv_{out2+}^2 = Mv_{out1+}v_{out3+} \quad (5.23)$$

$$\frac{v_{out4+}}{v_{out1+}} = \frac{v_{out4+} - Mv_{out3+}}{v_{out1+} + Mv_{out4+}} \Rightarrow -Mv_{out4+}^2 = Mv_{out1+}v_{out3+} \quad (5.24)$$

From equations (5.21) and (5.22), we can obtain:

$$-Mv_{out1+}^2 = Mv_{out3+}^2 \Rightarrow v_{out1+} = \pm jv_{out3+} \quad (5.25)$$

From equations (5.23) and (5.24), we can get:

$$-Mv_{out2+}^2 = Mv_{out4+}^2 \Rightarrow v_{out2+} = \pm jv_{out4+} \quad (5.26)$$

Substituting equation (5.26) into (5.21), we get:

$$-v_{out1+}^2 = \pm jv_{out4+}^2 \Rightarrow v_{out1+} = v_{out4+} \angle \pm 45^\circ \quad (5.27)$$

Similarly, we can find the following relationships:

$$v_{out2+} = v_{out1+} \angle \pm 45^\circ \quad (5.28)$$

$$v_{out3+} = v_{out2+} \angle \pm 45^\circ \quad (5.29)$$

$$v_{out4+} = v_{out3+} \angle \pm 45^\circ \quad (5.30)$$

The new oscillation frequency ω can be found by substituting $v_{out1+} = v_{out4+} \angle \pm 45^\circ$ into equation (5.17) or (5.20), then we can obtain:

$$(1 + M \angle \pm 45^\circ) G(j\omega) = 1 \quad (5.31)$$

For equation (5.31), there are two possible conditions that the oscillation may occur:

$$\phi(Z(j\omega_1)) = +\tan^{-1}\left(\frac{\sqrt{2}/2}{1+\sqrt{2}/2}M\right) \text{ or } \phi(Z(j\omega_2)) = -\tan^{-1}\left(\frac{\sqrt{2}/2}{1+\sqrt{2}/2}M\right).$$

As discussed in Chapter 4, for a resonator with a lossy inductor, the magnitude of its impedance peaks at a frequency higher than the resonant frequency. Therefore, the impedance magnitude is so small at ω_l that the loop gain is less than one. Hence no oscillation occurs at ω_l . On the other hand, oscillation is sustainable when ω

$$\text{satisfies } \phi(Z(j\omega_2)) = -\tan^{-1}\left(\frac{\sqrt{2}/2}{1+\sqrt{2}/2}M\right).$$

5.3.3 Phase Noise Performance

The proposed eight-phase VCO possesses low phase noise due to the use of series-VCO topology, and the cross-coupled structure of 4-stage VCOs. The following analysis will address these two aspects separately.

5.3.3.1. Phase Noise of Series-VCO

For the cross-coupled VCO with the coupling transistor in parallel with the switching transistor, both the phase noise and phase accuracy depend on the coupling strength $\alpha = W_{cpl} / W_{cw}$, where W_{cpl} and W_{cw} are the widths of the coupling transistor and switching transistor respectively. As the coupling strength increases, the oscillation frequency deviates from the tank resonance frequency. It has been proved that there is a trade-off between the phase noise and phase accuracy. When the oscillator oscillates at an off-resonant frequency, the I/Q phase accuracy is improved, but the phase noise performance is degraded. In this series coupling topology, the phase error is independent of the coupling strength [85], therefore the phase noise performance can be optimized by reducing the coupling strength without sacrificing the phase accuracy.

Furthermore, in most VCOs, the phase noise in the $1/f^3$ region is dominated by the $1/f$ noise of the tail current. In the series-coupled VCO topology, the effect is significantly reduced due to the degeneration provided by the cascaded structure that reduces the noise current that can reach the tank. Moreover, the effect of the noise from the switching transistor has also been significantly reduced as the noise current cannot find a direct path to the LC tank, thus its conversion to the close-in phase noise is less effective.

Besides the flicker noise of the tail transistor, other main phase noise contributors include the thermal noise from the LC-tank parasitic resistor, the transistor channel thermal noise and transistor gate noise. Because of the up-conversion effect, the flicker

noise will contribute to the phase noise in the $1/f^3$ region, while the thermal noise and gate noise are up-converted to $1/f^2$ noise.

An equivalent noise model for the designed VCO is depicted in Figure 5.6, where $\overline{i_b^2}$ is the flicker noise of the tail transistor, which is proportional to $K/C_{ox}WLf$, where K is the flicker noise coefficient, W and L are the channel width and length respectively, and C_{ox} is the gate-oxide capacitance; $\overline{i_{gcp}^2}$, $\overline{i_{gswn}^2}$ and $\overline{i_{gswp}^2}$ are the gate noise of the coupling transistor, and the N/PMOS switching pairs respectively, which are proportional to $8kT\delta C_{gs}\epsilon l$, where k is the Boltzmann constant, T is the absolute temperature, δ is the coefficient of the gate noise, C_{gs} is the gate-source capacitance and ϵ is the coefficient of the gate noise; $\overline{i_{icp}^2}$, $\overline{i_{tswn}^2}$ and $\overline{i_{tswp}^2}$ are the transistor channel thermal noise, which are proportional to $4kT\gamma g_m$, where γ is the coefficient of the channel thermal noise; finally $\overline{i_R^2}$ is the thermal noise of the tank lossy resistor and it is equal to $4kTG_{loss}$.

Figure 5.6 Equivalent noise circuit of the series VCO

With the knowledge of each noise contributor, the VCO components' sizing has been optimized for phase noise performance. Most of the parameters are process dependent, and there are a few circuit parameters we can control, namely, the channel length and channel width of the transistors, and the LC tank's quality factor. The optimization includes selecting large W and L for the tail transistor to minimize its flicker noise; using minimum channel length and relatively small W/L ratio for the switching and coupling transistors to reduce their gate noise and channel thermal noise. Finally, the thermal noise of the lossy LC tank can be minimized by utilizing relatively high Q on-chip inductor, which is subject to the supporting foundry's process. The Global Foundry 0.18 μm IC 6LM process has been used, and the inductor adopted in the

design is the symmetrical inductor with thick metal layers. The width of the inductor coil is $15\mu\text{m}$ and the turn-to-turn spacing is $3\mu\text{m}$. The inductor was realized as a 5.5nH differential inductor by stacking the fifth metal layer and the top metal layer to prevent the loss of the metal and substrate, achieving a measured Q of 10.3 at 2.5GHz as shown in the below figure.

Figure 5.7 Simulated quality factor of 5.5nH differential inductor

It has been addressed in [86] that the increase in number of the VCO stages helps to reduce the overall phase noise of the oscillator. This is because the noise Impulse Sensitivity Function (ISF) is inversely proportional to the number of LC tanks. Since the phase noise can be viewed as a disturbance in the phase as a result of an impulse noise, it is intuitive to expect that, as the number of VCO stages increases, the total phase disturbance is divided among the LC tanks, thus each LC tank takes only one

portion of the total disturbance. Therefore the phase noise of an N -stage VCO is lower than a single VCO, provided other design parameters are the same.

On the other hand, the phase noise of the N -stage VCO also can be analyzed quantitatively as below. The previous section gives the equivalent VCO circuit with various noise sources. The total noise can be summed up at the LC tank, and the VCO can be represented as a linear model with a single noise current injecting into the LC tank as shown in Figure 5.8.

Figure 5.8 Linear noise model of a VCO with coupling transistors

The eight-phase oscillator consists of four stages of such VCO, and its equivalent linear model is represented in Figure 5.9. Although nonlinearity is a fundamental property of all real oscillators as it is necessary for amplitude limiting, the linear model is still applicable in the noise aspect because the noise is much smaller in magnitude than the carrier [87]. The phase noise can be treated as a certain amount of injected noise which produces a certain amount of phase disturbance, it is rational to expect that doubling the injected noise will induce double disturbance. Therefore, linearity would appear to be a reasonable assumption as far as the noise-to-phase transfer function is concerned.

Figure 5.9 Linear noise model of eight-phase VCO

The phase noise of the 4-stage LC oscillator can be calculated using the linear modeling method as outlined in [88]. Application of this model on the N -stage LC oscillator results in the following expression:

$$L(\Delta f) = 10 \log \left(\frac{1}{8Q_N^2} \cdot \frac{N \cdot \overline{i_n^2}}{\overline{i_{sig}^2}} \cdot \left(\frac{f_{osc}}{\Delta f} \right)^2 \right) \quad (5.32)$$

where f_{osc} is the carrier frequency, Δf is the offset frequency, $\overline{i_n^2}$ and $\overline{i_{sig}^2}$ are the noise and signal current respectively, and Q_N is approximately equal to $Q_N \approx N \cdot Q_p \cdot \cos(\varphi)$, where Q_p is the loaded tank quality factor and φ is the phase angle between the tank current and voltage.

Compared to the single VCO or 2-stage cross quadrature VCO, the eight-phase VCO can improve the phase noise performance by 6dB and 3dB respectively according to equation (5.32), assuming all the other design parameters are the same.

5.4 Higher Band Operation

5.4.1 Circuit Description

Figure 5.10 Schematic of the frequency doubler

The frequency doubler utilizes the non-linear characteristics of the transistor amplifier and its schematic is illustrated in Figure 5.10. *NM1* and *NM2* are differential NMOS transistors, and v_{in+} , v_{in-} are the differential output signals from the eight-phase VCO. By joining the drains of *NM1* and *NM2* together, the differential fundamental components cancel out each other, and the 2nd order harmonic are added together at node v_{out} [81]. The inductor L_o and the parasitic capacitance at the node v_{out} form a resonator with resonant frequency at 5GHz. This helps to further filter out the unwanted components and amplify the 2nd order harmonics.

Considering only the AC components, the output signal at node v_{out} of this frequency doubler can be written as:

$$v_{out} = a_1 v_{in+} + a_2 v_{in+}^2 + \dots + b_1 v_{in-} + b_2 v_{in-}^2 + \dots \quad (5.33)$$

where $v_{in+} = A \cos(\omega_o t + \theta)$, $v_{in-} = A \cos(\omega_o t + \theta + 180^\circ)$, and $a_1, a_2, \dots, b_1, b_2, \dots$ are the harmonic coefficients for the system. Assuming the input signals are fully differential, and $NM1$ and $NM2$ are well matched, i.e. $a_1 = b_1, a_2 = b_2 \dots$, and other higher order harmonics are negligible, the output voltage expression can be simplified to:

$$\begin{aligned} v_{out} &= a_2 (v_{in+}^2 + v_{in-}^2) \\ &= 2a_2 [A^2 \cos^2(\omega_o t + \theta)] \\ &= a_2 A^2 [1 + \cos(2\omega_o t + 2\theta)] \end{aligned} \quad (5.34)$$

It is obvious from equation (5.33) that the fundamental frequency component ω_o is removed, and the 2nd-order harmonics $2\omega_o$ is generated and amplified. In such a way, the frequency doubling is achieved. Moreover, the phase of the signal is also doubled, thus the phase of the output signals from the four frequency doublers become $0^\circ, 90^\circ, 180^\circ, 270^\circ$.

The coefficient a_2 is determined by the second-order effect of the doubler, and it can be expressed as [4]:

$$a_2 = \frac{4\mu_0 C_{OX} v_{sat}^3 W L^2}{[2L v_{sat} + (V_{GS} - V_{th})(\mu_0 + 2L v_{sat} \theta)]^3} \quad (5.35)$$

The conversion gain of the frequency doubler is strongly dependent on a_2 . The above equation provides a guideline for the design of the frequency doublers with optimal conversion gain. In order to achieve a high conversion gain for enhanced output power at the second harmonic, MOSFETs with a large channel width and a minimum gate

length are desirable. Moreover, a low overdrive voltage is required to maximize the nonlinearity of the devices.

The power-down scheme is implemented in the frequency doubler. As shown in Figure 5.10, the power supply of the frequency doubler is connected to the band-select control voltage. When the system is operating in the lower frequency band, the band-select control voltage is grounded and the frequency doubler consumes no power.

In the proposed design, there are four doublers to convert the lower band signal to the higher band signal. In order to improve the symmetry of the differential signals in the higher band, center-tapped inductors are used for the doublers with differential outputs. The complete schematic of the proposed dualband QVCO including the output switches is illustrated in Figure 5.11. The input biasing network to the frequency doubler which consists of a decoupling capacitor and biasing resistor is not shown in the figure in order to make the figure look more compact. Open-drain transistors are used as the output buffers, and external Bias-Tees will be used during measurement.

Figure 5.11 Full schematic of proposed dual-band QVCO

5.4.2 Phase Noise Performance

According to Leeson's equation [9], the simplified phase noise of an oscillator can be expressed as:

$$L = 10 \log \left[\frac{FkT}{A} \frac{1}{8Q_L^2} \left(\frac{f_o}{\Delta f} \right)^2 \right] \quad (5.36)$$

where F is the device noise factor at operating power level A , k is the Boltzmann's constant 1.38×10^{-23} J/K, T is the absolute temperature, Q_L is the loaded quality factor, f_o is the oscillator carrier frequency and Δf is the frequency offset from the carrier.

It is obvious that the loaded quality factor Q_L of the LC tank will greatly affect the phase noise performance. The existing dual-band VCOs/QVCOs presented scaled down the inductance to achieve the higher band operation. Whereas in this proposed dual-band VCO, the higher frequency is achieved through frequency doubler without decreasing the inductance in the LC tank. The following analysis proves that this method is more advantageous in achieving relatively high loaded quality factor.

For a loaded LC tank with lossy inductor, its schematic can be represented as in Figure 5.12:

Figure 5.12 Loaded LC tank with lossy inductor

where L and C are the inductance and capacitance including all the parasitic effects, and R_s/R_p are the parasitic series/parallel resistors.

The equivalent impedance of the LC tank can be calculated as:

$$Z(j\omega) = \frac{R_p(j\omega L + R_s)}{R_p + R_s - \omega^2 L C R_p + j\omega(L + C R_s R_p)} \quad (5.37)$$

The loaded quality factor Q_L can be found as the ratio of reactance and the resistance of $Z(j\omega)$:

$$Q_L(\omega) = \frac{\omega(R_p L - C R_s^2 R_p) - \omega^3 L^2 C}{R_p R_s + R_s^2 + \omega^2 L^2} \quad (5.38)$$

In the proposed design, the tank capacitor (varactor) was selected to be centered at 0.5pF, and there is additional 0.3pF parasitic capacitor added to the oscillation nodes. The inductor was chosen to be 5.5nH, with quality factor Q of 10.3at 2.5GHz. With the above components' values, the loaded quality factor $Q_L(\omega)$ can be plotted based on equation (5.38).

Figure 5.13 Loaded quality factor versus frequency

Figure 5.13 shows the loaded quality factor versus frequency based for two scenarios:

Scenario 1: the solid line represents the case that the loaded LC tank oscillates at $\omega_o=2.5GHz$ with $L_l = 5.5nH$, which is the case for the proposed design

Scenario 2: the dashed line represents the case that the loaded LC tank oscillates at $\omega_o=5.0GHz$ with $L_2 = 1.3nH \approx \frac{1}{4}L_1$. which is the case for the designs using smaller inductor to achieve higher frequency. Because at higher frequency, the effect of parasitic capacitance becomes more significant, so L_2 needs to be slightly less than $\frac{1}{4}L_1$ in order keep the resonant frequency at 5GHz. In a typical 0.18 μm CMOS process from Global Foundry, the unloaded Q of a 1.3nH inductor is around 9 at 5GHz.

From the plot it is observed that the loaded Q of scenario 1 is approximately 1.79 times larger than that of scenario 2 at their respective oscillation frequencies, which in turn gives 10.1 dB improvements in the phase noise performance, with the assumption that all the other parameters in equation (5.38) are the same for both cases.

The phase noise for the high frequency band can be further improved by increasing the doubler's conversion gain through the careful sizing the transistors. Assuming a conversion gain of 0dB for the frequency double, the output phase noise is theoretically increased by 6dB with respect to the lower band phase noise in an ideal case [9]. The

increasing in conversion gain can decrease the phase noise in the higher band directly. According to equation (5.35), in order to obtain a high conversion gain, the transistors with a large channel width and a minimum gate length are desirable, and the gate overdrive voltage needs to be kept as low as possible.

5.5 Experimental Results

The Global Foundry 0.18 μm CMOS process is used to design and implement the dual-band eight-phase/quadrature VCO. Six metal layers are used in the process. Inductors are implemented by stacking the fifth metal layer and top metal layer (sixth metal layer) to prevent the loss of the metal and substrate. The PMOS-varactor in the accumulation mode is used in the design. Its capacitance C_{var} is 0.5pF, and the dynamic range C_{max}/C_{min} is approximately 2.1 with $0 < V_{ctrl} < 1.5\text{V}$.

Figure 5.14 Die photograph of dual-band QVCO

The die photograph of the design is shown in Figure 5.14, and its area is 1.14mm² including pads. The design has been measured on the wafer level. The ground-signal-signal-ground (GSSG) RF probes are used at the output pads. The pitch of the RF probe is 100 μm and the probe station used is Cascade Microtech 12000.

The output frequency has been measured using HP8564E spectrum analyzer, and it is 2.23GHz—2.68GHz for the lower band, and 4.46GHz--5.36GHz for the higher band. The total current consumption is 2mA for the lower band and 5.8mA for the higher band from 1.5V supply. The phase noise measurement was done using the Rohde & Schwarz FSUP26 Signal Source Analyzer, and the result was -126dBc/Hz for the lower band, and -123dBc/Hz for the higher band. Figure 5.15 and Figure 5.16 show the phase noises for the two bands respectively.

Figure 5.15 Measured phase noise of lower band signal

A widely used figure-of-merit (FOM) for the VCO is defined as [61]:

$$FOM = L\{f_{offset}\} - 20 \log\left(\frac{f_o}{f_{offset}}\right) + 10 \log\left(\frac{P_{DC}}{1mW}\right)$$

Therefore, the phase noise FOMs for the two frequency bands can be calculated to be -189.4dB and -185.1dB respectively.

Figure 5.16 Measured phase Noise of higher band signal

The digital oscilloscope Lecory 8600A has been used to capture the output waveform and measure the phase difference between the I/Q signals. Figure 5.17 and Figure 5.18 show the output waveforms for the lower band and higher band quadrature signals respectively.

Figure 5.17 Measured quadrature output waveforms for lower band

Figure 5.18 Measured quadrature waveforms for the higher band

For the lower band signals, not all the eight-phase signals were probed out, only the quadrature signals were measured. Nevertheless, the phase difference θ_L of the eight-phase signals can still be predicted from the I/Q phase difference θ_H in the higher band: $\theta_L = 1/2\theta_H$. The measured phase difference between I/Q signals are 90° and 89° for the lower band and higher band respectively, and the phase difference of the eight-phase signals can be estimated to be: $89^\circ/2=44.5^\circ$. Figure 5.19 shows the post layout simulation result of the eight-phase signal.

Figure 5.19 Simulated output waveform of the eight-phase VCO

When the circuit operates in the higher band, there is a leakage of the low frequency components to the output terminals through the non-ideal output switches. Therefore, the higher band signal is slightly modulated by the lower band signal as observed in Figure 5.18. The imbalanced DC level of the doubler's input signals may also cause the lower band signal to appear in the output of the doubler. However, this effect has been minimized by symmetrical layout of the eight-phase VCO. Figure 5.20 and Figure 5.21

show the post-layout simulation results of the higher band signals before and after the switches. The signals at the input of the switches are well-matched in amplitude and phase, but the signals at the output of the switches are modulated by the lower band signals, and there is distortion in the waveforms. This indicates that the leakage through the output switches is the main contributor to the distortion of higher band signal. In fact, the output switch is needed only when the VCO is to be integrated in a dual-band transceiver system, and it is not the main focus of this design. The output switch can be further optimized to improve the leakage problem. There are several ways to optimize the switch design, for example, by selecting proper NMOS/PMOS size such that the channel length is not too large to limit the speed, nor too small to have a large on-resistance. The ratio of PMOS and NMOS's W/L can also be optimized to make the output signal's rising and falling edges symmetrical. Other types of switches such as analog mux can be considered as well due to their better performance at high frequencies.

Figure 5.20 Simulated higher band signal at the output of the frequency doubler

Figure 5.21 Simulated higher band signal at the output of the switches

Table 5-1 summarizes the performance of the proposed dual-band eight-phase/quadrature VCO and the comparison with the published works.

Table 5-1 Summary of dual-band VCO performance and comparison with other works

	This Work	[78]	[79]	[81]	[82]	[87]
Technology	0.18 μ m CMOS	0.25 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Lower band (GHz)	2.23—2.68 (14.0%)	2.07— 3.4 (50%)	1.80— 2.06 (13.5%)	2.14 (24.9%)	15 (1.67%)	3.27—5.02 (42.4%)
Higher band (GHz)	4.46—5.36 (14.0%)	5.094— 5.96 (15.7%)	4.12— 4.89 (17.1%)	5.15 (24.9%)	30 (1.67%)	9.48—11.36 (18.0%)
PN FOM (dB)	-189.4/-185.1	-169.6/- 163	-181.8/- 180.5	-188.3/- 183.7	-178.6/- 176.5	-181.0/-182
No. of output phases	8/4	4/4	4/4	2/1	8/4	4/4
I/Q Phase difference	90°/89°	--	--	--	--	SBR 49dB/47dB ⁴
Power consumption	3mW/ 8.7mW	28mW	6.8mW	5.4mW/ 8mW	52mW	6mW/ 10mW

⁴ Based on equation (2.10), the SBR can be converted the 0.41°/0.51° phase error

5.6 Conclusion

A low-power low-phase noise eight-phase/quadrature dual-band VCO operating in 2.4GHz and 5.0GHz frequency bands has been presented in this paper. The dual-band VCO uses the frequency doubling method to generate the higher band signals from the lower band signals, and it shows improved phase noise FOM compared to other works. The VCO has been implemented in 0.18 μ m CMOS technology, and its measured frequency was from 2.23GHz—2.68GHz and 4.46GHz—5.36GHz. The measured phase difference between the I/Q signals is 90°/89° for the lower band higher band respectively. The phase noise FOM is -189.4dB/-185.1dB, while draining 2mA/5.8mA from 1.5V power supply.

CHAPTER 6

Conclusions and Recommendations

6.1 Conclusions

The quadrature oscillators and generators play important roles in the modern direct-conversion and low-IF transceivers. Various methods for generating quadrature signals have been explored and investigated in this thesis.

One way for quadrature signal generations is to use the RC polyphase network. The transfer functions of the 1st-, 2nd- and 3rd-order RC polyphase networks used for quadrature signal generation have been re-derived based on very basic principles. The new approach removed the need of the complex phasor and matrix analysis; and it was simple and comprehensive. The output signals' matching behavior has also been explored. A quadrature generator consisting of a VCO, a 2nd-order RC polyphase network and output buffers has been designed and fabricated. In the presence of 15% component variation, it still achieved less than 0.5dB mismatch in amplitude and much less than 0.5° phase error. The quadrature generator had a frequency tuning range from 2.18GHz to 2.48GHz and provided more than 200mV output swing. It consumed 3.9mA current.

Quadrature signals can be also produced by cross-coupling two VCOs. The operation principle of the Series QVCO has been presented based on circuit analysis. It has been

shown that by putting the coupling transistors in series with switching transistors, the quadrature signals could be generated intrinsically. A Parallel QVCO and a low power Series-QVCO have been designed and fabricated. The Series QVCO removed the tail current of the coupling transistors, and by using the current-use technique, a low power design has been achieved. The frequency tuning range of the S-QVCO was from 2.33 to 2.589GHz. The S-QVCO produced 240mV output amplitude with only 1.5mA current consumed, which is very low-power consuming compared to other state-of-the-art designs. The Parallel QVCO can provide wide frequency tuning range by using both the varactor tuning and coupling coefficient tuning mechanisms. Its measured output frequency was from 2.247GHz to 2.649GHz, and it provides 240mV output amplitude with maximum 3.4mA current consumption. The Cascode QVCO has also been investigated. It consumed very low power, but its performances on I/Q matching, frequency tuning range and phase noise still need to be improved.

Chapter 5 describes a low-power low-phase noise eight-phase/quadrature dual-band VCO operating in 2.5GHz and 5.0GHz frequency bands has. The dual-band VCO uses the frequency doubling method to generate the higher band signals from the lower band signals, and it shows improved phase noise FOM compared to other works. The VCO has been implemented in 0.18 μ m CMOS technology, and its measured frequency was from 2.23GHz—2.68GHz and 4.46GHz—5.36GHz, which covered the most popular ISM bands. The measured phase difference between the I/Q signals is 90°/89° for the lower band higher band respectively. The phase noise FOM is -189.4dB/-185.1dB, while draining 2mA/5.8mA from 1.5V power supply.

6.2 Recommendations

The phase noise is an important parameter in VCO/QVCO designs. With a proper design, noise from the active devices in the VCO/QVCO can be minimized. Indeed, the active devices are present only to replenish the lost energy in the resonant tank. They cannot improve the overall Q of the circuit. It has been shown that a substantial improvement in phase noise can be achieved by implementing the resonator tank with a high Q [66]. The improvement on the Q of inductors will also help to save the current consumption. In [66] and [90] it was shown that the Q of the inductor could reach about 100 in theory for gold bond wire inductor. However, this method is costly and it is susceptible to the effect of the contact resistance and other parasitic, which will reduce the Q significantly. Another method for improving the Q of the resonator tank is through crystal-like inductance-capacitance tank [91]. However, this does not help to improve the Q due to the requirement that all the inductors must be integrated on-chip. More work has to be done in order to provide a resonator tank with high Q that can be easily integrated.

Varactors with higher Q and wider tuning range are also needed to alleviate many problems in wide-band VCO/QVCO design.

As described in chapter 4, the cascode QVCO has the advantage of super low power consumption. However, its performance is limited due to the reduced voltage headroom, and the I/Q signals are not well-matched because of different DC bias conditions for the two VCOs. Techniques need to be explored to balance the two VCOs

to get good I/Q signals. Automatic gain error control or phase error control circuits can be implemented to further improve the I/Q signal matching.

Finally, for the dual-band QVCO to be integrated in a dual band transceiver system, switches are needed to select between the two bands. Non-ideal switches will let the un-wanted signal leak to the output, therefore the design of high performance switches that can transmit high frequency signal without distorting it is desired, and this presents a challenge to the circuit designers.

Author's Publications

J. Xie, M. A. Do, K. S. Yeo and C. C. Boon, "Analysis and Design of RC Polyphase Network for Quadrature Signal Generation in the 2.45GHz ISM Band", Proc. *IEEE International Symposium on Integrated Circuits (ISIC-2007)*, Singapore, 26-28 Sep 2007.

J. Xie, M. V. Krishna, M. A. Do, K. S. Yeo and C. C. Boon. "A Low Power Fully Programmable 1MHz Resolution 2.4 GHz Frequency Synthesizer", *IEEE BioCAS 2007*, Canada, Nov. 2007.

M. V. Krishna, J. Xie, M. A. Do, C. C. Boon, K. S. Yeo, and Aaron V. Do, "A 1.8V 3.6 mW 2.4 GHz Fully Integrated CMOS Frequency Synthesizer for IEEE 802.15.4", IFIP VLSI-SOC 2010, Complutense University of Madrid, Spain, 27-29 September 2010.

M.Vamshi Krishna, J.Xie, M.A.Do, C.C.Boon, K.S.Yeo and Aaron V.Do, "A 1.8-V 3.6-mW 2.4-GHz Fully integrated CMOS Frequency Synthesizer for IEEE 802.15.4", *Book Chapter, VLSI-SOC 2010, Springer publications*, Accepted.

J. Xie, M. V. Krishna, M. A. Do, K. S. Yeo and C. C. Boon "A Low-Power Low-Phase Noise Dual-Band Eight-phase/Quadrature VCO", submitted to *IEEE Transactions on VLSI Systems*.

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