Ultra wideband amplifier and pulse synthesizer design

Fang, Chao

2011

Chao, F. (2011). Ultra wideband amplifier and pulse synthesizer design. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/46512>

<https://doi.org/10.32657/10356/46512>

**ULTRA WIDEBAND AMPLIFIER AND PULSE
SYNTHESIZER DESIGN**

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A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2011

STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

Date

Chao Fang

DEDICATION

To

My Supervisor

And

My girlfriend and my parents

ACKNOWLEDGEMENTS

First of all, I would like to express my sincere thanks to the Positioning and Wireless Technology Center (PWTC) and A*STAR SERC for the financial support during the duration of my studies in School of Electrical and Electronic Engineering, Nanyang Technological University (NTU).

Next, I am very grateful to Dr. Law Choi Look, my project supervisor for his knowledge, vision and kindness. It has always been enjoyable for me to work under his continual guidance, assistance, patience and continuous motivation. I have learned a lot from him not only in research but also in life. And special thanks to him for providing me with the chance to network with both overseas researchers and people from industry. I would also like to give my special thanks to Prof James C. M. Hwang of Lehigh University, USA for his valuable time and efforts to review the draft papers.

I would also like to thank the staff in PWTC, Ms. Chai Ooy Mei and Ms. Than Thida for creating a smooth research environment and providing valuable supports to me.

I have benefited greatly over the years from interactions with my friends in NTU, especially those from PWTC. I am grateful to them for kindly helping me in study and life in NTU.

Last but not the least I would like to thank my parents and my dear Zhang Nan, for their forever love and support, whenever and wherever they are.

ABBREVIATIONS

BPF	Bandpass Filter
CSSDA	Cascaded Single-Stage Distributed Amplifier
DWS	Direct Waveform Synthesis
DLL	Delay Lock Loop
DOD	Department of Defence
FCC	Federal Communications Commission
HBT	Heterojunction Bipolar Transistor
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LPF	Low Pass Filter
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
PRF	Pulse Repetition Frequency
pHEMT	Pseudomorphic High Electron Mobility Transistor
RF	Radio Frequency
UWB	Ultra Wideband
SNR	Signal to Noise Ratio
VCO	Voltage Controlled Oscillator
WPAN	Wireless Personal Area Network

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SUMMARY

The objective of this Ph.D. dissertation is to describe the design and implementation of two key components for ultra-wideband (UWB) wireless system. The first is a high gain and low noise amplifier (LNA) for the UWB receiver. The second is a novel distributed UWB pulse synthesizer for the UWB transmitter.

First, the background knowledge on UWB wireless system is presented. Literature review on various broadband circuit techniques such as the reactively matched circuit technique, feedback circuit technique, lossy match circuit technique and distributed circuit technique are conducted. Various distributed amplifier topologies such as the cascode distributed amplifier, capacitively-coupled distributed amplifier and cascaded single-stage distributed amplifier are also discussed. Previous published UWB LNA and Federal Communications Commission (FCC) compliance UWB pulse generation circuits are reviewed and the gaps are identified which forms the author's research work.

Subsequently, a 3.1-10.6 GHz UWB two-stage low noise amplifier based on 0.15- μm pHEMT technology is presented. The size of the fabricated UWB LNA is $0.9\text{ mm} \times 2.5\text{ mm} = 2.25\text{ mm}^2$. The first stage of the LNA was designed by employing a resistive shunt feedback topology together with 2 T sections low pass structure in order to match to a 50-ohm antenna. At the same time this topology will

improve the noise performance compared to the distributed input stage. The second stage is implemented in common source configuration in order to achieve higher power gain compared to common gate configuration. Finally, resistive output matching network is used to drive an external 50-ohm antenna. Current sharing among the transistors of the two stages is employed to reduce power consumption. Frequency domain measurement results show that the 3.1-10.6 GHz 0.15- μm pHEMT MMIC amplifier has state of the art performance consuming only 12.9 mW of power. The power gain is 12.5 dB with gain flatness of ± 0.5 dB, and noise figure is below 4.0 dB. The input P_1 dB compression point of the designed UWB LNA at 7 GHz is -20.5 dBm. The input third-order intercept point at 7 GHz is -10.4 dBm. It has excellent input and output return loss of better than 12 dB and 15 dB respectively except at the high end of the band. Group delay is around 184 pS ± 28 pS, coupled with flat gain performance, resulting in very good pulse response.

A practical way to characterize the degree of pulse distortion introduced by the amplifier is developed. A FCC compliance UWB pulse is used as the characterization source. The amplifier pulse response is measured using a time domain sampling oscilloscope with delays and losses of cables and probes corrected in frequency domain. The correction procedure is verified by using a “through” standard. The similarity between the input and output pulses of the amplifier is quantified by a correlation coefficient. The characterization results of the amplifier show correlation coefficient of higher than 90% up to an input peak to peak pulse

voltage of 108 mV. Further investigations show that high pass filtering at the output of the amplifier can be used to improve the correlation coefficient at high input pulse levels.

The second part of the thesis focuses on the development of a novel UWB pulse synthesizer based on distributed amplifier topology. The basic concept is to combine several delayed Gaussian pulses with both positive and negative polarities to form an UWB pulse. The center frequency and -10 dB bandwidth of the output UWB pulse can be designed by varying the delay between each pulse and the number of delayed Gaussian pulses. Compared to other UWB pulse-formation methods, the synthesizer is capable of higher output power and higher efficiency. The frequency domain characteristic of the UWB pulse synthesizer is analyzed for its center frequency and -10 dB bandwidth. A prototype synthesizer utilizing 0.25- μm pHEMT is designed for center frequency of 4.0 GHz and bandwidth of 1.9 GHz. The size of the fabricated UWB pulse synthesizer is 20 mm x 30 mm. It consumes 1 mA current at 3 V supply with high energy efficiency of 17% at 10 MHz pulse repetition frequency (PRF). With a 1.5-V 100-ps width Gaussian pulse applied at the input, the output of the UWB pulse synthesizer is 4.5 V peak to peak amplitude into a 50- Ω load and the full width half maximum pulse duration is 1.0 ns. Approaches to maintain high efficiency by scaling the supply voltage for different input amplitudes and pulse-repetition frequencies have also been verified experimentally. With a 2-V 100-ps Gaussian input and a 5-MHz PRF, The power supply was scaled from 3 V to

5 V. The output peak-to-peak voltage is 6.4 V and the full width at half maximum remains at 1.0 ns. The spectrum remains the same in compliance with the FCC mask. The measured current consumption is 0.8 mA, which corresponds to an efficiency of 13%.

Finally the high peak power monolithic microwave integrated UWB pulse synthesizer design is discussed. The mechanism of the power limitation by employing the concept of HBT safe operation area is discussed. And the guideline to bias HBT transistors in different levels in order to accommodate different Gaussian input levels and thereby to achieve different output power levels is presented. The simulation results show that the HBT UWB pulse synthesizer has the amazing potential to generate about 12.5-V peak to peak amplitude UWB pulse with power efficiency as high as 27% in lower UWB band (3-5 GHz). And the similar simulation results for higher UWB band (6-10.6 GHz) and full UWB band (3.1-10.6 GHz) are also presented.

CHAPTER 1

Introduction

1.1 Background

Ultra-wideband (UWB) technology offers an unprecedented opportunity to impact the future communication world. The wide available bandwidth, the wide scope of the data rate/range trade-off, the potential of low-cost and low power circuit and the ability to resolve multi-path components present a unique reason for UWB systems to receive considerable interest recently [1]-[8]. And at the same time, the UWB technology offers a promising solution to improve RF spectrum utilization by

allowing new services to coexist with current radio systems with minimal or no interference [9]-[15]. This coexistence brings the advantage of avoiding the expensive spectrum licensing fees that could lead to low cost operation.

Ultra-wideband communication technique is different from all other communication techniques because it employs extremely narrow RF pulses to communicate between transmitters and receivers. It is not a new technology. In fact, in 1893 Heinrich Hertz used a spark discharge to produce electromagnetic waves for his experiment. These waves would be called colored noise today. Spark gaps and arc discharges between carbon electrodes were the dominant wave generators for about 20 years after Hertz's first experiments [16]. In 1901, Guglielmo Marconi employed the UWB technology to transmit Morse code sequences across the Atlantic Ocean using spark gap radio transmitters [17]. Unfortunately, the benefit of a large bandwidth and the capability of implementing multi-user systems provided by electromagnetic pulses were never considered at that time. Approximately fifty years after Marconi, the development of the sampling oscilloscope in the early 1960s and the corresponding techniques for generating sub-nanosecond baseband pulses speed up the development of UWB technology. After that time, the main focus moved from measurement techniques to develop radar and communications devices. In particular, radar was given a lot of attention because of the accurate results that could be obtained. The low-frequency components were useful in penetrating objects, and ground-penetrating radar was developed [18]-[19]. At that

time, UWB was recognized by other terms, such as carrierless, impulse radio, and baseband pulse. In 1973, the first US patent was awarded for UWB communications [20]. In 1989, the term ultra wideband was introduced by the U.S. Department of Defense [21]. However, before the 1990s, this technology was restricted to military and Department of Defense (DoD) applications under classified programs such as highly secure communications. Only in the late 1990s, the move to commercialize UWB communication devices and systems were beginning. Companies such as Time Domain [22] and in particular startups like XtremeSpectrum [23] were formed around the idea of consumer communication using UWB. And after the recent advancement in microprocessor and fast switching in semiconductor technology, UWB has been made ready for commercial applications [24]-[25].

In February 14, 2002, the U.S. FCC issued the first report and order that authorizes the unlicensed commercial deployment of UWB technology under a strict power control in 7.5 GHz spectrum [26]. The FCC has assigned conservative spectral masks between 3.1 GHz and 10.6 GHz for commercial UWB devices - that is, -41.3 dBm/MHz. And based on the FCC regulations, UWB devices are classified into three major categories: communications, imaging, and vehicular radar. Starting from that moment on, UWB systems have gained high interest among researchers and companies. There are two main developing streams of UWB system currently, multi-band OFDM (MB-OFDM) and impulse-based radio (IR) UWB system. The MB-OFDM UWB system is mainly used for high speed communication systems,

while IR UWB system is mainly used for imaging and vehicular radar applications.

The thesis focuses on the IR UWB system.

(a)

(b)

Fig. 1.1. FCC UWB spectrum mask (a) indoor (b) outdoor

For communication devices, FCC has assigned different spectral mask for indoor and outdoor UWB devices. The spectral mask for outdoor devices is 10 dB lower than that for indoor devices, between 1.61 GHz and 3.1 GHz and above 10.6 GHz. Fig. 1.1(a) and Fig. 1.1(b) show both UWB indoor and outdoor Spectrum Mask [27]. The average power limit in the UWB band is -41.3 dBm/MHz.

And the spectral mask allocation in other countries is shown in Fig. 1.2 [28]-[29].

Fig. 1.2. Spectral mask allocation in other countries [28]

1.2 Features of IR UWB System

Instead of traditional sine waves, UWB system sends several coded pulses per second across an ultra-wideband of spectrum and it is characterized by ultra-short

pulses, low power, immunity to interference, precise range, low cost, high data rate and precise localization capability.

1.2.1 Ultra-short duration pulses

Ultra-Wideband radio transmits the information using very narrow pulses (in the order of a fraction of a nanosecond) with very small duty cycle. The signal, in this way, extends over a large bandwidth. Both monocycle and “multi-cycle” nanosecond pulse can serve as UWB pulse. In fact, any form narrow pulse can serve as UWB pulse. But the nice waveform shape, for example, monocycle and “multi-cycle” offers flexibility for different modulation techniques. Here Gaussian monocycle pulse in both time and frequency domain are plotted in Fig. 1.3 as the example. Here the peak-to-peak amplitude of the Gaussian monocycle pulse in the time domain is normalized to 1 V and the main lobe in the frequency domain is normalized to 0 dB. The multi-cycle pulse has narrower bandwidth compare to the monocycle pulse case.

Fig. 1.3. A Gaussian monocycle pulse in both time and frequency domains

1.2.2 Low power spectral densities

UWB systems transmit information at Effective Isotropic Radiated power (EIRP)

level as low as -41.3 dBm/MHz across 3.1 GHz-10.6 GHz. Such power restriction allows UWB systems to reside below the noise floor of a typical narrowband receiver and enables UWB signals to coexist with current radio services with minimal or no interference. Fig. 1.4 shows this situation [30].

Fig. 1.4. Spectrum of UWB system compared with existing systems [30]

1.2.3 Large channel capacity

One of the major advantages of the large bandwidth for UWB pulses is improved channel capacity. Channel capacity, or data rate is defined as the maximum amount of data that can be transmitted per second over a communication channel. The large channel capacity of UWB communication systems is evident from Shannon's capacity formula

$$C = B \log_2(1 + SNR) \quad (1.1)$$

Where C represents the maximum channel capacity, B is the bandwidth, and SNR is the receiver signal-to-noise ratio. Therefore, having 7.5 GHz bandwidth available for UWB signals, a data rate of Gbps can be expected. However, due to the FCC's power limitation on UWB transmissions, such a high data rate is available only for short ranges, up to 10 meters. This makes UWB systems perfect candidates for short-range, high-data-rate wireless applications such as wireless personal area networks (WPANs). On the other hand, such a high bandwidth allows the trade off between data rate and range. This trade-off makes UWB technology ideal for a wide array of applications in military, civil, and commercial sectors.

1.2.4 Excellent multi-path interference immunity

The combination of larger spectrum and lower emission power of pulsed data means that ultra-wideband causes less self interference than narrowband radio designs while yielding low probability of detection and excellent multi-path immunity. As illustrated in Fig. 1.5 [31], monocycle travels from a transmitter to a receiver along two paths. Since the paths are of two different lengths, the second pulse will arrive after the first pulse. A receiver could lock on either pulse and receive the stronger signal. Alternatively, the energy from both signals may be added increasing the received signal-to-noise ratio.

Fig. 1.5. UWB multi-path immunity [31]

1.2.5 Low Cost

UWB transmission is carrierless, meaning that data is not modulated on a continuous waveform with a specific carrier frequency, as in narrowband and wideband technologies. This ability to directly modulate a pulse onto an antenna is perhaps as simple a transmitter can get, leading many manufacturers to be excited by the possibilities for extremely cheap transceivers. This is possible by eliminating many of the components required for conventional narrowband transmitters and receivers. For example: RF/IF conversion stages and local oscillators. Hence UWB systems are much less complex, allowing for significantly lower cost and smaller size.

1.2.6 Precise Localization

The use of short pulse RF waveforms provides inherent precision for time of arrival measurements. And a large bandwidth improves reliability, as the signal contains different frequency components, which increases the probability that at least some of them can go through or around obstacles. Furthermore, a large absolute bandwidth offers high resolution radars with improved ranging accuracy. Hence the UWB technology has precise localization capability.

1.3 Motivation and Objectives

Great interest in UWB wireless communication system has been aroused from both academic and industrial areas and numerous UWB devices have been designed and implemented after the FCC released the unlicensed use of UWB devices in the frequency band 3.1 -10.6 GHz. There are two main foreseen applications. One application is short range high data rate communication and the other application is longer range low data rate communication coupled with precision localization capabilities [4]-[5].

As an essential component for UWB wireless applications, a high performance low noise amplifier (LNA) is highly demanded in increasing the communication range. Study shows that an improvement of 2.0 dB in Noise Figure (NF) of the receiver results in range increase of around 1.6 times. Hence in order to increase the UWB

wireless system coverage, a high gain and low noise amplifier becomes one of crucial design tasks.

To date, there are many different UWB regulatory approvals around the world as stated in Fig. 1.2. The US Federal Communications Commission (FCC) has utilized the 3.1-10.6 GHz band with lower band of 3-5 GHz and upper band of 6-10.6 GHz [26]; the European Communications Commission (ECC) has recently announced support for the 6-8.5 GHz band, while Japan targets at the 7-10 GHz band. Hence for longer range low data rate communication system, generating the UWB pulse that has high peak power at low power consumption and at the same time with desired center frequency and -10 dB bandwidth meeting the spectrum regulation is a critical task.

With the motivation discussed above, the goal of this dissertation is to develop a high gain low noise amplifier and a UWB pulse synthesizer which is capable to generate the UWB pulse with high peak power at low average power consumption and at the same time with desired center frequency and -10 dB bandwidth meeting the spectrum regulation.

1.4 Major Contributions

The research outcome achieved in this PhD. Dissertation represents the design of two key components for UWB wireless system. One is a high performance UWB Low noise amplifier and the other one is a high efficiency and high peak power UWB pulse synthesizer.

The major contributions of this dissertation are listed as follows:

- A 3.1-10.6 GHz UWB two-stage pHEMT low noise amplifier based on 0.15- μm pHEMT technology was designed. The size of the fabricated UWB LNA is 0.9 mm x 2.5 mm = 2.25 mm². It achieves state of the art performance consuming only 12.9 mW of power. The power gain is 12.5 dB with gain flatness of ± 0.5 dB, and noise figure is below 4.0 dB across 3.1-10.6 GHz. The input P_{1dB} compression point at 7 GHz, is -20.5 dBm. The IIP3 point at 7 GHz is -10.4 dBm. It has excellent input and output return loss of better than 12 dB and 15 dB respectively except at the high end of the band. Group delay is around 184 pS $\pm$ 28 pS, coupled with flat gain performance, resulting in very good pulse response.
- A new practical way to characterize the degree of pulse distortion introduced by the UWB Low noise amplifier is discussed. The real FCC compliance UWB pulse is used as the characterization source. The pulse response characterization procedure is carried on the author designed UWB LNA by

using a time domain sampling oscilloscope with the delays and losses of cables and probes corrected in frequency domain. The correction procedure is verified by using a “through” standard. The exact similarity of the input and output pulses of the UWB LNA is qualified by the correlation coefficient of the input and output pulses.

- A novel ultra-wideband (UWB) pulse synthesizer is proposed, which uses a distributed amplifier to combine Gaussian pulses of different polarities, amplitudes and delays. The center frequency and bandwidth of the synthesized pulse can be adjusted by varying the number of the Gaussian pulses and the length of the delays between them. Compared to other UWB pulse generators, the present synthesizer is capable of higher peak power and higher efficiencies. The frequency domain characteristic of the proposed UWB pulse synthesizer method is analyzed extensively to show the capability of tuning the center frequency and -10 dB bandwidth of the output pulse. Using 0.25- μm pHEMTs, a prototype synthesizer has been designed and fabricated with a center frequency of 4.0 GHz and a bandwidth of 1.9 GHz. Under a Gaussian input pulse of 1.5 V and 100 ps, the synthesizer outputs into 50 Ω a 1 nS pulse of 4.5 V_{pp} . At a pulse-repetition frequency of 10 MHz, the synthesizer consumes 1 mA at 3 V with 17% efficiency. Approaches to maintain high efficiency by scaling the supply voltage for different input amplitudes and pulse-repetition frequencies have also been verified experimentally.

- The high peak power MMIC UWB HBT pulse synthesizer design is discussed.

The power limitation mechanism is discussed by employing the concept of HBT safe operation area. The guideline to bias HBT transistors in different levels to accommodate different Gaussian input levels and to achieve different output power levels is presented. Three design examples by using the commercial HBT are presented.

1.5 Organization of the Dissertation

The dissertation is organized as follows.

Chapter 2 gives a literature review on the various broadband amplifier techniques. And then the recent published Ultra wideband low noise amplifiers and FCC compliance UWB pulse generation methods are discussed. As a result of the literature review, the gaps of the author's research work are identified.

Chapter 3 focuses on the MMIC circuit design and analysis of the low noise amplifier based on 0.15- μm pHEMT technology. First, the frequency domain measurement results including S parameters, noise figure, group delay and P1dB compression point are presented. Subsequently, a practical way to characterize the degree of pulse distortion introduced by the designed UWB low noise amplifier is developed. A FCC compliance UWB pulse is used as the characterization source.

The time domain characterization results are also presented. The similarity between the input and output pulses of the amplifier is quantified by a correlation coefficient. The characterization results of the amplifier show correlation coefficient of higher than 90% up to an input peak to peak pulse voltage of 108 mV. Further investigations show that a simple high pass filter at the output of the amplifier can be used to improve the correlation coefficient at high input pulse levels.

Chapter 4 introduces a novel UWB pulse synthesizer based on distributed amplifier topology. First, the method of UWB pulse synthesizer was introduced. Following that, the frequency domain characteristic of the proposed UWB pulse synthesizer method is analyzed extensively to show the capability of tuning the center frequency and -10 dB bandwidth of the synthesized pulse. Then the analysis and design of the prototyped circuit is presented. Measurement results on prototyped circuit are also reported. Approaches to maintain high efficiency by scaling the supply voltage for different input amplitudes and pulse-repetition frequencies are presented and verified experimentally.

Chapter 5 presents the high peak power MMIC UWB HBT pulse synthesizer designed. The power limitation mechanism is discussed. The guideline to bias HBT transistors in different levels to accommodate different Gaussian input levels and to achieve different output power levels is presented. Design examples by using the commercial HBT are presented.

Finally, conclusions and future directions are made in Chapter 6.

CHAPTER 2

Literature Review

Broadband circuit techniques are important for the circuit design of UWB wireless system. Hence this chapter starts with reviewing the various broadband circuit techniques. Previous publications on the UWB low noise amplifiers and the FCC compliance UWB pulse generators are reviewed. Finally the research gaps for them are identified and those gaps form the author's research work.

2.1 Various Broadband Circuit Techniques

The most popular and well-established circuit techniques employed in the design of broadband amplifiers that are realized in hybrid and monolithic technologies are:

- Reactively matched circuit technique
- Distributed circuit technique
- Feedback circuit technique
- Lossy match circuit technique

In the following sections 2.1.1, 2.1.2, 2.1.3 and 2.1.4, the various circuit techniques are discussed.

2.1.1 Reactively Matched Amplifier

The input and output matching networks of the reactively matched amplifier are formed by the lossless reactive networks, with either lumped- or distributed-elements. The configuration of the reactively matched amplifier is shown in Fig. 2.1. Due to the reactively matched input and output circuits, the reactively matched amplifier is also termed as the lossless matched amplifier. The first reported reactively matched 2-18 GHz power amplifier employing GaAs MESFET devices [32] was designed using wideband impedance transformers

realized in MIC. The main deficiency of this amplifier design was that the terminal voltage standing wave ratios were very poor under small-signal conditions.

Fig. 2.1. Reactively matched amplifier circuit configuration

The matching circuits shown in Fig. 2.1 are used to accomplish gain compensation by selectively creating reflections between the matching networks and the active device. Because the matching networks are composed exclusively of reactive elements, the maximum gain, minimum noise figure, and maximum power output can be achieved for a given transistor with properly designed matching networks. In practice, the maximum gain can be achieved by optimizing the input matching circuit, and the output matching circuit can be optimized to achieve maximum output power and hence maximum power added efficiency.

The disadvantage of the reactively matched amplifier is its relatively poor

impedance matching. Although the lossless matching circuits provide the desired match over a narrow band of frequencies, the matching at other frequencies is degraded. The good ultra wideband matching is hard to be achieved. This can be improved by employing isolators in the case of a single-ended design or hybrid couplers as combiners and dividers in the case of balanced amplifiers. In the single-ended case, this will result in extra cost and an increase in the overall size of the amplifier module. The balance amplifier approach results in an increase in output power of 3 dB, however, this comes at expense of double the dc power consumption. Moreover, balanced amplifier requires quadrature hybrid couplers that are either narrow band or, if they are wideband, they are multi-sectional and very large. Thus, they are not amenable to integration.

2.1.2 Distributed Amplifier

2.1.2.1 General Information

Distributed amplifier has been widely employed for broadband application [33]-[44]. The problem of achieving a broadband match to the transistor input and output impedance is overcome by incorporating the input and output capacitances of a number of transistors into artificial transmission-line structures. The amplifier consists of an input line, incorporating the input capacitances of the transistors, and an output line incorporating the output capacitances. The signal on the input line is amplified and feed into the output line. As the result of this arrangement, the amplifier can operate over a very broad frequency range. The low frequency range

of the amplifier is determined by the bias network and the high frequency range is the cut-off frequency of the artificial transmission lines.

The technique suddenly became very popular with the realization that GaAs MESFETs could be used in monolithic distributed amplifier to achieve decade bandwidth microwave amplification [34]. Its real strength is that with MMIC technology the distributed amplifier can achieve extraordinarily wide bandwidth with a simple circuit topology that is insensitive to process variations.

In the most common configuration, the capacitances become the shunt capacitances in a constant-K low pass filter (LPF) ladder network. A single section constant-K LPF ladder is shown in Fig. 2.2(a). In the case of the FET distributed amplifier there is a gate-line and a drain-line, as shown in Fig. 2.2(b). The input signal travels down the gate-line, exciting each transistor in turn, before being absorbed by a terminating resistor. The trans-conductance of the transistors amplifies the signal and feeds it into the drain-line. If the phase velocities in the gate-line and drain-line are roughly equal, then the signals from each transistor will add constructively at the output port. At high frequencies the signals will largely cancel out at the reverse end of the drain-line, but this is not the case at low frequencies. A drain-line termination absorbs any undesired signals present at the reverse end.

Fig. 2.2. FET distributed amplifier: (a) a single section of constant-K Ladder (b) circuit schematic

The basic design of a FET distributed amplifier can be carried out very easily by considering the characteristics of the constant-K ladder. The characteristic impedance of the artificial transmission line is given by

$$Z_o = \sqrt{\frac{L}{C}} \quad (2.1)$$

and its cut-off frequency is given by

$$f_c = \frac{1}{\pi\sqrt{LC}} \quad (2.2)$$

It is evident that for a given Z_o (normally 50 ohm) and a given transistor capacitance, the inductance, L , and cut-off frequency f_c , are both fixed. Also, since the gate-source capacitance is considerably larger than the drain-source capacitance, it will determine the cut-off frequency and thus the maximum frequency of operation. A higher cut-off frequency could be achieved by using smaller gate-width FETs with a lower C_{gs} , but the trans-conductance, g_m , would also be correspondingly lower, giving less gain. Likewise, a larger device has higher g_m and gives more gain, but the higher C_{gs} lowers the cut-off frequency.

In the case of ideal lossless constant-K lines, it has been shown [35] that a distributed amplifier with n sections has a power gain given by

$$G = \frac{n^2 g_m^2 Z_o^2}{4} \quad (2.3)$$

In the ideal case, the gain can be increased by adding more sections. However, in practice the number of sections that can be used is limited by gate and drain-line losses.

Fig. 2.3. Simplified MESFET equivalent circuit

Referring to the simplified MESFET equivalent circuit in Fig. 2.3, the resistance R_i of each FET will absorb some of the signal traveling down the gate-line, and the resistance R_{ds} will absorb some of the signal traveling up the drain-line. It is found that the drain-line loss is essentially constant with frequency, whereas the gate-line loss increases rapidly with frequency and is the more

dominant limitation in most cases. The result of gate-line loss is the successive FETs along the gate-line receive a steadily decreasing level of input signal. The effect is so pronounced that after a certain number of sections the input signal becomes so weak that there is no benefit in adding more sections: there is found to be an optimum number of sections for given levels of gate and drain-line loss. Additional stages beyond this optimum number add virtually no signal to the drain-line because their input signal has been attenuated so much. Furthermore, these additional sections add more and more drain-line loss, so they are actually detrimental to the performance.

A more accurate gain expression is given by equation (2.4). [35].

$$G = \frac{g_m^2 Z_o^2 [\exp(-A_g n) - \exp(-A_d n)]^2}{4 (A_g - A_d)^2} \quad (2.4)$$

Where A_g is the gate-line attenuation, A_d is the drain-line attenuation.

The optimum number of devices N_{opt} that maximizes gain at a given frequency is given by the expression (2.5). [36].

$$N_{opt} = \frac{\ln(A_d / A_g)}{A_d - A_g} \quad (2.5)$$

In the above description, it has been assumed that the gate- and drain-lines have equal characteristic impedance and equal phase velocities. For the constant-K topology this can only be achieved if C_{gs} and C_{ds} are equal. However, in practice C_{ds} is much smaller than C_{gs} , and so steps must be taken to equalize the gate and drain-line with C_{ds} , in order to make the overall capacitance equal to C_{gs} . One common practice is to add a capacitor in parallel with the drain capacitance of each transistor in Fig. 2.3, which is shown in Fig. 2.4(a). However, this brute force approach is far from optimum and considerably higher performance can be achieved by employing m-derived sections on the drain line. Fig. 2.4(b) shows the topology.

(a)

(b)

Fig. 2.4. Gate and drain-line velocity compensation using (a) a capacitor parallel with drain capacitance of the transistor (b) an m-derived section

The following sections will present various modified distributed amplifiers based on the distributed amplification concept.

2.1.2.2 Various Modified distributed Amplifier

➤ Cascode distributed amplifier

The cascode arrangement of two FETs provides high gain, high output resistance and high reverse isolation. In addition, the maximum output voltage swing is

higher than for a single FET because the common-gate FET's gate is grounded at AC. As a result of these advantages, the cascode FET is often used in distributed amplifier, as shown in Fig. 2.5.

Fig. 2.5. The cascode distributed amplifier

➤ The capacitively-coupled distributed amplifier

A further limit to the achievable output power is the fact that the large gate-width transistors, suitable for high power, have a high C_{gs} , which leads to a reduction in bandwidth. In addition, gate-line loss means that the first FET on the gate-line will

receive considerably greater input voltage swing than the others further down the gate-line. Hence, this FET will go into gain compression too early. A neat solution to these limitations is to capacitively couple the FETs to the gate-line [37], as shown in Fig. 2.6. This technique allows larger FETs to be employed without lowering the cut-off frequency of the gate-line. In addition, if the coupling capacitors C_1 to C_n are varied, the effect of the gate-line loss can be accommodated so that each FET has the same gate voltage swing applied. In other words, the first FET has a relatively small coupling capacitor because the input signal is large, whereas the last FET on the gate-line is almost directly coupled to the gate-line with a large coupling capacitor. But with the capacitive coupling, the gain of the amplifier is reduced because of the potential divider action across C_{gs} and the coupling capacitor. The coupling capacitors are shunted with high value resistors R_{bias} in order to allow the DC gate bias to reach the gates.

Fig. 2.6. The capacitively-coupled distributed amplifier

➤ Cascade single-stage distributed amplifier (CSSDA)

Although the conventional distributed amplifier has the desirable attributes of flat gain and good terminal match over a wide frequency range, it is not efficiency in terms of gain and output power, and it requires multiple devices leading to a relatively large gain module. These drawbacks stimulated work for improving the design of conventional distributed amplifiers in terms of realizing a more compact circuit using fewer devices to produce high level of gain. Minnis [38] described the principles of the cascable amplifier for the first time.

Ben Y. Banyamin [39] reported a hybrid broadband distributed amplifier based on four cascaded single-stage distributed amplifiers (4-CSSDAs). The available gain produced by the 4-CSSDAs is significantly higher than conventional distributed amplifier using the same number of active devices. The measurement results show excellent performance with $39 \text{ dB} \pm 2 \text{ dB}$ gain, good input and output matching, and flat group delays.

Fig. 2.7 shows the cascaded single-stage distributed amplifier arrangement. In the cascaded single stage distributed amplifier arrangement, the idle drain termination is omitted for stages other than the last stage. With no idle drain termination, the voltage swing across the input gate of the next active device is increased, which consequently enhances the amplifier's gain. Kuo-Liang Deng [40] mixes the concepts of conventional distributed amplifier and the cascaded single-stage distributed amplifier and comes out with a novel GaAs pHEMT MMIC distributed amplifier. It achieved $22 \text{ dB} \pm 1.5 \text{ dB}$ gain from 0.1-40 GHz. It produced a gain-bandwidth product of 503 GHz, which is the highest among all reported GaAs-based distributed amplifier. The flat group delay also demonstrates the feasibility of this design for future digital optical communications and broad-band pulse applications.

Fig. 2.7. Cascaded single-stage distributed amplifier arrangement

2.1.3 Broadband Feedback Amplifier

The amplification of microwave signals employing amplifiers, which only require a single device to achieve the multi-octave bandwidth, was proposed by Niclas, et al [45]-[46]. These negative feedback amplifiers are based on the near ideal voltage controlled current source characteristics of the microwave FET device

operated at low frequencies. The feedback amplifier, shown in Fig. 2.8, employs shunt feedback between the gate and drain of the active device used in the circuit.

The major advantages of the feedback amplifier are:

- The circuit is less complex compared with the reactively matched and distributed amplifier circuits and therefore is easier to realize.
- The amplifier can provide higher power added efficiency performance when compared with the conventional traveling wave amplifiers.
- The amplifier offers a cost effective multi-octave bandwidth amplifier design.
- It has excellent performance in achieving flat gain and unconditional stability, and it provides very good input and output match.
- The amplifier can be realized in both hybrid MIC and MMIC circuit technologies.
- It provides lower distortion and sensitivity to active device variations.

The main disadvantage of this type of amplifier is the erosion of its output power and noise figure over the lower end of the frequency band due to loss associated with the feedback resistor.

Fig. 2.8. Feedback amplifier circuit topology

The feedback path consists of three elements, R_{fb} , L_{fb} and C_{fb} . The value of the feedback R_{fb} controls the gain and bandwidth of the amplifier. The gate inductance L_g , the drain inductance L_d , and the feedback inductance L_{fb} can be optimized to extend the amplifier's bandwidth [45]. The feedback inductance L_{fb} reduces the effectiveness of the negative feedback with increasing frequency. The drain inductance L_d is selected to compensate for the intrinsic drain-source capacitance of the device up to the cut-off frequency. The dc block capacitor C_{fb} is used to isolate the gate from the drain bias supply. The feedback amplifier can be very sensitive to frequency when implemented in hybrid technology. Also due to the less complex circuit, its implementation dominates in MMIC technology.

2.1.4 Lossy Matched Amplifier

The lossy matched amplifier employs resistors R_1 and R_2 at the input and output matching circuits, respectively, as illustrated in Fig. 2.9. These resistors are used to provide gain equalization (i.e flat gain response) by introducing high attenuation at low frequencies and low attenuation at high frequencies, while maintaining a good input and output matching over the desired broadband. This fact makes the amplifier suitable for cascading without the need for isolators to improve inter-stage matching, as is the case of the reactively matched amplifier. Therefore, they are relatively smaller and have lower power consumption. The amplifiers provide broadband performance at the expense of lower gain, low output power, high noise figure, and poor power added efficiency [45]. This is mainly due to losses in the resistors, which are used in the input and output matching and inter-stage matching networks.

Fig. 2.9. Lossy matched amplifier circuit configuration

2.2 Literature Review on UWB LNA and Comparative Advantage of Author's Research

2.2.1 Literature Review on UWB LNA

Recently the reactively matched UWB low noise amplifier based on CMOS technology is reported by Andrea bevilacqua [47]. Andrea expands the use of an inductively degenerated common-source amplifier, a technique widely used in narrow-band designs [48] by embedding the input network of the amplifying device in a multi-section reactive network so that the overall input reactance is resonated over a wider bandwidth. In this way, a wideband input match is achieved and, at the same time, a good noise performance is attained. The cascode configuration improves the input and output match, reverse isolation and the frequency response of the amplifier. The measurement results show that the proposed UWB LNA can achieve the minimum NF as low as 4.0 dB. But taking a closer view, we can see that the 4.0 dB NF is only achieved in a very narrow frequency range. The spot NF reaches 8 dB at 10 GHz. The highest gain can be achieved is only 10.4 dB. The very low quality factor of the integrated inductors on the silicon substrate introduces loss and noise.

Aly Ismail [49] reports another reactively matched UWB LNA based on SiGe technology. The reactive matching is achieved by using the impedance property of LC-ladder filters. The measured NF, gain and gain flatness show the high

performance of the proposed UWB LNA. But the input matching is only better than -10 dB.

Through the literature, the author finds that the input matching of the reported CMOS and SiGe reactively matched UWB LNA are both not good. Andrea bevilacqua [47] reports less than -9.9 dB input matching and Zhe-Yang Huang [50] reports less than -8.7 dB input matching by using CMOS technology. And Aly Ismail [49] reports less than -10 dB input matching by using SiGe technology. For UWB positioning, localization and ranging system, which employed both passive and active tag, the reflected pulse from the receiving antenna of the active tag may interfere with the reflected pulse (back scattering, useful signal) of the passive tag. So in order to reduce this interference, a very tough requirement is imposed on the input matching of the UWB LNA which is used for the active tag.

The distributed amplifier is believed to have a very good input matching. But the noise figure of UWB amplifier based on distributed amplifier topology is quite high. Ren-Chieh Liu [51] reports a 0.6-22 GHz broadband CMOS distributed amplifier with 4.3-6.1 dB noise figure from 1 GHz to 18 GHz. Kuan-Hung Chen [52] reports a 3.1-10.6 GHz CMOS distributed amplifier with 5-7 dB noise figure. The poor noise figure performance of the distributed amplifier is due to the 50 Ω input line termination resistor. Moreover, the power consumption of distributed amplifier is also quite high. Kambiz Moez [53] reports a 3-9.4 GHz CMOS

distributed amplifier with 30 mW power consumption.

2.2.2 Comparative Advantages of Author's Research

Hence the author designed a UWB LNA [54], where the first stage of the amplifier employs a resistive shunt feedback topology and two sections T-network to provide wideband input matching to 50- Ω antenna. The shunt feedback topology, which is mainly used for low UWB frequency band matching, is based on the broadband feedback amplifier topology. And the two sections T-network, which is mainly used for high UWB frequency band matching, is based on the reactively matched amplifier topology. This combination can narrow down the reactively match bandwidth from the whole UWB band to a portion of the UWB band. Hence a better input matching can be achieved. On the other hand, the resistive feedback topology will degrade the noise figure performance of the UWB LNA in the low frequency band, but both simulated and measurement results show that it can be controlled in the acceptable range. The inter-stage matching is based on lossy matching technique; hence the flat gain response is easy to be achieved. The lossy matching technique degrades the noise performance of the amplifier, but as the lossy matched amplifier configuration is used for the second stage of the amplifier, this degradation is not too severe. And finally the current-sharing DC bias topology is used to ensure low power consumption under the fixed 3 V battery operation. The fabricated amplifier exhibits state of the art performance consuming only 12.9 mW of DC power with power gain of 12.5 dB, ± 0.5 dB gain flatness, and 3.4-4.0 dB NF

across the whole 3.1-10.6 GHz. Input matching is better than -12.0 dB, output matching is better than -15 dB, group delay is $184 \text{ pS} \pm 28 \text{ pS}$, input 1-dB compression point at 7 GHz is -20.5 dBm and IIP3 at 7 GHz is -10.4 dBm.

2.3 Literature Review on FCC Compliance UWB Pulse Generator and Author's Novel Approach

2.3.1 Literature Review on FCC Compliance UWB Pulse Generator

Current impulse radio UWB (IR-UWB) pulse generation methods fall into six main categories. One way is to generate a pulse at base band and then up-convert to the target frequency band [55]-[58]. These carrier-based designs tend to have complex architectures, high power consumption and LO leakage due to the need of a local oscillator. For example, in [55] a very short triangle pulse is generated first. And then the generated short triangle pulse is mixed with a 4.0 GHz sine wave signal generated by a local oscillator in order to up convert the short triangle pulse into the designed frequency band. Finally the up-converted pulse is filtered and amplified on-chip before being sent to the off-chip UWB antenna. The peak to peak amplitude of the generated output pulse is only 0.26 V and the total power consumption including the power amplifier (PA), mixer and the local oscillator (LO) was 31.3 mW.

A second approach is to generate a pulse directly in UWB band [59]. In [59], a 5 ps fall time step pulse is generated from an external Picosecond Pulse Labs' pulse generator. The generated fast falling edge step pulse is filtered by a UWB band pass filter (BPF) which is implemented by broadside-coupled microstrip-coplanar waveguide structure [60]. The output pulse waveform after 1, 2, 3-sections of UWB BPF are studied in both time and frequency domain. The results show that in order to generate FCC compliance UWB pulse, at least 3-section UWB BPF is needed. The length of the 3-section UWB BPF is longer than 52.6 mm. Hence this method usually requires large band-pass filters for additional pulse shaping.

A third method is based on an ON/OFF switching operation of an oscillator [61]-[63]. For example, [62] presents the UWB pulse generator that generates the UWB pulse in the lower band of 3-5 GHz. The presented UWB pulse generator can deliver a large differential output swing of 7.2 V with 100- Ω load (which is power equivalent to 5.1 V with 50- Ω load) and at the same time consumes 224 μ A under 3.3 V power supply at 1 MHz pulse repetition frequency (PRF). However, the fast gate bias signal required to switch the buffer driver amplifier is difficult to be implemented.

A fourth method relies on the combinations of the rising and falling edges of the digital clock [64]. The UWB pulse generation consists of two blocks: A digital triangular pulse generator and an output stage driving a 50- Ω load. The digital

triangular pulse generator provides the input signal to the subsequent stages. The input digital pulse and its inverted pulse which are followed by a NAND or NOR gate generate the triangular pulse [65].

Fig. 2.10. Schematic of all digital FCC compliance UWB pulse generation circuit [65]

The NAND gate is low only when both inputs are high, and the NOR gate is high only when both inputs are low, the outputs of NAND and NOR gates are low and high at any given time, respectively. Four different polarity triangle pulses are generated at the nodes A, B, C and D shown in Fig. 2.10. Each triangular pulse is designed to have the same peak-to-peak amplitude. Finally the size and number of the inverters are used to control the delay time between the four triangle pulses in order to align the phase of the four triangle pulses correctly, as shown in Fig. 2.10.

Hence in the output stage, the four triangular pulses generated can be combined with correct delay. But in the real circuit design, the precise delay controls between the four triangle pulses are difficult to implement. The way to rely on the size and number of the inverters will be very sensitive to the process variation. And the CMOS circuit presented in [64] is only able to deliver UWB pulse with 680 mV peak to peak voltage.

Recently, a new waveform synthesis method based on high-speed digital-to-analog converter (DAC) was proposed for UWB pulse generation [66]. The method presented in [66] is to utilize DAC-based direct waveform synthesis (DWS). It has both good time and amplitude resolution. 6-bit DAC is employed to implement the task. Hence the usage of the UWB frequency spectrum (3.1 to 10.6 GHz) below 5 GHz requires ~ 8 GS/s, while ~ 16 GS/s is needed for the upper band. Such high sampling rate results in large circuit complexity and large DC power consumption at 360 mW.

The final way is to combine different delay edges with polarity control to form a short duration “logical” pulse and then filter it to obtain an UWB pulse [67]-[69]. Taking [67] as an example, the complete pulse generator architecture comprises flip-flops, a multiphase clock, combinatory logic and a balun, as depicted in Fig. 2.11. The basic concept is to combine different delayed edges by latching the flip-flops with delayed synchronous clocks so as to form a very short duration

“logical” pulse, and then to filter it, in order to generate an UWB pulse. The output pulse shape, and thus the corresponding spectrum, can be varied by acting on the delayed edge combination. In order to generate pulses in the UWB band, [67] show that the circuit should be able to produce and combine edges with precision of better than 50 ps. This precise time requirement results in large circuit complexity, which is shown in Fig. 2.11. In order to overcome the process and temperature variations, the delays needed be managed by the extra Delay Lock Loop (DLL) circuit in the receiver chip. The CMOS circuit is also only able to deliver small peak to peak voltage UWB pulse at 450 mV.

Fig. 2.11. Architecture of FCC compliance UWB pulse generator by combining different delay edges with polarity control [67]

2.3.2 Author’s Novel Approach

This paper takes a different approach from [67]-[69]. The proposed method relies on an external generated Gaussian input pulse, and then the Gaussian pulse is delayed

by the distributed circuit topology. Finally the different delayed Gaussian pulses with positive and negative polarities are combined to form an UWB pulse [70]. The capacitively-coupled distributed amplifier topology is employed to achieve the output pulse with Gaussian envelope. In the real implementation, the positive polarity pulse is generated from the reflected negative polarity pulse and then combined with the negative polarity pulse to form the UWB pulse. Compared to [67], the polarity control is eliminated. The novel circuit implemented utilizing pHEMT is able to generate 6.4 V peak to peak amplitude pulse into 50 ohms load with 2 V Gaussian input pulse.

CHAPTER 3

Ultra-wideband Low Noise Amplifier

3.1 Performance Overview

In this Chapter, a 3.1-10.6 GHz ultra-wideband (UWB) two-stage low noise amplifier based on 0.15- μm pHEMT is presented [54]. From device technology point of view, the low resistive loss between gate and source of pHEMT reduces input line loss and 0.15- μm pHEMT has better noise and gain performances than 0.25- μm pHEMT. From design point view, the first stage of the amplifier employs a resistive shunt feedback topology and two sections T-network to provide wideband input matching to 50- Ω antenna. The output matching of the second stage amplifier

and the inter-stage matching is achieved by a shunt resistive matching technique. Various inductances are used to compensate the gate-source and drain-source capacitance of the transistors to pick up the gain of the amplifier in high frequency band. The current-sharing DC bias topology is used to ensure low power consumption under fixed 3 V battery operation [50].

Table 3.1. Summary of LNA Performance and Comparison with Previous State-of-art Design

	Tech.	S_{11} (dB)	Gmax/Gmin (dB)	BW (GHz)	NFmin/NFmax (dB)	Pdiss (mW)
This work	0.15- μ m pHEMT	<-12.0	13/12	3.1-10.6*	3.4/4.0	12.9
[47]	0.18- μ m CMOS	<-9.9	9.3/- Φ	2.3-9.2 $\odot$	4.0/9.0	9
[50]	0.18- μ m CMOS	<-8.7	10.0/13.1	3.1-12.2	2.7/4.9	13.9
[51]	0.18- μ m CMOS	<-8	8.1/6.5	0.6-22	4.3/6.1	52
[53]	0.13- μ m CMOS	<-7	12/- Φ	3-9.4	1.8/4.7	30
[71]	0.13- μ m CMOS	<-9	8.6/11.7	1.5-8.1	3.6/6	2.62 $\oint$
[72]	0.18- μ m CMOS	<-5.7	10.8/- Φ	1.2-10.6	3.9/5.8	6.2
[73]	0.18- μ m CMOS	<-9	10.2/- Φ	0.5-11	3.9/4.5	14.4
[74]	0.13- μ m CMOS	<-17.5	8.15/7.69	1.3-12.1	2.5/4.56	10.68
[75]	0.13- μ m CMOS	<-7.3	12.4/11.1	0.1-14	2.7/3.7	14.4
[76]	InGaP/GaAs HBT	<-8	12.3/11.2	1.1-12.3	1.95/3.54	98
[49]	SiGe	<-10	21/- Φ	3-10	2.5/4.2	30
[77]	0.18- μ m SiGe	<-10	19.1 $\blacktriangle$ /- Φ	3-20	4.2/5.2	116

* -0.7 dB bandwidth $\odot$ -3 dB bandwidth Φ Not clearly shown in the reference papers $\oint$ core circuit power consumption $\blacktriangle$ Mid-bank gain at 11.5 GHz

Table 3.1 summarizes the performance of this low noise amplifier, with comparison to previous state-of-art low power CMOS design and SiGe design. This 3.1-10.6 GHz 0.15- μ m pHEMT MMIC amplifier has state of the art performance consuming

only 12.9 mW of power. The power gain is 12.5 dB with gain flatness of ± 0.5 dB, and noise figure is below 4.0 dB across the 3.1-10.6 GHz UWB band. The input $P_{1\text{dB}}$ power can reach -20.5 dBm at 7 GHz. The IIP3 point at 7 GHz is -10.4 dBm. It has excellent input and output return loss of better than 12 dB and 15 dB respectively except at the high end of the band. Group delay is around 184 pS ± 28 pS, coupled with flat gain performance, resulting in very good pulse response.

The rest of the chapter focuses on the design and implementation of the low noise amplifier in a 0.15- μm low noise pHEMT technology [78]-[80]. In section 3.2, the design challenges are indicated and proposed solutions are presented. In section 3.3, the input matching of the circuit is analyzed. The gain, power consumption and noise performance are optimized. The detail gain analysis and the selection of the feedback resistance are presented. Frequency domain measurement results carried out on the fabricated UWB LNA are reported in section 3.4. Finally the time domain FCC compliance UWB pulse response of the designed UWB LNA is presented in section 3.5.

3.2 Design Challenges and Proposed Solutions

Broadband systems have traditionally employed distributed amplifier topology. The problem of achieving a broadband match to the transistor input and output impedance is overcome by incorporating the input and output capacitances of a

number of transistors into artificial transmission-line structures. Chapter 2 gives the detail discussions on various distributed amplifier topologies.

But recently, for UWB system, the low power consumption requirement imposes lots of challenge on low power distributed amplifier design. And also for distributed amplifier, there is a 50-ohm termination resistor in the front of first stage of the amplifier; this will degrade the noise performance of the distributed amplifier substantially.

Fig. 3.1. Simplified circuit schematic of LNA

The proposed UWB LNA circuit is shown in Fig. 3.1. The circuit elements L_{bias} , C_{bias} , R_g , R_s and C_s serve as bias components and the circuit elements C_{DC} serve as the DC blocking capacitors. The first stage employ a resistive shunt feedback topology together with two T sections low pass structure in order to match to 50- Ω antenna. At the same time this topology will improve the noise performance compared to the distributed input stage. The second stage is implemented in common source configuration in order to achieve higher gain compared to common gate configuration. Current sharing design of the two stages is employed to reduce the power consumption of the UWB LNA. The inter-stage resistive matching technique is employed to improve the gain flatness. Finally the output matching topology also employed the resistive matching technique to drive an external 50- Ω load. The inductor L_4 is used to compensate the drain-source capacitance of the 2nd pHEMT to extend the bandwidth of the amplifier. L_5 reduces the effectiveness of resistive matching with increasing frequency.

3.3 Circuit Analysis

3.3.1 Gain, Noise Figure and Power Consumption Optimization

In order to optimize the gain, power consumption and noise performance, the number of stages of the amplifier and the bias current are determined carefully. In order to make sure the transistor operates in the linear region, the drain bias voltage

of the transistor is at least 1.0 V. Hence with fixed 3 V battery supply, we have three scenarios;

- 1-stage amplifier design with the drain bias at 3.0 V.
- 2-stage amplifier design with current sharing bias topology and drain bias voltage of each transistor at 1.5 V as shown in Fig. 3.1.
- 3-stage design, which is similar with Fig. 3.1 except that one more stage is added into the design and end up with the drain of each transistor biased at 1.0 V.

Since noise figure and gain performance are expected to degrade with frequency, the author chooses 10.6 GHz, the highest frequency in the FCC UWB band, as the worse case estimation to optimize gain, noise and power consumption performance.

Here the author further assumes perfect inter-stage matching between two transistors and plot the gain and noise figure performance versus power consumption of the three different scenarios. In order to simplify the complexity of the analysis, only one size of the pHEMT device is used here, which is 4 x 100 μm .

Fig. 3.2. Noise figure and gain versus power consumption under three bias scenarios

From Fig. 3.2, we can see that the 2-stage and 3-stage design are much better than 1-stage design after considering the gain, noise performance and the power consumption. Further comparison between the 2-stage and 3-stage design shows that the noise figure of the 2-stage design is slightly lower and the gain of the 3-stage design is higher. After considering the input 1 dB compression point will be lowered by the high gain design and also 1.0 V drain bias voltage is closed to the triode region of the transistor, we decided to choose the 2-stage design with current sharing topology shown in Fig. 3.1. The drain bias current of 4.3 mA, which is indicated in Fig. 3.2, is chosen.

3.3.2 Input, Inter-stage and Output Matching

Fig. 3.3 shows a conceptual schematic of a resistive shunt feedback amplifier. The input impedance of the resistive shunt feedback amplifier is expressed as [47] (assuming that the feedback amplifier low frequency input impedance is matched to Z_s)

$$Z_{in}(s) = Z_s / (1 + sZ_s C) \quad (3.1)$$

Z_s is the 50Ω source resistance and C is the input capacitance of the 1st stage amplifier, which is the same as C_{gs} of the input transistor. Hence the maximum input capacitance that can be afforded for an input reflection coefficient $S_{11} = -12 \text{ dB}$ at frequency $f = 10.6 \text{ GHz}$ can be expressed as

$$C \leq \frac{1}{\pi Z_s f} \sqrt{|S_{11}|^2 / (1 - |S_{11}|^2)} \quad (3.2)$$

From (3.2), the maximum input capacitance of the pHEMT is 156 fF. In order to meet this requirement, the largest available pHEMT transistor can not be used in the 1st stage. As a consequence, the highest gain and best noise performance are difficult to be achieved. The presented LNA employed two sections of T-network to transform the constant source impedance $Z_s = 50 \Omega$ into frequency dependent resistance $Z_s(s)$ whose impedance decreases as the frequency goes higher. The

simulated impedance $Z_s(s)$ is shown in Fig. 3.4 to confirm the impedance transformation. From equation (3.1), as source resistance Z_s decreases as the frequency goes higher, the maximum input capacitance requirement that can be tolerated to achieve an input reflection coefficient $S_{11} = -12\text{ dB}$ at higher frequency can be relaxed.

Fig. 3.3. Simple conceptual schematic of resistive shunt feedback amplifier

Fig. 3.4. The simulated source impedance after two sections T-network

Fig. 3.5 shows the input return loss S_{11}' , indicated in Fig. 3.1, without the two sections T-network and the input return loss S_{11} with the two sections T-network. The resistive matching technique is employed for inter-stage matching. And the inductor L_3 is used to compensate the gate-source capacitance of 2nd pHEMT transistor C_{gs2} to extend the bandwidth of the amplifier. This inter-stage matching technique contributes to the excellent gain flatness performance of the designed amplifier. The resistive matching technique is also employed for output matching. At low frequency band, L_4 and L_5 , indicated in Fig. 3.1, does not have significant effect at the output of the amplifier. The resistor R_o is in shunt with the

drain-source resistance of the second stage transistor to form the output impedance of the amplifier. Hence the value of the resistor R_o is obtained by

$$\begin{aligned} R_o // R_{ds2} &= R_L \\ \Rightarrow R_o &= \frac{R_L R_{ds2}}{R_{ds2} - R_L} = \frac{50 \times 115}{115 - 50} \Omega = 88 \Omega \end{aligned} \quad (3.3)$$

L_4 is used to compensate the drain-source capacitance of the 2nd pHEMT transistor C_{ds2} to extend the bandwidth of the amplifier. The value of L_4 is selected to make the resonant frequency of L_4 and C_{ds2} close to 10.6 GHz. Based on the available choice of the inductance, a 0.478 nH inductor is used, which make the resonant frequency of L_4 and C_{ds2} to be 9.2 GHz. L_5 is used to reduce the effectiveness of resistive matching with increasing frequency. The value used for L_5 is 0.478 nH.

3.3.3 Self-bias Configuration

The UWB LNA is DC biased by using self-bias mode [81], which is provided through source resistor R_s and source decoupling capacitor C_s , as illustrated in Fig.

3.1. The gate of the transistor is connected to ground via a large resistor R_g (2.4 k Ω in this design). As the gate current of the transistor is negligible, the potential of the transistor gate is 0 V. The current drawn by the transistor causes a potential drop across the source resistor R_s given by $V_{gs} = -V_s$. Because the transistor's source terminal is connected to the capacitor C_s , the potential at this terminal will rise up with respect to the potential of the gate until it eventually settles, thus providing the

correct gate-source bias voltage to forward bias the transistor. The value of the source resistor R_s determines the 4.3 mA current drawn by the transistor. By employing this self-bias technique, the UWB LNA can be operated from a single positive power supply.

Fig. 3.5. Input return loss S_{11}' without two T-network sections and S_{11} with two T-network sections.

3.3.4 Gain Analysis

In the following section, the detailed analysis on the voltage gain of the UWB LNA is shown. In order to simplify the analysis, the simplified small signal model for 0.15μm pHEMT device shown in Fig. 3.6 is used.

Fig. 3.6. Simplified small signal model for pHEMT device

Fig. 3.7. Simplified small signal circuit of the UWB LNA without the two T-network sections

The small signal circuit for the LNA without the two T-network sections at input is represented by Fig. 3.7.

The Y matrix of the network in the dash line box (1st stage) is

$$\begin{pmatrix} \frac{SC_{gs1}}{S^2L_1C_{gs1}+1} + \frac{1}{R_f} & -\frac{1}{R_f} \\ \frac{g_{m1}}{(S^2L_1C_{gs1}+1)(1+S^2L_2C_{ds1}+SL_2/R_{ds1})} & \frac{1+SC_{ds1}R_{ds1}}{(S^2L_2R_{ds1}C_{ds1}+SL_2+R_{ds1})} \\ -\frac{1}{R_f} & +\frac{1}{R_f} \end{pmatrix} \quad (3.4)$$

And the gain introduced by the network in the solid line box (1st stage) is

$$\begin{aligned} A_{v1} &= \frac{V_{out1}}{V_{RFin}} = -\frac{Y_{21}}{Y_{22}+Y} \\ &= \frac{-\frac{g_{m1}}{(S^2L_1C_{gs1}+1)(1+S^2L_2C_{ds1}+SL_2/R_{ds1})} + \frac{1}{R_f}}{\frac{1+SC_{ds1}R_{ds1}}{(S^2L_2R_{ds1}C_{ds1}+SL_2+R_{ds1})} + \frac{1}{R_f} + \frac{1}{R_1} + \frac{SC_{gs2}}{S^2L_3C_{gs2}+1}} \end{aligned} \quad (3.5)$$

The admittance Y in Fig. 3.7 is described by (3.6)

$$Y = \frac{1}{R_1} + \frac{SC_{gs2}}{S^2L_3C_{gs2}+1} \quad (3.6)$$

The gain associated with the admittance Y is

$$A_{v2} = \frac{V_{gs2}}{V_{out1}} = \frac{1}{S^2 L_3 C_{gs2} + 1} \quad (3.7)$$

The Y matrix of the network represented by the red color is

$$\begin{pmatrix} SC_{gs2} & 0 \\ \frac{g_{m2}}{1 + \frac{SL_5}{R_{ds2} // \frac{1}{SC_{ds2}} // (SL_4 + R_0)}} & \frac{1}{SL_5 + R_{ds2} // \frac{1}{SC_{ds2}} // (SL_4 + R_0)} \end{pmatrix} \quad (3.8)$$

$$A_{v3} = \frac{V_{RFout}}{V_{gs2}} = -\frac{Y_{21}}{Y_{22} + Y} = -\frac{g_{m2} R_L (R_{ds2} // \frac{1}{SC_{ds2}} // (SL_4 + R_0))}{SL_5 + R_{ds2} // \frac{1}{SC_{ds2}} // (SL_4 + R_0) + R_L} \quad (3.9)$$

Where R_L is the 50-Ω load impedance of the UWB LNA.

The overall voltage gain of the amplifier is

$$A_v = A_{v1} A_{v2} A_{v3} \quad (3.10)$$

Two different sizes of pHEMT transistors are used in the UWB LNA. The gate width of the pHEMT transistor used in the first and second stage is 4 x 100 μm and 4

x 50 μm respectively. Fig. 3.8 shows the ADS circuit schematic used to find g_{m1} of the first stage transistor. Basically the gate-source bias voltage V_{GS} is swept and at the same time the drain-source current I_{GS} is monitored. The g_{m1} can be computed by using (3.11).

$$g_{m1} = \text{diff}\left(\frac{I_{DS}}{V_{GS}}\right) \quad (3.11)$$

The g_{m2} of the second stage transistor can be obtained by using the same technique. Fig. 3.9 shows the I_{DS} and g_m plot of the first and second stage transistor. From I_{DS} plot of Fig. 3.9, the g_m value of the transistors when the drain-source current of the transistor is equal to 4.3 mA are $g_{m1}=69 \text{ mS}$ and $g_{m2}=51 \text{ mS}$.

Fig. 3.8. Circuit schematic with large signal model of the pHEMT transistor used to find the g_{m1} of the transistor used in UWB LNA

Fig. 3.9. Trans-conductance g_m and drain-source current I_{DS} of the pHEMT transistor obtained from the simulation result of the circuit shown in Fig. 3.8

By ignoring the effect of the gate-source capacitance and parasitic elements, the Y matrix (3.4) can be simplified as (3.12).

$$\begin{pmatrix} \frac{1}{R_f} & -\frac{1}{R_f} \\ g_{m1} - \frac{1}{R_f} & \frac{1}{R_f} \end{pmatrix} \quad (3.12)$$

By converting the Y matrix (3.12) to S matrix, the return loss S_{11} and the gain of the first stage S_{21} can be expressed as (3.13) and (3.14) respectively.

$$S_{11} = \frac{R_f - g_{m1}Z_0^2}{g_{m1}Z_0^2} \quad (3.13)$$

$$S_{21} = G = \frac{2(Z_0 - g_{m1}Z_0R_f)}{g_{m1}Z_0^2 + 2Z_0 + R_f} \quad (3.14)$$

Under the matched input condition, $S_{11} = 0$, Hence,

$$R_f = g_{m1}Z_0^2 = 0.069 \times 50^2 \Omega = 172.5 \Omega \quad (3.15)$$

By substituting (3.15) into (3.14), the gain of the first stage amplifier can be expressed as

$$S_{21} = G = 1 - \frac{R_f}{Z_0} = 1 - \frac{172.5 \Omega}{50 \Omega} = -2.45 V/V = 7.8 dB \quad (3.16)$$

The gate inductor L_1 and the drain inductor L_2 , indicated in Fig. 3.1, are used to extend the amplifier's band [45]. The drain inductor L_2 is selected to compensate for the drain-source capacitance C_{ds1} of the input stage transistor up to the cut-off frequency. Here the 0.213 nH inductor is selected for L_2 . The resonance frequency of L_2 and C_{ds1} is 10.8 GHz, which is close to the highest frequency of 10.6 GHz in the UWB band.

Fig. 3.10(a) and Fig. 3.10(b) show the simulated gain and input return loss as a

function of the feedback resistor value by including the effects of L_1, L_2 and the input capacitance of the transistor C_{gs1} . By trading off between gain and input return loss, the author chooses $R_f = 237 \Omega$ and the simulated gain of the first stage and input return loss are 8.3 dB and -8.9 dB respectively.

(a)

(b)

Fig. 3.10. Simulated gain and input return loss as a function of the feedback resistor value

The value of the circuit elements used in (3.4)-(3.9) is listed below.

- Parasitic circuit elements of the transistor are listed in the foundry design manual [82]:

$$\begin{aligned} g_{m1} &= 69 \text{ mS}, g_{m2} = 51 \text{ mS} \\ C_{ds1} &= 40 \text{ fF}, C_{gs1} = 220 \text{ fF}, R_{ds1} = 60 \Omega, \\ C_{ds2} &= 25 \text{ fF}, C_{gs2} = 130 \text{ fF}, R_{ds2} = 115 \Omega \end{aligned}$$

- The rest of the circuit components in Fig. 3.1:

$$\begin{aligned} L_1 &= 0.649 \text{ nH}, L_2 = 0.213 \text{ nH}, L_3 = 0.649 \text{ nH}, \\ L_4 &= 0.478 \text{ nH}, L_5 = 0.478 \text{ nH}, R_1 = 111 \Omega, \\ R_f &= 237 \Omega, C_f = 1.058 \text{ pF}, R_0 = 88 \Omega \end{aligned}$$

So the gain of the amplifier at 6 GHz can be calculated from (3.5), (3.6), (3.7), (3.9) and (3.10). The calculated result at 6 GHz is 11.5 dB, which is well matched with measured results shown in Fig. 3.14.

3.4 Frequency Domain Measurement Results

The designed UWB LNA is fabricated in a 0.15- μm pHEMT process. A microphotograph of the fabricated UWB LNA is shown in Fig. 3.11. Die size including the DC pads is 0.9 mm x 2.5 mm = 2.25 mm².

Fig. 3.11. Microphotograph of the fabricated LNA

Fig. 3.12 and Fig. 3.13 show the measured and simulated input and output reflection coefficients S_{11} , S_{22} for the fabricated UWB LNA. S_{11} is lower than -12 dB and S_{22} is lower than -15 dB except at the high end of the band. Fig. 3.14 and Fig. 3.15 shows the measured and simulated power gain S_{21} and reverse isolation S_{12} . The measured power gain S_{21} is 12.5 dB, and ± 0.5 dB gain flatness and the reverse isolation S_{12} is better than -32 dB. In order to measure S_{12} , Network Analyzer injects signal at the output of UWB LNA and measures the signal strength at the input of UWB LNA. Due to good isolation performance, the weak signal presents at the input of UWB LNA. This weak signal challenges Network Analyzer to cause large variations of measured S_{12} . The feedback amplifier topology in the first stage and good isolation performance S_{12} make the stability of designed UWB LNA less concern. The minimum value of stability factor K calculated from the measured S parameters is 2.2 at 11.3 GHz suggesting unconditional stability of the UWB LNA. Group delay is shown in Fig. 3.16; it decreases from 192 ps to 156 ps from 3.1 GHz to 5.5 GHz and then increases from 156 ps to 212 ps from 5.5 GHz to 10.6 GHz.

The maximum group delay variation is ± 28 ps.

The S parameters are measured on five different fabricated UWB LNA. The maximum observed spread of the parameters is less than 1 dB.

The measured spot NF for the fabricated UWB LNA is shown in Fig. 3.17. The minimum NF is as low as 3.4 dB, and the highest NF in 3.1 GHz to 10.6 GHz band is 4.0 dB.

The measured input P1dB compression point versus frequency is plotted in Fig. 3.18(a). The input P1dB compression point at 7 GHz can reach -20.5 dBm. The IIP3 point at 7 GHz is -10.4 dBm. The measured input third-order intercept point (IIP3) versus frequency is plotted in Fig. 3.18(b). Tone spacing is 1 MHz.

All these measurements are done under 3 V power supply and measured supply current I_d is 4.3 mA. Hence the DC power consumed by the LNA is 12.9 mW.

Fig. 3.12. Measured and simulated S_{11} of the fabricated UWB LNA

Fig. 3.13. Measured and simulated S_{22} of the fabricated UWB LNA

Fig. 3.14. Measured and simulated S_{21} of the fabricated UWB LNA

Fig. 3.15. Measured and simulated S_{12} of the fabricated UWB LNA

Fig. 3.16. Measured and simulated group delay of the fabricated UWB LNA

Fig. 3.17. Measured and simulated spot noise figure of the fabricated UWB LNA

(a)

(b)

Fig. 3.18. Measured (a) P_{1dB} at the input of the fabricated UWB LNA (b) input third-order intercept point (IIP₃) versus frequency

3.5 Time Domain UWB Pulse Response Characterization

3.5.1 Characterization Setup

Fig. 3.19(a) shows the time domain pulse response characterization setup [83]. Fig. 3.20 shows the block diagram of the time domain pulse response characterization setup [83], which consists of a FCC compliance UWB pulse generator and an Agilent Infinium DCA-J 86100C 20 GHz digital sampling oscilloscope. Fig. 3.19(b) shows the fabricated UWB LNA is under characterization. The variable DC-26.5 GHz attenuator and 4-12.4 GHz 3 dB coupler ensure broadband 50- Ω source impedance is presented to the UWB LNA input. The through port of the 3 dB coupler allows the oscilloscope to monitor the input pulse through channel 2. The output from the UWB LNA is sampled by channel 1 of the sampling oscilloscope. The waveform sampled by channel 1 can be used to derive the waveform at the output of the UWB LNA and the waveform sampled by channel 2 can be de-embedded to the input of the UWB LNA by accounting for the frequency response of the cable assemblies that include the 3 dB coupler.

(a)

(b)

Fig. 3.19. (a) The characterization setup of FCC compliance UWB pulse response of the UWB

LNA and (b) UWB LNA being probed

Fig. 3.20. Block diagram of the characterization setup

3.5.2 Calibration Procedure and Results

The cables used in the characterization setup have better than 20 dB return losses up to 18 GHz. Hence all S_{11} of the cables are not considered in the characterization process. The voltage waveform $V_s(t)$ presented at the input of the 4-12.4 GHz 3 dB coupler is monitored by channel 2 voltage waveform $V_2(t)$. The S parameters used in the monitoring including the 3 dB coupler are measured and S_{21} of the whole

monitoring network is noted as $S_{21monitor}$. Hence the voltage waveform $V_s(t)$ can be derived from $V_2(t)$:

$$v_s(t) = FFT^{-1} \left[\frac{FFT(v_2(t))}{S_{21monitor}} \right] \quad (3.17)$$

Where FFT and FFT^{-1} stand for Fourier and inverse Fourier transforms, respectively.

S_{21} of the whole input network of device under test including the 3 dB coupler is measured and indicated as $S_{21input}$. Hence the voltage waveform at the input of the device under test is:

$$v_{in}(t) = FFT^{-1} \left[FFT(v_s(t)) \times S_{21input} \right] \quad (3.18)$$

S_{21} of the whole output network of device under test is measured and indicated as $S_{21output}$. The voltage waveform at the output of the UWB LNA is:

$$v_{out}(t) = FFT^{-1} \left[\frac{FFT(v_1(t))}{S_{21output}} \right] \quad (3.19)$$

The above-described correction procedure is verified by using a “through” standard (a very short 50-Ω transmission line). Fig. 3.21(a) illustrates that the similar input

$v_{in}(t)$ and output $v_{out}(t)$ time domain voltage waveform at two ends of the “through” standard. The correlation coefficient of $v_{in}(t)$ and $v_{out}(t)$ is 0.99, which verifies the strong resemblance between $v_{in}(t)$ and $v_{out}(t)$. The correlation equation used is

$$\begin{aligned} & \text{Correlation Coefficient}(v_{in}, v_{out}) \\ &= \frac{n \sum v_{ini} v_{outi} - \sum v_{ini} \sum v_{outi}}{\sqrt{n \sum v_{ini}^2 - (\sum v_{ini})^2} \sqrt{n \sum v_{outi}^2 - (\sum v_{outi})^2}} \end{aligned} \quad (3.20)$$

Here v_{ini} and v_{outi} are i^{th} sample value of $v_{in}(t)$ and $v_{out}(t)$ respectively.

And Fig. 3.21(b) shows that similar input $v_{in}(t)$ and output $v_{out}(t)$ spectrum shape.

3.5.3 Characterization Results

Using the characterization setup shown in Fig. 3.19 and the correction procedure discussed above, the FCC compliance UWB pulse response of the UWB LNA is characterized. The peak to peak voltage $v_{pp}(t)$ of the input pulse $v_{in}(t)$ of the UWB LNA is increased from 11 mV to 119 mV. The correlation coefficient of the input pulse $v_{in}(t)$ and output pulse $v_{out}(t)$ is used to qualify the resemblance between $v_{in}(t)$ and $v_{out}(t)$. Table 3.2 lists the correlation coefficients of the input and output of the UWB LNA at various different input pulse levels.

Table 3.2. The Correlation Coefficients of the Input and Output at Different Input Levels

$v_{pp}(t)$	Correlation Coefficient
11 mV	0.95
38 mV	0.94
67 mV	0.93
97 mV	0.91
108 mV	0.90
119 mV	0.87

Fig. 3.22(a) and Fig. 3.23(a) shows that the input $v_{in}(t)$ and output $v_{out}(t)$ time domain voltage waveform of the fabricated UWB LNA when the peak to peak voltage $v_{pp}(t)$ of the input pulse is 11 mV and 38 mV respectively. The correlation coefficient of $v_{in}(t)$ and $v_{out}(t)$ is 0.95 and 0.94 respectively, which verifies the strong resemblance between $v_{in}(t)$ and $v_{out}(t)$ when the fabricated UWB LNA is operated in small input pulse level. Fig. 3.22(b) and Fig. 3.23(b) shows similar input and output spectrum shape of the fabricated UWB LNA. 12-13 dB amplification is also shown over 3.1-10.6 GHz in Fig. 3.22(b) and Fig. 3.23(b), which matches the frequency domain S_{21} measurement result presented in section 3.4.

(a)

(b)

Fig. 3.21. FCC compliance input (v_{in}) and output (v_{out}) (a) voltage waveforms and (b) spectrum shape de-embedded to two ends of a "through" standard for verification of the correction procedure

(a)

(b)

Fig. 3.22. FCC compliance input (v_{in}) and output (v_{out}) (a) voltage waveforms and (b) spectrum shape de-embedded to two ends of the UWB LNA when the $v_{pp}(t) = 11 \text{ mV}$.

(a)

(b)

Fig. 3.23. FCC compliance input (v_{in}) and output (v_{out}) (a) voltage waveforms and (b) spectrum shape de-embedded to two ends of the UWB LNA when the $v_{pp}(t) = 38 \text{ mV}$.

(a)

(b)

Fig. 3.24. FCC compliance input (v_{in}) and output (v_{out}) (a) voltage waveforms and (b) spectrum shape de-embedded to two ends of the UWB LNA when the $v_{pp}(t) = 119 \text{ mV}$.

Fig. 3.24 shows the time domain voltage waveform and spectrum shape of the input $v_{in}(t)$ and output $v_{out}(t)$, respectively, when the peak to peak voltage $v_{pp}(t)$ of the input pulse level is increased to 119 mV. The correlation coefficient of the input $v_{in}(t)$ and output $v_{out}(t)$ is 0.87.

Fig. 3.24(b) shows that the main difference between input $v_{in}(t)$ and output $v_{out}(t)$ is in the low frequency part. Hence a simple high pass filter (HPF) can be implemented in the output of the UWB LNA to improve the correlation coefficient of the input and output pulses. A simple second order high pass filter is implemented in ADS. The correlation coefficient of the input pulse and the output pulses after filtering is 0.91, which shows the resemblance improvement between the input and output pulses of the UWB LNA. The time domain voltage waveform and spectrum shape of the input $v_{in}(t)$ and output $v_{out}(t)$ after high pass filter is shown in Fig. 3.25. In the real UWB system [84], the tag receives the signal; amplify it and re-transmit back through a transmitting antenna. Hence the high pass filtering can be easily achieved by the transmitting antenna after the UWB LNA [85]-[87].

(a)

(b)

Fig. 3.25. (a) Time domain voltage waveform and (b) spectrum shape de-embedded to two ends of the UWB LNA after high pass filter when the $v_{pp}(t) = 119 \text{ mV}$.

3.6 Conclusion

We have presented the design and implementation of a low power UWB LNA in 0.15- μm low noise pHEMT technology. The good input and output matching and low noise performance are achieved for the whole 3.1-10.6 GHz frequency band of interest. Power gain as high as 13 dB is achieved, the gain flatness is 12.5 ± 0.5 dB, and it consumes only 12.9 mW power. The noise figure is below 4.0 dB. The input $P_{1\text{dB}}$ compression point of the designed UWB LNA at 7 GHz is -20.5 dBm. The IIP3 point at 7 GHz is -10.4 dBm. It has excellent input and output return loss of better than 12 dB and 15 dB respectively except at the high end of the band. Group delay is around 184 pS ± 28 pS group, coupled with flat gain performance, resulting in very good pulse response.

A new practical way to characterize the degree of pulse distortion introduced by the designed UWB LNA is discussed. The real FCC compliance UWB pulse is used as the characterization source. The characterization procedure is carried on the fabricated UWB LNA in time domain by using a sampling oscilloscope with the cable assemblies' delays and losses corrected in frequency domain. The exact degree of pulse distortion introduced by the UWB LNA is qualified by the correlation coefficient of the input and output pulses. The characterization is performed on the UWB LNA with the peak to peak voltage $v_{pp}(t)$ of the input pulse $v_{in}(t)$ varied from 11 mV up to 119 mV. The characterization results show that the correlation coefficient of the input and output pulses can maintain higher than 0.9 when the

input pulse level is increased to 108 mV. When the UWB LNA is operated in high pulse level, the main difference between the input and output pulse is the low frequency part, and simple investigation done in ADS shows that high pass filtering can be performed at the output of the fabricated UWB LNA to improve the correlation coefficient of the input and output pulses. To the best of the authors' knowledge, this is the first attempt to characterize the FCC compliance UWB pulse response of the UWB LNA.

CHAPTER 4

Ultra-wideband Pulse Synthesizer

4.1 Performance Overview

A novel ultra-wideband (UWB) pulse synthesizer is proposed [88], which uses a distributed amplifier to combine Gaussian pulses of different polarities, amplitudes and delays. The center frequency and bandwidth of the synthesized pulse can be adjusted by varying the number of Gaussian pulses and the delays between them. Compared to other UWB pulse generators, the present synthesizer is capable of higher peak power due to the high breakdown voltage of 0.25- μm pHEMTs and higher efficiencies due to the Class-C bias and automatic on-off operation with positive input pulses. A prototype synthesizer has been designed and fabricated with

a center frequency of 4.0 GHz and a bandwidth of 1.9 GHz. Under a Gaussian input pulse of 1.5 V and 100 ps width, it outputs into 50 Ω a UWB pulse of 4.5 V with 4 GHz centre frequency and 1 ns envelope width. At a pulse-repetition frequency of 10 MHz, it consumes 1 mA at 3 V with 17% efficiency. Approaches to maintain high efficiency by scaling the supply voltage for different input amplitudes and pulse-repetition frequencies have also been verified experimentally.

Table 4.1 compares the output amplitude, width and efficiency of UWB pulses generated by the different methods. The amplitude is measured peak to peak. The width is the full width at half maximum.

Table 4.1. Characteristics of UWB Pulses Generated by Different Methods

Reference	Amplitude (V)	Width (ns)	Efficiency	PRF (MHz)
[56]	0.26	3	0.16%	100
[58]	0.063	2.5	0.74%	567
[62]	5.1 ^a	0.9	7.9%	1
[63]	0.542	0.6	3.14%	50
	0.673	0.5	2.05%	50
[64]	0.68	0.25	0.94%	500
[66]	0.5	-	-	-
[67]	0.2	0.6	0.048%	80
[68]	0.12	0.5	0.07%	2000
[69]	0.08	0.8	0.029%	2500
[70]	4.5	1.0	10%	10
[88]	4.5	1.0	17%	10
	6.4	1.0	13%	5

^aConverted from 100- Ω load to 50- Ω load.

The efficiency is defined in (4.1) as the ratio between the emission power and average power consumption [62], [70]. PRF in (4.1) is the pulse repetition frequency and the pulse width is defined as the full width at half maximum. The generation method of the external Gaussian input pulse is presented in [89], which does not require an external DC supply and only relies on the rising edge of the incoming clock signal.

$$\eta = \frac{\text{Peak Output Power} \times \text{Pulse Width} \times \text{PRF}}{\text{DC Power Consumption}} \quad (4.1)$$

In section 4.2, the author emphasizes on analyzing the method of the UWB pulse synthesizer from both time domain and frequency domain. The ability to adjust the center frequency and bandwidth of the synthesized pulse by varying the number of the Gaussian pulses and the delays between them is demonstrated. In section 4.3, the author derives the power gain of the distributed UWB pulse synthesizer. The method to optimize the power supply voltage of UWB pulse synthesizer by optimizing the drain bias voltage through the load line of the transistor is presented [90]. And in section 4.3, the author also verified the ability to maintain high efficiency by scaling the supply voltage for different input amplitudes and pulse-repetition frequencies. In section 4.4, the measurement results with both 1.5 V amplitude, 10 MHz PRF Gaussian input pulse and 2 V amplitude, 5 MHz PRF Gaussian input pulse are presented.

4.2 Design Challenges

One of UWB major application is long-range low-data-rate communication with precision localization. For this application, it is critical to generate UWB pulses with high peak power and high efficiency at low pulse-repetition frequency (PRF) while complying with spectrum regulations. In chapter 2, section 2.3 various FCC compliance UWB pulse generation methods are presented. But most of the techniques are unable to generate high peak power UWB pulse. Hence the power amplifier is needed to amplify the generated UWB pulse into high peak power pulse. But it is not power efficient to amplify the UWB pulse by using the traditional continuous wave amplifier. Taking 10 MHz pulse repetition frequency as an example, the duty cycle of 1 ns UWB pulse is only 1%. If the amplifier is designed to be traditional continuous wave amplifier, only 1% DC power consumed by the amplifier is useful.

The proposed distributed UWB pulse synthesizer with a simplified architecture has been implemented in 0.25- μm gate-length depletion-mode pHEMTs, which are biased in Class-C for high-efficiency operation. For the negative branch of the distributed amplifier, each tap is automatically switched on and off by the positive input Gaussian pulse. Hence the depletion-mode pHEMTs is only on when there is Gaussian input pulse presented. However, the positive branch cannot be easily implemented with the depletion-mode pHEMTs in Class-C operation. To overcome the difficulty, the power splitter and the positive branch of the distributed amplifier

are eliminated and, instead, positive pulses are generated from reflected negative pulses. Section 4.3 and 4.4 has more detailed discussions.

4.3 Pulse-Synthesis Method

Fig. 4.1(a) shows the proposed UWB pulse synthesizer is based on a distributed amplifier with two branches and n taps. First, a Gaussian input pulse $g(t)$ is divided by a power splitter into two sub-pulses $g^+(t)$ and $g^-(t)$. Second, $g^+(t)$ is delayed by τ_1 then distributed to each tap of the distributed amplifier with additional delay τ_g and weight w_i^+ ($w_i^+ \geq 0$). In contrast, $g^-(t)$ is directly distributed to each tap with only tap-to-tap delay τ_g and is weighted by w_i^- ($w_i^- \leq 0$). Both $g^+(t)$ and $g^-(t)$ are terminated in matched loads to prevent reflection. Finally, the output pulse is synthesized by combining pulses from both the positive and negative branches of the distributed amplifier as

$$V_n^{out}(t) = \sum_{i=1}^n \left\{ w_i^+ g^+ \left[t - \tau_1 - (i-1)\tau_g \right] + w_i^- g^- \left[t - (i-1)\tau_g \right] \right\} \quad (4.2)$$

(a)

(b)

Fig. 4.1. Schematic of (a) original and (b) simplified distributed UWB pulse synthesizer

Assuming ideal splitter and equal weights so that $g^+(t) = g^-(t) = g(t)/\sqrt{2}$, $w_i^+ = 1$ and $w_i^- = -1$, (4.2) can be simplified as

$$V_n^{out}(t) = \frac{1}{\sqrt{2}} \sum_{i=1}^n \left\{ g[t - \tau_1 - (i-1)\tau_g] - g[t - (i-1)\tau_g] \right\} \quad (4.3)$$

The values of τ_1 , τ_g and n can be adjusted to optimize the synthesizer performance for different applications. By adjusting τ_1 , the center frequency of the output pulse $V_n^{out}(t)$ can be tuned [91]. By adjusting τ_g and n , the output width can also be tuned [91]. The adjustments can be analyzed by assuming a Gaussian input pulse [92] of

$$g(t) = \left(A/\sqrt{2\pi\sigma^2} \right) \exp(-t^2/2\sigma^2) \quad (4.4)$$

where σ is the standard derivation and $2\sigma\sqrt{2\ln 2}$ is the full width at half maximum.

The Fourier transform of (4.4) in the frequency domain is

$$g(\omega) = A \exp[-\omega^2\sigma^2/2] \quad (4.5)$$

where ω is the angular frequency, which is equal to $2\pi f$. Using (4.3)-(4.5), the output waveform and spectrum can be analyzed for synthesizers with different numbers of taps.

When $n = 1$

$$\begin{aligned} V_1^{out}(t) &= (1/\sqrt{2})[g(t - \tau_1) - g(t)] \\ V_1^{out}(\omega) &= [g(\omega)/\sqrt{2}][\exp(-j\omega\tau_1) - 1]. \end{aligned} \quad (4.6)$$

The corresponding power spectral density is

$$|V_1^{out}(\omega)|^2 = |g(\omega)|^2 2 \sin^2(\omega\tau_1/2) \quad (4.7)$$

Let $G_n(\omega)$ be the power gain of an n -tap synthesizer, then

$$|V_n^{out}(\omega)|^2 = |g(\omega)|^2 G_n(\omega) \quad (4.8)$$

and

$$G_1(\omega) = 2 \sin^2(\omega\tau_1/2) \quad (4.9)$$

$G_1(\omega)$ has peaks at $m\pi/\tau_1$ and nulls at $(m-1)\pi/\tau_1$, where m is an odd integer. And the peak has the value $10\log_{10}(2) = 3$ dB. This is the special case when both the center frequency and bandwidth are both determined by τ_1 , because τ_g is not involved when $n = 1$.

When $n = 2$,

$$\begin{aligned}
V_2^{out}(t) &= V_1^{out}(t) + V_1^{out}(t - \tau_g) \\
V_2^{out}(\omega) &= V_1^{out}(\omega) [1 + \exp(-j\omega\tau_g)] \\
G_2(\omega) &= 8 \cos^2(\omega\tau_g/2) \sin^2(\omega\tau_1/2).
\end{aligned} \tag{4.10}$$

In addition to peaks at $m\pi/\tau_1$ and nulls at $(m-1)\pi/\tau_1$, $G_2(\omega)$ has nulls at $m\pi/\tau_g$. Thus, while the center frequency is determined by τ_1 , the bandwidth may be determined by τ_g if $\tau_g > \tau_1$. And the peak has the value $10\log_{10}(8) = 9$ dB.

When $n = 3$,

$$\begin{aligned}
V_3^{out}(t) &= V_1^{out}(t) + V_1^{out}(t - \tau_g) + V_1^{out}(t - 2\tau_g) \\
V_3^{out}(\omega) &= V_1^{out}(\omega) [1 + \exp(-j\omega\tau_g) + \exp(-j2\omega\tau_g)] \\
G_3(\omega) &= 2 [1 + 2 \cos(\omega\tau_g)]^2 \sin^2(\omega\tau_1/2)
\end{aligned} \tag{4.11}$$

In addition to peaks at $m\pi/\tau_1$ and nulls at $(m-1)\pi/\tau_1$, $G_3(\omega)$ has nulls at $2(m \pm 1/3)\pi/\tau_g$.

And the peak has the value $10\log_{10}(18) = 12.6$ dB.

When $n = 4$,

$$\begin{aligned}
V_4^{out}(t) &= V_1^{out}(t) + V_1^{out}(t - \tau_g) + V_1^{out}(t - 2\tau_g) \\
&\quad + V_1^{out}(t - 3\tau_g) \\
V_4^{out}(\omega) &= V_1^{out}(\omega) \left[1 + \exp(-j\omega\tau_g) \right. \\
&\quad \left. + \exp(-j\omega 2\tau_g) + \exp(-j\omega 3\tau_g) \right] \\
G_4(\omega) &= 32 \cos^2(\omega\tau_g) \cos^2(\omega\tau_g/2) \sin^2(\omega\tau_1/2)
\end{aligned} \tag{4.12}$$

In addition to peaks at $m\pi/\tau_1$ and nulls at $(m-1)\pi/\tau_1$, $G_4(\omega)$ has nulls at $m\pi/2\tau_g$ and $m\pi/4\tau_g$. And the peak has the value $10\log_{10}(32) = 15.1$ dB.

Table 4.2. Peak Gain and Bandwidth with Increasing n

n	1	2	3	4
Peak Gain (dB)	3	9	12.6	15.1
Bandwidth (GHz)	6.6	3.1	2	1.5

Thus, the output spectra of synthesizers with different numbers of taps can be evaluated by using (4.9)-(4.12). To illustrate the cases for $\tau_g > \tau_1$, τ_g is fixed at $2\tau_1$. Fig. 4.2(a) plots gains $G_1(\omega)$, $G_2(\omega)$, $G_3(\omega)$, and $G_4(\omega)$ for $\tau_1 = 120$ ps and $\tau_g = 240$ ps. It can be seen that the bandwidth of the main lobe decreases with increasing n . At the same time the peak gain of the main lobe increases with increasing n . Table 4.2 lists the peak gain and 10-dB bandwidth for different n values.

With n fixed at 4 and τ_g fixed at $2\tau_1$, Fig. 4.2(b) shows that the peak frequency and bandwidth are both inversely proportional to τ_1 . Table 4.3 summarizes the peak frequency and 10-dB bandwidth for different τ_1 values.

Table 4.3. Peak Frequency and Bandwidth Based on the Synthesizer Gain

Delay τ_1 (ps) ^a	100	120	140	160
Peak Frequency	5.0	4.2	3.6	3.1
Bandwidth (GHz)	1.8	1.5	1.3	1.2

^a $\tau_g = 2\tau_1$. $n = 4$.

Following (4.8), the output spectrum is determined by not only the synthesizer gain $G(\omega)$, but also the shape of the input pulse $g(\omega)$. Using (4.12), Fig. 4.3 shows the calculated output waveform and spectrum for $n = 4$, $\tau_1 = 120$ ps, $\tau_g = 240$ ps, and $\sigma = 100$ ps with the peak-to-peak amplitude in the time domain normalized to 1 V and the main lobe in the frequency domain normalized to 0 dB. Compared to Fig. 4.2, the difference between the main lobe and the nearest side lobe is now reduced from 12.8 dB to 10 dB by the rich low-frequency content of the Gaussian input pulse. In order to utilize the spectral mask more efficiently, the side lobes can be suppressed by adjusting the weights w_i^+ and w_i^- of the distributed amplifier so that the output pulse follows a Gaussian envelope in the time domain as shown in Fig. 4.4(a). Fig. 4.4(b) shows that in this case the main lobe in the frequency domain is

approximately 30 dB higher than the nearest side lobe. The side lobe below 1.5 GHz becomes higher compared to Fig. 4.3. But this low frequency content is easy to be filtered out by AC coupling capacitor and UWB antenna. This approach is elaborated in the next section.

(a)

(b)

Fig. 4.2. Calculated synthesizer gain with (a) $\tau_1 = 120$ ps and $n = 1, 2, 3, 4$ and (b) $n = 4$ and $\tau_1 = 100, 120, 140, 160$ ps. In all case, $\tau_g = 2\tau_1$.

(a)

(b)

Fig. 4.3. Calculated synthesizer output (a) waveform and (b) spectrum with $n = 4$, $\tau_1 = 120$ ps, $\tau_g = 240$ ps, and $\sigma = 100$ ps.

(a)

(b)

Fig. 4.4. Calculated (a) waveform and (b) spectrum of the output pulse with a Gaussian envelope formed by varying the weights w_i^+ and w_i^- of the distributed amplifier. The rectangle-shaped FCC spectral mask is overlaid in (b) as a reference.

4.4 Circuit Analysis and Design

4.4.1 Simplified Distributed UWB Pulse Synthesizer

The proposed distributed UWB pulse synthesizer with a simplified architecture has been implemented in 0.25- μm gate-length depletion-mode pHEMTs, which are biased Class-C for high-efficiency operation [93]-[94]. For the negative branch of the distributed amplifier with negative w_i^- weights, each tap is automatically switched on and off by the positive input pulse. Fig. 4.5 shows the Class-C circuit schematic with Gaussian input pulse. However, the positive branch with positive w_i^+ weights cannot be easily implemented with the depletion-mode pHEMTs in Class-C operation. To overcome the difficulty, the power splitter and the positive branch of the distributed amplifier are eliminated and, instead, positive pulses are generated from reflected negative pulses. As shown in Fig. 4.1(b), in the simplified architecture, a negative pulse V_n is first formed by combining the pulses through the negative taps with w_i^- weights. The V_n pulse then travels both forward and backward as indicated by V_{nf} and V_{nb} in Fig. 4.1(b). When the backward traveling V_{nb} passes through the delay element τ_2 to reach the short-circuited termination, a positive V_{nr} is reflected. The reflected pulse V_{nr} then travels forward to combine with V_{nf} to form an UWB pulse with both positive and negative components at the output of the distributed amplifier. Note that V_{nr} is behind V_{nf} by $2\tau_1$. Therefore, the analysis of Section 4.3 is still valid provided $2\tau_2$ is used instead of τ_1 .

Fig. 4.5. Class-C operation with positive input Gaussian pulse

4.4.2 Circuit Design and Analysis

Fig. 4.6 shows the circuit design based on the simplified architecture of Fig. 4.1(b) with $n = 4$. A conventional distributed amplifier is implemented with discrete pHEMTs on a combination of ceramic and polymer boards. The typical $50\text{-}\Omega$ termination on the drain side of the pHEMTs is replaced by a short-circuited termination after a transmission line with delay τ_2 . A short transmission line with delay τ_d between the pHEMT drains used to connect the drains of the transistors, while a long transmission line with delay τ_g meanders between the pHEMT gates. As described in Section 4.3, the input pulse travels through τ_g and switches on each pHEMT successively, before being absorbed by a $50\text{-}\Omega$ termination. The w_i^- weights

are implemented with voltage dividers made of C_{div} and C_{gs} in series, where C_{gs} is the gate-source capacitance of each pHEMT. The 0.25- μm pHEMT dies used in this design is from RFMD [95]. Bond wires L_{g1} , L_{g2} and L_d [96]-[101] connect the pHEMTs with the transmission lines on the board and help compensate C_{div} , C_{gs} and C_{ds} to maintain the 50- Ω characteristic impedance, where C_{ds} is the drain-source capacitance of each pHEMT.

Fig. 4.6. Circuit schematic of the simplified distributed UWB pulse synthesizer with one branch and four taps

Fig. 4.7. (a) Linear pHEMT model [102] and (b) detailed circuit schematic formed by inserting

the pHEMT model into Fig. 4.6

The C_{div}/C_{gs} dividers are designed to give the proper w_i^- weights to ensure a Gaussian envelope for efficient spectrum utilization as discussed at the end of section 4.3. As shown in Fig. 4.4(a), four successive positive pulses of amplitudes $V_1 = V_4$, $V_2 = V_3 = 2.5 V_1$ and four successive negative pulses of the same amplitudes but 180° out of phase form an output pulse with a Gaussian envelope. For the pHEMTs used in the implementation, $C_{gs} = 0.38$ pF. Therefore, $C_{div} = 0.25$ pF would give $V_2 = 2.5 V_1$.

Given the C_{div}/C_{gs} ratio, it is tempting to simply let $w_1^- = w_4^- = -0.4$ and $w_2^- = w_3^- = -1$. However, the w_i^- values can only be determined after considering the transistor gain and parasitic loss. This is accomplished by analyzing the detailed circuit schematic of Fig. 4.7(b), which is formed by inserting the linear pHEMT model of Fig. 4.7(a) into Fig. 4.6. In the analysis, the bond wires L_{g1} , L_{g2} and L_d , as well as the transmission lines τ_2 and τ_d , are assumed to be lossless. The loss associated with τ_g is estimated to be 0.35 dB. The loss associated with the channel resistance R_i is considered, but the loss associated with the drain-source resistance R_{ds} is neglected. Delays other than τ_2 , τ_d and τ_g are all ignored.

With $V_{gg} = -1.0$ V, each pHEMT is biased below its threshold voltage of $V_{th} = -0.8$ V and the effective input voltage V_{eff} under an input pulse of $V_{in} = 1.5$ V is:

$$\begin{aligned}
V_{eff1} &= \frac{(V_{in} + V_{gg} - V_{th})/j\omega C_{gs}}{1/j\omega C_{gs} + 1/j\omega C_{div} + R_i} = 0.52 \text{ V} \\
V_{eff2} &= \frac{(V_{in} + V_{gg} - V_{th})/j\omega C_{gs}}{10^{Loss_g/20} (1/j\omega C_{gs} + R_i)} = 1.25 \text{ V} \\
V_{eff3} &= \frac{(V_{in} + V_{gg} - V_{th})/j\omega C_{gs}}{10^{2Loss_g/20} (1/j\omega C_{gs} + R_i)} = 1.20 \text{ V} \\
V_{eff4} &= \frac{(V_{in} + V_{gg} - V_{th})/j\omega C_{gs}}{10^{3Loss_g/20} (1/j\omega C_{gs} + 1/j\omega C_{div} + R_i)} = 0.46 \text{ V}
\end{aligned} \tag{4.13}$$

Fig. 4.8. g_m of the 0.25- μm pHEMT transistor used [95].

Fig. 4.8 shows the transconductance g_m versus the gate-source voltage of the pHEMT transistors used when 3.0 V drain supply voltage applied. Hence with the transconductance $g_m = 80 \text{ ms}$, (4.14) shows that the current through each pHEMT is

42 mA, 100 mA, 96 mA and 37 mA, respectively.

$$\begin{aligned}
I_1 &= -g_m V_{eff1} = -80 \text{ ms} \times 0.52 \text{ V} = -41.6 \text{ mA} \\
I_2 &= -g_m V_{eff2} = -80 \text{ ms} \times 1.25 \text{ V} = -100 \text{ mA} \\
I_3 &= -g_m V_{eff3} = -80 \text{ ms} \times 1.20 \text{ V} = -96.0 \text{ mA} \\
I_4 &= -g_m V_{eff4} = -80 \text{ ms} \times 0.46 \text{ V} = -36.8 \text{ mA}
\end{aligned} \tag{4.14}$$

As the drain current is divided between the 50- Ω transmission lines right and left, as well as the drain-source resistance $R_{ds} = 373 \Omega$, the effective drain impedance is 23 Ω . Therefore, the output voltage for each pHEMT is 0.97 V, 2.34 V, 2.21 V and 0.86 V, which match the measured results in Section 4.5. From the ratio of output and input voltages on each pHEMT, $w_1^- = -0.65$, $w_2^- = -1.56$, $w_3^- = -1.50$, and $w_4^- = -0.57$.

By properly combining the output voltage of each pHEMT, the forward traveling pulse at the synthesizer output is:

$$\begin{aligned}
V_{nf}(t) &= w_1^- V_{in}(t - 3\tau_d) + w_2^- V_{in}(t - \tau_g - 2\tau_d) \\
&\quad + w_3^- V_{in}(t - 2\tau_g - \tau_d) + w_4^- V_{in}(t - 3\tau_g) \\
V_{nf}(\omega) &= V_{in}(\omega) \left\{ \begin{aligned} &w_1^- \exp(-j3\omega\tau_d) + w_2^- \exp[-j\omega(\tau_g + 2\tau_d)] \\ &+ w_3^- \exp[-j\omega(2\tau_g + \tau_d)] + w_4^- \exp[-j3\omega\tau_g] \end{aligned} \right\}.
\end{aligned} \tag{4.15}$$

The backward traveling pulse V_{nb} can be similarly evaluated knowing that it is of the opposite polarity and is delayed by $2\tau_2 + 3\tau_d$. Combining V_{nf} and V_{nb} , the output pulse is

$$\begin{aligned}
 V_4^{out}(t) &= V_{nf}(t) - V_{nf}(t - 2\tau_2 - 3\tau_d) \\
 V_4^{out}(\omega) &= V_{nf}(\omega) \{1 - \exp[-j\omega(2\tau_2 + 3\tau_d)]\} \\
 G_4(\omega) &= |1 - \exp[-j\omega(2\tau_2 + 3\tau_d)]|^2 \\
 &\quad \cdot \left| \frac{w_1^- \exp(-j\omega 3\tau_d) + w_2^- \exp[-j\omega(\tau_g + 2\tau_d)]}{+w_3^- \exp[-j\omega(2\tau_g + \tau_d)] + w_4^- \exp(-j\omega 3\tau_g)} \right|^2.
 \end{aligned} \tag{4.16}$$

Fig. 4.9. Synthesizer gain calculated by using (4.16) with $\tau_d = 15$ ps or 0. The calculated gain for $\tau_d = 15$ ps is in general agreement with that simulated by using TOM3 pHEMT and transmission-line models

Eq. (4.16) can be used to calculate the synthesizer gain at any frequency. For example, Fig. 4.9 shows that with $\tau_2 = 60$ ps, $\tau_g = 240$ ps, and $\tau_d = 15$ ps, the gain calculated by using (4.16) is in general agreement with that simulated by using the nonlinear TOM3 model [102]-[106] for pHEMTs and distributed transmission-line model for the delays. In both cases, the gain at a center frequency of 4.17 GHz is estimated to be 16.5 dB.

Eq. (4.16) differs from (4.12) in terms of not only w_i , but also τ_d . Fig. 4.9 shows also the gain calculated by using (4.16) without τ_d . It can be seen that with τ_d reduced from 15 ps to 0, the peak gain increases from 16.5 dB to 18.6 dB. This shows that the layout of the distributed amplifier can be further optimized to minimize τ_d and to maximize the gain and efficiency of the synthesizer.

Fig. 4.10. Drain characteristics of the pHEMT overlaid with load lines optimized for (a) 1.5 V input with 3-V supply and (b) 2 V input with 5-V supply

Given the same gain but a lower PRF, the input pulse amplitude can be increased to boost the output pulse amplitude without violating the FCC regulation. Under a gain of 16.5 dB and a PRF of 10 MHz, a 1.5-V 100-ps Gaussian input pulse with a spectral density of -59 dBm/MHz at 4.17 GHz would result in an output pulse with -42.5 dBm/MHz at 4.17 GHz, which complies with the FCC regulation and agrees with the measured results of Sec. 4.5. If the PRF is reduced from 10 MHz to 5 MHz, the Gaussian input amplitude can be increased from 1.5 V to 2.0 V to maintain the output spectral density of -42.5 dBm/MHz at 4.17 GHz. However, to maintain the

same gain, the supply voltage must also be increased from 3 V to 5 V to accommodate the larger voltage swing as shown in Fig. 4.10. The impedance of the load line is around 23 ohms as discussed in page 110. The $I_{ds} - V_{ds}$ Curve in Fig. 4.10 is obtained by using the TOM3 model which is shown in Fig. 4.11. The datasheet of pHEMT transistor used in this design shows that drain-source current I_{ds} reaches maximum when V_{gs} equals 1 V [95]. The top line of $I_{ds} - V_{ds}$ curve is obtained when V_{gs} equals 1.0 V. In general, the supply voltage must be carefully scaled to provide high output amplitude with high linearity and high efficiency. To verify the above analysis, the fabricated synthesizer was tested under 2.0 V Gaussian input pulse and 5 V supply voltages. The output pulse of the UWB synthesizer is shown in Fig. 4.15.

From Fig. 4.10, the author can conclude that the output voltage swing of the pHEMT transistor reaches maximum level when the drain supply voltage equals 5 V and 2.0 V input Gaussian pulse. This is because the maximum input voltage of the transistor is limited at 1.0 V and hence, the maximum drain-source current of the pHEMT transistor and the 23-Ω load line limits the output voltage swing.

By changing V_{in} from 1.5 V to 2.0 V in Eq. (4.13), the effective input voltage V_{eff} applied to four different pHEMT transistors are $V_{eff1} = 0.72$ V, $V_{eff2} = 1.73$ V, $V_{eff3} = 1.66$ V, $V_{eff4} = 0.64$ V. With the transconductance $g_m = 80$ ms, Eq. (4.14) shows that the current through each pHEMT is 57.6 mA, 138.4 mA, 132.8 mA and 51.2 mA,

respectively. With effective drain impedance of $23\ \Omega$, the output voltage for each pHEMT is 1.32 V, 3.18 V, 3.05 V and 1.18 V, which match the measured results in Section 4.5.

TOM3_Model

TOM3

NFET=yes	Plk=1.5 V	Cds=0.000234 pF	Betatce=	wldsmax=
PFET=no	Kgamma=0.01194	Tau=0.001 nsec	Xti=2	wPmax=
Tnom=	Taugd=1000 nsec	Rd=	Eg=0.8	AllParams=
Ugw=1 um	Ctau=	Rdtc=	Imax=	
Ngf=1	Qgql=8.58E-16	Rg=	Fnc=	
Vto=-0.6471 V	Qgqh=7.349E-16	Rgmet=	R=	
Alpha=3.053	Qgi0=2.002E-6	Rs=	P=	
Beta=0.000682	Qgag=2.21	Rstc=	C=	
Lambda=-0.02432	Qgad=2.241	Is=1E-11 mA	Kf=	
Gamma=0.03358	Qggb=144.55	Eta=	Af=	
Q=0.9352	Qgcl=7.715E-17	Alphatce=	Ffe=	
K=4.279	Qgsh=8.451E-16	Gammac=	wVgfw=	
Vst=0.05677	Qgdh=2.073E-17	Msttc=	wBvgs=	
Mst=0.2041	Qgg0=1.227E-16	Vsttc=	wBvgd=	
Ilk=1.8E-6 mA	Capmod=	Vtotc=	wBvds=

Fig. 4.11. TOM3 model of the packaged transistor [102]

4.5 Measurement Result

Fig. 4.12(a) shows a photograph of the synthesizer fabricated with $n = 4$, $\tau_2 = 60$ ps, $\tau_g = 240$ ps, and $\tau_d = 15$ ps. The circuit size is approximately 20 mm $\times$ 30 mm. The delay τ_g is through a 29-mm 50- Ω microstrip line on an alumina substrate with a thickness of 0.254 mm and a dielectric constant of 9.9. As shown in Fig. 4.12(b), this line meanders within an area of 4 mm $\times$ 8.3 mm. The delay τ_2 is through a 9.4 mm long 50- Ω microstrip line with 2.4 mm on the alumina substrate and the remainder on a Roger RO4003C substrate with a thickness of 0.508 mm and a dielectric constant of 3.55. The main reason to involve the RO4003C substrate is to make it easy to place the passive surface mount components needed in the design.

(a)

(b)

Fig. 4.12. (a) Photograph of the fabricated distributed UWB pulse synthesizer (b) Dimension of the meander line τ_g

The fabricated synthesizer was first tested with a 1.5-V 100-ps Gaussian input and a 10-MHz PRF. The Gaussian input pulse is shown in Fig. 4.13. As discussed in Section 4.4, the supply voltage was optimized at 3 V in this case. Fig. 4.14 shows the measured output waveform and spectrum. The peak-to-peak amplitude is 4.5 V and the full width at half maximum is 1.0 ns. The center frequency and 10-dB bandwidth are 4.0 GHz and 1.9 GHz, respectively, in compliance with the FCC low-band mask. The measured current consumption is 1 mA, which corresponds to an efficiency of 17% as defined by (4.1).

Fig. 4.13. Measured 1.5 V and $\sigma=100$ ps Gaussian input pulse shape

The same synthesizer was next tested with a 2-V 100-ps Gaussian input and a 5-MHz PRF. Fig. 4.15 shows the measured output waveform and spectrum. The peak-to-peak voltage is 6.4 V and the full width at half maximum remains at 1.0 ns. The spectrum remains in compliance with the FCC mask. The measured current consumption is 0.8 mA, which corresponds to an efficiency of 13%.

As verified in the above, the supply voltage can be scaled to provide higher output amplitude with high linearity and high efficiency under different input conditions. This can be accomplished by laying out additional circuitry to adjust the input amplitude and PRF for different applications and to adaptively control the supply voltage for the pulse synthesizer according to the chosen input amplitude and PRF. Such adaptive control of the supply voltage has been used to improve the linearity and efficiency of RF power amplifiers [107]. The adaptive control circuitry can be best implemented in monolithically microwave integrated circuits (MMICs).

For expeditious and low-cost proof of concept, the proposed synthesizer was demonstrated by using discrete pHEMTs. Using MMICs, the pulse generator can be integrated with the pulse synthesizer to facilitate adaptive control of the supply voltage. In addition, parasitic delays such as τ_d can be minimized for maximum gain and efficiency. In this case, higher-impedance transmission lines can be used to minimize the die size but must be carefully traded off against additional loss.

(a)

(b)

Fig. 4.14. Measured output (a) waveform and (b) spectrum of the distributed UWB pulse synthesizer with 1.5-V 240-ps Gaussian input, 10-MHz PRF and 3-V supply. The rectangle-shaped FCC spectral mask is overlaid in (b) as a reference

(a)

(b)

Fig. 4.15. Measured output (a) waveform and (b) spectrum of the distributed UWB pulse synthesizer with 2.0-V 240-ps Gaussian input, 5-MHz PRF and 5-V supply. The rectangle-shaped FCC spectral mask is overlaid in (b) as a reference

4.6 Conclusions

The above theoretical analysis and measured results confirm that the proposed distributed UWB pulse synthesizer is capable of higher output amplitude and efficiency than many other UWB pulse generators. Using 0.25- μm pHEMTs, a prototype synthesizer has been designed and fabricated with a center frequency of 4.0 GHz and a bandwidth of 1.9 GHz. Under a Gaussian input pulse of 1.5 V and 100 ps pulse width, the synthesizer outputs into 50 Ω a Gaussian derivative pulse centered at 4 GHz with peak to peak amplitude of 4.5 V and 1 ns pulse envelope width. At a pulse-repetition frequency of 10 MHz, the synthesizer consumes 1 mA at 3 V with 17% efficiency. In addition, the supply voltage can be adaptively controlled to improve the linearity and efficiency of the proposed synthesizer.

CHAPTER 5

High Peak Power Monolithic Microwave Integrated Circuits UWB Pulse Synthesizer Designs

For positioning and localization application, there is no need for high data rate. But instead of high data rate, the high peak power can help increase the distance of positioning and localization system. Hence the high peak power and low pulse repetition frequency UWB pulse synthesizer is essential for UWB positioning and localization application system.

The prototype circuit of the distributed UWB pulse synthesizer in chapter 4 is built on 0.25- μm discrete pHEMT transistor dies. The circuit can be built in Monolithic Microwave Integrated Circuits (MMIC) form except the gate delay element τ_g . Using MMIC, the drain delay element τ_d can be designed to be close to 0 ps and hence, the center frequency and the -10 dB bandwidth of the distributed UWB pulse synthesizer can be designed more accurately. Both pHEMT and Hetero-junction Bipolar transistors (HBT) technology can be used to build the MMIC circuit of the distributed UWB pulse synthesizer.

Subrata Halder and some other researchers reported that order-of-magnitude improvement in power capacity can be achieved in single-finger HBT with less than 1-us pulses and <1% duty cycle, thereby approaching isothermal operation [108]-[115]. Without self heating, high-current and high-voltage I-V characteristics are governed by Kirk effect [116] and impact ionization [117]. In [119], Renfeng Jin reported that under true isothermal operation, GaAs HBTs were shown to survive strong impact ionization and have a much larger safe operating area than previously measured or predicted. An empirical model for impact ionization was constructed based on sub-nanosecond pulse characterization in [119]. The model can predict the HBT characteristics across the enlarged safe operating area, including strong avalanche breakdown and flyback. This chapter will use the same HBT transistor that was characterized in [119] to design the UWB pulse synthesizer to deliver high output voltage pulse.

In fact the distributed UWB pulse synthesizer is approaching isothermal operation because the input pulse is much shorter than 1-us and the duty cycle of the pulse is less than 1% with low PRF. Hence with HBT technology, the distributed UWB pulse synthesizer shows the potential to generate much higher peak power UWB pulse using transistors of small geometry.

5.1 Analysis of High Peak Power UWB Pulse Synthesizer

Fig. 5.1 shows the circuit schematic of the high peak power UWB pulse synthesizer for implementation in MMIC.

Fig. 5.1. The circuit schematic of the HBT UWB pulse synthesizer

In Fig. 5.1, the common-base configuration is employed in the output stage because higher output power can be achieved using common-base configuration compared with common-emitter configuration [108]. In order to better fit FCC peak power spectrum mask, a simple on-chip L-C high pulse filter was employed at the output of the UWB pulse synthesizer.

A single stage UWB pulse synthesizer as shown in Fig. 5.2 is isolated to facilitate the analysis of peak power performance. In order to simplify the analysis, a 50- Ω collector termination resistor (indicated in blue color) is added to the circuit as shown in Fig. 5.2.

Fig. 5.2. Single stage UWB pulse synthesizer with 50- Ω Collector termination resistor (indicated in blue color) or with short circuited stub (indicated in red color)

Fig. 5.3. The safe operating area of the HBT (2 μ m x 20 μ m x 1), Simulated Characteristics by using the Agilent HBT model with () and without (----) impact ionization are included in Figure [119]

For field-effect transistors, the output power is limited by a well-defined maximum current I_{MAX} , which is shown in Chapter 4. The output power of the pHEMT transistor is limited by the maximum current I_{MAX} which occurs at $V_{GS}=1.0$ V. Unlike field-effect transistors, bipolar transistors generally do not have a hard I_{MAX} limit. Instead, power limitation is governed by the safe operation area of the HBT transistor [117], [119]. A commercial HBT foundry is used in this chapter [118]. Fig. 5.3 shows the safe operating area of the commercial HBT (2 μ m x 20 μ m x 1) [119].

A 2.45-V 100-ps Gaussian input pulse is applied at the input with 100 KHz PRF. The Gaussian input pulse width is the full width at half maximum. The bias voltages V_B and V_C of the transistor B in Fig. 5.2 are optimized to 3.8 V and 9.5 V respectively.

The method of bias voltage optimization is explained later. Fig. 5.4 shows the simulated output Waveform V_{out} across the 50- Ω load R_L . Fig. 5.5 overlays the simulated dynamic load line of the output stage transistor B in Fig. 5.2 with the safe operating area of the HBT shown in Fig. 5.3. From Fig. 5.5, it can be seen that the HBT is under safe operation area with 2.45-V 100 KHz PRF Gaussian input.

Fig. 5.4. Simulated output Waveform of the single stage UWB pulse synthesizer with 50- Ω collector termination resistor

Fig. 5.5. Simulated dynamic load line of the output stage transistor B with 50- Ω collector termination resistor in Fig. 5.2. The safe and unsafe operation area of the transistor is overlaid as the reference.

Fig. 5.6. Simulated output Waveform of the single stage UWB pulse synthesizer with short circuited stub.

Fig. 5.7. Simulated dynamic load line of the output stage transistor B with short circuited stub.

The safe and unsafe operation area of the transistor is overlaid.

To generate the positive output waveform half cycle, the 50-Ω Collector termination resistor in Fig. 5.2 is removed and replaced with a short circuited stub (indicated in red color). Fig. 5.6 shows the simulated output waveform V_{out} across 50-Ω load R_L where the 6.5-V positive polarity pulse indicated in red color is due to the reflection of signal from the short circuited stub. This 6.5-V positive polarity pulse increases the maximum voltage that appears across the collector-emitter junction of transistor B. Fortunately, when the 6.5-V positive polarity pulse is reflected back from the short circuited stub and appears across the collector-emitter junction of the transistor B, the Gaussian input pulse is off and the collector current of the transistor B is 0.

Hence transistor B is still under safe operation area. Fig. 5.7 shows the simulated dynamic load line of the output stage transistor B without 50- Ω collector termination resistor overlaid with the safe operating area of the HBT shown in Fig. 5.2.

The bias voltages V_B and V_C of the transistor B are optimized to minimize the DC power consumption and at the same time are designed to be high enough to accommodate different levels of Gaussian input pulses. The optimized bias voltages V_B and V_C have to satisfy the following two criteria: (a) the peak collector current of the transistor A does not increase after the optimum bias voltage V_B (b) the peak collector current of the transistor B saturates after the optimum bias voltage V_C . If the optimum bias voltage V_C makes the transistor enter the unsafe operation area, it means that the Gaussian input level is too high and the peak collector current of the transistor B is clamped if the transistor is biased within safe operation. Hence the Gaussian input level is reduced and the process of the optimization is repeated to find the optimum bias voltages V_B and V_C .

Fig. 5.8 shows the simulated collector current of the transistor A with different bias voltage V_B in Fig. 5.2. Hence the peak collector current of the transistor A does not increase after $V_B = 3.8$ V. the optimum bias voltage V_B is 3.8 V.

Fig. 5.8. Simulated dynamic load line of the transistor A without 50- Ω collector termination resistor in Fig. 5.2 at 2.45 V Gaussian input pulse and different bias voltage V_B . The safe and unsafe operation area of the transistor is overlaid as the reference.

By fixing the bias voltage V_B at 3.8 V, the bias voltage V_C is increased and then the simulated dynamic load line of the transistor B is plotted as Fig. 5.9. Fig. 5.9 shows that the peak collector current of transistor B is increased when V_C is increased from 8.5 V to 9.5 V and then saturated when V_C is increased from 9.5 V to 10.5 V. And when $V_C = 9.5$ V, the dynamic load line of the transistor B is just going to touch the unsafe operation area of the transistor. Hence the optimum bias voltage V_C is 9.5 V and the maximum level of Gaussian input pulse does not clamp the output is 2.45 V.

Fig. 5.9. Simulated dynamic load line of the transistor B without 50- Ω collector termination resistor in Fig. 5.2 at 2.45 V Gaussian input pulse and different bias voltage V_C when $V_B = 3.8$ V. The safe and unsafe operation area of the transistor is overlaid as the reference.

The different amplitudes of Gaussian input pulse, the bias voltages are optimized by using the above discussed process. Fig. 5.10 shows the simulated output pulse amplitude (peak to peak) of the single stage UWB HBT pulse synthesizer as a function of input pulse amplitudes and corresponding bias voltages V_B and V_C of the transistor B shown in Fig. 5.2. It can be seen that the output amplitude increases linearly with the input amplitude up to approximately 13 V. From Fig. 5.7, it can be seen that the output amplitude of the single stage UWB HBT pulse synthesizer is eventually clamped at 13 V. If the bias voltage of the V_B and V_C of the transistor B

are increased further to accommodate the larger than 2.45-V Gaussian input, the HBT transistor is going to enter the unsafe operation area shown in Fig. 5.7.

Fig. 5.10. Simulated output pulse amplitude of the single stage UWB HBT pulse synthesizer shown in Fig. 5.2 (with short-circuit stub) as a function of input pulse amplitudes and corresponding bias voltage V_B and V_C of the transistor B.

5.2 Design Example of High Peak Power UWB Pulse Synthesizer

By employing the method discussed in Chapter 4, the following chapter shows three design examples by using the commercial HBT (2 μ m x 20 μ m x 1) [119].

5.2.1 UWB Low Band Pulse Synthesizer

The circuit schematic of the UWB low band (3-5 GHz) pulse synthesizer is shown in Fig. 5.1. The size of the transistor used in the pulse synthesizer is 2 μ m x 20 μ m x 1. The delay elements τ_2 and τ_g are designed as 60 ps and 120 ps respectively. Fig. 5.11 shows the simulated output waveform and spectrum of the distributed HBT UWB pulse synthesizer with 2.45-V 100-ps 100-KHz PRF Gaussian input. The maximum peak power allowable by FCC is 0 dBm/50MHz and the peak rectangle-shaped FCC low band peak power spectral mask is overlaid in Fig. 5.11(b). The simulation result shows that the peak to peak amplitude of the output pulse can reach 13 V. And the simulated DC power consumption is only 46 μ W.

(a)

(b)

Fig. 5.11. Simulated output (a) waveform and (b) spectrum of the distributed UWB pulse synthesizer with 2.45-V 100-ps Gaussian input. The rectangle-shaped FCC low band peak power spectral mask is overlaid in (b) as a reference.

In order to examine the power efficiency of the HBT UWB pulse synthesizer, the author inserts current probe (purple color) into the circuit as shown in Fig. 5.1. The DC power consumption is obtained by integrating voltage current product over 500-ns window and then divides by the I/PRF time window, which is 10-us. The RF power of the output pulse is obtained in a similar way. Table 5.1 shows the calculation of the power efficiency in Agilent ADS. The simulation results show that the HBT UWB pulse synthesizer has the amazing potential to generate the 13-V peak to peak amplitude UWB pulse with power efficiency as high as 27%.

Eqn $P_{dc} = \text{integrate}(10 \cdot I_{bias}, 45\text{ns}, 545\text{ns}, 10\text{ps}) / 10000\text{e-9}$

Eqn $P_{out} = \text{integrate}(V_{out} \cdot \text{conj}(V_{out}/50), 45\text{ns}, 545\text{ns}, 10\text{ps}) / (10000\text{e-9})$

Eqn $\text{Efficiency} = P_{out} / P_{dc} \cdot 100$

Pdc	Pout	Efficiency
0.000046	0.000012	26.989580

Table 5.1. Power efficiency calculation of UWB low band HBT pulse synthesizer in Agilent ADS

Fig. 5.12 shows the layout of the designed UWB low band HBT pulse synthesizer.

Fig. 5.12. The layout of the UWB low band (3-5 GHz) HBT pulse synthesizer

5.2.2 UWB High Band Pulse Synthesizer

The circuit schematic of the UWB high band (6-10.6 GHz) HBT pulse synthesizer is same as the circuit schematic of the UWB low band (3-5 GHz) pulse synthesizer.

The size of the transistor used in the pulse synthesizer is $2\mu\text{m} \times 20\mu\text{m} \times 1$. The delay elements τ_2 and τ_g are designed as 30 ps and 120 ps respectively. In order to better fit the FCC spectrum mask, a simple on-chip L-C high pulse filter was also employed at the output of the UWB pulse synthesizer. Fig. 5.13 shows the simulated output waveform and spectrum of the distributed HBT UWB pulse synthesizer with 2.45-V 100-ps Gaussian input. The simulation result shows that the peak to peak amplitude of the output pulse can reach above 10 V. The simulated DC power consumption is only 53 uW. The simulated power efficiency of the UWB pulse synthesizer is 18%. Table 5.2 shows the calculation of the power efficiency in

Agilent ADS.

(a)

(b)

Fig. 5.13. Simulated output (a) waveform and (b) spectrum of the distributed UWB pulse synthesizer with 2.45-V 100-ps Gaussian input. The rectangle-shaped FCC peak power spectral mask is overlaid in (b) as a reference.

$$\text{Eqn } P_{dc} = \text{integrate}(10 \cdot I_{bias}, 45\text{ns}, 545\text{ns}, 10\text{ps}) / 10000\text{e-9}$$

$$\text{Eqn } P_{out} = \text{integrate}(V_{out} \cdot \text{conj}(V_{out}/50), 45\text{ns}, 545\text{ns}, 10\text{ps}) / (10000\text{e-9})$$

$$\text{Eqn } \text{Efficiency} = P_{out} / P_{dc} \cdot 100$$

Pdc	Pout	Efficiency
0.000053	0.000009	17.647022

Table 5.2. Power efficiency calculation of UWB high band HBT pulse synthesizer in Agilent ADS

Fig. 5.14 shows the layout of the designed UWB high band HBT pulse synthesizer.

Fig. 5.14. The layout of the UWB high band (6-10.6 GHz) pulse synthesizer

5.2.3 UWB Full Band Pulse Synthesizer

Fig. 5.15 shows the circuit schematic of the UWB full band (3.1-10.6 GHz) pulse synthesizer. The size of the transistor used in the pulse synthesizer is $2\mu\text{m} \times 20\mu\text{m}$ $\times 1$. The delay elements τ_2 and τ_g are designed as 37.5 ps and 150 ps respectively. In order to better fit the FCC spectrum mask, a simple on-chip L-C high pulse filter was also employed at the output of the UWB pulse synthesizer. Fig. 5.16 shows the simulated output waveform and spectrum of the distributed HBT UWB pulse synthesizer with 2.45-V 100-ps Gaussian input. The simulation result shows that the peak to peak amplitude of the output pulse can reach 11.3 V. The simulated DC power consumption is only 22 μW . The simulated power efficiency of the UWB pulse synthesizer is 37%. Table 5.3 shows the calculation of the power efficiency in Agilent ADS.

Fig. 5.15. The circuit schematic of the UWB full band (3.1-10.6 GHz) pulse synthesizer

(a)

(b)

Fig. 5.16. Simulated output (a) waveform and (b) spectrum of the distributed UWB pulse synthesizer with 2.45-V 100-ps Gaussian input. The rectangle-shaped FCC peak power spectral mask is overlaid in (b) as a reference.

$$\text{Eqn } P_{dc} = \text{integrate}(10 \cdot I_{bias}, 45\text{ns}, 545\text{ns}, 10\text{ps}) / 10000\text{e-9}$$

$$\text{Eqn } P_{out} = \text{integrate}(V_{out} \cdot \text{conj}(V_{out}/50), 45\text{ns}, 545\text{ns}, 10\text{ps}) / (10000\text{e-9})$$

$$\text{Eqn } \text{Efficiency} = P_{out} / P_{dc} \cdot 100$$

Pdc	Pout	Efficiency
0.000022	0.000008	36.631503

Table 5.3. Power efficiency calculation of UWB full band HBT pulse synthesizer in Agilent ADS

Fig. 5.17 shows the layout of the designed UWB full band HBT pulse synthesizer.

Fig. 5.17. The layout of the UWB full band (3.1-10.6 GHz) pulse synthesizer

CHAPTER 6

Conclusions and Future Directions

6.1 Conclusions

In this dissertation, two key components for RF front end of ultra-wideband (UWB) wireless system are presented. One is a high gain and low noise amplifier (LNA) and the other one is a high-voltage and high-efficiency distributed UWB pulse synthesizer.

The designed UWB LNA covers the whole FCC frequency mask from 3.1 GHz to 10.6 GHz and employs 0.15- μm low noise pHEMT technology. The size of the

fabricated UWB LNA including DC pads is $0.9 \text{ mm} \times 2.5 \text{ mm} = 2.25 \text{ mm}^2$. The first stage of the UWB LNA was designed by employing a resistive shunt feedback topology together with two T sections low pass structure in order to match to $50\text{-}\Omega$ antenna. This topology improves the noise performance compared to the traditional distributed input stage. And the second stage is implemented in common source configuration in order to achieve the higher gain compared to common gate configuration. Finally the distributed output matching topology is to drive an external $50\text{-}\Omega$ antenna. Current sharing design of the two stages is employed to reduce the power consumption of the UWB LNA, in other words, to improve the efficiency of the UWB LNA. And the amplifier can be operated from a single positive supply without the need to have both positive and negative power supply to separate bias gate and drain by using self-bias mode. The 3.1-10.6 GHz $0.15\text{-}\mu\text{m}$ pHEMT MMIC amplifier has state of the art performance consuming only 12.9 mW of power. The power gain is 12.5 dB with gain flatness of $\pm 0.5 \text{ dB}$, and noise figure is below 4.0 dB. The input $P_{1\text{dB}}$ compression point at 7 GHz is -20.5 dBm. The IIP3 point at 7 GHz is -10.4 dBm. It has excellent input and output return loss of better than 12 dB and 15 dB respectively except at the high end of the band. Group delay is around $184 \text{ pS} \pm 28 \text{ pS}$, coupled with flat gain performance, resulting in very good pulse response.

And a new practical way to characterize the degree of pulse distortion introduced by the UWB LNA is carried on the designed UWB LNA. The real FCC compliance

UWB pulse is used as the characterization source. The pulse response characterization uses a time domain sampling oscilloscope with the delays and losses of cables and probes corrected in frequency domain. The correction procedure is verified by using a “through” standard. The exact similarity of the input and output pulses of the UWB LNA is qualified by the correlation coefficient of the input and output pulses. The characterization results show that the correlation coefficient of the input and output pulses can maintain higher than 0.9 when the peak to peak voltage of the input pulse is increased to 108 mV. And the simple investigation done in ADS shows that the high pass filter can be implemented in the output of the UWB LNA to improve the correlation coefficient of the input and output pulses when the peak to peak voltage of the input pulse is high. The high pass filter can be implemented by using UWB antenna easily.

And then the dissertation focuses on presenting a novel UWB pulse synthesizer based on distributed amplifier topology. The basic concept is to combine different delayed Gaussian pulses with both positive and negative polarities to form an UWB pulse. The center frequency and -10 dB bandwidth of the output UWB pulse can be designed by varying the delays between each pulse and the number of delayed Gaussian pulses. Compared to other UWB pulse generators, the present synthesizer is capable of higher voltages and higher efficiencies. And the frequency domain characteristic of the proposed UWB pulse synthesizer method is analyzed extensively to show that the center frequency and -10 dB bandwidth of the output

pulse can be adjusted. Using 0.25- μm pHEMTs, a prototype synthesizer has been designed and fabricated with a center frequency of 4.0 GHz and a bandwidth of 1.9 GHz. Under a Gaussian input pulse of 1.5 V and σ -100 ps, the synthesizer outputs into 50 Ω a pulse of 4.5 V and 1 ns. At a pulse-repetition frequency of 10 MHz, the synthesizer consumes 1 mA at 3 V with 17% efficiency. Approaches to maintain high efficiency by scaling the supply voltage for different input amplitudes and pulse-repetition frequencies have also been verified experimentally.

Finally, the dissertation opens a discussion on designing high-voltage UWB pulse synthesizer by using HBT technology. The simulation results show that the HBT UWB pulse synthesizer has the amazing potential to generate about 12.5-V peak to peak amplitude UWB pulse with power efficiency as high as 27% in lower UWB band (3-5 GHz). And the similar simulation results for higher UWB band (6-10.6 GHz) and full UWB band (3.1-10.6 GHz) are also presented.

6.2 Future Directions

In the conclusions of Chapter 3, the author measured the main difference between the input and output pulse spectrum is the low frequency part, and simple investigation done in ADS shows that high pass filtering can be performed at the output of the fabricated UWB LNA to improve the correlation coefficient of the input and output pulses. In the UWB system design, the UWB antenna can be

designed to serve as a simple high pass filter. Hence the simple investigation done in ADS shows that there is possibility to co-design the UWB LNA and antenna to improve the linearity of the UWB system.

And from Chapter 5, it emerges that a high-voltage UWB pulse synthesizer can be designed by using HBT technology. This is because the commercially available high yield InGaP/GaAs HBT can deliver very impressive power density when the HBT is under isothermal operation. The feature was studied in [119]. Chapter 5 used the same size HBT transistor based on the same foundry process in [119] and referred to the measurements results shown to design the high-voltage UWB pulse synthesizers. In the future, the similar measurement can be carried out on different sizes HBT transistors based on different HBT foundry processes. And the possibility to achieve even higher output pulse can be explored.

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