Fabrication and characterization of InP-based high electron mobility transistors

Liu, Yuwei

2009

Liu, Y. (2009). Fabrication and characterization of InP-Based high electron mobility transistors. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/46750>

<https://doi.org/10.32657/10356/46750>

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FABRICATION AND CHARACTERIZATION OF InP-BASED HIGH ELECTRON MOBILITY TRANSISTORS

LIU YUWEI

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

A thesis submitted to the Nanyang Technological University

in fulfillment of the requirement for the degree of

Doctor of Philosophy

2009

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other university or institution.

04/06/2009

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Acknowledgements

I would like to express my sincere gratitude to a number of people during my study at Nanyang Technological University, without their support and cooperation this work could not have been completed.

At the top of the list, I am very grateful to my supervisor Associate Professor Wang Hong for his foresight, wisdom, guidance, and enthusiasm. His broad knowledge and diligent effort has led me into the field of high frequency transistors. Most importantly, He always helps me with kindness and many fresh ideas to overcome a lot of problems in front of me. Without his invaluable suggestions and support, this work would not have been successful.

I would like to thank all the MMIC group members, Ms. Bu Jing, Ms Zeng Rong, Mr. Cheong Wai Cye, Mr. Tan Chee Leong, Dr. Yuan Kaihua, Dr. Tian Yuan, Dr. Yang Hong, and Dr. Neo Wah Peng, Ms. Ng Chai Wai for their valuable help, discussion, suggestion and friendship. In particular, my greatest gratitude goes to Dr. Lew Kim Luong, Mr. Tan Kian Hua and Dr. Loke Wan Kai.

I would not underestimate the contribution of all the clean room technicians, Mr. Muhd Fauzi Bin Abdullah, Mr. Mohamad Shamsul bin Mohamad, Madam Tan-Cheah Ai Mai, and Madam Lynn Lim-Lim Geok Hwon, Serene for maintaining all the equipment in this lab and keeps an ample supply of clean room chemicals and other materials.

Finally, I owe much to my parents for their endless devotion and encouragement. Most importantly, I express thanks to my husband for his support and encouragement.

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Summary

InP-based high electron mobility transistor (HEMT) is an important device in high frequency and low noise applications. In current work, studies on InP-based InGaAs single channel HEMT and InGaAs/InP composite channel HEMT were carried out. Some important issues such as the thermal stability of InGaAs/InP composite channel HEMT, surface passivation effect on InGaAs/InP composite channel HEMT, high-frequency noise of InP HEMT, and suppress of thermal noise in InGaAs/InP composite channel HEMT were investigated. They are summarized as following:

(1) Thermal stability of InGaAs/InP composite channel HEMT

InGaAs single channel HEMT and metamorphic InGaAs/InP composite channel HEMT structures were subjected to RTA treatment. Electrical and low-temperature PL measurements were used to probe the variation of material properties. It was revealed that, for RTA temperature lower than 550°C, the composite channel HEMT structures exhibit similar degradation behaviors as lattice-matched HEMT structures, i.e., decreases in n_s and PL intensity, which is presumably due to fluorine passivation of Si donors in the InAlAs barrier layer. However, for RTA temperature higher than 550°C, contrary to lattice-matched InP/InGaAs HEMT, the metamorphic HEMTs exhibit no further reduction of n_s and show improvement in PL intensity, which can be explained as a consequence of the dislocation network (gettering sink) located immediately beneath the device zone. As a whole, the metamorphic HEMT samples show less degradation as compared to the lattice-

matched HEMT, which may partially ease the concerns on the thermal stability of the metamorphic HEMT structures.

(2) Surface Passivation effect on transport properties in InGaAs/InP composite channel HEMT

The influence of SiN passivation on electron mobility of InGaAs/InP composite channel HEMT structures has been studied. An increase in effective mobility μ_e with a negligible change of sheet carrier density after SiN deposition is observed, which is different from the previous report on the InGaAs single channel structure. PL measurements were carried out on the different passivated samples. The variations of the PL peak position, the transition intensity, and the linewidth were analyzed to clarify the mechanism for the change in electrical properties. The results suggest that the enhancement of μ_e could be explained under the framework of electrons transfer from the InP sub-channel into InGaAs channel region due to the energy band bending at surface region caused by SiN passivation.

(3) Understanding of excess channel noise in InGaAs HEMT in impact ionization regime

The characterization and analysis of high frequency noise of InP-based high electron mobility transistors in the impact ionization regime reveal that different physical mechanisms are responsible for the excess channel noise at different frequency ranges. The excess noise at frequencies below 10GHz is mainly due to hole recombination in the channel. However, excess channel noise at higher frequencies could be dominated by the

fluctuation of impact ionization which has a much smaller time constant and therefore a much higher cutoff frequency.

(4) Suppress of thermal noise in InGaAs/InP composite channel HEMTs.

Detailed microwave noise characteristics of InP-based HEMT with single channel and composite channel are presented. A modeling of noise figure is carried out to extract the noise parameters and study the impact of channel structure on channel thermal noise of InP-based HEMT. Characterization of noise performance of InGaAs/InP composite channel HEMTs reveals a different bias dependence of $NF_{\min}$ compared to conventional single InGaAs channel devices. The composite channel HEMT shows a lower $NF_{\min}$ at high V_d with a relatively weak V_d dependence. This could be explained under the framework of suppression channel thermal noise due to the electron transfer from InGaAs channel to InP sub-channel at high V_d .

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Chapter 1 Introduction

With the discovery of a two-dimensional electron gas (2DEG) [1] at the AlGaAs/GaAs heterostructure interface in the low-band-gap GaAs side in 1978, and with the advent of the molecular beam epitaxy (MBE) growth technique for III-V compound semiconductors, significant progress has been made in the realization of a large variety of heterostructure high electron mobility transistors (HEMT). InP-based HEMTs are important microelectronic devices due to its superior high frequency characteristics, including the high maximum frequency of oscillation $f_{\max}$ (e.g. 600GHz as reported in [2]), the high cutoff frequency (e.g., $f_T > 550\text{GHz}$ as reported in [3]) and the low noise figure and high efficiency at millimeter wave frequency [4]. The superior performance of the InP-based HEMT arises directly from the intrinsic properties of the InAlAs/InGaAs material system. InGaAs channel with high indium content possesses high electron mobility and high electron velocity. Large conduction band discontinuity at the InGaAs/InAlAs heterojunction permits high 2DEG density to be obtained. These properties enable high current and transconductance resulting in high cut-off frequency and power at high frequency.

1.1 Motivation and Objectives

InP HEMTs have demonstrated superior performances, however, there still exists need and possibility to overcome certain disadvantages and improve performances. The high cost, limited size and brittle nature of InP substrate bring difficulties to lower cost and high volume production. In order to overcome these drawbacks, growing InP-based HEMTs on GaAs substrate, the so-called metamorphic HEMT (MHEMT) technique has

attracted large attention in recent years. By using a compositionally graded metamorphic buffer on a GaAs substrate, the technique provides a growth surface with a lattice constant equal/close to InP. The buffer is designed and grown to accommodate most of the strain that brings as less dislocation as possible to the top HEMT device layers. With a suitable buffer technique, MHEMTs have exhibited performances comparable to that of the devices based on InP substrate, including high gain, low noise and excellent power performance [5].

On the other hand, the microwave performance of InP-based HEMTs is limited by relatively low breakdown and high output conductance. The off-state and on-state breakdown voltages in InP-based HEMTs have been shown to be dominated by impact ionization in the channel layer, and are typically low due to the low breakdown field of narrow bandgap $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel. This results primarily from the high impact ionization coefficient of the InGaAs channel. To overcome this weakness, a composite channel consisting of an InGaAs channel and an InP subchannel was proposed and demonstrated. The most important feature of such a structure is that, at high electric field, more electrons accumulate in InP subchannel, and current path can switch from InGaAs channel to InP subchannel, which has high drift velocity and low impact ionization. It had been demonstrated that, by using the InGaAs/InP composite channel structure, the device breakdown voltage, frequency performance and output power could be remarkably improved.

Although MHEMT and composite channel-HEMT (CC-HEMT) have shown improvement in some devices performances, more studies on these structures are still needed to achieve deeper understanding and better performances. In this work, studies on InP-based single-channel HEMT, composite channel HEMT, and MHEMT were mainly focused on several issues as follows:

1.1.1 Thermal Stability of MHEMT structure

MHEMT technique is driven by interests in lower substrate cost of GaAs, a more matured backside process, and high flexibility for the energy band engineering. At the same time, however, since metamorphic buffer may induce additional surface and interface roughness and residual strain, the post growth stability of the metamorphic structure as well as device reliability become a major concern for the practical application of metamorphic technology. The stability of metamorphic structures is not yet thoroughly investigated. There is only a very limited experimental information available concerning thermal stability of the metamorphic HEMT structures. In a MHEMT structure, where a dislocation network is located immediately beneath the active device region (0.5-1 μm away) in the metamorphic buffer, it is unclear whether the dislocations will cause a negative/positive effect on the device quality. In order to have a better understanding on this issue, a comparison studies has been made on the same HEMT structures grown on InP substrate, and on GaAs substrate with metamorphic buffer.

1.1.2 Influence of SiN passivation on the transport properties of 2DEG in a composite channel HEMT structure

Passivation of the electronic device is important to improve the device performance and long-term reliability by preventing the device degradation induced by the environment and mechanical scratches. In a typical InP-based HEMT structure, InAlAs serves as the barrier layer to form a good Schottky gate. It has been found that the exposed InAlAs recess areas immediately next to the gate plays a critical role in determining the device characteristics such as I-V kink and gate leakage [6]. Although passivation of InP-based devices using plasma enhanced chemical vapor deposition (PECVD) silicon nitride

(SiN) has been used at production level, information on whether SiN passivation alters surface potential and surface Fermi level and how the SiN passivation affects the carrier transport in a HEMT structure is till very limited. A better understanding of the influence of SiN passivation on InAlAs/InGaAs HEMT structures and its physical origin is necessary for design, fabrication, and parameter optimization of InP HEMTs to further enhance the device performance. In the case of composite channel HEMT, the use of InP in channel region may pose a question whether the use of composite channel will result in the deterioration of the damage resistance of InP-based HEMT subjected to plasma process, since it has been found that InP material exhibits much lower resistance to plasma damage as compared to InAlAs. Therefore, it is important to assess and study the influence of SiN surface passivation on the electronic properties of the 2DEG in an InAlAs/InGaAs/InP CC-HEMT structure.

1.1.3 Origin of excess noise in InAlAs/InGaAs/InP HEMT in impact ionization regime

One of the attractive features of the HEMT as an amplifying device is its very low noise figure at high frequencies. The presence of an excess noise related to impact ionization in InP-based HEMTs has increasingly attracted attention [7,8,9]. It has been found that the enhancement of device noise in the impact ionization regime may substantially affect the device low noise application even at microwave frequencies. However, the origin of the excess noise is still inconclusive. Studies from Rouquette *et al.* [10] show that a time constant as small as 25 ps could be determined by fitting the noise spectral density to the form of Lorentzian function, which suggests the possibility of the excess noise in the impact ionization regime being induced by the fluctuation of impact ionization events. On the other hand, there is also a theoretical study implying that the

excess noise is related to the generation of holes by impact ionization and their further recombination. Therefore, it is of great interest to investigate the excess noise in the impact ionization regime to further understand this topic.

1.1.4 Noise characteristic in the composite channel HEMTs

The noise properties of InP-based HEMTs were analyzed by many researchers. Noise characteristics and models for InP-based lattice-matched and pseudomorphic HEMTs have been reported. However, little attention has been paid on the microwave noise characteristics of InP HEMTs with composite channel. Studies on composite channel HEMTs were mainly carried out to improve the device power performance [11,12,13], and no detailed study was made on InP-based HEMT with composite channel. Therefore, there is a need to study the detailed noise characteristics of composite channel HEMT and investigate whether the special channel structure will influence its noise performance.

1.2 Major Contribution of the Thesis

During this work, efforts and time were spent on the abovementioned research topics through electronic and optical characterization of HEMT structures, fabrication of sub-micron HEMT devices, and characterization of the noise performances of HEMT devices. The major contribution of this thesis can be summarized as follows:

(1) The thermal stability of metamorphic InP/InGaAs HEMT structures on GaAs substrate subjected to rapid thermal annealing has been systematically studied. Based on the characterization of the electrical and optical properties, we have observed that HEMT structures grown on a metamorphic strain-relief buffer exhibit better thermal stability when compared to a lattice-matched structure at annealing temperatures higher than 550°C. The

better thermal stability and enhanced photoluminescence (PL) intensity at high RTA temperatures observed in metamorphic structures suggest possible dislocation-related gettering effect due to the presence of the dislocation network (gettering sink) located immediately beneath the device zone. Our experimental observation may partially ease the potential concerns about the thermal stability of metamorphic HEMTs.

(2) The influence of SiN passivation on the electrical properties of InGaAs/InP composite channel HEMT structures has been studied by Hall measurements and PL measurements. An increase in effective mobility μ_e with a negligible change of sheet carrier density n_s after SiN deposition is clearly observed. The experimental results provide a strong evidence for modification of surface potential towards an unpinned surface, suggesting the presence of relatively low densities of interface states on InAlAs after SiN passivation. In CC-HEMT, the enhancement of μ_e could be a result of electron transfer from the InP subchannel into the InGaAs channel region.

(3) High frequency noise of InP-based HEMT in the impact ionization regime has been characterized. Analysis reveals that different physical mechanisms are responsible for the excess channel noise at different frequency ranges. The excess noise at frequencies below 10 GHz is mainly due to the hole recombination in the channel. However, excess channel noise at higher frequencies could be dominated by the fluctuation of impact ionization which has a much smaller time constant and therefore a much higher cutoff frequency.

(4) A detailed characterization of microwave noise characteristics on composite channel HEMT has been performed. Modeling of noise figure is carried out to extract the device noise parameters and study the impact of channel structure on the channel thermal noise of InP-based HEMT. Compared to conventional single InGaAs channel devices, the

composite channel HEMTs show a lower $NF_{\min}$ at high drain bias (V_d) with a much weaker V_d dependence. This could be explained under the framework of suppression of channel thermal noise due to the electron transfer from InGaAs channel to InP sub-channel at high V_d .

1.3 Organization of the thesis

This thesis is divided into seven chapters. The basic principles of HEMTs operation are reviewed and discussed in chapter 2. Chapter 3 reviews the experimental methods, including submicron InP-based HEMT fabrication process and technology, material characterization techniques, and the DC, RF and noise characteristics techniques of InP-based HEMTs. In Chapter 4, thermal stability of MHEMT was studied through characterization and analysis of electrical and optical properties of MHEMT structures treated by rapid thermal annealing. Chapter 5 reports the effect of SiN passivation on the composite channel HEMT structures, which also provides experimental evidence on modification of surface potential of InAlAs by SiN passivation. In Chapter 6, the channel noise of InP-based HEMT was characterized and analyzed to understand the mechanism of the excess channel noise in impact ionization regime. In chapter 7, characterization and analysis of the noise performance of CC-HEMT structure have been reported in details. The performance difference of CC-HEMT in comparison with a single channel HEMT is studied and explained. Finally, the conclusion of the present work with some suggestions for future work is given in Chapter 8.

Chapter 2 Theoretical Background of HEMT devices

The demonstration of enhanced mobility in modulation doped quantum well structures by Dingle *et al.* in 1978 [1], has sparked a race to produce a high performance transistor based on this phenomenon. In 1980, T. Mimura *et al.* from Fujitsu developed a high electron mobility transistor [14]. Within a relatively short time, several research laboratories had produced their own version of a high mobility transistor with different names for devices. Other names commonly applied to the device include modulation doped field effect transistor (MODFET), selectively doped heterojunction transistor (SDHT), two dimensional electron gas FET (TEGFET). Frequently, it is referred to by a general name of heterojunction field-effect transistor (HFET).

2.1 Development of HEMTs

HEMT structure include GaAs-based HEMTs (such as AlGaAs/GaAs, AlGaAs/InGaAs), InP-based HEMTs (InAlAs/InGaAs), and metamorphic HEMTs etc.

(a) GaAs-based HEMT and PHEMT

Due to easy epitaxy of materials and availability of high quality GaAs semi-insulating substrates, AlGaAs/GaAs HEMT is extensively studied in early stage. Unfortunately, the low conduction band discontinuity of AlGaAs/GaAs translates into poor carrier confinement and moderate velocity, which limits the maximum value of cutoff frequency. It was soon recognized that an energy barrier between channel and substrate would significantly improve the HEMT concept. Such a barrier can be achieved by the introduction of pseudomorphic InGaAs channel between the GaAs buffer and the

barrier, transforming the HEMT into a PHEMT. There are a number of reasons why the PHEMT offers performance advantage for high frequency applications over the conventional AlGaAs/GaAs HEMT. Firstly, the larger bandgap discontinuity between AlGaAs and InGaAs compared to that between AlGaAs and GaAs produces higher sheet carrier density (more charge transfer) and thus higher device current in the PHEMT compared to GaAs HEMTs. Secondly, the higher saturated electron velocity of InGaAs compared to GaAs results in higher gain and better frequency performance [15]. Thirdly, the improved carrier confinement in the InGaAs channel resulting from the larger bandgap discontinuity produces lower output conductance in the PHEMT. Finally, because the PHEMT can carry higher charge density in the channel than the conventional HEMT, the AlGaAs layer above the channel can be doped to a higher level without introducing excessive parasitic current. AlGaAs/InGaAs PHEMTs were used in both low noise and high power applications.

(b) InP-based InAlAs/InGaAs HEMTs

The development of HEMT grown on InP began about 1982. In these transistors, InAlAs barrier layer lattice-matched to the substrate are grown below and above the InGaAs channel. Their advantages over GaAs-based devices are (i) higher conduction band discontinuity: the conduction band discontinuity of lattice-matched InAlAs/InGaAs is about 0.5eV, while for AlGaAs/GaAs ($x_{Al}=0.3$), the conduction band discontinuity is only about 0.37eV. (ii) Higher indium content in the InGaAs channel. This means higher electron concentration in the channel, together with improved carrier transport properties. An InGaAs channel lattice matched to InP contains 53% indium. For pseudomorphic InP based HEMT, even higher In mole fractions are possible.

(c) Composite channel HEMT

Although the excellent performances of InP-based HEMTs at microwave and millimeter-wave frequencies have been achieved, the microwave performance of InP-based HEMTs is limited by relatively low breakdown and high output conductance. This results primarily from the high impact ionization coefficient of the InGaAs channel and low Schottky barrier height of InP-based HEMTs. The off-state and on-state breakdown voltage in InP-based HEMTs have been shown to be dominated by impact ionization in the channel layer, and are typically low due to the low breakdown field of narrow bandgap $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel.

A composite channel consisting of an InGaAs channel and an InP subchannel was proposed and demonstrated by Enoki *et al.* from NTT LSI Laboratories in early 1990s [16,17]. The composite channel structures take advantages of both the high drift velocity and low impact ionization of InP at high electric fields as well as the high electron mobility of InGaAs at low electric fields. At low electric field, the electron current transport is at InGaAs channel. At high electric field, more electrons accumulate in InP layer, and current path can switch from InGaAs channel to InP subchannel.

Such features are based on the changing electron distributions from low field end to high field end of gate, which corresponds to changing gate voltage relative to the changing channel potential. To obtain a quantitative depth profile of energy band and electron distribution for a composite channel, self-consistently solving the Poisson and Schrödinger equations in one dimension is needed, as had been studied in previous works by Enoki. The shift of charge centroid could be qualitatively well expected as a result of electron redistribution. At first, total 2DEG concentration changes when the gate bias changes with changing Fermi level, then for each layer, their respective electron density will also change following their relative energy changes to Fermi level. In Enoki's work,

the electron distribution at drain end and at source end of the gate was calculated and compared. Different electron distribution $n_s(x)$ was showed at the source end and at the drain end of the gate, due to channel potentials' difference. At the drain end, the n_s is much lower than that at the source end, and the charge centroid shifts to the layer sub-channel InP. Because the channel potential monotonically increases along the direction from source to drain, it is clear that abovementioned variation in $n_s(x)$ is a continuous trend. A schematic energy band diagram for a typical InP-based composite channel HEMT is shown in Fig. 2.1.

Fig. 2.1 Schematic energy band diagram for InP-based composite channel HEMT (a) at low electric field (b) at high electric field. [16]

It has been demonstrated that, by using the InGaAs/InP composite channel structure, the device breakdown voltage, frequency performance and output power could be remarkably improved due to the suppression of electron impact ionization and better electron transport properties at high electric field in the InP subchannel.

(d) Metamorphic HEMT grown on GaAs substrate

In 1990, K. Maezawa and T. Mizutani [18] from NTT LSI Laboratories demonstrated that it is possible to grow a 10nm $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ channel on substrate by growing a thick $\text{In}_{x/2}\text{Ga}_{1-x/2}\text{As}$ buffer on the GaAs substrate for $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel. This buffer layer is sufficiently thick so that the strain in the buffer is relaxed. The common $\text{InAlAs}/\text{InGaAs}/\text{InP}$ PHEMTs layer structures were grown on InP substrates. The InP substrates are used which provide lattice-matched conditions for the growth of high indium mole fraction epitaxial layer (~50%). However, GaAs substrate is preferred for production of high performance MMIC because they are inexpensive, mechanically strong and available in sizes exceeding 4 inches. In 1998, M. Zaknune *et al.* [19] reported an important progress on metamorphic HEMT. A f_T of 125GHz at $V_{ds}=1.5\text{V}$, an extrinsic transconductance of 650mS/mm and a current density of 750mA/mm associated to a high breakdown voltage of -13V have been measured on a 0.15 μm metamorphic $\text{In}_{0.3}\text{Al}_{0.7}\text{As}/\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$ SH-HEMT.

2.2 Basic principle of HEMT structure**2.2.1. Two-dimensional electron gas (2DEG)**

When the two semiconductors with different bandgaps and electron affinities are brought in contact (grown on each other), a heterojunction is formed. In thermal equilibrium, the Fermi level on either side of the interface must line up. The heterojunction exhibits discontinuities in the conduction band (ΔE_c) and valence band (ΔE_v). A critical parameter here is the discontinuity between the conduction bands of the two materials, ΔE_c . Ideally, the larger ΔE_c is, the greater the carrier density will be in the

well and the less likely that carriers will have enough energy to leave the well and conduct in the larger bandgap layer.

As shown in Fig. 2.2, in the heterojunction interface, electrons transfer leads to a dipole layer formed by the positively charged depletion layer in the barrier and the electron accumulation in the channel layer. Thus the conduction band of the channel layer very close to the heterojunction forms a quasi-triangular quantum well with quantized density of states perpendicular to the heterojunction. The transferred electrons have two degrees of freedom for motion parallel to the heterojunction. Thus, they are considered a quasi-two-dimensional electron gas. The 2DEG is contained within the potential-well and the electron energy bands are quantized.

Fig. 2.2 Energy-band diagram of 2DEG in a HEMT

The carriers in 2DEG in the heterostructure system lie within the undoped channel triangular quantum well away from the ionized impurity atoms in the depleted barrier layer above. These electrons in high concentration, when transported in the direction parallel to the heterointerface, suffer negligibly from the effect of Coulomb scattering, thus attaining a high value of carrier mobility (μ) approaching the maximum possible

value in the undoped channel material. The high sheet carrier concentration is also responsible for a high degree of screening effect that virtually eliminates the Coulomb scattering. The high mobility in 2DEG provides the basis for development of various HEMTs structures.

2.2.2. High-Field Effect

A. Velocity Saturation

At low electric-fields, the drift velocity (v) of carriers in a semiconductor is linearly proportional to the applied field (E). The mobility is independent of the electric field, since the time interval between collisions is independent of the applied field. This is a reasonable assumption when the drift velocity is small compared with the thermal velocity of carriers. At high electric-field, the carrier drift velocity increases sub-linearly with the applied field and approaches a saturation velocity of about 10^7 cm/s at sufficiently large fields, as the case for Si shown in Fig. 2.3. This can be understood because there is an energy loss mechanism that becomes dominant at high electric field. Carriers can acquire so much energy from high electric field that their average kinetic energy becomes higher than that of the lattice. Electrons with kinetic energies substantially above kT are known as hot electrons, where k is the Boltzmann's constant and T is the lattice temperature. With increasing electric field, the hot electrons will undergo more inelastic scattering with optical phonons and loss more energy, until the carrier velocity (and also energy) becomes saturation and independent of electric field.

For III-V semiconductors GaAs, InGaAs and InP etc., the behavior is a little bit more complicated. When the field increases to a high level, the drift velocity reaches a maximum above the saturation velocity, and then decreases as the field further increases,

as shown in Fig. 2.3. This phenomenon is due to the energy band structure of GaAs, InGaAs and InP, which allows the transfer of conduction electrons from a high-mobility Γ valley to higher-energy but low-mobility L valleys. At low electric field, all electrons remain in the lower-energy Γ valley. When the electric field is higher, some electrons will attain a high velocity, and hence a high kinetic energy. If this energy is sufficiently high the carriers can be expected to undergo a momentum relaxation process and move to the higher L valley. As a result, the average mobility of total electrons will decrease and hence the average electron drift velocity will decrease also.

Fig. 2.3 Electron velocity for InGaAs and InP at different electric fields

B. Velocity Overshoot

The data shown in Fig. 2.3 represent steady-state properties of the semiconductors. However, on short time scales, electron drift velocity could differ significantly from the long-time steady-state velocity. Transient velocity phenomena can result in carrier velocities several times greater than those expected from steady-state considerations. This phenomenon is known as velocity overshoot.

For GaAs and InP materials, the existence of low-mobility satellite conduction valleys (L valleys) is the key mechanism for achieving velocity overshoot. At a high electric field, the electrons can be accelerated to a transient high velocity during short time. However, when the electric field exceeding a certain threshold value so that electrons can achieve enough high energy, electron transfer from Γ valley to L valleys will take place accompanied by a loss in velocity. The transfer of electrons to the L valleys requires a momentum relax time, therefore, before the relaxation, the electrons can remain transient high velocity for a finite short time. Fig. 2.4 shows a Monte Carlo simulation for the average electron velocity in GaAs as a function of time.

Fig. 2.4 Monte Carlo simulation for the average electron velocity in GaAs as a function of time [20].

In a HEMT structure, the transport of 2DEG is greatly influenced by the electrical field in the direction parallel to the heterostructure interface. When the effective gate length in a HEMT structure becomes sufficiently small, the electrons, when subjected to a high field, could travel well above the bulk carrier saturation velocity. The enhanced

overshoot carrier velocity can be expected to provide an enhanced carrier average velocity for the transport of electrons from the gate source edge to the drain terminal, i.e., reduce the carrier transit time, and thus significantly enhance the high-speed performance of the device. For example, assuming the effective velocity is 1.5×10^7 cm/s, a HEMT with $0.15\mu\text{m}$ effective gate length potentially can have f_T as high as 1000 GHz. Of course, the real device performance is limited at much lower value due the parasitic elements.

C. Impact Ionization and Break-down

When the electric field in a semiconductor is increased above a certain value, the electron can gain kinetic energy before it collides with the lattice. On impact with the lattice, the electron imparts most of its kinetic energy to break a bond, that is, to ionize a valence electron from the valence band to the conduction band and there generate an electron-hole pair. Similarly, the generated electron-hole pair now begins to accelerate in the field and collides with the lattice again. In turn, they will generate other electron-hole pairs, and so on. This process is called the avalanche process or impact ionization process, resulting in breakdown of device involved.

The ionization energy required depends on the band structure, generally, larger-bandgap material need more energy to generate an electron-hole pair for the ionization process. The number of electron-hole pairs generated by an electron per unit distance traveled is called the impact ionization coefficient for the electron. As an example, Fig. 2.5 shows a comparison between the coefficients of InGaAs and InP materials. InP shows a lower impact ionization coefficient in comparison to InGaAs.

Fig. 2.5 Comparison of electron impact ionization coefficients between InGaAs and InP

2.2.3 Charge-control in a HEMT

In brief, in the HEMT structure, the 2DEG channel sheet charge is controlled by the Schottky barrier gate potential and the channel current flows in response to the increasing drain voltage until the current saturates due to the carrier saturation velocity. Fig. 2.6 shows the cross-sectional diagram of a typical HEMT. The HEMT consists of two Ohmic contacts, called the source and the drain, that allow current to flow into or out of the cap layer. A metal strip called the Schottky gate is in between these two contacts. The doping in barrier layer above the channel layer supplies electrons to the channel. Once a gate is present, the barrier layer is partially depleted of carriers due to the action of the gate metal Schottky potential, and the 2DEG sheet carrier concentration can be effectively controlled by applying an appropriate bias voltage. The gate electrode and the 2DEG form a parallel plate capacitor whose capacitance is given by Ref. [21]:

$$C_g = \frac{\varepsilon}{d_d + d_i + \Delta d} \quad (2.1)$$

Where, C_g is capacitance per unit area, ε is dielectric constant, d_d , d_i , and Δd are the thickness of the doped barrier layer, spacer thickness and the mean distance of the 2DEG from the barrier/channel interface, respectively.

Fig. 2.6 The device structure of a typical HEMT

The gate voltage at which the 2DEG is completely depleted of the carriers is defined as threshold voltage V_{th} , which is dependent on the barrier layer thickness $t_b = d_d + d_i$, and the doping level of the barrier layer. The V_{th} is given as [21]:

$$V_{th} = \phi_b - \Delta E_c + \Delta E_F - V_{dep} \quad (2.2)$$

and

$$V_{dep} = \frac{qN_d}{2\varepsilon} d^2 \quad (2.3)$$

where ϕ_b is the metal-to-barrier Schottky barrier potential, ΔE_c is the conduction band discontinuity, ΔE_F is the position of the Fermi level with respect to the bottom of the conduction band of channel material, V_{dep} is the total depletion voltage and N_d is the doping density in the barrier. The depth of the depletion region of barrier layer and 2DEG is dependent on the gate voltage. At a particular voltage, $V_{g,max}$, the barrier layer goes from complete depletion to free carrier conduction. When the gate voltage exceeds $V_{g,max}$, parallel conduction begins to occur in the barrier layer which contributes to the device current. Thus the useful gate swing (ΔV_g) that can be obtained without pushing the AlGaAs layer into conduction is given by:

$$\Delta V_g = (V_{g,max} - V_{th}) = \frac{qn_{s0}}{\epsilon} (d_d + d_i + \Delta d) \quad (2.4)$$

where n_{s0} is the maximum 2DEG sheet carrier concentration.

Based on the charge-control model first developed by Delagebeaudeuf *et al.* [22], the sheet carrier concentration (n_s) of the 2DEG in the channel is related to the applied gate voltage (V_{gs}) as:

$$qn_s = C_{gs} (V_{gs} - V_{th}) \quad (2.5)$$

where C_{gs} is the gate capacitance.

2.3 Basic device operation

2.3.1 DC characteristics

The above charge control analysis is based on a two-terminal device formed with a gate and substrate. The device is symmetrical about a midplane through the center of the

gate, and the channel charge density is constant in the entire channel. In a practical HEMT, there is a potential drop in the direction parallel to the channel, causing the channel charge density to be a function of position x . Therefore, denoting the channel potential resulting from the applied V_{ds} as $V_{cs}(x)$. Further the gate voltage is now made with respect to the source terminal, so the channel charge sheet density may be expressed as the following:

$$qn_s(x) = C_{gs} \cdot [V_{gs} - V_{th} - V_{cs}(x)] \quad (2.6)$$

Then, at DC condition, the continuity equation and the drift equation can be expressed as follow:

$$\frac{dI_{CH}(x)}{dx} = 0 \quad (2.7a)$$

$$I_{CH}(x) = -WC_{gs}\mu_n[V_{GS} - V_T - V_{CS}(x)]\frac{dV_{CS}(x)}{dx} \quad (2.7b)$$

where, W is the gate width.

At a fixed gate voltage, when the source-drain voltage increases, the source-drain current increase linearly (i.e. linear region) and then become saturation at a certain level (i.e. saturation region). In the linear region, the source drain current can be got by integration of Eq.2.7. Then when V_{DS} reaches $V_{DS,sat} = V_{GS} - V_T$, the current reach a highest value denoted by $I_{ds,sat}$, which could be understood from the channel pinch off at the drain end. Physically, the channel at the drain does not pinch off completely, there is a finite thickness of accumulations of charges and the qn_s at $x = L$ is nonzero. The drift velocity is high, but nonetheless finite, so a constant current is maintained through the channel. When $V_{DS} > V_{DS,sat}$ a narrow region is taken to exist between the tip of the pinchoff region and the drain contact. In this narrow region, qn_s is small, with carriers

traveling at high speed. Because the amount of accumulation thickness is small, this region can be viewed as a depletion region. The accumulation layer between the source and tip of the pinchoff supports only a voltage amount of $V_{DS,sat}$. Any excess voltage, $V_{DS} - V_{DS,sat}$, is dropped across this depletion region. As V_{DS} increases, the length of this narrow depletion region increase somewhat, but is taken to be still fairly small in comparison to the channel length. Therefore, the distance between the source and the pinchoff point remains close to L . Therefore, the drain current at saturation region and linear region can be expressed as follow:

$$I_{ds} = \frac{WC_{gs}\mu_n}{L} [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \quad \text{for } V_{DS} < V_{DS,sat} \quad (2.8a)$$

$$I_{ds} = \frac{WC_{gs}\mu_n}{L} \frac{(V_{GS} - V_T)^2}{2} = I_{D,sat} \quad \text{for } V_{DS} \geq V_{DS,sat} \quad (2.8b)$$

An implicit assumption of the above discussion is that the electron velocity is equal to the product of the mobility and the longitudinal electric field. In reality, the electron velocity cannot increase indefinitely as the electric field increase, as discussed in Section 2.2.2. The electron velocity increases linearly with $\mathcal{E}$ only when the field is smaller than the critical electric field ($\mathcal{E}_{crit}$) of about 10^3 V/cm. when the electric field becomes high, the velocity either increase towards the saturation velocity (v_{sat}), or increases toward a peak velocity (v_{peak}) at first before dwindling back to v_{sat} . For short channel HEMT, the field in the channel easily surpasses $\mathcal{E}_{crit}$ during device operation. Therefore, the analysis for short channel device must consider the velocity saturation. As shown in Fig. 2.7, the channel can be divided into two sub-regions when the electric field at drain exceeds $\mathcal{E}_{crit}$, the low-field region adjacent to the source, where $v_{drift}(x) < v_{sat}$, and the velocity-saturation region

adjacent to the drain, where $v_{drift}(x) = v_{sat}$. In the low-field region, $v_{drift}(x)$ is still given by $\mu_n \cdot \mathcal{E}$, increasing monotonically with x because $\mathcal{E}$ increases with x . Upon reaching the boundary of the saturation region, $v_{drift}(x) = v_{sat}$ for the remainder of the channel length. For the whole channel, a constant drain current is maintained. With adopting a drift velocity model given by:

$$v_{drift} = \mu_{n,0} |\mathcal{E}| / (1 + \frac{|\mathcal{E}|}{\mathcal{E}_{sat}}) \quad \text{if } \mathcal{E} < \mathcal{E}_{sat} \quad (2.9a)$$

$$v_{drift} = v_{sat} \quad \text{if } \mathcal{E} \geq \mathcal{E}_{sat} \quad (2.9b)$$

The drain current I_{ds} for a short channel HEMT, operating in saturation, can be expressed as:

$$I_{ds} = WC_{gs} [V_{GS} - V_T - V_{CS}(L)] \times v_{sat} \quad (2.10)$$

If a short channel HEMT operates at a condition the electrons may drift at peak velocity or at overshoot velocity, we may use effective average velocity v_{eff} in place of v_{sat} to be more generalized.

Fig 2.7 Schematic of electric fields in two sub-regions of a HEMT with velocity saturation occurs in channel.

At a fixed V_{ds} , source-drain current changes with the gate voltage. The transconductance g_m is defined as the slope of the $I_{ds} \sim V_g$ characteristics with the drain-source voltage held constant, i.e., $g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds} = \text{constant}}$. From Eq.2.10, the transconductance can be written as:

$$g_m = \frac{\partial I_{ds}}{\partial V_g} = WC_{gs} v_{eff} \quad (2.11)$$

The transconductance of the device is one of the most important indicators of device quality for microwave and millimeter wave application. When all other characteristics are equal, a device with high transconductance will provide greater gains and superior high-frequency performance. Another important characteristic is the drain output conductance g_o , which is defined as the derivative of the drain-source current with respect to drain-source voltage while gate-source voltage is held constant.

$$g_o = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{gs} = \text{constant}} \quad (2.12)$$

Output conductance plays a significant role in determining the maximum voltage gain attainable for the device and is extremely important for determining optimum output matching properties. In general, for a device to have a low value of output conductance is desirable.

2.3.2 RF characteristics

A. Two-port concept of Microwave Transistor

To study the RF and noise characteristics of a microwave transistor, it is necessary to discuss the two-port concept of electronic devices. Any active device such as a

microwave transistor can be treated as a two-port network. As shown in Fig. 2.8, the input of such a two-port network is connected to a signal source (often called the generator) consisting of a voltage source v_G and a source impedance Z_G , and the output is connected to a load with a load impedance Z_L . The input and output currents of the two-port network are i_1 and i_2 , respectively, whereas the input and output voltages are denoted v_1 and v_2 . The voltages and currents are in lower case to indicate that they are ac small-signal quantities.

Fig. 2.8 A microwave transistor (active device) as a two-port network with signal source and load.

In Fig. 2.8, the two-port network containing the microwave transistor is a black box and does not give any information on transistor performance. This information can be represented by a number of small-signal parameter sets such as Y , H , or Z parameters. Take Y parameters as an example, the relationship between Y parameters and the currents and voltages of the circuit in Fig. 2.8 is given by

$$Y \text{ parameters} \quad \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad \begin{aligned} i_1 &= y_{11}v_1 + y_{12}v_2 \\ i_2 &= y_{21}v_1 + y_{22}v_2 \end{aligned} \quad (2.13)$$

The four Y parameters are defined under ac short circuit condition by

$$\begin{aligned}
 y_{11} &= \left. \frac{i_1}{v_1} \right|_{v_2=0} && \text{input admittance} \\
 y_{12} &= \left. \frac{i_1}{v_2} \right|_{v_1=0} && \text{reverse transfer admittance} \\
 y_{21} &= \left. \frac{i_2}{v_1} \right|_{v_2=0} && \text{forward transfer admittance} \\
 y_{22} &= \left. \frac{i_2}{v_2} \right|_{v_1=0} && \text{output admittance}
 \end{aligned} \tag{2.14}$$

Fig. 2.9 shows the equivalent circuit of the active device using parameters. At frequencies up to about 100MHz, the external voltages and currents of the two-port network can be easily measured, and the Y parameters are determined based on Eq. (2.14).

Fig. 2.9 Equivalent circuit of an active device based on Y parameters

For operating frequencies in the microwave range, however, the measurement of the external voltages and currents and the realization of the required short-circuit conditions become more complicated. Therefore, another set of parameters, the S

parameters (Scattering parameters), is commonly used. S parameters are not defined as quotients of currents and voltages but as ratios of powers of traveling waves.

$$S \text{ parameters} \quad \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad \begin{aligned} b_1 &= s_{11}a_1 + s_{12}a_2 \\ b_2 &= s_{21}a_1 + s_{22}a_2 \end{aligned} \quad (2.15)$$

As in the case of Y parameters, the subscripts 1 and 2 designate the input and the output of the two-port network, respectively, whereas a and b are the powers of incoming (or incident) and outgoing (or reflected) waves. Figure 2.10 shows the two-port network with the incident (a_1, a_2) and reflected (b_1, b_2) waves.

Fig. 2.10 Two-port network characterized by S parameters

Y parameters can be converted into S parameters and vice versa, using simple conversion rules. All parameters introduced above depend on the specific bias conditions and on the operating frequency of the two-port network. In general, large values for the 21-parameters (parameters with subscript 21, e.g., y_{21} and s_{21}) are desirable. The 21-parameters describe the transistor's ability to control and amplify input signals.

B. Equivalent Network Model and Parameters Extraction

In a typical application of semiconductor devices, models are important for device design and performance prediction, especially the information that is not available or easily obtainable by direct measurement. The small-signal HEMT model is extremely important for active microwave circuit work. The models provide a vital link between measured s-parameters and the electrical processes occurring within the device. Each of the elements in the equivalent provides a lumped element approximation to some aspect of the device physics. A properly chosen topology in addition to being physically meaningful provides an excellent match to measured s-parameters over a very wide frequency range. When element values are properly extracted, the model is valid above the frequency range of the measurements, providing the possibility of extrapolating device performance to frequencies beyond some equipment's measurement capabilities.

When considering a real device, both the intrinsic and extrinsic (parasitic) effects must be represented by appropriate network elements before a comprehensive understanding of its potential can be achieved. Fig. 2.11 shows the cross-sectional layout of a HEMT structure and identifies the regions where the various elements of the parasitic resistance and capacitance are located. With these identified parasitic elements, an overall equivalent network model for the HEMT can be constructed as Fig 2.12. In Figs. 2.11 and 2.12, g_m is transconductance, g_o is the drain output conductance, and C_{gs} is the gate input capacitance. r_i is a series resistance linked to the intrinsic gate charging capacitance C_{gs} . (g_{gs} and g_{gd}) represent the gate-to-source and the gate-to-drain leakage conductance. r_{ss} , r_{dd} and r_{gg} represent the parasitic source, drain, and gate series resistance. C_{dg} represents the parasitic feedback capacitance between the gate and the drain. The gate-to-source parasitic capacitance includes two parts (C_{gs1} and C_{gs2}). The

inner component C_{gs1} depends on the details of the depletion between the lower corner of the gate metallization and the Ohmic contact metallization, and the n+ cap layer. The

Fig. 2.11 Schematic cross section of various elements of the parasitic resistance and capacitance in HEMT structure

Fig. 2.12 An overall equivalent network model for the HEMT structure including intrinsic and extrinsic parameters

outer component C_{gs2} comprises the interelectrode and fringing capacitances between the gate and the source metallization effectively extended by the n+ cap layer. C_{gp} represents the small parasitic capacitance from the gate pad to ground. C_{ds} represents the drain-to-source capacitance, which arises due to the fringing electric field between the two coplanar conducting regions of the 2DEG. C_{dp} represents a small drain pad capacitance that exists between the drain metallization pad and the ground plane via the substrate.

Before any device model can be used, values for the parameters required of the model must be determined. The process of determining these parameters is called “parameter extraction”. In brief, by DC measurement, the DC data may be used to extract the DC output conductance, DC transconductance, and the parasitic resistances. In addition, the forward-bias characteristics and DC breakdown properties of the gate-source and gate-drain diodes may be evaluated. S-parameters at multiple biases may be used to extract the equivalent circuit element values in model. From measured device S-parameters, RF element values of output conductance, transconductance, gate-source capacitance, and gate-drain capacitance in a small-signal equivalent circuit model can be obtained. The other intrinsic element values, C_{ds} , R_i , τ , parasitic resistances may also be extracted.

C. Cutoff-frequency and the maximum frequency of oscillation

The cutoff-frequency f_T and the maximum frequency of oscillation are the most important figures of merit for the frequency characteristics of microwave transistors. The current gain cut-off frequency (f_T) is related to the short-circuit current gain (h_{21}). This current gain is defined as the ratio of the small-signal output current to input current of the transistor with the output short-circuited. Such a current gain is frequency dependent,

and its magnitude rolls off at higher frequencies at a slope of -20dB/decade for any transistor.

The cut-off frequency is the frequency at which the current gain goes to unity (or 0dB). The current gain cutoff frequency f_T can be defined as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (2.16)$$

Hence to increase f_T , it is essential to increase the g_m and reduce C_{gs} and C_{gd} , which can be achieved by increasing electron velocity in the channel and reducing gate length. However, when the gate length become very short, it is necessary to reduce the other parasitic delays in the device and take into account short channel effects. A more rigorous expression for f_T , which includes the effects of parasitics on f_T was derived by Tasker and Hughes [23] is given as follow,

$$f_T = \frac{g_m / 2\pi}{[C_{gs} + C_{gd}][1 + (R_s + R_d)/R_{ds}] + C_{gd}g_m(R_s + R_d)} \quad (2.17)$$

It is clear from the equation that it is necessary to reduce source resistance R_s and drain resistance R_d to increase f_T .

Beside the current gain cutoff frequency, a more practical measure of HEMT is the maximum oscillation frequency f_{max} , which is the maximum frequency at which the transistor still provides a power gain. f_{max} is originally defined as the frequency at which the unilateral power gain U rolls off to unity. Sometimes in the literature, however, the frequency at which the maximum available gain MAG becomes unity is also designated as defined as f_{max} . For the HEMT, the expressions for these two different definitions used for f_{max} are given by [24],

$$f_{\max, MAG} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \frac{1}{[4g_{ds}(R_i + R_s + R_G) + \frac{2g_m C_{gd}}{C_{gs} + C_{gd}}(R_i + R_s + 2R_G)]^{1/2}} \quad (2.18a)$$

$$f_{\max, U} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \frac{1}{[4g_{ds}(R_i + R_s + R_G) + 4g_m R_G \frac{C_{gd}}{C_{gs} + C_{gd}}]^{1/2}} \quad (2.18b)$$

2.3.3 Noise Characteristics

One of the attractive features of the HEMT as an amplifying device is its very low noise figure at high frequency with a high associated power gain. Noise in electrical system is the internal generation of signals that cause degradation from the desired or theoretical response. The physical properties of materials result in various types of noise. Thermal noise originates because heat in the electrical device provides energy to the carriers causing random fluctuations in their movement. The lower the temperature the lower is this thermal noise. This noise is generated only in systems or circuit elements that dissipate power (resistive); purely reactive elements (ideal capacitors and transmission lines) do not generate noise. Semiconductor devices can also contribute flicker noise ($1/f$ noise) and generation-recombination noise.

Basically, the physical origin of high-frequency noise in HEMTs is fluctuations in the carrier density and/or the carrier drift velocity in the channel and in the parasitic resistances. These fluctuations cause random variations of the current passing through the transistor. The random current fluctuations in a particular channel segment represent the noise current generated (i). Because of the amplification effect inherent to the HEMT, the noise current i generated in the channel segment entails an amplified noise current i_d at the drain. The current fluctuations in all segments of the channel add up to be the total drain

current fluctuations called the drain noise current i_D . In addition, the current fluctuations in channel will also cause fluctuations of the gate current i_g corresponding to different segments of the channel. Adding up the i_g in all channel segments will then make a gate noise current i_G . Because the random nature of noise, it is impossible to accurately predict the noise current at a certain time. The mean value of a noise current with time is zero. Therefore, noise currents are described by the mean square values $\overline{i^2}$. The same holds for noise voltages (v_G and v_D).

A noise equivalent circuit could be given by adding the noise elements to the equivalent circuit network as shown in Fig. 2.12. As shown in Fig. 2.13, to be simple, the noise-free intrinsic transistor part is described only by the gate-source capacitance C_{gs} , the charging resistance R_i , and the transconductance g_m . For the extrinsic elements, only the parasitic gate and source resistances R_G and R_S are included in the noise consideration. The thermal noise generated R_G and R_S is taken into account by the noise voltage sources e_G and e_S , respectively. The signal source described by the source impedance Z_{source} and its noise voltage source e_{source} is connected to the transistor input.

Fig. 2.13 Simplified noise equivalent circuit of HEMTs [24].

The noise characteristics of two-port networks can be derived by considering the network of Fig. 2.14. A signal S_i with some noise N_i is present at the input of the device. Both the signal and noise will be affected by the system such that at the output a signal S_o with noise N_o is present. Because the transistor can not distinguish between the signal and

Fig. 2.14 A two-port network with both signal and noise present at input and output.

noise, both will be amplified. Besides the amplified signals and amplified external noises, an additional component appears at the output of the transistor: the intrinsic noise generated in the transistor. A figure of merit describing the amount of intrinsic noise produced in microwave transistors is the *noise figure* NF . The noise figure (commonly given in decibels) is defined by

$$NF_{dB} = 10 \log\left(\frac{S_i / N_i}{S_o / N_o}\right) \quad (2.19)$$

where,

$S_{i,o}$ = signal power at the input and output ports,

$N_{i,o}$ = noise power at the input and output ports, and

Note that under ideal conditions the two-port device will add no noise of its own to the signal. Rather, it simply amplifies or attenuates the signal and the input noise. Under these conditions, the noise factor $NF_{dB}=0\text{dB}$. When a two-port component contains active devices such as a HEMT, noise is generated by these devices and is added to the output of the two-port device. The generation of this noise is typically modeled using an equivalent circuit for the device that contains current or voltage noise sources to model the noise effects. These internal noise sources contribute only to the overall noise of the two ports and not to the gain. However, because these sources are internal to the device, the overall noise is affected by the matching circuitry connected to the HEMT.

One of the key factors influencing the noise figure of an amplifier circuit or active device is the generator admittance, $Y_g = G_g + jB_g$, connected at the input port of the device under test (DUT). This admittance is illustrated in Fig. 2.15. The effect on noise figure is given by [25]:

$$NF(Y_g) = NF_{\min} + \frac{R_n}{G_g} [(G_g - G_{opt})^2 + (B_g - B_{opt})^2] \quad (2.20)$$

where,

$NF_{\min}$ = minimum value of F with respect to Y_g ,

$Y_{opt} = G_{opt} + jB_{opt}$ is the admittance value at which $NF = NF_{\min}$, G_{opt} is the optimal input circuit conductance. B_{opt} is the optimal input susceptance, and

R_n = equivalent noise resistance of the DUT

Fig. 2.15 The circuitry connected at the input of a device significantly influences the device noise.

Equation (2.20) can also be expressed in terms of the generator or source reflection coefficient. The reflection coefficient is related to the admittance by:

$$\Gamma_g = \frac{Y_R - Y_g}{Y_R + Y_g} \quad (2.21)$$

where Y_R is the reference admittance for Γ . A similar expression can be written for the optimal source reflection coefficient, Γ_{opt} , which results in a minimum noise figure. Hence, Equation (2.20) can be written as

$$NF = NF_{min} + \frac{4R_n |\Gamma_g - \Gamma_{opt}|^2}{R_R (1 - |\Gamma_g|^2) |1 + \Gamma_{opt}|^2} \quad (2.22)$$

Equations (2.20)-(2.22) provide the basis for evaluating the noise figure when external circuitry is connected to the input of a device.

The meanings of the parameters Γ_{opt} and NF_{min} are obvious from their stated definitions. The parameter R_n is useful as an indication of the dependence of NF_{min} on the source admittance Y_g . A low value of R_n is desirable for most circuit applications because this allows a source admittance considerably different from Y_g to be used without seriously degrading the noise figure.

The noise parameters NF_{min} , R_n , and Γ_{opt} are properties only of the active device and are independent of any external circuitry connected to the device. However, these parameters depend on temperature, frequency, drain-source current etc. Using suitable equivalent circuit model, the noise parameters could be linked to related circuit elements, which allows description of HEMT noise behavior, predictions of noise figure. By S-parameters measurement and noise figure measurement, model parameters can be obtained from measured noise data.

Direct minimum noise figure measurement characterized the noise properties of a HEMT by applying a known admittance at the input of the device. The noise figure is monitored while adjusting the input impedance to achieve minimum noise figure. At this condition, the device exhibits minimum noise figure NF_{min} , and the optimal source

admittance is that which is applied at the device input (i.e., $Y_{opt} = Y_g$, and $NF_{min} = NF(Y_{opt})$). The equivalent noise resistance R_n is determined from considering equation (2.20).

A second and more accurate method measures the device noise figure at multiple source admittances, allowing an indirect characterization of the device noise parameters. This requires measurement of noise at a minimum of four unique source impedances. Extraction of device noise parameters is accomplished by considering equation (2.20), which relates device noise to the applied source admittance. Thus, given four known source admittances (Y_1, Y_2, Y_3 , and Y_4) and the measured noise figure at each source impedance (NF_1, NF_2, NF_3 , and NF_4), then the equation allows an algebraic solution for device noise parameters NF_{min} , X_{opt} , R_{opt} and R_n .

Chapter 3 Submicron HEMT Experimental Technology

3.1 Device structure

The InP-based HEMT used in this work is schematically shown in Fig. 3.1, the basic structure comprises of a semi-insulating InP structure followed by an InAlAs buffer layer, an InGaAs channel layer, an InAlAs spacer layer, an InAlAs donor layer, an InAlAs Schottky barrier layer, and an InGaAs cap layer. The conductive path in the InGaAs channel layer is generated by the transfer of free electrons out of the doped InAlAs layer into the InGaAs channel, where they form a 2DEG localized within an approximately 15nm-thick layer at the heterointerface of the InAlAs/InGaAs layer. Here the conduction band forms a quasi-triangular potential well by the electric field that result from the parent donors in the InAlAs and mobile electrons in the InGaAs channel.

Fig. 3.1 Schematic structure of an InP-based HEMT

Ideally, this very thin conductive layer in the quantum well is the only path under the gate electrode where mobile carriers flow. The InAlAs layers are entirely depleted of mobile carriers so that the gate modulates only the 2DEG. In following, the role of each layer is introduced briefly.

(a) Cap layer

The cap layer is usually made of heavily doped ($3 \times 10^{18} \sim 1 \times 10^{19} \text{ cm}^{-3}$) low bandgap materials such as InGaAs. The purpose is to enhance the ohmic contact quality and to provide a low access resistance region to the active channel. Moreover, the cap layer prevents oxidation of aluminum containing layers such as InAlAs.

(b) Schottky barrier layer

The purpose of this layer is to minimize problems caused when the gate is placed directly on a highly doped donor layer. This will lead to higher gate leakage and low gate to drain breakdown voltage. To overcome this, a large bandgap undoped layer is incorporated right above the donor layer. In our InGaAs channel HEMT, a large bandgap ($E_g = 1.46 \text{ eV}$) $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ is used.

(c) Donor layer

The donor layer consists of a material of higher bandgap than the channel. It is doped with N-typed impurities, typically silicon to provide electron to the channel of HEMT. P-type doping is also employed for digital device applications. Traditional way of HEMT doping is uniform bulk-like doping profile where the entire donor is doped at a fixed value. Highly doped layers enhance the leakage of the gate sitting on them and result in decrease of the breakdown voltage. An alternative way of doping is with delta-doping profile, which is also referred to as pulse, atomic layer or spike doping. This layer is only a few monolayers thick and heavily doped ($5 \times 10^{12} \text{ cm}^{-2}$ to $1 \times 10^{19} \text{ cm}^{-3}$). Besides allowing a high n_s value, the problem of gate leakage current is minimized since an undoped wide-bandgap material exists between the gate and the atomic planar doping region. This

approach allows the reduction of the separation of the gate from the channel increasing therefore the modulation efficiency of the 2DEG.

(d) Spacer layer

The purpose of the spacer is to separate the 2DEG carriers from their parent donors and thus reduces the Columbic scattering. A thinner spacer thickness increases the total sheet charge density available in the channel. This results in a reduced source resistance, higher transconductance and higher current density. On the other hand, a thicker spacer provides higher electron mobility due to less Columbic scattering and less charge density in the channel.

(e) Channel layer

A high quality material is essential for the channel in view of optimum carrier transport. It should be free of defects and residual impurities. The thickness of this layer is kept smaller than the critical layer thickness for the corresponding material in order to avoid dislocation formation.

(f) Buffer layer

This layer allows the growth of subsequent layers with high quality characteristics and prevents any impurities from diffusing to the channel because the interface of the substrate is too rough and defects for good epitaxial growth. The use of a buffer with bandgap higher than the channel also provides a high barrier and thus prevents the electrons from being injected into it.

3.2 Device Fabrication

Submicron HEMT fabrication process used in this work primarily involves five masking steps namely, mark formation, mesa isolation, ohmic metallization, pad interconnection, submicron gate formation using direct writing electron beam lithography. A mix and match technique is employed whereby all the steps except mushroom gate formation are fabricated using conventional optical lithography. In order to aid the understanding of the process flow, the cross sectional HEMT schematics are included in Fig. 3.2. In this section, several steps involved in submicron HEMT fabrication are discussed in detail, including the ohmic contact metallization, submicron T-gate formation using electron-beam lithography, selective gate recess process and submicron mushroom gate formation.

3.2.1 Ohmic metallization

The key parameters for high speed and low noise devices are high quality material, short gate-length and low parasitics. One parameter, which strongly affects device performance, is the sources resistance R_s . By reducing R_s the speed of the devices can be improved and the associated noise reduced. The purpose of ohmic contact on a semiconductor is to allow electrical current to flow into or out of the semiconductor. The contact should have a linear I-V characteristic, be stable over time and temperature, and contribute as little (parasitic) resistance as possible.

A multiple-layer metal scheme using Ni/Ge/Au/Ni/Au was chosen for our InP HEMTs. The process is optimized to obtain better surface morphology with minimal contact resistance by adjusting the layer thickness and annealing condition. Good surface

Fig. 3.2 Schematic Submicron HEMT fabrication process flow

morphology with clear and sharp edges of the Ohmic contact patterns, and smaller contact resistance ($<0.1\Omega\cdot\text{mm}$) were achieved.

3.2.2 Submicron T-gate formation using electron-beam lithography

In order to achieve a high operating frequency and high transconductance, a short gate is essential for HEMTs in addition to the high mobility of the two-dimensional electron gas [26]. The reduction in gate length also results in a decrease in the feedback capacitance, input capacitance and shorter transit time. However, because of the increases in parasitic gate resistance at extremely short gate lengths, the noise and associated gain degrade. Therefore, in order to obtain a low gate resistance while still retaining a very short footprint, several technologies such as trilayer resist process [27], multiple electron beam lithography [28], X-ray lithography [29] and deep UV Phase Shifting Mask Lithography [30] have been developed to fabricate a mushroom gate structure to reduce gate resistance. Multiple electron beam lithography technology has the capability to fabricate mushroom gates with wide heads.

Figure 3.3 shows a schematic of the submicron mushroom gate process used in this work. The gate fabrication starts with the spinning of polymethylmethacrylate (PMMA) at 700rpm for 1 minute (about 230nm thick) on HEMT sample and is baked for 1 hour at 160°C to remove the solvent. This layer PMMA will define the actual electrical gate length. Then a layer of MMA-PMMA co-polymer (dissolved in ethyl lactate, 11wt%) is

Fig. 3.3 Submicron gate fabrication process by electron beam lithography direct writing

added on the PMMA after spinning at 4000rpm for 1 minute and baked for another 1 hour at 160°C. This co-polymer layer is used for creating the top part of the gate to reduce the gate resistance. An electron beam lithography system based on a JEOL JSM 6600 Scanning Electron Microscope (SEM) with a RAITH laser interferometer stage and Elphy Plus software is used to fabricate mushroom gate. The system is used to expose the resist. After exposure, the sample is developed using a Methyl isobutyl ketone (MIBK): isopropanol (IPA)=1:3 solution at room temperature for 1 minute. An additional 1minute

of isopropanol (IPA) solution dip is used as developer stopper. The T-gate profile as shown in Fig. 3.3 can be formed.

3.2.3 Selective gate recess process

Selective etching is used in InP-based HEMTs processing to realize gate recess. By means of selective etching, the InGaAs cap layer can be removed fully while the underlying InAlAs Schottky layer can be exposed without obvious thickness reduction. This feature is very helpful to improve the pinch off voltage control and the process yield. In this work, good etch selectivity of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ over InAlAs is realized by using succinic acid: hydrogen peroxide (H_2O_2) solution. The succinic acid solution was prepared by adding 1-L H_2O to 200-g succinic acid powder, and then adding ammonium hydroxide (NH_4OH) until the pH was 5.05. After cooling, gate recess was realized in the etching solution of succinic acid: hydrogen peroxide (H_2O_2) = 6:1. We observed that the I_{DSS} drops sharply in the initial etching stage and saturates at etch time over 50s where the cap layer was just removed, as shown in Fig. 3.4. The good control is necessary to avoid under-recess or over-recess, which usually results in high gate leakage or very low current level, respectively. In actual process, we choose the etching time at about 80 seconds. A lateral extension of the recess around 0.15~0.2 μm could be achieved. The wide recess allows the full lateral extension of the drift region in InP-based HEMT structures [31].

Fig. 3.4 Etching current versus etching time for SA:H₂O₂=6:1 solution

After the chemical recess using a selective etchant, the gate contact was formed by Ti/Au deposition and lift-off process. Shown in Fig. 3.5 is a SEM image of the T-gate with a metal footprint of $\sim 0.25\mu\text{m}$ and about $0.2\mu\text{m}$ metal overhang in either side. A fabricated device with two gate fingers is shown in Fig. 3.6.

Fig. 3.5 SEM microphotograph of $0.25\mu\text{m}$ T-shape gate

Fig. 3.6 SEM microphotograph of the fabricated InP-based composite channel HEMT with two $0.25\ \mu\text{m}$ gates.

3.3 Characterization of Material Properties

A. Photoluminescence

Photoluminescence is the most widely used technique to characterize semiconductor materials. The basic theory of PL is that the luminescence excited by photons (usually a laser). Then, the excess carriers will recombine through various processes depending on material quality and energy band structures. There are various possible radiative recombination processes in a semiconductor are summarized in Fig. 3.7.

- (a) Band-to-band transition (e, h)
- (b) Conduction band-neutral acceptor transition (e, A^0)
- (c) Neutral donor-valence band transition (D^0, h)
- (d) Neutral donor-neutral acceptor transition (e, A^0)
- (e) Conduction band –neutral donor transition (e, D^0)
- (f) Neutral acceptor-valence band transition (A^0, h)

(g) Free exciton transition (X^0 , h)

(h^1) or (h^2) impurity related deep emission.

Fig. 3.7 The schematic diagram of various radiative recombinations in semiconductors

PL is a simple and direct tool to investigate the 2DEG properties and crystalline quality, moreover, it is nondestructive. The PL system used for this work is a SPEX-750M system. The samples could be mounted on the cold finger of a cryogenic closed-cycle helium cryostat, allowing a low temperature measurement up to $\sim 5\text{K}$. An Ar^+ laser ($5145\text{\AA}$) was used as the excitation source with a typical power density of 0.1 W/mm^2 . The luminescence from the specimen was dispersed through a 0.75 m grating spectrometer and detected by a liquid nitrogen cooled germanium detector in conjunction with a conventional lock-in technique.

B. Hall measurement

The Hall effect measurement is a useful tool to determine the carrier concentration and Hall mobility of a semiconductor. Such measurements are extremely useful in the

analysis of the electrical properties of semiconductors. As show in Fig. 3.8, When a magnetic field is applied at right angles to a current flow, an electric field E_H is generated which is mutually perpendicular to the current I and magnetic field B and is directly proportional to the product of the current density and magnetic field. Assuming that the

Fig. 3.8 schematic diagram of Hall effect theory

semiconductor is n-type and combining with the 4-probe technique to determine the material receptivity, the Hall mobility (μ) and the carrier concentration (n) can be related to $\rho = \frac{1}{q\mu_n n}$, where, ρ and q are the resistivity and the magnitude of the electron charge, respectively.

In this work, the carrier concentration and mobility were measured through Van der Pauw method using a Bio-Rad HL5500 system. To reduce parallel current effect in Hall measurements, the cap layer of HEMT samples was removed. All samples are 1cm $\times$ 1cm square shaped. Indium contact dots placed on four corners and the dot size is kept as small as possible (~ 0.5 mm) to reduce relative error. Ohmic contacts were formed by annealing indium on the samples in nitrogen ambient at 400°C for 60 sec, which is an optimum condition to form good contact. The good contact quality is confirmed by checking resistance between different contacts, which are close in value. The measurement

is carried out at room temperature, and the magnetic field applied was 0.32 Tesla. The current used for measurement is determined by system auto-set optimization, for our samples the current typically in the level of mA and the voltage is in level of Volt. Typical symmetry values in experiments fall in the range between 1 and 2, which shows good symmetry in sample preparation.

3.4 DC, RF and noise characterization

The device DC characteristics (I-V characteristics, Gate leakage, Breakdown, and g_m etc.) were carried out on wafer using a HP4156 semiconductor parameter analyzer. The ATN NP5 measurement system is used to characterize two-port devices for S-parameter and noise parameter measurement as a function of source impedance. These measurements can be carried out on a single contact of the device, without loading and re-contacting the devices on individual measurement. And the measurement allows the combination of measurement type, frequencies and biases. The system consists of several separate core component to perform the small-signal measurement, such as NP5 mainframe, Mismatch noise source (MNS) and a remote receiver module (PRM). These core component are combined with a test equipment (Network Analyzer, Noise Figure Meter, Computer and various other accessories) to make of this system. The schematic diagram is shown in Fig.3.9.

Fig. 3.9 Block diagram of overview of microwave noise measurement system

The NP5 system consists of a mainframe controller and two remote modules suitable for mounting on a probe station. The port 1 (input) module, the Mismatch Noise Source (MNS), contains solid state electronic tuner with a built-in bias tee and switching circuitry. The port 2 (output) module, the Remote Receiver Module (RRM), contains a bias tee, switching, circuitry, and a low noise amplifier.

The NP5 system is designed to make noise measurements of two-port devices. There are major categories of measurement types that the system performs in order to support noise characterization of the active DUT:

- a) DC measurements
- b) Small-signal S-parameter measurements
- c) Noise power measurement

The first two mainly supports the noise power measurements. NP5 system function comprises of three major interrelated parts: calibration, measurement, and report. The calibration is the most important step for achieving the good results.

Chapter 4 Studies on Thermal Stability of Metamorphic HEMT Structure

4.1 Introduction

Metamorphic InAlAs/InGaAs/InP HEMT structures grown on GaAs substrate have recently attracted considerable increased interest because it has lower substrate cost, a matured backside process and high flexibility for the energy band engineering. Though the post growth stability of the metamorphic structure as well as device reliability is a major concern for the practical application of metamorphic technology, the stability of metamorphic structures is not yet thoroughly investigated. There is only very limited experimental information available concerning thermal stability of the metamorphic HEMT structures [32]. It is believed that the presence of defects and dislocations in the active region of a device will provide a negative impact on the device stability and reliability. In general, a dislocation may serve as an effective sink to getter impurities and point defects during post-growth device processing and device operation. If such dislocation gettering and evolution happen in the device active region, we would expect a gradual degradation in the device performance which could result in catastrophic damage to the device. On the other hand, if the defect gettering process can be properly managed, it may provide an effective means to improve the device performance. A typical example is the defect and impurity gettering process that is widely used in the silicon industry. By introducing a large amount of defects and dislocations on the backside or in non-critical region of the silicon wafer, the defects and impurities in the active region will diffuse and segregate towards the backside of the wafer or gettering sinks during device processing. This subsequently improves the device performance and yield. In the case of MHEMT

structures, where a dislocation network is located immediately beneath the active device region (0.5-1 μm away) in the metamorphic buffer, it is unclear whether these dislocations will serve as a sink to getter the defects and thus improve the device quality, or whether the presence of the threading dislocations in the MHEMTs will instead deteriorate the structural stability.

In the present work, the effect of rapid thermal annealing on the optical and electrical properties of metamorphic HEMT structures grown on GaAs substrate with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ composite channel are systematically investigated. Surprisingly, the metamorphic structures exhibit better thermal stability with less degradation on n_s and mobility especially at RTA temperatures higher than 550°C. An improvement of the PL intensity in the temperature range of 550 to 650°C for metamorphic samples, similar to the results reported in Ref. [32], was clearly observed. This behavior is absent in lattice-matched HEMTs after high temperature RTA. PL intensity improvement as observed in metamorphic structures provide clear evidence of a dislocation related gettering of defects and impurities induced by the dislocation network in the metamorphic buffer immediately beneath the device zone.

4.2 Sample and Experimental Details

The HEMT structures with an InGaAs/InP composite channel used in this study were grown by solid source molecular beam epitaxy. The metamorphic structures were grown on (100) semi-insulating GaAs substrate with a step-graded $\text{In}_x\text{Al}_{1-x}\text{As}$ ($x=0\sim0.52$) metamorphic buffer layer. The growth temperature is about 300°C for the metamorphic buffer and is about 450 °C for the other part of structures. Generally speaking, the purpose of inserting a metamorphic buffer between substrate and the desired HEMT structure is to

accommodate the lattice mismatch and reduce the number of threading dislocations. A compositionally graded layer, such as the $\text{In}_x\text{Al}_{1-x}\text{As}$ used in our structure, is a good candidate. Unlike the uniform-composition layer, the graded layer changes its composition gradually and continuously accumulating small amounts of misfit strain during the growth, while the dislocation generation reduces the elastic strain in the layers. As pointed in the model by Kim *et al.* [33], in such a case, the misfit dislocations distribute along the thickness, and at the very top of the graded layer, the buffer region may be close to dislocation-free. Fig. 4.1 is a schematic illustration of the dislocation distribution in the metamorphic buffer.

Fig. 4.1 Schematic illustration of the dislocation distribution in the metamorphic buffer.

The lattice-matched structures on (100) InP substrates were also grown to serve as the control samples under same conditions, except without metamorphic buffer. The nominal indium composition for the InGaAs channel is 53%. Detailed epilayer structures are shown in Table 4.1. XRD measurements were carried out for HEMT structures, as shown in Fig.4.2. For LHEMT on InP substrate, XRD showed good lattice-matching for the whole structure. For MHEMT on GaAs substrates, XRD showed typical lattice-relaxation information from its metamorphic buffer.

Table 4.1 Lattice-matched and metamorphic HEMT structures used in this work

Layer	Material		Thickness (Å)
	Lattice-Matched	Metamorphic	
10	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$		100
9	$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$		200
8	Upper doping $5.0 \times 10^{12} / \text{cm}^2$		
7	$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$		50
6	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$		100
5	InP		50
4	$\text{N}^+ - \text{InP}$		100
3	$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$		50
2	Lower doping $1.5 \times 10^{12} / \text{cm}^2$		
1	$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$		2500
		$\text{In}_x\text{Al}_{1-x}\text{As}$ (graded)	7000
	InP substrate	GaAs substrate

Fig. 4.2 Typical XRD rocking curves from LHEMT and MHEMT structures

The metamorphic sample shows a slightly higher carrier sheet concentration ($n_s=5.12 \times 10^{12} \text{ cm}^{-2}$) and room temperature mobility ($\mu=6890 \text{ cm}^2/\text{V's}$) than those

measured from the lattice-matched sample with $n_s=4.33 \times 10^{12} \text{ cm}^{-2}$ and $\mu=6640 \text{ cm}^2/\text{V}\cdot\text{s}$. This could be attributed to a slightly high indium composition of InGaAs channel in the metamorphic HEMT sample owing to the fluctuation of growth condition.

To study the effect of RTA temperature on the material properties, the samples cut from the same wafer were annealed at different temperatures in the range of 350 to 650°C using a commercial RTA chamber. The annealing time is fixed at 10 seconds because the most common high temperature process during our HEMT device fabrication is RTA for Ohmic contact formation, where the typical anneal time is 10 sec. To maintain the thermal stability of surface and reduce potential oxidation, RTA was carried out in a N_2 ambient and the front surface of sample is closely covered with another dummy wafer to suppress potential element desorption. Therefore, it is believed the process would not bring noticeable surface desorption or change in the state of oxidation. After RTA, electrical and optical properties of samples are characterized by Hall measurements and low-temperature PL measurements, respectively.

4.3 Results and Discussion

Fig. 4.3 (a) and (b) show the n_s and room temperature mobility as the function of annealing temperatures for both InAlAs/InGaAs metamorphic and lattice-matched HEMT (LHEMT) structures. It can be seen that both our metamorphic and control samples show a reduction of n_s with increasing annealing temperatures. Surprisingly, compared to the control lattice-matched structure, the metamorphic structure displays much smaller degradation for n_s . The reduction of n_s in the metamorphic structure seems to saturate at about $4.6 \times 10^{12} \text{ cm}^{-2}$ when the annealing temperature is higher than 550°C, whereas the control sample shows a significant reduction of n_s at temperatures higher than 550°C. As

shown in Fig. 4.3(b), the variation of mobility is relatively small for both structures when the annealing temperatures are lower than 550°C. However, there is a significant reduction of mobility for the control wafer when the annealing temperature was higher than 550°C. Sugiyama *et al.* attributed the reduction of n_s at annealing temperature higher 550°C to the transfer of Si donors from Ga- or In- substitutional sites to interstitial sites [34,35]. It is, however, unclear whether the presence of defects, dislocations and residual strain in the

Fig. 4.3 Sheet carrier density n_s (a) and room temperature electron mobility (b) of metamorphic HEMT and lattice-matched HEMT structures as the function of annealing temperatures

metamorphic structure will retard this transfer process. Nevertheless, the n_s and mobility data shown here suggest that the metamorphic structure is stable during the thermal processing.

The reduction of n_s in InP HEMTs subjected to RTA at temperatures lower than 550°C has been intensively studied in recent years. One of the most popular explanations is the formation of a F-Si complex (donor passivation) in the InAlAs barrier. It is believed that the origin of F contamination is in the ambient (HF in the air) [36,37]. An increase in F concentration in the InAlAs layers after RTA has been observed in our samples using secondary ion mass spectrometry (SIMS) as shown in Fig. 4.4. Figs. 4.4 (a) and (b) show SIMS results for the samples without RTA treatment and after RTA at 450°C, respectively. It is found that the counts for F atoms in the sample after 450°C RTA is 2~4 times higher than that in sample without RTA, especially for InAlAs layers. The counts for As and P host atoms show no significant difference between samples without RTA and after RTA, indicating good repeatability of the measurements. First-principles calculations have suggested that, in InAlAs, fluorine and silicon atoms may form stable F-Si complex and thus reduce the carrier density [38]. However, F-Si complexes are neutral and their effect on the carrier-scattering and thus electron mobility should be minimal. Therefore, the formation of F-Si complex may serve as a good explanation to our Hall measurement results at RTA temperature lower than 550°C, which show a reduction of n_s with almost unaffected mobility when the RTA temperature is increased.

Fig. 4.4 SIMS results for the samples without RTA treatment (a) and after RTA at 450°C (b), respectively. The detection time from 0 to 1000s corresponds to the depth range from InGaAs cap layer to InP layer in the samples.

To gain further insights to the effect of RTA on the MHEMT structures, low temperature PL measurements were performed. In a HEMT structure, the occupation of the electron and hole subbands in the channel region could be largely affected by the n_s and the Fermi level (E_F). Therefore, by investigating the absolute and relative intensities from the first and second electron subbands to the first hole subband transitions, the variations of n_s and E_F subjected to RTA could be analyzed. For instance, if the electron density is very low, only the lowest subband (e_1) will be occupied. When the electron sheet density is increased, subsequently, and if the first subband is fully filled with electrons, more electrons will populate the second subband. The radiative recombination

of electrons and holes between different subbands could result in the emission of different wavelengths or photon energies and can be easily monitored by PL measurement.

Fig. 4.5 shows the typical PL spectra measured from metamorphic (solid line) and lattice-matched (dashed line) structures prior to RTA. The metamorphic sample shows a marginally lower emission intensity indicating that the material quality of the epilayer

Fig. 4.5 5K PL spectra of as-grown samples for InP-based MHEMT (solid line) and LHEMT (dashed line) structures

grown on the metamorphic buffer is not significantly different from that of lattice-matched sample. Transitions from the first and second electron subbands to first heavy-hole subband ($e_1 - hh_1$ and $e_2 - hh_1$) can be clearly observed. The emission at lowest energy corresponds to the transition of $e_1 - hh_1$ in the InGaAs channel region. The emission at high energy can be referred to the transition of $e_2 - hh_1$ of InGaAs channel. The $e_2 - hh_1$ transition in a symmetric quantum well could be forbidden due to the violation of the parity selection rule. However, in the asymmetric well given in our HEMT structures, it is

no longer parity restricted. For structures with an InGaAs channel well width of 15nm, which is several times larger than the mean separation of e_1 electrons from the interface, the electron-hole wave function overlap $\langle e_2 | hh_1 \rangle$ could be as larger as $\langle e_1 | hh_1 \rangle$ [39]. This results in a high probability of $e_2 - hh_1$ transition.

In both metamorphic and control wafers, the PL intensities of $e_1 - hh_1$ transition ($I_{e_1-hh_1}$) is much higher than the one of $e_2 - hh_1$ transition ($I_{e_2-hh_1}$), which suggests that, for given structures, the E_f is located at photon energies below the second electron subband [39, 40]. Compared to the lattice-matched sample, PL emissions in the metamorphic sample are shifted towards lower energy levels. The $e_1 - hh_1$ transition in the metamorphic sample is located at about 0.78 eV, which is about 40 meV lower than the one measured from the lattice-matched structure. The $e_2 - hh_1$ transitions for the metamorphic and lattice-matched sample are around 0.84 and 0.925 eV, respectively. Based on the 40meV red shift of $e_1 - hh_1$ transition, using a first order approximation, the indium composition in the InGaAs channel for the metamorphic sample is calculated to be ~3% higher than the control wafer, which is within the composition variation of the MBE growth. The relatively higher indium content, which results in narrower bandgap, can be used to explain the higher room temperature mobility in the metamorphic sample. It is also found that, for the MHEMT structure, the relative PL intensities of $e_2 - hh_1$ and $e_1 - hh_1$ peaks $I_{e_2-hh_1} / I_{e_1-hh_1}$ is slightly higher. Generally, $I_{e_2-hh_1} / I_{e_1-hh_1}$ could reflect the occupation condition of the electron density at the first sublevel e_1 and second sublevel e_2 . Higher $I_{e_2-hh_1} / I_{e_1-hh_1}$ implies higher electron population at e_2 and thus higher total electron concentration. This is in consistent with our Hall results that MHEMT structure shows slightly higher electron concentration than the LHEMT structure, which may also

result from slightly higher In composition in InGaAs channel due to the fluctuation of growth condition.

Although the metamorphic and lattice-matched heterostructures are almost identical, the splitting between the PL $e_2 - hh_1$ and $e_1 - hh_1$ energies is different (~60 and 105 meV, respectively). In general, the MHEMT structures present smaller splitting between the PL $e_2 - hh_1$ and $e_1 - hh_1$ energies. Similar results can be found from the literature. For example, the splitting between the PL $e_2 - hh_1$ and $e_1 - hh_1$ energies measured from MHEMT with 14 nm InGaAs channel reported in Ref. [32] is around 65 meV. A ~100 meV splitting between the $e_2 - hh_1$ and $e_1 - hh_1$ emissions for a LHEMT with a similar InGaAs channel thickness (15 nm) was reported by Sugiyama *et al.* [34] In an ideal condition, energy difference between the $e_2 - hh_1$ and $e_1 - hh_1$ should be the same for MHEMT and LHEMT, with assuming the HEMT structure was exactly identical and the metamorphic buffer provided a exactly same matrix as a InP substrate. Therefore, the smaller energy difference observed in this work and other literatures should origin from potential inconsistency occurred in above assumptions. As we know, although the design and the growth of a metamorphic buffer have been optimized, there are still certain amount of the dislocations could penetrate to upper layers. In addition, the difference between a non-ideal metamorphic buffer and InP substrate will cause difference in the strain field for upper layers. These differences in dislocations and strain field may influence the bandgaps of channel layer and barrier layer, doping uniformity and interface roughness in a complicated way. Therefore, exploring the potential reasons for the smaller splitting between the PL $e_2 - hh_1$ and $e_1 - hh_1$ energies in MHEMT would need more extensive studies with deliberated experiment design.

Figure 4.6 shows the low-temperature (5K) PL spectra measured from (a) metamorphic samples and (b) lattice-matched samples after RTA at different temperatures. In general, both structures exhibit the reduction of PL intensity with the RTA temperature except for the metamorphic sample annealed at 650°C. In Fig.4.7, the normalized PL intensities ($I_{\text{RTA}}/I_{\text{Fresh}}$) are re-plotted to provide a better illustration of the variation of PL intensity. Since the trend is same for the $e_1 - hh_1$ and $e_2 - hh_1$ transition peaks, only the intensities of $e_1 - hh_1$ transitions are shown for clarity.

Fig. 4.6 Low-temperature (5K) PL spectra measured from (a) MHEMT and (b) LHEMT samples after RTA at different temperatures.

For the metamorphic structure, the temperature-dependence of the PL intensity clearly depicts two distinct regions. At RTA temperatures lower than 550°C, the PL intensity decreases with the increase in the RTA temperature. When the RTA temperature is higher than 550°C, a reverse trend is seen. In addition, we had also compared the RT PL

integrated intensity for samples under different anneal temperatures, which shows same trend as 5K PL results.

In the low temperature region, both the metamorphic and control lattice-matched structures roughly follow a similar trend suggesting that a reduction of PL intensity for both structures may share the same degradation mechanism. Considering the reduction of PL intensity in Fig. 4.7, one would tend to suggest that RTA of metamorphic HEMT structure in the temperature range of 350 to 550°C could cause significant degradation of

Fig. 4.7 Normalized PL intensity ($I_{\text{RTA}}/I_{\text{fresh}}$) for MHEMT and LHEMT structures as a function of RTA temperature. Both MHEMT structure with single InGaAs channel and InGaAs/InP composite channel are used for test. Only the intensities of $e_1 - hh_1$ transition are shown for clarity.

material quality resulting in the decrease in PL intensity in accordance with well-established theory. This inference is, however, not supported by the measurement of

emission peak width. The full width at half maximum (FWHM) of the room temperature PL spectra for the samples annealed at different temperatures is plotted in Fig. 4.8. The FWHM is in the range of 120 to 170 meV, which is comparable to the data reported for InP-based HEMTs [41,42]. The FWHM of the samples are insensitive to annealing temperature. In fact, a decrease in FWHM of the metamorphic structure is clearly observed further suggesting an improvement in the material quality of the metamorphic structure after RTA. Generally, the FWHM of PL peak is directly related to material quality of the HEMT structure, including defect density, channel/barrier interface roughness etc. Although it is difficult to directly identify the exact reason for a reduction in PL FWHM, however, decreased defect density and enhanced uniformity are potential effects from RTA when it introduces atom-scale structural reorganization. Therefore, a decrease in PL FWHM of the HEMT generally suggests an improvement in the material quality, especially the channel region in HEMT structure.

Fig. 4.8 Room temperature FWHM of MHEMT and LHEMT samples annealed at different temperatures

Considering the correlations between the temperature dependence of Hall measurement and PL spectra presented in Figs. 4.3 and 4.7, the decrease in the PL intensity with the increase in annealing temperatures in the range of 350 to 550°C could be explained based on the reduction of n_s in an HEMT structure. The PL spectrum under consideration is identified as band-to-band (sub-band to sub-band) recombination involving the photogenerated hole and electrons in the InGaAs channel region. Thus, the PL emission intensity is determined by the channel electron density and the optically excited holes in the channel and barrier region [43,44]. Notice that the holes generated in the InAlAs and InP barriers may also drift into the InGaAs channel and subsequently recombine with the electrons in the two-dimensional electron gas. Assuming that the photo-generated electron density is much smaller than n_s , the PL intensity I_{PL} can be expressed by [45],

$$I_{PL} = Bn_s p_{excited} \quad (4.1)$$

Where B is the spontaneous recombination coefficient, $p_{excited}$ is the excited hole concentration in the channel region which could be directly related to the laser pumping intensity during the PL measurements. Therefore, for a fixed laser pumping intensity, a reduction in the PL intensity is expected if n_s is reduced by the fluorine passivation of Si donor.

It is interesting to look into the drastic increase in the PL intensity of the metamorphic samples annealed at temperatures higher than 550°C. To further validate the observation, PL measurements were performed on a set of metamorphic samples having a simpler structure with a single 12nm InGaAs channel. Similar results were obtained and are included in Fig. 4.7. This suggests that the increase in the PL intensity of samples annealed at high temperature is not a unique behavior for the composite channel

structures. In fact, the same trend can be found in results reported by Cui *et al.* [32], indicating some similarities on metamorphic devices. Cui *et al.* [32] suggest that the increase in the PL intensity of metamorphic devices after high temperature RTA could be due to the improvement of the crystal quality. Notice that such a behavior is not observed in the control lattice-matched samples. The discrepancy between the metamorphic and control samples at high annealing temperatures could be consistently explained by the defect or dislocation gettering effect due to the presence of a dislocation network in the metamorphic buffer.

Extensive studies in compound semiconductors such as GaAs or InP have shown a strong correlation between luminescence intensity and dislocation structures [46,47]. The role of the dislocations is confirmed to be that of gettering of nonradiative recombination centers [46,48]. In MHEMT structures, the existence of a metamorphic buffer with a larger number of dislocations distributed about 0.5 μm under the active layers may server as an effective sink for the gettering of impurities and native defects. This could be supported by the study on InP/InGaAsP heterostructures suggesting a diameter of $\sim 1.5 \mu\text{m}$ of the getter zone around the dislocation/defect [46]. During the RTA process, the impurities and native defects in the active layer may segregate into the dislocation network in the metamorphic buffer through the bulk diffusion or the diffusion via the threading dislocations. In order to achieve a significant dislocation gettering effect, an annealing temperature higher than 550°C is normally required according to the previous studies [49]. This is consistent with what was observed in the present work with the onset of the increase in PL intensity in the metamorphic samples at $\sim 550^\circ\text{C}$. If the increase in the relative PL intensity I_{RTA}/I_{fresh} is directly related to the annihilation rate of defects and impurities from the active region due to dislocation gettering, we would expect the I_{RTA}/I_{fresh} to follow:

$$I_{RTA}/I_{fresh} \propto \exp(-E_a / KT) \quad (4.2)$$

where E_a is the activation energy of the gettering process. The plotting of the dependence of the PL intensity on annealing temperature in range of 450-700°C (shown in Fig. 4.9) did indeed reveal an Arrhenius dependence of I_{RTA}/I_{fresh} on annealing temperature T . An activation energy in the range of 0.22-0.57 eV can be determined. The values are significantly lower than the activation energy of 1.13 eV for fluorine diffusion in InAlAs [50] and the activation energy of 1-1.3 eV for the thermal annealing of defect centers or migration of vacancies in InP [51,52]. It is unclear whether the presence of a high density of threading dislocations ($10^6 \sim 10^7 \text{ cm}^{-2}$) will enhance the diffusion of defects and impurities towards the dislocation network in the metamorphic buffer. Additional studies are required to understand the kinetics of the gettering effect observed in MHEMT structures.

Fig. 4.9 Temperature dependence of I_{RTA}/I_{fresh} at temperatures higher than 500°C in MHEMT structures.

Thermal interdiffusion at the heterointerface has been found in several material systems such as GaAs/AlGaAs [53], InGaAs/InP [54], and InAlAs/InGaAs [55] etc. The interdiffusion will limit the device process conditions. For the structures with a composite channel, the thermal stability of the InGaAs/InP heterointerface in the channel region could be even more important. Deterioration of the InGaAs/InP interface quality may result in the increase in interface scattering and thus the reduction of mobility. Measuring the relative shift of energy position of $e_1 - hh_1$ transition in quantum well has been widely used to monitor the interdiffusion. Fortunately, both metamorphic and control samples only exhibit a very small blue shift (<5 meV) as shown in Fig. 4.10. No sign of enhancement of thermal interdiffusion at the heterointerface is found in the metamorphic structures.

Fig. 4.10 Shifts of peak energy position of $e_1 - hh_1$ transition for MHEMT and LHEMT structures annealed at different temperatures.

4.4 Summary

We have compared the annealing effect of metamorphic InAlAs/InGaAs HEMT structures grown on GaAs substrates with the conventional InP-based HEMT structure. No evidence for the retardation of the structural thermal stability due to the incorporation of a strain-relief metamorphic buffer was observed. In fact, compared with the lattice-matched HEMT structures, the metamorphic structures show less degradation in both carrier sheet density and mobility when the annealing temperature is higher than 500°C. This is consistent with the recent observation by Cui *et al.* [32]. Low temperature PL characterization reveals an improved photoluminescence intensity in the temperature range of 550~700°C with negligible change in the PL emission energies in the MHEMT structures suggesting the presence of possible dislocation gettering effect. The dislocation network in the metamorphic buffer may serve as an effective sink for the gettering of impurities and native defects. The less than expected degradation in the electrical and optical properties of metamorphic HEMT structures subjected to RTA may partially ease the concerns on the device stability of metamorphic HEMT technology.

Chapter 5 Effect of SiN Passivation on Transport Properties in InGaAs/InP Composite Channel HEMT Structure

Chapter 5 Effect of SiN Passivation on Transport Properties in InGaAs/InP Composite Channel HEMT Structures

5.1 Introduction

Passivation of the electronic device is important to improve the device performance and long-term reliability by preventing the device degradation induced by the environment and mechanical scratches. In a typical InP-based HEMT structure, InAlAs serves as the barrier layer to form a good Schottky gate. It has been found that the exposed InAlAs recess areas immediately next to the gate plays a critical role in determining the device characteristics such as I-V kink and gate leakage [56,57,58]. As illustrated in Fig. 5.1, passivation of the access area between gate, source and drain, especially the exposed InAlAs in the recess window is necessary; this requires good control of the SiN/InAlAs interface.

Fig. 5.1 Cross section of an InP HEMT with SiN passivation. Passivation of the access area between gate, source, and drain, especially the exposed InAlAs in the recess window, is illustrated.

Although passivation of InP-based devices using PECVD silicon nitride has been used at production level, information on whether SiN passivation alters surface potential and surface Fermi level and how the SiN passivation affects the carrier transport in a HEMT structure is still very limited. A better understanding of the influence of SiN passivation on InAlAs/InGaAs HEMT structures and its physical origin is necessary for design, fabrication, and parameter optimization of InP HEMTs to further enhance the device performance.

The surface Fermi level is generally pinned in the energy gap at the semiconductor surface by a sufficiently large density of extrinsic surface states. It has been observed that for GaAs [59], AlGaAs [60], the Fermi level is firmly pinned at the midgap, while for InP, the Fermi level is pinned at 0.35 ± 0.01 eV below the conduction band edge [61]. However, recent studies indicated that the surface Fermi level pinning in InAlAs is relatively weak and can vary from 0.5 to 0.81 eV below the conduction band edge due to the lower surface state density of InAlAs [62]. This could impart favorable passivation of an InAlAs surface using dielectrics. However, experimental results for the passivation of an InAlAs surface using SiN remain inconclusive. By comparing the measured sheet carrier densities with the modeling results by a self-consistent simultaneous solution of Schrödinger's and Poisson's equations, Arps *et al.* [63] suggested a possible increase in the surface Fermi level towards the conduction band edge in InAlAs after PECVD SiN passivation. The shift in Fermi level at the InAlAs surface towards the conduction band edge after deposition indicates the possibility of passivation of surface states in InAlAs by PECVD SiN. A similar conclusion was made lately by Boudart *et al.* [64] from the observation that maximum drain of InP HEMT increases after SiN passivation, due to a decrease in surface potential. On the other hand, experimental data reported on InP HEMTs passivated by

inductively coupled plasma (ICP) PECVD SiN, which is supposed to have lower surface damage and better passivation, show a contradicting trend [65]. The experiment revealed a shift in the surface Fermi level towards the valence band edge in the drain and source access regions. Further experimental studies on SiN passivation to understand its physical origin are necessary. The results will be of relevance for designing a variety of optoelectronic, high-speed, and microwave devices involving InAlAs.

There is a growing interest in the use of InGaAs/InP composite channel design to improve breakdown, output conductance, gate leakage, and RF performance at high field [17]. Current studies are motivated by a desire to assess the influence of SiN surface passivation on the electronic properties of the 2DEG in an InAlAs/InGaAs/InP CC-HEMT structure. The carrier transport and optical properties in the CC-HEMT structures subjected to SiN passivation have been comprehensively characterized. Our results reveal that the deposition of SiN on the InAlAs/InGaAs/InP CC-HEMT epitaxial layer structure induces substantial and reversible changes in room temperature Hall mobility with negligible variation of sheet carrier density. This is different from the effects observed for the single InGaAs channel structure reported in Ref. [63]. However, the experimental results can be consistently explained by shifting the Fermi level at the InAlAs surface towards the conduction band edge, resulting in the spill-out of electrons from the doped InP subchannel to the InGaAs channel region which enhances the overall channel electron mobility. Low temperature PL measurements provide further evidence to support this mechanism. Moving the surface Fermi level towards the conduction band indicates that the SiN/InAlAs interface has a different, and possibly reduced, density of electronic states compared to the SiN free surface, which provides useful information for the use of PECVD SiN to passivate the InP HEMT devices with InAlAs barriers.

5.2 Experiments

The SiN passivation effects were studied on an InP HEMT structure grown by molecular beam epitaxy on semi-insulating (100) InP substrate. The detailed epilayer structure is shown in Table 5.1. The composite channels comprise of InGaAs and InP, where the nominal indium composition for the InGaAs channel is 53% and the InP subchannel consists of the doped InP and undoped InP channel. In the comparison structure, a single InGaAs channel HEMT structure, has a 14nm InGaAs channel layer with indium composition of 53% was used for the channel. The other layers remained unchanged.

TABLE 5.1 Epilayer structures of the HEMT wafers used in this work.

Layer	Material		Thickness (Å)
	Composite Channel	Single Channel	
10	In _{0.53} Ga _{0.47} As		100
9	In _{0.52} Al _{0.48} As		200
8	Upper doping 5.0×10 ¹² /cm ²		
7	In _{0.52} Al _{0.48} As		50
6	In _{0.53} Ga _{0.47} As	In _{0.53} Ga _{0.47} As (140 Å)	100
5	InP		50
4	n ⁺ -InP		100
3	In _{0.52} Al _{0.48} As		50
2	Lower doping 1.5×10 ¹² /cm ²		
1	In _{0.52} Al _{0.48} As		2500
	InP substrate		

After the formation of the isolation mesa, the Ni/Ge/Au/Ni/Au Ohmic contacts were formed on the InGaAs cap. To form the van der Pauw pattern for Hall measurements, the InGaAs cap in the region without contacts was removed by selective wet etching to expose the InAlAs barrier layer. The etching procedure is kept same for all samples to maintain the process uniformity. We try to do the SiN deposition immediately after sample etching to reduce potential formation of oxide patch afterwards; therefore the effect is minimized and may be considered similar for all samples. SiN was then deposited using PECVD

followed by contact pad opening. Samples with different SiN thicknesses were prepared. The SiN deposition was carried out in a Plasma-Therm model 790 PECVD system equipped with a capacitively-coupled 13.56 MHz source excitation. SiH₄, NH₃ and N₂ are used as reactant gas. The plasma ignition is without electron injection. RF induced plasma source ignites a plasma and creates a plasma field in the deposition gas. The sample is simply supported by a susceptor in the vacuum chamber. Since plasma-induced damage is concerned during the plasma ignition step within first several seconds when plasma was unstable and unbalanced as well as during deposition, a lower RF power of 40W was used to reduce the potential plasma damage on the surface. The deposition temperature is 300°C and the deposition rate is 140Å/min. Then the electrical and optical properties of the samples were characterized by Bio-Rad Hall effect measurement and PL measurement.

5.3 Results and discussion

Figure 5.2 shows the electron mobility μ_e and sheet carrier density n_s as a function of SiN layer thickness. Compared with the un-passivated sample, deposition of SiN onto the un-gated structures results in a drastic increase in μ_e . However, the n_s is only marginally affected. For example, after a 100nm SiN deposition, the μ_e is increased from 4050 to 5450cm²V⁻¹s⁻¹, while the variation of n_s is negligible (only changes from 2.45×10⁻¹²cm⁻² to 2.41×10⁻¹²cm⁻²). The most noteworthy observations from Fig. 5.2 are that the increase in μ_e is induced by SiN passivation but is insensitive to film thickness if the SiN thickness is larger than 150nm. The increase in μ_e is reversed upon removal of the SiN by wet etching. The almost unchanged μ_e with increase in SiN thickness in the

range of 100 to 800nm indicates that the variation of μ_e is unlikely due to the strain induced by SiN passivation.

Fig. 5.2 Sheet carrier density and mobility as function of SiN thickness for InP HEMT structures with an InGaAs/InP composite channel.

Many different factors could contribute to the variation of electron mobility in the 2DEG channel. For example, reducing surface, interface, and bulk material defect density due to hydrogen (H) passivation during the PECVD process may contribute to the increase in μ_e [66]. Furthermore, a change of surface potential by SiN surface passivation might also affect the carrier transport in the channel. However, the first two postulates could not be supported by the hall measurements made from the InP HEMT structures with a single InGaAs channel after PECVD SiN deposition. If the improving barrier/channel interface quality and hydrogen passivation played dominant roles for the increase in electron mobility, similar enhancement of electron mobility after SiN passivation should also be observed in the InP HEMT structures with a single InGaAs channel. This is, however, not the case as shown in Fig. 5.3 by comparison of Hall mobility measured from single InGaAs channel HEMT structures with different thicknesses of SiN. The electron mobility

in the single InGaAs channel structures seems insensitive to SiN passivation. A slight increase in sheet carrier density after coating the SiN was observed, which is in agreement with the results reported by Arps *et al.* [63]

Fig. 5.3 Sheet carrier density and mobility as the functions of SiN thickness for InP HEMT structures with a single InGaAs channel.

To have a better understanding on the enhancement of μ_e by SiN passivation, PL characterizations were carried out. Figure 5.4 shows the typical PL spectra measured at 5K from the samples with different SiN thickness. Two distinct emission peaks can be observed, which are attributed to the transitions of $e_1 - hh_1$ and $e_2 - hh_1$. For clarity, only three curves are shown in the plot. As shown in the Fig. 5.4(b), the peak positions are almost unaffected by the SiN passivation. The peak positions of $e_1 - hh_1$ and $e_2 - hh_1$ are centered at about 0.816 eV and 0.925 eV, respectively. The fluctuation of both peak positions only ranges about $\pm 0.003 \text{ eV}$. These indicate that no change of channel thickness and composition is induced by SiN passivation.

Fig. 5.4 (a) PL spectra for the samples with different SiN thickness. (b) PL peak positions of e_1-hh_1 .

It is generally believed that improvement of structural quality, such as reducing surface, interface and bulk material defect density, could be effectively monitored by PL intensity. Figure 5.5 compares the PL intensity from samples with different SiN thickness. Necessary corrections for the PL intensity had to be made so that the PL intensity for different samples can be directly compared in Fig. 5.5. The raw PL intensity data are plotted as the inset of Fig. 5.5. The PL correction was carried out with considering the PL

laser beam has different transmission when a SiN layer of different thickness is inserted between air and sample. The calculations are based on Fresnel equations of reflectance and transmission in two parallel interfaces [67]. For SiN layer thinner than 300 nm, no significant change of PL intensity is found. However, further increase in the SiN thickness results in an increase in the PL intensities by a factor of 20. It is unclear whether the drastic increase in PL intensity in the samples with thicker SiN is due to the long thermal annealing time during the PECVD process, or the possible H passivation in the structure. Only a partial recovery of the PL intensity observed on those samples with SiN thickness

Fig. 5.5 PL peak intensities of e_1-hh_1 and e_2-hh_1 emissions as a function of SiN thickness. Inset: PL peak intensities of e_1-hh_1 and e_2-hh_1 emissions without intensity correction as a function of SiN thickness.

larger than 300nm after the SiN is etched off may provide a possible support for the above postulation. Nevertheless, no evidence of change of material quality in the samples with SiN layer less than 300 nm was found. This shows that increase in μ_e , which occurs for

much thinner SiN, could not be directly linked to the mechanisms related to defect or dopant passivation.

One apparent feature of the PL spectra, which could be linked to the change of surface potential due to passivation, is a relative variation of the $e_1 - hh_1$ and $e_2 - hh_1$ intensities after SiN deposition. It can be interpreted as a change of Fermi level position in the InGaAs channel region associated with modification of the surface potential (surface Fermi level) value due to the SiN passivation. In the HEMT structures with the Fermi level staying below e_2 , a strong $e_1 - hh_1$ transition would be expected, which is the case presented in our samples. When the structure is passivated by SiN, the surface potential could be modified. If the Fermi level at the surface and well regions moves up, as illustrated in the schematic of conduction band diagram for a composite channel HEMT structure in Fig. 5.6, and the second subband becomes more populated, an increase in the $e_2 - hh_1$ recombination would be expected. As a result, the peak intensity ratio between $e_2 - hh_1$ and $e_1 - hh_1$ transitions ($I_{e_2-hh_1} / I_{e_1-hh_1}$) increases. In other words, increase in $I_{e_2-hh_1} / I_{e_1-hh_1}$ indicates that Fermi level in InGaAs channel is approaching e_2 from lower energy position. Previous studies on PL spectra in gated HEMT structures had shown excellent correspondence between the relative intensities of the two PL transitions and Fermi level position tuned by gated bias [68]. Therefore, even though the comparison of PL spectra measured from the passivated and unpassivated samples does not allow a quantitative determination of the surface potential (Fermi level) variation, studies on the changes of the ratio of PL emission intensities between $e_2 - hh_1$ and $e_1 - hh_1$ transitions ($I_{e_2-hh_1} / I_{e_1-hh_1}$) may still provide information on the possible modification of the surface potential by SiN passivation. Figure 5.7 shows $I_{e_2-hh_1} / I_{e_1-hh_1}$ as a function of SiN

thickness. An unambiguous similarity between the ratio of $I_{e_2-hh_1} / I_{e_1-hh_1}$ versus SiN thickness and the SiN thickness dependence of μ_e shown in Fig. 5.2 clearly appears. The increase in $I_{e_2-hh_1} / I_{e_1-hh_1}$ implies that the electron population at the second sublevel e_2 in

Fig. 5.6 Schematic of conduction band diagram for a composite channel HEMT structure before and after SiN passivation.

Fig. 5.7 Ratio of PL peak intensities between $e_2 - hh_1$ and $e_1 - hh_1$ transitions ($I_{e_2-hh_1} / I_{e_1-hh_1}$) from samples with different SiN thickness.

the InGaAs channel region is increased, which can be explained by more electrons transferred from the doped InP subchannel to the InGaAs channel region due to the decrease in surface potential. This is consistent with the results observed in the InP HEMT with a single InGaAs channel [63]. Furthermore, based on the data presented by PL and Hall measurements, if the increase in the μ_e or $I_{e_2-hh_1} / I_{e_1-hh_1}$ ratio is considered to be a good indicator for the effectiveness of SiN passivation of InP HEMT structures, the optimal thickness of PECVD SiN would be around 150nm.

From these observations, we may consistently explain the increase in electron mobility in InGaAs/InP CC-HEMT structures after SiN deposition based on the increase in electron population in the InGaAs channel region due to the increase in the InAlAs surface Fermi level towards the conduction band edge. In a composite channel structure, the effective mobility μ_e may be estimated according to the formula given by Petritz [69]:

$$\mu_e = \frac{\mu_{ch}^2 n_{s,ch} + \mu_{subch}^2 n_{s,subch}}{\mu_{ch} n_{s,ch} + \mu_{subch} n_{s,subch}} \quad (5.1)$$

where, μ_{ch} and μ_{subch} are the electron mobility of the InGaAs channel and the InP subchannel, respectively. $n_{s,ch}$ and $n_{s,subch}$ are the sheet carrier densities of the InGaAs channel and InP subchannel, respectively. After SiN deposition, the modification of surface potential or surface Fermi level bends downwards the energy band in the InGaAs channel region, subsequently causing the spill-out of electrons from the doped InP subchannel into the InGaAs channel. Therefore, we would expect an increased carrier density in the high mobility InGaAs channel and a decreased carrier density in the relatively low mobility InP subchannel which result in an enhanced electron mobility in the CC-HEMT structure. Note that the spill-out of electrons from the doped InP subchannel into the InGaAs channel will not affect the overall n_s in the CC-HEMT

structure which is the sum of $n_{s,ch}$ and $n_{s,subch}$. This explains the almost unchanged n_s after SiN passivation shown in Fig. 5.2.

Although the observed changes in 2DEG properties in InP/InGaAs CC-HEMT structures upon deposition of the SiN behave differently from the InP HEMT with a single InGaAs channel, the fundamental mechanisms are the same. The results from the InP/InGaAs CC-HEMT structures suggest that InAlAs surface properties, rather than thermal annealing or hydrogen passivation of the bulk defects incurred during PECVD deposition of SiN, are the relevant factors leading to the observed increase in electron mobility in the CC-HEMT structures. Stress within the InP/InGaAs CC-HEMT structures induced by the presence of SiN dielectrics is unlikely to be an important factor, as the increase in electron mobility appeared only when the SiN was deposited. Our experimental results provide a direct evidence of changing the InAlAs surface Fermi level position by SiN passivation; the Fermi level at the SiN/InAlAs interface is considerably closer to the conduction band than that at an unpinned surface, suggesting the presence of relatively low densities of interface states on InAlAs after SiN passivation. Measurement of electron mobility in a CC-HEMT structure may provide effective means to monitor the interface properties, which is useful for the optimization of the SiN deposition process for improving the device performance.

5.4 Summary

We have performed detailed studies of the influence of SiN passivation on carrier transport properties in InP HEMTs with an InGaAs/InP composite channel. In Previous studies on the single InGaAs channel structures, SiN passivation layers have been found to lead to a slight increase in sheet carrier density with negligible impact on mobility. However, our measurements on the InP CC-HEMT structure reveal a different behavior.

Deposition of SiN on ungated InGaAs/InP composite channel HEMT structures results in a large increase in electron mobility with little effect on electron density. PL measurements suggest that the enhancement of μ_e could be explained under the framework of electron transfer from the InP subchannel into the InGaAs channel region due to the energy band bending at the surface region caused by SiN passivation. The experimental results provide a strong evidence for modification of surface potential towards unpinned surface, suggesting the presence of relatively low densities of interface states on InAlAs after SiN passivation.

Chapter 6 Understanding of the Excess Channel Noise in InAlAs/InGaAs/InP HEMT in Impact Ionization Regime

6.1 Introduction

The presence of an excess noise related to impact ionization in InP-based HEMTs has increasingly attracted attention [7,70,71]. It has been found that the enhancement of device noise in the impact ionization regime may substantially affect the device low noise application even at microwave frequencies. The large noise observed in the impact ionization regime was initially ascribed to a high gate-drain leakage or measurement errors [72]. Rouquette *et al.* [73] and Murti *et al.* [7] lately show that a time constant as small as 25 ps could be determined by fitting the noise spectral density to the form of Lorentzian function, which suggests the possibility of the excess noise in the impact ionization regime being induced by the fluctuation of impact ionization events. On the other hand, a Monte Carlo simulation [71] has shown that the impact ionization and its related kink effect provoke an enhancement of the channel noise with a characteristic cutoff frequency related to the hole recombination. The generation of holes by impact ionization and their further recombination lead to fluctuations in the charge of the hole pile up and thus the excess noise. However, there is no experimental data to validate the contribution of hole recombination to the excess noise. In this work, we investigate the microwave noise of InP-based HEMTs to gain a fundamental understanding on the physical origin of the excess noise in the impact ionization regime, which has so far not received much attention. The results strongly suggest that hole recombination plays an important role in the enhancement of channel noise in the gigahertz range, while the contribution of the

fluctuation of impact ionization to the excess noise is substantial at relatively higher frequencies.

6.2 Experiments

The devices used in this study are InAlAs/InGaAs HEMTs with a strained $\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$ channel on semi-insulating InP substrate grown by MBE. The detailed layer structure consists of, from top to bottom, a 10 nm InGaAs cap layer, 20nm InAlAs barrier, $5 \times 10^{12} \text{cm}^{-2}$ upper Si δ -doping layer, 5nm InAlAs spacer, 15nm undoped InGaAs channel with 60% of indium content, and 250nm InAlAs buffer on InP substrate. The devices were passivated by 120nm of SiN deposited by PECVD. Two-finger devices with a gate length (L_g) and width (W_g) of 0.25 μm and 40 μm , respectively, were used for the high frequency noise characterization. The lateral extension of the recess is about 200nm controlled by selectively etching as mentioned in Chapter 3. According to studies by Strähle *et al.* [74], we can expect the length of drift region in InP-based InGaAs HEMT or InGaAs/InP composite HEMT is well below 100nm. Therefore, this lateral extension is wide enough to allow the full lateral extension of the drift region.

6.3 Results and discussion

Fig. 6.1 shows the I - V characteristics of the single InGaAs channel HEMT. The transistors demonstrated typical drain-source (I_d - V_d) - static output characteristics with a noticeable kink effect in the V_d range of 0.75 V to 1.5 V. The drain currents for the device is about 500mA/mm at $V_g=0.2\text{V}$, with obvious kink effect. The device threshold voltage

(V_{th}) is around 0.75 V and peak transconductance is around 600 mS/mm. The maximum f_T is about 105 GHz.

Fig. 6.1 I - V characteristics of a single InGaAs HEMT

The noise characterization was carried out using an ATN NP5 noise and S-parameter measurement system in the frequency range of 2~20GHz. As shown in Fig. 6.2, the electron impact ionization in the InGaAs channel induces a significant increase of the reverse gate current with respect to the Schottky diode gate leakage current resulting in a typical bell-shape curve. The bell-shaped curves start to emerge at $V_d > 0.9$ V with the peak showing at V_g around -0.6V. The evolution of high frequency noise in the impact ionization regime has been systematically characterized by varying V_g (at a constant V_d) and V_d (at a constant V_g) in the “bell-shape” region.

Fig. 6.2 Typical behavior of the increase in reverse gate current induced by channel electron impact ionization resulting in a bell-shaped gate current.

Figure 6.3 shows the minimum noise figure ($NF_{\min}$) as a function of frequency at different V_d . The bias condition of $V_g = -0.6$ V shown in this plot is to ensure that the devices were biased in the high impact ionization region during the noise measurements. At $V_d < 1$ V, $NF_{\min}$ is insensitive to V_d , and increases monotonically with the increase in frequency. However, as the drain voltage is further increased from 1 V to 2.5 V, a drastic increase in $NF_{\min}$ is measured. This increase corresponds to the triggering of the impact ionization mechanism in the channel (Figure 6.2). One salient feature to be highlighted is that, at V_d higher than 1.5 V, the $NF_{\min}$ versus frequency curves exhibit a reverse trend showing a higher $NF_{\min}$ value at lower frequencies. This has been reported by different research groups and is considered to be an important feature of the noise behavior due to

the presence of impact ionization in the channel [7,73]. However, a fundamental explanation on this anomalous enhancement of $NF_{\min}$ in the low gigahertz range has not been provided so far.

Fig. 6.3 $NF_{\min}$ versus frequency as a function of V_d measured in the bell-shape region.

The output noise of a HEMT is an overall contribution from the following two main noise sources: the channel noise $\overline{i_d^2}$ and gate current noise $\overline{i_g^2}$. The channel noise is composed of both the thermal noise and the flicker noise (can be ignored at high frequency). The gate current noise includes an induced gate noise and shot noise due to the gate leakage current. To gain a better insight into the physical origin of the excess microwave noise in the impact ionization regime, the experimental results were modeled by using an approach given in Ref. 75 to determine both the channel noise and the gate current noise. Fundamentally, there is no difference between the noise models for Si metal-oxide-semiconductor field-effect transistors and metal-semiconductor field-effect transistors or HEMTs (Refs. 76, 77) except for the negligible substrate effect and much smaller gate resistance observed in our InP HEMTs.

Figure 6.4(a) shows the extracted channel (drain) noise versus V_g as a function of V_d at 10 GHz. The figure gives the typical noise characteristic at 10GHz, while similar results were obtained at different frequencies from 2GHz to 20GHz. It is obvious that the extracted channel noise $\overline{i_d^2}$ presents a distinct bell-shaped behavior suggesting a close correlation between the channel noise and the carrier impact ionization and its related effects. The presence of the bell-shaped channel noise behavior at V_d higher than 1 V is consistent with the onset of the bell-shaped gate current shown in Fig. 6.2. The bell-shaped channel noise can be interpreted as a superposition of a conventional channel thermal noise component [78] and an impact ionization related noise component Δi_{dimp}^2 . The extracted V_g -dependent gate current noise $\overline{i_g^2}$ at different V_d are shown in Figure 6.4(b). Compared to that for channel noise, no clear bell-shaped behavior was observed except for the presence of a small shoulder in the range of V_g from -0.4 to -0.2V at $V_d=1.5\text{V}$ and 2V. The drastic increase in $\overline{i_g^2}$ at $V_g > 0$ could originate from an increase in the gate shot noise due to the large gate current. The contribution of the gate shot noise to the overall gate noise in the reverse gate bias region is insignificant. For example, in the bell-shaped gate current region, the peak leakage of $\sim 10\mu\text{A}$ at $V_d=2\text{V}$ only gives a gate shot noise ($2qI_G$) of $3.2 \times 10^{-24} \text{A}^2/\text{Hz}$ which is about ten times lower than the extracted $\overline{i_g^2}$. Hence, the major part $\overline{i_g^2}$ in the impact ionization regime should be the induced gate noise, i.e., the noise coupled to the gate through the gate capacitance from the noise generated in the channel.

Fig. 6.4 Extracted (a) channel noise $\overline{i_d^2}$ and (b) gate noise $\overline{i_g^2}$ versus V_g as a function of V_d at 10 GHz. The dot lines represent the background channel thermal noise.

To further understand the physical origin behind the additional channel noise component associated with the impact ionization, $\Delta \overline{i_d^2}$ at different frequencies were extracted by subtracting the background channel thermal noise from the total channel noise as illustrated in Fig. 6.4(a). Figure 6.5 shows the $\Delta \overline{i_d^2}$ as a function of frequency from 2 to 20 GHz. If the fluctuation of the carrier density in the channel region due to

impact ionization and its related effects, such as hole recombination and pileup that are responsible for the excess channel noise in the impact ionization regime, the spectral noise density could be predicted by using the Van der Ziel's channel current fluctuation model [79] in the form of

$$S_{i_d} = \frac{A\tau}{1 + (2\pi f)^2 \tau^2} \quad (6.1)$$

where τ is the characteristic time constant associated with the mechanism causing the carrier fluctuation. As we can see in Fig. 6.5, the $\overline{\Delta i_d^2}$ spectrum could not be fitted using a single time constant, implying the presence of more than one mechanism contributing to the excess channel noise in the impact ionization regime. The experimental data can be well fitted by using two noise components (S_{i_d-1} and S_{i_d-2} in Fig. 6.5) with time constants of $\tau_1=1$ ns and $\tau_2=9$ ps, respectively. Notably, the time constant of 1 ns is consistent with the reported hole recombination lifetime in InP HEMTs [80,81], corroborating the impact-ionization induced hole recombination mechanism. The mechanism responsible for the S_{i_d-2} could be due to the fluctuation of the impact ionization itself. Considering the impact ionization time constant, which is representative of the time for avalanche buildup, the time constant can be calculated using [82]:

$$\tau = Nk \frac{W}{v_m} M_0, \quad (6.2)$$

where k is the effective ionization rate, N is a constant depending on k (between 1/3 to 2), W is the width the avalanche region, v_m is mean velocity of the carrier in the InGaAs channel, and M_0 is the avalanche gain. To a first order approximation, using $W \cong L_g = 0.25 \mu\text{m}$, $k \cong 1$, $v_m \cong 1.5 \times 10^7$ cm/s [83], and M_0 less than 2 considering the weak

avalanche multiplication for $V_d = 1.2\text{V}$, we would expect an impact ionization time constant between 2.2 to 6.7 ps, which shows good agreement with τ_2 of 9ps.

Fig. 6.5 Excess channel noise component induced by impact ionization ($\overline{\Delta i_d^2}$) as a function of frequency. The experimental data are fitted by Van der Ziel's channel carrier fluctuation model using two noise components (S_{id_1} and S_{id_2}) with time constants of $\tau_1=1$ ns and $\tau_2=9$ ps, respectively.

In Fig.6.5, the pure thermal noise in the channel, i.e., in the noise in the channel without impact ionization is plotted as a reference background noise (shown as a dash dot line). The value of background noise can be obtained based on the extracted channel noise at low V_d , which impact ionization is trivial. As seen from Fig 6.4 (a), if we consider the device biased at $V_d = 0.5\text{V}$, the extracted channel noise value of $\overline{i_d^2}$ is around

$1 \times 10^{-21} A^2 / Hz$. Using this value of background noise as a reference level, it can be seen from Fig 6.5 that the hole recombination may result in an excess channel noise at frequency below 8GHz. The excess noise due to carrier fluctuation induced by impact ionization shows a much higher cutoff frequency (~ 40 GHz). These results strongly suggest that hole recombination plays an important role in the enhancement of channel noise in gigahertz range, while the contribution of the fluctuation of impact ionization to the excess noise is substantial at relatively higher frequencies. In addition to providing a new insight to the excess channel noise in InP HEMTs operating in the impact ionization regime, the findings here also provide important information for the understanding of noise behavior in HEMTs using a narrow bandgap material, such as InAs and InSb, where the impact ionization effect is significant.

6.4 Summary

In summary, the channel noise of InP-based single channel HEMTs has been characterized and analyzed to gain a fundamental understanding of the physical origin of the excess noise in the impact ionization regime. We find that different physical mechanisms are responsible for the excess channel noise at different frequency ranges. The excess noise in gigahertz range (below 10GHz) is mainly accounted for by the mechanism that is related to hole recombination in the channel, while the excess noise at higher frequencies could be attributed to the fluctuation of impact ionization which has a small (picosecond) time constant.

Chapter 7 Microwave Noise Characteristics of InGaAs/InP Composite Channel HEMT

7.1 Introduction

InP HEMTs are considered to be one of the most important devices for high frequency applications. Noise characteristics and models for InP-based lattice-matched and pseudomorphic HEMTs have been extensively studied [84,85]. Recent works on the composite channel HEMT have been focused only on the channel design to improve the power performance [11,12,13], however, little attention has been paid on the microwave noise characteristics of InP HEMTs with composite channel. In this work, a comparative study of the microwave noise performance between InP HEMTs with InGaAs/InP composite channel and InGaAs channel is performed. Detailed microwave noise characteristics of composite channel InP-based HEMT are presented. An interesting result is that, compared to conventional single InGaAs Channel HEMTs, the minimum noise figure ($NF_{\min}$) of composite channel HEMTs is insensitive to drain voltage (V_d) resulting in a much lower $NF_{\min}$ at high V_d . Analysis of channel thermal noise provides an insight to understand the influence of the channel structural design on the microwave noise performance.

7.2 Experiments

The composite channel HEMT used is consisting of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel and undoped InP channel and doped InP and all the layers are lattice-matched to InP, as shown

in Table 7.1. For the referenced single InGaAs channel device, a 15 nm In_{0.53}Ga_{0.47}As channel was used. The InGaAs/InP HEMT devices were fabricated using the conventional photolithography and a wet mesa isolation technique. The ohmic contact was evaporated by Ni/Ge/Au and alloyed at 280°C under N₂ protection. Submicron gate-length fabrication was defined by e-beam lithography using a bi-layer photoresist PMMA/MMA. For gate recess, a selective etching solution, succinic acid: H₂O₂, was used. Device fabrication was completed with the evaporation and lift-off the Ti/Au gate metal. The gate length of the CC-HEMT and single InGaAs channel HEMT are around 0.5µm and 0.3µm, respectively.

On-wafer S-parameter and noise measurements were carried out on a Cascade probe station. Device S-parameters were measured using a HP8510B network analyzer with frequency up to 50 GHz. Measurements of noise characteristics were conducted by using an ATN NP5 noise and S-parameter measurement system in the frequency range of 2 to 20 GHz.

Table 7.1 Layer Structure for InP HEMT with an InGaAs/InP Composite Channel

Layer	Comment	Material	Thickness (Å)	Doping Level (/cm ³)
8	Cap	InGaAs	100	5.0E+18
7	Barrier	InAlAs	200	-
6	Upper doping	-		5.0E+12 /cm ² Planar
5	Upper Spacer	InAlAs	50	-
4	Channel	In _{0.53} Ga _{0.47} As	100	-
	Sub-channel	InP	50	-
	Sub-channel	InP	100	2.0E+18
3	Lower spacer	InAlAs	50	-
2	Lower doping	-		1.5E+12 /cm ² Planar
1	Buffer	InAlAs	2000	-
InP Substrate				

7.3 Results and discussion

Fig. 7.1 shows the typical I - V characteristics of the HEMTs with InGaAs/InP composite channel and InGaAs single channel. The drain currents for both devices are about 450mA/mm at $V_g=0.3$ V. Compared to the referenced single InGaAs channel device, the composite channel device shows a remarkable suppression of kink effect with low output conductance. As pointed by Enoki *et al.* [17], this could be attributed to the reduction of electron impact ionization in the channel region for the composite channel structure. It is generally believed that the kink mechanism in HEMT is linked to the impact ionization. Holes generated by impact ionization at the drain side of the gate accumulate at the source side in the channel or substrate. This decreases the potential barrier for electrons, thus causing the drain-current increase, or kink phenomena. While in a composite-channel HEMT, electrons are thought to travel mainly in the InP subchannel at the drain side of the gate. Because of the low impact ionization coefficients of InP, hole generation are suppressed. Even if some holes are generated, hole accumulation is minimized by the high recombination rate due to the subchannel doping. Therefore the kink effect is suppressed or minimized.

Fig. 7.1 Typical I - V characteristics of InP HEMTs with different channel schemes. (Solid line: InGaAs/InP composite channel; Dashed line: InGaAs channel)

Fig. 7.2 (a) shows the minimum noise figure ($NF_{\min}$) as a function of V_g for a composite channel device at 10 GHz. For a given V_d , the $NF_{\min}$ versus V_g curves show the typical “U-shape” behavior. This could be due to the bias dependence of channel noise source as well as decrease in g_m at low I_d (or V_g) measured at different V_d . It is seen that $NF_{\min}$ is insensitive to drain bias for V_d higher than 1 V. The V_g -dependence of $NF_{\min}$ at different V_d measured from a single InGaAs channel HEMT is shown in Fig. 7.2 (b) for comparison. The increase in V_d results in a drastic increase of the $NF_{\min}$ for a single channel HEMT, while the variation of $NF_{\min}$ in the same gate bias range for the InGaAs/InP composite channel HEMT is negligible.

Fig. 7.2 NF_{min} versus V_g for (a) InGaAs/InP composite channel (b) for single InGaAs channel HEMTs measured at 10 GHz.

The significantly different V_d -dependence of NF_{min} between the composite channel HEMT and the referenced single InGaAs channel device can be clearly illustrated in Fig. 7.3. It can be seen that, for $V_g = -0.4$ V, NF_{min} of composite channel HEMT shows a noticeable reduction in voltage range of from 0.5 to 1 V and then tends to maintain the

smaller $NF_{\min}$ with the increase in V_d until $V_d=3$ V. Similar trends are observed for $V_g=0$. The variation of $NF_{\min}$ for the composite channel HEMT is less than 0.1 dB when V_d is changed from 1 V to 3 V. However, the increase of V_d from 0.5 to 2.5 V for the single channel HEMT results in more than 3 dB increase in $NF_{\min}$. Similar behavior can be observed for $V_g=0$ as shown in Fig. 7.3 (b). Our data indicates that a composite channel device may provide a larger low noise window in terms of drain bias as compared to the single channel structure.

Fig. 7.3 Comparison of $NF_{\min}$ as a function V_d measured between composite and single channel HEMTs at (a) $V_g = -0.4$ V and (b) $V_g = 0$ V.

Figure 7.4 further shows the $NF_{\min}$ of (a) the composite channel HEMT and (b) single channel HEMT as a function of frequency for the different V_d at a fixed gate bias $V_g=0$ V. It is clearly observed, for both devices, the $NF_{\min}$ tends to increase if the frequency is increased. However, the $NF_{\min}$ for the composite channel HEMT still keeps a

weaker V_d -dependence than the single channel device in the studied frequency range.

Similar comparison at another fixed gate bias ($V_g = -0.6$ V) gives the same trend, as shown in Figure 7.4(c) and 4(d).

Fig. 7.4 NF_{min} of the composite channel (a,c) and the single channel (b,d) as a function of frequency for the various V_d at a fixed gate voltage $V_g = 0$ V (a,b) or $V_g = -0.6$ V (c,d).

The V_d -independent NF_{min} observed in composite channel HEMTs could be explained by the carrier transport in the channel region as follows. At the lower drain bias, the channel current is dominated by the electrons transporting in the InGaAs channel for both devices and thus the dominant channel thermal noise should arise from the InGaAs

channel region. For single InGaAs channel HEMT, increasing of V_d causes the increase in electron impact ionization and thereby channel noise which in-turn results in high $NF_{\min}$. However, for the HEMTs with a properly designed InGaAs/InP channel, with the increase in V_d , the carrier transport may eventually switch from InGaAs channel towards the InP subchannel. The suppression of electron impact ionization may result in a lower channel noise.

Based on a first order approximation, the $NF_{\min}$ of a submicron HEMT can be estimated using a simplified analytical expression having the basic form of [86,87,88]:

$$NF_{\min} = 1 + 2 \frac{\omega C_{gs}}{g_m} \sqrt{K_g g_m (R_s + R_g)} \quad (7.1)$$

where K_g is a fundamental noise coefficient which is related to the channel thermal noise and the induced gate noise. It is instructive to see that the reduction of the fundamental noise (e.g. channel noise) thus K_g would directly affect $NF_{\min}$. However, variation of other device electrical parameters such as g_m and C_{gs} due to the change of device bias may also cause the change of $NF_{\min}$. Therefore, to validate above explanation, a detailed noise modeling to extract the channel thermal noise has to be performed. The noise parameters of the InP-based HEMT are obtained by fitting an equivalent circuit model using a number of sets of measured S-parameter and measured noise parameter. The noise figure of a HEMT is similar to that of a MESFET. Generally, there are basically two principal types of noise for the intrinsic noise of HEMT: channel thermal noise and gate noise. Channel thermal noise arises from the vibration of conduction electrons and holes due to their finite temperature. The two internal current noise sources, the induced gate noise ($\overline{i_g}$) and the channel noise ($\overline{i_d}$), are considered for the noise model of the HEMTs.

The noise source parameters can be defined as follows: [86]

$$\overline{i_d^2} = 4 \cdot k \cdot T_0 \cdot \Delta f \cdot g_m \cdot P \quad (7.2)$$

$$\overline{i_g^2} = 4 \cdot k \cdot T_0 \cdot \Delta f \cdot \frac{\omega^2 \cdot C_{gs}^2}{g_m} \cdot R \quad (7.3)$$

$$C = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2} \cdot \overline{i_d^2}}} \quad (7.4)$$

where, P describes the channel noise due to carrier fluctuations in the channel, R the gate noise induced from the channel noise, and Δf the frequency bandwidth. The correlation coefficient C describes the dependence of the gate noise on the channel noise. To gain a better insight on the noise characteristics, the experimental results were modeled by using the approach given in [75].

The drain (channel) thermal noise $\overline{i_d^2}$ and gate noise $\overline{i_g^2}$ for the devices are extracted and shown in Fig. 7.5 and Fig. 7.6, respectively. For the composite channel device, the $\overline{i_d^2}$ as a function of V_g is indeed insensitive to V_d bias as shown in Fig. 7.5(a). However, a remarkable bell-shape $\overline{i_d^2}$ versus V_g relation is observed for the single channel HEMT as shown in Fig. 7.5(b). As discussed in detail in Chapter 6, this strongly evidences the importance on the contribution of carrier impact ionization to the thermal noise in the single InGaAs channel device. Notice that, for $V_d = 2.5$ V, the $\overline{i_d^2}$ of composite channel HEMT at $V_g = -0.4$ V is about ten times lower than the one in the referenced InGaAs channel HEMT suggesting a remarkable suppression of channel noise. The induced gate noise $\overline{i_g^2}$ is also extracted and plotted in Fig. 7.6. In general, $\overline{i_g^2}$ is about 1 to 2 orders lower than $\overline{i_d^2}$.

Fig. 7.5 Drain (channel) thermal noise $\overline{i_d^2}$ as a function of V_d for (a) composite channel and (b) single channel HEMT.

Fig. 7.6 Gate noise versus $\overline{i_g^2}$ as a function of V_d for (a) composite channel and (b) single channel HEMT.

Re-plotting the data in Fig. 7.7 to better illustrate the V_d -dependence of noise, we clearly see that, in the composite channel HEMT, channel thermal noise is indeed insensitive to V_d , while an increasing trend is shown in the single channel device. This is in good agreement with the $NF_{\min}$ data shown in Fig. 7.3. Therefore, we believe that the

observed different V_d -dependence of $NF_{\min}$ can be directly linked to the different carrier transport properties in the channel region due to different channel configurations.

Fig. 7.7 Channel thermal noise $\overline{i_d^2}$ and gate noise $\overline{i_g^2}$ versus V_d for (a) composite channel and (b) single channel HEMTs.

7.4. Summary

In summary, noise performance characterization of InGaAs/InP composite channel HEMTs reveals a different bias dependence of $NF_{\min}$ compared to conventional single InGaAs channel devices. The composite channel HEMT shows a lower $NF_{\min}$ at high V_d with a relatively weak V_d dependence. This could be explained under the framework of suppression channel thermal noise due to the electron transfer from InGaAs channel to InP sub-channel at high V_d . Our results suggest that it could be of great importance to further look into the impact of channel structural optimization on the noise characteristics for InP composite channel HEMTs.

Chapter 8 Conclusions and Recommendation for Further Work

8.1 Conclusions

In this work, InP-based HEMT structures including single channel HEMT, composite channel HEMT, and metamorphic HEMT were studied through structure characterization, device fabrication as well as RF measurements. The work investigates several important topics on the relationship of InP-based HEMTs' performances on the buffer structure, SiN passivation, and channel structure. The work concerns on InP-base HEMT thermal stability, potential degradation from SiN passivation, and the channel structure effect on noise figure. Better understanding was also reached about the role of metamorphic buffer layer, change of InAlAs surface states by SiN passivation, and origin of excess noise in the impact ionization regime. The most significant contributions of this work are summarized as below.

(1) Through a comparative study of the effect of RTA on lattice-matched and metamorphic InP/InGaAs HEMT structures, we observed that HEMT structures grown on a metamorphic buffer exhibit better thermal stability, which may partially ease the potential concerns about the thermal stability of metamorphic HEMTs. The experimental results also suggest possible dislocation-related gettering effect due to the presence of the dislocation network (gettering sink) in the metamorphic buffer located immediately beneath the device zone.

(2) The influence of SiN passivation on the electrical properties of InGaAs/InP composite channel HEMT structures has been studied. Different from the behavior on the single InGaAs channel structures, an enhancement in effective mobility μ_e with a

negligible change of sheet carrier density n_s after SiN deposition is clearly observed. The increase of μ_e in CC-HEMT structure could be a result of electron transfer from the InP subchannel into the InGaAs channel region due to the modification of surface potential. The experiment results also provide a strong evidence for modification of surface potential towards an unpinned surface, suggesting the presence of relatively low densities of interface states on InAlAs after SiN passivation.

(3) High frequency noise of InP-based HEMT in the impact ionization regime has been characterized. A fundamental understanding of the physical origin of the excess noise in the impact ionization regime was achieved in this work. It is revealed that different physical mechanisms are responsible for the excess channel noise at different frequency ranges. The excess noise at frequencies below 10 GHz is mainly due to the hole recombination in the channel. However, excess channel noise at higher frequencies could be dominated by the fluctuation of impact ionization which has a much smaller time constant and therefore a much higher cutoff frequency.

(4) A comparative study of the microwave noise performance is performed to check the impact of channel structure on channel thermal noise of InP-based HEMT. Results reveal that InGaAs/InP composite channel has a different bias dependence of $NF_{\min}$ compared to conventional single InGaAs channel devices. The composite channel HEMT shows a lower $NF_{\min}$ at high V_d with a relatively weak V_d dependence. This could be explained under the framework of suppression channel thermal noise due to the electron transfer from InGaAs channel to InP sub-channel at high V_d . Our results suggest that it could be of great importance to further look into the impact of channel structural optimization on the noise characteristics for InP composite channel HEMTs.

8.2 Recommendations for further work

The studies on InP-based HEMT in this work have provided interesting experimental findings and better fundamental understanding, based on which further in-depth investigation would be of great interest for both basic physics study and potential device optimization. Therefore, we suggest several potential directions as following:

(1) As far as the role the metamorphic buffer in a MHEMT is concerned, it would be useful to explore the microscopic mechanism of how the gettering effect occurs as well as its dependence on some important factors. For example, more experiments at different anneal times and anneal temperatures would be helpful to achieve more information to understand kinetics of the gettering effect, which could be used to identify the complete kinetics process as well as the possible chemical and crystallographic processes involved. Since the strain relaxation and defect configuration of metamorphic buffer is related to the buffer structure design and growth conditions, it may also be interesting to investigate how the gettering effect depends on the dislocation network formed and the distance from device to buffer. It is also important to check its comprehensive impact on device performance and reliability. Given a positive effect, optimization of metamorphic buffer may allow potential adjust/control on the dislocation network to exploit the gettering effect.

(2) This work has confirmed that a relatively low densities of interface states on InAlAs barrier and the modification ability of surface potential towards an unpinned surface by SiN passivation. Therefore, it is worth performing more studies on mechanism analysis and process optimization of SiN passivation to improve device performance of InP-based HEMT. For example, it has been reported SiN produced by different deposition

techniques (catalytic CVD and plasma-enhanced CVD) has different effect on electronic property of channel.

(3) More qualitative theoretical works may be needed to explore the change of energy band and electron distribution for a composite channel HEMT, working at different operation conditions. Since composite channel HEMT has showed suppression of channel noise, it would be interesting to explore the possibility to optimize channel design, which may potentially achieve devices with better noise performance with lower $NF_{\min}$.

(4) PL characterization is a useful non-destructive tool to detect the structural and electronic properties of HEMT structures. More quantitative studies on the correlations between structure and PL results would be interesting. It is also meaningful to explore the mechanism of PL observations, such as that MHEMT tends to give a smaller splitting between the $e_2 - \hbar\hbar_1$ and $e_1 - \hbar\hbar_1$ emissions than LHEMT with same structure.

(5) There is a profound difference between 2D noise and 3D noise in III-V HEMT devices. In a composite channel HEMT, 2D noise may dominate in InGaAs channel, while 3D noise may dominate in InP subchannel. Therefore, it would be an interesting topic to investigate the distinction and hence observe the redistribution of carriers between the two parts of the channel for different voltage conditions.

List of Publications

1. Yuwei Liu, Hong Wang, "Experimental evidence for dislocation-related gettering in metamorphic InP/InGaAs high electron mobility transistor (HEMT) structures on GaAs substrate", **J. Appl. Phys.**, vol. 100, no. 3, p 34505-1-5, Aug. 2006.
2. Yuwei Liu, Hong Wang, "Influence of Silicon Nitride Passivation on Transport Properties in InAlAs/InGaAs/InP Composite Channel High Electron Mobility Transistor Structures", **Journal of Vacuum Science & Technology B**, vol. 24, no. 4, p 1711-15, Jul. 2006.
3. Hong Wang, Yuwei Liu, Rong Zeng, and Chee Leong Tan, "Understanding of the excess channel noise in InAlAs/InGaAs/InP high electron mobility transistors in impact ionization regime", **Appl. Phys. Lett.**, vol. 90, no. 10, p 103503-1-3, Mar. 2007.
4. Yuwei Liu, Hong Wang and K. Radhakrishnan, "Increase in electron mobility of InGaAs/InP composite channel high electron mobility transistor structure due to SiN passivation", **Thin Solid Films**, vol. 515, no. 10, p 4387-4389, Mar. 2007.
5. Yuwei Liu, Hong Wang, and Rong Zeng, "Microwave noise in InP/InGaAs composite channel high electron mobility transistors (HEMTs)" 2005 Asia-Pacific Microwave Conference, p 3-6, 2006.
6. Yuwei Liu, Hong Wang, "Influence of Silicon Nitride Passivation on InGaAs/InP Composite Channel High Electron Mobility Transistor Structures", 2005 International Conference on Indium Phosphate and Related Materials, p 520-2, 2005.

7. Yuwei Liu, Hong Wang, and Rong Zeng, "Microwave Noise Characteristics of InP-based High Electron Mobility Transistors with InGaAs channel and InGaAs/InP Composite Channel: A Comparative Study", 2005 International Conference on Indium Phosphate and Related Materials, p 437-9, 2005.
8. Yuwei Liu, Hong Wang, Yongzhong Xiong, "Photoluminescence and Electrical Properties of InGaAs/InP Composite Channel Metamorphic HEMT Structures Subjected to Rapid Thermal Annealing", 2004 International Conference on Indium Phosphate and Related Materials, p 606-8, 2004.

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