Low-voltage low-power CMOS flip-flops

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Low-Voltage Low-Power CMOS Flip-Flops

Phyu Myint Wai

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2009

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of my original research and has not been submitted for a higher degree to any other University or Institution.

Date

Phyu Myint Wai

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Abstract

As the clock frequency scales, the pipeline depth increases and the number of logic gates per stage decreases. The System-on-Chip (SoC) designs will therefore integrate tens of millions of transistors on one chip. But the packaging and cooling designs have only a limited ability to remove the excess heat produced by the systems. All these factors have resulted in power consumption to be considered as one of the main problems in achieving high performance designs. The energy consumption of the clocking sub-system that is composed of the clock distribution networks (buffers and wires) and clock storage elements (flip-flops and latches) is about 30% to 60% of the total system energy. For this clock system power, 90% is consumed by the flip-flops themselves and the last branches of the clock distribution network that drives the flip-flop directly. As clock frequency increases, the latency of the flip-flop will play an even greater role in the overall cycle time. As a result, it is essential to continue venturing into higher-end approaches and realizing more refined solutions to achieve low-voltage/low-power design while sustaining high-speed performance and small-area consumption. In this thesis, several innovative flip-flop designs for low-voltage low-power environments used are described.

The new designs of low-power high-performance output feedback single and double edge-triggered flip-flops presented which are mainly derived from its existing counterparts by successfully addressing the weakness of their counterpart circuits. Extensive simulation works using the 1.8 V/0.18 μm CMOS process from Chartered Semiconductor Manufacturing Pte. Ltd. (CHRT) have verified that the new flip-flop architectures reported provided significant improvement in terms of delay and power consumption while promising a small-area feature. These are achieved mainly by the legitimate and appropriate usage of logic structure and circuit techniques.

An area-efficient explicit-pulsed single/double edge-triggered flip-flop, which is based on the recently reported design is proposed to meet the increasing requirement for

low-power feature without compromising the speed performance. Extensive circuit simulations using the 0.18 μm CMOS technology from CHRT verify that the proposed design acts as a complement to the its contemporary flip-flop circuitry for different input switching activities.

In addition, a low-power single edge-triggered flip-flop based on static latch and dynamic pulse generator is designed. Simulation results showed that the new circuit offers substantial improvement over the conventional circuits with respect to speed and power-delay product, regardless of input switching activity.

Another proposed flip-flop circuit, namely the pulsed pass-gate level-converting flip-flop (PPG-LCFF) which is based on clustered voltage scaling scheme is introduced. Similar to the previous designs, this circuit is designed for low-voltage low-power applications. Extensive simulation results based on a 1.8 V/0.18 μm CMOS technology from CHRT verifies that the new PPG-LCFF promises a power-area-efficient advantage and note-worthy power-delay product superiority over the conventional and recently reported level converting flip-flops. Last but not least, sensitivity analyses of power and delay performance of flip-flops over process, voltage and temperature variations is discussed. The sensitivity analyses serve to identify the key performance parameters of flip-flop circuits that tend to be easily affected when the device or process parameters deviate from their nominal values. This is particularly important for scaled technologies and high-performance CMOS where the circuit speed is vulnerable to adverse effects caused by the reduced feature size that are imposed by increased tolerances. From the sensitivity analysis of flip-flop circuits, the designer is able to identify a suitable circuit that will present the different tradeoff choices among the performances, i.e., speed, power dissipation and robustness.

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List of Abbreviations

ASIC	Application-Specific Integrated Circuit
BAL	Basic and Logic
CCFF	Conditional Capture Flip-Flop
CDFF	Conditional Discharge Flip-Flop
CHRT	Chartered Semiconductor Manufacturing Pte. Ltd.
CMOS	Complementary Metal Oxide Semiconductor
C ² MOS	Complementary Clock Metal Oxide Semiconductor
CSSA	Clock Level Shifted Sense-Amplifier
CVS	Clustered Voltage Scaling
DSM	Deep-Submicronmeter
DETF	Double Edge-Triggered Flip-Flop
DFF	D-type Flip-Flop
DSP	Digital Signal Processing
DL	Data-transition Look-ahead
DB-MSFF	Double-Gated Clock Master-Slave Flip-Flop
DPC	Dual Pulse Clocked
DE-TPGL	Double Edge Transmission Gate Pulsed Latch
DET-FBFF	Double Edge-Triggered Output Feedback Flip-Flop
DRC	Design Rule Check
ep-FF	Explicit-Pulsed Flip-Flop
FB	Feedback
FSM	Finite State Machine
HLFF	Hybrid Latch Flip-Flop
ip-FF	Implicit-Pulsed Flip-Flop
IC	Integrated Circuit
LCFF	Level Converting Flip-Flop
LC	Level Converter
LVS	Layout Versus Schematic
MSHL	Master-Slave Half-Latch
MUX	Multiplexor
mC ² MOS	modified Clocked CMOS Flip-Flop
nMOS	n-channel Metal Oxide Semiconductor
Ni-MH	Nickel-Metal Hybrid
NDKFF	NAND-type Keeper Flip-Flop
NLO	Negative Latch Output
PDA	Personal Digital Assistant
PDP	Power-Delay Product
PHL	Pulsed Half-Latch
pMOS	p-channel Metal Oxide Semiconductor
PVT	Process, Supply and Temperature
PN	Precharged n-stage
PLO	Positive Latch Output
PPG	Pulsed Pass-Gate
PPG-LCFF	Pass-Gate Level-Converting Flip-Flop
RCSFF	Reduced Clock Swing Flip-Flop
SoC	System-on-Chip
SETFF	Single Edge-Triggered Flip-Flop
SDF	Semidynamic Flip-Flop
SEPFF	Static Explicit-Pulsed Flip-Flop
SPFF	Self-Precharging Flip-Flop

SET-FBFF	Single Edge-Triggered Output Feedback Flip-Flop
SN	Non-Precharged n-stage
STC-EPFF	Single-Transistor-Clocked Explicit-Pulsed Flip-Flop
SO	Split-Output
TGFF	Transmission Gate-based Flip-Flop
TSPC	True Single Phase Clocked
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration
XNOR	Exclusive NOR
XOR	Exclusive OR

Chapter 1

Introduction

1.1 Motivation

The Complementary Metal-Oxide Semiconductor (CMOS) device technology is the process of choice for high integration and performance at low-power. It is believed that CMOS will stay the mainstream process for many years to come. In recent years, aggressive scaling of CMOS to sub-micron levels has set the pace toward Ultra Large Scale Integration (ULSI) era where it is now possible to integrate a complete system on a single chip (or SoC). In addition to its high-performance and high integration features, CMOS is an excellent candidate for ultra low-power and low-cost applications [1].

Significant progress has been made towards producing devices with ever-decreasing miniaturized scale. It is anticipated that nanometer-scale devices will continue this trend. Figure 1.1 depicts the down-scaling of CMOS devices over 14 generations of CMOS [1]. Note that because of the etching process used to fabricate the transistor gates, the physical gate length is less than the drawn feature size. Below 200 nm this causes “super-scaling” of the physical gate length.

Figure 1.1 Evolution of CMOS technology [1].

The clock frequency of Very Large Scale Integrated (VLSI) Systems has been increasing continuously with the technology scaling while the System-On-Chip (SoC) designs continue to integrate tens of million of transistors on one chip. Unfortunately, the packaging and cooling designs have only a limited ability to remove the excess heat produced by the system (Figure 1.2) [2]. One of the most crucial factors that fuel the needs for low-power VLSI chips is the increased market demand for portable consumer electronics that are mainly powered by batteries. The craving for smaller, lighter, and more durable electronic products indirectly translates to low-power requirements. Laptop computers, Personal Digital Assistants (PDA's), cellular phones, pagers and wearable medical devices such as pacemakers and hearing aids have enjoyed considerable success among consumers, and the market for these and other portable devices is only projected to increase in the future [3].

Figure 1.2 Power and frequency versus technology generation [2].

For these applications, power consumption has become a critical design concern and has perhaps superseded speed and area, as the overriding implementation constraint [4] due to the contingent requirements on battery dimension and weight. To extend the duration and mobility of the portable battery-operated system, the battery life must be improved. Traditionally, Nickel-Cadmium batteries had been used in most applications that require rechargeable batteries. Nickel-Metal Hybrid (Ni-MH) and Lithium-Ion batteries have recently become popular batteries for portable applications for their

improved energy density and reduced toxic heavy metal [5]. The energy capacity of batteries has been improving over the last two decades, but at a very slow pace [6]. Moreover, the energy stored in a battery cannot be extracted to the full extent due to the strong dependence of the energy capacity on the mean value of the discharge current as well as the portion of energy that is wasted by the DC/DC converter [5]. Figure 1.3 illustrates a widening gap between the trends in the processor power consumption and improvement in battery capacity [7]. With a projection of this slow pace and limitation of battery technology, absence of low-power design techniques, will therefore hinder current and future portable devices advancement. The devices will suffer from either very short battery life or unreasonably heavy battery packs. As a result, the portable electronics market has provided a very strong motivation for low-power design.

Figure 1.3 A widening gap due to rapidly increasing power requirements and slowly improving battery technology [7].

One of the dominant sources of power consumption in digital VLSI systems is the switching component dissipated in circuit nodes with high switching probabilities. Nodes of this kind are mainly the clock nodes. Hence, reduction of the power consumed by the clocking subsystem that are composed of flip-flops and a clock distribution network can lead to a significant reduction in the overall system power consumption [8]. The power breakdown of a microprocessor (Figure 1.4) shows that the clocking system and switching logic are two main contributors of power consumption [9].

Figure 1.4 Power distribution of Itanium 2 processor [9].

In a synchronous digital system, the clock signal is used to define a time reference for the movement of data within that system [10]. Therefore, the logic operation must complete before the tick of the clock, since their final values are being captured by that clock event [11]. The synchronous system includes combinational logic and clock storage elements (i.e., flip-flops and latches), where they collectively constitute a finite state machine (FSM) [11]. D-type flip-flops are one of the major functions in FSM, which in turn form a critical part of the control logic. In order to boost processor clock frequency, modern processors typically adopt superpipelined execution [12], which also makes heavy use of D-type flip-flops (DFFs). In particular, DFF is one of the major components in FSM as well as it is widely used as a delay element in digital signal processing [13].

Based on the cell library design (neglecting off-chip power), power consumed by the clock and its components is of the highest. They also contribute the most significant portion of the overall power consumed (40% in static logic to over 60% in dynamic logic) [14]. Moreover, the power dissipation of the clocking network is 20 - 45% of the total power dissipation, where 90% of which is consumed by the flip-flops themselves

and the last branches of the clock distribution network [15, 16]. They not only occupy a large portion of the silicon area, but also consume a substantial amount of power.

As the clock speed is noted to increase rapidly; doubling every three years [17], the overheads due to the timing elements such as latches and flip-flops have formed a larger fraction of the cycle time. In addition, power requirement is increasingly important since the power consumption increases linearly with clock frequency while the power budget of high-performance portable digital systems is severely limited. Unless they are carefully designed and characterized, their performance can inflict a critical effect on the cycle time. Moreover, the key signal in all synchronous systems is the apparent clock and clock signal is normally heavily loaded by all the latches and flip-flops in the chip, and by the clock distribution network that covers the whole chip. Lastly, although the activity ratio of the clock signal is unity, the interconnect length of the clock trees has been increasing radically [18]. The design trend is thus to increase the pipeline stages for high throughput, and this has prompted the increased in the number of latches and flip-flops used in a chip [19]. In power constraint systems, the power efficiency of latches and flip-flops is therefore pivotal [20]. As a result, reducing the power consumed by flip-flops will have a direct impact on the total power consumed in microprocessors, any synchronous digital systems and DSP chips.

The above analysis suggests that the main area of focus is to address the power dissipation of flip-flops and latches. Researchers have been addressing the power dissipation problem at different levels starting from the elementary device/process level, physical/layout level, circuit level, logic level, architecture level, algorithm level, and all the way up to the system level [21, 22, 23] low-power behavioral synthesis to optimizing the threshold voltage at process level. In this PhD thesis, circuit level techniques on designing “low-voltage low-power CMOS flip-flops” are focused.

1.2 Objectives

Due to increasing clock frequency, large number of storage device on die, and the high-performance requirements, the clocking subsystem has become one of the largest, if not the largest, power consuming sections of the VLSI system. The reduction of power consumed by flip-flops will therefore have a direct impact on the total power consumed in the microprocessor, any synchronous digital systems or the DSP chip. In addition, from a timing perspective, flip-flop latency consumes a large portion of the cycle time as the operating frequency increases. Thus, the clocking subsystem must be designed to meet performance requirements while minimizing its power consumption. In other words, the goal of every VLSI design is to trade the performance for power. The amount of tradeoff shall depend on the application. The research presented in this thesis therefore focuses on the circuit techniques, with an aim to achieve energy or performance improvements of the flip-flops.

The objective of this project is to address the above-mentioned challenges. The fundamental goals are to stimulate new and innovative designs to develop low-voltage and low-power novel flip-flop circuits by integrating the CMOS technology in the deep submicron era, while sustaining a high-speed performance and small silicon area consumption. The scope of this project also covers a profound analysis on the state-of-the-art flip-flops used for high-speed and low-power applications. In addition, the proposed flip-flops must be able to operate at low voltage regime.

1.3 Research Contributions

The specific contributions of this research are outlined below:

- A new single edge-triggered output-feedback flip-flop (SET-FBFF) that achieves energy savings by reducing internal switching activities is proposed. In order to exploit the power savings due to halved clock frequency, an explicit-pulsed double edge-triggered flip-flop (DETFF) based on SET-FBFF is also presented, to illustrate the designs' ability in deriving performances that are the same as that of the SET-FBFF with significantly less clocked related power consumption in the flip-flop.
- A single/double edge triggered explicit pulsed flip-flop with local feedback (SET-/DET-SEPFB) is introduced. This flip-flop offers low-power and small area feature as compared to recently reported contemporary flip-flop circuits.
- A new single edge-triggered flip-flop (SETFF) that is derived from a novel static latch (SN2-latch), with innovative dynamic pulse generator for low-power high-speed applications is presented. Performance evaluation showed that the new circuit (SN2FF) offers substantial improvement over the contemporary circuits in terms of power-delay product (PDP) and silicon area.
- A novel DETFF with dynamic true-single-phase-clocked (TSPC) split-output (SO) is proposed. It employed the basic and logic combining section (BAL), merging the latches' outputs to realise the DETFF configuration. The main advantage of the proposed design (SO-BAL-DETFF) is the reduced loading of the clock signal and the lesser clock power consumption when compared to conventional design for all cases of input data activities. The reduced clock loading is achieved by having only two clocked transistors. The reduction in clock power of the proposed DETFF allows for a substantial power saving in the clock distribution network.
- A novel level-converting flip-flop that incorporates pass gate level converter and true single phase clock (TSPC) based dynamic pulse generator is presented. The proposed LCFF, namely PPG-LCFF, circuit is able to outperform power-delay

product (PDP) value with small area feature as compared to other reported LCFFs.

- In order to access the circuits' robustness, the power and delay sensitivity analyses on the process, supply voltage and temperature (PVT) variations of proposed flip-flop circuits and other selected conventional and recently reported designs for comparison are presented. From the sensitivity analysis, the designer is able to identify a suitable circuit that will present different tradeoff choices among the performances, i.e. speed, power dissipation and robustness. On top of that, the designer is able to identify the parameter that has the greatest influence on the circuits' performance.

1.4 Organization of the Thesis

The remainder of this thesis is organized as follows: Chapter 2 presents the general types and performance characteristics of flip-flops, including the timing characterization and power consumption metrics. Following that, the design optimization techniques as well as the approaches to minimizing energy consumption in flip-flops are discussed.

Chapter 3 provides a comprehensive literature review on the state-of-the-art low-power high-performance storage elements. The limitations of their performances are also discussed. The chapter is divided into two main sections. The first deals with single edge-triggered designs and the second covers the double edge-triggered flip-flops.

Chapter 4 introduces the proposed single edge-triggered flip-flops. These flip-flop circuits have been extensively simulated and analytically compared with their respective type of conventional and existing flip-flop designs.

In Chapter 5, the new double edge-triggered flip-flop designs and their performance comparison with existing designs are presented.

The sensitivity of the flip-flop circuit's delay and power dissipation due to process, supply voltage and temperature variations are analysed and discussed in Chapter 6.

Finally, the conclusion of this thesis is given in Chapter 7. Recommendation for future work is also presented in this chapter.

Chapter 2

Flip-Flops and Performance Metrics

This chapter is divided into four main sections and the first section describes the general types and characteristics of flip-flops. Timing and power dissipation metrics of flip-flops as well as the systematic transistor sizing technique to achieve the optimal power-delay tradeoff are then presented. In the last section of this chapter, the approaches to minimize the dynamic or switching power consumption of flip-flops are discussed.

2.1 General Types and Characteristics of Flip-Flops

Timing is key consideration in system and sequential circuit design. The reason for this is that all realizable circuits have inherent delay. This means that the actual time of arrival for input signals may not be the same as the expected time in ideal circuits, whereby the outputs that instantaneously change with the input. On top of that, the clocking subsystem is in fact subjected to abnormalities such as clock skew and clock jitter [24], [25] and these lead to timing issues. To combat these complex design issues, careful considerations must be given to the design of clocked storage elements or the sequential circuits [26]. As mentioned in chapter 1, the clocked storage elements are commonly used for data synchronization and data storage in Finite State Machine (FSM), as well as in pipelines (see Figure 2.1) and other DSP applications. Hence, information of timings to ensure optimum circuit performance is important.

Figure 2.1 Finite State Machines (FSM) and pipelined system in VLSI [11].

2.1.1 Latch versus Flip-Flop

A latch is a level-sensitive element with the following functional behaviors [27] [28]. When the control signal (clock) is at an active level, the latch is transparent. That is to say, the output follows any transition at the input. When the clock is at the inactive level, the latch is opaque. It will hold the output stage. Depending on the values of the active and inactive level of the clock signal, a latch can be of a high-level transparent (when active level is logical high) type or low-level transparent (when active level is logical low) type.

A flip-flop is an edge-sensitive element with the following behavior: the output captures the value of the input after the low-to-high transition of the clock or after the high-to-low transition of the clock, otherwise the flip-flop is non-transparent, i.e., it holds the captured value at the output. The transition of the clock that causes a change at the output is referred to as the capturing edge of the clock. Depending on which clock edge is capturing, the flip-flop can be rising edge-triggered or falling edge-triggered. Figure 2.2

shows the symbol representations and operational differences between a latch and a flip-flop. Many VLSI designs today are largely composed of flip-flops as opposed to latches because flip-flops allow for easier timing analysis and verification than latches due to their inherent shorter sampling time. On the other hand, this gain is without its disadvantage. Flip-flops are much more complex circuits and thus consume more energy than latches for the larger area. Nonetheless, the disadvantages are outweighed by the excellent timing properties they possess. This work is therefore concentrated on the design of flip-flops rather than latches.

Figure 2.2 Symbol and timing properties of: (a) latch and (b) flip-flop.

2.1.2 Types of Flip-Flops

Flip-flops can be classified based on the number of edges they utilize. Single edge-triggered flip-flop (SETFF) captures data on either the rising or falling clock edge. An alternative clocking strategy relies on the use of flip-flop circuits capable of capturing data on both clock edges (rising and falling edge). Such flip-flops are referred to as the double edge-triggered flip-flop (DETFF). The timing diagram illustrating the difference in operation of a SETFF and a DETFF is depicted in Figure 2.3 and it can be seen that the DETFF can achieve same data throughput with half of the clock frequency as compared to the SETFF [29].

Figure 2.3 Timing diagram illustrating the difference in operation of: (a) a SETFF and (b) a DETFF.

2.1.2.1 Single Edge-Triggered Flip-Flop (SETFF)

There are two main flip-flop styles present in today’s digital memory circuits – the master-slave latch pair and pulse-triggered latch. The master-slave latch is a particular arrangement of transparent latches in which two latches are connected in series and clocked with two independent clock phases. In this way, a master-slave latch pair behaves as an edge-triggered storage element (i.e., flip-flop). If the master latch is transparent on the low level of the clock, and the slave latch is transparent on the high level of the clock, the master-slave latch pair will be of “rising edge-triggered”, otherwise it is “falling edge-triggered”. These edge triggering mechanism are illustrated in Figure 2.4.

Figure 2.4 Master-slave latch pair and its timing diagram.

Pulsed-triggered latch is a latch configuration in which a short pulse, produced after either the rising or falling edge of the clock is used as a clock input to the latch. In this arrangement, the latch is only transparent for a short period of time after the active clock edge and is opaque otherwise, regardless of the timing waveform of the clock. In other words, the latch behaves as an edge-triggered flip-flop (see Figure 2.5).

Figure 2.5 Pulsed-triggered latch and its timing diagram.

2.1.2.2 Double Edge-Triggered Flip-Flop (DETFF)

As discussed, the double edge-triggered flip-flop (DETFF) captures the value of the input after both the rising and falling clock transitions. Otherwise, DETFF is non-transparent, i.e. it holds the captured value at the output. Thus, the double edge clocking strategy provides a one-time solution to the frequency scaling by retaining the data throughput of single edge clocking at half the clock frequency. However, in order to fully exploit the power savings in the clock distribution network, this approach must be comparable to those of SETFFs. Furthermore, the use of both clock edges to synchronize the operation causes timing to be sensitive to the clock duty cycle and increases clock uncertainties that can be generated by the clock distribution system.

A DETFF can be classified as:

- Pulsed latch, consisting of a clock pulse generator and a transparent latch, as shown in Figure 2.6 (b). The clock pulse generator creates a short pulse after both clock edges, which is then used as the clock input to the transparent latch.
- Latch-MUX (multiplexor) structure, that is made up of two latches that are connected in parallel and is transparent on the opposite levels of the clock. The circuit diagram is presented in Figure 2.6 (c). This multiplexor can select the output of the non-transparent latch at any time.
- Flip-Flop, which consists of the same building blocks as SETFFs (see Figure 2.6 (d)). It can be constructed from a positive edge-triggered flip-flop in parallel with a negative edge-triggered flip-flop. Since one of the two flip-flops is tristated in each clock phase, the results of the two flip-flops can be combined directly.

Figure 2.6 Double edge-triggered flip-flop techniques: (a) Symbol, (b) Pulsed latch, (c) Latch-MUX, and (d) flip-flop.

2.2 Timing Characteristics of Flip-Flops

In order to be able to quantitatively express the performance of a flip-flop, it is essential to analyze its timing behavior and to measure its power consumption. In this sub-section, prior to discussing the timing analysis of a flip-flop, the terms used to describe signal transitions and delay transitions between transitions (Figure 2.7) will be discussed. The terms associated with a single transition are measured when the signal reached the critical points 10%, 50% and 90% of its final value. The relative timing (delay, t_D) between two transitions is measured from the 50% point of one transition to the 50% point of the other transition [30] [31].

As an illustration, the rise time of a signal A, $t_{\text{rise,A}}$ is the time from the start (10%) to the end (90%) of a rising transition. The fall time of the signal A, $t_{\text{fall,A}}$ is the time from the start (90%) to the end (10%) of a falling transition. The pulse width of the signal A, $t_{\text{PW,A}}$ is the time from one transition on A to the next transition on A. The pulse width often refers to the duration where the clock pulse is at its high value.

Figure 2.7 Timing fundamentals: rise time, fall time, pulse width and delay.

The data and clock inputs of a flip-flop have to satisfy basic timing constraints such as the setup and hold times to ensure correct operation of the flip-flop. Setup and hold times define the time intervals during which an input datum has to be stable to ensure correct flip-flop operation. Detailed definitions of the setup and hold times are presented in the following two sub-sections.

2.2.1 Setup Time

The setup time is frequently defined as the timing interval before the latching clock edge whereby the data is not allowed to change for correct operation of a flip-flop [30] [31] [32]. This metric needs to be more precisely quantified because the setup time is characterized by an increase in the clock-to-output delay of a flip-flop as the data gets closer to the clock as shown in Figure 2.8 (a). Frequently, Application Specific Integrated Circuits (ASIC) standard cell libraries define the setup time as a specified increment in the clock-to-output delay. The assumption made here is that an increase in the clock-to-output delay by 10% from its nominal value can be tolerated. Therefore, setup time is the minimum data-to-clock offset that causes the clock-to-output delay to be 10% higher than its nominal value.

- Setup of logic “1” is the setup time measured when data undergoes a 0-1 transition.
- Setup of logic “0” is the setup time measured when data undergoes a 1-0 transition.

Setup time can be both positive (typical in master-slave latch pairs) and negative (typical in pulse-triggered latches) depending on the circuit topology, the supply voltage, and the simulation setup. In general, setup times of logic “1” and logic “0” are different. However, there are few cases when they are equal, for example, in fully balanced and in fully differential flip-flops [33].

2.2.2 Hold Time

The hold time is defined as the minimum allowed data arrival time after the latching clock edge in order to correctly capture the previous value. As in the case of setup time, the definition of the hold time is also based on the tolerance to an increase in the clock-to-output delay [30] [31] [32]. Hold time is therefore the minimum time interval during which a new datum has to retain its value after the active clock edge so that clock-to-output delay is 10% higher than its nominal value.

- Hold time of logic “1” is the hold time measured when data undergoes a 0-1 transition.
- Hold time of logic “0” is the hold time measured when data undergoes a 1-0 transition.

If the data changes too quickly, it can result in circuit malfunction, as illustrated in Figure 2.8 (b). Hold time can be negative (master-slave latch pairs) or positive (pulse-triggered latches). Like the setup time, hold time is also dependent on the circuit topology, the supply voltage and the simulation setup.

Figure 2.8 Timing characteristics of flip-flop: (a) setup, and (b) hold time.

2.2.3 Clock-to-Output Delay

The clock-to-output delay (t_{CQ}) is the delay time measured between the 50% mark of the active clock edge to the 50% mark of the output. That is, $t_{CQ,LH}$ if output undergoes a 0-1 transition or $t_{CQ,HL}$ if output undergoes a 1-0 transition. t_{CQ} is thus the maximum of the two delays ($t_{CQ,HL}$ and $t_{CQ,LH}$) [34]. Besides the data-to-clock offset of Figure 2.8 (a), it also depends on the clock slope, the process, the supply voltage, and the output load.

Ideally, it is desirable to have the delays through a flip-flop experienced by either the rising or falling input transition, to be similar. However, in general the delays cannot be identical since the two cases will experience a variety of rising and falling delays [35].

2.2.4 Data-to-Output Delay

The data-to-output delay (t_{DQ}) is the sum of clock-to-output delay (t_{CQ}) and the setup time. As discussed earlier, the setup time can be obtained by sweeping the input data (i.e., from 1-0 and 0-1) with reference to the active clock until a 10% increase in the clock-to-output delay (t_{CQ}) is observed.

The double edge-triggered flip-flops (DETFFs) apply all parameters defined for the SETFFs to the both clock edges [36] [37]. It is a custom practice that the worse of the parameters for the two edges is used as the only timing parameter.

2.3 Power Consumption Metrics & Power Delay Tradeoff

2.3.1 Power Consumption of CMOS Digital Circuits

This section discusses the power consumption of CMOS digital circuits briefly prior to flip-flop power consumption metric. There are four sources of power dissipation in digital CMOS circuits: switching (or dynamic) power, short-circuit power, leakage power, and static power [38]. These are summarized in the following Equation:

$$\begin{aligned} P_{avg} &= P_{dynamic} + P_{short-circuit} + P_{leakage} + P_{static} \\ &= \alpha \cdot C_L \cdot V_{DD}^2 \cdot f + I_{sc} \cdot V_{DD} + I_{leak} \cdot V_{DD} + I_{static} \cdot V_{DD} \end{aligned} \quad (2.1)$$

where α is the switching activity, f is the frequency, C_L is the load capacitance, V_{DD} is the supply voltage, I_{sc} is the short circuit current, I_{leak} is the leakage current, and I_{static} is the static current. The switching power $P_{dynamic}$ depend on the activity factor, α , or the average number of transitions for a circuit node per clock cycle, the load capacitance C_L , and the power supply voltage V_{DD} . The short-circuit power is controlled by the current that flows between V_{DD} and ground, I_{sc} . This current flows in static CMOS logic when both the P pull-up and N pull-down networks are on simultaneously during an output transition. I_{leak} , the main component of the leakage power, is the current due to leakage through reverse-biased PN junctions and subthreshold conduction of MOSFETs. With process scaling, this leakage has become increasingly significant when comes to the total power consumption.

Finally, the static power is due to the current sources engaged in the circuit, such as the biasing networks used in linear amplifiers, whose current sums to I_{static} . In a fully digital design with fast transients, the switching power $P_{dynamic}$ dominates in Equation 2.1. Consequently, low-power digital design focuses on reducing α , C_L , V_{DD} , and f . These

parameters can be reduced through algorithmic, architectural, and circuit techniques, and all of which have received a great deal of attention in recent years [39].

2.3.2 Power Consumption Measurement of Flip-Flops

To provide a real insight to the amount of power consumed in and around the flip-flop due to their presence, three main components of the power dissipation for a flip-flop are considered and is illustrated in Figure 2.9 [34].

- Local data power, P_{DATA} , which is determined from the current and voltage consumed by inverter INV_D during circuit operation (see Figure 2.9). INV_D is the data inverter that provides the input data to the flip-flop.
- Local clock power, P_{CLK} which again is determined from the current and voltage consumed by inverter INV_D during circuit operation. The clock drives INV_{CLK} is in turns is fed into the input of the flip-flop.
- Internal power consumption, P_{INT} , of the circuit under test, which is the intrinsic power dissipated during switching of the internal nodes within the flip-flop.

The internal power consumption is due to the switching activity of the internal nodes, due to the switching of both the clock and data input, and the leakage current as shown in Equation 2.2. The total average power consumption, P_{TOTAL} , is the sum of the three components shown in Equation 2.3.

$$P_{INT} = P_0 + C_{INT,CLK} \cdot V_{DD}^2 \cdot f_{CLK} + C_{INT,DATA} \cdot V_{DD}^2 \cdot f_{DATA} \quad (2.2)$$

$$P_{TOTAL} = P_{INT} + P_{DATA} + P_{CLK} \quad (2.3)$$

In Equation 2.2, P_0 is the leakage power consumption, present even if none of the inputs or internal nodes are switching. Parameters $C_{INT,CLK}$ and $C_{INT,DATA}$ are the equivalent internal capacitances for clock and input data switching, respectively. As the activity changes, different types of flip-flops behave differently. The switching activity of the internal nodes of the master-slave latches and double edge-triggered latch-MUX's

depends directly on the data input activity. Thus, these structures consume very little power when data is quiet, and regardless of the clock switching. In principle, the switching activity that is of DETFF style is constructed by two SETFFs in parallel is largely dependent on the clock rather than data due to the precharge-evaluate structure that is usually used. However, this architecture can be designed to reduce internal switching when the input data switching is low. The internal switching of the pulsed-latch is a result of both data switching and clock switching, due to the generation of the clock pulse. Thus, the parameter $C_{INT,CLK}$ is typically smaller and $C_{INT,DATA}$ is larger for the master-slave latches and latch-MUX's than that of the complete flip-flops and pulse-latches.

Power consumptions are measured using different input data activities: '0101' represents maximum switching activity ($\alpha = 1$), '0011' stands for 0.5 switching activity ($\alpha = 0.5$), and both '0000' and '1111' represent zero switching activity ($\alpha = 0$) [34].

Figurer 2.9 Power consumption measurement.

2.3.3 Power Delay Product (PDP)

The power consumption of a flip-flop can be approximated with the switching component which is proportional to $C_L \cdot V_{DD}^2 \cdot f$ as in Equation (2.1). The load capacitance C_L in Equation (2.1) consists of intrinsic components (parasitic drain capacitances which depend on transistor dimensions) and extrinsic components (interconnect/wiring capacitance and fan-out capacitances which are usually independent of transistor dimensions of the circuit under consideration). Therefore, one can reduce the power consumed by a flip-flop by reducing the supply voltage, the operating frequency or decreasing the switched capacitance (dependent on circuit size). All of these approaches increase the delay of a flip-flop and hence flip-flop with the lowest power will also have lower performance. One usually wants to know the minimum power for a given performance constraint or maximum performance for a given power dissipation. Therefore, both quantities need to be considered simultaneously. The simplest way to quantify the compromise between power and delay is to take the product of the two given by Equation 2.4.

$$PDP = P_{TOTAL} \times Delay \quad (2.4)$$

In Equation 2.4, the delay is the worst case data-to-output delay (t_{DQ}) (i.e., the maximum of $t_{DQ,LH}$ and $t_{DQ,HL}$). P_{TOTAL} is the total power consumption given by Equation 2.3.

2.3.4 Power Delay Tradeoff and Circuit Sizing Technique

Two basic parameters that determine overall performance: (1) speed and (2) power consumption at given frequency of operation. It is however well known that power can be traded off for speed and that superior can always be obtained at the expense of higher power consumption. Both of these parameters are dependent on the transistor sizing, supply voltage, and load capacitance of the circuit. There is no type of flip-flop

that is optimal for all paths. Performance critical paths require fastest operation, which results in sizing for peak performance, and thus large power consumption. The flip-flops in non-critical paths allow much less aggressive sizing due to the available time slack.

In order to provide a fair and insightful evaluation of the flip-flops, a systematic and effective way of sizing and optimizing each transistor is necessary. Therefore, a given flip-flop can either be optimized for high performance or for low power. To provide a good tradeoff between the conflicting sizing requirements for power and delay performances, the goal of optimization for most digital circuits is to minimize the Power-Delay-Product (PDP), i.e., optimal energy utilization for a given clock frequency. For a certain technology, the channel lengths of all transistors are nominally fixed at the minimal feature size, for e.g., at $0.18\text{-}\mu\text{m}$ in this study. The only parameter of interest (i.e., to be optimised) is hence the width of each transistor. Transistor sizing is optimised using an iterative procedure to achieve the minimum PDP_{CQ} (PDP with respect to the clock-to-output delay, t_{CQ}) and PDP_{DQ} (PDP with respect to the clock-to-output delay, t_{DQ}) for all designs. For each iteration, the parametric analysis simulation was carried out to achieve the optimum PDP_{CQ} and PDP_{DQ} for each transistor.

2.3.5 Simulation

Extensive simulations have been carried out on the proposed flip-flops that will be discussed in chapters 4 and 5 and some benchmark flip-flop circuits that will be discussed in chapter 3 based on the $0.18\text{-}\mu\text{m}$ CMOS Chartered Manufacturing Pte. Ltd (CHRT) technology. All the circuits discussed in this thesis were designed using Cadence's Virtuoso Custom Design Platform. The layouts have been drawn and optimized based on the actual n-well p-substrate CMOS process provided by the foundry, viz. Chartered Semiconductor Manufacturing Ltd. (CHRT). Besides layout compaction, Design Rule Check (DRC) has been performed by adhering to the minimum spacing restriction to avoid design rule violations and to ensure a margin of safety in the manufacturing process. Following that, Layout Versus Schematic (LVS) verification has been carried out to guarantee that the layout drawn truthfully represents the schematic design.

Waveform calculator that is included with the Cadence SPECTRE simulator can be used to perform many different measurements on the waveforms displayed in the waveform window. This includes computing the average of a waveform (e.g. power) over the entire length of the simulation or a given period of time, finding the propagation delay of between input and output signals, or addition/subtraction/multiplication/division of waveforms, etc. The power consumptions of the flip-flop, such as P_{INT} , P_{DATA} and P_{CLK} are measured by employing the testbench shown in Figure 2.9 during time 0 to 1 μ s. In particular, the average current flowing through the flip-flop design under test has been computed using Waveform Calculator. To do this, make sure that before simulation you select the Outputs > Save All > power (all) option in the Analog Design Environment window. The propagation delay between CLK to Q and D to Q are measured using the delay function from the waveform calculator. In addition, maximum operating clock frequency (MOCF) of the flip-flop is evaluated.

2.4 Approaches to Minimizing Flip-Flop Power Consumption

As discussed in chapter 1, a large portion of the power consumption in modern microprocessor designs is in the clock subsystem, including clock generation, distribution, and the final clocked storage elements. Due to increasing clock frequency, low skew requirements, and deep pipelining, demand for more power-conscious design of the clocked storage elements such as flip-flops and latches is on the rise. In this subsection, some widely used methods for power reduction are described. These include supply-voltage scaling, minimizing switched capacitance, minimizing switching activity, the use of low-swing circuit with multiple V_{DD} and clock gating techniques.

As mentioned in section 2.3, the dynamic switching power dissipation, being the dominant factor compared with the other components of power dissipation in digital CMOS circuits, has caught special attention in recent years. Dynamic power substantially increases in current and future technologies because of the ever increasing number of on-chip functionalities as well as a prolonging trend in getting higher clock frequencies. Many techniques have therefore been introduced to control this ever-increasing power

component at all levels of design abstraction—from device/process level to algorithm level. It should be stressed that the circuit techniques described for reducing dynamic power consumption may have impacts on the performance and silicon areas as well as on the remaining power components. It can be easily inferred from Equation (2.1) that the $P_{dynamic}$ of CMOS logic gates is proportional to the load capacitance, C_L , the square of V_{DD} , the switching activity α , and clock frequency f . Therefore, the guidelines for reduction power consumption are simply to minimize each of the parameters in the product expression. According to Equation (2.1), several techniques can be applied to minimize flip-flop power consumption. A designer should devise new techniques aiming at the decrease of power for each technique or any combination of them. Generally, the two main low-power reduction strategies concerning the reduction of supply voltage, V_{DD} , and the switched capacitance, C_{eff} , which is defined as the product of output capacitance times switching activity (i.e., $C_L \cdot \alpha$), are studied in this sub-section.

2.4.1 Supply Voltage Scaling

The reduction of the power supply voltage has a major impact on the power consumption due to the quadratic dependence of V_{DD} . Although such reduction is usually very effective, the circuit delay increases and the system throughput degrades. When a lower limit on the supply voltage is set by external constraints (as often happens in real-world designs), or when the performance degradation due to lowering the supply voltage is intolerable, the only means of reducing the dissipation is by lowering the effective capacitance, and will be discussed in more detail in next sub-section [25]. If C_L mainly consists of extrinsic components, and if this overall load capacitance can be estimated accurately and independently of the transistor dimensions, a simple first-order derivation can adequately predict the experimentally determined dependence and is given by [40]:

$$T_d = \frac{C_L \times V_{DD}}{I} = \frac{C_L \times V_{DD}}{\mu C_{ox} (W/L) (V_{DD} - V_{TH})^2} \quad (2.5)$$

Clearly, a speed penalty has to be paid for a V_{DD} reduction, with the delays drastically increasing as V_{DD} approaches the sum of the threshold voltages of the devices. In addition, a shift of the industrial approach to reduce the supply voltage is quite expensive. It also causes the circuit to slow down, for instance, the compatibility issues of input/output signals with the peripheral circuits [41].

The nominal power supply voltage for 0.18 μm technology is 1.8 V. however, for battery operated systems, the power supply voltage is reduced drastically to lower the power consumption. Also, an efficient low-voltage flip-flop should demonstrate a lower rate of incremental delay as the power supply voltage is reduced. Therefore, delay, power and PDP of all the flip-flops discussed in this thesis are computed as a function of power supply voltage. Again, since the setup time increases with reduced supply voltage, the simulations require relaxed setup time conditions to provide results over a wide range. Hence, in this analysis, t_{CQ} and PDP_{CQ} are determined for precise results.

2.4.2 Minimizing Effective Switched Capacitance

A very popular low power strategy is by reduction of the effective switched capacitance, C_{eff} for a given external load capacitance. Again, the total effective capacitance at some nodes inside the circuit is a product of the physical capacitance of that node and the switching activity. Physical capacitance includes clocked transistor capacitance and capacitance of non-clocked internal nodes. Reduction of the total physical clocked capacitance is more important because it is switched at every clock cycle, as opposed to the capacitance of the non-clocked nodes, which is switched only when the output changes. Based on this principle, we prefer to have as few clocked devices as possible and to use a single clock if it does not mean more clock devices.

A proper selection of flip-flop or latch topology that has inherently low switching activity at its internal nodes or smaller number of clocked nodes and clock gating can also be a good way for reducing switching activity. In General, the internal nodes of the static circuits have inherently lower switching activity than the internal nodes of the dynamic circuits due to the absence of dynamic nodes that need to be precharged at every

clock cycle. Dynamic operation also incurs overhead in energy that is consumed in the logic to generate the clock signals for driving dynamic nodes. This is not required if static logic is used [42]. Some internal nodes of the flip-flops are precharged and evaluated in each cycle without producing any useful activity at the output when the input is stable.

Reducing this redundant switching activity has a profound effect in reducing the power dissipation, and in the literature many techniques were presented for this purpose, such as conditional precharge technique [43], [44], conditional capture technique [45] and conditional discharge technique [46]. This will be discussed in detail in chapter 3.

2.4.3 Clock Gating Technique

Clock gating is an efficient way of reducing the overall energy consumption in flip-flop intensive digital systems when the energy in the clocking subsystem forms a significant portion of the overall system energy, or when the flip-flop data inputs have very small switching activities. The mechanism behind clock gating is to allow clocking of a flip-flop only if a new arriving datum is different from the current flip-flop output [47] [48] [49]. Finally, the load capacitance can be reduced by using certain circuit design styles and by proper transistor sizing.

2.4.4 Dual Supply Voltage Design using Cluster Voltage Scaling (CVS) Scheme

Lowering supply voltage results in a quadratic reduction in power dissipation but it significantly impacts delay. When both delay and power are constraints, there exists an optimum power for given delay of any block achieved through circuit sizing, supply and transistor threshold (V_{TH}) adjustments. In order to lower the supply voltage without system performance degradation, Clustered Voltage Scaling (CVS) has been developed in which critical and non-critical paths of the design are clustered. Since the speed requirements of the non-critical paths are lower than the critical paths, supply voltage of non-critical paths clusters can be lowered without degrading system performance.

Whenever an output from a low V_{DD} (V_{DDL}) cluster has to drive an input to a high V_{DD} (V_{DDH}) cluster, level conversion is required at the interface. To reduce the overhead of the level conversion, low V_{DD} clusters are followed by pipeline flip-flops and the level conversion is merged into the flip-flops [50]. These flip-flops, which simultaneously perform latching and level shifting, are called level converting flip-flops [50] [51] [52].

Chapter 3

Review of Low-Power/High-Performance Flip-Flops

This chapter reviews the representative flip-flops previously reported in the literature and used in the low-power and high-performance applications. Two dominant architectures in flip-flop design are master-slave latch pairs and pulsed-triggered latches. The new flip-flops reported nowadays are often derived from master-slave latch pairs or pulsed-triggered latches [53]. As discussed in chapter 2, a plethora of research efforts are concerned with the optimization of the clocking energy in the flip-flops [54]. An example of such flip-flops is the reduced clock swing flip-flops where the clock signal does not swing from rail-to-rail. Other techniques that were discussed in chapter 2 includes the internal clock gating [47] [48] [49], useful whereby the input data signal is not changing (data-transition look-ahead structures), the flip-flop that reduce redundant switching activity using conditional capture and conditional discharge techniques [45] [46], and dual supply voltage with clustered voltage scaling scheme [50] [51] [52] or triggering off of both clock edges (DETFFs). In this chapter, the study of flip-flops will be divided into two parts: single edge-triggered flip-flops (SETFFs) and double edge-triggered flip-flops (DETFFs). The design style and operation of each circuit implementation is discussed in detail.

3.1 Single Edge-Triggered Flip-Flops

3.1.1 Master-Slave Latch Pair

This section describes the conventional master-slave latch pairs: conventional transmission-gate based flip-flop (TGFF) [54] and clocked CMOS (C²MOS) flip-flop [34].

3.1.1.1 Transmission-Gate Based Flip-Flop

The single edge-triggered flip-flop based on the transmission-gate master-slave latch style (TGFF) [54] is presented in Figure 3.1. It is a conventional master-slave structure described earlier in section 2.1. This flip-flop is realized using two complementary transmission-gate latches operating on complementary clocks. In the TGFF, the forward path from the input D to the output Q consists of two inverters and two transmission-gates. The TGFF can be supplied with one-phase clock or two-phase clock (two-phase clocking strategy). To make a decision on which strategy to use is not possible without prior knowledge of the clocking strategy used at the system level. The TGFF is commonly used in standard CMOS cell libraries. However, TGFF consumes relatively high clock power and this implies a considerable number of clocked transistors in heavily pipelined circuits. The internal switching activity of the TGFF latch is mainly due to the input data switching. Moreover, both the clock and data loads are high, and this contributes to the total power consumption.

Figure 3.1 Transmission-gate-based flip-flop (TGFF) [54].

3.1.1.2 Modified Clocked CMOS (C²MOS) Flip-Flop

The modified clocked CMOS (C²MOS) master-slave flip-flop (mC²MOS) [34] is based on the combination of master-slave structure with the two C²MOS latches in complementary clock. The circuit presented in Figure 3.2 is a modification of the dynamic C²MOS master-slave latch by adding a C²MOS feedback at the output. The mC²MOS latch has large delay due to a p-MOS stack in the critical path. The only way to increase its speed is to increase the width of both p-MOS and n-MOS transistors in clocked CMOS inverters. However, this increase causes large clock power and large load on the critical internal node *S* (see Figure 3.2), resulting in poor energy-delay tradeoff. Like with the TGFF, in design of a system with mC²MOS flip-flop, there exists a tradeoff between the single-phase and the two-phase clock.

Figure 3.2 Modified C²MOS flip-flop (mC²MOS) [34].

3.1.2 Pulsed-Triggered Latch

This section describes the representative pulsed-triggered latch topologies. Pulsed-triggered flip-flops can be classified into two types, implicit and explicit, and this classification is due to the pulse generators they use. In implicit pulsed-triggered flip-flops or ip-FF, the pulse is generated inside the flip-flop, for example, hybrid latch flip-flop (HLFF) [55], and semidynamic flip-flop (SDFF) [56]. On the other hand, the explicit pulsed-triggered flip-flops, or ep-FF has its pulse generated externally. Examples of ep-FF are static explicit-pulsed flip-flop (SEPFF) [57] and single-transistor-clocked explicit-pulsed flip-flop (STC-EPFF) [57].

At a first glance, ep-FF consumes more energy due to the explicit-pulse generator. Then again, ep-FF has several advantages. First, ep-FF can have its pulse generator shared by neighboring flip-flops, a technique that is not straightforward to use in ip-FF. This sharing can help in distributing the power overhead of the pulse generator across many ep-FFs and a system using ep-FF will be more energy efficient than a system using ip-FF. Second, the double edge-triggering is straightforward to implement in ep-FF, but it is difficult to employ in ip-FF.

3.1.2.1 Hybrid Latch Flip-Flop

The hybrid latch flip-flop (HLFF) reported by Partovi et al. (1996) [55] is one of the high-performance flip-flops. It is a single-input single-output, positive edge-triggered flip-flop. It samples the data on one edge of the clock to eliminate the retardation of data flow on the opposite edge. By referring to Figure 3.3 it can be seen that prior to the rising edge of the clock the circuit is in the precharge phase, where node X is precharged to V_{DD} . The output inverters then hold the previously stored logical value at node Q , and the data is decoupled from node X because the second stage is off. At the rising edge of the clock (CLK), the pull-down sections of both the first and the second stages are enabled for a period of time defined by three-inverter delay chain (I1-3). During this period, the flip-flop is transparent and input D can be sampled into the flip-flop. If D is high in this period, node X goes low forcing Q to be high. If D is low, X will be set to high and Q

goes to low. Once CLKB goes low, node X is decoupled from D and is held at high or the p-MOS device that is driven by CLKB begins to precharge it to high. The falling edge of CLKB is the latching edge for the pull-down path of the second stage, while X rising is the latching edge for the pull-up path of the second stage. At the falling edge of the clock edge, node X is precharged to V_{DD} by the p-MOS transistor, M1, that is driven by CLK, and X remains high as long as the CLK stays low.

The HLFF [55] is fast, as the critical path from D to Q consists of a 3-input CMOS NAND gate and a fast dynamic second stage. However, the simplicity of the circuit has resulted in large internal power consumption, even when the input is not changing. If $D = 1$, the node X precharges high when $CLK = 0$ and evaluates to low when $CLK = 1$ in each clock cycle, regardless of whether this internal switching has effect on the output. In cases when Q is already high, this internal switching activity increases the power consumption, even though it does not perform any useful function.

Figure 3.3 Hybrid latch flip-flop (HLFF) [55].

3.1.2.2 Semidynamic Flip-Flop

The semidynamic flip-flop (SDFF) proposed by Klass in 1998 [56] is shown in Figure 3.4. This circuit is popularly engaged in high-performance applications because of its small delay, logic embedding feature and simple topology. The SDFF is composed of a dynamic front and a static back end. When the clock (CLK) is low, the circuit is in the precharge phase. Node X is precharged to V_{DD} and node Q is decoupled from the first stage. The static latch I5-6 holds the previous value of Q and QB . The evaluation phase begins at the rising edge of the CLK. The SDFF is transparent during a time window determined by the delay through two inverters (I1-2) and the NAND gate. If D is low, X remains high, driving Q low and QB high.

When D goes high, node X will discharge to drive Q to high and QB to low. Upon three gate delays after the rising edge of the CLK, the output, S , of the NAND gate goes low (see Figure 3.4), preventing discharge of node X by subsequent late 0-1 transitions on D . This circuit appears to be of edge-triggered due to the narrow capture and it is worth noting that a glitch occurs at Q when $D = Q = \text{high}$ which also implies increased in power consumption. This problem is also noted in the HLFF [55] design discussed earlier in sub-section 3.1.2.1. The disadvantages of SDFF [56] are the larger clock load and the bigger effective precharge capacitance; which again lead to greater power consumption especially for data patterns that contain more logic “ones”.

Figure 3.4 Semidynamic flip-flop (SDFF) [56].

3.1.2.3 Static Explicit-Pulsed Flip-Flop

The main structure of the static explicit-pulsed flip-flop (SEPFF) proposed by Zhao et al. (2002) [57] involves two cascaded static latches. The SEPFF schematic is depicted in Figure 3.5. SEPFF reduces the internal switching activity by eliminating the precharging at node X , to lower the power dissipation. Unlike the dynamic flip-flops, SEPFF has no precharge at each clock cycle. The internal node X follows the input D during the transparent interval. At the rising edge, $M3$ and $M6$ turn on for a short transparency duration, which equates to the delay incurred by the pulse generator, causing the input, D , to propagate to the output. The static latch ($I6$ - $I7$) maintains the output stage. During the transparency period when input D is stable and at high, X goes low, causing Q to go high. Node X remains low as long as D is high. This allows for savings in the dissipated power at node X , as a result of eliminating the redundant charging/discharging seen in dynamic flip-flops. However, the capacitive load at node X is somewhat larger as in HLFF [55], SDFF [56].

Figure 3.5 Static explicit-pulsed flip-flop (SEPFF) [57].

3.1.2.4 Single-Transistor-Clocked Explicit-Pulsed Flip-Flop

Zhao et.al., proposed dual path single-transistor-clocked explicit-pulsed flip-flop (called STC-EPFF) [57] that consists of two cascaded static latches sharing one clocked transistor (Figure 3.6). In order to reduce the capacitive load at node X , inverter $I8$ is added to get the complement of data D such that the 0-to-1 propagation delay is reduced. The inverter $I4$ is used to drive the nMOS transistor in the pull down path of the second stage. The output of the first stage drives only one pMOS transistor in STC-EPFF and thus the load on node X is reduced. The internal node X is asserted or disserted according to the input data D during the transparent interval. The internal nodes of STC-EPFF switches only when input changes. At the rising edge of the clock, the clocked transistor $M1$ turns on for a short time interval, which is the transparency period, and the circuit acts like two cascaded inverters allowing the input data to propagate to the output. After the transparency period, $M1$ switches off, causing the nMOS stacks of both stages to be disconnected from the ground supply rail, preventing the propagation of the input to the output. The output Q maintains its state by the keeper ($I6$ - $I7$).

Figure 3.6 Single-transistor-clocked explicit-pulsed flip-flop (STC-EPFF) [57].

3.1.3 Flip-Flops with Conditional Techniques for Reducing Switching Activities

One effective technique to obtain power savings inside a flip-flop can be devised by realizing the fact that a common property among various high-speed flip-flops is the utilization of dynamic structures. This dynamic behavior causes a lot of power to be wasted as a result of unnecessary internal switching activity, especially in moderate or lower data activity environments. Reducing these activities can effectively result in reducing the overall power dissipation, and in the literature many techniques were presented for this purpose such as conditional capture [45] and conditional discharge [46] techniques for high-performance flip-flops are reviewed in this sub-section.

3.1.3.1 Conditional Capture Flip-Flop

The conditional capture technique is reported in [45]. By disabling redundant internal transitions, this technique achieves significant power reduction at little or no delay penalties. Due to this property, it is particularly attractive from the point of view of high-performance VLSI implementations. The motivation behind the conditional capture technique is the considerable power consumption in driving the internal nodes when the value of the output is not changed (corresponding to low input activities). It is possible to disable the internal transitions when it is detected to ensure that they will not have an effect on the output.

The conditional capture flip-flop (CCFF) reported by Kong et al. (2001) [45] is illustrated in Figure 3.7. During the period in which the clock (CLK) is at a low logic value, the precharge node X is precharged to the supply voltage through transistor M1. Because CLKD is also at a low logic value, the output of the NOR gate, NB, is conditioned to the output, Q. If the output is at a low logic value, NB becomes high, and vice versa. Thus, the precharge node X discharges at the rising clock edge only when Q is at a low logic value and D is at a high logic value, which implies a pull-up transition of the output. For the remaining cases in which Q is at a high logic value or D is at a low logic value, X is held at the precharged voltage because at least M7 or M5 will

respectively remain off. The CCFF conditionally enables the discharge path and shuts it off after a brief transparency period. If the width of the transparency period becomes too narrow, the node X that must go low cannot be fully discharged to the ground level and thus, the flip-flop may experience static power dissipation.

Figure 3.7 Conditional capture flip-flop (CCFF) [45].

3.1.3.2 Conditional Discharge Flip-Flop

The conditional discharge scheme is employed in the conditional discharge flip-flop (CDFF) [46] in order to reduce the redundant switch power. The conditional discharge technique can be applied to both the implicit and explicit pulsed-triggered flip-flop, whereas the conditional capture technique can only be used to implement the implicit-pulsed flip-flop. Besides, the CCFF [45] is difficult to reconfigure for use in the double edge-triggering mechanism, since many transistors will be necessary. When CDFF employs the explicit single pulse generator [58] [see Figure 3.8 (a)], it will operate as SETFF. When it uses a dual pulse generator [58] [see Figure 3.8 (b)], it will operate as a DETFF. The schematic diagram of the single edge-triggering version of CDFF [46] is shown in Figure 3.8. It makes use of a discharge control nMOS transistor, M4, in the discharge path of the first stage.

When QB is 'high', which means Q is 'low' and X is 'high', M4 turns on, and the discharge path is enabled. If the input D makes a low-to-high during the sampling period that is determined by the delay incurred by the pulse generator, node X at Figure 3.8 is discharged to 'low', and Q is pulled to 'high' with QB is pulled down to 'low' which shuts off the nMOS stack in the first stage. For this transition (low-to-high), X is discharged only once, i.e., consecutive high level at D will not be sampled because the discharging path is inhibited by QB. If the input D was low during the sampling period, node X will remain high, forcing output Q to go low and QB high. Since node X is not precharged and discharged every clock cycle, no glitches will appear at the output node Q. When the input D stays high, Q will not be discharged at the beginning of each evaluation [30], as in the other precharged circuits such as HLFF [55], and SDFF [56].

(a)

(b)

(c)

Figure 3.8 Conditional discharge flip-flop (CDFF) [46]: (a) single pulse generator [58], (b) dual pulse generator [58], and (c) conditional discharge latch [46].

3.1.4 Flip-Flops with Reduced Clock Swing

As mentioned earlier, in any VLSI system, the clock system consumes 20-45% of the total chip power. And, 90% of the system clock power is consumed by the flip-flops themselves and the last branches of the clock distribution network which directly drives the flip-flops [15]. One reason for this large power consumption of the clock system is that the transition probability of the clock is 100% while that of the ordinary logic is about one-third on average. Consequently, in order to achieve low-power designs, it is important to reduce the clock system power. And to reduce the clock system power, it is effective to lower the clock voltage swing. Ideas for achieving achieve such clock voltage swing reduction were pursued in [16] and [59]. A reduced swing clock flip-flop technique targets the energy savings in the clocking of a flip-flop. This section presents two flip-flops with reduced swing clock operation: reduced clock swing flip-flop (RCSFF) [16] and NAND-type keeper flip-flop (NDKFF) [59].

3.1.4.1 Reduced clock swing flip-flop

Reduced clock swing flip-flop (RCSFF) [16] is proposed to lower the voltage swing of the clock system. The schematic diagram of RCSFF is given in Figure 3.9. The RCSFF is a positive edge-triggered flip-flop. It is composed of a true single-phase master-latch and a cross-coupled NAND slave-latch. The master-latch is a current-latch-type sense-amplifier. The salient feature of the RCSFF is that it can accept a reduced voltage swing due to the single-phase nature of the flip-flop. The voltage swing V_{Clock} can be as low as 1 V. Operational behavior of RCSFF is very similar to the behavior of SAFF. The differences are in the reduction of the clock swing and in the biasing of the precharge PMOS transistors in the RCSFF. The reduction in the clock swing leads to an increase in the leakage current of the precharge pMOS transistors in RCSFF. The leakage current of pMOS transistors P1 and P2 can be reduced by applying well bias V_{well} ($V_{well} > V_{DD}$). However, this scheme needs an additional area to separate the n-well region of clock-driven pMOS transistors, P1 and P2, from that of the other transistors. The RCSFF requires a reduced clock swing driver. The driver can be a specific circuit

that converts the rail-to-rail swing at its input to a lower swing at the output [16], or it can be a simple buffer powered up by an on-chip dc-dc converter or even an external voltage supply.

Figure 3.9 Reduced clock swing flip-flop (RCSFF) [16].

3.1.4.2 Reduced clock swing NAND-type keeper flip-flop

The schematic diagram of a NAND-type keeper flip-flop (NDKFF) [59] is shown in Figure 3.10. NDKFF is the implicit-pulsed based flip-flop since the clock pulse generator is generated by three inverters (I1-I3) internally. During this period, the first stage (M1-M4) captures high, and the second stage (M8-M11) captures low. Moreover, the level-keeping circuits composed of M5, M6 and M7 and I4-I5 keep the state of the internal node X and output node Q , to prevent them from being floating electrically. If input D of the flip-flop is 'high' during the transparency window, the internal node X is driven 'low', and the output node Q is driven 'high'. Once internal node X is driven 'low', it remains low as long as the input D is 'high', because of the path to ground provided by the feedback from the output Q . Only when the input D is switched from high-to-low later in the clock cycle, the internal node X can be driven 'high' again.

Similarly, if the input D is 'low' during the transparency window. The internal node X will then remain 'high', and this drives the output node Q to 'low'.

The state of the internal node X is set by the 2-input NAND of D and Q , which is composed of M1, M5, M6, and M7 in Figure 3.10. This feedback structure eliminates transitions when input D is the same as output Q . The configuration of NDKFF resembles that of HLFF [55] (Figure 3.3). HLFF is a pulsed-based flip-flop. In HLFF, unnecessary transitions are occurred at internal node X , when input D is high continuously during several clock cycles. This is because the precharging of X occurred at every cycle by M6 and it regardless of output Q and input D . In NDKFF, this problem is solved.

Furthermore, the supply voltage of three inverters I0-I3 is set to that of clock system, V_{CLK} . This enables the power of flip-flop to be saved. All transistors driven by the clock signals are nMOS transistors, which enables the NDKFF to operate both with reduced clock-swing signals that swing between zero and V_{CLK} ($V_{CLK} < V_{DD}$) and with full clock-swing signals. Therefore, NDKFF does not need additional clock driver or n-well while RCSFF requires additional clock driver and n-well.

Figure 3.10 Reduced clock-swing NAND-type keeper flip-flop (NDKFF) [59].

3.1.5 Flip-Flop with Clock Gating Technique

Again, in many applications, the power consumption of the IC clock system is one of the main sources of chip power dissipation. This is due to the high switching activity and the heavy capacitive loading of the clock network. Consequently, many techniques have been recently proposed to reduce clock system power dissipation, in particular [47] [48] [49]. The main feature of this flip-flop family is a mechanism for predictive turn off the internal clock when the input and output data are equal. Since there exists an overhead associated with local clock gating, the use of these flip-flops is justified for low switching activities of the input data.

3.1.5.1 Data-Transition Look-Ahead Flip-Flop

The schematic diagram of data-transition look-ahead (DL-DFF) [47] is given in Figure 3.11. It is a positive edge-triggered non-inverting flip-flop. A DL-DFF has three main features. First, the data-transition look-ahead (DL) circuit compares the input data with the hold data. Second, the clock control circuit cuts off the clock when the input and hold data are the same. And third, the dynamic circuit can be used a master latch because data are held in the master latch for less than a nanosecond.

When an input datum D is the same as the hold datum Q , the DL circuit makes $P1$ low. This turns the transmission gate in the clock control circuit off. As a result, both CK and CKN do not transit (dashed lines), but transit only when D and Q are different.

The pulse generator circuit generates a short pulse, CKI , at every rising edge of the external clock, CP . CKI then triggers the flip-flop if $D \neq Q$. If there was no pulse generator, this flip-flop could not triggered by data instead of the clock. For example, if $D \neq Q$ and the rising edge of CKI arrives, then the clock pulse, CK is generated and Q changes. However, if D changes again while the clock is still high and becomes different from Q , then another pulse of internal clock, CK , would be generated and the flip-flop would be actually triggered by the data.

Figure 3.11 Data-transition look-ahead D flip-flop (DL-DFF) [47].

3.1.5.2 Double-Gated Clock Master-Slave Flip-Flop (DB-MSFF)

The double-gated clock master-slave flip-flop (DB-MSFF) [48] applies the gating technique separately to the master latch and slave latch of a flip-flop. This will introduce overhead that is doubled, but significant reduction in power dissipation can be desired if input signal switching activity is low. The schematic of a DB-MSFF is shown in given 3.12. It is a negative edge-triggered flip-flop. In master latch (positive level sensitive latch), the comparison between D and Q is performed by a XOR gate, while the gating logic is a simple AND gate. If CLK is '0', CKG will also be '0' and the latch will be maintained in the proper hold-state. On the other hand, when CLK is '1' and D is different from Q, the gating logic enables the CKG signal so that the master latch can correctly switch. Note that if $D = Q$, the gating logic inhibits the propagation of switching activity from CLK to CKG.

A negative level-sensitive clock-gated latch (slave latch) is quite similar to the master latch. The difference is in the gating logic (implemented with an OR gate) and in the comparator logic (implemented with a XNOR gate).

Figure 3.12 Double-gated master-slave negative edge-triggered flip-flop (DB-MSFF) [48].

3.1.5.3 Differential CMOS Edge-Triggered Flip-Flop with Clock Gating (CGFF)

The differential CMOS edge-triggered flip-flop with clock gating (CGFF) [49] is a pulse-based flip-flop and it is an implicit-pulsed flip-flop. It is a negative edge-triggered flip-flop. The schematic diagram of the Diff-GFF is presented in Figure 3.13. A delayed clock CP1 is generated by the clock chain (I1-I3). The cascaded transistors, M7 and M8, generate a narrow pulse at the rising edge of the clock pulse. It is observed that whether or not the input signal D varies, there is always a narrow pulse to trigger the flip-flop. However, when the input signal D is in the low switching activity state it is not necessary to trigger the flip-flop for each clock pulse. For example, D stays 'high', and so the flip-flop need not be triggered. In this case, those narrow pulses to the flip-flop are redundant and the transitions that happened in the clock chain are also redundant. If the clock to the clock chain can be deactivated, the power can also be saved. Hence, designing a non-redundant transition clock chain (Figure 3.13) can be expected to save power when D input transitions are low. In Figure 3.13 (a), D and Q are the input and output signals of the flip-flop, respectively, and CLK is the clock signal. An XOR gate is used to compare the input D and the output Q. When $D = Q$, $XOR = 0$, while $XOR = 1$, when $D \neq Q$. the output of the XOR gate is used as an enable signal for the tri-state inverter. The clock chain is only driven by CLK when $D \neq Q$. The redundant transitions in the clock chain are therefore eliminated.

Figure 3.13 Differential edge-triggered CMOS flip-flop: (a) Differential CMOS latch, and (b) non-redundant clock chain [49].

3.1.6 Flip-Flop with Dual Voltage Circuit Technique using Clustered Voltage Scaling

As discussed in chapter 2, dual supply voltage (V_{DD}) design technique can be very effective in reducing power consumption of CMOS circuit without sacrificing system performance [50]. Whenever an output from a low V_{DD} (V_{DDL}) region has to drive an input to a high V_{DD} (V_{DDH}) region, a level conversion is needed at the interface. To reduce the overhead of level conversion, low V_{DD} regions are followed by pipeline flip-flops and the level conversion is merged into the flip-flops [50]. The flip-flops simultaneously perform latching and level shifting and hence are called level converting flip-flops (LCFFs) [50] [51] [52].

3.1.6.1 Clock Level Shifted Sense-Amplifier Based LCFF

Figure 3.14 shows a schematic diagram of the clock level shifted sense-amplifier flip-flop (CSSA) [50]. The circuit is composed by a sense amplifier master stage followed by a NAND-based set-reset slave latch. Since low swing data and clock are unable to drive pMOS transistors of the flip-flops, which are supplied by V_{DDH} , the clock signal is level-shifted up to V_{DDH} and applied to the pMOS precharge transistors of a sense amplifier flip-flop to enable correct precharging operation. Data is applied to the nMOS transistors of the flip-flop, and therefore does not need to be level-shifted. The main problem of this scheme is that it uses the dynamic precharge style especially when the clock signal has a very low voltage swing. If D is kept stable, one of the internal nodes will still have to be charged/discharged every clock cycle. There is hence inevitable internal redundant switching power consumption. Moreover, CSSA uses cross-coupled NAND gates as the set-reset latch that results in unsymmetrical output delays and limits the performance of the flip-flop.

Figure 3.14 Clock level shifted sense amplifier flip-flop (CSSA) [50].

3.1.6.2 Pulsed Half-Latch LCFF

Figure 3.15 depicts the pulsed half-latch (PHL) LCFF [51]. It uses the pass-transistor half-latch level converter (see Figure. 3.15). It has the same topology as the slave portion of master-slave half-latch (MSHL) [51], but its nMOS pass gate (M1) is driven by a pulsed clock, CLK_Pulse, generated from the clock, CLK using the NAND gate and the inverter delay line (see Figure. 3.15). One nMOS pass transistor M1 and one inverter, I2 are used to implement the level shifting. However, the data driving inverter I1 is working at low-voltage, V_{DDL} . The keeper I2 which is working at high voltage V_{DDH} , is fighting with I1 during level shifting. Level shift point (sf) is lifted to $(V_{DDL} - V_{th}$ of nMOS) through nMOS transistor M1, and keeper I2 will put it to V_{DDH} . The PHL has reduced threshold voltage due to the used of a pass transistor and the voltage difference, for keeper I2 to restore, which is $\{V_{DDH} - (V_{DDL} - V_{th})\}$, is quite large. Such voltage drop will impact the circuit switching [24].

Figure 3.15 Pulsed half latch level conversion flip-flop (PHL) [51].

3.1.6.3 Self-Precharged Level Conversion Flip-Flop

The schematic of the self-precharging flip-flop (SPFF) [52] is shown in Figure 3.16. It is composed of two stages. The first stage is a sampling circuit detecting the voltage at the input during a pulse window implicitly generated on the rising edge of the clock. Conditional capturing capability has been incorporated by using a feedback from the outputs through the NOR gates that drive the lowest nMOS transistor in the sampling paths. This helps in getting rid of redundant transitions from the dynamic nodes resulting in statistical power saving based on the data switching activity. The amount of power saving achieved by this internal clocking gating is larger than the incurred power overhead for relatively low data switching activities. However, for high data switching activities the conditional capturing may not be of benefit since there is less chance to gate the clock and prevent redundant internal switching.

If the dynamic node, X is discharged, the output goes high and the precharge transistor (M1) is turned on and the recharges the dynamic node. During the rest of the clock cycle, the NOR gate and M1 act like an inverter and a keeper and therefore keep the node X charged. If the output goes high due to a discharge on X , the feedback from the output to the sampling path turns off the sampling path so that the self-precharging operation does not cause any short circuit power consumption. In this flip-flop, data and clock can have any voltage swing and the level conversion occurs on the dynamic nodes, X . Another benefit of the self-precharging technique is that it reduces the clock load and reduces the clock power. Moreover, the switching activity of the self-precharging circuit is dependent on the data switching activity, which tends to be less than the clock switching activity. Therefore, for moderate and low data switching activities the power overhead of the self-precharging circuit is mitigated by the saving from the clock power.

Figure 3.16 Self-precharged level conversion flip-flop (SPFF) [52].

3.2 Double Edge-Triggered Flip-Flops

Potential benefit of double edge-triggered is the operation at half the clock frequency of the original single edge-triggered design, while delivering the same performance [see Figure 2.3]. By operating at halved frequency, the power consumption of the clock distribution network will be reduced. In order to exploit this advantage, the performance of the DETFFs must be comparable as to the original SETFF design. In addition, if the clock load of a DETFF is much larger compared to the SETFF, power savings due to the clock frequency reduction may be canceled by an increase of the switching capacitance. Therefore, clock load is an important performance parameter of a DETFF.

As discussed in chapter 2, DETFF can be classified into three main structures: (1) pulsed-latch structure, (2) latch_MUX structure, and (3) complete flip-flop structure (see Figure 2.6). Several DETFF papers have been published in the literature, for example [60-67]. In this section, the conventional and some recently reported DETFFs [63-67] in the literature will be discussed.

3.2.1 Conventional Double Edge-Triggered Flip-Flop

Figure 3.17 shows a DETFF, the $DET_{A\text{fghahi}}$, proposed by M. Afghahi and J. Yuan [63], which is a complete flip-flop design style that uses 20 transistors to implement two complementary SETFFs connected in parallel. Out of the 20 transistors 8 of them are clocked. For any of the clock logics, only one of the blocks is in active mode leaving the other in high-impedance mode for it to decide the output value and vice versa. As a result, the two flip-flops are just ANDed together with a common inverter at the output. However, due to unnecessary transitions at the internal nodes, the flip-flop consumes relatively large amount of power when the input is stable, at either low or high.

Figure 3.17 Conventional double edge-triggered flip-flop ($DETFF_{A\text{fghahi}}$) [63].

3.2.2 Latch-MUX based DETFF

J. S. Wang [64] proposed the True Single Phase Clock (TSPC) based DETFF of Figure 3.18. This design also makes use of a Latch-MUX structure. It has 18 transistors with only 4-clocked transistors, allowing lesser capacitive loading. However, the main problem with this circuit is the charge sharing at the internal nodes. When input D is high at the rising clock edge, the voltage at node Y12 pull to 1.33 V (see Figure 3.18) and the voltage at node Y21 becomes 0.51 V (at a supply voltage of 1.8 V using 0.18- μm technology). However, full swing is essential for scalable circuits and besides full swing ensures low static power dissipation. Any circuit driven by a signal with incomplete swing may experience static power dissipation. This problem is aggravated as the supply voltage is scaled down since the reduced swing of the internal nodes is directly related to the supply voltage. The circuit also consumes more power than DETFF_{Afghahi} during maximum input switching activities. These intermediate values on the Y11/Y12/Y21/Y22, reduce the driving strengths of transistors M13, M14, M15 and M16.

Figure 3.18 Latch-MUX based DETFF (DETFF_{Wang}) [64].

3.2.3 Dual Pulse Clocked Double Edge-Triggered Flip-Flop

In dual pulse clocked double edge-triggered flip-flop (DPC-DETFF) [65], the latching part is a split-output TSPC, as illustrated in Figure 3.19. The pulse-generator stage uses dual rail XOR/XNOR gates to generate clock pulses on the rising and falling edge of the clock. The clock pulses are then provided to the split-output TSPC latch to sample the input data. The design of the pulse generator stage is based on the pass-transistor logic. The split-output TSPC latch uses a PMOS transmission gate to connect nodes A and B (shown in Figure 3.19). The DPC-FF has a threshold drop in the clock generator which uses a differential structure. It aggregates the crossover fighting, since a pMOS cannot turn off immediately by $(V_{DD} - V_{th})$. Moreover, it has a larger number of clocked transistors, resulting in high power consumption. In addition it has a floating node at the output.

Figure 3.19 Dual pulse-clocked double edge-triggered flip-flop (DPC-DETF): (a) dual pulse generator, and (b) split output TSPC latch [65].

3.2.4 Double Edge Transmission Gate Pulsed Latch

A double edge transmission-gate pulsed latch (DE-TGPL) proposed by Tschanz [58] is shown in Figure 3.20. It consists of a clock pulse generator and a transmission-gate (TG) latch. The clock pulse generator creates a short pulse after each clock edge. During each pulse, the TG latch becomes transparent and captures the input data. At all other times, the latch is opaque and changing of output data is not allowed. The pulse after each clock edge is obtained by performing the XOR/XNOR function of the input clock and the delayed clock. The delayed clock is obtained by using an odd number of inverters. In this way, the clock and delayed clock are at the same logic level only during the short time after both edges of the clock. In Figure 3.20, the XOR pass transistor logic gate is used to obtain a short negative pulse, N_Pulse and a short positive pulse P_pulse after each clock edge. The main advantage of the DE-TGPL is its speed because the D-to-Q path traverses only a single TG and an inverter. However, the power consumption of the DE-TGPL is dominated by clock activity because of the large switching activity of the clock pulse generator.

Figure 3.20 A double edge transmission-gate pulsed latch (DE-TGPL) [58].

3.2.5 Static Double Edge-Triggered Pulsed Flip-Flop

Figure 3.21 shows another dual edge-triggered static pulsed flip-flops presented by Aliakbar [66]. This circuit makes use of a static differential latch [see Figure 3.21 (a)] and a dual pulse generator [see Figure 3.21 (b)]. The dual pulse generator consists of four inverters for generating the delay and the inverted clock signals, CK2 and CK3, together with two nMOS transistors, the pulse signal is generated at both the rising and falling edges of the clock. This pulse signal is then applied to a static differential latch to derive the DETFF. During the transparency period (determined by the pulse generator), when the input D is high, static node SB goes low, and this implies that outputs Q and QB will be at high and low, respectively. This differential circuit employs cross-coupled inverters (M1, M2, M3 and M4) for maintaining the output at all times. However, it has double input and output capacitive loads.

Figure 3.21 Static double edge-triggered differential pulsed flip-flop (Diff-FF): (a) static differential latch, and (b) dual pulse generator [66].

3.3 Summary

The choice of the flip-flop topologies depends very much on the targeted application. Flip-flop delay overhead is still the most dominant parameter in high-speed systems, although the energy consumption and especially the clocking component, is of increasing concern. Pulsed latches offer the smallest data-to-output delays due to the negative setup time. In low-power applications, flip-flops based on master-slave latch pair in general dissipates less energy than pulse-based flip-flops at the expense of increased delay. Therefore, practical applications where low-power is of primary concern would involve master-slave topologies.

From the examples presented, some of the main methods used in the design process to achieve low-power consumption in flip-flop circuits can be summarized. Internal clock gating is an efficient design technique for reducing energy consumption in flip-flops by virtually disabling the internal clock when data input pattern is constant. The advantage here is that energy is not expended during periods of input inactivity. There are several design issues associated with this technique. One major issue is the additional energy consumed in the newly added clock gating logic. In order for this technique to be considered efficient, the additional energy usually must be less than the energy in the internal clocked nodes. It must also be stressed that the switching activity of the input must be considered when deciding on the feasibility of internal clock gating. Clock gating should be used on low input data rates. Otherwise the energy consumed by the clock gating logic will dominate the total energy measure. The delay typically increases as a result of an increase in clock-to-output delay. The clock-to-output delay reflects an extra propagation delay from the additional clock gating logic. When the input pattern switches with high probability, another technique must be used to reduce the energy consumption. Many designs today resort to using the method of reduced swing clocking.

As the name implies, reduced swing clocking means that the clock signal does not complete a full rail-to-rail cycle. At a first glance, this technique appears to offer tremendous savings in energy because the energy expended in the clock nodes decreases quadratically with the maximum clock output level. This does not necessarily lead to an improvement in energy consumption because in typical circuits, reduced swing operation

sometimes requires exclusive transistor sizing and substrate biasing in order to suppress excessive leakage currents.

Another technique introduced in this chapter is the dual supply voltage technique, using clustered voltage scaling (CVS) scheme. Due to quadratic relations between voltage and power consumption, the reducing supply voltage is very efficient in decreasing power dissipation. A dual supply voltage design in which a reduction in supply voltage is applied only to circuits outside critical paths can save power without sacrificing either throughput or latency. The optimal CVS design relies on a level converter implemented in a flip-flop to minimize power, delay and area penalties due to level conversion. A key challenge in designing efficient dual supply circuits involves the cost of level converters (LC) placed on the boundary between V_{DDL} and V_{DDH} .

One last technique introduced in this chapter is the use of double edge-triggering (DET). DET offers many wonderful advantages to deal with the energy-performance tradeoff. Because both edges of the clock are utilized, there is an increase in energy efficiency. To achieve this efficiency, we must therefore lower the clock frequency to help minimize the energy and to maintain the same level of delay performance. It must be noted that there are a number of important issues regarding the use of DET. A careful control of the clock's duty factor is crucial to ensure that the combinational can have sufficient time to function correctly during both phase of a clock cycle.

Table 3.1 Pros and Cons of all flip-flops discussed.

Flip-Flops	Pros	Cons
Transmission-gate based flip-flop (TGFF) [54]	Low-power static design style	Poor driving capability
Modified C^2 MOS flip-flop (mC^2 MOS) [34]	Good driving capability	Large delay due to pMOS transistor stacking
Hybrid latch flip-flop (HLFF) [55]	Negative setup time	Large internal power at low input activities
Semidynamic flip-flop (SDFF) [56]	Negative setup time, smallest delay	Redundant switching activity at node X when data has low activities
Static explicit-pulsed flip-flop (SEPFF) [57]	Static design style: no precharge at each clock cycle	Large low-to-high output delay due to capacitive load at node X
Single transistor clocked explicit-pulsed flip-flop (STC-EPFF) [57]	High-speed	High impedance when clock pulse is low
Conditional capture flip-flop (CCFF) [45]	Eliminate redundant internal transition	Implicit pulsed-triggered & difficult to configure for use in double edge-triggering
Conditional discharge flip-flop (CDFF) [46]	Both implicit & explicit pulsed-triggered can be applied	Dynamic logic
Reduced clock swing flip-flop (RCSFF) [16]	Reduce clock system power	Separate n-well required
Reduced clock swing NAND-type keeper flip-flop (NDKFF) [59]	no redundant internal transition for logic “ones”	Larger capacitive load at node X
Data-transition look-ahead D flip-flop (DL-DFF) [47]	gated-clock: good candidate for low input activities	Large number of transistors
Double-gated master-slave negative edge-triggered flip-flop (DB-MSFF) [48]	gated-clock to both master-slave latch pair	Larger clock to output delay due to extra clock gating circuitries

Differential edge-triggered CMOS flip-flop [49]	Eliminate redundant transition in the clock chain	Unsuitable for low-voltage applications due to its pass-transistor based gated-clock logic circuit
Clock level shifted sense-amplifier flip-flop (CSSA) [50]	Sense-amplifier based design	Unnecessary charging/discharging at every clock cycle especially input data is stable
Pulsed half latch level conversion flip-flop (PHL) [51]	Low-power	Voltage drop occurred
Self-precharging level conversion flip-flop (SPFF) [52]	Prevent internal switching with level conversion	Use of implicit pulsed generator,
Conventional double edge-triggered flip-flop [63]	High-speed	Large number of clocked transistors
Latch-MUX based DETFF [64]	Smaller number of clocked transistors	Unable to achieve full-swing at internal nodes
Dual pulse-clocked double edge-triggered flip-flop (DPC-DETFF) [65]	High-speed, explicit pulsed-triggering	Floating node at output
A double edge transmission-gate pulsed latch (DE-TGPL) [58]	Sensitive to input noise	Large switching activity at clock pulse generator
Static double edge-triggered differential pulsed flip-flop (Diff-FF) [66]	Balanced output delays	Unsuitable for low-voltage application due to its non-full swing clock pulse generator

Chapter 4

Newly Developed Single Edge-Triggered Flip-Flops

This chapter describes the newly developed single edge-triggered flip-flops that had provided better performance or power improvements for the conventional and previously reported flip-flops. In section 4.1, the output feedback flip-flop that achieves power saving by reducing the internal switching activities will be presented. Section 4.2 discusses on a novel static explicit-pulsed flip-flop with local feedback which gives low power and small area features when compared to other counterpart designs. Section 4.3 will describe the new explicit-pulsed flip-flop based on novel static latch and True Single Phase Clock (TSPC) based dynamic pulse generator that can achieve low-power and higher performance as compared to the contemporary circuits. A new level-converting flip-flop with clustered voltage scaling using the dual supply voltage technique is then presented in section 4.4. This level-converting flip-flop incorporates pass-gate level-converting latch and TSPC based dynamic pulse generator and gives a substantial savings in power consumptions with shortest delay.

4.1 Output Feedback Flip-Flop

Many contemporary microprocessors selectively use master-slave and pulse-triggered flip-flops [18]. The master-slave flip-flop has superior race tolerance but yields poor latency and power efficiency. On the other hand, the pulsed-triggered flip-flop provides superior latency and power efficiency, but suffers from race tolerance. Nevertheless, the pulsed-based topology is still capable of constructing complex logic. One of the main advantages of pulse-triggered flip-flops is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time. Due to these timing issues, pulsed-based flip-flops provide higher performance than their master-slave counterparts.

Selection of a circuit style that has inherently low switching activity in the internal nodes or a small number of clocked nodes is also a good way for reducing energy. Conventional flip-flops such as the hybrid latch flip-flop (HLFF) [55] (see Figure 3.3) and the semidynamic flip-flop (SDFF) [56] (see Figure 3.4) are popularly used for high-speed digital systems due to the small latency between the latest data arrival and the corresponding output transition. However, the internal nodes are precharged and evaluated in each clock cycle without producing any useful activity at the output especially when the input is stable. Hence, the use of these designs is associated with considerable power consumption. One of the reasons for this is the high internal activity of the circuit even when input activity is small. Also, the increased output activity due to glitches when the output is at the high level contributes to the total power dissipation. The reduction of this redundant switching activity will have a profound effect in reducing the power dissipation. The conditional capture flip-flop (CCFF) [45] (see Figure 3.7) addresses this issue. It provides substantial power reductions for low input switching activities by eliminating redundant transitions of the internal precharge nodes. The static explicit-pulsed flip-flop (SEPFF) [57] (see Figure 3.5) eliminates the dynamic precharging of the pull-up transistor through the use of input data (D) instead of clock signal and this helps to reduce power dissipation especially when the input D is stable. Therefore, an area-efficient flip-flop, which is based on the modifications of the conditional capture flip-flop (CCFF), is proposed. It has been verified by circuit

simulations using the 0.18 μm CMOS technology from Chartered Semiconductor Manufacturing Pte Ltd (CHRT) that the proposed design that can eliminate the unnecessary internal transitions to minimize on the power dissipation regardless of its input activities, with no impact on its latency with small area consumption is developed in this work.

4.1.1 Circuit Operation

Figure 4.1 presents the schematic diagram of a positive edge-triggered flip-flop called the output feedback flip-flop (SET-FBFF) that is proposed in this research study. The circuit employs the two-stage concept where the pull-down section of the second stage functions only when the input D is set to 0. The n-MOS transistor M7, controlled by the inverted output signal QB, is employed at the discharge path of the first stage and so, precharge node *X* only drives the output to pull up transistor, M2, in the second stage. This not only eliminates unnecessary switching activity but also reduces the capacitive load at node *X*. The basic concept behind the proposed circuit is to generate a small pulse (sampling window) at the rising edge of the clock. This requires a NAND gate with a clock and a delayed inverter clock as its inputs. The delayed clock is generated with the help of I1. The trailing edge of this short pulse is used as a time reference for shutting off the flip-flop. A short “Time Window” is created for the flip-flop for accepting data, which is the way to create “edge” in the digital world [53]. This will ensure substantial internal power savings, in particular, at low input switching activity. On top of that, the capacitive load at node *X* is also reduced.

When the CLK is low, transistor M1 turns on. Node *X* is precharged to high, cutting off node Q from the input stage. Two inverters I4 and I5 are used to maintain the output when the circuit is in the hold mode. If the input D is high in the sampling window, and Q is assumed to be low initially that is QB is then high, *X* will be discharged through the pull down path M3, M5 and M7. The outputs, Q and QB, will then be of high and low respectively, which shuts off the n-MOS stack in the first stage. For this low-to-high transition of D, *X* is discharged only once, i.e., the consecutive high level of D will not be

sampled because the discharging path is inhibited by QB. Consider the next operation when input, D, is low in the sampling window, both the two pull down stacked transistors M4 and M6 will be simultaneously turned on to pull the output, Q, to ground.

Since node X is not charged and discharged at every clock cycle, no glitches appear at the output node Q when the input stays high, and Q will not be discharged at the beginning of each evaluation [30] cycle, as noted in other precharged dynamic circuits such as the HLFF [55] and SDFF [56]. The important advantage of our proposed FBFF is that it provides less internal power consumption than other reported SETFFs such as HLFF [55], SDFF [56], CCFF [45] and SEPFF [57], for all different input switching activities. For applications where the input data activity is inherently low, the proposed SET-FBFF design can therefore provide substantial power reduction. Moreover, the proposed SET-FBFF is easy to be implemented as a double edge-triggered flip-flop (i.e., DET-FBFF), by simply using an XOR gate instead of NAND gate. This will be discussed in the next chapter. As for CCFF [45], it is difficult for use in double edge-triggering mechanism since the duplication of NOR-gate and other clocked transistors are necessary. Moreover, the proposed design has less clocked transistors which means less clock power consumption than CCFF. Therefore, the proposed design acts as a viable contender in replacing the CCFF for the area advantage when it becomes more significant with reducing feature size/technology. This attribute blends well with the contemporary and ongoing process technology miniaturization.

Figure 4.1 Single edge-triggered output feedback flip-flop (SET-FBFF).

4.1.2 Results and Comparative Study

The reported flip-flops chosen for comparison with SET-FBFF are HLFF [55], SDFF [56], CCFF [45], and SEPFF [57]. All the SETFFs considered in this sub-section have been designed based on the 0.18- μm single-poly six-metal (1P6M) Chartered Semiconductor Manufacturing Pte. Ltd process at 1.8 V supply. The simulations are performed in SPECTRE simulator with the parasitics extracted from the layouts for all flip-flops discussed, by employing the sizing technique and simulation procedure discussed in section 2.3. The transistor widths are shown in Figure 4.1. The parameters of interest include delay, power consumption for different input activities, PDP, and so on. They are measured using Waveform calculator as discussed in sub-section 2.3.5.

The characteristics of all flip-flops presented are tabulated in Table 4.1. The power consumption break-up for different input activities is also illustrated in the graph of Figure 4.2. It can be seen that the proposed SET-FBFF consumes the least total power consumption among SETFFs discussed regardless of the input switching activity. With regards to power consumption, when compared to the CCFF [45], the SET-FBFF requires 11.3% less power during maximum input switching activity (i.e., at $\alpha = 1$) and 6% less power at the lowest input switching activity (at $\alpha = 0$ and with all's 1 input).

The important advantage of the proposed output feedback flip-flop (SET-FBFF) is that for all different input switching activities, it provides less internal power consumption than other reported SETFFs discussed, with no impact on its latency. As compared to previously reported SETFFs (HLFF [55], SDFF [56], CCFF [45] and SEPFF [57]), the SET-FBFF has the shortest delay along with the smallest silicon area. The SPECTRE simulation results indicated our proposed design consumes the least power regardless of the input activity among all reported SETFFs. However, for all's 0, SET-FBFF consumes about 2% more power than the HLFF. Since the nMOS transistor M7 of the first stage is always on when data "D" is set to "0", it reveals that the leakage power consumption of the circuit is proportional to the number of active transistors of the circuit under test. As for the PDP with regards to the data to output delay (PDP_{DQ}), the proposed SETFF outperformed the CCFF [45] design, which has the lowest PDP among other SETFFs (HLFF [55], SDFF [56], SEPFF [57]), by 11.1%.

As already discussed in section 2.4.1, the power delay product with respect to clock-to-output delay (PDP_{CQ}), is evaluated under different supply voltages is summarized in Figure 4.3. The best energy consumption versus supply voltage is seen from the proposed SET-FBFF. HLFF and SDFF have similar energy dissipation at 1.8V, 1.5V and 1.2V, but HLFF fails to operate below 1.2 V. The SEPFF has the worst PDP_{CQ} at all supply voltages and it fails to function at half of the nominal supply voltage. Overall, the proposed flip-flop has best performance with small-area feature at all supply voltages tested.

[1]-HLFF [55]; [2]-SDFF [56]; [3]-CCFF [45]; [4]-SEPFF [57]; [5]-SET-FBFF;

Figure 4.2 Power consumption break-ups for different input activities.

Figure 4.3 PDP_{CQ} versus supply voltage for 0.18 μm CMOS technology at $C_L = 50$ fF.

Table 4.1. Overall Performance of HLFF [55], Sdff [56], CCFF [45], SEPFF [57] and SET-FBFF.

Flip-Flops	Setup (ps)	Hold (ps)	t _{DQ} (ps)	P _{TOTAL} (μW) ¹	PDP _{DQ} (fJ)	# of transistors ²	Layout Area (μm) ²	MOCF (MHz)
HLFF[55]	-50.23	131.4	145	92.16	13.4	20	182.23	1.02
Sdff[56]	-33.52	103.23	129	101.28	13.1	23	242.8	1.2
CCFF[45]	-28.44	133	138	84.9	11.7	26	181.1	1.1
SEPFF[57]	-42.28	169	184	120.6	22.2	26 (12)	316.1	0.9
SET-FBFF	-56	133	138	75.3	10.4	22	160.8	1.1

¹f_{CLK} = 100 MHz @ maximum data activity (α = 1), and with V_{DD} = 1.8 V

²in parenthesis is number of transistors in clock generator (where applicable)

4.2 Static Explicit-Pulsed Flip-Flop with Local Feedback

The selection of a circuit style that has inherently low switching activity in the internal nodes or a small number of clocked nodes can be a good way for reducing energy. For example, in most cases, static circuits have smaller energy consumption than dynamic circuits, because the dynamic behavior causes a lot of power to be wasted as a result of unnecessary internal switching activity, especially in moderate or lower data activity environment. In this regard, Zhao [46] proposed the conditional discharge technique to combat the concern. A conditional discharge technique is proposed in [46] for both implicit and explicit-pulsed triggered flip-flops and therefore the implementation of both the single- and double-edge triggering will be straightforward. The single-edge triggered version of the CDFF [46] that employs the single pulse generator [58] is shown in Figure 3.8. In this technique, an nMOS transistor controlled by QB is inserted in the discharge path of the first stage which helps to eliminate the extra switching activity when the input is at a stable high. For low-to-high transition of D in the sampling period, X is discharged only once. This helps to reduce the internal switching activity and generates less glitches at the output. However, there are three transistors stack in the pull-down section of the first stage, and this causes a slow low-to-high output transition.

The internal nodes of static circuits in general have inherently lower switching activity than the internal nodes of the dynamic circuits due to the absence of dynamic nodes that need to be precharged every clock cycle. Accordingly, [57] proposed two flip-flop designs based on the Explicit-Pulsed approach, where the static Explicit-Pulsed Flip-Flop (SEPFF) is for low-power applications (Figure 3.5), and the Single-Transistor Clocked Explicit-Pulsed Flip-Flop (STC-EPFF) is for high-speed designs (Figure 3.6). The first stage of EPFF [58] is changed from dynamic to static and so it has become static Explicit-Pulsed Flip-Flop (SEPFF) [57] (refer to Figure 3.5). SEPFF yields savings in power dissipation as a result of eliminating precharging at node X. The second design STC-EPFF (Figure 3.6), where the clocked transistors of Figure 3.5 are merged into one transistor, helps to reduce the load on the clock pulse from two to one. In order to reduce the 0-to-1 propagation delay and the capacitive load at node X, a CMOS inverter is added to create the complement of D. The keepers are engaged to eliminate the floating node at

node X (see Figure 3.6). A simple but innovative static explicit-pulsed single/double edge-triggered flip-flop is therefore introduced in this section. Because of its static nature, the switching activity is dependent on the data switching activity which is usually less than the clock switching activity. The proposed circuit occupies smaller area as compared to the reported explicit-pulsed triggered designs [46] [57]. It has been verified by circuit simulations using the 0.18 μm CMOS technology from Chartered Semiconductor Manufacturing Pte. Ltd (CHRT). The operational principle is discussed in details in the following sub-section.

4.2.1 Circuit Operation

In the proposed design (see Figure 4.4), the dynamic precharging of the pull-up transistor M1 is controlled through the use of D instead of CLK_Pulse. By doing so, the switching activity at node X is determined only by the input D instead of the clock CLK_Pulse. Consequently, the switching activity is dependent on the data switching activity which is usually less than the clock switching activity at the internal node X . Moreover, to avoid charge coupling due to adjacent switching signals such as clock signal at node X for many consecutive high levels of D, a small-sized transistor M7 that is triggered by the output feedback signal is used. The schematic of the proposed static latch with local feedback is presented in Figure 4.4 (b). Hence, the proposed design is named the Static Explicit-Pulsed flip-flop with local Feedback (SEPFb). The single and double transparency window generation principles are straightforwardly applied to SEPFb by simply changing the pulse generators thus obtaining the SET-SEPFb and DET-SEPFb. Again, the double edge-triggered version of proposed static explicit-pulsed flip-flop with local Feedback (DET- SEPFb) will be presented in chapter 5.

The operating principle of the single edge-triggered version of the SEPFb is described as follows. The proposed SEPFb is composed of two static stages. When the transparency window arrives, the pull-down path of the first stage (M2-M3) responds with a 0-1 input transition, consequently the node X switches low. As a result, the output Q is pulled to V_{DD} via pMOS transistor M4. As for the 1-0 input transition, the high level

of X causes Q to go low through the pull-down path (M5-M6) of the second stage. When input D is at stable high (i.e., Q remains at high logic value), the local feedback transistor M7 keeps the value of node X low. As a result, node X will not be floating even when the clocked transistor is disabled, at outside the transparency window. Also node X will remain high as long as input D remains low. Since node X does not exercise precharge-evaluate sequence in each clock cycle, the internal power consumption for low input switching activity is saved. As compared to the earlier discussed flip-flop designs, the SEPFB utilizes a very small-size nMOS transistor M7 to prevent having floating at node X and it can save the area consumption of the circuit without sacrificing on power and delay performance.

Unlike the CDFP [46], SEPFB requires no precharging at each clock cycle and the switching activity of SEPFB is dependent on the data switching activity, which tends to be much less than the switching activity of the clock. Furthermore, SEPFB is able to reduce the load on the pulse generator output, from three to two transistors per flip-flop using only M2 and M5.

Figure 4.4 Static explicit-pulsed flip-flop with local feedback: (a) single pulse generator, and (b) static latch with local feedback.

4.2.2 Results and Comparative Study

In this sub-section, the simulated performances of the proposed flip-flops are compared against some recently developed designs CDFF [46], SEPFF [57] and STC-EPFF [57] that were earlier reviewed in chapter 3. According to the simulated and optimized gate area of the circuits, the most compact and area-optimum layouts are drawn based on the 0.18- μm single-poly six-metal (1P6M) Chartered Semiconductor Manufacturing Pte. Ltd (CHRT) process CMOS design rules for comparison on their layout area consumption. The optimised widths of the transistors are shown in Figure 4.4. All the parasitic elements were extracted from the layouts and back annotated in Cadence SPECTRE environment under a supply voltage of 1.8 V and a nominal temperature of 27°C. DRC (Design Rule Check) and LVS (Layout Versus Schematic) discussed in sub-section 2.3.5 were also performed. The clock frequency is set to 100 MHz. Each circuit drives an output load of 50 fF. The presented results calculated by using Waveform Calculator that is embedded in SPECTRE include delay, power consumption for different input activities, PDP, silicon area consumptions, and so on.

Figure 4.5 illustrates how power consumption changes as functions of the input switching activity, with transistor sizes (see Figure 4.4) optimized for 100% switching activity (i.e., $\alpha = 1$) for SETFFs. From Figure 4.5, the proposed SET-SEPFB noted to achieve the least power consumption for all input data activities. The Area-Power Delay Product ($\text{Area} \times \text{PDP}_{\text{CQ}}$) and Power-Delay Product with respect to t_{CQ} (PDP_{CQ}) are used as performance indicators for the circuits in comparison. Figures 4.6 and 4.7 depict the PDP_{CQ} and $\text{Area} \times \text{PDP}_{\text{CQ}}$ as a function of supply voltage, respectively. The overall performance parameters of all flip-flops discussed in this sub-section are tabulated in Table 4.2.

The design allows a 9.2% and 13.2% PDP_{DQ} reduction as compared to CDFF [46] and SEPFF [57], respectively. Apart from that, it has the smallest number of transistors amongst all flip-flops discussed. Although the delay performance of STC-EPFF [57] is 6.7% better than SET-SEPFB, proposed design contains 23.27% lesser number of transistors than STC-EPFF [57]. It can be noted from Figure 4.6 that the STC-EPFF [57]

exhibits the lowest energy consumption as a function of supply voltage. However, it can be seen from Figure 4.7 that the proposed circuit exhibits performance leverage over the other two circuits by offering a better $Area \times PDP_{CQ}$. The SEPFB is therefore a plausible solution to STC-EPFF for applications whereby area and power consumption is a prior concern rather than delay.

Figure 4.5 Power consumption for different input activities.

Figure 4.6 PDP_{CQ} versus supply voltage for 0.18 μm CMOS technology at $C_L = 50$ fF.

Figure 4.7 $\text{Area} \times PDP_{CQ}$ versus supply voltage for 0.18 μm CMOS technology at $C_L = 50$ fF.

Table 4.2. Overall Performances of CDFF [46], SEPFF [57], STC-EPFF [57] and SET-SEPFB.

Flip-Flops	Setup (ps)	Hold (ps)	t_{DQ} (ps)	P_{INT} (μW) ¹	PDP_{DQ} (fJ)	# of transistors ²	Layout Area ² (μW) ²	MOCF (GHz)
CDFF [46]	-60	380	175.9	47.2	8.3	28 (12)	107.8 (51.8)	1.2
SEPFF [57]	-50	450	381	46.7	8.6	26 (12)	96.5 (56.1)	1.18
STC-EPFF [57]	-8	250	166.9	44.5	7.4	27 (12)	103.5 (51.8)	1.42
SET-SEPFB	-55	425	179	42.6	7.6	23 (12)	83.96 (56.1)	1.21

¹ $f_{CLK} = 100$ MHz for SETFFs @ maximum data activity ($\alpha = 1$), and with $V_{DD} = 1.8$ V

²in parentheses is the physical layout area and number of transistors of the explicit single-pulsed generator (where applicable)

4.3 Explicit-Pulsed Flip-Flop using Static Latch and Dynamic Pulse Generator

Latches and flip-flops must provide low latency because of the tight timing budget in GHz operations. Power requirement is also becoming increasingly important since the power consumption increases linearly with clock frequency while the power budget of high-performance portable digital system is severely limited. In power-constrained systems, the power efficiency of latches and flip-flops is therefore pivotal [67]. As a result, it is important to trim down the power consumptions in the clock trees, latches and flip-flops.

The true-single-phase clocking (TSPC) [68], [69] has been demonstrated to be an efficient method for achieving very high-speed digital VLSI design. TSPC latches have the advantage of single-clock distribution, less clock routing area, high-speed and no clock skew. In addition, a clock signal is a global signal that must propagate through the entire clock network before reaching a transistor. Thus, the clock network must be as simple as possible, and the number of transistors controlled by the clock signal should be minimum. Based on this idea, a static level-sensitive latch utilising a two-stage non-precharged style in TSPC and a simple dynamic pulse generator to establish a low-power high-performance SETFF is proposed.

In this sub-section, a new low-power static positive level-sensitive latch as well as a simple and innovative single-pulse generator are presented. A pulse generator is engaged to be used with the proposed latch to create a low-power and high-performance single edge-triggered flip-flop (SETFF). The proposed design is a static level-sensitive latch, consists of two-stages (non-precharged type), and deploys the TSPC scheme, since TSPC latches have the advantage of single clock distribution, less clock routing area, high-speed and no clock skew.

4.3.1 Circuit Operation

The original TSPC [70] and its non-precharged version are considered to be superior in power savings [20]. There are four basic stages in TSPC: the precharged p- and n-stages, and the non-precharged (static) p- and n-stages; named PP, PN, SP, and SN stages as indicated in Figure 4.8 (a) [71]. In order to save power, the precharged node must be removed and the clock loads must be minimized. This work therefore proposed a positive level-sensitive latch utilising a two non-precharged n-stage (SN) version, and naming it the SN2-latch (see Figure. 4.8 (b)). It is a positive level-sensitive latch because the Q output reflects the input when the clock is 'high' and it works perfectly with both the 'high' and 'low' input data. In order to reduce the capacitive load at node X , a CMOS inverter, $I1$ is included to create the complement of D , for use to drive the nMOS transistor $M6$ of the second stage. The output of the first stage (i.e., node X) drives only the pull-up pMOS transistor, $M4$, and thus the 0-1 propagation delay is reduced. The first stage functions when input D is high whereas the pull-down section of the second stage operates only when the input D is set to low. When input D is logic 'high' during the latching period, X will be discharged through the pull down path $M2$ and $M3$ which implies that the pMOS transistor $M4$ of the second stage will pull the output Q to 'high'. If D is at a 'low' logic value at $CLK = \text{'high'}$, the output Q will be pulled to 'low' by the transistors $M5$ and $M6$.

Node X remains 'low' as long as input D is 'high'. SN2-latch requires no precharging at each clock cycle and the switching activity of SN2-latch is dependent on the data switching activity which tend to be much less than the clock switching activity. Moreover, the number of transistors in each pull-down path is limited to just two. Hence, the speed is improved and scaling with technology can be achieved. On top of that, the proposed latch can be constructed to an edge-triggered flip-flop by simply adding an external clock pulse generator, as in the differential CMOS pulsed flip-flop [66].

(a)

Figure 4.8 (a) Four basic TSPC stages, and (b) SN2-latch.

The transistor level implementation of the proposed flip-flop is given in Figure 4.9. A simple dynamic pulse generating circuit that produces a pulse signal at the positive edge of the clock signal was therefore created and applied externally to the proposed SN2-latch to construct a positive edge-triggered flip-flop. In the pulse-generating circuit [see Figure 4.9 (b)], a precharged n-stage (PN) is controlled by both the CLK and CLKB signals that are generated by INV1. The idea of generating a pulse signal based on TSPC PN is therefore proposed to reduce power dissipation. As the output pulse of the PN stage is negative, INV2 is engaged to convert it to a positive pulse. This complemented output pulse is to be used as a clock input to the SN2-latch. During the transparency period, which is created by the pulse generator, transistors M2 and M5 turn on, causing the input D to propagate to the output. The keepers (i.e., I2-I3 and I4-I5) are used to hold the output stages. The pulse generator determines many important parameters of the flip-flops such as setup time, hold time, clock-to-output delay and power consumption. For this reason the performance of a flip-flop is largely dependent on the design of the pulse generator. Therefore, due to advantages of innovative dynamic pulse generator that is being incorporated with novel static latch helps to achieve better performance than other flip-flops discussed in this sub-section.

Figure 4.9 TSPC based explicit-pulsed flip-flop (SN2FF): (a) SN2-latch, and (b) TSPC-PN based dynamic pulse generator.

4.3.2 Results and Comparative Study

The simulation procedure used for the assessment of the proposed design with the reported designs is the procedure discussed earlier in section 2.3. The widths of transistors are presented in Figure 4.8 and 4.9. The clock frequencies deployed for the DETFFs and the SETFFs were 50 MHz and 100 MHz respectively. The SN2-latch is first compared with the different latch designs such as TGATE latch [54] which is used as a master latch in the TGFF [54], mC²MOS latch used in mC²MOS flip-flop [34], and Differential latch utilized in static differential pulsed latch [66]. After the comprehensive evaluations of the different latch styles, various reported edge-triggered flip-flops that are based on these latches were again compared with proposed flip-flop design.

The power consumption break-ups for different input activities of latches discussed are all illustrated in Figure 4.10. The overall performances of latches are tabulated in Table 4.3 based on operating speed of 100 MHz for a V_{DD} of 1.8 V, with $C_L = 100$ fF using typical process. It is evident that the proposed SN2-latch was observed to have a considerable saving in power consumption for typical input switching activity when compared to the rest of the latches where: 28.2% saving than that of the mC²MOS-latch [34]; 31.6% saving when compared to TGATE [54]; and 46.3% less than the differential latch [66]. Furthermore, as for the PDP_{DQ} , the SN-latch is 25.6%, 56.1% and 56.9% better than TGATE [54], mC²MOS [34] and Diff latch [66], respectively.

The power consumption break-ups for different input activities of all flip-flops discussed such as TGFF [54], mC²MOS [34], Diff-FF [66] are all illustrated in Figure 4.11. The PDP_{CQ} versus different supply voltage to demonstrate the advantage of the proposed design at low supply voltage is shown in Figure 4.12. It can be seen that the proposed design has the lowest PDP_{CQ} amongst the other circuits in comparison. The overall simulation results for all flip-flops discussed in this sub-section are also tabulated in Table 4.4. It is clear from the Table 4.4 that proposed SN2FF has the lowest PDP_{CQ} when compared amongst the various flip-flop designs. This feature originates from incorporating the advantages of low-power static latch and dynamic pulse generator. As for the proposed flip-flop derived from the power efficient SN2-latch that has

incorporated the TSPC-PN based dynamic pulse generator circuit, it is able to outperform other reported works by about 51.8% to 68.1% in terms of the power-delay-product, taken with respect to the clock-to-output delay (PDP_{CQ}).

[1]-TGATE [54]; [2]-mC²MOS-latch [34]; [3]-Diff-latch [66]; [4]-SN2-latch

Figure 4.10 Latches power consumption break-ups for different input activities.

Table 4.3 Overall Performances of TGATE [54], mC²MOS-latch [34], Diff-latch [66], and SN2-latch.

Latches	t _{CQ} (ps)	t _{DQ} (ps)	P _{INT} (μW) ¹	P _{TOTAL} (μW) ¹	PDP _{DQ} (fJ)	# of Transistors
TGATE [54]	198.8	193.3	13.8	32.7	6.32	10
mC ² MOS-latch [34]	349.7	344.3	21.02	31.17	10.7	14
Diff-latch [66]	234.5	260.8	30.8	41.64	10.9	13
SN2-latch	158.2	210.4	12.17	22.37	4.7	8

¹f_{CLK} = 100 MHz @ maximum data activity (α = 1), and with V_{DD} = 1.8 V

[1]-TGFF [54]; [2]-mC²MOS [34]; [3]-Diff-FF [66]; [4]-SN2FF

Figure 4.11 Flip-flops power consumption break-ups for different input activities.

Figure 4.12 PDP_{CQ} versus supply voltage for 0.18 μm CMOS technology at $C_L = 50$ fF.

Table 4.4. Overall Performance of TGFF [54], mC²MOS [34], Diff-FF [66], and SN2FF.

Flip-Flops	Setup (ps)	Hold (ps)	t _{CQ} (ps)	P _{TOTAL} (μW) ¹	PDP _{CQ} (fJ)	# of transistors ²	Layout Area (μm) ²	MOCF (GHz)
TGFF [54]	50	10	232.3	47.62	11	18	156.7	0.9
mC ² MOS[34]	30	80.27	242.4	45.81	11.1	4	168.1	1.0
Diff-FF [66]	0	119.5	251.5	66	16.6	25 (12)	217.8	1.1
SN2FF	-124	139	112	47.24	5.3	23 (7)	180.5	1.02

¹f_{CLK} = 100 MHz for SETFFs and 50 MHz for DETFFs @ maximum data activity (α = 1), and with V_{DD} = 1.8 V

²in parentheses is referred to as the number of transistors in the pulse generator used in the circuit

4.4 Dual Supply Voltage Design using Clustered Voltage Scaling Scheme

Mobile systems that can operate for a longer period of time with limited battery capacity have been increasingly developed over time. Thus, the demand for semiconductor devices that operate at a lower voltage for use in mobile systems has escalated [72]. As such, various techniques [21] [23] have been introduced to reduce power consumption of semiconductor devices. Lowering the supply voltage results in a quadratic reduction in the power dissipation but it significantly impacts the delay. Supply voltage reduction is an effective way for reducing the power consumption of CMOS circuits. However, it is at the expense of the circuit delay. In order to lower the supply voltage without incurring system performance degradation, the clustered voltage scaling (CVS) technique [50] has been developed where the critical and non-critical paths of the designs are clustered. The use of dual supply voltages allows circuitries on the critical paths to remain operating at the original voltage, V_{DDH} , to maintain the circuit timing performance, leaving the rest of the circuits on the non-critical paths to operate at the low supply voltage, V_{DDL} , and hence achieving power reduction. In dual supply voltage circuits, when connecting a V_{DDL} supplied circuit to a V_{DDH} supplied circuit, it is necessary to insert a level converter at each low-to-high boundary, so as to function as the interface for preventing static current. To reduce the overhead of the level conversion, the low V_{DD} clusters are followed by the pipeline flip-flops, whereby the level conversion is merged with the flip-flops [50]. These flip-flops, which simultaneously perform latching and level shifting, are called level converting flip-flops [50] [51] [52].

Several level-converting flip-flops (LCFFs) have been proposed in the literature [50] [51] [52]. The clock and data inputs of a level-converting flip-flop have low voltage swing of V_{DDL} and the output has high voltage swing of V_{DDH} . However, low swing data and clock are unable to drive the pMOS transistors of the flip-flops, as they should be supplied by V_{DDH} . In order to resolve this problem, M. Hamada et.al., [50] developed the clock-level shifted sense-amplifying flip-flop (CSSA). In CSSA [50], the clock signal is level-shifted up to V_{DDH} and applied to the pMOS precharge transistor of a sense-amplifier

flip-flop [52]. The major disadvantage of this scheme is that the level shifting of the clock signal, which is always switching, can be very power consuming especially when the clock signal has very low voltage swing. In [52], H. M-Meimand and K. Roy proposed a self-precharge level converting flip-flop (SPFF) circuit that employs both the conditional capturing and self-precharging techniques to efficiently perform latching and level converting functions. The last two inverters at the output node are employed to enable self-precharge level shifted schemes, but they cause delay and power consumption overhead. Another LCFF called the pulsed half latch level conversion flip-flop (PHL) [51] has the same nMOS pass transistor level-shifting scheme that serves as the master-slave half-latch level-converting flip-flop (MSHL) [51]. In this scheme, fighting between the V_{DDH} -supplied and V_{DDL} -supplied inverter-loop level shifter is inevitable. A novel LCFF is therefore proposed to overcome this problem by employing pMOS level restore circuits instead of level shifter inverter loop. The proposed LCFF circuit is able to outperform power-delay product (PDP) value with small area feature as compared to other reported LCFFs.

This section is structured as follows. The sub-section 4.4.1 presents the operation of the new LCFF and highlights its advantages. Sub-section 4.4.2 is dedicated to the simulation comparison between the proposed LCFF and selected LCFFs.

4.4.1 Circuit Operation

As mentioned in chapter 2, the use of the dual supply voltage technique without using level converters leads to a weak turn-off of the pMOS transistor and, hence, a significant increase in the static current. The optimal CVS design relies on a level converter implemented in a flip-flop to minimize power, delay and area penalties due to level conversion. The pass-gate level converting circuit (STR1) proposed in [73] has been employed due to its smaller delay and lower power consumption. It is embedded in the latch stage to implement the LCFF. The proposed LCFF, which is shown in Figure 4.9, achieves a high-speed without compromising its power dissipation. Its fundamental concept is to avoid the threshold voltage drop at the internal node, and fighting between keeper I1 and I2 during level-shifting, so as to enhance the circuit speed.

The operation principle of the proposed design is explained here. It incorporates a True Single Phase Clock (TSPC) based pulse generator and pass gate level converting latch. The level converter proposed by S. H. Kulkarni and D. Sylvester [73] is embedded into the latch to perform level shifting. A TSPC precharged n-stage (PN) based pulse generator presented in sub-section 4.3 [see Figure 4.13 (b)] generates a pulse signal at the positive edge of the clock and is applied externally to the level-converting latch. With this implementation, the proposed LCFF is named as the pulsed pass-gate level-converting flip-flop (PPG-LCFF). In order to guarantee sufficient transparency window duration in the pulse generator, three inverters delay chain is utilized instead of just one, as illustrated in Figure 4.13. In Figure 4.13, the nMOS pass gate (M1) and M6 are driven by a pulsed clock CLK_Pulse, generated from CLK using the TSPC PN stage and the inverter delay line (I1-I3). The feedback devices M4 and M5 are used as keeper to help restore the threshold voltage drop at node $N1$.

The circuit operation is described as follows. During the transparency period, which is created by the pulse generator supplied by V_{DDL} , the clocked transistors M1 and M6, turn on. Assume initially that the output Q is 'high' and QB is 'low', the level restorer M4 and M5 both are on, causing node N1 to be pulled to V_{DDH} . In order to avoid severe leakage current flowing through a pMOS transistor M3 which is weakly turned off

by a V_{DDL} input, the output signal QB (V_{DDH} -supplied) is fed back to control the level restorer pMOS transistor M4. When the input V_{DDL} signal D is 'low' during the transparency period, M3 turns on to pull output QB to V_{DDH} and Q to go 'low'. When the input V_{DDL} signal D is 'high', pass nMOS transistor M2 is turned on, the low logic value is passed onto the output QB which causes Q to go V_{DDH} . As a result, node N1 holds a 'high' logic (V_{DDH}) value to completely turn off pMOS M3 that is supplied by V_{DDH} . Note that the proposed PPG-LCFF simultaneously performs latching and level shifting without needing extra level converting circuitries as in SPFF [52] and PHL [51]. It is worth highlighting that contrary to PHL [51], PPG encounters no fighting between V_{DDL} and V_{DDH} during level-shifting. In the case of PHL, it experiences fighting between keeper I1 and I2 during level-shifting. Therefore, the proposed circuit is able to ensure fast operation that is comparable to that of PHL [51] while avoiding its drawback.

Figure 4.13 Proposed pulsed pass-gate level-converting flip-flop (PPG-LCFF).

4.4.2 Results and Comparative Study

Extensive circuit simulations have been carried out to verify the circuit operation and characterize its performance in the vital aspects of power consumption, speed performance, transistor count, and silicon area requirement. The power consumption break-ups for different input activities is illustrated in the graph of Figure 4.14. It can be seen that the proposed PPG-LCFF consumes the least total power consumption among all LCFFs discussed regardless of the input switching activity. Figure 4.15 depicts the PDP_{CQ} at $V_{DDH} = 1.8$ V and 1.5 V. The proposed PPG-LCFF shows the second lowest energy consumption at low supply voltages. The CSSA demonstrates the worst PDP_{CQ} at $V_{DDH} = 1.5$ V due to its DCVSL style that causes large cross over fighting, resulting in large power particularly when the clock is low voltage swing. In lower supply voltage condition, proposed LCFF has the second best power consumption and best delay. The overall performances of LCFFs are tabulated in Table 4.5 at based on the clock frequency of 100 MHz for a V_{DDH} of 1.8 V and V_{DDL} of 70% of V_{DDH} and with $C_L = 50$ fF, using typical process. It is evident that the proposed LCFF can achieve substantial saving in power consumption when compared to the rest of the LCFFs where 40.6% was noted as compared to SPFF [52]; 30.8% saving than that of the CSSA [50]; and 12.4% saving when compared with PHL [52]. Furthermore, the proposed design attains 50.3% - 60.9% less PDP_{CQ} with respect to other reported works [50] [51] [52]. On top of that, the PPG-LCFF has the smallest PDP_{DQ} amongst all the LCFFs reported due to its largest negative setup time. Moreover, the results reported in Table 4.5 show that PPG-LCFF has the smallest number of transistors. Considering the high performance LCFF circuits, the lowest power dissipation is obtained with the proposed PPG. It is worthwhile to note that, in the PPG and PHL, the pulse generator can be shared among many pass gate latches to further reduce the power dissipation. A novel LCFF that permits substantial savings in power consumption, with the shortest delay, and is well suited for the critical paths in CVS designs. The PPG-LCFF yields over 61% reduction in PDP_{DQ} and about 40% improvement in power dissipation together with smallest area consumption. The PPG-LCFF also eliminates the threshold voltage drop that is noted in PHL [51] by using

pMOS level restoring devices. A further performance comparison based on the PDP shows that the proposed LCFF is the candidate of choice when power and speed are of equal design priority. In addition, the proposed design has promising usage in critical path in low-voltage system design.

[1]-CSSA [50]; [2]-SPFF [52]; [3]-PHL [51]; [4]-PPG-LCFF.

Figure 4.14 LCFFs power consumption break-ups for different input activities.

Figure 4.15 PDP_{CQ} versus supply voltage for 0.18 μm CMOS technology at $C_L = 50 \text{ fF}$.

Table 4.5. Overall performance of reported LCFFs.

LCFFs	P_{TOTAL} (μW)	t_{CQ} (ps)	t_{DQ} (ps)	Setup (ps)	PDP_{DQ} (fJ)	# of transistors	MOCF (GHz)
CSSA [50]	37.88	488	472	- 16	17.8	25	1.18
SPFF [52]	44.15	483	413	-70	18.2	32	1.07
PHL [51]	29.94	507	477	-30	14.3	23	1.2
PPG-LCFF	26.22	352	272	-80	7.1	19	1.25

4.5 Summary

One of the many important factors that affect power consumption is the choice of circuit technique for flip-flops and latches. Hence, a new low power single edge-triggered flip-flop (SETFF) that serves to eliminate unnecessary internal transitions at the internal node is first presented in this chapter. This is a pulsed latch design and is known as the output feedback flip-flop (FBFF) since it utilizes the output signal to eliminate unnecessary switching activities. The simulation results showed that for maximum input switching activity the SET-FBFF can achieve a 8.8% reduction in power dissipation when compared to CCFF [45], which has the least power dissipation amongst other SETFFs such as HLFF [55], SDFF [56] and SEPFF [57]. The improvement in power consumption is even more pronounced for zero switching activity. The important advantage of the proposed output feedback flip-flop (FBFF) is that for all different input switching activities, it provides less internal power consumption than other reported SETFFs, with no impact on its latency. Apart from that, under low supply voltage condition, the proposed FBFF has the best PDP_{CQ} as compared to its counter part designs.

Secondly, this chapter introduces a static explicit-pulsed flip-flop for low-power and high-performance applications. The design can be catered for both single- and double-edge triggering by simply replacing the explicit pulse generator. Besides, it uses static true single phase clocked (TSPC) CMOS latches together with output feedback transistor. When clocked by a single short pulse/double short pulse, the proposed flip-flop acts like a single-/double-edge triggered flip-flop respectively. In summary, the design achieves energy savings by reducing internal switching activity. Moreover, the proposed circuit exhibits performance leverage over the other three circuits, such as CDFF, SEPFF and STC-EPFF by offering a better $Area \times PDP_{CQ}$ for all different supply voltages.

Thirdly, a new low-power static positive level-sensitive latch as well as a simple and innovative single-pulse generator is also introduced. The innovative pulse generator is then used with the SN2-latch to create a low-power and high-performance single edge-triggered flip-flop (SETFF). The proposed static level-sensitive latch is of a two-stage non-precharged type, and deploys true-single-phase-clocking (TSPC) scheme. This is

because the TSPC latches have the advantage of single clock distribution, less clock routing area, high-speed and no clock skew. The SPECTRE simulation results derived for typical input activities showed that the SN2-latch can attain a maximum power saving of 46.3% when compared to other reported designs. As for the proposed flip-flop (SN2FF) derived from the proposed static latch with incorporation of the dynamic pulse generator circuit, it is able to outperform other reported works by about 51.8% to 68.1% for its power-delay-product taken with respect to the clock-to-output delay (PDP_{CQ}). In addition, the proposed SN2FF has been shown to operate the most efficiently at low supply voltages.

Finally, a novel level-converting flip-flop that incorporates pass gate level converter and true single phase clock (TSPC) based dynamic pulse generator is presented. It is evident that the proposed LCFF can achieve substantial saving in power consumption when compared to the rest of the LCFFs where 50.7% was noted as compared to SPFF [52]; 49.2% saving than that of the CSSA [50]; 20.5% saving when compared with PHL [51]. Furthermore, the proposed design achieves 45% - 64.5% less PDP_{CQ} with respect to other reported works [50] [51] [52]. The proposed PPG-LCFF shows the second lowest energy consumption at low supply voltages as well. On top of that, the PPG-LCFF has the smallest PDP_{DQ} amongst all LCFFs reported due to its largest negative setup time.

The choice of flip-flops is dependent on the application objectives but for optimal performance, it is best to use low power flip-flops throughout the system leaving high-speed flip-flops at the critical paths. The proposed flip-flops reported in this chapter outperforms other reported flip-flops in terms of performance, power and area consumption, and are therefore well suited for the major circuit paths within a design. The new designs are therefore suitable for used in low-voltage low-power CMOS VLSI/ULSI subsystem designs.

The pulsed flip-flops allow time borrowing across cycle boundaries as a result of the zero or negative setup time but suffer from large hold time requirement and master-slave flip-flops suffer from positive setup time (which reduces the performance) but eliminate the hold time violation. Due to these timing issues, the pulsed flip-flops are able to attain higher performance than their master-slave counterparts.

Chapter 5

Latch-MUX Based and Pulsed Double Edge-Triggered Flip-Flops

In this chapter, new latch-MUX based and pulsed based double edge-triggered flip-flops are introduced. A latch-MUX based DETFF utilizes TSPC split-output latch as well as basic and logic combining section (BAL) to merge the latches' outputs for realization of the DETFF configuration. The DETFF versions of the output feedback flip-flops and static explicit-pulsed flip-flop with local feedback are introduced in this chapter. This chapter is structured as follows. Section 5.1 presents the newly developed split-output TSPC based DETFF explaining how it is constructed and simulated. Comparison with conventional and other reported DETFFs are also discussed. Sections 5.2 and 5.3 describe the structures and operating principles of the two pulsed based DETFFs, respectively. In the same section, the simulated performances of new DETFFs and the flip-flops chosen for comparison circuits are all explained.

5.1 Split-Output TSPC Based Double Edge-Triggered Flip-Flop

Typically, the clock signal has to be distributed to several hundreds of thousands of the clocked storage elements (also known as flip-flops and latches). Therefore, when compared to other nodes in the design, the clock signal has the largest fan-out and hence, several levels of amplification (buffering) are necessary. As a consequence, the clock system by itself can use up to 40-50% of the power of the entire VLSI chip [74]. Within the clock system power, 90% is contributed by the flip-flops themselves as well as the last branch of the clock distribution network that is directly driving the flip-flops [16]. They are not only responsible for the correct timing, functionality, and performance of the chips, but also contribute a significant amount of the total active power to their clocked devices. Hence, simpler clocked latches and lower load capacitance of the clock tree are preferred for lower power applications. As a consequence, many techniques have recently been proposed to reduce the clock system power dissipation, including lower voltage-swing clocking schemes [75], the use of gated clocks [47], [48], and the introduction of flip-flop circuits with reduced number of clocked transistors [71].

One of the approaches amenable to high-performance as well as low-power application is the use of double edge-triggered technique. The main advantage of this approach is that the system operates at half the frequency of conventional single-edge clocking design style, while maintaining the same data throughput [77-79]. A substantial power savings in the clock distribution network can therefore be achieved.

True single phase clocking (TSPC) [68], [69] has been demonstrated to be an efficient methodology to achieve very high-speed digital VLSI design. TSPC flip-flops have the advantage of single clock distribution, less clock routing area, high-speed and no clock skew. In addition, a clock signal is a global signal that must propagate through the entire clock network before reaching a transistor. Thus, the clock network must be as simple as possible, and the number of transistors controlled by the clock signal should be minimum. DETFF based on the TSPC technique is therefore a suitable design for high-speed and low-power VLSI application.

In conventional double edge-triggered flip-flop (DETFF_{Afghahi}) [63], 20 transistors are used to implement two parallel complementary single edge-triggered flip-

flops (SETFFs), of which 8 are clocked. However, this flip-flop has unnecessary internal transitions that may lead to a substantial increase in the overall power dissipation for a constant input. Another DETFF [64] design proposed by Wang J.S, which has 18 transistors and fewer clock capacitive loading, offers a lower clock power consumption. However, the circuit suffers charge sharing at the internal nodes. In the DETFF reported by Cheng and Lin [65], a dual-pulse train generation circuit and pulse-clocked DETFF are involved. The dual-pulsed-clocked double edge-triggered flip-flop (DPC-DETFF) has fewer transistors when compared to [63] and [64]. Nonetheless, when the input is stable at high or low, it consumes a significant amount of power due to its pulse generator. Therefore, a low-power DETFF based on split-output single-phase clocked dynamic latches, with simpler circuit structure is introduced in this sub-section. On top of that, another key contribution of the proposed DETFF is the reduced loading of the clock signal since it has lesser number of clocked-transistors per flip-flop. With that, power dissipation for constant input must be minimized by reducing the number of clocked-transistors and ensuring that there are no unnecessary internal transitions. Sub-section 5.1.1 introduces the proposed circuit structure and its operation principle. The results obtained and circuits' comparisons are given in sub-section 5.1.2.

5.1.1 Circuit Operation

In the proposed latch-MUX based DETFF, 16 transistors are engaged but only 2 of which are clocked. It is based on the Latch-MUX structure and uses the split-output dynamic latches introduced in [69]. A merging circuit that utilises the Basic AND Logic Combining Section (BAL-CS) proposed by Mishra, Rofail and Yeo [79] is also involved (see Figure 5.1). The BAL-CS circuit consists of two pMOS that are connected in series to detect the common low output of the two latches, as well as two nMOS in series connected in the pull down section to detect the common high output of the two latches. In fact, it can be viewed as having a basic AND combination in the pull-up and pull-down network. The design therefore does not require clocked transistors at the MUX section, and is named split-output with basic and logic combining section, SO-BAL-

DETFF. When the clocked transistor is turned on, the split-output can be used to drive the next stage like an inverter. Detailed operation of the proposed SO-BAL-DETFF is described in the following paragraph.

The operation of the circuit can be explained via two scenarios: case (1) and case (2), where: case (1)- the input makes a high to low transition when clock is a low and a low to high transition when the clock is a high; and case (2)- the input makes a high to low transition when the clock is a high and a low to high transition when the clock is a low. The higher of the two contributes the actual power dissipation of the flip-flop. In case (1), it was assumed that both the input and the clock (CLK) are at logic 'high', and so both M1 and M2 will be in the off state, with M3 operating in the on state. At the same time, M7 and M8 are both on and M6 is off. This will cause N3 and N4 to be tied together, pulling the logic of them to be at 'low'. Hence, M9 followed by M14 will be turned on by the signal NLO ('high'). When the clock changes phase, M4 is switched on, pulling the logic of PLO to 'high'. This will turn on M13 and turn off M11, and consequently QB will be at 'low'. When the input and clk are at logic 'low', the two nodes N1 and N2 will be pulled to V_{DD} by pMOS pullup transistors M1 and M2. M5 will be switched on to pull the logic of PLO to 'low'. This will turn on transistor M11. When the CLK changes phase, N3 and N4 will be pulled to ' V_{DD} ' and ' $(V_{DD} - V_{TH})$ ', respectively, to turn on M10, setting the logic of NLO to 'low'. Since M10 is ON, M12 and M14 will be switched on and off, respectively, to raise QB to a 'high' logic level.

Similar analysis can be carried out for case (2); when the input is 'high' and clock is 'low', both M2 and M3 will operate in the 'on' state. This will cause the logic of N1 and N2 to be pulled to 'low'; however N1 will not go to V_{SS} . This is because pMOS is weak for pull down. Hence, M4 is switched 'on' to pull the signal 'PLO' to V_{DD} . This will turn on transistor M13. When the clock goes 'high', pull down transistors M7 and M8 are both 'on'. N3 and N4 will be pulled to ' V_{SS} ', to turn on M9. This will then turn on transistor M14, to cause the QB to go 'low'. When the input is 'low' and clock is 'high', nodes N3 and N4 will be pulled to V_{DD} and ' $(V_{DD} - V_{TH})$ ' respectively. This will turn on transistor M10, causing signal NLO to be pulled to 'low', to turn on M12. When the clock changes phase and the input is still at 'low', the transition will cause transistors M5

and M11 to be turn on. Consequently, QB will also be at ‘high’. Hence, both the positive latch output (PLO) and negative latch output (NLO) are able to drive the transistors in the combining section without any charge coupling problems, as compared to other DETFFs [58], [59].

Figure 5.1 Split-output latch-MIX based DETFF (SO-BAL-DETFF).

The key advantage of SO-BAL-DETFF is that it provides less clock power consumption than other reported DETFFs [63], [64], [65] for all different input switching activities. This feature originates from having reduced clocked transistors. If the incoming value remains at a high or low logic value, no internal power dissipation will occur except for the clock path. This leads to a significant power reduction especially for low input switching activities. The internal power consumption of the proposed flip-flop has strong dependency on the switching activity of the input data, and hence their advantage of low power can be exploited in applications where the data activity is inherently low. The circuit, however, has a drawback in that all the node voltages of the two latches are unable to achieve full voltage swing when the input and clock are at different logic states, i.e., low input and high clock level and vice versa. Nonetheless, their PLO and NLO signals that are of full swing can be used to drive the combining section without any charge coupling problems. In other words, this design uses two series pMOS and nMOS transistors in the basic and logic combining section and thus a slow down in the output transition as compared to [63] and [65] is inevitable.

5.1.2 Results and Comparative Study

All flip-flops considered in this Subsection have been designed up to the layout level using a single-poly, six-metal, 0.18- μm Chartered Semiconductor Manufacturing Limited CMOS process. All circuits are simulated using Cadence SPECTRE with a supply voltage of 1.8 V at a nominal temperature of 27°C. Parasitic extraction from the layouts drawing are also performed. The clock frequency used in simulations is 100 MHz. Moreover, to estimate their driving capabilities, the output is loaded with a load capacitor C_L of 50 fF. The power consumptions of the flip-flop, such as P_{INT} , P_{DATA} and P_{CLK} are measured by employing the testbench shown in Figure 2.9 during time 0 to 1 μs . As discussed in section 2.3.5, the average current flowing through the flip-flop design under test has been computed using Waveform Calculator that can be used to perform many different measurements on the waveforms displayed in the waveform window.

The proposed SO-BAL-DETFF has been simulated and compared to other reported DETFFs [63], [64], [65]. The power consumption break-ups for different input activities are also illustrated in the graph of Figure 5.2. It can be seen that SO-BAL-DETFF consumes 12% less power for the highest input switching activity and 82.4% less power for the lowest input switching activity ($\alpha = 0$ and with all 1's) as compared to DET_{Afghahi} [63]. The simulation results also showed that the proposed DETFF consumes the least clock related power. This is due to lesser clock load as compared to other reported DETFFs. As discussed in section 2.4.1, the values of PDP_{CQ} evaluated under different supply voltages are summarized in Figure 5.3. The PDP_{CQ} of proposed DETFF has lesser than that of DET_{Afghahi} for higher voltages but the trend reverses for low supply voltages due to its pMOS stack transistors at BAL section. Under low supply voltage condition, although it has the lowest power consumption, its delay is relatively higher than that of the DET_{Afghahi}. Therefore, its application for low-voltage conditions is limited and its best energy consumption is around 1.5 V. However, it is still a better choice for battery-power applications of 1.5 V V_{DD} . The Results of the simulations are shown in Table 5.1. The power dissipation presented in Table 5.1 is the higher power of the two cases, i.e., case (1) or (2), for maximum switching activities (i.e., $\alpha = 1$). As mentioned

previously, t_{DQ} is the maximum amongst the four combinations of data-to-output delay with a power that is the higher of the two cases (discussed previously in chapter 2) in Table 5.1.

The simulation results showed that the proposed design can achieve a 12% - 43.7% reduction in power dissipation for maximum input switching activity when compared to other reported designs [63], [64], [65]. With reference to area occupation, the layout of our proposed DETFF consumes 10% - 20.6% less silicon area with respect to the other presented DETFFs in [63], [64], [65]. The improvement in power consumption will be even more pronounced for zero switching activity. The power-delay-product (PDP) with respect to maximum t_{DQ} , PDP_{DQ} , is also reduced by 11.23% and 53.36% when compared to $DET_{Afgahhi}$ [63] and DET_{Wang} [64], respectively. Although the PDP_{DQ} of the BAL-SO-DETFF is 16% larger than DET_{Cheng} [65], the proposed design consumes 89.2% less power than Wang [64] when the input signal is a stable high.

The important advantage of the proposed DETFF is that it provides less clock power consumption than other reported DETFFs, for all different input switching activities. This feature originates from having reduced clocked transistors. The reduced clock power of the proposed DETFF allows for substantial power saving in clock distribution network. The advantage of low power can be exploited in applications especially those with low data switching activity. Therefore, it has promising usage in low-power applications.

[1]-DET_{Afghahi} [63], [2]-DET_{Wang} [64], [3]-DET_{Cheng} [65], [4]-SO-BAL-DETFF.

Figure 5.2 Power consumption break-ups for different input activities.

Figure 5.3 PDP_{CQ} as a function of supply voltage for 0.18 μm CMOS technology at $C_L = 50$ fF.

Table 5.1 Overall performances of DET_{Afghahi}, DET_{Wang}, DET_{Cheng}, and SO-BAL-DETFF.

DETFFs	Setup (ps)	P _{TOTAL} (μW) ¹	t _{DQ} (ps)	PDP _{DQ} (fJ)	# of transistors	Total Width (μm)	Layout Area (μm) ²	MOCF (GHz)
DET _{Afghahi} [63]	314.7	81.56	515.3	42.02	20	51.6	51.6	1.02
DET _{Wang} [64]	421.4	127.4	627.3	79.9	18	53	53	0.98
DET _{Cheng} [65]	109.7	100.66	315.2	31.7	20 (14)	47	47	1.1
SO-BAL-DETFF	314.2	71.77	520.1	37.3	16	46.6	46.6	1.0

¹f_{CLK} = 100 MHz @ maximum data activity (α = 1), and with V_{DD} = 1.8 V

5.2 Output Feedback Double Edge-Triggered Flip-Flop

As already discussed in section 4.1, the selection of a circuit style that has inherently low switching activity in the internal nodes or a small number of clocked nodes can be a good way for reducing energy. The use of conventional flip-flops such as the hybrid latch flip-flop (HLFF) [55] (see Figure 3.3) and the semidynamic flip-flop (SDFF) [56] (see Figure 3.4) are associated with considerable power consumption. One of the reasons for this is the high internal activity of the circuit even when input activity is small. Also, increased output activity due to glitches when the output is at the high level contributes to the total power dissipation. The conditional capture flip-flop (CCFF) [45] (see Figure 3.7) therefore addresses this issue to provide substantial power reductions for low input switching activities by eliminating redundant transitions of the internal precharge nodes. However, for higher switching activities, the overall power consumption of the CCFF is slightly larger than the HLFF. The static explicit-pulsed flip-flop (SEPPFF) [57] (see Figure 3.5) eliminates dynamic precharging of the pull-up transistor through the use of input data (D) instead of clock signal and this helps to reduce power dissipation especially when input D is stable. Therefore, a novel flip-flop that can eliminate the unnecessary internal transitions to minimize power dissipation regardless of its input activities, with no impact on its latency is developed in this thesis. The single edge-triggered mechanism of proposed output feedback flip-flop (SET-FBFF) was introduced in chapter 4. Sub-section 5.2.1 presents the operating principle of the double edge-triggered output feedback (DET-FBFF). A simulation results comparison between the DET-FBFF and DETFFs chosen (DE-TGPL [58] and Diff-FF [66]) are discussed in sub-section 5.2.2.

5.2.1 Circuit Operation

An efficient double edge-triggered flip-flop may be realized by replacing the single pulse generator in the single edge-triggered output feedback flip-flop (SET-FBFF) with dual pulse generator. One approach for obtaining a DET-FBFF from a SET-FBFF is to generate a transparency window after each clock edge. The simplest way to do this is to generate an XOR/XNOR logic function of the clock and delayed clock. In the proposed dual-pulse generator presented in this thesis [see Figure 5.4 (b)], the logical XOR of CLK and CLKB gives a short negative pulse after the rising and falling edges of the clock, and these negative short pulses are engaged by inverter, I5, to obtain a short positive pulse [Figure 5.4 (b)]. By applying this method to the output feedback latch, a double edge-triggered output feedback flip-flop (DET-FBFF) of Figure 5.4 can be obtained. This pulse generator may be local for each flip-flop or be shared among multiple flip-flops.

The operating principle of both the SET-FBFF (see Figure 4.1) and DET-FBFF (see Figure 5.4) are the same except for pulse generating circuitry. During the transparency windows, for input D that transits from 0-1 the first stage of the circuit will operate. As D changes from 1-0, the second stage operates. The output inverters hold the previous value of Q and QB. The operation of DET-FBFF is the same as the SET-FBFF except that DET-FBFF captures the value of the input D after both rising and falling clock transitions. As in SET-FBFF, node X will only be discharged during the transparency period, when both D and Q at high logic values. In other words, for the case of $D = Q = 1$, node X does not exercise a pre-charge-evaluation sequence at each clock cycle. Consequently, both SET-FBFF and DET-FBFF are able to eliminate redundant charging/discharging at the internal node, attaining reduced power consumption for the low input activity. Since the path from D to Q of the DET-FBFF is identical to the SET-FBFF, the latency and throughput of the DET-FBFF is the same as that of the SET-FBFF, while the clock frequency is halved. As a result, the power dissipation of DET-FBFF that engaged a local pulse generator may be significantly less than the SET-FBFF without compromising the performance.

Figure 5.4 Double edge-triggered output feedback flip-flop (DET-FBFF): (a) output feedback latch, and (b) dual pulse generator and its timing diagram.

5.2.2 Results and Comparative Study

The reported flip-flops chosen for comparison with DET-FBFF is compared against the recently reported flip-flops, DE-TGPL [58] and Diff-FF [66]. All flip-flops have been designed based on the single-poly six-metal (1P6M) Chartered Semiconductor Manufacturing Pte. Ltd at 1.8 V supply voltage. All simulations are conducted using SPECTRE simulator with the parasitic extracted from the layouts for all flip-flops discussed. The flip-flops' sizes are optimized using the sizing technique discussed in section 2.3.4 and transistors' widths are shown in Figure 5.4. The presented simulated results include delay, power consumption for different input activities, PDP, silicon area consumptions, and so on. These parameters are measured using Waveform Calculator that is included in cadence SPECTRE as discussed in section 2.3.5.

The total average power consumption is evaluated under different supply voltages and is summarized in Figure 5.5. At higher supply voltages of 1.8 V and 1.5 V, the proposed DET-FBFF has the best PDP_{CQ} when compared to other circuits in comparison. At 1.2 V V_{DD} , its total power consumption drops at a slightly lower rate and its delay rises at a much higher rate, compared to SET-FBFF due to its pass-transistor dual pulsed generator. Hence, it results in a higher energy consumption at low voltage of 1.2 V. All the flip-flops studied in this work except for SET-FBFF are unable to operate at low voltage of 0.9 V. This shows that the XOR-XNOR cells used in DET-FBFF does not scale well below 1.2 V. The characteristics of DETFFs discussed in this sub-section are tabulated in Table 5.2. The values in Table 5.2 are at 1.8 V V_{DD} . It can be seen that the proposed DET-FBFF consumes the least total power consumption among all DETFFs. With regards to PDP_{DQ} , the DET-FBFF requires about 16.3% less PDP_{DQ} when compared to the Diff-FF [66], and 22.3% less PDP_{DQ} when compared to DE-TGPL [58]. With the inclusion of the local pulse generator, both proposed designs (i.e., SET-FBFF and DET-FBFF) offer the same performances except that the DET-FBFF is able to achieve an even better power performance in that it allows 15.5% less power consumption than SET-FBFF. It should be noted that in the event of flip-flops circuitries sharing a single pulse generator, the size of the pulse generator must be larger than the

pulse generator that is engaged for use with just one flip-flop circuit. To avoid having distorted clock pulses, the flip-flops must be placed as close as possible to the single pulse generator that is to be shared among all.

Figure 5.5 PDP_{CQ} as a function of supply voltage for 0.18 μm CMOS technology at $C_L = 50\text{ fF}$.

Table 5.2. Overall Performances of DE-TGPL [58], Diff-FF [66], DET-FBFF and SET-FBFF.

Flip-Flops	Setup (ps)	Hold (ps)	t _{DQ} (ps)	P _{TOTAL} (μW) ¹	PDP _{DQ} (fJ)	# of transistors ²	Layout Area (μm) ²	MOCF (GHz)
DE-TGPL [58]	-72	130	156	71.6	11.2	20 (12)	222.2	1.1
Diff-FF [66]	0	119.5	142	73.5	10.4	23 (12)	217.8	0.87
DET-FBFF	-66	130	138	63.6	8.7	22 (8)	158.3	0.92
SET-FBFF	-56	130	138	75.3	10.4	22	160.8	1.1

¹f_{CLK} = 50 MHz @ maximum data activity (α = 1), and with V_{DD} = 1.8 V

²in parentheses is number of transistors in clock generator (where applicable)

5.3 Static Explicit-Pulsed Flip-Flop with Local Feedback

Again, static circuits, in most cases, have smaller energy consumption than dynamic circuits, because the dynamic behavior causes a lot of power to be wasted as a result of unnecessary internal switching activity, especially in moderate or lower data activity environment. A simple but innovative static explicit-pulsed single edge-triggered flip-flop (SET-SEPFB) was therefore introduced in previous chapter 4 and double edge-triggered version of SEPFB (DET-SEPFB) is presented in this section. The proposed DET-SEPFB is compared with the DETFF versions of CDFF [46], SEPFF [57] and STC-EPFF [57]. The Because of its static nature, the switching activity is dependent on the data switching activity which is usually less than the clock switching activity. The proposed circuit occupies smaller area as compared to the reported explicit-pulsed triggered designs [46] [57]. The operation principle is given in the following sub-section 5.3.1 and the performance comparisons amongst different DETFFs are presented in sub-section 5.3.2.

5.3.1 Circuit Operation

The operation principle of DET-SEPFB is the same as the SET-SEPFB (see Figure 4.4) where the input D is captured at positive edge of the clock. As already explained in sub-section 4.2.1, the dynamic precharging (i.e. static mode) of the pull-up transistor M1 through the use of D instead of the clock pulse. In this way, switching activity at node X is determined only by the input D rather than the clock CLK. Consequently, it eliminates unnecessary transitions of the internal node X . Moreover, to avoid charge coupling due to adjacent switching signals such as clock signal at node X for many consecutive high levels of D, a small-sized transistor M7 that is triggered by the output feedback signal is used. The schematic of the proposed static latch with local feedback is again presented in Figure 5.6 (a). Hence, the proposed design is named Static Explicit-Pulsed flip-flop with local Feedback (SEPFB). The double transparency window generation principle is straightforwardly applicable to SEPFB by simply changing the single pulse generator

shown earlier in Figure. 4.4 (a) with the double pulse generator [(see Figure 5.6 (a)], thus obtaining the SET-SEPFB and DET-SEPFB as in CDFF [46].

The operating principles of the single and double edge-triggered versions are the same, except for the transparency window occurs after each rising and each falling edge of the clock in the double pulse generator. When the transparency window arrives, the pull-down path of the first stage (M2-M3) responds with a 0-1 input transition, and consequently node X will switch to 'low'. As a result, the output Q is pulled to V_{DD} via pMOS transistor M4. As for the 1-0 input transition, the high level of X causes Q to go low through the pull-down path (M5-M6) of the second stage. When input D is at stable high (i.e., Q remains at high logic value), the local feedback transistor M7 keeps the value of node X low. As a result, node X will not be floating even when the clocked transistor is disabled, at outside the transparency window. Also node X will remain high as long as input D is 'low'. As mentioned in the beginning of this sub-section, the feedback transistor M7 is able to prevent having a floating at node X . Since node X does not exercise precharge-evaluate sequence in each clock cycle, the internal power consumption for low input switching activity is saved.

Figure 5.6 Static explicit-pulsed flip-flop with local feedback: (a) dual pulse generator, and (b) static latch with local feedback.

5.3.2 Results and Comparative Study

In this sub-section, the simulated performance of the DET-SEPFB is compared against some recently developed designs, such as the CDFF [46], SEPFF [57] and STC-EPFF [57] reviewed in chapter 3. All double edge-triggered versions of respective flip-flop have been designed up to the layout level using the Chartered Manufacturing Pte. Ltd 0.18- μm 1P6M n-well p-substrate CMOS process. Besides layout compaction, the author has also performed Design Rule Check (DRC) by adhering to the minimum spacing restriction to avoid design rule violations and to ensure a margin of safety in the manufacturing process. Following that, Layout Versus Schematic (LVS) verification has been carried out to guarantee that the layout drawn truthfully represents the schematic design. All the parasitic elements were extracted from the layouts and back annotated in Cadence SPECTRE environment under a supply voltage of 1.8 V and a nominal temperature of 27° C. The clock frequency is set to 50 MHz. Each circuit drives an output load of 50 fF. The presented simulated results include delay, power consumption for different input activities, PDP, silicon area consumptions, and so on are calculated using the Waveform Calculator explained in section 2.3.5.

Figure 5.7 illustrates how the power consumption changes as a function of the input switching activity, with transistor sizes optimized for 100% switching activity (i.e., $\alpha = 1$) for both single and double edge-triggered versions of flip-flops discussed. From Figures 5.7, the proposed DET-SEPFB is noted to achieve the least power consumption during high input data activities. Figure 5.8 depicts the PDP_{CQ} versus supply voltage. It shows that the proposed DETFF has the second best energy consumption amongst all flip-flops studied in this section. This is because, although it has the lowest power consumption as a function of supply voltage, its t_{CQ} is higher than that of STC-EPFF. Therefore, it can be a good candidate in low-power low-voltage applications when delay performance is not prior concern. The overall performance parameters of all flip-flops discussed in this section are tabulated in Table 5.3.

This work develops a novel static explicit-pulsed flip-flop for low-power and high-performance applications. Among the explicit-pulsed DETFF designs discussed here, the proposed DET-SEPFB is able to achieve the least power consumption for all

input activities with the smallest number of transistors, as compared to the CDFF [46], SEPFF [57] and STC-EPFF [57]. Therefore, DET-SEPFB can provide a potential power savings in the clock distribution system by using the double-edge clocking scheme.

Figure 5.7 Power consumption break-ups for different input activities.

Figure 5.8 PDP_{CQ} as a function of supply voltage for 0.18 μm CMOS technology at $C_L = 50$ fF.

Table 5.3. Overall performances of CDFF [46], SEPFF [57], STC-EPFF [57], DET-SEPFB and SET-SEPFB

DETFFs	t_{CQ} (ps)	Setup (ps)	Hold (ps)	t_{DQ} (ps)	Power (μW) ¹	PDP _{DQ} (fJ)	# of transistors [#]	Layout Area [#] (μW) ²	MOCF (GHz)
CDFF [46]	287	-30	355	199.6	45.4	9.1	28 (12)	107.8 (52.1)	0.8
SEPFF [57]	284	-23	365	176.4	44.1	7.8	26 (12)	96.5 (52.1)	1.0
STC-EPFF [57]	233	-8	235	158.4	42.2	6.7	27 (12)	103.5 (52.1)	1.13
DET- SEPFB	271	-20	398	178	40.6	7.2	23 (12)	83.96 (52.1)	0.9
SET- SEPFB	234	-55	425	179	42.6	7.6	23 (12)	83.96 (56.1)	1.21

Note: $f_{CLK} = 50$ MHz for DETFFs and 100 MHz for SETFF @ maximum data activity ($\alpha = 1$),
and with $V_{DD} = 1.8$ V

[#]In parentheses is the number transistor and layout area of the clock generator (where applicable)

5.4 Summary

In this chapter, first, a double edge-triggered flip-flop with dynamic true-single-phase-clocked (TSPC) based split-output (SO) is presented. It makes use of the basic and logic combining section (BAL) to merge the latches' outputs to realize the DETFF configuration. The main advantage of the proposed design (SO-BAL-DETFF) is the reduced loading of the clock signal and the lesser clock power consumption when compared to other reported DETFFs for all cases of input data activities. The reduced clock loading is achieved by having only two clocked transistors. The reduction in clock power of the proposed DETFF allows for a substantial power saving in the clock distribution network. Besides, the physical layout area and the total power consumption for the case of maximum input data activities are reduced by 10.1% to 20.6 % and 12% to 43.7%, respectively, when compared to other DETFFs. Apart from that, it can achieve a good performance for battery-powered applications of 1.5 V V_{DD} and able to operate at frequency of 1 GHz with current optimized sizing.

Secondly, in order to exploit the power savings due to halved clock frequency, an explicit-pulsed double edge-triggered flip-flop based on SET-FBFF presented in chapter 4 is introduced. A new low power output feedback double edge-triggered flip-flop DET-FBFF serves to eliminate unnecessary internal transitions at the internal node. An important advantage of the proposed output feedback flip-flop (FBFF) is that for all different input switching activities, it provides less internal power consumption than other reported SETFFs, with no impact on its latency. The simulation results show that the proposed DET-FBFF consumes the least total power consumption among all DETFFs. With regards to PDP_{DQ} , the DET-FBFF requires about 16.3% less PDP_{DQ} when compared to the Diff-FF [66], and 22.3% less PDP_{DQ} when compared to DE-TPGL [58]. With the inclusion of the local pulse generator, if a local pulse generator is used in each explicit-pulsed flip-flop, the total power consumption of our DET-FBFF is 9.8% - 16.8% lower than other simulated DETFFs [58] [66]. Besides that, the proposed DET-FBFF has the best PDP_{CQ} when compared to its counter part designs for supply voltages of up to 1.2 V.

Thirdly, a static explicit-pulsed double-edge triggered flip-flop version is described. The design uses static true-single-phase-clocked (TSPC) CMOS latches together with output feedback transistor. They achieve energy savings by reducing internal switching activity by taking the advantage of static structures. Its switching activity is therefore dependent on the data switching activity which tends to be less than clock switching activity. The area advantage of the proposed DET-SEPFB is exploited as compared to other explicit-pulsed triggered designs. The proposed DET-SEPFB is able to achieve the least power consumption for low input activity with the smallest area advantage of up to 17.4 %, as compared to the STC-EPFF [57]. Moreover, the results show that the proposed DETFF has the second best energy consumption amongst all other flip-flop circuits in comparison. Therefore, all-in-all the proposed designs are suitable for low-voltage applications in which low-power is a crucial important rather than delay performance.

Chapter 6

Power and Delay Sensitivity Analyses of Flip-Flops on Process, Voltage and Temperature

In this chapter, in order to thoroughly assess the robustness of the flip-flop circuits, all proposed flip-flop topologies discussed in this thesis as well as its counterpart circuits are analyzed in terms of their delay and power dependence on the process, supply voltage and temperature (PVT) variations. The main objective of this chapter is to identify the key performance parameters of flip-flop circuits that tend to be easily affected when the device or process parameters deviate from their nominal values. This is particularly important for scaled technologies and high-performance CMOS where the circuit speed is vulnerable to adverse effects caused by the reduced feature size that are imposed by increased tolerances. From the sensitivity analysis of flip-flop circuits, the designer is able to identify a suitable circuit that will present the different tradeoff choices among the performances, i.e., speed, power dissipation and robustness. On top of that, the designer will then be able to identify which parameter has the greatest impact on the circuits' performance.

6.1 Introduction

In past years, the delay uncertainty has become a fundamental aspect in the design of deep-submicronmeter (DSM) CMOS digital circuits [80]-[82]. As transistors become increasingly tiny in today CMOS generation, it is much harder to control and use for a variety of reasons. Firstly, they become increasingly vulnerable to process variations. Although this can be overcome by operating the transistors at high supply voltages, a high operating voltage is infeasible as it will degrade the reliability or even damage the transistors [83] [84]. Secondly, there is a threat posed by noise, leading to increased error rates in ICs. Thirdly, as more transistors are packed into a die, that may soon reach

several billions in a single IC, and as operating clock frequencies are increased with technology scaling, the amount of heat dissipated in an IC will approach unreasonable levels [40].

Indeed, the delay and power consumptions of logic gates and interconnects are affected by variations due to process, environmental and supply voltage. In particular, the process fluctuation introduces statistical inter-die/intra-die variations, both in the physical properties (e.g. threshold voltage) and geometries of the layers which transistors and interconnects consists of. All of which in translate into delay and power variations [85]. Environmental variations also contribute to the delay uncertainty, such as in the case of temperature that varies both in the time (according to the instantaneous power consumption) and space (due to nonuniform power consumption) domains, to affect the physical properties and hence the delay of logic gates and interconnects. The third source of delay and power sensitivities that is due to the supply voltage variations are always observed in integrated circuits (ICs). This is attributed to the time-varying voltage drops in the supply distribution network that are determined by the large currents drawn by the switching logic gates [86].

Since the operating frequencies of microprocessors doubles every year, the overheads due to timing elements such as latches and flip-flops are forming a larger fraction of the cycle time. Therefore, violations in the timing constraint of a clocked register can cause any synchronous system to malfunction. In addition, flip-flops that are commonly used as delayed cells play major roles in any digital signal processing (DSP) architecture. Not only they occupy a large portion of the silicon area, but also consume a substantial amount of power. In order to access the circuits' robustness, the delay and power sensitivities of flip-flop circuits due to the process, voltage and temperature (PVT) are carefully analyzed and evaluated in this chapter.

6.2 Impact of PVT variations on Flip-Flops Performance

Factors that mainly affect propagation delays include: temperature, supply voltage, process variations, fanout loading, and interconnect loading. And, power dissipation is dependent on the power-supply voltage, frequency of operation, internal capacitance, and output load [25]. In this sub-section, the impact of process, supply voltage and temperature variations on flip-flop circuits' performances such as timing and power are discussed. There are a number of strategies that are commonly employed to simulate the performance of an IC, at the extremes of the processing technology. In practice, conventional corner simulation involves performing simulations using two sets of device models: high and low (or fast and slow) corner models which represent the extremes of the processing technology. The advantage of corner simulation is to provide a quick answer to the designer, to determine if the circuit will function under certain process extremes. It requires only two additional simulation iterations for each situation analyzed. The process, voltage and temperature are referred to as a library variable [87] and their parameters for all process corners (i.e., typical, slow and fast) are tabulated in Table 6.1.

As explained earlier in chapter 2, the total power dissipation in CMOS digital circuits is hence expressed as the sum of the four power components:

$$P_{avg} = \alpha_T \cdot C_{load} \cdot V_{DD}^2 \cdot f_{CLK} + V_{DD} (I_{short-circuit} + I_{leakage} + I_{static}) \quad (6.1)$$

where α_T is the total activity factor of the output node, C_{load} is the total capacitance of the output node, V_{DD} is the supply voltage, f_{CLK} is the operating frequency, $I_{short-circuit}$ is the short-circuit current, $I_{leakage}$ is the leakage current and I_{static} is the static current. Amongst them, the dynamic power is the major component and is typically the dominant entity accounting for at least 84% [88] of the total power dissipation at 0.18 μm CMOS technology (see Figure 6.1). It can be noticed from Figure 6.1 [89] that, leakage power has become a major component of the total power budget of the processors developed in nanoscale CMOS technologies. Therefore, the power dissipation is mainly dependent on

the power-supply voltage, frequency of operation, internal capacitance and output load for 0.18 μm CMOS technology node.

Figure 6.1 Total power as a function of technology node [89].

To determine how the delay of digital circuit varies with operating conditions, the simple alpha-power law model [90] can be engaged.

$$t_d \approx \frac{C_L V_{DD}}{k(V_{DD} - V_{TH})^\alpha} \quad (6.2)$$

where $k \approx (\frac{W}{L})\mu_n C_{ox}$, and is the velocity saturation coefficient. From Equation (6.2), it is evident that the main factors that affect circuits' performances are the process parameters, supply voltage, temperature, fanout loading, and interconnect loading. However, in this work, only PVT variation is considered. The corner-testing PVT condition ensures that the designs work under all operating temperatures. Basically, there are two types of transistors in a CMOS process, the nMOS and pMOS transistors, foundries provide the value that from the four different corners and denoted as fast-fast (FF), slow-slow (SS), fast-slow (FS), slow-fast (SF) and typical-typical (TT). For the parameters of transistors

in the “Typical” process corner are normal. “Slow” means higher threshold voltage, lower mobility and thicker gate oxide. “Fast” means lower threshold voltage, higher mobility and thinner gate oxide. The worst-case corners include the fast or slow process, high or low temperature and high or low voltage. The corner simulation conditions are summarized in Table 6.1.

Table 6.1 Corner simulation conditions

Parameter	Minimum	Typical	Maximum
Process (P)	Slow-slow	Typical	Fast-fast
Supply voltage (V)	1.62 V	1.8 V	1.98 V
Temperature (T)	0°C	27°C	125°C

6.2.1 Process Variations

Process variations are due to variations in the manufacture conditions such as temperature, pressure and dopant concentrations [91]. ICs are produced in lots of 50 to 200 wafers with approximately 100 dice per wafer. The electrical properties in different lots can therefore be very different. There are also slighter differences in each lot and not to mention the variation in a single manufactured chip. There is bound to be variation in process parameter throughout a chip. This causes the circuits' performance to be different everywhere in a chip [92].

6.2.2 Supply Voltage Variation

In high performance synchronous digital IC, effects such as the IR drop and $L\frac{di}{dt}$ noise can effect the voltage level at the power supply [85]. Furthermore, power saving mechanisms such as clock gating and system standby that control the switching activity of large circuit blocks within an IC may also affect the power supply level [93].

6.2.3 Temperature Variations

With increasing the die area, circuit density, and on-chip power dissipation the variation of temperature across on ICs becomes significant [94] [95]. The operating temperature of a circuit block depends on the proximity to a hot spot within a die. The threshold voltage of a transistor depends on the temperature. Fluctuations in the die temperature therefore affect the device characteristics, thereby varies the performance of an IC.

6.3 Results and Discussions

In this project, extensive numerical simulations have been carried out on all the flip-flop circuits discussed using SPECTRE. Their power and delay sensitivities to the process, voltage and temperature (PVT) are evaluated. The simulations are all based on the 0.18- μm CMOS from Chartered Semiconductor Manufacturing (CHRT)'s process with load capacitance of 50 fF. The power dissipation measured is the average power consumption, P_{avg} at a clock frequency of 100 MHz and with maximum switching activity (i.e., $\alpha = 1$). The variations in t_{CQ} due to PVT variations are determined when the arrival of input data for the pulsed based flip-flop and for the master-slave/latch-MUX based flip-flop is at the zero setup time and at a relax setup time (50% of pulse width), respectively. The maximum of these two, which is the t_{CQ} , are taken as a delay metric of the flip-flop circuits. Transient analysis has also been performed on each condition, and at one at a time.

Sub-section 6.3.1 presents the results for SETFFs while the results of DETFFs are shown in sub-section 6.3.2.

6.3.1 Results on Single edge-triggered flip-flops

In this sub-section, the power and delay sensitivity analyses of SETFFs over PVT variations are evaluated. For the purpose of clarity, only representative subset of the flip-flops presented is selected for analysis of their behavior under PVT variations. Figure 6.2 (a) presents the delay sensitivities based on PVT variations of HLFF [55], SDFF [56], CCFF [44], SEPFF [57], and SET-FBFF circuits. Figure 6.2 (b) shows the percentage change in P_{avg} of HLFF [55], SDFF [56], CCFF [44], SEPFF [57], and SET-FBFF all based on the process corner conditions of Table 6.1.

It can be seen from Figure 6.2 (a) the delay is affected mainly by the process variations rather than the power. Figure 6.2 (b) shows that the variation in V_{DD} can affect the power consumption at a rate that is much greater than the rate of delay variation. This is because while the dynamic power consumption of the digital CMOS circuits is mainly proportional to the square of supply voltage V_{DD} in Equation. (6.1), the delay of the circuit is proportional to $\frac{V_{DD}}{(V_{DD} - V_{th})^\alpha}$ in Equation (6.2) [96]. Another finding is the negligible sensitivity of power to temperature variation as compared to process and supply voltage variations. However, the delay sensitivity to temperature at 125°C becomes significant as compared to the power sensitivity since the threshold voltage of a transistor depends on the temperature.

(a)

(b)

a- HLFF, b-SDFF, c-CCFF, d-SEPFF, e-SET-FBFF.

Figure 6.2 Sensitivity analysis of HLFF, SDFF, CCFF, SEPFF and SET-FBFF: (a) delay and (b) power.

As seen in Figure 6.2 (a), the HLFF [55] is the least sensitive at the slow process corner when compared to other flip-flop designs. In HLFF [55], the short pulse (i.e., transparency period) is generated by a three inverters delay chain. Other flip-flop designs such as the SDFF, SEPFF, and SET-FBFF however employ a NAND-gate to generate the short clock pulse. At fast process corner, HLFF [55] and CCFF [44] have better delay sensitivities as compared to SDFF [56], SEPFF [57], and SET-FBFF. With supply voltage variation, again HLFF [55] has the better delay uncertainty than other designs. However, for PVT variations at slow process, low voltage and at a temperature of 0°C, three designs, HLFF [55], CCFF [44] and SET-FBFF are noted to almost equal delay sensitivity and it is in contrary to the SDFF [56] and SEPFF [57]. At fast process, high voltage and at 125°C, CCFF [44] has a smallest t_{CQ} variation. The temperature variation introduces similar variations in the propagation delay of all flip-flops discussed.

It is evident from Figure 6.2 (b) that at slow process corner, the power sensitivity of SDFF [56] is the most significant as compared to other designs. It is observed that with variations in the supply voltage, the power sensitivities of the flip-flops discussed remain the same at both the high and low supply voltages. At fast process, high voltage and at a temperature of 125°C, SEPFF [57] is demonstrated the most sensitivity to variation in P_{avg} followed by the HLFF [55].

Figure 6.3 (a) presents the delay sensitivities based on the PVT variations of CDFF [46], STC-EPFF [57], and SET-FBFF designs. The effects of PVT variations on P_{avg} for CDFF [46], STC-EPFF [57], SET-FBFF, presented in Table 6.1 is plotted in Figure 6.3 (b).

As denoted in Figure 6.3 (a), the STC-EPFF [57] is the least sensitive at slow process corner as compared to CDFF [46], SET-FBFF. At fast process corner, these three flip-flops have almost equal delay uncertainty. This is because they use same pulse generator. However, the PVT variation at slow process, 1.62 V and at a 0°C, STC-EPFF [57] has showed the least variation as compared to CDFF [46] and SET-SEPFB. At fast process, 1.98 V and 125°C causes SET-SEPFB to have a slightly better t_{CQ} variation than the two flip-flops (i.e., CDFF and STC-EPFF).

From Figure 6.3 (b) which demonstrates power sensitivity at slow process corner, the CDFF [46] is seen to be the most significant as compared to STC-EPFF and SET-SEPFB which have equal power sensitivities. With supply variations, the power sensitivities of STC-EPFF and SET-SEPFB designs are the same at low supply voltage, while CDFF [46] is most sensitive when the supply voltage is reduced. At slow process, low voltage with a temperature of 0°C, SET-SEPFB is noted to have the least sensitivity to variation in P_{avg} with STC-EPFF [57] being the second sensitive. The power sensitivity of SET-SEPFB is of the least in terms of temperature variation amongst the flip-flops discussed

(a)

(b)

a- CDF, b-STC-EPFF, c-SEPFB

Figure 6.3 Sensitivity analysis of CDF, STC-EPFF, and SEPFB: (a) delay, and (b) power.

The effects of PVT variations on the delay variations of TGFF [54], C²MOS [34], Diff-FF [66], and SN2FF designs are illustrated in Figure 6.4 (a). Figure 6.4 (b) shows the percentage change in P_{avg} of TGFF [54], C²MOS [34], Diff-FF [66], and SN2FF based on the corner conditions discussed earlier in Table 6.1.

As denoted in Figure 6.4 (a), TGFF and C²MOS flip-flops are the least sensitive and SN2FF is the second least sensitive to process variations at slow process corner. With regards to supply voltage variations, C²MOS flip-flop has smallest delay uncertainty while Diff-FF has the largest delay variation and SN2FF has average delay sensitivity to supply variations amongst five flip-flop circuitries. When the supply voltage increases, three designs, SN2FF, and Diff-FF [66] have almost equal delay sensitivity than TGFF [54] and C²MOS [34]. The Diff-FF design is unable to operate over PVT variations, in particular, at slow process, low voltage and temperature at 0°C. For fast process, high voltage with 125°C causes C²MOS [34] to vary very minimally for the t_{CQ} . The temperature variation introduces similar variation in the propagation delay of the flip-flops TGFF [54], C²MOS [34], Diff-FF [66], and SN2FF.

It can be seen from Figure 6.4 (b) that the power sensitivity of SN2FF is of the least significant as compared to other designs for slow process corner. With supply variations, the power sensitivities of TGFF [54], C²MOS [34], Diff-FF [66], and SN2FF noted to vary the same at both the high and low supply voltages. Likewise, there are similar sensitivities to temperature variations for all flip-flops. As for the power variations due to changes in PVT, in particular, at slow process for 1.62 V with 0°C, again, the Diff-FF design failed to operate. The SN2FF has the least power sensitivity to the PVT corner variations.

(a)

(b)

a- TGFF, b- C^2 MOS, c-SN2FF, d-Diff-FF.

Figure 6.4 Sensitivity analysis of TGFF, C^2 MOS, SN2FF, and Diff-FF: (a) delay, and (b) power.

Figure 6.5 (a) shows the percentage change in t_{CQ} of all level converting flip-flops discussed in this thesis. They are CSSA [50], SPFF [52], PHL [51], and PPG-LCFF based on PVT corner conditions as described in Table 6.1. The power sensitivities based on PVT corner variations of LCFFs are presented in Figure 6.5 (b).

As depicted in Figure 6.5 (a), the PHL [51] is the most sensitive at slow process corner as compared to other LCFFs. At fast process corner, CSSA [50] and SPFF [52] have better delay sensitivities as compared to PHL [51] and PPG-LCFF. When the voltage is reduced, the delay variation of CSSA is noted to be the most significant whereas for PPG-LCFF, it is the least significant. At high voltage, similar variations in the propagation delay are noted in all LCFFs discussed. At 125°C, SPFF and PPG-LCFF exhibit lesser delay variations than other two LCFFs. For PVT variations at slow process, low voltage and temperature at 0°C, the variation in delay of PHL [51] is the most significant while that of CSSA is the least significant. The delay of CSSA [50] is less sensitive to PVT variations, such as at fast process, $V_{DDH} = 1.98$ V with 125°C, as compared to other LCFFs investigated.

It can be seen from Figure 6.5 (b) that the power sensitivity due to process variations is negligible as compared to the supply voltage variations. With supply variations, the power sensitivities of the flip-flops discussed are all the same at low supply voltage with PHL having the least power sensitivity at high supply voltage amongst the LCFFs reported. With regard to PVT variations whereby fast process, supply voltage of 1.98 V with 125°C cause the CSSA [50] and PPG-LCFF to have better power sensitivities as compared to SPFF [52] and PHL [51]. The PHL [51] is unable to operate at slow process with $V_{DDH} = 1.62$ V at 0°C, where CSSA demonstrated less power sensitivity than SPFF and PPG-LCFF. The power variations are similar for all LCFFs as temperature varies.

(a)

(b)

a- CSSA, b-SPFF, c-PHL, d-PPG-LCFF.

Figure 6.5 Sensitivity analysis of LCFFs: (a) delay, and (b) power.

6.3.2 Results on Double Edge-Triggered Flip-Flops

In this sub-section, the impact of PVT variations on the delay and power of DETFFs are analyzed. The operating clock frequency is fixed at 50 MHz. Figure 6.5 (a) shows the effects of the PVT variations on the delay of DET_{Afghahi} [63] DET_{Wang} [64], DET_{Cheng} [65] and SO-BAL-DETFF based on the corner conditions listed in Table 6.1. Figure 6.5 (b) presents the power sensitivities based on the PVT variations of DET_{Afghahi} [63] DET_{Wang} [64], DET_{Cheng} [65] and SO-BAL-DETFF designs. They are based on the master-slave and latch-MUX structures. The variation in t_{CQ} due to PVT variations is determined when the input data arrives at each flip-flop reaches 50% of the pulse width. The power dissipation measured is the average power consumption, P_{avg} at a clock frequency of 50 MHz, with maximum switching activity (i.e., $\alpha = 1$) and a capacitive load of 50 fF.

The $DET_{Afgahahi}$, [63] is of the least sensitive at slow process corner and SO-BAL-DETFE follows suit when comparison are made with two other DETFEs, the DET_{Wang} and DET_{Cheng} . This is demonstrated in Figure 6.6 (a). The supply voltage variation introduces similar variations in the propagation delay of $DET_{Afgahahi}$, and SO-BAL-DETFE. Likewise, DET_{Wang} and DET_{Cheng} have similar sensitivity to the supply voltage variations. At 125°C, both DET_{Wang} and DET_{Cheng} exhibit lesser delay variations than the other two DETFEs. With regard to PVT variations, $DET_{Afgahahi}$ [63] is the smallest while that of SO-BAL-DETFE is the second smallest amongst the four DETFEs introduced.

In Figure 6.6 (b), the power sensitivity due to process variations is tabulated and noted to be negligible when compared to supply voltage variation. Impact of process variations over power sensitivities of $DET_{Afgahahi}$ and DET_{Wang} are lesser than that of DET_{Cheng} and SO-BAL-DETFE. The supply voltage variation introduces similar variations in the propagation delay of $DET_{Afgahahi}$ and DET_{Wang} . And, the power sensitivities of SO-BAL-DETFE is slightly better than that of DET_{Cheng} . With regard to PVT variations at fast process with V_{DD} of 1.98 V at 125°C, power sensitivity of DET_{Wang} [64] is the smallest among four DETFEs evaluated. However, all four DETFEs have showed similar power sensitivities over the PVT variations, of slow process, at $V_{DD} = 1.62$ V and $T = 0^\circ\text{C}$. The power sensitivity due to temperature variation of $DET_{Afgahahi}$ is slightly higher when compared to the other three DETFEs investigated.

(a)

(b)

a- $DET_{Afghahi}$, b- DET_{Wang} , c- DET_{Cheng} , d- SO-BAL-DETFF.

Figure 6.6 Sensitivity analysis of $DET_{Afghahi}$, DET_{Wang} , DET_{Cheng} , and SO-BAL-DETFF:
(a) delay, and (b) power.

Figure 6.7 (a) presents the delay sensitivities based on PVT variations (see Table 6.1) of double edge-triggered versions of CDFF [46], STC-EPFF [57], DET-FBFF, DET-SEPFB, and TGPL [58] designs. The effect of PVT variations on P_{avg} of CDFF [46], STC-EPFF [57], DET-FBFF, DET-SEPFB, and TGPL [58] is given in Figure 6.7 (b).

From Figure 6.7 (a), it is evident that the DET-FBFF is the most sensitive at slow process corner as compared to other DETFFs. However, the delay sensitivity of DET-FBFF is slightly better than other DETFFs at fast process corners. With regard to the supply voltage and PVT variations at slow process corner and $V_{DD} = 1.62$ V at 0°C , the delay sensitivity of DET-FBFF is the most significant. However, it has better delay sensitivity with respect to temperature variations when compared to the other four DETFFs investigated. Both the DET-SEPFB and TGPL [58] have similar sensitivity to the supply voltage at 125°C . The PVT variation for slow process introduces similar variations in the delay of STC-EPFF [57], and DET-SEPFB whereas the CDFF [46] and TPGL [58] have similar delay sensitivity. The delay of STC-EPFF [57], and DET-SEPFB is less sensitive to the PVT variations, such that fast process with $V_{DD} = 1.98$ V at 125°C , as compared to the other DETFFs discussed.

It can be noticed from Figure 6.7 (b) that the power sensitivity due to process variations of DET-FBFF is the most significant amongst all the DETFFs investigated. And the power sensitivity of CDFF [46] is of the smallest whereas that of DET-SEPFB is the second smallest over the process variations. When the supply voltage is reduced, the power sensitivities of CDFF is noted to be slightly better and DET-FBFF is somewhat more sensitive to voltage variations when compared to that of STC-EPFF, DET-FBFF, DET-SEPFB, and TGPL. The power variations of DET-FBFF and TGPL are more sensitive than other DETFFs over the temperature variation. With regard to PVT variations at slow process and $V_{DD} = 1.62$ V at 0°C , it has the greatest impact on TGPL and DET-FBFF second sensitive amongst the five DETFFs investigated. The DET-FBFF is also the most sensitive to PVT variations at fast process corner, high voltage and high temperature conditions.

(a)

(b)

a-CDFF, b-STC-EPFF, c-DET-FBFF, d-DET-SEPFB, e-TGPL

Figure 6.7 Sensitivity analysis of CDFF, STC-EPFF, DET-FBFF, DET-SEPFB, TGPL: (a) delay, and (b) power.

6.4 Summary

Violations in the timing constraints of flip-flop circuits can cause a synchronous system to malfunction. The effects of process (P), supply voltage (V) and temperature (T) variations on the timing characteristics of flip-flops that determine the timing constraints are investigated in this chapter. Moreover, in power-constrained systems, the power efficiency of flip-flops is pivotal. Therefore, the effects of PVT variations on the flip-flops' power dissipation are also evaluated. Based on the results evaluated, all proposed flip-flops in this thesis are able to function well at all simulation conditions. However, amongst all the proposed flip-flops, the double edge-triggered version of the output feedback flip-flop (DET-FBFF) experiences the greatest sensitivity to the PVT variations. In particular, at slow process and low supply voltage. This is because DET-FBFF employed pass transistors to generate short pulses at both clock edges. Therefore, pass gates are more sensitive to PVT variations due to its threshold voltage drop. All in all, the proposed LCFF, (i.e., PPG-LCFF) is the most robust amongst all the flip-flops proposed.

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

The rapidly increasing clock frequencies have contributed directly to the clock-related power consumption of microprocessors. The power consumed by the clock can reach half of the processor power, which is growing at roughly 20% per year. Furthermore, with the growing popularity of mobile computing devices, and the advent of ubiquitous wireless networking, there has been a premium placed on low-power design methodologies. Reducing the power consumption of a design translates directly into increased battery life of the mobile device. This has led to the design of VLSI/ULSI systems of increasing complexity and increasingly restrictive power budgets.

As the performance targets in the processor market cannot be accommodated by the technology scaling only, the designers routinely resort to reducing the number of logic gates per pipeline stage, deepening the pipeline, and increasing the clock frequency. In such designs, the clocked storage elements such as flip-flops and latches used for pipeline synchronization occupy an increasingly large portion of the clock cycle and total power. There have been many successful approaches to reducing power consumption of Systems on a Chip (SoCs). This work focuses on the design methodologies to improve the performance of flip-flop designs, which encompass critical elements that execute elementary and crucial operations in any digital VLSI/ULSI designs. In this thesis, the several techniques for designing flip-flops which are feasible for achieving power saving and area efficiency, without sacrificing speed performance are thoroughly investigated. In summary, the contributions of this thesis are as follows:

- A new low-power single edge-triggered flip-flop (SETFF) that serves to eliminate unnecessary internal transitions at the internal node is presented. The important advantage of the proposed output feedback flip-flop (FBFF) is that for all different input switching activities, it provides less internal power consumption than other

reported SETFFs, with no impact on its latency. It improved significantly in terms of power consumption while promising computation speed, as verified by the extensive simulation results using the 1.8 V/0.18 μm CMOS process from Chartered Semiconductor Manufacturing Pte. Ltd. (CHRT). As for the power-delay-product (PDP_{DQ}), with regards to the data to output delay, the proposed SET-FBFF outperformed the conditional capture flip-flop (CCFF) design, which has the lowest PDP among all other contemporary SETFFs, by 8.8%. In order to exploit the power savings due to halved clock frequency, an explicit-pulsed double edge-triggered flip-flop based on SET-FBFF is also presented in this thesis, to illustrate the designs' ability to derive performances that are same as that of the single edge-triggered version, with significantly less energy consumption in the flip-flop as well as in the clock distribution network.

- A static explicit-pulsed single-/double-edge triggered flip-flops is proposed. The design uses static true-single-phase-clocked (TSPC) CMOS latches together with output feedback transistor and when clocked by a single short pulse/double short pulse acts like a single-/double-edge triggered flip-flop. It achieves energy savings by reducing internal switching activity. For the single-edge triggering, the proposed design (i.e., SET-SEPFB) is able to achieve smallest energy consumption for all input activities as compared to its counterpart flip-flop designs. As for the double-edge triggering, the DET-SEPFB offers much better performance in terms of speed while using less power for maximum or moderate input activity and less silicon area than contemporary flip-flops. Moreover, the proposed circuit exhibits performance leverage over the other three circuits, such as CDFF, SEPFF and STC-EPFF by offering a better $\text{Area} \times \text{PDP}_{\text{CQ}}$ for all different supply voltages.
- A new low-power and high-performance single edge-triggered flip-flop (SETFF) employs a static positive level-sensitive latch as well as simple and innovative single-pulse generator. The static level-sensitive latch is of a two-stage non-precharged type, and deploys true-single-phase-clocking (TSPC) scheme. This is because the TSPC latches have the advantage of single clock distribution, less clock

routing area, high-speed and no clock skew. Based on the 0.18- μm single-poly six-metal CMOS technology, the SPECTRE simulation results derived for maximum input activities showed that the proposed flip-flop (SN2FF) is able to outperform other reported works by about 51.8% to 68.1% for its power-delay-product taken with respect to the clock-to-output delay (PDP_{CQ}).

- A novel pulsed based level-converting flip-flop that incorporates pass-gate level converter and true single phase clock (TSPC) based dynamic pulse generator is also presented. The simulation results obtained using Chartered Semiconductor Manufacturing Limited 0.18- μm technology showed a 64.5% improvements in the power-delay-product (PDP_{CQ}) and 50.7% savings of power dissipation as compared to other reported works. The proposed PPG-LCFF shows the second lowest energy consumption at low supply voltages as well. The new design is therefore suitable for use in low-power and high-performance CVS designs.

- A double edge-triggered flip-flop (DETFF) with dynamic true-single-phase-clocked (TSPC) split-output (SO) is presented. It makes use of the basic and logic combining section (BAL) to merge the latches' outputs to realise the DETFF configuration. The main advantage of the proposed design (SO-BAL-DETFF) is the reduced loading of the clock signal and the lesser clock power consumption when compared to other reported DETFFs for all cases of input data activities. The reduced clock loading is achieved by having only two clocked transistors. The reduction in clock power of the proposed DETFF allows for a substantial power saving in the clock distribution network. Besides, the physical layout area and the total power consumption for the case of maximum input data activities are reduced by 10.1% to 20.6 % and 12% to 43.7% respectively when compared to other DETFFs. Apart from that, it can achieve a good performance for battery-powered applications of 1.5 V V_{DD} and able to operate at frequency of 1 GHz with current optimized sizing.

- In order to thoroughly assess the robustness of flip-flop circuits, all proposed flip-flop topologies in this thesis and its counterpart circuits are analyzed in terms of their delay and power dependence on the process, supply voltage and temperature (PVT) variations.

7.2 Recommendations for Future Research

This thesis has presented newly developed flip-flops and these circuits have shown significant Power-Delay Product (PDP) enhancement as compared to the contemporary designs. However, there are more rooms for future improvement.

First, the fabrication of a chip using proposed flip-flops in deep submicron technology should be considered in order to better understand, test, and prove the functionality of the new structure. Such a work will provide a valuable experience and at the same time observe the effects of process variations discussed in chapter 6 for the flip-flop circuits' performance.

Second, the choice of flip-flops is dependent on the applications objectives but for optimal performance, it is best to use low-power flip-flops throughout the systems leaving high-speed flip-flops at the critical paths. The further work should investigate the suitable applications that can benefit from the power and area-efficiency of the proposed flip-flops. The proposed flip-flops can be implemented into applications where it is extensively used such as the finite impulse response (FIR) filter and other DSP applications. As the number of filter taps increases, the required number of flip-flops in the pipeline stages must also increase linearly.

Third, since an economic driver for Application-Specific Integrated Circuits (ASICs) is the increasing demand for mobile and consumer devices, they are becoming part of everyday life with high usage, and hence, need to be robust. For example, a device that combines cellular telephony with a PDA is used many times during the day without

recharging. This is forcing the designers to look at power as an important metric when they design chips for these devices. Such low power designs are becoming more and more commonplace. Low-power has always been the forte of custom design methodologies. Whether in system design, process and logic selection or implementation, low-power design was handled by specialist designers using custom tools. The increased demand for mobile and consumer applications with high device integration has pressured circuit designers to adopt the faster and automated design approaches. Synthesizable ASIC designs can meet such time-to-market calls with moderate power consumption. However, to achieve low-power, various custom design approaches must be adopted and automated. The ASICs are built with a set of circuit specifications written in a standard description language such as Verilog or VHDL. A designer “synthesizes” the design from Verilog/VHDL to an IC, verifies the circuit behaviour, to finally create a circuit layout to produce an ASIC. The synthesis-based design methodology is the most widespread use in digital design today and the D-flip-flop is the basic memory element in the standard cell based design methodology for digital ICs. The further work should therefore extend the proposed flip-flops, into developing a synthesizable flip-flop for inclusion in the standard cell library, and perhaps to replace the existing flip-flop. The synthesizable flip-flop is augmented with extended voltage range characterization and cells, with an aim to achieve maximum power reduction without changing the underlying architecture nor using a specialized process technology.

Lastly, increasing process variations are posing a major challenge as CMOS technologies continue to scale deeper into the nanometer regime. Also, random fluctuations in process parameters such as t_{ox} , V_{th} and so on will cause corresponding variations in the drain current even under the same biasing conditions. These random variations in the drain current may be translated into random variations in circuit performances such as power consumption and propagation delay. In order to assess the circuit robustness at random variations, the process corner analysis performed in this dissertation can be extended to a statistical analysis (Monte Carlo simulation) using statistical process model.

Author's Publications

Journals:

- [1] M. W. Phyu, W. L. Goh, and K. S. Yeo, "High-performance output feedback flip-flop for ultra low-power applications," *International Journal of Electrical Engineering (IJEE)*, vol. 13, no. 1, pp. 41-50 (2006).
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- [4] W. L. Goh, K. S. Yeo and M. W. Phyu, "Delay and power sensitivity analysis of single edge-triggered flip-flops," submitted to *Journal of Circuits, Syst., Computers*, pending second revision.
- [5] M. W. Phyu, W. L. Goh, and K. S. Yeo, "Impact of PVT variations on double edge-triggered flip-flops power and delay: Analysis and Comparison," submitted to *IET Proc. Circuits, Devices, and Systems*.
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