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INTERFACE CHARACTERIZATION OF WAFER BONDING

SUN LINA

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Master of Engineering

2009

STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the results of original research and has not been submitted for a higher degree to any other University or Institution.

05/06/2009
Date

孙丽娜
Sun Lina

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ABSTRACT

Wafer bonding technology presents one way of fabricating power diode devices directly rather than in a semiconductor bulk. It provides an effective way with great potential for the power diode mass production. However, for practical applications of wafer bonding technique, it is important to determine the optimized process conditions to achieve good electrical performance.

In the present study, Medium Vacuum Wafer Bonding (MVWB) technique is studied. Comparing with the other wafer bonding techniques, MVWB shows advantages in many areas. Through MVWB, good bonding quality and strength can be achieved under low temperature, leading to energy saving and electrical performance improvement.

MVWB is performed successfully to fabricate PN^+ junction samples and characterization on the interface defects of the junction samples is carried out with the results presented in this work. Four main important process parameters, namely annealing temperature, annealing time, heating rate before the annealing and cooling rate at the end of annealing, are identified and investigated in the MVWB. Capacitance-voltage (C/V) profiling, current-voltage (I/V) profiling techniques and Deep-level Transient Spectroscopy (DLTS) are applied in this project for the

calculation of defect generation lifetime and determination of the activation energy as well as the density of the interface defects.

Base on the experimental results, it can be deduced that with proper experimental conditions, low defect density and high generation lifetime is achievable performance of the PN^+ junction is approaching to the ideal case.

Simulation of non-standard power diode structures has been performed using MEDICI and simulated annealing. The electrical performance has been compared among the different structures and the optimized structural parameters of different power diodes have been determined through simulated annealing. Based on the results, the Carrier Lifetime Control power diode shows excellent electrical properties and has been selected for the future work using MVWB under the optimized process condition presented in this work.

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Chapter 1 INTRODUCTION

1.1 Motivation

Wafer bonding is increasingly becoming a key technology for materials integration in various areas of microelectromechanical systems (MEMS), microoptoelectromechanical systems (MOEMS), microelectronics, optoelectronics, semiconductor-on-insulator (SOI) and displays. It is also widely used for vacuum packaging, hermetic sealing and encapsulation [1, 2].

There are numerous bonding methods and can be divided into two categories, indirect and direct bonding methods.

Using additive intermediate layer to bond two wafers together at low temperature is one of the straightforward indirect bonding methods [1]. However, the difference between the thermal expansion coefficients of the intermediate material and the substrates will induce stress upon thermal cycling. Moreover, no direct contact can

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be achieved between the two substrates, while direct material-material contact is necessary for many electrical devices.

Direct bonding methods are available, such as anodic bonding and conventional bonding. However, anodic bonding requires ionic conductivity materials and high electric field which may induce sodium ions of glass that can degrade the performance of our devices and cause serious problems; while conventional direct bonding techniques require high temperature annealing to obtain high bonding quality. Such high bonding temperature could result in some problems such as residual stress at the bonded interface due to the difference in the thermal expansion coefficients between the substrates, damage of metal electrodes on the substrates after the bonding [4], and the prevention of temperature sensitive components inclusion in the bonded wafers [5].

Direct wafer bonding in vacuum has been therefore proposed, such as bonding in ultrahigh vacuum (UHV) [6] and in low vacuum [7]. However, UHV wafer bonding requires expensive apparatus and costly process, which is not appropriate for mass-production. It also usually requires preheating ($\sim 600^{\circ}\text{C}$) of the wafers prior to bonding, or application of pressure during bonding in addition to UHV condition [3]. On the contrary, the cost-effective vacuum wafer bonding, low vacuum wafer bonding, cannot achieve very good bonding quality on the bonding strength and efficiency [7].

Therefore, medium vacuum wafer bonding (MVWB) has been explored and optimized to achieve good bonding strength and efficiency at low temperature with

shorter duration [9]. The mechanism and effects of various process parameters on the bonding quality of MVWB has been studied and illustrated into details [9]. According to the advantages such as high bonding quality that medium vacuum Si-Si wafer bonding technique can achieve, it enables the production of high performance power diode devices feasible and becomes a good option for mass production in industry.

Fig 1.1 shows the device structure of a Carrier Lifetime Control (CLC) power diode as an example of a high performance power diode, with t_5 denoting the lifetime control region. CLC (Carrier Lifetime Control) power diode is obtained by introducing recombination centers to adjust the minority carrier lifetime, leading to the reduction of the leakage current and the peak reverse recovery current. Its performance comparison with the standard power diode as computed using Medici is shown in Fig 1.2, and its superior performance of having low forward voltage, low reverse leakage current and high switching speed can be seen vividly.

Figure 1.1: Device structure of a Carrier Lifetime control power diode

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(a) V_F vs. t_{rr} for both diodes. One can see that CLC diode can have a much lower t_{rr} at lower V_F also; (b) Enlarged view of (a)

(c) Leakage current vs. t_{rr} for both diodes. One can see that the reverse leakage Current is much lower for CLC diode. The unit for the current is A/ μ m

Figure 1.2: Superior Performance of CLC diode as compared to the Standard Power Diode

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However, to fabricate CLC diode is not practical using current technology due to the high energy consumption and complex fabrication process. Therefore, it will be greatly meaningful if MVWB method can be applied to the fabrication of CLC diode. Comparing with the conventional diode fabrication process, MVWB is advantageous in both low energy consumption and process simplicity. However, design of CLC diode is not within the scope of the thesis.

With the wafer bonding technique, the energy saving of producing even the standard power diodes will be tremendous since only temperature below 400°C and duration of less than 5 hours are needed as compared to the standard fabrication process of above 1000°C and more than 30 hours of diffusion.

However, in order to ensure our wafer bonding process can indeed be applicable for power diode fabrication, electrical characterization of the bonded interface is essential. It is well known that the presence of defects has a key impact on the electrical properties of semiconductor devices. It may induce unwanted leakage current in the devices, and a reduction in the carrier lifetime and diffusion length. Having this in mind, we conducted the present research work and examine experimentally the effect of four process conditions used in the MVWB on the electrical properties of the bonded interface of a PN⁺ junction. The four process conditions are the Annealing temperature, Annealing time, Heating rate before the annealing, Cooling rate at the end of annealing. The wafer bonding process of PN junction diodes includes two main parts, i.e. wafer bonding in air and the following annealing process carried out in vacuum furnace. The first part has been optimized

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and published by Assoc. Prof Tan Cher Ming. [73] For the second part, furthermore investigation of the process conditions was needed to make it more suitable for industrial production. The annealing process can be divided into three sub-parts, heating of the bonded wafers, annealing at constant temperature and cooling down of the bonded wafers at the end of the overall annealing process. Therefore, the main four affecting parameters, annealing time, annealing temperature, heating rate and cooling rate, are selected for bonding interface defects characterization.

C/V and I/V profiling is applied to all the PN^+ junction samples to calculate the generation lifetime for the investigation on the effect of the experimental conditions on the properties of the interface defects. DLTS analysis is also applied for the identification of defects and its density.

1.2 Objectives

The main objectives of this work are as follows:

1. Compare the electrical performance of non-standard power diode structures by simulation and select the structure with best electrical behaviour for the future mass-production.

For mass production, besides high electrical performance, sensitivity of structure and doping parameters of the diode with respect to inherent process variations must also be examined to evaluate its practicality and manufacturability. High sensitivity generally implies that the diode design is non-manufacturable at a reasonable cost and yield.

2. Study the effect of the four experimental process conditions on the bonding interface defects and the electrical performance of the PN junction diode devices fabricated.

1.3 Contributions of this thesis

The major contribution of the thesis covers the following aspects:

1. Low temperature MVWB is performed successfully, and the performance of the fabricated devices is improved dramatically through experimental conditions investigation. The two important parameters are found to be annealing temperature and annealing time.
2. Effects of the important experimental parameters on the interface defects are investigated through different techniques. Activation energy and density of the defects is also obtained and presented in our work.
3. Systematic study of the electrical performance of different non-standard power devices has been carried out in this project. Simulation on non-standard power devices is performed using MEDICI and simulated annealing. DOE is applied for analyzing the relationship between the electrical behaviors of devices and their structure parameters. MEDICI has been a proven method to simulate electrical behavior for high voltage power rectifier structures and has been applied widely in electrical devices modeling [10, 74-76]. However, currently there is no measured data available because the adopted structure with the specific doping parameters in the simulation has not been fabricated as it is not within this project's scope. Device with optimized structure parameters will be fabricated in the future.

1.4 Organization of this thesis

The thesis is organized in six chapters.

Chapter one is the introduction of the thesis, including motivation, objectives, contribution and organization. The literature reviews of non-standard power devices and wafer bonding technology are presented in chapter two. Chapter three presents the comparative study of non-standard power diodes using MEDICI and simulated annealing. The experimental procedure of MVWB is presented in chapter four. The instruments and characterization methods used in present work are also introduced in this chapter. Chapter five is devoted to the analysis of the effects of experimental conditions on the electrical performance of the PN junction fabricated using MVWB. The generation lifetime, activation energy and defect density is presented in this chapter. Finally, chapter 6 summarizes the results in this work and gives recommendation for future work.

Chapter 2 LITERATURE REVIEW

In this chapter, a brief introduction on various non-standard power diodes and a review on the development of wafer bonding technology will be presented.

2.1 Development of Non-standard Power Diode

Structures

The quest for faster switching, lower forward voltage drop and higher reverse blocking voltage in power diodes has been on-going for more than a decade and it is becoming more crucial as most of the other power semiconductor devices are able to achieve high switching speed and low loss operation. The difficulty in achieving the required high performance for power diodes stems from its simple device structure such that all the electrical performances of a diode are closely linked to one another through just a few device structural and doping parameters. As a result, extensive device simulation combined with statistical optimization

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algorithms is required to optimize the electrical performance parameters of the diode.

Various non-standard power diode structures have been proposed in the past based on different principles in order to optimize its electrical performance parameters. From the understanding of the device physics of power diodes, three main principles are employed in order to achieve high diode performance, namely the drift region control method, carrier injection method and carrier lifetime control method [10].

BUFFER diode structure was first reported in 1981 [11], in which the drift region control technique was employed. A lightly doped N^- layer is inserted between the P^+ and N layers of a standard diode. This N^- layer helps in achieving softer recovery, high punchthrough voltage and reduced voltage spikes. Subsequently, the SPEED (Self-Adjusting P-Emitter Efficiency Diode) structure was proposed using the carrier injection (emitter efficiency) control method [10,12] in which a thick lightly-doped p-emitter region is integrated with highly doped P^+ region pockets at the surface. This structure improves the reverse recovery characteristics, reduces forward voltage drop and maintains a high reverse blocking voltage. Lastly, the CLC (Carrier Lifetime Control) method to engineer the minority carrier lifetime profile in a diode so as to reduce the leakage current, turnoff time and the peak reverse recovery current was developed [13,14].

Although the non-standard power diode structures mentioned above generally perform better than the standard power diode, not all the electrical parameters of

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these diodes can be optimized at the same time. While a few parameters are optimized, others might be more degraded as compared to the standard diode. It is therefore necessary to span the large parameter space of the possible range of values for the structural and doping parameters in order to determine the optimal value of the electrical parameters in each device and investigate the practicality of their implementation with respect to the values of the other non-optimized parameters. Furthermore, the sensitivity of the optimized parameters with respect to inherent process variations of power diode manufacturing must be examined in order to assess its manufacturability. In general, a high sensitivity implies that the diodes are non-manufacturable at a reasonable cost and yield. It is the purpose of this work to explore the practicality and manufacturability of the various power diode structures in comparison to the simple conventional standard diode structure.

MEDICI device simulator [15] is employed in this work. Design of Experiment methodology (DOE) is used to examine the large parameter space effectively and Simulated Annealing (SA) algorithm is applied to determine the optimal values of the electrical parameters of the diodes.

2.2 Wafer Bonding Technique

Wafer bonding generally refers to a process by which two wafers fuse and adhere to each other if they are put into close contact. Since the first systematic investigation performed in 1936 by Rayleigh on room temperature adhesion between two optically polished glass plates [16], the topic of wafer bonding technique has been studied for several decades. Widespread attention in modern wafer bonding techniques was attracted with the report on silicon-silicon wafer bonding for silicon-on-insulator structure by two groups [17, 18] in 1986, in which a high-temperature bond-strengthening heat treatment was performed after the initial bonding of the two wafers at room temperature.

With the development of a number of new techniques and devices, such as high performance microelectronics (e.g. high performance partially depleted and fully depleted CMOS [19], double gate CMOS [20, 21], and 3D device integration [22]), photonics and optoelectronics [23], and Microelectromechanical systems (MEMS) [24, 25], wafer bonding technique has been gaining more and more interest and becoming more popular recently. Moreover, the capability of layering dissimilar materials makes it possible to integrate devices on a single chip by applying wafer bonding techniques.

2.2.1 Categories of wafer bonding techniques

Various wafer bonding techniques have been developed based on different procedure and applications, and can be generally divided into three categories:

1) Direct bonding (fusion bonding)

Without the assistance of any significant pressure, electrical fields or intermediate layers [1], two wafers are contacted directly, leading to strong bond adhesion between the two bonded wafers. This bonding technique is widely used in the SOI technology.

2) Anodic bonding

This technique is based on the joining of an electrical conducting material (e.g. silicon) together with an ionic conductive material (e.g. alkali-containing glass) [2, 3]. Strong and hermetic bonds can be achieved using this technique and therefore, anodic bonding is commonly used for micro-sensor fabrication and hermetic sealing of micromachined devices.

3) Intermediate layer bonding

In recent years, materials such as metal, glass and organic compounds of variable thickness have been reported to be used as intermediate layers in low temperature bonding methods [26, 27, 28]. This kind of bonding technique has been widely used in some special fields, such as optically pumped VCSELs

[29] and chemical analysis devices [30] because of its low requirement on the bonding surface topography and the environment of cleanroom.

In our work, direct wafer bonding technique is selected for the fabricate of PN junction diode for interface characterization, as well as CLC diode in the future work, for its advantages on the possibility of thicker and better silicon quality (work layer) with lower defect density at the bonding interface comparing with the epitaxial grown substrate technique, and suitability for industrial mass production. Thus, direct wafer bonding technique will be discussed in details in the next section.

2.2.2 Direct wafer bonding process

As direct wafer bonding is applied in this work, the term wafer bonding throughout the thesis will be referring to direct wafer bonding unless otherwise stated.

A standard silicon wafer bonding fabrication process flow is illustrated in Fig 2.1. The process is generally accomplished by four basic steps. Firstly, the surface of the wafer is prepared for bonding. Then the two mating wafers are brought into contact face to face at room temperature with or without any applied force. The bonding is usually initialized by pressing slightly at one point of the wafer edge to squeeze out the trapped air, then the bonded area spreads laterally over the entire wafer area, typically in a few seconds. Comparing with the metallic, covalent, or ionically bonded solids, the bonding strength achieved at room temperature is usually relatively weak. Therefore, to fulfill the requirement of most of the applications, a heat treatment is applied after the wafers are bonded at room

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temperature to strengthen the bonds across the interface. Normally one of the wafers is then thinned to a thickness in the range of several micros down to a couple of nanometers depending on the special needs. More details of the silicon wafer bonding process will be presented in the sequent sections.

Based on different mechanisms, there are two distinct kinds of wafer bonding, namely the hydrophilic and hydrophobic wafer bonding [1]. In our work, only hydrophilic wafer bonding will be discussed because hydrophilic wafer bonding at low temperature will be able to achieve better bonding quality [1].

Figure 2.1: Schematic diagram of wafer bonding process flow

2.2.2.1 Requirement of initial wafers

It is well known that the forces involved in wafer bonding are mainly short-range intermolecular forces, such as Van der Waals forces, electrostatic Coulombic

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forces and capillary forces [18]. Therefore, for successful bonding, adequate smoothness, flatness and cleanliness of the bonding surface, as well as the hydrophilicity of the mating wafer surface are essential.

Physical quality of the as-bonded wafers plays a key role in determining the quality of wafer bonding, and it can be commonly described using two parameters, *surface flatness* and *micro-roughness*.

Surface flatness is a global, macroscopic measure of the deviation of the front side of the wafer from a specified reference plane when the backside of the wafer is considered to be ideally flat, as when the wafer is sucked onto an ideally clean, flat vacuum chuck. Total thickness variation (TTV) is used to describe the surface flatness here, which is the discrepancy between the highest and lowest elevation of the front side of the wafer.

During the bonding process at room temperature, both wafers will be elastically deformed to achieve conformity of the two surfaces. Therefore, the non-uniform starting wafers may result in periodic strain patterns (contrast fluctuations) corresponding to typical spatial frequencies of the bonded pair. If the level of the flatness non-uniformity is too high and beyond the limitation, unbonded areas may be resulted.

Micro-roughness is a local, microscopic parameter of wafer surface quality that is crucial in wafer bonding. It is usually characterized by a value of root mean square (RMS), abbreviated as R_q , measured by using scanning tunneling microscopy

(STM) and AFM (atomic force microscopy). It has been demonstrated experimentally that for silicon wafer bonding at room temperature via hydrogen bonds, surface roughness less than 5 Å is tolerable [31]. This value is typical for commercially available prime grade bulk silicon wafers while surface average roughness less than 1 Å is also achievable [1].

Practically both pure mechanical polishing and chemical-mechanical-polishing (CMP) can achieve a high degree of flatness, parallelism and smoothness of silicon and silica glass pieces. But pure mechanical polishing may introduce a significant subsurface damage layer of ~20 µm in depth. Therefore, CMP is preferred in wafer bonding for the wafer surface polishing [1].

2.2.2.2 Surface cleaning

Clean wafer surface that is free of particulate, organic, and metallic contamination is also highly demanded in wafer bonding. This is crucial because the surface cleanliness will affect both the structural and electrical properties of the bonding interfaces directly and therefore, the electrical properties of the bonded materials as well [1].

The surface cleaning techniques adopted must be able to remove all the contaminations on the wafer surface without degrading its smoothness. Wet-chemistry wafer cleaning technique commonly used in the semiconductor industry is fully applicable to wafer bonding and therefore, employed in the wafer bonding technology. Hydrogen-peroxide-based “RCA” wet cleans are most commonly

applied in wafer bonding as well as in the semiconductor industry. The silicon wafer surfaces usually are terminated by hydroxyl (OH) groups after standard RCA cleaning ($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_4\text{OH} = 5:1:1$), and are called hydrophilic surfaces [32]. The existence of hydroxyl groups on the hydrophilic wafer surfaces has already been verified by infrared spectroscopy measurements [39].

2.2.2.3 Surface activation

It is well known that Van der Waals dispersion force is ubiquitous and is applicable to almost all substances that are in intimate contact (so-called optical contact). Generally speaking, any two solid-state plates of almost any material can bond to each other at room temperature provided that their surfaces are sufficiently flat and clean to achieve optical contact and therefore, Van der Waals forces that are sufficiently strong among the surface molecules of the two plates (sometimes only after some local elastic or plastic deformation of the solid). In practice, producing an optically smooth and flat surface can be very costly, and is hardly possible for some materials. Therefore, a reactive bonding surface would be highly desirable to alleviate the requirement on surface smoothness.

2.2.2.4 Annealing

To enhance the bonding interface adhesion, the water molecules at the interface must be removed by dissolving into the surrounding materials or diffusing out of the interface in order to promote the condensation reaction between the OH groups shown as follows:

The reaction starts immediately at room temperature when the wafers are in sufficient proximity [34]. However, at temperature below 425°C, the above reaction is reversible and most of the covalent Si-O-Si bonds cannot remain at the bonding interface with the existence of water. Even at temperature higher than 425°C, there are still some water molecules and OH groups at the bonding interface. To make the bonding energy reach the bulk fracture energy level, an annealing, typically at higher than 800°C for hydrophilic Si/Si bonding, is necessary to remove the remaining water molecules and to fill up the interface microgaps by means of viscous flow of the native oxide [35]. The details of annealing are in the section of “conventional wafer bonding mechanism”.

2.2.3 Conventional wafer bonding mechanism

For conventional wafer bonding, which is hydrophilic, the bonding at room temperature is caused by hydrogen bonds between the chemisorbed water molecules on the opposing wafer surfaces. To form stronger Si-O-Si bonds, the hydrogen bonds between two wafer surfaces have to be broken up in order to allow the silanol groups to react with each other. During the process, high temperature annealing is desired to enhance the diffusion of the absorbed and produced water [36] as seen in Fig. 2.2. A detailed bonding model of conventional silicon described by Tong et. al. [1] is widely accepted.

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Figure 2.2: Proposed bonding model for hydrophilic Si wafer bonding at different temperature. (a) Room temperature~110°C: Formation of stable hydrogen bonding between molecular water across the bonding interface. (b) 110~150°C: Removal of interface molecular water and formation of siloxane bonds. (c) 150~800°C: Stable siloxane bonds. (d) >800°C: Viscous flow of interface oxide [1].

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For hydrophilic wafer bonding, the annealing period can be divided into four stages as shown in Fig. 2.2:

i) From room temperature to 110°C: slow fracture effect and interface water rearrangement.

During room-temperature bonding, the two wafers bond to each other via hydrogen bonding between the absorbed water molecules on the two surfaces. The linkage of two or three water molecules can form a bridge across the two bonding surfaces. All or most of the molecular water can only be removed from the surfaces upon heating above 120°C in air [37, 38], while no significant effect during annealing from room temperature to 110°C. Since the water film structure exists at this stage [37], the main interface reactions in this temperature range should be : (a) The slow fracture effect of Si-O-Si bonds on both surfaces via attack by the water molecules [37], i.e. the reverse reaction (2.1); (b) Rearrangement of the interface water molecules to form more stable hydrogen-bonded structures. The reactions are both time and temperature dependent. An increased density of silanol groups at the interface will result in the enhancement of bonding energy.

ii) From 110 to 150°C: condensation of silanol groups across the interface.

When the interface is drying gradually during annealing at >110°C, some of the molecular water diffuses along the bonding interface to the ambient, while some water modules will diffuse through the surrounding native oxide and react with Si

to from SiO_2 and hydrogen [1, 38]. Thus, the forward reaction of reaction (2.1) will readily occur and more Si-O-Si groups between two surfaces will be produced. The oxide formed contributes to close the interface microgaps. The formation of strong siloxane bonds at the interface results in a rapid increase in surface energy of the bonded pair.

iii) From 150 to 800°C: bonding energy limited by contacted area.

It is believed that almost all silanol groups in the real contacted areas can be converted to siloxane bonds at $\sim 150^\circ\text{C}$ [37]. From 150 to 800°C, the surface energy of the bonded pairs has reached the value determined by the contacted area at the interface over which all silanol groups at the interface have converted to siloxane bonds. However, because the bonding surfaces are never perfectly smooth, the area over which the conversion really occurs is limited. Besides, inert gases such as nitrogen trapped in nanocavities formed due to the micro-roughness of the two bonded surfaces may prevent the formation of siloxane bonds. Therefore, to get fully bonded wafer pair, higher temperature annealing is required.

iv) From 800°C to above: complete bonding via oxide flow.

For hydrophilic Si/Si pairs, annealing at temperature higher than 800°C is sufficient to increase the contact area at the interface by means of viscous flow of the oxide which is to fill up the interface microgaps and to form more siloxane bonds. After being annealed for sufficient duration, completed bonded wafer pair may be achieved.

2.2.4 Low temperature wafer bonding

The bonding strength of wafer bonding at room temperature in air is usually very weak because it is the Van der Waals force and hydrogen bond that is acting [40]. This bonding strength is not strong enough to enable the bonded wafer pairs to sustain further processing such as lapping, thinning and patterning. Therefore, it is essential for the bonded wafer pairs to be annealed at elevated temperature after the room temperature bonding in order to enhance the bonding strength. However, the high temperature post-annealing applied in the bonding process may limit the application areas of wafer bonding due to the following problems that may occur [41, 42].

- i) Thermal induced mechanical stress in bonding of materials with different thermal expansion coefficients;
- ii) Undesirable changes and reactions in the case of materials and structures which are sensitive to high temperature;
- iii) The occurrence of precipitates of oxides and vacancies at the bonded interface during the heat treatment.

Due to the problems mentioned above, it is crucial to achieve strong bonding strength through low temperature annealing. Up to now, there are a number of studies done which are aiming at the development of effective methods that can yield strong bonding strength at low temperature or even at room temperature [6-8, 43-48].

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One of the effective approaches is to activate the wafer surfaces using dry or wet methods after cleaning and before room temperature bonding. In some cases, the cleaning and activation processes are combined in which the bonding surfaces can be activated by cleaning treatment such as RCA cleaning. A DHF solution treatment to enhance the low temperature bonding energy of thermal oxide covered wafer bonding has been reported [46]. It was also found that surface activation done by dipping the wafers into hot nitric acid [47], or hot NH_4OH solution [48] can effectively enhance the bonding strength at low temperature comparing with the treatment using only standard RCA solution.

Plasma exposure treatment on wafer surface is also able to enhance the bonding energy at the bonding interface [43-45]. An amorphous surface layer on silicon wafers prepared by As^+ ion implantation, or thin film sputtering deposition, is proved to be very effective in enhancing the bonding energy [46].

Vacuum wafer bonding is another effective approach to achieve high bonding strength at low temperature. Tong et. al. [7] demonstrated the improvement of the bonding strength at low temperature by applying low vacuum. It is believed that the out-diffusion of water and inert gas trapped at the interface is the main cause of the improvement, which is accelerated under low vacuum condition at low temperature. Bonding conducted under ultra-high vacuum (UHV) is also very attractive for bonding wafers without native oxide [6]. For in situ bonded pair of thermally cleaned hydrophobic silicon wafers under UHV, covalent bonds have been achieved at room temperature [6]. Very strong bonding strength has also been

achieved at room temperature for silicon and gallium wafers cleaned and activated using argon fast atom beam under UHV and in situ bonded under an external pressure [49]. But UHV wafer bonding technique usually requires the wafers to go through a preheating process ($\sim 600^{\circ}\text{C}$) prior to bonding, or be applied a pressure during bonding besides UHV. It is too costly to apply this technique to the industrial mass production [2].

Because of the simplicity and evident improvement of bonding strength at low temperature, vacuum wafer bonding were chosen as wafer bonding methods in this work.

2.2.5 Bonding interface imaging

The bonding quality of a bonded wafer pair is commonly described in terms of bonding efficiency and bonding strength. Bonding efficiency is expressed as the percentage of the bonded area over the entire wafer area, and is usually measured from the scanning image of the bonding interface. Bonding strength is another important parameter obtained by determining the tensile strength or surface energy of the bonding interface. A number of nondestructive and destructive techniques are used to characterize the bonding quality.

Both of bonding efficiency and bonding strength for medium vacuum wafer bonding have been evaluated and published by Prof. Tan Cher Ming in his paper [78]. In this paper, the effect of the experimental conditions on bonding efficiency and strength has been discussed and summarized based on experimental results. In

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the paper, both pull test and acoustic microscopy method has been induced for the examination of bonding efficiency and bonding strength.

One of the most serious problems occur in wafer bonding is the formation of unbonded area, also named as interfacial bubble. The causes for the formation of interfacial bubble can be large Total Thickness Variation (TTV) and micro-roughness of the wafer surfaces, residual particles, air trapped at the interface, as well as insufficient density of bonding species.

Total Thickness Variation (TTV) is a global parameter to describe the overall flatness of wafer surface, which is the discrepancy between the highest and lowest elevation of the front side of the wafer.

Figure 2.3: TTV measurement schematic diagram

Figure 2.3 above [77] shows a wafer placed between two non-contact measurement probes. By monitoring changes between the upper probe face and the upper wafer surface (A) and the bottom probe face and the bottom wafer surface (B), thickness can be calculated.

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First the system must be calibrated with a wafer on known thickness (T_w). The area of known thickness is placed between the probes and an upper probe to wafer gap (A) and a lower probe to wafer gap (B) is acquired. The total gap (G_{total}) between the upper and lower probes is then calculated as follows [77]:

$$G_{total} = A + B + T_w \quad (2.2)$$

With the system calibrated, wafers of unknown thickness can now be measured. When the wafer is placed between the probes, a new value of A and B is acquired. Thickness is calculated as follows [77]:

$$T_w = G_{total} - (A + B) \quad (2.3)$$

Figure 2.4: Example of thickness vs wafer location 2D graph

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During an automated scanning of the wafer, a series of point measurements (shown in the figure above) is taken and stored. Following completion of the scan, TTV is calculated as follows [77]:

$$TTV = T_{\max} - T_{\min} \quad (2.4)$$

There are several commonly used imaging techniques available for measuring the interface bubbles for wafer bonding, such as optical microscopy, X-ray topography, acoustic microscopy, interface etching and cross-sectional analysis [1].

Optical microscopy: It is inexpensive, efficient and especially useful to use optical microscopy in adhesive wafer bonding since the bonding defects in adhesive wafer bonding are usually not very dependent on the wafer materials. However, this method requires at least one of the bonded wafers is transparent to visible light (e.g. a glass wafer), which means it is not suitable for characterization of the bonded wafers consisting of nontransparent materials.

X-ray topography: This method is used to obtain an image of the deviations from ideal and undistorted lattice planes, and it can only be applied to single crystalline materials. X-ray topography has a typical spatial resolution of 2-20 μm , but is comparably expensive and time-consuming.

Acoustic microscopy: This technique makes use of the fact that acoustic waves can propagate through solid-state materials. The changes of the elastic properties of

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the materials will vary the scattering of acoustic waves and thus make it possible to detect the voids and defects at bonding interface. Ultrasonic waves first encounter an interface between the two materials when introduced, where they are partly reflected and partly transmitted. If without defects, the only reflections one can record are those from the front and the back of the piece. But if a defect is encountered, the wave will be reflected at that local interface and an echo will show on the oscilloscope. Depending on the frequency range adopted, the resolution of acoustic microscopy can reach up to 10 μm . Acoustic microscopy measurements are easy to operate, fast and applicable to almost all materials.

Interface etching: One of the bonded wafers has to be sacrificially etched to a thin etch-stop layer while using interface etching. Voids and defects can then be visually inspected through the thin etch-stop layer using optical microscopy. If larger defects are present at the bonding interface, the etch-stop layer may buckle or burst open, indicating the unbonded areas. For silicon wafers, the interface etching can be performed using wet etching or deep reactive ion etching (DRIE), in which SiO_2 can be used as the etch-stop layer.

Cross-sectional analysis: This is done by cleaving or dicing a bonded wafer pair perpendicular to the bonding interface. The cross-section of the bonding interface can then be inspected using optical microscopy or scanning electron microscopy (SEM). In some cases, the cross-sections of the diced samples must be polished in order to obtain clear image of the bonding interface. This technique is especially

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useful for the inspection of bonding with thin intermediate bonding materials such as adhesives.

In this work, acoustic microscope is used. Optical microscopy is not applicable because SiO_2 wafer is used and it is not transparent to visible light. X-ray topography isn't selected because it is expensive and time-consuming. Last two methods, interface etching and cross-sectional analysis aren't used as a result of the destruction they cause to the samples, leading to their inapplicability for the following characterization.

2.3 Defects at the Bonding Interface

It is well known that the presence of defects has a key impact on the electrical properties of semiconductor devices. It may induce unwanted leakage current in the devices, and a reduction in the carrier lifetime and diffusion length. In this work, the effect of different experimental conditions on the interface defects of PN junction structure fabricated by using the Medium Vacuum Wafer Bonding technique will be studied.

2.3.1 Defects

The interface of directly bonded silicon wafers is generally not perfect as defects always exist in semiconductors. The defects can be structural or transient defects. In the former case, the correct arrangement of atoms in real crystals is permanently altered, whereas transient defects are elementary excitations such as phonons (i.e., quanta of lattice vibrational energy) [50]. The structural defects will be the focus in this project, which may be foreign atoms (impurities) or crystalline defects.

2.3.1.1 Impurities

Impurities can be divided into shallow-level and deep-level impurities. Shallow-level impurities are generally referring to the dopant atoms introduced intentionally. Deep-level impurities are those electrically active non-dopant impurities that have energy levels in the forbidden energy gap. The term “deep-level” comes from their energy levels that are generally quite far removed from the

band edges. The deep-level impurities play an important role in introducing recombination/generation centers to reduce the silicon device lifetime even at densities as low as 10^{10} atoms/cm³ [51]. Moreover, the introduction of deep-level impurities can also increase the substrate resistivity at relatively higher densities.

2.3.1.2 Crystalline defects

Native crystalline atomic defects include vacancies, empty lattice sites, interstitials, excess atoms present in the lattice, and antistructure defects. Native atomic defects can be divided into two categories, *bulk* and *surface defect*, while the latter one is of our research focus.

Surface defects structures include point defects and line defects. Point defects are also called zero-dimensional defects, including adatom, vacancy, adatom island, and vacancy island. Line defects are one-dimensional defects, such as dislocations.

Vacancy refers to point defect in a crystal wherein an atom, such as Si, is missing from one of the sites. An isolated vacancy in the lattice is termed as Schottky defect, while a vacancy associated with an interstitial atom (i.e. vacancy-interstitial pair) is referred to as a Frenkel defect. Adatom is an atom that lies on a crystal surface, and can be thought of as opposite to a surface vacancy. Adatom island refers to interstitial cluster on a surface. Vacancy island is vacancy cluster on a surface.

Figure 2.5: Simple native and foreign point defects (took from wikipedia)

Dislocations include edge dislocation and screw dislocation. In real situation, the dislocation is generally mixed of these two. Fig 2.6 below shows the edge and screw dislocations (took from wikipedia).

Figure 2.6: Types of dislocations (a) Edge dislocation (b) Screw dislocation

2.3.1.3 Oxygen-precipitation induced extended defects

Silicon crystals grown by the Czochralski method typically contain between 5×10^{17} and 10^{18} cm^{-3} dissolved oxygen atoms. As a result of the observed fact that the amount of oxygen and its radial and axial distribution has a direct impact on the yield of devices and integrated circuits, the oxygen in silicon became the most

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extensively studied impurity and a systematic study has been performed in the past base on pn junction lifetime analysis.

Silicon oxide precipitates may form at the commonly used processing temperatures due to the existence of supersaturated interstitial oxygen in silicon crystals. The effect of different kinds of thermal pre-treatment, on the formation of oxygen-precipitation induced extended defects was studied by Claeys [52]. The well characterized wafers either treated with an oxygen precipitation nucleation step in nitrogen (nucl), or an internal gettering cycle consisting of an oxygen-out-diffusion step followed by the nucleation treatment (IG). The results were compared with the wafers without any thermal treatment.

It was found that the amount of precipitate oxygen depended on both the initial oxygen concentration and the thermal pre-treatment. Besides, from TEM analysis, a Defect Lean Zone (DLZ) was more likely to present in the wafers with high initial oxygen content after the diode processing [53]. The Precipitate/Dislocation complexes (PD) and isolated Platelike SiO_x precipitates (P) were observed. The average PD and precipitate size is larger in IG wafers than for wafers without a pre-treatment, due to the much larger critical precipitate radius in case that a high temperature out-diffusion step is implemented. Two minority traps were detected in a high oxygen content p-type wafer without pre-treatment by using DLTS, ET_1 at $E_c - 0.23$ eV and ET_2 at $E_c - 0.43$ eV, and it is suggested that the electrical properties of oxide precipitates and their associated extended defects are dominated by these two electron traps. Besides, leakage current is most likely generated by

deep level ET_2 as well [53]. The results of lifetime measurement also showed that in material with high oxygen content, the IG process sequence would help increase the carrier lifetime which decreased for increasing oxygen content of the starting material [52].

Extraction methods for the minority carrier generation lifetime and the diffusion current in PN junction diodes have been developed for further investigation of the defects characteristics, and will be discussed in the chapter 5.

2.3.2 Bonding interface characterization

2.3.2.1 Capacitance-voltage profiling (C/V profiling)

Capacitance-voltage (C/V) profiling is a technique used for characterization of semiconductor materials and devices. It works on the depletion region in a Schottky diode or pn junction, a region which may contain ionized donors and electrically active defects or traps, but is empty of conducting electrons and holes. By varying the voltage applied to the junction, the width of the depletion region will be varied, leading to the changes of the diode capacitance. A C/V profile can be obtained by measuring the capacitance at various voltage levels, and may provide information on the semiconductor's internal characteristics, such as its doping profile and electrically active defect densities.

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The Schottky diode or pn junction under reverse bias behaves like a parallel-plate capacitor where the depletion layer width, which is associated with the applied voltage, acts as the spacing between the two plates.

A dc bias V is applied to the metal contact, and produce a reverse-biased depletion region of width W . The differential or small signal capacitance is defined by

$$C = -\frac{dQ_s}{dV} \quad (2.5)$$

where Q_s is the semiconductor charge. The capacitance is determined by superimposing a small-amplitude ac voltage v on the dc voltage V . The ac voltage typically varies at frequencies of 10 kHz to 1 MHz with an amplitude of 10 to 20mV.

Fig 2.7 shows a C - V curve of a reverse-biased PN junction which is measured by using C - V profiling machine directly.

Figure 2.7: Example of ideal C - V curve of biased PN junction [54]

2.3.2.2 Deep-level transient spectroscopy (DLTS)

DLTS is a powerful tool to study defect in semiconductor by measuring the electrical effects of defect states in the depletion region. In DLTS, effect of carrier emission is monitored by observing the capacitance transient of the semiconductor junction when the junction returns to equilibrium state from the initially biased state. Lattice defects such as vacancies and dislocations in the semiconductor will introduce an electronic energy state into the forbidden gap. In n-type samples, the observed defects will emit electrons to the conduction band and will lie above the middle of the gap. In p-type semiconductors, the spectral features correspond to defect states below mid-gap, and the holes are emitted to the valence band. [55] The emission of carriers leads to the changes in junction capacitance.

As the DLTS works by observing the capacitance changes which is associated with the width of depletion region, the samples for DLTS measurement can be either Schottky diodes or PN junctions. With the Schottky diodes, measurement of minority carrier traps is not possible as there is no injection of minority carriers. While with PN junctions, both majority and minority carrier traps can be observed.

During measurement, Schottky diodes or PN junctions are first biased by a DC reverse bias, removing the free carriers from the depletion region. A forward pulse will be subsequently applied to introduce carriers into the deep level defects with carrier. Upon removal of the pulse, the filled states emit these captured carriers during a thermal process with a characteristic time constant depending on the

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position of the defect state in the forbidden gap and on the available thermal energy. [55]

Among all types of defects, only point defects have sufficiently low formation energies, and may be formed in thermal equilibrium. Besides, their number also increases with thermal activation. Therefore, with temperature increasing, the density of point defects at the PN junction interface increases. For the other defects with higher dimensionality, such as dislocation, defect formation starts during growth and/or processing of semiconductor when activation energy level is reached, i.e. higher temperature. Therefore, the density of defects is supposed to increase with the increasing of temperature, which can be deduced from the temperature dependence of capacitance. The types of defects can be identified by their activation energy by using DLTS.

The capacitance transient is measured as a function of temperature, and the defect states are characterized by analyzing the temperature dependence of the capacitance transients. By using a double box-car averaging technique [55], peaks for each defect level in the forbidden gap of the silicon sample at a particular emission rate are found as a function of temperature. The typical raw data obtained by using DLTS is shown in Fig 2.8. An Arrhenius plot of $\ln(T^2 e_n^{-1})$ vs $1000/T$, where T is the absolute temperature in K, e_n is the emission rate of carriers, which can be obtained by looking for emissions at different rates and monitoring the temperature of the associated peak. The activation energy for carrier emission from the traps to the nearest band (E_c for electrons, E_v for holes) can be deduced from

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the slope of the Arrhenius plot. The final results of DLTS spectra by using Arrhenius plot are shown in Fig 2.9 as an example. From Fig 2.9, one can find that the trap activation energy, defect concentration, as well as the trap type (electron or hole) can be obtained from DLTS analysis. As the temperature varies, different types of defects are activated when their activation energy level is reached, leading to the detection of that type of defects by DLTS. There are five kinds of electron traps, together with two types of hole traps in Fig 2.9, all with different activation energy levels.

Figure 2.8: Typical raw data obtained by using DLTS

Figure 2.9: Typical DLTS spectra using an instrument time constant of 6 ms [56]

If the number of defects is much less than the number of free carriers, then the concentration of the defects can be obtained from the capacitance transient as a function of temperature.

$$N_T = \frac{2\Delta C}{C_0} (N_D - N_A) \frac{V_R}{V_P} \quad (2.6)$$

where N_T is the number of defects, $(N_D - N_A)$ is the number of free carriers, V_R is the reverse bias voltage, V_P is the pulse height in volts, ΔC is measured from the peak height, and C_0 is the capacitance of the sample at the peak temperature. [55]

A complete analysis of DLTS data yields the defect state concentration, the activation energy for the electronic transition, the majority carrier capture cross-section, and the depth distribution of the defect. The limit of detection of capacitance transient spectroscopy is approximately 10^{-5} times the background free

carrier concentration [55]. In our work, DLTS analysis for activation energy and defect state concentration is included while the other analysis will be future work.

2.3.2.3 Current-voltage profiling (I/V profiling)

I/V measurement of the experimental samples was carried out using HP4156A. Voltage supply to obtain the profiles ranges from 10 to -200 volts, in step of 0.5 volts. *I/V* profile of sample group B1.3 is shown below as an example.

Figure 2.10: I/V curve of sample group B1.3

The samples are firstly forward biased during which the depletion region becomes narrower, and the built-in electric field for the majority carriers is reduced. Thus, a large current flows across the junction. The majority carriers diffuse into the opposite side across the junction, become minority carriers and recombine with the majority carriers.

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The samples start to be reverse biased when the supply voltage become negative, which aids the built-in barrier field in the depletion region. The depletion region becomes wider because the majority carriers are pulled back from the junction. It is the minority carriers that contribute the current under reverse bias. Therefore, the current is small as there are few minority carriers available. The current through a pn junction is related to the applied voltage by the Shockley equation [79].

$$i_D = I_s \left[\exp\left(\frac{v_D}{nV_T}\right) - 1 \right] \quad (2.7)$$

Under reverse bias, supply voltage v_D is negative. I_s is the saturation current and $i_D = -I_s$ when v_D is sufficiently large in magnitude.

2.4 Design and Analysis of Experiments

In general, to find out the key parameters experimentally, typical approach of changing one factor at a time is used, which does not allow for factor interactions to be investigated adequately. In contrast, design and analysis of experiments can determine readily not only how each factor affects the response variable of interest, but also how each factor might interact with one another [57].

Response surface methodology (RSM) [58] comprises a group of statistical techniques for empirical model building and model exploitation. By careful design and analysis of experiments, it seeks to relate a response, or output variable to the levels of a number of predictors, or input variables, that affect it.

RSM have been proved valuable in the solution of a large variety of problems. The main applications are as follows:

1. Approximate mapping of a surface within a limited region
2. Choice of operating conditions to achieve desired specifications
3. Search for optimal conditions

In this project, Response Surface Methodology (RSM) has been embedded in the software that has been applied to obtain the expressions for all the output electrical parameters of STANDARD, SPEED, BUFFER and CLC diodes based on the MEDICI simulation data.

2.5 Summary

The development of non-standard power diodes was presented in this chapter, such as BUFFER diode, SPEED diode, and CLC diode. Structures and advantages of these diodes were briefly introduced and compared.

Wafer bonding technology was also reviewed in this chapter. Comparing with the conventional wafer bonding technique, vacuum wafer bonding technique, especially medium vacuum wafer bonding showed great potential on improving the bonding efficiency and quality under lower temperature through simpler process. Some brief introduction was also given on the interface viewing methods.

Introduction of the defects and impurities at the interface were also covered in this chapter, together with defects detection techniques that would be applied in our project.

Chapter 3 COMPARATIVE STUDY OF NON- STANDARD DIODES

3.1 Overview and Motivation

A device simulation for STANDARD, SPEED, BUFFER and CLC diodes was conducted using Design of Experiment (DOE) matrix and the MEDICI simulation tool. Structure and doping concentrations for optimization of different power diodes were obtained. Sensitivity analysis of the power diodes was also performed base on the simulation results in order to compare the suitability of different power diode structures for industrial mass-production.

3.2 Power Diode Structures and Definitions

a. Standard power diode

The structure of a standard power diode (P^+NN^+) is shown in Fig 3.1 where N_d^+ is fixed at $1 \times 10^{21} \text{ cm}^{-3}$ in order to reduce the number of parameters for the full factorial DOE matrix. The range of values for each of the input parameters is given in Table 3.1. The standard power diodes generally have poor switching speed, large peak reverse recovery current, high reverse transient currents and voltage spikes when they are used in high voltage applications with low forward voltage drops [12]. This is the main reason behind the exploration of other non-standard diode structures.

Figure 3.1: Standard power diode structure

b. SPEED diode

The structure of the SPEED power diode (P^+PNN^+) is shown in Fig 3.2 where the thickness of the N^+ layer (t_4) is fixed at $50\text{ }\mu\text{m}$ and the sum ($t_5 + t_6$) is fixed at $600\text{ }\mu\text{m}$. The corresponding range of values for the input parameters labeled in the figure is given in Table 3.1.

Figure 3.2: SPEED diode structure

The SPEED power diode is based on the *emitter efficiency control* technique. By controlling the carrier injection efficiency in the P^+ interface regions, reverse recovery characteristics can be improved. The thick lightly-doped p-emitter region causes injection efficiency to be low thereby reducing the total stored charge in the drift region. The lower the stored charge is, the faster the reverse recovery behavior. The P^+ pocket regions at the surface are implanted in order to minimize the forward voltage drop while keeping the reverse blocking voltage high [10].

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c. BUFFER diode

The structure of the *buffer* power diode ($P^+N^-NN^+$) is shown in Fig 3.3 with N_d^+ set to $1 \times 10^{21} \text{ cm}^{-3}$ and t_4 set to $50 \text{ }\mu\text{m}$. The parameters' range for this buffer diode is given in Table 3.1. Buffer diodes are based on the *drift region control* method where the lightly doped epitaxially grown extra N^- layer together with highly doped N-layer help prevent punchthrough and increase the residual stored charge, thus ensuring softer recovery. This is in contrast to a short standard power diode which frequently exhibits snappy recovery. However, due to the longer structure of a buffer diode, it tends to have a higher forward bias voltage and higher peak forward recovery voltage which is undesirable as it results in higher power consumption. [10]

Figure 3.3: BUFFER diode structure

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d. Carrier lifetime control (CLC) diode

The structure of the *CLC* power diode (P^+NN^+) investigated in this study is shown in Fig 3.4 with t_3 fixed at $50\ \mu\text{m}$ and N_d^+ fixed at $1 \times 10^{21}\ \text{cm}^{-3}$. Other parameters vary as defined by the DOE matrix. The range of the input structural and doping parameters is shown in Table 3.1. The carrier lifetimes are reduced by introducing recombination centers through various means in order to reduce the leakage current and the peak reverse recovery current.

Figure 3.4: CLC diode structure

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Table 3.1 Range of input parameter values for different diode structures

Parameter	MIN	MAX		Parameter	MIN	MAX
STANDARD POWER DIODE						
t_1 (μm)	10	100		t_6 (mm)	0.7	1.1
t_2 (μm)	50	200		N_a^+ (cm^{-3})	1×10^{18}	1×10^{21}
t_3 (μm)	50	50		N_d (cm^{-3})	1×10^{14}	1×10^{17}
SPEED POWER DIODE						
t_1 (μm)	10	50		t_6 (mm)	100	500
t_2 (μm)	10	50		N_a^+ (cm^{-3})	1×10^{18}	1×10^{21}
t_3 (μm)	50	200		N_a (cm^{-3})	1×10^{14}	1×10^{18}
t_4 (μm)	50	50		N_d (cm^{-3})	1×10^{14}	1×10^{18}
t_5 (μm)	100	500		N_d^+ (cm^{-3})	1×10^{18}	1×10^{21}
BUFFER POWER DIODE						
t_1 (μm)	10	100		N_a^+ (cm^{-3})	1×10^{18}	1×10^{21}
t_2 (μm)	5	50		N_d^- (cm^{-3})	1×10^{12}	1×10^{15}
t_3 (μm)	5	150		N_d (cm^{-3})	1×10^{14}	1×10^{18}
t_5 (μm)	700	1100				
CLC POWER DIODE						
t_1 (μm)	10	100		t_6 (mm)	700	1100
t_2 (μm)	50	100		N_a^+ (cm^{-3})	1×10^{14}	1×10^{17}
t_4 (μm)	0	25		N_d (cm^{-3})	1×10^{18}	1×10^{21}
t_5 (μm)	0	25				

3.3 MEDICI Simulation and Statistical Analysis

Given the range of values for the input doping and structural parameters for each type of diode, different combinations of the various input parameters can be obtained using a full-factorial design of experiment (DOE) matrix [57]. The output electrical parameters of each type of diode can then be obtained from the MEDICI simulation for the given combinations of the input parameters.

The Continuity and Poisson Equation toolboxes in MEDICI [15] are used to describe the high-level injection based device physics of the power diode.

To extract the values of the various electrical parameters of the four diodes studied here, including the standard power diode, an appropriate standard input waveform with similar dV/dt slope must be provided, as shown in Fig 3.5.

The expected output current transient waveform for the input waveform shown in Fig 3.5 is shown in Fig 3.6 with the characteristic parameters described in Table 3.2.

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Figure 3.5: Input waveforms for the diode under study

The standard input waveform shown in Fig 3.5 above is provided to achieve 80% breakdown voltage (V_{br}) of each diode structure. Different combination of input doping and structural parameters of the diode structures are determined by applying DOE matrix. Time (TD, TR, TP, TF, TP, TH) is adjusted accordingly to make sure that dV/dt slopes of the input waveform provided to the different structures are the same.

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Figure 3.6: Output power diode current waveform signal illustrating the definitions of various electrical parameters

Table 3.2 Definitions for the electrical output parameters

V_R	Reverse Breakdown Voltage
V_F	Forward Voltage Drop
I_{RM}	Reverse Transient Peak Current
S	Softness Factor
t_s	Time difference between $I = 0$ and $I = I_{RRM}$
t_{rr}	See Fig 3.6
$M1$	S/t_{rr}
$M2$	$1/(t_{rr} V_F)$
$M3$	$1/(t_{rr} I_R)$

3.4 Response Surface Method (RSM) Analysis

Following the extraction of the output electrical parameter values for different combinations of the input doping and structural parameter values, the Response Surface Method (*RSM*) [59] is used to obtain an empirical relationship showing the dependence of the respective output electrical parameters on the input device parameters. The expressions for all the output electrical parameters of STANDARD, SPEED, BUFFER and CLC diodes obtained using *RSM* are shown in Appendices A - D.

3.5 Analysis of Variance (ANOVA)

After having obtained the empirical relationships above, it is necessary to determine the most significant doping and structural parameters which have the greatest impact on the electrical parameter value for each of the diodes. This information is obtained by performing an *analysis of variance* (ANOVA) [60] and the results of this analysis are indicated in Table 3.3 below.

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Table 3.3 Significant input parameters (*) for each electrical parameter

STANDARD DIODE									
	V_F	V_R	I_{RM}	S	t_a	t_{sk}	M1	M2	M3
t_2	*	*	*	*	*	*	*	*	*
t_6				*		*			
N_a^-			*						*
N_d	*	*	*		*		*	*	
SPEED DIODE									
	V_R	V_F	I_{RM}	S	t_a	t_{sk}	M1	M2	M3
t_1	*	*		*				*	
t_2	*	*						*	
t_3	*	*	*	*					*
t_5	*	*	*	*				*	
N_a^-		*			*	*			
N_a	*	*		*		*		*	*
N_d	*	*	*	*		*	*	*	*
N_d^-		*					*		
BUFFER DIODE									
	V_F	V_R	I_{RM}	S	t_a	t_{sk}	M1	M2	M3
t_1								*	
t_2	*	*	*	*	*	*	*	*	
t_3	*	*	*				*	*	*
t_5			*	*				*	*
N_a^-	*				*				
N_d^-	*	*		*			*		
N_d	*	*		*	*	*	*	*	*
CLC DIODE									
	V_F	V_R	I_{RM}	S	t_a	t_{sk}	M1	M2	M3
t_1	*	*	*	*	*	*	*	*	*
t_2		*		*					*
t_3									
t_4		*			*	*		*	*
t_5		*		*				*	*
t_6				*	*	*		*	*
N_a^-	*	*		*				*	*
N_d	*	*	*		*	*	*	*	*

3.6 Simulated Annealing for Global Optimization

To compare the optimum performance capabilities of all the four diodes, it is necessary to optimize their electrical parameters given by the empirical equations in Appendices A - D. Since most of these equations have 4 – 8 input variables and *global optimization* to find the most optimal value of an electrical parameter is required, an efficient *n-dimensional global optimization* based mathematical algorithm is needed. While there are many local optimization algorithms available, global optimization algorithms are few, and, the most efficient of them is the *Simulated Annealing (SA)* algorithm [61, 62].

SA is applied to optimize the empirical diode electrical parameter equations. In this case, the objective function F to be maximized corresponds to the electrical parameters such as V_F , V_R , t_s , t_{rr} , I_{RM} , S etc... and the input vector x represents the set of structural and doping parameters $\{N_D, N_A, t_4, t_6 \dots\}$.

Equation (3) in Appendix A which describes the t_s parameter of a STANDARD diode is chosen as an example. Executing the *SA* algorithm, Fig 3.7 shows the convergence of t_s towards the global minimum after more than 20000 transitions. Transition is the change of system state according to certain probability distribution [61]. Fig 3.8 shows the decreasing trend of the *acceptance ratio (AR)*, which represents the fraction of successful state transitions towards the optimized values. Lower AR means a smaller fraction of state transitions can be accepted as solutions based on the acceptance criterion [61]. Very low values of AR around 0.01%

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serves as a good criteria for acceptance of the optimized solution and termination of this intensive search algorithm.

Figure 3.7: Convergence of t_s to global minimum

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Figure 3.8: Acceptance Ratio (AR) trend as t_s reached global minimum

The optimal values for each of the output electrical parameters and the corresponding values for the other non-optimized output parameters are all described in Table 3.4 (a) and Table 3.4 (b) below for each of the four diodes using the *SA* method. The shaded cells in the tables represent the value of the optimized output electrical parameters.

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Table 3.4 (a) Optimal values for each electrical parameter and the corresponding on-optimal parameters for STANDARD and SPEED diodes

OPTIMIZED PARAMETER	STANDARD DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rx}	M_1	M_2	M_3
	V_R	-1.14×10^8	-13.54	-144.31	-79.89	-63.46	-32.68	-63.35	-94.64	-559.95
	V_F	0.997	0.868	1.031	0.876	0.872	0.890	0.873	0.889	1.145
	I_{RM}	-0.00333	-0.00660	-9.84×10^{-6}	-0.0105	-0.00927	-0.00553	-0.00896	-0.00414	-1.65×10^{-4}
	S	3.698	35.61	0.3187	253.58	196.23	0.836	24.76	7.45	102.32
	t_s	5.24×10^{-6}	1.10×10^{-6}	3.12×10^{-6}	1.09×10^{-6}	1.01×10^{-6}	1.70×10^{-6}	1.02×10^{-6}	1.62×10^{-6}	3.45×10^{-6}
	t_{rx}	2.49×10^{-7}	9.90×10^{-7}	5.23×10^{-6}	7.18×10^{-6}	5.55×10^{-6}	2.22×10^{-6}	6.61×10^{-7}	2.18×10^{-6}	3.00×10^{-6}
	M_1	2.30×10^7	6.32×10^7	2.09×10^7	6.84×10^7	6.60×10^7	5.12×10^7	7.32×10^7	5.47×10^7	2.08×10^7
	M_2	6.39×10^6	2.25×10^7	1.15×10^7	1.89×10^6	1.98×10^7	2.25×10^7	2.26×10^7	2.52×10^7	2.77×10^6
	M_3	-2.99×10^{12}	-1.70×10^{12}	-9.78×10^{12}	-8.29×10^{12}	-1.54×10^{12}	-3.14×10^{12}	-6.62×10^{12}	-9.55×10^{11}	-4.89×10^{12}
OPTIMIZED PARAMETER	SPEED DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rx}	M_1	M_2	M_3
	V_R	-925.18	-102.37	-122.29	-485.25	-18.57	-70.77	-180.23	-137.73	-20.27
	V_F	3.28	0.421	0.594	1.36	1.01	0.869	0.480	0.795	1.81
	I_{RM}	-0.00202	-0.00289	-3.83×10^{-6}	-0.00773	-0.00813	-0.00498	-0.00103	-0.00236	-0.0111
	S	1.21	1.19	1.00	2.95	1.65	0.942	1.38	1.99	1.134
	t_s	2.42×10^{-6}	1.17×10^{-6}	1.63×10^{-6}	7.27×10^{-6}	1.28×10^{-12}	1.22×10^{-6}	9.69×10^{-10}	1.82×10^{-10}	1.25×10^{-6}
	t_{rx}	5.09×10^{-6}	1.77×10^{-6}	1.67×10^{-6}	4.65×10^{-6}	2.24×10^{-6}	2.02×10^{-6}	5.72×10^{-6}	7.22×10^{-6}	7.81×10^{-6}
	M_1	4.47×10^7	2.95×10^8	2.82×10^8	6.03×10^7	2.32×10^8	2.24×10^8	3.61×10^8	2.57×10^8	1.85×10^8
	M_2	1.26×10^7	1.34×10^8	8.35×10^7	1.64×10^7	1.02×10^8	1.56×10^8	1.52×10^8	1.94×10^8	1.61×10^8
	M_3	-7.85×10^{10}	-2.19×10^9	-3.22×10^{10}	-2.58×10^8	-7.43×10^{10}	-3.47×10^{10}	-5.09×10^{10}	-3.37×10^{10}	-1.84×10^{11}

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Table 3.4 (b) Optimal values for each electrical parameter and the corresponding on-optimal parameters for BUFFER and CLC diodes

OPTIMIZED PARAMETER	BUFFER DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rr}	M_1	M_2	M_3
	V_R	-1.31×10^3	-52.19	-344.16	-332.85	-777.70	-309.93	-204.00	-103.34	-314.73
	V_F	0.931	0.849	0.988	0.997	0.978	0.945	0.925	0.893	0.938
	I_{RM}	-9.86×10^{-4}	-0.0247	-3.81×10^{-5}	-0.0602	-0.0269	-0.0385	-0.0708	-0.105	-0.0548
	S	3.63	0.782	2.93	6.47	5.76	2.63	4.41	0.897	1.45
	t_s	1.37×10^{-7}	4.11×10^{-8}	5.33×10^{-8}	6.61×10^{-8}	2.44×10^{-8}	1.00×10^{-8}	2.72×10^{-8}	1.87×10^{-8}	3.58×10^{-8}
	t_{rr}	4.79×10^{-7}	1.36×10^{-7}	2.78×10^{-8}	4.17×10^{-8}	2.38×10^{-8}	1.92×10^{-8}	4.85×10^{-8}	2.64×10^{-8}	5.48×10^{-8}
	M_1	1.52×10^0	2.51×10^0	5.86×10^0	1.24×10^0	9.68×10^0	6.93×10^0	1.29×10^0	8.06×10^0	9.29×10^0
	M_2	5.93×10^0	2.78×10^0	1.96×10^0	2.39×10^0	1.78×10^0	2.61×10^0	3.53×10^0	4.60×10^0	3.79×10^0
	M_3	-1.14×10^0	-1.76×10^0	-2.95×10^0	-9.38×10^0	-6.13×10^0	-4.08×10^0	-1.50×10^0	-2.54×10^0	-3.40×10^0
OPTIMIZED PARAMETER	CLC DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rr}	M_1	M_2	M_3
	V_R	-3.65×10^3	-77.57	-86.94	-161.68	-737.03	-840.90	-159.39	-38.97	-233.77
	V_F	6.20	0.752	0.877	0.901	1.96	2.12	0.968	1.06	1.12
	I_{RM}	-0.0297	-0.0174	-0.00786	-0.0189	-0.0239	-0.0174	-0.0206	-0.0199	-0.0122
	S	3.26	5.03	0.318	9.21	4.88	0.396	9.17	5.00	5.01
	t_s	4.43×10^{-7}	1.48×10^{-7}	2.17×10^{-7}	2.15×10^{-7}	2.29×10^{-8}	2.42×10^{-8}	9.03×10^{-8}	3.42×10^{-8}	1.17×10^{-7}
	t_{rr}	8.24×10^{-7}	4.99×10^{-7}	2.47×10^{-7}	6.67×10^{-7}	2.40×10^{-7}	2.75×10^{-8}	5.19×10^{-7}	2.31×10^{-7}	3.05×10^{-7}
	M_1	1.58×10^0	5.58×10^0	4.76×10^0	7.21×10^0	5.25×10^0	4.30×10^0	7.38×10^0	6.90×10^0	6.32×10^0
	M_2	9.80×10^0	2.74×10^0	2.49×10^0	3.21×10^0	2.61×10^0	2.40×10^0	3.31×10^0	3.26×10^0	3.04×10^0
	M_3	-2.92×10^{11}	-5.73×10^{11}	-6.26×10^{11}	-6.88×10^{11}	-5.18×10^{11}	-6.30×10^{11}	-6.82×10^{11}	-6.28×10^{11}	-7.78×10^{11}

3.7 Sensitivity Analysis

Having determined the optimal values of each individual electrical parameter for every diode, it is now necessary to examine the magnitude of change of these electrical parameter values for a certain percentage change in the structural/doping parameter value. This is necessary because fabrication processes are frequently subject to variations of around 10% in power diode manufacturing. The effects of these variations on the electrical parameters must be examined in order to investigate its manufacturability. If the electrical parameters of a type of diode are very sensitive to the variation of the structural parameters, then the type of diode will not be suitable for manufacturing due to higher costs and lower output yield.

Sensitivity of an n -dimensional function f with respect to one of its variables x_i is simply defined as a partial derivative $\frac{\partial f(x_1, \dots, x_n)}{\partial x_i}$.

With this definition, *sensitivity analysis* is performed for all the electrical parameters with respect to all the structural/doping input parameters for all the four diodes examined. A 10% change in the input variable is assumed and the percentage change in the corresponding output variable is calculated. The sensitivity analysis is performed only with respect to the significant variables identified from the *ANOVA* analysis. Table 3.5 lists the effect of 10% variation of a single input parameter on the electrical output parameter for all the four diodes.

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Table 3.5 Sensitivity analysis of each electrical parameter with respect to 10% change in the diode structure parameters

Structure Parameters	ELECTRICAL PARAMETERS								
	STANDARD DIODE								
	V_T	V_{BE}	I_{BES}	S	t_c	t_{sw}	M_1	M_2	M_3
t_c	0.15 %	2.27 %	-732.64 %	-7.75 %	8.12 %	-8.76×10^2	-3.65 %	1.36 %	26.03 %
t_{sw}	----	----	----	55.61 %	----	6.01×10^3	----	----	----
N_a^+	----	----	-11.97 %	----	----	----	----	----	2.04 %
N_d	-0.0921 %	-4.12 %	41.55 %	----	-0.61 %	----	1.12 %	1.20 %	----
SPEED DIODE									
t_1	0.93 %	2.85 %	----	3.67 %	----	----	----	0.39 %	----
t_2	0.0497 %	0.630 %	----	----	----	----	----	2.25 %	----
t_3	4.9 %	15.64 %	117.72 %	3.12	----	----	----	----	5.59 %
t_c	1.85 %	2.69 %	769.48 %	0.80 %	----	----	----	5.59 %	----
N_a^+	----	0.389 %	----	----	22100 %	16.59 %	----	----	----
N_s	0.301 %	0.464 %	----	1.23 %	----	51.04 %	----	0.91 %	1.76 %
N_d	3.43 %	3.61 %	327.68 %	1.28 %	----	15.07 %	1.13 %	1.00 %	1.92 %
N_d^+	----	0.548 %	----	----	----	----	0.49 %	----	----
BUFFER DIODE									
t_1	----	----	----	----	----	----	----	0.121 %	----
t_2	0.183 %	4.68 %	2799.35 %	3.38 %	2776.90 %	358.85 %	0.806 %	0.539 %	----
t_3	0.0834 %	1.86 %	6190.79 %	----	----	----	0.388 %	0.469 %	7.45 %
t_c	----	----	5569.56 %	5.37 %	----	----	----	2.65 %	30.74 %
N_a^+	0.0670 %	----	----	----	4145.08 %	----	----	----	----
N_s	15.9 %	1.15 %	----	0.466 %	----	----	0.394 %	----	----
N_d	0.0423 %	1.39 %	----	1.06 %	810.26 %	42.66 %	0.672 %	0.105 %	1.69 %
CLC DIODE									
t_1	64.95 %	1.11 %	16.18 %	7.44 %	24000 %	3010.35 %	12.19 %	9.09 %	8.73 %
t_2	----	0.985 %	----	7.96 %	----	----	----	----	1.13 %
t_3	----	----	----	----	----	----	----	----	----
t_c	----	0.326 %	----	----	387.41 %	827.38 %	----	0.0130 %	0.10 %
t_{sw}	----	0.173 %	----	0.683 %	----	----	----	0.0157 %	1.45 %
t_{tr}	----	----	----	5.11 %	12300 %	2003.87 %	----	0.0621 %	3.47 %
N_a^+	3.11 %	0.266 %	----	0.340 %	----	----	----	0.286 %	0.0353 %
N_d	5.89 %	1.65 %	2.25 %	----	370.28 %	116.81 %	1.01 %	1.00 %	1.29

Since most of the structural/doping factors are subject to process-induced variations simultaneously, it would be useful to also assess the impact on the electrical parameter by varying all the input parameters simultaneously by +10%. Table 3.6 shows the results for this condition of all parameters varying by +10%.

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Table 3.6 Sensitivity analysis of each electrical parameter when all the input parameters change by 10%

Output Parameter [% CHANGE]				
STANDARD DIODE				
V _R	V _F	I _{RM}	S	t _s
6.46 %	0.74 %	1270.43 %	56.50 %	11.96 %
t _{IT}	M ₁	M ₂	M ₃	
9510.36 %	7.72 %	8.00 %	31.29 %	
SPEED DIODE				
V _R	V _F	I _{RM}	S	t _s
9.21 %	21.43 %	2120.37 %	11.91 %	145400 %
t _{IT}	M ₁	M ₂	M ₃	
219.09 %	4.18 %	10.88 %	19.92 %	
BUFFER DIODE				
V _R	V _F	I _{RM}	S	t _s
9.63 %	0.98 %	15175.59 %	9.27 %	23465.57 %
t _{IT}	M ₁	M ₂	M ₃	
2051.04 %	4.51 %	4.00 %	30.50 %	
CLC DIODE				
V _R	V _F	I _{RM}	S	t _s
4.73 %	80.73 %	61.58 %	17.01 %	42628.82 %
t _{IT}	M ₁	M ₂	M ₃	
7296.73 %	13.49 %	10.29 %	13.39 %	

3.8 Results and Discussion

From Table 3.4, we can see that the CLC diode has the highest reverse breakdown voltage (V_R) and the highest values of $M1$ and $M2$ as compared to the other type of diodes. Moreover, it has a reasonably low value of t_{rr} . These trends could be attributed to the localized recombination centers introduced at the PN junction in the drift region of the CLC diode in order to reduce the minority carrier lifetime locally, leading to reduction of the reverse recovery parameters with higher avalanche breakdown voltage, V_R . However, both the leakage current I_{RM} and forward voltage drop V_F are increased as a result. From Table 3.4, it can be seen that the value of I_{RM} is the highest for the CLC diodes, and V_F for CLC diode is also relatively high comparing with other non-standard diodes. But the large $M1$ and $M2$ values implies that the CLC diode has a better balance between the switching speed and the softness of reverse recovery, as well as the switching speed and forward voltage drop.

In comparison, SPEED diodes have the lowest optimal forward voltage drop (V_F) and lowest storage time, t_s . This is due to the fact that the low injection efficiency provided by the thick lightly doped p-emitter results in reduced storage charge in the drift region at typical on-state current levels, thus contributing to a quicker reverse recovery, i.e. smaller t_s . The reduced storage charge also reduces the leakage current. The highly doped P+ regions provide high injection efficiency only at high current densities to minimize forward voltage drop (V_F). The reduced storage charge implies high di/dt during recovery causing voltage spikes and

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snappy recovery to occur. Thus, the softness factor (S) is the lowest for SPEED diodes.

As for the BUFFER diode data in Table 3.4, leakage current (I_{RM}) and recovery time t_{rr} are quite low and reverse breakdown voltage (V_R) is relatively high as compared to the other types of diodes. The additional N-layer helps prevent the depletion region from reaching the NN^+ junction thereby avoiding the occurrence of punch-through breakdown. The N-layer also facilitates extra charge storage leading to softer recovery. The avalanche breakdown voltage is also increased due to the low doping of the N-layer. However, due to the comparatively longer configuration and lightly doped N- layer of the BUFFER diode, the forward voltage drop (V_F) is one of the highest amongst all the novel devices studied.

The conventional STANDARD diode is superior to the other novel non-standard structures only in two aspects viz. softness factor (S) and M3. Since there is adequate charge storage in the drift region of standard diodes, recovery is slow and smooth, thus causing the softness factor (S) to be the highest. A large M3 value indicates a better performance for the conventional diode in terms of the trade-off between switching speed and leakage current. As for the other electrical performance parameters, the non-standard device structures have better optimal performances than the standard one.

The analysis so far has only focused on the values of each of the individual optimized parameter values. We have not considered the corresponding values of the non-optimal electrical parameters for a given optimal output parameter. For

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example, while $V_R = -3650V$ is the highest reverse breakdown voltage, which is found in a CLC diode, the corresponding non-optimal V_F value is as large as $6.20V$, which is too high to be practical. Similarly, while $V_F = 0.421V$ is the lowest forward voltage drop observed in a SPEED diode, the corresponding value of reverse bias breakdown (V_R) is only $-102.37V$, which could be too small for some applications. Therefore, consideration of individual optimized parameters alone is not sufficient and it is more useful to compare the devices using M1, M2 and M3 which have a combination of a few electrical parameters embedded in them. M1 and M2 are the highest in CLC diodes whereas M3 is highest for the standard diode. In this way, the practicality of a diode may be assessed from multi-dimensional perspective.

The sensitivity analysis was carried out next and the sensitivity data in Tables 3.5 and 3.6 which are based on the ANOVA sensitivity matrix results in Table 3.3 which shows the set of the most significant input data variables for each electrical output parameter.

For the STANDARD diode, the I_{RM} value is highly sensitive to t_2 and N_D while t_{rr} is highly sensitive to t_2 and t_6 . S is also found to be very sensitive to t_6 . All the other parameters are relatively insensitive to any process variations. Similar conclusions for the other type of diodes can be made.

On the whole, certain sensitivity trends are consistently observed. I_{RM} , t_s and t_{rr} are the three most critical electrical parameters which vary significantly ($>10\%$, as practice commonly in industry) with respect to minor process variations.

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Sensitivity for I_{RM} , t_s and t_{rr} are the lowest in CLC, Standard and SPEED diodes respectively, as revealed by the data in Table 3.6. All these three parameters are extremely sensitive in the case of a BUFFER diode. Therefore, it may be concluded that the BUFFER diode structure is not manufacturable and commercially unfeasible.

The results above reflect the real situation in the power diode industry that manufacturability is a key concern for the t_{rr} and I_{RM} parameters, which is presented by the variable M3, as defined in Table 3.2.

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3.9 Summary

Simulation on power device performance was carried out and the results were presented in this chapter using software such as MEDICI, simulated annealing and so on. It can be found out that not all of the structure parameters can be optimized at the same time. By comparing the electrical behaviors of different power diode structures, CLC diode was selected and recommended for the future fabrication work according to its excellent electrical performance.

Chapter 4 EXPERIMENTAL PROCEDURES

In this chapter, the experimental procedure for PN junction diodes fabrication using wafer bonding and electrical property characterization will be presented.

4.1 Overview of Experimental Process Flow

The experiment procedure includes fabrication & characterization of the PN junction diodes. The fabrication process using MVWB was performed by the author in Shanghai Kunshan Sino Silicon Technology. Two silicon wafers of different type (P or N) are firstly bonded using Medium Vacuum Wafer Bonding techniques. After that, a layer of nickel will be deposited onto both sides of the wafer bonding pairs using PECVD and forms the contacts. C-SAM scanning will then be applied to obtain an interface voids distribution map, which will be used for sample cutting in the following step. The edge damage caused by dicing saw in the cutting step will be etched away in the next etching step, and the diced samples

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(PN junction diodes) will be sent to I/V & C/V measurement. Finally, DLTS analysis is carried out to find out the activation energy and density of the bonding interface defects.

Figure 4.1: Experimental flow in this work. The detail of each step will be elaborated in the later sections

4.2 Medium Vacuum Wafer Bonding

There are several vacuum wafer bonding methods published, such as wafer bonding in ultrahigh vacuum (UHV) (10^{-10} mbar) [6], wafer bonding after Ar beam surface activation in high vacuum (10^{-8} mbar) [8], wafer bonding at medium vacuum level (10^{-4} mbar) [63, 64], and wafer bonding at low vacuum level (several mbar) [7].

As discussed in Chapter 2, conventional direct wafer bonding usually requires high-temperature annealing above 800°C or even 1000°C to achieve strong bonding, which is apparently uneconomical. Moreover, many serious problems will arise with high temperature treatment, such as the thermally induced mechanical stress in the bonding materials with different thermal expansion coefficients. Mechanically, severe stresses can lead to deformation, debonding, and even fracture of the pair. In addition, stress can also degrade the performance of device fabricated on the bonded structure. For industrial practice, the time and temperature required for p+ and n+ deep diffusion of a typical p+nn+ power diode rating above 400V and 1A is around 1100°C and more than 36 hours [80]. This represents tremendous power consumption in the manufacturing of power diode.

In contrast, it is possible to achieve higher bonding strength and bonding efficiency at low annealing temperature by MVWB, showing great advantages of MVWB over the conventional direct wafer bonding techniques. Besides, the bonding speed, defined as the reciprocal of the time to achieve saturation bonding strength, is dramatically enhanced and exhibits the huge potential to be employed for mass-

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production. By applying the low temperature direct wafer bonding method developed by Prof Tan Cher Ming, the time and temperature to fabricate power diode can be reduced to 4 hours at 400°C, leading to great reduction of energy consumption in power diode manufacturing industry. Therefore, MVWB deserves detailed study.

To get the quantitative degree of the interface stress induced by the annealing in the Si-Si wafer bonding structure, simulation using ANSYS, a finite-element analysis software was carried out. The result is shown in Figure 4.2.1.

Figure 4.2: Stress vs distance graph of Si-Si bonding structure obtained using ANSYS

The simulation is based on the withdrawal speed of 500mm/min, which is the max withdrawal velocity can be achieved due to the equipment limitation. From Fig.

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4.2, it can be observed that the max stress generated at the interface is 17.2 MPa, much smaller than the bonding strength limitation as 20 MPa [9]. Therefore, our experiment with withdrawal velocity slower than 500mm/min is safe to carry out.

4.2.1 Materials and instruments used in wafer bonding

This wafer bonding process is performed in Shanghai, China using the facilities of Kunshan Sino Silicon Technology Co. Ltd.

Materials:

To form PN^+ junction, we have the following wafers:

1. *P-type Si wafer: Boron doped*

Doping $N_a = 5.0 \times 10^{14} \text{ cm}^{-3}$

Diameter: 6 inches

Thickness: 400 μm

Orientation: [100]

2. *N-type Si wafer: Arsenic doped*

Doping $N_d = 2.0 \times 10^{19} \text{ cm}^{-3}$

Diameter: 6 inches

Thickness: 400 μm

Orientation: [100]

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Instruments:

A. Vacuum Furnace

Annealing at less than 500°C is performed in a Vacuum Furnace with the lowest vacuum level as 10^{-3} mbar and highest annealing temperature as 600°C.

Figure 4.3: Vacuum Furnace used for MVWB annealing

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B. RCA Cleaning Bath

Figure 4.4: RCA Cleaning Bath for wafer cleaning process

C. Spin Dryer

Figure 4.5: Spin Dryer

4.2.2 Process of wafer bonding

The process of MVWB is shown schematically in Figure 4.6. The detail of each step will be described below.

Figure 4.6: MVWB process flow

4.2.2.1 Wafer Cleaning (Surface Preparation)

The effect of the wet chemical cleaning process on the surface microroughness of silicon wafers was studied by Miyashita et al [65]. The surface microroughness was found to increase in wet chemical processing, in particular in $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ cleaning (RCA1 cleaning). It has been shown that the microroughness does not increase at all if the NH_4OH mixing volume ratio in RCA1 solution is suppressed at a low level in contrast to the conventional mixing volume ratio of 1:1:5. However, the actual ratio is confidential due to patent application.

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Figure 4.7: Wafer cleaning process flow

4.2.2.2 Room Temperature Bonding

After cleaning and drying, P-type and N-type wafers were bonded into pairs in the air under room temperature in class 1000 clean room.

The two wafers were contacted with each other in air from one edge as shown in the Figure below. Most of the air could be squeezed out and less bubble will be produced in this way.

Figure 4.8: Schematic of wafer contact

4.2.2.3 Annealing

The effect of different annealing process on interface/crystalline defects and junction performance under vacuum circumstances is to be investigated.

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Experiment on different medium vacuum wafer bonding annealing processes was performed for comparison.

The bonded wafer pairs were sent to vacuum furnace for annealing. Four groups of experiment were designed to investigate the influence of the four most determining experimental parameters on the performance of the devices fabricated and the interface properties. Details of the parameters are shown in Table 4.1. The vacuum level is 1×10^{-3} mbar due to the limitation of the vacuum furnace available. The ranges of the parameter values are set by making reasonable variation on the experimental results provided by Yu for achieving enhanced bond strength. [9]

From the MVWB process described above, the cleaning process has been optimized by Yu [9], and thus cleaning process will not be experimented. The room temperature bonding is also straight forward, and we have found that the best bonding is occur without applied load [9], and thus again it will not be experimented.

For the annealing, the obvious four parameters that we can experiment about are the annealing temperature, annealing time, heating rate before the annealing and the cooling rate after the annealing. As such, we divide the samples into 4 groups. Group A experiment is designed to study the effect of annealing time; effect of annealing temperature is investigated by group B; the effect of increasing rate of temperature is studied by group C; and group D is designed to investigate the effect of decreasing rate of temperature.

Table 4.1 MVWB bonding conditions in vacuum bonder used in this work

Vacuum Bonding Group		Process								
		Number of Bonded Wafer Pairs	Vacuum Level (mbar)	Applied Load (KN)	Heating		Annealing		Cooling	
					min	°C/min	°C	hour	hour	°C/hour
Group A	A1	6 pieces (3 pairs)	10 ⁻³	0	30	12.5	400	2	7	53.5
	A2	6 pieces (3 pairs)	10 ⁻³	0	30	12.5	400	3	7	53.5
	A3	6 pieces (3 pairs)	10 ⁻³	0	30	12.5	400	4	7	53.5
Group B	B1	6 pieces (3 pairs)	10 ⁻³	0	22	12.5	300	3	5.14	53.5
	B2	6 pieces (3 pairs)	10 ⁻³	0	30	12.5	400	3	7	53.5
	B3	6 pieces (3 pairs)	10 ⁻³	0	38	12.5	500	3	8.89	53.5
Group C	C1	4 pieces (2 pairs)	10 ⁻³	0	15	25	400	3	7	53.5
	C2	4 pieces (2 pairs)	10 ⁻³	0	30	12.5	400	3	7	53.5
	C3	4 pieces (2 pairs)	10 ⁻³	0	60	6.25	400	3	7	53.5
	C4	4 pieces (2 pairs)	10 ⁻³	0	15	31.7	500	3	8.89	53.5
	C5	4 pieces (2 pairs)	10 ⁻³	0	30	15.8	500	3	8.89	53.5
	C6	4 pieces (2 pairs)	10 ⁻³	0	60	7.9	500	3	8.89	53.5
Group D	D1	4 pieces (2 pairs)	10 ⁻³	0	30	12.5	400	3	6	62.5
	D2	4 pieces (2 pairs)	10 ⁻³	0	30	12.5	400	3	7	53.5
	D3	4 pieces (2 pairs)	10 ⁻³	0	30	12.5	400	3	9	41.7
	D4	4 pieces (2 pairs)	10 ⁻³	0	40	11.9	500	3	6	79.2
	D5	4 pieces (2 pairs)	10 ⁻³	0	40	11.9	500	3	7	67.9
	D6	4 pieces (2 pairs)	10 ⁻³	0	40	11.9	500	3	9	52.8

4.3 Metal Contact Formation

4.3.1 Sputtering

2 μ m thick Nickel (Ni) layer was deposited onto both sides of bonded wafer pairs using PECVD in SIMTECH (Singapore Institute of Manufacturing Technologies). The vacuum level in the PECVD chamber is kept around 10^{-5} mbar for sputtering. The sputtering process takes about 4 hours per round.

4.3.2 Post Sputtering Annealing

After sputtering, the bonded wafer pairs were annealed at 350°C for 20 minutes to improve the contact between the silicon and metal layer through the formation of nickel silicide [66]. To suppress the degradation of contact conductivity, annealing was carried out in a nitrogen environment furnace to avoid oxidation of metal layer.

4.4 C-SAM Scanning

Scanning acoustic microscopy (C SAM) was applied to obtain a map of trapped bubbles (void) distribution at the interface of the wafer pairs and examine the bonding efficiency. The map will be used for sample cutting using dicing saw, and the area without voids as observed under C-SAM is cut out into small pieces samples for experiment. The resolution of SAM to detect the bubbles is $2.5\mu\text{m}$. A C SAM graph obtained from a quarter of certain bonding pair is show in Fig 4.9 as an example. The area selected in this graph will be cut out and diced into small pieces for experimental measurement.

Figure 4.9: An example of C-SAM Micrograph

4.5 Sample Cutting

After C-SAM scanning, the maps of bonded wafer pairs showing voids distributed at the bonding interface are obtained and the areas without voids (voids diameter < 2.5 μ m) are cut out and diced into small pieces (5x5mm) for the following experimental measurement using DISCO DAD341 AUTOMATIC DICING SAW in SIMTECH.

Figure 4.10: DISCO DAD341 AUTOMATIC DICING SAW [67]

4.6 Edge Damage Etch

Edge damage of the dice caused by dicing saw would lead to large leakage current under large voltage supply because of the large electric field generated around the dice. This will be seen later on in the next section. Therefore, the damage is to be removed by acid etching.

The composition of the mixed acid (etchant) used for the etching process is listed below in weight ratio as this is the standard ratio used in power diode manufacturing.

HF (hydrofluoric acid, 48.8~49.5 wt%) : HNO₃ (nitric acid, 70 wt%) :
CH₃COOH (acetic acid, 99.5 wt%) = 5:5:3.

During etching, the electrodes on the top and bottom of the dice are protected from the etchant with standard glue. The etching duration is 10s. The details of the process are shown below.

- a. Spread and cover the electrodes with standard glue.
- b. Mix the acids following the ratio showing above in a Teflon beaker.
- c. Dip the chips into the mixed acids for 10s.
- d. Rinse the chips in DI water, using ultrasonic bath.
- e. Drop the chips into beaker with acetone, using ultrasonic bath.
- f. Dry the chips, place onto a tissue to let it dry.

4.7 IV & CV Measurement

Both IV and CV measurement of the diced samples is carried out, and the results obtained are used for the calculation of generation lifetime at the interface region, which is shown in the next chapter.

The devices are placed on probe station shown below in Fig 4.11 and 4.12 during measurement, which provide low leakage and signal loss. I/V and C/V profiles are obtained using HP4156A and HP4284A respectively, shown in Fig 4.13 and 4.14. Voltage supply ranges from 5 volts to -40 volts for C/V profiling, and from 10 volts to -200 volts for I/V profiling, due to the functional limitation of the equipment.

Figure 4.11: Probe station used for I/V profile measurement

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Figure 4.12: Sample holding stage & probe needle

Figure 4.13: HP4284A for C/V profile retrieval

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Figure 4.14: HP4156A, for I/V profile retrieval

4.8 Deep-level Transient Spectroscopy Analysis

Deep-level Transient Spectroscopy (DLTS) analysis is carried out to obtain the defect activation energy and defect density at the sample bonding interface. The principle of the DLTS is through observing the capacitance transient associated with the change in depletion region width as the diode returns to equilibrium from an initial non-equilibrium state. The capacitance transient is measured as a function of temperature (usually in the range from liquid nitrogen temperature to room temperature 300K or above). By using a double box-car averaging technique, peaks at a particular emission rate are found as a function of temperature from the emissions at different rates and the temperature of the associated peak. Arrhenius plot can be obtained which will be elaborated in chapter 5 section 5.3. The DLTS system used in this work is the Bio-Rad DL8000 Deep Level Transient Spectrometer System as shown in Fig 4.15.

The devices are placed into the chamber as shown below in Fig 4.16 and 4.17. The chamber will be vacuumed during measurement. Both the temperature and voltage supply in the chamber can be varied. The range for temperature variation is from 50K to 300K, while the range for voltage supply is from -20 to 20 volts due to the function limitation of the equipment.

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Figure 4.15: DL8000 Deep Level Transient Spectrometer System

Figure 4.16: Chamber of DL8000 DLTS

Figure 4.17: Top view of DL8000 DLTS chamber

4.9 Summary

The process flow of PN junction fabrication using MVWB technique was described. The instruments used in the process were also introduced in details. Characterization methods and equipments such as C-SAM, I/V , C/V and DLTS were presented in this chapter as well.

Chapter 5 EFFECTS OF WAFER BONDING

PROCESS PARAMETERS ON THE

ELECTRICAL

CHARACTERIZATION OF

INTERFACE DEFECTS

5.1 Theory & Procedure of Generation Lifetime

Calculation

5.1.1 Generation lifetime

Carrier lifetime can be divided into two broad categories: recombination lifetime and generation lifetime. The former one is used when there are excess carriers in the semiconductor and recombination dominates [51].

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There are three generation mechanisms: multiphonon generation via G-R centers, optical generation and impact ionization [51]. Optical generation can be neglected when there are no photons of energies larger than the band gap incident on the semiconductor devices. The electron-hole pair generation caused by impact ionization will be insignificant if the reverse bias voltage is below the impact ionization breakdown. Multiphonon generation is a thermally activated process, in which electrons are thermally excited from generation-recombination centers into the conduction band and holes are similarly thermally excited from generation-recombination centers into the valence band [51].

5.1.2 Theory of generation lifetime calculation

The generation lifetime t_g can be calculated from the reverse generation current density and the diffusion current density, while the recombination lifetime t_r can be calculated from the reverse current extrapolated to zero bias, which gives an estimate of the diffusion component of the leakage current. However, the reverse current is too small to be measured accurately in most cases. Hence, we do not employ this method.

Minority carrier generation lifetime can be extracted from I/V and C/V characteristics following a simple procedure [68, 69]. The area diffusion current density J_{dA} within the reverse saturation current density can be obtained from forward bias area current density J_A versus bias voltage V_F plot, by extrapolating the curve to the zero bias point ($V_F=0$). The generation current density J_{gA} versus

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reverse bias voltage V_R plot can therefore be derived from reverse bias area current density J_R versus bias voltage V_R curve according to Eq. 5.1

$$J_{gA} = J_R - J_{dA} \quad (5.1)$$

The depletion region width (W_A) as a function of V_R , $W_A(V_R)$, can be plotted based on the C/V profile since W_A and junction capacitance C are related through Eq. 5.2 for abrupt junction as in our case.

$$W_A = \frac{C}{AK_s \epsilon_0} \quad (5.2)$$

therefore, the area generation width W_{gA} [28] can be expressed as a function of V_R as follows

$$W_{gA} = \sqrt{W_A^2 - W_{A0}^2} \quad (5.3)$$

where W_{A0} is the depletion width at zero bias, which can be obtained by extrapolating W_A vs V_R plot to the point at $V_R=0$.

For PN^+ diode in our project, the maximum electric field F_m in the abrupt junction depletion region at a given reverse bias voltage V_{RI} is expressed in Eq. (5.4) [70]

$$F_m = -\frac{qN_A}{K_s \epsilon_0} x_p \quad (5.4)$$

where x_p is given by [70]

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$$x_p = \left[\frac{2K_s \epsilon_0 (V_{bi} - V_{R1})}{q} \frac{N_D}{N_A (N_A + N_D)} \right]^{1/2} \quad (5.5)$$

For a given reverse bias voltages, values of J_{gA} and W_{gA} can be obtained from Eq. 5.1 and Eq. 5.3 respectively. Consequently, one can plot J_{gA} versus W_{gA} curve, of which the slope at every point is a function of W_{gA} , $S(W_{gA})$.

From Eq. 5.4, the values of F_m at different reverse bias voltages V_R can be obtained. By relating V_R and W_{gA} through W_A versus V_R plot obtained above and Eq. 5.3, F_m can then be plotted versus W_{gA} , $F_m(W_{gA})$. Therefore, at given values of W_{gA} , both $F_m(W_{gA})$ and $S(W_{gA})$ can be obtained. Then by plotting S vs F_m curve, the generation current enhancement factor (Γ) can be derived by taking the slope of S vs F_m curve as follows [70].

$$\Gamma = \frac{d(J_{gA} / W_{gA})}{dF_m} \quad (5.6)$$

Since F_m is a function of V_R , the generation current enhancement factor (Γ) can also be expressed as a function of V_R , $\Gamma(V_R)$.

Finally, for a given reverse bias voltage, W_{gA} , Γ and J_{gA} can all be derived. Therefore, the generation lifetime t_g can be obtained through Eq. 5.7.

$$t_g = \frac{qn_i W_{gA} \Gamma}{J_A - J_{dA}} = \frac{qn_i W_{gA} \Gamma}{J_{gA}} \quad (5.7)$$

From Eq.5.3 and Eq.5.7, t_g versus W_A curve can be plotted.

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5.1.3 Procedure of generation lifetime calculation

In this section, the procedure to calculate the generation lifetime of interface defects by using reverse-biased I/V & C/V measurement results will be illustrated. Experimental results of group B1.3 (before edge damage etching process) will be taken as an example. Figures 5.1 and 5.2 show the I/V and C/V curves of a sample in group B1.3.

Figure 5.1: I/V profiling curve of group B1.3

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Figure 5.2: C/V profiling curve of group B1.3

W_{ga} vs V plot is obtained by applying Eq. 5.2 and 5.3 to the C/V experimental results, and is shown in Fig 5.3.

Figure 5.3: W_{ga} vs V plot of group B1.3

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On the other hand, J_{ga} vs V plot can be obtained from the I/V curve using Eq. 5.1 and is shown in Fig 5.4.

Figure 5.4: J_{ga} vs V plot of group B1.3

Then J_{ga} vs W_{ga} plot can be obtained from J_{ga} vs V plot and W_{ga} vs V plot as

Figure 5.5: J_{ga} vs W_{ga} plot of group B1.3

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The slope (S) of J_{ga} vs W_{ga} plot can be obtained, and the plot of S vs W_{ga} curve si as shown in Fig 5.6.

Figure 5.6: S vs W_{ga} plot of group B1.3

The maximum electric field in the depletion region F_m vs V curve can be plotted by substituting Eq. 5.5 into Eq. 5.4, and we have Fig 5.7.

Figure 5.7: F_m vs V plot of group B1.3

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F_m vs W_{ga} plot is therefore can be obtained from F_m vs V and W_{ga} vs V curves as in Fig. 5.8.

Figure 5.8: F_m vs W_{ga} plot of group B1.3

From S vs W_{ga} and F_m vs W_{ga} curves, S vs F_m can be plotted, of which the slope is the enhancement factor Γ that will be used for the calculation of carrier generation lifetime.

Figure 5.9: S vs F_m of group B1.3

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The carrier generation lifetime t_g can be calculated following Eq. 5.7. For a known voltage value, both x_p and t_g can be calculated, and the curve t_g vs x_p can be plotted, as shown below in Fig 5.10. Fig 5.11 shows the t_g vs x_p curve after noise removing by neglecting the unreasonable spikes.

Figure 5.10: t_g vs x_p plot of group B1.3

Figure 5.11: Smoothed t_g vs x_p plot of group B1.3

5.2 Effects of Experimental Parameters on Generation

Lifetime of the PN Junction Diode Fabricated

As mentioned in Chapter four, the obvious four parameters during annealing process that we can experiment about are the annealing temperature, annealing time, heating rate before the annealing and the cooling rate after the annealing. Therefore, the samples are divided into 4 groups for the experiment, namely group A, B, C and D. Group A is designed to study the effect of annealing time; while the effect of annealing temperature is investigated by group B; the effect of increasing rate of temperature is studied by group C; and group D is designed to investigate the effect of decreasing rate of temperature.

The experimental results for group C4-C6 and D4-D6 will not be shown here due to the abnormal early breakdown caused by small voids formed at the wafer bonding interface. Examples of the C-SAM graphs for group C4-C6 and D4-D6 are shown on Fig 5.12, lots of micro voids has been observed from the graph, distributing at the bonding interface.

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Figure 5.12: Examples of the C-SAM graphs for group C4-C6 and D4-D6

MEDICI simulation on the effect of interface voids has been carried out in order to show the effect of micro voids at the bonding interface. Different amount (zero, one, two and three, evenly distributed) of small voids of size $0.04\mu\text{m}^2$ has been placed at the interface, and the simulation result is shown on Fig 5.13.

Figure 5.13: Simulation results of logI vs V curve of junction diode with micro voids at the bonding interface

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The above graph plotted based on the MEDICI simulation result shows that the interface voids will engage early breakdown of the pn junction. Comparing with the ideal pn junction structure, of which the breakdown voltage is approaching - 500v, the structures with voids have much lower breakdown voltage, less than - 400v from the graph. Based on the data retrieved from the simulation, it shows that more voids will lead to lower breakdown voltage.

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5.2.1 Results of group A

The I/V curves of the group A samples are measured, and the results are shown in the Figures below. The measuring range for I/V is $-200\sim10$ volts, while the range for C/V is $-40\sim10$ volts due to equipment limitations.

The I/V curves obtained before and after etching process are both shown for comparison in the Figures below, and one can see that the leakage current is reduced dramatically after the etching process.

5.2.1.1 I/V measurement result of Group A1

Figure 5.14: I/V curves of group A1 before & after etching

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Figure 5.15: I/V curve of group A1, focusing on reverse biased portion

5.2.1.2 I/V measurement results of group A2

Figure 5.16: I/V curves of group A2 before & after etching

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Figure 5.17: I/V curve of group A2, focusing on the reverse biased portion

5.2.1.3 I/V measurement results of group A3

Figure 5.18: I/V curves of group A3 before & after etching

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Figure 5.19: I/V curve of group A3, focusing on the reverse biased portion

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5.2.1.4 Comparison between group A1, A2 and A3

MEDICI simulation has been performed to simulate the ideal performance of PN junction for comparison. The I/V curves of the selected samples from group A1, A2 and A3 are compared. Ideal I/V curve is obtained by simulation using MEDICI, and the logarithm values are used for comparison between the ideal I/V and the experimental results of A1, A2 and A3. The C/V curves of the selected samples from group A1, A2 and A3 are also compared in Fig 5.28. From Fig 5.20 and 5.21, it can be seen that the breakdown voltage of group A3 is much larger than A1 and A2, and its leakage current is also the smallest among the three groups.

Figure 5.20: Comparison between the I/V curves of group A1, A2 & A3 before etching

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Figure 5.21: Comparison between the I/V curves of group A1, A2 & A3 before etching, focusing on the reverse biased portion

Figure 5.22: Comparison between the I/V curves of group A1, A2 & A3 after etching

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Figure 5.23: Comparison between the I/V curves of group A1, A2 & A3 after etching, focusing on the reverse biased portion

Figure 5.24: Comparison between the I/V curves of group A1, A2 & A3 samples before and after etching

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Figure 5.25: Comparison between the I/V curves of group A1, A2 & A3 samples before and after etching, with the reverse biased portion on focus

The I/V curves of group A before and after etching process, obtained from experimental results, are compared in logarithmic scale with the ideal I/V retrieved from the simulation results using MEDICI, as shown in Fig 5.26 and 5.27 below.

From the Fig 5.26 and 5.27, it can be observed that compared with the $\log I/V$ curves before etching, the $\log I/V$ curves of group A after etching are much closer to the ideal curve in the reverse biased region, which indicates the dramatic improvement of the device performance through etching process.

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Figure 5.26: Comparison between the $\log I/V$ curves of group A1, A2 & A3 samples before etching with the ideal curve

Figure 5.27: Comparison between the $\log I/V$ curves of group A1, A2 & A3 samples after etching with the ideal curve

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5.2.1.5 C/V measurement results of group A

Figure 5.28: Comparison between the C/V curves of group A1, A2 & A3 samples

5.2.1.6 Generation lifetime of group A1, A2 and A3

The generation lifetime of group A1, A2 and A3 is calculated, and is shown in the Fig 5.29, 5.30, and 5.31.

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Figure 5.29: Generation lifetime of group A1

Figure 5.30: Generation lifetime of group A2

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Figure 5.31: Generation lifetime of group A3

Group A is designed to monitor the effect of annealing duration on the electrical properties of the diode. The annealing duration for group A1, A2 and A3 are 2, 3 and 4 hours, respectively, while all the other conditions are kept the same. From Figures 5.29-5.31, we see that the generation lifetime of the three groups increases drastically when the depletion distance goes beyond 10 μm , which implies that the bonding interface defects are cluster within the region of 10 μm from the bonding interface into the p-type wafer (defect region).

From Figures 5.29-5.31, it can also be observed that the generation lifetime in the defect region is increasing as the annealing time increases. The generation lifetime of group A3 in the defect region is the largest among the three groups, which is about 5×10^{-10} second.

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Also, the generation lifetime of group A1 and A2 has no significant difference, and is much lower than that of group A3. **This implies that the annealing time for group A2 (3 hours) is not long enough to achieve good performance.**

The generation lifetime results are in good agreement with the experimental results shown in Fig 5.23, in which group A3 shows smaller leakage current comparing with the other two groups

5.2.2 Results of group B

Similar with the previous section with group A, the I/V and C/V characteristics are measured for samples of group B, and the results of group B1, B2 and B3 are shown below. Generation lifetime is also calculated.

5.2.2.1 I/V measurement results of group B1

Similarly with samples in group A, the samples in group B1 are also etched to ensure a low leakage current. Both I/V curves measured before and after the etching process are shown in the Figure below, and it can be observed that there is a big reduction of the leakage current value after etching.

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Figure 5.32: I/V curves of group B1 before & after etching

Figure 5.33: I/V curve of group B1, focusing on the reverse biased portion

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5.2.2.2 I/V measurement results of group B2

Figure 5.34: I/V curves of group B2 before & after etching.

Figure 5.35: I/V curve of group B2, focusing on the reverse biased portion

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5.2.2.3 *I/V* measurement results of group B3

The *I/V* curves of group B3 is shown in Fig 5.36. From this graph, it can be seen that the breakdown voltage of samples in group B3 is very low comparing with B1 and B2. Besides, the PN junction samples are very difficult to turn on at the forward bias. It is believed that the low breakdown voltage is due to the precipitation of oxygen in the silicon as can be seen from Fig 5.45 that the defect region extended beyond the typical defect regions (10 μ m) due to wafer bonding as established earlier.

Figure 5.36: *I/V* curves of group B3 before & after etching

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Figure 5.37: I/V curve of group B3, focusing on the reverse biased portion

5.2.2.4 Comparison between group B1, B2 and B3

The I/V curves of group B1, B2 and B3 are compared. Ideal I/V curve is obtained by simulation using MEDICI, and the logarithm values are used for comparison between the ideal I/V and the experimental results. The C/V curves are also compared in Fig 5.42. From Fig 5.38 and 5.39, it can be seen that the I/V curves of group B1 and B2 are very similar, with larger breakdown voltage and smaller leakage current as compared to group B3. Group B3 shows very poor electrical performance here.

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Figure 5.38: Comparison between the I/V curves of group B1, B2 & B3 samples before and after etching

Figure 5.39: Comparison between the I/V curves of group B1, B2 & B3 samples before and after etching, with the reverse biased portion on focus

Similar with group A, the I/V curves of group B before and after etching process, obtained from experimental results, are also compared in logarithmic scale with the

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ideal I/V retrieved from the simulation results using MEDICI, as shown in Fig 5.40 and 5.41 below.

From the Fig 5.40 and 5.41, it can be observed that the device performance is improved after etching.

Figure 5.40: Comparison between the $\log I/V$ curves of group B1, B2 & B3 samples before etching with the ideal curve

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Figure 5.41: Comparison between the logI/V curves of group B1, B2 & B3 samples after etching with the ideal curve

5.2.2.5 C/V measurement results of group B

Figure 5.42: Comparison between the C/V curves of selected group B samples

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5.2.2.6 Generation lifetime of group B1, B2 and B3

Figure 5.43: Generation lifetime of group B1

Figure 5.44: Generation lifetime of group B2

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Figure 5.45: Generation lifetime of group B3

The effect of annealing temperature is investigated with group B. The annealing temperature for group B1, B2 and B3 are 300°C, 400°C and 500°C, respectively, while all the other conditions are kept constant. From the generation lifetime graph of group B, the size of the defect region of group B is similar to that of group A and group B2 has the best performance with highest level of generation lifetime. **Therefore, it can be concluded that within the range from 300°C to 400°C, higher annealing temperature will results in better performance.** But annealing temperature beyond 400°C will induce oxygen precipitation, causing an increase in the leakage current, lower the reverse breakdown voltage and extend the region of defect. Therefore, while it is generally good to have higher annealing temperature to reduce the defects, too high the temperature is not advisable.

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5.2.3 Results of group C

Similar with the previous section with groups A and B, the I/V and C/V characteristics are measured for samples of group C, and the results of group C1 and C3 are shown below. Early breakdown occurs in the samples of group C2 with extremely large leakage current, which may be due to surface contamination before bonding or small voids existing at the interface. Therefore, the results of group C2 are not further analyzed. Generation lifetime is also calculated.

5.2.3.1 I/V measurement results of group C1

Similar with samples in both group A and B, the samples in group C1 are also etched to ensure a low leakage current. Both I/V curves measured before and after the etching process are shown in the Figure below, and one can observe that there is a significant reduction in the leakage current after etching process.

Figure 5.46: I/V curves of group C1 before & after etching

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Figure 5.47: I/V curve of group C1, focusing on the reverse biased portion

5.2.3.2 I/V measurement results of group C3

Figure 5.48: I/V curves of group C3 before & after etching

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Figure 5.49: I/V curve of group C3, focusing on the reverse biased portion

5.2.3.3 Comparison between group C1 and C3

The I/V curves of group C1 and C3 are compared in both linear and log scale. Logarithm values are adopted to show the difference between the I/V curves of group C1 and C3 more clearly. From Fig 5.50, it can be seen that the reverse biased part of the linear I/V curves of group C1 and C3 are very close to each other, with differences between these two are in scale of 10^{-6} . Group C2 shows very poor electrical performance and is not selected for comparison in this case.

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Figure 5.50: Comparison between the $\log I/V$ curves of group C1& C3 samples before and after etching process

Figure 5.51: Comparison between the I/V curves of group C1 & C3 samples before and after etching, with the reverse biased portion on focus

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5.2.3.4 Generation lifetime of group C1 and C3

Figure 5.52: Generation lifetime of group C1

Figure 5.53: Generation lifetime of group C3

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Experiment of Group C is designed to investigate the effect of heating rate during annealing process on the electrical properties of the diode. The heating rate for group C1, C2 and C3 are 25, 12.5 and 6.25°C/min respectively, while all the other conditions are kept the same.

From Fig 5.52 and 5.53, one can see that there is an obvious increase in the generation lifetime of the two groups, group C1 and C3, when the depletion distance goes beyond 9~10 μm , similar to groups A and B.

Besides, from Fig 5.52 and 5.53, it can be observed that there is no significant difference between the generation lifetime in the defect region of group C1 and C3, which agrees with the I/V measurement results. The generation lifetime of both groups in the defect region fluctuates in the range of $1 \times 10^{-10} \sim 4 \times 10^{-10}$ second with average lifetime time around 2×10^{-10} second. This implies that the heating rate may not be a significant affecting factor to the generation lifetime of the PN junction diode.

However, from the I/V measurement results, the Peak Inverse Value (PIV) for group C1 and C3 when the leakage current reaches 1 μA is -98.5 volts and -23 volts. Besides, the breakdown voltage (V_{br}) of group C1 is around 200 volts while that of group C3 is larger than 200 volts but cannot be measured as it is beyond the functional limitation of the equipment (-200 volts). Therefore, one can see that the heating rate does have an influence on the PIV and V_{br} .

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5.2.4 Results of group D

Both the I/V and C/V characteristics are measured for samples of group D, and the results of group D1 and D3 are shown below. The samples of group D2 are not performing well during the I/V measurement with early breakdown and very large leakage current observed, which may due to surface contaminations or small voids at the interface. Therefore, the results of group D2 are not analyzed further.

Besides micro voids, metal contamination at the interface will also lead to large leakage current early breakdown [81]. DLTS is applied in this project to identify the contamination at the bonding interface and metal contaminations have been detected at the interface. The author has tried to apply DLTS analysis on sample groups C4-C6 and D4-D6. However, the sample groups are not examinable with DLTS machine because their large leakage current goes beyond the maximum allowable leakage current of the equipment and will lead to great harm to the equipment due to its functional limitation.

5.2.4.1 I/V measurement results of group D1

The I/V measurement results of sample group D1 are shown below, including both curves before and after etching process. Much lower leakage current is obtained after etching process comparing with that measured before etching process, leading to a much better electrical performance of the PN junction diode.

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Figure 5.54: I/V curves of group D1 before & after etching

Figure 5.55: I/V curve of group D1, focusing on the reverse biased portion

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5.2.4.2 *I/V* measurement results of group D3

Figure 5.56: *I/V* curves of group D3 before & after etching

Figure 5.57: *I/V* curve of group D3, focusing on the reverse biased portion

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5.2.4.3 Comparison between group D1 and D3

The I/V curves of group D1 and D3 are compared in both linear and log scale. Not much difference can be found in the range of 0 to -90 volts from Fig 5.58 as the reverse biased portion of the linear I/V curves of group D1 and D3 in this region are very close to each other. Breakdown voltages of these two samples groups are also quite similar. Logarithm values are used to show the difference between the I/V curves of group D1 and D3 as well.

From the I/V measurement results of group D, the Peak Inverse Value (PIV) for group D1 and D3 when the leakage current reaches $5\ \mu\text{A}$ corresponds to -6 volts and -9.5 volts respectively. On the other hand, the breakdown voltage (V_{br}) for group D1 and D3 are -160 volts and -130 volts respectively. **Therefore, one can deduce that the cooling rate may not play an important role in affecting the electrical behavior of the diode.**

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Figure 5.58: Comparison between the I/V curves of group D1 & D3 samples before and after etching, with the reverse biased portion on focus

Figure 5.59: Comparison between the $\log I/V$ curves of group D1 & D3 samples before and after etching process

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5.2.4.4 Generation lifetime of group D1 and D3

Figure 5.60: Generation lifetime of group D1

Figure 5.61: Generation lifetime of group D3

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The effect of cooling rate during annealing process on the electrical performance of the PN junction diode is studied through experiment of Group D. The cooling rate for group D1, D2 and D3 are 62.5, 53.5 and 41.7°C/hour respectively, while all the other experimental conditions are kept the same. As mentioned in the previous section, the measurement results of group D2 are not used for the comparison or calculation due to the extremely large leakage current and early breakdown voltage occurred in I/V measurement. The interface contaminations introduced during cleaning or bonding processes is possibly the main cause for the unqualified electrical behavior of sample group D2. The cooling rate for group D1, that is, 62.5°C/hour is the naturally cooling rate in vacuum, and the fastest cooling rate is the maximum rate the vacuum furnace can achieve.

From Fig 5.60 and 5.61, similar with the other experimental groups A, B and C, an obvious increase in the generation lifetime can be observed when the depletion distance reaches around 9 μm .

As shown in Fig 5.60 and 5.61 that the generation lifetime in the defect region of group D1 and D3 is very similar, which agrees with their experimental I/V results very well.

5.3 Results of Deep-Level Transient Spectroscopy

DLTS analysis was carried out with the samples of the best or worst performance from each experimental group. For group A, the best and worst samples are from group A1 and A3 respectively, while the best and worst samples of group B are corresponding to B2 and B3. Similar for group C, the best and worst samples are selected from C1 and C3 respectively. Temperature scanning for all the groups is done and the results are shown in Fig 5.62-5.64. The reverse voltage, pulse voltage and pulse time for the temperature scanning are -3 volts, -0.50 volts and 50 ms respectively.

For simplicity, the best sample in group A is symbolized as A_{best} , while the worst sample is represented as A_{worst} . Similarly, the best and worst samples of group B and C are symbolized as B_{best} , B_{worst} , C_{best} and C_{worst} respectively. Due to the large leakage current occurs in group D which is beyond the measurement capability of the DLTS system, the DLTS analysis results of group D will not be included in this work

Arrhenius plots are generated according to the temperature scanning results and are shown in Fig 5.65 to 5.67. Activation energy E_T and density N_T of the interface defects are therefore obtained and listed in Table 2. Because the samples are of PN^+ junction diodes, the depletion region is mainly in P-side when the samples are reverse-biased. Therefore the reference energy level of E_T is the valence band (E_V).

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Figure 5.62: Temperature scanning graphs of A_{best} and A_{worst}

Figure 5.63: Temperature scanning graphs of B_{best} and B_{worst}

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Figure 5.64: Temperature scanning graphs of C_{best} and C_{worst}

From Fig 5.62, it can be seen that the both the position and the shape of the DLTS signal versus temperature plots are different between the best and worst samples of group A. One can also observe that there are two obvious peaks shown in both of the temperature scanning graphs in Fig 5.62, implying that there are two types of defects existing. The activation energy and density of the defects can be obtained from the plot of A_{best} . However, due to the leakage current, neither the activation energy nor the density of the defect corresponding to the lower peak in the temperature scanning graph of A_{worst} can be obtained.

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Figure 5.65: Arrhenius plots of A_{best} and A_{worst}

Figure 5.66: Arrhenius plots of B_{best} and B_{worst}

Figure 5.67: Arrhenius plot of C_{best} and C_{worst}

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Arrhenius plots of the best and worst samples from group A, B and C are shown in Fig 5.65, 5.66 and 5.67. The activation energy and defect density of each sample is listed in the Table below.

Table 5.1 Activation energy, majority carrier cross capture section and defect density of the best and worst samples from each experimental group

Sample Group		E_T (eV)	σ_{maj} (cm ²)	N_T (cm ⁻³)	Possible Defect	Reference
A	Best	0.34	5.90×10^{-18}	1.30×10^{11}	Dislocation	[55]
		0.29	5.90×10^{-18}	3.82×10^{10}	Fe	[55]
	Worst	0.34	4.24×10^{-19}	6.67×10^{12}	Dislocation	[55]
B	Best	0.41	1.83×10^{-11}	3.18×10^{13}	Al-O pair	[71, 72]
	Worst	0.40	2.66×10^{-7}	1.30×10^{14}	Al-O pair	[71, 72]
C	Best	0.35	3.35×10^{-13}	2.21×10^{11}	Au	[55]
	Worst	0.21	2.19×10^{-17}	6.60×10^{10}	Vacancy pair	[55]

As shown in Table 5.1, two kinds of hole traps are detected in A_{best} with activation energy of H_1 (0.34eV) and H_2 (0.29eV), which may be identified as dislocation and Fe [55]. The hole trap detected in A_{worst} is of the same activation energy level with H_1 (0.34eV) and is supposed to be of the same type with H_1 (0.34eV). The defect density of H_1 (0.34eV) in A_{worst} is 50 times more than that in A_{best} , which agrees with the I/V measurement results showing that the leakage current of A_{best} is much smaller than that of A_{worst} . The density of the other type of defect H_2 (0.29eV) detected in A_{best} is much smaller comparing with that of H_1 (0.34eV), and does not play an important role in degrading the PN junction diode performance.

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The energy levels of the hole traps detected in B_{best} and B_{worst} are very similar with each other, and may be of the same type, H_3 (0.41eV) which is suspected to be Al-O pair. The defect density of H_3 (0.41eV) in B_{best} is much smaller than that in B_{worst} , which is in good agreement with the I/V measurement results because the leakage current of B_{best} is much smaller than that of B_{worst} . The Al is found to be from the wafer surface introduced during the pre-treatment before the high temperature process. The presence of oxygen also confirms the annealing induced oxygen precipitation earlier.

It can be observed that there are two kinds of hole traps detected in C_{best} and C_{worst} , H_4 (0.35eV) and H_5 (0.21eV). H_4 (0.35eV) is suspected to be Au, while H_5 (0.21eV) may be vacancy-vacancy by comparing with the data given in [55].

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5.4 Summary

Low temperature medium vacuum wafer bonding was performed and the effects of the four important experimental parameters, i.e. annealing temperature, annealing duration, heating and cooling rate, were investigated experimentally through DOE. I/V and C/V techniques were applied to calculate the generation lifetime at the bonding interface of the PN junction devices, while DLTS was used to obtain the density and energy of the interface defects.

Chapter 6 CONCLUSION AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Conclusion

Compare with the conventional diode fabrication process, it was found that with the medium vacuum wafer bonding technique, the energy saving of producing even the standard power diodes will be tremendous since only temperature below 400°C and duration of less than 5 hours are needed as compared to the standard fabrication process of above 1000°C and more than 30 hours of diffusion. The bonding quality is also improved dramatically and stronger bonding strength can be achieved.

In this report, PN junction fabrication experiment using Medium Vacuum Wafer Bonding technique are carried out to characterize the effect of different experimental conditions, including heating and cooling rate, annealing temperature and duration, on the electrical properties of the diode.

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C SAM is applied to map the spatial distribution of voids at the bonding interface, and dicing saw is used for cutting out the samples. Generation carrier lifetime, which is closely related to the leakage current and the interface defect density, is determined by using I/V and C/V profiling techniques. The measurement and calculation results are both shown and discussed in this report. MEDICI simulation has also been applied to provide the ideal I/V behavior of PN junction for comparison with the experimental results obtained. DLTS analysis has also been carried out for the retrieval of energy and density of interface defects.

From the study, one can see that the defect region due to wafer bonding is around 10 μm . The severity of the defects is reduced with larger annealing time. No significant different on the defect density for annealing temperature between 300-400°C. However, too high the temperature (above 400°C) will induce oxygen precipitate, and increase the amount of defects. Also, it is found that the rate of temperature increases during the annealing does not have any significant effect on the defects severity. The best generation lifetime for the bonded PN junction obtained so far is 0.5 ns, and the smallest defect region is 9 μm . The smallest reverse leakage current is 6.3 $\mu\text{A}@200\text{V}$ in comparison to 3.44 $\mu\text{A}@200\text{V}$ for the ideal diode of the same doping composition. The generation carrier lifetime assigned for simulation is 4 ns, which is corresponding to the highest generation carrier lifetime obtained from the experimental results of the non-defect region (around 10 μm away from the interface). It is also found from the results of group C and D that although the Heating rate and Cooling rate may not affect the leakage current and generation lifetime of the devices significantly, they do affect the PIV

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and V_{br} . Table 6.1 below shows the corresponding PIV, V_{br} and their ratio for all the experimental groups, with ideal PIV at -182 volts at $-5\mu A$.

Table 6.1: Values of some other electrical performance indexes

Group Name		PIV (v)	V_{br} (v)	PIV/ V_{br}	PIV _{actual} /PIV _{ideal}
A	A1	-2.5@5 μA	-120	2.08×10^{-2}	1.37×10^{-2}
	A2	-1.0@5 μA	-195	5.13×10^{-3}	5.49×10^{-3}
	A3	-1.5@5 μA	---	---	8.24×10^{-3}
B	B1	-2.5@5 μA	---	---	1.37×10^{-2}
	B2	-7.0@5 μA	---	---	3.85×10^{-2}
	B3	-0.5@5 μA	-100	5.00×10^{-3}	2.75×10^{-3}
C	C1	-98.5@1 μA	-200	4.93×10^{-1}	5.41×10^{-1}
	C3	-23.0@1 μA	---	---	1.26×10^{-1}
D	D1	-6.0@5 μA	-160	3.75×10^{-2}	3.30×10^{-2}
	D3	-9.5@5 μA	-130	7.31×10^{-2}	5.22×10^{-2}

6.2 Recommendation for Future Work

In this thesis, MVWB conditions have been optimized to achieve better electrical properties of bonding interface and therefore, the electrical performance of power diodes. Simulation has also been carried out to compare the electrical behavior of different non-standard power device structures and to decide the optimized device parameters of the devices. However, it is by no means exhaustive, and some more work still needs to be further investigated.

❖ Auto-bonding of MVWB

In our work, wafer bonding in the air is operated manually, which may cause misalignment and scratch to the interface of the two bonded wafer pair during the bonding process. Auto-bonding is suggested for more accurate process and better bonding interface properties.

❖ In-situ MVWB

Particles and contaminants in the environmental air can cause severe bubble problem to the bonding interface of the wafer pair. Therefore, in-situ MVWB is recommended to improve the bonding quality and electrical performance of the devices.

❖ Characterization Methods

The I/V and C/V measurement carried out in our work is done in the air using probe station instead of vacuum. In this case, leakage current and noise may be induced during the measurement process and cause error.

The vacuum probe station for measurement was not available for the author to use. However, the facilities used in this project can help to reduce the noise generated during the measurement using cables with less signal loss. Pins of the very probe station are made of gold to ensure good conduction between the sample contact and the cables. Besides, during the fabrication of sample dice, edge damage has been etched away to reduce the leakage

current caused by the electric field generated around the dice under large voltage supply. Therefore, the impact on accuracy is insignificant. *IV* profiling of sample group A3.1 using DLTS (vacuum chamber) has been carried out to verify the impact on accuracy. Graph below shows comparable measurement results from Probe station and DLTS.

Figure 6.1: Comparison of *IV* curves of DLTS and Probe station

Author's Publications

- [1] Cher Ming Tan, Lina Sun, Guangyu Huang and Nagarajan Raghavan, "The physical limit and manufacturability of power diode with carrier lifetime control," *2nd IEEE Conference on Industrial Electronics and Applications (ICIEA 2007)*
- [2] Cher Ming Tan, Sun Lina, "Going Green for Discrete Power Diode Manufactures", *IEEE ICIEA 2009*, China.

Appendix

Appendix A: RSM EQUATIONS FOR THE STANDARD DIODE

$$\begin{aligned}
 V_R = & -62612.0 + 3.03t_1 - 29.22t_2 - 2.43t_6 + 221.16 \log_{10}(N_a^+) + 7759.25 \log_{10}(N_d) \\
 & - 0.0109t_1^2 - 0.000920t_1t_2 + 0.0000172t_1t_6 - 0.0865t_1 \log_{10}(N_a^+) - 0.00183t_1 \log_{10}(N_d) \\
 & + 0.00873t_2^2 + 0.0000989t_2t_6 + 0.324t_2 \log_{10}(N_a^+) + 1.29t_2 \log_{10}(N_d) + 0.00000642t_6^2 \\
 & + 0.062t_6 \log_{10}(N_a^+) + 0.075t_6 \log_{10}(N_d) - 9.41 \log_{10}^2(N_a^+) + 3.69 \log_{10}(N_a^+) \log_{10}(N_d) \\
 & - 247.14 \log_{10}^2(N_d)
 \end{aligned} \tag{1}$$

$$\begin{aligned}
 V_f = & 13.37 + 0.00362t_1 + 0.0013t_2 + 0.00099t_6 - 0.634 \log_{10}(N_a^+) - 0.855 \log_{10}(N_d) \\
 & + 0.00000160t_1^2 + 0.00000134t_1t_2 + 1.72 \times 10^{-8}t_1t_6 - 0.00020t_1 \log_{10}(N_a^+) \\
 & + 0.00000315t_1 \log_{10}(N_d) + 0.00000983t_2^2 - 7.77 \times 10^{-7}t_2t_6 - 0.0000146t_2 \log_{10}(N_a^+) \\
 & - 0.0000803t_2 \log_{10}(N_d) + 2.94 \times 10^{-7}t_6^2 - 0.0000126t_6 \log_{10}(N_a^+) - 0.000073t_6 \log_{10}(N_d) \\
 & + 0.00763 \log_{10}^2(N_a^+) + 0.0226 \log_{10}(N_a^+) \log_{10}(N_d) + 0.0147 \log_{10}^2(N_d)
 \end{aligned} \tag{2}$$

$$t_s = 1 \times 10^{-8} \left(\begin{aligned} & 3.26 - 0.00218t_1 + 0.113t_2 + 0.0354t_6 + 3.43 \log_{10}(N_a^+) - 6.53 \log_{10}(N_d) \\ & + 0.000112t_1^2 - 0.0000725t_1t_2 - 0.00000330t_1t_6 + 0.0000275t_1 \log_{10}(N_a^+) \\ & + 0.000114t_1 \log_{10}(N_d) - 0.000111t_2^2 - 0.0000200t_2t_6 + 0.000314t_2 \log_{10}(N_a^+) \\ & - 0.00404t_2 \log_{10}(N_d) + 0.00000160t_6^2 + 0.00000722t_6 \log_{10}(N_a^+) \\ & - 0.00221t_6 \log_{10}(N_d) - 0.0669 \log_{10}^2(N_a^+) - 0.0522 \log_{10}(N_a^+) \log_{10}(N_d) \\ & + 0.290 \log_{10}^2(N_d) \end{aligned} \right) \tag{3}$$

$$t_{rr} = 1 \times 10^{-8} \left(\begin{aligned} & -14023.8 + 2.11t_1 + 22.68t_2 + 0.505t_6 + 719.68 \log_{10}(N_a^+) \\ & + 662.58 \log_{10}(N_d) - 0.0184t_1^2 - 0.0000875t_1t_2 - 0.00000301t_1t_6 \\ & - 0.00297t_1 \log_{10}(N_a^+) - 0.000975t_1 \log_{10}(N_d) + 0.0215t_2^2 - 0.0320t_2t_6 \\ & - 0.0145t_2 \log_{10}(N_a^+) - 0.0381t_2 \log_{10}(N_d) + 0.00288t_6^2 \\ & - 0.000320t_6 \log_{10}(N_a^+) - 0.0691t_6 \log_{10}(N_d) - 17.29 \log_{10}^2(N_a^+) \\ & - 2.71 \log_{10}(N_a^+) \log_{10}(N_d) - 17.58 \log_{10}^2(N_d) \end{aligned} \right) \tag{4}$$

Appendix

$$\begin{aligned}
S = & -4915.94 + 0.736t_1 + 7.85t_2 + 0.132t_6 + 247.83 \log_{10}(N_a^+) + 240.10 \log_{10}(N_d) \\
& - 0.00662t_1^2 + 0.000119t_1t_2 + 0.00000215t_1t_6 - 0.00115t_1 \log_{10}(N_a^+) \\
& - 0.000193t_1 \log_{10}(N_d) + 0.00777t_2^2 - 0.0112t_2t_6 - 0.00994t_2 \log_{10}(N_a^+) \\
& - 0.00532t_2 \log_{10}(N_d) + 0.00102t_6^2 - 0.000127t_6 \log_{10}(N_a^+) - 0.0220t_6 \log_{10}(N_d) \\
& - 6.08 \log_{10}^2(N_a^+) - 0.595 \log_{10}(N_a^+) \log_{10}(N_d) - 6.69 \log_{10}^2(N_d)
\end{aligned} \tag{5}$$

$$\begin{aligned}
M_1 = & -6.48 \times 10^8 - 255965.0t_1 - 149889.0t_2 - 423707.0t_6 + 1.01 \times 10^8 \log_{10}(N_a^+) \\
& - 1.96 \times 10^7 \log_{10}(N_d) + 634.21t_1^2 + 2132.96t_1t_2 + 39.14t_1t_6 - 6896.3t_1 \log_{10}(N_a^+) \\
& - 525.93t_1 \log_{10}(N_d) + 2129.38t_2^2 + 475.32t_2t_6 - 59160.0t_2 \log_{10}(N_a^+) \\
& + 3768.89t_2 \log_{10}(N_d) + 63.91t_6^2 - 770.0t_6 \log_{10}(N_a^+) + 15845.1t_6 \log_{10}(N_d) \\
& - 565066.0 \log_{10}^2(N_a^+) - 4.50 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_d) + 3.25 \times 10^6 \log_{10}^2(N_d)
\end{aligned} \tag{6}$$

$$\begin{aligned}
M_2 = & 3.02 \times 10^8 - 210370.0t_1 - 615261.0t_2 - 52742.9t_6 - 7.56 \times 10^6 \log_{10}(N_a^+) \\
& - 2.27 \times 10^7 \log_{10}(N_d) + 55.58t_1^2 + 136.46t_1t_2 + 5.47t_1t_6 + 9485.19t_1 \log_{10}(N_a^+) \\
& - 540.37t_1 \log_{10}(N_d) - 385.37t_2^2 + 222.43t_2t_6 + 2280.71t_2 \log_{10}(N_a^+) + 27939.3t_2 \log_{10}(N_d) \\
& - 28.31t_6^2 + 850.0t_6 \log_{10}(N_a^+) + 3388.31t_6 \log_{10}(N_d) + 82383.8 \log_{10}^2(N_a^+) \\
& + 118600.0 \log_{10}(N_a^+) \log_{10}(N_d) + 630845.0 \log_{10}^2(N_d)
\end{aligned} \tag{7}$$

$$\begin{aligned}
M_3 = & -1.23 \times 10^{15} - 1.14 \times 10^{11}t_1 + 5.01 \times 10^{12}t_2 - 2.51 \times 10^{11}t_6 + 1.49 \times 10^{14} \log_{10}(N_a^+) \\
& - 4.70 \times 10^{13} \log_{10}(N_d) + 1.04 \times 10^9t_1^2 - 46118.3t_1t_2 - 202592.0t_1t_6 \\
& - 1.94 \times 10^6t_1 \log_{10}(N_a^+) - 265926.0t_1 \log_{10}(N_d) - 1.26 \times 10^9t_2^2 + 148667.0t_2t_6 \\
& - 2.45 \times 10^{11}t_2 \log_{10}(N_a^+) - 7.44 \times 10^6t_2 \log_{10}(N_d) + 7.19 \times 10^7t_6^2 - 740083.0t_6 \log_{10}(N_a^+) \\
& + 7.67 \times 10^9t_6 \log_{10}(N_d) - 3.15 \times 10^{12} \log_{10}^2(N_a^+) - 9.24 \times 10^8 \log_{10}(N_a^+) \log_{10}(N_d) \\
& + 1.28 \times 10^{12} \log_{10}^2(N_d)
\end{aligned} \tag{8}$$

$$\begin{aligned}
I_{RM} = & -0.0953 - 0.0000553t_1 - 0.000113t_2 + 0.0000400t_6 - 0.00903 \log_{10}(N_a^+) \\
& + 0.0228 \log_{10}(N_d) - 1.16 \times 10^{-7}t_1^2 - 6.88 \times 10^{-8}t_1t_2 + 8.99 \times 10^{-8}t_1t_6 \\
& - 3.64 \times 10^{-7}t_1 \log_{10}(N_a^+) - 2.33 \times 10^{-8}t_1 \log_{10}(N_d) - 5.94 \times 10^{-7}t_2^2 + 6.23 \times 10^{-8}t_2t_6 \\
& + 0.0000204t_2 \log_{10}(N_a^+) - 0.00000826t_2 \log_{10}(N_d) - 7.70 \times 10^{-9}t_6^2 \\
& - 8.55 \times 10^{-8}t_6 \log_{10}(N_a^+) - 0.00000247t_6 \log_{10}(N_d) + 0.000123 \log_{10}^2(N_a^+) \\
& + 0.0000868 \log_{10}(N_a^+) \log_{10}(N_d) - 0.000699 \log_{10}^2(N_d)
\end{aligned} \tag{9}$$

Appendix B: RSM EQUATIONS FOR THE SPEED DIODE

$$\begin{aligned}
V_R = & -52216.6 - 4.78t_1 - 59.24t_2 - 7.99t_3 + 550.20 \log_{10}(N_a^+) + 1508.22 \log_{10}(N_a) \\
& + 4398.81 \log_{10}(N_d) - 134.08 \log_{10}(N_d^+) - 1.76t_5 + 0.0457t_1^2 - 0.172t_1t_2 - 0.0199t_1t_3 \\
& - 0.735t_1 \log_{10}(N_a^+) + 0.183t_1 \log_{10}(N_a) + 1.066t_1 \log_{10}(N_d) + 0.0665t_1 \log_{10}(N_d^+) \\
& + 0.00203t_1t_5 + 0.0575t_2^2 + 0.0143t_2t_3 + 0.363t_2 \log_{10}(N_a^+) + 3.49t_2 \log_{10}(N_a) \\
& - 1.40t_2 \log_{10}(N_d) + 0.708t_2 \log_{10}(N_d^+) - 0.00217t_2t_5 + 0.00529t_3^2 - 0.0325t_3 \log_{10}(N_a^+) \\
& + 0.0188t_3 \log_{10}(N_a) + 0.729t_3 \log_{10}(N_d) - 0.318t_3 \log_{10}(N_d^+) + 0.00129t_3t_5 \\
& + 8.12 \log_{10}^2(N_a^+) - 17.98 \log_{10}(N_a^+) \log_{10}(N_a) - 8.55 \log_{10}(N_a^+) \log_{10}(N_d) \\
& - 17.97 \log_{10}(N_a^+) \log_{10}(N_d) - 0.216t_5 \log_{10}(N_a^+) - 49.13 \log_{10}^2(N_a) \\
& + 9.03 \log_{10}(N_a) \log_{10}(N_d) + 10.32 \log_{10}(N_a) \log_{10}(N_d^+) + 0.199t_5 \log_{10}(N_a) \\
& - 133.73 \log_{10}^2(N_d) + 1.16 \log_{10}(N_d) \log_{10}(N_d^+) + 0.0344t_5 \log_{10}(N_d) + 7.68 \log_{10}^2(N_d^+) \\
& + 0.0910t_5 \log_{10}(N_d^+) + 0.000474t_5^2
\end{aligned} \tag{10}$$

$$\begin{aligned}
V_f = & 45.62 - 0.043t_1 + 0.126t_2 + 0.143t_3 - 0.299 \log_{10}(N_a^+) - 2.12 \log_{10}(N_a) \\
& - 3.42 \log_{10}(N_d) + 0.0396 \log_{10}(N_d^+) - 0.0170t_5 + 0.000122t_1^2 - 0.000270t_1t_2 \\
& - 0.00000396t_1t_3 - 0.000306t_1 \log_{10}(N_a^+) + 0.00162t_1 \log_{10}(N_a) + 0.00222t_1 \log_{10}(N_d) \\
& - 0.0012t_1 \log_{10}(N_d^+) + 0.0000525t_1t_5 + 0.000195t_2^2 + 0.0000655t_2t_3 \\
& - 0.00119t_2 \log_{10}(N_a^+) - 0.00395t_2 \log_{10}(N_a) - 0.00270t_2 \log_{10}(N_d) \\
& + 0.000167t_2 \log_{10}(N_d^+) + 0.00000825t_2t_5 + 0.0000104t_3^2 + 0.000348t_3 \log_{10}(N_a^+) \\
& - 0.00183t_3 \log_{10}(N_a) - 0.00682t_3 \log_{10}(N_d) - 0.0000648t_3 \log_{10}(N_d^+) - 0.00000736t_3t_5 \\
& + 0.0315 \log_{10}^2(N_a^+) + 0.0176 \log_{10}(N_a^+) \log_{10}(N_a) + 0.00228 \log_{10}(N_a^+) \log_{10}(N_d) \\
& - 0.0660 \log_{10}(N_a^+) \log_{10}(N_d) + 0.000147t_5 \log_{10}(N_a^+) + 0.00832 \log_{10}^2(N_a) \\
& + 0.0859 \log_{10}(N_a) \log_{10}(N_d) + 0.00696 \log_{10}(N_a) \log_{10}(N_d^+) + 0.00043t_5 \log_{10}(N_a) \\
& + 0.0552 \log_{10}^2(N_d) + 0.0241 \log_{10}(N_d) \log_{10}(N_d^+) + 0.000263t_5 \log_{10}(N_d) \\
& + 0.0197 \log_{10}^2(N_d^+) + 0.0000243t_5 \log_{10}(N_d^+) + 0.00000195t_5^2
\end{aligned} \tag{11}$$

$$t_s = 1 \times 10^{-8} \left(\begin{aligned}
& 0.355 - 0.730t_1 - 0.580t_2 + 0.193t_3 + 2.63 \log_{10}(N_a^+) + 7.61 \log_{10}(N_a) \\
& + 11.53 \log_{10}(N_d) - 15.80 \log_{10}(N_d^+) - 0.0292t_5 + 0.00156t_1^2 + 0.00103t_1t_2 \\
& - 0.000361t_1t_3 + 0.0141t_1 \log_{10}(N_a^+) + 0.00695t_1 \log_{10}(N_a) \\
& - 0.0102t_1 \log_{10}(N_d) + 0.0202t_1 \log_{10}(N_d^+) + 0.0000275t_1t_5 + 0.00129t_2^2 \\
& - 0.000323t_2t_3 + 0.0149t_2 \log_{10}(N_a^+) + 0.00478t_2 \log_{10}(N_a) \\
& - 0.00673t_2 \log_{10}(N_d) + 0.0124t_2 \log_{10}(N_d^+) - 0.00000720t_2t_5 \\
& - 0.00000894t_3^2 - 0.00474t_3 \log_{10}(N_a^+) - 0.000759t_3 \log_{10}(N_a) \\
& + 0.00177t_3 \log_{10}(N_d) - 0.00428t_3 \log_{10}(N_d^+) - 0.0000104t_3t_5 \\
& - 0.171 \log_{10}^2(N_a^+) + 0.0212 \log_{10}(N_a^+) \log_{10}(N_a) \\
& - 0.0988 \log_{10}(N_a^+) \log_{10}(N_d) + 0.230 \log_{10}(N_a^+) \log_{10}(N_d^+) \\
& + 0.00027t_5 \log_{10}(N_a^+) - 0.277 \log_{10}^2(N_a) - 0.0941 \log_{10}(N_a) \log_{10}(N_d) \\
& + 0.0865 \log_{10}(N_a) \log_{10}(N_d^+) + 0.000713t_5 \log_{10}(N_a) - 0.126 \log_{10}^2(N_d) \\
& - 0.195 \log_{10}(N_d) \log_{10}(N_d^+) - 0.000410t_5 \log_{10}(N_d) + 0.307 \log_{10}^2(N_d^+) \\
& + 0.00119t_5 \log_{10}(N_d^+) - 0.00000713t_5^2
\end{aligned} \right) \tag{12}$$

Appendix

$$t_{rr} = 1 \times 10^{-8} \left(\begin{aligned} &-84.43 + 0.189 t_1 + 0.163 t_2 + 0.100 t_3 + 0.327 \log_{10}(N_a^+) \\ &+ 15.65 \log_{10}(N_a) - 4.93 \log_{10}(N_d) + 0.228 \log_{10}(N_d^+) + 0.0183 t_5 \\ &- 0.000284 t_1^2 - 0.0000384 t_1 t_2 + 0.0000147 t_1 t_3 - 0.0109 t_1 \log_{10}(N_a^+) \\ &+ 0.000442 t_1 \log_{10}(N_a) + 0.00545 t_1 \log_{10}(N_d) - 0.00115 t_1 \log_{10}(N_d^+) \\ &- 0.0000933 t_1 t_5 + 0.00188 t_2^2 + 0.000134 t_2 t_3 - 0.00388 t_2 \log_{10}(N_a^+) \\ &- 0.0147 t_2 \log_{10}(N_a) + 0.00769 t_2 \log_{10}(N_d) - 0.00397 t_2 \log_{10}(N_d^+) \\ &- 0.0000183 t_2 t_5 - 0.0000389 t_3^2 - 0.00404 t_3 \log_{10}(N_a^+) \\ &- 0.000544 t_3 \log_{10}(N_a) + 0.00139 t_3 \log_{10}(N_d) - 0.00174 t_3 \log_{10}(N_d^+) \\ &+ 0.00000648 t_3 t_5 - 0.0639 \log_{10}^2(N_a^+) + 0.00505 \log_{10}(N_a^+) \log_{10}(N_a) \\ &+ 0.144 \log_{10}(N_a^+) \log_{10}(N_d) + 0.0214 \log_{10}(N_a^+) \log_{10}(N_d^+) \\ &- 0.000526 t_5 \log_{10}(N_a^+) - 0.467 \log_{10}^2(N_a) - 0.204 \log_{10}(N_a) \log_{10}(N_d) \\ &+ 0.131 \log_{10}(N_a) \log_{10}(N_d^+) - 0.000352 t_5 \log_{10}(N_a) + 0.147 \log_{10}^2(N_d) \\ &- 0.0459 \log_{10}(N_d) \log_{10}(N_d^+) + 0.000199 t_5 \log_{10}(N_d) \\ &- 0.0417 \log_{10}^2(N_d^+) + 0.0000518 t_5 \log_{10}(N_d^+) - 0.00000434 t_5^2 \end{aligned} \right) \quad (13)$$

$$\begin{aligned} S = &35.52 + 0.301 t_1 + 0.215 t_2 - 0.0432 t_3 - 6.07 \log_{10}(N_a^+) - 1.66 \log_{10}(N_a) \\ &- 7.28 \log_{10}(N_d) + 9.49 \log_{10}(N_d^+) - 0.000281 t_5 - 0.00141 t_1^2 + 0.000100 t_1 t_2 \\ &+ 0.000155 t_1 t_3 - 0.00650 t_1 \log_{10}(N_a^+) - 0.00254 t_1 \log_{10}(N_a) + 0.00429 t_1 \log_{10}(N_d) \\ &- 0.00549 t_1 \log_{10}(N_d^+) - 0.0000715 t_1 t_5 - 0.000253 t_2^2 + 0.000210 t_2 t_3 \\ &- 0.00158 t_2 \log_{10}(N_a^+) - 0.00989 t_2 \log_{10}(N_a) + 0.000261 t_2 \log_{10}(N_d) \\ &- 0.00242 t_2 \log_{10}(N_d^+) + 0.0000160 t_2 t_5 - 0.0000287 t_3^2 + 0.00000601 t_3 \log_{10}(N_a^+) \\ &- 0.000279 t_3 \log_{10}(N_a) + 0.00194 t_3 \log_{10}(N_d) + 0.000658 t_3 \log_{10}(N_d^+) \\ &- 0.00000306 t_3 t_5 + 0.152 \log_{10}^2(N_a^+) + 0.0108 \log_{10}(N_a^+) \log_{10}(N_a) \\ &+ 0.0262 \log_{10}(N_a^+) \log_{10}(N_d) - 0.0121 \log_{10}(N_a^+) \log_{10}(N_d^+) + 0.000195 t_5 \log_{10}(N_a^+) \\ &+ 0.0923 \log_{10}^2(N_a) - 0.106 \log_{10}(N_a) \log_{10}(N_d) + 0.0171 \log_{10}(N_a) \log_{10}(N_d^+) \\ &+ 0.000124 t_5 \log_{10}(N_a) + 0.201 \log_{10}^2(N_d) + 0.0819 \log_{10}(N_d) \log_{10}(N_d^+) \\ &- 0.0000138 t_5 \log_{10}(N_d) - 0.269 \log_{10}^2(N_d^+) - 0.000344 t_5 \log_{10}(N_d^+) \\ &+ 0.00000656 t_5^2 \end{aligned} \quad (14)$$

$$\begin{aligned} M_1 = &1.26 \times 10^{10} + 2.74 \times 10^7 t_1 + 3.01 \times 10^6 t_2 - 4.21 \times 10^6 t_3 - 4.40 \times 10^8 \log_{10}(N_a^+) \\ &- 4.55 \times 10^8 \log_{10}(N_a) - 4.55 \times 10^8 \log_{10}(N_d) - 2.03 \times 10^8 \log_{10}(N_d^+) + 845869.0 t_5 \\ &- 4986.64 t_1^2 - 29117.0 t_1 t_2 + 3428.39 t_1 t_3 - 365098.0 t_1 \log_{10}(N_a^+) - 488428.0 t_1 \log_{10}(N_a) \\ &- 336305.0 t_1 \log_{10}(N_d) - 326473.0 t_1 \log_{10}(N_d^+) - 1350.53 t_1 t_5 + 8373.74 t_2^2 + 1594.44 t_2 t_3 \\ &+ 251975.0 t_2 \log_{10}(N_a^+) - 129213.0 t_2 \log_{10}(N_a) - 128538.0 t_2 \log_{10}(N_d) \\ &- 140654.0 t_2 \log_{10}(N_d^+) - 3758.77 t_2 t_5 + 966.76 t_3^2 + 137736.0 t_3 \log_{10}(N_a^+) \\ &- 29071.4 t_3 \log_{10}(N_a) - 27741.7 t_3 \log_{10}(N_d) + 84744.8 t_3 \log_{10}(N_d^+) + 1159.26 t_3 t_5 \\ &+ 6.02 \times 10^6 \log_{10}^2(N_a^+) + 1.18 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_a) + 2.20 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_d) \\ &+ 7.64 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_d^+) + 2658.14 t_5 \log_{10}(N_a^+) + 9.17 \times 10^6 \log_{10}^2(N_a) \\ &+ 1.15 \times 10^7 \log_{10}(N_a) \log_{10}(N_d) + 385563.0 \log_{10}(N_a) \log_{10}(N_d^+) - 27875.3 t_5 \log_{10}(N_a) \\ &+ 4.79 \times 10^6 \log_{10}^2(N_d) + 7.04 \times 10^6 \log_{10}(N_d) \log_{10}(N_d^+) - 47733.5 t_5 \log_{10}(N_d) \\ &- 1.33 \times 10^6 \log_{10}^2(N_d^+) + 2627.56 t_5 \log_{10}(N_d^+) + 295.83 t_5^2 \end{aligned} \quad (15)$$

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$$\begin{aligned}
M_2 = & 1.66 \times 10^9 - 1.47 \times 10^7 t_1 + 1.81 \times 10^7 t_2 - 4.64 \times 10^6 t_3 + 1.58 \times 10^7 \log_{10}(N_a^+) \\
& - 8.91 \times 10^7 \log_{10}(N_a) - 3.95 \times 10^7 \log_{10}(N_d) - 4.41 \times 10^7 \log_{10}(N_d^+) - 1.89 \times 10^6 t_5 \\
& + 9487.66 t_1^2 + 38719.7 t_1 t_2 - 8380.73 t_1 t_3 + 326608.0 t_1 \log_{10}(N_a^+) + 395286.0 t_1 \log_{10}(N_a) \\
& + 269085.0 t_1 \log_{10}(N_d) - 44180.2 t_1 \log_{10}(N_d^+) - 5277.17 t_1 t_5 + 4100.16 t_2^2 + 7014.65 t_2 t_3 \\
& - 225791.0 t_2 \log_{10}(N_a^+) - 491515.0 t_2 \log_{10}(N_a) - 763184.0 t_2 \log_{10}(N_d) \\
& + 76513.6 t_2 \log_{10}(N_d^+) + 3839.69 t_2 t_5 + 810.77 t_3^2 + 45344.1 t_3 \log_{10}(N_a^+) \\
& + 44371.0 t_3 \log_{10}(N_a) + 65281.5 t_3 \log_{10}(N_d) + 101220.0 t_3 \log_{10}(N_d^+) - 226.25 t_3 t_5 \\
& + 1.64 \times 10^6 \log_{10}^2(N_a^+) - 2.93 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_a) - 2.85 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_d) \\
& - 559469.0 \log_{10}(N_a^+) \log_{10}(N_d^+) + 37008.2 t_5 \log_{10}(N_a^+) + 2.84 \times 10^6 \log_{10}^2(N_a) \\
& + 5.21 \times 10^6 \log_{10}(N_a) \log_{10}(N_d) - 1.53 \times 10^6 \log_{10}(N_a) \log_{10}(N_d^+) + 35441.9 t_5 \log_{10}(N_a) \\
& + 1.05 \times 10^6 \log_{10}^2(N_d) - 255037.0 \log_{10}(N_d) \log_{10}(N_d^+) + 25173.1 t_5 \log_{10}(N_d) \\
& + 1.66 \times 10^6 \log_{10}^2(N_d^+) + 13575.4 t_5 \log_{10}(N_d^+) + 93.68 t_5^2
\end{aligned} \tag{16}$$

$$\begin{aligned}
M_3 = & -1.30 \times 10^{13} - 1.05 \times 10^{10} t_1 - 4.21 \times 10^{10} t_2 - 1.99 \times 10^{10} t_3 + 3.54 \times 10^{11} \log_{10}(N_a^+) \\
& + 5.18 \times 10^{11} \log_{10}(N_a) + 5.76 \times 10^{11} \log_{10}(N_d) + 2.17 \times 10^{11} \log_{10}(N_d^+) + 5.06 \times 10^8 t_5 \\
& - 3.32 \times 10^7 t_1^2 - 1.95 \times 10^7 t_1 t_2 - 738004.0 t_1 t_3 + 7.21 \times 10^8 t_1 \log_{10}(N_a^+) \\
& - 6.21 \times 10^8 t_1 \log_{10}(N_a) - 5.34 \times 10^8 t_1 \log_{10}(N_d) + 8.38 \times 10^8 t_1 \log_{10}(N_d^+) \\
& - 2.42 \times 10^6 t_1 t_5 - 3.89 \times 10^7 t_2^2 - 2.55 \times 10^7 t_2 t_3 + 6.19 \times 10^8 t_2 \log_{10}(N_a^+) \\
& + 7.98 \times 10^8 t_2 \log_{10}(N_a) + 9.47 \times 10^8 t_2 \log_{10}(N_d) + 5.28 \times 10^8 t_2 \log_{10}(N_d^+) \\
& - 9.23 \times 10^6 t_2 t_5 - 2.13 \times 10^6 t_3^2 + 2.38 \times 10^8 t_3 \log_{10}(N_a^+) + 2.49 \times 10^8 t_3 \log_{10}(N_a) \\
& + 6.33 \times 10^8 t_3 \log_{10}(N_d) + 3.91 \times 10^7 t_3 \log_{10}(N_d^+) + 1.62 \times 10^6 t_3 t_5 - 6.72 \times 10^9 \log_{10}^2(N_a^+) \\
& - 6.22 \times 10^9 \log_{10}(N_a^+) \log_{10}(N_a) - 9.11 \log_{10}(N_a^+) \log_{10}(N_d) \\
& + 4.89 \times 10^9 \log_{10}(N_a^+) \log_{10}(N_d^+) + 2.07 \times 10^7 t_5 \log_{10}(N_a^+) - 3.38 \times 10^9 \log_{10}^2(N_a) \\
& - 1.25 \times 10^{10} \log_{10}(N_a) \log_{10}(N_d) - 5.15 \times 10^9 \log_{10}(N_a) \log_{10}(N_d^+) \\
& - 3.33 \times 10^7 t_5 \log_{10}(N_a) - 5.23 \times 10^9 \log_{10}^2(N_d) - 3.35 \times 10^9 \log_{10}(N_d) \log_{10}(N_d^+) \\
& - 5.38 \times 10^7 t_5 \log_{10}(N_d) - 5.83 \times 10^9 \log_{10}^2(N_d^+) + 4.66 \times 10^7 t_5 \log_{10}(N_d^+) - 393910.0 t_5^2
\end{aligned} \tag{17}$$

$$\begin{aligned}
I_{RM} = & 0.171 + 0.000179 t_1 + 0.000060 t_2 + 0.000212 t_3 - 0.0242 \log_{10}(N_a^+) \\
& + 0.00107 \log_{10}(N_a) + 0.0270 \log_{10}(N_d) - 0.0169 \log_{10}(N_d^+) - 0.0000215 t_5 + 0.00000278 t_1^2 \\
& + 6.01 \times 10^{-7} t_1 t_2 + 3.31 \times 10^{-7} t_1 t_3 - 0.0000144 t_1 \log_{10}(N_a^+) - 0.0000190 t_1 \log_{10}(N_a) \\
& - 5.35 \times 10^{-7} t_1 \log_{10}(N_d) + 0.0000065 t_1 \log_{10}(N_d^+) + 1.67 \times 10^{-7} t_1 t_5 + 0.00000454 t_2^2 \\
& - 2.91 \times 10^{-7} t_2 t_3 - 0.0000129 t_2 \log_{10}(N_a^+) - 0.00000776 t_2 \log_{10}(N_a) \\
& - 0.0000134 t_2 \log_{10}(N_d) + 0.0000122 t_2 \log_{10}(N_d^+) + 6.84 \times 10^{-8} t_2 t_5 - 4.61 \times 10^{-7} t_3^2 \\
& + 0.00000322 t_3 \log_{10}(N_a^+) + 0.00000347 t_3 \log_{10}(N_a) - 0.00000910 t_3 \log_{10}(N_d) \\
& - 0.00000337 t_3 \log_{10}(N_d^+) + 9.37 \times 10^{-8} t_3 t_5 + 0.000632 \log_{10}^2(N_a^+) \\
& + 0.0000720 \log_{10}(N_a^+) \log_{10}(N_a) - 0.000156 \log_{10}(N_a^+) \log_{10}(N_d) \\
& + 0.0000220 \log_{10}(N_a^+) \log_{10}(N_d^+) - 6.27 \times 10^{-7} t_5 \log_{10}(N_a^+) - 0.000426 \log_{10}^2(N_a) \\
& + 0.000563 \log_{10}(N_a) \log_{10}(N_d) + 0.000110 \log_{10}(N_a) \log_{10}(N_d^+) + 0.00000262 t_5 \log_{10}(N_a) \\
& - 0.000809 \log_{10}^2(N_d) - 0.000276 \log_{10}(N_d) \log_{10}(N_d^+) - 0.00000206 t_5 \log_{10}(N_d) \\
& + 0.000488 \log_{10}^2(N_d^+) - 7.36 \times 10^{-7} t_5 \log_{10}(N_d^+) + 1.96 \times 10^{-8} t_5^2
\end{aligned} \tag{18}$$

Appendix C: RSM EQUATIONS FOR THE BUFFER LAYER DIODE

$$\begin{aligned}
V_R = & -30818.6 - 1.26t_1 - 62.02t_2 - 24.40t_3 - 1.68t_5 + 1369.42 \log_{10}(N_a^+) \\
& - 1469.01 \log_{10}(N_d^-) + 3403.86 \log_{10}(N_d) + 0.0189t_1^2 - 0.00459t_1t_2 - 0.0000199t_1t_3 \\
& - 0.000371t_1t_5 + 0.0204t_1 \log_{10}(N_a^+) - 0.0608t_1 \log_{10}(N_d^-) - 0.0000139t_1 \log_{10}(N_d) \\
& - 0.108t_2^2 - 0.00674t_2t_3 + 0.000229t_2t_5 - 0.00948t_2 \log_{10}(N_a^+) + 5.64t_2 \log_{10}(N_d^-) \\
& - 1.28t_2 \log_{10}(N_d) + 0.00383t_3^2 + 0.00129t_3t_5 + 0.012t_3 \log_{10}(N_a^+) + 0.0113t_3 \log_{10}(N_d^-) \\
& + 1.35t_3 \log_{10}(N_d) + 0.000699t_5^2 + 0.0129t_5 \log_{10}(N_a^+) + 0.0890t_5 \log_{10}(N_d^-) \\
& - 0.0626t_5 \log_{10}(N_d) - 34.39 \log_{10}^2(N_a^+) - 5.06 \log_{10}(N_a^+) \log_{10}(N_d^-) \\
& + 1.69 \log_{10}(N_a^+) \log_{10}(N_d) + 100.44 \log_{10}^2(N_d^-) - 74.84 \log_{10}(N_d^-) \log_{10}(N_d) \\
& - 71.58 \log_{10}^2(N_d)
\end{aligned} \tag{19}$$

$$\begin{aligned}
V_f = & 7.03 - 0.00684t_1 - 0.000404t_2 + 0.00467t_3 + 0.00109t_5 - 0.451 \log_{10}(N_a^+) \\
& - 0.0926 \log_{10}(N_d^-) - 0.172 \log_{10}(N_d) + 0.00000206t_1^2 + 0.00000949t_1t_2 + 0.00000365t_1t_3 \\
& - 0.00000207t_1t_5 + 0.0000496t_1 \log_{10}(N_a^+) + 0.000532t_1 \log_{10}(N_d^-) \\
& - 0.0000274t_1 \log_{10}(N_d) + 0.00000452t_2^2 + 0.0000187t_2t_3 - 0.00000316t_2t_5 \\
& - 0.000301t_2 \log_{10}(N_a^+) + 0.000117t_2 \log_{10}(N_d^-) + 0.000467t_2 \log_{10}(N_d) + 0.0000112t_3^2 \\
& + 2.93 \times 10^{-8}t_3t_5 + 0.0000103t_3 \log_{10}(N_a^+) - 0.00000954t_3 \log_{10}(N_d^-) - 0.000369t_3 \log_{10}(N_d) \\
& + 4.82 \times 10^{-7}t_5^2 - 0.000067t_5 \log_{10}(N_a^+) - 0.0000356t_5 \log_{10}(N_d^-) + 0.00000344t_5 \log_{10}(N_d) \\
& + 0.00953 \log_{10}^2(N_a^+) + 0.00697 \log_{10}(N_a^+) \log_{10}(N_d^-) + 0.00196 \log_{10}(N_a^+) \log_{10}(N_d) \\
& - 0.00158 \log_{10}^2(N_d^-) - 0.000796 \log_{10}(N_d^-) \log_{10}(N_d) + 0.00501 \log_{10}^2(N_d)
\end{aligned} \tag{20}$$

$$t_s = 1 \times 10^{-8} \left[\begin{aligned}
& 357.60 + 0.0186t_1 - 0.0887t_2 + 0.0222t_3 + 0.00786t_5 - 25.93 \log_{10}(N_a^+) \\
& + 3.92 \log_{10}(N_d^-) - 15.60 \log_{10}(N_d) - 0.000134t_1^2 + 0.000474t_1t_2 \\
& - 3.89 \times 10^{-7}t_1t_3 + 0.00000431t_1t_5 - 0.00273t_1 \log_{10}(N_a^+) \\
& + 0.00798t_1 \log_{10}(N_d^-) - 0.00394t_1 \log_{10}(N_d) + 0.00629t_2^2 + 0.000359t_2t_3 \\
& + 0.000201t_2t_5 + 0.0410t_2 \log_{10}(N_a^+) + 0.0257t_2 \log_{10}(N_d^-) \\
& - 0.0979t_2 \log_{10}(N_d) - 0.000253t_3^2 + 1.75 \times 10^{-7}t_3t_5 - 0.0000207t_3 \log_{10}(N_a^+) \\
& + 0.00769t_3 \log_{10}(N_d^-) - 0.00512t_3 \log_{10}(N_d) - 0.0000190t_5^2 \\
& + 0.000511t_5 \log_{10}(N_a^+) + 0.000282t_5 \log_{10}(N_d^-) + 0.000456t_5 \log_{10}(N_d) \\
& + 0.861 \log_{10}^2(N_a^+) - 0.145 \log_{10}(N_a^+) \log_{10}(N_d^-) - 0.431 \log_{10}(N_a^+) \log_{10}(N_d) \\
& - 0.264 \log_{10}^2(N_d^-) + 0.262 \log_{10}(N_d^-) \log_{10}(N_d) + 0.674 \log_{10}^2(N_d)
\end{aligned} \right] \tag{21}$$

Appendix

$$t_{rr} = 1 \times 10^{-8} \left(\begin{aligned} &1285.55 + 1.37t_1 - 2.37t_2 + 0.440t_3 - 0.171t_5 - 36.94 \log_{10}(N_a^+) \\ &- 16.13 \log_{10}(N_d^-) - 88.78 \log_{10}(N_d) + 0.0000359t_1^2 + 0.000795t_1t_2 \\ &+ 0.0000434t_1t_3 + 0.000188t_1t_5 \\ &- 0.00965t_1 \log_{10}(N_a^+) - 0.0339t_1 \log_{10}(N_d^-) - 0.0540t_1 \log_{10}(N_d) + 0.0153t_2^2 \\ &+ 0.00226t_2t_3 + 0.00107t_2t_5 + 0.107t_2 \log_{10}(N_a^+) + 0.102t_2 \log_{10}(N_d^-) \\ &- 0.181t_2 \log_{10}(N_d) - 0.000814t_3^2 - 0.000289t_3t_5 - 0.000781t_3 \log_{10}(N_a^+) \\ &+ 0.0345t_3 \log_{10}(N_d^-) - 0.0323t_3 \log_{10}(N_d) - 0.0000626t_5^2 \\ &+ 0.000485t_5 \log_{10}(N_a^+) - 0.000239t_5 \log_{10}(N_d^-) + 0.0156t_5 \log_{10}(N_d) \\ &+ 1.74 \log_{10}^2(N_a^+) + 0.00764 \log_{10}(N_a^+) \log_{10}(N_d^-) - 2.04 \log_{10}(N_a^+) \log_{10}(N_d) \\ &- 0.870 \log_{10}^2(N_d^-) + 2.19 \log_{10}(N_d^-) \log_{10}(N_d) + 2.78 \log_{10}^2(N_d) \end{aligned} \right) \quad (22)$$

$$\begin{aligned} S = &-53.46 + 0.0762t_1 - 0.262t_2 + 0.0347t_3 - 0.0361t_5 + 11.15 \log_{10}(N_a^+) + 4.24 \log_{10}(N_d^-) \\ &- 7.38 \log_{10}(N_d) + 0.000185t_1^2 - 0.000621t_1t_2 + 0.0000164t_1t_3 + 0.0000801t_1t_5 \\ &+ 0.00467t_1 \log_{10}(N_a^+) - 0.00934t_1 \log_{10}(N_d^-) - 0.00739t_1 \log_{10}(N_d) - 0.00255t_2^2 \\ &+ 0.000382t_2t_3 + 0.0000497t_2t_5 - 0.00318t_2 \log_{10}(N_a^+) + 0.00165t_2 \log_{10}(N_d^-) \\ &+ 0.0265t_2 \log_{10}(N_d) - 0.0000379t_3^2 - 0.0000527t_3t_5 + 0.0000163t_3 \log_{10}(N_a^+) \\ &+ 0.00254t_3 \log_{10}(N_d^-) - 0.00221t_3 \log_{10}(N_d) - 0.00000409t_5^2 - 0.000665t_5 \log_{10}(N_a^+) \\ &- 0.000416t_5 \log_{10}(N_d^-) + 0.00357t_5 \log_{10}(N_d) - 0.369 \log_{10}^2(N_a^+) \\ &+ 0.269 \log_{10}(N_a^+) \log_{10}(N_d^-) + 0.00436 \log_{10}(N_a^+) \log_{10}(N_d) - 0.185 \log_{10}^2(N_d^-) \\ &- 0.287 \log_{10}(N_d^-) \log_{10}(N_d) + 0.250 \log_{10}^2(N_d) \end{aligned} \quad (23)$$

$$\begin{aligned} M1 = &-2.52 \times 10^9 - 3.82 \times 10^6 t_1 + 2.09 \times 10^6 t_2 - 696966.0t_3 + 789979.0t_5 \\ &+ 1.24 \times 10^8 \log_{10}(N_a^+) + 7.91 \times 10^7 \log_{10}(N_d^-) + 6.84 \times 10^7 \log_{10}(N_d) - 1435.88t_1^2 \\ &- 8452.88t_1t_2 + 170.50t_1t_3 + 204.70t_1t_5 + 214959.0t_1 \log_{10}(N_a^+) - 38520.4t_1 \log_{10}(N_d^-) \\ &+ 15559.7t_1 \log_{10}(N_d) - 45385.9t_2^2 + 9847.97t_2t_3 - 105.88t_2t_5 - 82370.4t_2 \log_{10}(N_a^+) \\ &- 90451.9t_2 \log_{10}(N_d^-) + 187847.0t_2 \log_{10}(N_d) + 2442.08t_3^2 - 533.55t_3t_5 \\ &+ 3498.85t_3 \log_{10}(N_a^+) - 5432.18t_3 \log_{10}(N_d^-) + 8450.26t_3 \log_{10}(N_d) - 99.04t_5^2 \\ &- 17557.1t_5 \log_{10}(N_a^+) - 5266.25t_5 \log_{10}(N_d^-) - 10725.5t_5 \log_{10}(N_d) \\ &- 4.78 \times 10^6 \log_{10}^2(N_a^+) + 3.67 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_d^-) + 1.18 \times 10^6 \log_{10}(N_a^+) \log_{10}(N_d) \\ &- 1.30 \times 10^6 \log_{10}^2(N_d^-) - 7.05 \times 10^6 \log_{10}(N_d^-) \log_{10}(N_d) + 589462.0 \log_{10}^2(N_d) \end{aligned} \quad (24)$$

$$\begin{aligned} M2 = &-5.57 \times 10^8 - 383899.0t_1 + 2.32 \times 10^6 t_2 + 30797.5t_3 + 255438.0t_5 \\ &+ 2.74 \times 10^7 \log_{10}(N_a^+) - 3.15 \times 10^7 \log_{10}(N_d^-) + 4.34 \times 10^7 \log_{10}(N_d) - 1480.15t_1^2 \\ &- 789.01t_1t_2 - 116.32t_1t_3 - 161.17t_1t_5 + 30025.9t_1 \log_{10}(N_a^+) - 17497.8t_1 \log_{10}(N_d^-) \\ &+ 21846.9t_1 \log_{10}(N_d) + 702.15t_2^2 + 867.12t_2t_3 - 861.66t_2t_5 - 11133.7t_2 \log_{10}(N_a^+) \\ &- 29763.3t_2 \log_{10}(N_d^-) - 75544.7t_2 \log_{10}(N_d) + 962.33t_3^2 - 70.21t_3t_5 \\ &- 1804.6t_3 \log_{10}(N_a^+) - 25404.7t_3 \log_{10}(N_d^-) + 9505.0t_3 \log_{10}(N_d) - 15.06t_5^2 \\ &- 710.42t_5 \log_{10}(N_a^+) + 1634.58t_5 \log_{10}(N_d^-) - 11977.4t_5 \log_{10}(N_d) \\ &- 665736.0 \log_{10}^2(N_a^+) - 157611.0 \log_{10}(N_a^+) \log_{10}(N_d^-) + 45579.2 \log_{10}(N_a^+) \log_{10}(N_d) \\ &+ 1.48 \times 10^6 \log_{10}^2(N_d^-) - 102033.0 \log_{10}(N_d^-) \log_{10}(N_d) - 912292.0 \log_{10}^2(N_d) \end{aligned} \quad (25)$$

Appendix

$$\begin{aligned}
M3 = & 7.88 \times 10^{11} - 2.03 \times 10^8 t_1 - 3.39 \times 10^8 t_2 - 6.27 \times 10^8 t_3 - 2.92 \times 10^8 t_5 \\
& - 3.83 \times 10^{10} \log_{10}(N_a^+) - 2.06 \times 10^{10} \log_{10}(N_d^-) - 1.46 \times 10^{10} \log_{10}(N_d) + 1.29 \times 10^6 t_1^2 \\
& + 231083.0 t_1 t_2 + 46922.2 t_1 t_3 + 51978.8 t_1 t_5 + 368500.0 t_1 \log_{10}(N_a^+) + 1.94 \times 10^6 t_1 \log_{10}(N_d^-) \\
& - 1.63 \times 10^6 t_1 \log_{10}(N_d) + 4.53 \times 10^6 t_2^2 + 136305.0 t_2 t_3 - 9009.17 t_2 t_5 - 1.81 \times 10^6 t_2 \log_{10}(N_a^+) \\
& + 8.77 \times 10^6 t_2 \log_{10}(N_d^-) - 1.46 \times 10^6 t_2 \log_{10}(N_d) - 932473.0 t_3^2 - 890231.0 t_3 t_5 \\
& - 28034.5 t_3 \log_{10}(N_a^+) + 1.23 \times 10^6 t_3 \log_{10}(N_d^-) + 9.16 \times 10^7 t_3 \log_{10}(N_d) - 103208.0 t_5^2 \\
& - 11416.7 t_5 \log_{10}(N_a^+) - 93666.7 t_5 \log_{10}(N_d^-) + 3.29 \times 10^7 t_5 \log_{10}(N_d) \\
& + 9.54 \times 10^8 \log_{10}^2(N_a^+) + 4.65 \times 10^7 \log_{10}(N_a^+) \log_{10}(N_d^-) + 3.59 \times 10^7 \log_{10}(N_a^+) \log_{10}(N_d) \\
& + 7.29 \times 10^8 \log_{10}^2(N_d^-) - 2.42 \times 10^7 \log_{10}(N_d^-) \log_{10}(N_d) - 6.29 \times 10^8 \log_{10}^2(N_d)
\end{aligned} \tag{26}$$

$$\begin{aligned}
I_{rm} = & 0.504 + 0.00393 t_1 - 0.00472 t_2 - 0.000677 t_3 - 0.000155 t_5 - 0.0526 \log_{10}(N_a^+) \\
& + 0.00344 \log_{10}(N_d^-) + 0.0128 \log_{10}(N_d) - 0.00000473 t_1^2 + 0.00000352 t_1 t_2 - 7.23 \times 10^{-7} t_1 t_3 \\
& - 5.12 \times 10^{-7} t_1 t_5 - 0.000149 t_1 \log_{10}(N_a^+) - 0.0000484 t_1 \log_{10}(N_d^-) + 0.0000335 t_1 \log_{10}(N_d) \\
& - 0.000033 t_2^2 - 0.0000032 t_2 t_3 + 0.0000064 t_2 t_5 + 0.000124 t_2 \log_{10}(N_a^+) \\
& - 0.000243 t_2 \log_{10}(N_d^-) + 0.000146 t_2 \log_{10}(N_d) - 0.0000028 t_3^2 + 3.13 \times 10^{-7} t_3 t_5 \\
& + 0.0000206 t_3 \log_{10}(N_a^+) + 0.000109 t_3 \log_{10}(N_d^-) - 0.0000352 t_3 \log_{10}(N_d) - 5.69 \times 10^{-8} t_5^2 \\
& + 1.47 \times 10^{-7} t_5 \log_{10}(N_a^+) + 3.56 \times 10^{-7} t_5 \log_{10}(N_d^-) + 0.0000011 t_5 \log_{10}(N_d) \\
& + 0.00210 \log_{10}^2(N_a^+) - 0.0000270 \log_{10}(N_a^+) \log_{10}(N_d^-) - 0.00169 \log_{10}(N_a^+) \log_{10}(N_d) \\
& - 0.00109 \log_{10}^2(N_d^-) + 0.00146 \log_{10}(N_d^-) \log_{10}(N_d) - 0.000218 \log_{10}^2(N_d)
\end{aligned} \tag{27}$$

Appendix D: RSM EQUATIONS FOR THE CLC DIODE

$$\begin{aligned}
V_R = & -14537.1 - 114.49t_1 + 10.75t_2 - 1.52t_4 + 3.45t_5 + 1.91t_6 + 3934.04 \log_{10}(N_d) \\
& - 1709.81 \log_{10}(N_a^+) + 0.0364t_1^2 + 0.0168t_1t_2 + 0.0309t_1t_4 + 0.0337t_1t_5 + 0.00397t_1t_6 \\
& + 7.05t_1 \log_{10}(N_d) - 0.234t_1 \log_{10}(N_a^+) - 0.0887t_2^2 + 0.000158t_2t_4 + 0.0606t_2t_5 \\
& + 0.000176t_2t_6 - 0.00135t_2 \log_{10}(N_d) + 0.0240t_2 \log_{10}(N_a^+) - 0.337t_4^2 + 0.0112t_4t_5 \\
& + 0.00703t_4t_6 + 0.00313t_4 \log_{10}(N_d) + 0.0665t_4 \log_{10}(N_a^+) - 0.348t_5^2 - 0.000205t_5t_6 \\
& + 0.0167t_5 \log_{10}(N_d) - 0.0979t_5 \log_{10}(N_a^+) - 0.00110t_6^2 - 0.00913t_6 \log_{10}(N_d) \\
& - 0.00556t_6 \log_{10}(N_a^+) - 127.96 \log_{10}^2(N_d) - 0.899 \log_{10}(N_d) \log_{10}(N_a^+) + 44.53 \log_{10}^2(N_a^+)
\end{aligned} \tag{28}$$

$$\begin{aligned}
V_f = & 19.43 + 0.224t_1 - 0.0253t_2 - 0.0561t_4 - 0.0253t_5 - 0.000171t_6 - 5.64 \log_{10}(N_d) \\
& + 2.51 \log_{10}(N_a^+) - 0.0000340t_1^2 + 0.0000232t_1t_2 + 0.0000236t_1t_4 + 0.0000466t_1t_5 \\
& - 0.00000222t_1t_6 - 0.0124t_1 \log_{10}(N_d) - 0.00120t_1 \log_{10}(N_a^+) - 0.00000345t_2^2 \\
& + 0.0000226t_2t_4 + 0.0000840t_2t_5 + 0.00000525t_2t_6 + 0.000303t_2 \log_{10}(N_d) \\
& + 0.000679t_2 \log_{10}(N_a^+) - 0.0000739t_4^2 + 0.000249t_4t_5 + 0.00000883t_4t_6 \\
& + 0.000377t_4 \log_{10}(N_d) + 0.00193t_4 \log_{10}(N_a^+) - 0.000177t_5^2 - 0.00000407t_5t_6 \\
& + 0.000535t_5 \log_{10}(N_d) + 0.000591t_5 \log_{10}(N_a^+) - 4.42 \times 10^{-7}t_6^2 - 0.0000773t_6 \log_{10}(N_d) \\
& + 0.0000939t_6 \log_{10}(N_a^+) + 0.185 \log_{10}^2(N_d) + 0.0102 \log_{10}(N_d) \log_{10}(N_a^+) \\
& - 0.0720 \log_{10}^2(N_a^+)
\end{aligned} \tag{29}$$

$$t_x = 1 \times 10^{-8} \left(\begin{aligned}
& 164.77 - 0.142t_1 + 0.550t_2 + 6.11t_4 + 0.00588t_5 - 0.0851t_6 + 6.04 \log_{10}(N_d) \\
& - 22.61 \log_{10}(N_a^+) + 0.00139t_1^2 + 0.000195t_1t_2 - 0.0152t_1t_4 - 0.000431t_1t_5 \\
& + 0.00107t_1t_6 - 0.127t_1 \log_{10}(N_d) + 0.0698t_1 \log_{10}(N_a^+) - 0.00572t_2^2 \\
& - 0.00129t_2t_4 - 0.000775t_2t_5 - 0.00000847t_2t_6 + 0.00290t_2 \log_{10}(N_d) \\
& + 0.0140t_2 \log_{10}(N_a^+) + 0.0179t_4^2 - 0.00663t_4t_5 - 0.00370t_4t_6 \\
& - 0.00390t_4 \log_{10}(N_d) - 0.123t_4 \log_{10}(N_a^+) - 0.0162t_5^2 + 0.0000802t_5t_6 \\
& - 0.0538t_5 \log_{10}(N_d) + 0.0729t_5 \log_{10}(N_a^+) + 0.0000289t_6^2 \\
& + 0.00207t_6 \log_{10}(N_d) + 0.000104t_6 \log_{10}(N_a^+) + 0.509 \log_{10}^2(N_d) \\
& - 1.01 \log_{10}(N_d) \log_{10}(N_a^+) + 0.912 \log_{10}^2(N_a^+)
\end{aligned} \right) \tag{30}$$

$$t_{rr} = 1 \times 10^{-8} \left(\begin{aligned}
& 177.03 + 0.464t_1 - 0.962t_2 + 8.65t_4 + 4.98t_5 - 0.230t_6 - 21.93 \log_{10}(N_d) \\
& + 6.31 \log_{10}(N_a^+) + 0.00111t_1^2 + 0.000668t_1t_2 - 0.0151t_1t_4 - 0.00197t_1t_5 \\
& + 0.00108t_1t_6 - 0.193t_1 \log_{10}(N_d) + 0.0923t_1 \log_{10}(N_a^+) - 0.00454t_2^2 \\
& - 0.0110t_2t_4 - 0.00213t_2t_5 + 0.0000166t_2t_6 + 0.0780t_2 \log_{10}(N_d) \\
& + 0.0257t_2 \log_{10}(N_a^+) + 0.0219t_4^2 - 0.00855t_4t_5 - 0.00360t_4t_6 \\
& - 0.158t_4 \log_{10}(N_d) - 0.0999t_4 \log_{10}(N_a^+) - 0.00758t_5^2 - 0.00103t_5t_6 \\
& - 0.303t_5 \log_{10}(N_d) + 0.0729t_5 \log_{10}(N_a^+) + 0.0000612t_6^2 \\
& + 0.00874t_6 \log_{10}(N_d) - 0.000382t_6 \log_{10}(N_a^+) + 1.55 \log_{10}^2(N_d) \\
& - 1.52 \log_{10}(N_d) \log_{10}(N_a^+) + 0.330 \log_{10}^2(N_a^+)
\end{aligned} \right) \tag{31}$$

Appendix

$$\begin{aligned}
S = & -112.23 - 0.0557t_1 - 0.294t_2 + 0.0656t_4 + 0.575t_5 - 0.0146t_6 + 0.201 \log_{10}(N_d) \\
& + 12.98 \log_{10}(N_a^+) + 0.000675t_1^2 + 0.0000167t_1t_2 - 0.000647t_1t_4 - 0.000309t_1t_5 \\
& - 0.0000290t_1t_6 + 0.00485t_1 \log_{10}(N_d) - 0.00458t_1 \log_{10}(N_a^+) + 0.000787t_2^2 - 0.000469t_2t_4 \\
& - 0.000206t_2t_5 + 0.0000194t_2t_6 + 0.00874t_2 \log_{10}(N_d) + 0.00160t_2 \log_{10}(N_a^+) + 0.00180t_4^2 \\
& + 0.000566t_4t_5 - 0.0000868t_4t_6 - 0.0176t_4 \log_{10}(N_d) + 0.0160t_4 \log_{10}(N_a^+) + 0.00297t_5^2 \\
& - 0.000192t_5t_6 - 0.0284t_5 \log_{10}(N_d) - 0.000626t_5 \log_{10}(N_a^+) + 0.0000107t_6^2 \\
& - 0.000181t_6 \log_{10}(N_d) + 0.0000936t_6 \log_{10}(N_a^+) + 0.0577 \log_{10}^2(N_d) \\
& - 0.106 \log_{10}(N_d) \log_{10}(N_a^+) - 0.295 \log_{10}^2(N_a^+)
\end{aligned} \tag{32}$$

$$\begin{aligned}
M1 = & 2.87 \times 10^9 - 2.14 \times 10^7 t_1 - 3.20 \times 10^6 t_2 + 4.00 \times 10^6 t_4 + 5.91 \times 10^6 t_5 + 569855.0t_6 \\
& - 2.81 \times 10^8 \log_{10}(N_d) - 3.02 \times 10^7 \log_{10}(N_a^+) + 37968.5t_1^2 + 1746.0t_1t_2 - 30401.7t_1t_4 \\
& + 4041.78t_1t_5 - 1386.57t_1t_6 + 1.24 \times 10^6 t_1 \log_{10}(N_d) - 97058.2t_1 \log_{10}(N_a^+) + 5265.95t_2^2 \\
& + 10310.0t_2t_4 + 9503.2t_2t_5 + 332.27t_2t_6 + 109562.0t_2 \log_{10}(N_d) + 5577.33t_2 \log_{10}(N_a^+) \\
& - 34897.7t_4^2 + 26264.3t_4t_5 - 6040.91t_4t_6 - 218766.0t_4 \log_{10}(N_d) + 337979.0t_4 \log_{10}(N_a^+) \\
& + 7246.21t_5^2 - 2632.78t_5t_6 - 301343.0t_5 \log_{10}(N_d) - 32992.2t_5 \log_{10}(N_a^+) - 92.88t_6^2 \\
& - 18491.1t_6 \log_{10}(N_d) + 2971.0t_6 \log_{10}(N_a^+) + 9.10 \times 10^6 \log_{10}^2(N_d) \\
& - 2.54 \times 10^6 \log_{10}(N_d) \log_{10}(N_a^+) + 1.72 \times 10^6 \log_{10}^2(N_a^+)
\end{aligned} \tag{33}$$

$$\begin{aligned}
M2 = & 4.16 \times 10^9 - 1.21 \times 10^7 t_1 + 1.30 \times 10^6 t_2 + 2.35 \times 10^6 t_4 + 442535.0t_5 + 357994.0t_6 \\
& - 2.34 \times 10^8 \log_{10}(N_d) - 2.32 \times 10^8 \log_{10}(N_a^+) + 11017.8t_1^2 - 797.38t_1t_2 - 3649.33t_1t_4 \\
& + 1457.42t_1t_5 - 342.83t_1t_6 + 580806.0t_1 \log_{10}(N_d) + 100902.0t_1 \log_{10}(N_a^+) - 4322.53t_2^2 \\
& + 4155.52t_2t_4 + 747.36t_2t_5 - 59.39t_2t_6 + 13564.7t_2 \log_{10}(N_d) - 40878.3t_2 \log_{10}(N_a^+) \\
& - 39805.5t_4^2 - 1233.47t_4t_5 - 799.19t_4t_6 - 59101.3t_4 \log_{10}(N_d) + 12750.4t_4 \log_{10}(N_a^+) \\
& - 22765.9t_5^2 - 73.16t_5t_6 - 20276.7t_5 \log_{10}(N_d) + 16089.6t_5 \log_{10}(N_a^+) - 149.47t_6^2 \\
& - 3810.29t_6 \log_{10}(N_d) + 252.71t_6 \log_{10}(N_a^+) + 5.26 \times 10^6 \log_{10}^2(N_d) \\
& + 2.49 \times 10^6 \log_{10}(N_d) \log_{10}(N_a^+) + 4.88 \times 10^6 \log_{10}^2(N_a^+)
\end{aligned} \tag{34}$$

$$\begin{aligned}
M3 = & -1.31 \times 10^{13} + 2.70 \times 10^{10} t_1 - 3.82 \times 10^9 t_2 - 3.50 \times 10^9 t_4 + 2.09 \times 10^{10} t_5 \\
& + 4.65 \times 10^8 t_6 + 8.51 \times 10^{11} \log_{10}(N_d) + 5.73 \times 10^{11} \log_{10}(N_a^+) - 1.50 \times 10^7 t_1^2 \\
& + 350256.0t_1t_2 + 3.44 \times 10^6 t_1t_4 - 1.49 \times 10^6 t_1t_5 + 399982.0t_1t_6 - 1.27 \times 10^9 t_1 \log_{10}(N_d) \\
& - 3.12 \times 10^8 t_1 \log_{10}(N_a^+) + 2.31 \times 10^7 t_2^2 - 3.00 \times 10^6 t_2t_4 - 996680.0t_2t_5 - 13752.5t_2t_6 \\
& + 1.93 \times 10^7 t_2 \log_{10}(N_d) + 4.58 \times 10^6 t_2 \log_{10}(N_a^+) + 9.57 \times 10^7 t_4^2 + 8.69 \times 10^6 t_4t_5 \\
& + 192214.0t_4t_6 - 4.42 \times 10^7 t_4 \log_{10}(N_d) + 7.90 \times 10^7 t_4 \log_{10}(N_a^+) + 5.15 \times 10^7 t_5^2 \\
& - 7.91 \times 10^6 t_5t_6 - 9.12 \times 10^8 t_5 \log_{10}(N_d) - 6.40 \times 10^7 t_5 \log_{10}(N_a^+) - 213285.0t_6^2 \\
& - 5.01 \times 10^7 t_6 \log_{10}(N_d) - 1.04 \times 10^6 t_6 \log_{10}(N_a^+) - 1.78 \times 10^{10} \log_{10}^2(N_d) \\
& - 8.72 \times 10^9 \log_{10}(N_d) \log_{10}(N_a^+) - 1.08 \times 10^{10} \log_{10}^2(N_a^+)
\end{aligned} \tag{35}$$

Appendix

$$\begin{aligned}
I_{rm} = & -0.397 - 0.000838t_1 - 0.000176t_2 + 0.000752t_4 - 0.000880t_5 - 0.0000762t_6 \\
& + 0.0316\log_{10}(N_d) + 0.0244\log_{10}(N_a^+) - 4.24 \times 10^{-8}t_1^2 - 3.11 \times 10^{-8}t_1t_2 - 0.00000275t_1t_4 \\
& - 1.27 \times 10^{-7}t_1t_5 - 1.82 \times 10^{-7}t_1t_6 + 0.0000439t_1\log_{10}(N_d) + 0.0000208t_1\log_{10}(N_a^+) \\
& + 0.00000118t_2^2 - 8.66 \times 10^{-7}t_2t_4 - 2.28 \times 10^{-7}t_2t_5 + 8.18 \times 10^{-9}t_2t_6 \\
& - 0.00000519t_2\log_{10}(N_d) + 0.00000427t_2\log_{10}(N_a^+) - 0.00000274t_4^2 + 5.59 \times 10^{-7}t_4t_5 \\
& - 5.26 \times 10^{-7}t_4t_6 + 0.0000124t_4\log_{10}(N_d) - 0.00000667t_4\log_{10}(N_a^+) + 0.00000695t_5^2 \\
& + 4.58 \times 10^{-7}t_5t_6 + 0.0000589t_5\log_{10}(N_d) - 0.0000290t_5\log_{10}(N_a^+) + 2.41 \times 10^{-8}t_6^2 \\
& + 0.00000254t_6\log_{10}(N_d) + 3.72 \times 10^{-7}t_6\log_{10}(N_a^+) - 0.000678\log_{10}^2(N_d) \\
& - 0.000962\log_{10}(N_d)\log_{10}(N_a^+) - 0.000291\log_{10}^2(N_a^+)
\end{aligned} \tag{36}$$

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