Low jitter frequency multiplier

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A LOW JITTER FREQUENCY MULTIPLIER

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A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2010

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Abstract

This thesis I explore the research in the area of low jitter frequency multipliers before proposing a novel new design for such a multiplier. The thesis begins with an analysis of the random and deterministic noise arising from conventional phase-locked loop (PLL) and delay-locked loop (DLL) based frequency multipliers. Although the DLL is a better candidate for use as a low jitter frequency multiplier, analysis shows that the jitter performance of the DLL can be jeopardized by the cascading structure of the delay cells. Thus, a new architectural form is proposed. In this design, the delay chain of the conventional DLL is replaced by a polyphase filter (PPF) to generate clock edges for frequency multiplication purposes. A fundamental jitter analysis shows that the random jitter performance of the proposed PPF frequency multiplier outperforms that of the conventional DLL. Because the clock edges generated by the PPF have a larger mismatch when compared to their DLL counterparts, an analog-based phase error calibration (PEC) circuit is proposed to reduce the phase error. In doing so, both the random and deterministic jitter can be minimized and a frequency multiplier with better jitter performance is achieved.

To verify the proposed work, a 200MHz frequency multiplier with a multiplication ratio of eight times was designed using a crystal frequency of 25 MHz and simulated for a 200MS/s analog-to-digital converter (ADC) with a minimum effective 8-bit resolution. The frequency multiplier's output jitter was also predicted from the proposed behavior simulation models. The prototype was fabricated in a 0.13 μ m CMOS process, and the measured jitter was found to be 2.46ps (rms), ± 9.33 ps (pk-pk) while the normalized rms jitter was found to be 0.049%. The achievable maximum static phase error of the calibration circuit is 2.4ps. Earlier work in this area has shown that the normalized jitter serves as a key performance metric

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and our comparison of the proposed design with earlier designs shows the new design to hold significant promise in this regard.

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Chapter 1

Introduction

1.1 Motivations

Clocks or periodic signals play an important role in the synchronization of electronics systems [69]-[71]. In most digital applications such as microprocessors, digital signal processors (DSP) and application-specific integration circuits (ASIC), clocks are used to provide timing-related information to update system states and to latch onto data synchronously in order to achieve higher throughput and data rates [1]. Mixed-signal circuits like ADC and digital-to-analog converters (DAC) also play an important role in linking the digital system with the physical world in analog domain. The clock drives the sampling circuit to sample continuous-time signals from the input of the ADC and converts these signals into time discrete digital data for digital processing. Meanwhile, clocks are also very important for the generation of quasi-analog signals from discrete-time digital data through DACs [2], [3]. In narrowband radio frequency (RF) communication system, a clock from a local oscillator (LO) in a transmitter circuit is used to drive the mixer to up-convert intermediate frequency (IF) signals into high frequency RF signals for transmission over the airwaves, or to down-convert the RF signals into IF signals for reception purposes in receiver circuits [4].

The performance of integrated circuits, particularly in the area of integration density has gone through an astounding revolution in the last couple of decades. This is mainly from the successive improvements in the area of device miniaturization and the concomitant increase in device density leading to dramatic increases in the

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complexity of circuits on a single chip. According to Moore's Law, which is a historical observation made by Intel executive Gordon Moore, the number of transistors in a square millimeter of silicon is increasing exponentially -- doubling approximately every two years. The functionality and speed of the integrated circuit will increase proportionally to the number of transistors. Moore's Law describes this level of development as being an important driving force of technological and social change in the late 20th and early 21st centuries. With the continuous advancement of semiconductor technology and the scaling of devices, the clock speed of a digital circuit has now reached a few GHz. The trend of continuous improvement has continued for more than half a century and is not expected to stop for another decade or so. This trend has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy. Fig. 1.1 shows the growth of transistor counts in Intel processors and compares this to the predictions of Moore's Law [9].

From Fig. 1.1, it is clear that circuit speed increases exponentially with time. With such increasing speed, it becomes impractical to use external crystal oscillators as a clock source as crystal oscillators are difficult and expensive to manufacture at 100MHz or higher. Therefore, a frequency multiplier circuit is needed to multiply the low reference frequency from the crystal oscillator to suit the high frequencies required for the operation of an integrated circuit.

Fig. 1.1: Growth of Transistor Counts for Intel Processor According to Moore's Law.

There are several types of frequency multipliers which can be divided into two major categories. The first is the direct frequency multiplier, and the second is the indirect frequency multiplier. The direct frequency multiplier generates a higher output frequency by using a combination of multipliers, mixers, dividers and low pass filters. For instance, an input reference frequency can be multiplied by injecting it into a non-linear device like a Step Recovery Diode (SRD). The output of the diode will generate a large number of harmonics, and a band pass filter is then used to select the required harmonic frequency. Another method of direct frequency multiplication involves the use of a series of mixers to up-convert the reference frequency into a

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higher output frequency. However, the methods described above require a great deal of hardware and a larger circuit area. Further, in passing through numerous devices, the output signal will be substantially reduced and this method is therefore not suitable for implementation in an integrated circuit. Meanwhile, an indirect frequency multiplier generates a higher output frequency using a PLL [10]-[13], [17]-[48]. The PLL consists of a phase frequency detector (PFD), loop filter (LP), voltage-controlled oscillator (VCO) and a divider. The output frequency is indirectly generated from a VCO and the output phase is locked with the reference frequency phase through a feedback mechanism [2], [5], [6]. Because of the benefits of miniaturization and low power consumption, this is the most common frequency multiplier implemented in integrated circuits.

There are two types of PLLs which are commonly implemented in integrated circuits. The first is LC-tank VCO based, whereas the second is a ring oscillator VCO based PLL. An LC-tank VCO uses an on-chip spiral inductor and capacitor to form an LC resonator. A cross-couple NMOS, which is a negative resistive source, is used to compensate for energy loss in the LC resonator and maintain the oscillation of the VCO [5]. The advantage of the LC-tank VCO is that it provides better jitter or phase noise performance. It is for this reason that this architecture is widely used in the frequency synthesizers of wireless communication transceivers. On the other hand, the ring oscillator VCO consists of a number of delay cells in a loop. As long as the loop gain satisfies both Barkhausen's criteria, the oscillation will start. That means the loop gain is higher than one, and the total phase shift is 360° at the same frequency. However, the jitter performance of this PLL is inferior to that of LC-tank PLL due to the impact of noise from the transistors' delay cells.

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If the jitter requirements are not too stringent the ring oscillator PLL is the preferable architectural form for most applications because of its low cost, low power and system-on-chip requirements. The ring oscillator can achieve a very compact layout area in an integrated circuit. On the contrary, an LC-tank VCO needs an extra processor for spiral inductor fabrication. It not only occupies a significantly large area, it also increases the cost of the chip [67], [68].

With the continuous advancement of semiconductor technology and the scaling of devices, the speed of digital circuits will continue to increase. The resolution and speed of ADCs and DACs in a mixed-signal system like that in an integrated transceiver chip will also increase in response to the demands of higher digital processing speeds, and their jitter requirements will also become more stringent. Fig. 1.2 shows the jitter requirement of an ADC clock [65], [66].

Fig. 1.2: ADC Clock Jitter Requirements.

Motivations

The market for wireless communication has grown explosively in recent years with the fast development of new products and services. Current devices on the market, such as cordless/cellular telephones, bluetooth, WiFi, WiMax, and GPS/satellite receivers use the frequency spectrum between 800 MHz and 5 GHz for communication. As more wireless devices become available, spectrum usage will become higher and the phase noise requirements of their transceivers' local oscillators are likely to become more stringent [5] in order to maximize spectrum usage and optimize performance.

In this context, the jitter or phase noise of a clock becomes a critical parameter with which to determine the performance of a system. The large jitter clock of a microprocessor, DSP processor and ASIC may cause data to be latched wrongly, increases the data error rate and cause the malfunctioning of the system. In mixed-signal circuits like the ADC and DAC, a large jitter on the clock driving the sampling circuit will reduce the dynamic range of the circuit. In a transceiver, poor phase noise will reduce the signal-to-noise ratio (SNR) of the received signal, thus increasing the bit error rate of the transceiver system.

In light of these considerations, the conventional approach to frequency multiplier design using PLL architecture does not work to fully optimize the jitter performance. As the PLL is an indirect frequency multiplier, the output frequency is generated from an on-chip VCO with poor jitter and phase noise performance. To optimize the PLL output's jitter and phase noise, the VCO output phase is locked with a clean reference clock through the feedback mechanism. The loop bandwidth of the PLL will determine the PLL's output jitter and phase noise performance. The higher the loop bandwidth, the more sensitive the PLL's feedback mechanism. As a result, the timing error generated by the VCO can be corrected more rapidly. However, the

Motivations

PLL is a second order system. The loop bandwidth is limited by the stability requirement of the loop, which is approximately one tenth of the reference frequency [78]. Therefore, the VCO timing error will add to the accumulating timing error from one cycle to another until it is large enough for correction through the feedback loop [79]-[82]. This signature characteristic of PLL jitters or phase noises poses a significant challenge in low jitter and low phase noise applications such as wireless communication transceivers.

A DLL based frequency multiplier has also been proposed to solve the jitter accumulation problem of PLLs [50]. The DLL generates the output frequency directly from a clean reference clock. A delay chain with a number of delay cells will lock at the period of a reference clock and the edge of each delay cell will be combined using an edge combiner circuit that generates a multiplied output frequency. In this way, the DLL not only achieves a low phase noise clock for wireless communication transceivers [50], but also a low jitter clock for digital applications [14]-[16], [49]-[64], [100]. Fig. 1.3 shows the results of a survey of PLL, multiplying delay-locked loop (MDLL) and DLL jitter performances as reported in the literature.

The jitter performance of the conventional DLL has not been optimized and the delay chain architecture in the DLL continues to accumulate random jitter from all delay cells [88]. Furthermore, noise from the MOS transistors present in the delay cells include the MOS thermal noise and flicker noise which contribute significant levels of random jitter to the output clock. In addition, the devices' mismatch in delay cells, the charge pump current source and current sink also contribute to the jitter in the output clock [88].

Motivations

Fig. 1.3: Survey of Jitter Performance of PLL, MDLL and DLL

1.2 Objectives

This project aims to study low jitter frequency multipliers as well as to design, analyze and implement such a frequency multiplier. We begin this effort by studying different forms of conventional frequency multiplier architectures such as PLL and DLL, and use these as a benchmark for our own design. We then propose a novel circuit architecture using CMOS process technology that seeks to overcome the limitations arising from conventional techniques. Experiments will be conducted on the prototype IC to validate the new frequency multiplier architecture, which is targeted for effective use in 8-bit 200Msps ADCs suitable for wideband applications such as 1000BASE-T and IEEE 802.11n [101]. Based on [6] and [65], the sampling clock jitter requirement for an effective 8-bit 200Msps ADC is 5.1ps rms.

1.3 Major Contributions

The literature on PLL and DLL based frequency multipliers is extensively reviewed, and used as a benchmark against which to study new forms of frequency multipliers. DLL has been shown to have the potential to achieve a lower jitter performance than its PLL counterpart. However, DLL based multipliers suffer the effects of unavoidable random noise arising from delay cells in the chain which becomes the bottleneck of DLL circuits. A novel form of frequency multiplier architecture is presented in this thesis to help alleviate the problem of jitter accumulation. This new design is then theoretically compared to more conventional forms of architecture through a series of analytical calculations in order to determine its potential for use as a low jitter frequency multiplier. Behavior simulation models are also established to help in the prediction of jitter performance.

The results of experiments conducted using the proposed frequency multiplier are presented. The multiplier has been fabricated using a standard 0.13 μ m CMOS process. In comparing the new design to prior works, it is clear that the proposed architecture achieves a far superior Figure of Merit (FOM) in jitter performance. We demonstrate the technical merits of the new design as well as the potential use of such low-jitter circuit designs.

1.4 Organization

This thesis is organized as follows. Chapter 2 begins with an introduction of clocks used in digital systems, mixed-signal circuits and in RF transceivers. Limitations associated with the use of such clocks are highlighted along with the reasons for this. This is then followed by a discussion on the impact of the clock's imperfections on digital systems, mixed-signal circuits and RF transceivers.

Chapter 3 begins with a survey of the literature. The fundamentals of a conventional PLL and DLL-based frequency multiplier are described and an analysis is conducted on both the random and deterministic noise associated with the two multipliers before these are compared. Based on the comparisons, DLL is found to be the more appropriate circuit architecture for use as a low jitter frequency multiplier. The bottleneck that is associated with the DLL's ability to optimize jitter performance is then discussed at length.

Chapter 4 proposes a new form of frequency multiplier architecture. Principles adopted in the design of the new architecture are described and analytical calculations are presented comparing the proposed architecture with more conventional forms of DLL on the basis of their jitter performance.

Chapter 5 details the implementation of the prototype. Each sub-block of the prototype is explained before simulation results are presented.

Chapter 6 discusses the layout considerations as well as the layout techniques of the proposed frequency multiplier.

Chapter 7 presents simulations of the jitter performance of the prototype for the purpose of validating theoretical predictions of its performance. We present a comparison of predicted and measured results and further compare the measured

Organization

results with that of current, state-of-the-art frequency multipliers. Lastly, the limitations of the proposed frequency multiplier are discussed.

Chapter 8 presents concluding remarks and makes recommendations for future research work.

Chapter 2

Clock in Electronic Systems

2.1 Introduction

The integration density and performance of integrated circuits have gone through an astounding revolution in the last couple of decades. Circuit speeds have increases exponentially with time [9] and clocks have come to play an important part in the synchronization of many electronic systems including digital circuits, mixed-signal data converter circuits and RF transceivers. In this chapter, we discuss in detail the function of clocks in synchronous digital circuits, mixed-signal data converter circuits, and in RF transceivers.

Unfortunately, it is virtually impossible to design a perfect clock for practical use. In the following section, we discuss the various sources of a clock's imperfection including thermal noise, flicker noise and mismatches in the devices. These imperfections will have an impact on the timing of the clock. This imperfection is known in the time domain as timing jitter and in the frequency domain as phase noise. The impact of the clock's imperfections will be discussed at length. In particular, the timing jitter directly affects the data error rate as well as the maximum operating frequency of a high-speed digital circuit. The dynamic range of a mixed-signal data converter circuit will also be affected. In an RF transceiver, the phase noise of the frequency synthesizer will reduce the sensitivity of the transceiver.

2.2 Roles of Clock

All sequential circuits used in digital systems have one property in common, mainly that a well-defined ordering of the switching events must be imposed if the circuit is to operate correctly. In the absence of such a condition, the wrong data might be written into the memory elements [1]. Most sequential circuits belong to a class of synchronous systems, which means the latching of data into the memory elements is orchestrated by a number of globally distributed clock signals. The synchronous pipelined datapath of a typical digital system is shown in Fig. 2.1.

Fig. 2.1: Synchronous Pipelined Datapath of Digital System.

In synchronous pipelined datapaths, depending on the input data, the combination logic CL1 is likely to conduct simple logic processing. The results of this processing

Roles of Clock

becomes the input of the memory element, register R1. Since the processing time is data dependent, $t_{l,min}$ and $t_{l,max}$ are the minimum and maximum delays of the combination logic respectively. The input data must be settled at a minimum time of $t_{l,max}$ before the clock's rising edge (t_ϕ) is applied on register R1. In the figure, the data is settled $t_m + t_{l,max}$ before the clock's rising edge, where t_m is the timing margin. When the clock's rising edge is applied on the register R1, the data will latch onto the output of register R1, where $t_{r,min}$ and $t_{r,max}$ are the minimum and maximum propagation delays of the register respectively. Following this, the data at the output of the register will not be affected by the input of register R1. Before the data reaches the input of the next combination logic CL2, it will pass through an interconnect with a propagation delay of t_i . The second logic processing step is performed and the results are kept at the input of the second register R2, while waiting for the next clock rising edge, $t_\phi + T$.

In mixed-signal data converter circuits, the ADC and DAC are circuits that interface between the analog and digital environments respectively. The clock plays an important role in the process of converting analog signals to digital signals or vice versa, and the sample-and-hold circuit in the ADC and the output data of the DAC are both driven by a clock [2], [3]. Fig. 2.2 shows the input and output signals of the ADC and DAC. The sample-and-hold circuit at the input of the ADC is controlled by a periodic timing clock. The analog signal will be sampled by the circuit at every period of the clock and the digital output signal represents the analog signal at the instant of every clock period. Meanwhile, the DAC outputs the digital signal based on the timing of the clock. The output signal of the DAC will be filtered by a low pass filter to remove higher-order harmonics and to produce a smooth analog signal as shown in Fig. 2.2.

Fig. 2.2: Input and Output Signals of ADC and DAC.

A frequency synthesizer in an RF transceiver is a clock generation circuit with a specific frequency for frequency translation. The IF signal in a transmitter at IF frequency (f_{IF}) from the baseband will be up-converted by a local oscillator (LO) frequency (f_{LO}) from the frequency synthesizer through a mixer. The up-converted RF signal contains a higher carrier RF frequency (f_{RF}) as well as information associated with the IF signal, that is transmitted through the air. At the receiver's end, the RF signal will be amplified by a low noise amplifier (LNA) and down-converted by f_{LO} through a mixer. The carrier frequency in the received RF signal will be discarded and the IF signal carrying information will be passed along to the baseband circuit for further processing [4]. The frequency translation using the ideal frequency synthesizer spectrum is shown in Fig. 2.3 below.

Fig. 2.3: Frequency Translation with Ideal Frequency Synthesizer Spectrum.

The RF signal at receiver consists of low power desired channel and high power adjacent channel. This is a very common arrangement in wireless communication. Because desired channel users are located close to the base-station, and adjacent channel users are located further away, the base-station needs to transit a much higher power signal for adjacent channel users than for channel users who are closer. When the RF signal is down-converted by the ideal LO signal, both the desired and adjacent channels will be down-converted to IF signals with the same shape and frequency offset. The undesired adjacent channel will then be filtered out by the IF filter.

2.3 Imperfection of Clock

In most clock generation circuits used currently, an active circuit is used to satisfy system integration requirements. Like MOS transistors, active circuits are noisy, with the most significant noise source being the thermal noise generated in the resistive channel of the transistor's active region. This thermal noise is caused by the random motion of electrons in an ohmic conductor which introduce fluctuations in voltage across the conductor. Further, the dangling bonds at the oxide-silicon interface give rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing flicker noise in the drain current [5]. These noise sources cause uncertainties at the clock output. Because the generation of noise is a random process, the clock suffers random timing fluctuations known as random jitter. The timing of the clock edge can be represented by a Gaussian distribution function [5]. The time and frequency domain of an ideal clock as well as that of a real-life clock that suffers random fluctuations are shown in Fig. 2.4. In an ideal clock, the clock edge occurs exactly at T_o period, and the spectrum of the clock is centered at a LO frequency (f_{LO}), where $f_{LO}=1/T_o$. The random timing fluctuation in the frequency domain will spread the carrier power over neighboring frequencies and create a phase noise "skirt" [75].

Imperfection of Clock

Fig. 2.4: Time and Frequency Domain for Ideal and Non-Ideal Clock with Random Noise.

The clock generation circuit is a circuit that generates an output clock from a reference clock. The output clock will be used to drive other circuits for synchronization purposes. Because the power supply and substrates are shared between these circuits, the periodic fluctuation of the reference circuit and other driven circuits can easily couple into the clock generation circuit. This will cause the generated clock edge to fluctuate after a few periods. In addition, the device mismatch in the clock generation circuit will also introduce systematic clock fluctuations, which will repeat after a few periods of clock. This systematic timing fluctuation is known as the deterministic jitter. The time and frequency domains for ideal and non-ideal clocks that suffer the effects of such systematic noise are shown in Fig. 2.5. In the non-ideal clock, a periodic systematic fluctuation occurs at every T_{os} period. This fluctuation will translate into a spurious tone in the clock's spectrum [88]. The frequency offset of the spurious tone from the clock's frequency (f_{LO}) is $1/T_{os}$.

Imperfection of Clock

Fig. 2.5: Time and Frequency Domain for Ideal and Non-Ideal Clock with Systematic Noise.

2.4 System Impact of Clock Jitter

The ideal clock is unachievable in the real world, and both random and systematic timing fluctuations typically have a profound impact on the system as described in Chapter 2.2. In a high-speed digital circuit, the frequency of the clock increases to a maximum. Fig. 2.6 shows that the minimum clock period (T_{min}) of the high speed digital circuit is equal to $t_{l,max} + t_{r,max} + t_i + t_m$. As long as T_{min} is larger than $t_{l,max} + t_{r,max} + t_i$, the output data from register R1 can be passed through the combination logic CL2 and latched successfully onto the register R2. The timing margin (t_m) provides a safeguard for the correct operation of the digital circuit. However, when timing fluctuations rise, the timing margin will be reduced, and if the timing fluctuation is large enough, it is possible that no margin may remain at all. In this case, the digital circuit will clock the data wrongly onto the register, increasing the data error rate or even causing some digital systems to malfunction. To eliminate this problem, the timing margin has to be increased at the expense of the operating speed.

System Impact of Clock Jitter

Fig. 2.6: Impact of Timing Fluctuation on Digital System.

In a mixed-signal data converter circuit, the clock drives the sample-and-hold circuit in the ADC to reproduce the analog signal in the digital domain. Ideally, a perfect clock would be able to accurately reproduce the analog signal. However, the reality remains that the timing fluctuations of any clock will cause the data sampled from the analog signal to deviate from the ideal signal. As depicted in Fig. 2.7, the errors become more significant at the portion of the analog signal which has a high slew rate. For a high resolution ADC, the timing fluctuation of the clock must be lower than 0.5 LSB of the ADC. Otherwise, it will affect the ADC’s sampling resolution and degrade its dynamic range.

System Impact of Clock Jitter

Fig. 2.7: Impact of Timing Fluctuation on ADC.

In an RF transceiver, the imperfections of the clock (which in frequency domain terms is translated into phase noise “skirt”) will down-convert the RF signal into an IF signal with extra “skirting” on both sides as illustrated in Fig. 2.8. The large skirting in the adjacent channel will leak into the desired channel and reduce the SNR of the desired channel, thus affecting the sensitivity of the receiver. As in the transmitter, the phase noise “skirt” will up-convert the IF signal into an RF signal and the extra “skirting” on both sides of the RF signal will cause interference to the neighboring channels.

System Impact of Clock Jitter

Fig. 2.8: Impact of Phase Noise on RF transceiver.

Chapter 3

Frequency Multiplier Architectures

3.1 Introduction

The direct use of crystal oscillators as clocks for electronic systems is impractical because of the higher speed requirements of integrated circuits. In addition, crystal oscillators operating at frequencies of 100MHz or higher are difficult to manufacture and expensive. A frequency multiplier circuit is thus necessary to generate higher clock frequencies for the electronic system from a reference frequency generated by a crystal oscillator.

There are many ways to implement a frequency multiplier. However, because of their relatively low power requirements, small surface area and system integration on CMOS process, PLL and DLL based designs are the most popular forms. The PLL-based frequency multiplier is a feedback system that locks the reference clock's phase with the feedback clock's phase. The feedback clock is generated by an N -divider which is driven by a VCO [2], [5], [6] with an output frequency that is N times the reference frequency. Because of the PLL's low phase noise and low spurious tones, it provides relatively superior performance and is currently the most commonly used frequency multiplier. Another popular frequency multiplier type is the DLL-based circuit. DLL is a PLL with its VCO replaced by a voltage-controlled delay line (VCDL) that consists of N delay cells. The feedback system of the DLL locks the delay of the VCDL such that it is equal to the period of the reference clock. Each clock edge generated by delay cells in VCDL is combined by an edge combiner (EC)

Frequency Multiplier Architectures

to generate N times the output frequency [2]. The advantage of the DLL is that the jitter does not accumulate from one cycle to another, allowing it to achieve better jitter performance [50], [79].

In this chapter, we discuss the fundamental operation of the PLL and DLL architectures along with the effects of random and deterministic noise. The noise performance of the PLL and DLL are compared with the intention of selecting the architecture with the potential to achieve the lowest jitter.

3.2 Phase Locked Loop Fundamentals

Fig. 3.1: Architecture of Conventional PLL-based Frequency Multiplier.

Fig. 3.1 shows the architecture of a conventional PLL-based frequency multiplier which consists of a crystal oscillator that serves as a reference clock, a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a differential-to-single-ended converter (D2S), a voltage-controlled oscillator (VCO) and an N -divider (divide ratio of N). The VCO consists of a number of delay cells [2], [5], [6], [72]-[74].

The PLL is essentially a feedback system that compares the clock phase of the N -divider (ϕ_{div}) with the reference clock phase of the crystal oscillator (ϕ_{ref}). A low jitter crystal oscillator is used as reference clock to achieve a low jitter frequency multiplier. When the PLL is powered up, the control voltage (V_c) equals to 0V, such that the VCO oscillates at a free running frequency. In this example, we assume the free running frequency is lower than the locking frequency. The operational

Phase Locked Loop Fundamentals

waveform of the PFD is shown in Fig. 3.2. PFD is a digital circuit that compares the phase difference that exists between the reference clock (V_{ref}) and N -divider clock (V_{div}). When the N -divider's clock phase (ϕ_{div}) is lagging behind that of the reference clock's phase (ϕ_{ref}), the output of the PFD will generate a pulse signal (UP) with a width that is proportional to the phase difference ($\phi_{ref} - \phi_{div}$) between V_{ref} and V_{div} . Meanwhile, the DN will generate a minimum pulse width signal. The purpose of this is to eliminate the dead zone problem on the PFD. As illustrated in Fig. 3.2, the area of the UP signal is larger than that of the DN signal. Therefore, more current is charged into the LF than that which sinks from it. As a result, the control voltage (V_c) is charged up, and this serves to increase the frequency of the VCO. The effect of the resistor R_I is excluded in the LF for simplicity of illustration.

Fig. 3.2: Operation Waveforms of PFD.

At steady state, the ϕ_{ref} and ϕ_{div} are aligned and the frequencies of the reference clock (f_{ref}) and N -divider clock (f_{div}) are the same. Since the N -divider is driven by the

Phase Locked Loop Fundamentals

VCO, the VCO's output frequency (f_{out}) becomes N times higher than that of the f_{div} . Therefore, $f_{out} = N \cdot f_{ref}$, and the frequency multiplier has a multiplication factor of N . The operation waveforms of the PLL-based frequency multiplier at a steady state are shown in Fig. 3.3 and the multiplication factor of the PLL is set at eight for purposes of illustration.

Fig. 3.3: Operation Waveforms of PLL-based Frequency Multiplier at Steady State.

Due to the two pure integrators exist in the feedback loop, which is contributed by CP combined with the LF capacitor and integration function of the VCO. The closed-loop system contains two imaginary poles that cause disturbances in system stability. To address this instability, a resistor R_I is added in the LF such that it introduces a zero into the loop. Given that the CP drives the series combination of R_I and C_I in the LF, each time a current is injected into the LF, the control voltage (V_c) experiences a large jump. The resulting ripple disturbs the VCO severely. To address this disturbance and suppress the ripple, a second capacitor (C_2) which is smaller than C_I is added in parallel to R_I and C_I . [5].

3.3 PLL Noise Analysis

3.3.1 PLL Random Noise Analysis

In the implementation of a PLL-based frequency multiplier, the specification of the jitter or phase noise essentially determines the architecture of the VCO. Although an LC-tank oscillator has better jitter or phase noise than a ring oscillator, there are some trade-offs in the performance of the two oscillator types. Firstly, when cost is a primary concern, the ring oscillator PLL-based frequency multiplier is clearly the superior choice for digital CMOS processing as the LC-tank oscillator needs additional processing capabilities for inductor fabrication that dramatically increase the cost of fabrication. In addition, the area of the inductor is very large compared to that of a ring oscillator. Most importantly perhaps, the ease of process migration makes the ring oscillator a better choice.

In this analysis, the frequency multiplier is designed to have a multiplication factor of eight. This requires the clock to be easily generated by a 25MHz crystal oscillator for a 200Msps ADC. The VCO is a ring oscillator with differential delay cells to better supply noise and reject substrate noise. Three delay cells are used to minimize the jitter and power consumption of the VCO. This is the minimum number of delay cells required to start up the oscillation properly [5], [76] as two delay cells are unable to achieve a phase shift of more than 360° for proper startup.

According to [89], the jitter variance of the PLL output due to the VCO jitter is

$$\sigma_{\Delta_{N1}}^2 = \sigma_{\Delta_{VCO}}^2 \cdot \frac{N}{\varepsilon_{PLL} \cdot \left[2 - \varepsilon_{PLL} \cdot \left(1 + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1} \right) \right]} \quad (3-1)$$

PLL Noise Analysis

where $\sigma_{\Delta t_{VCO}}^2$ is the variance of the VCO period jitter, N is the divider ratio, T_{ref} is the period of reference of the crystal oscillator clock and ε_{PLL} is the normalized loop bandwidth of the PLL [89]. It can be shown that

$$\varepsilon_{PLL} = \frac{I_{CP} \cdot K_{VCO} \cdot R_1 \cdot T_{ref}}{2\pi \cdot N} \cong w_0 \cdot T_{ref} \quad (3-2)$$

where I_{CP} is the CP source and sink current, K_{VCO} is the VCO gain, and w_0 is the PLL loop bandwidth.

Meanwhile, the jitter variance of the PLL output due to the PFD, CP and divider can be represented as follows

$$\sigma_{\Delta t_{N2}}^2 = \sigma_{\Delta t_{synth}}^2 \cdot \frac{\varepsilon_{PLL} + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1} \cdot (2 + \varepsilon_{PLL})}{2 - \varepsilon_{PLL} \cdot \left(1 + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1}\right)} \quad (3-3)$$

where $\sigma_{\Delta t_{synth}}^2$ is the jitter variance of the PFD, CP and divider that referred back to the input of the PFD.

The jitter variance of the PLL output due to the jitter of the input reference from the crystal oscillator clock can be obtained as

$$\sigma_{\Delta t_{N3}}^2 = \sigma_{\Delta t_{ref}}^2 \cdot \frac{\varepsilon_{PLL} + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1} \cdot (2 + \varepsilon_{PLL})}{2 - \varepsilon_{PLL} \cdot \left(1 + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1}\right)} \quad (3-4)$$

where $\sigma_{\Delta t_{ref}}^2$ is jitter variance of the input reference crystal oscillator clock.

PLL Noise Analysis

Finally, the resistor in the LF will cause thermal noise at the input of the VCO, contributing to the jitter at the output of the PLL. The jitter variance due to the LF resistor can be represented as

$$\sigma_{\Delta N4}^2 = kT \cdot \frac{K_{VCO} \cdot T_{ref}^2}{\pi \cdot N \cdot I_{CP}} \cdot \frac{1}{(2 - \varepsilon_{PLL})} \quad (3-5)$$

where k is the Boltzmann constant and T is the absolute temperature.

Since $\sigma_{\Delta N1}^2, \sigma_{\Delta N2}^2, \sigma_{\Delta N3}^2$ and $\sigma_{\Delta N4}^2$ are caused by the thermal noise and flicker noise of transistors in the VCO, PFD/CP, crystal oscillator and LF resistor respectively, each noise is independent and uncorrelated. According to [5], in noise analysis, the average noise power, P_{av} , of the two added noise waveforms $x_1(t)$ and $x_2(t)$ can be shown as

$$\begin{aligned} P_{av} &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} [x_1(t) + x_2(t)]^2 dt \\ &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} [x_1(t)]^2 dt + \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} [x_2(t)]^2 dt + \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} [2 \cdot x_1(t) \cdot x_2(t)] dt \\ &= P_{av1} + P_{av2} + \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} [2 \cdot x_1(t) \cdot x_2(t)] dt \end{aligned} \quad (3-6)$$

where P_{av1} and P_{av2} denote the average power of $x_1(t)$ and $x_2(t)$ respectively. The third term in equation (3-6) indicates the correlation between $x_1(t)$ and $x_2(t)$ or how similar these two waveforms are. If the noise waveforms were generated by independent devices, they would be uncorrelated and the third term would be zero. In such a case, $P_{av} = P_{av1} + P_{av2}$. Thus, the total output jitter variance of the PLL output can be represented as

$$\sigma_{\Delta NT}^2 = \sigma_{\Delta N1}^2 + \sigma_{\Delta N2}^2 + \sigma_{\Delta N3}^2 + \sigma_{\Delta N4}^2 \quad (3-7)$$

PLL Noise Analysis

In practical implementation of the PLL, the noise from the reference clock ($\sigma_{\Delta t_{N3}}^2$) and the LF resistor ($\sigma_{\Delta t_{N4}}^2$) are very small and can be neglected in comparison to the other noise sources. Therefore, the equation (3-7) can be rewritten as

$$\begin{aligned}\sigma_{\Delta t_{NT}}^2 &= \sigma_{\Delta t_{N1}}^2 + \sigma_{\Delta t_{N2}}^2 \\ &= \sigma_{\Delta t_{VCO}}^2 \cdot \frac{N}{\varepsilon_{PLL} \cdot \left[2 - \varepsilon_{PLL} \cdot \left(1 + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1} \right) \right]} + \sigma_{\Delta t_{synth}}^2 \cdot \frac{\varepsilon_{PLL} + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1} \cdot (2 + \varepsilon_{PLL})}{2 - \varepsilon_{PLL} \cdot \left(1 + \frac{T_{ref}}{2 \cdot R_1 \cdot C_1} \right)} \\ &\cong \sigma_{\Delta t_{VCO}}^2 \cdot \frac{N}{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})} + \sigma_{\Delta t_{synth}}^2 \cdot \frac{\varepsilon_{PLL}}{2 - \varepsilon_{PLL}}\end{aligned}\quad (3-8)$$

where it is assumed that $\frac{T_{ref}}{2 \cdot R_1 \cdot C_1}$ is negligible with respect to one [89]. From (3-8),

it is clear that when the PLL's normalized bandwidth (ε_{PLL}) increases, the noise contributed by the VCO at PLL output ($\sigma_{\Delta t_{N1}}^2$) can be suppressed. However, the noise contributed by the PFD, CP and divider at PLL output ($\sigma_{\Delta t_{N2}}^2$) will increase and vice versa.

From [76], the delay of a delay cell (t_d) can be expressed as

$$t_d = V_{pp} \left(\frac{C_L}{I_{ss}} \right) \quad (3-9)$$

where V_{pp} , C_L and I_{ss} are one half of the full differential output swing, output capacitance and tail current of a delay cell respectively. The normalized jitter ($\frac{\Delta t_d}{t_d}$)

can be obtained as

$$\frac{\Delta t_d}{t_d} = \sqrt{\frac{kT}{C_L}} \cdot \frac{\xi}{V_{GS} - V_T} \quad (3-10)$$

PLL Noise Analysis

where ξ and $V_{GS}-V_T$ are the noise contribution factors and overdrive voltages of the NMOS differential pair transistors, respectively.

From equation (3-9) and (3-10), the jitter of a delay cell (Δt_d) can be rearranged as

$$\begin{aligned}\Delta t_d &= a_v \xi \cdot \sqrt{\frac{kT \cdot t_d}{V_{pp}}} \cdot \frac{1}{\sqrt{I_{ss}}} \\ &= a_v \xi \cdot \sqrt{\frac{kT}{2 \cdot M \cdot N \cdot f_{ref} \cdot V_{pp}}} \cdot \sqrt{\frac{1}{I_{ss}}}\end{aligned}\quad (3-11)$$

where $a_v = \frac{V_{pp}}{V_{GS} - V_T}$, $t_d = \frac{1}{2 \cdot M \cdot N \cdot f_{ref}}$, a_v , M and f_{ref} are small-signal gains of the delay cell, the number of delay cells in the VCO and the reference frequency, respectively.

To simplify the analysis, the noise contributed by PFD, CP and the divider ($\sigma_{\Delta t_{synth}}^2$) are first assumed to be negligible and the ring oscillator VCO is assumed to be the most dominant noise source in the PLL. Thus, equation (3-8) will become

$$\sigma_{\Delta NT}^2 \cong \sigma_{\Delta VCO}^2 \cdot \frac{N}{\epsilon_{PLL} \cdot (2 - \epsilon_{PLL})} \quad (3-12)$$

PLL Noise Analysis

From (3-11) and (3-12), the rms random jitter of the PLL output can be expressed as

$$\begin{aligned}
 \Delta t_{rj,PLL} &= \sqrt{\sigma_{\Delta t_{NT}}^2} \\
 &\cong \sqrt{\sigma_{\Delta t_{VCO}}^2 \cdot \frac{N}{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})}} \\
 &\cong \sqrt{\left(2 \cdot M \cdot a_v^2 \xi^2 \cdot \frac{kT}{2 \cdot M \cdot N \cdot f_{ref} \cdot V_{pp}} \cdot \frac{1}{I_{ss}} \right) \cdot \frac{N}{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})}} \\
 &\cong \sqrt{\left(4 \cdot \frac{kT}{f_{ref} \cdot V_{pp}} \cdot \frac{M}{I_T} \right) \cdot \frac{1}{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})}} \quad (3-13) \\
 &\cong \sqrt{\frac{4 \cdot M}{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})}} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}} \\
 &\cong \sqrt{\frac{12}{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})}} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}} \\
 &\cong \frac{1}{\sqrt{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})}} \cdot \sqrt{12} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}} \\
 &\cong \alpha \cdot \sqrt{12} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}}
 \end{aligned}$$

where $\sigma_{\Delta t_{VCO}}^2 = 2 \cdot M \cdot (\Delta t_d)^2$ and $\alpha = \frac{1}{\sqrt{\varepsilon_{PLL} \cdot (2 - \varepsilon_{PLL})}}$ are defined as the accumulation factors of the PLL [79]. From the equation above, it is clear that the random jitter of the PLL due to noise from the VCO can be minimized by increasing the normalized bandwidth (ε_{PLL}). However, for reasons of stability, the upper limit of the PLL normalized bandwidth is set at about 1/20th the reference frequency used at the input of the PFD, after considering process-related variations [36].

PLL Noise Analysis

The maximum normalized loop bandwidth can be expressed as

$$\varepsilon_{PLL,max} \cong W_{0,max} \cdot T_{ref} \cong \frac{2 \cdot \pi \cdot f_{ref}}{20} \cdot T_{ref} \cong \frac{\pi}{10} \quad (3-14)$$

Thus, the minimum accumulation factor is

$$\begin{aligned} \alpha_{min} &= \frac{1}{\sqrt{\varepsilon_{PLL,max} \cdot (2 - \varepsilon_{PLL,max})}} \\ &= \frac{1}{\sqrt{\frac{\pi}{10} \cdot \left(2 - \frac{\pi}{10}\right)}} \\ &\cong 1.37 \end{aligned} \quad (3-15)$$

After taking the noise contributed by the PFD, CP and divider ($\sigma_{\Delta t_{synth}}^2$) into consideration, it becomes necessary to decrease the PLL's normalized bandwidth to suppress the contribution of $\sigma_{\Delta t_{synth}}^2$ to the output jitter. There is an optimum bandwidth value at which both the noise contributed to the PLL by the VCO and the other PLL blocks (PFD, CP and divider) are equal [89]. By setting the bandwidth at this value, the accumulation factor of the PLL increases such that it is larger than 1.37. This figure depends on the amount of noise contributed by the PFD, CP and divider.

3.3.2 PLL Deterministic Noise Analysis

It is impossible to design a circuit for use in a CMOS process that matches 100% [83]-[85] and the mismatch between the circuits to the output clock is architecture dependant. In the PLL, the period of the output clock is totally transparent to the delay cell mismatch. As shown in Fig. 3.4, the period of the output clock (T_{out}) is defined as twice the total delay of the delay cells in the VCO. It is expressed as follows:

$$T_{out} = 2 \cdot (t'_d + 2 \cdot t_d) \quad (3-16)$$

where the t'_d is the delay of the mismatch delay cell (grey delay cell), while t_d is the delay of an ideal delay cell. As illustrated in Fig. 3.4, the first and second period of the $\phi_0(V_{out})$ are equal, and they are not affected by the mismatch in the delay cell. The only question is whether the T_{out} is larger or smaller than the ideal period, but in a steady state, this mismatch is compensated for by the control voltage (V_c).

Fig. 3.4: The Effect of Delay Cells Mismatch in PLL.

The mismatch between the CP current source and the CP current sink will cause further jitters at the PLL output clock. The operation waveforms of CP in an ideal case are shown in Fig. 3.5(a).

PLL Noise Analysis

Fig. 3.5: Operation Waveforms of CP at (a) Ideal Case (b) Non-ideal Case with CP Current Mismatch (c) Non-ideal Case at Steady State.

In the ideal case, the CP source current (I_{UP}) and sink current (I_{DN}) are equal. I_{UP} and I_{DN} will charge and discharge the LF at the same time and with the same period. Therefore, no net charge or discharge arises from the LF and the control voltage (V_c) will remain constant. In this example, there are mismatches in both current sources and the I_{UP} is larger than I_{DN} . The feedback mechanism of the PLL will cause the divider clock phase (ϕ_{div}) to lead the reference clock phase (ϕ_{ref}) with the static phase error of ϕ_{err} compensating for the mismatch in the current sources. With this compensation, the total charge and discharge of the LF becomes equal, bringing the net charge in the LF to zero [86]. However, the static phase error between the reference clock (V_{ref}) and divider clock (V_{div}) will generate a ripple at control voltage (V_c) which will cause a phase change in the PLL output clock for every reference clock period. Thus, it introduces jitter at the PLL output clock. This phase change at the PLL output clock is proportional to the mismatch of the current sources. Because the mismatch is systematic in that it causes a fix pattern jitter at the output clock, it is known as a deterministic jitter.

PLL Noise Analysis

For purposes of analysis, it is assumed from Fig. 3.5(c) that $I_{UP} = I_{CP}$ and $I_{DN} = (1 - \varepsilon) \cdot I_{CP}$, where I_{CP} is the ideal charge pump current and ε is the normalized current mismatch of I_{DN} compared with I_{UP} . At steady state, the total net charge to the LF is zero. This leads to

$$\begin{aligned}
 Q_{UP} &= Q_{DN} \\
 I_{CP} \cdot t_{pw} &= (1 - \varepsilon) \cdot I_{CP} \cdot (t_{err} + t_{pw}) \\
 1 &= (1 - \varepsilon) \cdot \left(1 + \frac{t_{err}}{t_{pw}} \right) \\
 1 &= 1 - \varepsilon + \frac{t_{err}}{t_{pw}} - \varepsilon \cdot \frac{t_{err}}{t_{pw}} \\
 1 &\cong 1 - \varepsilon + \frac{t_{err}}{t_{pw}} \\
 t_{err} &\cong \varepsilon \cdot t_{pw}
 \end{aligned} \tag{3-17}$$

where Q_{UP} , Q_{DN} , t_{err} and t_{pw} are the charges from the I_{UP} , the charges to the I_{DN} , the static phase error in the time domain and the minimum pulse width reset signal of the PFD respectively. Herewith, it is assumed that $\varepsilon \ll 1$ and $\varepsilon \cdot \frac{t_{err}}{t_{pw}} \ll \frac{t_{err}}{t_{pw}}$. From Fig. 3.5(c), the maximum value of V_c will discharge (V_{pk}). Assuming a constant current from a charge pump discharges a capacitor over a period of time, V_{pk} can be derived as follows:

$$\begin{aligned}
 V_{pk} &= \frac{(1 - \varepsilon) \cdot I_{CP} \cdot t_{err}}{C_2} \\
 &= \frac{(1 - \varepsilon) \cdot I_{CP} \cdot \varepsilon \cdot t_{pw}}{C_2} \\
 &\cong \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}}{C_2}
 \end{aligned} \tag{3-18}$$

where C_2 is the parallel capacitor in the LF. The output signal of the VCO can be obtained as [5]

$$V_{out}(t) = V_m \cdot \cos(w_0 \cdot t + 2\pi \cdot K_{VCO} \cdot \int V_c \cdot dt) \tag{3-19}$$

PLL Noise Analysis

where V_m and w_0 are VCO output amplitudes and the VCO's free running frequency respectively. The term $2\pi \cdot K_{VCO} \cdot \int V_c \cdot dt$ in the equation is the excess phase (ϕ_{ex}) of the VCO with respect to the free running frequency. Therefore, the excess phase due to the glitch of the mismatch is derived as follows:

$$\begin{aligned}
 \phi_{ex} &= 2\pi \cdot K_{VCO} \cdot \int V_c \cdot dt \\
 &= 2\pi \cdot K_{VCO} \cdot \frac{1}{2} \cdot V_{pk} \cdot (t_{err} + t_{pw}) \\
 &= \pi \cdot K_{VCO} \cdot \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}}{C_2} \cdot (1 + \varepsilon) \cdot t_{pw} \\
 &\cong \pi \cdot K_{VCO} \cdot \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}^2}{C_2}
 \end{aligned} \tag{3-20}$$

Thus, the timing error due to the CP mismatch is obtained as

$$\begin{aligned}
 \Delta t_{CP} &= \frac{\phi_{ex}}{w_0} \\
 &\cong \frac{\pi \cdot K_{VCO} \cdot \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}^2}{C_2}}{2\pi \cdot f_{out}} \\
 &\cong K_{VCO} \cdot \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}^2}{2 \cdot f_{out} \cdot C_2}
 \end{aligned} \tag{3-21}$$

Although the CP is updated for every reference clock period, the timing error due to the CP mismatch happens only once in every eight cycles of the output clock. Thus, the rms of the deterministic jitter due to CP mismatch can be represented as

$$\begin{aligned}
 \Delta t_{dj,PLL_CP} &= \sqrt{\frac{(\Delta t_{CP})^2}{N}} \\
 &= K_{VCO} \cdot \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}^2}{2 \cdot \sqrt{N} \cdot f_{out} \cdot C_2} \\
 &= K_{VCO} \cdot \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}^2}{2 \cdot \sqrt{8} \cdot f_{out} \cdot C_2}
 \end{aligned} \tag{3-22}$$

3.4 Delay Locked Loop Fundamentals

Fig. 3.6: Architecture of Conventional DLL-based Frequency Multiplier.

Fig. 3.6 shows the architecture of a conventional DLL-based frequency multiplier. The DLL-based frequency multiplier consists of a crystal oscillator that serves as a reference clock, a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a differential-to-single-ended converter (D2S), a voltage-controlled delay line (VCDL) and an edge combiner (EC) [2], [87]. The VCDL consists of a number of delay cells. In this example, the VCDL consists of eight delay cells for the multiplication factor of eight.

The DLL-based frequency multiplier takes advantage of the low jitter crystal oscillator clock edge (ϕ_{ref}) and uses it as a reference clock edge. The reference clock edge (ϕ_{ref}) will pass through the VCDL and generate a series of clock edges, ϕ_1 to ϕ_8 .

Delay Locked Loop Fundamentals

Because the delay of each cell in the VCDL is equal, the generated clock edges, ϕ_1 to ϕ_8 , will be spaced equally. The last clock edge (ϕ_8) will be fed back to the PFD and it will be compared with the reference clock edge (ϕ_{ref}). The operation of the PFD in this scenario is the same as the PFD of the PLL illustrated in Fig. 3.2. The leading or lagging of the last clock edge (ϕ_8) with respect to the reference clock edge (ϕ_{ref}) will cause the PFD to generate either an *UP* or *DN* pulse with which to turn on the current source or current sink of the CP. The pulse width of the *UP* and *DN* signal is proportional to the phase difference between ϕ_{ref} and ϕ_8 . The current source or sink from the CP will charge up or charge down the control voltage (V_c) at LP. This control voltage (V_c) will then adjust the delay of the delay cells in the VCDL. At steady state, the last clock edge (ϕ_8) will be aligned with the reference clock edge (ϕ_{ref}). The total delay of the VCDL is equal to that of one period of the crystal oscillator reference clock (T_{ref}). Consequently, the clock edges generated by VCDL will be spaced equally with the delay of $\frac{1}{8} \cdot T_{ref}$, where T_{ref} is the period of the reference clock from the crystal oscillator. Since the clock edges generated by the VCDL are seen as differential signals, a D2S becomes necessary in order to convert the differential signal to a rail-to-rail single-ended signal for digital edge combination purposes. In the EC circuit, there are pulse generators that generate a signal with pulse widths close to half the period length of the output clock (T_{out}) when each rising edge occurs at the input of EC. After edge combination, the output clock frequency (f_{out}) is equal to $8 \cdot f_{ref}$ with the duty cycle close to 50% and where the f_{ref} is the reference clock frequency. The operation waveforms of the DLL-based frequency multiplier at steady state are illustrated in Fig. 3.7.

Delay Locked Loop Fundamentals

Fig. 3.7: Operation Waveforms of the DLL-based Frequency Multiplier.

Unlike in the PLL, there is only one integrator in the feedback loop of the DLL which is contributed to by the CP in combination with the LF capacitor. This pre-empts stability related concerns similar to those in the PLL from occurring. The single capacitor in the LF becomes sufficient and the loop filter zero is no longer necessary.

There is another variant of DLL, which is known as a multiplying delay-locked loop (MDLL). The MDLL consists of delay cells connected in a closed loop much like a VCO. The output of the MDLL clock will be aligned with that of the reference clock after a few periods of the reference clock [91], [92]. MDLL takes advantage of the realigning of the output clock with the reference clock such that the resultant jitter performance of the MDLL lies in between that of the PLL and DLL. The MDLL output clock's random jitter is better than that of the PLL's because of jitter accumulation in the PLL. The MDLL only accumulates for a few cycles before realigning with the reference clock and it is not therefore better than the DLL in this

Delay Locked Loop Fundamentals

regard. Nonetheless, MDLL can reduce the deterministic jitter due to the mismatch in the delay cells of the DLL. This is because the output clock of the MDLL is not defined by the clock edges of the delay cells and the EC. The MDLL's output is like that of the VCO of the PLL, which is transparent to the mismatch in the delay cells.

3.5 DLL Noise Analysis

3.5.1 DLL Random Noise Analysis

In this analysis, the DLL-based frequency multiplier is designed to have a multiplication factor of eight. The VCDL is constructed with differential delay cells for better supply noise and substrate noise rejection. To minimize the jitter and power consumption of the VCDL, the number of delay cells is a multiplication factor of eight. We ignore the noise contribution of the D2S and EC as these are not dominant sources. The D2S consists only of one differential pair amplifier, while the conventional delay chain consists of at least eight differential pair amplifiers. Therefore, the random device noise contributed by the whole delay chain is much higher than that of the single D2S. Meanwhile, the EC consists of high speed digital circuits with a high slew rate. Such a high slew rate signal has less exposure time to the device noise, thus providing better jitter or noise performance.

According to [89], the jitter variance of the last output tap of the DLL that arises from the jitter in the delay cells is given as follows:

$$\sigma_{\Delta_{N1}}^2 = \sigma_{\Delta_d}^2 \cdot N \cdot \frac{2}{2 - \varepsilon_{DLL}} \quad (3-23)$$

where $\sigma_{\Delta_d}^2$ is the jitter variance of a delay cell, N is the number of delay cells in the VCDL, and ε_{DLL} is the normalized loop bandwidth of the DLL [89]. ε_{DLL} can be defined as

$$\varepsilon_{PLL} = \frac{I_{CP} \cdot K_d}{C_f} \cong w_0 \cdot T_{ref} \quad (3-24)$$

where I_{CP} is the CP source and sink current, K_d is the VCDL gain, C_f is the capacitance in the LF, w_0 is the DLL loop bandwidth and T_{ref} is the period of the reference clock from the crystal oscillator.

DLL Noise Analysis

Meanwhile, the jitter variance of the DLL output due to the PFD and CP can be expressed as

$$\sigma_{\Delta N2}^2 = \sigma_{\Delta PFD}^2 \cdot \frac{\epsilon_{DLL}}{2 - \epsilon_{DLL}} \quad (3-25)$$

where $\sigma_{\Delta PFD}^2$ is jitter variance of the PFD and CP that refers back to the input of the PFD.

The jitter variance of the DLL's output arising from the jitter of the input reference clock from the crystal oscillator is obtained as

$$\sigma_{\Delta N3}^2 = \sigma_{\Delta ref}^2 \cdot \left(1 + \frac{4 \cdot \epsilon_{DLL}}{2 - \epsilon_{DLL}} \right) \quad (3-26)$$

where $\sigma_{\Delta ref}^2$ is the jitter variance of the input reference clock from the crystal oscillator.

Assuming that the jitter from each noise source is uncorrelated, the total output jitter variance at the last output tap of the DLL can be represented as

$$\sigma_{\Delta NT}^2 = \sigma_{\Delta N1}^2 + \sigma_{\Delta N2}^2 + \sigma_{\Delta N3}^2 \quad (3-27)$$

The DLL takes advantage of the crystal oscillator's low jitter reference clock edge to generate clock edges that space equally across a period of the reference clock for frequency multiplication purpose. The resultant noise from the reference clock ($\sigma_{\Delta N3}^2$) is thus very small and can be neglected in relation to other larger noise sources. The equation (3-27) can so be simplified as

$$\begin{aligned} \sigma_{\Delta NT}^2 &\cong \sigma_{\Delta N1}^2 + \sigma_{\Delta N2}^2 \\ &\cong \sigma_{\Delta d}^2 \cdot N \cdot \frac{2}{2 - \epsilon_{DLL}} + \sigma_{\Delta PFD}^2 \cdot \frac{\epsilon_{DLL}}{2 - \epsilon_{DLL}} \end{aligned} \quad (3-28)$$

From above equation, it is clear that the total jitter variance is at a minimum when the value of the normalized loop bandwidth (ϵ_{DLL}) is low. It can be noted that the noise

DLL Noise Analysis

contributed by the PFD and CP ($\sigma_{\Delta PFD}^2$) is suppressed by the large capacitor value in the LF. Therefore, the jitter caused by the PFD and CP can be neglected and the VCDL's m^{th} tap output jitter arising from noise in the delay cells is approximately equal to the stochastic jitter of the uncontrolled VCDL [89]. This yields

$$\Delta t_{dm} = \sqrt{m} \cdot \Delta t_d \quad (3-29)$$

where m is the number of delay cells cascaded at the m^{th} tap output of the VCDL. Since the number of delay cells equals the multiplication factor, the m^{th} tap output of the VCDL has m delay cells cascaded.

From equation (3-11), the jitter of a delay cell, Δt_d , can be rearranged as

$$\begin{aligned} \Delta t_d &= a_v \xi \cdot \sqrt{\frac{kT \cdot t_d}{V_{pp}}} \cdot \frac{1}{\sqrt{I_{ss}}} \\ &= a_v \xi \cdot \sqrt{\frac{kT}{N \cdot f_{ref} \cdot V_{pp}}} \cdot \sqrt{\frac{1}{I_{ss}}} \end{aligned} \quad (3-30)$$

The DLL multiplication frequency output is the combination of the clock edges defined by the VCDL, and so the DLL's output rms random jitter can be expressed as

$$\begin{aligned} \Delta t_{rj,DLL} &= \sqrt{\frac{\sum_{m=1}^N (\Delta t_{dm})^2}{N}} \\ &= \sqrt{\frac{\sum_{m=1}^N m \cdot (\Delta t_d)^2}{N}} \\ &= a_v \xi \cdot \sqrt{\frac{kT}{N \cdot f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_{ss}}} \cdot \sqrt{\frac{\frac{N}{2} \cdot (1+N)}{N}} \\ &= 2 \cdot \sqrt{\frac{1}{2} \cdot (1+N)} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}} \\ &= \sqrt{18} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}} \end{aligned} \quad (3-31)$$

where $I_{ss} = \frac{I_T}{N}$, $a_v \xi \cong 2$, $N=8$, I_T is the total tail current of delay cells in the VCDL.

DLL Noise Analysis

Unlike the PLL, the DLL output jitter can be minimized by reducing the normalized loop bandwidth (ε_{DLL}). This bandwidth reduction will not increase the accumulation factor of the DLL, which is defined as $\frac{2}{2 - \varepsilon_{DLL}}$. On the other hand, it will reduce the accumulation factor to one. Therefore, the jitter of the DLL does not accumulate from one cycle to another cycle of the reference clock. The clock edge after the output of the last tap will be refreshed by the low jitter reference frequency after each cycle of the reference clock.

3.5.2 DLL Deterministic Noise Analysis

The output frequency of the DLL (f_{out}) is defined by the clock edges, $\phi_1 - \phi_8$, which are generated by the delay cells in the VCDL. Therefore, any mismatch in the delay cell will generate a timing error at the output clock of the DLL. The mismatch effect is illustrated in Fig. 3.8.

Fig. 3.8: The Effect of Delay Cells Mismatch in DLL.

As shown in Fig. 3.8, the first delay cell in the VCDL is mismatched (denoted in grey) such that the delay of the delay cell is t'_D , and the other delay cells have a delay of t_D . Since the delay is defined as the period of the output clock, the period of the first output clock (T'_{out}) is different from the periods of the other output clocks (T_{out}) as shown in Fig. 3.8. The output clock will introduce a fixed timing offset from the ideal clock edge ($T'_{out} - T_{out}$) for every eight cycles of the output clock (or every period of the reference clock). Because each delay cell has a value that differs uniquely from

DLL Noise Analysis

the ideal delay value, a fix pattern jitter is introduced to the output clock. This jitter is called the deterministic jitter.

From [89], the delay mismatch can be described mathematically as follows:

$$d_i = [1 + e_i] \cdot d_{tune} \quad (3-32)$$

where d_i is the particular delay of delay cell i , d_{tune} is a nominal level of delay which is controlled by the VCDL's control voltage (V_c) and e_i is a random variable that describes the mismatch in the delay cell. The variable e_i is assumed to have a mean of zero and the mismatch in the delays associated with different cells is assumed to be uncorrelated. At a steady state, the total delay of the VCDL will be locked at one period of the reference clock (T_{ref}). From [89], the deterministic jitter variance of the m^{th} tap output of VCDL can be calculated as

$$\sigma_{\Delta t_m}^2 \cong T_{ref}^2 \cdot \frac{m(M-m)}{M^3} \cdot \sigma_{e_i}^2 \quad (3-33)$$

where $\sigma_{e_i}^2$ is the variance of e_i . Since the DLL multiplication frequency output is the combination of the clock edges defined by the VCDL, the DLL's output deterministic jitter arising from the delay cell can be expressed as follows:

$$\begin{aligned} \Delta t_{dj,DLL_DC} &= \sqrt{\frac{\sum_{m=1}^N \sigma_{\Delta t_m}^2}{N}} \\ &= \sqrt{\frac{\sum_{m=1}^N T_{ref}^2 \cdot \frac{m(M-m)}{M^3} \cdot \sigma_{e_i}^2}{N}} \\ &= \frac{T_{ref} \cdot \sigma_{e_i}}{N^2} \sqrt{\sum_{m=1}^N m(N-m)} \\ &= \frac{T_{ref} \cdot \sigma_{e_i}}{8^2} \sqrt{\sum_{m=1}^8 m(8-m)} \\ &= \frac{T_{ref} \cdot \sigma_{e_i}}{64} \sqrt{84} \\ &\cong \frac{0.14 \cdot \sigma_{e_i}}{f_{ref}} \end{aligned} \quad (3-34)$$

DLL Noise Analysis

where σ_{e_i} is the standard deviation of e_i and $N=M=8$.

As described in Chapter 3.3.2, the mismatch between the CP current source and the sink in the PLL will cause a static phase error to occur between the reference and feedback clocks. Since the DLL's output clock is defined using the VCDL's clock edges, any mismatch or phase error in the clock edge will cause a static timing error at the output clock. The timing error due to the CP mismatch is illustrated in Fig. 3.9.

Fig. 3.9: The Effect of CP Mismatch in DLL.

As can be seen in Fig. 3.9, it is clear that the static phase error between the ϕ_0 and ϕ_8 will generate a static timing error (t_{err}) on the output clock (V_{out}) for every eight cycles of the output clock. From equation (3-17),

$$t_{err} \cong \varepsilon \cdot t_{pw} \quad (3-35)$$

where ε is the normalized current mismatch of the charge pump current (I_{CP}) and t_{pw} is the minimum pulse width reset signal of the PFD.

DLL Noise Analysis

The DLL's output rms deterministic jitter due to CP mismatch can be expressed as follows:

$$\begin{aligned}
 \Delta t_{dj,DLL_CP} &= \sqrt{\frac{t_{err}^2}{N}} \\
 &= \sqrt{\frac{\varepsilon^2 \cdot t_{pw}^2}{N}} \\
 &= \frac{\varepsilon \cdot t_{pw}}{\sqrt{N}} \\
 &= \frac{\varepsilon \cdot t_{pw}}{\sqrt{8}}
 \end{aligned} \tag{3-36}$$

3.6 PLL and DLL Noise Comparison

The output jitter of the PLL and DLL-based frequency multiplier consists of two types of jitter. The first is random jitter which arises mainly from the delay cell circuit in the PLL and DLL, while the latter is deterministic jitter which comes from the mismatch of the circuits such as the ones in the CP current and delay cells. Because they are designed differently, each suffers differently from the effects of the various noise sources.

In the PLL, the timing of the output frequency is generated by a ring oscillator. The random timing error generated by the noise from the delay cells in a ring oscillator will determine the starting point of the next cycle. However, this error is very small and will not be corrected by the PFD in one cycle of the reference clock. Instead, it is reduced gradually over several cycles, depending on the dynamics of the PLL. Therefore, the timing error from one cycle to another are accumulated until the error is large enough to be corrected in the feedback loop as illustrated in Fig. 3.10. This maximum error is determined by the normalized loop bandwidth in the PLL. Meanwhile, the DLL's output frequency timing is generated from the clock edges defined in the VCDL, such that the timing error in the DLL will only accumulate from within the cycle of the reference clock. This is because the first clock edge of the each subsequent cycle will be triggered by the clean reference clock and no jitter accumulates from one cycle to another in the DLL [79].

PLL and DLL Noise Comparisons

PLL and DLL Noise Comparisons

TABLE 3-1: Random Jitter and Deterministic Jitter Equations of PLL and DLL.

PLL Based Frequency Multiplier	
Random Jitter	$\Delta t_{rj,PLL} \cong \alpha \cdot \sqrt{12} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}}$
Deterministic Jitter (CP current mismatch)	$\Delta t_{dj,PLL_CP} = K_{VCO} \cdot \frac{\varepsilon \cdot I_{CP} \cdot t_{pw}^2}{2 \cdot \sqrt{8} \cdot f_{out} \cdot C_2}$
DLL Based Frequency Multiplier	
Random Jitter	$\Delta t_{rj,DLL} = \sqrt{18} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}}$
Deterministic Jitter (CP current mismatch)	$\Delta t_{dj,DLL_CP} = \frac{\varepsilon \cdot t_{pw}}{\sqrt{8}}$
Deterministic Jitter (delay cells mismatch)	$\Delta t_{dj,DLL_DC} \cong \frac{0.14 \cdot \sigma_{ei}}{f_{ref}}$

The random and deterministic jitter equations of both the PLL and DLL architectures are summarized in Table 3-1. From the random jitter equations, it appears that the PLL jitter depends on accumulation factor (α), which in practice, has a minimum value of 1.37 as set by considerations of loop stability. This minimum accumulation factor only occurs when the noise contributed by the PFD, CP and divider ($\sigma_{\Delta t_{synth}}^2$) is small. In practice, the $\sigma_{\Delta t_{synth}}^2$ will be much larger than in the ideal situation because of the supply and substrate noise arising from the switching of digital circuits in the PFD, the CP and the divider. Thus the accumulation factor will

PLL and DLL Noise Comparisons

be much larger. Moreover, the supply and substrate noise of the PFD, CP and divider are not easy to predict and they make the optimum loop bandwidth hard to achieve, unless an external loop bandwidth is employed [11]. Meanwhile, the DLL does not suffer from the same level of noise accumulation as the PLL as it does not have the same optimized loop bandwidth. The DLL noise can be decreased by minimizing the loop bandwidth. In doing so, the noise contributed by the reference, PFD and CP will be minimized and the delay cells become the only noise contributors. Thus, it becomes clear that the DLL has a better random jitter performance than the PLL.

As demonstrated in Chapter 3.3.2, the mismatch of delay cells in the VCO will not contribute to the deterministic jitter at the PLL's output. The deterministic jitter is only contributed to by the mismatch in the CP current. From Table 3-1, the deterministic jitter of the DLL comes from both the mismatch in the CP and in the delay cells. Therefore, the PLL has better deterministic jitter in comparison to DLL.

However, the deterministic jitter is not a big impediment to the achievement of a low jitter frequency multiplier as the timing error is systematic and predictable such that it can be sensed and calibrated by applying a calibration circuit [98], [99]. Therefore, DLL is still a potential approach for low jitter frequency multiplier due to the better random jitter performance.

Chapter 4

Proposed Polyphase Filter Based Frequency Multiplier

4.1 Introduction

Chapter 3 describes the most commonly used PLL and DLL based frequency multipliers. Their random and deterministic noises are analyzed. Because no random jitter accumulates from one cycle to another in the DLL-based frequency multiplier, DLL becomes the more suitable circuit architecture with which to achieve a low jitter. Although the DLL is more sensitive to mismatches in the various devices, and it has a higher deterministic jitter than the PLL, the systematic error of its deterministic jitter can be predicted and calibrated with a calibration circuit. Unfortunately, the DLL's random jitter is not yet optimized. Random noise from the first to last delay cells in the VCDL will accumulate such that the random jitter arising from the last delay cell will be the largest. Furthermore, the delay cell consists of transistors, which will contribute flicker and thermal noise. A higher level of power consumption is needed to reduce the noise. A polyphase filter based frequency multiplier is thus proposed to alleviate the problem.

In the proposed architecture, the VCDL is replaced by a passive *RC* polyphase filter that generates the clock edges for frequency multiplication. The random noise contributed to the output jitter is reduced due to the passive *RC* circuit in the polyphase filter. Only the resistor contributes noise to the polyphase filter. The offset

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due to the polyphase filter mismatch will be calibrated by a proposed phase error calibration circuit.

This chapter begins with an introduction to the new polyphase filter based frequency multiplier. The proposed phase error calibration circuit will be described in detail before an analysis is presented of the random and deterministic noise associated with the proposed architecture. Finally, results of the noise analysis will be compared with that of the conventional DLL-based frequency multiplier.

4.2 Polyphase Filter Based Frequency Multiplier

Fundamentals

Fig. 4.1: Proposed Architecture of Polyphase Filter Based Frequency Multiplier.

Fig. 4.1 shows the architecture of the proposed frequency multiplier. It consists of a polyphase filter (PPF), eight units of voltage-controlled delay cells (VCDC), an edge combiner (EC) and a phase error calibration (PEC) unit.

Two passive stages of RC PPF [93], [94] are used as a clock phase generator circuit in this frequency multiplier as shown in Fig. 4.2. The four clock phases generated by the PPF are $Ph_1 = V_o \angle 0^\circ$, $Ph_2 = V_o \angle 90^\circ$, $Ph_3 = V_o \angle 180^\circ$ and $Ph_4 = V_o \angle 270^\circ$. Eight output clock edges can be generated using the differential of the clock phases. An illustration of the PPF output clock phases and eight differential clock phases is provided in Fig. 4.3.

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Fig. 4.2: Two Stages of Passive RC Polyphase Filter.

Fig. 4.3: Phasor Diagram of the PPF Output and Eight Differential Clock Phases.

The reference frequency of the frequency multiplier is generated by a crystal oscillator which is the source of a low jitter differential sine wave (X_{o1} and X_{o2}). From this differential sine wave, the PPF will generate four clock phases (Ph_1 to Ph_4) that are separated by 90° . Eight single-ended rail-to-rail clock edges (ϕ_0 to ϕ_7) will be generated for frequency multiplication purposes by applying the differential clock phases from the PPF to the VCDC. The VCDC is a differential amplifier with an active current mirror load. The functions of the VCDC are (i) to convert differential

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clock phases from PPF to single-ended rail-to-rail clock edges for the EC, and (ii) to provide delay variations for calibration purposes via the control voltage (V_{c1} to V_{c7}). Meanwhile, the V_{c0} is biased by a fixed reference voltage (V_{ref}) as the first clock edge (ϕ_0) is selected as the reference for calibration purposes. Finally, the eight clock edges from the VCDC will be combined by a digital EC to generate the multiplication frequency (f_{out}). However, the mismatch between the PPF and other devices will cause unequal phase spacing between adjacent clock edges. The static phase error will induce deterministic jitter at multiplication frequency (f_{out}). It is for these reasons that a PEC circuit is employed.

The clock edges which are defined by a passive RC PPF and VCDC serve to eliminate the use of a cascade structure in the delay chain. The jitter of the clock edges is only contributed by the VCDC and thermal noise from resistors in PPF. Since the VCDC provides the delay variation for calibration, the delay of the VCDC can be minimized just by covering the maximum phase error at the clock edges. Thus, the VCDC has better immunity against supply and substrate noise, and this helps to minimize the jitter of the clock edges. The deterministic jitter caused by static phase error is minimized by the PEC.

Fig. 4.4 shows the architecture of the PEC circuit which consists of a delay-to-voltage converter (DVC) and a comparator, which together act as a delay sensing circuit that measures the delay of the adjacent clock edges from the multiplication frequency (f_{out}). In addition, there are eight units of switched current sources and sinks (SCSS) that work to update the control voltages of the VCDC (V_{c1} to V_{c7}) and the calibration voltage of the comparator (V_{cal}).

Polyphase Filter Based Frequency Multiplier Fundamentals

Fig. 4.4: Architecture of the PEC Circuit.

Polyphase Filter Based Frequency Multiplier Fundamentals

Fig. 4.5: Operation Waveforms of the PEC Circuit.

The operation of the PEC circuit is illustrated in Fig. 4.5. The multiplication frequency (f_{out}) of the circuit consists of eight repeated clock edges (ϕ_{o0} to ϕ_{o7}), which are generated by the VCDC. The clock edge of f_{out} (ϕ_{o0}) will reset the D-flip-flop (DFF) before the clock edge with a delay of 4ns (ϕ'_{o0}) will clock the DFF, and the output data (Q) will go high. The clock edge of f_{out} (ϕ_{o1}) will then reset the DFF again and the signal Q will go low. t_{Q0} is the pulse width of Q that represents the delay between ϕ'_{o0} and ϕ_{o1} . Different clock phase pairs have their respective pulse widths and the pulse signal Q will switch on the current source (I_c) to charge the C_{c1} . The output of the DVC (V_T) will thus be charged to a voltage level (V_{Tpeak0}) that is proportional to t_{Q0} , and that can be expressed as

$$V_{Tpeak0} = \left(\frac{I_c}{C_{c1}} \right) \times t_{Q0} \quad (4-1)$$

Polyphase Filter Based Frequency Multiplier Fundamentals

By inserting a 4ns delay chain, the delay between ϕ'_{o0} and ϕ_{o1} can be reduced from 5ns to 1ns and t_{Q0} will be 5 times reduced. Since the mean value of V_{Tpeak0} is designed to be approximately 1V, reducing the t_{Q0} permits more headroom to boost the I_c/C_{c1} and sensitivity of the DVC.

The delay information is translated to the voltage domain and this voltage level is compared with a calibration voltage (V_{cal}) that occurs when the clock signal of the comparator (CK_{comp}) is high. If the delay of ϕ'_{o0} and ϕ_{o1} are shorter, the t_{Q0} becomes smaller. As V_{Tpeak0} becomes lower than V_{cal} , the negative output of the comparator will generate a pulse signal (UP), while the signal DN remains low. The UP signal will then switch on the current source of the SCSS to charge the capacitor in the VCDC, hence increasing the V_{c1} to increase the delay of the VCDC. Following this, the signal V_T is reset to zero by V_{Trst} before the delay sensing operation's next cycle. This operation will continue until the clock edge reaches ϕ'_{o6} and ϕ_{o7} . Since all delays are calibrated according to an arbitrarily selected calibration voltage (V_{cal}), all clock edges (ϕ_{o1} to ϕ_{o7}) have the same delay. However, the delay of the last clock edge (ϕ_{o7}) and the first clock edge of next cycle (ϕ_{o0}^*) are different from the others. To space all the clock edges equally, V_{cal} will be updated according to the delay sensed from clock edge ϕ_{o7} and ϕ_{o0}^* . If the V_{cal} is higher than the targeted V_{cal} , the delay of each adjacent clock edge from ϕ_{o0} to ϕ_{o7} will be higher than 5ns, while the delay of clock edge ϕ_{o7} and ϕ_{o0}^* will be smaller than 5ns. Therefore, the V_{Tpeak7} of this stage will be smaller than V_{cal} . By reversing the UP and DN signal, the UP signal generated by the comparator will switch on the current sink of the SCSS to discharge C_{c2} , hence decreasing the V_{cal} . This negative feedback operation will cause all clock edges (ϕ_{o0} to ϕ_{o0}^*) to be spaced equally and this operation is synchronized by a reset signal from

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ϕ_7 .

The PEC is a continuously calibration loop that contributes noise to the frequency multiplier. However, the bang-bang feedback loop of the PEC allows the level of noise contributed to be minimized by reducing the current source and sink in the SCSS [95]. At the initial stage, the current source and sink in the SCSS is set at $250\mu\text{A}$ in order to reduce the settling time. When a steady state is achieved, the current will be reduced to $1\mu\text{A}$ to minimize the noise contribution of the PEC.

The advantage of this PEC is that only one delay sensing circuit is used to measure the mismatch of the clock edge. Any mismatch caused by the current source I_c , capacitor C_{cl} and the offset of the comparator will be reflected equally every time a delay is sensed at the clock edges. The calibration only involves a delay comparison, therefore the mismatch and offset will cancel each other out. The calibration incorporates the output of the frequency multiplier, such that any mismatch in the EC circuit and the routing from the VCDC to EC will be detected and calibrated.

4.3 Noise Analysis

4.3.1 Random Noise Analysis

In this analysis, we emphasize the important role played by the random jitter of the clock edges' generation circuit. The PPF replaces the delay chain which is the dominant noise source in a conventional DLL. The noise source of the VCDC and EC are first ignored in this analysis in order to simplify the comparison between the clock edge generation circuits of the two types of frequency multipliers.

Fig. 4.6 shows the two-stage RC PPF. This PPF consists of eight resistors and eight capacitors. Resistors R_A to R_D have the same value, denoted by R_1 . Resistors R_E to R_H also have the same value, denoted by R_2 . The input signals from the crystals X_{o1} and X_{o2} are V_i and $-V_i$ respectively. For the purposes of this analysis, it is assumed that the X_{o1} and X_{o2} are 180° out of phase.

Fig. 4.6: Two-stage RC Polyphase Filter.

Resistors are the only noise sources in the PPF. Because the clock phases of the frequency multiplier are defined by the differential output of the PPF, it becomes

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necessary to determine the differential output noise contributed by the resistors. Fig. 4.7 shows a simplified version of the PPF circuit with a noise source of R_E (V_{RE}) that is suitable for Kirchoff's Law analysis.

Fig. 4.7: Simplified Circuit for PPF with Noise Source of Resistor R_E .

From Fig. 4.7, by applying Kirchoff's Voltage Law on loop 1, one can obtain

$$\begin{aligned} -V_{RE} + I_1(Z_2) + I_3(Z_2) + I_5(Z_2) + I_3(Z_2) &= 0 \\ I_1(Z_2) + I_2(0) + I_3(2 \cdot Z_2) + I_4(0) + I_5(Z_2) &= V_{RE} \end{aligned} \quad (4-2)$$

By applying Kirchoff's Voltage Law on loop 2, one can obtain

$$\begin{aligned} I_2(-Z_1) + I_1(-Z_2) + V_{RE} + I_2(-Z_1) &= 0 \\ I_1(-Z_2) + I_2(-2 \cdot Z_1) + I_3(0) + I_4(0) + I_5(0) &= -V_{RE} \end{aligned} \quad (4-3)$$

Noise Analysis

By applying Kirchoff's Voltage Law on loop 3, one can obtain

$$\begin{aligned} I_2(Z_1) + I_4(-Z_1) + I_3(-Z_2) &= 0 \\ I_1(0) + I_2(Z_1) + I_3(-Z_2) + I_4(-Z_1) + I_5(0) &= 0 \end{aligned} \quad (4-4)$$

By applying Kirchoff's Current Law on node A, this gives

$$\begin{aligned} I_1 &= I_2 + I_3 \\ I_1(1) + I_2(-1) + I_3(-1) + I_4(0) + I_5(0) &= 0 \end{aligned} \quad (4-5)$$

By applying Kirchoff's Current Law on node B, this gives

$$\begin{aligned} I_3 &= I_4 + I_5 \\ I_1(0) + I_2(0) + I_3(1) + I_4(-1) + I_5(-1) &= 0 \end{aligned} \quad (4-6)$$

The following is the matrix solution for the above equations:

$$\begin{bmatrix} Z_2 & 0 & 2 \cdot Z_2 & 0 & Z_2 \\ -Z_2 & -2 \cdot Z_2 & 0 & 0 & 0 \\ 0 & Z_1 & -Z_2 & Z_1 & 0 \\ 1 & -1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 & -1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} V_{RE} \\ -V_{RE} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} Z_2 & 0 & 2 \cdot Z_2 & 0 & Z_2 \\ -Z_2 & -2 \cdot Z_2 & 0 & 0 & 0 \\ 0 & Z_1 & -Z_2 & Z_1 & 0 \\ 1 & -1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 & -1 \end{bmatrix}^{-1} \begin{bmatrix} V_{RE} \\ -V_{RE} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4-7)$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} \frac{(2 \cdot Z_1^2 + 4 \cdot Z_1 \cdot Z_2 + Z_2^2)}{Z_2 \cdot (2 \cdot Z_1 + Z_2) \cdot (4 \cdot Z_1 + Z_2)} \cdot V_{RE} \\ \frac{(3 \cdot Z_1 + Z_2)}{(2 \cdot Z_1 + Z_2) \cdot (4 \cdot Z_1 + Z_2)} \cdot V_{RE} \\ \frac{Z_1}{Z_2 \cdot (4 \cdot Z_1 + Z_2)} \cdot V_{RE} \\ \frac{Z_1}{(2 \cdot Z_1 + Z_2) \cdot (4 \cdot Z_1 + Z_2)} \cdot V_{RE} \\ \frac{2 \cdot Z_1^2}{Z_2 \cdot (2 \cdot Z_1 + Z_2) \cdot (4 \cdot Z_1 + Z_2)} \cdot V_{RE} \end{bmatrix}$$

Noise Analysis

According to the design parameters in Chapter 5.3, $R_1 = R$, $R_2 = \frac{3}{2} \cdot R$ and

$C_1 = C_2 = C$. Further, $Z_1 = \frac{1}{\frac{1}{R} + s \cdot C}$ and $Z_2 = \frac{3}{2} \cdot R + \frac{1}{s \cdot C}$. Therefore, the transfer

function from the noise source of resistor R_E (V_{RE}) to the differential clock phase output Ph_1-Ph_2 ($V_{Ph1-Ph2}$) is given as follows:

$$\begin{aligned}
 tf_{RE} &= \frac{V_{Ph1-Ph2}}{V_{RE}} \\
 &= \frac{V_{Ph1} - V_{Ph2}}{V_{RE}} \\
 &= \frac{\left[I_1 \cdot \left(\frac{1}{s \cdot C_2} \right) + I_2 \cdot Z_1 \right] - \left[I_3 \cdot \left(\frac{1}{s \cdot C_2} \right) - I_2 \cdot Z_1 \right]}{V_{RE}} \\
 &= \frac{(3 \cdot Z_1 + Z_2) \cdot (2 \cdot s \cdot C_2 \cdot Z_1 + 1)}{s \cdot C_2 \cdot (2 \cdot Z_1 + Z_2) \cdot (4 \cdot Z_1 + Z_2)} \\
 &= \frac{2 \cdot (3sRC + 1) \cdot (3s^2 R^2 C^2 + 11sRC + 2)}{(3s^2 R^2 C^2 + 13sRC + 2) \cdot (3s^2 R^2 C^2 + 9sRC + 2)}
 \end{aligned} \tag{4-8}$$

The magnitude square of the transfer function ($|tf_{RE}|^2$) is

$$\begin{aligned}
 |tf_{RE}|^2 &= \frac{|2|^2 \cdot |1 + j(3wRC)|^2 \cdot |(2 - 3w^2 R^2 C^2) + j(11wRC)|^2}{|(2 - 3w^2 R^2 C^2) + j(13wRC)|^2 \cdot |(2 - 3w^2 R^2 C^2) + j(9wRC)|^2} \\
 &= \frac{4 \cdot [1 + (3wRC)^2] \cdot [(2 - 3w^2 R^2 C^2)^2 + (11wRC)^2]}{[(2 - 3w^2 R^2 C^2)^2 + (13wRC)^2] \cdot [(2 - 3w^2 R^2 C^2)^2 + (9wRC)^2]} \\
 &= \frac{4 \cdot [1 + (3 \cdot 2\pi f RC)^2] \cdot [(2 - 3 \cdot 2^2 \pi^2 f^2 R^2 C^2)^2 + (11 \cdot 2\pi f RC)^2]}{[(2 - 3 \cdot 2^2 \pi^2 f^2 R^2 C^2)^2 + (13 \cdot 2\pi f RC)^2] \cdot [(2 - 3 \cdot 2^2 \pi^2 f^2 R^2 C^2)^2 + (9 \cdot 2\pi f RC)^2]}
 \end{aligned} \tag{4-9}$$

Noise Analysis

The integral from 0 to infinity of the magnitude square of the transfer function gives the following computation

$$\begin{aligned}
 & \int_0^{\infty} \frac{4 \cdot [1 + (3 \cdot 2\pi f RC)^2] \cdot [(2 - 3 \cdot 2^2 \pi^2 f^2 R^2 C^2)^2 + (11 \cdot 2\pi f RC)^2]}{[(2 - 3 \cdot 2^2 \pi^2 f^2 R^2 C^2)^2 + (13 \cdot 2\pi f RC)^2] \cdot [(2 - 3 \cdot 2^2 \pi^2 f^2 R^2 C^2)^2 + (9 \cdot 2\pi f RC)^2]} df \\
 &= \left[\frac{558\sqrt{290}}{4147\pi RC(157 + 13\sqrt{145})^{\frac{3}{2}}} \cdot a \tan \left[\frac{6\sqrt{2}\pi f RC}{(157 + 13\sqrt{145})^{\frac{1}{2}}} \right] \right. \\
 &+ \frac{18\sqrt{2}}{11\pi RC(157 + 13\sqrt{145})^{\frac{3}{2}}} \cdot a \tan \left[\frac{6\sqrt{2}\pi f RC}{(157 + 13\sqrt{145})^{\frac{1}{2}}} \right] \\
 &+ \frac{31968\sqrt{145}}{\pi RC \cdot 377(-157 + 13\sqrt{145})(314 - 26\sqrt{145})^{\frac{1}{2}}} \cdot a \tan \left[\frac{12\pi f RC}{(314 - 26\sqrt{145})^{\frac{1}{2}}} \right] \\
 &- \frac{11232}{\pi RC \cdot 11(-157 + 13\sqrt{145})(314 - 26\sqrt{145})^{\frac{1}{2}}} \cdot a \tan \left[\frac{12\pi f RC}{(314 - 26\sqrt{145})^{\frac{1}{2}}} \right] \\
 &+ \frac{5\sqrt{6}}{11\pi RC(23 + 3\sqrt{57})^{\frac{1}{2}}} \cdot a \tan \left[\frac{2\sqrt{6}\pi f RC}{(23 + 3\sqrt{57})^{\frac{1}{2}}} \right] \\
 &+ \frac{335\sqrt{342}}{5643\pi RC(23 + 3\sqrt{57})^{\frac{1}{2}}} \cdot a \tan \left[\frac{2\sqrt{6}\pi f RC}{(23 + 3\sqrt{57})^{\frac{1}{2}}} \right] \\
 &- \frac{670\sqrt{57}}{1881\pi RC(138 - 18\sqrt{57})^{\frac{1}{2}}} \cdot a \tan \left[\frac{12\pi f RC}{(138 - 18\sqrt{57})^{\frac{1}{2}}} \right] \\
 &\left. + \frac{30}{11\pi R^3 C^3(138 - 18\sqrt{57})^{\frac{1}{2}}} \cdot a \tan \left[\frac{12\pi f RC}{(138 - 18\sqrt{57})^{\frac{1}{2}}} \right] \right]_0^{\infty}
 \end{aligned}$$

Noise Analysis

$$\begin{aligned}
&= \frac{558\sqrt{290}}{4147\pi RC(157+13\sqrt{145})^{\frac{3}{2}}} \cdot \frac{\pi}{2} + \frac{18\sqrt{2}}{11\pi RC(157+13\sqrt{145})^{\frac{3}{2}}} \cdot \frac{\pi}{2} \\
&+ \frac{31968\sqrt{145}}{\pi RC \cdot 377(-157+13\sqrt{145})(314-26\sqrt{145})^{\frac{1}{2}}} \cdot \frac{\pi}{2} \\
&- \frac{11232}{\pi RC \cdot 11(-157+13\sqrt{145})(314-26\sqrt{145})^{\frac{1}{2}}} \cdot \frac{\pi}{2} + \frac{5\sqrt{6}}{11\pi RC(23+3\sqrt{57})^{\frac{1}{2}}} \cdot \frac{\pi}{2} \\
&+ \frac{335\sqrt{342}}{5643\pi RC(23+3\sqrt{57})^{\frac{1}{2}}} \cdot \frac{\pi}{2} - \frac{670\sqrt{57}}{1881\pi RC(138-18\sqrt{57})^{\frac{1}{2}}} \cdot \frac{\pi}{2} \\
&+ \frac{30}{11\pi R^3 C^3(138-18\sqrt{57})^{\frac{1}{2}}} \cdot \frac{\pi}{2} \\
&= \frac{833}{2574RC}
\end{aligned}
\tag{4-10}$$

Finally, the differential clock phase output noise contributed by resistor R_E is derived as follows

$$\begin{aligned}
V_{NRE} &= \sqrt{4kTR_2 \left(\frac{833}{2574RC} \right)} \\
&= \sqrt{4kT \frac{3}{2} R \left(\frac{833}{2574RC} \right)}
\end{aligned}
\tag{4-11}$$

The same method can be used to find the differential clock phase output contributed by the remaining resistors. Table 4-1 provides a summary of the contributions of all resistors in the PPF.

Noise Analysis

TABLE 4-1: Summary of Resistors Noise Contributions in the PPF.

Noise Source	Differential Clock Phase Output Noise
R_A	$V_{NRA} = \sqrt{4kTR\left(\frac{595}{5148RC}\right)}$
R_B	$V_{NRB} = \sqrt{4kTR\left(\frac{61}{1287RC}\right)}$
R_C	$V_{NRC} = \sqrt{4kTR\left(\frac{5}{2574RC}\right)}$
R_D	$V_{NRD} = \sqrt{4kTR\left(\frac{361}{5148RC}\right)}$
R_E	$V_{NRE} = \sqrt{4kT\frac{3}{2}R\left(\frac{833}{2574RC}\right)}$
R_F	$V_{NRF} = \sqrt{4kT\frac{3}{2}R\left(\frac{1225}{7722RC}\right)}$
R_G	$V_{NRG} = \sqrt{4kT\frac{3}{2}R\left(\frac{7}{1287RC}\right)}$
R_H	$V_{NRH} = \sqrt{4kT\frac{3}{2}R\left(\frac{86}{3861RC}\right)}$

Noise Analysis

From Table 4-1, the differential clock phase output noise (V_N) contributed by all the resistors can be calculated as follows:

$$\begin{aligned}
 V_N &= \sqrt{V_{NRA}^2 + V_{NRB}^2 + V_{NRC}^2 + V_{NRD}^2 + V_{NRE}^2 + V_{NRF}^2 + V_{NRG}^2 + V_{NRH}^2} \\
 &= \sqrt{4kTR \left[\frac{595}{5148RC} + \frac{61}{1287RC} + \frac{5}{2574RC} + \frac{361}{5148RC} + \frac{3}{2} \left(\frac{833}{2574RC} \right) + \frac{3}{2} \left(\frac{1225}{7722RC} \right) + \right.} \\
 &\quad \left. \frac{3}{2} \left(\frac{7}{1287RC} \right) + \frac{3}{2} \left(\frac{86}{3861RC} \right) \right] } \\
 &= 2 \cdot \sqrt{\frac{kT}{C}}
 \end{aligned} \tag{4-12}$$

To verify the accuracy of equation (4-12), a noise simulation is performed on the PPF illustrated in Fig. 4.6 using a Cadence Spectre simulator. Ideal resistors and capacitors are used in the simulation. $R_1 = R$ and $R_2 = \frac{3}{2} \cdot R$ are used in the simulation, where R is an arbitrary value. Meanwhile, $C_1 = C_2 = C$ is also used such that C changes from 0.5pF to 10pF by increments of 0.5pF. The PPF's differential integrated output noise is plotted against its capacitance and both the simulated and predicted results derived from equation (4-12) are shown in Fig. 4.8. From the figure, it appears that the simulation results totally match that of equation (4-12), such that the PPF of the differential integrated output noise is inversely proportional to $\sqrt{C}$. Different R values are used in the simulation, but it is found that the PPF of the differential integrated output noise is independent of the R value.

Fig. 4.8: Simulation and Prediction Results of PPF Differential Integrated Output Noise versus Capacitance.

After calculating the output noise arising from the differential clock phase, we seek to determine the amplitude of the PPF output. Fig. 4.9 shows a simplified version of the PPF circuit with a complementary single-ended input signal of V_i .

Fig. 4.9: Simplified Circuit of PPF with Input Signal.

From Fig. 4.9, by applying Kirchoff's Voltage Law on loop 1, one can obtain

$$\begin{aligned} -V_i + I_1(Z_1) + I_2(Z_2) + I_4\left(-\frac{1}{s \cdot C_1}\right) + V_i &= 0 \\ I_1(Z_1) + I_2(Z_2) + I_3(0) + I_4\left(-\frac{1}{s \cdot C_1}\right) + I_5(0) &= 0 \end{aligned} \quad (4-13)$$

By applying Kirchoff's Voltage Law on loop 2, one can obtain

$$\begin{aligned} V_i + I_4\left(-\frac{1}{s \cdot C_1}\right) + I_3(-Z_2) + I_1(-Z_1) + V_i &= 0 \\ I_1(Z_1) + I_2(0) + I_3(Z_2) + I_4\left(\frac{1}{s \cdot C_1}\right) + I_5(0) &= 2 \cdot V_i \end{aligned} \quad (4-14)$$

By applying Kirchoff's Voltage Law on loop 3, one can obtain

$$\begin{aligned} -V_i + I_5(R_1) + I_4\left(\frac{1}{s \cdot C_1}\right) + -V_i &= 0 \\ I_1(0) + I_2(0) + I_3(0) + I_4\left(\frac{1}{s \cdot C_1}\right) + I_5(R_1) &= 2 \cdot V_i \end{aligned} \quad (4-15)$$

By applying Kirchoff's Current Law on node A, one can obtain

$$\begin{aligned} I_1 &= I_2 + I_3 \\ I_1(1) + I_2(-1) + I_3(-1) + I_4(0) + I_5(0) &= 0 \end{aligned} \quad (4-16)$$

By applying Kirchoff's Current Law on node B, one can obtain

$$\begin{aligned} I_3 + I_5 &= I_2 + I_4 \\ I_1(0) + I_2(1) + I_3(-1) + I_4(1) + I_5(-1) &= 0 \end{aligned} \quad (4-17)$$

Noise Analysis

Below is the matrix solution for the above equations:

$$\begin{bmatrix} Z_1 & Z_2 & 0 & -\frac{1}{s \cdot C_1} & 0 \\ Z_1 & 0 & Z_2 & \frac{1}{s \cdot C_1} & 0 \\ 0 & 0 & 0 & \frac{1}{s \cdot C_1} & R_1 \\ 1 & -1 & -1 & 0 & 0 \\ 0 & 1 & -1 & 1 & -1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} 0 \\ 2 \cdot V_i \\ 2 \cdot V_i \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} Z_1 & Z_2 & 0 & -\frac{1}{s \cdot C_1} & 0 \\ Z_1 & 0 & Z_2 & \frac{1}{s \cdot C_1} & 0 \\ 0 & 0 & 0 & \frac{1}{s \cdot C_1} & R_1 \\ 1 & -1 & -1 & 0 & 0 \\ 0 & 1 & -1 & 1 & -1 \end{bmatrix}^{-1} \begin{bmatrix} V_{RE} \\ -V_{RE} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4-18)$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} \frac{2}{(2 \cdot Z_1 + Z_2)} \cdot V_i \\ \frac{-2 \cdot (-Z_1 + Z_1 \cdot s \cdot R_1 \cdot C_1 - R_1 - Z_2)}{(2 \cdot Z_1 + Z_2) \cdot (Z_2 + Z_2 \cdot s \cdot R_1 \cdot C_1 + 2 \cdot R_1)} \cdot V_i \\ \frac{2 \cdot (-Z_1 + Z_1 \cdot s \cdot R_1 \cdot C_1 + Z_2 \cdot s \cdot R_1 \cdot C_1 + R_1)}{(2 \cdot Z_1 + Z_2) \cdot (Z_2 + Z_2 \cdot s \cdot R_1 \cdot C_1 + 2 \cdot R_1)} \cdot V_i \\ \frac{2 \cdot s \cdot C_1 \cdot (R_1 + Z_2)}{(Z_2 + Z_2 \cdot s \cdot R_1 \cdot C_1 + 2 \cdot R_1)} \cdot V_i \\ \frac{2 \cdot (1 + Z_2 \cdot s \cdot C_1)}{(Z_2 + Z_2 \cdot s \cdot R_1 \cdot C_1 + 2 \cdot R_1)} \cdot V_i \end{bmatrix}$$

Noise Analysis

The transfer function from the PPF's single-ended input (V_i) to the single ended output at $Ph_I (V_o)$ can be derived as follows:

$$\begin{aligned}
 tf_{vo} &= \frac{V_o}{V_i} \\
 &= \frac{I_2 \cdot \left(\frac{1}{s \cdot C_2} \right) + I_1 \cdot Z_1 - V_i}{V_i} \\
 &= \frac{-[s^2 R_1 C_1 R_2 C_2 + s(R_1 C_1 + R_2 C_2) - 1]}{[s^2 R_1 C_1 R_2 C_2 + s(R_1 C_1 + R_2 C_2 + 2R_1 C_2) + 1]}
 \end{aligned} \tag{4-19}$$

The single-ended output peak amplitude can be expressed as

$$\begin{aligned}
 |V_o| &= |V_i| \cdot |tf_{vo}| \\
 &= |V_i| \cdot \left| \frac{[s^2 R_1 C_1 R_2 C_2 + s(R_1 C_1 + R_2 C_2) - 1]}{[s^2 R_1 C_1 R_2 C_2 + s(R_1 C_1 + R_2 C_2 + 2R_1 C_2) + 1]} \right| \\
 &= |V_i| \cdot \frac{|(-1 - w^2 R_1 C_1 R_2 C_2) + jw(R_1 C_1 + R_2 C_2)|}{|(1 - w^2 R_1 C_1 R_2 C_2) + jw(R_1 C_1 + R_2 C_2 + 2R_1 C_2)|} \\
 &= |V_i| \cdot \frac{\sqrt{(-1 - w^2 R_1 C_1 R_2 C_2)^2 + w^2 (R_1 C_1 + R_2 C_2)^2}}{\sqrt{(1 - w^2 R_1 C_1 R_2 C_2)^2 + w^2 (R_1 C_1 + R_2 C_2 + 2R_1 C_2)^2}}
 \end{aligned} \tag{4-20}$$

Noise Analysis

To simplify the analysis, it is assumed that $w_i R_1 C_1 \cong w_i R_2 C_2 \cong I$, where $|V_i|$ and w_i are the input peak amplitude and the input frequency respectively. The approximation will vary from the actual results by less than 10%. When $w=w_i$, the results can be simplified such that

$$\begin{aligned}
 |V_o| &\cong |V_i| \cdot \frac{\sqrt{(-1 - w^2 R_1 C_1 R_2 C_2)^2 + w^2 (R_1 C_1 + R_2 C_2)^2}}{\sqrt{(1 - w^2 R_1 C_1 R_2 C_2)^2 + w^2 (R_1 C_1 + R_2 C_2 + 2R_1 C_2)^2}} \\
 &\cong |V_i| \cdot \frac{\sqrt{(-1 - w_i^2 R_1 C_1 R_2 C_2)^2 + w_i^2 (R_1 C_1 + R_2 C_2)^2}}{\sqrt{(1 - w_i^2 R_1 C_1 R_2 C_2)^2 + w_i^2 (R_1 C_1 + R_2 C_2 + 2R_1 C_2)^2}} \quad (4-21) \\
 &\cong |V_i| \cdot \frac{\sqrt{(-1-1)^2 + (1+1)^2}}{\sqrt{(1-1)^2 + (1+1+2)^2}} \\
 &\cong \frac{|V_i|}{\sqrt{2}}
 \end{aligned}$$

Noise Analysis

From Fig. 4.3, it is clear that the peak amplitude of the first (Ph_1 - Ph_2) and second (Ph_4 - Ph_2) differential clock phases are $\sqrt{2} \cdot |V_o|$ and $2 \cdot |V_o|$ respectively. Therefore, the slew rate of the first differential clock phase (SR_1) and second differential clock phase (SR_2) can be obtained as follows:

$$\begin{aligned} SR_1 &= w_i \cdot \sqrt{2} \cdot |V_o| \\ &= w_i \cdot |V_i| \end{aligned} \quad (4-22)$$

$$\begin{aligned} SR_2 &= w_i \cdot 2 \cdot |V_o| \\ &= w_i \cdot \sqrt{2} \cdot |V_i| \end{aligned} \quad (4-23)$$

At this juncture, the input current passing through the PPF (I_i) equals the total current driven by the three V_i sources illustrated in Fig. 4.9. It can be shown that

$$\begin{aligned} I_i &= I_1 + I_4 + I_5 \\ &= \frac{2}{(2 \cdot Z_1 + Z_2)} \cdot V_i + \frac{2 \cdot s \cdot C_1 \cdot (R_1 + Z_2)}{(Z_2 + Z_2 \cdot s \cdot R_1 \cdot C_1 + 2 \cdot R_1)} \cdot V_i + \frac{2 \cdot (1 + Z_2 \cdot s \cdot C_1)}{(Z_2 + Z_2 \cdot s \cdot R_1 \cdot C_1 + 2 \cdot R_1)} \cdot V_i \\ &= \frac{4V_i[s^2(R_1C_1C_2 + R_2C_1C_2) + s(C_1 + C_2)]}{s^2(R_1C_1R_2C_2) + s(R_1C_1 + R_2C_2 + 2R_1C_2) + 1} \end{aligned} \quad (4-24)$$

Therefore, the input current peak amplitude ($|I_i|$) can be expressed as

$$\begin{aligned} |I_i| &= \frac{4 \cdot |V_i| \cdot [s^2(R_1C_1C_2 + R_2C_1C_2) + s(C_1 + C_2)]}{|s^2(R_1C_1R_2C_2) + s(R_1C_1 + R_2C_2 + 2R_1C_2) + 1|} \\ &= \frac{4 \cdot |V_i| \cdot [-w^2(R_1C_1C_2 + R_2C_1C_2) + jw(C_1 + C_2)]}{|[1 - w^2(R_1C_1R_2C_2)] + jw(R_1C_1 + R_2C_2 + 2R_1C_2)|} \\ &= \frac{4 \cdot |V_i| \cdot \sqrt{w^4(R_1C_1C_2 + R_2C_1C_2)^2 + w^2(C_1 + C_2)^2}}{\sqrt{[1 - w^2(R_1C_1R_2C_2)]^2 + w^2(R_1C_1 + R_2C_2 + 2R_1C_2)^2}} \end{aligned} \quad (4-25)$$

Noise Analysis

To simplify the analysis, it is assumed that $w_i R_1 C_1 \cong w_i R_2 C_2 \cong 1$ and $C_1 = C_2 = C$. The approximation will vary from the actual results by less than 10%. When $w = w_i$, the results can be simplified such that

$$\begin{aligned}
 |I_i| &\cong \frac{4 \cdot |V_i| \cdot \sqrt{w^4 (R_1 C_1 C_2 + R_2 C_1 C_2)^2 + w^2 (C_1 + C_2)^2}}{\sqrt{[1 - w^2 (R_1 C_1 R_2 C_2)]^2 + w^2 (R_1 C_1 + R_2 C_2 + 2 R_1 C_2)^2}} \\
 &\cong \frac{4 \cdot |V_i| \cdot \sqrt{(w_i R_1 C_1 \cdot w_i C_2 + w_i R_2 C_2 \cdot w_i C_1)^2 + (w_i C_1 + w_i C_2)^2}}{\sqrt{[1 - (w_i R_1 C_1 \cdot w_i R_2 C_2)]^2 + (w_i R_1 C_1 + w_i R_2 C_2 + 2 w_i R_1 C_2)^2}} \quad (4-26) \\
 &\cong \frac{4 \cdot |V_i| \cdot \sqrt{2(w_i C + w_i C)^2}}{\sqrt{(1+1+2)^2}} \\
 &\cong 2 \cdot \sqrt{2} \cdot w_i \cdot C \cdot |V_i|
 \end{aligned}$$

Since the input of the PPF is a sinusoidal waveform from a crystal oscillator, and the PPF is a passive circuit, the current passing through the PPF is sinusoidal too. The current of the PPF is provided from a push-pull inverter in the crystal oscillator. Therefore the current consumption of the PPF (I_{rms}) is set at the rms value of the I_i , and can be obtained as follows

$$\begin{aligned}
 I_{rms} &= \frac{|I_i|}{\sqrt{2}} \\
 &= 2 \cdot w_i \cdot C \cdot |V_i|
 \end{aligned} \quad (4-27)$$

Noise Analysis

Taking into account (4-12), (4-22) and (4-27), the jitter of first and second differential clock phase (Δt_{p1} and Δt_{p2}) can be calculated as follows:

$$\begin{aligned}
 \Delta t_{p1} &= \frac{V_N}{SR_1} \\
 &= \frac{2 \cdot \sqrt{\frac{kT}{C}}}{w_i \cdot |V_i|} \\
 &= \frac{2 \cdot \sqrt{\frac{kT \cdot 2 \cdot w_i \cdot |V_i|}{I_{rms}}}}{w_i \cdot |V_i|} \\
 &= 2 \cdot \sqrt{\frac{2kT}{w_i \cdot |V_i| \cdot I_{rms}}} \\
 &= 2 \cdot \sqrt{\frac{2kT}{2\pi f_i \cdot \frac{|V_i|_{pp}}{2} \cdot I_{rms}}} \\
 &= 2 \cdot \sqrt{\frac{2kT}{\pi f_i \cdot |V_i|_{pp}}} \cdot \frac{1}{\sqrt{I_{rms}}}
 \end{aligned} \tag{4-28}$$

$$\begin{aligned}
 \Delta t_{p2} &= \frac{V_N}{SR_2} \\
 &= \frac{2 \cdot \sqrt{\frac{kT}{C}}}{\sqrt{2} \cdot w_i \cdot |V_i|} \\
 &= \frac{\sqrt{2} \cdot \sqrt{\frac{kT}{C}}}{w_i \cdot |V_i|} \\
 &= \sqrt{2} \cdot \sqrt{\frac{2kT}{\pi f_i \cdot |V_i|_{pp}}} \cdot \frac{1}{\sqrt{I_{rms}}}
 \end{aligned} \tag{4-29}$$

where $|V_i| = \frac{|V_i|_{pp}}{2}$, and $|V_i|$ and $|V_i|_{pp}$ are the input signal peak amplitude and the peak-to-peak amplitudes respectively.

Noise Analysis

The 1st, 3rd, 5th and 7th differential clock phase outputs illustrated in Fig 4.3 have the same amplitude. Therefore, the jitter can be denoted as Δt_{p1} and the remaining differential clock phase's output jitter can be denoted as Δt_{p2} . The random jitter ($\Delta t_{rj,PPF}$) of the PPF-based frequency multiplier output that is contributed by the eight differential clock phases can be calculated as follows:

$$\begin{aligned}
 \Delta t_{rj,PPF} &= \sqrt{\frac{(\Delta t_{p1})^2 + (\Delta t_{p2})^2 + (\Delta t_{p1})^2 + (\Delta t_{p2})^2 + (\Delta t_{p1})^2 + (\Delta t_{p2})^2 + (\Delta t_{p1})^2 + (\Delta t_{p2})^2}{8}} \\
 &= \sqrt{\frac{2kT}{\pi f_i |V_i|_{pp}}} \cdot \frac{1}{\sqrt{I_{rms}}} \cdot \sqrt{\frac{2^2 + (\sqrt{2})^2 + 2^2 + (\sqrt{2})^2 + 2^2 + (\sqrt{2})^2 + 2^2 + (\sqrt{2})^2}{8}} \\
 &= \sqrt{\frac{6}{\pi}} \cdot \sqrt{\frac{kT}{f_i |V_i|_{pp}}} \cdot \frac{1}{\sqrt{I_{rms}}}
 \end{aligned}
 \tag{4-30}$$

4.3.2 Deterministic Noise Analysis

A PEC circuit is introduced to calibrate the systematic mismatch in the clock edges and to reduce the deterministic jitter arising from the polyphase filter. The proposed PEC circuit is only one delay sensing circuit being used to measure the delay mismatch of every clock edge at the frequency multiplier output. The mismatch in each of the clock edges is measured at different times in this design, and only one clock edge delay mismatch is measured in every period of the frequency multiplier output. Therefore, eight output clocks are needed to measure all the delay mismatches in the output clock edges, the sum of which is equal to one reference clock period. The advantage of the PEC is that any mismatch arising in the delay sensing circuit, for example from the current source (I_c), the capacitor (C_{cl}) or the offset of the comparator will be equally observed for every calibration cycle. The calibration is only involved in delay comparison, therefore, any mismatch and offset due to the delay sensing circuit will cancel each other out. More specifically, the calibration senses the output of the frequency multiplier, so any mismatch arising from the EC of the circuit or from the routing from the VCDC to the EC will be detected and calibrated.

Other than the systematic mismatch in the clock edges, there exists another source of deterministic jitter that arises at a steady state from the PEC's bang-bang feedback loop. A MATLAB Simulink model for the PEC circuit is developed to examine the behavior of the system at steady state. A simplified model of MATLAB Simulink for PEC circuits is shown in Fig. 4.10. The model simulates the small signal behavior of the PEC circuit in a steady state condition. The comparator is modeled by a signum function and an inverter, which represents the inverted polarity of the comparator output (DN/UP). The SCSS is represented by eight integrators and the

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transfer function of the SCSS (K_{SCSS}). Each integrator is sampled after every eight clock cycles and is offset by one clock from the previous integrator. This represents the SCSS only switch to each VCDC at every clock cycle. The output of the integrator has a delay of eight clock cycles which represents the signal of the clock edge passing through the delay chain before V_c is updated. The updated V_c will only affect the clock edge delay in the next clock cycle. At this juncture, the VCDC is modeled by the transfer function of the VCDC (K_{VCDC}) and the K_{DVC} is the transfer function of the DVC. MUX is clocked by a counter, and it represents the DVC which measure the delay at the different clock edges for every clock cycle.

The simulation starts with an ideal steady state condition in which the signal variations of the control voltage (ΔV_c), output clock edge ($\Delta \phi_o$) and other components are small and can be assumed to be equal to zero ($nT=0$). However, in reality, a variation level of zero is impossible to achieve in the bang-bang feedback loop. The influence of noise causes the comparator to output high or low states randomly, even when both inputs are zero. The simulation starts when a small value offset is injected at the input of the comparator (ΔV_T) at $nT=1$ and the response of the PEC at steady state is shown Fig. 4.11. The control voltage (ΔV_c) will vary from -2 to +3 quantum steps, such that each quantum step equals to K_{SCSS} . This is equivalent to the SCSS current charges/discharges to the capacitor on control voltage in 1ns at every cycle. The variation in the control voltage at a steady state is more than one quantum error as the delay error sensed by the DVC cannot be reflected instantly through the feedback loop. The jitter of the clock edge arising from the PEC circuit at steady state is $K_{SCSS} \cdot K_{VCDC}$. This variation in the clock edge is a periodic variation with ten reference clock periods that the PEC is not able to calibrate. Nonetheless, the deterministic jitter can be minimized by reducing the $K_{SCSS} \cdot K_{VCDC}$ in the design stage.

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The jitter of the clock edge jitter arising from the PEC feedback loop at a steady state is defined as

$$\begin{aligned}
 \Delta t_{ph1,PEC} &= \sqrt{\frac{[(-2)^2 + (-1)^2 + (0)^2 + (1)^2 + (2)^2 + (3)^2 + (2)^2 + (1)^2 + (0)^2 + (-1)^2] \cdot (K_{SCSS} \cdot K_{VDC})^2}{10}} \\
 &= \sqrt{\frac{25 \cdot (K_{SCSS} \cdot K_{VDC})^2}{10}} \\
 &\cong 1.58 \cdot K_{SCSS} \cdot K_{VDC}
 \end{aligned} \tag{4-31}$$

The deterministic jitter at the output of the proposed frequency multiplier arising out of the PEC feedback loop at steady state can be defined as

$$\begin{aligned}
 \Delta t_{dj,PEC} &= \sqrt{\frac{(\Delta \phi_{o0})^2 + (\Delta \phi_{o1})^2 + (\Delta \phi_{o2})^2 + (\Delta \phi_{o3})^2 + (\Delta \phi_{o4})^2 + (\Delta \phi_{o5})^2 + (\Delta \phi_{o6})^2 + (\Delta \phi_{o7})^2}{8}} \\
 &= \sqrt{\frac{(0)^2 + (\Delta t_{ph1,PEC})^2 + \dots + (\Delta t_{ph7,PEC})^2}{8}} \\
 &= \sqrt{\frac{(0)^2 + (1.58 \cdot K_{SCSS} \cdot K_{VDC})^2 + \dots + (1.58 \cdot K_{SCSS} \cdot K_{VDC})^2}{8}} \\
 &\cong 1.48 \cdot K_{SCSS} \cdot K_{VDC}
 \end{aligned} \tag{4-32}$$

Fig. 4.10: Simplified MATLAB Simulink Model for

Fig. 4.10: Simplified MATLAB Simulink Model for PEC Circuit.

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Fig.4.11: Control Voltage Variation at Steady State of PEC Circuit.

4.3.3 Phase Error Calibration Loop Noise Analysis

The PEC consists of a number of active devices including the DVC, comparator and SCSS, each of which contributes to the noise of the frequency multiplier. A random noise analysis of the PEC bang-bang feedback loop is required to determine the parameters that affect its contribution to the frequency multiplier. Knowledge of the values of these parameters is also necessary in order to reduce the noise contributed by the PEC and to ensure it is minimal in comparison to that of the PPF as determined in the design stage.

Fig.4.12: Simplified Block Diagram of PEC Bang-bang Feedback Loop.

Fig. 4.12 shows a simplified block diagram of the PEC's bang-bang feedback loop in the s-domain. From the figure, the PEC loop is locked with reference calibration voltage (ΔV_{cal}), which is assumed to be zero at a steady state. Meanwhile, V_{noise} is defined as random noise from the PEC devices, which includes the DVC's output noise and the input referred noise of the comparator. In this analysis, we ignore

Noise Analysis

the noise contributed by the SCSS as this consists of a current source with capacitor output loading (C_d). Thus, the noise contributed by the SSCC will be much smaller than that contributed by the DVC and the comparator and the simulation results provided in Table 7-2 of Chapter 7.2 show this assumption to be true. The comparator is represented by a signum function with a differential input of $\Delta V_{cal,noise}$ and ΔV_T from the DVC output. The comparator outputs only a value of 1 or -1 to the SCSS at the n -th sampling time t_n . The integrator of the capacitor C_d is located at the control input of VCDC and is represented by $\frac{1}{s}$. ΔV_c denotes the variation in control voltage while the output jitter variation is represented by $\Delta \phi_o$, which will be detected by DVC for feedback correction.

The simplified block diagram of PEC the bang-bang feedback loop is the same as that of the first order bang-bang PLL in [95]. According to [95], the standard deviation of the output jitter for the first order bang-bang PLL is

$$\sigma_{bb} = 0.79 \cdot \sqrt{\theta_{bb} \cdot \sigma_j} \quad (4-33)$$

where θ_{bb} is the phase change occurring in the loop after one update and σ_j is the standard variation of the input noise. The standard deviation of the random output jitter of the PEC bang-bang feedback loop arising from noise from the DVC and comparator can be represented as

$$\Delta t_{rj,PEC} = \frac{0.79 \cdot \sqrt{V_{bb} \cdot \sigma_n}}{K_{DVC}} \quad (4-34)$$

where V_{bb} is defined as the quantum V_T change after one update, and σ_n is the standard variation of the input noise (V_{noise}) due to the DVC's output noise and the comparator's input referred noise. The V_{bb} can be represented by following equation

$$V_{bb} = K_{SCSS} \cdot K_{VCDC} \cdot K_{DVC} \quad (4-35)$$

By substituting equation (4-35) into equation (4-34),

$$\begin{aligned}\Delta t_{rj,PEC} &= \frac{0.79 \cdot \sqrt{K_{SCSS} \cdot K_{VCDC} \cdot K_{DVC} \cdot \sigma_n}}{K_{DVC}} \\ &= 0.79 \cdot \sqrt{\frac{K_{SCSS} \cdot K_{VCDC}}{K_{DVC}} \cdot \sigma_n}\end{aligned}\quad (4-36)$$

To ensure that the random noise from the PEC does not affect the output jitter performance of the frequency multiplier, the random jitter of the PEC must be much smaller than that of the open loop frequency multiplier ($\Delta t_{rj,OL}$), which includes the PPF, VCDC and EC. It should be at least 10 times smaller as shown in the following equation:

$$\begin{aligned}\Delta t_{rj,PEC} &\ll \Delta t_{rj,OL} \\ \Delta t_{rj,PEC} &\cong \frac{1}{10} \cdot \Delta t_{rj,OL} \\ (0.79)^2 \cdot \left(\frac{K_{SCSS} \cdot K_{VCDC}}{K_{DVC}} \cdot \sigma_n \right) &\cong \frac{1}{100} \cdot \Delta t_{rj,OL}^2 \\ \frac{K_{SCSS} \cdot K_{VCDC}}{K_{DVC}} &\cong 0.016 \cdot \frac{\Delta t_{rj,OL}^2}{\sigma_n}\end{aligned}\quad (4-37)$$

From equation (4-37), it is clear that K_{SCSS} , K_{VCDC} and K_{DVC} will affect the noise contributions of the PEC. To minimize the noise contribution of PEC, K_{SCSS} and K_{VCDC} must be as small as possible, while K_{DVC} must be as large as possible.

4.4 Jitter Performance Comparison

TABLE 4-2: Random Jitter and Deterministic Jitter Equations of DLL and PPF Based Frequency Multiplier.

DLL Based Frequency Multiplier	
Random Jitter	$\Delta t_{rj,DLL} = \sqrt{18} \cdot \sqrt{\frac{kT}{f_{ref} \cdot V_{pp}}} \cdot \frac{1}{\sqrt{I_T}}$
Deterministic Jitter (CP current mismatch)	$\Delta t_{dj,DLL_CP} = \frac{\varepsilon \cdot t_{pw}}{\sqrt{8}}$
Deterministic Jitter (delay cells mismatch)	$\Delta t_{dj,DLL_DC} \cong \frac{0.14 \cdot \sigma_{ei}}{f_{ref}}$
PPF Based Frequency Multiplier	
Random Jitter	$\Delta t_{rj,PPF} = \sqrt{\frac{6}{\pi}} \cdot \sqrt{\frac{kT}{f_i V_i _{pp}}} \cdot \frac{1}{\sqrt{I_{rms}}}$
Deterministic Jitter (PEC Bang-bang Feedback)	$\Delta t_{dj,PEC} \cong 1.48 \cdot K_{SCSS} \cdot K_{VDC}$

Analyses of the random and deterministic noises associated with the DLL and PPF-based frequency multipliers have been presented in Chapter 3.5.1 and Chapter 4.3.1 respectively. Table 4-2 provides a summary of the random and deterministic jitter equations of each architecture type. In the random noise analysis, we evaluate only the noise contributed by the delay cells in the DLL and the PPF in the PPF-based frequency multiplier as this is critical for defining the clock edges in both architectures. Meanwhile, the PEC in the PPF based frequency multiplier contributes

Jitter Performance Comparison

a minimal level of random noise to the output frequency. From the random jitter equations of the DLL and PPF frequency multipliers listed in Table 4-2, it is apparent that under identical power consumption and swing conditions, the PPF-based frequency multiplier has better jitter performance than the DLL. Because the PPF is a passive circuit, its random noise performance is much better than that of a conventional delay chain which is constructed using an active circuit. Thus, the PPF is no longer a dominant noise source in the PPF-based frequency multiplier. However, the VCDC in PPF-based frequency multiplier continues to contribute random noise to the circuit, much like the D2S does in a conventional DLL. Since the VCDC circuit has the same architecture as the D2S in the conventional DLL along with an additional variable current source for delay variation control, the random noise contributed by active devices is closed in both the VCDC and D2S. Therefore, the overall random jitter performance of the PPF-based frequency multiplier is still much better than that of the conventional DLL frequency multiplier.

As obvious from the mismatch equations listed in Table 4-2, the deterministic jitter of the DLL without a calibration circuit depends mainly on the delay cell mismatch in the VCDL and on the mismatch in the CP. Although results of the simulation show the deterministic jitter of the PPF-based frequency multiplier arising from the mismatch in the devices to be negligible (the mismatch and offsets of the devices are transparent in the PEC circuit), the PEC still contributes deterministic jitter arising from its PEC bang-bang feedback as shown in Table 4-2. The deterministic jitter of the PPF-based frequency multiplier thus depends on two controllable parameters (K_{SCSS} and K_{VCDC}), and can be minimized by designing a circuit with small K_{SCSS} and K_{VCDC} values. The trade-off for these small values is a longer locking time. On the contrary, the mismatch parameters in the DLL (σ_{e_i} and ε)

Jitter Performance Comparison

only can be minimized by increasing the layout area and current consumption of DLL [89], [90]. In conclusion, the proposed PPF-based frequency multiplier has both better random and deterministic jitter performance than DLL-based frequency multipliers.

Chapter 5

Prototype Implementation

5.1 Introduction

A prototype of the polyphase filter based frequency multiplier was fabricated using 0.13μm CMOS 1.5V process technology. Fig. 5.1 shows a block diagram of the prototype's implementation. In this IC prototype, an on-chip master bias circuit is used to generate a reference current that is mirrored throughout the entire chip to provide the necessary biasing currents. At the same time, an on-chip oscillator with external crystals is employed as a reference clock for the frequency multiplier.

Fig. 5.1: Implementation Block Diagram of the Prototype.

5.2 Crystal Oscillator Design

Fig. 5.2: Schematic Circuit of Crystal Oscillator.

Fig. 5.2 shows a schematic of a Pierce oscillator. It consists of an internal inverter, a biasing circuit, a startup circuit and an external crystal. The transistor M1 and M2 forms a class AB inverter that provides an approximately 180° phase shift from the input (X_{01}) to output (X_{02}). The transistors M6-M20 and R2 provide a biasing to the inverter and the biasing voltage for the gates of the class AB inverter are generated by passing a constant current through a pair of diodes connected transistors M7-M10. Transistor M21, M22 and R3 provide a startup current to the biasing circuit when the supply voltage is ramped up. A reverse diode connected to the transistors

Polyphase Filter Design

M3 and M4, acts as an amplitude limiter to limit the inverter output voltage close to V_{dd} or ground. By doing so, it reduces the harmonics and distortion of the output voltage, thus maintaining the signal in the sine wave. The high value resistor R1 provides negative feedback and sets the bias point of the inverter near the mid-supply, which sets the operation of the inverter at the high gain linear range.

Meanwhile, the external crystal is modeled by the static capacitance (C_{x0}), motional capacitance (C_{x1}), motional inductance (L_{x1}), series resonant frequency resistance (R_{x1}) and loading capacitance (C_{x2} and C_{x3}). The above parameters are provided by the crystal supplier. The π network formed by the external crystal provides an additional 180° phase shift, bringing the total phase shift around the crystal oscillator to 360° . This satisfies one of the conditions required to sustain oscillation. Another condition for proper startup and sustained oscillation is that the close loop gain should be equal to or more than one. To verify the crystal oscillator for proper startup and sustained oscillation, an AC simulation is performed on the open loop of the crystal oscillator. This allows us to obtain the gain and phase margin. Because the oscillator drives the PPF, the model of the PPF is added to the output of the crystal oscillator. The RC value of the PPF is determined by the method described in Chapter 5.3 and the result of the AC simulation is illustrated in Fig. 5.3 and it shows that gain and phase margins of 9dB and -13° respectively will indeed guarantee that the oscillation starts up and is sustained. Transient simulation is also performed, the results of which are shown in Fig. 5.4 and Fig. 5.5. This simulation also shows that the crystal oscillator can startup properly and that it can sustain the oscillation. The startup time is around 800us and the output signal of the crystal oscillator is maintained in a sine wave form with minimal distortion. The crystal oscillator consumes 0.38mA of current at a steady state.

Polyphase Filter Design

Fig. 5.3: AC Simulation Result of Crystal Oscillator Open Loop.

Fig. 5.4: Startup Simulation of Crystal Oscillator.

Polyphase Filter Design

Fig. 5.5: Transient Simulation Result of Crystal Oscillator.

5.3 Polyphase Filter Design

A passive RC PPF [93], [94] is used as a clock-phase generation circuit in this frequency multiplier. Fig. 5.6 shows (a) the one-stage and (b) two-stage passive RC PPF. To achieve a functional PPF, the RC time constant of the PPF must be equal to $\frac{1}{2 \cdot \pi \cdot f_i}$, where f_i is the targeted input frequency for this design, which is 25MHz.

Fig. 5.6: (a) One-stage Passive RC Polyphase Filter.

(b) Two-stage Passive RC Polyphase Filter.

The RC time constant variation in the CMOS process can be as large as $\pm 20\%$ for a 3-sigma variation. From the simulation results shown in Fig. 5.7, the RC time constant variation will cause the phase error of the single-stage RC PPF to be as large as ± 609 ps. Therefore, two stages of passive RC PPF (see Fig. 5.6) are needed to cover the process variation. The first stage and second stage of the PPF have an RC time constant of $\frac{1}{2 \cdot \pi \cdot (30\text{MHz})}$ and $\frac{1}{2 \cdot \pi \cdot (20\text{MHz})}$ respectively and the two-stage PPF reduces the phase error from ± 609 ps to ± 65 ps. By choosing the RC time constant of

$\frac{1}{2 \cdot \pi \cdot (30\text{MHz})}$ and $\frac{1}{2 \cdot \pi \cdot (20\text{MHz})}$, the notches shown in Fig. 5.7 are located at 30MHz and 20MHz respectively. These are very close to the input frequency of 25MHz which serves to minimize the phase error over the process corner variation.

Fig. 5.7: One-stage and Two-stage Polyphase Filter Phase Error Simulation.

Because the designed RC time constant of the first stage PPF is two-thirds that of the second stage PPF, we are presented with two options in relation to the resistor and capacitor values. The first option is to maintain the PPF capacitor (C_p) size at both stages, while $R_{p1}=2 \times R_{unit}$, and $R_{p2}=3 \times R_{unit}$. The second option is to maintain the size of the PPF resistor (R_p) at both stages, while $C_{p1}=2 \times C_{unit}$, and $C_{p2}=3 \times C_{unit}$. The first

Polyphase Filter Design

option is selected after taking into account layout area efficiency and component-matching considerations. This is because the layout of capacitor is larger than the resistor. Choosing multiple C_{units} to form a C_p will further increase the area due to the minimum spacing of the capacitor in the design rules. The smaller value of the C_{unit} will also serve to degrade the matching of the capacitor.

The only noise source of the PPF arises from the thermal noise of its resistor. The power of the total noise is thus proportional to the resistor value as discussed in Chapter 4.3. Therefore, a lower value resistor is preferable. However, the minimum value of such a resistor is limited by the gain and phase margin of the crystal oscillator. To make sure that the crystal oscillator can start up properly, the gain margin must be larger than 1 or 0dB, and the phase margin must be lower than 0. Fig. 5.8 and Fig. 5.9 show the gain and phase margins of a crystal oscillator versus that of a unit resistor. From the figure, the minimum unit resistor value for the oscillator to start up properly in relation to the corner variation is 1.1 k Ω . Therefore, in this design, R_{p1} , R_{p2} and C_p are 2.2k Ω , 3.3k Ω and 2.4pF respectively.

Polyphase Filter Design

Fig. 5.8: Gain Margin of Crystal Oscillator versus PPF Unit Resistor.

Fig. 5.9: Phase Margin of Crystal Oscillator versus PPF Unit Resistor Value.

Polyphase Filter Design

After determining the resistor and capacitor values of the PPF, it is necessary to determine the mismatch in the clock edges arising from the mismatch in the resistor and capacitor. A series of simulations are run by sweeping the resistor and capacitor mismatch from 0% to 5%. The results of the simulation are shown in Fig. 5.10. The worst cases appear to arise from mismatches in the resistor at the second stage. With a resistor of a reasonable size, it is easy to achieve a mismatch of less than 1% in the CMOS process such that the worst possible delta phase error is 0.2° or 22ps. This value is lower than the phase error due to the RC time constant mismatch.

Fig. 5.10: Delta Phase Error due to Resistor and Capacitor Mismatch in PPF.

Other than the RC time constant and the mismatch in the resistor and capacitor arising from process variation, there are several reasons for the clock phases generated by the PPF to be mismatched. First, the phase shift of the reference signal

Polyphase Filter Design

from the crystal oscillator (X_{o1} and X_{o2}) is more than 180° because of the delay in the inverter component of the oscillator circuit. Second, the harmonic from the reference signal also increase the mismatch of the clock phases. Third, the crossing points of the differential clock phases in the PPF occur at different common voltage levels. Fourth, the propagation delay of each VCDC is different.

A post layout simulation becomes necessary to verify that the phase error contributed by all components (crystal oscillator, PPF, VCDC and EC) are within reasonable range and can be calibrated. The maximum phase error over the process corner at the EC output (f_{out}) is around -250ps. The simulation results are summarized in Table 5-1.

TABLE 5-1: EC Output Phase Error over Process Corners.

		Typical		Slow		Fast	
Clock Edge	Ideal Delay	Clock Edge Delay	Phase Error	Clock Edge Delay	Phase Error	Clock Edge Delay	Phase Error
$\phi_{o0} - \phi_{o1}$	5.000ns	4.973ns	-27ps	4.940ns	-60ps	4.910ns	-90ps
$\phi_{o0} - \phi_{o2}$	10.000ns	9.951ns	-49ps	9.940ns	-60ps	9.966ns	-34ps
$\phi_{o0} - \phi_{o3}$	15.000ns	14.773ns	-227ps	14.814ps	-186ps	14.844ns	-156ps
$\phi_{o0} - \phi_{o4}$	20.000ns	19.910ns	-90ps	19.875ns	-125ps	19.945ns	-55ps
$\phi_{o0} - \phi_{o5}$	25.000ns	24.872ns	-128ps	24.804ps	-196ps	24.836ns	-164ps
$\phi_{o0} - \phi_{o6}$	30.000ns	29.921ns	-79ps	29.880ns	-120ps	29.962ns	-38ps
$\phi_{o0} - \phi_{o7}$	35.000ns	34.780ns	-220ps	34.808ns	-192ps	34.859ns	-141ps

Although there is a loss and difference amplitude of the differential clock phases from PPF, this is not a concern as long as the signal from the crystal oscillator

Polyphase Filter Design

and the PPF output signal are large enough to drive the VCDC input fully on or off. The jitter performance is the only drawback to the system. The jitter contributed by the smaller amplitude of the differential clock phase is $\sqrt{2}$ larger, but this is unlikely to adversely impact the jitter improvements rendered by this new method.

5.4 Voltage-Controlled Delay Cell Design

Fig. 5.11: Schematic Circuit of VCDC.

A schematic of the VCDC is shown in Fig. 5.11. Transistors M1-M6 form a differential amplifier with an active current mirror load. The differential amplifier will convert the differential clock phase from the PPF to a single-ended rail-to-rail output clock edge after passing through the inverter for edge combination. The gain of the differential amplifier is made as high as possible to optimize noise performance and reduce the noise contribution of the device to the output jitter. Larger sized transistors M1 and M2 are also used to minimize contribution of flicker noise.

Since each phase clock in the PPF produces a large signal, the differential amplifier exhibits slewing behavior. Thus, the delay of the differential amplifier can be approximated as follows:

$$t_d \cong V_p \left(\frac{C_p}{I_{ss}} \right) \quad (5-1)$$

Voltage-Controlled Delay Cell Design

where $\frac{I_{ss}}{C_p}$ is the slew rate, V_p is one half of the full output swing and C_p is the effective capacitance associated with the output of the differential amplifier. I_{ss} is the total tail current contributed by the static biasing current I_5 and the dynamic biasing current I_6 . I_5 is fixed to avoid a zero tail current when V_c is too high. Thus, the delay variation of the VCDC necessary for calibration purposes can be achieved by storing the charge in the MIM capacitor C_d , and by defining the V_c . In this design, the delay variation of the VCDC is -350ps at worst, and -250ps of this delay is allocated to cover the maximum phase error at multiplication frequency (f_{out}). The remaining delay of -100ps is treated as an over-design margin. Fig. 5.12 shows the delay in the VCDC variation over the process corners. The VCDC's typical transfer function can be estimated from Fig. 5.12 and defined as

$$\begin{aligned}
 K_{VCDC} &= \frac{\Delta\phi_o}{\Delta V_c} \\
 &= \frac{100ps}{100mV} \\
 &= 1ns / V
 \end{aligned}
 \tag{5-2}$$

Voltage-Controlled Delay Cell Design

Fig. 5.12: VCDC Delay Variation over Process Corners.

5.5 Edge Combiner Design

Fig. 5.13: Digital Edge Combiner.

Fig. 5.13 shows the digital EC used in the frequency multiplier. All the signals in the EC are single-ended rail-to-rail digital signal. Each of the eight clock edges (ϕ_0 to ϕ_7) generated by the VCDC will pass through a digital pulse generator (PG) to generate a series of pulse signals (P_a to P_h) with narrow pulse widths of around 1ns. All such narrow pulse width signals will then be combined by a digital OR-gate to generate the multiplication frequency (f_{out}). The f_{out} from the OR-gate will be fed to the PEC circuit for calibration. To achieve a multiplication frequency signal with a duty cycle close to 50%, the f_{out} will pass through another PG, which will then generate a signal with a pulse width close to half a period of the f_{out} , which is around 2.5ns. An output buffer with the capability to drive a 50 Ω instrument load is used for measurement purposes.

The schematic of the pulse generator (PG) is shown in Fig. 5.14. It consists of an inverter delay chain and a digital AND-gate. The delay of the inverter delay chain equals the pulse width generated at the output. The schematic of the output buffer necessary to drive a 50 Ω load is shown in Fig. 5.15. It is a pure digital inverter with

Edge Combiner Design

two pre-drivers that drive the PMOS and NMOS of the inverter. The inverters in the pre-driver P have a higher trip point, while the inverters in the pre-driver N have a lower trip point. The pre-drivers are included in the design to prevent a direct-path current by preventing both the PMOS and NMOS from turning on together for short period of time during switching. When the output charges up a load, the NMOS will be turned off before the PMOS charges the load and vice-versa. The output buffer can drive a high impedance load of 50 Ohm in parallel with a 10pF load.

Fig. 5.14: Pulse Generator.

Fig. 5.15: Output Buffer.

5.6 Phase Error Calibration Design

Fig. 5.16: Implementation Block Diagram of PEC Circuit.

Fig. 5.16 shows a block diagram illustrating the implementation of the PEC circuit. The PEC consists of a delay-to-voltage converter (DVC), one comparator, and eight units of switched-current-source-and-sink (SCSS).

The DVC consists of a delay chain, one D-flip-flop, and one charge pump (consisting of a current source I_c , and a capacitor, C_{cl}). The function of the DVC is to convert the delay of two adjacent output clock edges to the voltage domain as illustrated in Fig. 5.17.

Fig. 5.17: Operation Waveforms of the DVC Circuit.

As can be seen in the figure, the delay between ϕ'_{o0} and ϕ_{o1} is reduced by inserting a 4ns delay chain. The delay between ϕ'_{o0} and ϕ_{o1} is represented by the pulse width of signal Q (t_{Q0}). The pulse signal Q will switch on the current source (I_c) to charge C_{c1} such that the output of DVC (V_T) will be charged to voltage level (V_{Tpeak0}). V_{Tpeak0} is proportional to the t_{Q0} , and can be expressed as

$$V_{Tpeak0} = \left(\frac{I_c}{C_{c1}} \right) \times t_{Q0} \quad (5-3)$$

The design value of I_c is 800 μ A, the value of C_{c1} is 800fF and the typical value for t_{Q0} is around 1ns. Therefore, the V_{Tpeak0} is around 1V. At this level of sensitivity, any 1ps delay variation of ϕ_{o1} will translate to a 1mV variation at V_{Tpeak0} , which is a reasonable voltage variation for detection by a comparator.

The transfer function of the DVC circuit (K_{DVC}) is defined as

$$\begin{aligned}
 K_{DVC} &= \frac{V_{Tpeak0}}{t_{Q0}} \\
 &= \frac{I_c}{C_{cl}} \\
 &= \frac{800\mu A}{800fF} \\
 &= 1GV/s
 \end{aligned} \tag{5-4}$$

The circuit schematic of the DVC charge pump, which serves as a sub-block in the DVC, is shown in Fig. 5.18.

Fig. 5.18: Schematic of DVC Charge Pump.

The DVC charge pump consists of a single-to-differential converter, which will convert the single-ended input signal (Q) from the D-flip-flop to a differential signal, UP and UPb . The differential output will drive the input of a differential amplifier with a diode-connected load. The amplifier is biased by I_{ss} of $800\mu A$. When the signal Q is high, the differential amplifier input transistor, M1 and M2 will steer the I_{ss}

current from M3 to M4. M6 will then mirror the current from M4 and charge up the C_{cl} . V_T will be reset to 0V by V_{Trst} when M7 is turned on, subsequently discharging the charges on C_{cl} .

The 4ns delay chain in the DVC is of the inverter type. The delay value of the delay chain will vary as a result of variations in the processes. A 4-bits MUX is used to select the delay value of the delay chain when the delay varies under different process corners. Fig. 5.19 provides a schematic of the delay chain.

Fig. 5.19: Schematic of DVC Delay Chain.

When the power is up, the delay of the DVC delay chain is set to a minimum. Therefore, when the delay between ϕ'_{o0} and ϕ_{o1} is the largest, so is the pulse width of Q (t_{Q0}). As a result, the output of the DVC (V_T) will be charged to V_{dd} , which is 1.5V. The delay will increase in steps of 250ps at every cycle until the V_{Tpeak0} is less than 1V at which time the settings will be stored. At this stage, the delay between ϕ'_{o0} and ϕ_{o1} is around 1ns. Fig. 5.20 illustrates the delay coverage of the DVC delay chain. For the design to be viable, the delay chain must achieve a 4ns delay at both slow and fast corner conditions. Although the delay is barely below 4ns for the fast corner, it

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increase the t_{Q0} only slightly such that it is larger than 1ns. Given that the V_{Tpeak0} is proportional to t_{Q0} , the value of V_{Tpeak0} will slightly larger than 1V. At steady state, the V_T and V_{cal} will have the same value of slightly above 1V, which is the input common voltage of the comparator. However, this slight increment in the input common voltage will not affect the performance of comparator.

Fig. 5.20: DVC Delay Chain Variation over the Process Corner.

Since the purpose of the DVC in this circuit is to detect delay variations of 1ps between ϕ'_{o0} and ϕ_{o1} , the comparator operating in the next stage has to detect variations in V_T that are as low as 1mV. Each process of comparing V_T and V_{cal} must be settled within the pulse width of CK_{comp} , which is around 1ns. Therefore a high

speed latched comparator is needed. Fig. 5.21 shows the circuit schematic of the comparator, while Fig. 5.22 shows the differential-to-single-ended converter which serves as the sub-block in the comparator.

Fig. 5.21: Schematic of Comparator

Fig. 5.22: Schematic of Differential-to-single-ended Converter in Comparator.

Fig. 5.23: Operation Waveforms of Comparator.

The comparator consists of a preamplifier in the first stage, a track-and-latch in the second stage and two differential-to-single-ended converters. The preamplifier is a differential amplifier with a diode-connected load (M1-M7). The preamplifier is used to increase the resolution and to minimize the effect of kickbacks. Although the output of the amplifier is larger than the input, it is still much smaller than the voltage level that is needed to drive the digital circuit. Therefore, the track-and-latch stage (M8-M13) is used to amplify the signal again to the rail-to-rail digital signal. When the CK_{comp} is low, the track-and-latch stage is turned off and the transistor M10 will be turned on, such that the V_{op} and V_{on} are forced to a common mode voltage in order to erase the memory of the previous value. The V_{op} and V_{on} can reach V_{dd} or ground much faster in this way, thus improving the overall speed. At this juncture, transistor M13 will be turned off, such that the latch is disabled and the current consumption is reduced. The comparator conducts its comparison of the inputs and outputs when CK_{comp} is high. The latch is enabled as the high value of CK_{comp} will cause M10 to be

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turned off and M13 to be turned on. When there is an unbalance in the inputs of the latch, the positive feedback provided by the latch will switch the output voltage (V_{op} and V_{on}) to the rail-to-rail output voltage. The output of the latch will pass through two differential-to-single-ended converters, in which one of the two input polarities is inverted. A schematic of the differential-to-single-ended converter is provided in Fig. 5.22. The inverter at the output is designed to have lower trip point (V_{trip}). Therefore, only when V_{se} is lower than the V_{trip} , will the inverter be triggered. The operation waveforms of the comparator are presented in Fig. 5.23. The differential-to-single-ended converter will generate a pulse signal (DN and UP) that travels to the SCSS for delay compensation purposes. The comparator is simulated through all corners to make sure the resolution that is achievable is less than 1mV and the speed is fast enough to provide the correct output value of under 1ns.

The SCSS consists of eight current sources and sinks, seven of which control the V_c of the eight VCDCs respectively, while the remaining one controls the V_{cal} of the DVC comparator. Fig 5.24 shows a schematic of one current source and sink which comprises two differential switches (M1, M2 and M3, M4) and two digital single-to-differential converters.

As mentioned in Chapter 4.3.3, the parameters K_{SCSS} , K_{VCDC} and K_{DVC} need to be determined at the design stage in order to minimize the effect of PEC random noise on the output jitter. K_{VCDC} is determined by the phase error of the clock edges and the delay variation of the VCDC as it moves through the process corner. Meanwhile, K_{DVC} is determined by the V_{Tpeak0} and t_{Q0} . The nominal value of V_{Tpeak0} is 1V, which is a reasonable value for a circuit with a supply voltage of 1.5V. While the nominal value of t_{Q0} is 1ns as limited by the operating frequency of the multiplier, the only parameter that can be adjusted is K_{SCSS} that can be defined as

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$$\begin{aligned}
 K_{SCSS} &= \frac{\Delta V_c}{\text{cycle}} \\
 &= \frac{I_{SS} \cdot \Delta t_{PG}}{C_d} \cdot \frac{1}{\text{cycle}}
 \end{aligned} \tag{5-5}$$

where ΔV_c is the voltage variation arising from the SCSS current I_{SS} charging or discharging from the capacitor C_d . Δt_{PG} is the switch on time of the current source and sink at every cycle. From equation (4-37), and simulation results in Table 7-1 and 7-2, K_{SCSS} can be determined as follows

$$\begin{aligned}
 \frac{K_{SCSS} \cdot K_{VDC}}{K_{DVC}} &\cong 0.016 \cdot \frac{\Delta t_{rj,OL}^2}{\sigma_n} \\
 K_{SCSS} &\cong 0.016 \cdot \frac{K_{DVC}}{K_{VDC}} \cdot \frac{\Delta t_{rj,OL}^2}{\sigma_n} \\
 K_{SCSS} &\cong 0.016 \cdot \frac{1GV/s}{1ns/V} \cdot \frac{(1.46ps)^2}{\sqrt{(373uV)^2 + (190uV)^2}} \\
 K_{SCSS} &\approx 81.6\mu V
 \end{aligned} \tag{5-6}$$

Because Δt_{PG} is limited by the operating frequency of the multiplier, only I_{SS} and C_d can be adjusted to achieve a low K_{SCSS} . The lowest reasonable biasing current of the SCSS (I_{SS}) is thus 1 μ A. Based on the selected I_{SS} and Δt_{PG} of 1ns, C_d is theoretically calculated as

$$\begin{aligned}
 \frac{I_{SS} \cdot \Delta t_{PG}}{C_d} &= K_{SCSS} \\
 C_d &= \frac{I_{SS} \cdot \Delta t_{PG}}{K_{SCSS}} \\
 &= \frac{1\mu A \cdot 1ns}{81.6\mu V} \\
 &= 12.25pF
 \end{aligned} \tag{5-7}$$

Herewith, C_d is set at 10pF, a value close to the calculated value. This value of C_d is unlikely to degrade much on output jitter performance and smaller the area. Therefore, the transfer function of the SCSS is defined as the voltage variation of V_c at every updated cycle from the comparator. It is given as follows:

$$\begin{aligned}
 K_{SCSS} &= \Delta V_c \\
 &= \frac{I_{SS} \cdot \Delta t_{PG}}{C_d} \\
 &= \frac{1\mu A \cdot 1ns}{10pF} \\
 &= 100\mu V
 \end{aligned}
 \tag{5-8}$$

The biasing of the current source and sink is set at $1\mu A$ in order to minimize the variation in V_c . However, to reduce the settling time at the initial stage, the current is set as large as $250\mu A$ for the first 64 cycles of the reference clock. This is counted by a 6-bit counter from the time at which the power is switched on. Given that each current source and sink is switched on for $1ns$ at every cycle, a $10pF$ capacitor C_d will be charged up $25mV$ at every cycle. The design provides for enough cycles to charge the capacitor from $0V$ to $1.5V$ in the worst case. In a typical case, the capacitor C_d only needs to charge from $0V$ to $0.75V$. An additional 250 cycles are needed to charge the capacitor C_d to the desired voltage when the biasing current is switched to $1\mu A$. Thus, the settling time for the frequency multiplier is about 314 cycles of the reference clock, or $12.56\mu s$ based on the reference clock frequency of $25MHz$.

A unity gain buffer is connected in between the output of the two switches, so that the common drain voltage of M1 and M3 can track the voltage of V_c . This is in order to maintain the symmetrical behavior of M1/M2 and M3/M4. Each current source and sink is enabled by setting the Sel signal at high and the sequence of the signal is controlled by a digital shift register, which is in turn synchronized by a reset signal from ϕ_7 .

Fig. 5.24: Schematic of One Current Source and Sink.

The schematic of the buffer is shown in Fig. 5.25. The buffer is a two-stage operational amplifier with negative feedback. Transistors M1-M4 and M6 form the first stage of the differential amplifier with an active current mirror load, while transistors M5 and M7 form the single-ended common-source amplifier. R_c and C_c are the compensation resistor and capacitor respectively that improve the gain and phase margins of the amplifier.

Fig. 5.25: Schematic of Buffer in Current Source and Sink.

To prevent the feedback circuit from oscillating, an AC simulation is performed on the open loop buffer. This enables the circuit to obtain the gain and phase margins. Fig. 5.26 shows that the gain margin and phase margin are 50dB and 50° respectively, which are safe levels that prevent oscillation. The unity gain bandwidth is 30MHz, and the input range for the buffer is between 0.4V and 1.38V. The limited range of the buffer at lower voltages is not of concern in this circuit. This is because all the clock edge delays are faster than the ideal delay in the difference corner. The V_c values of VCDC at each clock phase will be higher than the reference V_c value, which is 0.85V at a steady state. The buffer consumes a total of 75μA of current.

Fig. 5.26: AC Simulation Results of Buffer Open Loop.

A single to differential converter is implemented by digital circuit, the schematic of which is shown in Fig. 5.27. One of the inverters in the “outb” path is designed to be longer to provide a slower path that will allow the rising and falling edge from “out” and “outb” to be aligned.

Fig. 5.27: Schematic of Single to Differential Converter.

Chapter 6

Layout

6.1 Floor Plan

Having detailed the architecture of the multiplier, the design of its circuits and the results of the simulations, we now turn our attention to the layout of the frequency multiplier. Fig. 6.1 shows the floor plan of the frequency multiplier. The differential input (X_{o1} and X_{o2}) of the frequency multiplier is connected to an external differential crystal oscillator. The frequency multiplier is a mixed-signal circuit and its differential input signal ensures better immunity against common mode noise, generated from multiple sources including the power supply, the ground and the bounce in the substrate arising from the digital circuits. The differential input will be applied directly to the polyphase filter (PPF) and the four clock phases it generates will pass through eight adjacent VCDCs in order to ease the route of the clock phase to the VCDC. The output signals of the VCDCs will couple directly to the inputs of the EC located at the bottom of the VCDCs. Meanwhile, the SCSS and SR are located at the top of VCDCs. Feedback from the f_{out} is fed directly into the DVC, which is located on the left side of the VCDC. The comparator is also placed in the vicinity of DVC and SCSS to ensure the shortest possible route between the comparator's input (from DVC and SCSS) and output (to SCSS). Next, the noisy buffer, which is a high speed switching digital circuit that drives the 50Ω load, is placed far away from the EC to reduce issues related to the coupling of the substrate noise. The input of the reference

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clock and the output of the frequency multiplier are oriented at 90° to minimize the effect of mutual inductance coupling between the bonding wires. Finally, the most sensitive circuits, namely the bandgap and the biasing circuit, are located as far as possible from the output buffer to minimize the coupling of the substrate noise.

Fig. 6.1: Floor Plan of Proposed Frequency Multiplier.

6.2 Low Noise Considerations

Given that the main objective of this research effort is to achieve a low jitter frequency multiplier for the high-speed ADC, the noise immunity of the circuit layout is of primary concern. Because the frequency multiplier consists of highly sensitive analog circuits and high speed switching digital circuits, the noise generated from the digital circuits can easily couple through the supply, ground and signal lines, as well as through the substrates. Therefore, the noise isolation of both circuits is vital and the management of the supply and ground lines needs to be carefully considered. It is critical to isolate the substrates and shield the signal lines in order to minimize the noise coupling.

6.2.1 Supply and Ground Noise Isolation

In order to effectively isolate the noise arising from the supply and ground lines, it is useful to consider the highly sensitive analog circuits and the noisy digital circuits separately. The highly sensitive analog circuits include the PPF, the VCDC, the DVC, the comparator, the SCSS, the bandgap and the biasing circuit. The noisy digital circuits include the SR, the EC and the buffer. The digital circuits switch at high speeds, requiring a large current to be drawn from the supply and the ground over short periods when the circuit is turned on. Because the supply and ground of the digital circuit are connected to their respective packaging pins through an inductive bonding wire, a large voltage bounce will occur at both lines. The supply and ground of the analog circuits will be separated from the digital circuits to prevent the bounce from feeding into the highly sensitive analog circuits. Although the digital circuits are noise generating, but building blocks like EC and buffer are critical circuits that will affect the jitter of the output frequency. Therefore, each digital circuit is assigned a

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separate supply and ground line. In addition, the digital supply and ground lines of the EC and SR are connected to their respective packaging pins in a star configuration as shown in Fig. 6.2 to reduce the usage of the pins. Given that the buffer needs to drive a 50Ω load, the current it draws is very large, and it becomes necessary to reserve individual supply and ground pins for it. Double bonds will also be implemented on the supply and ground pads linked to the packaging pins to increase the current capacity of the pins and also to reduce the inductive effect of the bonding wires, thus minimizing the supply and ground bounce. To further reduce this bounce, decoupling dual-MIM capacitors are added in between the supply and ground lines of every digital circuit [7], [8].

Fig. 6.2: Digital Circuits Supply and Ground Pins in Star Configuration.

The highly sensitive analog circuits use a differential configuration. The biasing current passing through the analog supply and ground lines are constant and

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no bouncing issues arise on them. All the supply and ground lines share the same pad and pin, and the star configuration applies on the pad of the analog circuit just as it does on the digital circuit as shown in Fig. 6.3. The supply and ground lines for each analog circuit are separated to reduce unnecessary noise coupling through the lines. However, there still exist a digital switching circuit in the analog circuits including the delay chain, the DFF and the PG in the DVC which have separate supply and ground lines. These circuits use individual pads and pins to reduce the noise from coupling and affecting the other analog circuits. A decoupling dual-MIM capacitor is also added in between the supply and ground line for every analog circuit.

Fig. 6.3: Analog Circuits Supply and Ground Pads in Star Configuration.

6.2.2 Substrate Noise Isolation

Because the NMOS and PMOS devices are fabricated on the same silicon substrate in this CMOS process, the layout profile creates unwanted paths between the various devices in the circuit. A high speed switching digital circuit will inject noise into the substrate and this will couple onto the highly sensitive analog circuit directly. To minimize the coupling of the substrate noise, the highly sensitive analog circuit has to be placed as far as possible away from the noisy digital circuit. For instance, the bandgap and biasing circuit is placed far away from the buffer.

In the CMOS process, the bulk of the NMOS is typically placed on the global p-substrate that is shared and easily polluted by the digital circuits. This is not the case for the PMOS, as it has its bulk on a dedicated n-well and it can be tied to the VDD through a dedicated low-impedance path. Further improvements at the level of the substrate noise isolation can be achieved in the analog circuits by using a triple well NMOS to replace the normal NMOS. The triple well NMOS is a normal NMOS within a p-well that is isolated from the global p-substrate. The isolation is accomplished by inserting a buried n-type layer between the local p-well and the p-substrate as shown in Fig. 6.4. Since the p-well is totally isolated from the substrate, the substrate noise coupling from the digital circuits can be further suppressed for better noise isolation.

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Fig. 6.4: Cross Section of the Triple Well NMOS.

Guard rings are employed to isolate the sensitive analog circuits from the digital circuits and to further reduce the coupling in the substrate noise [8]. A guard ring is a continuous ring made of substrate ties that surrounds a sensitive circuit, providing a low-impedance path to the ground for the charge carriers produced in the substrate. With its large depth attributes, the n-well can also augment the operation of a guard ring by stopping the noise currents from flowing near the surface. Fig. 6.5 shows the layout of the guard ring while Fig. 6.6 provides a cross-sectional view.

Fig. 6.5: Layout of Guard Ring.

Fig. 6.6: Cross Section of Guard Ring.

6.2.3 Signal Lines Isolation

Finally, the attention has to be paid to the sensitive signals lines. The input of the frequency multiplier (X_{o1} and X_{o2}), the four clock phases generated from the PPF, the eight rail-to-rail clock edges generated by the VCDCs and the frequency multiplier output signal (f_{out}) are the most critical signals lines. This is mainly because they define the clock edges generated from the low jitter crystal oscillator for frequency multiplication. When noise couples into the signal lines, the output jitter performance of the frequency multiplier deteriorates and shielding is required to protect the signal lines. The left, right, top and bottom of the signal lines are shielded to prevent noise from coupling from nearby noisy signal lines as shown in Fig. 6.7. The shielding is grounded by a quiet ground line from the analog circuit itself. Meanwhile, digital circuit signals are prohibited from crossing or even going close to the signal line.

Fig. 6.7: Shielding of Sensitive Signal Line.

The microphotograph of the proposed frequency multiplier is fabricated using 0.13μm process technology and is illustrated in Fig. 6.8. The frequency multiplier

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including the bandgap and the biasing circuit occupies an area of 0.49mm^2 whilst consuming a power of 16.4mW at a 1.5V supply.

Fig. 6.8: Microphotograph of Proposed Frequency Multiplier.

Chapter 7

Results and Discussions

7.1 Introduction

The objective of this study is to achieve a low jitter frequency multiplier. Having implemented each sub-block of the multiplier, the next step in our effort is to examine the most critical performance parameter of the frequency multiplier we designed, namely its jitter performance. Because of the PEC's large and complicated feedback mechanism, direct jitter performance simulation by Cadence Spectre simulator will consume a lot of unrealistic time and processing resources. To ease the process of simulation, the frequency multiplier is partitioned into sub-blocks and the parameter of each is individually tested for its jitter performance by the Cadence Spectre simulator. Calculations are performed to predict the output jitter, and a MATLAB Simulink model is run for the PEC feedback system. The fabricated prototype is then set up for testing purposes. The measured jitter performance of the prototype is compared with the simulated jitter performance and both are discussed at length.

7.2 Jitter Simulation Results

Because of the complexity and bang-bang behavior of the PEC circuit, the PPF-based frequency multiplier is split into two parts in the jitter simulation. The first part is the open loop clock edge generation circuit, which consists of a PPF, VCDC and EC. The second part is a bang-bang closed loop calibration circuit (PEC). The current from the SCSS is set at 1 μ A at a steady-state, and so it can be assumed the noise contributed by the PEC is relatively small. The clock edge generation circuit is further assumed to be an open loop system driven by a periodic signal from the crystal oscillator. The jitter of the clock edge generation circuit is simulated using a periodic noise analysis conducted by the Cadence Spectre simulator as described in [96], [97]. The simulation results of the components in the clock edge generation circuit are shown in Table 7-1. The output random jitter ($\Delta t_{rj,OL}$) frequency multiplier is calculated at 1.46ps.

At this juncture, the periodic noise analysis of each component like the DVC delay chain, DVC charge pump, comparator and SCSS are simulated to predict the noise of the PEC output (the input of control voltage, V_c , of each VCDC) and the bang-bang feedback loop arising from each component. The results of this simulation are shown in Table 7-2. The simulated noise is then modeled by random noise sources with equal rms values. Each random noise source is then injected into the MATLAB Simulink model of the PEC circuit as shown in Fig. 7.1 for high level simulation purposes. The noise sources from each component are assumed to be uncorrelated and the results of the MATLAB Simulink simulation are shown in Fig. 7.2 and Table 7-3. These include the deterministic noise due to the bang-bang feedback loop described in

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Chapter 4.3.2 and random noise from PEC components such as the DVC, comparator, SCSS and VCDC.

TABLE 7-1: Periodic Noise Analysis Results of PPF, VCDC and EC (open loop).

	PPF	VCDC	EC	Total Phase Jitter
ϕ_{00}	$V_N=64.99\mu\text{V}$ $SR=72.81\text{MV/s}$ $\Delta t=0.89\text{ps}$	$V_N=7.56\text{mV}$ $SR=5.35\text{GV/s}$ $\Delta t=1.41\text{ps}$	$V_N=1.18\text{mV}$ $SR=26.09\text{GV/s}$ $\Delta t=0.045\text{ps}$	$\Delta t_0 = 1.67\text{ps}$
ϕ_{01}	$V_N=61.96\mu\text{V}$ $SR=100.57\text{MV/s}$ $\Delta t=0.62\text{ps}$	$V_N=7.27\text{mV}$ $SR=6.81\text{GV/s}$ $\Delta t=1.07\text{ps}$	$V_N=1.08\text{mV}$ $SR=26.10\text{GV/s}$ $\Delta t=0.041\text{ps}$	$\Delta t_1 = 1.24\text{ps}$
ϕ_{02}	$V_N=65.05\mu\text{V}$ $SR=75.47\text{MV/s}$ $\Delta t=0.86\text{ps}$	$V_N=7.53\text{mV}$ $SR=5.66\text{GV/s}$ $\Delta t=1.33\text{ps}$	$V_N=1.16\text{mV}$ $SR=25.78\text{GV/s}$ $\Delta t=0.045\text{ps}$	$\Delta t_2 = 1.58\text{ps}$
ϕ_{03}	$V_N=61.30\mu\text{V}$ $SR=99.18\text{MV/s}$ $\Delta t=0.62\text{ps}$	$V_N=7.13\text{mV}$ $SR=6.62\text{GV/s}$ $\Delta t=1.08\text{ps}$	$V_N=1.08\text{mV}$ $SR=26.07\text{GV/s}$ $\Delta t=0.041\text{ps}$	$\Delta t_3 = 1.25\text{ps}$
ϕ_{04}	$V_N=64.64\mu\text{V}$ $SR=72.23\text{MV/s}$ $\Delta t=0.90\text{ps}$	$V_N=7.36\text{mV}$ $SR=5.28\text{GV/s}$ $\Delta t=1.39\text{ps}$	$V_N=1.19\text{mV}$ $SR=26.08\text{GV/s}$ $\Delta t=0.046\text{ps}$	$\Delta t_4 = 1.66\text{ps}$
ϕ_{05}	$V_N=61.55\mu\text{V}$ $SR=97.74\text{MV/s}$ $\Delta t=0.63\text{ps}$	$V_N=7.08\text{mV}$ $SR=6.72\text{GV/s}$ $\Delta t=1.05\text{ps}$	$V_N=1.08\text{mV}$ $SR=25.77\text{GV/s}$ $\Delta t=0.042\text{ps}$	$\Delta t_5 = 1.23\text{ps}$
ϕ_{06}	$V_N=64.95\mu\text{V}$ $SR=74.78\text{MV/s}$ $\Delta t=0.87\text{ps}$	$V_N=7.24\text{mV}$ $SR=4.93\text{GV/s}$ $\Delta t=1.47\text{ps}$	$V_N=1.23\text{mV}$ $SR=26.09\text{GV/s}$ $\Delta t=0.047\text{ps}$	$\Delta t_6 = 1.71\text{ps}$
ϕ_{07}	$V_N=61.77\mu\text{V}$ $SR=98.51\text{MV/s}$ $\Delta t=0.63\text{ps}$	$V_N=7.18\text{mV}$ $SR=6.71\text{GV/s}$ $\Delta t=1.07\text{ps}$	$V_N=1.08\text{mV}$ $SR=25.88\text{GV/s}$ $\Delta t=0.042\text{ps}$	$\Delta t_7 = 1.24\text{ps}$
Total Output Jitter				$\Delta t_{rj,OL} = 1.46\text{ps}$

Note: V_N is output integrated noise in Vrms , SR is the output signal slew rate in V/s , Δt is the output jitter in ps rms .

TABLE 7-2: Periodic Noise Analysis Results of DVC, Comparator and SCSS.

DVC Delay Chain + Charge Pump	Output Integrated Noise = 373 μVrms
Comparator	Input Referred Noise = 190 μVrms
SCSS	Output Integrated Noise = 9.26 μVrms

Fig. 7.1: Simulink Model with Random Noise for PEC Circuit.

Fig. 7.1: MATLAB Simulink Model with Random Noise for PEC Circuit.

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Fig. 7.2: Control Voltage Noise due to PEC Components at Steady State.

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TABLE 7-3: Control Voltage Noise due to PEC Components at Steady State.

PEC Output	Vc Noise	ϕ_o Jitter (rms)
V_{c0}	0 μ Vrms	0ps
V_{c1}	257.6 μ Vrms	0.258ps
V_{c2}	370.9 μ Vrms	0.371ps
V_{c3}	417.2 μ Vrms	0.417ps
V_{c4}	430.4 μ Vrms	0.430ps
V_{c5}	409.3 μ Vrms	0.409ps
V_{c6}	380.1 μ Vrms	0.380ps
V_{c7}	322.7 μ Vrms	0.323ps
Total Output Jitter		$\Delta t_{rj,PEC} = 0.35ps$

From Table 7-1 and Table 7-3, the predicted random jitter due to the PPF, VCDC, EC and PEC is:

$$\begin{aligned}\Delta t_{rj, fout_pre} &= \sqrt{(\Delta t_{rj,OL})^2 + (\Delta t_{rj,PEC})^2} \\ &= \sqrt{(1.46)^2 + (0.35)^2} \text{ ps} \\ &= 1.50 \text{ ps}\end{aligned}\tag{7-1}$$

Meanwhile, the systematic mismatch in the clock edge can be calibrated by the PEC circuit as described in Chapter 4.3.2. The predicted deterministic jitter due to the clock edge mismatch is close to zero. However, in practical implementation, there exist some non-ideal effects due to imperfections in the circuits and in the IC environment. A single-ended biasing circuit and a reference voltage are employed to realize the proposed frequency multiplier. The control voltage, output of the VCDC and DVC are also single-ended circuits. These single-ended circuits are sensitive to

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the 25MHz that is coupled from the crystal oscillator through the supply and the substrate, which may not be considered a low frequency concern. The finite PSRR, the guard ring, the triple-well isolation and the decoupling capacitors cannot eliminate the coupling noise completely, and will cause some modulation in the biasing, the reference voltage, the VCDC control voltage, the VCDC output and DVC. A behavior model of the proposed frequency multiplier is developed to predict the effect of the 25MHz substrate noise on the performance of the PEC calibration, as well as to explain the discrepancy between what is expected in theory and the circuit's actual functioning. A 25MHz small-signal substrate bounce is injected into the frequency multiplier and the results of the static phase error due to the bounce arising from the 25MHz substrate is shown in Table 7-4 below.

TABLE 7-4: Static Phase Error due to 25MHz Substrate Bounce.

Delay Phase	Ideal Delay	Simulation Delay	Offset from Ideal
$\phi_{o0}-\phi_{o1}$	5.00000ns	4.99968ns	-0.32ps
$\phi_{o0}-\phi_{o2}$	10.00000ns	9.99957ns	-0.43ps
$\phi_{o0}-\phi_{o3}$	15.00000ns	14.99901ns	-0.99ps
$\phi_{o0}-\phi_{o4}$	20.00000ns	19.99816ns	-1.84ps
$\phi_{o0}-\phi_{o5}$	25.00000ns	24.99944ns	-0.56ps
$\phi_{o0}-\phi_{o6}$	30.00000ns	29.99950ns	-0.50ps
$\phi_{o0}-\phi_{o7}$	35.00000ns	34.99973ns	-0.27ps

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From the table above, it is clear that the 25MHz substrate bounce will affect the operation of the PEC circuit and cause a static phase error as large as 2ps. As a result, the predicted output deterministic jitter of the proposed frequency multiplier is:

$$\begin{aligned}
 \Delta t_{dj, fout_pre} &= \sqrt{\frac{(\varepsilon_{\phi 0})^2 + (\varepsilon_{\phi 1})^2 + (\varepsilon_{\phi 2})^2 + (\varepsilon_{\phi 3})^2 + (\varepsilon_{\phi 4})^2 + (\varepsilon_{\phi 5})^2 + (\varepsilon_{\phi 6})^2 + (\varepsilon_{\phi 7})^2}{8}} \\
 &= \sqrt{\frac{(0)^2 + (-0.3)^2 + (-0.4)^2 + (-1.0)^2 + (-1.8)^2 + (+0.6)^2 + (-0.5)^2 + (-0.3)^2}{8}} ps \\
 &= 0.81 ps
 \end{aligned} \tag{7-2}$$

where ε_{ϕ} is the static phase error of clock edges. Because the first clock edge (ϕ_{00}) is that of the reference clock used for calibration purpose, the static phase error of the first clock edge ($\varepsilon_{\phi 0}$) equals to zero. Hence, the overall predicted output jitter of the proposed frequency multiplier from the simulation, after taking the substrate bounce behavior model into account, is

$$\begin{aligned}
 \Delta t_{fout_pre} &= \sqrt{(\Delta t_{rj, fout_pre})^2 + (\Delta t_{dj, fout_pre})^2} \\
 &= \sqrt{(1.50)^2 + (0.81)^2} ps \\
 &= 1.70 ps
 \end{aligned} \tag{7-3}$$

The predicted jitter is within the minimum requirements for an effective 8-bit 200Msps ADC based on [6] and [65], which is 5.1ps rms.

7.3 Test Setup

The design and fabrication of the proposed frequency multiplier prototype is followed by its performance characterization. The key performance measures of the prototype are the jitter and static phase errors of the multiplied output frequency. Fig. 7.3 shows a prototype PCB that was fabricated for the measurement of the chip. The die of the prototype was packaged inside an LPCC package, while an Abracon 25MHz crystal and two 30pF capacitors were used to integrate it with the on-chip oscillator to provide a clean reference clock. The measurement setup is shown in Fig. 7.4. An Agilent E3631A power supply provided a clean power for the DUT. The jitter and phase error of the measurement was taken by an Agilent Infiniium 54855A oscilloscope.

Fig. 7.3: Prototype PCB for the Prototype Measurement.

Fig. 7.4: Measurement Setup.

7.4 Jitter Measurement Results

A 25MHz sinusoidal reference frequency is generated from an internal on-chip oscillator with an external crystal. Given a multiplication ratio of eight, the output frequency is 200MHz and the prototype can generate an output frequency range of between 136MHz to 280MHz with a reference frequency of between 17MHz and 35MHz. The measured output time interval error (TIE) of the jitter histogram at 200MHz is shown in Fig. 7.5. The rms and peak-to-peak TIE jitter are 2.46ps and 18.65ps respectively. The normalized jitter in this work is 0.049% at 200MHz.

Fig. 7.5: Measured Jitter Performance of Proposed Frequency Multiplier.

Phase Error Calibration Performance Results

7.5 Phase Error Calibration Performance Results

The DUT needs to be synchronized by a crystal reference clock in order to measure the phase error generated by the clock edges at output frequency (f_o). The delay of each clock edge at output frequency (f_o) can be measured after the reference clock is implemented as a synchronized clock for the oscilloscope and the phase error of each clock edge can be calculated against the edges of the ideal clock. The results of the measurements are shown in Table 7-5.

TABLE 7-5: Static Phase Error Before and After Calibration.

Delay Phase	Ideal Delay	Before Calibration		After Calibration	
		Measurement	Offset	Measurement	Offset
$\phi_{o0}-\phi_{o1}$	5.0000ns	4.8018ns	-198.2ps	4.9977ns	-2.3ps
$\phi_{o0}-\phi_{o2}$	10.0000ns	9.9610ns	-39.0ps	9.9978ns	-2.2ps
$\phi_{o0}-\phi_{o3}$	15.0000ns	14.8095ns	-190.5ps	14.9982ns	-1.8ps
$\phi_{o0}-\phi_{o4}$	20.0000ns	19.8872ns	-112.8ps	19.9988ns	-1.2ps
$\phi_{o0}-\phi_{o5}$	25.0000ns	24.9216ns	-78.4ps	25.0024ns	+2.4ps
$\phi_{o0}-\phi_{o6}$	30.0000ns	30.0254ns	+25.4ps	29.9982ns	-1.8ps
$\phi_{o0}-\phi_{o7}$	35.0000ns	34.8416ns	-158.4ps	34.9979ns	-2.1ps

Phase Error Calibration Performance Results

The measured output deterministic jitter of the frequency multiplier due to the static phase error on each clock edge can be calculated as follows

$$\begin{aligned}
 \Delta t_{dj, fout_mea} &= \sqrt{\frac{(\varepsilon_{\phi 0})^2 + (\varepsilon_{\phi 1})^2 + (\varepsilon_{\phi 2})^2 + (\varepsilon_{\phi 3})^2 + (\varepsilon_{\phi 4})^2 + (\varepsilon_{\phi 5})^2 + (\varepsilon_{\phi 6})^2 + (\varepsilon_{\phi 7})^2}{8}} \\
 &= \sqrt{\frac{(0)^2 + (-2.3)^2 + (-2.2)^2 + (-1.8)^2 + (-1.2)^2 + (+2.4)^2 + (-1.8)^2 + (-2.1)^2}{8}} ps \\
 &= 1.88 ps
 \end{aligned}
 \tag{7-4}$$

where ε_{ϕ} is the static phase error of the clock edges. Again, because the first clock edge (ϕ_{00}) serves as a reference for calibration purposes, the static phase error of the first clock edge ($\varepsilon_{\phi 0}$) equals to zero.

Comparison of Simulated and Measured Jitter

7.6 Comparison of Simulated and Measured Jitter

From Chapter 7.2, the predicted random output jitter, deterministic output jitter and overall output jitter of the proposed frequency multiplier from the simulation models are

$$\Delta t_{rj, f_{out_pre}} = 1.50 ps \quad (7-5)$$

$$\Delta t_{dj, f_{out_pre}} = 0.81 ps \quad (7-6)$$

$$\Delta t_{f_{out_pre}} = 1.70 ps \quad (7-7)$$

From Chapter 7.3, the measured random output jitter, deterministic output jitter and overall output jitter of the proposed frequency multiplier are

$$\Delta t_{rj, f_{out_mea}} = 1.59 ps \quad (7-8)$$

$$\Delta t_{dj, f_{out_mea}} = 1.88 ps \quad (7-9)$$

$$\Delta t_{f_{out_mea}} = 2.46 ps \quad (7-10)$$

The measured random output jitter is calculated based on the measured deterministic output jitter and the overall output jitter, after assuming that both random and deterministic jitter is uncorrelated.

$$\begin{aligned} \Delta t_{rj, f_{out_mea}} &= \sqrt{(\Delta t_{f_{out_mea}})^2 - (\Delta t_{dj, f_{out_mea}})^2} \\ &= \sqrt{(2.46)^2 - (1.88)^2} ps \\ &= 1.59 ps \end{aligned} \quad (7-11)$$

Comparison of Simulated and Measured Jitter

The random output jitter that is predicted is very close to the measured output jitter, which is 1.59ps. Measurement results show a level of uncorrelated random noise that differs from the predicted value by 0.53ps. The excess uncorrelated random noise is calculated as follows

$$\begin{aligned}
 \Delta t_{rj, fout_exc} &= \sqrt{(\Delta t_{fout_mea})^2 - (\Delta t_{dj, fout_pre})^2} \\
 &= \sqrt{(1.59)^2 - (1.50)^2} \text{ ps} \\
 &= 0.53 \text{ ps}
 \end{aligned} \tag{7-12}$$

This excessive random noise can be attributed by the crystal oscillator, power supply and substrate that exist in the practical environment.

We note however, that the predicted deterministic output jitter is somewhat under-estimated from the measurement results. This is mainly because of the limitations related to the prediction of substrate bounce at the different components located in different parts of the chip, as well as shielding errors in the current layout. For instance, in the comparator layout, there is a portion of the sensitive signal line that is not shielded properly. This line (V_T) runs in parallel with the high switching clock signal of the comparator (CK_{comp}) for a length of around 40 μm and a spacing of around 1 μm to form a coupling capacitor between the lines. The CK_{comp} clock signal line will couple the switching noise to the V_T , and the signal line will define the delay of each clock edge as measured by the DVC. A behavioral model of the proposed frequency multiplier is developed to predict the effect of the coupling noise. The static phase errors arising from the coupling noise are shown in Table 7-6 below.

Comparison of Simulated and Measured Jitter

TABLE 7-6: Static Phase Error due to Coupling Noise.

Delay Phase	Ideal Delay	Simulation Delay	Offset from Ideal
$\phi_{o0}-\phi_{o1}$	5.0000ns	4.99981ns	-0.19ps
$\phi_{o0}-\phi_{o2}$	10.0000ns	10.00002ns	0.02ps
$\phi_{o0}-\phi_{o3}$	15.0000ns	15.00019ns	+0.19ps
$\phi_{o0}-\phi_{o4}$	20.0000ns	20.00067ns	+0.67ps
$\phi_{o0}-\phi_{o5}$	25.0000ns	25.00110ns	+1.10ps
$\phi_{o0}-\phi_{o6}$	30.0000ns	30.00110ns	+1.10ps
$\phi_{o0}-\phi_{o7}$	35.0000ns	35.00070ns	+0.70ps

Thus, the predicted output deterministic jitter of the proposed frequency multiplier due to the coupling noise from CK_{comp} is:

$$\begin{aligned}\Delta t_{dj, fout_coup} &= \sqrt{\frac{(\varepsilon_{\phi 0})^2 + (\varepsilon_{\phi 1})^2 + (\varepsilon_{\phi 2})^2 + (\varepsilon_{\phi 3})^2 + (\varepsilon_{\phi 4})^2 + (\varepsilon_{\phi 5})^2 + (\varepsilon_{\phi 6})^2 + (\varepsilon_{\phi 7})^2}{8}} \\ &= \sqrt{\frac{(0)^2 + (-0.2)^2 + (0.0)^2 + (+0.2)^2 + (+0.7)^2 + (+1.1)^2 + (+1.1)^2 + (+0.7)^2}{8}} ps \\ &= 0.66 ps\end{aligned}\tag{7-13}$$

where ε_{ϕ} is the static phase error of clock edges. Because the first clock edge (ϕ_{o0}) serves as a reference for calibration purpose, the static phase error of the first clock edge ($\varepsilon_{\phi 0}$) equals to zero.

7.7 Performance Comparisons

A summary of the prototype measurements and other related information is provided in Table 7-7.

TABLE 7-7: Summary of Frequency Multiplier Prototype

Process	CMOS 0.13μm
Supply	1.5V
Power Consumption	16.4 mW
Area	0.49 mm ²
Input Frequency	25 MHz
Output Frequency	200 MHz
Operating Frequency Range	136 MHz -280 MHz
Phase Error Reduction Method	Analog Calibration
Rms Output Jitter	2.46 ps rms
Peak-to-peak Output Jitter	18.65 ps peak-to-peak
Maximum Phase Error	2.4 ps
Settling Time	12.56μs

Performance Comparisons

The current consumption of each block in the frequency multiplier is summarized in Table 7-8. The PEC digital circuit consumes a greater current level than other components of the frequency multiplier as the calibration of each clock edge is done in every period of output frequency 200MHz, which is not an optimum level for current consumption. The current consumption can be reduced if the calibration is designed instead to occur at every period of a 25MHz reference clock. The trade off for this lower level is a longer settling time for the frequency multiplier.

TABLE 7-8: Current Consumption of Each Block in Frequency Multiplier

Block	Current Consumption
Crystal Oscillator	0.38 mA
BandGap and Biasing Circuit	1.00 mA
Voltage-Controlled Delay Cell	1.60 mA
Edge Combiner	0.48 mA
Phase Error Calibration	3.48 mA (analog circuit) 3.99 mA (digital circuit)
Total Current Consumption	10.93 mA

Performance Comparisons

Fig. 7.6 shows the normalized rms jitter performance metrics [13], [14], [23] that are used to compare different types of frequency multipliers with output frequencies ranging from 50MHz to 1.3GHz in the reported works. At 200MHz, the normalized rms jitter of the design proposed in this study is 0.049% which is the lowest of all other frequency multipliers with nearby frequencies. The second lowest jitter is achieved by [11], which employs a PLL with an optimized loop bandwidth.

The performance of the calibration circuit used in our new study is also compared to that of others in Table 7-9. At 2.4ps, our circuit achieves the smallest phase error of all compared designs after calibration. This work and [98] employs an analog calibration technique to minimize the phase error at the same operating frequency. However, the phase error achieved in this work is three times better than [98]. It also achieves lower current consumption over a reasonable area after taking into account of the different processes used. Another attempt to design a suitable multiplier was made by [99] who employed a digital calibration technique, but the current design far outperforms their phase error of 3.5ps.

Performance Comparisons

Fig. 7.6: Normalized Jitter of Frequency Multiplier.

Performance Comparisons

TABLE 7-9: Performance Comparison of Calibration Circuit.

Reference	[98]	[99]	[100]	This work
Process	0.25um	0.18um	0.18um	0.13um
Supply	2.5V	1.8V	1.8V	1.5V
Power	80mW	81mW	12mW	16.4mW
Area	1.6mm ²	1.03mm ²	0.05mm ²	0.49mm ²
Application	DLL-based Multi-phase clock @250MHz	DLL-based Multi-phase clock @2GHz	MDLL-based Frequency Multiplier @2GHz	PPF-based Frequency Multiplier @200MHz
Phase Error Reduction Method	Analog Calibration	Digital Calibration	Circuit Technique	Analog Calibration
Maximum Phase Error	7.1ps	3.5ps	5.0ps*	2.4ps

* Simulated Result

7.8 Limitations

We have previously discussed the improvements made in the proposed frequency multiplier over its more conventional counterparts. The measurement results from the fabricated prototype confirm the superiority of the proposed design. Nonetheless, there remain several limitations in the practical implementation of the design due to imperfections in the circuits and IC environment.

First, the proposed frequency multiplier has a better normalized rms jitter at lower frequency ranges of 500MHz and below as the random jitter due to the delay cells in the PLL or DLL can be reduced by using the PPF. From equation (7-8) and (7-9), it is apparent that the deterministic jitter due to the static phase error of the PEC is comparable to the random jitter of the PPF and VCDC. However, when the proposed frequency multiplier is designed for higher frequency ranges upward of 1GHz, equation (4-30) predicts that the random jitter of PPF will be reduced. The static phase error will not be reduced by reducing the period of the output clock when the output frequency is increased. This is because the static phase error of the PEC is independent of the output frequency of the frequency multiplier. As mentioned in Chapter 7.2, the static phase error of the PEC is affected mainly by substrate noise coupled from the crystal oscillator. Thus, the deterministic jitter arising from the static phase error of the PEC becomes the dominant noise source in the circuit and improvements in the jitter from random noise arising from the replacement of the PPF are insignificant at higher frequency ranges.

Second, the architecture of the PPF dictates that its reference frequency be determined by the values of the resistor and capacitor and the resistor and capacitor values have to be fixed in the early stage of design in order for the reference frequency of the PPF to be known. However, the reference frequency cannot be

Limitations

changed after implementation as it limits the operation of the frequency multiplier to a restricted range of frequencies. Thus, as listed in Table 7-7, the frequency multiplier is only able to operate in the 136MHz to 280MHz range, which is a -32% to 40% variation on the typical frequency of 200MHz.

Lastly, the 90° phase shift of the PPF output clock means that the achievable multiplication factor of the proposed frequency multiplier is a factor of 4 (4, 8, 16 etc). It is impossible for the frequency multiplier to have other multiplication factors or to be changed after the implementation of the design. This is not the case in the PLL in which the multiplication factor can be easily changed by changing the value of the divider.

These limitations make it clear that there remains some room for improvement in the design of the frequency multiplier proposed in this study. The research necessary to facilitate such improvements will be discussed in Chapter 8.2.

Chapter 8

Conclusions and Recommendations

8.1 Conclusions

An analysis was conducted of the random and deterministic jitter of both conventional frequency multiplier designs as well as that of a novel design proposed in this study. The analysis revealed that the conventional frequency multiplier design that uses PLL and DLL may not be optimum for minimizing jitter performance. The conventional PLL causes random jitter to accumulate from one cycle to another, causing the performance to be even poorer than that of conventional DLL designs. Although the conventional DLL does not accumulate random jitter from one cycle to another, the delay chain architecture in the DLL still accumulates random jitter from the first to last delay cell. Noise from devices associated with the MOS transistors in the delay cell, including the MOS thermal noise and flicker noise also contribute significant levels of random jitter at the output clock. This prevents the optimization of the jitter performance of the conventional DLL. Mismatches among the delay cell, the current source of the charge pump and the sink also contributes deterministic jitter to the output clock.

A new design concept is proposed in this thesis which involves the use of a passive *RC* polyphase filter to replace the delay chain in the DLL. The polyphase filter eliminates the cascading structure of the delay chain in the DLL. Because it consists only of resistors and capacitors, the main noise source is the thermal noise from the resistors. The noise contributed by the resistor is much lower than that

Conclusions

contributed by the MOS transistor, thus allowing for better random jitter performance. The phase error due to the mismatch in the devices can be minimized by applying the phase error calibration circuit, thus improving the overall jitter performance.

An analytical model was developed for the proposed frequency multiplier and the random jitter it generated was compared with that of the conventional DLL. The jitter analysis shows that the polyphase filter-based frequency multiplier has a better random jitter performance than the conventional DLL.

A 200MHz frequency multiplier targeted for use with a minimum of an 8-bit 200Msps ADC was designed and simulated with a multiplication ratio of eight in order to verify the effectiveness of the techniques and architecture employed in the circuit. The jitter performance of the frequency multiplier has also been predicted from the proposed behavior simulation models.

Finally, the fabricated IC prototype was evaluated by way of experiment. The measured random jitter of the fabricated frequency multiplier was found to be very close to that of randomly generated jitter. The measured deterministic jitter is a bit higher than that predicted by the simulation conducted using the behavior model, but better results can be expected through improvements a number of areas, including in the behavior models used for jitter verification and in the circuit and layout techniques employed in our PPF frequency multiplier IC prototype.

8.2 Recommendations for Further Research

This is the first reported attempt to use PPF as a means of constructing a frequency multipliers. Results of the implementation of the first-ever silicon prototype of this design demonstrates that the circuit architecture has great potential for future application, as well as a room for further improvement.

One of the improvements that can be made is in the multiplier's phase error performance as the deterministic jitter arising from the static phase error on every clock edge contributes a significant level of jitter to the total. The PEC phase errors recorded in this study are as large as 2.4ps, and the static phase error contributes a deterministic jitter of 1.88ps rms toward the device's total output jitter of 2.46ps. Predictions from the behavioral model simulation show that the substrate bounce will contribute a significant portion of the total static phase error. It is therefore necessary for a more sophisticated behavior substrate bounce model to be developed that can allow for accurate prediction of the simulated deterministic jitter. The limitation of proposed architecture in higher frequency ranges arising from the static phase error is discussed in Chapter 7.8, and reducing the static phase error of the PEC will not only further improve the jitter performance of the proposed design, it will also increase the potential of the proposed architecture to be used in a higher frequency range. A differential topology can be employed in the biasing circuit, voltage reference circuit, the control voltage of VCDC and DVC to improve the substrate and supply noise rejection level of the critical circuits. This is also essential if the circuit is slated for usage at even higher frequencies.

A proper shielding is necessary for the critical signal, V_T , to prevent unwanted noise coupling from the clock signal CK_{comp} . The behavior model simulation demonstrates that the coupling noise feeding into V_T indeed contributes a significant

Recommendations for Further Research

static phase error to the clock edges after calibration. By minimizing the static phase error, the total output jitter of the proposed frequency multiplier can be further improved to be as good as 1.57ps rms.

From Table 7-8, it is clear that the largest proportion of the frequency multiplier's current consumption can be attributed to the PEC's digital circuit. This is because each clock edge is calibrated at every period of output frequency 200MHz, which presents a limited time of 5ns within which the PEC has to complete its task. This requires that it be designed for a high rising and falling time, and that the digital circuit will consume a relatively higher amount of transition current. As the current consumption of the PEC digital circuit is not yet optimized for this first-cut design, a worthy project for future undertaking is that of designing the calibration cycle to be done in every 25MHz period of the reference clock. A lower rising and falling time can be achieved by relaxing the period of the calibration cycle. This will also serve to reduce the current consumption of the PEC digital circuit. The only trade off for this is that a longer locking time is necessary for the frequency multiplier because of the longer time needed for calibration. In most applications, this longer locking time is allowed in the system start up or initial state.

On another note, given that the multiplication factor of the current design is eight, a PPF technique employing a higher multiplication factor should certainly be investigated which will improve the flexibility of the multiplication factor. Similarly, although the current frequency multiplier is designed for use at 200MHz ADC, a higher frequency level, specifically one above 1GHz should be explored for use in the RF transceiver in order to improve on the phase noise in RF wireless applications.

Author's Publications

- [1] J. K. Yin and P. K. Chan, "A low-jitter polyphase-filter-based frequency multiplier with phase error calibration," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 7, pp. 663-667, Jul. 2008.
- [2] J. K. Yin and P. K. Chan, "Analysis of Polyphase Filter Based Multiphase Clock in Frequency Multiplier," is under review by *IEEE Transactions on Circuits & Systems, Part I*.

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