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Study of SiC Oxidation for Device Application

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Summary

Silicon carbide (SiC) is a wide bandgap semiconductor that exhibits many excellent electrical properties such as high critical field strength and thermal conductivity. As a result, it has attracted a lot of attention for high temperature, high power and high frequency device applications. In addition, SiC can be thermally oxidized to form silicon dioxide (SiO_2), which is a critical building block of silicon complimentary metal-oxide-semiconductor (MOS) technology. This means that Si CMOS processes can be possibly transferred directly to SiC based CMOS devices. This renders SiC very attractive and offers many great advantages compared to other wide bandgap semiconductors such as gallium nitride (GaN). The development of SiC device applications is further propelled by the fact that high quality 4-inch 4H-SiC substrates are commercially available.

To realize SiC based MOS devices, a high quality SiC/ SiO_2 interface is necessary, as in the case of Si based MOS technology. However, at present the SiC/ SiO_2 interface is still too defective for device application. The interface states density (D_{it}) and the oxide fixed charge (Q_{ox}) of SiC MOS structure are about two orders higher than those of Si MOS structure. This project aims to investigate the oxidation process of N-type 4H-SiC, such as oxidation temperature and annealing ambient, and their effects on the interface states density and oxide fixed charge. Thermally grown SiO_2 is examined as gate dielectric on N-type 4H-SiC by x-ray photoelectron spectroscopy (XPS), ellipsometry and capacitance-voltage (C-V) measurements. From XPS, it is found that C-C bonds only exist at the SiO_2 /SiC interface, whereas SiO_xC_y and Si-C bonds are only found in the

SiO₂. At points further away from the interface and into the SiO₂, there are more SiO_xC_y bonds relative to Si-C bonds. This result can be attributed to the dynamic oxidation process that transforms Si-C bonds into SiO_xC_y bonds, which are then further oxidized to form SiO₂ bonds. Ellipsometry is used to investigate the optical constants of thermal SiO₂ on 4H-SiC. It is found that there exists a transition layer between SiO₂ and 4H-SiC, which has a higher optical constant than pure SiO₂. The thermal oxidation temperature can influence the composition of the transition layer, especially the SiC volume fraction. Higher oxidation temperature has resulted in a lower SiC volume fraction. Nitridation of the thermal SiO₂ using N₂O at different temperatures was also studied. Over the temperature range from 950 °C to 1150 °C, it is found that nitridation at 1050 °C gives relatively the lowest interface state density. The trap cross section constant was also investigated by AC conductance method. Higher temperature nitridation is found to result in smaller capture cross-section.

Apart from thermal SiO₂ on 4H-SiC, other dielectrics such as silicon nitride (SiN_x), tantalum pentoxide (Ta₂O₅) and aluminum nitride (AlN) were also investigated. SiN_x deposited by plasma enhanced chemical vapor deposition (PECVD) was optimized and deposited on 4H-SiC to form MIS structures. It is found that the interface state density for the sample annealed at 700 °C for 30mins is comparable with that obtained for thermal SiO₂. High-k Ta₂O₅ dielectrics were deposited by the pulsed DC magnetron sputtering technique. Due to the smaller band offset between Ta₂O₅ and 4H-SiC, a dielectric stack of Ta₂O₅ and thermal SiO₂ was formed for the 4H-SiC MIS structure. Upon high temperature annealing, the breakdown field in the dielectric stack is found to be higher

than pure thermal SiO_2 . AlN was deposited using the radio frequency magnetron sputtering technique. Deep-level-transient spectroscopy (DLTS) was used to evaluate the deep energy traps in the AlN deposited on 4H-SiC and Si. The defect densities of AlN are lower when grown on 4H-SiC substrates than on Si substrates. Defects located at 0.35 - 0.42 eV below the conduction band, attributed to dangling bonds of nitrogen atoms, are seen in samples grown with higher nitrogen flow rate. Shallow level defects, observed at approximately 0.1 eV below the conduction band, can be attributed to the recently discovered prismatic stacking fault in the AlN atomic structure.

Following the studies on 4H-SiC MOS and MIS structures, depletion-mode metal oxide semiconductor field effect transistors (MOSFETs) using SiO_2 as the gate dielectric were successfully fabricated and characterized. By applying different gate voltages, this device can operate in the depletion mode or accumulation mode. The drain current versus drain voltage ($I_{DS} - V_{DS}$) relation in the accumulation range is similar to the traditional enhancement-mode MOSFETs except that the threshold voltage (V_{TH}) is replaced with the flat-band voltage (V_{FB}). The effective electron field mobility in the accumulation layer has been determined under different gate voltages in the accumulation mode, and it is found to be around $17 \text{ cm}^2/\text{Vs}$. The result is comparable with that of inversion layer in enhancement-mode MOSFETs, and the lower mobility is attributed to the low quality interface between SiO_2 and 4H-SiC. The electron mobility in the physical channel is also deduced in the accumulation region and it is found to be around $110.5 \text{ cm}^2/\text{Vs}$.

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Chapter 1 Introduction

1.1 Motivation

Silicon Carbide (SiC) is a wide bandgap semiconductor that has been intensively investigated in recent years due to its various advantages [1, 2]: (1) the saturated electron velocity (2.0×10^7 cm/s) is two times higher than that of silicon (Si), (2) the critical electric field (3.0 MV/cm) is 10 times higher than that of Si and (3) the thermal conductivity (5.0 W/cm K) is around 3 times higher than that of Si. Due to these excellent physical properties, SiC based semiconductor electronic devices and circuits are being actively researched and developed for use in high temperature, high power and high radiation conditions where conventional semiconductors cannot perform adequately. This research into SiC is also propelled by the progress made in the manufacture of SiC wafers, where larger wafers with lower defect density and at lower cost are readily available.

In addition to the above advantages, SiC can be oxidized to form silicon dioxide (SiO₂), which is a well-established dielectric widely used in Si complimentary metal-oxide-semiconductor (CMOS) technology. Therefore, it is possible to fabricate all the devices found in Si integrated circuit technology using SiC. The success of SiC MOS technology critically depends on achieving a high quality SiO₂/SiC interface. Though the native oxide of SiC is SiO₂, the SiO₂/SiC interface quality has been found to be far from ideal, exhibiting high defect density and consequently leading to unacceptably low channel mobility for SiC metal-oxide-semiconductor field effect transistor (MOSFET) [3]. A lot of effort has been devoted in the recent years towards investigating the physical reasons for the high interface states density and how the interface quality can be improved.

Several methods have been proposed, such as nitric oxide annealing [4] and hydrogen post-oxidation annealing [5]. However, up to date the interface of SiO₂/SiC is still too defective for device application. The interface states density (D_{it}) is still in the range of $1 \times 10^{11} \sim 1 \times 10^{12} / \text{cm}^2 \text{ eV}$, which is around two orders of magnitude higher compared to SiO₂/Si interface. Thus, to fully exploit the potential of SiC, further studies are needed to investigate the cause of the low SiO₂/SiC interface quality and develop new processes to lower the interface states density and oxide fixed charge for thermally grown SiO₂ on SiC. Besides thermal SiO₂, it would be interesting to explore others dielectrics with higher dielectric constants to be used as the gate dielectric for SiC MOSFETs. In addition, since the interface of SiO₂/SiC is defective, devices with novel structures that are not affected by the interface quality should also be considered in the effort towards realizing high performance SiC devices.

1.2 Objectives

The objectives and scope of this project are summarized as follows:

1. We aimed to investigate the interface quality of SiO₂/SiC and explore how it can be improved. Among the most extensively investigated SiC polytypes for electronic applications, namely the 3C, 4H and 6H polytypes, 4H-SiC is the most promising due to its significantly larger electron mobility and its reduced anisotropy. Therefore, in this work, 4H-SiC will be studied. N-type 4H-SiC will be oxidized at different temperatures from 950°C to 1150°C. Post-annealing of the oxidized samples in diluted nitrous oxide (N₂O) will be carried out from 900°C to 1100°C. This study serves to investigate the effects of growth temperature and annealing temperature on

the properties of the $\text{SiO}_2/\text{4H-SiC}$ interface. A number of characterization tools will be employed to study the $\text{SiO}_2/\text{4H-SiC}$ interface. X-ray Photoelectron Spectroscopy (XPS) will be used to examine the carbon related bonding configuration in the thermal SiO_2 . Ellipsometry will be employed to investigate the optical properties of the thermal SiO_2 , with the interface composition modeled by the effective medium approximation (EMA). Terman's method and AC conductance method will be used to extract the interface states density under different oxidation conditions. Furthermore, the trap cross section will also be investigated using the AC conductance method.

2. Apart from thermal SiO_2 , other dielectric materials which include SiN_x , Ta_2O_5 , AlN will also be examined as potential gate dielectrics for 4H-SiC. These dielectrics will be investigated using a structure of metal-insulator-semiconductor (MIS) capacitors. Different annealing conditions will be applied to study their effects on the interface states.
3. Due to the poor interface quality of $\text{SiO}_2/\text{4H-SiC}$, a new MOSFET structure, an accumulation mode 4H-SiC MOSFET, whose performance is less dependent on the quality of the $\text{SiO}_2/\text{4H-SiC}$ interface will be studied. The work involves the design, fabrication and characterization of the accumulation mode 4H-SiC MOSFET devices. Based on the electrical characteristics of the devices, a model will be developed to deduce the device parameters such as channel mobility and accumulation layer mobility, and evaluate its channel depth and channel doping concentration.

1.3 Major Contribution of the Thesis

The contributions in this research work are summarized as follows:

1. A thorough physical analysis has been carried out for thermal SiO_2 grown on 4H-SiC. Carbon related bonding distribution has been investigated. By analyzing the C1s core level spectra of x-ray photoelectron, it has been found that C-C bonds only exist at the SiO_2 /4H-SiC interface. Whereas in the thermal SiO_2 , only SiC_xO_y and Si-C bonds are observed. Further away from the interface into the SiO_2 , there are more SiO_xC_y bonds relative to Si-C bonds. This result can be attributed to the dynamic oxidation process that transforms Si-C bonds into SiO_xC_y bonds, which are further oxidized to form SiO_2 bonds and CO. This process occurs both at the interface and in the bulk of the SiO_2 . This observation suggests that the carbon components in the SiO_2 may be minimized by re-oxidation at lower temperature over an extended period of time, which is helpful toward eliminating the carbon in the SiO_2 and preventing further oxidation of the 4H-SiC substrate.
2. Through ellipsometry studies, it is found that there exists an interface layer between 4H-SiC and SiO_2 , and the interface quality is related to the refractive index of this interface transition layer. It was found that, in the investigated oxidation temperature range from 950°C to 1150°C, the interface is further oxidized and has less carbon related component at high oxidation temperature, which means that its quality is better. This observation is consistent with the results of electrical measurements which show that higher oxidation temperature will result in lower interface states density.

3. Other dielectrics such as SiN_x , Ta_2O_5 , and AlN were investigated as gate dielectrics for 4H-SiC MIS structure. SiN_x deposited by plasma enhanced chemical vapor deposition (PECVD) was found to have the lower interface state density as thermal SiO_2 on 4H-SiC after post-deposition annealing at 700 °C for 30 minutes near 4H-SiC conduction edge. Due to the smaller bandgap and band offset with 4H-SiC, Ta_2O_5 was stacked with a thin layer of thermal SiO_2 to form 4H-SiC MIS structure. It was found that the leakage current of $\text{SiO}_2/\text{Ta}_2\text{O}_5$ is quite low even under high electrical field stress. The defect density of AlN grown by RF magnetron sputtering on Si and 4H-SiC wafers have been studied by the deep-level-transient spectroscopy (DLTS). It is found that the defect densities in AlN are generally lower when deposited on 4H-SiC than on Si. Defining the conduction band edge as E_c , the defect peaks observed in our result at $E_c - E = 0.18 - 0.22$ eV, $0.47 - 0.62$ eV and $0.73 - 0.80$ eV have been identified as levels of the nitrogen vacancy triplet, whereas the peaks at $E_c - E = 0.35 - 0.42$ eV are associated with DX-like centres, formed with the involvement of Si atoms in the AlN layers grown on Si. A broad defect peak at $E_c - E = 0.15 - 0.45$ eV in nitrogen-rich layers grown on 4H-SiC could originate from dangling bonds of nitrogen atoms.
4. Accumulation mode 4H-SiC MOSFETs have been designed, fabricated and characterized. The electron accumulation layer mobility deduced of $17.5 \text{ cm}^2/\text{Vs}$ is similar to the electron mobility reported for enhancement-mode 4H-SiC MOSFET. The rather low electron accumulation layer mobility is attributed to the poor interface quality, as what has been found in enhancement-mode 4H-SiC based MOSFETs by

other researchers [6]. A simple drain current model has been developed for our enhancement-mode 4H-SiC based MOSFETs. The physical channel mobility and the channel doping concentration have also been evaluated. The channel doping concentration has been found to be consistent with the result obtained from secondary ion mass spectrometry (SIMS) after considering the ionization rate of 4H-SiC at room temperature.

1.4 Organization of the Thesis

In Chapter one of this thesis, a brief introduction to SiC and the problems facing SiC technology development are discussed. The motivation and the objectives of this study are also presented. In Chapter two, a literature review of the properties of SiC is presented and the published results on SiC oxidation are reviewed. In Chapter three, the material and electrical characterization techniques used to study the SiO₂/4H-SiC interface in this work are introduced and reviewed. In Chapter four, the results of thermal SiO₂ grown on 4H-SiC are presented. The effects of the nitridation temperature on the interface traps are discussed. In Chapter five, the results of other dielectrics, namely SiN_x, Ta₂O₅ and AlN, grown on 4H-SiC to form MIS structure are presented. In Chapter six, depletion mode SiC MOSFETs are designed, fabricated and characterized. The accumulation layer mobility and bulk channel mobility extracted from the DC current-voltage measurements are presented. A summary of the work carried out in this project as well as the conclusions and recommendations for future research are presented in Chapter seven.

Chapter 2 Physical Properties of Silicon Carbide

2.1 Introduction

Human beings entered the era of solid-state electronics in 1947, the year that the first transistor was demonstrated by John Bardeen, Walter Brattain and William Shockley [7]. At the very beginning, there were several candidates, silicon (Si), silicon carbide (SiC) and germanium (Ge) that were considered as the semiconductor material for the great solid-state electronics era. Ge was chosen as the early solid-state device substrate, because it was relatively simple to produce single crystal Ge. Si has more desirable physical properties such as a larger bandgap and a more stable natural oxide. Although Si was difficult to manufacture due to its higher melting temperature, it ultimately replaced Ge and the rate of development of Si devices was phenomenal once those early problems were resolved.

Today, nearly sixty years after the invention of the first transistor, Si and SiO₂ are still the mainstream semiconductor and dielectric respectively used in solid-state electronics. However, there are certain applications under extreme conditions, such as high temperature and high power, which require semiconductors with physical properties that are beyond what Si can offer. This role can be nicely fulfilled by silicon carbide (SiC), a wide bandgap semiconductor, due to its excellent physical and electrical properties. In this chapter, the physical properties of SiC will be reviewed. The crystal structure of SiC will be introduced first, followed by other physical properties of SiC, such as bandgap, critical field, saturation drift velocity, thermal conductivity, and the figures of merit. The

oxidation of SiC will then be reviewed. The kinetics of SiC oxidation will be discussed, accompanied by a review of the methods available to improve the quality of thermal silicon dioxide (SiO₂) grown on SiC. In addition, alternative gate dielectrics on SiC will be presented.

2.2 Properties of Silicon Carbide

2.2.1 Crystal Structure and Polytypes of SiC

It is well known that the conventional semiconductor Si, which is widely used in modern very-large-scale integrated (VLSI) circuit technology, has a diamond crystal structure. Unlike Si, SiC occurs in the so called Zinc-Blende or Sphalerite structure [1]. SiC comprises two elements, silicon and carbon, both of which belong to group IV in the periodic table. Si and C are bonded covalently in SiC and the chemical composition is 50% for each element. This means that each Si atom has four nearest neighboring C atoms, and likewise each C atom has four nearest neighboring Si atoms. Thus, the basic structure of SiC is tetragonal with either C atom situated at the center of mass outlined by four neighboring Si atoms or Si atom situated at the center of mass outlined by four neighboring C atoms. Figure 2.1 shows the basic structure of a SiC bond. The distance between the C atom and each of the Si atoms is approximately 1.89 Å and the distance between the same kind of neighboring atoms (Si or C) is around 3.08 Å [1].

SiC exhibits two-dimensional polymorphism called polytype. All polytypes have a hexagonal frame of SiC bilayers. The hexagonal frame can be viewed as sheets of

spheres of the same radius and the sheets are the same for all lattice planes. However, the relative position of the plane directly above or below are shifted somewhat to fit in the

Fig. 2.1 Basic bonding structure of SiC showing a C atom surrounded tetrahedrally by 4 neighbor Si atoms.

“valleys” of the adjacent sheet in a close-packed arrangement. Hence, there are two inequivalent positions for the adjacent sheets. By labeling the possible positions as A, B and C, one can begin constructing polytypes by arranging the sheets in a specific repetitive order [8]. The only cubic SiC polytype is 3C-SiC, which has the stacking sequence ABCABC.... The simplest hexagonal structure that can be built is 2H, which has a stacking sequence ABAB.... The two most important polytypes, 6H-SiC and 4H-SiC, have stacking sequences ABCACBABCACB...and ABCBABCB..., respectively. The number in the above notations of the resulting crystal structure determines the number of layers before the sequence repeats itself, and the letter determines the resulting structure of the crystal, C for cubic, H for hexagonal and R for rhombohedral. In total, there are more than 100 polytypes for SiC. Figure 2.2 shows the schematic cross-section

of five different SiC polytypes [9]. All polytypes of SiC consist of equal proportion of silicon and carbon atoms, but due to the different stacking sequences between the planes, their electronic and optical properties are different from each other [9].

Fig. 2.2 Schematic cross-section of five different SiC polytypes [9].

Table 2.1 summarizes the physical properties of SiC compared to some technologically important semiconductors. These properties will be elaborated shortly. It can be seen that except for electron mobility, the saturated electron velocity, critical breakdown field, and thermal conductivity of 4H-SiC and 6H-SiC are superior compared to those of Si. From Table 2.1, it can be appreciated why SiC is an attractive semiconductor for power and radio-frequency (RF) applications.

2.2.2 Bandgap

The bandgap of SiC depends on the polytype, and varies between 2.39 eV for 3C-SiC to 3.33 eV for 2H-SiC. The most commonly used polytype is 4H-SiC, which has a bandgap of 3.26 eV [2]. The wide bandgap makes it possible to use SiC for high temperature

operation while retaining its desirable semiconducting properties. Thermal ionization of electrons from the valence band to the conduction band, which is the primary challenge for Si devices during high temperature operation, is not a problem for SiC based devices because of the wide bandgap.

Semiconductor		Si	GaAs	InP	Silicon Carbide			GaN	Diamond
Characteristics	Units				4H-SiC	6H-SiC	3C-SiC		
Bandgap	eV	1.1	1.42	1.35	3.24	3.023	2.39	3.49	5.5
Electron Mobility (300K)	cm ² /Vs	1500	8500	5400	//c-a 800	//c-a 60	950	1000~2000	1800
					^c-a 800	^c-a 400			
Saturated Electron Velocity	10 ⁷ cm/s	1	1.3	1	2	2	2	1.3	2.7
Critical Electric Field	MV/cm	0.3	0.4	0.5	3	3	3	3	10
Thermal Conductivity	W/cm.K	1.5	0.5	0.7	4.5~4.9	4.5~4.9	4.5~4.9	>1.5	6~20
Relative Dielectric Constant	Constant	11.8	12.8	12.5	9.7	9.7	9.7	9	5.57

Table 2.1 Properties of SiC compared to some technologically important semiconductors.

2.2.3 Critical Field

For semiconductors used in power devices, the most important and frequently quoted parameter is the breakdown electric field strength, or the critical electric field. This property determines how large an electric field the semiconductor can sustain before it breaks down electrically. As can be seen in Table 2.1, the breakdown electric field strength of SiC is extremely high, about ten times than that of Si [9].

2.2.4 Saturated Drift Velocity

For semiconductors used in high-frequency devices, an important parameter to consider is the saturated drift velocity (v_{sat}). In SiC, the v_{sat} is 2×10^7 cm/sec, which is twice that of Si [21]. A large saturated drift velocity allows high speed operation, and is important toward achieving a high channel current for microwave devices. Clearly SiC is an ideal semiconductor for such applications.

2.2.5 Thermal Conductivity

For high power and high frequency device applications, the thermal conductivity of the semiconductor used is an important consideration due to the increased heat generation. An increase in temperature generally leads to changes in the physical properties of the semiconductor, and typically affects the device performance adversely. The most serious effect is the degradation of carrier mobility, which decreases with increasing temperature. High-purity semi-insulating SiC material has the highest reported thermal conductivity of 4.9 W/(cm-K). Lower thermal conductivities are reported for doped crystals but they are all above 4 W/(cm-K) at room temperature, which is comparable to the thermal conductivity of copper of 4.0 W/(cm-K) [10]. Due to the high thermal conductivity, SiC based devices are well-suited for high temperature and high power operation.

2.2.6 Figures of Merit

Several figures of merit have been developed to measure the importance of various material properties and enable comparisons between materials for high frequency and

high power applications. The two most important figures of merit are Keyes Figure of Merit (KFOM) and Baliga Figure of Merit (BFOM). Keyes proposed a figure of merit which compares semiconductor materials on the basis of switching speeds that could in principle be obtained with transistors fabricated in the material[11].

$$KFOM = \kappa \sqrt{\frac{cv_{sat}}{4\pi\epsilon}} \tag{2.1}$$

where k and ϵ are the thermal conductivity and the dielectric constant of the semiconductor, respectively, and c is the speed of light in vacuum. On the other hand, Baliga proposed a figure of merit for low frequency applications which is given by [12]

$$BFOM = \epsilon\mu E_B^3 \tag{2.2}$$

where μ and E_B are the low-field carrier mobility and dielectric strength of the material respectively.

Material	KFOM	BFOM
Si	1	1
GaAs	0.41	22
6H-SiC	5	920
4H-SiC	5.9	1840
GaN	8.5	24.6
Diamond	32	101

Table 2.2 Comparison of figure of merits for Si, GaAs, 6H-SiC, 4H-SiC, GaN, and diamond (Values are normalized to that of Si) [12, 13].

Table 2.2 shows the figures of merit for Si, GaAs, 6H-SiC, 4H-SiC, GaN, and diamond normalized to those of Si. It can be clearly seen that both 4H-SiC and 6H-SiC are more

favorable compared to Si for high frequency and high power applications. In terms of KFOM, GaN and diamond, particularly diamond, are much better than those of 6H-SiC and 4H-SiC. However, from technology point of view, SiC is still preferred because of its process compatibility with Si, and the fact that it has a native oxide SiO₂ which is a well-understood, established and proven dielectric.

2.3 Thermal Silicon Dioxide Grown on SiC

2.3.1 Thermal Oxidation Model for Si and SiC

To understand the oxidation of SiC, it is important to first review the oxidation of Si. For Si oxidation, the chemical reactions in oxygen or water vapor are given as follows [14].

For thermal oxidation of Si, an increase in temperature will lead to a monotonic increase in the oxidation rate. The thermal oxidation rate in Si can be described by a linear-parabolic dependence of temperature usually referred to as the Deal-Grove model [15]. The relationship between the SiO₂ thickness d_0 and the oxidation time t can be expressed as

$$d_0^2 + Ad_0 = B(t + \tau) \quad (2.5)$$

where A and B are constants related to the mechanism of the oxidation process and the quantity τ represents a shift in the time coordinate to account for the presence of any initial SiO₂ layer. Equation 2.5 is the well known, mixed linear-parabolic relationship. One limiting case occurs for long oxidation time when $t \gg \tau$ and $t \gg A^2/4B$, in which case Eq. 2.5 can be reduced to the parabolic law in oxidation.

$$d_0^2 = Bt \quad (2.6)$$

The other limiting case occurs for short oxidation time when $(t + \tau) \ll A^2/4B$, in which case Eq. 2.5 is reduced to

$$d_0 = \frac{B}{A}(t + \tau) \quad (2.7)$$

Equation 2.7 is the linear law in oxidation. For long oxidation time, the oxidation rate is given by Eq. 2.7 is reduced as it is limited by the diffusion of the reacting species through the SiO_2 . In the case of dry oxidation, the reaction is limited by transport of oxygen through the silicon dioxide layer. The parameter B is proportional to the diffusion coefficient of the reacting species and is called the parabolic rate constant. For short oxidation time, the oxidation rate given by Eq. 2.7 is limited by the reaction rate at the SiO_2/Si interface. The constant B/A denotes the linear rate constant [14].

The linear-parabolic relationship, which has been applied for the oxidation of Si, has also been widely used to describe the oxidation of SiC [16]. The proposed chemical reaction at the interface that occurs between the Si atoms in the SiC lattice and the oxygen molecules is [17]

An additional possible reaction is

In addition, there are a number of secondary reactions that will determine the equilibrium at the reaction interface [17]:

The kinetics is more complicated for the oxidation of SiC when comparing with oxidation of Si. The reaction interface equilibrium will shift in time as the oxygen flux becomes limited by diffusion. In this case, the inter-reaction between Eq.2.10 and 2.11 will determine the reaction rate. The degradation of SiO₂/SiC interface quality is believed to be due to the carbon [6]. However, there is no solid evidence on how carbon affects the microstructure at the interface.

For the oxidation of SiC, one interesting observation is that the oxidation rate depends on the terminal face of the substrate being oxidized and is generally greater on the C-face than on the Si-face for a given polytype [17,18]. During the linear growth, the oxidation rate is determined by the surface reactions. The difference in the growth rates between the two faces (Si and C) can be explained by the in-diffusion of O₂ [18]. During parabolic growth, the main controlling mechanism is the out diffusion of carbonaceous species in both dry and wet oxidation and also the diffusion of O₂. In dry oxidation, SiO₂ grown on the C-face can be described by an initial linear function and, once a layer of SiO₂ is formed, a parabolic function. This change indicates that the growth on the C-face is limited in the first step by the chemical reactions at the interface, and in the second step by the diffusion of O₂ through the SiO₂ from the gas/SiO₂ interface. SiO₂ grown on the Si-face follows generally the same rule, that is, first linear followed by parabolic dependence [17]. However, it has also been reported [19] that the dry oxidation of the Si-face of 3C-SiC, 4H-SiC and 6H-SiC is linear up to 300 hrs. As the atom density is different on different crystal direction face, the oxidation rate will be maximized on the

C-face and minimized on the Si-face, and other faces will have an intermediate growth rate [20]. The oxidation rates have also been shown to depend on the polytype. In dry oxidation experiments [20], it has been shown for 6H-SiC, 4H-SiC and 3C-SiC that the oxidation rate on the Si-face increases when the degree of hexagonality decreases. In contrast, it does not depend on the polytype for the C-face.

Using the empirical Deal-Grove model, the thermal activation energy of the linear and parabolic regions for the oxidation of SiC can be calculated from experimental data. In the literature, there is a large scatter of such data [16]. This is attributed to the dependence of the oxidation rate on factors such as the initial crystal orientation and oxidation method. As there are also secondary reactions in the oxidation process, the activation energies of the oxidation rate and the reacting species involved in the oxidation process may change with the oxidation temperature.

2.3.2 Interface Properties

The metal-SiO₂-Si structure is by far the most important metal-insulator-semiconductor (MIS) structure. The exact nature of the SiO₂/Si interface is not yet fully understood. A common accepted picture of the interface is that the chemical composition of the interfacial region, as a consequence of thermal oxidation, is a single-crystal silicon followed by a monolayer of SiO_x, that is, incompletely oxidized silicon, then a strained region of SiO₂, and the remaining is stoichiometric, strain-free and amorphous SiO₂ [14].

For a practical metal-oxide-semiconductor (MOS) structure, there are interface traps and oxide charges that will affect the ideal MOS characteristics. The basic classifications of

Fig. 2.3 Charges in thermally oxidized silicon.

these traps and charges are shown in Fig. 2.3 [21], which include (1) *Interface Trapped Charge (Q_{it})*: these are positive or negative charges due to structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation or similar bond-breaking processes. The interface trapped charge is located at the interface. Unlike fixed charge or trapped charge, interface trapped charge is in electrical communication with the underlying semiconductor. Interface traps can be charged or uncharged, depending on the surface potential. Most of the interface trapped charge can be neutralized by low-temperature hydrogen or forming gas anneals. This charge trap has also been called surface states, fast states, interface states, and so on. (2) *Fixed oxide Charge (Q_f)*: this is a positive charge, due primarily to structural defects in the SiO_2 layer less than 2 nm from the interface. The density of this charge, whose origin is related to the oxidation process,

depends on the oxidation ambient and temperature, cooling conditions, and on substrate orientation. Since the fixed oxide charge cannot be determined unambiguously in the presence of moderate densities of interface trapped charge, it is only measured after a low-temperature hydrogen or forming gas anneal, which minimizes interface trapped charge. The fixed oxide charge is not in electrical communication with the underlying semiconductor substrate. (3) *Oxide Trapped Charge (Q_{ot})*: this charge may be positive or negative depending on holes or electrons being trapped in the bulk of the SiO_2 . Trapping may result from ionizing radiation, avalanche injection, Fowler-Nordheim tunneling, or other mechanisms. Unlike fixed charge, oxide trapped charge is sometimes annealed by low-temperature treatments, although neutral traps may remain. (4) *Mobile Oxide Charge (Q_m)*: this is caused primarily by ionic impurities such as Na^+ , Li^+ , K^+ , and possibly H^+ . Negative ions and heavy metals may also contribute to this charge though they are typically not mobile below 500°C .

SiC is the only compound semiconductor that undergoes a chemical reaction with oxygen to form a native SiO_2 insulator. This is seen as one of the most important technological advantages of SiC and has motivated considerable effort in its development. The basic classifications of traps and charges in thermal SiO_2 on SiC are similar to those in thermal SiO_2 on Si . For silicon MOS devices, the channel mobility is comparable to the bulk silicon mobility because of the excellent SiO_2/Si interfaces properties [14]. On the other hand, the MOS inversion mobilities in N-type 4H- SiC are known to be as low as $15\text{--}20\text{ cm}^2/\text{Vs}$ in the year 2000 [22], and consequently the channel resistance in SiC MOSFETs is high. The high fixed charge and interface state densities in the thermal SiO_2 on SiC

also limit the control of the threshold voltages for SiC MOSFETs. In SiC technology development, the improvements in substrate size and quality, and progress in epitaxy growth and doping control, implantation and implant activation have greatly accelerated SiC based device research. However, a lack of good understanding and control over the MOS properties of SiC MOS devices has rendered the study of oxide-semiconductor interface as the most pressing area of research before viable SiC MOSFETs could be demonstrated.

2.3.3 Methods to Improve SiO₂/SiC Interface Quality

Obtaining high quality SiO₂ is the main challenge in the fabrication of SiC based MOSFETs, since high quality SiC wafers with different sizes are already commercially available. For the oxidation work, the key obstacle is the high interface states density (D_{it}) at the SiO₂/SiC interface, which can degrade the MOSFET channel mobility considerably [29]. In the past ten years, researchers have devoted great efforts towards improving the quality of thermal SiO₂ grown on SiC. Since 1995, research on SiC oxidation and MOS application has been intensively carried out by different research groups around the world, in particular, Cree Research, Inc. and Purdue University [3, 27, 29]. In the following, some key process steps that could affect the SiO₂/SiC interface quality will be discussed.

1) Cleaning technology

Cleaning of wafer surface plays an important role in the development of Si technology. Substrate surface cleaning procedures have a strong influence on the final interface quality [14]. For SiC, most investigators used a variation of a silicon based procedure,

that is, the well-known “RCA Clean” [23]. Afanasev *et. al* [24] used an ozone preclean in which the surface is exposed to UV light to form a sacrificial SiO₂ layer prior to cleaning. Zetterling *et. al* [25] exposed the surface to oxygen plasma prior to thermal oxidation. Both authors claimed that their methods have resulted in a significant improvement in the interface quality compared to samples processed without the precleaning step.

Fig. 2.4 Loading process effect on interface states density [3].

2) Loading procedure

It is known that silicon atoms preferentially evaporate from the surface leaving a carbon-rich, or graphitic surface if SiC is heated up slowly [3]. To minimize this effect, samples can be loaded at around 800°C before the temperature is slowly raised to the final

oxidation temperature [3]. Shenoy from Purdue University claimed that this procedure reduces the interface state density by about a factor of two [26]. Figure 2.4 shows the effects of the loading process on the interface states density [26].

3) Annealing

Oxidation of SiC is normally conducted in the temperature range from 1000°C to 1150°C [1,3,4]. The oxidation is typically followed by a 30 min in-situ anneal in Ar or N₂. [3] This anneal is believed to allow CO to diffuse out of the SiO₂ after the oxidation. However, up to date, there is no concrete evidence on this hypothesis. Anecdotal evidence suggested that annealing improves the high-temperature reliability of the SiO₂ [27]. Besides annealing in inert gas after oxidation, other gases such as hydrogen and nitridation gas (N₂O, NO, NH₃) have also been used to improve the SiO₂/SiC interface quality. Fukuda K. *et. al* [28] reported that hydrogen post-oxidation annealing (H₂ POA) at 800°C for 30mins reduced the D_{it} at the energy range of 0.2-0.6 eV below the conduction band for N-type 4H-SiC MOS structures on the (0001) Si face. Moreover, they also found that the H₂ POA process was effective in reducing D_{it} of MOS capacitors on the (11 $\bar{2}$ 0) face. The interface trap density could be reduced by one order of magnitude compared to thermal oxidation without H₂ POA. On the other hand, there was report that claimed hydrogen POA did not result in improvement in the D_{it} [29]. The group in Purdue University annealed 4H-SiC samples in forming gas (H₂/Ar) from 700°C to 1000°C and found that both the fixed charge and the interface states density did not have significant difference compared to the unannealed control wafer [27]. Therefore,

there is a need to further investigate the exact effects of hydrogen POA on the interface states density.

4) Nitridation

Nitrided SiO_2 on SiC have been studied, motivated by the improved reliability in Si thin gate oxide MOSFET by the incorporation of nitrogen into the SiO_2 [14,30] Li H. F. investigated the nitridation effect on SiO_2 grown on both 4H- and 6H-SiC [30,31]. The author claimed that nitridation can greatly improve the interface states density compared to oxidation processes that do not include nitridation. Figure 2.5 shows the interface states density with and without nitridation annealing [31].

Li H. F. et al [32] further investigated SiO_2 /4H-SiC structures annealed in nitric oxide and argon gas ambiances using X-ray photoelectron spectroscopy. A SiO_2 /4H-SiC interface with complex intermediate oxide/carbon states was found in the case of the Ar annealed sample. These compounds, however, were absent in the NO annealed sample. At the interfaces, the nitrogen 1s (N 1s) photoelectron spectrum was symmetrical and could be fitted with one peak, representing the strong $\text{Si}\equiv\text{N}$ bond. The N 1s and C 1s XPS spectra acquired in the bulk of the dielectric revealed not only the presence of $\text{Si}\equiv\text{N}$ bond but also a trace amount of N-C bond.

G. Y. Chung et al. [22] found that annealing in nitric oxide after a standard oxidation/re-oxidation process resulted in a slight increase in the defect state density in the lower portion of the band gap for P-type SiC and a significant decrease in the density of states

in the upper half of the gap for N-type SiC. Theoretical calculations provided an explanation for these results in terms of N passivating C and C clusters at the interface.

Fig. 2.5 Interface state density versus gate voltage (nitridation effect) [31].

P. T. Lai *et al.* [33] found that after nitridation, a significantly smaller shift of flatband voltage during high-field stress was observed compared to N_2 annealed devices. This indicated that a much better SiO_2 reliability could be achieved by replacing strained Si-O bonds with stronger Si-N bonds during nitridation. Kinetics of NO nitridation was investigated by K. McDonald *et al.* [34,35]. They found that nitrogen content at the interface initially increased with time and temperature, but nitrogen was subsequently removed from the interface at temperatures above 1050°C . This nitrogen removal, and the associated SiO_2 growth on the SiC substrate, was caused by O_2 formed through the thermal decomposition of NO.

The mechanisms responsible for the improvement of the interface states density by nitridation were proposed by V. V. Afanasev et al. [36]. The author suggested that the dominant positive effect of nitridation is in significantly reducing the slow electron trap density. These traps are likely to be related to the defects located in the near-interfacial SiO₂ layer. Also, they found that the fast interface states related to clustered carbon were also reduced by nitridation. At present, nitridation is still being intensively investigated [4,36]. A lot more effort would be needed to fully understand the nitridation mechanism and address the issue of high interface states density.

2.4 Non-thermal SiO₂ on SiC

As thermal oxidation of SiC results in high interface states density and fixed charge, other techniques have been attempted to form SiO₂ on SiC. Chappel et al. [37] have grown SiO₂ on 4H-SiC by low temperature (<300°C) plasma oxidation. The MOS capacitors fabricated from those plasma oxidized 4H-SiC exhibited stable CV characteristics, with interface state density and fixed charge of $2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ and $1.3 \times 10^{12} \text{ cm}^{-2}$, respectively. Sridevan et al. [38] have fabricated SiC MOS structure using gate SiO₂ deposited by the chemical vapor deposition (CVD) technique. The gases used were Silane (diluted with argon) and nitrous oxide. The SiO₂ was found to have an interface state density of $7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and a low effective charge density of $1.1 \times 10^{11} \text{ cm}^{-2}$. The quality of the deposited SiO₂ was found to be comparable to the quality of thermal SiO₂. Tan *et. al* [39] investigated MOS capacitors formed by oxidation of polycrystalline silicon deposited by chemical vapor deposited (CVD) on SiC. The oxidation temperature and time required to oxidize the polysilicon were low enough to

ensure insignificant oxidation of the underlying SiC. The method resulted in uniform SiO₂ formation on nonplanar SiC surfaces, such as those occurring in the U-shaped MOS power transistor. The quality of the SiO₂/SiC interface on the Si-face of SiC was comparable to that formed by thermal oxidation.

2.5 Other Dielectrics on SiC

Besides SiO₂, other dielectrics have also been investigated to form SiC MIS structure [41,43]. These investigations were motivated by the need to achieve high breakdown voltage SiC power devices, as very often the maximum blocking voltage is limited by the breakdown of the SiO₂, rather than the SiC. This occurs because the electric field in the SiO₂ is higher than the peak electric field in the SiC by the ratio of their dielectric constants, about a factor of 2.5. Thus, an insulator with a dielectric constant closer to that of SiC is desirable to reduce the electric field in the dielectric and increase the breakdown voltage of the device. Among the alternative dielectrics, AlN is a good candidate for the following reasons: (1) its lattice is matched to SiC; (2) its thermal stability is much better than SiO₂ and thus enables operation at higher temperatures [41].

Zetterling *et. al* investigated single crystalline AlN grown on 4H-SiC and 6H-SiC substrates using the metal organic chemical vapor deposition (MOCVD) technique at 1200°C [41,40]. Figure 2.6 shows the measured high-frequency C-V results for the sample [41]. Though the high-frequency C-V curves revealed accumulation, depletion and deep depletion regions, large flatband voltage shift and the stretching out of the C-V

Fig. 2.6 Simultaneous capacitance and conductance versus voltage characteristics for a 220nm thick AlN film on the N-type 6H-SiC [41].

curves implied that the fixed charge and interface trap density were too high. More work is needed to further investigate how the quality of the AlN/4H-SiC interface can be improved.

Motivated by the high k dielectrics employed in Si technology, some researchers have applied these dielectrics directly on 4H-SiC and a few reports have been published [43]. There are several issues related to such high k dielectrics used in the SiC MIS structure. One problem is that for high k dielectrics, given the higher permittivity, their bandgaps are typically smaller [42]. This will lead to a smaller band offset between the conduction bands of SiC and the dielectrics, and consequently result in a much higher leakage current.

Fig. 2.7 C-V curves of 4H-SiC MOS capacitors combining 20nm thick HfO_2 with different types of SiO_2 interlayer: (1) SiO_2 grown in NO and N_2O by products during HfO_2 deposition (solid lines). (2) SiO_2 grown during exposure to UV radiation and ozone (dashed lines). (3) 3nm thermally grown SiO_2 (dotted lines) [43].

V. V. Afanasev *et. al* [43] deposited high dielectric permittivity HfO_2 layers on ultrathin thermally grown SiO_2 on 4H-SiC (0001) and demonstrated good insulating properties for the insulating stack. The stack combined the ultrathin SiO_2 on 4H-SiC and the associated high energy barriers for electron and hole injection from the 4H-SiC into the HfO_2 . Fig. 2.7 shows the C-V results of the N-type and P-type 4H-SiC MOS capacitors combining 20nm of HfO_2 with three different types of SiO_2 interlayer. They demonstrated that with a large electric field applied to the SiC surface up to 3 MV/cm, the electric field in the insulator was still maintained at a moderate level. This is desirable for SiC high power

device application. As the quality of thermal SiO_2 grown on 4H-SiC has not yet reached a level suitable for device application, more and more researchers are exploring alternative dielectric materials as the gate dielectric. However, as mentioned in this section, further research is needed before some practical alternative gate dielectrics can be found for 4H-SiC MOS applications.

2.5 Summary

In this chapter, the properties of SiC, which include crystal structure, bandgap, critical field, saturation electron velocity and thermal conductivity have been presented. Thermal oxidation of SiC has also been reviewed. The linear-parabolic relationship, which has been successfully applied to model the oxidation of Si, has also been widely used for the oxidation of SiC. Due to the presence of carbon, the interface of thermal SiO_2/SiC is much more defective compared to that of SiO_2/Si . This is the reason behind the low channel mobility of SiC based MOSFETs. Various methods employed to improve the SiO_2/SiC interface quality have been discussed. Besides thermal SiO_2 , a review of the other dielectrics on SiC has also been carried out.

Chapter 3 Characterization and Analytical Techniques

3.1 Introduction

In this chapter, the characterization and analytical techniques used in this study will be presented. The characterization techniques are categorized into two groups: One for the characterization of the physical properties of silicon dioxide and other dielectrics on 4H-SiC, and the other for the electrical characterization of their interfaces.

3.2 Physical Characterization

3.2.1 X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy is a surface analytical technique that can be used to probe information concerning the chemical bonding of the samples. [44] In this study, XPS was used to study the bonding in the thermal oxide formed on 4H-SiC. The samples under investigation are irradiated by monochromatic soft X-rays and the characteristic kinetic and binding energies of emitted core electrons are measured. Primary X-rays of 1~2 keV energy is typically used to eject photoelectrons from the sample under investigation. The measured energy of the ejected electron E_{sp} is related to the binding energy of the electron E_b referenced to the Fermi Energy E_F , by

$$E_b = h\nu - E_{sp} - q\phi_{sp} \quad (3.1)$$

where $h\nu$ is the energy of the primary X-rays and ϕ_{sp} is the work function of the spectrometer [44]. The spectrometer and the sample are electrically connected forcing their Fermi levels to be lined up. As E_b is dependent on the X-ray energy, it is important

that the incident X-ray energy is monochromatic. The basic photoelectron generation process is shown in Fig. 3.1 [44]

Fig.3.1. Illustration of the photoelectron generation process. (a) The ground state with injecting X-ray photon; (b) photoelectric interaction between the photon and electron in the specific core level; (c) The excited state with a photoelectron emission leaving a positive hole in the core level [44].

A Kratos AXIS spectrometer equipped with monochromatic Al K α (1486.71 eV) X-ray source was employed in this study. The XPS analysis was conducted with an ultra high vacuum (UHV) system with a pressure typically near 1×10^{-10} Torr. Such a UHV environment was reached via a combination of pump systems. The use of a roughing pump and a turbo molecular pump could first attain a pressure near 1×10^{-6} torr.

Fig.3.2 Schematic illustration of measurement of photoelectrons [44].

Subsequently, a pressure near 1×10^{-10} Torr could be obtained by the main diffusion pumps with liquid nitrogen cooling system both for the chambers and the spectrometer. An ion pump was used for the X-ray anodes. Further pumping of the system could be performed using two titanium sublimation pumps if necessary.

The photoelectron selection is based on a hemispherical electron energy analyzer as illustrated in Fig. 3.2 [44]. The electrostatic potential between the two metal plates can be modulated by applying different voltages. Thus it allows electrons with a particular energy to pass through the plates and reach the detector. A higher resolution for the analyzer can be achieved by lowering the passing energy, which however will lead to lower detection intensity. The detector has an angle specific function and it can map electrons with different distribution angles of $\pm 2^\circ$, $\pm 5^\circ$ and $\pm 7^\circ$. Sample translation and rotation are necessary in angle resolved XPS measurements, which can be performed by the manipulator. The sample introduction system is designed to allow rapid sample replacement without interfering with the vacuum in the main chamber. This renders the measurement process more efficient as the pump-down time is typically long. The sample introduction system consists of a load lock, which can be brought to atmospheric pressure to load samples and pumped down to $\sim 10^{-7}$ Torr in a short time. It also consists of a swing arm, which is controlled magnetically to mount and shift the samples. Normally, it takes 0.5 hour to load samples and vacuum the chamber. Besides surface elemental scan, depth profile analysis can be performed with the assistance of Ar ion sputtering. Elemental depth profiling of the surface layer and interfacial structure can be determined

by sputtering off film surface layer by layer using an argon ion gun with energy of 15 keV and a sputtering rate of 3 nm/min.

In this work, X-ray spectrometer was used to characterize the bonding and presence of carbon and silicon for thermal oxide grown on 4H-SiC. Depth profiling of the oxide layer was also carried out to investigate the details of the oxidation process.

3.2.2 Ellipsometry

Ellipsometry is a contactless and non-invasive technique to measure changes in the polarization state of light reflected from a surface [45]. It allows the determination of film thickness and optical constants. For a beam of linearly polarized light, the electric field E can be represented by two components. One is the s -direction taken to be normal to the direction of propagation and parallel to the sample surface. The other is the p -direction which is taken to be normal to the direction of propagation and contained in the plane of incidence. Normally, when a polarized light is reflected from a sample surface, both its amplitude and the phase will be modified depending on the optical properties of the sample [45]. Figure 3.3 shows the schematic geometry of the linearly polarized light with p and s polarizations encountering a sample that comprises three media, labeled as medium 0, 1 and 2.

The Fresnel reflection coefficients for p and s components of light traveling from medium 0 to medium 1 are given by [46],

$$r_{01p} = \frac{N_1 \cos \phi_0 - N_0 \cos \phi_1}{N_1 \cos \phi_0 + N_0 \cos \phi_1} \quad (3.2a)$$

$$r_{01s} = \frac{N_0 \cos \phi_0 - N_1 \cos \phi_1}{N_0 \cos \phi_0 + N_1 \cos \phi_1} \quad (3.2b)$$

The subscript 0, 1 and 2 denote the corresponding medium while the subscript p and s denote the corresponding polarizations. N_i and ϕ_i are the complex refractive index and the incident angle at medium i respectively.

Fig. 3.3. Schematic illustration of polarized light encountering a three-medium system.

Similarly, the Fresnel reflection coefficients representing light traveling from medium 1 to 2 can be expressed as [46],

$$r_{12p} = \frac{N_2 \cos \phi_1 - N_1 \cos \phi_2}{N_2 \cos \phi_1 + N_1 \cos \phi_2} \quad (3.3a)$$

$$r_{12s} = \frac{N_1 \cos \phi_1 - N_2 \cos \phi_2}{N_1 \cos \phi_1 + N_2 \cos \phi_2} \quad (3.3b)$$

For the system illustrated in Fig. 3.3, the overall reflection coefficients for the p and s polarizations, R_p and R_s are given by [46],

$$R_p = \frac{r_{01p} + r_{12p} \exp(-j2\beta)}{1 + r_{01p} r_{12p} \exp(-j2\beta)} \quad (3.4a)$$

$$R_s = \frac{r_{01s} + r_{12s} \exp(-j2\beta)}{1 + r_{01s} r_{12s} \exp(-j2\beta)} \quad (3.4b)$$

The exponent β can be expressed in terms of the thickness of medium 1, L_1 , the complex refractive index of medium 1, N_1 , and the wavelength, λ , as

$$\beta = 2\pi \left(\frac{L_1}{\lambda} \right) N_1 \cos \phi_1 \quad (3.5)$$

For the entire optical system, the ratio of reflection coefficient (ρ) is given by [46]

$$\rho = R_p / R_s = \tan(\psi) \exp(j\Delta) \quad (3.6)$$

where $\tan(\psi) = \frac{|R_p|}{|R_s|}$, $\Delta = \Delta_p - \Delta_s$. ψ and Δ are called the ellipsometric angles.

For a homogeneous medium, $N = n - jk$ where n is the real part of the refractive index

and k is the extinction coefficient. The absorption coefficient α is related to k by $\alpha = \frac{4\pi k}{\lambda}$,

where λ is the wavelength in vacuum. The dielectric function ε of the medium is related to the refractive index as follows [46]:

$$\varepsilon = \varepsilon_1 + j\varepsilon_2 \quad (3.7)$$

$$\varepsilon_1 = n^2 - k^2 \quad (3.8)$$

$$\varepsilon_2 = 2nk \quad (3.9)$$

Therefore, from the measured ellipsometric data ψ and Δ , others parameters such as ρ , N , L , ε can be deduced and the optical and dielectric properties of the material can be determined.

In this work a spectroscopic ellipsometer (J. A. Woolam Co. VASE) was used to characterize the optical properties of thermal oxide formed on 4H-SiC. The ellipsometric angles ψ and Δ were measured in the wavelength range from 400 to 1100 nm, in step of 10 nm. The incident angle was fixed at 69° or 75°.

3.2.3 Fourier Transform Infrared Spectroscopy (FTIR)

Fourier transform infrared spectroscopy (FTIR) can be used to characterize thin films in terms of their composition and bond structure. This technique is based on the absorbance of infrared radiation and is sensitive to bulk changes in the rotational, bending, and stretching vibration modes of the molecules in the film. FTIR is a useful technique for characterizing the bonding configuration and the composition of thin films deposited under different conditions. In our study, the technique was used to study amorphous hydrogenated silicon nitride (a-SiN_x:H) films, which were applied as a dielectric layer on 4H-SiC to form a metal-insulator semiconductor (MIS) structure. The infrared absorption was measured using a Perkin-Elmer 2000 Fourier Transform Infrared (FTIR) spectrometer. The measurements were carried out over a scanning range of 400 cm⁻¹ to 4000 cm⁻¹ at room temperature, with a spectral resolution of 1 cm⁻¹.

3.3 Electrical Characterization

3.3.1 Basic MOS Theory

The Metal-Oxide-Semiconductor (MOS) is the core structure in modern microelectronics [7,21]. The two-terminal MOS capacitor is both the simplest of MOS devices and the heart of all MOS devices. The MOS capacitor is a simple two-terminal device composed of a thin SiO_2 layer sandwiched between a silicon substrate and a metallic field plate. A second metallic layer present on the bottom side of the semiconductor provides an electrical contact to the semiconductor substrate. The terminal connected to the field plate and the field plate itself is referred to as the gate; the silicon-side terminal, which is normally grounded, is called the back or substrate contact. To theoretically analyze the MOS structure, it is necessary to simplify the real MOS structure to an ideal MOS structure by assuming the following properties: (1) the metallic gate is sufficiently thick so that it can be considered as an equipotential region under ac as well as dc biasing conditions; (2) the SiO_2 is a perfect insulator with zero current flowing through the SiO_2 layer under all static biasing conditions; (3) there are no charge centers located in the SiO_2 or at the SiO_2 -semiconductor interface; (4) the semiconductor is uniformly doped; (5) the semiconductor is sufficiently thick so that, regardless of the applied gate potential, a field-free region (the so-called substrate 'bulk') is always encountered before reaching the back contact; (6) an ohmic contact has been established between the semiconductor and the metal on the back side of the device, and (7) the metal oxide semiconductor capacitor (MOS-C) is a one dimensional structure with all parameters varying only along the direction normal to the interfaces [7].

In the operation of the MOS-C, a voltage V_G is applied to the gate, and the back side of the MOS-C is grounded. Under an applied V_G , the semiconductor Fermi energy is unaffected by the bias and remains invariant. This is a direct consequence of the assumed zero current flow through the structure under all static biasing conditions. The applied bias voltage separates the Fermi energies at the two ends of the structure by an amount equal to qV_G , where q is the electron charge. Thus, the metal and semiconductor Fermi levels may be considered to be connected to the outside world. In applying a biasing voltage, one grabs onto the handles and rearranges the relative up-and-down positioning of the Fermi levels. The back contact is grounded and the semiconductor-side handle therefore remains fixed in position. The metal-side handle, on the other hand, is moved downward if $V_G > 0$ and upward if $V_G < 0$. Since the barrier heights are fixed quantities, the movement of the metal Fermi level obviously leads in turn to a distortion in other features of the energy band diagram. There is no band bending in the metal because it is an equipotential region. In the SiO_2 and semiconductor, the energy bands must exhibit an upward slope or downward slope depending on the V_G applied. In the SiO_2 taken to be an ideal insulator with no carrier or charge centers, Poisson's equation yields

$$dE_{OX} / dx = 0 \Rightarrow E_{OX} = \text{Constant} \quad (3.10)$$

where E_{OX} is the electrical field inside the oxide. Hence, the slope of the energy bands in the SiO_2 is a constant. In the semiconductor, the band bending is expected to be more complex [7].

By applying a different V_G , different band bending will occur in the semiconductor [21]. Taking the semiconductor substrate to be N-type, by applying different V_G , several

situations will occur: (1) **Accumulation**. It occurs when a positive bias is applied on the gate electrode. The application of $V_G > 0$ lowers the Fermi level, E_F , in metal more than the E_F in the semiconductor and causes a positive sloping of the energy bands in both the SiO_2 and semiconductor. The resulting energy band diagram is shown in Fig. 3.4(a). It is noted that the electron concentration inside the semiconductor, $n = n_i \exp[(E_F - E_i)/kT]$, increases as one approaches the SiO_2 -semiconductor interface, where n_i is intrinsic carrier density, E_i is the intrinsic Fermi level, k is Boltzmann's constant and T is temperature. This condition, where the majority carrier concentration is greater near the SiO_2 -semiconductor interface than in the bulk of the semiconductor, is known as accumulation. In this situation, positive charge is placed on the MOS-C gate. Correspondingly, to maintain a balance of charge, negatively charged electrons must be drawn toward the semiconductor-insulator interface. The charge inside the device is shown in Fig. 3.4(b). (2) **Depletion**. It occurs when a small negative V_G is applied to the MOS-C gate electrode. This slightly raises the E_F in the metal relative to the E_F in the semiconductor and causes a small negative sloping of the energy bands in both the insulator and semiconductor, as displayed in Fig. 3.4(c). It can be clearly seen that the concentration of the majority carrier electrons has been decreased, that is depleted, in the vicinity of the SiO_2 -semiconductor interface. A similar conclusion can be reached from charge considerations. Setting $V_G < 0$ places a negative charge on the gate, which in turn repels electrons from the SiO_2 -semiconductor interface and exposes the positively charged donor sites. The approximate charge distribution is shown in Fig. 3.4(d). This situation is known as depletion. (3) **Inversion**. It occurs when a large negative bias is applied to the MOS-C gate. As V_G is increasingly more negative, the

bands at the semiconductor surface will bend up more and the hole concentration at the surface will likewise increase systematically from less than n_i when $E_i(\text{surface}) < E_F$, to bigger than n_i where $E_i(\text{surface})$ exceeds E_F . By further increasing V_G negatively, the following condition may result [7]

$$E_i(\text{surface}) - E_i(\text{bulk}) = 2[E_F - E_i(\text{bulk})] \quad (3.11)$$

$$p_s = n e^{[E_i(\text{surface}) - E_F]/kT} = n_i e^{[E_F - E_i(\text{bulk})]/kT} = n_{\text{bulk}} = N_D \quad (3.12)$$

where p_s is the surface charge density and N_D is the donor doping density. The gate voltage at which $p_s = N_D$ is known as the threshold voltage V_T . For a further increase in the negative bias V_G , p_s exceed $n_{\text{bulk}} = N_D$ and the surface region will change in character from N-type to P-type. The minority carrier concentration at the surface now exceeds the bulk majority carrier concentration and this condition is referred to as inversion. Energy band and charge diagrams depicting the inversion condition are displayed in Fig. 3.4 (e) and 3.4 (f) respectively.

If analogous biasing considerations are performed for an ideal P-type device, similar results will be achieved. It is important to note that the biasing voltages in a P-type device are reversed in polarity relative to those in an N-type device.

3.3.2 Capacitance-Voltage Characteristics

With dc current flow blocked by the SiO_2 , the major observable exhibited by a MOS-C is capacitance. The measured capacitance-voltage (C-V) characteristics are of considerable practical importance. The characteristics serve as a powerful diagnostic tool for the

Fig.3.4 Energy band diagrams and block charge for ideal N-type MOS-C under accumulation [(a) and (b) respectively], depletion [(c) and (d) respectively] and inversion [(e) and (f) respectively].

identification of deviations from the ideal in both the SiO_2 and the semiconductor. High and low frequency C-V data derived from a representative N-type substrate MOS-C are displayed in Fig. 3.5.

Fig. 3.5 Capacitance vs. Gate Voltage diagram of MOS Capacitor. Flatband voltage (V_{FB}) separates the accumulation region from the depletion regime. Threshold voltage (V_T) separates the depletion regime from the inversion regime. C_{HF} is high frequency capacitance while C_{QS} is quasi-static or low frequency capacitance.

To explain the observed C-V characteristics, we consider how the charge inside an N-type MOS-C responds to the applied ac signal as the dc bias is systematically changed from accumulation, through depletion, to inversion. Under accumulation the dc state is

characterized by the pile-up of majority carrier right at the SiO₂-semiconductor interface. Furthermore, as majority carriers are involved, the state of the system can change very rapidly. For typical semiconductor doping, the majority carrier, the only carrier involved in the operation of the accumulated device, can equilibrate with a time constant of the order of 10⁻¹⁰ to 10⁻¹³ sec. Consequently, at standard probing frequencies of 1 MHz or less it is reasonable to assume the device can follow the applied ac signal quasi-statically, with the small ac signal adding or subtracting a small ΔQ on the two sides of the SiO₂. Since the ac signal merely adds or subtracts a charge close to the edges of an insulator, the charge configuration inside the accumulated MOS-C is essentially that of an ordinary parallel-plate capacitor. Therefore, under either low or high probing frequencies, the capacitance of the MOS-C is given by

$$C(acc) = C_{ox} = \frac{\epsilon_{ox} \epsilon_0 A}{d_{ox}} \quad (3.13)$$

where ϵ_{ox} is the relative permittivity of the SiO₂, ϵ_0 is the permittivity of free space, A is the area of gate electrode and d_{ox} is the thickness of the gate SiO₂ [47].

Under depletion biasing, the dc state of an N-type MOS-C is characterized by a $-Q$ charge on the gate and a $+Q$ depletion layer charge in the semiconductor. The depletion layer charge is directly related to the withdrawal of majority carrier from an effective width W adjacent to the SiO₂-semiconductor interface. Thus, only majority carriers are involved in the operation of the device and the charge state inside the system can change very rapidly. When the ac signal places an increased negative charge on the MOS-C gate, the depletion layer inside the semiconductor widens almost instantaneously; that is, the depletion width quasi-statically fluctuates about its dc value in response to the applied ac

signal. If the stationary dc charge is conceptually eliminated, all that remains is a small fluctuating charge on the two sides of a double-layer insulator. For all probing frequencies this situation is clearly analogous to two parallel plate capacitors (C_{ox} and C_s) in series, where

$$C_{ox} = \frac{\epsilon_{ox} \epsilon_0 A}{d_{ox}} \quad (\text{SiO}_2 \text{ capacitance}) \quad (3.14)$$

$$C_s = \frac{\epsilon_s \epsilon_0 A}{W} \quad (\text{Semiconductor capacitance}) \quad (3.15)$$

and W is the depletion width. The total depletion capacitance is given by [47]

$$C(depl) = \frac{C_{ox} C_s}{C_{ox} + C_s} = \frac{C_{ox}}{1 + \frac{\epsilon_0 W}{\epsilon_s d_{ox}}} \quad (3.16)$$

As the MOS-C is increasingly biased into depletion, from the flat band condition to the onset of inversion, W increases and $C(depl)$ correspondingly decreases.

Once inversion is achieved an appreciable number of minority carriers pile up near the SiO₂-semiconductor interface in response to the applied dc bias. The dc width of the depletion layer reaches a maximum at W_T . The ac charge response is not immediately obvious. The inversion layer charge might conceivably fluctuate in response to the ac signal. Alternatively, the semiconductor charge required to balance ΔQ changes in the gate charge might be derived from small variations in the depletion width. Even a combination of the two extremes is a logical possibility. The result is that the observed charge fluctuation depends on the frequency of the ac signal used in the capacitance measurement [47].

If the measurement frequency is very low ($\omega \rightarrow 0$), minority carrier can be generated or annihilated in response to the applied ac signal and the time-varying ac state is essentially a succession of dc states. Just as in accumulation, situations can occur where charge is being added or subtracted close to the edges of a single-layer insulator. Thus,

$$C(inv) = C_{ox} \quad \text{for } \omega \rightarrow 0 \quad (3.17)$$

On the other hand, when the measurement frequency is very high ($\omega \rightarrow \infty$), the relatively sluggish generation-recombination process will not be able to supply or eliminate minority carrier in response to the applied ac signal. The number of minority carrier in the inversion layer therefore remains fixed at its dc value and the depletion width simply fluctuates about the W_T dc value. Similar to depletion biasing, this situation is equivalent to two parallel-plate capacitors in series

$$C(inv) = \frac{C_{ox}C_s}{C_{ox} + C_s} = \frac{C_{ox}}{1 + \frac{\epsilon_0 W_T}{\epsilon_s d_{ox}}} \quad \text{for } \omega \rightarrow \infty \quad (3.18)$$

W_T is a constant independent of the dc inversion bias and $C(inv) = C(depl) = \text{constant}$. Finally, if the measurement frequency is such that a portion of the inversion layer charge can be created/annihilated in response to the ac signal, an inversion capacitance intermediate between the high and low frequency limits will be observed [47].

The band structure, charge distribution, and qualitative capacitance of MOS-C under different gate biasing conditions have been presented. Now we will discuss how to determine some useful parameters using the high frequency C-V measurement [47].

(1) Conductivity type. It can be easily shown that the high-frequency C-V curve is not completely symmetrical around its “valley region” and that the particular shape of this

portion of the curve is related to the conductivity type of the semiconductor in the surface space charge region. In particular, the slope of the C-V curve in the valley is negative for P-type material and positive for N-type material. This is due to the fact that surface charge due to minority carriers varies more rapidly for a given change in surface potential than surface charge due to ionized dopants.

(2) Oxide thickness. The SiO₂ thickness (d_{ox}) can be determined from the C-V measurements by measuring the insulator capacitance in the accumulation region and relating it to the SiO₂ thickness. The dielectric constant of thermal SiO₂ is assumed to be 3.9.

(3) Substrate doping. The maximum-minimum capacitance technique is usually used for determining the average substrate doping concentration. This simple technique is sufficient for uniformly doped substrates but gives only an average doping concentration for non-uniform doping concentrations. The average doping concentration is determined by transcendently solving for N_A in the following equation [47]:

$$N_A = \frac{4(kT/q) \ln(N_A/n_i)}{q\epsilon_s A^2} \left(\frac{C_{min}}{1 - (C_{min}/C_{OX})} \right) \quad (3.19)$$

where k is the Boltzmann's constant, T is the temperature, q is the electronic charge, n_i is the intrinsic carrier density of the semiconductor, ϵ_s is the permittivity of the semiconductor, A is the area, C_{OX} is the SiO₂ capacitance and C_{min} is capacitance in the depletion range.

(4) Effective oxide charge. There are several types of oxide charges within the SiO₂. It is difficult to identify each of these charges. Normally, the effective oxide charge is used to represent these charges. The effective oxide charge is defined as follows

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{OX}} \quad (3.20)$$

where V_{FB} is the flatband voltage, which can be deduced by comparing the measured and theoretical C-V curves; Φ_{MS} is the work function difference between the metal and semiconductor and Q_f is the effective oxide charge.

The main criteria in judging the quality of SiO₂ thermally grown on Si are the densities of the interface trap and fixed charge using either a C-V measurement or ac conductance measurement. Both interface trap and fixed charge directly affect the threshold voltage of MOSFETs, which is a very important parameter in modern digital circuit application. In transferring these measurement techniques from Si to SiC, it is extremely important to take into account the significantly larger bandgap of SiC and the corresponding increase in the ionization energy of the defect states at the SiO₂/SiC interface. The consequences due to these differences are as follows: (a) The minority carrier generation rate at room temperature in SiC is negligible [48]. As a result, inversion is not observed without external carrier generation or injection, for example using optical or thermal excitation. (b) To measure the distribution of deeper states within the bandgap of SiC, the thermal energy must be increased so as to increase the minority charge emission rate [49]. (c) AC conductance measurement is sensitive only to those states that are able to exchange their charge within the period of the ac voltage. For SiC, this technique is therefore only able to measure relatively fast states. These limitations dictate the conditions under which the

experiments should be carried out and consequently the interpretation of the data obtained.

There have been a number of reports on the electrical properties of SiC/SiO₂ interface [24,26]. The conclusions focused on a number of general observations: (i) the more slowly oxidized Si face has a significantly lower defect density than the C face, (ii) defect concentrations as deduced by C-V measurement are higher in P-type than N-type material and there is no difference for Al or B doping [50,51], (iii) passivation with NO or N₂O reduces the observed levels of SiO₂ defects, however, it remains much higher than the value in Si/SiO₂ interface. Different reports have revealed a wide spread in the observed density of defects in the form of interface density from $3 \times 10^{11}/\text{cm}^2$ to $2 \times 10^{13}/\text{cm}^2$ and fixed charge from $1 \times 10^{11}/\text{cm}^2$ to $1 \times 10^{13}/\text{cm}^2$ [1,4,22]. Besides the differences in the oxidation processes, one possible reason why there is such a wide spread in the interface state density and fixed charge reported lies in the measurement itself and the interpretation of the results. For example, many of the previous work loosely defined the term ‘fixed charge’ and as a result there is some confusion between the fixed charge present near the interface and at the interface. Much of the apparent fixed charge can probably be associated with interface defects.

3.3.3 Determination of Interface States Density

In this section, two methods used to determine the SiO₂/4H-SiC interface states density in this study will be presented. The Terman’s method will be reviewed first, followed by the alternating current (AC) conduction method.

(a) Terman's method

Terman developed one of the methods for determining the interface trap density by high-frequency capacitance measurement [52]. This method relies on a high frequency C-V measurement at a frequency sufficiently high so that the interface traps cannot respond to the ac signal. Thus, those interface traps do not contribute to any capacitance. Although the interface traps do not respond to the ac signal, they do respond to the slowly varying dc gate voltage and cause the high frequency C-V curve to stretch out along the gate voltage axis as the interface trap occupancy changes with the gate bias. As an illustration, Fig. 3.6 shows the stretching out between the ideal C-V curve and the experimental high frequency C-V curve of one of our samples. Essentially, this charge exchange induced by the interface traps leads to a flattening of the high frequency C-V curve. Terman exploited this effect to determine the interface states density (D_{it}) distribution from the shape of the recorded high frequency C-V curve [49].

Fig. 3.6 Ideal and experimental high frequency C-V curves.

The flattening of the C-V curve can be expressed by the shift ΔV_G which the experimental high frequency C-V curve is shifted with respect to the ideal curve.

$$\Delta V_G = V_{G,meas} - V_{G,ideal} \quad (3.21)$$

where $V_{G,meas}$ is the experimental gate voltage at certain capacitance; $V_{G,ideal}$ is the calculated gate voltage with the same capacitance. Knowing $N_{A,D}$ and C_{OX} , $V_{G,ideal}$ can readily be calculated as a function of ψ_s using Eq. 3.19. In the process, the relationship between the measured high frequency C-V and ψ_s can also be obtained. Thus, ΔV_G is obtained as a function of ψ_s as an intermediate result, and it is given by [52]

$$\Delta V_G = \frac{Q_{it} + Q_f}{C_{OX}} + \frac{\Phi_{MS}}{q} \quad (3.22)$$

where Q_{it} is the charge trapped in the interface traps, Q_f is the fixed oxide charges, Φ_{MS} is the work function difference between the metal and semiconductor, and q is the electronic charge.

Differentiating Eq. 3.22, with respect to ψ_s yields [52]

$$D_{it} = \frac{C_{OX}}{q} \left(\frac{dV_G}{d\psi_s} - 1 \right) - \frac{C_s}{q} = \frac{C_{OX}}{q} \frac{d(\Delta V_G)}{d\psi_s} \quad (3.23)$$

It should be noted that the quantities Q_f and Φ_{MS} do not appear in Eq. 3.23. Thus, the D_{it} expression does not depend on the charge type of the interface states. Owing to the differentiation, only the change in the number of trapped charges is relevant rather than their amount or polarity. Since the shift ΔV_G only appears clearly in the depletion region of the C-V curve, the interface states can only be detected in that limited range of bandgap adjacent to the majority carrier band edge.

The limitation of the Terman's method is that it assumes negligible response of the interface states to the AC signal at the test frequency. This condition cannot be met over the entire accessible energy of the bandgap, especially when the test frequency is at 1 MHz, which is a commonly used frequency. Surface potential fluctuations [53], although commonly observed in MOS structures are also not taken into account in the Terman's analysis.

(b) AC conduction method

In 1967, Nicollian and Goetzberger proposed a conductance method to determine interface states density D_{it} of MOS structure [54]. Since then, the conductance method has been generally considered to be the most sensitive method to determine D_{it} . The conductance method is essentially based on the measurement of complex admittance of a MOS structure. This means that both the capacitance C_m and conductance G_m are obtained from this measurement. In addition, this measurement provides the full frequency dependence of capacitance and conductance. This supplies additional information about the dynamic behavior of the interface states and the statistical distribution of the interface charges. In an ideal MOS structure, there is only a capacitive part or a susceptance. In the $G_m/\omega \sim \omega$ curve, where ω is the angular frequency, the peak in G_m indicates that there is a dissipative part present in the sample. This energy loss is due to the capture and emission of carrier by the interface states. The analysis can be carried out [54], using the relatively simple Shockley-Read-Hall theory for interface traps.

In this theory, the traps can only change their occupancy by one unit of charge, and each trap has a single energy level independent of occupancy.

To analyze the conductance data, one must use an equivalent circuit as shown in Fig. 3.7 to obtain the information about the surface states. The parallel conductance and capacitance, G_p and C_p , are extracted from the measured capacitance and conductance, C_m and G_m , which have already been corrected for series resistance arising from non-ideal contacts to the electrode of the substrate [54].

Fig. 3.7 Simple equivalent circuits for AC conductance measurement: (a) the experimental admittance with G_m , the measured conductance and C_m , the measured capacitance. (b) the circuit used to analyze the data.

The expressions for G_p and C_p are [54]

$$\frac{C_p}{C_{ox}} = \frac{1 - C_m / C_{ox}}{(1 - C_m / C_{ox})^2 + (G_m / \omega C_{ox})^2} \quad (3.24)$$

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (3.25)$$

The distribution of the interface trap energies throughout the semiconductor bandgap in the depletion regime is considered to be continuous. As in the Si-SiO₂ MOS structure [54,55], the expressions for the parallel conductance and capacitance in terms of the interface states parameters are [54]

$$G_p / \omega = qAD_{it} \int_{-\infty}^{+\infty} \frac{\exp\{-\xi^2 / (2\sigma_g^2)\}}{\sqrt{2\pi}\sigma_g} \times \frac{\ln(1 + \omega^2 \tau^2 e^{-2\xi})}{2\omega\tau e^{-\xi}} d\xi \quad (3.26)$$

$$C_p = qAD_{it} \int_{-\infty}^{+\infty} \frac{\exp\{-\xi^2 / (2\sigma_g^2)\}}{\sqrt{(2\pi)\sigma_g}} \times \frac{\tan^{-1}(\omega\tau e^{-\xi})}{\omega\tau e^{-\xi}} d\xi \quad (3.27)$$

where q is electronic charge, A is the electrode area, D_{it} is the number of interface states per unit area and per electronvolt, σ_g is the standard deviation of the surface potential caused by fluctuations of interface states, τ is the response time of the continuum of interface states, and ξ is the surface potential. From Eq. 3.27, the equivalent parallel conductance G_p is determined directly by the interface states density, but the parallel capacitance depends both on the interface states and the depletion capacitance. Thus, the experimental data for G_p vs. ω frequency can be fitted to Eq. 3.27 by varying the parameters D_{it} , σ_g , and τ . The same method is used to relate the D_{it} with the energy level of the trap as in the Terman's method [52].

3.4 Summary

In this chapter, the characterization tools used in this project have been reviewed. The basic theories involved in the XPS, ellipsometry and FTIR techniques are presented. These tools are used to characterize the physical properties of thermal SiO₂ and other dielectrics on 4H-SiC. The basic MOS theory has also been reviewed, followed by a detailed analysis of the C-V measurement as a powerful tool for MOS capacitor characterization. The interface states density characterization methods used in this study, namely the Terman's method and AC conductance method, are presented. As 4H-SiC is a wide band-gap semiconductor, the C-V curves of 4H-SiC based MOS capacitor are different from those of Si based MOS capacitors. The particular features of C-V curves of 4H-SiC based MOS capacitor have been highlighted.

Chapter 4 Investigation of Thermal SiO₂ on 4H-SiC

4.1 Introduction

The unique property of SiC lies in that it can be thermally oxidized to form SiO₂ as in the case of silicon. Since SiO₂ is the most widely used gate dielectric for Si technology up to date, it is possible that the gate dielectric processes for Si based technology can be directly transferred to SiC. In recent years, metal-oxide-semiconductor (MOS) structure based on SiC substrate has been widely investigated [3,29,56]. Though great effort has been put into understanding the SiC oxidation process and how the SiO₂/SiC interface quality can be improved, device grade SiO₂/SiC interface with sufficiently low defect density still has not been achieved to date [57,58]. It is believed that the reason for the observed low channel mobility in SiC MOS devices is the high interface states density at the SiO₂/SiC interface. As half of the atoms are C, the SiO₂/SiC interface is much more defective comparing to the SiO₂/Si interface [59]. To obtain detailed information about the SiO₂/SiC interface, such as interface composition and bonding configuration, which are believed to be related to the high interface states density, a number of X-ray photoemission spectroscopy (XPS) and ellipsometry measurements have been carried out [32, 60,61,62,63, 72]. By analyzing the Si 2p and C 1s core level spectra from XPS measurements, it was found that complex intermediate oxide/carbon compound was formed at the SiO₂/SiC interface, which was believed to be responsible for the high interface states density [60,64]. In another study using ellipsometry measurements, it was reported that there exists interface layers with high refractive indices between the SiC substrate and the SiO₂ layer, the values of which are larger than those of SiO₂ [61]. Due

to the complicated structure at the SiO₂/SiC interface, more effort is still needed to clarify the interface bonding configuration and optimize the oxidation process.

In this chapter, XPS and ellipsometry were used to investigate the SiO₂/4H-SiC interface layer components for samples oxidized at different temperatures from 950°C to 1150°C. The carbon distribution in the thermal SiO₂ on 4H-SiC was studied using XPS. The technique was further used to analyze the carbon bonding configuration across the entire SiO₂ layer for 4H-SiC oxidized at 1100°C. For the samples oxidized at 1100°C, post-oxidation annealing in diluted N₂O was further carried out at different temperatures from 900°C to 1100°C. The Terman's method and AC conductance method were used to determine the interface states density of these samples. The trap cross section of the samples was also studied by the AC conductance method.

4.2 Basic 4H-SiC Oxidation Study

We have carried out a basic study of the effects of oxygen flow rate and oxidation time on the oxidation rate of 4H-SiC. The samples employed in this work consist of Si-face vicinal (0001) nitrogen doped (with effective carrier concentrations of $6-7 \times 10^{18} \text{ cm}^{-3}$ and resistance of about 0.02 Ω/cm) n-type 4H-SiC bulk-grown wafers from Cree Research Inc, NC, USA. The samples have been diced into pieces of about 5mm×5mm. For this part of the work, we only used bare 4H-SiC wafers without any epilayer. The samples were cleaned using the standard RCA cleaning process prior to oxidation. This cleaning process is widely used for Si as well as for SiC, and the details can be found in Chapter

six. First, the effects of the flow rate of oxygen on the oxidation rate of 4H-SiC under dry oxidation have been investigated. The detailed oxidation conditions are as follows:

Sample	Ramping up Condition	Oxidation Condition	Cooling Down Condition
1	45°C/min→850°C, 15°C/min→1100°C	1100°C, 3h, 600sccm	1°C/min→800°C
2	45°C/min→850°C, 15°C/min→1100°C	1100°C, 3h, 800sccm	1°C/min→800°C
3	45°C/min→850°C, 15°C/min→1100°C	1100°C, 3h, 1000sccm	1°C/min→800°C
4	45°C/min→850°C, 15°C/min→1100°C	1100°C, 3h, 1200sccm	1°C/min→800°C
5	45°C/min→850°C, 15°C/min→1100°C	1100°C, 3h, 1400sccm	1°C/min→800°C

Table 4.1 Oxidation conditions under different oxygen flow rates.

These five samples were put in a quartz boat before loaded into the furnace at room temperature. After oxidation, the furnace was cool down naturally from 800°C to room temperature before the samples were unloaded. In the second set of experiments, the oxidation rate of 4H-SiC under dry oxidation was studied as a function of oxidation time, at a fixed oxygen flow rate of 800 sccm. As appreciable oxidation of SiC begins at 950°C, the samples in this experiment were loaded and unloaded directly at 1100 °C to obtain more accurate oxidation rates. The oxidation conditions are as follows:

Sample	Flow Rate (sccm)	Oxidation Time (h)
1	800	1
2	800	2
3	800	2.68
4	800	6

Table 4.2 Oxidation conditions at different oxidation times.

The thickness of the oxide layer formed in these two experiments was deduced using spectroscopic ellipsometry measured from 400nm to 1100nm. The oxidation rate is one of the most important parameters to be investigated in the oxidation of 4H-SiC. As stated in Chapter two, oxidation of SiC is commonly reported to obey the Deal-Grove model. So far most of oxidation work have been carried out at 1100°C. Therefore, we have also used this temperature for the oxidation to investigate the effects of oxygen flow on the oxidation rate. For the samples described in Table 4.1, the thickness of the oxide layer was found to vary between 33nm to 38nm, with no correlation to the oxygen flow rate. This suggests that at 1100°C, 600sccm flow of oxygen is adequate to supply enough oxygen for the oxidation. In other words, the oxidation is limited either by the reaction rate or diffusion rate, but not the oxygen supply rate.

Figure 4.1 shows the thickness of the oxide layer as a function of the oxidation time, for the samples described in Table 4.2. As can be seen, the first three points satisfied the Deal-Grove model linear relation as described in Eq. (2.7). The best fitted linear equation to these data points is $d\text{ (}\mu\text{m)} = 0.01515 \cdot t\text{ (hr)} - 0.0042$. The slope obtained is quite low compared to the oxidation of Si that has a slope of about 0.10625 [55], signifying the

much lower oxidation rate of SiC compared to Si. In Eq. (2.7), the ratio B/A is called the linear rate and is proportional to the reaction rate of the slowest reaction. The constant is activated as $\exp(-E_{B/A}/kT)$ and we have obtained $E_{B/A}$ equal to 18.5 kcal/mol, which is in the range of values reported from 17 kcal/mol to 58 kcal/mol [65]. In the literature, the Deal-Grove model parameters are quite scattered for SiC oxidation [24] For example, the linear parameter can vary from 9.7 to 141. For longer oxidation time, we have only one data point available at 6 hours. Nevertheless, it can be seen that the relation between the oxide thickness and oxidation time is no longer linear and appears parabolic.

Fig. 4.1 Dry oxidation of silicon face of 4H-SiC at 1100°C.

4.3 Effects of Oxidation Temperature

In this section, we oxidized 4H-SiC at different temperatures from 950°C to 1150°C. The SiO₂/4H-SiO₂ interfaces formed under different oxidation temperatures were characterized by XPS and ellipsometry. The 4H-SiC samples used in this work consist of

a 10 μm epitaxial layer (with a net dopant concentration $N_d - N_a = 2 \times 10^{15} \text{ cm}^{-3}$) grown on Si-face 4H-SiC bulk ($N_d - N_a = 5 \times 10^{19} \text{ cm}^{-3}$) wafers. These wafers were purchased from CREE Research and cut into $5 \times 5 \text{ mm}^2$ pieces. Before thermal oxidation, the wafers were cleaned using the conventional Radio Corporation of America (RCA) cleaning technique followed by a 1 minute dip in 5% hydrofluoric acid (HF) to remove the native SiO_2 . Thermal oxidation of the wafers were carried out using ultra-pure O_2 (99.999%) at 950°C , 1050°C , and 1150°C for 6 hours.

Spectroscopic ellipsometric measurements have been carried out with the wavelength range from 400 nm to 1100 nm at an incidence angle of 69° . Besides the oxidized samples, ellipsometric measurements were also carried out for a RCA cleaned 4H-SiC wafer that was not oxidized, to obtain the ellipsometry data for the 4H-SiC substrate. The optical constants of stoichiometric SiO_2 and SiO needed in the data analysis were obtained from the literature [66]. For XPS measurements, the base vacuum of the XPS chamber was at $2.67 \times 10^{-7} \text{ Pa}$. Argon sputtering with an accelerating voltage of 4 keV was used to slowly etch the SiO_2 layer and allow composition profiling to be carried out. Deconvolution was performed using Gaussian lineshape functions after a linear background subtraction. For electrical measurements, aluminum was thermally evaporated, and patterned as gate electrodes (area = $1.8 \times 10^{-4} \text{ cm}^2$) to form the MOS capacitors. To extract the interface states density (D_{it}) for each sample, high frequency capacitance-voltage (C-V) measurements were carried out.

For the fitting of the spectroscopic ellipsometric data, various models with different complexity were used and evaluated using the following maximum likelihood estimator.

The mean-squared error (MSE) of each model was defined by

$$MSE = \frac{1}{2N - M} \sum_{i=1}^N \left[\left(\frac{\Psi_i^{\text{mod}} - \Psi_i^{\text{exp}}}{\sigma_{\Psi,i}^{\text{exp}}} \right)^2 + \left(\frac{\Delta_i^{\text{mod}} - \Delta_i^{\text{exp}}}{\sigma_{\Delta,i}^{\text{exp}}} \right)^2 \right] \quad (4.1)$$

where N is the number of experimental ellipsometric data pairs (Ψ, Δ) , M is the number of variable parameters in the model, and σ is the standard deviations of the experimental data points. The raw spectroscopic ellipsometric data for the sample oxidized at 1150°C are shown in Fig. 4.2 as discrete dots.

Fig. 4.2 Ellipsometric parameters for sample oxidized at 1150°C: (a) Ψ and (b) Δ . The insert shows the improvement of three layer model over two layer model.

The fitting results using two different models are also shown. The dotted line shows the fitting results of the two-layer model which consists of a semi-infinite substrate and a stoichiometric SiO_2 layer. It is known that there exists complex silicon oxycarbide SiC_xO_y layer between the SiC substrate and the SiO_2 layer due to incomplete oxidation of SiC [67]. Therefore, a three layer model that comprises a semi-infinite substrate, a thin interface layer and a stoichiometric SiO_2 layer was also used to fit the experimental data. To estimate the interface layer composition between the 4H-SiC substrate and SiO_2 , it is reasonable to assume that it is made up of three components: 4H-SiC, SiO_2 and SiO, the latter being due to the incomplete oxidation. The Bruggeman effective medium approximation (EMA) as described by the following equation was used to obtain the effective optical constants of the interface layer [68]:

$$f_A \frac{\epsilon_A - \epsilon}{\epsilon_A + 2\epsilon} + f_B \frac{\epsilon_B - \epsilon}{\epsilon_B + 2\epsilon} + f_C \frac{\epsilon_C - \epsilon}{\epsilon_C + 2\epsilon} = 0 \quad (4.2)$$

where ϵ is the effective optical constants of the interface layer, ϵ_A , ϵ_B and ϵ_C are the optical constants of 4H-SiC, SiO and SiO₂ respectively, and f_A , f_B and f_C are their respective volume fractions. Instead of fixing the thickness of the interface layer as in other reported work [69, 67], we treat the thickness of the interface layer as a variable fitting parameter in this study to obtain more accurate results. In our fitting, it was found that the volume fraction of SiO₂ always ended up zero in the interface layer, which means that stoichiometric SiO₂ may not appear at the interface. This is reasonable when considering there may not be adequate oxygen to diffuse through the SiO₂ layer and reach the SiO₂/4H-SiC interface. In the oxidation of Si, non-fully oxidized interfaces have also been observed [63]. Therefore, in our fitting, only 4H-SiC and SiO are considered as the components in the interface layer. The fitting result using the three layer model for the sample oxidized at 1150°C is shown in Fig. 4.1. The difference between the three-layer model and the two-layer model is highlighted in the insert of Fig. 4.1, which clearly shows that the three layer model provides a better fit compared to the two layer model, particularly at shorter wavelengths. This may be related to the onset of absorption in the interface layer that consists of 4H-SiC and SiO, and therefore the three-layer model that accounts for this interlayer provides a better fit. The same fitting processes were also applied to the samples oxidized at 950°C and 1050°C.

Oxidation Temperature (°C)	Oxide Total Thickness (nm)	Interface Layer Thickness (nm)	EMA (4H-SiC) Volume Fraction (%)
950	14.8	3.94	60.9
1050	30.1	2.58	46.8
1150	55.2	0.95	32.7

Table 4.3 EMA results of different temperature oxidation.

Table 4.3 shows the fitting results of the thickness of the top SiO₂ layer and the interface layer using the EMA for the three samples oxidized at different temperatures. As can be seen, the oxide thickness increases sharply from 14.8 nm to 55.2 nm as the oxidation temperature increases from 950°C to 1150°C. This strong dependence of the oxidation rate on temperature has also been commonly reported. [16] It can also be seen that as the oxidation temperature increases from 950°C to 1150°C, the interface layer thickness decreases from 3.94 nm to 0.95 nm, despite an increase in the thickness of the top SiO₂ layer. That is, the samples oxidized at higher oxidation temperature have thinner interface layer, probably due to more complete oxidation of 4H-SiC. In terms of volume fraction, it is noted that the volume fraction of 4H-SiC decreases with increasing oxidation temperature, which is consistent with the thinner interface layer observed at higher temperature arising from the more complete oxidation of 4H-SiC. A lower volume fraction of 4H-SiC means a lower carbon content at the interface, which is desirable as it should lead to a lower interface state density [32]. As the root reason for the poor performance of 4H-SiC MOS devices [70], the carbon related compounds should be avoided in oxidation. Our results show that in the range of 950~1150 °C higher temperature oxidation is useful to partially remove the carbon related compounds.

Arising from a number of reactions involved at the interface of $\text{SiO}_2/4\text{H-SiC}$, the formation and removal of carbon related compounds is related to the partial pressure gradients of the various species such as O_2 and CO [71]. The oxidation temperature can affect the pressure gradients and thus lead to different oxidation results. The exact reactions involved may be quite complicated [71] and more studies are needed to understand the physical mechanism behind the interface reactions.

XPS was used to identify the bonding at the $\text{SiO}_2/4\text{H-SiC}$ interface for samples oxidized at different temperatures. Ar was used to sputter the top SiO_2 layer by layer at a sputtering rate of 3 nm/min, until the $\text{SiO}_2/4\text{H-SiC}$ interface was reached. The $\text{SiO}_2/4\text{H-SiC}$ interface was defined at where the oxygen and silicon distribution lines cross each other. In each sputtering step, the XPS spectra were recorded by multiple scanning in the range of binding energies of interest. Figure 4.3 shows the C1s core level spectra at the interface for the samples oxidized at different temperatures. The spectra were deconvoluted using several Gaussian lineshape functions after a linear background subtraction.

The C1s spectra were best fitted with three Gaussian peaks at about 282.7 eV, 283.7 eV and 284.6 eV. These are respectively attributed to the C-Si bonds arising from 4H-SiC substrate, to the $\text{C-Si}_x\text{O}_y$ bonds related to the oxycarbon compound and to the C-C bonds due to the so-called carbon cluster [67, 69]. Upon the deconvolution, the relative areas of the different bonding types have been calculated. We define the bonding percentage of the each bond as the integrated area associated with the bond over the sum of the

integrated areas associated with all the three types of bonds. The results are shown in Fig. 4.4.

Fig. 4.3 Deconvolution results of the C1s core level spectrum for samples oxidized at 950°C, 1050°C and 1150°C.

It is noted that at the interface, the Si-C bonding concentration decreases with increasing oxidation temperature. The concentration of Si-C bonding may be regarded as a degree of oxidation at the SiO₂/4H-SiC interface, with a smaller Si-C bonding concentration implying a more complete oxidation. The samples oxidized at 950°C have a higher Si-C bonding concentration, which suggests that the interface is relatively far from complete oxidation to form stoichiometric SiO₂. On the other hand, the samples oxidized at 1150°C

have lower Si-C bonding concentration, which means that the interface is relatively more oxidized to form SiO₂.

Fig. 4.4 The percentage of the different carbon bonding components at the interface of the samples oxidized at different temperatures.

It is to be noted that this result is concordant with the ellipsometry results that revealed lower 4H-SiC volume fraction at the interface at higher oxidation temperature. Our ellipsometry and XPS results show that higher oxidation temperature is useful to enhance the oxidization of 4H-SiC substrate at the interface, whereas lower temperature oxidation would leave more Si-C bonding and the complex compound (C-Si_xO_y bonds) at the interface. The latter may be responsible for the higher D_{it} at the interface as deduced from electrical measurements to be shown shortly.

To study the SiO₂/4H-SiC interface properties, MOS capacitors based on the above three samples oxidized at different temperatures were fabricated. High frequency capacitance-voltage (C-V) measurements were carried out for the MOS capacitors. Using the Terman's method [52], the interface states density (D_{it}) was calculated near the 4H-SiC conduction band for the samples. The D_{it} results are shown in Fig. 4.5 as a function of the energy below the conduction band edge E_C . As the C-V measurements were conducted at room temperature, only the D_{it} that is within 0.5 eV away from E_C can be accurately established.

As can be seen from the results, the sample that was oxidized at 1150°C has lower D_{it} compared to the other two samples oxidized at lower temperatures. However, the values are still slightly higher than the published results of 4H-SiC oxidized at similar temperatures [45]. This may be attributed to the post-oxidation annealing [45] which was not carried out for our samples. It was found earlier from the ellipsometry and XPS results that lower temperature oxidation would leave more Si-C bonding and the carbon complex compound at the interface. These could likely account for the higher D_{it} observed for the samples oxidized at lower temperatures. [46]

Fig. 4.5 Energy distributions of interface states density in 4H-SiC band gap obtained by the Terman’s method using the high frequency C-V data.

4.4 Carbon Distribution in Thermal SiO₂

As discussed in Chapter two, many researchers have worked on reducing the D_{it} by means of nitrous oxide (N₂O) or nitric oxide (NO) annealing [31,72]. Todate, the D_{it} for SiC MOS structure is still close to two orders of magnitude larger than what have been observed for Si MOS structure [14]. As the presence of carbon atoms is believed to degrade the electrical performance of SiC MOS structure [60], it is very important to understand the mechanisms by which carbon atoms react and diffuse through the SiO₂,

and how they can be reduced, if not eliminated. In this section, we employed XPS to investigate the bonding and concentration of carbon in 4H-SiC MOS structures.

Fig. 4.6 XPS spectra at different SiO₂ depths measured from the SiO₂ surface.

The samples used in this study are N-type 4H-SiC with a doping concentration of $2 \times 10^{15} \text{ cm}^{-3}$. The oxidation was conducted at 1100°C for 5 hours using ultra-pure O₂ (99.999%). The resulting oxide thickness is around 43 nm as deduced by ellipsometry. To investigate the carbon bonding components across the SiO₂ layer, we concentrate on the C 1s core level spectra measured after the samples were sputtered at different times. The sputtering of the oxide was carried out using an argon ion gun with an energy level of 15 keV, which gave rise to a sputtering rate of 3 nm/min. The damage caused to the films due to the Ar ion etching is a potential problem in XPS measurements [44]. Normally this

damage is related to the etch rate. The faster the etching, the more the damage induced. In our experiments, to minimize the damage, the etch rate was controlled to a low value of about 3 nm/min. Furthermore, as the detected photoemission represents an average effect derived from a depth of 3-50 Å from the surface, therefore, the influence of any damage to the XPS results should be insignificant. The C 1s core level spectra at 282.7 eV measured at different depths in the SiO₂ from its surface are shown in Fig. 4.6. It can be clearly seen that there is a decrease in the C 1s peak intensity for depths that are further away the interface. This is consistent with the fact that the carbon atoms diffuse outward through the SiO₂ during the oxidation process and therefore a higher concentration is expected at points nearer the interface.

Figures 4.7 (a), (b) and (c) show the C 1s XPS spectra measured at the SiO₂/4H-SiC interface at a depth of 42 nm, near the SiO₂/SiC interface at a depth of 33 nm and near the SiO₂ surface at a depth of 15 nm respectively. Also shown in the figures are the fitting results of the spectra using several Gaussian lineshape functions. At the interface of SiO₂/4H-SiC, the XPS spectrum was best fitted with three Gaussian lineshape functions, as illustrated in Fig. 4.6 (a). The three peaks observed are at 282.7 eV (Si-C), 283.7 eV (SiO_xC_y), and 285.5 eV (C-C). In fitting the XPS spectra measured at different depths, the binding energies for the Si-C, C-C, and the SiO_xC_y bonds were found to be close to each other within ± 0.08 eV, but not exactly identical. This is due to the different fractions of oxygen and carbon in the SiO_xC_y bonds and the change in the bonding environment at different depths that would affect the binding energies.

(a)

(b)

(c)

Fig. 4.7 The C 1s XPS spectrum at the SiO₂/SiC interface (a), near the SiO₂/SiC interface (b), near SiO₂ surface (c). The insets of (b) and (c) are the Si 2p XPS spectra measured concurrently.

The presence of carbon clusters (C-C bonds) at the SiO₂/SiC interface has been previously reported [73] which is consistent with what we have observed. These carbon clusters are not found inside the SiO₂ of our samples, as can be seen from the fitting results shown in Figs. 4.7 (b) and (c). This means the carbon clusters (C-C bonds) do not exist in the oxide bulk. However, there are still SiO_xC_y and Si-C bonds present inside the SiO₂ [72], albeit with decreasing concentrations towards the surface. The insets of Figs. 4.7 (b) and (c) show the Si 2p core level XPS spectra collected at the same spot and same etching depth as where the C 1s spectra were measured. The results further confirm the existence of Si-C bonds within the SiO₂. We have computed the integrated area associated with the SiO_xC_y and Si-C bonds to compare the relative change in their

concentrations. It is found that the $\text{SiO}_x\text{C}_y/\text{Si-C}$ integrated area ratio has a value of 0.23 at a depth of 33 nm from the SiO_2 surface and 0.47 at a depth of 15 nm from the SiO_2 surface. Therefore, although the overall C 1s peaks weaken for points that are further away from the $\text{SiO}_2/4\text{H-SiC}$ interface, there are more SiO_xC_y bonds relative to Si-C bonds. The result can be interpreted in terms of the dynamic oxidation process that transforms Si-C bonds into SiO_xC_y bonds, which are then further oxidized to form SiO_2 and CO. This process occurs not only at the interface, but also in the bulk of the SiO_2 . Overall, the interface will shift further into 4H-SiC substrate and carbon will diffuse out of the SiO_2 in the form of CO.

In conclusion, our XPS results on the variation of the bonding and concentration of carbon throughout the oxide layer indicated the presence of carbon clusters (C-C bonds) only at the interface, and there are also SiO_xC_y and Si-C bonds found in the bulk of the SiO_2 . It may be possible to minimize the carbon components in the SiO_2 by re-oxidation at lower temperature over an extended period of time. This will help remove the carbon in the SiO_2 , and yet prevent any further oxidation of the 4H-SiC substrate.

4.5 Effects of N_2O Nitridation Temperature on Interface Traps

In this section, the nitridation results of thermal SiO_2 on 4H-SiC carried out using diluted N_2O at temperatures from 900°C to 1100°C are presented. The samples were characterized by high frequency capacitance-voltage (C-V) and AC conductance measurements. The trap time constant of majority carriers and the capture cross section of the traps [54] at the $\text{SiO}_2/4\text{H-SiC}$ interface are also investigated. The information

obtained will be helpful in providing a better understanding of the nature of the interface states.

Thermal oxidation of N-type 4H-SiC wafers were carried out using ultra-pure O₂ (99.999%) at 1100°C for 3 hours after a conventional RCA cleaning process and 1 min dip in 5% hydrofluoric acid. Upon oxidation, the wafers were further annealed in diluted N₂O (10% N₂O in N₂) for 3 hours at 900°C, 1000°C, and 1100°C. N₂O instead of NO was used for the nitridation as it is an industry-preferred ambient and has been shown to give better D_{it} results [32, 74]. Aluminum was thermally evaporated, and patterned as gate electrodes (area = 1.8×10^{-4} cm²) to form MOS capacitors. The experimental conditions for electrical characterization are exactly the same as those presented in Chapter three.

Nitridation Temperature (°C)	SiO ₂ Thickness (nm)	Flatband Voltage (V)	Effective Oxide Charge (C/cm ²)
900	17.6	3.7	4.5×10^{12}
1000	17.7	2.7	3.3×10^{12}
1100	18	4.1	4.9×10^{12}

Table 4.4 Characteristics of MOS capacitors deduced from HF C-V curves for samples nitrided at different temperatures.

Fig. 4.8 Normalized high frequency C-V curves of samples nitrided at different temperatures.

Figure 4.8 shows the high frequency capacitance-voltage (C-V) curves of the three samples, normalized to the SiO_2 capacitance. The gate voltage was swept from accumulation to depletion. Table 4.4 lists the SiO_2 thickness, flat-band voltage and effective oxide charge calculated from the high frequency C-V curves. The SiO_2 thickness, deduced from the accumulation capacitance, increases very slightly with the nitridation temperature, which may be due to further oxidation at higher temperature. The sample nitrided at 1000°C has the smallest flat-band voltage of 2.7 V, and thus the smallest effective oxide charge.

The D_{it} of the samples measured with respect to the conduction band edge, deduced by the Terman's method [55] based on the high frequency C-V curves, are shown in Fig. 4.9.

Fig. 4.9 Energy distributions of interface states density in 4H-SiC band gap obtained by Terman's method.

As the C-V measurements were conducted at room temperature, only the D_{it} that is within 0.5 eV away from conduction band can be accurately established. It can be seen from the results that nitridation at 1000°C gives slightly lower D_{it} and thus better SiO₂/4H-SiC interface quality. The result is concordant with the lowest effective oxide charge obtained from this sample, as presented in Table 4.2. Nevertheless, overall it can be seen from Fig. 4.8 that nitridation at the temperature range from 900°C to 1100°C does not produce drastic differences in the interface states density. It is also noted that D_{it} of the nitrided samples which were oxidized at 1100°C are in trend with the D_{it} of those samples shown in Fig. 4.5 oxidized from 950°C to 1150°C without nitridation. Therefore, we conclude that the nitridation of our samples in diluted N₂O does not produce any significant

difference to the interface quality. In literature, nitric oxide (NO) or nitrous oxide (N₂O) is widely studied. NO nitridation is reported to be helpful to remove interface states density of SiO₂/SiC interface [4]. In term of N₂O nitridation, there are contradict results. Some authors claim that N₂O is effective to improve the interface quality of SiO₂/SiC. [61,74]. There are also results claim that N₂O is degrading the interface quality [75]. Our results show that diluted N₂O dose not make any dramatic difference to SiO₂/4H-SiC interface quality.

The AC capacitance C_m and conductance G_m were measured for the three samples at different angular frequency ω (125 Hz ~ 6.28 MHz). The results can be interpreted using the equivalent circuit that is commonly adopted [54]. The equivalent parallel conductance is given by [54]:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (4.3)$$

Using Eq. 4.3, the term G_p/ω can be determined using the measured G_m and C_m . It is related to the D_{it} by the following equation [54]

$$G_p / \omega = qAD_{it} \int_{-\infty}^{+\infty} \frac{\exp\{-\xi^2 / (2\sigma_g^2)\}}{\sqrt{2\pi}\sigma_g} \times \frac{\ln(1 + \omega^2 \tau^2 e^{-2\xi})}{2\omega\tau e^{-\xi}} d\xi \quad (4.4)$$

where q is the electronic charge, A is the electrode area, D_{it} is the number of interface states per unit area and per electron-volt, σ_g is the standard deviation of the surface potential caused by fluctuations of the interface states, τ is the trap time constant of the interface states and ξ is the surface potential. The parameters D_{it} , τ and σ_g in Eq. 4.4 are fitted to produce a good match between the theoretical and experimental G_p/ω curves.

Fig. 4.10 Equivalent parallel conductance, G_p , normalized to the angular frequency ω as a function of angular frequency ω . The points are experimental values and the curves are the best fitted theoretical data (for sample nitrided at 1000°C).

Figure 4.10 illustrates the fitting results for the sample nitrided at 1000°C measured at different dc gate bias voltages V_g from 0.9 V to 1.7 V. Similar good fits are also obtained for the other two samples. Figure 4.11 shows the D_{it} deduced by the AC conductance method with reference to the conduction band edge energy. Similar to the results obtained using Terman's method, the sample nitrided at 1000°C has the lowest D_{it} among the three samples. In absolute terms, the D_{it} obtained from the Terman's method is slightly higher near conduction band ($E_C - E < 0.3$ eV). Indeed, the Terman's method is known to result in an over-estimation of the D_{it} , especially near the conduction band edge, as it relies on the theoretical C-V curve and assumes that the D_{it} do not respond to the AC signal [76].

Fig. 4.11 Energy distributions of interface states density in 4H-SiC band gap obtained from AC conductance method.

Figure 4.12 plots the trap time constant as a function of energy. The trap time constant decreases with increasing nitridation temperature across the different energy levels investigated. It also increases with the energy of the trap deeper into the band gap. It is noted that the range of trap time constants observed in our samples is similar to those observed for SiO₂/Si system [77]. The reason for the decrease in the trap time constant with increasing nitridation temperature has also been observed for Si and is believed to be related to the nitrogen incorporated at the interface [77].

Fig. 4.12 Energy distributions of interface trap across section in 4H-SiC band gap obtained by AC conductance method.

The trap time constant is related to the trap capture cross-section and trapped electron emission rate by

$$\tau = \frac{1}{V_{th} \sigma_e N_d} \exp[\Phi_s / kT] \quad (4.5)$$

$$e_n = \frac{1}{\tau} \quad (4.6)$$

where V_{th} is electron thermal velocity of 4H-SiC, σ_e is the electron capture cross section, N_d is the doping concentration, Φ_s is the surface potential, k is the Boltzmann's constant, T is the temperature and e_n is the electron emission rate of traps [55,78]. Figure 4.13

shows the capture cross-section of the traps versus trap energy in the band gap. It is noted that high temperature nitridation increases the trap capture cross-section. However, there is only a slight difference in the capture cross-section between the two samples nitrided at 1000°C and 1100°C. The drastic decrease in the trap capture cross section towards the conductance band edge is noted to be similar to results observed for SiO₂/Si interfaces [79,80].

Fig 4.13 Energy distributions of interface trap capture cross-section in 4H-SiC band gap obtained by AC conductance method.

It is known that N₂O decomposes at high temperature to produce N₂, O₂ and NO with relative concentrations that depend on the pressure and temperature in the oxidation furnace. Consequently there are two competitive processes: passivation of the interface by nitridation (mainly NO) and further oxidation. The former improves the interface

quality, while the latter produces new SiO₂ layer and interface. The initial decrease in D_{it} from 900°C to 1000°C may be attributed to the nitridation process, while the subsequent increase from 1000°C to 1100°C may be due to further oxidation, as a result of enhanced N₂O decomposition to O₂. This oxidation process produces more oxycarbon compound and degrades the interface quality. There is therefore a trade-off between nitrogen incorporation at the interface and further oxidation of the SiC substrate in the nitridation process.

The nitridation results as a function of temperature show that higher temperature nitridation increases the trap emission rate. This behavior has also been observed for Si [79,80], however, the mechanism behind it as well as how the emission rate can be controlled, is still not fully understood. It has been suggested that nitridation annealing by nitric oxide (NO) or nitrous oxide (N₂O) may not physically remove the interface states densities, but instead shift the energies of those interface states in the band gap [81]. Therefore, nitridation annealing can remove the interface states detrimental effects.

It is reported that the capture cross section (σ_e) is a function of interface states energy [81]. In this study, the sample nitrided at 900°C gives highest interface states density, which means that there is relatively less nitrogen incorporated at the SiO₂/4H-SiC interface. Thus, it is expected that there is less shift of the interface states to energy levels outside of the energy gap of 4H-SiC [4]. Therefore, the capture cross section (σ_e) for the 900°C annealed sample is smaller as there are relatively more interface states at the SiO₂/4H-SiC interface. For samples annealed at 1000°C and 1100°C, as the interface states density

is quite close in near the conduction band, the σ_e values for those two therefore are also almost in same level. More efforts are needed to clarify the exact reason beyond the increase in the trap emission rate.

4.6 Summary

In this chapter, thermally grown SiO_2 on 4H-SiC was examined as a gate dielectric for potential device application. Ellipsometry was used to investigate the optical constant of thermal SiO_2 on 4H-SiC. It is found that there exists a transition layer between SiO_2 and 4H-SiC, which has a higher optical constant than pure SiO_2 . The thermal oxidation temperature has an influence on the transition layer 4H-SiC volume fraction, with a higher oxidation temperature resulting in a lower 4H-SiC volume fraction. By x-ray photoelectron spectroscopy, it is found that C-C bonds only exist at the SiO_2 /4H-SiC interface in our 4H-SiC samples oxidized at 1100°C . Whereas in the SiO_2 , only SiC_xO_y and Si-C bonds are observed. For points further away from the SiO_2 /4H-SiC interface into the SiO_2 , there are more SiO_xC_y bonds relative to Si-C bonds. This result can be attributed to the dynamic oxidation process that transforms Si-C bonds into SiO_xC_y bonds, which are then further oxidized to form SiO_2 bonds. Samples of thermal oxide on 4H-SiC formed at 1100°C were nitrided using N_2O at different temperatures from 900°C to 1100°C . It is found that the nitridation at 1000°C gives relatively low interface state density. The trap capture cross section was also investigated by the AC conductance method and it is found that higher temperature nitridation results in larger capture cross section.

Chapter 5 Alternative Dielectrics on 4H-SiC

5.1 Introduction

In recent years, great effort has been put into investigating thermal SiO₂ on 4H-SiC for device application [3,29,56]. Though the interface states density of SiO₂/4H-SiC and fixed charges in thermal SiO₂ have improved over the years, they are still too high for practical MOS application. Thus, besides thermal SiO₂, researchers have also looked into other dielectrics as alternative to SiO₂. The review of alternative dielectrics investigated has been presented in Chapter two. In this chapter, silicon nitride (SiN_x), tantalum pentoxide (Ta₂O₅), and aluminum nitride (AlN) have been investigated as gate dielectrics for 4H-SiC metal-insulator-semiconductor (MIS) application. Electrical and physical measurements were carried out for these potential gate materials.

5.2 PECVD Deposited Silicon Nitride (SiN_x)

At present, the oxidation of 4H-SiC produces poor SiO₂/4H-SiC interface quality and suffers from slow oxidation rate compared to the oxidation of Si [3, 29]. To overcome these problems, alternative dielectrics can be considered to form 4H-SiC based MIS structure. Motivated by the improvement of interface states density after introducing nitrogen into the SiO₂/4H-SiC interface [1], we study silicon nitride, which is widely used in Si processes, as a potential good candidate for 4H-SiC MIS application due to the abundant nitrogen in the dielectric. In this section, we present results on the study of SiN_x grown by the plasma enhanced chemical vapor deposition (PECVD) technique as gate dielectric for 4H-SiC MIS structure. The 4H-SiC used for the fabrication of MIS

capacitor consists of a 10 μm epitaxial layer ($N_d = 2 \times 10^{15} \text{ cm}^{-3}$) grown on Si-face 4H-SiC bulk wafer ($N_d = 5 \times 10^{19} \text{ cm}^{-3}$). Before thermal oxidation, the wafers were cleaned using conventional RCA technique followed by a 1 minute dip in 5% HF acid to remove the native SiO_2 . NH_3 , SiH_4 , N_2 are used in our PECVD system to deposit SiN_x . As it has been shown that nitrogen is helpful in reducing the interface states density for SiO_2 /4H-SiC structure [4], therefore, a larger nitrogen concentration in the SiN_x is preferred. We used a series of different flow rates for the gases, which are summarized in Table 5.1. Other deposition conditions were fixed as follows: pressure: 800 mTorr; temperature: 300°C; rf power: 60W.

Sample	NH_3 Flow Rate (sccm)	SiH_4 Flow Rate (sccm)	N_2 Flow Rate (sccm)	FTIR Area Ratio (Si-N/N-H)
1	50	100	500	13.52
2	50	50	500	21.008
3	50	10	500	22.366
4	50	100	1000	16.989

Table 5.1 Deposition conditions for a- SiN_x .

The bonding configurations in the films have been characterized using Fourier Transform Infrared Reflectometry (FTIR). The results are shown in Fig. 5.1, including the assignments of the various absorption peaks. The labeling of the samples in terms of 1 to 4 in Fig. 5.1 is the same as that shown in Table 5.1.

Fig. 5.1 FTIR result of deposited a-SiN_x

In Figure 5.1, the peaks at the wavenumber of 850 cm⁻¹, 1200 cm⁻¹, and 3340 cm⁻¹ are assigned to Si-N stretching mode, N-H rocking mode, and N-H stretching mode respectively [82,83]. The peaks of N-H (1200 cm⁻¹) and Si-N (850 cm⁻¹) were fitted with Gaussian lineshape functions and their integrated areas were calculated to determine the relative nitrogen concentration. Before the fitting, the linear background was eliminated for each sample. To ensure that we have a large amount of N in the SiN_x layer, we would require a high concentration of Si-N bond in the films. We have compared the integrated absorption area ratio associated with Si-N and N-H, the results of which are shown in Table 5.1. It can be seen that more Si-N bonds relative to N-H bonds are found in sample 3, which can be attributed to the largest N₂/SiH₄ and NH₃/SiH₄ flow rates ratio used compared to the other samples. Therefore, we have selected the flow rates used for

sample 3, but with the N₂ flow rate further increased to 1000 sccm to maximize the presence of N in the films, that is NH₃: SiH₄: N₂= 50:10:1000, to deposit the SiN_x layer to be used in our MIS structure. The silicon nitride films were deposited using the above gas flow rates for 12 minutes, which resulted in a film thickness of 80nm. After the deposition, the samples were annealed in N₂ at 500°C, 700°C, 900°C for 30 mins to improve the interface quality. Aluminum was evaporated and patterned as gate electrode (area = 1.8 × 10⁻⁴ cm²) for the MIS capacitors. C-V and I-V measurements were conducted at room temperature under dark condition to characterize the structures.

Fig. 5.2 C-V curves for samples annealed at different temperatures.

Figure 5.2 shows the high frequency C-V curves of the three samples with different annealing conditions, as well as the sample that was unannealed. It can be clearly seen that only for the sample annealed at 700°C that the C-V curve reveals accumulation,

depletion, and deep depletion regions. This means that annealing at 700°C results in better interface quality in the annealing temperature range investigated. The improvement in the interface quality with annealing temperature from the unannealed samples to those annealed at 700°C can be explained by the decrease in the Si dangling bond in the SiN_x film and at the interface [84]. At annealing temperature higher than 700°C, the deterioration of the C-V curve is attributed to the increase in the Si dangling bonds, which is believed to be associated with the release of trapped hydrogen from microvoids in the SiN_x [84]. This trapped hydrogen removal is different from hydrogen atom release at lower annealing temperature. The release of hydrogen trapped in microvoids of the structure will lead the degradation of the electrical characteristics by leaving behind unpassivated internal surfaces [6].

The C-V hysteresis measurements were conducted for the sample annealed at 700°C, and the results are shown in Fig. 5.3. The frequency of the measurement was set at 1 MHz. As can be seen in Fig. 5.3, the negligible shift between the two C-V curves means that the slow trap density in our sample is negligible. Otherwise, there would be a significant shift between the C-V curves arising from the response of the slow traps to the sweep in the dc bias voltage applied. From Fig. 5.3, it can be seen that the flatband voltage is quite large. This means that there are still quite a lot of fixed charges in the annealed SiN_x film which may come from the Si dangling bond defects in the films [84]. Further improvement on the deposition condition is needed to reduce them.

The interface states density of sample annealed at 700°C was deduced by the Terman's method at room temperature, and the results are shown in Fig. 5.4. The D_{it} value is around $1.25 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at around 0.2 - 0.3 eV from the 4H-SiC conduction band, which is slightly lower than the value of SiO₂ grown by thermal oxidation on 4H-SiC as presented in Chapter four. The lower interface states density may be due to the absence of complex intermediate oxide/carbon compound at the SiN_x/4H-SiC interface, as the carbon related defects are believed to give rise to fast interface states that are shallower in energy [36]. However, at 0.3 - 0.45 eV (check the range of the cross-over) away from 4H-SiC conduction band edge, the D_{it} of the SiN_x sample annealed at 700°C is higher than the value in SiO₂/4H-SiC sample. This may be attributed to the dangling bonds at the SiN_x/4H-SiC interface. Overall, our results have shown that SiN_x is a potential dielectric for 4H-SiC based MIS application as proper accumulation and depletion regions can be observed in the high frequency C-V curve. It is possible that the Si dangling bonds in the SiN_x can be further reduced by optimizing the deposition and annealing conditions. It should also be noted that as the permittivity of SiN_x is higher than that of SiO₂, SiN_x/4H-SiC is more suitable for high voltage application than SiO₂/4H-SiC, as the latter will suffer from enhanced electric field when a large voltage is applied to the structure.

Fig. 5.3 High frequency C-V curves for SiN_x annealed at 700°C.

Fig. 5.4 Interface state density from Terman's method for sample annealed at 700°C.

5.3 Ta₂O₅ Based Dielectric Stack

For 4H-SiC MOS application, the field strength in the insulator is scaled by a factor of $\varepsilon(4\text{H-SiC})/\varepsilon_i$, where $\varepsilon(4\text{H-SiC}) = 9.7$ and ε_i is the relative dielectric constant of the insulator. In the case of SiO₂/4H-SiC, the electric field in SiO₂ is larger than that in 4H-SiC by a factor of 2.5, which is equal to the ratio of their dielectric constants. Due to the excellent dielectric strength of 4H-SiC, the maximum blocking voltage of 4H-SiC MOS structures is limited by the gate SiO₂ breakdown instead of 4H-SiC breakdown. This poses a serious reliability problem for the gate SiO₂. This problem can be alleviated by using alternative insulating materials with higher dielectric constants, such as SiN_x, Al₂O₃ and AlN [85,86]. Other dielectrics with even higher dielectric constants (high k), such as HfO₂, have also been investigated to further reduce the electric field in the dielectrics, and also to increase the capacitance [43].

In this section, the results of 4H-SiC metal-insulator-semiconductor (MIS) structure using tantalum pentoxide (Ta₂O₅) as the dielectric are presented. The Ta₂O₅ was deposited by the pulsed DC magnetron sputtering technique. Ta₂O₅ is attractive as it has a high dielectric constant of about 20 and high chemical and thermal stabilities [87]. It is a relatively mature dielectric extensively used in high-density dynamic random access memories (DRAMs) and as gate dielectric in thin film transistors [88]. Moreover, its growth process based on sputtering is also compatible with the current Si technology.

The Ta₂O₅/4H-SiC MIS structures investigated were found to exhibit rectifying current-voltage (I-V) characteristics. This is quite commonly observed for high k dielectrics as

generally they do not have very large band gaps and hence will result in small band offset at the dielectric/4H-SiC interface [43]. To alleviate this problem, in this work we have also introduced a thin layer of large band gap thermal SiO₂ to form Ta₂O₅/SiO₂/4H-SiC MIS structures. This has lowered the leakage current by about one order of magnitude. Substantial improvement has been obtained when the Ta₂O₅ was subjected to oxygen annealing at 900°C for 30 minutes. Besides I-V measurement, high frequency capacitance-voltage (C-V) measurements were also used to characterize the samples.

The wafers used in this work consist of a 10 µm epitaxial layer ($N_d = 2 \times 10^{15} \text{ cm}^{-3}$) grown on Si-face 4H-SiC substrates ($N_d = 5 \times 10^{19} \text{ cm}^{-3}$) purchased from CREE Inc. The samples underwent the RCA cleaning as stated in section 5.2. For those samples with a layer of thermal SiO₂ introduced, the wafers were first oxidized using ultra-pure O₂ (99.999%) at 1150°C for 1 hour. The SiO₂ thickness was determined to be 8~10 nm from ellipsometry measurements. The samples with and without thermal SiO₂ layer grown were loaded into a Unaxis LLS EVO pulsed DC magnetron sputtering system for Ta₂O₅ deposition at room temperature. The films were formed by sputtering a tantalum target (purity of 99.95%) using a gas mixture of high purity Ar (99.9995%) and O₂ (99.999%), with both having the same flow rate of 100 sccm. Typical thickness of the Ta₂O₅ films deposited is 60 nm. For electrical measurements, aluminum was thermally evaporated and patterned as gate electrode (area = $1.8 \times 10^{-4} \text{ cm}^2$) and back contact to form MIS capacitors. High frequency capacitance-voltage (C-V) measurements were carried out using the same condition as stated in section 4.2. The dielectric constant of the Ta₂O₅ was determined from the accumulation capacitance of the Ta₂O₅/4H-SiC MIS structure to be about 20. To

improve the quality of the as-deposited Ta₂O₅ and the interface between Ta₂O₅ and SiO₂, some of the samples were annealed in oxygen at 900°C for 30 mins.

Figure 5.5 shows the I-V characteristics of the Ta₂O₅/4H-SiC MIS capacitor, where the Ta₂O₅ is as deposited without any further annealing. A large injection current is observed when the gate voltage (V_g) exceeds 4 V with respect to the n+ substrate. The optical band gap (Tauc gap) of the Ta₂O₅ was determined to be around 4.3 eV using the spectroscopic ellipsometry. Therefore, the injection current is attributed to the small band offset and hence small barrier height at the Ta₂O₅/4H-SiC interface. Thus, when positive voltage is applied on the gate (> 4 V), electrons are accumulated at the Ta₂O₅/4H-SiC interface.

Figure 5.5 I-V characteristics of Ta₂O₅/4H-SiC MIS structure.

Due to the small barrier height from 4H-SiC to Ta₂O₅, electrons are injected from the 4H-SiC into the Ta₂O₅ and give rise to the current observed. Indeed, no current injection was observed for the same Ta₂O₅ formed on Si substrates, as the barrier height is much larger due to the smaller band gap of Si [89].

Figure 5.6 shows the I-V characteristics of the Ta₂O₅/SiO₂/4H-SiC MIS capacitors. The as-deposited sample still exhibits a current injection under positive V_g . However, the current density at the same V_g is about one order of magnitude lower compared to the Ta₂O₅/4H-SiC MIS capacitors without the SiO₂ layer, as shown in Fig. 5.5.

Figure 5.6 I-V characteristics of Ta₂O₅/SiO₂/4H-SiC MIS structure without and with annealing

From Fig. 5.6, it is shown that the Ta₂O₅/SiO₂/4H-SiC MIS capacitors post-annealed at 900°C do not reveal any current injection behavior. It is known that for Ta₂O₅/Si structures, an interface layer of SiO₂ will be formed after annealing which resulted in lower leakage current [90,91]. For our Ta₂O₅/SiO₂/4H-SiC structure, a thin layer of SiO₂ has already been intentionally introduced, as it is not easier for 4H-SiC to form oxide compared to Si. The improvement in the leakage current is likely due to the effects of the thermal annealing on the Ta₂O₅ and the Ta₂O₅/SiO₂ interface, in terms of lowering the defects and improving their quality. [90] In Fig. 5.6, the leakage current of the annealed samples, even at V_G up to 15 V is less than 1×10^{-6} A/cm². At $V_G = 15$ V, the electric field inside the Ta₂O₅ and SiO₂ layer are determined to be 1.29 MV/cm and 7.29 MV/cm respectively. For a similar voltage, devices using SiO₂ as the sole layer of dielectric would not have functioned due to the very high electric field developed in SiO₂. Therefore, our results reveal the potential advantages of using the Ta₂O₅/SiO₂ dielectric stack for 4H-SiC MIS structures.

High frequency C-V measurement was used to evaluate the interface quality of SiO₂/4H-SiC. Figure 5.7 shows the 1 MHz high frequency capacitance-voltage (C-V) curves for the as-deposited and annealed Ta₂O₅/SiO₂/4H-SiC MIS capacitors normalized to the accumulation capacitance. The gate voltage was swept from accumulation to depletion, then immediately back from depletion to accumulation.

Figure 5.7 C-V characteristics of Ta₂O₅/SiO₂/4H-SiC MIS structure without and with annealing.

The C-V curves of the annealed samples reveal a small flat band voltage of about 2.0 V with minimal hysteresis, compared to 9.4 V for the as-deposited sample. The slope of the C-V curves in the depletion range is comparable for the two samples with and without annealing, which means that the interface states density level do not significantly change after annealing. The much smaller flat band voltage of the annealed sample indicates that the high temperature annealing is effective in removing the fixed charge inside the Ta₂O₅ layer. The reduced hysteresis suggests a relatively low density of slow charge traps in the annealed samples.

Figure 5.8 Interface states density of Ta₂O₅/SiO₂/4H-SiC MIS structure without and with annealing deduced by the Terman's method.

Figure 5.8 shows that density of interface states calculated from the high frequency C-V curve for the as-deposited and annealed Ta₂O₅/SiO₂/4H-SiC samples using the Terman's method [55]. As the C-V measurements were taken at room temperature, only a shallow range of D_{it} from the conduction band edge can be accurately established. Due to the insulating nature of the Ta₂O₅/SiO₂ stack, the transfer of charge during the C-V measurements occurred between the top metal electrode and the SiO₂/4H-SiC interface, hence the D_{it} deduced reflects the interface state density at the SiO₂/4H-SiC interface. The interface state density was noted to improve slightly after the high temperature anneal, which may be attributed to the re-oxidation of the SiO₂/4H-SiC interface, which has been shown to slightly reduce the interface states density [92].

In this section, the sputtered Ta_2O_5 combining with a thin SiO_2 layer has been shown to be a possible dielectric material for 4H-SiC MIS application. With optimization of the growth and annealing conditions for Ta_2O_5 , it is possible that the electrical characteristics of the $\text{Ta}_2\text{O}_5/\text{SiO}_2/4\text{H-SiC}$ MIS capacitors can be further improved to render it as an attractive candidate for high power 4H-SiC based MIS devices.

5.4 Density of Defect States of Aluminum Nitride Grown on Silicon and Silicon Carbide Substrates at Room Temperature

Aluminum nitride (AlN) has played an increasing role in microelectronics, such as in surface acoustic wave filters [93], blue light photodiodes and photodetectors [94], field-effect [95] and high-electron-mobility [96] transistors. It may be a potential candidate for 4H-SiC based MIS application due to the high permittivity and relatively wider bandgap of AlN. Its successful application requires a good understanding of its physical properties, which are closely related to features of its density of single-electron states $N(E)$, both within and beyond its bandgap. The features of $N(E)$ are primarily determined by the microstructure of AlN films. It has also been reported that the type of substrate and its crystalline orientation are also critical factors that determine the properties of the AlN layers grown [97,98]. At present, influences of the substrates on the $N(E)$ of AlN deposited have not been comprehensively studied.

This section is devoted to the experimental investigation of the distribution of relatively shallow defect states in thin AlN films. The films were deposited by radio frequency (RF,

13.56 MHz) magnetron sputtering of Al target in an argon-nitrogen (Ar-N₂) mixture using the Denton-18 system. The pure Al (99.9995%) disk has a round form with 3-inch diameter and 0.25-inch thickness. The total gas pressure at deposition varied from 3.0 to 8.0 mTorr for different nitrogen flow rates. The substrates used include <100> oriented crystalline silicon (Si) wafers (P-type, 1-10 Ω -cm) and N-type 4H silicon carbide (4H-SiC) wafers (Si face, 8° off-axis toward the <11 $\bar{2}$ 0>orientation) which comprise 400 μ m thick nitrogen doped n⁺ substrate ($N_d = 5 \times 10^{19} \text{ cm}^{-3}$) and 10 μ m thick n-epilayer ($N_d = 3 \times 10^{15} \text{ cm}^{-3}$). Two different substrates were used as the properties of AlN grown on them under the same deposition conditions may differ considerably because of fundamental differences in their spatial symmetry and composition. The Si and 4H-SiC wafers were cleaned using conventional RCA technique followed by a 1-minute dip in 5% hydrofluoric acid to remove the native SiO₂ prior to deposition. The sample holder was not intentionally heated during the deposition. The nominal substrate temperature was found to be very close to room temperature. A series of films were deposited with the nitrogen flow rate varied from 4.0 to 20.0 sccm while keeping the Ar flow rate constant at 10 sccm. The RF power was fixed at 300 W and the deposition time set at 30 minutes. These conditions have resulted in deposited AlN films with thickness in the range of 40 – 60 nm. Aluminium (Al) was deposited on both the top and bottom surfaces of the AlN/P-Si and AlN/N-4HSiC sandwiched structures using the same sputtering system. The top Al layer was deposited immediately upon the completion of the AlN growth without vacuum breaking. Standard wet lithography was employed to form circular top Al electrodes with diameter of 1 mm. The deposition of the back-side Al had been done simultaneously for

all the samples to avoid any possible changes to the metal deposition conditions that may influence the electrical properties of the resultant structures.

Deep-level-transient spectroscopy (DLTS) technique was applied to investigate the $N(E)$ of the AlN films. A 'Bio-Rad' DL8000 system was used for the 'capacitance' DLTS measurements of the sandwich metal-insulator-semiconductor structures of Al/AlN/P-Si/Al and Al/AlN/N-SiC/Al. These measurements have been performed in the temperature range of 20 - 315 K at a frequency of 1 MHz. Two different algorithms for the $N(E)$ spectra deconvolution from 'raw' DLTS data have been applied: Mellin-transform-based 'regularization' algorithm [99] and standard Fourier-transform-based algorithm [100].

The $N(E)$ spectra deconvoluted from the DLTS data are given in Figs. 5.9 and 5.10 for AlN grown on Si and 4H-SiC substrates respectively. The conduction band edge E_C of AlN is taken as the reference (zero) energy level, and the spectra deduced are for states nearer to the conduction band since N-type direct current (DC) conductivity dominates in AlN crystals [101]. As can be seen, there is a reasonable quantitative agreement between the two techniques in deducing the $N(E)$ of the AlN layers grown on both the Si and 4H-SiC substrates.

FIG. 5.9 (a), (b). Distribution of density of defect states in AlN films grown on silicon substrates as deduced from DLTS data via the Mellin-transform-based ‘regularization’ algorithm (lines) and standard Fourier-transform-based algorithm (symbols). The AlN layers were deposited at different flow rates of nitrogen as indicated. Filled rectangles indicate the energy levels of the nitrogen vacancy triplet.

The peaks I and III seen in Figs. 5.9 (a) and (b) can be identified as donor-like defect levels originated from nitrogen vacancy in AlN [102,103,104]. The energies that correspond to the triplet of this vacancy are indicated by filled rectangles in Fig. 5.9 (a), (b). The peak II that is located over the energy range $E_c - E = 0.35 - 0.42$ eV obviously differs from the levels of the nitrogen vacancy. Most probably such defects are caused by the so-called DX-centers [105,106], which are formed in AlN in the presence of Si atoms. The activation energy of these defects can range from 0.39 to 0.45 eV [106], which is quite close to what we have observed. The DX-centers in our samples can be created in the vicinity of the AlN/Si interface. This idea is indirectly supported by the fact that this peak is practically absent in the AlN films deposited on 4H-SiC substrates over the same nitrogen flow rates of 4 – 6 sccm (see Fig. 5.10(a)). Although the surface of the 4H-SiC wafers is also terminated with Si atoms, however, the cohesive energy of Si-C bond (6.66 eV) is considerably larger than that of Si-Si bond in silicon (4.84 eV) [107]. Thus, the probability of Si atoms involvement in the formation of such defect centres in AlN is higher for the layers grown on Si.

FIG. 5.10 (a), (b). Distribution of density of defect states in AlN films grown on 4H-SiC substrates as deduced from DLTS data via the Mellin-transform-based ‘regularization’ algorithm (circles) and standard Fourier-transform-based algorithm (lines). The AlN layers were deposited at different flow rates of nitrogen as indicated.

The general shape of the $N(E)$ distributions in Fig. 5.10(a) and (b) differs from those in Figs. 5.9(a) and (b), though the defect peaks at $E_c - E = 0.73 - 0.80$ eV are probably also originated from nitrogen vacancy. The differences can be accounted for in terms of the structural quality of AlN layers grown on Si and 4H-SiC substrates. In-plane lattice mismatch of hexagonal 4H-SiC and AlN is only about 0.9% [98], whereas there are fundamental differences in the spatial symmetry of lattices of AlN and Si. As a result, AlN layers grown on 4H-SiC are expected to contain less defects and imperfections compared to similar films grown on Si. These deductions are in qualitative agreement with the $N(E)$ spectra shown in Figs. 5.9(a) and (b) and 5.10(a). Firstly, there are only two prominent peaks located at $E_c - E \approx 0.1$ eV and $0.73 - 0.80$ eV seen in Fig. 5.10(a), compared to three peaks observed in Figs. 5.9(a) and (b). Secondly, the intensity of the most prominent $N(E)$ peak in Figs. 5.9(a) and (b) and 5.10(a) is higher for the Si based than the 4H-SiC based structures. Therefore, it is reasonable to conclude that the structural quality of the AlN layers is higher when grown on 4H-SiC substrates.

It is noted that relatively low defect density and consequently high structural quality are observed for AlN grown on 4H-SiC within a limited range of nitrogen flow from 4.0 to 8.0 sccm. At higher nitrogen flow rates a prominent and broad defect peak appears at $E_c - E = 0.15 - 0.45$ eV (Fig. 5.10(b)). It could be caused by dangling bonds of nitrogen atoms in 'non-stoichiometric' AlN films deposited at large nitrogen flow rates. Nitrogen dangling bonds could also be formed because of partial substitution of Si-Si and Si-C bonds at the AlN/substrate interfaces with Si-N bonds, due to the higher bonding energy of Si-N bonds [108]. The chemical valency of silicon and sp^3 -hybridized carbon atoms is

four, while for nitrogen atoms it is five. Consequently, some of the valence bonds of newly attached nitrogen atoms will remain unsaturated (dangling). The energies of such dangling bonds in the defect spectra of hydrogenated amorphous silicon (a-Si:H) is normally placed at 0.1 – 0.3 eV below E_c [109]. The energies of such defects in AlN could be shifted towards midgap because of the significantly larger bandgap of AlN (6.2 eV in crystalline sample) compared to a-Si:H (about 1.7-1.8 eV for high-quality material).

The $N(E)$ distributions in AlN layers grown on Si and 4H-SiC substrates reveal a high density of shallow defects with $E_c - E = 0.05 - 0.15$ eV. For some samples these states are practically overlapped with the conduction band tail (see Fig. 5.9(b) and 5.10(b)). For ‘stoichiometric’ AlN deposited on 4H-SiC such shallow defect levels are clearly separated from the conduction band tail (see Fig. 5.10(a), for nitrogen flow rate of 5 and 6 sccm). In our opinion, such shallow defects can be originated from ‘prismatic stacking faults’ reported recently by Northrup [110]. The energy level of such defects was predicted to be about 0.1 eV below E_c [110], which is in reasonable quantitative agreement with the energy level of the shallow peak observed in our results.

5.5 Summary

In this chapter, several dielectrics are investigated for 4H-SiC MIS structure. SiN_x deposited by PECVD was optimized and it is found that the interface state density value is slightly improved in the range of 0.2 eV from the conduction band of 4H-SiC comparing with the value of thermal SiO_2 . But in the range of 0.2~0.5 eV from the conduction band of 4H-SiC, the SiN_x shows worse interface states density comparing

with the value of thermal SiO_2 . High-k material Ta_2O_5 , due to the smaller band offset, is examined in a dielectric stack with thermal SiO_2 . After high temperature annealing, the leakage of the dielectric stack is much improved comparing with the leakage of as deposited sample. It is found that the interface states density determined by the Terman's method on the annealed Ta_2O_5 stack is slightly higher than that of thermal oxide reported in Chapter four. RF Sputtered AlN was deposited on 4H-SiC and Si. DLTS was used to evaluate the deep energy traps in AlN deposited on 4H-SiC and Si. The defect densities of AlN are lower when grown on 4H-SiC substrates than on Si substrates. Defects located at 0.35 - 0.42 eV below the conduction band, attributed to dangling bonds of nitrogen atoms, are seen in samples grown with higher nitrogen flow rate. Shallow level defects, observed at approximately 0.1 eV below the conduction band, can be attributed to the recently discovered prismatic stacking fault in the AlN atomic structure.

Chapter 6 Design, Fabrication and Characterization of 4H-SiC Based FET

6.1 Introduction

The excellent physical properties of silicon carbide (SiC) and the fact its native oxide is SiO₂ render it ideally suited for the fabrication of high-voltage and high-temperature metal oxide semiconductor field effect transistors (MOSFETs) [2]. SiC enhancement-mode MOSFET with different device structures have been demonstrated in recent years [111,112,113,114]. Despite the enormous research effort, the performance of 4H-SiC based MOSFETs reported has not reached a level suitable for practical application [114, 115,26]. This is mainly due to the low inversion channel mobility, attributed to the defective interface between SiO₂ and 4H-SiC [12,22]. Various methods have been proposed to circumvent the poor inversion layer mobility, which include high temperature annealing in nitric oxide (NO) [4,6] and hydrogen post-oxidation annealing [5,28]. Nevertheless, the inversion layer mobility reported so far in the range of 15~45 cm²/Vs is still too low for practical MOSFETs application [115,116]

Depletion mode MOSFETs have been proposed as one possible way to avoid the problem of low inversion layer mobility in enhancement MOSFETs [124, 117, 118, 119]. Such devices would have a structure very similar to metal semiconductor field effect transistor (MESFET), except that the Schottky gate is replaced by a MOS gate that comprises a thermally grown SiO₂ layer. The conduction of current is through the majority carriers in

a physical channel, which have much higher channel mobility, rather than the minority carriers in an inversion layer. In addition, such depletion mode MOSFETs can also operate in accumulation mode. There are several advantages associated with such devices. Firstly, the scattering of electrons due to the poor $\text{SiO}_2/4\text{H-SiC}$ interface quality is mitigated since the conduction is through the physical channel layer instead of a very thin inversion layer near the interface. Secondly, the device can be biased with large positive gate voltages (V_{GS}) to get strong electron accumulation in the n-channel, and give rise to a drain current beyond what can be achieved based on a similar MESFET device. A large positive V_{GS} is not possible in MESFETs as it will lead to forward biasing of the Schottky gate. Thirdly, higher input impedance and lower leakage current are expected due to the presence of the insulating SiO_2 layer, compared to a conventional MESFET. In a previous work on depletion mode MOSFETs, the bulk carrier mobility and accumulation layer mobility were determined by hall measurement, and the former was found to be higher than the latter [120]. The relatively low accumulation layer mobility observed is mainly due to the trapping of the accumulation carriers by the interface states. Detailed study on such depletion mode devices have been carried out in 6H-SiC [121,122] and a model for the drain current has also been presented. [122] In this chapter, we will fabricate and characterize 4H-SiC depletion mode MOSFETs and deduce the drift mobility of electrons in the accumulation and depletion regimes as a function of the gate voltage from the current-voltage characteristics of the devices [119,124].

6.2 Process Integration

To fabricate the depletion-mode MOSFETs, a micro-fabrication process was developed in a class 100 clean room. The main fabrication process consists of the following steps: (1) cleaning of 4H-SiC wafer; (2) forming of mesa isolation structure; (3) recess etching to form channel; (4) growth of SiO₂ gate dielectric; (6) forming of source and drain contacts and (7) gate metal deposition. In these steps, the lift-off process was used to transfer the mask pattern onto the processed wafer. In the source and drain electrode formation, a self-aligned process was used. In the following, the lift-off and self-aligned process will be introduced, and the detailed information on the main fabrication process will then be presented.

6.2.1 Lift-off Process

In semiconductor wafer fabrication, the term “lift-off” refers to the process of creating patterns on the wafer surface through an additive process, as opposed to the more familiar patterning techniques that involve subtractive processes, such as etching [14]. Lift-off is most commonly employed in patterning metal films for interconnections. As a patterning technique, “lift-off” process offers the following advantages: (1) Composite layers consisting of several different materials may be deposited one material at a time and then ‘patterned’ with a single “lift-off”. (2) Problems related to residues that are difficult to remove are avoided since there is no etching of the patterned layer. (3) Sloped side walls are possible, resulting in good step coverage. On the other hand, the main disadvantage of the lift-off process lies in the difficulty of creating the required stencil patterns for successful lift-off.

Depending on the type of lift-off process used, the patterns can be defined with extremely high fidelity and for very fine geometries. To achieve good lift-off process, the following conditions are necessary: (a) During film deposition, the substrate does not reach temperatures high enough to burn the photoresist. (b) The film quality must not be adversely affected by the outgassing of the photoresist, which is inevitable in vacuum systems. (c) Adhesion of the deposited film on the substrate must be very good. (d) The film can be easily wetted by the solvent. (e) The film is thin enough and/or grainy enough to allow solvent to seep underneath. (f) The film is not elastic nor thin and/or brittle enough to tear along adhesion lines.

Figure 6.1 illustrates the lift-off process used in this work. Photoresist AZ5214E was used to form a negative wall profile using its image reversal property, although it is in fact a positive photoresist. To begin the process, a layer of AZ5214E was coated onto a clean wafer with 4000 rpm for 30 sec as shown in Fig. 6.1 (a). It was then baked at 105°C on a hotplate for 95 seconds. The resulting photoresist thickness was around 1.1 ~1.3 μm . After that, the mask pattern was transferred to the resist using the Karl Suss mask aligner with an exposure energy of 14 mJ/cm^2 for 4 seconds. Then, the wafer was hard baked in an ultraclean oven at 110°C for 8 minutes. This step was very critical for the whole lift-off process, since a special crosslinking agent in the resist formulation becomes active in the exposed areas. This together with the exposed photoactive compound led to an insoluble and light insensitive substance.

Fig. 6.1 Basic instruction of lift-off process.

On the other hand, the unexposed areas still behaved like a normal unexposed positive photoresist. It should be noted that this reaction was active only for a hardbake temperature of 110°C or beyond. However, it should not be higher than 130°C , otherwise, the resist will thermally cross-link in the unexposed areas and result in no pattern formed on the wafer. After the hard bake, the wafer was subject to flood expose. The unexposed areas in the first exposure were dissolved in standard developer for positive photoresist and with the crosslinked areas remained. The overall result was a negative image of the mask pattern formed, as shown in Fig. 6.1 (b). After that, metal film was directly

deposited on the top of the patterned photoresist using e-beam evaporation, which is shown in Fig. 6.1 (c). After metal deposition, the unwanted metal was lifted off by dissolving the underlying photoresist in acetone, as shown in Fig. 6.1 (d). In the 4H-SiC MOSFET fabrication, this process was used to form the metal mask for mesa and recess etching, as well as source, drain and gate metal contacts.

6.2.2 Self-Aligned Process

Self-aligned process is widely used in IC fabrication [14]. The steps involved in the self-aligned process in this work are almost similar to those in the lift-off process, except that there is one additional etching of SiO_2 to open the source and drain window. After that, metal was deposited within the source and drain area.

6.2.3 Starting Wafer and Cleaning

The wafers used in this work were purchased from CREE Inc. The wafer consists of the following sequential layers: a semi-insulating substrate; a P-type buffer layer ($0.5\ \mu\text{m}$, $N_a = 1.0 \times 10^{15}\ \text{cm}^{-3}$); a N-type channel layer ($0.28\ \mu\text{m}$, $N_d = 2.4 \times 10^{17}\ \text{cm}^{-3}$); and a highly doped N-type cap layer ($0.2\ \mu\text{m}$, $N_d = 1.0 \times 10^{19}\ \text{cm}^{-3}$). The thickness and doping of the multi-epilayers were analyzed using secondary ion mass spectrometry (SIMS) measurement provided by Charles Evans & Associates. The SIMS results for the nitrogen (N) and aluminum (Al) concentration in the wafer are shown in Figs. 6.2 (a) and (b) respectively. The N concentration of $2.0 \times 10^{16}\ \text{cm}^{-3}$ in the buffer layer corresponds to the SIMS N detection limit and hence does not reflect the actual N concentration, which is believed to be much lower. The wafers were diced into $1\text{cm} \times 1\text{cm}$ for device fabrication.

Fig. 6.2 SIMS result of the 4H-SiC wafer used for device fabrication: (a) N and (b) Al.

Wafer surface cleaning is very critical in modern IC fabrication. In this work, the wafer was cleaned before each process step. The wafer was directly degreased in acetone, isopropanol, and de-ionized (DI) water under ultrasonic conditions for 15 mins each. This was to remove photoresist or any grease that may remain on the sample surface. The acetone removed unhardened photoresist and grease while isopropanol was mainly used for degreasing and dissolving acetone. After that, the wafer was cleaned using Radio Corporation of America (RCA) process. The RCA cleaning technique has three major steps which are listed as follows. (1) $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{NH}_4\text{OH} = 5 : 1 : 1$ solution for 15mins at 80°C . This step serves to remove insoluble organic contaminants. (2) $\text{H}_2\text{O} : \text{HF} = 50 : 1$ solution for 1 min. This step is to strip the silicon dioxide layer. (3) $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{HCl} = 5 : 1 : 1$ for 15 mins at 80°C . This step is to clean ionic and heavy metal atomic contaminants. Finally the wafer was dried in an oven at 110°C for 30 mins prior to further processing.

6.2.4 Mesa Isolation and Channel Recess Etching

Metal mask (30 nm Ti and 200 nm Ni) was used in the etching process in this work. The metal mask was deposited on the 4H-SiC wafer to cover the active region using the lift-off process. Reactive ion etching (RIE) was used to etch all 4H-SiC epilayers to reach the semi-insulating substrate to form mesa isolation. The RIE recipe of 4H-SiC is based on a gas mixture of $\text{CHF}_3\text{-O}_2$. The details of the recipe are as follows: rf power is 200W, process pressure is 100 mTorr, total gas flow rate is 10 sccm and the O_2 gas flow rate is 2 sccm. The resulting etching rate of this recipe is 35.6 nm/min. After etching, the metal mask was removed by hydrofluoric acid (HF) and the wafer was subjected to the RCA

cleaning process. In the next step, a metal mask was deposited using the lift-off process and the channel region was opened for recess etching. The N^+ top layer was etched by RIE and after recess etching, the metal mask was removed by HF and subsequently the wafer was cleaned by the RCA process.

6.2.5 Gate SiO_2 Thermal Oxidation

After recess etching, there is surface damage on the etched region due to the physical ion bombardments. A surface sacrificial oxidation process was used to remove this damage. After that, thermal oxidation to form gate SiO_2 layer was conducted at 1150°C for 6 hrs, which was then followed by nitrogen annealing for 1 hr. The gate oxide does not undergo any nitridation processes, such as annealing in nitric oxide (NO) or nitrous oxide (N_2O) further. The resulting gate SiO_2 thickness is 50 nm. The final channel thickness was around $0.12\text{ }\mu\text{m}$, carefully designed to be approximately equal to the maximum depletion width of the channel when a large negative gate voltage (V_{GS}) is applied, to ensure that it can be fully depleted.

6.2.6 Formation of Source and Drain Contacts

After thermal oxidation, the SiO_2 layer on the source and drain regions need to be removed for the formation of ohmic contacts. The self-aligned process was used in this step. The oxide was patterned and wet etched to open the source and drain contact regions. A 100 nm Ni/100 nm gold layer was deposited, and then underwent rapid thermal annealing at 970°C for 3 mins in a nitrogen ambient to form ohmic contacts.

6.2.7 Formation of Gate Contact

Similar to source and drain metal deposition, the gate metal was deposited using the lift-off process. A 200 nm layer of Ni was deposited to form the gate metal contact without further thermal treatment. The gate metal is located in the middle between the source and drain contacts.

After the five-step process, the device fabrication process was completed. The cross-sectional view of the fabricated depletion-mode 4H-SiC MOSFET is shown in Fig. 6.3.

Fig. 6.3 The cross-sectional view of depletion mode 4H-SiC MOSFET.

6.3 Characterization of Depletion Mode 4H-SiC MOSFET

6.3.1 Electrical Characterization of Depletion Mode 4H-SiC MOSFET

The DC characterization of the depletion-mode MOSFETs was carried out using a HP 4156B precision semiconductor parameter analyzer. The measured drain current I_{DS} against drain voltage V_{DS} characteristics with the source grounded are shown in Fig. 6.4.

Fig. 6.4 Drain current versus drain voltage measured at different gate voltages.

The gate voltage V_{GS} applied was varied from -1 V to 11 V, in step of 1 V. For V_{GS} less than the flatband voltage of $V_{FB} = 4 \text{ V}$, which was deduced separately from high frequency capacitance voltage ($C-V$) measurements, the device is in depletion condition and the channel thickness is modulated by the applied gate voltage V_{GS} . When V_{GS} decreases below V_{FB} , I_{DS} decreases as the physical channel is increasingly being depleted and eventually pinched off at $V_{GS} \approx -1 \text{ V}$, as can be seen from Fig. 6.4. Analysis of the leakage current between the gate and drain contacts confirmed that the small current observed at $V_{GS} = -1 \text{ V}$ arises from the leakage through the thermal SiO_2 layer. The MOSFETs fabricated are normally-on devices and in the operation regime of $V_{GS} \leq V_{FB}$,

they are very similar to MESFETs. For $V_{GS} > V_{FB}$, I_{DS} increases substantially due to the accumulation of electrons in the channel near the $\text{SiO}_2/4\text{H-SiC}$ interface. In this accumulation regime, specifically at $V_{DS} = 25$ V, I_{DS} is increased by about 3.3 times when V_{GS} is increased from 4 V (flat band condition) to 11 V. The possibility of operating in the accumulation mode to result in large drain current certainly renders such devices attractive for high power applications. Also note that a large dynamic range is possible for the input voltage V_{GS} , which is an added advantage of such depletion MOSFETs.

When operating in accumulation region, the drain current flows through both the accumulation layer and the physical channel layer. It can be written as a sum of the current in accumulation layer (I_{ACC}) and the current in physical channel (I_{CH}) [122]:

$$\begin{aligned} I_{DS} &= I_{ACC} + I_{CH} \\ &= -\frac{W}{L} \int_0^{V_{DS}} dV \mu_s Q_{acc} + \mu_n \frac{W}{L} q n_c \int_0^{V_{DS}} dV a^* \end{aligned} \quad (6.1)$$

In Eq. 6.1, μ_s is the electron mobility in the accumulation layer (surface mobility), μ_n is the channel bulk mobility, Q_{acc} is the charge density in the accumulation layer, W/L is the ratio of the width to the length of the active device and n_c is the electron density in the channel layer. a^* is the thickness of the bulk conduction channel which is given by $a^* = a - w_n$, where a is the physical channel layer thickness and w_n is the depletion width penetration into the channel layer arising from the channel-buffer junction. Taking into consideration the incomplete ionization of the dopants, w_n is determined to be about several nanometers. Given that a is about 0.12 μm , therefore we can neglect w_n and obtain $a^* \approx a$.

We define the y -axis as increasing from the source to the drain and with its origin set at the source. The local charge density $Q_{acc}(y)$ in the accumulation layer at a distance y is given by [122],

$$Q_{acc}(y) = -C_{ox} \left[V_{GS} - V_{FB} - \phi_s(acc) + \frac{Q_{it}}{C_{ox}} - V(y) \right] \quad (6.2)$$

where C_{ox} is the oxide capacitance, V_{FB} is the flatband voltage, $\phi_s(acc)$ is the accumulation surface potential, Q_{it} is the additional interface trapped charge between flatband and accumulation and $V(y)$ is the potential in the channel at a distance y . Under strong accumulation, the voltage drop due to the interface trapped charge (Q_{it}/C_{ox}) and the accumulation surface potential ($\phi_s(acc)$) can be neglected compared to the applied gate voltage V_{GS} [123]. Furthermore, by considering a very small drain voltage V_{DS} , the potential along the channel $V(y)$ can also be neglected compared to V_{GS} . Therefore, $Q_{acc}(y)$ can be approximated as

$$Q_{acc}(y) = -C_{ox} (V_{GS} - V_{FB}) \quad (6.3)$$

Substitute Eq. 6.3 into Eq. 6.1 and integrate, we obtain the drain current as

$$I_{DS} = \mu_s C_{ox} \frac{W}{L} (V_{GS} - V_{FB}) V_{DS} + \frac{V_{DS}}{\rho L / (W a)} \quad (6.4)$$

$$\frac{1}{\rho} = q\mu_n n_c \quad (6.5)$$

where ρ is the resistivity of the bulk channel layer. As can be seen from Eq. 6.5, under the accumulation mode, the bulk channel layer can be treated as a resistor with a length of L and a thickness of a . It is to be noted that the first term in Eq. 6.5, that is the current in the accumulation layer I_{ACC} , is similar to what is commonly used for enhancement

mode MOSFETs, except that the threshold voltage is replaced by V_{FB} for the accumulation layer.

6.3.2 Accumulation Layer Channel Mobility and Physical Channel Mobility in Depletion

Figure 6.5 plots I_{DS} versus V_{GS} for small V_{DS} of 50 mV to 200 mV. As can be seen, I_{DS} exhibits two distinct slopes in the range of $-1 \text{ V} < V_{GS} < 4 \text{ V}$ and $V_{GS} > 4 \text{ V}$. The first range with a larger slope corresponds to the operation where the physical channel is depleted, while the second range with a smaller slope corresponds to the operation where an accumulation layer is formed. The voltage at the transition point between the two regimes corresponds to V_{FB} . It can be estimated from the graph as the intersection point of two extrapolated straight lines from the I_{DS} versus V_{GS} curves in the two regions of operation. As illustrated for the curves measured at $V_{DS} = 50 \text{ mV}$ and 100 mV , the flat band voltage is approximately 4 V. This value is close to that deduced from separate CV measurements.

By neglecting any influence in the channel mobility μ_n that could arise from different gate biases under accumulation condition, I_{CH} can be considered as a constant current independent of V_{GS} . Therefore as seen from Eq. 6.4 I_{DS} is linearly related to V_{GS} for different V_{DS} , and from the slopes the electron mobility in the accumulation layer μ_s can be determined. We have fitted the I_{DS} versus V_{GS} curves with straight lines at different V_{DS} from 50 mV to 200 mV, as illustrated in Fig. 6.5.

Fig. 6.5 Drain current versus gate voltage at small drain voltages of 50 mV to 200mV.

Two distinct slopes can be seen in the curves and the flat band voltage is estimated using the intersection point of two extrapolated straight lines.

The fitting was carried out over the range of V_{GS} much greater than V_{FB} ($V_{GS} > 7.0$ V) to ensure that the condition of strong accumulation is fulfilled. By using the known C_{OX} , W/L and V_{FB} values, the accumulation mobility was deduced consistently to be $\mu_s = 17.5 \pm 0.1$ cm²/Vs from the best fitted slopes over the range of $V_{DS} \leq 200$ mV investigated [124]. This value of μ_s can be treated as average accumulation mobility over the range of $V_{GS} > 7.0$ V. The electron mobility in the accumulation layer deduced is comparable to what had been reported for the inversion layer of enhancement mode 4H-SiC MOSFET [9]. It is noted that in a previous work on 4H-SiC MOSFETs, the field effect mobility measured under strong accumulation was found to about 5 cm²/Vs [120], about 3 times

lower than the values obtained for our devices. Considering the gate oxide of our device was not nitridated by NO or N₂O, nor optimized for high interface quality, it is possible to further improve this accumulation mobility. It is also noted that a previous work on similar devices fabricated using 6H-SiC had deduced an electron mobility of 94.0 cm²/Vs in the accumulation layer using the larger first slope of the I_{DS} versus V_{GS} curve [4]. As can be seen from our discussion, this is incorrect and can result in a grossly over-estimated mobility.

By setting $I_{DS} = 0$ in Eq. 6.4, we can obtain the intercept of the linear I_{DS} versus V_{GS} curve at the V_{GS} axis. It is given by

$$V_{GS0} = -\frac{a}{\rho \mu_s C_{ox}} + V_{FB} \quad (6.6)$$

and is independent of V_{DS} . Figure 6.6 plots I_{DS} versus V_{GS} , similar to Fig. 6.5, except over a much wider range of V_{GS} to reveal the intercept at the V_{GS} axis. At different V_{DS} , the linear extrapolation of the I_{DS} versus V_{GS} curves intercept at nearly a common point of $V_{GS0} = -17.4$ V, -17.4 V, -17.3 V and -17.1 V respectively as V_{DS} increases from 50 mV to 200 mV, in step of 50 mV. Therefore the V_{GS0} values deduced are indeed nearly independent of V_{DS} . This verifies the approximations made in deriving Eq. 6.4, as well as the assumption that μ_n is not sensitive to V_{GS} under the accumulation condition. By rearranging Eq. 6.6, and using Eq. 6.5, we obtain

$$\mu_n = \frac{\mu_s C_{ox}}{q a n_c} (V_{FB} - V_{GS0}) \quad (6.7)$$

from which the channel mobility μ_n can be determined. Based on the average accumulation mobility $\mu_s \approx 17.5$ cm²/Vs, and n_c which was experimentally deduced to be

$1.2 \times 10^{17} \text{ cm}^{-3}$ (to be explained shortly), the channel mobility μ_n was determined to be $110.5 \pm 0.5 \text{ cm}^2/\text{Vs}$ over the range of V_{DS} investigated from 50 mV to 200 mV. This value of μ_n can be treated as average channel mobility under strong accumulation condition.

Fig. 6.6 Drain current versus gate voltage at small drain voltages of 50 mV to 200mV. At different V_{DS} , the linear extrapolation of the I_{DS} versus V_{GS} curves intercept at nearly a common point.

Using the average channel mobility μ_n obtained, the channel current I_{CH} can be deduced and consequently the accumulation mobility μ_s can be determined as a function of V_{GS} using Eq. 6.4.

Fig. 6.7 Accumulation electron mobility plotted as a function of the gate voltage. The results deduced are consistent over the different small V_{DS} investigated.

The accumulation mobilities deduced are shown in Fig. 6.7 as a function of V_{GS} . As Eq. 6.4 was developed on the basis of strong accumulation, therefore, only the results obtained for V_{GS} much greater than V_{FB} ($V_{GS} \geq 7$ V) are meaningful and shown in Fig. 6.7. The μ_s versus V_{GS} results are rather consistent over the different small V_{DS} investigated, which further justifies the use of Eq. 6.4 in describing the drain current under strong accumulation. The fact that the μ_s deduced at different V_{DS} exhibit a wider spread at smaller V_{GS} , and eventually converge as V_{GS} increases provides another indication that Eq. 6.4 is valid only under the condition of strong accumulation. From Fig. 6.7, we note that generally there is a decrease in the electron mobility in the accumulation layer with

increasing V_{GS} . The decrease may be due to the enhanced scattering at the interface under higher V_{GS} . This decrease in mobility is similarly observed for inversion devices as the devices were increasingly biased from weak to strong inversion [125,126]. The electron mobility in the accumulation layer deduced lies in the lower range of values reported for the inversion layer of enhancement mode 4H-SiC MOSFET [127,124]. The lower mobility may be attributed to the poorer quality of the SiO_2 /4H-SiC interface, which was not treated with any nitridation.

Under depletion mode ($V_p < V_{GS} < V_{FB}$), where V_p is the pinch-off voltage, and small V_{DS} , the drain current flows through the physical channel and is given by

$$I_{DS} = \frac{V_{DS}}{\rho L / [W(a - W_d)] + R_D + R_S} \quad (6.8)$$

where W_d is the depletion width in the channel and R_D and R_S model the total drain and source resistances respectively. In the above we have neglected the depletion width penetration into the channel layer arising from the channel-buffer junction, which earlier on has been shown to be negligible compared to the channel thickness.

6.3.3 Channel Doping Concentration Determined by I-V Characterization

The depletion width of a MOS capacitor is given by [21]

$$W_d = \left[-\frac{2 \epsilon_s \phi_s}{q N_D^+} \right]^{1/2} \quad (6.9)$$

where ϵ_s is the permittivity of the semiconductor, ϕ_s is the band bending (negative for N-type substrate) and N_D^+ is the concentration of the ionized donor. The applied gate

voltage V_{GS} accounts for the flat band voltage, the voltages across the SiO_2 V_{ox} and the depletion region in the semiconductor ϕ_s ,

$$V_{GS} = V_{FB} + V_{ox} + \phi_s \quad (6.10)$$

In the above, the potential drop arising from any additional interface trapped charge between flat band and depletion is neglected, as it is expected to be negligible compared to the contribution from the depletion charge under the depletion mode of operation. V_{ox} is given by

$$V_{ox} = -\frac{Q_{dep}}{C_{ox}} = -\frac{N_D^+ W_d q}{C_{ox}} \quad (6.11)$$

where Q_{dep} is the depletion charge per unit area. Combing Eq. 6.9 to 6.11, we have

$$V_{GS} = V_{FB} - \frac{N_D^+ W_d q}{C_{ox}} - \frac{N_D^+ W_d^2 q}{2\epsilon_s} = V_{FB} - N_D^+ W_d q \left(\frac{1}{C_{ox}} + \frac{W_d}{2\epsilon_s} \right) \quad (6.12)$$

When there is no depletion layer formed, $W_d = 0$ and $V_{GS} = V_{FB}$. On the other hand, when the channel is fully depleted, $W_d = a$ and V_{GS} is equal to the pinch-off voltage V_p ,

$$V_p = V_{FB} - N_D^+ a q \left(\frac{1}{C_{ox}} + \frac{a}{2\epsilon_s} \right) \quad (6.13)$$

The above equation allows us to determine the ionized donor concentration N_D^+ . Using $V_p = -1.0$ V, $V_{FB} = 4.0$ V, $a = 0.12$ μm and other parameters of the MOS capacitors, N_D^+

was deduced to be $1.2 \times 10^{17} \text{ cm}^{-3}$. Arising from the incomplete ionization of donors, we have $N_D^+ < N_D$, and they are related by the following equation [128]

$$N_D^+ = \frac{N_D}{1 + A (N_D / N_C) \exp(E_D / KT)} \quad (6.14)$$

where N_C is the effective density of state at the conduction band, E_D is the donor energy level and A is degeneracy factor. Taking the doping concentration N_D deduced from SIMS of about $2.4 \times 10^{17} \text{ cm}^{-3}$, $N_C = 1.7 \times 10^{19} \text{ cm}^{-3}$, $E_D = 0.084 \text{ eV}$ and $A = 2$ [128, 129] the calculated N_D^+ is $1.39 \times 10^{17} \text{ cm}^{-3}$, which is close to the value deduced experimentally. The difference may be due to experimental errors involved in the determination of V_p , V_{FB} and a , as well as the uncertainty in the values of the parameters used in Eq. 6.14.

Equation 6.12 can be rearranged and expressed as

$$\frac{q N_D^+}{2 \epsilon_s} W_d^2 + \frac{N_D^+ q}{C_{ox}} W_d + (V_{GS} - V_{FB}) = 0 \quad (6.15)$$

from which the depletion width can be calculated as follows

$$W_d = -\frac{\epsilon_s}{C_{ox}} + \frac{1}{2} \sqrt{\left(\frac{2\epsilon_s}{C_{ox}}\right)^2 - \frac{8\epsilon_s}{q N_D^+} (V_{GS} - V_{FB})} \quad (6.16)$$

Using the above equation and the N_D^+ of $1.2 \times 10^{17} \text{ cm}^{-3}$, it is possible to determine the variation of the depletion width of the device as a function of V_{GS} .

Fig. 6.8 Drain current at small drain voltages measured at different V_{GS} in the depletion region. Linear relations can be seen between V_{DS} and I_{DS} .

6.3.4 Determination of Channel Mobility under Depletion Mode Operation

Using Eq. 6.8, we can determine the channel mobility under depletion mode as a function of V_{GS} . Figure 6.8 plots I_{DS} versus V_{DS} in the depletion mode with $V_{GS} \leq 4 \text{ V}$. For small V_{DS} the channel can be modeled as a series combination of the channel resistance and R_D and R_S (see Eq. 6.8). This is supported by the linear relation observed between I_{DS} and V_{DS} , as illustrated in Fig. 6.8 over the range of $2.0 \text{ V} \leq V_{GS} \leq 4.0 \text{ V}$. From the best fitted straight lines, the total resistance which is given by the inverse of the slope can be deduced. For $V_{GS} < 2.0 \text{ V}$ the I_{DS} versus V_{DS} curves do not exhibit a good linear relation

as the channel is substantially depleted and hence this range is not considered in our analysis. Using Eq. 6.8 and $\mu_n \approx 110.5 \text{ cm}^2/\text{Vs}$ deduced earlier under strong accumulation condition, $R_D + R_S$ is determined to be $324.5 \text{ } \Omega$ under the flat band condition ($V_{GS} = 4 \text{ V}$). Assuming that the source and drain resistances remain nearly constant when the channel is increasingly depleted, we can determine the channel mobility under depletion mode using Eq. 6.8, and the results are shown in Fig. 6.9. The increase in μ_n at decreasing V_{GS} has been observed previously in similar 6H-SiC buried channel devices [121], attributed to fact that with an increase in the depletion width, the carriers are further away from the SiO_2 interface and hence experience less scattering.

A previous work on 4H-SiC MOSFETs has reported a lower field effect mobility of about $27 \text{ cm}^2/\text{Vs}$ for the channel under depletion mode [120]. A more recent report on 4H-SiC lateral junction field effect transistors (JFETs) of similar channel doping has obtained channel mobility ranging from $70 \text{ cm}^2/\text{Vs}$ to $398 \text{ cm}^2/\text{Vs}$ depending on the channel opening and the channel length [130]. This is comparable with the range deduced in this work of about $110.8 \text{ cm}^2/\text{Vs}$ to $130.8 \text{ cm}^2/\text{Vs}$.

6.4 Summary

In this chapter, 4H-SiC based depletion-mode MOSFET has been fabricated and characterized by DC I - V measurements. By applying different gate voltages, the device can operate in depletion mode or accumulation mode. Using the I_{DS} - V_{DS} characteristics measured in both the depletion as well as the accumulation regions, the average electron mobilities in the accumulation layer and the bulk channel layer have been determined to

be about 17.5 cm²/Vs and 110.5 cm²/Vs respectively. Based on the model developed, the mobilities were further determined as a function of the gate voltage and the doping density in the channel layer was also deduced.

Fig. 6.9 The bulk channel mobility deduced as a function of the gate voltage when the device operates in the depletion mode.

Chapter 7 Conclusion and Recommendation

7.1 Conclusion

This project investigated the interface quality of SiO_2 /4H-SiC and explored how it can be improved for device application. Thermal oxidation of 4H-SiC at different temperatures and post-annealing of the oxidized samples in diluted nitrous oxide (N_2O) were carried out to study their effects on the properties of the SiO_2 /4H-SiC interface. Through ellipsometry study, it was found that there exists a transition layer between SiO_2 and 4H-SiC that has a higher optical constant than pure SiO_2 . Modeling the transition layer using the effective medium approximation (EMA), it was also noted that higher oxidation temperature had resulted in a relatively lower 4H-SiC volume fraction in the layer. Using X-ray photoemission spectroscopy (XPS), it was found that C-C bonds only exist at the SiO_2 /4H-SiC interface, whereas in the SiO_2 layer, only SiC_xO_y and Si-C bonds were observed. Furthermore, for points further away from the SiO_2 /4H-SiC interface, there were more SiO_xC_y bonds observed relative to Si-C bonds. This result can be attributed to the dynamic oxidation process that transforms Si-C bonds into SiO_xC_y bonds, which were then further oxidized to form SiO_2 bonds. On the nitridation of the samples in the temperature range from 900°C to 1100°C , it was found that nitridation at 1100°C gave relatively low interface state density and higher temperature nitridation had resulted in interface states with smaller cross section constant.

Besides thermally grown SiO_2 on 4H-SiC, other dielectrics such as SiN_x deposited by plasma enhanced chemical vapor deposition (PECVD) technique, sputtered Ta_2O_5 were

examined. SiN_x deposited by the plasma enhanced chemical vapor deposition (PECVD) technique was optimized and it was found that the interface state density around 0.2 eV from the conductance band of 4H-SiC is slightly lower than that of thermal oxide formed on 4H-SiC. But the SiN_x results in higher interface states density value around 0.5 eV from the conductance band of 4H-SiC when comparing with that value of thermal oxide. High-k Ta_2O_5 films were deposited using the pulsed DC magnetron sputtering system. Due to the lower bandgap of Ta_2O_5 and consequently the smaller band offset between Ta_2O_5 and 4H-SiC, a thin layer of thermal SiO_2 was inserted in between to lower the leakage current. Under high temperature post-deposition annealing, the breakdown field in the dielectric stack was found to be higher than pure SiO_2 . RF Sputtered AlN was deposited on both 4H-SiC and Si substrates, and Deep-level-transient spectroscopy (DLTS) was used to evaluate the deep energy traps and their dependence on the substrate type. The defect densities of AlN were found to be lower when grown on 4H-SiC substrates than on Si substrates. Defects located at 0.35 - 0.42 eV below the conduction band, attributed to dangling bonds of nitrogen atoms, were seen in samples grown with higher nitrogen flow rate. Shallow level defects, observed at approximately 0.1 eV below the conduction band, can be attributed to the recently discovered prismatic stacking fault in the AlN atomic structure.

Based on those results on dielectrics, we have also explored the application of depletion mode metal oxide semiconductor field effect transistors (MOSFETs). 4H-SiC based depletion-mode MOSFETs had been fabricated and characterized by current-voltage measurements. Such devices operate under depletion and accumulation modes and hence

do not suffer from the problem related to low inversion layer mobility. Using the I_{DS} - V_{DS} characteristics measured in both the depletion as well as the accumulation regions, the average electron mobilities in the accumulation layer and the bulk channel layer have been determined to be about 17.5 cm²/Vs and 110.5 cm²/Vs respectively. A conduction model has been purposed for this depletion mode MOSFET. Based on the model developed, the mobilities were further determined as a function of the gate voltage and the doping density in the channel layer was also deduced.

7.2 Recommendations for Future Research

Though 4H-SiC based MOSFETs have attracted much attention in recent years, practical 4H-SiC MOSFET still have not been realized for integrated circuit (IC) application. This work includes three major parts: thermal SiO₂ based dielectric investigation, study of alternative dielectric materials, and fabrication and characterization of depletion mode MOSFETs. The following investigations are recommended for future study:

- Re-oxidation at lower temperature over an extended period of time is helpful to remove the carbon in the SiO₂, and yet prevent any further oxidation of the 4H-SiC interface. This process can minimize the carbon components in the SiO₂ and at SiO₂/4H-SiC interface, which is desired for improve the interface quality.
- Nitridation with NO in thermal SiO₂ has shown improvement in terms of lowering the SiO₂/4H-SiC interface states density. This is believed to be due to the formation of stronger Si≡N bonding at the interface. To incorporate more nitrogen at the interface, oxidation and annealing in NO at higher pressure can be carried

out using high pressure annealing system. Higher pressure can introduce more nitrogen at the interface as the oxidation is limited by the reaction species.

- Due to the excellent dielectric strength of 4H-SiC, the maximum blocking voltage of 4H-SiC metal-oxide-semiconductor (MOS) structures is limited by the gate SiO₂ breakdown instead of 4H-SiC breakdown. Thus, high dielectric materials are proposed to replace thermal oxide for 4H-SiC MOS application. Normally, the band gap of an insulator decreases with increasing dielectric constant [131]. Therefore, this will result in a low energy band offset between 4H-SiC and the high permittivity insulator. To overcome this problem, rare earth element oxide may be possible candidates as high permittivity gate dielectrics on 4H-SiC, for example, Ruthenium oxide (RuO₂).
- For 4H-SiC based MOSFET application, the main barrier is still the low inversion channel mobility due to the low quality SiO₂/4H-SiC interface. Thus, depletion mode MOSFETs may be a possible solution for this problem. Though our results on 4H-SiC depletion-mode MOSFETs have shown that the accumulation layer mobility is still too low, nitridation of SiO₂ by growth or annealing in NO may be a possible way to improve the accumulation layer mobility.

Author's Publications

Journal Papers

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3. **P. Zhao**, Rusli, B. K. Lok, F. K. Lai, C. C. Tin, J. H. Zhao, R. M. Yar, "Investigation of Ta₂O₅/SiO₂/4H-SiC MIS capacitors", *ICMAT 2005*, Vol. 83, pp. 58-60, 2006.
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