Direct conversion 2.4-GHz receiver front end design for wireless applications

Do, Aaron

2006

Do, A. (2006). Direct conversion 2.4-GHz receiver front end design for wireless applications. Master's thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/46876>

<https://doi.org/10.32657/10356/46876>

Nanyang Technological University

Downloaded on 26 Apr 2023 18:24:38 SGT

4435673

Direct Conversion 2.4-GHz Receiver Front End Design for Wireless Applications

Aaron Do

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Master of Engineering

2006

~~2005~~

TK
7871.58
.B74
D631
2006

ACKNOWLEDGEMENTS

I have come a long way in my research towards this thesis since I picked up my first RFIC design book, and I could not have reached this stage without the generous support of several mentors and friends.

First and foremost I would like to acknowledge the help of my two principal mentors, my supervisor, Prof. Zhang Yue Ping and my father, Prof. Do Manh Anh. Both professors provided useful advice and insights drawn from their own experience in the communications area. Among my mentors I would also like to thank Prof. Ma Jian Guo for enduring the brunt of the endless and often repetitive questions I posed.

I cannot overemphasize my thanks to Ms. (soon to be Dr.) Jia Lin who solved countless problems which arose throughout my research and allowed me to use her VCO design in my project. Finally, I would like to thank Mr. (soon to be Dr.) Li Qiang, the technical staff of CICS, IC Design I and IC Design II, and my original research group for help during the project.

CONTENTS

Acknowledgements	i
Contents	ii
Thesis Abstract	vi
List of Figures	viii
List of Tables	x
1. Introduction	1
1.1 Motivation	1
1.2 Objectives	2
1.3 Main Contributions of Thesis	3
1.4 Organization	4
2. Performance Measures and Architectures	6
2.1 Performance Parameters	6
2.1.1 Power Consumption	6
2.1.2 Gain	7
2.1.3 Noise Figure	8
2.1.4 Linearity	9
2.1.5 Cascaded System	12
2.1.6 LO Leakage and DC Offset	14
2.1.7 Reverse Isolation and Matching	15
2.2 Architecture	16

2.2.1	High-IF Receiver	16
2.2.2	Low-IF Receiver	17
2.2.3	Zero-IF Receiver	19
2.2.4	Friis Equation Modification	23
3.	State of the Art	26
3.1	LNA Design	26
3.2	Mixer Design	28
3.3	DC Offset Correction and Reduction	29
3.3.1	AC Coupling and DC Coupling with DC Feedback	29
3.3.2	Harmonic Mixing	30
3.3.3	Digital Calibration	31
3.4	Problems in Current Design and Project Goal	31
4.	Inductive Degeneration LNA Design	33
4.1	Two-Port Noise Theory	33
4.1.1	Noise Resistance and Conductance	33
4.1.2	The Generic Two-Port Network	34
4.2	Inductive Degeneration LNA Design	35
4.2.1	The Standard Design	35
4.2.2	Gain	39
4.2.3	Noise Figure	43
4.2.4	Linearity	47

5.	Mixer Design	49
5.1	DC Offset	50
5.2	The Active Mixer	52
5.3	Passive Mixers	54
5.4	Novel Design	60
6.	Differential Design	64
6.1	Current Reuse	64
6.2	A Novel Current Reuse Method	67
7.	Results	71
7.1	The LNA	73
7.2	Standard Front End	78
7.3	Novel Front End	82
7.4	Summary	87
8.	Layout for Testability	89
8.1	Design Symmetry	89
8.2	Shielding	89
8.3	Component Placement	90
8.4	Layout for Equipment Conformity	91
8.5	Post-Layout Simulation	93

9.	Conclusion and Further Work	97
9.1	Further Work	98
	Author's Publications	100
	References	101

Thesis Abstract

The 2.4 GHz ISM (industrial scientific and medical) band is a worldwide unlicensed band commonly used for WLAN (Wireless Local Area Network). Apart from 802.11b, 802.11g, and Bluetooth, the 2.4 GHz band is used for various dedicated short range communications systems which do not follow mainstream standards. Modern RF front-ends must meet rising demands of small form factor, low cost and long battery life in mobile systems. This all points to the elusive system-on-a-chip concept which aims to integrate the RF front-end with the data converters and the digital baseband processing unit using the low-cost standard CMOS process. The Direct Conversion Receiver (DCR) has been identified as the architecture best suited for full system integration. This follows from the few components and the possibility of eliminating off-chip components. For mobile systems, the major problems in direct conversion front end design are low-frequency flicker noise, DC-offset, and power consumption. In this thesis, we aim to tackle the noise figure problem while maintaining low power operation. We also provide a possible solution to the DC-offset problem.

In this thesis, we first prove that the minimum possible noise figure of a DCR or low-IF receiver given noiseless components is 3 dB. This follows from the information loss due to random phase mismatch between the LO (local oscillator) and RF signal in DCRs and the superposition of image noise on channel noise in low-IF receivers. A modified Friis equation (noise figure of a cascaded system) is presented which applies to all low-IF or zero-IF receivers. A full analysis of two-port noise theory and LNA and mixer operation

is then presented. Based on this analysis, a method for optimizing LNA noise figure and input matching is proposed. Using this method, it is possible to design a matched, sub 2 dB noise figure LNA. We then make a comparison between active and passive mixers which shows that the active mixer degenerates into a passive mixer and an amplifier when low flicker noise design techniques are used. Typically active mixers use current injection and increased LO voltage to lower the output flicker noise. When low flicker noise techniques are not used, the active mixer exhibits high DC-offset. We then present a novel circuit design technique to greatly reduce DC-offset arising from LO self-mixing. In theory this method can reduce both LO-IF and LO-RF leakage without bound. After the fundamental flaw in harmonic mixers is exposed, it is concluded that the novel method is the best circuit design technique for reducing DC-offset. To address the problem of power consumption, a novel current reuse method is presented which leads to a 1.6 mA Low Noise Amplifier (LNA) with the performance of a 5 mA design. The ideas presented are used in the design of a fully integrated double balanced front end (LNA, Mixer) using device models extracted from the same fabricated devices. The design has passed the post-layout simulation stage and will be fabricated and tested.

LIST OF FIGURES

Figure 2.1: Cascaded Noise Figure	13
Figure 2.2: High-IF Front End	16
Figure 2.3: Low-IF Receiver	18
Fig. 2.4: Cascaded Noise Illustration	25
Figure 4.1: Two Port Noise Representation	34
Figure 4.2: Inductive Degeneration LNA	37
Figure 4.2: Simple Small Signal Inductive Degeneration Matching Stage	38
Figure 4.4: MOSFET Noise Models	43
Figure 5.1: LO leakage Illustration	50
Figure 5.2: Gilbert Cell	52
Figure 5.3: Passive Mixer Topologies	53
Figure 5.4: Source Input Impedance	54
Figure 5.5: Drain Input Impedance	55
Figure 5.6: LO-RF Isolation of Topology 1 ($V_{LO} = 250$ mV)	56
Figure 5.7: LO-RF Isolation of Topology 2 ($V_{LO} = 250$ mV)	57
Figure 5.8: Standard Front End Performance Degradation with Isolation	58
Figure 5.9: Novel Design Performance Degradation with Isolation	59
Figure 5.10: Novel Single Balanced LNA, Buffer and Mixer	60
Figure 5.11: LO-IF Isolation versus Load Capacitance	61
Figure 6.1: Current Reuse Method	64
Figure 6.2: Low Noise Mixer	66
Figure 6.3: Alternative Current Reuse Configuration	67

Figure 6.4: Combined Gain, Phase Difference (A) and Gain Difference (B)	68
Figure 6.5: LNA Noise Figure (A) and S11 (B)	69
Figure 7.1: Front End Test Bench	71
Figure 7.2: Modified Test Bench for LNA Testing	73
Figure 7.3: LNA Voltage Gain	74
Figure 7.4: LNA Noise Figure	75
Figure 7.5: LNA Input Return Loss	75
Figure 7.6: LNA Schematic	76
Figure 7.7: Standard Front End	78
Figure 7.8: Single Sideband Noise Figure	79
Figure 7.9: Standard Front End Voltage Gain	80
Figure 7.10: Standard Front End Isolation	81
Figure 7.11: Novel Front End	83
Figure 7.12: Novel Front End Single Sideband Noise Figure	84
Figure 7.13: Novel Front End Voltage Gain	85
Figure 7.14: Novel Front End LO leakage	86
Figure 8.1: Shielding	89
Figure 8.2: Wafer Probe Station Layout	90
Figure 8.3: Final Probe Station Layout	91
Figure 8.4: Final Design Layout	92
Figure 8.5: Post-Layout Voltage Gain	93
Figure 8.6: Post-Layout Noise Figure	94
Figure 8.7: Post-Layout LO leakage	95

LIST OF TABLES

Table 3.1: State of the Art in LNA Performance	27
Table 3.2: State of the Art in Mixer/Front End Performance	28
Table 5.1: Simulated RF Front End isolation	61
Table 6.1: LNA and Phase Splitter Performance	68
Table 7.1: Component Parameters	76

CHAPTER 1

INTRODUCTION

1.1 Motivation

The 2.4 GHz ISM (Industrial Scientific and Medical) band is a worldwide unlicensed band commonly used for WLAN (Wireless Local Area Network) applications [1]. Apart from 802.11b, 802.11g, and Bluetooth standards, the 2.4 GHz band is also used for various dedicated short range communications systems which do not follow mainstream standards. For mobile communications, the demands have been small size, long battery life and low cost. The solution to all of these problems is the full integration of the RF front end with the mixed signal circuits and the digital baseband circuits. This concept is known as System-on-Chip (SOC) [2]. The front end is the first stage of a receiver usually comprising a low noise amplifier (LNA), a mixer, and a filtering.

Among the possible technologies available for RFIC design are GaAs (Gallium Arsenide), SiGe (Silicon Germanium), SOI (Silicon on Insulator), Bipolar, and CMOS (Complementary Metal Oxide Semiconductor). Though GaAs, SiGe, Bipolar and SOI have clearly demonstrated better gain and noise performance than CMOS, CMOS remains as a popular process for RFIC design. Of the mentioned processes, only SiGe and CMOS offer the possibility of a single chip solution. Unfortunately, choosing SiGe leads to a high cost of production. Therefore, only CMOS offers the possibility of a low cost single chip solution. It is no surprise that although many RF devices were initially

designed in SiGe or GaAs, eventually are made in CMOS as witnessed in Bluetooth and 802.11 markets [3].

For Narrowband applications, there are three possible receiver architectures: high-IF, low-IF and zero-IF. The zero-IF receiver is also known as a homodyne or direct conversion receiver (DCR) and has received a lot of attention lately because it offers the possibility of a single chip design [4]. Unlike the high-IF or low-IF receivers, the homodyne receiver does not require that the signal go off-chip to get the necessary image rejection and good selectivity, and does not require a high speed Analog-Digital Converter (ADC). However, the DCR has problems of its own, such as LO self-mixing induced DC-offset and low-frequency flicker noise. While the flicker noise problem has largely been solved [5] in mixer design, there is no adequate solution to date for the DC-offset problem.

The theme of this study therefore is the design of direct-conversion receivers in CMOS, with emphasis on low-power, noise optimization and DC-offset reduction.

1.2 Objectives

The aim of this thesis is to design a Low-Noise Amplifier (LNA) and Mixer with features of low-noise, low-power, and low DC-offset. The designs will be done using the Chartered Semiconductor Manufacturing (CSM) 0.18 μm CMOS Process Design Kit (PDK) which uses device models based on measurements of the same fabricated devices.

The LNA will meet standard design requirements of gain, linearity, matching, and unconditional stability while showing improvement in noise figure at low power consumption. The Mixer will also meet these requirements while showing low LO self-mixing and low flicker noise. The RF front end will operate between 2.4 GHz and 2.5 GHz which satisfies all 2.4 GHz ISM standards.

1.3 Main Contributions of the Thesis

Several new ideas have been developed and are presented in this thesis. From the system standpoint, we prove that the minimum noise figure of a direct-conversion receiver is 3 dB. Because of this, we propose a necessary modification to the Friis equation for calculation of noise figure in cascaded systems employing DCRs.

We also present several novel circuit design techniques for optimization of noise, power consumption and DC-offset. In particular, we present a method for noise optimization in inductive degeneration LNAs. We also show that the active Mixer degenerates into an amplifier and a passive Mixer when flicker noise is minimized. We also present a novel Mixer topology which results in improved performance. To solve the problem of LO-self mixing induced DC-offset, we present a means to minimize LO-leakage to both IF and RF ports. Lastly, a novel current-reuse method is proposed for LNA-Phase-Splitter co-design which leads to a 30 % reduction in power consumption for the front ends employing active phase-splitting.

1.4 Organization

This thesis is organized into nine chapters including the introduction. Because the LNA and mixer were designed together, the analyses will take place in the earlier chapters and the results will be presented in chapter 7.

Performance Measures and Architectures: This chapter will first cover all the performance parameters which describe the LNA and Mixer, and then discuss the basic receiver architectures.

State of the Art: In this chapter, we present the state of the art in LNA design, Mixer design, and DC-offset correction methods.

Inductive Degeneration LNA Design: Here we will first cover the basics of two-port noise theory, and then we will present the inductive degeneration LNA and show how it can be optimized in terms of gain and noise figure.

Mixer Design: In this chapter, we present our comparison of active and passive Mixers. We also propose a novel passive Mixer topology which results in improved performance.

Current Reuse: This chapter introduces current reuse, which is a method to reduce power consumption. We also present a novel current reuse method for LNA-Phase-Splitter co-design.

Results: This chapter will present results obtained from simulation of the novel front end and standard front end.

Layout for Testability: In this chapter we cover layout design techniques necessary for successful circuit operation. We also discuss how layout was optimized for the available test equipment. Finally, we will present the post-layout simulation results.

Conclusion and Future Work: This chapter will summarize the work done and give insight to possible improvements in the proposed designs.

CHAPTER 2

PERFORMANCE MEASURES AND ARCHITECTURES

This chapter will briefly discuss the parameters typically used to assess a design's performance and the different receiver architectures.

2.1 Performance Parameters

In general, we are concerned with gain, noise figure, linearity, power consumption, reverse isolation, matching, LO-leakage, and DC-offset. Typically the designer must also ensure unconditional stability of the circuit and must keep the silicon area occupied by the circuit within constraints. In general unconditional stability can be ensured by removing any positive feedback loops and limiting the out-of-band gain. The silicon die size can be reduced by limiting the number of inductors and large capacitors, and practicing good layout techniques.

2.1.1 Power Consumption

Because the RF front end is always on, it is important to keep its power consumption low. The DC power consumption is found by taking the supply voltage multiplied by the DC current. For a mobile system, the battery operates at a fixed voltage level (typically 3.3 V, 2.5 V, or 1.8 V). Therefore, the only way to lower power consumption is by lowering the current consumption. Lowering the supply voltage requirements below that of the rest of

the system will not lower power consumption unless more than one supply voltage is used for the receiver.

For a MOSFET, the DC current can be adjusted by changing the biasing or changing the device size.

2.1.2 Gain

The power gain of an amplifier is the power delivered to the load divided by the power available at the input, where the power available at the input is the power delivered by the source when it is conjugate matched to the input [6].

$$P_{av} = \frac{V_s^2}{4R_s} \quad (2.1)$$

However, the maximum power gain is not achieved by a conjugate match between the source and the input [7]. This is because a MOSFET is a trans-conductance amplifier, not a power amplifier. Because of this, we are actually more concerned with the voltage gain than the power gain. At the ADC (Analog Digital Converter), the voltage level will be sensed and converted to a digital signal. We still, however, require good matching at the LNA input to prevent reflection of the received signal back to the antenna. The Voltage Gain (S_{21}) is calculated as,

$$S_{21} = 20 \log \left(\frac{V_{out}}{V_{in}} \right) \quad (2.2)$$

For a common source amplifier, the voltage gain is proportional to the input impedance, while for an inductive degeneration LNA, the voltage gain is inversely proportional to the input impedance. Since the impedance mismatch between the source and the input determines the return loss of the amplifier, there is a tradeoff between gain and return loss.

The trans-conductance (g_m) of a MOSFET is determined by the width to length ratio (W/L) and V_{gs} of the device [8]. So in general, there is a tradeoff between gain and power dissipation.

2.1.3 Noise Figure

The noise performance of a system is measured by the noise factor (F), or the noise figure (NF) which is F expressed in decibels. From the IEEE definition [6],

$$F = \frac{\text{(total output noise power)}}{\text{(output noise power due to source noise)}} \quad (2.3)$$

This applies when the source is at a temperature of 290 K. The input source is usually a 50 ohm source. Therefore the input noise is only the noise generated by the 50 ohm resistance. Thus regardless of the input source, under matched conditions the available noise power will equal kTB , where k is Boltzmann's constant, T is the absolute temperature and B is the concerned bandwidth. The alternate definition which is [9],

$$F = \frac{\text{Output Signal to Noise Ratio}}{\text{Input Signal to Noise Ratio}} = \frac{SNR_{in}}{SNR_{out}} = \frac{\text{Output Noise Power}}{G * \text{Input Noise Power}} \quad (2.4)$$

is misleading since it implies that the output noise is always equal to the input noise multiplied by a factor $F.G$, where G is the gain. This is only true when all the input noise is generated by the source impedance. Therefore, even if the noise figure of a circuit is 3 dB, the overall noise figure can be less depending on the preceding stage's gain and noise figure.

For the Mixer, we are primarily concerned with lowering the flicker noise which is dominant below 1 MHz [6]. Flicker noise increases with DC current consumption. Although there is no universally accepted flicker noise equation, one possible model is [10],

$$i_{fD}^2 = k_f \frac{I_D^{A_f}}{f \cdot C_{ox} \cdot L_{eff} \cdot W_{eff}} \cdot \Delta f \quad (2.5)$$

where A_f is the flicker noise exponent, k_f is the flicker noise component, C_{ox} is the oxide capacitance, L_{eff} is the effective channel length, W_{eff} is the effective channel width, Δf is the bandwidth, f is the frequency of interest, I_D is the DC drain current, and i_{fD} is the drain flicker noise. From the equation we can see the $1/f$ nature and increase in flicker noise with DC drain current.

The noise figure of a system is related to the minimum detectable signal (MDS) and this sets the maximum operating range of a signal within power transmission constraints [11].

We can calculate the MDS using the following equation.

$$MDS = P_{noise\ floor} + NF + SNR_{min} (dB) \quad (2.6)$$

$P_{noise\ floor}$ is the noise floor level and is taken as -174 dBm, and SNR_{min} is the required signal to noise ratio at the ADC.

2.1.4 Linearity

The linearity of a system determines the upper limit on the power level of a received signal [11]. Together with the noise figure, it is used to determine the dynamic range of the system. It is important to maintain high linearity to minimize gain compression and desensitizing of the desired signal by an interferer. If we represent the output of a nonlinear system as,

$$y(t) = a_0 + a_1x(t) + a_2x^2(t) + a_3x^3(t) + \dots \quad (2.7)$$

and the input signal as,

$$x(t) = A_0 \cos(\omega_0 t) + A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \quad (2.8)$$

where ω_0 is the desired frequency component, then the output can be rearranged as,

$$\begin{aligned}
 y(t) = & \left\{ a_1 + a_3 \left[\frac{3A_0^2}{4} + \frac{3}{2}(A_1^2 + A_2^2) \right] \right\} A_0 \cos(\omega_0 t) \\
 & + \left\{ a_1 + a_3 \left[\frac{3A_1^2}{4} + \frac{3}{2}(A_0^2 + A_2^2) \right] \right\} A_1 \cos(\omega_1 t) \\
 & + \left\{ a_1 + a_3 \left[\frac{3A_2^2}{4} + \frac{3}{2}(A_1^2 + A_0^2) \right] \right\} A_2 \cos(\omega_2 t)
 \end{aligned} \tag{2.9}$$

where we have only included the fundamental components. From this equation, we can see that regardless of the interfering signal's frequency, we can get desensitization and gain compression. Gain compression comes from the nature of the receiver, which is limited by its supply voltage, and is reflected in the $3/4a_3A_0^3$ term where a_3 is negative. Desensitization comes from the terms involving A_1 and A_2 in the desired band.

Because odd ordered nonlinearity results in in-band distortion, it is of primary concern. The two parameters commonly used to measure nonlinearity are the third-order intercept point (IP_3) and the 1 dB compression point. The IP_3 is reached at a certain input level when the magnitude of the third order intermodulation is equal to the linear output [11], [6]. The 1 dB compression point is reached at a certain input level when the actual output power is 1 dB less than the linearly predicted output power. We used IP_3 to judge the large signal performance of small signal circuits such as LNAs, and Mixers. The 1 dB compression point is more relevant to large signal circuits such as power amplifiers.

As the signal moves to the later stages of the system, the signal level increases due to the gain stages. Thus linearity becomes more important in the later stages. When the RF signal is down-converted to the IF, it becomes easier to meet linearity requirements. Furthermore, it is easier to design quality filters at low frequency. However, the noise level at the baseband is higher than that at the RF band due to the presence of flicker noise. Therefore the gain of the RF stages must be large enough to attenuate to IF noise, but small enough to ensure high linearity.

2.1.5 Cascaded System

While it is important to ensure a low noise figure of the front end, this requirement is not sufficient. The overall noise figure depends on the following stages noise figure and the gain. The relationship is described by equation (2.10), and is known as the Friis equation [6].

$$F = 1 + F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \quad (2.10)$$

Assuming we can combine the second stage and all the following stages of the front end together, we can plot the overall noise figure versus the gain for different values of the second following stages' total noise figure (Figure 2.1). In Figure 2.1, the gain is on the X-axis, the total noise figure is on the Y-axis, and each curve represents a different value of the total noise figure of the stages after the LNA. From Figure 2.1, we require a 25 dB gain to get an overall noise figure of 2.75 dB if the following stages have a 20 dB combined noise figure. We have assumed the LNA has a NF of 2 dB.

Figure 2.1: Cascaded Noise Figure

For linearity, it is easier to get high linearity at baseband. Therefore, it is better to have most of the gain in the later stages. Thus there is a tradeoff between linearity and noise figure in cascaded systems. While the noise figure of a system is dependent mostly on the noise figure of the first stage, the linearity of a system is mostly dependent on the linearity of the last stage. We can find the total IIP_3 of a system by using the following equation,

$$\frac{1}{P_{IP3}} = \frac{1}{P_{IP3,1}} + \frac{G_1}{P_{IP3,2}} + \frac{G_1 G_2}{P_{IP3,3}} + \dots \quad (2.11)$$

Where $P_{IP3,n}$ is the n^{th} stage IIP_3 and P_{IP3} is the overall IIP_3 . For heterodyne systems, it is typically easier to obtain high linearity in the low frequency amplification stages due to the lack of high frequency parasitic effects. The designer will usually design the RF front end with just enough gain to minimize the effects of the IF stages' noise and leave most of the gain to the low frequency stages.

2.1.6 LO-leakage and DC-Offset

For LO-leakage we are primarily concerned with LO-RF leakage, LO-IF leakage and LO-leakage back to the antenna. After the LNA input stage, we are primarily concerned with the voltage level of a signal, not the power level. Therefore we can measure the LO-RF isolation by,

$$\text{LO-RF Isolation} = 20 \log \left(\frac{V_{RF}}{V_{LO}} \right) \quad (2.12)$$

For the LO-IF Isolation simply replace V_{RF} with V_{IF} . The main problem arising from LO leakage is DC-offset. DC-offset can be time-invariant, or time varying, and is measured in millivolts (mV). Time-invariant DC-offset arises from LO-self mixing when it leaks to the RF or IF port. When the LO leaks all the way back to the antenna and is transmitted, it can be received and then mix with itself. This leads to time-varying DC-offset and is more obvious when the transceiver is moving and there are multiple reflection paths.

A DC-Offset in the receiver chain is viewed as an un-modulated carrier at baseband. Hence it can desensitize or block the desired signal. This follows from the linearity analysis shown previously.

2.1.7 Reverse Isolation and Matching

For matching we are only concerned with input matching. S-parameters (S_{11} , S_{12} , S_{22} , and S_{21}) are used to measure the reflection and feed through in a matched system. S_{11} can be calculated as,

$$S_{11} = \left| \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \right| \quad (2.13)$$

where Z_0 is typically 50 ohms and Z_{in} is the input resistance when the output port is terminated by Z_0 . Typically we require S_{11} to be at least -10 dB. In a 50 ohm system, this means an input resistance of around 26 ohm. When the output is not terminated by Z_0 , the input reflection coefficient can be calculated as,

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (2.14)$$

where Γ_L is the load reflection coefficient with a reference impedance of Z_0 . From this equation we can see that the input reflection coefficient is equal to S_{11} when the output is terminated by Z_0 ($\Gamma_L=0$), or the isolation from the output to the input is infinite ($S_{12}=0$).

Hence, to make the Γ_{in} independent of the following stage, we must have good reverse isolation.

2.2 Architectures

There are three basic receiver architectures: the high-IF, low-IF, and zero-IF receivers [12]. For the Bluetooth standard, the frequency spans 2402 MHz to 2480 MHz. Therefore we can choose an IF of more than 78 MHz, less than 78 MHz or 0 Hz [13]. This section will briefly discuss each architecture and present a case for selection of the zero-IF architecture.

2.2.1 High-IF Receiver

In the high-IF receiver, the IF is greater than the operating bandwidth. The advantages of the high-IF receiver are selectivity, sensitivity and good noise performance. Figure 2.2 shows a typical high-IF front end.

Figure 2.2: High-IF Front End

The input filter rejects the image of the high IF stage and also acts as a band select filter. This is a high-Q off-chip filter and often it is split in two with the high-Q image reject

filter placed after the LNA. Typically, the better the out-of band rejection of the filter, the higher the insertion loss. If the filter is placed at the input of the system, its insertion loss will set the minimum noise figure of the system. Therefore it is often advantageous to have the filter with the best rejection after the LNA. The tradeoff is that out of band interferers will not be completely rejected and can desensitize the desired signal when passing through the nonlinear LNA.

The LNA boosts the signal without significantly degrading the SNR (Signal to Noise Ratio). Then the Mixer down-converts the RF signal to the IF, which is greater than the operating bandwidth of the system. This is also the channel select Mixer and therefore the following filter will reject in-band interferers.

Because of the high Q filtering required at a high IF, full integration is difficult for this architecture. Furthermore, its complexity is high since two down-conversion stages are necessary. For these reasons, this architecture will not be used for the project.

2.2.2 Low-IF Receiver

For the low-IF receiver, the IF is less than the system bandwidth. Because the IF is low frequency, a second down-conversion stage is unnecessary, and ADC (analog-digital conversion) can be performed directly after the down-conversion. The performance requirements on the ADC, however, are still high. In general we should sample a signal at a rate of around 10 times the operating frequency. The low-IF architecture also requires

bandpass filters after down-conversion which are more difficult to design than the low-pass filters used in direct conversion receivers.

Because the image frequency is inside the bandwidth, an image-reject architecture is required. Figure 2.3 shows an image-reject architecture [6].

Figure 2.3: Low-IF Receiver

Either IF-I or IF-Q is digitally phase shifted by 90 degrees and then the signals are added to cancel the image signal. The following expressions show how the architecture works.

$$I_{out} = A \sin(f_{LO} - f_{RF}) + B \sin(f_{IM} - f_{LO}) \quad (2.15)$$

$$Q_{out} = A \cos(f_{LO} - f_{RF}) + B \cos(f_{IM} - f_{LO}) \quad (2.16)$$

Shift Q_{out} by -90 degrees then take I_{out} minus Q_{out} .

$$\begin{aligned}
I_{out} - (Q_{out} - 90^\circ) &= \\
A \sin(f_{LO} - f_{RF}) + B \sin(f_{IM} - f_{LO}) - A \cos(f_{LO} - f_{RF} - 90^\circ) + B \cos(f_{IM} - f_{LO} + 90^\circ) \\
&= A \sin(f_{LO} - f_{RF}) + B \sin(f_{IM} - f_{LO}) + A \sin(f_{LO} - f_{RF}) - B \sin(f_{IM} - f_{LO}) \\
&= 2A \sin(f_{LO} - f_{RF})
\end{aligned} \tag{2.17}$$

As you can see, the image reject architecture also requires two Mixers. In certain special cases, there may be very few channels and low channel bandwidth compared to the overall bandwidth. In these cases, we can space the channels such that no channel frequency is another channel's image frequency. Thus an image reject architecture is not required.

One severe drawback of the low-IF receiver is its noise figure. This is because regardless of whether the image channel is used, its noise will be down-converted to the IF. Since the whole bandwidth is amplified by each preceding stage, the image noise is amplified by the same amount as the desired channel. Hence regardless of the noise figure and gain of the LNA, the minimum noise figure of a low-IF receiver is 3 dB. If the low-IF stage is preceded by a high-IF stage, then the low-IF image noise can be pre-filtered using a good channel select filter. In this case the minimum noise figure given noiseless components approaches 0 dB.

2.2.3 Zero-IF Receiver

The zero-IF receiver, also known as the Direct Conversion Receiver (DCR) is recently becoming popular because of the possibility of full integration of the RF front end. The architecture is the same as the low-IF architecture (Figure 2.3) except the band-pass filters can be replaced with low-pass filters which are easier to design. Quadrature down-conversion is necessary to prevent signal loss. This is due to the random phase mismatch between the signal carrier and local oscillator of the receiver. This is shown by the following equations. Assume we use frequency or phase modulation [14].

$$x_{FM}(t) = \cos(\omega_c t + \beta \sin(\omega_m t)) = \sum_{k=-\infty}^{\infty} J_k(\beta) \cos(\omega_c + k\omega_m)t \quad (2.18)$$

When k is odd,

$$J_{-k} = -J_k \quad (2.19)$$

When k is even,

$$J_{-k} = J_k \quad (2.20)$$

Take the case when k is odd and let the amplitude be A/2.

$$LO = \cos(\omega_c t + \phi) \quad (2.21)$$

$$x_{IF}(t) = \frac{A}{2} \cos(\omega_c + k\omega_m)t \cos(\omega_c t + \phi) - \frac{A}{2} \cos(\omega_c - k\omega_m)t \cos(\omega_c t + \phi) \quad (2.22)$$

After filtering the high frequency components,

$$\begin{aligned}
 x_{IF}(t) &= A/2 [\cos(k\omega_m t - \phi) - \cos(-k\omega_m t - \phi)] \\
 &= A/2 [\cos(k\omega_m t)\cos(\phi) + \sin(k\omega_m t)\sin(\phi)] + A/2 [-\cos(-k\omega_m t)\cos(\phi) - \sin(-k\omega_m t)\sin(\phi)] \\
 &= A \sin(k\omega_m t) \sin(\phi)
 \end{aligned} \tag{2.23}$$

If we take the case where k is even, it is easy to show that,

$$x_{IF}(t) = A \cos(k\omega_m t) \cos(\phi) \tag{2.24}$$

As we can see, given the phase mismatch conditions, it is possible to lose either the odd or even sidebands. Hence quadrature mixing is required.

Due to the random phase mismatch, there is also degradation in the overall noise figure. From equations 2.22 and 2.23, on average, each of the quadrature LO mixing stages results in a 3 dB signal power loss. Noise however does not suffer the same power loss on down-conversion. Hence the overall SNR is degraded by 3 dB. Narrowband noise can be represented by the following equation [15],

$$n(t) = x(t)\cos(\omega_c t) - y(t)\sin(\omega_c t) \tag{2.25}$$

where $x(t)$ and $y(t)$ are uncorrelated and have the same means and variances. Furthermore, $x(t)$ and $y(t)$ have the same spectral power densities and within the bandwidth,

$$G_x(f) = G_y(f) = G_n(f - f_c) + G_n(f + f_c) \quad (2.26)$$

Based on equations 2.24 and 2.25, we can see that regardless of the LO phase, the zero-IF noise will always have the same power density. This is because for noise, the $k=a$ and $k=-a$ sidebands are uncorrelated unlike in the signals case. Let the noise be represented as,

$$\begin{aligned} n(t) &= x_1(t)\cos(\omega_c + \omega_m)t - y_1(t)\sin(\omega_c + \omega_m)t \\ &+ x_2(t)\cos(\omega_c - \omega_m)t - y_2(t)\sin(\omega_c - \omega_m)t \end{aligned} \quad (2.27)$$

When multiplied by a cosine signal of random phase, the resulting baseband noise is,

$$\begin{aligned} n(t) &= x_1(t)\cos(k\omega_m t - \phi) - y_1(t)\sin(k\omega_m t - \phi) \\ &+ x_2(t)\cos(-k\omega_m t - \phi) - y_2(t)\sin(-k\omega_m t - \phi) \\ &= x_1(t)\cos(k\omega_m t)\cos(\phi) + x_1(t)\sin(k\omega_m t)\sin(\phi) \\ &+ x_2(t)\cos(-k\omega_m t)\cos(\phi) + x_2(t)\sin(-k\omega_m t)\sin(\phi) \\ &- y_1(t)\sin(k\omega_m t)\cos(\phi) + y_1(t)\cos(k\omega_m t)\sin(\phi) \\ &- y_2(t)\sin(-k\omega_m t)\cos(\phi) + y_2(t)\cos(-k\omega_m t)\sin(\phi) \\ &= \cos(k\omega_m t)[\cos(\phi)(x_1(t) + x_2(t)) + \sin(\phi)(y_1(t) + y_2(t))] \end{aligned}$$

$$+ \sin(k\omega_m t) [\sin(\phi)(x_1(t) - x_2(t)) + \cos(\phi)(y_2(t) - y_1(t))] \quad (2.28)$$

Remember that x_1 , x_2 , y_2 and y_1 are uncorrelated, and their signal power adds directly. The average power of a sinusoid is half its amplitude. Hence it is easy to see that the average power of both the RF and IF noise is,

$$n^2 = 2x^2 \quad (2.29)$$

Hence the overall SNR is degraded by a factor of 2 during down-conversion. Because this results regardless of the input noise power, the whole receiver has a minimum possible noise figure of 3 dB. This is true even when the zero-IF stage is preceded by a high-IF stage.

While the direct conversion receiver offers simplicity, and the possibility of full integration, it is not without problems. Because we are converting to baseband, time varying DC-Offsets caused by self mixing of the LO (Local Oscillator) and RF signals can degrade the signal quality. Furthermore, as the frequency gets lower than 1 MHz, flicker noise begins to dominate over thermal noise [10]. As we will see later, the problem of flicker noise can be avoided by reducing the current consumption of the Mixer. Furthermore, there are techniques which can be used to curb the DC-Offset problem (section 3.3).

2.2.4 Friis Equation Modification

Calculation of noise figure when employing a low-IF receiver or DCR requires a modification of the Friis equation. We should take the DSB noise figure of the Mixer and use the following equation for noise factor.

$$F = 2 \left(F_1 + \frac{F_2 - 1}{G_1} + \dots \right) + \frac{F_n - 1}{G_1 G_2 \dots G_n} \quad (2.30)$$

The terms in brackets represent all devices up to and including the Mixer, and the terms outside represent all IF components. From equation 2.29, given noiseless components, the noise figure results in a minimum of 3 dB. We can see how this is true by a quick example. Take three devices, an amplifier followed by a low-IF/zero-IF Mixer and another amplifier. This is shown in Figure 2.4. From the figure,

$$N_{out} = 2[(N_1 + G_1 N_{in})G_2 + N_2]G_3 + N_3 \quad (2.31)$$

$$\begin{aligned} F &= \frac{N_{out}}{G_1 G_2 G_3 N_{in}} \\ &= 2 \left(\frac{G_1 N_{in} + N_1}{G_1 N_{in}} + \frac{N_2}{G_1 G_2 N_{in}} \right) + \frac{N_3}{G_1 G_2 G_3 N_{in}} \\ &= 2 \left(F_1 + \frac{F_2 - 1}{G_1} \right) + \frac{F_3 - 1}{G_1 G_2} \end{aligned} \quad (2.32)$$

where we have calculated F_m (noise factor of the m^{th} stage) as,

$$F_m = \frac{N_m}{G_m N_{in}} \quad (2.33)$$

As previously explained, N_{in} is the same for each component when matched conditions is assumed. Since the minimum value of F_1 is 1, the overall minimum noise figure is 3 dB.

Fig. 2.4: Cascaded Noise Illustration

CHAPTER 3

STATE OF THE ART

This chapter will review the state of the art in LNA and Mixer design. The performance of several designs will be presented and a few of the best performances will be analyzed.

3.1 LNA Design

Table 3.1 shows the performance of several LNAs in the low gigahertz range. Most of the examples use CMOS technology, and several designs use SiGe (Silicon Germanium). Several 2.4 GHz CMOS examples are presented, but only one example has measured results. Apart from the GaAs (Gallium Arsenide) example, all LNAs use the inductive degeneration topology. It should be noted that in general, differential designs require twice the power consumption of single ended designs, and their power consumption should be halved when compared with single ended designs. In the table, a design is deemed not fully integrated if it uses any off chip components or if it cannot be interfaced on chip with the digital baseband since this would prevent it from being used in a single chip design. This automatically means only CMOS designs are fully integrated. While SiGe can be used for full integration, the entire chip would have to be in SiGe, and the result is higher cost.

Table 3.1: State of the Art in LNA Performance

REF	freq (GHz)	DC	VG (dB)	NF (dB)	S11 (dB)	IP3 (dBm)	Tech (um)	Measured	Integrated	Diff**
[16]	2.4	3 mA	19	2.4	-10		0.5 CMOS	NO	NO	NO
[17]	2.4	18.3 mW	18.3	1.6			0.3 CMOS	NO	YES	NO
[17]	2.4	40.8 mW	19.2	2			0.3 CMOS	NO	?	NO
[18]	2.4	4.2 mA	11	3	-50		0.25 CMOS	NO	NO	NO
[19]	2.4	1.75 mA	51	1.65			0.18 CMOS	NO	NO	NO
[20]	2.4	10.8 mA	33	0.9	-23	25*	0.35 CMOS	NO	NO	NO
[21]	2.4	7.94 mA	12	4	-10	-2	0.18 CMOS	YES	YES	NO
[22]	2.4	3 mA	19	2.4	-10		0.5 CMOS	NO	NO	NO
[7]	1.23	6 mA	20	0.8	-11	-11	0.25 CMOS	YES	NO	NO
[23]	5.75	16 mA	14.2	0.9		0.9	0.18 CMOS	YES	NO	YES
[23]	5.75	12 mA	14.1	1.8		4.2	0.18 CMOS	YES	NO	YES
[24]	1.575	8 mA	17	4.8			0.35 CMOS	YES		YES
[25]	5.2	8 mA	19.3	2.45		14.2*	0.35 CMOS	YES	NO	NO
[26]	1.5	20 mA	22	4.5		12.7*	0.6 CMOS	YES	NO	NO
[27]	1.9	9.2 mA	20.6	2		-4.5	0.25 CMOS	NO	YES	YES
[28]	5.25	16 mA	16	2.5			0.25 CMOS	YES	YES	YES
[29]	5.25	5 mA	11	2.17	-45	0.3	0.25 CMOS	YES	NO	NO
[30]	5.8	9 mA	13	2.1	-6	-10	SiGe	YES	NO	YES
[31]	5.8	6.36 mA	16	1.9	-10	0	SiGe	NO	NO	NO
[32]	2.1	4.7 mA	16	1.2	-15	-6	0.5 SiGe	NO	NO	NO
[33]	1.98	4.8 mA	10.2	2.3	-15	-16	0.35 SiGe	YES	NO	NO
[34]	5.2	14.2 mA	14.9	2.5			SiGe	YES	NO	YES
[35]	2.45	14 mA	26	2.2	-9		0.25 SiGe	NO	NO	NO
[36]	5.2	8 mA	15	2.1		-7	SiGe	NO	NO	YES
[37]	2	6.0 mA	22.4	1.6		8	GaAs	YES	NO	NO

* Output Referred

** Differential

From the table, we can see that the best performance comes from the GaAs followed by the SiGe designs. Many SiGe designs show measured noise figures of less than 2.5 dB, and the GaAs design has a noise figure of 1.6 dB. Furthermore, the GaAs design was

implemented without large on-chip inductors. While it is possible to get the required performance using CMOS, we typically need high power consumption.

3.2 Mixer Design

Table 3.2 shows the state of the art in Mixer design using CMOS. Some of the designs are full front ends. Where possible, Mixer performance is quoted. Because double sideband (DSB) NF is numerically smaller than single sideband (SSB) NF, it is usually quoted. When SSB NF was quoted, we subtracted 3 dB from the final figure before entering it in the table. Several designs use a single ended LNA followed by a phase splitter. Under the DIFF (Differential) column, they appear as MIX. Almost all of the designs use some variation of the Gilbert cell Mixer. There are three passive Mixers (Reference [39], [5], [49]) which are typical switching Mixers.

Table 3.2: State of the Art in Mixer/Front End Performance

REF	Tech (um)	Gain (dB)	DSB NF (dB)	NF (dB)/kHz	Current (mA)	IP3 (dBm)	IF(L/H/Z)	MEASURED	DIFF
[38]	0.35	24.7	20		10.4	-7	L	YES	YES
[39]*	0.18	14.36	13		4.02	-1	L	YES	YES
[40]	0.35	26.6	8.9		1.2	-0.1	H	NO	YES
[41]	0.35	9.48	17.69		4.7	3	H	NO	YES
[42]	0.18	1	14.3		5.9	11	H	NO	YES
[43]	0.35	23	4.4	33/1	8	-1.5	Z	YES	YES
[44]	0.35	9	15		5	5	L	YES	YES
[5]*	0.18	29	5.3	5.3/45	7.5	-21	Z	YES	MIX
[45]	0.18	20	8.5	25/1	4.4	4	Z	YES	YES
[46]	0.18	16	14.3		2.9	2.5	L	YES	YES
[47]	0.18	26.5	1.5		14.6		L	YES	MIX
[48]	0.18	19	11		2.36	3	L	YES	MIX
[49]*	0.18	-2.2	8.8		0	6.5		NO	MIX

*Passive Mixer

From the table, we can see that the best noise performance comes from passive Mixers. In fact only three designs were meant for direct conversion and the two active designs show very poor noise figure at low frequency. The overall direct conversion front end using the passive Mixer exhibits high voltage gain, but uses a single ended input and an active phase splitter. This could explain the poor linearity.

3.3 DC-Offset Correction and Reduction

There are several DC-Offset correction methods available [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], but only two methods to actually limit LO leakage. The methods available include double balancing, device sizing, AC coupling, DC coupling with DC feedback, harmonic mixing, and digital calibration. Using a fully balanced design is a standard practice which ideally prevents LO leakage and cancels second order nonlinearity. By device sizing, we mean using the minimum possible device size. This will limit the parasitic capacitance from the LO port to the IF or RF port.

3.3.1 AC Coupling and DC Coupling with DC Feedback

AC coupling is the simplest way to remove DC-Offset. The idea is just to use a high pass filter to remove the DC component. Unfortunately, the filter would need an extremely low corner frequency necessitating off-chip design. Furthermore, unless the filter exhibits ideal characteristics (infinite out-of-band rejection and in-band feed-through), the filter would distort the frequency components near to DC. The same goes for DC coupling

with DC feedback [52], [62], [63], [64]. The advantage of DC coupling and feedback is that it is possible to implement this method on-chip. Unfortunately, the settling time of the feedback loop may prohibit its use.

3.3.2 Harmonic Mixing

Harmonic mixing is a sticky issue. The idea is to use a harmonic of the desired frequency in the mixing thereby preventing in-band leakage [55], [60]. It is true that there is no in-band leakage in harmonic Mixers, but the LO does not need to be in the same band as the desired signal to mix with itself. Likewise, the RF signal does not need to be in the same band as the LO to mix with itself.

While it is possible to filter out LO leakage to the IF and RF ports since it is not in the desired band, the required performance of such a filter would prevent on-chip design since typically the LO frequency is only half of that of the RF signal. High-Q on-chip inductors usually have a low quality factor, e.g. 6.94 for a 7.81 nH inductor using the CSM PDK. Since the input/output impedance of the Mixer tends to be only a few hundred ohms (section 5.3), we are looking at a quality factor of around 2.5 at the RF/IF port. If we use the second harmonic of 2.45 GHz (1.225 GHz), we can expect to reject the LO leakage by an extra 12 dB over the standard design. This was estimated based on a simple LC parallel combination where the impedance is,

$$|Z_L| = \frac{Q\omega L}{\sqrt{1 + Q^2(1 - \omega^2 LC)^2}}$$

Q is the quality factor at the Mixer RF or IF port, ω is the test frequency, L is the inductance, and C is the capacitance.

Furthermore, harmonic mixing requires octet phases and is thus more complex. Lastly, harmonic Mixers tend to have poor gain compared to conventional Mixers. In fact simulations on a harmonic Mixer showed more than 10 dB conversion loss. Given these drawbacks, harmonic mixing is not a good solution to the DC-Offset problem in single-chip receivers.

3.3.3 Digital Calibration

There are also several digital calibration methods for DC-offset correction [50], [57], [58], [59]. Unfortunately, these methods typically require extra ADC and DAC (digital analog converter) blocks. Those methods involving feedback also increase the required settling time of the circuit. Most digital calibration methods are highly complex and power hungry. This usually means they need to be designed on a separate chip. Lastly, many digital calibration methods are system specific.

3.4 Problems in Current Design and Project Goal

From the lists of state of the art designs, we can see that so far it is difficult to have a CMOS fully integrated receiver with a low noise figure for the front end. The only possible exception is reference 20 which achieves a 2.5 dB LNA noise figure while consuming 16 mA of current. In CMOS, clearly high power consumption is necessary for good noise performance. Furthermore, the presence of low frequency flicker noise in

active Mixers has prevented low noise figures from being achieved in DCRs. The closest candidate is reference 29 which has a 5.3 dB noise figure at 45 kHz IF. A better understanding of passive Mixer operation is needed before it will be widely accepted. Lastly, all of the current DC-offset correction methods come with significant tradeoffs.

The goal of this project is to design a front end which can be implemented in a direct conversion system. We wish to minimize the noise figure and power consumption of the front end while providing an improved solution to LO self-mixing induced DC-offset. This project will require a method for noise optimization of LNAs, a comparison of active and passive Mixers, and a method to reduce LO leakage or correct DC-Offset.

CHAPTER 4

INDUCTIVE DEGENERATION LNA DESIGN

This section will cover the theory of inductive degeneration LNA design. Before going into the actual LNA design, we will discuss two port noise theory.

4.1 Two Port Noise Theory

The LNA's noise figure is the determining factor on the overall noise performance of a receiver system. The LNA can be represented as a two-port network, and by analyzing a generic two-port network, we can devise a means to optimize the input matching for low noise figure.

4.1.1 Noise Resistance and Conductance

All resistors generate thermal noise. The noise can be represented as a series noise voltage source or a parallel noise current source. The noise voltage and noise current are found respectively by [6],

$$\overline{e_n^2} = 4kTR\Delta f \quad (4.1)$$

$$\overline{i_n^2} = \frac{4kT\Delta f}{R} \quad (4.2)$$

If we divide these equations by $4kT\Delta f$, we get the equivalent noise resistance and noise conductance respectively. We will see later that this form is more convenient for noise matching.

4.1.2 The Generic Two-Port Network

The noise in a two port network can be represented by Figure 4.1 [6].

Figure 4.1: Two Port Noise Representation

The definition of noise factor is the total output noise power divided by the output noise power due to the input source noise. If we divide the numerator and the denominator by the gain, we get equation 4.3.

$$F = \frac{\overline{i_s^2} + \left| i_n + Y_s e_n \right|^2}{\overline{i_s^2}} \quad (4.3)$$

But i_n may be partially dependent on e_n . Therefore, we express i_n as, $i_n = i_u + i_c$, where i_u is the uncorrelated part and i_c is the correlated part, and $i_c = Y_c e_n$, where Y_c is the correlation admittance and has no physical meaning. Furthermore, if we express each noise source as a resistance value (equations (4.4) – (4.6)), we obtain equation (4.7). It

should be noted that these resistance values are not actual resistances but simply representations of noise in a convenient form.

$$R_n \equiv \frac{\overline{e_n^2}}{4kT\Delta f} \quad (4.4)$$

$$G_u \equiv \frac{\overline{i_u^2}}{4kT\Delta f} \quad (4.5)$$

$$G_s \equiv \frac{\overline{i_s^2}}{4kT\Delta f} \quad (4.6)$$

$$F = 1 + \frac{G_u + R_n \left[(G_c + G_s)^2 + (B_c + B_s)^2 \right]}{G_s} \quad (4.7)$$

The admittances, Y_c and Y_s , have been split into their equivalent conductance (G_c and G_s) and susceptances (B_c and B_s). To find the minimum noise factor, differentiate F (equation 4.7) with respect to G_s to find the optimum G_s , and then differentiate F with respect to B_s to find the optimum B_s . Then replace these values into equation 4.5.

$$B_{opt} = -B_c \quad (4.8)$$

$$G_{opt} = \sqrt{\left(\frac{G_u}{R_n} + G_c^2 \right)} \quad (4.9)$$

$$F_{min} = 1 + 2R_n(G_{opt} + G_c) \quad (4.10)$$

$$F = F_{min} + \frac{R_n}{G_s} \left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2 \right] \quad (4.11)$$

From these equations we can see that the optimum source susceptance is the negative of the correlation susceptance (B_c). The correlation susceptance is not necessarily the susceptance looking into the input port, which makes equation 4.8 difficult to satisfy when maximum power transfer is desired. Furthermore, there is an optimum source impedance which results in the minimum noise figure, Z_{opt} ($Z_{opt} = G_{opt} + j.B_{opt}$).

From equation 4.11, we can see that in order to minimize the noise figure, we should first minimize F_{min} . Next we need to minimize R_n . We should also try to make G_{opt} as close as possible to G_s and B_{opt} as close as possible to B_s . G_s and B_s are fixed.

4.2 Inductive Degeneration LNA Design

This section will cover basic narrowband LNA design using the inductive degeneration topology. The inductive degeneration configuration is generally accepted as giving the best performance among narrowband LNAs, because it can provide perfect matching with high gain, and low noise all with just one transconductance stage. Because no other topology comes close to matching the performance of this topology, we will not go into analyses of other topologies.

4.2.1 The Standard Design

The important design parameters are gain, noise figure, input and output matching, linearity, and power consumption. Figure 4.2 shows an inductive degeneration LNA. M_2 is the cascode transistor. It provides high isolation from the output to the input. This makes the input reflection coefficient independent of the load resistance. M_2 also has very

low input impedance ($1/g_m$) and so it prevents the miller multiplication of C_{gd} of M_1 . The low input impedance also lowers the voltage gain from the gate to the drain of M_1 . This prevents unwanted feedback.

Figure 4.2: Inductive Degeneration LNA

Because of the low out of band gain, the low voltage gain from the source to the drain of M_1 , and the high isolation from output to input, the inductive degeneration LNA is typically unconditionally stable.

Resistive Input Matching

The sole purpose of the degeneration inductor is to provide a real part to the input impedance. If we assume that the degeneration inductor resonates with the gate capacitance at the desired frequency, we can use a simple MOSFET model to calculate the input resistance.

Figure 4.3: Simple Small Signal Inductive Degeneration Matching Stage

From the figure,

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in} - V_{gs}}{j\omega L_s} \quad (4.12)$$

$$I_{in} = V_{gs} \cdot j\omega C_{gs} \quad (4.13)$$

$$I_{out} = g_m V_{gs} = g_m \frac{I_{in}}{j\omega C_{gs}} \quad (4.14)$$

$$I_{Ls} = I_{out} + I_{in} = I_{in} \left(1 + \frac{g_m}{j\omega C_{gs}} \right) \quad (4.15)$$

$$I_{Ls} = \frac{V_{in} - V_{gs}}{j\omega L_s} = \frac{V_{in} - I_{in} / j\omega C_{gs}}{j\omega L_s} = \frac{V_{in}}{j\omega L_s} + I_{in} \quad (4.16)$$

Equating equations 4.15 and 4.16 gives,

$$I_{in} \left(1 + \frac{g_m}{j\omega C_{gs}} \right) = \frac{V_{in}}{j\omega L_s} + I_{in} \quad (4.17)$$

$$R_{in} = \omega_T L_s \quad (4.18)$$

Therefore the input resistance can be increased by increasing the degeneration inductance.

4.2.2 Gain

If we take a simple resistive termination amplifier, where the matching is attained by adding a resistor from the gate of the input transistor to ground, the overall transconductance is,

$$G_m = \frac{R_{in}}{R_{in} + R_s} g_m = g_m / 2 \quad (4.19)$$

The key to improving the gain in LNAs is the gate inductor. The gate inductor resonates in series with C_{gs} of M_1 . Thus the voltage across C_{gs} becomes $Q_{in} V_s$. The effective G_m is therefore,

$$G_m = \frac{I_{out}}{V_s} = \frac{g_m}{\omega_0 C_{gs} (R_s + R_g)} = \frac{\omega_T}{\omega_0 (R_s + R_g)} = Q_{in} g_m \quad (4.20)$$

where R_g is the intrinsic gate resistance of the transistor. Therefore, using a gate inductor results in a $2Q_{in}$ increase in the transconductance. Unfortunately, the input impedance of

a transistor is almost completely reactive. R_g tends to be very small. We need a way to increase the input resistance. This is the purpose of the degeneration inductor. The inductive degeneration LNA has a gain of,

$$G_m = \frac{I_{out}}{V_s} = \frac{g_m}{\omega_0 C_{gs} (R_s + \omega_T L_s + R_g)} = \frac{\omega_T}{\omega_0 (R_s + \omega_T L_s + R_g)}$$

$$= Q_{in} g_m \quad (4.21)$$

where,

$$R_{in} = \omega_T L_s + R_g \quad (4.22)$$

From equation 4.22, we can see that inductive degeneration results in a tradeoff between gain and input matching. Note that when using the CSM PDK, high quality inductor L_g may not be large enough to resonate with the intrinsic capacitance of M_1 (C_{gs}) using typical device widths. External capacitor C_l can be added to ensure resonance. Since L_g is fixed, Q_{in} is fixed. Therefore, increasing the device width increases the gain until C_l is no longer required. Increasing the device size however results in increased power consumption.

Optimum g_m versus DC Current

As we can see, the overall G_m is directly proportional to the transistor g_m . For a given power consumption, we can optimize the gain versus power consumption by calculating g_m divided by I_{DS} .

$$I_{DS} = \frac{1}{2} K \frac{W}{L} (V_{OD})^2 = \frac{1}{2} g_m (V_{OD}) \quad (4.23)$$

$$\frac{g_m}{I_{DS}} = \frac{2}{V_{OD}} \quad (4.24)$$

where V_{OD} is the DC gate overdrive voltage, and K is a technology dependent constant.

As we can see, g_m is optimized by lowering V_{OD} as much as possible. To keep the transistor operating in the saturation region however, it is necessary to ensure the DC gate source voltage exceeds the threshold voltage by around 100 mV [6].

The Load

The load of the LNA is the following stage which is usually the input impedance of a MOSFET (C_{next}). The load Q of the circuit (Q_L) is limited by M_2 's output resistance, and the quality factor of the inductor. Thus the total resistance seen at the drain of M_2 is,

$$R_{drain, M_2} = Q_L \omega_0 L_2 \quad (4.25)$$

Knowing the voltage at the drain of M_2 , we can use the capacitive divider concept to calculate the voltage at the following stage,

$$V_{out} = V_{drain} \frac{C_2}{C_2 + C_{next}} \quad (4.26)$$

where V_{drain} is the voltage at the drain of M_2 . Finally, the overall voltage gain is,

$$V_{out}/V_{source} = G_m Q_L \omega_0 L_2 \frac{C_2}{C_2 + C_{next}} = \frac{G_m Q_L}{\omega_0 C_{next}} \quad (4.27)$$

Thus in order to improve the voltage gain, we should increase Q_L and reduce C_{next} .

The Overall Voltage Gain

By substituting equation (4.22) into (4.27), we can obtain the overall voltage gain. After some manipulation we get,

$$Voltage\ Gain = \frac{g_m Q_{in} Q_L}{\omega_0 C_{next}} = \frac{Q_L \omega_T}{\omega_0^2 C_{next} (R_{in} + R_s)} \quad (4.28)$$

This result is not fixed since the cutoff frequency is reduced depending on the size of C_L .

This is explained by the following equation,

$$\omega_T \approx g_m / C_{gs} \quad (4.29)$$

The overall gain reaches its maximum value when C_I is not needed. If M_1 is widened any further there will be no change in ω_T . In practice however, since L_g has a series resistance, as it is made smaller, it dissipates less power, and higher gain is seen.

Increasing the Voltage Gain

The easiest way to increase the voltage gain is to sacrifice the input matching [7]. Typically an input return loss of 10 dB meets requirements. This equates to an input resistance of 26 ohm. From equation 4.22, lowering the input resistance results in higher Q_{in} , and increased gain. Lowering the input resistance can be accomplished by lowering L_g .

If even more gain is required, the only solutions are to either try a different topology or cascade two or more stages.

4.2.3 Noise Figure

There are several methods which have been proposed to minimize the LNA noise figure [66], [67]. This section will present a simple method which does not require lengthy optimization simulations. Assuming M_1 of Figure 4.2 provides a large enough gain, we can neglect the noise contributions of M_2 , L_2 and C_2 . If C_I is small, its noise contribution due to its finite quality factor is also negligible. Furthermore, we can treat L_g as being in series with the LNA, and since there is no power gain across L_g , its noise figure adds directly to M_1 .

$$F_{total} = F_{L_g} + F_{LNA} - 1 \approx F_{L_g} + F_{M_1} - 1 \quad (4.30)$$

Thus, to analyze the noise figure, we need only consider M_1 . We can use two port noise theory to calculate the noise figure. Figure 4.4 shows the MOSFET noise model followed by the same model with the noise sources referred to the input. Equations (4.31) to (4.34) describe the MOSFET noise sources.

Figure 4.4: MOSFET Noise Models

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f \quad (4.31)$$

$$\overline{i_g^2} = 4kT\delta g_g\Delta f \quad (4.32)$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (4.33)$$

$$c \equiv \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2} \overline{i_d^2}}} \quad (4.34)$$

where i_d is the drain noise current and i_g is the induced gate noise current. g_g is the NQS (Non-Quasi-Static) gate resistance [68], [69] and is proportional to the square of the capacitance across the gate and source be it external or otherwise. c is the correlation coefficient for the correlation between the gate and drain noise. In theory, $c = -j0.395$. T is the absolute temperature, k is Boltzmann's constant, γ is $2/3$ in saturation for long channel devices, g_{d0} is the channel conductance when the drain source voltage is zero, and Δf is the bandwidth. δ is $4/3$ in saturation for long channel devices. Good analyses of these parameters are found in [70], [71], [72].

MOSFET Noise Analysis

By comparing the models of figure 4.4, it is easy to show that the noise performance of a MOSFET can be derived to obtain equations 4.33 to 4.36. R_n is the noise resistance, B_{opt} is the optimum source susceptance, G_{opt} is the optimum source conductance, and F_{min} is the minimum possible noise factor.

$$R_n = \frac{\gamma}{\alpha g_m} \quad (4.35)$$

$$B_{opt} = -\omega C_{gs} \cdot (1 - \alpha |c| \sqrt{\frac{\delta}{5\gamma}}) \quad (4.36)$$

$$G_{opt} = \alpha \omega C_{gs} \sqrt{\frac{\delta(1 - |c|^2)}{5\gamma}} \quad (4.37)$$

$$F_{min} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)} \quad (4.38)$$

From the general noise figure expression which is valid for all two port networks,

$$F = F_{\min} + \frac{R_n}{G_s} \left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2 \right] \quad (4.39)$$

we can see that to obtain minimum noise figure, G_{opt} (equation 4.35) must equal to the source conductance, and $F_{\min}$ (equation 4.36) must be as low as possible. Furthermore, from equations 4.33 and 4.37, g_m should be as large as possible. Notice that if equation 4.35 is satisfied, then the circuit will not resonate at the desired frequency.

From equation 4.36, if the operating frequency is fixed, then the only way to obtain noise matching is by properly sizing C_{gs} . As explained in the section on gain, addition of an external capacitor to increase C_{gs} results in a lower cutoff frequency. This results in a higher $F_{\min}$ (equation 4.36). Thus to obtain a lower noise figure, M_1 should be sized so that G_{opt} equals G_s . This implies that at high frequency it is possible to get noise matching by changing M_1 's width without sacrificing gain since at high frequency, smaller inductors are needed.

For equation 4.36, only ω_T can be manipulated. As explained in the section on gain, ω_T has its optimum value when L_g completely resonates with C_{gs} . Beyond that, the only way to increase ω_T is to increase the drain source bias voltage of M_1 . Due to channel length modulation, this results in a higher g_m and hence higher ω_T . V_{DS} can be increased by increasing the gate bias voltage or the size of M_2 .

$$G_m = G_{m0}(1 + \lambda V_{DS}) \quad (4.40)$$

Note that in practice, increasing the size of M_1 can lower the noise figure and increase the gain if it results in a smaller inductor L_g . The smaller series resistance of L_g will have a smaller voltage drop resulting in higher gain and less noise. Increasing device width also lowers R_n and thus can improve the noise figure.

4.2.4 Linearity

We can write the expression for the current of the LNA using the Taylor series expansion,

$$i_{DS} = I_{dc} + g_m V_{in} + \frac{g_m'}{2!} V_{in}^2 + \frac{g_m''}{3!} V_{in}^3 + \dots \quad (4.41)$$

Only odd ordered nonlinearity results in in-band distortion. Therefore minimizing third order nonlinearity is essential for improving linearity. In other words we need to minimize the second derivative of the transconductance. It has been shown in [46] that the second derivative of the transconductance is strongly dependant on the biasing conditions. While it would require high power consumption to simply bias the LNA at a point where third order nonlinearity is low, the method proposed in [46] requires no extra power. The idea is to add another transistor in parallel with M_1 which is biased below the threshold voltage at a point where its second derivative of the transconductance is opposite in magnitude with that of M_1 .

While this idea seems correct, and excellent results have been reported, simulation results of this method in Cadence were inconclusive. Because linearity is not the focus of this work, it will not be further discussed.

CHAPTER 5

MIXER DESIGN

The two main categories of Mixers are active and passive. The difference is active Mixers consume power whereas passive Mixers do not [6]. Before analyzing the active and passive Mixer, we will discuss the DC-offset problem and its possible solutions.

5.1 DC-Offset

DC-offset is caused mainly by self-mixing of the LO signal [11], [73]. Ideally, a double balanced topology will prevent LO and RF leakage by creating a virtual ground between the positive and negative LO and RF signals. Typically we are only concerned with LO leakage since the LO is usually at a much higher voltage level than the RF signal. For instance, the RF signal at the Mixer input may be as high as 0 dBm, while the LO signal is usually around 30 dBm in passive Mixers.

There are two types of DC-Offset: time varying and time-invariant. The time-varying DC-Offset occurs when the LO signal leaking to the antenna is transmitted. It reflects off multiple surfaces and returns to the same antenna. The resulting DC-offset can be time-varying when the environment is changing like in the case where the receiver is mobile. To prevent time-varying DC-offset, we must provide high isolation from the Mixer to the antenna.

Time-invariant DC-offset occurs when the LO leaks directly to the Mixer RF port and mixes with itself. Self mixing can also result when the LO leaks to the IF port. To get proper mixing, the switching stage is either in the saturation region or the triode region. The saturation region is for active Mixers without current injection since the drain source voltage of the switching stage can be higher than the gate source voltage. The triode region is for active Mixers with current injection and passive Mixers since the drain source voltage of the switching stage is usually much smaller than the gate source voltage. The equation for drain current in the saturation and triode respectively are,

$$I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (5.1)$$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (5.2)$$

where μC_{ox} is constant, W/L is the aspect ratio, V_{GS} is the gate source voltage, V_T is the threshold voltage, and V_{DS} is the drain source voltage. From equation 5.2, in active Mixers without current injection, no LO leakage is required to get DC-Offset since the self mixing term is due to V_{GS}^2 . In the triode region equation, the self mixing term is due to $V_{GS} V_{DS}$ which can be expanded as $V_G V_D$, $V_G V_S$, $V_D V_D$, and $V_S V_S$, where $V_G V_D$ and $V_G V_S$ are dominant. Clearly leakage to the drain and source of the switching transistors is needed for self-mixing.

Figure 5.1 shows a typical switching stage. The LO is applied to Y, and it can leak to Z and X.

Figure 5.1: LO leakage Illustration

To calculate the leakage from Y to X we need to know the impedance from Y to X ($1/j\omega C_{gs}$) and the impedance looking into X from C_{gs} , Z_S . The resulting leakage is,

$$\frac{V_{RF}}{V_{LO}} = \frac{Z_S}{Z_S + 1/j\omega C_{GS}} \quad (5.3)$$

To calculate the leakage from the LO to the IF, we need to know the impedance from Y to Z ($1/j\omega C_{gd}$) and the impedance looking into Z from C_{gd} , Z_D . The resulting leakage is,

$$\frac{V_{IF}}{V_{LO}} = \frac{Z_D}{Z_D + 1/j\omega C_{GD}} \quad (5.4)$$

Until now, the known method of reducing leakage was to minimize the device size. Since there is no current gain across the Mixer, the device size doesn't affect the gain.

We will see however, that there are simple ways to reduce LO leakage. One commonly used method to improve LO-IF isolation is to simply add a large capacitor connecting the IF port to ground. The capacitor would be large enough to short the RF signal to ground while presenting a large impedance to the baseband signal. Simulation results for this method will be shown in the section on passive Mixers.

We cannot use the same technique to limit LO-RF leakage since the RF signal would be shorted to ground. From equation 5.3, however, we can lower Z_S . All we need to do is lower the output impedance of the previous stage. This can be done by using a buffer with low output impedance. This method will be further discussed in the section on passive Mixers.

5.2 The Active Mixer

Figure 5.2 shows a double balanced active Mixer (Gilbert Cell) [6]. The main advantage of the active Mixer is the conversion gain. The conversion gain is provided by the extra transconductance stage M_1 and M_2 .

Figure 5.2: Gilbert Cell

One of the major drawbacks of the active Mixer is the noise figure. When converting to baseband, flicker noise becomes dominant [6], [10]. So far no explanation for flicker noise has been universally accepted, but most models show flicker noise to be directly dependant on current consumption and inversely dependant on transistor length [6], [10].

Since the transistor length is fixed, one widely used method to curb this problem is to inject DC current into the RF transconductance stage to reduce the current in the switching stage [44], [45]. This is accomplished by the two PMOS transistors M_7 and M_8 . Another method is to increase the LO voltage swing [74].

If we reduce the current in the switching stage, and increase the LO voltage, the noise corner frequency will decrease due to the increased dominance of thermal noise over flicker noise. The limit of the lowest possible flicker noise is reached when the switching stage consumes no power and the LO voltage is large enough for complete on-off

switching of the switching stage transistors. We can accomplish this by replacing the resistive loads by capacitive loads and increasing the LO voltage. It is easy to see that at this point we will have an RF differential amplifier and a passive Mixer. Thus, to the author, there is no apparent usefulness of active CMOS Mixers.

5.3 Passive Mixers

Because there is no drain source voltage drop in passive Mixers, no DC current is used. Since we must have a gate source voltage drop to ensure the transistors can turn on, we can devise two fundamental passive Mixer topologies. They can be implemented in both NMOS and PMOS. Figure 5.3 shows the two topologies.

Figure 5.3: Passive Mixer Topologies

Configuration B. is the standard passive Mixer configuration which we will call the drain driven Mixer (DD Mixer). The RF signal is applied to the drain and IF signal appears at

the source. A better passive Mixer topology is proposed and shown (configuration A.). We will call it a source driven Mixer (SD Mixer). If we remove the RF ports and measure the impedance looking into the source and drain of the transistor, we will get the curves shown in Figure 5.4 and Figure 5.5 respectively.

Figure 5.4: Source Input Impedance

Figure 5.5: Drain Input Impedance

From these figures, we can see that the SD Mixer topology gets lower input impedance and higher output impedance. This means that it will have higher LO-RF, IF-RF, and LO-IF-RF isolation. In the SD Mixer topology we have used a 1 pF capacitive load and compared it with the standard design.

We should note that because the mixer is passive, the transistor is symmetric meaning it exhibits the same characteristics looking into both the drain and the source. Therefore the discrepancy in the input impedances must be a result of the load. In the source driven mixer, the load capacitor exhibits low (1 pF at 2.45 GHz $\approx$ 65 ohm) RF impedance and very large (1 pF at 1 MHz $\approx$ 160 kohm) low frequency impedance. Therefore, the high frequency input impedance is low, and at low frequency our load is limited by the transistor's intrinsic parasitic output resistance. For the drain driven mixer, the load is

always equal to R_{load} (10 kohm in this case), and the input and output impedances are both decided by the transistor's parasitic resistance.

Figure 5.6 and Figure 5.7 show the resulting LO-RF isolation. LO leakage can be analyzed using the method shown in [75].

Figure 5.6: LO-RF Isolation of Topology 1 ($V_{LO} = 250\text{ mV}$)

Figure 5.7: LO-RF Isolation of Topology 2 ($V_{LO} = 250 \text{ mV}$)

As mentioned previously, we can improve the LO-IF-RF isolation by increasing the load capacitance. In the standard design, this leads to severe degradation in the gain and noise performance. The novel design fairs better in this respect. To show this, we designed two fully-balanced, quadrature front ends. The designs used identical LNAs (only C_2 of Figure 4.2 was modified for resonance) but the first design used a DD mixer and the second design used a SD mixer. We tested the performance degradation by applying a 100 mV, 5 degree LO mismatch. Figures 5.8 and 5.9 show the performance degradation of the standard design and the novel design respectively. We swept the output capacitance from 100 fF to 5 pF. From the figures, in the DD design, the gain drops from

22.5 dB to 14 dB while in the SD design, the gain drops from 21.5 dB to 18.5 dB. In the DD design the NF increases with isolation, and it decreases with isolation in the SD design.

Figure 5.8: Standard Front End Performance Degradation with Isolation

Figure 5.9: Novel Design Performance Degradation with Isolation

5.4 Novel Design

Using the novel Mixer topology and the proposed methods to minimize LO-IF and LO-RF isolation, we can design a full front end. Figure 5.10 shows a single balanced version of the novel design. Because a passive mixer is used, there should be no direct amplification of the LO. The single balanced design is presented here for ease of understanding. A double balanced design, which will cancel any unwanted amplification of the LO, will be presented in chapter 7.

Figure 5.10: Novel Single Balanced LNA, Buffer and Mixer

We used a push-pull source follower as a buffer [76]. With 6 mA of current consumption, this buffer has an output impedance of only 2.5 ohm. We can see the affect of the Mixer load capacitors by sweeping the capacitors from 100 fF to 10 pF. LO+ was set at 450 mV while LO- was set at 550 mV. The phase difference used was 10 degrees. Figure 5.11 shows the resulting isolation.

Figure 5.11: LO-IF Isolation versus Load Capacitance

From the figure, every doubling of the load capacitance results in a doubling of the LO-IF isolation. The overall isolation of three topologies is shown in table 1. The novel design includes the buffer and a 6 pF load capacitor. The DD Mixer and SD Mixer have neither. All designs are tested with the same LNA where only the inter-stage capacitor (C_2 , Figure 4.2) was modified for resonance at the operating frequency.

Table 5.1: Simulated RF Front End isolation

	Novel Design	DD Mixer	SD Mixer (100fF load)
LO-RF Isolation (dB)	72	31	45
LO-IF Isolation (dB)	55	7	19

From Table 5.1, both the LO-RF and LO-IF isolation are improved by using the proposed methods. In chapter 9 we will present further results and comparisons between the novel topology and the standard topology.

CHAPTER 6

DIFFERENTIAL DESIGN

From the previous section, we can see that RF transceiver front ends are preferably differential, although many designs employ a single ended LNA a phase splitter and a double balanced Mixer. Double balanced Mixers are essential for preventing LO-RF leakage and the DC-offset. Using a single ended LNA and phase splitter, however, paves the way for a novel current reuse method.

6.1 Current Reuse

Current reuse is a technique which can improve circuit performance without any increase in power consumption [43], [77]. Basically, we often have more voltage headroom than we need in a circuit. For example, the 0.18 μm CSM process allows for a 1.8 V supply voltage. With a threshold voltage of around 0.48 V in the CSM PDK, we only need V_{GS} to be around 0.63 V and V_{DS} to be 0.28 V while still accounting for process variation. While there would be some performance degradation due to channel length modulation, good circuit performance would still be obtained.

If an LNA uses 5 mA of current at a 1.8 V supply voltage, its total power consumption is 9 mW, but 6.2 mW of it is wasted ($9 \text{ mW} - 5 \text{ mA} * 2 * 0.28 \text{ V}$). There are various ways of implementing current reuse. The most obvious LNA implementation using current reuse would be the simple CMOS inverter [77]. The same current powers the NMOS and

PMOS transistor, and each transistor works as both a source and a load. Unfortunately this idea can only lead to at most a 3 dB gain increase. This comes at the cost of an extra source degeneration inductor, blocking capacitors to separate the DC levels at the input PMOS and NMOS transistors, and an extra biasing level for the PMOS transistor. Clearly this is not a good trade.

Better performance can be obtained by stacking a second stage on top of the first as shown in Figure 6.1 [25]. This circuit can realize much higher gain than the standard inductive degeneration method.

Figure 6.1: Current Reuse Method

In Figure 6.1, L_1 and C_1 block the RF signal while allowing DC current to pass. L_{g2} and L_{s2} can be removed resulting in only one extra inductor as compared to a standard LNA.

Theoretically, this would lower the gain and improve the noise figure. Unfortunately, this circuit is good for improving gain, but not good for saving power. For this circuit, the current through M_1 must still be large enough to provide a low noise figure. Furthermore, because we are essentially cascading two LNA stages, far more gain than necessary is provided. This is especially true with smaller device sizes. Another potential problem with this architecture is instability. Because of the high voltage gain across M_1 , the circuit may oscillate at a certain frequency. To curb this problem, an extra cascode stage needs to be inserted between M_1 and L_1 .

Another practice which can be considered as current reuse is replacing the transconductance stage of a Gilbert Cell with the transconductance stage of an LNA. Figure 6.2 shows a low noise mixer. The overall circuit would be a Mixer with high gain and low noise figure. Given the previous analysis on active Mixers however, the same performance could probably be obtained using an LNA and a passive Mixer. Furthermore, this current reuse method can only be used with active Mixers, so the circuit would automatically have high flicker noise. One other problem that arises in this topology is high leakage from the VCO to the antenna due to the absence of a cascode stage in the LNA. The advantage of this topology is that there is no need for load inductors, and so space is saved.

Figure 6.2: Low Noise Mixer

6.2 A Novel Current Reuse Method

This section describes a new current reuse method which to the author's knowledge has not been previously studied. Basically we can recognize that at zero frequency, the inductive degeneration LNA looks like a current source. Thus with proper biasing of the cascode stage, we can redirect its DC current to another circuit such as a phase splitter. Figure 6.3 shows a possible implementation of this method.

Figure 6.3: Alternative Current Reuse Configuration

Table 6.1 shows the performance of the circuit in the CSM 0.18 μm CMOS process. All RF MOS devices and passive components are from a silicon verified PDK. Excellent performance is obtained from both the LNA and the phase splitter. For a standalone LNA design, it is not normally possible to obtain 1.7 dB noise figure and 17.7 dB gain with only 1.6 mA of current. Figure 6.4 shows the gain from each differential end, the gain mismatch, and the phase mismatch. Figure 6.5 shows S_{11} and the NF of the LNA. To simulate the LNA alone, we replaced the 10 pF capacitor between the LNA output and the phase splitter input with a 450 fF capacitor terminated with a 50 ohm port.

Table 6.1: LNA and Phase Splitter Performance

Parameter	LNA	LNA Phase Splitter Combination
Frequency (GHz)	2.45	2.45
S21 (dB20)	17.7	21.4
Noise Figure (dB10)	1.7	2.0
Gain Error (dB10)	N.A.	0.006
Phase Error (deg)	N.A.	0.24
IIP3 (dBm)	-8.85	-9.05
S11 (dB20)	-10	-10
DC Current (mA)	1.61*	7.15
Supply Voltage (V)	1.8	1.8

* measured through M₂ (figure 6.3)

Figure 6.4: Combined Gain, Phase Difference (A) and Gain Difference (B)

Figure 6.5: LNA Noise Figure (A) and S11 (B)

The reason this design works is because a typical LNA does not require the full 1.8 V voltage supply. The component which determines the performance of the LNA is M_1 , and excellent performance can be obtained with a V_{DS} of only 0.3 to 0.4 V. This leaves up to 1.5 V for the phase splitter operation. It is important to note that as inductor L_{block} gets smaller, M_2 must be biased at a higher g_m . This will lower M_2 's input impedance and allow AC current to flow to the output of the LNA. If L_{block} is made too large and M_2 is reduced in size accordingly, then the input impedance of M_2 may become very small. This would result in high voltage gain across M_1 and could lead to instability. Hence it is important to make L_{block} large enough to meet power requirements but small enough to ensure stability. This design is unconditionally stable.

CHAPTER 7

RESULTS

Having presented the design methodologies of our front end, we will present the designs of two double balanced front ends and their simulation results. The first uses the standard Mixer and the second uses the novel Mixer with the buffer. Both front ends use the same LNA which is optimized for low noise figure at low power.

Because it is not possible to test a quadrature front end with the equipment available, we restricted the designs to being double balanced. The testing equipment is further discussed under the section on Layout for Testability. Another complication that arose was the fact that SpectreRF cannot be used to test a full front end (including the VCO (Voltage Controlled Oscillator)). Therefore, we tested the LO voltage and used a sinusoidal source to represent the VCO. Figure 7.1 shows the test-bench used.

Figure 7.1: Front End Test Bench

From Figure 7.1, the IF voltage is measured across the two capacitors on the right. The RF input is supplied by a 50 ohm port and an ideal Balun.

Because both designs use the same LNA, we will present the LNA's results first. The LNA used is exactly the same as that in section 4.

7.1 The LNA

To test the LNA, we modified the original test bench as in Figure 7.2.

Figure 7.2: Modified Test Bench for LNA Testing

Because the Mixer stage is still attached, there is a slight degradation in the LNA's voltage gain. The following figures illustrate the LNA performance. Figure 7.3 shows the LNA voltage gain, Figure 7.4 shows the noise figure, and Figure 7.5 shows the input return loss. Figure 7.6 shows the LNA design. Table 7.1 shows the component parameters. As we can see, the voltage gain is 15 dB even with the mixer still attached and the 3 dB bandwidth is from 2.04 GHz to 2.92 GHz. The simulated noise figure is less than 1.7 dB over the 2.4 GHz to 2.5 GHz bandwidth and the input return loss is better than 12 dB over the same bandwidth.

Figure 7.3: LNA Voltage Gain

Figure 7.4: LNA Noise Figure

Figure 7.5: LNA Input Return Loss

Figure 7.6: LNA Schematic

Table 7.1: Component Parameters

Component	Value
M ₁ (width)	150 μm
M ₂ (width)	60 μm
L _s	0.45 nH
C ₁	270 fF
L _g , L2	7.81 nH
V _{b1}	0.63 V
V _{b2}	1.5 V
C2	400 fF

SpectreRF uses two measurements for stability, k_f and $B1f$. For unconditional stability, k_f must be more than 1 at all frequencies and $B1f$ must be more than zero. Both are satisfied by the LNA. The total current consumption of the single ended LNA is 4.36 mA at a 1.5 V supply voltage. Hence the power consumption is 6.54 mW. Because we use a balanced topology, the total current consumption is 8.72 mA, and the power consumption is 13.08 mW.

Although only simulation results are shown, the performance of this LNA is better than the state of the art LNA in terms of noise figure and power consumption. The simulations use the CSM PDK which is based on silicon verified components. The next section will present the results of the standard front end design.

7.2 Standard Front End

Figure 7.7 shows the standard front end. It consists of the standard inductive degeneration LNA followed by a doubled balanced drain driven passive Mixer. Because the only DC current used is drawn by the LNA, the current consumption is only 8.72 mA. The LNA is modified by changing C_2 from 400 fF to 6 pF. This accounts for the input capacitance of the Mixer. All of the switching transistors are minimum size (30 μm), and the load resistors are 10 k Ω each. V_{bias} is set at 0.24 V since the VCO used in the later post-layout simulation has a DC voltage of 0.84 V. The standard front end achieves an IIP3 of -15.8 dBm. This was simulated using the two-tone test with a 500 kHz separation of the tones.

Figure 7.7: Standard Front End

Figure 7.8 shows the single sideband noise figure of the standard front end. Given that there is a 3 dB increase in the noise figure due to image superposition, we can see that there is little degradation in the noise figure due to the Mixer. The LNA NF is 1.6 dB and the front end DSB NF is 1.65 dB. Furthermore, the noise corner frequency is very low (less than 1 kHz). This type of noise performance is ideal in direct conversion receivers.

Figure 7.8: Single Sideband Noise Figure

Figure 7.9 shows the voltage gain of the front end. Basically the RF input is swept from 2.35 GHz to 2.55 GHz and the output voltage is measured. The LO is fixed at 2.45 GHz. We can see from the figure that the gain peaks when the RF input is at around 2.42 GHz. The gain variation is less than 0.1 dB indicating that good gain flatness is achieved in the desired band (2.4 GHz to 2.5 GHz). The reader should note that the voltage gain of the full front end (23.6 dB) is much higher than that measured from the LNA (15 dB). This is because the mixer was still attached to the LNA when the LNA voltage gain was measured.

Figure 7.9: Standard Front End Voltage Gain

Figure 7.10 shows the LO-RF and LO-IF isolation of the standard front end. This was simulated with LO+ set at 650 mV and LO- set at 850 mV. As we can see, the isolation is less than 30 dB to both the RF and IF ports. The isolation peaks at around 180 degrees phase which is when LO+ and LO- are exactly out of phase. Based on these measurements of LO-IF and LO-RF isolation, we can expect significant DC-Offset between the IF ports of the mixer.

Figure 7.10: Standard Front End Isolation

In conclusion, this design shows excellent gain and noise performance, but has poor DC-Offset performance. The next section will present the novel design which aims to remove the DC-Offset.

7.3 Novel Front End

The novel front end uses a buffer with low output impedance between the LNA and the Mixer. We used a source driven Mixer with capacitive loads to improve the isolation. The total current consumption of the front end is 14.7 mA. 8.72 mA is from the LNA and 5.98 mA is from the buffer. The total power consumption is thus, 22.05 mW. The novel front end achieves an IIP3 of -12.1 dBm. Figure 7.11 shows the novel front end. All biasing resistors are 10 k Ω . The load capacitors are 10 pF each. The matching/coupling capacitors from the LNA to the buffer are 1.3 pF each, and the matching/coupling

capacitors from the buffer to the Mixer are 5.6 pF each. We call these matching/coupling capacitors because they make sure the resonant frequency at the output node of each stage is correct, while also blocking DC signals. For the buffer, both the NMOS and PMOS transistors have a device width of 150 microns. The output impedance of the buffer is 8 ohm for each side.

Figure 7.11: Novel Front End

Figure 7.12 shows the simulated single-sideband noise figure of the front end. As we can see the noise figure is around 4.92 dB. Although the noise figure is good, it is worse than that in the standard design case. We can also see that we have very low flicker noise. In fact even with the IF as low as 100 Hz, the noise corner frequency is not detected. In a real design, such good noise performance is unlikely.

Figure 7.12: Novel Front End Single Sideband Noise Figure

Figure 7.13 shows the simulated voltage gain of the novel front end. From the figure, we can see that good gain flatness (0.6 dB variation) is achieved. Although the peak gain occurs above 2.45 GHz, the parasitic capacitances in the real design will force this number down.

Figure 7.13: Novel Front End Voltage Gain

The major improvement in this designs performance is in the LO leakage. Figure 7.15 shows the LO-RF and LO-IF isolation when the AC amplitude of LO+ is 650 mV, and that of LO- is 850 mV. Note that to test isolation, we cannot introduce device mismatch since only fixed device sizes are available in the CSM PDK. Therefore, amplitude and phase mismatch of the LO was introduced instead. As we can see, the LO-IF and LO-RF isolation is better than 60 dB. From Figure 7.14, we see that the isolation peaks when the phase error is zero. As we can see, by using the proposed circuit modifications, both LO-RF and LO-IF isolation can be improved by more than 30 dB. In fact, by increasing the power consumption of the buffer and the size of the mixer load capacitors, we can further improve LO-RF and LO-IF isolation to the desired level.

Figure 7.14: Novel Front End LO leakage

In conclusion, the novel design exhibits much better LO isolation and DC-Offset. Furthermore, we can expect the noise and voltage gain performance of the standard design to severely degrade when the novel isolation methods are used. This was proven in section 5.3 on passive Mixers. Although the novel design requires more power consumption, standard DC-Offset reduction techniques are also typically power hungry. Furthermore, standard methods come with the various tradeoffs mentioned in section 3.3. In the next chapter we will present the layout as well as post-layout simulation results of our chosen design.

7.4 Summary

This results section has presented three sets of results. First we presented the LNA which uses the methods outlined in section 6 to optimize the noise figure. By keeping V_{GS} as

low as possible (0.63 V), we were able to increase the device size which results in higher gain when L_g is fixed and lower noise figure. The second set of results was for the standard front end. Because of the passive Mixer operation, we obtained very low flicker noise. Finally, the third design illustrated how LO leakage can be minimized by increasing the output capacitance and lowering the impedance seen looking into the RF port of the Mixer. We showed that the improvement in the LO-IF and LO-RF isolation was more than 30 dB over the standard design.

CHAPTER 8

LAYOUT FOR TESTABILITY

The layout of a design is the determining factor on whether the circuit will work, whether it will not work or whether it will work well. Layout is so important that several books are dedicated to it [78], [79]. The goal of this section is not to present exact layout guidelines, such as how the metal width of a line is calculated so it can support the desired current, but to highlight certain important points when designing direct conversion front ends. This section will briefly discuss design symmetry, shielding, and component placement. We will then discuss how the layout was made to conform to the available test equipment. Finally we will present the post-layout simulation results.

8.1 Design Symmetry

The main purpose of a balanced design is to cancel second order distortion. Hence it is important to have good design symmetry. One simple way to ensure good design symmetry is to design one symmetric half of the circuit and then mirror it to the other side. Lack of design symmetry in front ends leads to LO leakage which then results in DC-Offset.

8.2 Shielding

The purpose of shielding is to prevent capacitive coupling of a signal from one line to another. A shield is usually formed by several layers of metal and a diffusion layer all joined together and shorted to ground. Assuming we have two signal lines. Without a shield, we would have a capacitor connecting the two signal lines. Figure 8.1 shows the result of shielding. The shielding capacitor could be hundreds to thousands of times the size as the coupling capacitors. Hence it is easy to see the no signal will leak from A to B.

Figure 8.1: Shielding

In the front end, the most important element to shield is the VCO. This is because the VCO signal level is very high (more than 1 V peak to peak). As previously explained, LO leakage to the RF ports can cause self mixing. That said, the LO line leaving the VCO shielding should be as short as possible and should go as directly as possible to the Mixer LO port.

8.3 Component Placement

To get circuit performance, it is also necessary to place the components correctly. For example, try not to have other signal lines running over or near the LO signal lines. Furthermore, there is a minimum spacing required from inductors to any other metal line.

For the CSM PDK, this is about 50 microns and 100 microns from one inductor to another. Because of this, each inductor can easily occupy an area of 250 by 250 microns. With six required inductors, we can see that a full front end is necessarily large.

8.4 Layout for Equipment Conformity

Because the design is not intended to be packaged, we will have to do on-wafer testing. Since we are using a balanced design, we need differential probes. The probe station is arranged such that signals are input from the sides. Usually the bias voltages are input from the top and bottom. Figure 8.2 shows the probe layout which is ideal for this project.

Figure 8.2: Wafer Probe Station Layout

One problem is a bias circuit would have to be added for V_{bias} . Another problem is that we don't have a differential signal generator available to us. Therefore there could be difficulty in getting good amplitude and phase match between the LO differential signals. To curb this problem, we used an on-chip differential output VCO to directly feed the front end. The design of the VCO was borrowed from a colleague and the design has been silicon verified. Using a VCO allowed us to remove the LO signals from the probe station and also gave us room for extra bias voltages. Figure 8.3 shows the final probe station layout. V_{cont} is a control signal for the VCO. Figure 8.4 shows the layout of the front end.

Figure 8.3: Final Probe Station Layout

Figure 8.4: Final Design Layout

From Figure 8.4, we can see the shielding and bond pads surrounding the entire layout. Adding extra bond pads at the output allows us to independently test the LNA, Buffer output and the Mixer output. For example, when the LNA output is disconnected, it looks like an open circuit and therefore does not have much effect on the overall circuit. From Figure 8.4, we can also see that the VCO is shielded, and the LO+ and LO- metal lines cross over a minimum area of other metal lines.

8.5 Post-Layout Simulation

For post-layout simulation, the VCO had to be removed. This is because SpectreRF is unable to test a frequency conversion stage when the LO is derived from the circuitry.

The component values are the same as in section 7.1 and 7.3 with the exception of C_1 in the LNA which is changed from 270 fF to 150 fF to account for the parasitic capacitance introduced by the bonding pads. The power consumption of the full front end is the same (22.05 mW) as in the schematic phase. The Novel Design achieves and IIP3 of -13.9 dBm in post-layout simulation.

Figure 8.5 shows the front end voltage gain. From the figure, we can see that there is a significant gain increase from the schematic to the post-layout phase. Furthermore, the peak gain occurs at 2.42 GHz. The gain flatness is around 0.3 dB.

Figure 8.5: Post-Layout Voltage Gain

Figure 8.6 shows the post-layout noise figure of the novel front end. If we were to take the double sideband noise figure, it would be less than 2 dB. The noise corner frequency is around 100 Hz. In a fabricated design, we cannot expect such good performance.

Figure 8.6: Post-Layout Noise Figure

Figure 8.7 show the LO leakage to the IF and RF ports. Once again we have set the AC amplitude of LO+ to 650 mV and LO- to 850 mV. From Figure 8.7, the LO-IF and LO-RF isolation are better than 60 dB. The post-layout simulation results are very close to the schematic simulation results.

Figure 8.7: Post-Layout LO leakage

CHAPTER 9

CONCLUSION AND FURTHER WORK

The theme of this thesis was the design of low noise direct conversion receiver design with low DC-offset. Our goal was to minimize the noise figure and the LO self-mixing induced DC-Offset. Because we chose to implement a receiver for mobile communications, it was also necessary to optimize the power consumption.

The novel front end designed showed a noise figure of less than 2 dB which is better than any reported figure among fully integrated CMOS receivers. Furthermore, the noise corner frequency is 100 Hz which is 450 times better than the state of the art. Using only 14.7 mA of current, the power consumption of the novel front end is comparable to current designs. The Novel Design also incorporates a novel DC-offset reduction technique which results in a 35 dB improvement in LO leakage. Furthermore, the novel technique does not come with the performance tradeoffs of other proposed methods. Although there are obvious performance improvements in the novel design, they cannot be fully confirmed until a fabricated design is tested.

In this thesis, we have also presented a novel current reuse method which can greatly reduce LNA power consumption while maintaining high LNA performance. This thesis also presents several analyses which contribute to RFIC design knowledge base. These analyses are: minimum noise figure of a DCR, modified Friis equation for low-IF and

homodyne receivers, LNA noise figure optimization, comparison of active and passive Mixers, and LO leakage calculation.

9.1 Further Work

For the novel design, one area which was not fully developed was the buffer design. In this thesis we designed a simple push pull source follower. There were two designs presented. The 6 mA design has a 2.5 ohm output impedance and the 3 mA design has an 8 ohm output impedance. To the author's knowledge, there are two possible improvements to this design. Firstly, we can share the current between the LNA and the buffer like what was done in the LNA, Phase Splitter co-design. Secondly, we could use a stacked source follower to get lower output impedance. Both methods would result in lower power consumption.

There is also the possibility of using Op-Amp feedback techniques to get the low output impedance. It is not normally possible to design an Op-Amp at such high frequency, but the feedback techniques would still apply to a certain degree.

Another obvious area of further work is in testing a fabricated design. Because of complications which arose when attempting to have the design fabricated, we only have simulated results for the novel front end. Layout and post-layout simulation is complete however, and tapeout and testing will be a subject of future work.

Chartered Semiconductor Manufacturing has supported various RFIC design projects in NTU with free tape-out. The free tape-out, however, is subject to the availability of chip area and there is usually a waiting time of up to 9 months. So far, several projects in NTU have been designed using the CSM PDK and successfully implemented using the 0.18 μm CSM RF CMOS process.

AUTHOR'S PUBLICATIONS

Do Aaron, Zhang Yue Ping, Do Manh Anh, "A Simple DC-Offset Reduction Technique for CMOS Passive Mixers" Under Review at *IEEE Transactions II: Circuits and Systems*

REFERENCES

- [1] R. W. Woodings, M. Gerrior, Cypress Semiconductor, "Avoiding Interference in the 2.4-GHz ISM Band", 2005,
<http://www.mwec.com/showArticle.jhtml?articleID=163700631>
- [2] A. Matsuzawa, "RF-SoC—Expectations and Required Conditions", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 50, pp. 245-253, 2002
- [3] P. Meade, UWB Insider, "SiGe vs. CMOS: Can One Chip fit all?" 2004,
http://www.uwbinsider.com/technology/2_3_SiGe_CMOS.html.
- [4] C. Andren, "Use Direct Conversion to Shrink WLAN Radio Costs",
Communications Systems Design, 2002, pp. 44-48, www.CommsDesign.com
- [5] S. Zhou, M. C. F. Chang, "A CMOS Passive Mixer with Low Flicker Noise for Low-Power Direct-Conversion Receiver", *IEEE Journal of Solid-State Circuits*, Vol. 40, pp. 1084-1093, May 2005.
- [6] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998
- [7] P. Leroux, J. Janssens, M. Steyaert, "A 0.8-dB NF ESD-Protected 9-mW CMOS LNA Operating at 1.23 GHz", *IEEE Journal of Solid-State Circuits*, Vol. 37, pp. 760-765, 2002
- [8] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001
- [9] B. Razavi, *RF Microelectronics*, Prentice Hall PTR, 1998
- [10] H. Aoki, M. Shimasue, "Channel Width and Length Dependent Flicker Noise Characterization for n-MOSFETs", *Proc. IEEE 2001 Int. Conference on Microelectronic Test Structures*, Vol. 14, 2001, pp. 257-261

- [11] WJ Communications, Technical Notes Vol. 7, "High Dynamic Range Receiver Parameters"
- [12] A. Bateman, "Transmitter & Receiver Architectures", 2005,
http://www.avren.com/Courses/TX_RX_Architectures_plain.htm
- [13] Palo Wireless Bluetooth Resource Center, "Bluetooth Radio", 2005,
<http://www.palowireless.com/infotooth/tutorial/radio.asp>
- [14] Center for Computer Research in Music and Acoustics (CCRMA), Stanford University, "FM Spectra", 2005,
http://ccrma.stanford.edu/%7Ejos/mdft/FM_Spectra.html
- [15] C. Lee, "Narrowband Noise Representation", 2005,
http://www.elec.mq.edu.au/~cl/files_pdf/elec321/lect_nb_noise.pdf
- [16] X. P. Li, H. S. Kim, Mohammed Ismail and Hakan Olsson, "A Novel Design Approach for GHz CMOS Low Noise Amplifiers", *Radio and Wireless Conference*, 1999, pp. 285-288
- [17] A. Pascht, J. Fischer, M. Berroth, "A CMOS Low Noise Amplifier at 2.4 GHz with Active Inductor Load", *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2001, pp. 1-5
- [18] M. C. Sun, S. Tenqchen, Y. H. Shu, W. S. Feng, "A 2.4 GHz CMOS Image-Reject Low Noise Amplifier", *Proceedings of the 2003 International Symposium on Circuits and Systems*, Volume 1, 2003, pp. I-329 - I-332
- [19] E. Kunz, S. Parke, "2.4GHz High Gain Low Power Narrowband Low-Noise Amplifier (LNA) in 0.18 μ m TSMC CMOS", *IEEE Workshop on Microelectronics and Electron Devices*, 2004, pp. 52-54

- [20] J. N. Yang, C. Y. Lee, T. Y. Hsu, T. R. Hsu, Chung-Cheng Wang, "A 1.5-V, 2.4GHz CMOS Low-Noise Amplifier", *Proc. 43rd Midwest Symposium on Circuits and Systems*, 2000, pp. 1010-1012
- [21] B. Chi, B. Shi, "A 1.8V 2.4GHz CMOS On-Chip Impedance Matching Low-Noise Amplifier for WLAN Applications", *Proceedings of the 2003 International Symposium on Circuits and Systems*, 2003, pp. II-188 - II-191
- [22] H. S. Kim, X. Li, M. Ismail, "A 2.4GHz CMOS Low Noise Amplifier using an Inter-stage Matching Inductor", *42nd Midwest Symposium on Circuits and Systems*, 1999, pp. 1040 -1043
- [23] D. J. Cassan, J. R. Long, "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18- μ m CMOS", *IEEE Journal of Solid-State Circuits*, Vol. 38, pp. 427-435, 2003.
- [24] A. R. Shahani, D. K. Shaeffer, T. H. Lee, "A 12-mW Wide Dynamic Range CMOS Front End for a Portable GPS Receiver", *IEEE Journal of Solid-State Circuits*, Vol. 32, pp. 2061-2070, December 1997.
- [25] C. Y. Cha, S. G. Lee, "A 5.2-GHz LNA in 0.35 μ m CMOS Utilizing Inter-Stage Series Resonance and Optimizing the Substrate Resistance", *IEEE Journal of Solid-State Circuits*, Vol. 38, pp. 669-672, April 2003.
- [26] D. K. Shaeffer, T. H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier", *IEEE Journal of Solid-State Circuits*, Vol. 32, pp. 745-759, May 1997.
- [27] J. L. Ny, B. Thudi, J. McKenna, "A 1.9 GHz Low Noise Amplifier", class project for EECS 522, Department of Electrical Engineering and Computer Sciences, University of Michigan at Ann Arbor.

- [28] T. P. Liu, E. Westerwick, "5-GHz CMOS Radio Transceiver Front End Chipset", *IEEE Journal of Solid-State Circuits*, Vol. 35, pp. 1927-1933, December 2000.
- [29] H. W. Chiu, S. S. Lu, Y. S. Lin, "A 2.17-dB NF 5-GHz-Band Monolithic CMOS LNA With 10-mW DC Power Consumption", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, pp. 813-824, March 2005.
- [30] M. Soyuer, J. O. Plouchart, H. Ainspan, J. Burghartz, "A 5.8-GHz 1 -V Low-Noise Amplifier in SiGe Bipolar Technology", *IEEE Radio Frequency Integrated Circuits Symposium*, 1997, pp. 19-22
- [31] J. Sadowy, J. Graffeuil, E. Tournier, L. Escotte, R. Plana, "Advanced Design of high linearity, Low noise amplifier for WLAN using a SiGe BiCMOS Technology.", *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2001, pp. 6-11
- [32] G. Zhang, A. Dengi, L. R. Carley, "Automatic Synthesis of A 2.1 GHz SiGe Low Noise Amplifier", *IEEE Radio Frequency Integrated Circuits Symposium*, 2002, pp. 125-128
- [33] J. Kaukovaori, M. Hotti, J. Ryyanen, J. Jussila, K. Halonen, "A Linearized 2-GHz SiGe Low Noise Amplifier for Direct Conversion Receiver", *Proceedings of the 2003 International Symposium on Circuits and Systems*, 2003, pp. II-200 - II-203
- [34] U. Erben and E. Sonmez, "Fully differential 5 to 6 GHz low noise amplifier using SiGe HBT Technology", *Electronics Letters*, Vol. 40, pp. 39-41, January 2004

- [35] S. Mou, J. Ma, K. S. Yeo, M. A. Do, "An Integrated SiGe Dual-band Low Noise Amplifier for Bluetooth, HiperLAN and Wireless LAN Applications", *33rd European Microwave Conference*, Munich 2003, pp. 5-8
- [36] F. Plessas, G. Kalivas, "A 5-GHz, Variable Gain, SiGe Low Noise Amplifier", *Proc. 24th International Conference on Microelectronics (MIEL 2004)*, May 2004, pp. 609-612
- [37] K.W. Kobayashi, L.T. Tran, A.K. Oki, and D.C. Streit, "Noise optimization of a GaAs HBT Direct-coupled low noise amplifier", *IEEE MTT-S International Microwave Symposium Digest*, 1996, pp. 815-818
- [38] P. B. Khannur, K. S. Ling, "A 2.45GHz Fully-Differential CMOS Image-Reject Mixer for Bluetooth Application", *IEEE Radio Frequency Integrated Circuits Symposium*, 2002, pp. 439-442
- [39] C. G. Tan, "A High-Performance Low-Power CMOS Double-Balanced IQ Down-Conversion Mixer for 2.45-GHz ISM Band Applications", *IEEE Radio Frequency Integrated Circuits Symposium*, 2003, pp. 457-460
- [40] C. C. Chang, R. M. Weng, J. C. Htiang, K. Hsu, K. Y. Lin, "A 1.5 V High Gain CMOS Mixer for 2.4-GHz Applications", *The 2001 IEEE International Symposium on Circuits and Systems*, 2001, pp. 782-785
- [41] J. Cui, Y. Lian, M. F. Li, "A Low Voltage Dual-Gate Integrated CMOS Mixer for 2.4 GHz Band Applications", *IEEE International Symposium on Circuits and Systems*, 2004, pp. I - 964-7

- [42] H. C. Wei, R. M. Weng, K. Y. Lin, "A 1.5 V High-Linearity CMOS Mixer for 2.4 GHz Applications", *The 2004 IEEE International Symposium on Circuits and Systems*, 2004, pp. I - 561-4
- [43] H. Sjöland, A. K. Sanjaani, A. A. Abidi, "A Merged CMOS LNA and Mixer for a WCDMA Receiver", *IEEE Journal of Solid-State Circuits*, Vol. 38, pp. 1045-1050, June 2003
- [44] T. J. Jung, C. C. K. Sau, Jack Lau, "A 2.4 GHz Four Port Mixer for Direct Conversion Used in Telemetry", *The 2001 IEEE International Symposium on Circuits and Systems*, 2001, pp. 378-381
- [45] K. J. Koh, M. Y. Park, C. S. Kim, H. K. Yu, "Subharmonically Pumped CMOS Frequency Conversion (Up and Down) Circuits for 2-GHz WCDMA Direct-Conversion Transceiver", *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 871-884, June 2004.
- [46] T. W. Kim, B. Kim, K. Lee, "Highly Linear Receiver Front End Adopting MOSFET Transconductance Linearization by Multiple Gated Transistors", *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 223-229, January 2004.
- [47] Z. Li, R. Quintal, K. K. O, "Dual-Band CMOS Front End With Two Gain Modes for Wireless LAN Applications", *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 2069-2073, November 2004.
- [48] I. Kwon, K. Lee, "An Integrated Low Power Highly Linear 2.4-GHz CMOS Receiver Front End Based on Current Amplification and Mixing", *IEEE Microwave and Wireless Components Letters*, Vol. 15, pp. 36-38, January 2005.

- [49] J. Lon, R. J. Webber, "An Integrated 2.4 GHz CMOS RF Front End", *IEEE Aerospace Conference Proceedings*, 2004, pp. 2378-2383
- [50] S. Sampei, K. Feher, "Adaptive DC-offset compensation algorithm for burst mode operated direct conversion receivers", *Proceedings of Vehicular Technology Conference*, 1992, pp. 93-96
- [51] J. C. Gu, S. L. Yu, "Removal of DC-Offset in current and voltage signals using a novel Fourier filter algorithm", *IEEE Transactions on Power Delivery*, Vol. 15, 2000, pp. 73-79
- [52] B. Matinpour, S. Chakraborty, L. Laskar, "Novel DC-offset cancellation techniques for even-harmonic direct conversion receivers", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 48, pp. 2554-2559, Dec. 2000
- [53] B. Lindoff, "Using a direct conversion receiver in EDGE terminals-a new DC offset compensation algorithm", *IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, 2000, pp. 959-963
- [54] Y. You et. Al, "Performance of simple timing synchronization and DC-offset compensation schemes for a short-ranged Bluetooth network", *IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, 2000, pp.1320-1324
- [55] Z. Zhang, Z. Chen, L. Tsui, J. Lau, "A 930 MHz CMOS DC-offset-free direct-conversion 4-FSK receiver", *IEEE International Solid-State Circuits Conference*, 2001, pp. 290-291
- [56] M. Faulkner, "DC-Offset and IM2 removal in direct conversion receivers", *IEE Proceedings-Communications*, 2002, pp. 172-184

- [57] I. Sohn, E. Jeong, Y.H. Lee, "Data-aided approach to I/Q mismatch and DC-Offset compensation in communication receivers", *IEEE Communications Letters*, Vol. 6, pp. 547-549, 2002
- [58] C. K. Ho, S. Sun, P. He, "Low complexity frequency offset estimation in the presence of DC-Offset", *IEEE International Conference on Communications*, 2003, pp. 2051-2055
- [59] C. Lanschutzer, A. Springer, L. Maurer, Z. Boos, R. Weigel, "Integrated adaptive LO-leakage cancellation for W-CDMA direct upconversion transmitters", *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2003, pp. 19-22
- [60] H. Yoshida et. Al, "Fully differential direct conversion receiver for W-CDMA using an active harmonic Mixer", *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2003, pp. 395-398
- [61] H. Wang, M. Lin, Y. Li, H. Chen, "A novel dynamic DC-offset canceller", *Proceedings. 5th International Conference on ASIC*, 2003, pp. 639-642
- [62] P. Laferriere, D. Rahn, C. Plett, J. Rogers, "A 5Ghz Direct-Conversion Receiver With DC-Offset Correction", *Proceedings of the 2004 International Symposium on Circuits and Systems*, 2004, pp. 269-272
- [63] J. Yan, Y. Zheng, Y. P. Xu, " A novel DC-offset cancelling circuit for DCR", *IEEE International Symposium on Circuits and Systems*, 2005, pp. 396-399
- [64] A. T. Phan, C. W. Kim, M. S. Jung, Y. A. Shim, J. Y. Kim, S. G. Lee, "A Novel 1.5V DC-Offset Cancellation CMOS Down Conversion Mixer", *Proceedings of IEEE International Symposium on Circuits and Systems*, 2005, pp. 3704-3707

- [65] P. U. Su, Y. H. Chen, T. Y. Yang, "A 0.35- μ m SiGe WCDMA Direct Conversion Transmitter With DC-Offset Compensation for Carrier Leakage Reduction", *Proceedings of the International Symposium on VLSI Design, Automation and Test*, 2005, pp. 149-152
- [66] P. Andreani, H Sjöland, "Noise Optimization of an Inductively Degenerated CMOS Low Noise Amplifier", *IEEE Transactions On Circuits and Systems-II: Analog And Digital Signal Processing*, Vol. 48, pp. 835-841, 2001
- [67] M. Egels, J. Gaubert, P. Pannier and S. Bourdel, "Design method for fully integrated CMOS RF LNA", *Electronics Letters*, Vol. 40, No. 24, 2004
- [68] R. Lu, "CMOS Low Noise Amplifier Design for Wireless Sensor Networks", University of California at Berkeley, 2003
- [69] J. Janssens, M. Steyaert, "Optimum MOS Power Matching by Exploiting non-quasistatic effect", *Electronic Letters*, Vol. 35, pp. 672-673, 15 Apr 1999
- [70] A. J. Scholten et. Al, "Noise Modeling for RF CMOS Circuit Simulation", *IEEE Transactions on Electron Devices*, Vol. 50, pp. 618-632, 2003
- [71] M. J. Deen, C. H. Chen, "MOSFET Modeling for Low Noise, RF Circuit Design", *Proceedings of the IEEE Custom Integrated Circuits Conference*, 2002, pp. 201-208
- [72] C. H. Chen, M. J. Deen, "Channel Noise Modeling of Deep Submicron MOSFETs", *IEEE Transactions on Electron Devices*, Vol. 49, pp. 1484-1487, 2002
- [73] J. J. Liu, "Analysis and Design of CMOS Mixers for Direct Conversion Receivers", M.S. Thesis, School of EEE, NTU, Singapore, 2005.

- [74] Z. Zhang, J. Lau, "Experimental Study on MOSFET's Flicker Noise under Switching Conditions and Modelling in RF Applications", *IEEE Custom Integrated Circuits Conference*, 2001, pp. 393-396
- [75] M. A. Do, J. J. Liu, K. S. Yeo and J. G. Ma, "Analysis of LO-leakage in CMOS Gilbert Mixer by Cadence SpectreRF for Direct Conversion Application", *IEEE Asia-Pacific Conference on Circuits and Systems*, 2004, pp. 309-312
- [76] J. G. Kenny, G. Rangan, K. Ramamurthy, G. Temes, "An Enhanced Slew Rate Source Follower", *IEEE Journal of Solid-State Circuits*, Vol. 30, pp. 144-146, Feb. 1995
- [77] F. Gatta, E. Sacchi, F. Svelto, P. Vilmercati, R. Castello, "A 2-dB Noise Figure 900-MHz Differential CMOS LNA", *IEEE Journal of Solid-State Circuits*, Vol. 36, pp. 1444-1452, 2001
- [78] A. Hastings, *The Art of Analog Layout*, Pearson Education Asia Limited, Tsinghua University Press, 2004
- [79] C. Saint, J. Saint, *IC Mask Design*, McGraw Hill, 2003