A transducer for tomograph imaging applications

Peng, Jia

2006

Peng, J. (2006). A transducer for tomograph imaging applications. Master's thesis,
Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/46917>

<https://doi.org/10.32657/10356/46917>

Nanyang Technological University

Downloaded on 26 Apr 2023 19:22:26 SGT

**A Transducer For Tomography^{Ph} Imaging
Applications**

Peng Jia

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Master of Engineering

2006

TK
7872
.T6
P398
2006

STATEMENT OF ORIGINALITY

I hereby certify that the content of this thesis is the results of work done by me and has not been submitted for higher degree to any other university or institution.

Aug 1st, 2006

Date

PENG JIA

ACKNOWLEDGMENTS

It is my pleasure to express my sincere gratitude and appreciation to my supervisor, Associate Professor Chan Pak Kwong. It was he who chose this promising topic for my research work. His never-ending flow of ideas, great acknowledgments in IC design field and infectious enthusiasm led me through a very rewarding path. His concern and insight have helped me grow far beyond the boundaries of academic research. In particular, I want to thank Prof. Chan for the much-needed encouragement in the past one year, and for his admirable integrity.

Special thanks are also extended to my friends Fan Xian Ping, Ng Kian Ann and Lee Wing Foon for unconditionally offering their friendship. If it is not for their unselfish help and assistance, my progress in research would not have been so smooth. Their companionships make me have a wonderful and enjoyable research life.

Finally, I would like to acknowledge my husband Hongliang, my daughter Junlu and all my family members for their consistent love and support and always putting their highest priority on my education.

Abstract

This project aims at designing a tomography based switched-capacitor capacitance measuring system to detect the presence of individual articles or droplets within the process vessels or pipelines in the form of capacitive-to-voltage conversion. The performance of the front-end interface is crucial to the performance of the measuring system. A new fully-integrated switched-capacitor (SC) front-end capacitive transducer, which employs the correlated double sampling (CDS) technique to reduce the dc offset and $1/f$ noise of the CMOS amplifier, is proposed. It utilizes the resettable topology to facilitate the high speed charging and discharging operation under heavy stray capacitance of 150 pF. In addition, the non-ideal analysis of the transducer is presented. This includes the establishment of different types of error source models together with practical mismatch effects in the derivation of second-order analytical expressions, with particular emphasis on investigating the parasitic bootstrapping gain factor affecting the other errors due to the existence of heavy stray capacitors. The conservative simulation results have shown that the capacitive transducer differential output displays the baseline dc offset of 0.083 mV at 25 °C, the baseline capacitance change of 1 fF from 25 °C to 40 °C and the output temperature coefficient of 0.045 mV/ °C from 25 °C to 100 °C at the measuring capacitance of 1 pF. When the capacitive transducer is extended to a complete system comprising the transducer itself plus the back-end electronics like the differential-to-single-ended chopping amplifier and 3rd order filter, the results have also shown that the system still maintains a good linear relationship between C_x (detected capacitor) and the output voltage. The system can achieve more than 400 frames per second data sampling rate.

TABLE OF CONTENTS

Chapter 1	Introduction	1
1.1	Motivations	1
1.2	Objectives	3
1.3	Major Contributions of the Thesis	4
1.4	Organization of the Thesis	5
Chapter 2	Design Techniques for Precision Analog	6
2.1	The Need for Offset Cancellation Technique in the ECT Sensor	7
2.2	Chopper Stabilization Approach	9
2.3	Auto Zero Cancellation Approach	14
2.4	Chopper Stabilization Technique versus Auto Zero Technique	18
Chapter 3	Background of Tomography	19
3.1	Tomography Imaging Basics	19
3.2	Review of tomography sensing interfaces	22
3.3	Limitations of the Previous ECT Systems	28
Chapter 4	Architecture Design	31
4.1	The Proposed Capacitive Measuring System	31
4.2	The Novelty and Advantages of the Proposed System Architecture	32
Chapter 5	Circuit Design	35
5.1	Proposed Sensor Interface	35
5.1.1	Basic Structure of Proposed Sensor Interface without CDS	35
5.1.2	Proposed Sensor Interface with CDS	38
5.2	The Chopper Amplifier Gain Stage	47
5.3	The Continuous-Time Filter	48
5.4	House Keeping Circuits	51
5.4.1	High-Speed op-amp for front-end transducer	52
5.4.2	Chopper-stabilized op-amp for gain stage	55
5.4.3	Biasing Circuit Design	58
5.4.4	Biphasic Non-Overlapping Clock	61
5.4.5	Gain-Enhanced VI converter	62

Chapter 6	Analysis of Front-End Tomography Transducer	64
6.1	Transducer Settling Error	64
6.2	Switch Errors	66
6.3	Analysis of Transducer including Error Source Models	70
6.4	Analyzing Differential Operation of SC Transducer	76
Chapter 7	Layout Design Considerations	81
7.1	Introduction	81
7.2	Resistors	81
7.2.1	Resistivity and Sheet Resistance	81
7.2.2	Temperature Variation	83
7.2.3	Voltage Modulation	84
7.2.4	Matching of resistors	85
7.2.5	Resistors in AMS 0.6 μ m CMOS process	86
7.3	Capacitors	87
7.4	MOS Transistors	89
7.5	Sensor layout	95
Chapter 8	Results and Discussions	98
8.1	The Front-End CV converter	98
8.2	The Chopper Operational Amplifier	107
8.3	The Continuous-Timer Filter	109
8.4	Integrated System	112
Chapter 9	Conclusion and Recommendation	122
9.1	Conclusion	122
9.2	Recommendation	124
References		126
Author's publications		130

LIST OF FIGURES

Figure 2.1 Noise power spectrum of a standard CMOS op-amp.....	6
Figure 2.2 Chopper stabilization technique.....	11
Figure 2.3 Noise power spectrum of chopper technique.....	12
Figure 2.4 Residual offset introduced by chopper technique.....	14
Figure 2.5 Noise power spectrum of auto-zeroing technique.....	15
Figure 2.6 Auto-Zero principle.....	16
Figure 2.7 Auto-Zero with auxiliary opamp.....	17
Figure 3.1 A typical electrical capacitive unit.....	20
Figure 3.2 Cross sectional view of typical ECT sensor with 12 electrodes.....	21
Figure 3.3 The charge/discharge capacitance measuring circuit.....	25
Figure 3.4 The ac-based capacitance measuring circuit.....	26
Figure 3.5 Complete capacitance measurement channel for one electrode which can be set as excitation or detection.....	28
Figure 4.1 Overall system block diagram.....	32
Figure 5.1 Proposed front-end capacitance measuring circuit without CDS.....	36
Figure 5.2(a) Front-end ECT transducer with CDS.....	40
Figure 5.2(b) The switch control signals for the CDS transducer.....	41
Figure 5.3(a) Simplified circuit during T1.....	42
Figure 5.3(b) Simplified circuit during T2.....	42
Figure 5.3(c) Simplified circuit during T3.....	43
Figure 5.3(d) Simplified circuit during T4.....	43
Figure 5.4 Chopper amplifier gain stage.....	47

Figure 5.5 RC low-pass filter.....	49
Figure 5.6 Sallen-Key low-pass filter.....	50
Figure 5.7 The third-order low-pass filter.....	51
Figure 5.8(a) A high-speed two stage op-amp.....	54
Figure 5.8(b) Small-signal model for high speed op-amp.....	55
Figure 5.9 Chopper-stabilization op-amp.....	57
Figure 5.10 The biasing circuit with startup circuit.....	60
Figure 5.11 Schematic of non-overlapping biphasic clock circuit.....	62
Figure 5.12 Non-overlapping biphasic clock signal.....	62
Figure 5.13 Gain-enhanced VI converter.....	63
Figure 6.1 Switching off respective NMOS switch on a op-amp voltage source model during charge transfer phase for V_{out2} at T1 and V_{out1} at T3.....	67
Figure 6.2 Auto-zero phase ϕ_1 and charge transfer phase ϕ_2 of CD1.....	71
Figure 6.3 Auto-zero phase ϕ_2 and charge transfer phase ϕ_1 of CD2.....	72
Figure 6.4 Differential output of transducer based on ideal subtractor and filter.....	77
Figure 7.1 The definition of the width and length of a resistor.....	83
Figure 7.2 Layout of two matched resistors.....	85
Figure 7.3 Simple model of resistor with parasitic capacitance.....	86
Figure 7.4 Layout of two matched capacitors.....	88
Figure 7.5 Simple model of capacitor with parasitics.....	89
Figure 7.6 MOS transistor layout.....	90
Figure 7.7 Layout of two matched transistors.....	91
Figure 7.8 Dummy line for horizontal shielding.....	93

Figure 7.9 Analog and digital section sharing the same power supply.....	94
Figure 7.10 Improved way to reduce the noise coupling from the digital section into the analog section.....	94
Figure 7.11 The layout of the whole sensor system.....	97
Figure 8.1 AC analysis of the front-end op-amp.....	99
Figure 8.2 The set-up diagram for front-end transducer simulation.....	101
Figure 8.3 Output voltage versus C_x from 0 to 10fF.....	103
Figure 8.4 Output voltage versus C_x from 0 to 2pF.....	104
Figure 8.5 Output voltage versus temperature from 0 to 100°C with $C_x=0$ pF.....	105
Figure 8.6 Output voltage versus temperature from 0 to 100°C with $C_x=1$ pF.....	105
Figure 8.7 The ac analysis of chopper operational amplifier.....	108
Figure 8.8 The simulated common mode rejection ratio for chopper op-amp.....	109
Figure 8.9 The simulated cut-off frequency of the continuous-time filter in different process conditions.....	110
Figure 8.10 The noise simulation for 3 rd order low-pass filter.....	111
Figure 8.11 The integrated system for system simulation.....	112
Figure 8.12 The simulation results of the first stage outputs and the final filter output.....	114
Figure 8.13 The simulation results of the first stage output and the second chopper amplifier stage output	115
Figure 8.14 The zoom-in view of the first stage output waveforms.....	116
Figure 8.15 Monte Carlo simulation results for V_{out} with $C_x=1$ pF.....	117
Figure 8.16 Step response of the proposal capacitance measuring circuit.....	118

Figure 8.17 Simulation results showing the relationship between the capacitance C_x and the DC output voltage.....119

Figure 8.18 Simulation results showing relationship between the temperature and the output DC voltage at $C_x=1\text{fF}$120

Figure 8.19 Simulation results showing relationship between the temperature and the output DC voltage at $C_x=1\text{pF}$121

Figure 9.1 The boost-strapped circuit.....125

CHAPTER 1

Introduction

1.1 Motivations

Tomography process provides the real-time cross-sectional images of the distribution of materials in a process [1]. By analyzing two suitably spaced images it will be possible to measure the direction and speed of material movement. In the last decade, techniques have been developed rapidly to visualize the internal behavior of industrial tomography process, for example: the gas /oil flows in oil pipelines, the gas /solid flows in pneumatic conveyors [47] and the separation /mixing processes in chemical vessels [3]. A wide range of applications is possible to process [48]-[49], with the interrogation of mixing and separation processes being the prime candidates. By tomographically imaging the density and velocity distribution of the vessel contents, a more structured approach to modeling, design, and operation should be possible.

A Capacitance Tomography System is normally subdivided into three basic parts [1]: the capacitor sensor, the sensor electronics and the image display. The performance of the sensor electronics part is crucial to the performance of the whole system. To measure fine detail such as a small gas bubble inside an oil pipe as an example, the Electrical Capacitance Tomography (ECT) [2] sensing interface is the sensor electronics and should

display an adequate resolution for detection of minute capacitance change whilst maintaining very stable performance against the time and temperature. Consequently, the basic requirements for the design of a quality ECT sensor are translated to the following characteristics [2]:

- 1) Low baseline drift. (few tens mV)
- 2) Stray-immune, because ECT's stray capacitance (typically 150 pF) to earth is huge compared with the measured capacitance.
- 3) Fast data acquisition speed. (Data capture rate > 100 frames/second)
- 4) Wide dynamic range of measurement (10 fF to 2 pF).
- 5) High sensitivity and precision (0.3 fF, corresponding to a 2% gas void fraction change in the central area of the pipe).

There are two types of Electrical Capacitance Tomography systems (ECT):

- 1) The switched-capacitor (SC) ECT system [2]-[3]
- 2) The AC based ECT system [4]-[6].

Both systems are researched successfully by the University of Manchester, Institute of Science and Technology (UMIST). The former was the first successful approach using a charging and discharging circuit to build a real-time ECT transducer. The shortcomings are the heavy parasitic capacitance effect [8] and the large base line drift caused by the system offset. The later can overcome the charge injection and the clock feedthrough problems, but the ultimate sensitivity still relies on the linearity, accuracy and baseline drift of the analog processing circuits, like rectifier and multiplier. Hence, there is a need

for the measurement interface circuit to get good performance for the above issues by reaching the optimized solution among all the critical issues.

1.2 Objectives

The objectives of this project are as follows:

- a) To investigate a new capacitive sensor interface which employs correlated double-sampling technique [7] for the flicker noise and offset cancellation, whilst minimizing the dominant error source contributed by the charge injection effect.
- b) To design and simulate a tomography switched-capacitor measurement chip for a 12-electrode system using 0.6 μm AMS CMOS process.
- c) To address the circuit design issues such as offset, input-referred noise, charge injection for the design of a high-performance transducer.
- d) To analysis the non-ideal effects on the proposed switched-capacitor correlated double-sampling ECT transducer, which is not only suitable for fully integration but it also offers improved performance with respect to the prior-art transducers.

1.3 Major Contributions of the Thesis

The contributions of this thesis are summarized as follows:

- a) A new Electrical Capacitance Measuring Circuit has been proposed [9]. This includes a new front-end ECT circuit using the correlated double-sampling technique (CDS) followed by a chopped differential-to-single-ended amplifier and a 3rd order low-pass filter.
- b) HSPICE simulations have been performed to compare with the prior-art works, demonstrating that the proposed capacitance measuring system has a better performance in terms of precision, offset sensitivity and offset drift.
- c) The post-layout simulation has been conducted to verify the realistic operation of the system.
- d) Non-ideal effects of the front-end transducer have been analyzed, taking into account of the switch errors, gain errors, dc offset, component mismatches and heavy stray capacitors.

1.4 Organization of the Thesis

Chapter 1 gives the fundamental background about the electrode capacitance tomography sensor. Chapter 2 introduces the main offset cancellation techniques for precision analog design. Chapter 3 reviews the basic function of the ECT sensor and the different tomography imaging sensing systems. It also presents the existing problems in the current-art systems. Chapter 4 presents the proposed capacitive tomography sensing system. Chapter 5 details the circuit design for each building block, including the proposal of new front-end ECT interface circuit. Chapter 6 analyzes the non-ideal effects of the front-end tomography transducer. Chapter 7 discusses the layout perspective from system to the circuit. Chapter 8 deals with the discussion of the simulation results. This is then followed by Chapter 9 for drawing the concluding remarks and giving the recommendations for the future work.

CHAPTER 2

Design Techniques for Precision Analog

The purpose of the offset cancellation techniques is to reduce the effects of the narrow-band noise sources at the input of an operational amplifier stage. A brief analysis into the noise power spectrum of the standard CMOS operational amplifier (two-stage op-amp) is shown in Fig. 2.1 [7].

Fig. 2.1 Noise power spectrum of a standard CMOS op-amp

Fig. 2.1 shows the standard CMOS amplifier’s typical input-referred noise spectrum. From the plot, it can be seen that for rather high frequency, the noise can be considered as

frequency independent or white. This is usually called the thermal noise floor. At low frequency, the noise power is increasing almost linearly with decreasing frequency and therefore commonly called $1/f$ noise. The frequency at which the $1/f$ noise becomes dominant over the white noise is called the $1/f$ noise corner frequency. At very low frequency, offset (typical few mV) becomes the dominant error and may change due to aging and temperature variations. This implied that it had a certain bandwidth and could therefore be considered as a very low frequency noise source. There are two main offset-cancellation techniques, known as chopper stabilization (CHS) techniques and auto-zeroing (AZ) [including correlated double-sampling (CDS)] [7]. They will be discussed as follows.

2.1 The Need for Offset Cancellation Technique in the ECT Sensor

In an ECT sensory system, many non-ideal factors will limit the measurement scope. For the design of front-end stage, operational amplifiers are often encountered. Due to high-gain requirement for reason of resolution, the nonzero input-referred dc offset V_{os} (typically in a range of 1mV to 10mV) of op-amp are amplified significantly by the system. As a result, the output dc offset is pronounced. Not only does it limit the headroom of output swing, it also introduces drift against time and drift against temperature. Current ECT adopts baseline calibration arrangement such that the ECT controller samples the system offset and stores it in the system for further signal processing to subtract the offset effect. Although the method is effective to cancel the system offset, it needs regular calibration, which therefore increases the frequency of

interrupt action, which may not be desirable for a high-speed ECT system because of the goal of sampling images as high rate as possible. In order to reduce the offset for reduction of offset calibration time and increasing the stability of ECT system, the ECT sensor interface circuit itself should exhibit intrinsic low offset performance such that less interrupt time is achieved for final system offset calibration and higher capture rate is obtained. Besides, the $1/f$ noise is regarded as low-frequency noise, in the process of offset cancellation; the $1/f$ noise will be reduced significantly, thus leading to higher signal-to-noise ratio of the system. In addition to that, this benefits the use of CMOS technology for the ECT sensor design in terms of low cost, low power consumption and ease of VLSI integration. All of these advantages give the rationales on the need for offset cancellation in the ECT sensor.

2.2 Chopper Stabilization Approach

The chopper stabilization approach [7] uses circuit technique to shift the input noise energy from the base band to some high frequency so that it will not mix with the input signal. Unlike the AZ process, the CHS technique does not use sampling, but rather applies modulation to transpose the signal to a higher frequency where there is no $1/f$ noise, and then demodulates it back to the base band after amplification.

The principle of chopper stabilization [16] is illustrated in Fig. 2.2. The technique is implemented using a two-stage amplifier which has an open loop gain A . Two multipliers that are controlled by a chopping square wave were inserted at the input and the output of the first stage.

Since the first multiplier is between the inputs signals and inputs of amplifier's first stage, the signal can be modulated and translated to the odd harmonic frequencies of the chopping waves, while the noise (dc offset and $1/f$ noise) is unaffected. After the second multiplier, the signal can be demodulated back to the original base band while the noise is modulated to a higher frequency band as shown in Fig 2.2(b).

In Fig 2.2(a), the input of the chopper amplifier is a dc signal V_{in} , the signal at the output of the first chopper modulator will be a square wave with period T and amplitude V_{in} . Assuming the amplifier is an op-amp with input dc offset V_{os} , open loop gain A and an infinite bandwidth, the signal from the first stage output is simply the same square wave

from the first chopper with an amplitude $A \cdot V_{in}$ plus dc offset $A \cdot V_{os}$. The V_1 voltage from the output of the first stage is:

$$V_1 = A \cdot V_{in} \cdot \frac{4}{\pi} \left(\sin \omega t + \frac{1}{3} \sin 3\omega t + \frac{1}{5} \sin 5\omega t + \dots \right) + A \cdot V_{os} \quad (2.1)$$

Since the noise and offset are modulated only once, they are transposed to the odd harmonics of the output chopping square wave, leaving the amplifier ideally without any offset and low frequency noise. The signal V_{out} after demodulation and filter is again a dc signal of value $A \cdot V_{in}$.

$$V_{out} = A \cdot V_{in} \quad (2.2)$$

The signal from the second chopper modulator will pass through a third order low-pass filter, while the noise at the higher band of frequency will be filtered.

Fig. 2.2 Chopper stabilized technique

The noise power spectrum of the chopper amplifier is flat, as shown in Fig. 2.3 [7], with the dc offset and $1/f$ noise being removed perfectly. A chopping clock is required in this technique. This chopping frequency must be higher than $1/f$ corner frequency to effectively remove the offset and $1/f$ noise [7].

Fig. 2.3 Noise power spectrum of chopper technique

The residual noise of a chopper amplifier is fundamentally lower than the auto-zero amplifier. This is because the chopper amplifier is not sampled, which makes it impossible for the wideband thermal noise to fold back into baseband, shown in Fig. 2.4. The major problem of the chopper technique is that the chopper amplifier itself does introduce a residual offset, which was in the order of few tens μV . This offset is dependent on the f_{chop} . This residual offset at a chopper amplifier originated mainly from

the spikes of the input chopper. In turn, these spikes originated from the charge injection mismatch of the switches. Thus, after demodulation of the spikes, a residual offset occurs. It can be seen that the residual offset V_{os} is determined by the number of spikes and the energy content of the spikes, as illustrated in Fig. 2.4. Here, V_{dd} is the high voltage level of the chopping clock, the value is determined by the supply voltage of the system.

If the chopper frequency is reduced, the residue offset can be reduced. However, caution must be taken such that if the f_{chop} is reduced below $1/f$ noise corner frequency, the $1/f$ noise will not be effectively removed; if the f_{chop} were higher, more residue spikes would be introduced by the chopper switches. Here, it is important to choose the value of f_{chop} properly so that it is effectively sufficient to be slightly above $1/f$ corner frequency and yet kept the offset residue to a minimal level.

Fig. 2.4 Residual offset introduced by chopper technique

2.3 Auto Zero Cancellation Approach

The basic principle of auto-zeroing is sampling the unwanted quantity (1/f noise and offset) and then subtracting it from the instantaneous value of the contaminated signal either at the input or the output of the operational amplifier. The noise power spectrum of the chopper amplifier is shown in Fig. 2.5 [7].

Fig. 2.5 Noise power spectrum of auto-zeroing technique

The principle of the auto-zero technique is shown in Fig. 2.6 [16]. In the sampling phase (at which ϕ_1 is high and ϕ_2 is low), the output and the input of the amplifier are shorted together, so that the offset is sampled on capacitor C_{az} . In the amplification phase, the offset sample is subtracted. The $1/f$ noise is removed if the sampling frequency is higher than the corner frequency.

Fig. 2.6 Auto-Zero principle

The most important disadvantage of this circuit is the need for a sampling phase. This makes the output signal not continuously available. This can be overcome by using an auxiliary op-amp. The improved circuit is shown in Fig. 2.7 [16]. Besides, the problem of charge injection can be reduced by using low-sensitivity auxiliary inputs.

When Φ_1 is high, the offset of the auxiliary op-amp is sampled on capacitor C_1 . During the second phase (when Φ_2 is high), the offset of the main op-amp is measured with the auxiliary op-amp and sampled on C_2 . The offset of the main op-amp is therefore compensated while the output signal is continuously available. This method is used in many stand-alone op-amps.

Fig. 2.7 Auto-zero with auxiliary op-amp. Both amplifiers have low-sensitivity auxiliary inputs to reduce problem of charge injections

The advantage of the Auto-zero with auxiliary op-amp is the elimination of sampling phase that permits the continuous output signal.

The disadvantages are the complicated circuitry and subject to charge injection effect.

2.4 Chopper Stabilization Technique versus Auto Zero Technique

The relative advantages and disadvantages of the CHS (Chopper Stabilization) technique versus auto zero technique are listed below:

- 1) Auto zero cancellation technique is inherently a sampled-data method; CHS is based on modulation rather than sampling, and hence it can be used for continuous-time signals.
- 2) Auto zero cancellation technique reduces the low-frequency noise or offset by high pass filtering; CHS translates it to some out-of band frequency.
- 3) The output noise of an auto zero stage is normally dominated by the under sampled wideband noise; in a continuous-time CHS stage, the noise spectrum is not folded, and hence $1/f$ noise remains dominate in the base band before the second modulation. After demodulation, white noise is folded into the base band and replaces the $1/f$ noise. If the chopping frequency is much larger than the $1/f$ noise corner frequency, the base band white noise in the output is only very slightly larger than it was without CHS.
- 4) Auto zero cancellation technique can be used to enhance the effective gain of the operational amplifiers used in the signal processing. A continuous-time CHS system, by contrast, causes the operational amplifier to amplify a higher-frequency signal, and hence its effective gain is usually reduced.

CHAPTER 3

Background of Tomography

3.1 Tomography Imaging Basics

Electrical Capacitance Tomography (ECT) [2] is a technique for obtaining information about the distribution of the contents of closed pipes or vessels by measuring variations in the dielectric properties of the material inside the vessel [1]. Typical information obtainable includes cross-sectional images of the vessel contents and the measurement of the volume fraction and velocities of the content of pipes for multiple phase flows.

The feasibility of high speed ECT for measuring the component distribution has been demonstrated by many case studies. The earliest description of an electrical capacitance tomography system was in 1989 by Huang et al. [8] who described an 8-electrode slow reconstruction system (reconstruction by PC) which gave images of sand/air mixtures in a cross-sectional view of a pipe. The ECT system has been developed rapidly in the late 1980's. In 1991, UMIST developed the world's first real-time ECT system [46]. It can collect measurement data from a 12 electrodes sensor at rate of 100 frames per second, and display on-line images at a rate of 40 frames per second for 20*20 pixel division. Since then, there has been continual effort to improve the performance of the system and to develop it into the industrial product.

A typical ECT system shown in Fig. 3.1 [2] consists of a capacitance sensor, a capacitance measuring unit and a computer unit to display the cross-sectional image of

the content. The functions of the capacitance measuring unit include selection of electrode-pair combinations, measurement of capacitance between all possible combination pairs of the electrode and conversion of measured capacitance values into electronic signals.

Fig. 3.1 A typical electrical capacitive unit

A typical ECT pipeline sensor [6] consists of a set of measurement electrodes mounted symmetrically around the circumference of the insulating pipe as shown in Fig. 3.2. The electrical capacitances between all combinations of the electrodes with each set are measured. This information is then processed by a software algorithm, used to construct the image of the contents of the cross section of the vessel enclosed by the sensor, based on variations in the permittivity of the material inside the vessel.

Fig. 3.2 Cross sectional view of typical ECT sensor with 12 electrodes

The capacitance electrode can be mounted either inside or outside the vessel. If the vessel wall is an electrical insulator such as plastic, the electrodes are normally mounted on the outside surface of the pipe or vessel, and earth screen, which surrounds the measurement electrodes, minimizes external electrical noise. Radial earthed screen is fitted between the electrodes to reduce the inter-electrode capacitance external to the sensor pipe, particularly the standing capacitance between adjacent electrode pairs. For a sensor with N electrodes, there are $N(N-1)/2$ single-electrode pairs and hence $N(N-1)/2$ independent capacitance measurement [6].

The inter-electrode capacitance of an ECT sensor depends mainly on the electrode size. For a given number of electrodes, the capacitance is proportional to the axial length of electrodes. To obtain wide-spatial-bandwidth signals, short electrodes are preferable. However, short electrodes result in small capacitance value. For a 12 electrode system, typically, the length of electrodes is selected as 10 cm, and the stand capacitance values are small, ranging from 0.01pF to 2 pF [2].

In an ECT sensor, three sources determine the stray capacitance [6]:

- i) The capacitance between the measurement electrode and the earthed screen
- ii) The capacitance of the shielding cable connecting the electrode to a capacitance measuring circuit
- iii) The input capacitance of the CMOS switches in the capacitance measuring circuit.

The typical stray capacitance is around 150 pF. So it is very important for the sensor system to be stray-immune. In addition, it should also have high signal-to-noise ratio (SNR), low drift and wide bandwidth to enable a high data-sampling rate.

3.2 Review of Tomography Sensing Interfaces

To measure fine detail such as a small gas bubble inside an oil pipe as an example, the ECT sensing interface should display adequate resolution for detection of minute capacitance change whilst maintaining very stable performance against the time and temperature [9]. Consequently, the basic requirements [2] for a quality ECT transducer are summarized as below:

- i. Low baseline drift against time and temperature [32]
- ii. Stray immune [41]
- iii. High sensitivity and precision
- iv. Fast data capture rate.

Among many different capacitance measuring circuits, the charge/discharge circuit [2] and the AC-based circuit [4]-[5] are the most suitable for use in ECT systems because of their stray-immunity.

Previous works [2]-[3] on ECT is using the charging and discharging circuit [2] to build the ECT interfaces circuit as shown in Fig. 3.3. One electrode of the measured capacitance C_x (excitation electrode) is connected with a pair of CMOS switches, S1 and S2, and another (detection electrode) is connected with switches S3 and S4. A cycle of operation consists of a charge phase and a discharge phase, acting on the measured capacitance C_x . A pseudo-differential QV converter, which incorporates the filter function, is formed by two operational amplifiers (op-amps) OP1, OP2. In a first half of the cycle, the switches S1 and S3 are closed first to charge C_x to voltage V_{ref} , and the charging current flows into the input of the capacitance detector CD1 and generates a negative voltage output at V_{out1} . In the second half of the cycle, switches S2 and S4 close to discharge C_x to earth potential. The discharge current flows out of the current detector CD2 and produces a positive voltage output at V_{out2} . Here C_{f1} and C_{f2} are identical and serve as the filter element with respective resistor R_{f1} and R_{f2} . C_{in1} and C_{in2} represent the parasitic capacitances arising from the tomography setup. They have no significant effect on capacitance measurement because the inverting input of OP1 and OP2 are always kept

at virtual ground voltage. Assume the typical charge/discharge cycle repeats at frequency f and $R_{f1} = R_{f2} = R_f$, the two output voltages can be

$$V_{out1} = -fV_{ref}R_fC_x + \varepsilon_1 \quad (3.1)$$

$$V_{out2} = fV_{ref}R_fC_x + \varepsilon_2 \quad (3.2)$$

The differential output voltage $V_{out2} - V_{out1}$ is taken as the output signal of the basic circuit, from (3.1) and (3.2). This gives

$$V_{out2} - V_{out1} = 2fV_{ref}R_fC_x + \varepsilon_2 - \varepsilon_1 \quad (3.3)$$

From the above equations, it can be easily found that the output voltage of the circuit is proportional with the switching frequency f , feedback resistor R_f , reference voltage V_{ref} and detectable capacitor C_x . Here, ε_1 and ε_2 are the output offset voltages of CD1 and CD2, caused mainly by the charge injection effect of the CMOS switches and the offset effect of operational amplifiers. The charge injection comes from the critical switches S3 and S4. Despite the pseudo-differential structure can suppress the charge injection, in the presence of mismatch effect in discrete switches, they can be significant because of high supply (+/-15V) being used in the system.

In UMIST ECT sensor on the basis of charging and discharging circuit, discrete components are used. V_{ref} is regarded as a low impedance reference and considered to have 1% accuracy from commercial voltage reference component. R_f has the accuracy of 1% using discrete component and C_f does not have accuracy requirement because it serves as a filter element.

Since the excitation electrode is always connected with low impedance supplies, and the detecting electrode is always at virtual earth potential, so stray capacitances have

virtually no effect on the measurement. The charge/discharge circuit is a successful approach in terms of resolution, linear response and data capture rate (100 frames per second).

Fig. 3.3 The charge/discharge capacitance measuring circuit

Another approach, the ac-based capacitance measuring circuit [4], as depicted in Fig. 3.4, can avoid the charge injection problem without using MOS switches. In this circuit, the $OP1$ and $OP2$ in the front-end circuit are configured non-inverting amplifiers to form a pseudo-differential structure. The left-side electrode (the negative input of $OP2$) is used as an excitation electrode. An amplitude-controllable sine-wave voltage source V_i is applied to its non-inverting input. The inverting input of $OP2$ is kept at the same potential

and hence the left-side electrode is excited by the sine wave V_i . The right-side electrode is used as a detection electrode. Assume $R_{f1} = R_{f2} = R_f$ and $C_{f1} = C_{f2} = C_f$, the output voltage of OP2 is

$$V_{out1} = j\omega C_x R_f V_i / (j\omega C_f R_f + 1) \quad (3.4)$$

when the capacitance C_f is small such that $\omega C_f R_f \ll 1$, (3.4) can be simplified as

$$V_{out1} = -j\omega C_x R_f V_i \quad (3.5)$$

Obviously, the output of the front-end circuit is linear with the measured capacitance C_x . The sensitivity is proportional to the frequency and amplitude of the excitation voltage and the feedback resistance R_f .

Fig. 3.4 The ac-based capacitance measuring circuit

Like the charge/discharge circuit, this circuit is also stray-immune. Since the inverting input of the left side op-amp is kept at the excitation voltage, C_{p1} is driven by the voltage source provided the op-amp operates in feedback mode properly and the equivalent

output impedance from the inverting input point is small. Therefore, C_{p1} would not affect the capacitance measurement. Since the inverting input of the right side op-amp is always kept at virtual earth, the potential across C_{p2} is zero. Therefore, C_{p2} also has no effect on the capacitance measurement.

Fig. 3.5 [4] shows a complete measurement channel, including the front-end circuit, an AC amplifier, a rectifier and a Butterworth low-pass filter. The AC signal from the front-end circuit is further amplified 10 times and then rectified into a DC signal plus AC harmonics [4]. The harmonics is rejected by the low-pass filter and the resultant DC signal represents the capacitance measurement.

Fig. 3.5 Complete ac-based capacitance measurement channel for one electrode which can be set as excitation or detection

The comparison between the charge/discharge capacitance measuring circuit and the ac-based capacitance measurement circuit is shown in Table 3.1 below:

Table 3.1 The comparison between charge/discharge ECT circuit and ac-based ECT circuit

	Data capture rate	Excitation voltage	Equivalent charge injection capacitance	Op-amp unity gain bandwidth	Op-amp slew rate
Charge/Discharge ECT [2]	> 100 frames per second	dc	0.05 pF	4 MHz	2.4 V/ μ S
Ac-based ECT circuit [4]	>1000 frames per second	ac	nil	150 MHz	300V/ μ S

3.3 Limitations of the Previous ECT Systems

The main limitations of the charge/discharge capacitance measuring circuit and AC based capacitance measuring circuit in UMIST ECT systems [2] have been observed. The shortcomings of the charge/discharge approach are given as follows:

- a) Effect of heavy parasitic capacitors: For given design values on feedback resistor and reference voltage, the sensitivity of the circuit depends on the switching frequency, which will be limited by the op-amp bandwidth and the stray capacitors C_{p1} and C_{p2} (150 pF). Despite employment of wide bandwidth op-amps, two large external capacitors C_{in1} , C_{in2} are also needed to ensure the virtual ground potential remain stable during the high-speed charge transfer operation.

- b) Large baseline drift: Although the pseudo-differential structure reduces the output offset voltage caused by the charge injection and clock feedthrough effects, the discrete implementation still exists about 20% to 30% of the remaining effect that appears as residual dc offset (equivalent of typical 0.03 pF for static C_x). This is accounted for the mismatch of discrete feedback components, large supply operation (+/- 15V) that increases the residual dc arising from charge injection and clock feedthrough through mismatch of MOS switches [13], and potential dc offsets of the op-amps. As a result, it requires very frequent calibration to compensate the intrinsic large base-line drift against the time and temperature.

The shortcomings of AC based ECT are as follows:

- a) Resolution limitation: In AC based ECT system, there is nonlinear element arising from the rectifier in the back-end signal-processing block. The nonlinear effect would jeopardize the system performance of the ECT transducer, limiting the resolution at the level of 10 fF [4].
- b) Sensitivity limitation: The circuit sensitivity of the AC based ECT is directly proportional to the frequency and amplitude of the excitation signal. It is necessary to employ a very high excitation frequency for a high imaging rate, like 1000 frames/second [42]. However, the frequency of the applied excitation signal is limited by the gain bandwidth (150MHz in UMIST ECT example) and slew rate (SR) of op-amp. The output of the op-amp is given by

$$V_{out} = V_p * A_{cl} * \sin \omega t \quad (3.6)$$

$$SR = \left(\frac{dV_{out}}{dt} \right) \Big|_{\max} = V_p * A_{cl} * 2\pi f_{\max} \quad (3.7)$$

From (3.7), if $SR = 300V/\mu s$, $V_p = 15V$, $A_{cl} = 1$, we get

$$f_{\max} = 314kHz \quad (3.8)$$

Although it can support high frame rates, it increases the power consumption substantially in the system design because of employment of high bandwidth high slew rate op-amp. However, the amplitude of the excitation signal is limited by the op-amp supply because the modern CMOS process technologies support typical 5V supply or below. Hence, the sensitivity of the AC based ECT can hardly be high with respect to the objective for an integrated solution.

CHAPTER 4

Architecture Design

4.1 The Proposed Capacitance Measuring System

An improved capacitance measuring system is proposed and presented, as depicted in Fig. 4.1, includes: (i) the front-end sensor interface circuit (ii) the chopper amplifier gain stage and (iii) the third-order continuous-time low-pass filter.

The front-end circuit incorporates the CDS technique to cancel the dc offset and the $1/f$ noise. The differential outputs of front-end circuit are coupled to the second stage with gain of 24. Chopper operational amplifier is used here to remove the dc offset and $1/f$ noise in the second stage so that they will not be amplified by the gain significantly. The third-order low-pass filter is designed with a 5 kHz cut-off frequency to reject the clock noise and high-frequency noise.

In this system, there are two non-overlapping clock generators [10]. One of them is the master clock generator with input clock frequency of 500 kHz, which is used to drive the switched-capacitor circuit implemented in the front-end interface circuit. The other non-overlapping secondary clock of 25 kHz is used as the chopper clock generator. This is used to drive the input and output chopper of the differential amplifier in the second stage. Each chopper consists of 4 cross-coupled NMOS transistors.

Fig. 4.1 Overall system block diagram

4.2 The Novelty and Advantages of the Proposed System Architecture

With incorporating CDS technique in the front-end stage and CHS technique in the second gain stage for complete system gain, the proposed switched-capacitor ECT system is able to minimize the dc offset, $1/f$ noise and temperature drift, leading to intrinsic low baseline drift characteristic. Contrasting to the bipolar supplies used in the previous works, by means of level shifting the analog ground to 1V, the circuit can be integrated in typical CMOS process and operate at a single 5V supply because the on resistance of MOS switches can be made sufficient small (at $V_{gs}=4V$, NMOS on resistor is 100 Ohm with $L=0.6\mu m$ $W=100\mu m$). Since the resettable topology is applied in the system to facilitate high speed charging and discharging operation under heavy stray capacitance of 150 pF. It can be shown later that more than 400 frames per second in data sampling rate

can be achieved in the proposed ECT system, which gives obvious improvement when compared with 100 frames per second in prior-art charge/discharge ECT design. It will also be demonstrated that the sensitivity of 1.5V/pF and the resolution of minimum 1fF are attainable under robust environment. The overall performance will be sufficient for the application and comparable with the prior-art works [2]-[3].

Before embarking on the circuit design, both the system specifications and basic blocks specifications are defined first. The basic blocks include front end circuit, chopper op-amp and 3rd order low pass filter. Table 4.1 shows the requirements for the proposed capacitive tomography sensing system, while Table 4.2, Table 4.3 and Table 4.4 are the target specifications for the three basic blocks.

Table 4.1 System specification of proposed ECT sensor

Supply voltage	5V
Cx detectable range	1 fF~ 2 pF
Stray capacitor	150 pF
Data capture rate	> 100 frames per second
Fully integration	Yes

Table 4.2 The front-end circuit specifications

Specification	Front end circuit
Switching frequency	250kHz
Bandwidth of op-amp	> 40MHz
Gain of op-amp	80dB
Current consumption of op-amp	< 3mA
Virtual ground	1V
Maximum output voltage at full scale	0.125V
Settling time (with 0.01% accuracy)	<1 μ S
Feedback capacitor	< 10pF
Slew rate	>200V/ μ S

Table 4.3 The chopper operational amplifier specifications (chopper is disabled)

Specification	Chopper op-amp
Gain	> 80 dB
Unity gain bandwidth	< 20 MHz
Chopper frequency	25kHz
CMRR (common mode rejection ration)	> 80dB

Table 4.4 The 3rd order low pass filter specifications

Specification	3 rd order low pass filter
Cut off frequency	5kHz
Power consumption	< 1mW
Integrated noise at 5kHz bandwidth	< 200 μ V

CHAPTER 5

Circuit Design

As previously described, the sensor system includes the front-end circuit, the chopper-stabilized difference amplifier and the third-order low-pass filter. This section is concerned with the choice of appropriate circuit topology that leads to the system implementation together with the description of the circuit operation.

5.1 Proposed Sensor Interface

5.1.1 Basic structure of proposed sensor interface without CDS

The basic structure of switched-capacitor front-end interface (without CDS) is shown in Fig 5.1 [9]. The typical operation of each capacitance detector will be separated into two phases: charge transfer phase and reset phase. The phases in CD1 and CD2 are complementary. Assume S1, S3, S6 are closed first, the detected capacitor C_x is charged to the reference voltage V_{ref} . The charging current flows through the feedback capacitor C_{f1} in CD1 and generates a negative voltage V_{out1} . In the mean time, the V_{out2} of the CD2 is reset to virtual ground by connecting the output to the negative input of the op-amp in the form of a voltage follower. In the next phase, when S2, S4 and S5 are closed, the detected capacitor C_x is discharged to earth potential. The discharging current flows

out of feedback capacitor C_{f2} in CD2 and it causes a positive voltage V_{out2} , whereas the V_{out1} of the CD1 is reset to virtual ground by closing S5.

Fig. 5.1 Proposed front-end capacitance measuring circuit without CDS

In order to simplify the analysis, the mismatch of C_{f1} and C_{f2} can be ignored in the basic front-end ECT circuit without CDS. Assume $C_{f1} = C_{f2} = C_f$, analog ground $V_Q = 1V$, the two output voltages (V_{out1}, V_{out2}) during charge transfer phase can be defined as

$$V_{out1} = -(C_x / C_f) V_{ref} + V_Q + \varepsilon_1 \quad (5.1)$$

$$V_{out2} = (C_x / C_f) V_{ref} + V_Q + \varepsilon_2 \quad (5.2)$$

where ε_1 and ε_2 are the charge injection error combined with op-amp offset terms arising from respective CD1 and CD2. Assume the S_3 and S_4 have similar charge injection effects and the two op-amps in CD1 and CD2 have matched offset voltages, ε_1 and ε_2 are close to each other and can be reduced via differential operation. According to (5.1) and (5.2), the outputs of the front-end circuit are linear with the capacitor C_x . The circuit sensitivity is inversely proportional to the feedback capacitor C_f and directly proportional to the amplitude of the reference voltage V_{ref} . Small feedback capacitor (5pF to 10pF) and large value of reference voltage ($\geq 1V$) can achieve a high sensitivity of the circuit. Besides, the equations also indicate that the gain is independent of the clock frequency. Finally, the choice of the clock frequency is limited by the op-amp bandwidth, stray capacitor and feedback capacitor.

The two output voltages (V_{out1}, V_{out2}) will be forced to the analog ground during the reset phase. Due to the low-impedance drive of the unity gain topology at this phase, the parasitic capacitances can be either charged or discharged quickly to the defined biasing point. Hence, no external capacitors C_{in1} and C_{in2} are needed with respect to the prior-art circuit [2]–[6].

The proposed ECT circuit in Fig. 5.2 is stray-immune. The parasitic capacitances C_{p1} and C_{p2} arise mainly from three sources [6]: the capacitance between the measurement electrode and earth screen; the capacitance of the shielding cable connecting the electrode to a capacitance measuring circuit; the input capacitance of a MOS switch on the capacitance measuring circuit. Since the op-amp has sufficient high gain to maintain the

inverting input at artificial analog ground, the parasitic capacitances C_{p1} and C_{p2} will not affect the accuracy of the capacitance measurement. On the other hand, the effective gain bandwidth of the op-amp will be reduced by the ratio of the stray capacitance to the feedback capacitance. Hence, an op-amp with unity gain bandwidth of 43 MHz is designed in order to allow fast response under heavy stray capacitances. A capacitor of 150 pF is assumed for the stray capacitance, which is a typical value in ECT sensor.

5.1.2 Proposed sensor interface with CDS

The basic structure in previous section can eliminate the charge injection caused by the charge/discharge of the switches. But it cannot remove the dc offset and 1/f noise from the CMOS operational amplifier.

A front-end circuit designed for ECT measurement system is presented in Fig. 5.2(a). It is based on switched-capacitor front-end interface which employs the correlated double-sampling (CDS) technique [7] – [10] to reduce the dc offset and 1/f noise of the CMOS amplifiers. The front-end circuit with CDS technique consists of two capacitance detectors: CD1 (Capacitance Detector 1) and CD2 (Capacitance Detector 2). They are arranged in a pseudo-differential circuit architecture. Each capacitance detector comprises one high-speed op-amp, with its non-inverting input tied to the virtual ground V_Q and its inverting terminal tied to a CDS switched-capacitor network. For measuring C_x , the source electrode is connected with three MOS switches S1, S2 and SGND whereas the detecting electrode is connected with the switches SN1 and SN2.

Fig. 5.2(b) shows the waveforms for switch control signals. Derived from the non-overlapping biphasic clock signals ϕ_1 and ϕ_2 , the front-end sensor consists of four

operation phases. They are: reset phase, auto-zero phase, charge transfer phase and hold phase. In association with the switch control signals S4 – S9 obtained directly from ϕ_1 and ϕ_2 , multiple switch control clock signals S1, S2, SGND, SN1 and SN2 are derived by the clock generator. These signals configure the circuit at each operation phase, as illustrated in Fig. 5.3(a), Fig. 5.3(b), Fig. 5.3(c) and Fig. 5.3(d), respectively.

For the functional analysis, it is assumed that the op-amps have infinite gain but having finite offsets to demonstrate the CDS function. According to the circuit topologies, the effective voltage references applied to the source electrode are defined as $V_{ref1} = \Delta V_{ref} + V_Q$ and $V_{ref2} = V_Q - \Delta V_{ref}$, where ΔV_{ref} is defined as the incremental bias voltage with respect to analog ground reference V_Q .

Fig. 5.2(a) Front-end ECT transducer with CDS

Fig. 5.2(b) The switch control signals for the CDS transducer

Fig. 5.3(a) Simplified circuit during T1

Fig. 5.3(b) Simplified circuit during T2

Fig. 5.3(c) Simplified circuit during T3

Fig. 5.3(d) Simplified circuit during T4

The basic function of the proposed ECT circuit with CDS can be separated into 4 operation phases: Reset phase (CD1), Auto-zero phase (CD1), Charge transfer phase (CD1) and Hold phase (CD1). According to the circuit topologies, the effective voltage references applied to the source electrode are defined as $V_{ref2} = V_Q - \Delta V_{ref}$ and $V_{ref1} = \Delta V_{ref} + V_Q$, where ΔV_{ref} is defined as the incremental bias voltage with respect to analog ground reference V_Q .

Phase T1:

Phase 1 is reset phase in CD1, and charge transfer phase in CD2. During T1 as shown in Fig. 5.3(a), the switches S1, S6, SN1, SGND, S7 and S8 are off, while the switches S2, S4, S5, SN2 and S9 are on. The CD1 is working in reset phase whereas the CD2 is working in charge transfer phase. In reset phase, the OP1 is configured as a unity-gain amplifier. Hence the V_{out1} becomes

$$V_{out1} = V_Q + V_{os1} \quad (5.3)$$

Since the dc offset of the OP2 was stored by the feedback capacitor C_{f2} in its previous T4 phase (auto-zero phase), the effect of offset V_{os2} is cancelled during its charge transfer phase at T1:

$$V_{out2} = V_Q + (C_x / C_{f2}) \Delta V_{ref} \quad (5.4)$$

Phase T2:

Phase 2 is auto-zero phase in CD1 and hold phase in CD2. During T2, as shown in Fig. 5.3(b), the switches S4, S5, SN1, SGND and S9 are on, while the S1, S2, S6, SN2, S7

and S8 are off. The CD1 is working in auto-zero phase and the CD2 is working in hold phase. The outputs of CD1 and CD2 remain the same as described by (5.3) and (5.4).

Phase T3:

Phase 3 is charge transfer phase in CD1 and reset phase in CD2. During T3 as shown in Fig. 5.3(c), the switches S1, S6, SN1, S7 and S8 are on, while S2, S4, S5, SGND, SN2 and S9 are off. The CD1 is now working in charge transfer phase but the CD2 is working in reset phase. Since the CD1 circuit has already stored the input offset during previous T2 phase, when the output is sampled in phase T3, the input offset voltage of the OP1 can be canceled. This gives

$$V_{out1} = V_Q - (C_x / C_{f1}) \Delta V_{ref} \quad (5.5)$$

Simultaneously, the output of CD2 in reset mode at T₃ is

$$V_{out2} = V_Q + V_{os2} \quad (5.6)$$

Phase T4:

Phase 4 is hold phase in CD1 and auto-zero phase in CD2. During T4 as shown in Fig. 5.3(d), the switches S6, SGND, SN2, S7 and S8 are on, while the S1, S2, S4, S5, SN1 and S9 are off. The CD1 is working in hold phase whereas the CD2 is working in auto-zero phase. Similar to the operation in T2, the outputs of CD1 and CD2 remain the same values as those of T3. They are still governed by (5.5) and (5.6).

Table 5.1 has summarized the status of CD1, CD2 and all switches in the four phases. It is given as follows:

Table 5.1 The status of CD1, CD2 and all switches in the four phases

	S1	S2	SGND	SN1	SN2	S4	S5	S6	S7	S8	S9	CD1	CD2
T1	off	on	off	off	on	on	on	off	off	off	on	Reset	Charge transfer
T2	off	off	on	on	off	on	on	off	off	off	on	Auto-zero	Hold
T3	on	off	off	on	off	off	off	on	on	on	off	Charge transfer	Reset
T4	off	on	on	off	off	off	off	on	on	on	off	Hold	Auto-zero

The SC CDS ECT circuit in Fig. 5.2(a) is also stray-immune. The C_{p1} is driven by the voltage sources and it would not affect the capacitance measurement. Since the inverting input of OP1 and OP2 are always kept at virtual earth, Therefore, C_{p2} also has no effect on the capacitance measurement. The use of auto-zero phase in this scheme ensures that the analog ground can be fast settled and remain stable because the buffer structure has lower impedance to force the analog ground when compared with the prior-art counterpart in Fig. 3.3. This gives the benefit for elimination of capacitors C_{in1} and C_{in2} , thus saving significant number of external capacitors in a multi-electrode ECT system on the basis of Fig. 5.1. By level shifting the analog ground to 1V, the circuit can operate at a single supply voltage whilst yet the turn-on resistance of the switches can be made sufficient small for a 5V chip design when compared with a +/-15V design in the prior-art circuits. From (5.4) and (5.5), the sensitivity of the SC CDS ECT front-end circuit is independent of switching frequency, thus gaining another extra advantage for relaxing the accuracy and drift requirements of the clock.

5.2 The Chopper Amplifier Gain Stage

The signal with maximum amplitude 125mV with detectable capacitance 2pF is not large enough at the output of interface stage. Thereby, it needs a second gain stage to amplify the signal to a sufficient value with maximum voltage change 3V. For offset cancellation, good linearity and dynamic range consideration, the chopper stabilization amplifier [15], [17] is adopted. Accurate gain can be achieved since the closed-loop gain is determined by resistor ratio, which can be set quite precisely in an integrated circuit. To minimize errors due to finite offset voltage and $1/f$ noise, chopper stabilization (CHS) technique is used. The CHS technique has already been discussed in detail in Chapter 2. The schematic for the chopper amplifier gain stage is shown in Fig. 5.4.

Fig. 5.4 Chopper amplifier gain stage

The differential-to-single-ended amplifier is set to have gain of 24 by resistor R_1 , R_2 , R_3 and R_4 . If $R_1 = R_3 = 25k$, $R_2 = R_4 = 600k$, we can get:

$$Gain = R_2 / R_1 = 24 \quad (5.7)$$

The chopper action is driven by a clock frequency which must be higher than the $1/f$ noise frequency of the conventional CMOS op-amp. During chopping, the $1/f$ noise is translated to the odd harmonic of the chopping frequency. Therefore it is important that this odd harmonic of the chopping frequency does not interfere with the main clock frequency component. Based on this consideration, a chopping frequency of 25 kHz is chosen together with a 500 kHz main clock.

5.3 Continuous - Time Filter

The main limitation on the data acquisition speed of an ECT system comes from the cut-off frequency of the low-pass filter. For 500 kHz excitation and 5 kHz cut-off frequency, the transient time of the capacitance measuring circuit is within 200 μ s. Since the electrodes are energized sequentially, the total time taken by the capacitance measuring circuits is $N \times 200\mu$ s, where N is the number of electrodes. For a 12 electrodes system, the total settling time for one frame measurement is about $12 \times 200\mu$ s, so it is very easy for the system to achieve more than 400 frames/second data acquisition speed.

In the proposed ECT system, there are high frequency components in the sample-data signal and the chopper, the continuous-time filter is needed to attenuate those high frequency noise and spikes. This low-pass filter (LPF) [31],[33] is used as the continuous-time filter in the sensor interface design and passes frequency from DC to a

specified cutoff frequency f_0 , whereas high frequencies are attenuated. There are two types of analog filter, namely passive filter and active filter. One example for a RC passive filter [53] is shown below:

Fig. 5.5 RC low-pass filter

The transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + sRC} \quad (5.8)$$

and the cut-off frequency is

$$f_0 = \frac{1}{2\pi RC} \quad (5.9)$$

For active filter design, the typical Sallen-Key filter network [30],[36], as shown in Fig. 5.6, has been widely used in practice. The choice of the Sallen-Key filter structure is due to its simplicity, low power consumption, low offset contribution and good linearity. Despite of limited common-mode range, it is acceptable for internal stage design.

Fig. 5.6 Sallen-Key low-pass filter

Using nodal analysis, we get

$$\left(\frac{1}{R_1} + \frac{1}{R_2} + sC_1 \right) V_1 - \frac{V_{in}}{R_{in}} - V_{out} \cdot sC_2 - \frac{V_2}{R_2} = 0 \quad (5.10)$$

$$\left(\frac{1}{R_2} + sC_2 + sC_1 \right) V_2 - \frac{V_1}{R_2} = 0 \quad (5.11)$$

$$V_{out} = V_2 \quad (5.12)$$

Solving the above equations, the transfer function is obtained as

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_1 C_1 R_2 C_2}}{S^2 + \left(\frac{1}{R_2 C_2} + \frac{R_1 + R_2}{R_1 R_2 C_1} \right) S + \frac{1}{R_1 R_2 C_1 C_2}} = \frac{\omega_0^2}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} \quad (5.13)$$

where

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

and

$$Q = \frac{1}{\left(1 + \frac{R_2}{R_1}\right) \sqrt{\frac{R_1 C_2}{R_2 C_1}}}$$

In this project, the third-order low-pass filter is realized by combining the first-order passive RC filter and the second-order Sallen-Key filter. The circuit is shown in Fig. 5.7.

Fig. 5.7 The third-order low-pass filter

The transfer function of the circuit is

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R_1 R_2 R_3 s^3 + (2R_1 R_3 + R_1 R_2 + R_2 R_3) s^2 + (R_1 + R_2 + 2R_3) s + 1} \quad (5.14)$$

In this design, the distributive RC effect in high-order Sallen-Key filter also helps the reduction of the values for R and C components. Taken into account of over-design to overcome the process variations, the nominal cut-off frequency is set at 5 kHz.

5.4 House Keeping Circuits

In order to meet the high sensitivity requirement, sensor circuits should exhibit low noise, low offset and maintain good power supply rejection ratio. In this section, critical design

considerations for basic blocks such as high performance amplifiers and reference current generator are discussed in details. This is then followed by the description of the digital circuitries.

5.4.1 High-speed op-amp for front-end transducer

From the proposed front-end circuit, the stray capacitors C_{p1} and C_{p2} are of little effect on accuracy of the capacitance measurement, provided that the op-amp has sufficient high gain to maintain analog ground at the input. On the other hand, the effective gain bandwidth of the op-amp will be reduced by the ratio of the stray capacitance to the feedback capacitance. Hence, a dedicated high-speed op-amp with 43MHz bandwidth is designed so as allow fast response under heavy stray capacitances. A capacitor of 150 pF is assumed for the stray capacitance, which is a typical value in ECT sensor.

A schematic [9] of the high-speed op-amp is shown in Fig. 5.8(a). For simplicity, the biasing network is not shown. It consists of a folded cascode gain stage followed by an inverting class-A output stage. The use of folded cascode results in high output impedance in the first stage, thereby maximizing the dc gain of the op-amp. Through RC Miller compensation [10][45], this structure can attain 43 MHz unity gain bandwidth with dc gain of 80 dB using the AMS 0.6 μm CMOS technology. The current consumption for this op-amp is 2 mA.

The capacitor C_c , realizes what is commonly called Miller compensation. It controls the dominant first pole ω_{p1} , and therefore the gain bandwidth is ω_{ta} based on $\omega_{ta} = A_0 \omega_{p1}$.

A simplified small-signal model for the op-amp is shown in Fig. 5.8(b). Here, R_1 is the output impedance of the first stage, C_1 is the parasitic capacitance which includes C_{db4} , C_{db6} and C_{gs5} . R_2 is the output impedance of the second stage, C_2 is the output load capacitance. This circuit can be inspected with nodal equations [10]:

$$g_{m1}V_{in} + \frac{V_1}{R_1} + sC_1V_1 + \left(\frac{sC_c}{1 + sC_cR_c} \right)(V_1 - V_{out}) = 0 \quad (5.15)$$

$$g_{m5}V_1 + \frac{V_{out}}{R_2} + \left(\frac{sC_c}{1 + sC_cR_c} \right)(V_{out} - V_1) = 0 \quad (5.16)$$

These equations can be solved to give

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a\{1 - s[(C_c / g_{m5}) - R_cC_c]\}}{1 + bs + cs^2 + ds^3} \quad (5.17)$$

where

$$a = g_{m1}g_{m5}R_1R_2$$

$$b = (C_2 + C_c)R_2 + (C_1 + C_c)R_1 + g_{m5}R_1R_2C_c + R_cC_c$$

$$c = R_1R_2(C_1C_2 + C_cC_1 + C_cC_2) + R_cC_c(R_1C_1 + R_2C_2)$$

$$d = R_1R_2R_cC_1C_2C_c$$

If R_c is assumed to be less than R_1 or R_2 and the poles are widely spaced, then the roots of Eq (5.17) can be approximated as:

$$p_1 \cong \frac{-1}{(1 + g_{m5}R_2)R_1C_c} \cong \frac{-1}{g_{m5}R_2R_1C_c} \quad (5.18)$$

$$p_2 \cong \frac{-g_{m5}C_c}{C_1C_2 + C_cC_1 + C_cC_2} \cong \frac{-g_{m5}}{C_2} \quad (5.19)$$

$$p_3 = \frac{-1}{R_cC_1} \quad (5.20)$$

$$\text{and } z_1 = \frac{1}{C_c(1/g_{m5} - R_c)} \quad (5.21)$$

From equation above, it is easy to control the nulling resistor to shift RHP zero to the second pole for frequency compensation strategy [26].

Fig. 5.8(a) A high-speed two stage op-amp

(b)

Fig. 5.8 (b) Small-signal model for high-speed op-amp

5.4.2 Chopper-stabilized op-amp for gain stage

The second stage in the proposed ECT system is a gain stage. Since the signal coming from the first stage is not large enough (maximum 125mV), the dc offset of the second stage is very crucial because it will be boosted by the gain factor of 24 times. Chopper-stabilized technique [7] is introduced into the op-amp in order to cancel the dc offset. The chopper stabilization technique is to apply modulation to transpose the signal to a higher frequency where there is no $1/f$ noise, and then demodulates it back to the base band after amplification. It is the method of choice if the system is a continuous-time one to start with and if low baseband noise is an important requirement. The basic chopping principle has already been described in Chapter 2.

The chopper modulators are often realized with simple MOS switches, which will introduce residual offset to the system. Any spike caused by the modulator non-idealities and appearing at the amplifier input will be amplified and demodulated by the output modulator, giving rise to a residual dc component. The most important factors of the MOS switches affecting residual offset are clock feedthrough and channel charge

injection. They can be reduced by using the complementary switches so that the charges released by one switch can be absorbed by the complementary switch.

Since the time constant τ of these parasitic spikes is generally much smaller than the half chopper period $T/2$, most of the spike energy appears at frequencies higher than the chopper frequency. Using an amplifier with bandwidth twice of the chopper frequency, it can greatly reduce the offset voltage referred to the input. [7]

A schematic of the chopper op-amp is shown as Fig. 5.9 [15], [40]. It is implemented with a two-stage amplifier plus a pair of chopper switches. Each chopper switch comprises 4 cross-coupled NMOS transistors. One group of chopper switches would be inserted before the pair of differential input “in+” “in-“ of the first stage. The other group of chopper switches would be inserted between the first stage and second stage of the op-amp.

The differential signals are fed to the two inputs “INP+” “INP-“ of the first chopper. As the chopper is driven by a non-overlapping clock CLK and CLKB, at any one instant, only two of the NMOS switches would be turned on. One pair would turn on at CLK high while the other pair will be turned on at CLKB high. Due to this switching from CLK to CLKB and vice versa, the input signal is chopped. From frequency point of view, the signal is modulated and translated to the odd harmonic frequencies of the chopping square wave of 25 kHz. During this modulation, the input signal is translated to the higher frequency band leaving the noise of the op-amp unaffected at the base band. This modulated signal is then fed into the first stage of the op-amp where it is amplified.

Fig. 5.9 Chopper-stabilization op-amp

After the first stage amplification, the modulated signal is then fed to the output chopper which is implemented in the immediate stage of the op-amp. After the output chopper, the signal is fed to the final gain stage of the op-amp. The overall open-loop gain of the op-amp is about 95 dB. In the immediate stage, the low-frequency noise of the op-amp will be modulated to the higher frequency while the signal is demodulated back to base band. Hence, both the noise and signal are amplified but at different band of frequency. With the use of a low-pass filter, the signal is recovered with removal of noise.

5.4.3 Biasing Circuit Design

The biasing circuit which supplies the biasing current for op amp is given in Fig. 4.11.

The biasing circuit consists of the transistors M4-M9 and the resistor R. Since

$\left(\frac{W_4}{L_4}\right) = \left(\frac{W_5}{L_5}\right)$, the current-mirror pair M4 and M5 forces I_{m8} to be equal to I_{m9} . Thus

$$V_{gs9} = V_{gs8} + I_8 * R \quad (5.22)$$

Assume the threshold voltages are identical for transistor M8 and M9, we get

$$\sqrt{\frac{2I_{d9}}{\mu_n C_{ox} \left(\frac{W_9}{L_9}\right)}} = \sqrt{\frac{2I_{d8}}{\mu_n C_{ox} \left(\frac{W_8}{L_8}\right)}} + I_{d8} * R \quad (5.23)$$

For $I_{d8}=I_{d9}$, equation(4.22) can be rewritten as

$$\sqrt{\frac{2I_{d9}}{\mu_n C_{ox} \left(\frac{W_9}{L_9}\right)}} = \sqrt{\frac{2I_{d8}}{\mu_n C_{ox} \left(\frac{W_8}{L_8}\right)}} + I_{d9} * R \quad (5.24)$$

Therefore, the design equation for the resistor R is

$$R = \frac{2}{\sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_9 I_9}} \left(1 - \sqrt{\frac{\left(\frac{W}{L}\right)_9}{\left(\frac{W}{L}\right)_8}} \right) \quad (5.25)$$

Since $g_{m9} = \sqrt{2\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_9 I_{d9}}$, the design equation for g_{m9} can be expressed as

$$g_{m9} = \frac{2 \cdot \left(1 - \sqrt{\frac{\left(\frac{W}{L}\right)_9}{\left(\frac{W}{L}\right)_8}} \right)}{R} \quad (5.26)$$

It can be seen that the geometric ratio and the value of the resistor R determine the transconductance of M9 to a first-order approximation, which is independent of the variations in supply voltage, temperature and process parameters. Since the currents passing through the transistors are derived from the same bias network, all transconductances are also stabilized. The ratios of the currents are mainly dependent on geometry. The ac transconductance parameters for respective transistors are proportional to the transconductance g_{m9} .

$$g_{mi} = \sqrt{\frac{\left(\frac{W}{L}\right)_i \cdot I_{di}}{\left(\frac{W}{L}\right)_9 \cdot I_{d9}}} \cdot g_{m9} \quad (5.27)$$

Fig. 5.10 The biasing circuit with startup circuit

The start-up circuit consists of transistors M1- M3. In the event that all currents in the bias loop are zero, M2 is off. M1 operates as an active resistive load that is always on. The gate of M3 will be pulled high. This transistor M3 will draw current into the bias loop, hence starting up the circuit. Once the loop has been started up, M2 will be on and sink all the current from M1, pulling the gate of M3 low. As a result, M3 turns off and the startup loop is isolated.

5.4.4 Biphasic Non-Overlapping Clock

A simple digital block [38] is designed to generate all these switch control signals properly. The block includes: biphasic non-overlapping clock, clock divider and some delay cells. Here, clock divider uses only one D flip-flop to generate a clock signal with half frequency of the master clock. Delay cells consist of resistor and capacitor to get the proper delay time.

The most important circuit in the logic block is the biphasic non-overlapping clock. It generates Φ_1 (S4, S5, S9) and Φ_2 (S6, S7, S8) for the front-end transducer. The simple schematic of the non-overlapping biphasic clock circuitry is shown in Fig. 5.11 [39]. Non-overlapping biphasic clock signals mean that both the output would not have a logic of “1” at the same time. This is essential for the proper operation of the switched-capacitor circuits, as they would isolate two operating phases. The Fig. 5.12 shows the definition of the non-overlapping two-phased clock signals. The non-overlapping biphasic clock circuitry basically consists of a SR latch but with additional inverters placed along the feedback path. The feedback path is used to ensure that the logic of the two outputs is always complementary to each other. The inverter along the feedback path is used to add delay around 2.4 nS such that the two-phased clock signals would not overlap each other. In addition, buffers had been added to the outputs in order to enhance the driving capability of this circuitry.

Fig. 5.11 Schematic of non-overlapping biphasic clock circuit

Fig. 5.12 Non-overlapping biphasic clock signals

5.4.5 Gain-Enhanced VI Converter

The gain-enhanced VI converter is used in the system to generate an accurate current source for fast-speed operational amplifier in front-end stage. As shown in Fig 5.13, the output of the operational amplifier drives the PMOS transistor with the resistors R_{int} and $1/g_{mp2}$. The reference input is applied at the negative input of the op-amp and the feedback is obtained from the transistor network with gain feature, contrasting to the follower-like structure in conventional technique [37]-[38]. This transistor network is an inverting amplifier (MP1 and R_{int}) incorporating the source-degeneration resistance of $1/g_{mp2}$ by a diode-connected transistor as part of a current mirror. The simplified small-signal analysis shows that

$$V_o = \frac{A_1 \left(\frac{g_{mp1} R_{int}}{1 + g_{mp1} / g_{mp2}} \right) V_{REF}}{1 + A_1 \left(\frac{g_{mp1} R_{int}}{1 + g_{mp1} / g_{mp2}} \right)} \quad (5.28)$$

where A_1 is the open-loop gain of the op-amp. The effective loop gain is boosted by the control network (MP1, R_{int} and $1/g_{mp2}$), thereby forcing V_o to be closer to V_{REF} . Thus, the reference current is

$$I_R = V_{REF} / R_{int} \quad (5.29)$$

It is interesting to note that the circuit enables higher loop gain under non-ideal effects whilst maintaining reasonable accuracy. Therefore, this leads to a relatively smaller area for the same precision in design consideration when compared with the prior works [37]-[38].

Fig. 5.13 Gain-enhanced VI converter

Chapter 6

Analysis of Front-End Tomography Transducer

6.1 Transducer Settling Error

Based on the switched-capacitor operation, the transducer should settle within acceptable error tolerance (with 0.01% error) during charge transfer phase for CD2 in T1 or CD1 in T3 with reference to Fig. 5.3(a) and Fig. 5.3(c), respectively. A high-speed op amp with wide bandwidth [22]–[24] is necessary in the front-end ECT transducer in order to have fast response when sampling the high frequency input. The schematic of the op-amp in the front-end transducer has already shown in Fig. 5.8(a). It can attain 43 MHz unity gain bandwidth with phase margin of 61° , dc gain of 80 dB and the total current consumption of 2 mA.

The small-signal settling behavior [12] of the transducer is related to the finite gain-bandwidth product of op-amps, and dictated by the parasitic non-inverting gain configuration according to the topology comprising the parasitic capacitor C_{p2} and feedback capacitors C_{f1} and C_{f2} in Fig. 5.3(a) and Fig. 5.3(c), respectively. Since the stray capacitor C_{p2} is always much larger than others in tomography application, the closed-loop parasitic gains are $A_{v1} = (C_{f1} + C_{p2})/C_{f1}$ and $A_{v2} = (C_{f2} + C_{p2})/C_{f2}$. For $C_{f1} = C_{f2} = 8$ pF and $C_{p2} = 150$ pF, $A_v = A_{v1} = A_{v2} = 19.75$. Therefore, the first-order closed-loop bandwidth is $BW = GBW / A_v = 2.177$ MHz and the amplifier time constant

becomes $\tau_d = 1/2\pi BW = 0.0731 \mu\text{S}$. If the gain circuit is assumed as a first-order system, the settling time [11] is approximated by

$$t_s(\varepsilon) \approx \tau_d \ln\left(\frac{1}{\varepsilon}\right) \approx \frac{A_v}{2\pi GBW} \ln\left(\frac{1}{\varepsilon}\right) \quad (6.1)$$

where ε is defined as the settling error. For 0.01 percent settling error and $GBW = 43$ MHz, one can obtain $\ln(1/\varepsilon) = 9.21$. The settling time can be estimated as $t_s(\varepsilon) = 0.0731 * 9.21 = 0.673 \mu\text{S}$. Since the maximum available current I_0 in the input stage of op-amp is biased at $600 \mu\text{A}$ and the Miller capacitor C_c is 0.75 pF , the slew rate is $SR = I_0/C_c = 800 \text{ V}/\mu\text{S}$. For the full-scale output voltage step of 250 mV with reference to the analog ground of 1 V in the current tomography transducer design, the slew time is 0.31 ns , which is insignificant for the overall settling time and of little concern. Hence, the total step response time for the front-end transducer is around $0.673 \mu\text{S}$, which is considered short enough for the respective output of transducer to settle within half period of $2 \mu\text{S}$ in the non-overlapping clocks, which are derived from the divider circuit having switching frequency of 250 kHz . In final remark, the settling error does not contribute any significant effect to the precision of the SC CDS ECT transducer if adequate time is allowed. The switching time of transducer is over-designed to avoid this settling time problem.

6.2 Switch Errors

Refer to Fig. 5.2(a), the critical switches that contribute significant errors are S4 and S7 in the SC CDS ECT transducer. Fig. 6.1 shows the simplified model that accounts for the switch error sources [13]. S₄ and S₇ are implemented by NMOS transistors and will be turned off when the CD₁ or CD₂ change from auto-zero phase to charge transfer phase. Each time when a switch is turned off, the charges in its conducting channel are released and moved towards the MOS source and drain terminals, causing charge injection effect. Simultaneously, the control clock voltage, transited from supply V_{dd} to V_{ss} (0 V), is coupled to nodes via C_{ov1}, C_{ov2} and the associated capacitance with reference to ground, causing clock feed through effect. Although the op-amp voltage source provides low impedance path to absorb error charges from charge injection and clock feed through, it is not the case for the high-impedance node (inverting input of op-amp) which is being connected to the parasitic hold capacitor (formed by the parasitic capacitor C_{p2}). Hence, the switch errors are of particular pronounced at this high-impedance node. In addition, dependent on the polarity of output, there will be a modulation of threshold voltage in the switch under body effect, thus part of the charge injection exhibits signal-dependent property. Further mismatch of threshold voltages and aspect ratios in the switch pair gives additional residual errors, which stem from incomplete cancellation of the charges in a non-ideal differential switch pair.

Fig. 6.1 Switching off respective NMOS switch on a op-amp voltage source model during charge transfer phase for V_{out2} at T1 and V_{out1} at T3.

Assume V_B is the bulk voltage, V_g is the gate voltage of the NMOS switches. In response to incremental C_x , V_{out2} goes high but V_{out1} goes low according to (5.4) and (5.5). Due to the decrease of V_{out1} , the source of switch transistor S4 is now defined in the output. This hints that signal-dependent charge injection will occur in S4 because the bulk-to-source voltage is no longer a constant bias. Similarly, due to the increase of V_{out2} , the source of switch transistor S7 is located at the virtual earth node. It implies that the charge injection to this node is purely a dc offset effect.

When S4 or S7 turns off in respective CD1 and CD2, the error voltages introduced by the charge injection and clock feed through effects to the virtual grounds of op-amps are

$$\Delta V_{e1} = \frac{Q_{ch1}}{2C_{p2}} - (V_{dd} - V_{ss}) \frac{C_{ov1}}{C_{ov1} + C_{p2}} \quad (6.2)$$

$$\Delta V_{e2} = \frac{Q_{ch2}}{2C_{p2}} - (V_{dd} - V_{ss}) \frac{C_{ov1}}{C_{ov1} + C_{p2}} \quad (6.3)$$

where it is assumed that half of the charge is split on each side based on fast clock transition [13],[20], and here:

$$Q_{ch1} = -W_1 L_1 C_{ox} (V_g - V_Q - \Delta V_{out1} - V_{t1})$$

$$Q_{ch2} = -W_2 L_2 C_{ox} (V_g - V_Q - V_{t2}),$$

$$V_{t1} = V_{t01} + K_1 (\sqrt{2\phi_f + V_Q - V_B + \Delta V_{out1}} - \sqrt{2\phi_f}) + K_2 (V_Q + \Delta V_{out1} - V_B),$$

$$V_{t2} = V_{t02} + K_1 (\sqrt{2\phi_f + V_Q - V_B} - \sqrt{2\phi_f}) + K_2 (V_Q - V_B)$$

In the above equations, the symbols have their usual meanings.

Consider the mismatch among aspect ratios and threshold voltages in the switch transistor pair S4 and S7 in Figure 6.1, it can be assumed that $W_1 L_1 = W_2 L_2 + \Delta(W_2 L_2)$ and $V_{t01} = V_{t02} + \Delta V_t$, where $W_2 L_2$ and V_{t02} are treated as nominal references in the switch pair. Since $C_{p2} \gg C_{ov1}, C_{ov2}$, and the terms

$$-(V_{dd} - V_{ss}) C_{ov1} / (C_{ov1} + C_{p2}) \text{ and } -(V_{dd} - V_{ss}) C_{ov2} / (C_{ov2} + C_{p2})$$

in (6.2) and (6.3) tend to zero. Although the residual clock feed through occurs under mismatch of switches, it can also be ignored because of very large parasitic hold capacitor C_{p2} . By further expanding the above bulk-modulated V_{t1} expression into approximated terms through binomial series and substituting these approximated V_{t1} terms, the mismatch assumptions and the channel charge definitions into (6.2) and (6.3) again, the switch errors dominated by charge injection are now approximated as follows:

$$\Delta V_{e1} \approx \frac{-W_1 L_1 C_{ox}}{2C_{p2}} (V_{eff1} - \Delta V_{out1} * m) = \frac{-(W_2 L_2 + \Delta W_2 L_2)}{2C_{p2}} (V_{eff1} - \Delta V_{out1} * m + \Delta V_{out1}^2 * n) \quad (6.4)$$

$$\Delta V_{e2} \approx \frac{-W_2 L_2 C_{ox}}{2C_{p2}} (V_{eff2}) = \frac{-W_2 L_2 C_{ox}}{2C_{p2}} (V_{eff1} + \Delta V_{t0}) \quad (6.5)$$

where

$$V_{eff1} = V_g - V_Q - V_{t01} - K_1 (\sqrt{2\phi_f + V_Q - V_B} - \sqrt{2\phi_f}) - K_2 (V_Q - V_B) \quad (6.6)$$

$$V_{eff2} = V_g - V_Q - V_{t02} - K_1 (\sqrt{2\phi_f + V_Q - V_B} - \sqrt{2\phi_f}) - K_2 (V_Q - V_B) \quad (6.7)$$

$$m = 1 + K_2 + \frac{K_1}{2\sqrt{2\phi_f + V_Q - V_B}} \quad (6.8)$$

$$n = \frac{\gamma}{8(2\phi_f + V_Q - V_B)^{3/2}} \quad (6.9)$$

From (6.4)-(6.9), it has shown that the induced charge injection dc offset errors to the virtual earth nodes depend on the channel area of the switch, value of parasitic hold capacitor, gate-overdrive bias and difference in threshold voltages between the two critical switches. The signal-dependent charge injection error, as described in (6.4), is a function of the incremental ac output and its squared ac output. Note that the parameters m and n are defined by the process constants, bulk potential and quiescent bias to both source and drain. As can be observed from (6.4) and (6.5), part of charge injection is output signal dependent but another part of charge injection is independent of the output. It is important to note that the signal-dependent part contributes non-linear effect and the closed-loop expression for signal-dependent charge injection will be further examined in next subsection.

6.3 Analysis of Transducer including Error Source Models

For second-order analysis of a practical SC transducer, a comprehensive list of error sources is established. This includes critical switch error sources, op-amp error sources arising from offset, finite open-loop gain and finite common mode rejection ratio. Fig. 6.2(a) shows the auto-zero phase ϕ_1 of CD1 (T2 in Fig. 5.3(b)), with dc offset $V_{os1}(n-1/2)$ and input common mode error $V_{cmrr1}(n-1/2)$. Fig. 6.2(b) shows the charge transfer phase ϕ_2 of CD1 (T3 in Fig. 5.3(c)), with dc offset $V_{os1}(n)$, switch error ΔV_{e1} , finite gain error ε_1 and input common mode error $V_{cmrr1}(n)$. Similarly, The CD2 in auto-zero phase (previous T4 in Fig. 5.3(d)) and transfer phase (T1 in Fig. 5.3(a)) are shown in Fig. 6.3(a) and Fig. 6.3(b) respectively, the notations of error voltage sources have the similar meanings but they are not repeated here.

(a) Auto - zero phase ϕ_1 of CD1 at T2 in topology of Fig. 5.3 (b)

(b) Charge transfer phase ϕ_2 of CD1 at T3 in topology of Fig. 5.3 (c)

Fig. 6.2 Auto-zero phase ϕ_1 and Charge transfer phase ϕ_2 of CD1

Fig. 6.3 Auto-zero phase ϕ_2 and Charge transfer phase ϕ_1 of CD2

During ϕ_1 , the basic voltage equations of CD1 in Fig. 6.2(a) are

$$V_{out1}(n-1/2) = V_{os1}(n-1/2) + V_Q + V_{cmrr1}(n-1/2) \quad (6.10)$$

$$V_{cf1}(n-1/2) = -V_{os1}(n-1/2) - V_{cmrr1}(n-1/2) \quad (6.11)$$

$$V_{cx}(n-1/2) = -V_{os1}(n-1/2) - V_{cmrr1}(n-1/2) \quad (6.12)$$

$$V_{cp2}(n-1/2) = -[V_{os1}(n-1/2) + V_Q + V_{cmrr1}(n-1/2)] \quad (6.13)$$

During ϕ_2 , the basic voltage equations of CD1 in Fig. 6.2(b) are

$$V_{cx}(n) = \Delta V_{ref} - [V_{os1}(n) + \Delta V_{e1} + \varepsilon_1 + V_{cmrr1}(n)] \quad (6.14)$$

$$V_{cf1}(n) = \Delta V_{out}(n) - [V_{os1}(n) + \Delta V_{e1} + \varepsilon_1 + V_{cmrr1}(n)] \quad (6.15)$$

$$V_{cp2}(n) = -[V_{os1}(n) + \Delta V_{e1} + \varepsilon_1 + V_Q + V_{cmrr1}(n)] \quad (6.16)$$

The change of charges in capacitors C_x and C_{cp2} are obtained as

$$\Delta Q_{cx1} = C_x [V_{cx}(n) - V_{cx}(n-1/2)] \quad (6.17)$$

$$\Delta Q_{cp2} = C_{cp2} [V_{cp2}(n) - V_{cp2}(n-1/2)] \quad (6.18)$$

and thus the change of charges in capacitor C_{f1} is

$$\Delta Q_{cf1} = \Delta Q_{cx1} + \Delta Q_{cp2} = C_x (\Delta V_{ref} - \Delta V_{e1} - \varepsilon_1) - C_{cp2} (\Delta V_{e1} + \varepsilon_1) \quad (6.19)$$

where it is assumed that $V_{os}(n) = V_{os}(n-1/2)$ and $V_{cmrr1}(n) = V_{cmrr1}(n-1/2)$. The voltage

developed across the feedback capacitor C_{f1} at time n is

$$V_{cf1}(n) = V_{cf1}(n-1/2) - \frac{\Delta Q_{cf1}}{C_{f1}} \quad (6.20)$$

where $V_{cf1}(n-1/2)$ is defined in (6.11). Since the output voltage of CD1 is defined by

$$V_{out1}(n) = V_Q + \Delta V_{out1}(n) \quad (6.21)$$

Putting (6.15) into (6.21), the incremental output voltage of CD1 at time n is given by

$$V_{out1}(n) = V_Q + V_{os1}(n) + \Delta V_{e1} + \varepsilon_1 + V_{cmrr1}(n) + V_{cf1}(n) \quad (6.22)$$

Substituting (6.11), (6.19) into (6.20) and the final result of $V_{cf1}(n)$ expression is further substituted into (6.22), one can relate (6.21) and (6.22) to solve the incremental output as

$$\Delta V_{out1}(n) = \frac{-\frac{C_x}{C_{f1}} \Delta V_{ref} + (1 + \frac{C_{p2}}{C_{f1}}) \Delta V_{e1}}{1 - \frac{1}{A_1} \left(1 + \frac{C_x + C_{p2}}{C_{f1}} \right)} \cong \frac{-\frac{C_x}{C_{f1}} \Delta V_{ref} + (1 + \frac{C_{p2}}{C_{f1}}) \Delta V_{e1}}{1 - \frac{1}{A_1} \left(1 + \frac{C_{p2}}{C_{f1}} \right)} \quad (6.23)$$

using the definition of $\varepsilon_1 = \frac{\Delta V_{out}(n)}{A_1}$ and assuming $C_{p2} \gg C_x$. This gives the output

expression of CD1:

$$V_{out1}(n) \cong V_Q + \frac{-\frac{C_x}{C_{f1}} \Delta V_{ref} + (1 + \frac{C_{p2}}{C_{f1}}) \Delta V_{e1}}{1 - \frac{1}{A_1} \left(1 + \frac{C_{p2}}{C_{f1}} \right)} \quad (6.24)$$

Similarly, the output expression of CD2 in Fig. 6.3(a) and Fig. 6.3(b) is obtained as follows:

$$V_{out2}(n-1) \cong V_Q + \frac{-\frac{C_x}{C_{f2}} (-\Delta V_{ref}) + (1 + \frac{C_{p2}}{C_{f2}}) \Delta V_{e2}}{1 - \frac{1}{A_2} \left(1 + \frac{C_{p2}}{C_{f2}} \right)} \quad (6.25)$$

and the incremental ac voltage for CD2 output is

$$\Delta V_{out2}(n-1) \cong \frac{-\frac{C_x}{C_{f2}}(-\Delta V_{ref}) + (1 + \frac{C_{p2}}{C_{f2}})\Delta V_{e2}}{1 - \frac{1}{A_2}\left(1 + \frac{C_{p2}}{C_{f2}}\right)} \quad (6.26)$$

From (6.23), ΔV_{e1} is signal-dependent switch error which also relates to the output according to (6.4). Thus, substituting (6.23) back into (6.4) again, we get

$$\Delta V_{e1} \approx \frac{-W_1 L_1 C_{ox}}{2C_{p2}} \left[V_{eff1} - \frac{\left(1 + \frac{C_{p2}}{C_{f1}}\right)\Delta V_{e1} - \frac{C_x}{C_{f1}}(\Delta V_{ref})}{K_{\varepsilon1}} m + \frac{C_x^2 (\Delta V_{ref})^2}{C_f^2 K_{\varepsilon1}^2} n \right] \quad (6.27)$$

where $K_{\varepsilon1} = 1 - \frac{1}{A_1}\left(1 + \frac{C_{p2}}{C_{f1}}\right)$. Solving (6.27) for ΔV_{e1} in CD1 gives

$$\Delta V_{e1} \approx \frac{-W_1 L_1 C_{ox} \left[V_{eff1} K_{\varepsilon1} C_{f1} + m C_x \Delta V_{ref} + \frac{n C_x^2 (\Delta V_{ref})^2}{K_{\varepsilon1} C_{f1}} \right]}{2C_{p2} K_{\varepsilon1} C_{f1} - W_1 L_1 C_{ox} m (C_{p2} + C_{f1})} \quad (6.28)$$

Note that the switch error ΔV_{e2} in CD2 output (6.26) is a function of bias voltages and mismatches in threshold voltages according to (6.5). From (6.24) and (6.25), it is interesting to observe that not only the fundamental dc offset is canceled in the CDS transducer, but also the input common mode error in each single-ended output. This relaxes the common-mode rejection requirement for the op-amp design. However, other non-ideal effects such as the gain error and switch error are boosted by the parasitic gain factor, which is regarded as the error multiplying factor induced by the heavy stray capacitors in tomography operation environment. This is a reasonable from intuitive

viewpoint. Nevertheless, these errors can be reduced significantly through the differential operation in next sub-section.

6.4 Analyzing Differential Operation of SC Transducer

There are two circuit techniques to obtain a differential output: switched-capacitor or continuous-time differential-to-single-ended converter [18]-[19]. The work is based on the continuous-time approach. The rational is to avoid the potential switch errors associated with the SC converter. Hence, the corresponding discrete-time output obtained from CD2 will be subtracted by a continuous-time subtracting circuit in series with a filter as shown in Fig. 6.4. In differential operation scenario, both the CD circuit errors are represented by the mismatch errors associated with switch pair, feedback capacitor pair and op-amp open-loop gain pair during integrated circuit fabrication environment.

Fig. 6.4 Differential output of transducer based on ideal subtractor and filter

In order to facilitate the continuous-time differential operation, a switch network is inserted between the respective output of CD2, CD1 and the respective input of signal-processing stage (which consists of ideal subtractor and ideal 5th-order low-pass filter [54] having 5 kHz cutoff frequency). It is driven by the control clock signals having unsymmetrical duty cycles as shown in Fig. 6.4. Under the clocking scheme, the switch network passes the detected signal in hold phase but it blocks the output coming from reset, auto-zero and charge transfer phase of the CD2 or CD1. To maintain purity of analog ground, an artificial ground is re-established. This is achieved by means of the switches, SW₄ and SW₂, shorting to the analog ground V_Q during reset, auto-zero and charge transfer phase of CD2 or CD1. It is noted that when either switch SW₁ or SW₃ is switched off, the charge injection will be shunted by the respective on-state switch SW₂ or SW₄ to low-impedance analog ground. This turns out that the switch errors are

negligible. The quality of outputs will not be deteriorated by the switch network. Due to three quarter period of clock dedicated for the output at analog ground V_Q , each respective sample-data output signal from the output of the switch network will become a quarter in values during continuous-time averaging process. It turns out that the combined sensitivity in this differential case will be half of that of each CD but the errors from CD2 and CD1 are still minimized in subtraction process. This can be demonstrated by the following proof:

When ϕ_3 and ϕ_4 are off at time $(n-3/2)$,

$$V_{sub1}(n-3/2) = V_Q + \Delta V_{out1} \quad (6.29)$$

$$V_{sub2}(n-3/2) = V_Q \quad (6.30)$$

$$V_a(n-3/2) = V_{sub2}(n-3/2) - V_{sub1}(n-3/2) = -\Delta V_{out1}(n-3/2) \quad (6.31)$$

When ϕ_3 and ϕ_4 are off at time $(n-1)$,

$$V_a(n-1) = V_{sub2}(n-1) - V_{sub1}(n-1) = 0 \quad (6.32)$$

When ϕ_3 is off and ϕ_4 is on at time $(n-1/2)$,

$$V_a(n-1/2) = V_{sub2}(n-1/2) - V_{sub1}(n-1/2) = \Delta V_{out2}(n-1/2) \quad (6.33)$$

When ϕ_3 and ϕ_4 are off at time (n) ,

$$V_a(n) = V_{sub2}(n) - V_{sub1}(n) = 0 \quad (6.34)$$

Since the two sample-data differential input signals are averaged in continuous-time domain in the analog signal-processing block. Thus, the average output of the front-end transducer is given as

$$V_{out} \cong \frac{V_a(n-3/2) + V_a(n-1) + V_a(n-1/2) + V_a(n)}{4} = \frac{\Delta V_{out2}(n-1/2) - \Delta V_{out1}(n-3/2)}{4} \quad (6.35)$$

Substituting (6.28) into (6.23), (6.5) into (6.26), the results of which are then substituted into (6.35), and neglecting higher-order terms, we obtain

$$V_{out} \cong \frac{\frac{2C_x}{C_f} \Delta V_{ref} \left(1 - \frac{\Delta C_f}{2C_f} \right) + \left(1 + \frac{C_{p2}}{C_f} \right) \left[\frac{-WLC_{ox}(V_{eff1} + \Delta V_{r0})}{2C_{p2}} \right] - \left(1 + \frac{C_{p2}}{C_f} \right) \left\{ \frac{- (WL + \Delta WL) C_{ox} \left[V_{eff1} C_f \left(1 - \frac{1}{A} \left(1 + \frac{C_{p2}}{C_f} \right) + \frac{\Delta C_f}{C_f} \right) + m C_x \Delta V_{ref} + \frac{n C_x^2 (\Delta V_{ref})^2}{C_f \left[1 - \frac{1}{A} \left(1 + \frac{C_{p2}}{C_f} \right) + \frac{\Delta C_f}{C_f} \right]} \right]}{2C_{p2} C_f \left[1 - \frac{1}{A} \left(1 + \frac{C_{p2}}{C_f} \right) + \frac{\Delta C_f}{C_f} \right] - (WL + \Delta WL) C_{ox} m (C_{p2} + C_f + \Delta C_f)} \right\}}{4 \left[1 - \frac{2}{A} \left(1 + \frac{C_{p2}}{C_f} \right) \right]} \quad (6.36)$$

where the mismatch definitions are denoted as $W_1 L_1 = W_2 L_2 + \Delta(W_2 L_2) = WL + \Delta(WL)$,

$C_{f1} = C_{f2} + \Delta C_{f2} = C_f + \Delta C_f$, $A_1 = A_2 + \Delta A_2 = A + \Delta A$. WL , C_f and A are parameters

having nominal values, $\Delta(WL)$, ΔC_f and ΔA are the parameters representing random

mismatch. It is apparent that in the numerator that the first term represents the signal with measured C_x together with its sensitivity error factor arising from the mismatch of feedback capacitors, the second term represents the charge injection error of CD2 with threshold voltage mismatch plus parasitic gain bootstrapping factor, the third term represents the charge injection error of CD1 including switch area mismatch, feedback capacitor mismatch, the parasitic gain bootstrapping factor and effect of finite gain on parasitic gain factor. In the denominator, it is observed that the finite gain of the op-amps contribute errors to all the terms in the numerator. If the open-loop gains of both op-amps are maintained high, the mismatch in gain ΔA can be negligible in the analysis.

Chapter 7

Layout Design Considerations

7.1 Introduction

Before an integrated circuit can be manufactured, a layout must be created. It is used to create the masks for the different fabrication steps. A proper layout is essential for a well-performing circuit. The chip area can be minimized by a carefully planned layout. Device properties such as matching, noise and high-frequency performance also rely on good layout. There are processes available for fabricating the IC chips designed. In the design, a standard 0.6 μm CMOS N-well process is being used.

To create a good layout [12], [44], it is necessary to know which devices are critical for the performance of the circuit. The effort should be concentrated on those devices, making the critical parameters as good as possible. In this Chapter, the focus is on the layout of both passive and active devices, and how to achieve, for instance, high matching accuracy. Passive devices such as resistors, capacitors and active devices on MOS layout for small area, low noise and high speed are discussed.

7.2. Resistors

7.2.1 Resistivity and sheet resistance

The process offers a choice of several different resistor materials. Some are better suited to fabricating high-value resistors whilst others for fabricating low-value ones. High

resistivity is greatly an advantage, as it results in low area for large resistances. Properties such as accuracy, linearity and parasitic capacitance to the substrate must also to be considered. In a CMOS technology, various types of integrated resistors are fabricated using various resistive layers available. Here, diffusion (P^+ , n^+ or well) and polysilicon are good examples.

- Small resistance ($R_{sh} < 100 \text{ Ohm}$)

For low resistivity, poly-resistor can be used as a high-performance resistor. It has the highest linearity, low parasitic capacitance and moderate temperature drift. However, the accuracy of about $\pm 25\%$ is poor, and another drawback of it is the low resistivity, which is about 20Ω per square in typical process.

Another option is to use diffusion resistors. In a CMOS process, the source/drain diffusion is often used. The resistivity and temperature drift are about the same as poly. The resistor will exhibit more nonlinear property and have a larger parasitic capacitance with respect to the substrate, which makes the poly resistor a better choice for meeting many design requirements.

- Large resistance ($R_{sh} > 1k \text{ Ohm}$)

For high resistivity, the nwell of a CMOS process can be used. The resistance is about $1.2k \Omega$ per square. The drawback of well resistors is large non-linearity and suffers from high parasitic capacitances. This leads to the other choice for high resistive poly resistor, about $1k \Omega$ per square. This is mainly because of much better performance in the aspect of linearity and parasitic effect when compared with the nwell resistor.

In the layout of the sensor circuits, all the high value resistors use high resistive poly instead of nwell resistor. For the resistors with small values ($< 1\text{ k Ohm}$), the low resistive poly resistor is chosen in the layout to get the good linearity and low parasitic capacitance.

The parameter that would determine the absolute value of a resistor in IC is the sheet resistance and area as shown below:

Fig. 7.1 The definition of the width and length of a resistor

$$R = R_{sh} \times \frac{L}{W} \quad (7.1)$$

where R_{sh} is the sheet resistance.

7.2.2 Temperature Variation

Resistivity depends on temperature in a complex, nonlinear manner. Like any nonlinear function, this one can be expanded into a polynomial series. Unless considerable accuracy is required or the temperature varies widely, only the first two terms of the series are significant

$$R(T) = R(T_0) \left[1 + 10^{-6} TC_1 (T - T_0) \right] \quad (7.2)$$

where $R(T)$ is the resistance at the desired temperature, T ; $R(T_0)$ is the resistance at some other temperature, T_0 ; and TC_1 is the linear temperature coefficient of resistivity (TCR) in parts per million per degree Celsius (ppm/°C). A factor of 10^{-6} has been inserted into equation (7.2) to balance the units involved.

Matched resistors must consist of the same material to ensure that temperature variations do not degrade their matching.

7.2.3 Voltage Modulation

Practical resistors always exhibit some degree of non-linearity; in other words, their resistance varies with applied voltage. Voltage modulation arises from several sources, including self-heating, high-field velocity saturation, and depletion region encroachment. A resistor dissipates power equal to the product of the voltage across it and the current through it. This dissipation causes internal heating. Plastic packages conduct heat rather poorly, so even small amounts of internal heating can cause substantial temperature increases inside the package. Most resistors have relatively large temperature coefficients, and even modest increases in temperature can cause significant resistance variations.

Poly resistors are especially vulnerable to self-heating because they reside on top of the thick-field oxide, which acts as a thermal insulator between the poly resistors and the silicon substrate.

The rate of carrier drift in weak electric fields is proportional to the electric-field intensity. As the field increases, the drift velocity of the carriers eventually becomes diffusion-limited, and the resistance begins to increase. Poly resistors may also exhibit nonlinearities if they are so short that appreciable voltage drops can appear across individual poly grains. Under these conditions, the resistance of the barrier regions between grains becomes a function of the voltage drop across the resistor.

Additional voltage nonlinearities occur in lightly doped diffused resistors, especially base pinch resistors, due to modulation of the depletion regions around reverse-biased junctions. Heavily doped resistors do not experience appreciable voltage nonlinearities because the depletion regions extend only a minute distance into them. Emitter resistors, for example, show practically no voltage modulation.

7.2.4 Matching of resistors

The relative accuracy (matching) of two or more resistors is critical. Special measures then have to be taken when drawing the layout. The matched resistors are made from a number of identical elements, which are placed with the same orientation. Dummy resistor elements can be used in order to create almost identical surroundings of the resistors with an inter-digitized approach. The common techniques are interdigitized or common centroid layout. Note that the common centroid approach can be used for all matching, not just for resistors. An example of two matched resistors in an interdigitized style is shown in Fig. 7.2.

Fig. 7.2 Layout of two matched resistors

If good matching is required, the resistors must be wide enough (5 μ m width for RPOLYH resistor), as the influence of width fluctuations is then decreased. A large area also has an averaging effect on fluctuations of layer resistivity. There is thus a conflict between small area and good matching. The parasitics involved are mainly capacitances to the substrate. They result in an upper frequency limited above. They can also pick up undesired signals from the substrate. Shown in Fig. 7.3, the parasitic capacitance is distributed along the resistor, and reduces the resistor's effect in the circuit.

Fig. 7.3 Simple model of resistor with parasitic capacitance

7.2.5 Resistors in AMS 0.6 μ m CMOS process

In the ECT sensor circuit design, AMS 0.6 μ m CMOS process is used, which includes 5 basic types of resistors: NWELL, POLY1, NDIFF, PDIFF and RPOLYH. Table 7.1 shows their sheet resistors, temperature coefficients, voltage coefficients and matching parameters that provided in the process specifications for reference.

Table 7.1 Resistors specifications for AMS 0.6um CMOS process

Note: The resistor matching is described by

$$\sigma(\Delta R / R) = AR / (W \bullet L)^{1/2}$$

	Sheet resistance	Temp coefficient	Voltage coefficient	Match(AR)
NWELL	1.0kΩ	$6.6 \times 10^{-3} / K$	Nil	3.5%μm
POLY1	33Ω	$0.75 \times 10^{-3} / K$	Nil	12.5%μm
NDIFF	32Ω	$1.8 \times 10^{-3} / K$	Nil	Nil
PDIFF	60Ω	$1.65 \times 10^{-3} / K$	Nil	Nil
RPOLYH	1.2kΩ	$-1.05 \times 10^{-3} / K$	$1 \times 10^{-3} / V$	3.5%μm

7.3 Capacitors

Capacitor is a two-terminal device. There are various types of capacitor available in the CMOS processes, namely poly1-poly2, poly-metal, poly1-Diff (gate oxide) and so on. The capacitor is usually implemented using two conducting layers separated by silicon-oxide. The thinner oxide can implement the bigger value of capacitance per unit area. The thinnest oxide in a CMOS process is the gate-oxide. Area efficient capacitors can therefore be implemented using MOS transistors. They are biased in strong inversion. The source and drain are used as one terminal and the gate as the other. The drawback is that the capacitance is highly voltage dependent. In this standard CMOS process, a second poly-silicon layer is available. Excellent capacitor can be implemented between the two poly layers, which are separated by an oxide with a thickness comparable to that the gate-oxide. Just as for resistor, the matching of capacitors can be critical. The relative

error of capacitor ratio is normally of 0.1%, which is much lower than the error of the absolute value of a capacitor. This can be realized with careful layout as shown in Fig. 7.4 [44]. Just as for the resistors, the devices are split into identical pieces, which they are placed so that the two devices get a common center of mass. It is noted that the devices are surrounded by dummies. They can be skipped if the requirements are modest. Just as for resistors, large devices result in better matching, thanks to statistical averaging.

Fig. 7.4 Layout of two matched capacitors

There are mainly two types of parasitic that must be considered. The first is parasitic capacitance from the bottom plate of the capacitor to the layer below. The bottom plate of the capacitor must be connected to a low impedance node in order to minimize the effect of this capacitance. The second effect is series resistance. For instance, the resistivity of the poly layers might cause a significant series resistance. The maximum distance to a contact to metal must be short enough. A MOS gate capacitor must also be short enough. How large a resistance depends on the frequency of operation. A simple capacitance model with parasitic components is shown in Fig. 7.5. The time constant associated with

the parasitic resistance and the effective capacitance should not be made dominant with respect to the operation frequency.

Fig. 7.5 Simple model of capacitor with parasitics

In AMS 0.6um CMOS process, there are 3 types of common used capacitors: POLY1-DIFF, MET1-POLY1/POLY2, POLY1-POLY2. Table 7.2 shows their area capacitance, temperature coefficients that are provided in the process specifications for reference.

Table 7.2: Capacitors parameters in AMS 0.6um CMOS process

Capacitor	Area capacitance	Temp coefficient
POLY1-DIFF	2.76fF/ μm	Nil
MET1-POLY1/POLY2	0.053fF/ μm	Nil
POLY1-POLY2	0.86fF/ μm	$0.03 \times 10^{-3}/\text{K}$

7.4 MOS Transistors

Active devices in MOS technology refer to the MOS transistor. The layout of the transistors is more complicated than that of the passive devices, as several different layers (fabrication steps) are involved. This section will be focused on layout of high-performance MOS transistors. The most commonly performance requirements in this

sensor system design are high speed, low noise and small area. The heart of the layout of a MOS transistor is simply the crossing of two rectangles: one is polysilicon and the other is diffusion (Fig. 7.6). The polysilicon defines two separate areas in the diffusion rectangle, which are the source and the drain terminals.

Fig. 7.6 MOS transistor layout

The relative accuracy (matching) of two or more transistor is critical. The matched transistors are made from a number of identical elements, which are placed to create almost identical surroundings of transistor with a common center of gravity (common centroid). The common center of gravity is used for all matching. The idea is that a gradient in, for instance, layer thickness will affect all devices with the same center of gravity equally. An example of two matched transistors in a common-centroid layout is shown in Fig. 7.7 [44].

Fig. 7.7 Layout of two matched transistors

(a) Layout for low noise

The noise of a transistor can be divided into two categories. First, there is the noise generated in the channel of the transistor. This noise is unaffected by the layout, as long as the width and length of the transistor are not changed. The second category is the noise generated by layout dependent resistances in series with the transistor terminals. A low noise transistor should have a layout that makes the noise of the second category considerably smaller than that of the first. The most important layout dependent resistance concerning noise is the one in series with the gate. Modern CMOS processes use polysilicon gates. This material has a rather high resistivity compared with metal. In combination with the narrow gate (short channel) of high performance devices, this calls for attentions when the layout is drawn. To get a low resistance, the gate must be connected as densely as possible to metal. Another source of noise is coming from bulk resistance. The noise of the bulk affects the drain current through g_{mb} . Since g_{mb} is much smaller than g_m , the resistance of the bulk is allowed to be considerably larger than

the resistance of the gate. To get a low enough bulk resistance, the transistor should be surrounded as closely as possible by a metal ring with bulk contacts. This also reduces the disturbances from other parts of the circuits, which can be regarded as noise.

(b) Layout for high speed

Just as with noise, the speed limiting phenomena can be divided into two categories. One is the parasitic associated with the active part of the transistor, which is unaffected by the layout. The other is the layout-dependent parasitic capacitance between the transistor terminals. Also, the parasitic resistance in series with the gate can affect the speed, and therefore it belongs to this category. To minimize the gate resistance, the gate connection should be as densely as possible to metal. To accurately predict the influence of gate-resistance, the gate should be modeled as a distributed RC network. To minimize the parasitic capacitance from drain and source to bulk, the area of the drain and source diffusions should be minimized, which is also advantageous for the total area. High-speed transistors are often used with bulk and source to ground. The capacitance associated with the source diffusion does not affect the performance.

(c) Noise coupling

The noise can be coupled into circuit from several sources: from digital circuit, from power supply from substrate and so on. The noise on the substrate is produced by the capacitive coupling of logic nodes with the substrate. Typically, drain contacts in wide transistors of logic gates are kept as small as possible. The area of the drain-to-substrate diodes is consequently small and coupling via the substrate is reduced.

The noise can also be coupled from the lateral metal path. The usual means of reducing this problem is to place the lines carrying analog signals reasonably far away from the line carrying digital signals. Moreover, a dummy line placed between the analog and digital lines biased at a “quiet” voltage achieves a horizontal shielding (Fig. 7.8).

Fig. 7.8 Dummy line for horizontal shielding

In the analog part, the ripple of the power supply is another source of noise. At low frequency, the ripple will not affect the performance of the circuits because of high PSRR (power supply rejection ratio). However, at high frequency, PSRR becomes very poor and the noise will inject into the circuit. The possible solution is to control the noise generation at its source. As shown in Fig. 7.9, both the analog and digital part share a common resistance R_1 so it carries the supply current of both the analog section (I_A) and digital one (I_D). The digital supply current contains some recurring large noise spikes that are due to the switching transients of the digital logic circuits. Hence, the line voltage at the analog section will also be affected by these noise signals.

Fig. 7.9 Analog and digital section sharing the same power supply

This undesirable effect could be reduced by using different power supply lines in order to reduce the common impedance as shown in Fig. 7.10, which is also adopted in the layout of sensor.

**Fig. 7.10 Improved way to reduce the noise coupling
From the digital section into the analog section**

To prevent the digital circuitry from injection noise to the analog circuitry, the analog part is keeping as far as possible from the digital circuitry. Moreover, n^+ guard ring is used to shield the digital circuitry from its environment. This is because the n^+ guard ring provides a low resistive path to the substrate for the stray current.

7.5 Sensor layout

The layout of the whole sensor system is shown in Fig. 7.11. The only digital block—clock generator was located in the bottom right side in the layout and was isolated with double guard ring. Each of the analog blocks, such as front-end interface stage, chopper gain stage, LPF and all the bias current circuits, were surrounded by a guide ring with plenty of bulk contacts to reduce the bulk noise effect. A dummy ground line was placed between the analog and digital ground lines to reduce the coupled noise between the lateral metal paths. To prevent the digital circuitry from injecting noise to analog circuit, the two supply rails were separated, which were named VDDD, GNDD, VDDA and GNDA respectively. Each analog block had their own power supply. All the individual power supply line was connected to the pads in a star configuration. Since an n-well process was used, the digital and analog PMOS transistors were naturally isolated by separate wells. The NMOS transistors, however, interacted via common low-resistive p substrate.

The layout of the front-end stage is very important to the system. Two identically designed capacitance detectors were included. Any offset from this stage can be further amplified by the following gain stage, thus affecting the accuracy of the detection seriously. The offset can be caused by the asymmetries of the differential PMOS input pair in the op-amp, the mismatch of the feedback capacitors and the mismatch of the switch networks in two capacitance detectors. In the layout, to achieve greater matching characteristic, dummy transistors as well as common-centroid technique are used for the input transistors, switch transistors and current mirrors. The feedback capacitors were split into identical pieces and placed so that the two capacitors got a common center of

mass, and surrounded by dummies as well. To reduce the noise coupled from the substrate, a n-well was biased at the analog power supply, thus shielding the plate of the capacitor from the substrate. The relative error of the two feedback capacitances is normally of about 0.1% with careful layout.

The gain of the chopper gain stage is defined by the resistor ratio. Hence, the relative matching accuracy of the resistors are very critical. Because of the requirements for high resistance, good linearity and low parasitic capacitance, high poly resistors were used in the layout. The resistors were made of a number of identical elements, which were placed in the same orientation. Dummy resistors were used in order to create almost identical surroundings of the resistors with a common center of gravity (common centroid). For good matching purpose, the width of the resistors was chosen at 5 μm that is recommended in the design rule manual of the process. The chopper amplifier itself is a two-stage amplifier and a pair of chopper switches. Each chopper switch has 4 NMOS transistors that need to be cross-coupled in order to reduce the charge injections effect. The two-stage chopper amplifier is located in the left side of the chopper gain stage the input transistor pair is also made to be cross coupled for better matching.

The matching is not critical for the resistors in the LPF. The parasitic capacitance distributed along the resistor will affect the LPF frequency response. Consider the resistors variation and the parasitic capacitances, the cut-off frequency can be varied from 4.38 kHz to 6.05 kHz, which is still acceptable for the specification.

Fig. 7.11 The layout of the whole sensor system

Chapter 8

Results and Discussions

8.1 The front-end CV converter

The front-end CV converter is the most important block in the system. It includes the two high-speed op-amps and feedback networks. In order to have fast enough settling time at heavy stray capacitors under high switching frequency, the op-amp needs to be designed to have very high bandwidth. The open-loop gain should be as large as possible to reduce the finite gain error. The simulation results for the gain and phase margin of the front-end op-amp are shown in Fig. 8.1. In the typical case, the op-amp has DC gain of 80 dB, phase margin of 61 degree at unity gain bandwidth of 43 MHz [25]-[27]. Table 8.1 lists the sizes of the transistors used in the Fig. 5.8(a) [9].

Table 8.1 The transistors sizes in front-end amplifier

Transistor	W/L
MP1, MP2	40/4
MN1, MN2	160/2
MN3, MN4	40/2
MP5, MP6,MP7,MP8	80/2
MN9	40/1

Fig. 8.1. AC analysis of the front-end op-amp

In order to simulate the differential output of the front-end transducer, the corresponding discrete-time output obtained from CD2 or CD1 will be made the difference by a continuous-time subtracting circuit in series with a filter as shown in Fig.8.2. A switch network is inserted between the respective output of CD2, CD1 and the respective input of signal-processing stage. For predicting the non-ideal differential output, the mismatch

values are applied to estimate a conservative output. In this case, the output (6.36) is made to exhibit higher value to reflect the actual higher error whenever possible. This leads to practical fabrication error assumptions that $\Delta V_{to} = -5$ mV, $\Delta(WL) = +10\%$ of WL and $\Delta C_f = -0.1\%$ of C_f . It is given that the process parameters are $\Phi_f = 0.405$ V, $V_{to1} = 0.848$ V, $C_{ox} = 2.72 \times 10^{-3}$ F/m², K_1 (1st order body factor in BSIM3 Model) = 1.057 V^{1/2}, K_2 (2nd order body factor in BSIM3 Model) = -0.123, and the design parameters are $V_Q = 1$ V, $\Delta V_{ref} = 1$ V, $V_B = 0$ V, $V_g = 5$ V, $A = 10,000$, $W = 10$ μ m, $L = L_{eff} = 0.55$ μ m (0.6 μ m drawn length), $C_f = 8$ pF and $C_{p2} = 150$ pF, we get $V_{eff1} = 2.682$ V (equation 6.6), $m = 1.27$ (equation 6.8) and $n = 0.0543$ V⁻¹ (equation 6.9). The empirical equation of (6.36) becomes

$$V_{out} = (0.0625 + 0.0016)C_x + 6.432 \times 10^{-5} + 4.32 \times 10^{-5} C_x + 4.7 \times 10^{-7} C_x^2 \quad (8.1)$$

The first fundamental sensitivity term is much larger than the second sensitivity error term which is caused by mismatch of feedback capacitor pair. If the layout of integrated capacitors were not addressed properly, the second numerical value would be increased to affect the accuracy of sensitivity but it is not harmful because of the system gain calibration. As interpreted from the third, fourth and fifth terms in (8.1), they are generated by the difference of two switch errors. These include a residual dc offset term, a linear sensitivity error term and a nonlinear sensitivity error term. They cannot be canceled completely in differential operation because of (i) the mismatch in NMOS switches and (ii) different characteristic of charge injection impacting on NMOS switches. Nevertheless, the individual contribution is still minute. Thus, the final residual

error displays very small linear and nonlinear sensitivity errors and exhibits minute baseline dc offset that will drift with time and temperature.

In order to verify the empirical equation (8.1) obtained from (6.36), design and process parameters and practical mismatch assumptions in fabrication, the realistic HSPICE transistor-level simulation was carried out using the AMS 0.6 μm CMOS process parameters.

Fig. 8.2 The set-up for front-end transducer simulation

The specified parameters are listed in Table 8.2.

Table 8.2: Parameters and their values for front-end CV converter simulations

Parameter	Value
Feedback capacitor C_f	8 pF
Supply voltage	5V
Switching frequency	250 kHz
Excitation voltage ΔV_{ref}	1 V
Measured capacitor C_x Min~Maximum value	1 fF ~2pF
Artificial dc offset in high speed op-amp 1	5mV
Artificial dc offset in high speed op-amp 2	-2mV

The comparison among the predicted, simulated and ideal output against the detection capacitance C_x is illustrated in Fig. 8.3 and Fig. 8.4. In these figures, the term “equation” means the predicted first stage output values based on equation (8.1); the term “simulation” means simulated results of the first stage outputs based on post layout simulation; the term “ideal” means the ideal first stage output regardless of all nonlinear items and errors. As can be seen in both figures, the predicted output values are close to the simulation results, ranging from 0 to 10fF and ranging from 0 to 2pF for different C_x values. In addition, in the presence of non-ideal effects, at small capacitance detection range (0 – 10fF), the simulated or predicted sensitivity values show slight nonlinear deviation from the ideal sensitivity value of 62.5 mV/pF in this front-end transducer design, but the derivation becomes negligible when operated in higher C_x values. For

entire sensor system, the final sensitivity can be scaled to the targeted value through the back-end amplifying block such as chopper difference amplifier [9] or chopper differential difference amplifier [15]. Furthermore, despite the feedback capacitors has offered up to 0.1% matching performance, their absolute values of 8pF would be subject to about maximum of +/-10 % variation on the sensitivity in the context of the fabrication accuracy. However, it is not a critical issue because the system gain will be adjusted during low permittivity and high permittivity calibration procedures [6].

Due to the residual charge injection error as mentioned above, the simulated dc offset of 0.083 mV at zero value of C_x is observed. Since the offset value (equivalent of 1.33fF) is low when compared with few ten mV (equivalent of 0.03 pF) encountered in the prior-art SC ECT transducer using discrete implementation [2], this validates that the SC CDS ECT transducer offers significant reduction in baseline dc offset.

Fig. 8.3 Output voltage versus Cx from 0 to 10fF

Fig. 8.4 Output voltage versus Cx from 0 to 2pF

For assessing the baseline drift characteristic with temperature effect, Fig. 8.5 shows the plot of output against different temperature at zero value of C_x . For temperature from 25°C to 40 °C, the change of the output is 0.065 mV, which is then translated to the change of 1 fF based on the design sensitivity of 62.5 mV/pF. Compared to the reported result [2] for a change of 5 fF from 25°C to 40 °C, the SC CDS ECT transducer has achieved considerable improvement on the baseline drift characteristic with temperature. Regarding the output stability of the detected C_x against a broad range of temperature, the simulated output is plotted in Fig. 8.6 to illustrate the output fluctuation from 25°C to 100 °C for $C_x = 1$ pF. It can be calculated the temperature coefficient of the output is 0.045 mV/°C. Compared to the estimated value of -6mV/°C in the reported result of [3], the SC CDS ECT transducer offers significant lower operation temperature coefficient.

Fig. 8.5 Output voltage versus temperature from 0 to 100°C with $C_x=0\text{fF}$

Fig. 8.6 Output voltage versus temperature from 0 to 100°C with $C_x=1\text{pF}$

Table 8.3 shows the summary of the comparison between different SC transducers. Based on the technical merits of the SC CDS ECT transducer, the intrinsic stability allows the reduction in the frequency of baseline correction in an ECT system, thus minimizing the number of interrupt time in system controller. With improved integrated design approach, the component matching level is enhanced because integrated capacitors have better matching characteristic than integrated resistors. Due to elimination of external components in this SC CDS ECT transducer design, it is possible to integrate the entire transducer with high-performance voltage references, ADC, DACs and communication interface for each system-on-chip (SOC) integrated electrode. This permits another level of miniaturization for an ECT system, implying the possibility for realizing a portable ECT system in future.

Table 8.3: Comparison of baseline and stability performance for different SC transducers

Parameter	SC ECT [2]	SC ECT [3] Integrated Electrode	SC CDS ECT This Work
Baseline dc offset	few tens mV	————	0.083 mV
Change of baseline capacitance with temp. at $C_x = 0$ (25 °C to 40 °C)	5 fF	————	1fF
Output tempco. at $C_x = 1$ pF (25 °C to 100 °C)	————	-6 mV/°C	0.045 mV/°C
Stray Capacitors	150 pF	50 pF	150 pF

8.2 The Chopper Operational Amplifier

In order to further amplify the signal from the first stage, a second stage with 24 times in gain is needed. Since the dc offset and $1/f$ noise will also be amplified by 24 times, it is important to introduce an offset cancellation scheme in this stage so that it will not degrade the overall offset performance of the whole ECT system.

A chopper operational amplifier is used here to play the role for dc offset cancellation in the second stage. It consists of a two-stage amplifier plus a pair of chopper switches as shown in Fig 5.9 in Chapter 5.

The two-stage amplifier is designed to have 98dB gain with 95° phase margin and 19MHz unity gain bandwidth as shown in Fig 8.7. Fig 8.8 shows the simulation result for the common mode rejection ratio of the amplifier. The CMRR is more than 100dB at low frequency, which is important for ECT applications.

Fig 8.7 The ac analysis of chopper operational amplifier

Fig 8.8 The simulated common mode rejection ratio of chopper op-amp

8.3 The Continuous-Time Filter

The cut-off frequency of the continuous-time filter is 5 kHz, with over design to cope with the worst case process variation. The simulation results of the frequency responses are shown in Fig. 8.9. Fig 8.10 depicts the noise root spectral density for the Sallen Key low pass filter. From the results shown, the integrated noise is 143 μ V in 5 kHz bandwidth.

Fig. 8.9 The simulated cut-off frequency of the continuous-time filter in different process conditions

Fig 8.10 The noise simulation for 3rd order low-pass filter

8.4 Integrated System

To evaluate the whole system performance, the transistor-level HSPICE simulation is carried out on the basis of the model parameters of the AMS 0.6 μm CMOS process. The simulated integrated system, as depicted in Fig 8.11 [9], includes (i) the front-end sensor interface circuit (ii) the chopper amplifier gain stage and (iii) the third-order continuous-time low-pass filter.

Fig. 8.11 The integrated system for system simulation

The specified parameters are listed in Table 8.4.

Table 8.4: Parameters and their values for system simulations

Parameter	Value
Feedback capacitor C_f	8 pF
Switching frequency	250 kHz
Chopping frequency	25 kHz
Excitation voltage ΔV_{ref}	1 V
Measured capacitor C_x	1 fF – 2 pF
Temperature range	0 °C ~ 100°C

The simulation output waveforms of overall system including the CDS front-end stage, chopper second stage and third order filter (the final stage) are shown in Fig 8.12 and Fig 8.13. The intentional dc offsets have been added in the CDS front-end stage (5mV for CD1 and –2mV for CD2) and chopper second stage (5mV) respectively in order to simulate the non-ideal condition. From the final dc output, the simulated capacitor C_x is referred to almost 1pF in value, which is independent of offsets being added. This has demonstrated that the CDS circuit is insensitive to offsets of op-amps.

Fig 8.12 The simulation results of the first stage outputs and the final filter output

Fig 8.13 The simulation results of the first stage outputs and the second chopping amplifier stage output

Fig 8.14 shows the zoom in view of the output waveforms from the first stage of transducer. It can be seen that different phases of operation for CD1 and CD2 outputs are shown in time domain.

Fig 8.14 The zoom-in view of the first stage output waveforms

In order to confirm the sensitivity of the proposed ECT system design against variation of process parameters, 30 Monte Carlo simulation runs had been done for the overall system. The simulation was based on the detection of C_x at 1pF and the result is shown in Fig 8.15. In parameters setting, $\Delta C_f = \pm 1\%$, $\Delta V_{th} = \pm 5\text{mV}$, $V_{os1} = \pm 5\text{mV}$ (the dc offset in front-end op-amp in CD1), $V_{os2} = \pm 3\text{mV}$ (the dc offset in front-end op-amp in CD2). The

final output voltage V_{out} after the filter is plotted. From the results, the ideal output voltage is 2.5V, with variation of $\pm 0.03V$ with reference to 1.5V as 1V is set at analog ground. This corresponds to the change of $\pm 2\%$ in output reading, which is considered to be low sensitivity to variation of process parameters.

Fig 8.15 Monte Carlo simulation result for V_{out} with $C_x=1pF$

Fig. 8.16 illustrates the step response of the capacitance measuring circuit when the capacitor C_x is changed in steps from 1 fF to respective values at 500 fF, 1 pF, 1.5 pF and 2 pF. The results have shown that the settling time of each step is around 120 μS . Parallel measurements channels will be used here to increase the overall data capture speed. For 12 electrode system, the total settling time for one frame measurement is about $12 * 120 \mu S = 1.44 mS$. So it is easy for the system to handle more than 400 frames per second rate.

Fig. 8.16 Step response of the proposal capacitance measuring circuit

Fig. 8.17, Fig. 8.18 and Fig. 8.19 are the comparison results between the previous circuit [1] and the proposed circuit. Intentional offsets of 5 mV have been added in the circuit of Fig. 3.3 and the proposed circuit Fig. 5.1. The comparison circuits are based on the similar type of proposed block diagram as described in Fig. 8.11.

Fig 8.17 illustrates the final output results versus different capacitor values, starting from 1 fF to 2 pF. These results have confirmed that the proposed circuit exhibits much lower baseline drift caused by the system offset and displays very good linearity when compared with the previous work.

Fig. 8.17 Simulation results showing the relationship between the capacitance Cx and the DC output voltage

Fig. 8.18 illustrates the output voltage of the system versus the temperature variation (0 to 100 °C) with capacitance of 1 fF, while Fig. 8.19 illustrates the output versus the temperature variation at 1 pF. The results have shown that the proposed system has stable output voltage against temperature when compared with the previous circuit.

Fig. 8.18 Simulation results showing relationship between the temperature and the output DC voltage at Cx=1fF

Fig. 8.19 Simulation results showing relationship between the temperature and the output DC voltage at Cx=1pF

Chapter 9

Conclusion and Recommendation

9.1 Conclusion

Different approaches for the ECT system and the offset cancellation techniques have been reviewed. A new switched-capacitor ECT sensory system including CDS front-end stage, second CHS gain stage and Sallen-Key low-pass filter stage for realizing a tomography imaging system electronics has been presented. A new front-end interface has been proposed. It is based on the switched-capacitor capacitive transducer which employs the correlated double-sampling technique to reduce the dc offset and $1/f$ noise of the CMOS amplifiers and utilizes the resettable topology to facilitate the high speed charging and discharging operation under heavy stray capacitance of 150 pF. The influence of non-ideal effects to a fully-integrated switched-capacitor CDS tomography based transducer has been investigated in details. The analytical expressions, either single-ended outputs or differential output, have also been derived. These give the significant insight and understanding on how the heavy stray capacitors, design parameters, process parameters, non-ideal components, mismatch effects of components impacting on the performance of the SC transducer in terms of sensitivity factor and residual baseline dc offset. The hand-calculated predictions are close to the HSPICE simulation results using the realistic Level 49 BSIM3 models. It has shown that all the non-ideal effects will cause negligibly small error for ECT application. From the simulated results, it is concluded that the proposed front-end circuit reduces the $1/f$ noise

and the dc offset greatly without losing speed by introducing the CDS technique, resettable topology and level-shifting technique for the front-end capacitance detection circuit, whilst the use of the chopper stabilization technique for the back-end signal-processing task maintains the quality of processing signal [9]. This leads to low offset and low temperature drift performance. Hence, high sensitivity as well as resolution down to 1 fF can be achieved even under heavy parasitic capacitances of 150 pF. There is still some finite offset generated in the system. This offset can be calibrated by the baseline correction arrangement.

The complete system simulations have also shown a good linear relationship between C_x and the output voltage with small base line drift, which is small when compared with previous research works. Monte-Carlo simulations further confirm the low sensitivity of system against variation of process parameters.

Using CMOS process technology, the proposed circuit can be cheaply implemented. This design can be integrated together with the digital controller, DAC and ADC for each sensor electrodes directly, which eliminates long screened cables from electrodes to capacitance measuring circuits and reducing external interface and improving the system performance ultimately.

9.2 Recommendation

In the proposed ECT system, the CDS circuit in the front-end stage and the chopper modulator in the second gain stage are realized using MOS switches. The MOS switch non-idealities including the clock feed through and channel-charge injection will affect residual offset. They become the main cause of the base line drift in the system.

In the front-end transducer, the base line drift can cause around 1.33 fF error, which can be reduced by eliminating the signal-dependent charge injection effect of MOS switches.

In the front-end transducer, the charge injection of capacitance detector 1 is signal-dependent with the function of the incremental ac output and its squared ac output, while the charge injection of capacitance detector 2 is a constant value. The charge injections from the two CDs cannot be cancelled perfectly by the subtractor in the later stage. The non-ideal differential transducer output would be suffered from the signal-dependent switch error. This error can be reduced by using boost-strapped switch [34] instead of conventional NMOS switch with any fixed gate voltage. Fig. 9.1 [34] shows the actual boost-strapped circuit. It operates on a single phase clock ϕ that turns the switch M11 on and off. When the switch is on, its gate voltage V_g is greater than the analog input signal V_{in} by a fixed difference of V_{cc} . This ensures that the switch is operated in a manner consistent with the reliability constraints. Because the switch V_{gs} is relatively independent of the signal, the charge injections from the two CDs can be removed by the subtractor effectively.

Fig. 9.1 The boost-strapped circuit

The proposed ECT sensor is suitable for use with capacitance tomographic imaging system having 12 electrodes [2]. For further increase in the number of the electrodes or the length of the electrode to be greatly shortened to reduce the averaging effect along the axial direction, the present circuit architecture based on the charge transfer principle will be continued for further improvement.

References

- [1] Dickin, F.J.; Hoyle, B.S.; Hunt, A.; Huang, S.M.; Ilyas, O.; Lenn, C.; Waterfall, R.C. ; Williams, R.A.; Xie, C.G.; Beck, M.S.;" Tomographic imaging of industrial process equipment: techniques and applications", Circuits, Devices and Systems, IEE Proceedings G, vol. 139, no. 1, pp. 72 – 82, Feb. 1992.
- [2] S. M. Huang, C. G. Xie, R. Thorn, D. Snowden and M.S. Beck, "Design of sensor electronics for electrical capacitance tomography", IEE Proc. Part G, Circuits, Devices and Systems, vol. 139, no. 1, pp. 83-88, Feb. 1992.
- [3] P. M. Williams, R. J. Haycock and T. A. York, "Integrated electrodes for electrical capacitance tomography", Proc. IEEE Instrumentation and Measurement Technology Conference (IMTC), vol. 1, pp. 472-475, May 1998.
- [4] H. Hahnel, W. Q. Yang and T. A. York, "An AC-based capacitance measuring circuit for tomography systems and its silicon chip design", Advances in Sensors, IEE Colloquium, pp. 6/1 - 6/8, Dec. 1995.
- [5] W. Q. Yang and T. A. York, "Capacitance tomography sensor without CMOS switches", IEE Electronics Letters, vol. 33, no. 14, pp. 1211-1213, July 1997.
- [6] W. Q. Yang and T. A. York, "New AC-based capacitance tomography system", Proc. IEE Science, Measurement and Technology, vol. 146, no. 1, pp. 47-53, Jan. 1999.
- [7] Christian C. Enz and Gabor C. Temes, " Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, Correlated double sampling and chopper stabilization", Proceedings of the IEEE, Volume 84, Issue 11, Page(s):1584 – 1614, Nov. 1996.
- [8] Huang,S.M., Plaskowski, A.B., Xie,C.G., and Beck, M.S.:" Capacitance-based tomographic imaging system", Electron, Lett., 24,(7), pp.418-419, 1998.
- [9] J. Peng and P.K. Chan "A tomography based switched-capacitor measuring circuit with Low offset and low temperature drift", Proc. IEEE Instrumentation and Measurement Technology Conference (IMTC), vol. II, pp. 1429-1432, May 2004.
- [10] David A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.
- [11] F. Silveira and D. Flandre, "Operational amplifier power optimization for a given total (slewing plus linear) settling time", Proc. IEEE Symposium on Integrated Circuits and Systems Design (SBCCI), 2002.
- [12] C. T. Chuang, " Analysis of the settling behavior of an operational amplifier". IEEE Journal of Solid-state Circuit, Vol. SC-17, NO.1, February 1982.
- [13] J. H. Shieh, M. Patil and B. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches", IEEE Journal of Solid-State Circuits, vol. SC-22, no. 2, pp. 277-281, April 1987.

- [14] R. Jacob Baker, Harry W. Li and David E. Boyce, *CMOS Circuit Design, Layout and Simulation*, IEEE Press, 1998.
- [15] P. K. Chan, K. A. Ng and X. L. Zhang, "A CMOS chopper-stabilized differential difference amplifier for biomedical integrated circuits", Proc. IEEE Midwest Symposium on Circuits and Systems (MWCAS), vol. III, pp. 33-36, July 2004.
- [16] Bakker, A and Huijsing, J.H., "Offset reduction in current-mode Microsystems", Circuits and Systems, 1996. ISCAS '96., 'Connecting the World', 1996 IEEE International Symposium on Volume 4, Page(s):344 - 347 vol.4, May 1996.
- [17] C.C. Enz, E.A. Vittoz and F. Krummenacher, "A CMOS Chopper amplifier", IEEE SC-22 , pp. 335-342, 1987.
- [18] L.K. Baxter, *Capacitive Sensors Design and Applications*, IEEE press, 1997.
- [19] R. Unbehauen and A. Cichocki, "MOS Switched-Capacitor and Continuous-Time Integrated Circuits and Systems Analysis and Design," Springer-Verlag, 1989.
- [20] S. D. Willingham and K. W. Martin, "Effective Clock-Feedthrough Reduction in Switched Capacitor Circuits," IEEE International Symposium on Circuits and Systems, vol. 4, pp. 2821 – 2824, 1990.
- [21] R. Unbehauen and A. Cichocki, *MOS Switched-Capacitor and Continuous-Time Integrated Circuits and Systems Analysis and Design*, Springer-Verlag, 1989.
- [22] K. Martin and A. Sedra, "Effects of the OPAMP Finite Gain and bandwidth on the performance of Switched-Capacitor Filters," IEEE Trans. Circ. Syst., vol. 28, pp. 882-892, Aug. 1981.
- [23] R.C. Yen and P. R. Gray, "A MOS Switched-Capacitor Instrumentation Amplifier," IEEE Journal. Solid-State Circ., vol. 17, pp. 1008-1013, Dec. 1982.
- [24] K. Martin, L. Ozcolak and G. C. Temes, "A Differential SC Amplifier," IEEE Journal. Solid-State Circ., vol. 22, pp. 104-106, Feb. 1987.
- [25] L.E. Larson and G. C. Temes, "SC Building Blocks with Reduced Sensitivity to Finite Amplifier Gain", Bandwidth and Offset Voltage, Proc. IEEE Int. Symp. Circ. Syst., pp. 334-338, 1987.
- [26] Hiok-Tiaq Ng; Ziazadeh, R.M. and Allstot, D.J., "A multistage amplifier technique with embedded frequency compensation", Solid-State Circuits, IEEE Journal of vol. 34, no. 3, pp. 339 – 347, March 1999.
- [27] K. Nagaraj, "SC Circuits with Reduced Sensitivity to Finite Amplifier Gain", Proc. IEEE. Int. Symp. Circ. Syst., pp. 618-621, 1986.
- [28] F.J. Wang and G. C. Temes, "A Fast Offset-Free S/H Circuit," IEEE Journal of Solid-State Circ., vol. 23, pp.1270-1272, Oct. 1988.

- [29] J. Robert, etc., "Offset and Clock feedthrough compensated SC Integrators," Proc. IEEE Int. Symp. Circ. Syst., pp. 817, 1986.
- [30] Bector, S., "Design of a third-order single amplifier filter", IEEE Transactions on Circuits and Systems, vol. 22, no. 4, pp. 329 – 334, Apr. 1975.
- [31] F. W. Stephenson, *RC Active Filter Design Handbook*, Wiley Electrical and Electronics Technology Handbook series.
- [32] N. A. Radev and K. P. Ivanov, "Area-efficient gain and offset compensated very-large-time-constant SC integrator," Electronics letters, vol. 36, 2000.
- [33] J. Silva-Martinez and A. Vazquez-Gonzalez "Impedance scalers for IC active filters," Proceedings of the IEEE International Symposium, vol. 1, pp. 151 –154, 1998.
- [34] Abo, A.M. and Gray, P.R.;" A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter", IEEE Journal of Solid-State Circuits, vol. 34, no. 5, pp. 599 – 606, May 1999.
- [35] P.K. Chan, L.S. Ng, L. Siek, B.L. Tan and C. L. Ang, "Flicker noise optimization of CMOS operational amplifiers," International Conference on Noise in Physical Systems and 1/f Fluctuations (ICNF), August. 1999.
- [36] Y. P. Tsividis and J. O. Voorman, *Integrated Continuous-time Filters- Principle, Design and Applications*, IEEE Press, 1993.
- [37] W. Steinhagen and W.L.Engl, "Design of integrated analog CMOS circuit – a multichannel telemetry transmitter", IEEE Journal, Solid-State Circuit, vol.SC-13, pp. 799-805, Dec.1978.
- [38] R. Woudsma and J. M. Noteboom, "The modular design of clock-generator circuits in a CMOS building-block system," IEEE Journal of Solid-State Circuits, vol. SC-20, pp. 770-774, June. 1985.
- [39] J. P. Uyemura, *Fundamentals of MOS Digital Integrated Circuits*, Addison-Wesley, pp. 420-424, 1988.
- [40] Bakker, A.; Thiele, K. and Huijsing, J.H.; "A CMOS nested-chopper instrumentation amplifier with 100-nV offset", IEEE Journal of Solid-State Circuits, vol. 35, no. 12, pp.1877 – 1883, Dec. 2000.
- [41] S. M. Huang, R. G. Green. A. Plaskowski, and M. S. Beck, " A high frequency stray-immune capacitance transducer based on the charge transfer principle," IEEE Trans. Instrum. Meas.,vol. 37, pp. 368-373, June 1988.
- [42] W. Q. Yang, "Further developments in AC-based capacitance tomography system, " Proc. Inst. Elect. Eng. Sci. Meas, Technol.,vol. 72, no. 10, pp. 3902-3907, Oct. 2001.
- [43] W. Q. Yang. "Hardware Design of Electrical Capacitance Tomography Systems", Measurement Science & Technology, vol.7. no. 3, March 1996.
- [44] Alan Hasting, *The Art of Analog Layout*, Pearson Prentice Hall, 2005.

- [45] Gray, Hurst and Lewis Meyer, *Analysis and Design of Analog Integrated Circuit*, Kluwer Academic Publishers, 1997.
- [46] W. Q. Yang, A. L. Stott, M. S. Beck and C. G. Xie, "Development of capacitance tomographic imaging systems for oil pipeline measurement", *Rev. Sci. Instrum*, (8), pp. 4326-4332, 1995.
- [47] S. McKee, T. Dyakowski, R. A. Williams, T.A. Bell and T. Allen. "Solids flow imaging and attrition studies in a pneumatic conveyor." *Powder Technol.*, 1005, 82, pp. 105-113, 1995.
- [48] G. Dickin, and M. Wang, "Electrical resistance tomography for process applications", *Meas. Sci. Technol.*, 1006, 7, (3), pp.247-260, March 1996.
- [49] N. White and R. Waterfall, "ECT for the condition monitoring of wood poles carrying overhead power lines". *Proceedings of IEE colloquium on Advances in electrical tomography*, Manchester, 1006, pp. 13/1-13/3.
- [50] E. Pickup, R. Deloughry and T. Hartley, "Measurement of small capacitance changes for use in tomography imaging", *Process Tomography- 95*, pp.256-265, Bergen, April 1995.
- [51] W. Q. Yang, "Charge injection of electrical capacitance tomography systems", *Meas. Sci. Technol.*, 1006, 7, (3) pp. 1073-1078, July 1996.
- [52] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001.
- [53] M. Banu and Y. Tsividis, "Detailed analysis of nonidealities in MOS fully integrated active RC filters based on balanced networks", *vol. SC-18*, no.6, Dec..1983.
- [54] D.J. Allstot and K.S. Tan, "Simplified MOS switched capacitor ladder filter structures," *IEEE Journal. Solid-State Circuits*, vol. 16, pp. 724-729, Dec. 1981.

Author's publication:

- [1] J. Peng and P.K. Chan "A tomography based switched-capacitor measuring circuit with Low offset and low temperature drift", Proc. IEEE Instrumentation and Measurement Technology Conference (IMTC), vol. II, pp. 1429-1432, May 2004.
- [2] J. Peng and P.K. Chan "Analysis of Non-Ideal Effects on a Tomography Based Switched-Capacitor Transducer", IEEE Sensors Journal, under 1st revision, 2006.