Design and fabrication of micromachined RF switches and integrated switching circuits

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Design and Fabrication of Micromachined RF Switches and Integrated Switching Circuits

Tang Min

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2007

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STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

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Date

Tang Min

Tang Min

Dedicated to my family

*Our greatest glory is not in never falling,
but in rising every time we fall.*

————— *Confucius*

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TABLE OF CONTENTS

Acknowledgement	i
Table of Contents	ii
Abstract	vii
List of Figures	viii
List of Tables	xviii
1. Introduction	1
1.1 Motivation	1
1.2 Objectives	3
1.3 Major contribution	4
1.4 Organization	8
2. Literature Review	10
2.1 Review of RF MEMS Switches	10
2.1.1 Basic principles and configurations of RF MEMS switch	12
2.1.2 Vertical RF MEMS switches	15
2.1.3 Lateral RF MEMS switches	18
2.2 RF MEMS Switching Circuits	22
2.3 Fabrication Process of High-Aspect-Ratio Suspended Structures	26
2.4 Glass Etching Techniques	29
2.5 Summary	31
	ii

3. Lateral RF MEMS Switches	32
3.1 Electrical Design and Simulation	33
3.1.1 RF circuit design of the lateral switch	34
3.1.2 RF circuit model of the lateral switch	36
3.1.3 Double-beam lateral switch	43
3.2 Mechanical Design and Simulation	45
3.2.1 Static behavior	46
3.2.1.1 Electrostatic force F_e	46
3.2.1.2 Restoring force F_r	48
3.2.1.3 Threshold voltage V_{th}	50
3.2.2 Dynamic analysis	56
3.2.2.1 Frequency response	56
3.2.2.2 Effective mass	57
3.2.2.3 Switching time	61
3.2.2.4 Release time	64
3.3 Experiment Results and Discussions	64
3.3.1 RF response characterization	68
3.3.1.1 The single-beam switch and the double-beam switch	69
3.3.1.2 Cantilever beam design effect	73
3.3.1.3 Metal coating effect	79
3.3.1.4 Lifetime of the lateral switch	81
3.3.1.5 The lateral switch with a separate fixed-electrode	82

3.3.2 Mechanical measurements	85
3.3.2.1 Static behavior	85
3.3.2.2 Dynamic behavior	87
3.4 Summary	89
4. Integrated Switching Circuits	92
4.1 Si-Core Transmission Line	93
4.1.1 Design of the Si-core CPW	94
4.1.2 Losses of the Si-core CPW	98
4.1.2.1 Conductor loss	98
4.1.2.2 Dielectric loss	100
4.1.2.3 Radiation loss	102
4.1.3 Effect of the material properties and process variations	103
4.1.3.1 Effect of the substrate material	103
4.1.3.2 Effect of the core material	105
4.1.3.3 Effect of the process variations	107
4.1.4 Experimental results and discussions	111
4.1.4.1 Comparison between simulation results and measurement results	112
4.1.4.2 Effect of the geometrical parameters	115
4.1.4.3 Effect of the material properties	118
4.2 Integrated Switching Circuits	122
4.2.1 SP2T switching circuit	123
4.2.1.1 Design of the in-line SP2T switching circuit	123
4.2.1.2 Modeling and simulation of the SP2T switching circuit	125

4.2.1.3 Different types of SP2T switching circuits	129
4.2.2 Design of the SP3T switching circuit	132
4.2.3 Design of the SP4T switching circuit	134
4.2.4 Experimental results and discussions	136
4.2.4.1 In - line SP2T switching circuit	137
4.2.4.2 Different designs of the SP2T switching circuits	140
4.2.4.3 SP3T switching circuit	143
4.2.4.4 SP4T switching circuit	145
4.3 Summary	147
5. Fabrication Technology	150
5.1 Fabrication Process Flow	151
5.2 Si-Thin Film-Glass Anodic Bonding	158
5.2.1 Si-thin film-glass anodic bonding mechanism	159
5.2.2 Preparation of bonding samples	161
5.2.3 Experimental results and discussions	162
5.3 KOH Anisotropic Etching	167
5.3.1 Layout design consideration	167
5.3.2 Etching temperature effect	171
5.4 Self-Aligned Etching of the Glass	173
5.5 Shadow Mask Techniques	175
5.5.1 Design and fabrication of the shadow mask	175
5.5.2 Metal deposition through a shadow mask	180
5.6 Summary	184

6. Conclusions and Recommendations	186
6.1 Conclusions	186
6.2 Recommendations	189
 Appendix A Equivalent Circuit Model of the Transmission Line	192
Appendix B Radiation Loss	195
Publication List	197
References	200

ABSTRACT

This thesis presents a new type of lateral switches and switching circuits for high frequency applications fabricated by a single-mask substrate transfer process.

The lateral RF MEMS switch consists of silicon-core coplanar waveguide (CPW) transmission line and a cantilever-beam electrostatic actuator. The movable part is a high-aspect-ratio silicon (Si) cantilever beam coated by metal. The electromagnetic modeling and design as well as mechanical modeling and design are depicted in detail. Both the RF response and the mechanical behaviour are verified by extensive experiments. The switch shows an insertion loss of below 1 dB at 50 MHz – 25 GHz. Both return loss and isolation are higher than 20 dB. The switching speed is 35 μ s. The life span is more than one million switching cycles.

Different types of single-pole-multiple-throw (SPMT) switching circuits are designed based on the investigation of the Si-core CPW, including single-pole-double-throw (SP2T), single-pole-three-throw (SP3T) and single-pole-four-throw (SP4T) switching circuits. In particular, three SP2T switching circuits are designed for low loss, high isolation and small circuit area. All SPMT switching circuits can work at 50 MHz - 10 GHz. The insertion loss is below 1 dB. The return loss and isolation are above 15 dB.

A single-mask substrate transfer micromachining process is developed for the lateral switches and switching circuits on the glass substrate. The fabrication techniques of Si-thin film-glass anodic bonding, silicon thinning using KOH solution, glass self-aligned etching and shadow mask are discussed in detail. The advantages of this process are high-aspect-ratio, low-loss, high flexibility and low-cost.

LIST OF FIGURES

Figure 2-1	(a) The schematic of a shunt switch circuit configuration, (b) SEM micrograph and (c) schematic cross sectional view of a vertical capacitive shunt switch [28-31].	14
Figure 2-2	The schematic illustration of (a) a series switch circuit configuration, (b) top view, (c) cross sectional view along A-A' and (d) cross sectional view along B-B' of a vertical metal-contact series switch [46].	14
Figure 2-3	The schematic illustration of a comb-drive actuated lateral switch fabricated using nickel surface micromachining process (a) top view and (b) cross sectional view [68].	18
Figure 2-4	The schematic illustration of a thermally actuated lateral switch (a) 3D view and (b) cross sectional view [77].	19
Figure 2-5	The schematic illustration of an electrostatically actuated lateral switch (a) top view and (b) cross sectional view [80].	20
Figure 2-6	Six types of SP2T switching circuits (a) 1st type [87-88], (b) 2nd type [89], (c) 3rd type [91], (d) 4th type [93], (e) 5th type [94], and (f) 6th type [95].	23
Figure 3-1	Schematics of the lateral switch (a) top view and (b) cross sectional view along A-A'.	35
Figure 3-2	The equivalent circuit of the lateral switch.	37

Figure 3-3	Simulation results of S-parameters with various capacitances C_s at the open-state of the lateral switch ($R_l = 1 \Omega$, $L = 148 \text{ pH}$, $C_g = 30 \text{ fF}$).	37
Figure 3-4	Simulation results of S-parameters with various resistance sum at the close-state of the lateral switch ($L = 148 \text{ pH}$, $C_g = 30 \text{ fF}$).	39
Figure 3-5	Simulation results of S-parameters with various inductances L at the close-state of the lateral switch ($R_l = 1 \Omega$, $R_c = 1.8 \Omega$, $C_g = 30 \text{ fF}$).	41
Figure 3-6	Simulation results of S-parameters with various capacitances C_g when the switch is at the close-state ($R_l = 1 \Omega$, $R_c = 1.8 \Omega$, $L = 148 \text{ pH}$).	43
Figure 3-7	The schematic of the top view of a double-beam lateral switch.	44
Figure 3-8	The equivalent circuit of the double-beam lateral switch.	45
Figure 3-9	The schematic of the top view of an electrostatic actuator.	45
Figure 3-10	Normalized electrostatic force and restoring force on the movable cantilever beam with various applied bias voltages.	51
Figure 3-11	The shape of cantilever beam with various applied bias voltages.	51
Figure 3-12	Calculated threshold voltage V_{th} with various lengths (l_1+l_2), $l_2/(l_1+l_2)$ ratio and initial gap distance g_0 ($l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_m = 0$, $g_{Si} = 6 \mu\text{m}$).	53
Figure 3-13	Calculated threshold voltage V_{th} with various cantilever beam widths (w_1, w_2) ($l_1 = 275 \mu\text{m}$, $l_2 = 165 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $g_{Si} = 6 \mu\text{m}$, $w_m = 0$).	53

Figure 3-14	Calculated threshold voltage V_{th} with various thicknesses of Al coated at sidewalls wAl ($l_1 = 275 \mu\text{m}$, $l_2 = 165 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $g_{Si} = 6 \mu\text{m}$, $w_2 = 5 \mu\text{m}$).	55
Figure 3-15	Frequency response of a beam with resonant frequency of 15 kHz and $k = 0.94$.	57
Figure 3-16	Effective mass and part mass of the cantilever beam versus the ratio of $l_2 / (l_1 + l_2)$ ($w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.6 \mu\text{m}$, $l_1 + l_2 = 440 \mu\text{m}$ and $l_3 = 10 \mu\text{m}$, $h = 35 \mu\text{m}$).	60
Figure 3-17	Natural Resonant frequency versus the ratio of $l_2 / (l_1 + l_2)$ ($w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.6 \mu\text{m}$, $h = 35 \mu\text{m}$).	60
Figure 3-18	Time domain response of a cantilever beam with different metal coating and Q-factor ($V_{bias} = 40 \text{ V}$).	62
Figure 3-19	Time domain response for the cantilever beam with different applied voltage ($Q = 1$).	63
Figure 3-20	Simulation results of release time for the cantilever beam with different Q-factors.	63
Figure 3-21	SEM micrograph of a lateral switch with the hole-mass (G: ground, S: signal).	66
Figure 3-22	AFM micrograph showing the surface roughness of the sidewall of a cantilever beam coated with Al. Roughness = $250 \text{ \AA}$.	66
Figure 3-23	SEM micrograph of the contact point on the cantilever beam.	67
Figure 3-24	Comparison between measured and fitted S-parameters of the single-beam switch (Switch A).	70

Figure 3-25	Plot of the fitted resistance, $R_f + R_c$, of Switch A with frequency.	70
Figure 3-26	SEM micrograph of a double-beam lateral switch with the solid mass.	72
Figure 3-27	Comparison between measured and fitted S-parameters of the double-beam switch (Switch B).	72
Figure 3-28	Comparison of measured S-parameters between the single-beam switch (Switch A) and the double-beam switch (Switch B).	73
Figure 3-29	Comparison between measured and fitted S-parameters of a single-beam switch with the solid mass (Switch C, $w_1 = 2.0 \mu\text{m}$, $w_2 = 5 \mu\text{m}$).	74
Figure 3-30	Comparison between measured and fitted S-parameters of a single-beam switch with the solid mass (Switch D, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$).	75
Figure 3-31	Comparison between measured and fitted S-parameters of a single-beam switch with the hole mass (Switch E, $w_1 = 2.4 \mu\text{m}$, $w_2 = 15 \mu\text{m}$).	75
Figure 3-32	Comparison of measured S-parameters between Switch C ($w_1 = 2.0 \mu\text{m}$) and Switch D ($w_1 = 2.4 \mu\text{m}$).	76
Figure 3-33	Comparison of measured S-parameters between Switch D (solid-mass, $w_2 = 5 \mu\text{m}$) and Switch E (hole-mass, $w_2 = 15 \mu\text{m}$).	76
Figure 3-34	Comparison between measured and fitted S-parameters of switch F ($l_2 = 235 \mu\text{m}$).	77

Figure 3-35	Comparison between measured and fitted S-parameters of switch G ($l_2 = 350 \mu\text{m}$).	78
Figure 3-36	Comparison of measured S-parameters between Switch F ($l_2 = 235 \mu\text{m}$) and Switch G ($l_2 = 350 \mu\text{m}$).	78
Figure 3-37	Comparison of measured results of the single-beam switch with various thick Al coating (a) the insertion loss and the return loss, and (b) the isolation.	80
Figure 3-38	Measured S-parameters of Switch B with different switching cycles.	82
Figure 3-39	SEM micrographs of a lateral switch with separate fixed-electrode.	84
Figure 3-40	Comparison of measured S-parameters between Switch D (separate electrode) and Switch A (combined electrode).	84
Figure 3-41	Comparison of measured and calculated threshold voltage V_{th} of the lateral switch with various g_0 ($l_1 = 220 \mu\text{m}$, $l_2 = 210 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0 \mu\text{m}$).	86
Figure 3-42	Measured and calculated V_{th} with various ($l_2 / (l_1 + l_2)$) ratio with and without (w/o) Al coating ($l_1 + l_2 = 430 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $g_{Si} = 6 \mu\text{m}$).	87
Figure 3-43	Comparison of measured, calculated and simulated displacement of the free-end of the cantilever beam with $0.63 \mu\text{m}$ thick Al on sidewalls ($l_1 = 275 \mu\text{m}$, $l_2 = 165 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.63 \mu\text{m}$, $g_0 = 4.8 \mu\text{m}$, $d_0 = 2.8 \mu\text{m}$).	87
Figure 3-44	The sketch diagram of the testing setup for dynamic behavior of the lateral switch.	88

Figure 3-45	The experimental results of switching performance of a lateral switch (a) the close-state, (b) the open-state.	89
Figure 4-1	Schematic cross-sectional view of the CPW.	94
Figure 4-2	(a) vector E-field distribution, and (b) characteristic impedance of the Si-Core CPW ($S/W/G = 110/45/300 \mu\text{m}$, $h_r = 12 \mu\text{m}$, $w_r = 20 \mu\text{m}$).	97
Figure 4-3	Calculated conductor loss curves with respect to the line unit series resistance and characteristic impedance.	99
Figure 4-4	Calculated conductor loss curves with respect to the line unit shunt conductance and characteristic impedance.	101
Figure 4-5	Calculated radiation loss curves with respect to frequency and substrate permittivity.	103
Figure 4-6	Comparison of simulation results between the Si-core CPW on glass and HRSi substrate ($S/W/G = 110/45/300 \mu\text{m}$, $h_r = 12 \mu\text{m}$, and $w_r = 20 \mu\text{m}$, LRSi core) (a) attenuation, and (b) shunt conductance G .	104
Figure 4-7	Comparison of the RF properties of Si-core CPW with different core resistivity ($S/W/G = 110/45/300 \mu\text{m}$, $h_r = 12 \mu\text{m}$, and $w_r = 20 \mu\text{m}$).	105
Figure 4-8	Comparison of the distributed RLGC parameters of the Si-core CPW on glass substrate (a) capacitance and inductance, (b) conductance and resistance.	106
Figure 4-9	The schematic of cross sectional view of a Si-core CPW transmission line.	108

Figure 4-10	Simulation results of HRSi-core CPWs with various conductor thickness, T . (S/W/G = 110/45/300 μm)	109
Figure 4-11	Simulation results of HRSi-core CPWs with various undercut dimensions. (S/W/G = 110/45/300 μm)	110
Figure 4-12	SEM micrograph of a 1-mm-long Si-core CPW transmission line.	111
Figure 4-13	Comparison of the measurement and the simulation results of a HRSi-core CPW on a glass substrate ($T = 62 \mu\text{m}$, $h_r \approx 6 \mu\text{m}$, $w_r \approx 10 \mu\text{m}$ and 1- μm -thick Au coating).	112
Figure 4-14	Comparison of the measured and the simulated RLGC parameters of a HRSi-core CPW on a glass substrate (a) L and C , and (b) R and G .	113
Figure 4-15	Measured results of 1-mm-long LRSi-core CPWs on glass with different dimensions (1- μm -thick Au was coated) (a) characteristic impedance and (b) attenuation.	117
Figure 4-16	Comparison of attenuation of LRSi-core CPW on SOI and glass substrate.	119
Figure 4-17	Comparison of resistance and conductance of LRSi-core CPW on SOI and glass substrate.	119
Figure 4-18	Comparison of characteristic impedance and attenuation between the HRSi-core CPW and the LRSi-core CPW on glass.	121
Figure 4-19	Comparison of resistance and conductance between the HRSi-core CPW and the LRSi-core CPW on glass.	121
Figure 4-20	The in-line SP2T switching circuit (a) schematic diagram and (b) layout design (G: ground; S: signal; Ai-Ai': bond wires).	124

Figure 4-21	Equivalent circuits of SP2T switching circuit (a) complete transmission-line model, and (b) Lumped equivalent circuit model.	126
Figure 4-22	Simulation results of the return loss of the SP2T switching circuit using circuit model.	126
Figure 4-23	Full-wave EM simulation results of S-parameters of the in-line SP2T switching circuit with and without bond wires.	128
Figure 4-24	Surface current distribution on the in-line SP2T switching circuit with one switch open and the other switch closed.	128
Figure 4-25	The parallel SP2T switching circuit (a) Schematic diagram and (b) layout design (G: Ground; S: Signal; Ai-Ai': bond wire).	130
Figure 4-26	The single-beam SP2T switching circuit (a) Schematic diagram and (b) layout design (G: Ground; S: Signal; Ai-Ai': bond wire).	131
Figure 4-27	The SP3T switching circuit (a) schematic diagram, (b) layout design (G: Ground; S: Signal; Ai-Ai': bond wire), and (c) lumped equivalent circuit.	133
Figure 4-28	The SP4T switching circuit (a) schematic diagram, (b) layout design (G: Ground; S: Signal; Ai-Ai': bond wire), and (c) lumped equivalent circuit.	136
Figure 4-29	The in-line SP2T switching circuit (a) SEM micrograph, (b) measured and fitted results of a SPST switch on glass, (c) measured results without bond wires, and (d) measured and fitted results with three bond wire.	139

Figure 4-30	SEM micrographs (a) the parallel SP2T switching circuit, and (b) the single-beam SP2T switching circuit.	141
Figure 4-31	Comparison of the measured S-parameters of the three SP2T switching circuits.	142
Figure 4-32	Experimental and fitted results of a SP3T switching circuit (a) SEM micrograph, (b) insertion loss and return loss, and (c) isolation.	144
Figure 4-33	Experimental and fitted results of a SP4T switching circuit (a) SEM micrograph, (b) insertion loss and return loss, and (c) isolation.	147
Figure 5-1	Schematic of the fabrication process flow.	156
Figure 5-2	Schematic of the anodic bonding setup.	158
Figure 5-3	Schematic of the shear test setup.	163
Figure 5-4	Plot of measured shear strength of different samples.	164
Figure 5-5	SEM micrograph of the bonding interface region of silicon - thin film - glass bonding pair (a) Sample C and (b) Sample D.	165
Figure 5-6	Schematic top view and cross-sectional view showing the influence of the edges' orientation on the silicon etching profile (a) 0° or 90°, and (b) 45° to <110> prime orientation flat.	169
Figure 5-7	SEM micrographs showing cross section of the micromachined structures with different layout placement (a) 0° and (b) 45° to <110> prime orientation flat.	170
Figure 5-8	Experimental results of the surface roughness of silicon etched by 35 wt.% KOH at different temperatures (a) 40 °C, (b) 50 °C, (c) 60 °C, and (d) 70 °C.	172

Figure 5-9	SEM micrograph of the cross sectional view of a glass cavity after 30 mins self-aligned etching.	173
Figure 5-10	SEM micrograph of the high-aspect-ratio comb-drive actuator.	174
Figure 5-11	Fabrication process flow of the shadow mask.	176
Figure 5-12	Schematic of the cross sectional view of the shadow mask.	178
Figure 5-13	Optical photos of the shadow mask (a) the front and (b) the back.	179
Figure 5-14	Schematic of the metal deposition through a shadow mask.	181
Figure 5-15	Two methods of the usage of a shadow mask (a) the backside of the shadow mask faces the device wafer, and (b) the front side of the shadow mask faces the device wafer.	181
Figure 5-16	Optical photo of a single-beam SP2T switching circuit after Al coating through the shadow mask.	183
Figure 5-17	SEM micrograph of cross sectional view illustrating the step coverage of the metal deposition through a shadow mask using E-beam evaporation.	183
Figure 6-1	A schematic showing the wafer level packaging of the parallel SP2T switching circuit (a) Top view looking through the glass side (b) cross sectional view along A-A' and (c) cross sectional view along B-B'.	191
Figure A-1	The equivalent circuit model per unit length of the CPW.	193

LIST OF TABLES

Table 2-1	Comparison of characteristics of lateral MEMS switches.	21
Table 2-2	Comparison of characteristics between different MEMS SP2T switching circuits.	26
Table 3-1	Electrical properties of some metal materials.	39
Table 3-2	Mechanical properties of materials used in the lateral switch.	50
Table 3-3	The effect of the cantilever beam design parameters on the threshold voltage.	55
Table 3-4	Parameters of the cantilever beam for the dynamics simulations.	62
Table 3-5	Cantilever beam parameters and fitted circuit values of lateral switches at 10 GHz.	68
Table 3-6	Comparison between fitted and calculated circuit values of Switch A.	71
Table 3-7	Variation trends of switch characteristics with increase of cantilever beam parameters.	91
Table 4-1	Dielectric properties of the fabrication materials.	101
Table 4-2	Comparison of the simulated and measured attenuation contributed by the unit resistance and the conductance of the glass-based HRSi-core CPW at 20 GHz.	114
Table 4-3	Geometrical parameters of four 1-mm-long Si-core CPWs.	116

Table 4-4	Comparison of measured and fitted RLGC parameters and attenuations of Si-core CPW with different substrate materials and core materials at 20 GHz.	122
Table 5-1	Tabular sample preparation and tested average shear strength of anodic bonding.	162
Table 5-2	The etching rate and surface roughness of silicon vs. etching temperature in 35 wt.% aqueous solution of KOH.	171

CHAPTER 1

INTRODUCTION

1.1 Motivation

Wireless communication has an explosive growth in emerging consumer and military applications of radio frequency (RF), microwave, and millimeter-wave circuits and systems. These applications include wireless personal communication systems (PCS), wireless local area networks (WLAN), satellite communications, and automotive electronics (for instance, radar systems for adaptive cruise control and parking aid). Future personal hand-held communication systems and communication satellites are expected to have the characteristics of low weight and volume, small power consumption, large data bandwidth, and greater functionality. Smaller size and weight, ever increasing frequency and greater functionality call for the use of highly integrated RF front-end circuits. Continuing chip scaling has a great contribution in achieving this goal. However, as working frequencies get higher, data bandwidth gets larger, and most of all, when multiple broadband signals have to be handled in the same device, the conventional RFIC technologies face a barrier to further integration. Discrete RF components such as high-Q inductors, ceramic resonators, quartz crystal resonators, varactor diodes and mechanical switches, which are relatively bulky and expensive, have a limiting role in further reducing the circuit size. On the other hand, various RFIC technologies, including BiCMOS, silicon germanium (SiGe) and gallium arsenide (GaAs), cannot produce on-chip components with high-quality offered by these discrete components which are

Chapter 1: Introduction

required by most wireless applications. Microelectromechanical system (MEMS) [1] technology is now rapidly emerging as an enabling technology that produces small, low weight and high performance on-chip components to replace some of the bulky and expensive discrete components.

RF MEMS [2-6] refers to the design and fabrication of MEMS for RF applications, which are highly miniaturized mechanical machine with moving parts and used for switching, frequency selection, tuning and matching in the RF front-end circuits. The main components are micromachined switches, tunable capacitors, high-Q inductors, high-Q mechanical resonators and filters, micromachined transmission lines, and thin film bulk acoustic resonators (FBAR) and filters. The most widely recognized advantages of RF MEMS components are superior RF performance, tunability, and linearity over a broader range of operating frequencies compared to their electronic counterparts.

Compared to other MEMS technologies, RF MEMS is at its early stage. However, during the past 15 years we have witnessed its exponential growth due to its commercial and defense potential. The RF MEMS switch is one of the first studied devices, which can be used to replace the solid-state switches (for instance, PIN diodes and gallium arsenide (GaAs) field-effect-transistors (FETs)). The use of RF MEMS switch is particularly attractive for applications in which energy savings (either RF or DC control) are at a premium. The possible applications are from cellular phones to WLAN, including GPS-based systems, phased array antenna systems, spacecraft communications and automatic test equipment. The advantages of the MEMS switch include low power consumption, great linearity and low insertion loss with high isolation at high frequency range. The power consumption of RF MEMS switch is in the order of μW as compared

with mW of PIN diode switch. It has great linearity because the MEMS devices do not contain a semiconductor junction with the associated non-linearity. Finally, for the solid-state switches, the insertion loss generally is larger than 0.5 dB when the frequency is above 2 GHz and 1-3 dB when the frequency is from 18 to 40 GHz [7-8]. The RF MEMS switch demonstrates superior RF performance from DC-40 GHz and some designs can even work up to 100 GHz with insertion loss of 0.1 to 1 dB and isolation of above 20 dB [3].

1.2 Objectives

The main objective of this study is to develop high-performance RF switches and switching circuits using MEMS technology. The study includes both theoretical investigations and experimental implementations. It focuses on the investigation of lateral RF MEMS switches and single-pole-multiple-throw (SPMT) switching circuits implemented using Si-core coplanar waveguide (CPW) transmission lines and lateral RF MEMS switches. A low-loss single-mask substrate transfer process for the lateral switches and switching circuits on a glass substrate is implemented and discussed.

The lateral RF MEMS switches consist of a Si-core CPW transmission line and an electrostatic actuator. The movable part of the actuator is a cantilever beam with beam-mass structure. The cantilever beam moves in plane to connect the circuit by electrostatic forces or to disconnect the circuit by removing the bias voltage. The fixed electrode of the actuator can either be a part of the ground line or a separate structure. The electromagnetic modelling and design as well as the mechanical modelling and design of

Chapter 1: Introduction

the lateral switch will be presented. Experiments will be implemented to verify the modelling and the design.

The study of the switching circuits focuses on the analysis of the Si-core CPW transmission lines and the design of the SPMT switching circuits. The attenuation of the Si-core CPW due to the substrate material, core material and the process tolerances is studied thoroughly through an equivalent RLGC circuit model. Then, the SPMT switching circuits, with special focus on the single-pole-double-throw (SP2T) switching circuits, are designed using the Si-core CPW transmission lines and lateral RF MEMS switches. Bond wires are used at the discontinuities to equalize the potential of the ground plane. The experiment results are compared with the theoretical study.

A single-mask substrate transfer fabrication process is developed for the fabrication of the high-aspect-ratio suspended silicon structures on the glass substrate. The lateral switches and switching circuits are implemented using silicon back-bone structure patterned in desired shapes followed by substrate transfer from the silicon to a glass. After glass self-aligned etching to release the suspended structures, a layer of metal is coated on the structures to propagate RF signals. Key processes include silicon - thin film - glass anodic bonding, silicon thinning by aqueous solution of potassium hydroxide (KOH) etching, glass self-aligned etching and shadow mask.

1.3 Major contribution

This thesis concentrates on research related to RF MEMS. It focuses on lateral RF MEMS switches and SPMT switching circuits configured using the Si-core CPW transmission lines and lateral switches. New concepts and ideas are developed and

Chapter 1: Introduction

evaluated by experiments. An integrated fabrication process for the lateral switches and switching circuits on the glass substrate is developed. The major contributions of the thesis are listed below.

The microwave elements, including the Si-core CPW transmission lines, the lateral switches, the SPMT switching circuits, are implemented using a silicon back-bone structure which is patterned in desired shapes followed by metal overcoat. These Si-core metal coated structures can work up to 25 GHz, both theoretically and experimentally.

Lateral RF MEMS switches with different topology are designed, fabricated and characterized. The switches are formed by integrating the Si-core CPW transmission line and an electrostatic actuator on a Si-on-insulator (SOI) or a silicon-on-glass (SiOG) wafer. The movable part of the actuator is a high-aspect-ratio silicon cantilever beam which is covered by a layer of metal. The switches can have one or two cantilever beams. The fixed electrode of the actuator can either be a part of the ground line or a separate structure standing on the substrate. The prototype has a dimension of less than $800\text{ }\mu\text{m} \times 700\text{ }\mu\text{m}$. The insertion loss is below 1 dB and return loss and isolation are above 20 dB up to 25 GHz. The threshold voltage is 23 V and switching time is 35 μs . The RF life span is more than one million switching cycles.

An electrical model of the lateral switches is developed for the analysis and optimization of RF circuit design of the lateral switches. The RF performance of the lateral switches can be improved by optimizing the circuit parameters of the switches. The circuit parameters can be tuned by changing either the design of the transmission line or the cantilever beam.

Chapter 1: Introduction

A static behavior model and a dynamic behavior model are developed for the analysis and optimization of the mechanical design of the lateral switch. The static model shows that when the electrode part of the cantilever beam is within the range of 35-75 % of the total beam length, the threshold voltage has small variation. The dynamic model shows that the effective mass of the cantilever beam is 51-85 % of the actual total mass. The dynamic response is determined by the quality factor and the applied bias voltage. When the quality factor is within the range of 0.5 - 2, the lateral switch possesses a short switching and settling time. A larger applied voltage raises its switching speed.

Si-core CPW transmission line has been studied thoroughly. The attenuation related to the substrate materials, core materials and process tolerances are analyzed using the RLGC model. The experimental results show that the loss is mainly dominated by the conductor loss. The surface metal is coated as thick as possible to reduce the conductor loss. A glass substrate is more favorable compared to a silicon substrate. A silicon core with high resistivity is better than the one with low resistivity. The experimental results also shows that the Si-core CPW transmission line supports quasi-TEM mode propagation up to 25 GHz with attenuation of less than 4 dB/cm.

Three single-pole-double-throw (SP2T) switching circuits are designed, fabricated and characterized. An equivalent circuit model is introduced for design and analysis of the circuits. An in-line SP2T switching circuit with two cantilever beams in line is studied thoroughly through circuit analysis and EM simulation. The EM simulation and experimental results of the in-line SP2T switching circuit shows that bond wires are

Chapter 1: Introduction

essential to suppress the parasitic slot line mode since many discontinuities exist in the ground planes of the SPMT switching circuits. The in-line SP2T switching circuit with three bond wires has an insertion loss of less 1 dB at 20 GHz. Additionally, the parallel SP2T switching circuit with two cantilever beams arranged in parallel shows the lowest insertion loss of below 1 dB at 22 GHz. The single-beam SP2T switching circuit with one cantilever beam to move in two directions has the smallest circuit size of 0.92 mm^2 .

A single-pole-three-throw (SP3T) and a single-pole-four-throw (SP4T) switching circuit are designed, fabricated and characterized. The SP3T switching circuit has an insertion loss of 0.7 dB at 15 GHz. The return loss is 17 dB at 15 GHz. The isolation is larger than 20 dB up to 20 GHz. The SP4T switching circuit, on the other hand, has an insertion loss of less than 1 dB at 10 GHz. Both the return loss and the isolation are higher than 22 dB at 10 GHz.

A single-mask substrate transfer fabrication process is developed for the lateral switches and the switching circuits on a glass substrate. The silicon back-bone structures are patterned in desired shapes by a silicon deep reactive ion etching (DRIE) process. Then, the silicon back-bone structures are transferred from the silicon substrate to a glass substrate using Si-thin film-glass anodic bonding followed by silicon thinning using the grinding/ polishing process and KOH wet etching. Next, the structures are released by glass self-aligned etch. Finally, a layer of metal is coated on the circuits through a shadow mask. The main advantages of this integrated process are high-aspect-ratio, low loss and low cost with high flexibility.

Chapter 1: Introduction

Key processes which include Si-thin film-glass anodic bonding, Si thinning by KOH etching, glass self-aligned etching and shadow mask are discussed in detail. Based on the analysis of the Si-thin film-glass anodic bonding mechanism, thermal oxide and SiON are chosen as the intermediate layer of the Si-thin film-glass anodic bonding because these materials are found to provide sufficient bonding strength with shear strength larger than 11 MPa for the grinding and polishing process. These materials also have strong resistant to KOH etching. In terms of the etching rate and surface roughness, the aqueous solution of KOH with concentration of 35 wt.% at 40 °C has been selected thin the silicon wafer, which provides smooth etching surface. Based on the analysis of the crystallography dependent etching of the silicon in the KOH etching, the device layout is adjusted to be 45° to the <110> prime wafer flat in a (100) silicon wafer for flat etching surface on the top of the device. The glass is etched through the silicon pattern of the device layer directly to release the movable structures. This process is mask-less and self-aligned. High-resolution shadow mask is developed by etching an open window from the front using the silicon DRIE process, followed by KOH etching-through process from the backside.

1.4 Organization

This thesis is organized into six chapters. Chapter 1 provides the motivation, the objectives, and the major contributions of the thesis. The motivation part explains why the PhD project is to be carried out. The objective states the main focus of my research. And the contribution part lists out the findings and innovations of this thesis.

Chapter 1: Introduction

Chapter 2 reviews literatures related to the present work. Concentration is focused on RF MEMS switches, RF MEMS switching circuits and high-aspect-ratio suspended structures fabrication processes and the glass etching techniques. It provides a background of the research.

Chapter 3 covers the design, modelling and experimental verification of the lateral RF MEMS switches. Both the RF circuit and the mechanical modelling and their respective designs of the lateral switches are presented. The experiments are used to verify and evaluate the modelling and the design.

Chapter 4 focuses on the analysis of the Si-core CPW transmission lines and the design of the SPMT switching circuits. Attenuation of the Si-core CPW due to the substrate materials, the core materials and the process variations are analyzed. Then, the SPMT switching circuits are designed using the Si-core CPW transmission line and the lateral RF MEMS switches with special emphasis on the SP2T switching circuits. The experiment results are compared to the theoretical study.

Chapter 5 presents a simple single-mask substrate transfer process for the fabrication of the high-aspect-ratio suspended silicon structures. The key fabrication processes which include silicon-thin film-glass anodic bonding, the silicon thinning using aqueous solution of KOH, the self-aligned wet etching of the glass, and the fabrication and usage of the shadow mask are discussed.

Chapter 6 concludes by highlighting the major contributions of this PhD project. This chapter also provides some recommendations on the future works.

Chapter 2

Literature Review

This chapter provides an overview of the RF MEMS switches, switching circuits, the fabrication processes of the high-aspect-ratio suspended silicon structures and the glass etching techniques. Section 2.1 reviews literature related to RF MEMS switches, including some basic principles and configurations of different types of vertical switches and lateral switches. The advantages, current limitations and possible opportunities of the lateral RF MEMS switches are also discussed. Section 2.2 focuses on the discussions of the RF switching circuits with special emphasis on the single-pole-multiple-throw (SPMT) switching circuits. Section 2.3 discusses various fabrication processes of the high-aspect-ratio suspended silicon structures, including their respective advantages and limitations. Finally, Section 2.4 introduces different glass etching techniques with emphasis on the wet etching methods.

2.1 Review of RF MEMS Switches

Microelectromechanical system (MEMS) is a technology that enables batch fabrication of miniature structures, devices, and systems, which combines the electrical and mechanical functions [1]. Like CMOS technology, MEMS encompasses design and simulation tools and methodology, process technology and packaging. When applying MEMS components to high-frequency circuits (for instance, radio frequency (RF),

Chapter 2: Literature Review

microwave or millimeter wave), the technology is commonly referred as RF MEMS [2]. RF MEMS components that are currently under development in laboratories around the world include RF switches, voltage-tunable capacitors, high-Q micromachined inductors, film bulk acoustic resonators (FBAR), micromachined resonators and filters. RF MEMS can be used for switching and frequency selection in the RF and IF filtering stages, tuning and matching in the RF front-end in heterodyning communication transceivers and further. The main advantages of the RF MEMS components compared to other RF technologies are miniaturization, low manufacturing cost and performance enhancement [2-6]. In this section, the recent research and development in RF-MEMS switches is discussed.

High frequency switches are essential elements in a variety of communication systems operating in the microwave regime, for instance in mobile phones and wireless local area networks (WLAN), and in the millimeter wave regime, for instance in the automotive radar, missile and satellite communication systems. The switches are used in wireless communications and radar systems for switching between the transmit (Tx) and receive (Rx) paths, for routing signals to the different blocks in multi-band/multi-standard phones, for RF signal routing in phase shifters used in phased array antennas, and much more. The main performance characteristics of an RF switch are the insertion loss in the on-state, the isolation in the off-state, the return loss in both of the on and off state, the power consumption, the bandwidth, the linearity, the power handling and the switching speed. Currently, the majority of RF switches are PIN diode [7] and GaAs FET [8-10] - based semiconductor switches. They demonstrate fast switching speed, but are restricted by high power consumption (in particular for PIN diodes). Some of them also introduce

Chapter 2: Literature Review

significant losses (in particular for FETs) as frequency is above several GHz. Moreover, the non-linear characteristics of these semiconductor switches are extremely undesirable for the non-constant envelope modulation scheme used for the 3rd generation mobile phones. RF MEMS switches [11] offer great potential benefits compared to semiconductor switches in terms of high isolation, in particular at high frequencies (> 30 GHz) and low loss over a wide frequency range (compared to FETs at the higher frequencies), extremely low standby power consumption (compared to PIN diodes) and excellent linearity characteristics [12-14]. Other advantages include the integration capability with other high – quality passives (for instance high – Q inductors, tunable capacitors and tunable filters) and the flexible choice of the substrate. Drawbacks remain the rather high driving voltage and the relatively slow response. In short, RF MEMS switches are not suitable for every problem and every application, but these switches definitely offer great potential benefits for a wide range of applications.

2.1.1 Basic principles and configurations of RF MEMS switch

RF MEMS switch is a switching device that is fabricated using the micromachining technology, where the switching between the on- and off- states is achieved via the mechanical displacement of a freely movable structure. The displacement is induced by a microactuator. Various actuation mechanisms then exist, including electrostatic [15-17], electrothermal [18], magnetostatic [19] and electromagnetic [20-24] means. Most often, the RF MEMS switch relies on electrostatic actuation, which is based on the attractively electrostatic force existing between charges of opposite polarity. An electrostatic drive offers extremely low power consumption since power is required only during switching. The other advantages of using electrostatic

Chapter 2: Literature Review

actuation are its simple fabrication technology, compared to electromagnetic excitation, the high degree of compatibility with a standard IC process line, and its ease of integration with planar and microstrip transmission lines. For many applications, the main drawback is to overcome the high driving voltage. When the available supply voltage is limited, for instance within the range of 3 to 5 V in handheld phones, on-chip high-voltage generators [25] may be incorporated either monolithically or in a hybrid fashion [26].

From a functional point of view, two pairs of electrodes are identified irrespective of the actuation mechanism. One pair, the actuation electrodes, is used for the DC actuation signal and the other, the switching electrodes or contacts, for the RF signal. The two pairs can be insulated from each other resulting in a four-terminal configuration. Sometimes a common ground is used, in which case a three-terminal device results. Or, the RF and DC bias signals share the same control lines, in which case two-terminal configuration results. A drawback of the switch with two or three terminal configuration is that it requires biasing elements, like blocking capacitors and choke inductors, to decouple the RF signal from the DC actuation signal, like PIN diode switches [27]. For a switch with four-terminal configuration, biasing elements are not needed, but the fabrication process is more complex as insulating layers are required as part of the armature to insulate the DC lines from the RF signal lines.

RF MEMS switches can be used in series mode, with the actuated state of the device passing the signal, or in shunt mode, with the actuated state terminating a transmission line by shorting it to ground. The contacts for RF switching can either be resistive contacts or capacitive contacts. Resistive contacts are implemented as metal-to-

Chapter 2: Literature Review

Figure 2-1 (a) The schematic of a shunt switch circuit configuration, (b) SEM micrograph and (c) schematic cross sectional view of a vertical capacitive shunt switch [28-31].

Figure 2-2 The schematic illustration of (a) a series switch circuit configuration, (b) top view, (c) cross sectional view along A-A' and (d) cross sectional view along B-B' of a vertical metal-contact series switch [46].

Chapter 2: Literature Review

metal direct contact, whereas in a capacitive contact, a thin dielectric film is used between the two metallic contact surfaces. The resistive contact allows the device to be used for low-frequency applications including DC, as well as high-frequency applications. The capacitive contact is only suitable for high-frequency applications (e. g. > 5 GHz). A capacitive shunt switch and a metal-contact series are schematically illustrated in Figure 2-1 and Figure 2-2, respectively.

The RF MEMS switches can be classified as vertical switches and lateral switches based on its motion direction of the switching structure. The vertical switches perform out of wafer plane displacement and surface contact. The lateral switches perform in wafer plane displacement and sidewall contact. The vertical RF MEMS switches are usually fabricated using surface micromachining process and metal is used as its structural material. On the other hand, the lateral RF MEMS switches are usually fabricated using bulk micromachining process and single-crystal-silicon or polysilicon is used as its structural material. Most RF MEMS switches which were developed in last decades are vertical switches due to their excellent RF performance. However, the lateral switches have shown some promising performance in dynamics and fabrication processes are simpler compared to its counterparts. As such, recent research interest has been attracted toward the lateral switches. In the next two sections, the vertical and lateral switches are introduced.

2.1.2 Vertical RF MEMS switches

Many vertical RF MEMS switches have been developed. Among all, two types of these vertical switches stand out. They are electrostatically actuated capacitive shunt switches [28-45] and electrostatically actuated resistive series switches [46-63].

Chapter 2: Literature Review

The capacitive shunt switch implemented on a coplanar waveguide (CPW) transmission line was reported in 1995 [28-29] and subsequently a modified one was published in 1998 [30-31], as shown in Figure 2-1. Since then, a number of switches based on this design have been developed and tested by several different research organizations [32-45]. This RF-MEMS capacitive shunt switch consists of a suspended movable metal bridge, which is mechanically anchored and electrically connected to the ground of the CPW. In operation, the DC control voltage and RF signal are superimposed and applied to the signal line. At the on-state, the bridge is up, hence the switch capacitance is small, on the order of 10-100 fF, and hardly affects the impedance of the line. At this state, the RF signal is allowed to pass through freely. At the off-state, when a DC bias voltage is applied, the bridge is pulled down onto a dielectric layer placed locally on top of the signal line. The switch capacitance becomes high that is between 1 to 10 pF, causing an RF short to ground. A high down-capacitance at its off-state and a small up-capacitance at its on-state are desired to obtain high isolation and low loss in the off- and on- state respectively.

The resistive series switch was first published in 1995 [46], as shown in Figure 2-2. Since then, the design has been improved and adapted for specific applications [47-50]. Based on this design, a number of resistive series switches have been developed [51-61]. In the resistive series switches, the signal line is interrupted. The armature is composed of a dielectric film with locally portions of metal for the switching contacts and the actuation electrode. The armature consists of a cantilever beam, but doubly-supported structures (like a bridge) are also possible [62-63]. In the absence of a DC voltage, the armature is up and the RF input is only weakly coupled to the RF output via a small

Chapter 2: Literature Review

capacitance. When sufficient DC bias is applied, the armature is pulled down which closes the contact. The signal line is now shorted between the input and the output. The switch is at its on-state. The contact resistance of the electrical contacts must be as small as possible to minimize losses.

The vertical RF MEMS switches demonstrate excellent RF performance. However, some drawbacks remain. First, the fabrication process using surface micromachining technology is relatively complicated. The transmission line, the dielectric layer, the bridge or armature, and the contacts are patterned and processed separately. Four to nine masks are needed in this fabrication process. Second, mechanical properties such as Young's modulus and residual stress of the switching structures (bridges or armatures) may be different locally depending on the fabrication processes [64]. The switching structures tend to deform by an internal stress gradient or by thermal effects arising from the fabrication process [65]. It is difficult to planarize the switching structures [66-67]. As a result, there is significant discrepancy between the designed threshold voltage and the experimental result. And the switch may be unusable. Third, the switching structure tend to stick to the underneath electrode during the wet-release process due to surface stress. Dry release process using the reactive ion etching can be used to solve this problem. However, it is difficult to remove the sacrificial material completely and keep a smooth contact surface in the dry release process. As a result, the contact of the vertical switch is affected and the down-state capacitance of the shunt switch is reduced [67]. Therefore, the isolation of the switch is degraded. All these shortcomings cause the disparity of the vertical switch performances and the degradation of the fabrication yield.

2.1.3 Lateral RF MEMS switches

The lateral RF MEMS switches perform in wafer plane displacement and sidewall contact. The lateral switches have the benefit of co-fabrication. The movable switching structure, the contacts, the transmission line, and the support structures can be fabricated in a single lithographic step. Besides, the actuator design is more flexible. It is easy to get a mechanical force in opposing directions even when electrostatic designs are used. The lateral RF MEMS switches can use different materials as the structure materials, for instance, nickel, polysilicon and single-crystal-silicon. To date, three main types of lateral switches have been reported. All of them are the resistive series switches.

The first type of lateral switch is the comb-drive or cantilever beam actuated lateral switch which uses electroless plated nickel as its structure material [68-69]. The schematic illustration of a comb-drive actuated lateral switch [68] is shown in Figure 2-3. In the plating process, the nickel height is restricted to 10 - 50 μm and the smallest possible width is limited to 5 μm . The actuation voltage is within the range of 35 to 150 V. The contact resistance is 5 - 20 Ω . No RF performance has been reported.

Figure 2-3 The schematic illustration of a comb-drive actuated lateral switch fabricated using nickel surface micromachining process (a) top view and (b) cross sectional view [68].

Chapter 2: Literature Review

Figure 2-4 The schematic illustration of a thermally actuated lateral switch (a) 3D view and (b) cross sectional view [77].

The second type of the lateral switch is the electrothermally or electrostatically actuated switch using polysilicon as the structure material [70-79]. The electrothermally actuated switch has been demonstrated RF performance up to 50 GHz [77-79], as shown in Figure 2-4. The switch utilizes a parallel six-beam thermal actuator which requires actuation voltage of 2.5 – 3.5 V. The mechanical structures are fabricated using 2- μm polysilicon surface micromachining process and four masks. Silicon nitride is used as a structural connection to isolate the RF signal and the DC bias. 0.3 - 0.5 μm of gold is deposited on the polysilicon to form a transmission line and contact bumps. The switch has an isolation of -20 dB at 40 GHz. The insertion loss is -0.1 dB at 50 GHz after de-embedding the substrate effect and -1.0 dB before de-embedding the substrate effect. The switching - on time is 300 μs . Although this type of lateral switch has exhibited high RF performance and low actuation voltage, the drawbacks are the complicated fabrication process, the high power consumption due to the thermal actuation, the slow switching speed and the fragile switching structure.

Figure 2-5 The schematic illustration of an electrostatically actuated lateral switch (a) top view and (b) cross sectional view [80].

The third type of the lateral switch is an electrostatically actuated switch using single crystal silicon as its structural material [80-82] and fabricated using a single-mask bulk micromachining process. The electrostatic actuator can either be a comb-drive or a cantilever beam. The switching structures are fabricated using deep reactive ion etching (DRIE) process on silicon-on-insulator (SOI) wafer. The metal contact is realized by depositing a thin layer of metal directly on the entire surfaces of the switch structures, as shown in Figure 2-5. Compared to other RF MEMS switches, the fabrication process of this type of lateral switch is the simplest. Single crystal silicon has negligible biaxial stress and vertical stress gradient, and superior thermal characteristics. Adapting a silicon process in fabricating the lateral switch can reduce the deformation of the switch structure caused by either the thermal effects or the stress gradients. As a result, the third type of lateral switch can provide better mechanical characteristics. However, most of the time, this lateral switches can only work at DC. To investigate the possibility of this lateral switch to work at the high frequencies, the literature survey is extended to the RF

Chapter 2: Literature Review

Table 2-1 Comparison of characteristics of lateral RF MEMS switches.

References	[68]	[77]	[80]	[82]	This work
Actuation mechanism	Electrostatic	Thermal	Electrostatic	Magnetic+ Electrostatic	Electrostatic
Structure material	Nickel	polySi	Silicon	Silicon	Silicon
Power consumption	μW	18 to 99 mW	μW	11.3 nJ/cycle	μW
Frequency (GHz)	DC	DC to 40	DC	DC	DC-25
Insertion loss (dB)	-	0.1	-	-	0.1 to 1.0
Return loss (dB)	-	-	-	-	22
Isolation (dB)	-	20	-	-	22
Switching Voltage (V)	35 to 150	2.5 to 3.5	50 to 260	10	23.3
Contact resistance (Ω)	5 to 20	0.1 to 0.3	1000	2 to 8	1 to 2
Switching speed (μs)	-	300	30	100 (close) 20 (open)	36
Size (mm^2)	-	0.8 x 0.34	> 1.2 x 0.6	> 2 x 2	0.8 x 0.4

behaviour of the non-solid-metal-core structures which consist of metal-coated structures with non-metal material as the core. A metal-coated silicon-core high-aspect-ratio transmission line was developed in 1995 [83] and subsequently an improved one in 1998 [84-85]. The transmission line is fabricated by a Single Crystal Reactive Etching and Metallization (SCREAM) process. It consists of pairs of parallel-plate waveguide formed from two deep (150 μm) suspended single crystal silicon beams with 0.5- μm -thick metal

coating on the sidewalls. The attenuation is less than -0.18 dB/cm at 10 – 50 GHz. A step impedance filter and a continuous microactuated phase shifter have been realized using this transmission line [83-85]. High - Q inductors with polysilicon as the core material and copper as the surface metal have been demonstrated in [86]. The spiral structure of an inductor is formed using polysilicon surface micromachining process and is suspended over a 30- μ m-deep cavity in the silicon substrate beneath. Copper is electrolessly plated onto the polysilicon spiral to achieve low resistance. High quality factors (Qs) over 30 and self-resonant frequencies higher than 10 GHz have been achieved. It is expected that the lateral switch using the metal-coated silicon-core structures may work at high frequencies when the device is designed properly. Table 2-1 compares the characteristics between different lateral switches and this work.

2.2 RF MEMS Switching Circuits

Integrating RF switches in a transmission line network forms a RF switching circuit, such as a single-pole-multiple-throw (SPMT) switching circuit, a tunable filter, and a phase shifter. This section focuses on the literature review of the RF MEMS SPMT switching circuits, which are used to switch RF signals between different destinations. The SPMT switching circuits are the key components in transmitting/ receiving (T/R) circuits, switchable filters, reconfigurable antennas, and switching matrixes, etc. In the SPMT switching circuit, a total of m switches are incorporated in a $(m+1)$ port junction device. When a SPMT switching circuit works, one switch is closed and the remaining $(m-1)$ switches are open.

The major part of SPMT switching circuits is the single-pole-double-throw (SP2T)

Chapter 2: Literature Review

Figure 2-6 Six types of SP2T switching circuits (a) 1st type [87-88], (b) 2nd type [89], (c) 3rd type [91], (d) 4th type [92], (e) 5th type [93], and (f) 6th type [94].

Chapter 2: Literature Review

switching circuit. So far, six types of RF MEMS SP2T switching circuits have been developed. The first type is the most common one with two capacitive shunt MEMS switches placed a quarter wavelength from the center of the T - junction [87-88], as shown in Figure 2-6 (a). When one switch is actuated, the virtual RF short is transformed to an open at the T-junction thus blocking almost all the signal from passing to that port. An insertion loss of 0.81 dB and an isolation of 20.3 dB at X-band, and an insertion loss of 0.43 dB and an isolation of 28.7 dB at K-band have been demonstrated. A pull-in voltage of 9 V is achieved through changing the shape of the beam. The second design is a monolithic SP2T MEMS switching circuit [89-90], which places two MEMS resistive series switches at two output armatures to operate in a 2.3 GHz diversity antenna, as shown in Figure 2-6 (b). This switching circuit has an insertion loss of 0.2 dB and an isolation of 50 dB from DC to 4 GHz. The pull-in voltage is 30 V and the switching time is 20 μ s. The mechanical life span is 10^9 switching cycles. The third design is a Ku-band SP2T switching circuit based on the toggle switch [91], as shown in Figure 2-6 (c). Two toggle switches are perpendicular to each other where both have fixed connections with a flexible metal band to two output ports. If one toggle switch is on, the switch can be connected to the input port and the signal is routed to the output port. This SP2T switching circuit exhibits the insertion loss of 0.96 dB and the isolation of 30 dB from 7 to 20 GHz. The switching voltages are 30 V to close and 35 V to open. The fourth design is a double cantilever-beam MEMS switching circuit developed for wireless applications, as shown in Figure 2-6 (d). Two beams are controlled by a single actuation electrode. An RF performance with 50 dB isolation below 5 GHz and < 0.18 dB insertion loss up to 30 GHz was observed [92]. The fifth design is a 35-60 GHz SP2T MEMS switching circuit

Chapter 2: Literature Review

[93] in which two resistive series switches are placed at the end of each output line and a short-ended $50\ \Omega$ line is connected at the cross-junction, as shown in Figure 2-6 (e). When one switch is actuated, the open-ended line formed by the open-state of the switch and the short-ended line comprises double resonance pair which transform to be open at the cross-junction. This circuit presents the insertion loss below 1 dB and the isolation higher than 19 dB from 35 GHz to 60 GHz. The actuation voltage is 35 V. All SP2T switching circuits mentioned above use vertical MEMS switches. Only one lateral SP2T MEMS switching circuit was reported for satellite based communications [94], as shown in Figure 2-6 (f). It uses thermal actuated lateral MEMS switch fabricated by silicon deep reactive ion etching (DRIE) process. The microstrip transmission is fabricated on a glass wafer separately. The two wafers are bonded together and the device is packaged using an alumina cavity package, with DC and RF contacts on opposite sides. The isolation of this SP2T switching circuit is better than 50 dB at 1 - 6 GHz. The insertion loss is 1 dB at 2 GHz and 1.7 dB at 6 GHz. Table 2-2 compares characteristics of different types RF MEMS SPDT switching circuits.

There is very limited work on other single-pole-multiple-throw switching circuits. A single-pole-three-throw (SP3T) switching circuit has been implemented in hybrid form where three cantilever beams are micromachined separately and then integrated on an alumina substrate using flip-chip technology [95]. It exhibits the insertion loss of 0.5 dB at 16 GHz and the isolation of 20 dB at 18 GHz. A SP3T switching circuit is proposed in [96], where the circuit consists of three resistive series switches based on fixed-fixed beam architecture in a coplanar environment. A single-pole-four throw (SP4T) switching circuit using four series switches is built in [97], which shows good match up to 20 GHz

Chapter 2: Literature Review

Table 2-2 Comparison of characteristics between different MEMS SP2T switching circuits.

References	[87]	[87]	[88]	[89]	[91]	[93]	[94]	[95]	This work
Actuation mechanism	ES	ES	ES	ES	ES	ES	ES	Therm	ES
Frequency (GHz)	8 to 12	18 to 26	26 to 40	DC to 15	12 to 18	DC to 30	35 to 60	1 to 6	0.05 to 20
Insertion loss (dB)	0.81	0.43	0.3	0.1 to 0.2	0.96	0.18	0.5 to 1	0.2 to 1.7	0.2 to 0.9
Return loss (dB)	-	-	40	-	17	30	10 to 24	-	16.3 to 33
Isolation (dB)	20.3	28.7	30	40	30	50	19 to 26	50	65 to 26
Switching Voltage (V)	9	9	-	30	30/on 35/off	15	35	3	23
Switching speed (μs)	52 /on 213 /off	-	-	20	-	60	-	-	35
Size (mm ²)	17.4	4.4	-	-	-	-	2	64	1.48

*ES – Electrostatic; Therm – Thermal

with an isolation of 50 dB at 10 GHz. A single-pole eight-throw (SP8T) switching circuit using the rotary switch is reported recently, which has an insertion loss of 2.16 dB and an isolation of 31 dB at 20 GHz [98].

2.3 Fabrication Process of High-Aspect-Ratio Suspended Structures

High-aspect-ratio (HAR) suspended silicon structures are extensively used in MEMS devices, such as comb-drive actuators, inertial sensors, and RF MEMS devices. The aspect ratio is defined as the maximum depth of a trench (or a wire) divided by the

Chapter 2: Literature Review

width of the trench (or the wire). High aspect ratio is always desirable to provide sufficient lateral capacitance, to increase the sensitivity of the sensor and to suppress the out-of-plane motion. The width of the high-aspect-ratio suspended structures is commonly within the range of 1 μm to 20 μm . The depth is commonly larger than 20 μm .

It is usually very difficult to realize thick structures with high-aspect-ratio using surface micromachining technology. In 1992, the so-called SCREAM (Single Crystal Reactive Etching and Metallization) process was developed to form a MEMS structure with thickness of 20 μm and aspect ratio greater than 10 on silicon wafer [99-100]. In SCREAM process, the reactive ion etching (RIE) process is used to form high-aspect-ratio structures. Then, a thin layer of silicon dioxide (SiO_2) is deposited to protect the sidewalls of the silicon structures. Next, the SiO_2 is etched to expose the silicon at the bottom of the trench. The movable structures are released by a silicon isotropic etching. Finally, the metal is deposited. SCREAM process is a low-cost process, where only a normal silicon wafer and single mask are required. However, this process has two major shortcomings. First, the etching depth of the structures varies with the trench width of the structures due to the aspect-ratio-depending-etching (ARDE) effect of the RIE. Wide trenches are normally etched deeper than the narrow trenches. ARDE effect can be avoided when the etching trenches are designed to be highly uniform. However, it is very difficult to realize in the real device design. Second, the release process sacrifices some silicon of the structures and results in irregular shape at the bottom of the silicon structures. Silicon-on-insulator (SOI) based process can avoid those problems well. In the SOI wafer, the device silicon layer with uniform thickness is separated from the handle silicon layer by a buried oxide layer. After deposition and patterning of the hard mask –

Chapter 2: Literature Review

generally SiO_2 , the device layer is etched via DRIE to form high-aspect-ratio structures. Then, the movable structures are released using wet etching of the buried oxide or DRIE over-etching [101-102]. A glass substrate is more desirable than a silicon substrate for high frequency applications, such as radio frequency integrated circuits (RFIC) and RF MEMS devices, because of its low substrate loss characteristic [103-104]. The straightforward method to construct devices or circuits on the glass substrate is to first build RF circuits on a silicon wafer or a SOI wafer, and then transfer them to a glass substrate [103]. Bulk silicon dissolved wafer process is developed in such a way to fabricate 1-25 μm thick movable devices on a glass substrate, in which device structures are etched on a silicon wafer and heavily boron doped, then the silicon wafer is anodically bonded to a glass followed by the silicon dissolving to leave heavily boron doped devices attached to the glass substrate [105]. However, it is difficult to fabricate thick MEMS structures using the silicon dissolved wafer process due to the limitation of the diffusion process. The typical diffusion time is 15-20 hours for a diffusion depth of 15-20 μm . In order to supply thick device silicon layer ($> 30 \mu\text{m}$) on the glass, the conventional SOG process is widely used [106-108]. In the conventional SOG process, some shallow trenches are etched in a glass wafer or the backside of a silicon wafer first. After the silicon wafer is anodically bonded to the glass wafer, the silicon wafer is thinned from the backside using either mechanically grinding/ polishing or chemically etching. Then, the device structures' patterns are aligned to the shallow trenches via a double-side alignment, followed by the formation of the high-aspect-ratio structures by etching through the silicon layer via DRIE process. The SOG-based process is more flexible compared to the SOI-based process. The thickness of the silicon layer can be

Chapter 2: Literature Review

adjusted freely. Additionally, high resistivity silicon can also be chosen as the device layer. Besides, the glass substrate exhibits lower loss than the silicon substrate at RF and microwave frequencies range. Therefore, SOG-based process is more favorable for the RF MEMS applications. However, the conventional SOG-based process has three shortcomings. First, the Si-glass stack always bows or warps after anodic bonding due to residual stress of the bonding. Therefore, lithography resolution, double-side alignment and yield are restrained. Second, since the glass is a poor thermal conductor, the substrate temperature ramps rapidly during the DRIE process. Therefore, it worsens the DRIE etching quality of the silicon high-aspect-ratio structures. Third, since glass is an insulating material, the notching effect is strong. The notching effect can be reduced using low frequencies ionization (380 kHz) in the high-density inductively coupled plasma (ICP) etch tool through the removal of the accumulated charges on the insulating surfaces. The notching effect can also be reduced by depositing and patterning a layer of metal on the glass or the silicon before anodic bonding [109]. However, when the etching structures are deep ($\sim 100\ \mu\text{m}$) and over-etching is long, the structures can still be damaged by the notching effect.

2.4 Glass Etching Techniques

Glass is a popular construction material in MEMS technologies due to its inertness, stability and transparency at certain wavelengths. Because of its low dielectric losses, glass is also attractive as a substrate for RF applications. Silicon wafers with RF devices fabricated using IC and micromachining technology are bonded to planar glass wafers whereupon silicon is being partly removed [105]. This, so called substrate transfer

Chapter 2: Literature Review

technology, allows gaining all advantages of low losses in glass at RF frequency range, still utilizing silicon technology for device application. Bonding of 3D – structured glass substrate to a core RF silicon wafer with wafer-to-wafer electrical interconnects may enable realization of a variety of novel RF structures (high-Q passives, transmission lines, suspended ground planes, integrated antenna, on-chip shielding, RF MEMS switches, etc.) and represents a truly added value to the concept of wafer-level chip-scale packaging. Shallow and deep recesses in glass wafers are usually required for release or protection of RF MEMS structures. Several methods have been used to structure silicon-bondable glasses. They are summarized below.

Wet etching of glass using chromium (Cr) + gold (Au) + photoresist as the etching mask is commonly used [110-112]. A chromium layer is used to improve the adhesion of gold to glass. Even though this method is simple and compatible with standard lithography techniques, this type of mask cannot be used to etch large depths as the pin-holes appear early. Additionally, it is observed that a large lateral under-etching of the chromium appears. By heating the substrate before and after the mask deposition, the lateral under-etching can be reduced [113]. The drawbacks of this method are poor adhesion to substrate and bad resistance to the HF aqueous solution, which limit its utilization to shallow glass etching.

Deep etching of borosilicate glass using a polysilicon (polySi) thin film mask deposited by LPCVD has been reported [114]. The LPCVD polysilicon mask can be used to etch through a Pyrex glass wafer with thickness of 500 μm . This method is compatible with the standard lithography techniques and no under-etching (except the one which is isotropically induced, for instance, one time etching depth) is generated. The drawback of

Chapter 2: Literature Review

this method is that the Na^+ ions diffuse out of the glass and contaminate the furnace during the high temperature LPCVD deposition process. The electrical characteristics of silicon are then seriously degraded by this contamination. A similar method using PECVD silicon carbide as mask has also been reported in [115].

Deep wet etching of borosilicate glass using an anodically bonded silicon substrate as mask has been report in 1998 [116]. The mask layer is a silicon wafer which is previously microstructured in the aqueous solution of KOH and anodically bonded to a Pyrex glass wafer. This method is compatible with the standard lithography techniques and can be used to etch the entire glass wafer. However, since KOH etching forms inclined walls and has poor uniformity through the whole wafer, the drawbacks of this method are poor accuracy of pattern and difficulty of layout design.

Other methods such as powder blasting [117], laser drilling [118] and mechanical drilling [119] can also be used. These methods enable to obtain straight walls in glass wafer. However, critical dimensions and roughness of etched surface is sometimes insufficient for RF applications.

2.5 Summary

In summary, this chapter provides a review of literature on works related to RF MEMS switches, single-pole-multiple-throw switching circuits, fabrication processes of high-aspect-ratio suspended silicon structures and glass etching techniques. It shows that the fusion of MEMS and RF does not only improve RF performance with low insertion loss, high isolation and low power consumption, but also leaves a broad space for the improvement in the device design and process development.

CHAPTER 3

LATERAL RF MEMS SWITCHES

The objective of this chapter is to study the lateral RF MEMS switch. The switch connects/ disconnects the RF circuit by in-plane motion of a cantilever beam. Compared to other electrostatic actuators, e. g., comb-drive, torsional actuator and rotary actuator, the cantilever actuator has smaller structure and is easier in achieving large actuation force. The silicon-core CPW is employed to configure the switch, which enables easy series and shunt elements connection without metal filled via holes. The main advantages of the lateral switch are reliable mechanical performance and simple fabrication process.

This chapter is organized as follows. First, the RF design, circuit modelling and simulation of the lateral RF MEMS switch are presented. The RF performance of the switch can be improved by optimizing the electrical parameters of the switch. The electrical parameters can be tuned by changing either the design of the transmission line or the cantilever beam. Second, the mechanical design and optimization of the cantilever beam of the lateral switch are discussed. The analytical solution of the threshold voltage of the cantilever beam is provided. The dynamic responses, such as switching time and release time of the switch are studied. Finally, the experimental results of the lateral switch on its insertion loss, return loss, isolation, threshold voltage, switching speed are discussed. Comprehensive modelling and design of the lateral switch are verified by extensive experiments of both electrical and mechanical characteristics.

3.1 Electrical Design and Simulation

As a controlling device in a signal route, RF MEMS switch is desired to be as non-invasive as possible. Several figure-of-merits are used to evaluate the degree of invasiveness of the switch, including the insertion loss, the return loss and the isolation. Their definitions, which are widely accepted in the RF MEMS community, are as follows.

The insertion loss of an RF switch is the RF loss dissipated in the device, typically characterized by S_{21} between the input and output of the switch in its pass-through state, which is the closed state for a series switch. The return loss of an RF switch is the RF loss reflected back by the device. This is characterized by S_{11} at the input of the switch in its pass-through state. The isolation of an RF switch is the RF isolation between the input and output, which is characterized by S_{21} of the switch in its blocking state, which is the open state for a series switch [2].

In the RF MEMS community, the insertion loss, the return loss and the isolation can also be represented by the absolute values of the corresponding S-parameters of the switch. To simplify the description in this thesis, these parameters will be represented using their corresponding S-parameters directly in the figures and using the absolute values of S-parameters in the descriptions.

The main contributing factors of the insertion loss are resistive loss due to the finite resistance of the signal lines and contact at low to medium frequencies, and loss due to the skin depth effect at high frequencies. The main contributing factor of the return loss at the close state is the mismatch of the switch's total characteristic impedance. The main contributing factors of the isolation are the capacitive coupling and the surface leakage.

Chapter 3: Lateral RF MEMS Switches

In this section, the RF circuit design and lumped-element modeling of the lateral switch are discussed. The main purpose is to study the effect of the design parameters on the RF performance and to realize lateral switches with low insertion loss, high return loss and high isolation. Since the lateral switch is a metal-contact series switch, the on-state and the close-state, the off-state and the open-state are used interchangeably.

3.1.1 RF circuit design of the lateral switch

A lateral switch consists of a silicon-core coplanar waveguide (Si-core CPW) and an electrostatic actuator, as shown in Figure 3-1 (a). A cantilever beam is equipped with a fixed connection at one port. The free-end of the cantilever beam comes into contact with the contact bump at the other port upon turning on the switch. The cantilever beam serves as the signal line alone. The ground lines beside the cantilever beam are extended towards the cantilever beam to avoid drastic increase in the characteristic impedance of this section. The width of the gaps between the cantilever beam and the ground lines is 20-30 μm . The characteristic impedance of the cantilever beam section, Z_0 , is about 78 Ω simulated by a three-dimensional (3D) full wave finite-element-method (FEM) analysis tool - Ansoft's high frequency structure simulator (HFSS) V8.0 [120]. At the free-end of the cantilever beam, one ground line protrudes toward the cantilever beam further to serve as a fixed electrode. Therefore, no additional fixed electrode is required. When sufficient DC bias voltage is applied between the cantilever beam and the ground line, the cantilever beam is pulled towards the fixed electrode by the electrostatic force until its free-end hits the contact bump, resulting in the close-state of the switch. When DC bias voltage is removed, the mechanical stresses of the beam overcome the stiction forces and

Chapter 3: Lateral RF MEMS Switches

Figure 3-1 Schematics of the lateral switch (a) top view and (b) cross sectional view along A-A'.

pull the cantilever beam away, resulting in the open-state of the switch. Due to the asymmetrical layout of the lateral switch, the S-parameters of the two ports are not reciprocal. The return loss of port 2 is better than that of port 1 at the open-state since the open stub at port 2 is shorter than that at port 1. Hence, generally port 2 acts as the input port and port 1 acts as the output port to block more RF signal at the open-state. Figure 3-1 (b) shows the cross sectional view of the lateral switch along A-A'. The switch is fabricated on a SOI wafer. The substrate is 500- μm -thick high resistivity silicon (HRSi).

Chapter 3: Lateral RF MEMS Switches

The device layer is 35- μm -thick low resistivity silicon (LRSi). The cantilever beam is suspended on the substrate. The switch structures are made of LRSi. A thin layer of metal is coated on the top and sidewalls of the switch structures to propagate RF signal.

3.1.2 RF circuit model of the lateral switch

Figure 3-2 shows the equivalent circuit of the lateral switch. The model consists of a characteristic impedance, Z_0 , for the input and output sections of the Si-core CPW, a line resistor, R_l , of the cantilever beam, a line inductor, L , of the cantilever beam, a switch series capacitor, C_s (open-state) or a contact resistor, R_c (close-state), and a shunt coupling capacitor, C_g . The equivalent circuit is modelled using the design tool of Agilent EESof's Advanced Design System (ADS). The line resistance R_l , inductance L , switch open capacitance C_s and close resistance R_c , and shunt capacitance C_g are allowed to vary to fit the measurement results or the simulation results obtained from ADS.

According to the T-equivalent circuit model, S_{21} of the circuit can be given by [27]

$$S_{21} = \frac{2}{2 + (Z_0 + Z_1 + Z_2) / Z_3 + \left(Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3} \right) / Z_0} \quad (3-1a)$$

where

$$Z_1 = R_l + j\omega L \quad (3-1b)$$

$$Z_2 = \begin{cases} \frac{1}{j\omega C_s} & \text{at the open-state} \\ R_c & \text{at the close-state} \end{cases} \quad (3-1c)$$

$$Z_3 = \frac{1}{j\omega C_g} \quad (3-1d)$$

ω is the angular frequency ($\omega = 2\pi f$, f is the signal frequency).

Chapter 3: Lateral RF MEMS Switches

Figure 3-2 The equivalent circuit of the lateral switch.

Figure 3-3 Simulation results of S-parameters with various capacitances C_s at the open-state of the lateral switch ($R_l = 1 \Omega$, $L = 148 \text{ pH}$, $C_g = 30 \text{ fF}$).

At the open-state, the switch capacitance, C_s , is an important factor that affects the isolation of the switch. For $S_{21} \ll -10 \text{ dB}$ and $\omega C_s Z_0 \left[2 - \omega^2 C_g L + \frac{C_g}{C_s} + \frac{R_l}{Z_0} \left(1 + \frac{C_g}{C_s} \right) \right]$

$\ll 1$, the switch isolation can be approximately expressed as

$$S_{21} \approx j2\omega C_s Z_0 \quad (3-2)$$

Chapter 3: Lateral RF MEMS Switches

Therefore, the series capacitance, C_s , of the open-state switch can be extracted from the simulated or measured isolation of the switch using Eq (3-2). Figure 3-3 shows the simulated isolation of an open-state switch with various series capacitances of C_s . The isolation of the open-state switch increases with the decrease in C_s . The equivalent series capacitance C_s of our practical lateral switches is 3-10 fF. Up to 25 GHz, the isolation is higher than 25 dB for $C_s = 3$ fF and 15 dB for $C_s = 10$ fF.

At the close-state, the insertion loss and the return loss are derived as

$$S_{21} = \frac{2}{2 + (R_l + R_c)/Z_0 - \omega^2 C_g L(1 + R_c/Z_0) + j\omega [C_g (Z_0 + R_l + R_c + R_l R_c/Z_0) + L/Z_0]} \quad (3-3a)$$

$$S_{11} = \frac{(R_l + R_c)/Z_0 - \omega^2 C_g L(1 + R_c/Z_0) + j\omega [C_g (R_l - R_c - Z_0 + R_l R_c/Z_0) + L/Z_0]}{2 + (R_l + R_c)/Z_0 - \omega^2 C_g L(1 + R_c/Z_0) + j\omega [C_g (Z_0 + R_l + R_c + R_l R_c/Z_0) + L/Z_0]} \quad (3-3b)$$

At low frequencies, $\omega [C_g (Z_0 + R_l + R_c + R_l R_c/Z_0) + L/Z_0] \ll 2 + (R_l + R_c)/Z_0$ and $\omega^2 C_g L(1 + R_c/Z_0) \ll 2 + (R_l + R_c)/Z_0$, the insertion loss and the return loss of the switch can be simplified as

$$S_{21} \approx 2 / [2 + (R_l + R_c)/Z_0] \quad (3-4a)$$

$$S_{11} \approx (R_l + R_c) / [2Z_0 + (R_l + R_c)] \quad (3-4b)$$

Figure 3-4 shows the simulated results of the insertion loss and the return loss of the switch at the close-state with various resistance sums of $(R_l + R_c)$. The RF performances of the switch at the close-state deteriorate with the increase in the resistance sum $(R_l + R_c)$. When $R_l + R_c < 2 \Omega$, the insertion loss is less than 0.2 dB up to

Chapter 3: Lateral RF MEMS Switches

10 GHz. When $(R_l + R_c)$ increases to $10\ \Omega$, the insertion loss is larger than 0.8 dB at 10 GHz. The return loss decrease with $(R_l + R_c)$ Therefore, in order to achieve low insertion loss and high return loss, the resistance sum $(R_l + R_c)$ should be as small as possible.

The resistance sum $(R_l + R_c)$ of the switch at the close-state can also be extracted from the simulated or measured insertion loss of the switch using Eqs (3-4a) and (3-4b).

Figure 3-4 Simulation results of S-parameters with various resistance sum at the close-state of the lateral switch ($L = 148\ \text{pH}$, $C_g = 30\ \text{fF}$).

Table 3-1 Electrical properties of some metal materials

Material	Conductivity $\sigma\ (\text{S.m}^{-1})$	Skin depth, $\delta\ (\mu\text{m})$		
		10 GHz	25 GHz	40 GHz
Al	3.80×10^7	0.82	0.52	0.4
Au	4.55×10^7	0.75	0.47	0.37
Cu	5.88×10^7	0.66	0.42	0.33

Chapter 3: Lateral RF MEMS Switches

It is found that the measured resistance sum ($R_l + R_c$) decreases with the increase in the metal thickness of the coating layer since the cantilever beam resistance, R_l , is determined by the thickness of the coated metal and the contact resistance, R_c , is largely affected by the metal thickness too. The effect of the metal thickness on the beam resistance, R_l , is discussed. Due to the skin effect of metal at high frequencies, the fields decay by an amount of $1/e$ in a depth of one skin depth. The skin depth, δ_s , of metal is given by [27]

$$\delta_s = \sqrt{\frac{2}{\omega\mu_0\sigma}} \quad (3-5)$$

where μ_0 is the permeability of the vacuum ($\mu_0 = 4\pi \times 10^{-7}$ H/m), σ is the conductivity of the metal. The conductivity and the skin depth of the metal used in our experiments are listed in Table 3-1. The skin depth of aluminium (Al) is 0.83 μm at 10 GHz and 0.53 μm at 25 GHz. The surface resistivity, R_s , of the metal is given by

$$R_s = \begin{cases} 1/(\sigma\delta_s) & (t \geq \delta_s) \\ 1/(\sigma t) & (t < \delta_s) \end{cases} \quad (3-6)$$

where t is the metal thickness. Then, the resistance of a cantilever beam, R , can be expressed as

$$R = R_s \sum_i \frac{l_i}{w_i} \quad (3-7)$$

where l_i and w_i are the length and the width of different sections of the cantilever beam. Therefore, the resistance of the cantilever beam increases with frequency due to the skin effect. For instance, for a cantilever beam with $l = 460$ μm , $w = 3.3$ μm , $t_l = 1.2$ μm , and $t_s = 1.2$ μm , the calculated resistance of the beam R_l keeps constant of 3 Ω from DC to 4.6 GHz, then increases with frequency after 4.6 GHz. At 25 GHz, the resistance is 7.1 Ω .

Chapter 3: Lateral RF MEMS Switches

When the coating thickness and the conductivity of the metal are larger, the beam resistance is smaller. The RF power dissipation decreases and the insertion loss of the switch is lower. Therefore, to achieve high RF performance, the metal layer with high conductivity has to be coated as thick as possible.

The series inductance L can be calculated by [27]

$$L = \frac{Z_l \beta l}{\omega} = \frac{Z_l l \sqrt{\epsilon_{\text{eff}}}}{c} \quad (3-8)$$

where Z_l is the impedance of the cantilever beam, l is the whole length of the cantilever beam, β is the phase constant, ϵ_{eff} is the relative effective permittivity, and c is the speed of the light in vacuum ($c = 3.0 \times 10^8$ m/s). In this design ($l = 400\text{-}500$ μm , $\epsilon_{\text{eff}} \approx 1.66$, $Z_l = 50\text{-}78$ Ω), the equivalent series inductance is 86-167 pH. In Figure 3-5, the simulated results show that the RF performances of the switch at the close-state become better when

Figure 3-5 Simulation results of S-parameters with various inductances L at the close-state of the lateral switch ($R_l = 1$ Ω , $R_c = 1.8$ Ω , $C_g = 30$ fF).

Chapter 3: Lateral RF MEMS Switches

the inductance increases from 10 pH to 100 pH. However, when the inductance L increases further, the insertion loss and the return loss begin to deteriorate, especially at a high frequency range.

C_g is the shunt coupling capacitance between the cantilever beam and the fixed electrode, which can be estimated as

$$C_g = \frac{\epsilon_0 l_2 h}{g_0 - y} + C_f \quad (3-9)$$

where ϵ_0 is the permittivity of the air (8.854×10^{-12} F/m), l_2 is the length of the fixed electrode, h is the height of the cantilever beam, g_0 is the original gap distance between two electrodes, y is the displacement of the electrode part of the cantilever beam, and C_f is the fringing field capacitance which is 20-60% of C_g [3]. This coupling capacitance is fairly large ($C_g \gg C_s$) and affects the loss mechanism at the close-state of the switch. In Figure 3-6 it shows that the RF performance, including the insertion loss and the return loss of the switch at the close-state, improves when C_g increases from 10 fF to 60 fF, whereas the RF performance begins to deteriorate when C_g increases further to 125 fF. It is noted that when the switch is actuated, the gap between the two electrodes, g ($= g_0 - y$), decreases. Hence, the coupling capacitance at the close-state, $C_{g,c}$, is slightly larger than the one at the open-state, $C_{g,o}$. On the other hand, the structure design of the cantilever beam and the distance between the cantilever beam and the fixed electrode also determine the mechanical performance of the switch in terms of the threshold voltage and the switching speed. Therefore, it is important to select the values of l_2 and g_0 for the switch design to compromise between electrical and mechanical performances.

Figure 3-6 Simulation results of S-parameters with various capacitances C_g when the switch is at the close-state ($R_l = 1 \, \Omega$, $R_c = 1.8 \, \Omega$, $L = 148 \, \text{pH}$).

3.1.3 Double-beam lateral switch

Low insertion loss and high power handling are desired for wireless communication systems. Low insertion loss means low power loss and longer lifetime. The transmission power in the handset is 2 W in GSM850/900, 1 W in GSM1800/1900 and 3 mW in UMTS. Therefore, high power handling is needed in multi-band/ multi-mode systems. In order to achieve low insertion loss and high power handling, a double-beam lateral switch is proposed and shown in Figure 3-7. Two cantilever beams are used in the signal route together to propagate RF signal. Both fixed connections of two cantilever beams are on Port 1 and two contact bumps are on Port 2. At the free-end of two cantilever beams, both ground lines extend towards the nearby cantilever beams to serve as their fixed electrodes respectively. Therefore, once sufficient DC bias voltage is

Chapter 3: Lateral RF MEMS Switches

applied between the signal line and two ground lines at Port 1, both cantilever beams are pulled by the electrostatic force and move towards two ground lines respectively until they hit two contact bumps at Port 2. Similar to the single-beam switch, the two-port S-parameters of the double-beam switch are not reciprocal due to the asymmetrical layout. Generally, Port 2 acts as the input port and Port 1 acts as the output port for better signal isolation from the source at the open-state of the switch.

Figure 3-8 is the equivalent circuit of the double-beam lateral switch, which can be reduced into the form of the equivalent circuit model of the single-beam lateral switch. Therefore, for the double-beam switch, the resistor $R_l = R_{l0} / 2$, the inductor $L = L_0 / 2$, the series capacitor of the switch at the open-state $C_s = 2C_{s0}$, the contact resistor of the switch at the close-state $R_c = R_{c0} / 2$ and the shunt coupling capacitor $C_g = 2C_{g0}$, assuming that two cantilever beams are identical. Hence, the electrical model of the single-beam switch can also be used for the double-beam switch.

Figure 3-7 The schematic of the top view of a double-beam lateral switch.

Figure 3-8 The equivalent circuit of the double-beam lateral switch.

3.2 Mechanical Design and Simulation

The fundamental mechanical design of the lateral switch is an electrostatic actuator, as shown in Figure 3-9. The actuator consists of four components: a suspended cantilever beam serving as a movable electrode, an anchor on the substrate to support the cantilever beam, a fixed electrode opposite to the cantilever beam, and a contact bump.

The cantilever beam OC is a beam-mass structure, as shown in Figure 3-9. For the beam OA, the width is w_1 and the length is l_1 . For the mass AC, the width is w_2 and the length is (l_2+l_3) in which l_2 is the length of the electrode section AB and l_3 is the length of

Figure 3-9 The schematic of the top view of an electrostatic actuator.

Chapter 3: Lateral RF MEMS Switches

the remaining part BC. The mass width, w_2 , is designed to be relatively wider than the beam width, w_1 , so that low threshold voltage can be maintained and big deformation of the electrode section of the cantilever beam can be avoided. Hence, no separate stop-bumpers or landing pads are required to avoid short circuit between the two electrodes.

The original distance between the two electrodes is g_0 , and the distance between the contact bump and the mass part is d_0 . d_0 is relatively smaller than g_0 so that the cantilever beam can touch the contact bump when the switch is actuated. In Figure 3-9, X- and Z- axes are assumed to be oriented parallel to the length and the depth of the cantilever beam respectively, and Y-axis is directed towards the fixed electrode.

3.2.1 Static behavior

For the design of the lateral switch, low threshold voltage is always desired. According to the working mechanism of the electrostatic actuator, the threshold voltage is determined by two forces – the electrostatic force, F_e , and the restoring force, F_r .

3.2.1.1 Electrostatic force F_e

When a DC bias voltage, V , is applied between two electrodes, the electrostatic force, F_e , causes the mass to move towards the fixed electrode and the beam is bent. The bending of the mass part is negligible because it has much higher flexure rigidity than the beam, which has been verified by the simulation. The displacement of the mass increases with voltage until pull-in occurs. If the displacement of the beam OA and mass AC from its original position are designated as $y_1|_x$ and $y_2|_x$ respectively, the electrostatic force, F_e , on the mass can be derived as

$$F_e = \int_{l_1}^{l_1+l_2} \frac{\epsilon_0 h V^2 dx}{2(g_0 - y_2)^2} = \frac{\epsilon_0 h l_2 V^2}{2(g_0 - \alpha - \theta l_2)(g_0 - \alpha)} \quad (3-10a)$$

Chapter 3: Lateral RF MEMS Switches

where $y_2|_x = \alpha + \theta(x - l_1), \quad l_1 \leq x \leq l_1 + l_2$ (3-10b)

$$\alpha = y_2|_{x=l_1} = y_1|_{x=l_1} \quad (3-10c)$$

$$\theta = y_2'|_x = y_1'|_{x=l_1} \quad (3-10d)$$

where (') denotes the derivative with respect to position x . As the electrostatic force is not uniform, the bending moment, M_0 , caused by the electrostatic force can be calculated as [121]

$$M_0 = \int_{l_1}^{l_1+l_2} \frac{\varepsilon_0 h V^2 (x - l_1) dx}{2(g_0 - \alpha + \theta l_1 - \theta x)^2} = \frac{\varepsilon_0 h V^2}{2\theta^2} \left(\ln \frac{g_0 - \alpha - \theta l_2}{g_0 - \alpha} + \frac{\theta l_2}{g_0 - \alpha - \theta l_2} \right) \quad (3-11a)$$

For small θ , M_0 can be approximated as

$$M_0 = \frac{\varepsilon_0 h V^2 l_2^2}{2(g_0 - \alpha)} \left(\frac{1}{g_0 - \alpha - \theta l_2} - \frac{1}{2(g_0 - \alpha)} \right) \quad (3-11b)$$

The equation for the displacement of the beam $y_1|_x$ is determined by [121]

$$E_l I_l y_1''|_x = M_0 + F_e(l_1 - x), \quad 0 \leq x \leq l_1 \quad (3-12)$$

where E_l is Young's modulus of the beam and I_l is the moment of inertia of the cross-sectional area of the beam. At $x = 0$, the boundary conditions are

$$y_1|_{x=0} = y_1'|_{x=0} = 0 \quad (3-13)$$

By solving Eqs (3-10c), (3-10d), (3-12) and (3-13), α and θ can be obtained as

$$\alpha = \frac{3M_0 l_1^2 + 2F_e l_1^3}{6E_l I_l} \quad (3-14a)$$

$$\theta = \frac{2M_0 l_1 + F_e l_1^2}{2E_l I_l} \quad (3-14b)$$

Therefore, at a specific applied DC bias voltage V , F_e and M_0 are determined by α and θ from Eqs (3-10a), and (3-11a) and (3-11b), whereas α and θ are determined by M_0 and

Chapter 3: Lateral RF MEMS Switches

F_e from Eqs (3-14a) and (3-14b). Thus, F_e , M_θ , α and θ can be found together through numerical iterations. For a voltage equal to or larger than a specific value, the iteration results become divergent. This voltage is called threshold voltage. Using this method, the threshold voltage can be calculated through step-by-step calculation. Once α and θ are known, the displacement of the mass is found by Eq. (3-10b). For an actuator with $l_1 = 275 \mu\text{m}$, $l_2 = 165 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.45 \mu\text{m}$, $g_0 = 4.8 \mu\text{m}$, $d_0 = 2.8 \mu\text{m}$, the threshold voltage is calculated to be 23.7 V. The maximum stable displacement of the mass center is $1.37 \mu\text{m}$, which is a little smaller than $1/3g_0$.

3.2.1.2 Restoring force F_r

Once the mass part is displaced, an elastic restoring force by the beam tends to pull the mass back towards its original position. At the end of the electrode part AB of the mass, the restoring force, F_r , can be written as [121]

$$F_r = -k y_2 |_{x=l_1+l_2+l_3} = -k [\alpha + \theta(l_2 + l_3)] \quad (3-15)$$

where k is the equivalent stiffness of the cantilever beam. Suppose the mass is subject to a concentrated force at the midpoint of the electrode section, the equivalent stiffness, k can be derived as [121]

$$k = \frac{12E_1I_1E_2I_2}{E_2I_2[4l_1^3 + 9l_1^2l_2 + 6(l_1^2l_3 + l_1l_2^2 + l_1l_2l_3)] + E_1I_1(5l_2^3 + 6l_2^2l_3)/4} \quad (3-16)$$

where E_2 is the Young's modulus of the mass and I_2 is the moments of inertia of the cross-sectional area of the mass. Before the metal coating, the beam is merely made up of single-crystal-silicon. E_1 , E_2 , I_1 , and I_2 are given by

$$E_1 = E_2 = E_{Si} \quad (3-17a)$$

$$I_1 = \frac{1}{12} w_1^3 h \quad (3-17b)$$

Chapter 3: Lateral RF MEMS Switches

$$I_2 = \frac{1}{12} w_2^3 h \quad (3-17c)$$

where E_{Si} is Young's modulus of the single-crystal-silicon. After the metal coating, the beam is made of single-crystal-silicon covered by metal on the top and sidewalls. Therefore, E_1 , E_2 , I_1 , and I_2 can be expressed as [121]

$$E_1 = \frac{E_{Si} w_1 + 2E_m w_m}{w_1 + 2w_m} \quad (3-18a)$$

$$E_2 = \frac{E_{Si} w_2 + 2E_m w_m}{w_2 + 2w_m} \quad (3-18b)$$

$$I_1 = \frac{1}{12} (w_1 + 2w_m)^3 h \quad (3-18c)$$

$$I_2 = \frac{1}{12} (w_2 + 2w_m)^3 h \quad (3-18d)$$

where E_m is Young's modulus of the metal, w_m is the thickness of the metal coated at sidewalls of the silicon beam. The mechanical properties of the material for lateral switches are given in Table 3-2. Typically, $w_1 = 2.5$ to $3 \mu\text{m}$, $w_2 = 5$ to $15 \mu\text{m}$, $w_m < 1 \mu\text{m}$. Since $E_{Si} w_1 > 5E_m w_m$, the equivalent stiffness is dominated by silicon structures. After the metal coating, the initial gap distance between two electrodes, g_0 , and the initial gap distance between the beam end and the contact bump, d_0 , are expressed as

$$g_0 = g_{Si} - 2w_m \quad (3-19a)$$

$$d_0 = d_{Si} - 2w_m \quad (3-19b)$$

where g_{Si} and d_{Si} are the initial gap distance between the two silicon electrodes and the initial gap distance between the silicon beam and the silicon contact bump before metal coating, respectively.

Chapter 3: Lateral RF MEMS Switches

Table 3-2 Mechanical properties of materials used in the lateral switch.

Material	Density (kg/m ³)	Young's Modulus (GPa)	Poisson's Ratio
Si	2330	162	0.27
Al	2700	70	0.35
Au	19280	80	0.44
Cu	8960	128	0.36

3.2.1.3 Threshold voltage V_{th}

The balanced position of the mass part can be found as the force is balanced

$$F = F_e + F_r = 0 \tag{3-20}$$

The curves of normalized F_e and $|F_r|$ as functions of the normalized displacement y/g_0 are shown in Figure 3-10. For a specific mechanical structure, k is a constant. Therefore, the curve for the restoring force, F_r , is a straight line starting from the origin of the coordinates. The curve for the electrostatic force, F_e , is a hyperbola. When the applied bias voltage, V , is less than a specific voltage V_{th} , the two curves have two intersections, i.e. Eq (3-20) has two solutions. It is found that the two intersections move closer with the increased bias voltage V and F_e increases. The intersections coincide when $V = V_{th}$. When $V > V_{th}$, the two curves do not intersect since $F_e > -F_r$ at all displacements, that is, the mass part always collapses to touch the contact bump. V_{th} is the threshold voltage, which can be calculated using the iteration method, as discussed in 3.2.1.1.

Chapter 3: Lateral RF MEMS Switches

Figure 3-10 Normalized electrostatic force and restoring force on the movable cantilever beam with various applied bias voltages.

Figure 3-11 The shape of cantilever beam with various applied bias voltages.

Chapter 3: Lateral RF MEMS Switches

Figure 3-11 shows the shape of a cantilever beam ($l_1 = 275 \mu\text{m}$, $l_2 = 165 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.45 \mu\text{m}$, $g_0 = 4.8 \mu\text{m}$, $d_0 = 2.8 \mu\text{m}$) with various bias voltages, which is simulated by commercial 3D simulation software – LS DYNA. The displacement of the cantilever beam increases with the bias voltage. The deformation of the beam OA of the cantilever beam increases with the bias voltage, whereas the mass part AC of the cantilever beam moves almost without deformation. The simulated threshold voltage is 24 V, which is close to the calculated result, 23.7 V using the iteration method.

The threshold voltage, V_{th} , is determined by the cantilever beam design and the original gap between two electrodes, g_0 . Figure 3-12 shows that the threshold voltage, V_{th} , decreases when the original gap between the two electrodes, g_0 , decreases or the length sum, $(l_1 + l_2)$, increases. When the cantilever beam length ratio, $l_2 / (l_1 + l_2)$, is within the range of 30 – 75 %, V_{th} only change within 10% of the minimum value of V_{th} , which is referred as $[V_{th}]_{min}$. The corresponding length ratio $[l_2 / (l_1 + l_2)]_{min}$ to $[V_{th}]_{min}$ is 50% when $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, and $w_{Al} = 0$. It also shows that $[l_2 / (l_1 + l_2)]_{min}$ is independent of the initial gap, g_0 , and the length sum, $(l_1 + l_2)$.

Figure 3-13 shows that V_{th} is more dependent on the beam width, w_1 , than the mass width, w_2 . The effect of the mass width, w_2 , is negligible. V_{th} increases with beam width, w_1 . The mass structure can be designed as a hole-mass structure, as shown in Figure 3-21 (a). The hole-mass has three advantages compared to the solid-mass. First, the solid-mass with the width of more than $5 \mu\text{m}$ is not easy for release due to the constriction in the fabrication process. However, this problem can be solved by the mass with etched holes. Second, the etched holes reduce the effective mass of the mass

Chapter 3: Lateral RF MEMS Switches

Figure 3-12 Calculated threshold voltage V_{th} with various lengths ($l_1 + l_2$), $l_2 / (l_1 + l_2)$ ratio and initial gap distance g_0 ($l_3 = 10 \mu m$, $w_1 = 2.4 \mu m$, $w_2 = 5 \mu m$, $w_m = 0$, $g_{Si} = 6 \mu m$).

Figure 3-13 Calculated threshold voltage V_{th} with various cantilever beam widths (w_1 , w_2) ($l_1 = 275 \mu m$, $l_2 = 165 \mu m$, $l_3 = 10 \mu m$, $g_{Si} = 6 \mu m$, $w_m = 0$).

Chapter 3: Lateral RF MEMS Switches

structure, and increase the flexibility of the whole cantilever beam structure. Third, the lateral switch with the hole-mass structure can provide better RF performance than that with the solid-mass structure. Section 3.3.1 provides a more detailed discussion on the cantilever beam effect on the RF performance of the lateral switch.

The effect of the metal thickness, w_m , of sidewalls on the threshold voltage is more complicated. For further elaboration, take an example where aluminium is used as a coating metal. The effect of the aluminium (Al) thickness, w_{Al} , is shown in Figure 3-14. Initially when Al thickness on sidewalls, w_{Al} , increases, the threshold voltage, V_{th} , increases slightly. However, after the threshold voltage, V_{th} gets to its maximum, it decreases with the increase in w_{Al} . This observation can be explained by two effects that arise from the metal coating at sidewalls. On the one hand, the metal increases the stiffness of the cantilever beam which tends to increase the restoring force, F_r and the threshold voltage, V_{th} . On the other hand, the metal coating reduces the original gap between the two electrodes from g_{Si} to $(g_{Si}-2w_m)$, which tends to increase the electrostatic force, F_e , and reduce the threshold voltage, V_{th} . When w_{Al} is small, the increase in F_r dominates the increase in F_e . As a result, V_{th} increases. However, once w_{Al} exceeds a specific value, the increase in F_e dominates the increase in F_r . Therefore, V_{th} falls. In general, the change of the threshold voltage, V_{th} , due to the metal coating is less than 5 V since w_{Al} is less than 1 μm . The effect of the beam parameters of w_1 , w_2 and w_{Al} on the threshold voltage, V_{th} , is summarized in Table 3-3 when $l_1 = 275 \mu m$, $l_2 = 165 \mu m$, $l_3 = 10 \mu m$, and $g_{Si} = 6 \mu m$.

Chapter 3: Lateral RF MEMS Switches

Figure 3-14 Calculated threshold voltage V_{th} with various thicknesses of Al coated at sidewalls

w_{Al} ($l_1 = 275 \mu m, l_2 = 165 \mu m, l_3 = 10 \mu m, g_{Si} = 6 \mu m, w_2 = 5 \mu m$).

Table 3-3 The effect of the cantilever beam design parameters on the threshold voltage

Beam width w_1 (μm)	Mass width w_2 (μm)			Al thickness at sidewalls w_{Al} (μm)		
	$(w_{Al} = 0)$			$(w_2 = 5 \mu m)$		
	2.5	5	15	0.2	0.6	1.0
2.0	17.25	17.25	17.25	19.45	22.15	22.45
2.4	22.65	22.65	22.65	24.7	26.8	26.35
3.0	31.65	31.65	31.65	33.25	34.35	32.6
3.5	39.9	39.9	39.9	41.05	41.05	38.1

3.2.2 Dynamic analysis

3.2.2.1 Frequency response

The frequency response of the cantilever beam is useful to determine the switching time of the lateral switch and the mechanical bandwidth over which the lateral switch can be used. The frequency response can be determined by d'Alembert's principle as [122]

$$my'' + by' + ky = f_{ext} \quad (3-21)$$

where (') denotes the derivative with respect to time t , y is the lateral displacement of the cantilever beam relative to the origin of the fixed electrode, m is the effective mass, k and b are the effective stiffness and the damping coefficient of the simplified system, and $f_{ext}(t)$ is the electrostatic force. The electrostatic force, $f_{ext}(t)$, between the two electrodes generated by a bias voltage, V , can be simplified as

$$f_{ext}(t) = \frac{\epsilon_0 h l_2 V^2}{2(g_0 - y)^2} \quad (3-22)$$

Based on the Laplace transforms, the frequency response of the cantilever beam with small vibration amplitude is

$$\frac{Y(j\omega)}{F(j\omega)} = \frac{1/k}{1 - (\omega/\omega_0)^2 + j\omega/(Q\omega_0)} \quad (3-23)$$

where ω is the working angular frequency, ω_0 is the natural resonant angular frequency and Q is the quality factor of the cantilever beam. ω_0 and Q are expressed as

$$\omega_0 = \sqrt{k/m} \quad (3-24)$$

$$Q = k/(\omega_0 b) \quad (3-25)$$

The quality factor Q of the cantilever beam is determined by several different variables,

Chapter 3: Lateral RF MEMS Switches

Figure 3-15 Frequency response of a beam with resonant frequency of 15 kHz and $k = 0.94$.

such as the pressure, the temperature, and the intrinsic material dissipation. Figure 3-15 shows the variation in the frequency response for a cantilever beam with resonant frequency of 15 kHz and $k = 0.94$. The variation in the quality factor is seen by the amplitude change at 15 kHz. In practice, it is beneficial to have a structure with $0.5 \leq Q \leq 2$. Structures with $Q \leq 0.5$ result in a slow switching time, while structures with $Q \geq 2$ results in a long settling time when release.

3.2.2.2 Effective mass

It is noted that the effective mass of the cantilever beam is not equal to the actual mass of the cantilever beam since only the end portion of the cantilever beam is moving. The effective mass, m , can be estimated by Rayleigh's Energy method [122]. Assume the cantilever beam is subject to a concentrated load, P , at the center of the electrode section

Chapter 3: Lateral RF MEMS Switches

of the cantilever beam. Referring to Figure 3-9, we can consider the displacement $y|_x$ and kinetic energy, E_k of the cantilever beam at three portions respectively.

The first part is the beam ($0 < x \leq l_1$). Its kinetic energy E_{k1} is given by

$$\begin{aligned} E_{k1} &= \frac{1}{2}(\rho_{Si}w_1 + 2\rho_m w_m)h \int_0^{l_1} \dot{y}_1^2 dx \\ &= \frac{1}{2}m_1 \left(\frac{P}{2E_1 I_1} \right)^2 \frac{-4l_1^4 + 25l_1^3 l_2 + 10l_1^2 l_2^2}{30} \end{aligned} \quad (3-26a)$$

where

$$y_1 = \frac{Px^2}{6E_1 I_1}(3l_1 - x) + \frac{Pl_2 x^2}{2E_1 I_1} = \frac{Px^2}{6E_1 I_1}(3l_1 + 3l_2 - x) \quad (3-26b)$$

$$m_1 = (\rho_{Si}w_1 + 2\rho_m w_m)l_1 h \quad (3-26c)$$

The second part is from the beginning of the electrode to the center of the electrode of the cantilever beam ($l_1 < x \leq l_1 + l_2 / 2$). The kinetic energy E_{k2} is given by

$$\begin{aligned} E_{k2} &= \frac{1}{2}(\rho_{Si}w_2 + 2\rho_m w_m)h \int_{l_1}^{l_1 + l_2/2} \dot{y}_2^2 dx \\ &= \frac{1}{2}m_2 \left[\left(\frac{P}{E_1 I_1} \right)^2 \frac{l_1^2 (l_1 + l_2)^2}{8} + \frac{P^2}{E_1 I_1 E_2 I_2} \frac{l_1 l_2^2 (l_1 + l_2)}{24} + \left(\frac{P}{E_2 I_2} \right)^2 \frac{49l_2^4}{5760} \right] \end{aligned} \quad (3-27a)$$

where

$$y_2 = \frac{Pl_1^3}{3E_1 I_1} + \frac{Pl_2 l_1^2}{2E_1 I_1} + \frac{P(l_1^2 + 2l_1 l_2)(x - l_1)}{2E_1 I_1} + \frac{P(x - l_1)^2 [3l_2 - (x - l_1)]}{6E_2 I_2} \quad (3-27b)$$

$$m_2 = (\rho_{Si}w_2 + 2\rho_m w_m)l_2 h \quad (3-27c)$$

The third part is from the center of the electrode to the end of the cantilever beam ($l_1 + l_2 / 2 < x \leq l_1 + l_2 + l_3$). The kinetic energy E_{k3} is given by

Chapter 3: Lateral RF MEMS Switches

$$\begin{aligned}
E_{k3} &= \frac{1}{2}(\rho_{Si}w_2 + 2\rho_m w_m)h \int_{l_1+l_2/2}^{l_1+l_2+l_3} \dot{y}_3^2 dx \\
&= \frac{1}{2}m_2 \left[\frac{P(l_1^2 + l_1 l_2)}{2E_1 I_1} + \frac{Pl_2^2}{8E_2 I_2} \right]^2 \left(\frac{1}{2} + \frac{l_3}{l_2} \right)
\end{aligned} \tag{3-28a}$$

where

$$y_3 = \frac{P(4l_1^3 + 3l_2 l_1^2)}{12E_1 I_1} + \frac{P(l_1^2 + l_1 l_2)(x - l_1)}{2E_1 I_1} + \frac{Pl_2^3/4}{6E_2 I_2} + \frac{P \frac{l_2^2}{4} \left(x - l_1 - \frac{l_2}{2} \right)}{2E_2 I_2} \tag{3-28b}$$

Therefore, the total kinetic energy E_k are given by

$$E_k = E_{k1} + E_{k2} + E_{k3} = \frac{1}{2} m \dot{y}_{\max}^2 \tag{3-29a}$$

where the velocity $\dot{y}_{\max}$ at the end of the cantilever beam is

$$\dot{y}_{\max} = \dot{y}_3 \Big|_{x=l_1+l_2+l_3} = \frac{P(l_1^2 + l_1 l_2)}{2E_1 I_1} + \frac{Pl_2^2}{8E_2 I_2} \tag{3-29b}$$

The effective mass, m , can be obtained by solving Eq (3-29a). Figure 3-16 shows the portion mass m_1 , m_2 and the effective mass, m , of a cantilever beam changes with the ratio of $(l_2/(l_1 + l_2))$ when $l_1 + l_2 = 440 \mu\text{m}$ and $l_3 = 10 \mu\text{m}$. It shows that the effective mass, m , is mainly determined by the mass of the electrode part, m_2 . The effective mass, m , is 51 – 85% of the actual total mass of the cantilever beam $[m_1 + m_2(1 + l_3/l_2)]$ when the ratio of $[l_2/(l_1 + l_2)]$ is within the range of 30% - 75%.

Figure 3-17 shows the natural resonant frequency of the cantilever beam changes with the ratio of $(l_2/(l_1 + l_2))$ and the sum of $(l_1 + l_2)$. It shows that the natural resonant frequency of the cantilever beam changes slightly when $l_2/(l_1 + l_2)$ is within the range of 0.3 - 0.75. For example, when $(l_1 + l_2) = 440 \mu\text{m}$ and $l_3 = 10 \mu\text{m}$, the resonant frequency

Chapter 3: Lateral RF MEMS Switches

Figure 3-16 Effective mass and part mass of the cantilever beam versus the ratio of $l_2/(l_1+l_2)$ ($w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.6 \mu\text{m}$, $l_1+l_2 = 440 \mu\text{m}$ and $l_3 = 10 \mu\text{m}$, $h = 35 \mu\text{m}$).

Figure 3-17 Natural Resonant frequency versus the ratio of $l_2/(l_1+l_2)$ ($w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.6 \mu\text{m}$, $h = 35 \mu\text{m}$).

Chapter 3: Lateral RF MEMS Switches

is 15 ± 0.5 kHz as $l_2 / (l_1 + l_2)$ is within the range of 0.3 - 0.75. The natural resonant frequency of the cantilever beam decreases with the increase of $(l_1 + l_2)$ due to the increase of the effective mass and the decrease of the stiffness of the cantilever beam.

3.2.2.3 Switching time

The switching time is obtained using Eq. (3-21) when $y = g_0$. Substitute Eqs (3-22), (3-24) and (3-25) into Eq (3-21), the dynamic response equation can be obtained as

$$y'' + \frac{\omega_0}{Q} y' + \omega_0^2 y = \frac{\varepsilon_0 h l_2 V^2}{2(g_0 - y)^2 m} \quad (3-30)$$

The equation governs the simple 1-D nonlinear model and can be solved with a nonlinear simultaneous differential equation solver - *Mathematica* [123].

Assume that the cantilever beam has the parameter values shown in Table 3-4. Figure 3-18 presents the time-domain response for the cantilever beam coated with gold (Au) and aluminium (Al) for different Q factors. The applied voltage is 40 V. It shows there is a substantial improvement from $Q = 0.5$ to $Q = 2$, but little improvement when Q is above 2. The beam coated with Al responds faster than the beam coated with Au since mass of the Al is smaller than the mass of the Au. Figure 3-19 shows that the switching time depends significantly on the applied voltage. The calculated switching time is 23 μ s when the applied voltage is 40 V and 43 μ s when the applied voltage is 30 V as $Q = 1$ and the coating metal is Al. This is because the larger the applied voltage, the stronger the electrostatic force and the shorter the time required to make the first contact. The corresponding contact force values are 77.6 μ N, 106 μ N and 139 μ N for 30 V, 35 V and 40 V respectively.

Chapter 3: Lateral RF MEMS Switches

Table 3-4 Parameters of the cantilever beam for the dynamics simulations

Parameters	Values	Parameters	Values
l_1 (μm)	275	ρ_{Si} (kg/m^3)	2330
l_2 (μm)	165	ρ_{Au} (kg/m^3)	19320
l_3 (μm)	10	ρ_{Al} (kg/m^3)	2700
w_1 (μm)	2.5	E_{Si} (GPa)	162
w_2 (μm)	5.0	E_{Al} (GPa)	70
w_m (μm)	0.6	E_{Au} (GPa)	80
g_{Si} (μm)	6.0	Mass, m	107 (Al)
d_{Si} (μm)	4.0	(nanogram)	264 (Au)
h (μm)	35	Stiffness	0.86 (Al)
		k (N/m)	0.88 (Au)
		Frequency	14.3 (Al)
		ω_0 (KHz)	9.2 (Au)

Figure 3-18 Time domain response of a cantilever beam with different metal coating and Q-factor
($V_{\text{bias}} = 40 \text{ V}$).

Chapter 3: Lateral RF MEMS Switches

Figure 3-19 Time domain response for the cantilever beam with different applied voltage (Q = 1).

Figure 3-20 Simulation results of release time for the cantilever beam with different Q-factors.

3.2.2.4 Release time

The nonlinear dynamic analysis equation can also be used to model the release mechanism of the switch when $f_{ext}(t) = 0$. The restoring force ($= k \cdot g_0$) is 3.8 - 4.6 μN as parameter values of the switch are shown in Table 3-4. Figure 3-20 presents the release response for the cantilever beam coated with Al and $Q = 0.5, 1, 2$, and 4. When $Q = 2$ and 4, the beam oscillates and takes a longer time to stabilize. When $Q = 0.5$ and 1, the beam takes a shorter time to stabilize.

3.3 Experiment Results and Discussions

The lateral switches discussed in this chapter are fabricated using silicon-on-insulator (SOI) wafer, which includes a 35- μm -thick low resistivity silicon (LRSi) device layer, a 2- μm -thick silicon dioxide (SiO_2) layer and a 500- μm -thick high resistivity silicon (HRSi) handle layer ($> 4000 \Omega\cdot\text{cm}$). The fabrication process begins with the deposition and patterning of SiO_2 on the device layer. Then, the switch structures are etched in the device layer until the buried oxide using deep reactive ion etching (DRIE) technique. Next, the cantilever beam is released by removing the buried oxide using buffered oxide etchant (BOE). Finally, a thin layer of aluminium is coated on the top and sidewalls of the switch structures using E-beam evaporation. The process detail is presented in Pub. [1].

For a typical lateral switch, the signal line width, S , the ground line width, G , and the space between the signal line and the ground line, W , of the Si-core CPW port, are 66 μm , 100-300 μm , and 67 μm , respectively. Therefore, the port can accommodate 150- μm -pitch ground-signal-ground coplanar probes, at the same time, the characteristic

Chapter 3: Lateral RF MEMS Switches

impedance of the Si-core CPW is about $50\ \Omega$. The design dimensions of the electrostatic actuator are $l_1 = 210$ to $275\ \mu\text{m}$, $l_2 = 165$ to $220\ \mu\text{m}$, $l_3 = 10$ to $30\ \mu\text{m}$, $w_1 = 2$ to $3\ \mu\text{m}$, $w_2 = 5$ to $15\ \mu\text{m}$, $g_{\text{Si}} = 4$ to $6\ \mu\text{m}$ and $d_{\text{Si}} = 3$ to $4\ \mu\text{m}$. There are four main concerns in selecting these dimensions. First, to keep a small device area, generally $< 1\ \text{mm}^2$, a short cantilever beam is required. Second, good RF performance needs a short and wide cantilever beam, and a large gap distance between the cantilever beam and the fixed-electrode, as discussed in Section 3.1.2. Third, to obtain low actuation voltage and fast switching speed, a long and narrow cantilever beam and a small gap distance between the cantilever beam and the fixed electrode are necessary. Fourth, w_1 , w_2 , g_{Si} and d_{Si} should be large enough for easy fabrication. A proper design of the electrostatic actuator satisfies these four requirements. The cantilever beam has length of 450 to $500\ \mu\text{m}$ and therefore the entire device is about $700\ \mu\text{m}$ long. The length ratio $[l_2 / (l_1 + l_2)]_{\text{min}}$ is 35% to 75%. This gives low threshold voltage and low insertion loss.

Figure 3-21 shows a SEM micrograph of a lateral switch. The switch has a size of $400\ \mu\text{m} \times 700\ \mu\text{m}$ in area. The actuator dimensions are: $l_1 = 275\ \mu\text{m}$, $l_2 = 165\ \mu\text{m}$, $l_3 = 10\ \mu\text{m}$, $w_1 = 2.4\ \mu\text{m}$, $w_2 = 15\ \mu\text{m}$, $g_{\text{Si}} = 6\ \mu\text{m}$ and $d_{\text{Si}} = 4\ \mu\text{m}$. A hole-mass structure is employed in the cantilever beam of the switch, which is $15\ \mu\text{m}$ wide. Every hole is $10\ \mu\text{m}$ wide and $30\ \mu\text{m}$ long, so that the etching rate of holes is closed to other structures during DRIE process. Figure 3-22 is an AFM micrograph showing the surface roughness of a cantilever beam with Al coating. The surface roughness is $250\ \text{\AA}$, which is much smaller than Al skin depth up to $100\ \text{GHz}$. Therefore, only a small percent of the total current sees this roughness. The power loss due to this roughness is negligible [124].

Chapter 3: Lateral RF MEMS Switches

Figure 3-21 SEM micrograph of a lateral switch with the hole-mass (G: ground, S: signal).

Figure 3-22 AFM micrograph showing the surface roughness of the sidewall of a cantilever beam coated with Al. Roughness = 250 Å.

Chapter 3: Lateral RF MEMS Switches

Figure 3-23 SEM micrograph of the contact point on the cantilever beam.

Figure 3-23 shows the zoomed view of the contact part of a cantilever beam after tens of switching cycles. The contact is a small point at the top of the cantilever beam sidewall, instead of the whole depth. That is because the cantilever beam is not absolutely straight due to the limitation of the fabrication process. The metal deposited at the upper side of the cantilever beam is slightly thicker than that at the bottom. Therefore, the gap between the cantilever beam and the contact bump on the upper part is slightly narrower than the bottom. The contact point is about $1\text{ }\mu\text{m} \times 0.7\text{ }\mu\text{m}$ in area. It is easy to realize effective contact since the contact force focuses on this small point. However, the contact resistance is larger due to the small contact area.

3.3.1 RF response characterization

The RF responses of lateral switches are measured using HP 8510C Vector Network Analyzer (VNA) with tungsten - tip 150 μm - pitch Cascade Microtech ground-signal-ground coplanar probes. The system is calibrated using short-open-load-through (SOLT) on-wafer calibration technique. All tests are performed in the room environment without any package or protection. Before RF testing, each switch is actuated tens of cycles to make contact surfaces adapt to each other and the contact resistance becomes constant. Table 3-5 lists the actuator dimensions and fitted circuit parameters of all switches discussed in this section. $g_{\text{Si}} = 6\text{ }\mu\text{m}$, $d_{\text{Si}} = 4\text{ }\mu\text{m}$. Except Switch H and I, the other switches (Switch A to G) are coated with 1.2- μm -thick Al. The second column is the key parameter to differentiate each switch. R is the total resistance ($R = R_f + R_c$).

Table 3-5 Cantilever beam parameters and fitted circuit values of lateral switches at 10 GHz.

No	Para- meters	L (μm)	L_1 (μm)	L_2 (μm)	L_3 (μm)	w_1 (μm)	w_2 (μm)	R (Ω)	L (pH)	$C_{\text{g,c}}$ (fF)	$C_{\text{g,o}}$ (fF)	C_s (fF)
A	1-beam	450	275	165	10	2.4	5	4.2	148	28	20	6.5
B	2-beam	450	275	165	10	2.4	5	2.4	60.4	67	56	7
w_1/w_2 (μm) (Single-beam switch with separated fixed-electrode)												
C	2.0/5.0	447	210	215	22	2.0	5	5.4	149	22.6	16	13
D	2.4/5.0	447	210	215	22	2.4	5	5.1	140	22.6	16	13.2
E	2.4/15	447	210	215	22	2.4	15	4.2	130	22.6	16	13.5
L_2 (μm) (Double-beam switch)												
F	235	450	187	235	28	2.4	5	2.8	58	70	63	7
G	350	450	72	350	23	2.4	5	3.4	55.6	77	70	7
t_{Al} (μm) (Single-beam switch)												
H	0.8	450	275	165	10	2.4	5	5.0	182	56	50	5.5
I	1.5	450	275	165	10	2.4	5	1.8	147	34	24	5.8

3.3.1.1 The single-beam switch and the double-beam switch

Figure 3-24 shows measured and fitted S-parameters of a single-beam lateral switch (Switch A). The design dimensions of the cantilever actuator of the lateral switch are $l_1 = 275 \mu\text{m}$, $l_2 = 165 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$ (solid mass), $g_{\text{Si}} = 6 \mu\text{m}$ and $d_{\text{Si}} = 4 \mu\text{m}$. 1.2- μm -thick Al is deposited. The switch has an insertion loss of 0.37 dB, return loss of 23 dB and isolation of 27 dB at 10 GHz. The equivalent circuit model values are fitted using the measured S-parameters in ADS. It is found that the fitted S-parameters are in good agreement with the measured results. Therefore, the equivalent circuit model of the lateral switch in Figure 3-2 is valid. Table 3-6 compares fitted and calculated values of the equivalent circuit models of Switch A. The fitted inductance, L is close to the calculated value. The fitted parasitic capacitance, C_{gc} , at the close-state and C_{go} , at the open-state are 28 fF and 20 fF respectively, which are a little larger than the calculated values 22.9 fF and 15.6 fF due to the fringing field capacitance. Therefore, the fringing field capacitance is about 5.1 fF at the close-state and 4.4 fF at the open-state. The calculated DC resistance of the cantilever beam, R_l , is 0.4Ω , while the fitted total resistance, R ($=R_l+R_c$), is 2.6Ω . Therefore, the contact resistance is about 2.2Ω . The fitted total resistance increases with frequency, as shown in Figure 3-25. The resistance is 2.6Ω at DC and 4.2Ω at 10 GHz. One reason is the skin effect at high frequency, as discussed in Section 3.1.1. The contact resistance may increase with frequency too. Third, the two ground lines' potential is not same at the high frequency due to the asymmetrical structure of the switch, which results in more loss at the high frequency. In this section, if without specific clarification, all switches' total resistance, R_l+R_c , is set to increase with frequency in the equivalent circuit model.

Chapter 3: Lateral RF MEMS Switches

Figure 3-24 Comparison between measured and fitted S-parameters of the single-beam switch (Switch A).

Figure 3-25 Plot of the fitted resistance, $R_l + R_c$, of Switch A with frequency.

Chapter 3: Lateral RF MEMS Switches

Table 3-6 Comparison between fitted and calculated circuit values of Switch A.

	$R_l + R_c$ @ DC (Ω)	$R_l + R_c$ @ 10 GHz (Ω)	L (pH)	C_{gc} (fF)	C_{go} (fF)	C_s (fF)
Fitted value	2.6	4.2	148	28	20	6.7
Calculated value*	0.5	1.0	150	22.9	15.6	-

Figure 3-26 shows the SEM micrograph of a double-beam switch. The switch has a size of $800\text{ }\mu\text{m} \times 700\text{ }\mu\text{m}$. A solid-mass structure is employed in the cantilever beam. The actuator design dimensions and fitted circuit elements at 10 GHz are listed in Table 3-5 (switch B). Figure 3-27 compares measured and fitted S-parameters of the double-beam switch. The fitted S-parameters agree with the measured results well. Figure 3-28 compares measured S-parameters between the single-beam switch (switch A) and the double-beam switch. The double-beam switch has a lower insertion loss than the single-beam switch by 0.1 dB from 0.05 to 25 GHz. The return loss of the double-beam switch is larger than the single-beam switch from 0.05 to 17 GHz and lower than the latter when the frequency is above 17 GHz. The isolation of two switches is close to each other. The fitted total resistance, R , of the double-beam switch is $2.4\text{ }\Omega$ at 10 GHz, which is close to half of the single-beam switch. The lower total resistance also results in higher return loss at low frequency range for the double-beam switch, as predicted in Section 3.1.2. The fitted inductance, L , of the double-beam switch is 60.4 nH, which is also close to half of the single-beam switch. Lower inductance results in lower insertion loss at high frequencies for the double-beam switch. The parasitic capacitance at the close-state, C_{gc} , and at the open state, C_{go} , of the double beam switch is nearly 2 times of the single-beam

Figure 3-26 SEM micrograph of a double-beam lateral switch with the solid mass.

Figure 3-27 Comparison between measured and fitted S-parameters of the double-beam switch (Switch B).

Figure 3-28 Comparison of measured S-parameters between the single-beam switch (Switch A) and the double-beam switch (Switch B).

switch, which results in higher return loss at low frequencies for the double-beam switch. The open capacitance, C_s , of the double-beam switch is slightly larger than the single-beam switch. Therefore, the equivalent circuit model of the double-beam switch, as shown in Figure 3-8, is verified to be valid. The double-beam switch can provide lower insertion loss than the single-beam switch. However, when two beams in the double-beam switch are not symmetrical, the double-beam switch performances may deteriorate and become worse than the single-beam switch.

3.3.1.2 Cantilever beam design effect

The cantilever beam is the main part of the signal line in the lateral switch. Therefore, the design parameters (beam width, mass shape and length) of the cantilever beam have a significant role in determining the RF performance of the lateral switch.

Chapter 3: Lateral RF MEMS Switches

Figure 3-29, Figure 3-30 and Figure 3-31 compare measured and fitted S-parameters of Switch C, D and E, respectively. In Switch C, $w_1 = 2.0 \mu\text{m}$, $w_2 = 5 \mu\text{m}$. In Switch D, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$. And in Switch E, $w_1 = 2.4 \mu\text{m}$, $w_2 = 15 \mu\text{m}$. Other structure parameters are the same. In these switches, fixed electrode is separated from the ground line, as shown in Figure 3-39. All switches have an insertion loss of below 0.8 dB, a return loss of above 15 dB, and an isolation of above 17 dB up to 20 GHz. Fitted S-parameters agree well with measured results. Table 3-5 shows both the total resistance, R , and the inductance, L , decrease with the beam width, either w_1 or w_2 . The parasitic capacitance at the close-state, $C_{g,c}$, and at the open-state, $C_{g,o}$, of these three switches are the same. The open capacitance, C_s , increases slightly with the beam width. Therefore, the beam width mainly affects the beam resistance and the inductance, as predicted in Section 3.1.2.

Figure 3-29 Comparison between measured and fitted S-parameters of a single-beam switch with the solid mass (Switch C, $w_1 = 2.0 \mu\text{m}$, $w_2 = 5 \mu\text{m}$).

Chapter 3: Lateral RF MEMS Switches

Figure 3-30 Comparison between measured and fitted S-parameters of a single-beam switch with the solid mass (Switch D, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$).

Figure 3-31 Comparison between measured and fitted S-parameters of a single-beam switch with the hole mass (Switch E, $w_1 = 2.4 \mu\text{m}$, $w_2 = 15 \mu\text{m}$).

Chapter 3: Lateral RF MEMS Switches

Figure 3-32 Comparison of measured S-parameters between Switch C ($w_1 = 2.0 \mu\text{m}$) and Switch D ($w_1 = 2.4 \mu\text{m}$).

Figure 3-33 Comparison of measured S-parameters between Switch D (solid-mass, $w_2 = 5 \mu\text{m}$) and Switch E (hole-mass, $w_2 = 15 \mu\text{m}$).

Chapter 3: Lateral RF MEMS Switches

Figure 3-32 compares measured results between Switch C ($w_1 = 2.0 \mu\text{m}$) and Switch D ($w_1 = 2.4 \mu\text{m}$). It is found that the switch with $w_1 = 2.4 \mu\text{m}$ has slightly lower insertion loss and higher return loss than the switch with $w_1 = 2.0 \mu\text{m}$. This is because narrower cantilever beam results in larger beam resistance, R_l , and inductance, L , than the wider cantilever beam. The isolations of the two switches change marginally.

Figure 3-33 compares measured S-parameters between Switch D (solid-mass, $w_2 = 5 \mu\text{m}$) and Switch E (hole-mass, $w_2 = 15 \mu\text{m}$). The insertion loss of the hole-mass switch is lower than the solid-mass switch by about 0.1 dB. The return loss of the hole-mass switch is higher than the solid-mass switch by about 2.5 dB. This is because the hole-mass offers lower beam resistance R_l and inductance L compared to the solid-mass. The isolation of the hole-mass switch is slightly lower than the solid-mass switch since wider mass structure result in slightly larger open capacitances, C_s .

Figure 3-34 Comparison between measured and fitted S-parameters of switch F ($l_2 = 235 \mu\text{m}$).

Chapter 3: Lateral RF MEMS Switches

Figure 3-35 Comparison between measured and fitted S-parameters of switch G ($l_2 = 350 \mu\text{m}$).

Figure 3-36 Comparison of measured S-parameters between Switch F ($l_2 = 235 \mu\text{m}$) and Switch G ($l_2 = 350 \mu\text{m}$).

Chapter 3: Lateral RF MEMS Switches

When sum (l_1+l_2) and l_3 are kept constant, a change in the length of the fixed electrode, l_2 , affects the RF performance of the lateral switch due to the effect of the shunt coupling capacitance, C_g . Figure 3-34 and Figure 3-35 compares measured and fitted S-parameters of Switch F ($l_2 = 235 \mu\text{m}$) and Switch G ($l_2 = 350 \mu\text{m}$), respectively. For both switches, sum (l_1+l_2) and l_3 are $422 \mu\text{m}$ and $25 \mu\text{m}$, respectively. The measured S-parameters agree well with fitted results for both switches. Figure 3-36 compares measured S-parameters between Switch F and Switch G. At 10 GHz, the insertion loss increases from 0.37 dB to 0.41 dB when l_2 increases from $235 \mu\text{m}$ to $350 \mu\text{m}$, whereas the return loss increases from 21 dB to 22.7 dB. The isolations of two switches change marginally. Theoretically, the resistance, R , should decrease with l_2 . However, the resistance of Switch G is 4.3Ω at 10 GHz, which is larger than that of Switch F, 3.8Ω . That is because of larger contact resistance of Switch G. The threshold voltage of Switch G ($l_2 = 350 \mu\text{m}$) is 30 V and that of Switch F ($l_2 = 235 \mu\text{m}$) is 23 V. Therefore, when 40 V bias voltage is applied, the contact force of Switch G is smaller than that of Switch F, which results in higher contact resistance for Switch G. The parasitic capacitance at the close-state, $C_{g,c}$, increases from 70 fF to 77 fF when l_2 increases from $235 \mu\text{m}$ to $350 \mu\text{m}$. The inductance decreases slightly with l_2 . As discussed in Section 3.1.2, the increase of parasitic capacitance, $C_{g,c}$, results in increase of the return loss. Therefore, the return loss of Switch G is larger than Switch F.

3.3.1.3 Metal coating effect

The thickness of the metal coating affects the RF performance of lateral switches since it determines the switch resistance. Figure 3-37 (a) and (b) compare measured S-parameters of a single-beam switch with various thicknesses of Al coating at the close-

Chapter 3: Lateral RF MEMS Switches

(a) The insertion loss and return loss at the close-state

(b) The isolation at the open-state

Figure 3-37 Comparison of measured results of the single-beam switch with various thick Al coating (a) the insertion loss and the return loss, and (b) the isolation.

Chapter 3: Lateral RF MEMS Switches

state and open-state, respectively. The Al thickness is 0.8 μm for Switch H, 1.2 μm for Switch A and 1.5 μm for Switch I. At 10 GHz, the insertion loss decreases from 0.62 dB to 0.2 dB when the Al thickness increases from 0.8 μm to 1.5 μm . The main reason is the total resistance, $R_t + R_c$ is reduced from 5 Ω to 1.8 Ω due to thicker metal coating. It is noted that the return loss of Switch H with 0.8- μm -thick Al coating are larger than the other two switches with thicker metal coating. This conflicts with the fact that the return loss increases when the metal coating increases from 1.2 μm to 1.5 μm . It is found that a shunt conductance G ($=3.5 \times 10^{-4}$ S) is needed to add in the circuit model of Switch H to fit the measured S-parameters, but is unnecessary for the other two switches. This indicates that when 0.8- μm -thick Al is coated, the metal on sidewalls is too thin to isolate the silicon-core effect. The device silicon layer works as the substrate of the top metal strips, which causes larger parasitic capacitance, $C_{g,c}$ and more dielectric loss. Hence, the metal coating should be larger than 0.8 μm for low loss. The insertion loss of the switch decreasing with the metal thickness significantly means the switch loss is dominated by the conductor loss. The switch RF performance can be improved further by coating thicker metal.

3.3.1.4 Lifetime of the lateral switch

Resistive switches usually fail due to an excessive increase in electrical contact resistance. Generally failure occurs when the contact resistance is greater than 5 Ω , even though the cantilever beam remains deflecting and making contact. The lifetime study includes both cold and hot switching lifetime. The cold-switching refers to opening and closing the switch with zero RF signal level through the contact. On the other hand, the hot-switching refers to opening and closing the switch with a specified RF signal level

Figure 3-38 Measured S-parameters of Switch B with different switching cycles.

through the contact [2]. It is known that the lifetime of hot switching is shorter compared to the lifetime of cold switching due to larger heat dissipation. However, testing on the hot switching lifetime is currently unavailable because the RF testing equipment is relatively costly and cannot be exclusively occupied for a long time. Therefore, only testing on the cold switching lifetime of the lateral switch is carried out. The testing results shows that the cold switching lifetime exceeds million switching cycles (Figure 3-38). The insertion loss and the return loss of a double-beam switch deteriorate by 0.1 dB and 1.5 dB at 10 GHz respectively after one million cold switching cycles. The isolation changes marginally.

3.3.1.5 The lateral switch with a separate fixed-electrode

For the lateral switch design, the fixed electrode can be designed either as part of the ground line (combined electrode) or as a separate part (separate electrode), as shown in Figure 3-39. When there is a switch with separate electrodes in the real circuit, the bias

Chapter 3: Lateral RF MEMS Switches

network which utilizes DC blocking capacitors and RF choke inductors are necessary to decouple the RF signal from the DC actuation signal. This can be achieved in exactly the same way as those for the PIN diode switches [27]. In this experimental setup, one probe connecting to the high potential of an external power supply is put on the fixed electrode of the switch. The other probe connecting to the ground potential of the external power supply is put on the wafer chuck, not on the signal line. As a result, the cantilever beam can also be actuated without the coupling of the DC actuation signal.

Figure 3-40 compares measured S-parameters between Switch A (combined electrode) and Switch D (separate electrode). It shows the switch with the separate electrode can work at high frequencies too. Both switches have an insertion loss of below 1 dB and a return loss of above 15 dB up to 25 GHz. However, the isolation of Switch D is 14 dB at 25 GHz, whereas that of Switch A is 21 dB. From 0.05 GHz to 25 GHz, the isolation of Switch D is lower than Switch A by about 7 dB. That is because Switch D has larger open capacitance, C_s , as shown in Table 3-5. The open capacitance of Switch D is 13.2 fF, whereas that of Switch A is 6.5 fF. From Figure 3-39, it is found that except the end of the cantilever beam, part of the signal line also faces the input port in Switch D, which increases the open capacitance. Therefore, the isolation of Switch D can be improved by using the cantilever beam alone as the signal line of the switch part. It is noted that the parasitic capacitance, $C_{g,c}$, of Switch D of 22.6 fF, is less than Switch A of 28 fF, although Switch D has longer electrode part, l_2 , than Switch A. This is because the parasitic capacitance of Switch D is contributed by two capacitors in series. One is the capacitor between the cantilever beam and the separate electrode. The other is the capacitor between the separate electrode and the ground line.

Figure 3-39 SEM micrographs of a lateral switch with separate fixed-electrode.

Figure 3-40 Comparison of measured S-parameters between Switch D (separate electrode) and Switch A (combined electrode).

3.3.2 Mechanical measurements

3.3.2.1 Static behavior

Since the pull-in of the cantilever beam is sharp and sudden, accurate measurement of the threshold voltage required for reaching pull-in can be easily performed at wafer level using the standard electrical test equipment with a microscope.

Figure 3-41 shows the comparison of the measured and calculated threshold voltage, V_{th} of the lateral switch with various original gap distances, g_0 , where $l_1 = 220 \mu\text{m}$, $l_2 = 210 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, and $w_{Al} = 0 \mu\text{m}$. The threshold voltage, V_{th} increases with g_0 . The increase in g_0 by $0.5 \mu\text{m}$ increases the threshold voltage, V_{th} by about 2.5 V. The effect of $(l_2 / (l_1 + l_2))$ ratio on the threshold voltage, V_{th} is shown in Figure 3-42. The threshold voltage, V_{th} is $20 \pm 1 \text{ V}$ when the $(l_2 / (l_1 + l_2))$ ratio is within the range of 35 – 75 % before the metal coating. Figure 3-42 also shows the metal coating effect on the threshold voltage. When a $0.63\text{-}\mu\text{m}$ -thick Al is coated on the sidewalls of the lateral switch, the threshold voltage of the switch increases about 5 V. However, the measured results of the switch with $0.63\text{-}\mu\text{m}$ -thick Al on sidewalls do not fit so well to the calculation results compared to the switch without Al coating. The reason may be due to the residual stress introduced by the evaporated Al.

Figure 3-43 shows the comparison among measured, calculated and simulated displacement results of the free-end of a switch with $0.63 \mu\text{m}$ Al coated on sidewalls. The measurement method of the displacement of the free-end of the cantilever beam is as following. First, the lateral switch is fixed on a probe station, which has a microscope above it. A camera is connected with the microscope. Then, two micro-probes connected to an external power source are put on the two electrodes.

Chapter 3: Lateral RF MEMS Switches

After a bias voltage is applied, the camera takes a photo of the contact part once the cantilever beam becomes stable. Comparing the photo at some voltage with the photo at 0 V, we can calculate the displacement of the free-end of the cantilever beam. It can be seen that the displacement of the free-end of the cantilever beam increases with the applied bias voltage. When the bias voltage increases to 23.3 V, the cantilever beam is attracted to touch the contact tip rapidly. Therefore, the threshold voltage of this switch is 23.3 V. The measurement result is consistent with the calculated and the simulated result.

Figure 3-41 Comparison of measured and calculated threshold voltage V_{th} of the lateral switch with various g_0 ($l_1 = 220 \mu\text{m}$, $l_2 = 210 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0 \mu\text{m}$).

Chapter 3: Lateral RF MEMS Switches

Figure 3-42 Measured and calculated V_{th} with various $(l_2 / (l_1 + l_2))$ ratio with and without (w/o) Al coating ($l_1 + l_2 = 430 \mu m$, $l_3 = 10 \mu m$, $w_1 = 2.4 \mu m$, $w_2 = 5 \mu m$, $g_{Si} = 6 \mu m$).

Figure 3-43 Comparison of measured, calculated and simulated displacement of the free-end of the cantilever beam with $0.63 \mu m$ thick Al on sidewalls ($l_1 = 275 \mu m$, $l_2 = 165 \mu m$, $l_3 = 10 \mu m$, $w_1 = 2.4 \mu m$, $w_2 = 5 \mu m$, $w_{Al} = 0.63 \mu m$, $g_0 = 4.8 \mu m$, $d_0 = 2.8 \mu m$).

3.3.2.2 Dynamic behavior

The testing setup of the dynamic behavior of the lateral switch is illustrated in Figure 3-44. A square wave signal is applied to the fixed electrode of the switch; a serial resistor and 10 V DC voltage supply are connected across the movable electrode of the switch's signal path; a two-channel oscillograph is used to observe the driving signal as well as the waveform on the resistor.

A lateral switch with $l_1 = 275 \mu\text{m}$, $l_2 = 165 \mu\text{m}$, $l_3 = 10 \mu\text{m}$, $w_1 = 2.4 \mu\text{m}$, $w_2 = 5 \mu\text{m}$, $w_{Al} = 0.63 \mu\text{m}$, $g_{Si} = 6 \mu\text{m}$ and $d_{Si} = 4 \mu\text{m}$ is tested and the results are illustrated in Figure 3-45. The upper waveform in Figure 3-45 (a) and (b) is the square-wave driving signal while the lower waveform is the responding waveform of the current through the switch on the series resistor. The driving voltage is 35 V. Although the resistance of the resistor is fairly large ($1 \text{ M}\Omega$), the time delay due to this resistance is less than $1 \mu\text{s}$ since the parasitic capacitance is less than 40 fF . When the switch turns off, a strike-arc happened, resulting in a glitter in the waveform of the bias voltage, as shown in Figure 3-45 (b). The switching time is $35 \mu\text{s}$ and the release time is $36 \mu\text{s}$.

Figure 3-44 The sketch diagram of the testing setup for dynamic behavior of the lateral switch.

(a) the close-state

(b) the open-state

Figure 3-45 The experimental results of switching performance of a lateral switch (a) the close-state, (b) the open-state.

3.4 Summary

Different types of lateral switches for 50 MHz – 25 GHz applications are presented in this chapter. These includes single-beam and double-beam switches, switches with part of the ground line as a fixed electrode and switches with separate fixed electrode. All lateral switches are implemented using Si-core CPW and an electrostatic cantilever-actuator. A high-aspect-ratio cantilever beam with beam-mass structure is

Chapter 3: Lateral RF MEMS Switches

employed as the actuation part of the lateral switch. The design and circuit modelling as well as the mechanical design and modelling of the lateral switch have been presented. Comprehensive modelling and design of the lateral switches are verified by extensive testing of both RF response and mechanical behaviour. The measurements show that the optimized lateral switches have low insertion loss (< 1 dB), high return loss and isolation (> 20 dB) at 50 MHz to 25 GHz. The threshold voltage is less than 25 V. The switching speed is 35 μ s. The RF lifetime is more than one million switching cycles.

Table 3-7 summarizes the change in RF and mechanical characteristics of the lateral switch with the change in various geometrical parameters. There is a trade-off between the RF performance and the mechanical performance of the switch actuator. For example, when the beam length, l , decreases or the beam width, w_1 , of the cantilever beam increases, the RF performances become better. However, the threshold voltage and the switching speed increase at the same time. To obtain low threshold voltage (< 30 V) and good RF performance (the insertion loss < 1 dB, the return loss > 20 dB and isolation > 20 dB up to 25 GHz), the electrode part of the cantilever beam should be within the range of 35 – 75 % of the total length of the cantilever beam. The hole-mass is an effective method to reduce the insertion loss without increasing the threshold voltage. However, the width of the hole-mass cannot be too large since the isolation decreases with the mass width. The double-beam switch is another effective method to reduce the insertion loss and to maintain the mechanical performance. To obtain high isolation, only cantilever beam should serve as the signal line. Metal should be deposited as thick as possible to cover the switch structures since the conductor loss is the dominant factor of the insertion loss of the lateral switch.

Chapter 3: Lateral RF MEMS Switches

It is found that the lateral switches can provide comparable RF performance with the vertical switches. The main advantages of the lateral switches over the vertical switches are reliable mechanical performance and simple fabrication process. It is difficult to control the threshold voltage of a vertical switch due to the residual stress of the metal thin film structures. However, the measured threshold voltage of the lateral switch is closer to the designed value because of the excellent mechanical properties of the single crystal silicon. Generally, the fabrication process of the vertical switch needs five to nine masks. However, the fabrication process of the lateral switch only needs one to three masks. Comparing to other MEMS lateral switches, these lateral switches have lower power consumption, faster switching speed, greater RF performance and high-frequency wide-band operation, as shown in Table 2-1 of Section 2.2.

Table 3-7 Variation trends of switch characteristics with increase of cantilever beam parameters.

	Insertion loss	Return loss	Isolation	Threshold voltage	Switching time	Release time
Total length, l	↑	↓	↑	↓	↓	↑
Ratio, $l_2/(l_1+l_2)$	↑	↓	↑	↓ to min then ↑	↓ to min then ↑	↓
Beam width, w_1	↓	↑	-	↑	↑	↓
Mass width, w_2	↓	↑	↓	-	↑	↓
Metal thickness w_m	↓	↑	↑	↑ to max Then ↓	↑ to max then ↓	↓
Electrode gap, g_0	↓	↑	↑	↑	↑	↓
Contact gap, d_0	↑	↓	↑	-	↑	↓

CHAPTER 4

INTEGRATED SWITCHING CIRCUITS

The objective of this chapter is to investigate silicon-core coplanar waveguide (Si-core CPW) transmission line and integrated switching circuits theoretically and experimentally. The design of the Si-core CPW is presented first. Then, the attenuation related to different substrate materials, core materials and process variations are analyzed. The experimental results verify that the Si-core CPW support quasi-TEM mode propagation up to 25 GHz with attenuation less than 4 dB/cm.

Based on the Si-core CPW and the lateral switches, single-pole-multiple-throw (SPMT) switching circuits are designed, fabricated and measured. First, an in-line single-pole-double-throw (SP2T) switching circuit with two cantilever beams in a line is studied using circuit analysis and full-wave EM simulation. Then, two unique SP2T switching circuits are derived. One of them with two cantilever beams arranged in parallel shows lower insertion loss because of the better circuit matching. The other with only one cantilever beam has smaller circuit size. An extension of this design idea on the single-pole-three-throw (SP3T) and the single-pole-four-throw (SP4T) switching circuits are demonstrated. Experimental results are discussed. The advantages of these SPMT switching circuits are low loss, high isolation and small footprint.

4.1 Si-Core Transmission Line

At RF and microwave frequencies, transmission lines are used to carry electrical signal from one point to another. Transmission lines have to be impedance matched, that is, all transmission lines in a circuit are designed to be $50\ \Omega$ of characteristic impedance to prevent unwanted reflections in high frequency circuits. To do this, the signal line and the ground lines are arranged in a certain configuration where dielectric is in between. Coplanar waveguide (CPW) is a planar transmission line which is compatible with microwave and millimeter wave integrated circuit technology, as shown in Figure 4-1 (a). CPW is relatively insensitive to variations in substrate thickness. It has low radiation loss and allows circuit elements to be easily connected in shunt as well as in series. These characteristics have made CPW an exceptional candidate for high-frequency low-cost high-performance circuits.

In coplanar lines, the field is tightly concentrated in the apertures between conductors, leading to current crowding for the conventional thin-film techniques. When the conductor thickness is larger, the current can be distributed and the loss can be reduced. This makes it possible to work in high power applications due to the increased conduction interface. A new type of CPW transmission line with Si-core and metal overcoat is introduced in this section, in which the signal and ground lines' thickness is 50 to 75 μm . The Si-core CPW transmission line demonstrates all advantages that conventional thin-film CPW has. These include balanced propagation and coplanar configuration. The Si-core CPW can be implemented using a silicon back-bone structure patterned in desired shapes followed by a metal overcoat. This section focuses on the design and characterization of the Si-core CPW transmission line.

Chapter 4: Integrated Switching Circuits

4.1.1 Design of the Si-core CPW

As shown in Figure 4-1, the Si-core CPW has geometry similar to the conventional thin-film CPW. It consists of three parallel plate waveguides. The difference is that each waveguide of the Si-core CPW is formed from a single-crystal-silicon plate with thickness of 50 to 75 μm which is coated with a thin layer of metal on the top and sidewalls. RF signal can then propagate along the metal on the top surface and also along sidewalls of the transmission line. The core material can either be low resistivity silicon ($\rho \leq 10 \Omega\cdot\text{cm}$) or high resistivity silicon ($\rho \geq 1000 \Omega\cdot\text{cm}$). The substrate can either be glass in Si-on-glass (SiOG) - based process or high resistivity silicon in silicon-on-insulator (SOI) - based process. The recesses formed in the substrate under waveguides serve three purposes - to help the release of movable structures in the RF MEMS circuits, to avoid metal connection to short circuit after metal coating and to reduce the dielectric loss of the transmission line.

Figure 4-1 Schematic cross-sectional view of the CPW.

Chapter 4: Integrated Switching Circuits

The characteristic impedance of CPW depends significantly on its geometrical parameters, including the center conductor width, S , the ground width, G , and the conductor separation, W , and the substrate material properties, such as the substrate thickness, H , and the relative permittivity, ϵ_r . In the Si-core CPW, other process parameters also affect the characteristic impedance. These include the thickness, T , and the resistivity, ρ , of the core material, the depth of the recesses, h_r , the undercut width, w_r , the thickness of the metal on the top, t_t , and at sidewalls, t_s , as shown in Figure 4-1 (b).

The design of the Si-core CPW involves three steps. First, based on process requirements, some parameter values are determined, including the substrate parameters, H and ϵ_r , the silicon core thickness, T , the recess depth, h_r , and the undercut width, w_r . Unless otherwise stated, in the following simulation and analysis, $H = 500 \mu\text{m}$, $\epsilon_r = 4.6$, $T = 50$ to $80 \mu\text{m}$ and $w_r = 1.6h_r$ to $1.8h_r$. To accommodate $150 \mu\text{m}$ -pitch ground-signal-ground coplanar probes, the distance between the two ground lines, $S + 2W$, is chosen to be $200 \mu\text{m}$ and the ground line width, G , is chosen within the range of $100 \mu\text{m}$ to $400 \mu\text{m}$. Second, the characteristic impedance, Z_0 , of the CPW is approximated by [125]

$$Z_0 = \frac{40\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k_1)}{K(k_1')} \quad (4-1a)$$

where

$$\epsilon_{eff} = 1 + \frac{\epsilon_r - 1}{2} \frac{K(k_2')K(k_1)}{K(k_2)K(k_1')} \left[1 + \frac{T}{2W} \frac{K(k_1)}{K(k_1')} \right] + \frac{T}{2W} \frac{K(k_1)}{K(k_1')} \left[2 + \frac{T}{2W} \frac{K(k_1)}{K(k_1')} \right] \quad (4-1b)$$

$$k_1 = \frac{S + 2W + 2G}{S + 2W} \sqrt{\frac{(S + 2W)^2 - S^2}{(S + 2W + 2G)^2 - S^2}} \quad (4-1c)$$

Chapter 4: Integrated Switching Circuits

$$k_2 = \frac{\sinh\left[\frac{\pi(S+2W+2G)}{4H}\right]}{\sinh\left[\frac{\pi(S+2W)}{4H}\right]} \sqrt{\frac{\sinh\left[\frac{\pi(S+2W)}{4H}\right] - \sinh\left(\frac{\pi S}{4H}\right)}{\sinh\left[\frac{\pi(S+2W+2G)}{4H}\right] - \sinh\left(\frac{\pi S}{4H}\right)}} \quad (4-1d)$$

$$k_n' = \sqrt{1 - k_n^2} \quad n = 1, 2 \quad (4-1e)$$

where K is the complete elliptic integrals of the first kind, ϵ_{eff} is the effective relative permittivity, ϵ_r is the relative permittivity of the substrate material. The center conductor width, S , and the conductor separation, W , can be given to get the required characteristic impedance. Finally, three-dimensional (3D) finite-element-method (FEM) simulation is carried out using Ansoft's HFSS to adjust the dimension values of the center conductor width, S , the ground width, G , and the conductor separation, W . In the simulation model of Ansoft's HFSS, the material properties of every layer are carefully chosen to achieve a good match between the measured and theoretical results. The width of the signal line, S , and the width of the ground lines, G , are adjusted based on the simulation results to obtain the required characteristic impedance.

Figure 4-2 (a) shows the simulated vector electric field (E-field) distribution of the Si-core CPW at 20 GHz. The electric field radiates from the center signal conductor to the two ground conductors. The dominant mode for this kind of transmission line is quasi-transverse electromagnetic (TEM) mode, which is similar to the conventional thin-film CPW transmission line. It is found that there is strong penetration of the E-field into the substrate and the silicon core. Therefore, the material properties of the substrate and the core have significant effects on the performance of the Si-core CPW. The simulated characteristic impedance versus frequency of a Si-core CPW is shown in Figure 4-2 (b). The characteristic impedance of this Si-core CPW is about 51.5Ω when $S/W/G$ are equal

Chapter 4: Integrated Switching Circuits

(a)

(b)

Figure 4-2 (a) vector E-field distribution, and (b) characteristic impedance of the Si-Core CPW

(S/W/G = 110/45/300 μm , $h_r = 12 \mu\text{m}$, $w_r = 20 \mu\text{m}$).

Chapter 4: Integrated Switching Circuits

to 110/45/300 μm , $h_r = 12 \mu\text{m}$, $w_r = 20 \mu\text{m}$, $T = 50 \mu\text{m}$, $H = 500 \mu\text{m}$, $\epsilon_r = 4.6$, $t_t = 1 \mu\text{m}$ and $t_s = 0.5 \mu\text{m}$ respectively. The characteristic impedance decreases with frequency slowly.

4.1.2 Losses of the Si-core CPW

The attenuation, α , is an important characteristic indicating the efficiency of the coplanar lines transmit power. The attenuation of the Si-core CPW consists of three losses, namely conductor loss, α_c , dielectric loss, α_d , and radiation loss, α_r .

4.1.2.1 Conductor loss

The conductor loss, α_c , resulting from the finite conductivity of the metal, in Np/cm is given by

$$\alpha_c = \frac{R}{2Z_0} \quad (4-2)$$

Therefore, the conductor loss is determined by the line unit resistance and the characteristic impedance. Decreasing the line unit resistance or increasing the line characteristic impedance can reduce the conductor loss. Figure 4-3 plots the conductor loss, α_c , as a function of the line unit resistance, R , with the characteristic impedance, Z_0 , of the transmission line as a parameter. When $Z_0 = 50 \Omega$ and $R = 40 \Omega/\text{cm}$, the conductor loss is 3.5 dB/cm. When Z_0 decreases to 42 Ω , the conductor loss increases to 4.1 dB/cm.

In the Si-core CPW, the line unit resistance, R , is determined by the metal resistance of the signal line, $R_{s,m}$ and ground lines, $R_{g,m}$. They are expressed as

Chapter 4: Integrated Switching Circuits

Figure 4-3 Calculated conductor loss curves with respect to the line unit series resistance and characteristic impedance.

$$R_{s,m} = \begin{cases} R_{s,dc} = \frac{1}{\sigma(2t_s T + t_t S)} & (\text{if } R_s(f) \leq R_{s,dc}) \\ R_s(f) = \frac{1}{\sigma\delta_s [2T(1 - e^{-t_s/\delta_s}) + S(1 - e^{-t_t/\delta_s})]} & (\text{if } R_s(f) > R_{s,dc}) \end{cases} \quad (4-3a)$$

$$R_{g,m} = \begin{cases} R_{g,dc} = \frac{1}{\sigma(2t_s T + t_t G)} & (\text{if } R_g(f) \leq R_{g,dc}) \\ R_g(f) = \frac{1}{\sigma\delta_s [2T(1 - e^{-t_s/\delta_s}) + G(1 - e^{-t_t/\delta_s})]} & (\text{if } R_g(f) > R_{g,dc}) \end{cases} \quad (4-3b)$$

where T and S are the thickness and the width of the signal line; t_s and t_t are the metal thickness on the top and sidewalls of the transmission line, as shown in Figure 4-1 (b); σ is the conductivity of the metal and δ_s is the skin depth, which is determined by Eq. (3-5).

Chapter 4: Integrated Switching Circuits

At low frequency range, the resistance is determined by the DC resistance, $R_{s,dc}$ and $R_{g,dc}$. However, when the frequency increases, the current is crowded outside the surface of the conductor. The line resistance is determined by the $R_s(f)$ and $R_g(f)$ at high frequency range.

4.1.2.2 Dielectric loss

The dielectric loss, α_d , is due to the displacement current in the guiding medium of the transmission line. The dielectric loss, α_d , in Np/cm is given by [27]

$$\alpha_d = \frac{1}{2} G Z_0 = \frac{\omega \sqrt{\mu_0 \epsilon_0 \epsilon_r} \tan \delta}{2} * \frac{1}{100} \quad (4-4a)$$

where $\tan \delta$ is the loss tangent of the guiding medium. The loss tangent specifies the lossy nature of the dielectric material and is defined as

$$\tan \delta = \frac{\sigma_d}{\omega \epsilon_0 \epsilon_r} \quad (4-4b)$$

where σ_d is the electrical conductivity of the dielectric material. Electromagnetic waves experience higher loss when they propagate through a dielectric medium with a larger loss tangent or conductivity. Table 4-1 lists material properties of four dielectric materials used in this thesis and their dielectric loss at 20 GHz. It can be seen that the dielectric loss sorted in the ascending sequence is air, glass, high resistivity silicon (HRSi) and low resistivity silicon (LRSi).

Figure 4-4 plots the dielectric loss, α_d , as a function of the unit shunt conductance, G , with the characteristic impedance, Z_0 , as a parameter. The dielectric loss increases with the unit conductance and the characteristic impedance. When $Z_0 = 50 \, \Omega$ and $G = 0.005 \, \text{S/cm}$, the dielectric loss is 1.08 dB/cm. When G increases to 0.02 S/cm, the dielectric loss increases to 4.34 dB/cm.

Chapter 4: Integrated Switching Circuits

Table 4-1 Dielectric properties of the fabrication materials

Material	ϵ_r	$\tan \delta$	σ_d (S. m ⁻¹)	α_d (dB/cm)
Glass	4.6	0.003	-	0.12
HRSi	11.9	-	0.05	0.24
LRSi	11.9	-	100	474.30
Air	1.0	0	-	0

Figure 4-4 Calculated conductor loss curves with respect to the line unit shunt conductance and characteristic impedance.

Chapter 4: Integrated Switching Circuits

4.1.2.3 Radiation loss

In addition to the conductor loss and the dielectric loss, radiation from unwanted parasitic modes and coupling of power to surface waves contribute to radiation loss, α_r . The parasitic mode in the CPW is the odd mode with anti-phase voltages in the two slots, which is excited at the discontinuities. Radiation from this mode can be minimized by maintaining symmetry of the circuits and thus avoiding its excitation by using air-bridges or bond wires at periodic intervals to short it out. For any CPW with a finite substrate thickness, the surface wave modes of the substrate are also responsible for the leakage. Surface waves are the guided modes of a dielectric slab with finite thickness. Excitation of surface modes depends on the polarizations and symmetries of the transmission line.

Figure 4-5 plots the radiation loss, α_r , as a function of the frequency, f , with the substrate permittivity, ϵ_r , as a parameter. In this scenario, $H = 500 \mu\text{m}$, $S = 110 \mu\text{m}$, $W = 45 \mu\text{m}$ and $G = 300 \mu\text{m}$. It shows that the radiation loss is substantially affected by the permittivity of the substrate at high frequency range. The higher the permittivity, the faster the radiation loss increases with frequency. For instance, at 40 GHz, when $\epsilon_r = 4.6$ (glass), the radiation loss of the substrate is 0.006 dB/cm whereas when $\epsilon_r = 11.9$, the radiation loss of the substrate increases to 0.046 dB/cm. However, comparing with the conductor loss and the dielectric loss, the radiation loss is negligible when frequency is below 40 GHz. The radiation losses dominate for frequencies over 200 GHz for coplanar lines with dimensions of the order of a few tens of microns, as experimentally demonstrated in [126].

Figure 4-5 Calculated radiation loss curves with respect to frequency and substrate permittivity.

4.1.3 Effect of the material properties and process variations

Based on the equivalent circuit model of the Si-core CPW, some factors affect the RF properties of the Si-core CPW, such as the substrate material, the core material and the process variations.

4.1.3.1 Effect of the substrate material

Figure 4-6 compares the simulation results of the Si-core CPW on glass and on high resistivity silicon substrate. The dielectric properties of the glass and the high resistivity silicon have already been listed in Table 4-1. The core material is the low resistivity silicon with $\rho = 1 \text{ } \Omega\cdot\text{cm}$. The attenuation, α , and the shunt conductance, G , are extracted from simulated S-parameters. As elaborated in Section 4.1.2, the substrate is the main contributory factor to the dielectric loss through the shunt conductance, G .

Chapter 4: Integrated Switching Circuits

Figure 4-6 Comparison of simulation results between the Si-core CPW on glass and HRSi substrate ($S/W/G = 110/45/300 \mu\text{m}$, $h_r = 12 \mu\text{m}$, and $w_r = 20 \mu\text{m}$, LRSi core) (a) attenuation, and (b) shunt conductance G .

Chapter 4: Integrated Switching Circuits

Figure 4-6 (a) shows that a 50 Ω Si-core CPW on the glass substrate has lower attenuation than that on the high resistivity silicon substrate. According to the analysis in section 4.1.2.2, the conductance, G , of the high resistivity silicon is larger than the glass. This is verified by Figure 4-6 (b). When the frequency increases, the shunt conductance, G , on the HRSi substrate increases faster than the glass substrate. The difference of the conductance between them becomes larger for frequency above 5 GHz.

4.1.3.2 Effect of the core material

The effect of the core material is shown in Figure 4-7. In the simulation models, the substrate is 500- μm -thick glass. S/W/G are 110/45/300 μm . h_r , w_r , and T are 12 μm ,

Figure 4-7 Comparison of the RF properties of Si-core CPW with different core resistivity (S/W/G = 110/45/300 μm , h_r = 12 μm , and w_r = 20 μm).

Chapter 4: Integrated Switching Circuits

Figure 4-8 Comparison of the distributed RLGC parameters of the Si-core CPW on glass substrate (a) capacitance and inductance, (b) conductance and resistance.

Chapter 4: Integrated Switching Circuits

20 μm and 50 μm respectively. Figure 4-7 shows that the characteristic impedance, Z_0 , increases slightly from 48 Ω to 50 Ω when the core material changes from the low resistivity silicon to the high resistivity silicon. It also shows that the LRSi-core CPW has higher attenuation than the HRSi-core CPW. This difference becomes larger when the frequency increases.

The RLGC parameters have been extracted and compared in Figure 4-8 to give a full understanding on the core material. Figure 4-8 (a) shows that when the core resistivity of the Si-core CPW increases, the unit inductance, L , increases a little and the unit capacitance, C , decreases a little. Therefore, the characteristic impedance which is determined by $\sqrt{L/C}$ at high frequencies (> 5 GHz), increases. The effect of the core material on the unit resistance, R , and the unit shunt conductance, G , is shown in Figure 4-8(b). The unit resistance, R , of the LRSi-core CPW is slightly less than the HRSi-core CPW when the frequency is below 3 GHz and becomes slightly larger than the HRSi-core CPW when the frequency is above 3 GHz. The shunt conductance, G , of the LRSi-core CPW is significantly larger than that of the HRSi-core CPW, especially at high frequencies. This results in higher dielectric loss for LRSi-core CPW than HRSi-core CPW. Therefore, the attenuation of LRSi-core CPW is larger than the HRSi-core CPW. This difference increases with frequency.

4.1.3.3 Effect of the process variations

In addition to the geometrical dimensions, the types of the substrate material and the core material, the RF properties of the Si-core CPW are also affected by the process variations. These include the transmission line thickness, T , the etching depth of the glass recesses, h_r , and the undercut width, w_r , as shown in Figure 4-9.

Chapter 4: Integrated Switching Circuits

The characteristic impedance, Z_0 , of a Si-core CPW is reduced from $55\ \Omega$ to $44\ \Omega$ when the transmission line thickness, T , increases from $50\ \mu\text{m}$ to $80\ \mu\text{m}$, as shown in Figure 4-10 (a). This is, because an increase in the conductor thickness results in an increase in the line unit capacitance, C , which reduces the characteristic impedance. Figure 4-10 (b) shows that the attenuation slightly decreases with an increase in the conductor thickness. This is because the surface current is distributed in the larger area, which leads to the lower conductor loss.

Figure 4-11 (a) and (b) show that when the substrate is etched more, that is with larger w_r and h_r , the characteristic impedance of the Si-core CPW increases from $47.6\ \Omega$ to $51.4\ \Omega$, and the attenuation slightly decreases. This is because when the connection of the conductor to the substrate is smaller, there is smaller wave penetration into the substrate, which leads to smaller unit capacitance and smaller dielectric loss.

Compared to the slight change of the attenuation, the characteristic impedance of the Si-core CPW is significantly affected by the process variations. Therefore, the process control is important for the RF properties of the Si-core CPW, in particular the characteristic impedance, which determines the impedance matching of the RF circuits.

Figure 4-9 The schematic of cross sectional view of a Si-core CPW transmission line.

Chapter 4: Integrated Switching Circuits

(a) Characteristic impedance

(b) Attenuation

Figure 4-10 Simulation results of HRSi-core CPWs with various conductor thickness, T .
($S/W/G = 110/45/300 \mu\text{m}$)

Chapter 4: Integrated Switching Circuits

(a) Characteristic impedance Z_0

(b) Attenuation

Figure 4-11 Simulation results of HRSi-core CPWs with various undercut dimensions.

(S/W/G = 110/45/300 μm)

4.1.4 Experimental results and discussions

The RF responses of the Si-core CPW have been measured using the HP 8510C Vector Network Analyzer with tungsten-tip 150 μm - pitch Cascade Microtech ground-signal-ground coplanar probes. The system is calibrated using the standard short-open-load-through (SOLT) on-wafer calibration technique. A 5-mm plastic plate is placed between the probe chuck and the sample to remove higher order modes of propagation. All experiments are performed in the room environment without any packaging. A SEM micrograph of a Si-core CPW coated with 1- μm -thick gold (Au) is shown in Figure 4-12. The thickness of the transmission line, T , is 62 μm and the length, L , is 1 mm.

Figure 4-12 SEM micrograph of a 1-mm-long Si-core CPW transmission line.

Chapter 4: Integrated Switching Circuits

4.1.4.1 Comparison between simulation results and measurement results

Figure 4-13 compares the measurement results with the post-simulation results of a 1-mm-long HRSi-core CPW on glass. The S/W/G are 110/45/400 μm . The transmission line is 62- μm -thick. The glass cavity parameters, h_r and w_r , are about 6 μm and 10 μm , respectively. In the post-simulation model of HFSS, all geometrical parameters are set based on the experimental values. For example, the metal on the top and sidewalls are 1 μm and 0.3 μm , respectively. The metal spreads on glass. Figure 4-13 shows that the simulation results are in good agreement with the measurement results. The characteristic impedance of the glass-substrate, HRSi-core CPW is about 47 Ω when the frequency is above 10 GHz. The attenuation increases with frequency, which is 4 dB/cm at 25 GHz.

Figure 4-13 Comparison of the measurement and the simulation results of a HRSi-core CPW on a glass substrate ($T = 62 \mu\text{m}$, $h_r \approx 6 \mu\text{m}$, $w_r \approx 10 \mu\text{m}$ and 1- μm -thick Au coating).

Chapter 4: Integrated Switching Circuits

Figure 4-14 Comparison of the measured and the simulated RLGC parameters of a HRSi-core CPW on a glass substrate (a) L and C , and (b) R and G .

Chapter 4: Integrated Switching Circuits

Table 4-2 Comparison of the simulated and measured attenuation contributed by the unit resistance and the conductance of the glass-based HRSi-core CPW at 20 GHz.

	Z_0 (Ω)	R (Ω/cm)	G (S/cm)	α_c (dB/cm)	α_d (dB/cm)	α (dB/cm)
Measurement	47.0	37.6	0.0017	3.48	0.34	3.82
Simulation	46.8	35.2	0.002	3.27	0.4	3.67

The unit RLGC parameters of simulation results and measurement results are compared in Figure 4-14. The measured unit RLGC values match well with the simulated results. The unit inductance, L , and the unit capacitance, C , are kept constant from 10 to 25 GHz, which are 2.85 nH/cm and 1.3 pF/cm, respectively, as shown in Figure 4-14 (a). The resistance, R , and shunt conductance, G , increase with the frequency, as shown in Figure 4-14 (b). Table 4-2 compares simulated and measured attenuation due to the unit resistance, R , and the shunt conductance, G , of the HRSi-core CPW on glass at 20 GHz. The measured conductance, G , is 0.0017 S/cm, resulting in the dielectric loss, α_d , of 0.34 dB/cm. The measured resistance, R , of 37.6 Ω/cm contributes to the conductor loss, α_c , of 3.48 dB/cm. The conductor loss is nine times higher than the dielectric loss. Therefore, the large unit resistance, R , is the dominant factor of the attenuation of the Si-core CPW.

By investigating the fabrication process in Chapter 5, the large unit resistance is due to low quality metal deposition. The metal is deposited using E-beam evaporation. Generally, the E-beam evaporation has poor step coverage. The metal coated on sidewalls is found to be only 1/3 of the metal coated on the top surface. Therefore, only 3000-4000 Å gold can be coated on sidewalls when 1- μm -thick gold is deposited on the top of silicon structures. On the other hand, the surface current of the proposed Si-core CPW is

Chapter 4: Integrated Switching Circuits

mainly concentrated on sidewalls of the apertures, as shown in Figure 4-2 (a). Therefore, more loss is caused by the thin metal coating of sidewalls. The increase of the shunt conductance, G , caused by the metal spreading on the substrate during E-beam evaporation is very small. Compared to the conductor loss, the dielectric loss is negligible.

4.1.4.2 Effect of the geometrical parameters

The performance of the Si-core CPW depends on the geometrical parameters significantly, including the signal width, S , the ground width, G , and the conductor separation, W . Four 1-mm-long LRSi-core CPW with various $S/W/G$ are fabricated on glass and measured. Their $S/W/G$ parameters are summarized in Table 4-3. Note that $S+2W$ and G are the same for Design A, B and C. Design D is optimized using Ansoft HFSS, whose simulated characteristic impedance is close to 50 Ω . The other parameters are $T \approx 50 \mu\text{m}$, $h_r \approx 6 \mu\text{m}$ and $w_r \approx 10 \mu\text{m}$.

The characteristic impedance, Z_0 , and the attenuation, α , extracting from measured S-parameters are shown in Figure 4-15 (a) and Figure 4-15 (b), respectively. As shown in Figure 4-15 (a), the variation of the characteristic impedance of the Si-core CPW is larger when the frequency is below 5 GHz, indicating slow-wave mode propagation. However, when the frequency rises above 5 GHz, the characteristic impedance, Z_0 , reduces gradually for all structures, indicating that the quasi-TEM mode propagation is supported above 5 GHz. In quasi-TEM mode propagation, the characteristic impedance of the transmission line is inversely proportional to the square root of the line capacitance. When the space between the signal line and the ground line, W , is smaller, the unit inductance, L , is less and the unit capacitance, C , is larger, which lead to smaller characteristic impedance. This tendency is observed in Design A, B and C.

Chapter 4: Integrated Switching Circuits

At the high frequency, impedance matching is important to minimize signal oscillations which are caused by the reflection of the electromagnetic wave at the impedance discontinuity. Therefore, it is most desirable to design a transmission line with the characteristic impedance of 50 Ω . Design D achieves the characteristic impedance of about 50 Ω at 5-25 GHz. Figure 4-15 (b) shows that the attenuation of the Si-core CPW increases with the signal line width, S . When $S+2W$ is a constant, the Si-core CPW with wider signal line shows larger attenuation. That is because more electromagnetic field leaks into the substrate, e. g. dielectric loss is larger. However, Design D with $S/W/G = 110/45/400$ μm has lower attenuation than the design C with $S/W/G = 60/320/150$ μm . That is because the sum ($S+2W$) of Design C is larger than the glass substrate thickness of 500 μm , whereas the sum ($S+2W$) of Design D is much less than 500 μm . This leads to larger frequency dispersion and radiation loss in Design C compared to Design D. Therefore, geometrical parameters of the Si-core CPW must be adjusted to obtain the desired characteristic impedance, at the same time, suppress the unwanted radiation loss and the frequency dispersion when designing the Si-core CPW.

Table 4-3 Geometrical parameters of four 1-mm-long Si-core CPWs.

Design No.	Signal, S (μm)	Space, W (μm)	Ground, G (μm)	Sum, $S+2W$ (μm)
A	680	10	150	700
B	300	200	150	700
C	60	320	150	700
D	110	45	400	200

Chapter 4: Integrated Switching Circuits

(a)

(b)

Figure 4-15 Measured results of 1-mm-long LRSi-core CPWs on glass with different dimensions (1- μm -thick Au was coated) (a) characteristic impedance and (b) attenuation.

4.1.4.3 Effect of the material properties

Both the substrate material and the core material affect the RF performance of the Si-core CPW.

The effect of the substrate material on the Si-core CPW is illustrated in Figure 4-16 and Figure 4-17. For the SOI-based LRSi-core CPW, S/W/G are 66/67/100 μm . The substrate is 500- μm -thick high resistivity silicon. The core material is 35- μm -thick low resistivity silicon. 2- μm -thick thermal oxide is between the substrate and the device silicon layer. 1.2- μm -thick Al is coated. For the glass-based LRSi-core CPW, S/W/G are 110/45/400 μm . The substrate is 500- μm -thick glass. The core material is 60- μm -thick low resistivity silicon. $h_r \approx 6 \mu\text{m}$, $w_r \approx 10 \mu\text{m}$. 1- μm -thick gold is coated. The measured unit RLGC parameters, the characteristic impedance and the attenuation are extracted from measured S-parameters. The fitted unit RLGC parameters are fitted from the measured RLGC parameters. The fitted attenuation and the fitted characteristic impedance are calculated from the fitted RLGC parameters. It is found that the fitted attenuation and characteristic impedance agree well with the measured results. As expected in section 4.1.3.1, the SOI-based CPW has larger shunt conductance than the glass-based CPW, especially at high frequencies range. Therefore, the SOI-based CPW has higher dielectric loss than the glass-based CPW, as shown in Figure 4-17. It is noted that up to 13 GHz, the resistance of the SOI-based CPW is less than the glass-based CPW due to thicker metal coating. When the frequency is above 13 GHz, both the resistance and the conductance of the SOI-based CPW arise suddenly, resulting in larger attenuation than the glass-based CPW, as shown in Figure 4-16.

Figure 4-16 Comparison of attenuation of LRSi-core CPW on SOI and glass substrate.

Figure 4-17 Comparison of resistance and conductance of LRSi-core CPW on SOI and glass substrate.

Chapter 4: Integrated Switching Circuits

The effect of the core material of the Si-core CPW is illustrated in Figure 4-18 and Figure 4-19. S/W/G are 110/45/400 μm . The substrate is 500- μm -thick glass. $h_r \approx 6$ μm , $w_r \approx 10$ μm and 1- μm -thick Au is deposited. The thickness of waveguides of both Si-core CPWs is about 60 μm . the unit capacitance of the LRSi-core CPW is 1.33 pF/cm, which is slightly larger than that of the HRSi-core CPW of 1.30 pF/cm. However, as expected in Section 4.1.3.2, the inductance of the HRSi-core CPW is larger than the LRSi-core CPW. They are 2.85 nH/cm and 2.26 nH/cm, respectively. As a result, the characteristic impedance of the HRSi-core CPW of 47 Ω is larger than that of the LRSi-core CPW of 41.2 Ω , as shown in Figure 4-18. Figure 4-19 shows that the unit shunt conductance, G , of the HRSi-core CPW is less than that of the LRSi-core CPW, resulting in lower dielectric loss. The unit resistance, R , of the HRSi-core CPW is significantly lower than the LRSi-core CPW, resulting in lower conductor loss. Therefore, the HRSi-core CPW has lower attenuation than the LRSi-core CPW, as shown in Figure 4-19.

Table 4-4 compares measured and fitted RLGC parameters, the characteristic impedance, the attenuation between the SOI-based LRSi-core CPW, the glass-based LRSi-core CPW and the glass-based HRSi-core CPW at 20 GHz. It can be seen that glass-based HRSi-core CPW has the lowest resistance, conductance and attenuation. The conductor loss is the dominant factor of the attenuation. Thicker metal should be coated to reduce the attenuation of the Si-core CPW.

Based on this study, it can be concluded that to achieve the low-loss Si-core CPW, some useful guidelines are (i) depositing sufficiently thick metal and improving the step coverage of the metal deposition; (ii) using low loss substrate, such as glass; and (iii) using high resistivity silicon as the core material.

Chapter 4: Integrated Switching Circuits

Figure 4-18 Comparison of characteristic impedance and attenuation between the HRSi-core CPW and the LRSi-core CPW on glass.

Figure 4-19 Comparison of resistance and conductance between the HRSi-core CPW and the LRSi-core CPW on glass.

Chapter 4: Integrated Switching Circuits

Table 4-4 Comparison of measured and fitted RLGC values and attenuations of Si-core CPW with different substrate materials and core materials at 20 GHz.

CPW parameters	SOI-based LRSi-core		Glass-based LRSi-core		Glass-based HRSi-core	
	Measured	Fitted	Measured	Fitted	Measured	Fitted
R (Ω/cm)	69.7	65.1	53	53	37.6	37.4
L (nH/cm)	4.1	4.1	2.26	2.29	2.85	2.83
G (S/cm)	0.012	0.011	0.007	0.006	0.0017	0.0014
C (pF/cm)	1.95	1.95	1.33	1.33	1.30	1.30
Z_0 (Ω)	45.9	46.2	41.2	41.5	47	46.7
α_c (dB/cm)	6.59	6.11	5.58	5.55	3.48	3.48
α_d (dB/cm)	2.39	2.37	1.25	1.08	0.34	0.28
α (dB/cm)	10.04	8.48	6.88	6.63	3.82	3.76

4.2 Integrated Switching Circuits

With the configuration of the Si-core CPW and lateral switches, the microwave switching circuits can be designed and fabricated. In chapter 3, lateral switches have been developed, which can only switch one RF signal ON or OFF. However, RF signal often must be switched between different destinations, such as switched filter banks, multi-bit true-time-delay phase shifters and reconfigurable antennas. A straightforward application of the Si-core CPW and the lateral RF MEMS switches is the single-pole-multiple-throw (SPMT) switching circuit. The basic SPMT switching circuits include single-pole-

Chapter 4: Integrated Switching Circuits

double-throw (SP2T), single-pole-three-throw (SP3T) and single-pole-four-throw (SP4T) switching circuits. Generally, m lateral switches are incorporated in a $(m+1)$ port devices, which constitutes a SPMT switching circuit. When the SPMT switching circuit works, one switch is closed and the remaining $(m-1)$ switches are open. To achieve good RF performance, the topology of the switching circuit plays an important role and should be designed carefully. The design guidelines of the SPMT switching circuits are (i) to keep the impedance match of the active branch for low insertion loss and high return loss; (ii) to design each branch symmetrical for similar results at every output port; and (iii) to make design compact for low cost in a batch fabrication.

In this section, different types of SPMT switching circuits are designed using the Si-core CPW transmission line and the lateral switches. These include SP2T, SP3T and SP4T switching circuits, with special focus on the SP2T switching circuits.

4.2.1 SP2T switching circuit

Based on different circuit topologies, three different SP2T switching circuits are developed. They are the in-line SP2T switching circuit, the parallel SP2T switching circuit and the single-beam SP2T switching circuit. As the basis of the SPMT switching circuit, the in-line SP2T switching circuit is discussed in detail, including the design, equivalent circuit modeling and the full-wave EM simulation. Then, other two types of SP2T switching circuits are derived.

4.2.1.1 Design of the in-line SP2T switching circuit

The schematic of the in-line SP2T switching circuit is shown in Figure 4-20 (a). It consists of a T-junction with a series switch located at each of the output arms. The signal

Chapter 4: Integrated Switching Circuits

can therefore be routed to two different output ports with one switched off and the other switched on. Figure 4-20 (b) shows the layout of the in-line SP2T switching circuit. The lateral metal-contact switch placed at each output port involves a cantilever beam in the direction of the signal line. That is, the two cantilever beams in the switching circuit are in a line. The cantilever beam is equipped with a fixed connection at the output port. The free-end of the cantilever beam comes into contact with the contact bump at the T-junction upon turning on the switch. Therefore, the cantilever beam does not only act as a movable electrode of the actuator, but also forms part of the signal line. The ground

(a) Schematic diagram

(b) Layout design

Figure 4-20 The in-line SP2T switching circuit (a) schematic diagram and (b) layout design (G: ground; S: signal; A_i-A_i': bond wires)

Chapter 4: Integrated Switching Circuits

lines beside the cantilever beam are extended toward the cantilever beam to avoid a drastic increase in the characteristic impedance of this part. The gap distance between the cantilever beam and the ground lines is $30\text{ }\mu\text{m}$. At the free-end of the cantilever beam, one ground line protuberates toward the cantilever beam to serve as a fixed electrode. Therefore, no additional fixed electrode is required. DC bias voltage for actuation is applied between the signal line and ground lines of the output port. When the bias voltage is applied between the signal line and the ground lines at port 2 or port 3, one lateral switch can be closed and the other is kept open. Then the RF signal propagates from input port to one of the output ports. Due to the discontinuity of the CPW ground plane, the RF power can be converted from the desired CPW mode to the parasitic coupled slot line mode, as depicted in Section 4.1.2.3. To equalize the potential of the ground plane, bond wires are used at the discontinuity. In Figure 4-20 (b) the bond wires are denoted as A_i - A_i' . A total of three bond wires are used in this design.

4.2.1.2 Modeling and simulation of the SP2T switching circuit

Since only one switch in the SP2T switching circuit is activated to the close-state at any time, the equivalent circuit consists of an open stub with an open-state switch connected between the input transmission-line section and an output section with a close-state switch. The complete transmission-line model is shown in Figure 4-21 (a), where lateral switches are modeled using a simple capacitor $C_s = 12\text{ fF}$ at the open-state and a contact resistor $R_c = 1.2\text{ }\Omega$ at the close-state. The parasitic capacitance between the cantilever beam and ground lines, C_g , is also considered in the model. Figure 4-21 (b) shows the lumped equivalent circuit model of the SP2T switching circuit. The cantilever beam is described by the beam inductance, L_b , and the beam resistance, R_b . The

Chapter 4: Integrated Switching Circuits

Figure 4-21 Equivalent circuits of SP2T switching circuit (a) complete transmission-line model, and (b) Lumped equivalent circuit model.

Figure 4-22 Simulation results of the return loss of the SP2T switching circuit using circuit model.

Chapter 4: Integrated Switching Circuits

transmission line sections are replaced with their lumped *RLC* circuits. Since the transmission line section is quite short ($< 500 \mu\text{m}$), the shunt conductance is extremely small ($< 10^{-4} \text{ S}$) and is ignored in the model. The series-L and shunt-C configuration means that the insertion loss of the SP2T switching circuit exhibits a “low-pass” characteristic and the cutoff frequency depends on the length of the open stub. It is important to reduce the length of the stub by placing switches as close as possible to achieve wide bandwidth. With the layout in Figure 4-20 (b), the electrical length of the stub is only 3° at 10 GHz. This is relatively small and the SP2T switching circuit can maintain an impedance match up to around 40 GHz. As shown in Figure 4-22, the simulated return loss at the input port and the output port is higher than 13 dB at 40 GHz when one switch is closed and the other is open.

The equivalent-circuit model provides a useful insight into a SP2T switching circuit. However, it does not take into account the parasitic coupling that exists at the T-junction and the suppress role of the bond wires. Therefore, a full-wave EM analysis is introduced using Ansoft’s HFSS. Figure 4-23 shows the simulated S-parameters of the in-line SP2T switching circuit with and without bond wires using Ansoft’s HFSS. It is observed that the bond wires have significant effects on the RF responses at high frequencies range ($> 15 \text{ GHz}$). When the circuit is designed with three bond wires, the insertion loss is below 0.8 dB and the isolation is above 27 dB up to 30 GHz. However, when the circuit is designed without bond wires, the insertion loss is 1.3 dB and the isolation is 18 dB at 30 GHz. The surface current distribution with one switch open and the other switch closed is illustrated in Figure 4-24. It can be seen that the current mainly flows along the sidewalls of the transmission line and the cantilever beam. When the left

Chapter 4: Integrated Switching Circuits

Figure 4-23 Full-wave EM simulation results of S-parameters of the in-line SP2T switching circuit with and without bond wires.

Figure 4-24 Surface current distribution on the in-line SP2T switching circuit with one switch open and the other switch closed.

Chapter 4: Integrated Switching Circuits

switch is at its open-state, very little current is flowing along the left beam due to the capacitive coupling. When the left switch is at its close-state, most current is flowing along the left beam. The right beam has the similar behavior as the left beam. It is noted that the current distribution patterns in Figure 4-24 (a) and (b) are not exactly symmetrical since the mesh generated by the computer is asymmetrical.

4.2.1.3 Different types of SP2T switching circuits

Two other different designs of the SP2T switching circuits will be discussed here, which improve the RF performance and compactness of the SP2T switching circuits. In the in-line SP2T switching circuit, two lateral switches are in a line. However, two lateral switches can also be parallel to each other. The parallel SP2T switching circuit is implemented with this configuration, as shown in Figure 4-25. Two cantilever beams share one ground line between them. At the free-end of the cantilever beams, the common ground line protuberates toward two cantilever beams respectively to serve as the common fixed electrode of two lateral switches. When applying bias voltage between the signal line and ground lines at Port 2, the cantilever beam of Switch 1 moves towards the common ground line pulled by the electrostatic force until its free end hits the T-junction. Then, the RF signal propagates from Port 1 to Port 2. Little signal goes to Port 3 because Switch 2 is at its open-state. Similarly, when Switch 2 is closed, RF signal propagates from Port 1 to Port 3 and little goes to Port 2. When this SP2T switching circuit is in a circuit, the high DC potential is applied on the signal line through a RF choke inductor and the DC ground potential is applied on the common ground line to actuate the corresponding switch. A DC block capacitor is inserted between the switch signal line and other circuit parts. Because of the discontinuity of the CPW ground plane,

Chapter 4: Integrated Switching Circuits

the RF power can be converted from the desired CPW mode to the parasitic coupled slot line mode. To equalize the potential of ground planes, four bond wires are used at the discontinuities of ground planes.

Figure 4-25 The parallel SP2T switching circuit (a) Schematic diagram and (b) layout design (G: Ground; S: Signal; A_1 - A_4 : bond wire).

Chapter 4: Integrated Switching Circuits

(a)

(b)

Figure 4-26 The single-beam SP2T switching circuit (a) Schematic diagram and (b) layout design
(G: Ground; S: Signal; A_i-A_i': bond wire).

Chapter 4: Integrated Switching Circuits

The first two designs of the SP2T switching circuits require two cantilever beams. The last design – the single-beam SP2T switching circuit only requires one cantilever beam to move in both directions, as shown in Figure 4-26. Two fixed electrodes are located at either side of the cantilever beam. The ground potential of the bias voltage is applied on the cantilever beam and sufficient bias voltage is applied on one of the fixed electrode. Then, the cantilever beam moves towards this fixed electrode and hits the contact bump on the corresponding output port. As a result, the RF signal propagates to this output port and is blocked to the other port. To suppress the slot line mode at high frequency range, three bond wires are used to equalize the potential of ground plane which are denoted as A_i - A_i' in Figure 4-26 (b). The size of the single-beam SP2T switching circuit is reduced because only one beam is used.

4.2.2 Design of the SP3T switching circuit

Based on the design of the in-line SP2T switching circuit, a new type of SP3T switching circuit is developed and shown in Figure 4-27 (a) and (b). Each branch is perpendicular to the adjacent branch. The bias voltage is applied between the signal line and the ground line at the output port. At any time only one switch is activated to the close-state and other two switches keep at the open-state. Then, the RF signal propagates from input port to that output port and is isolated to other two output ports. Four bond wires are required to equalize the potential of the ground planes. The lumped equivalent model is obtained by adding a branch with an open switch to the lumped equivalent model of the SP2T switching circuit, as shown in Figure 4-27 (c). The SP3T switching circuit consists of two open-stubs connected between the input transmission line section and output branch section with a closed switch. Since the open-stubs are capacitive in

Chapter 4: Integrated Switching Circuits

Figure 4-27 The SP3T switching circuit (a) schematic diagram, (b) layout design (G: Ground; S: Signal; A_i - A_i' : bond wire), and (c) lumped equivalent circuit.

Chapter 4: Integrated Switching Circuits

nature, when there are more open-stubs, higher loss is expected at high frequencies range. Therefore, the insertion loss of the SP3T switching circuit is expected to be larger than the in-line SP2T switching circuit.

It is noted that the branches to the “near port” – Port 2 (Output 1) and Port 4 (Output 3) are perpendicular to the input port, whereas the branch to the “far port” – Port 3 (Output 2) is in the same line with the input port. This asymmetrical structure results in the different RF performances between the near port and far port, which will be verified by the measurement results in Section 4.2.4.

4.2.3 Design of the SP4T switching circuit

Based on the design of the in-line SP2T switching circuit, a SP4T switching circuit is designed and shown in Figure 4-28. This is a five-port switching circuit which has a “star” configuration. Each of branches of the SP4T switching circuit is located with an angle of 72° from the adjacent branch. Four lateral switches are located at the four output branches respectively. Since part of the ground line works as the fixed electrode, the bias voltage is applied between the signal line and the ground lines of one output port to close the corresponding lateral switch. When one switch is activated, the other three switches are kept at the open-state. Then, RF signal propagates from the input port to that output port, and is isolated to other three output ports. The lumped equivalent circuit of the SP4T switching circuit is shown in Figure 4-28 (c). The SP4T switching circuit consists of three open-stubs connected between the input section and the output section with a closed switch. The insertion loss of the SP4T switching circuit is expected to be larger than the SP3T and SP2T switching circuits because more open stubs connected to the active branch.

Chapter 4: Integrated Switching Circuits

(a)

(b)

Chapter 4: Integrated Switching Circuits

(c)

Figure 4-28 The SP4T switching circuit (a) schematic diagram, (b) layout design (G: Ground; S: Signal; A_i-A_i': bond wire), and (c) lumped equivalent circuit.

4.2.4 Experimental results and discussions

The SPMT switching circuits are fabricated on a glass wafer by a substrate transfer process. The detail of the fabrication process is discussed in chapter 5. The substrate is 500- μm -thick glass. The device structure layer is 62- μm -thick high resistivity silicon ($\rho > 4000 \Omega\cdot\text{cm}$), which is coated with 1- μm -thick gold. After the fabrication process, 1-mil-thick gold wires have been bonded at the discontinuities to equalize the potential of the ground plane using the wire-bonding technique. The actuator design in all switching circuits is: $l_1 = 230 \mu\text{m}$, $l_2 = 220 \mu\text{m}$, $l_3 = 18 \mu\text{m}$, $w_1 = 2.5 \mu\text{m}$, $w_2 = 5 \mu\text{m}$ (solid mass), $g_{\text{Si}} = 4 \mu\text{m}$ and $d_{\text{Si}} = 3 \mu\text{m}$. The insertion loss and the return loss of the SPMT switching circuits are determined by S_{21} and S_{11} respectively, through the input and

Chapter 4: Integrated Switching Circuits

output branch that contains the closed switch, while the switch in the other output branches are in the open-state. The isolation of the SPMT switching circuit is characterized by S_{21} along the signal line with the switch at the open-state.

4.2.4.1 In - line SP2T switching circuit

The SEM micrograph of an in-line SP2T switching circuit is shown in Figure 4-29 (a). It occupies 1.48 mm^2 ($= 1.85 \text{ mm} \times 0.8 \text{ mm}$) in area. The measured and fitted S-parameters of the corresponding SPST switch are shown in Figure 4-29 (b). The fitted RF results of the SPST switch agree with the measured results well. It shows the SPST switch has an insertion loss of 0.7 dB, a return loss of 23 dB and an isolation of 25 dB up to 25 GHz. The fitted lumped circuit parameters of the SPST switch are: $L_b = 114 \text{ pH}$, $C_{g,\text{close}} = 34 \text{ fF}$, $C_{g,\text{open}} = 30 \text{ fF}$, $C_s = 3.5 \text{ fF}$. The fitted total switch resistance, $R_b + R_c$, increases with frequency due to the skin effect and is fitted as

$$R_b + R_c = 1.5 + \sqrt{f} \quad (4-5)$$

The measured RF results of the in-line SP2T switching circuit with and without bond wires are shown in Figure 4-29 (c) and (d) respectively. The bond wires are essential in suppressing the parasitic slot line mode and in keeping the desired quasi-TEM mode, especially at high frequency. With three bond wires, the insertion loss of the in-line SP2T switching circuit is less than 1 dB up to 22 GHz. The return loss and the isolation are higher than 15 dB and 25 dB up to 22 GHz, respectively, as shown in Figure 4-29 (d). However, without bond wires, the RF performance of the circuit deteriorates with frequency quickly since the parasitic slot line mode dominates at high frequency. The insertion loss is 1 dB at 6 GHz and increases rapidly to 5.5 dB at 10 GHz, as shown

Chapter 4: Integrated Switching Circuits

(a) SEM micrograph

(b) SPST switch on glass

Chapter 4: Integrated Switching Circuits

(c) Measured results of the SP2T switching circuit without bond wires

(d) Measured and fitted results of the SP2T switching circuit with three bond wires

Figure 4-29 The in-line SP2T switching circuit (a) SEM micrograph, (b) measured and fitted results of a SPST switch on glass, (c) measured results without bond wires, and (d) measured and fitted results with three bond wire.

Chapter 4: Integrated Switching Circuits

in Figure 4-29 (c). The return loss is reduced from 17 dB at 6 GHz to 7 dB at 10 GHz, which are unfavourable compared to the in-line SP2T switching circuit with bond wires.

The circuit simulation results of the in-line SP2T switching circuit based on Figure 4-21(b) is shown in Figure 4-29 (d). The beam resistance, R_b , is found to be proportional to $\sqrt{f}$ due to the skin effect. The simulated return loss and insertion loss agree well with the experimental results. The simulated isolation agrees with the measured isolation up to 12 GHz. However, from 12 GHz to 25 GHz, the measured isolation is better than the simulated results because the circuit model does not describe the parasitic coupling effect at the T-junction.

4.2.4.2 Different designs of the SP2T switching circuits

The SEM micrograph of the parallel SP2T switching circuit without bond wires is shown in Figure 4-30 (a). The circuit size is 1.3 mm^2 ($1 \text{ mm} \times 1.3 \text{ mm}$) in area.

The SEM micrograph of the single-beam SP2T switching circuit is shown in Figure 4-30 (b). Since the fixed electrodes of this design are separated from the ground lines, the bias lines are designed to apply the bias voltage using an external power supply. By using a shadow mask, the bias line structures are sheltered from the metal coating except the DC pads. Therefore, the bias lines have high resistance due to the high resistivity of the device silicon layer. The bias line connected to the signal line is a meander structure to provide a high inductance. The circuit size is 0.92 mm^2 ($= 1.15 \text{ mm} \times 0.8 \text{ mm}$) in area, excluding the bias lines.

A comparison of the measured S-parameters among three SP2T switching circuits is provided in Figure 4-31. The parallel SP2T switching circuit has achieved an insertion

Chapter 4: Integrated Switching Circuits

(a)

(b)

Figure 4-30 SEM micrographs (a) the parallel SP2T switching circuit, and (b) the single-beam SP2T switching circuit.

Figure 4-31 Comparison of the measured S-parameters of the three SP2T switching circuits.

loss of less than 1 dB up to 22 GHz. Both the return loss and the isolation are above 22 dB up to 25 GHz. The parallel SP2T switching circuit is found to have the best insertion loss and return loss. This implies that the parallel SP2T switching circuit provides the best impedance matching and conducts the RF power most effectively.

The insertion loss of the single-beam SP2T switching circuit is 0.52 dB at 5 GHz and 1 dB at 17 GHz. The return loss and isolation are above 17 dB and 20 dB up to 25 GHz respectively. Compared with the other two designs, the insertion loss of the single-beam SP2T switching circuit is the least favorable. That is because the two fixed electrodes, which are located beside the cantilever beam, increase the parasitic shunt capacitance, C_g of the switch. As a result, more RF power is guided to the ground plane.

4.2.4.3 SP3T switching circuit

The SEM micrograph of the SP3T switching circuit is shown in Figure 4-32 (a). It occupies 2.45 mm^2 ($= 1.85 \text{ mm} \times 1.325 \text{ mm}$) in area. The measured S-parameters are shown in Figure 4-32 (b)-(c). The measured insertion loss and the return loss of the SP3T switching circuit are 0.7 dB and 17 dB at 15 GHz, respectively. The isolation is higher than 20 dB up to 20 GHz. Depending on which port is turned on, the SP3T switching circuit exhibits either a “near port” or the “far port” RF response. The insertion loss and return loss of the “far port” (Port 3) are better than the “near port” (Port 2 and Port 4). Since the “near port” is at an acute angle to the input port, there is some parasitic coupling that affects the input-output match. Hence, the “near port” exhibits a narrower return loss bandwidth than the “far port”. The two “near ports” (Port 2 and Port 4) experimental results are slightly different, especially when the frequency is higher than 15 GHz. That is because two beams in two “near ports” are not exactly same

(a)

Chapter 4: Integrated Switching Circuits

(b)

(c)

Figure 4-32 Experimental and fitted results of a SP3T switching circuit (a) SEM micrograph, (b) insertion loss and return loss, and (c) isolation.

Chapter 4: Integrated Switching Circuits

after fabrication. The circuit simulation results are compared with the measurement results in Figure 4-32 (a) – (b) too. The circuit simulation results are in good agreement with the measurement results of the “far port”, and differs with the “near port” results since circuit model cannot account for the coupling that exits at the acute angle. The measured insertion loss and return loss of the SP3T switching circuit are slightly worse than the SP2T switching circuits. This is because the active circuit consists of two open-stubs connecting the input port and the output port, which results in more capacitive coupling.

4.2.4.4 SP4T switching circuit

The SEM micrograph of the SP4T switching circuit, which occupies 3.47 mm^2 ($= 1.77 \text{ mm} \times 1.96 \text{ mm}$) in area, is shown in Figure 4-33 (a). The comparison between the measured results and the simulated results are shown in Figure 4-33 (b) and (c). The measured insertion loss is lower than 1 dB from 50 MHz to 10 GHz. The SP2T and SP3T switching circuit have achieved comparable results up to 22 GHz and 17 GHz respectively. Both the return loss and the isolation of the SP4T switching circuit are higher than 22 dB at 10 GHz. The measured S-parameters reveal the same thing in the SP4T switching circuit as the SP3T switching circuit, that is, the RF response depends on the closed switch either on the “near port” or “far port”. When the closed switch is at the “far port”, the insertion loss is better than the “near port”. In this SP4T switching circuit, the “near port” is Port 2 and Port 5, and the “far port” is Port 3 and Port 4. The insertion losses of the far ports are 0.2 dB lower than the one at the near ports at 10 GHz. The circuit simulation results fit the “far port” results very well and differ with the “near port” results a little due to the circuit model limitation.

Chapter 4: Integrated Switching Circuits

(a)

(b)

(c)

Figure 4-33 Experimental and fitted results of a SP4T switching circuit (a) SEM micrograph, (b) insertion loss and return loss, and (c) isolation.

4.3 Summary

In this chapter, the Si-core CPW and integrated micromachined switching circuits are studied, theoretically and experimentally.

The design and the full-wave EM simulation of the Si-core CPW are presented. The losses of the Si-core CPW transmission line related to the substrate material, the core material and the process variations are analyzed using the RLGC model. The analysis shows that the substrate material and the core material have influence on the dielectric loss. High-resistivity and low-loss material is more favorable for the substrate and the core material for the low-loss Si-core CPW transmission line. The process variations,

Chapter 4: Integrated Switching Circuits

including the thickness of the silicon backbone and the undercut dimensions are also significantly affect the RF performance of the Si-core CPW. It is shown that these process variations must be set as small as possible to improve the RF performance of the Si-core CPW transmission line. The experimental results also verify that the Si-core CPW supports quasi-TEM mode propagation up to 25 GHz with attenuation of less than 4 dB/cm. It is found that the conductor loss dominates the attenuation of the Si-core CPW. To achieve the low-loss Si-core CPW, some useful guidelines are (i) depositing sufficiently thick metal and improving the step coverage of the metal deposition; (ii) utilizing low loss substrate, such as glass; and (iii) using high resistivity silicon as core material.

By directly applying the Si-core CPW and lateral switches, SPMT switching circuits are designed, fabricated and measured. The in-line SP2T switching circuit, which has two cantilever beams in a line, is designed with the equivalent circuit analysis and the full-wave EM simulation. From the EM simulation and experimental verification, the bond wires are essential for the SPMT switching circuits to suppress the parasitic slot line mode. This is because there are many discontinuities in the ground planes of the SPMT switching circuits. The in-line SP2T switching circuit with three bond wires has insertion loss of less than 1 dB up to 20 GHz, compared to only 6 GHz for that insertion loss without bond wires. The parallel SP2T switching circuit with two cantilever beams in parallel demonstrates lowest insertion loss, which is less than 1 dB at 22 GHz. This is because the parallel SP2T switching circuit has better circuit matching. The single-beam SP2T switching circuit, however, has smallest circuit size (0.92 mm^2) because only one cantilever beam is used.

Chapter 4: Integrated Switching Circuits

The SP3T and SP4T switching circuits are also designed and fabricated. The SP3T switching circuit has an insertion loss of 0.7 dB and a return loss of 17 dB at 15 GHz. The isolation is higher than 20 dB up to 20 GHz. The SP4T switching circuit has an insertion loss of less than 1 dB up to 10 GHz. Both the return loss and the isolation are higher than 22 dB at 10 GHz.

Compared to other SPMT switching circuits, these lateral SPMT switching circuits have smaller device area and demonstrate comparable RF performances, as shown in Table 2-2. Besides, the lateral SPMT switching circuits have the advantages of reliable mechanical performance and simple fabrication process. Generally, the measured threshold voltage of the vertical switch is larger than the designed value due to the residual stress in the metal membrane structures. However, the measured threshold voltage of the lateral switch is very close to the designed value because of the excellent mechanical properties of the single-crystal silicon. The vertical SPMT switching circuits are fabricated using five to nine masks. The lateral SPMT switching circuits are fabricated using a single mask. Therefore, the integration of lateral switches and Si-core CPW transmission lines provides a low-loss low-cost SPMT switching circuit.

CHAPTER 5

FABRICATION TECHNOLOGY

The objective of this chapter is to develop a single-mask substrate transfer process for the fabrication of the glass-substrate high-aspect-ratio (HAR) suspended silicon structures. The fabrication process begins with the formation of the HAR silicon structures using deep reactive ion etch (DRIE) process. Then, the HAR structures are transferred to a glass wafer via a silicon-thin-film-glass anodic bonding and a silicon thinning technique. Finally, the HAR structures are released using self-aligned wet etching of the glass. This single-mask substrate transfer process provides low-loss, high-yield and highly flexible glass-substrate fabrication technique for RF applications.

The structure of this chapter is organized as follows. First, the full fabrication process flow is described in Section 5.1. Then, the key steps are discussed in Sections 5.2 - 5.5. The Si-thin-film-glass anodic bonding is explored in section 5.2 with special emphasis on the effect of the bonding material (the material type of the thin film, the silicon resistivity and the glass thickness) on the bonding strength. The issues related to the silicon thinning using the aqueous solution of potassium hydroxide (KOH) is discussed in Section 5.3, and the release method of the self-aligned wet etching of the glass is investigated in Section 5.4. Finally, a shadow mask fabrication process which is placed in context with its primary use as metal deposition mask at selected areas is introduced in Section 5.5. Section 5.6 provides a summary.

5.1 Fabrication Process Flow

The substrate transfer fabrication process uses a silicon wafer and a glass wafer to fabricate high-aspect-ratio suspended MEMS structures. The silicon wafer is 8" 730- μm -thick silicon wafer, which either has low resistivity ($\rho = 1\text{-}10\ \Omega\cdot\text{cm}$) or high resistivity ($\rho > 4000\ \Omega\cdot\text{cm}$). The glass wafer is 8" borosilicate Pyrex 7740 glass wafer with thickness of 500 μm or 1 mm. The process flow is shown in Figure 5-1 and explained as follows.

(i) Deposition and pattern of the silicon dioxide (SiO_2)

The fabrication begins with the deposition of a 2- μm -thick SiO_2 using plasma enhance chemical vapor deposition (PECVD), which serves as a hard mask for the subsequent DRIE process. Then, photoresist is spun and photolithography is done to define beams, contact bumps, transmission lines and electrical interconnects simultaneously. Finally, the pattern is transferred to the mask SiO_2 layer using reactive ion etching (RIE) and the photoresist is stripped using oxygen plasma etching.

(ii) Deep silicon etch

Deep silicon trenches are etched via Surface Technology System's (STS) high-density inductively coupled plasma (ICP) DRIE using SiO_2 as the hard mask. The DRIE process consists of a sequence of alternating etching and passivation cycles. The etching and passivation time are 8 sec and 5 sec in each cycle, respectively. The passivation phase deposits a thin layer of fluorocarbon polymer over all surfaces of trenches. Then the polymer is removed from the bottom of etched features with assistance of ion energy during each etch cycle. The rest of the etch cycle is a short isotropic etch of the exposed silicon. As the vertical etch rate is faster than the lateral etch rate, highly anisotropic profiles can be achieved. The wide trenches are etched faster than the narrow trenches

Chapter 5: Fabrication Technology

because of the aspect-ratio-dependent-etching (ARDE) effect of the DRIE process. As a result, the structure height ranges from 60 to 80 μm depending on the trench width.

(iii) Deposition of the sidewall protective thin film

After removing the SiO_2 mask via RIE, a protective thin film (thermal SiO_2 or silicon oxynitride (SiON)) is deposited on all exposed structures in the furnace to prevent erosion of silicon structures from the KOH solution during the silicon thinning process. Therefore, the protective thin film has to be resistible to the KOH solution and anodically bondable to the glass wafer. The bonding shear stress has to be strong enough to resist the subsequent grinding and polish process. The effect of this protective thin film on the anodic bonding is discussed in detail in Section 5.3.

(iv) Silicon-thin film-glass anodic bonding

The glass wafer stacks on the silicon wafer and the stacks are put in the bonding chuck of Electronic Vision EV bonder - EVG520 of EV group. The glass and the silicon with thin film coating are anodically bonded together. The bonding temperature of 400 $^{\circ}\text{C}$, voltage of 800 V, piston force of 1800 N, chamber pressure of 3 mbar, and bonding time of 1 hour and 30 mins are used. The material effect, including the thin film type coated on the silicon wafer, the thickness of the glass wafer and the resistivity of the silicon wafer, on the bonding strength are in Section 5.2.

(v) Grinding and polishing for silicon thinning

Grinding is employed to thin the backside of the silicon wafer rapidly using the GRIND-X GNX200 machine until about 10 μm silicon is left on the deepest trenches. The grinding rate is approximately 100 $\mu\text{m}/\text{min}$. The silicon is ground by 660 μm within 10 mins. The grinding surface is quite flat and no apparent tilting is observed. Then, the

Chapter 5: Fabrication Technology

polishing process is used to remove the grinding marks to smooth the silicon surface. The polishing step sacrifices about 5- μm -thick silicon. However, the grinding and the polishing process cannot be used to expose the silicon device structures directly since the brush and the slurry used in the grinding and polishing process may damage the tiny beams and block some of the small trenches.

(vi) KOH wet etching for silicon thinning

The whole stacks are submerged in 35% KOH solution at 40 °C to etch the silicon until all the silicon structures are exposed to the air. The wider and deeper trenches are opened earlier, followed by the narrower and shallower trenches. The protective thin film can protect the sidewalls of the exposed silicon structures from the erosion of the KOH. However, due to the crystallography dependent etching of silicon in aqueous solution of KOH, the V-shape groove may form on the top of the structure. This problem can be avoided by using appropriate layout placement which is discussed in section 5.3 in detail.

(vii) Removal of the protective thin film

The exposed protective thin film is removed using its respective wet etchant. For example, buffered oxide etchant (BOE) is used to remove the thermal SiO_2 and phosphorous acid is used to remove the silicon oxynitride.

(viii) Glass self-aligned etch

The stacks are dipped in the aqueous solution of hydrofluoric acid (HF) with the concentration of HF (49%): H_2O = 1: 5 for 30 mins to etch the glass and release movable structures. Silicon structures serve as the hard mask for glass etching. Therefore, glass etching is a self-aligned process. After rinsing in DI water and dipping in isopropyl alcohol (IPA), the stack is dried by baking at 90 °C.

Chapter 5: Fabrication Technology

(ix) Metal deposition

A shadow mask can be optionally bonded to the processed wafer stack temporarily using photoresist as an intermediate layer. Then a thin layer of metal is coated through the shadow mask using E-beam evaporation to cover the top surface and sidewalls of the silicon structures. Both wafer-to-wafer alignment and bonding are performed in an Electronic Vision EV Aligner and bonder - EVG520 of EV group. The shadow mask is bonded to the stack under pressure of 1000 N for 10 mins at room temperature. The fabrication process of shadow mask is presented in Section 5.5.

(x) De-bond of the shadow mask

The bonded wafers are heated at 150 °C to soften the photoresist so that the shadow mask can be manually separated from the wafer stack. The photoresist is wiped off using acetone. The shadow mask is reusable.

(xi) Dicing and wire-bonding

The wafer is manually diced into dies using a diamond cutter. The die has a size of 2 cm × 3 cm. Then, 1-mil-thick gold wires are bonded at the discontinuities of the ground planes of devices using a manual wire-bonding machine. These bond wires could be replaced by the metal interconnections during the wafer-level packaging, as discussed in Section 6.2. Now the device is ready for testing.

Chapter 5: Fabrication Technology

(i) Deposition and pattern of a 2- μm -thick SiO_2

(ii) Silicon DRIE etch using SiO_2 as hard mask to form HAR structures

(iii) Deposition of the protective thin film after removal of the SiO_2

(iv) Anodic bonding of the silicon wafer with a glass wafer

(v) Grinding and polishing to thin the silicon

(vi) KOH etching to open all trenches

Chapter 5: Fabrication Technology

(vii) Wet etching to remove the protective thin film

(viii) Glass self-aligned etching to release the suspended HAR silicon structures

(ix) Metal deposition through a shadow mask using E-beam evaporation

(x) De-bond of the shadow mask

Glass
 Silicon
 SiO₂
 Thin film
 Cr/Au

Figure 5-1 Schematic of the fabrication process flow.

Chapter 5: Fabrication Technology

The height of the silicon structures is controlled in a two-step process. First, time-controlled DRIE etching is used to etch high-aspect-ratio silicon structures until the narrowest trenches are 5 μm deeper than the desired depth. Due to the ARDE effect of the DRIE, wide trenches are deeper than the narrow trenches. Thus, during KOH etching, wide trenches are exposed to KOH solution earlier compared to narrow trenches. The structures bounded by wide trenches are etched down continuously. After the narrowest trenches are exposed, the whole wafer is overetched for another half-an-hour in KOH solution to open the structures completely since DRIE etching bottom is not perpendicular. The height of the silicon structures can be controlled within 5 μm .

This single-mask substrate transfer process can provide high-aspect-ratio suspended structures on the glass substrate because the DRIE process is done on the bare silicon wafer. The notching effect, which always exists in the conventional SOG-based process [106-108], is avoided. The double-side alignment is also avoided since the suspended structures are released using glass self-aligned etching. Only one mask is needed. At last, a shadow mask is developed for the metal deposition and metal pattern problem of the movable structures is bypassed. This new fabrication process is not only providing RF MEMS switches and circuits with high RF performance, but also can be used for the fabrication of the optical MEMS devices, microactuators, inertial sensors etc.

It is noted that the bonding quality of the silicon-thin film-glass anodic bonding pair is critical for this substrate transfer process as the bonding pair has to resist the subsequent grinding and polishing process and the KOH etching environment. For the silicon KOH etching process, the crystallography dependent etching may result in non-flat etching surface and the layout placement has to adjust to avoid it. These two

Chapter 5: Fabrication Technology

processes of the silicon-thin film-glass anodic bonding and KOH etching will be discussed in detail in Section 5.2 and 5.3, respectively. The self-aligned glass etch will be discussed in Section 5.4. The shadow mask related issues, such as the fabrication process and the spreading effect of the metal deposition will be discussed in Section 5.5.

5.2 Si-Thin Film-Glass Anodic Bonding

The silicon-thin film-glass anodic bonding process is the key process of the substrate transfer process. The basic setup of the anodic bonding process is shown in Figure 5-2. The glass surface is placed against the thin film on silicon surface. This sandwich structure is heated on a hot plate and a negative voltage is applied to the glass. The substrates are heated to 400 °C and a bias voltage of 800 V is applied between the glass and the silicon wafer. Then, an electrostatic force and the migration of ions create an irreversible chemical bond at the interface between the individual wafers.

Figure 5-2 Schematic of the anodic bonding setup.

5.2.1 Si-thin film-glass anodic bonding mechanism

The anodic bonding can be explained by the formation of the Si-O-Si bonds originating from silicon oxidation at the interface [127]. When the temperature increases, the Na^+ ions are more mobile for the Pyrex glass to behave like a conductor. Hence, in the very first moment, most of the voltage applied drops across a small gap of a few microns between the two surfaces. The high electric field in this area creates a strong electrostatic pressure, which acts on the two surfaces and effectively pulls them together. Thus, an intimate contact is formed. This contact is necessary to allow the two surfaces to react chemically and form the Si-O-Si bond. Simultaneously, the Na^+ ions start drifting the cathode, neutralizing the cathode while creating a depletion zone adjacent to the silicon anode. During the charging process of the depletion zone, the electric field is sufficiently high to allow a drift of oxygen anions to the anode. They react with the silicon anode and create a Si-O-Si bond. Subsequently, when the depletion zone becomes too large, the process stops. In terms of the anodic bonding mechanism associated with the reaction between hydroxide groups [128], the anodic bonding consists of the oxidation of silicon and the hydrogen bonding between hydroxy groups. The chemical reaction equations are expressed as

When a thin film of dielectric material with thickness of g_d , is coated on the silicon wafer, part of the applied voltage drops in the dielectric film and the other part drops in the air gap, g_0 . The voltage that drops in the air gap induces the electrostatic pressure, P , between the two surfaces, which is given by [129]

Chapter 5: Fabrication Technology

$$P = \frac{\varepsilon_0 V_{eff}^2}{2g_0^2 \left(1 + \frac{\varepsilon_0 g_d}{g_0 \varepsilon_d}\right)^2} \quad (5-3)$$

where ε_0 and ε_d are the permittivity of the air and the thin film respectively, g_0 and g_d are the gap distance of the air and the thickness of the thin film respectively, and V_{eff} is the effective applied voltage applied at the interface between the glass and the silicon. Therefore, the electrostatic pressure, P increases with the effective voltage, V_{eff} . As the thickness of the thin film increases or the permittivity of the thin film decreases, the electrostatic pressure, P , decreases. High electrostatic pressure results in an intimate contact of the bonding surface and helps strong bonding, and vice versa. When the thin film consists of two or more dielectric layers with permittivity of ε_i and thickness of g_i ($i = 1, 2, \dots, n$), the thickness, g_d , and the equivalent permittivity, ε_d , are given by

$$g_d = \sum_{i=1}^n g_i \quad (5-4)$$

$$\varepsilon_d = \frac{g_d}{\sum_{i=1}^n \frac{g_i}{\varepsilon_i}} \quad (5-5)$$

And the ratio of g_d/ε_d ratio is determined by

$$\frac{g_d}{\varepsilon_d} = \sum_{i=1}^n \frac{g_i}{\varepsilon_i} \quad (5-6)$$

Therefore, for multi-layer dielectric deposition, the ratio of g_d/ε_d increases and the electrostatic pressure, P , decreases. The chemical reaction for the bond formation is also affected due to the change of the bonding interface material.

5.2.2 Preparation of bonding samples

Three process parameters are considered in this study. They are the material type of the thin film coated on the silicon wafer, the thickness of the glass wafer and the resistivity of the silicon wafer. In order to determine the effect of the various parameters on the bonding quality, six types of anodic bonding sample are prepared, as listed in Table 5-1. Sample A is a bare silicon wafer bonded with a 500- μm -thick glass wafer. The anodic bonding of silicon and glass is very strong. However, when silicon structures are exposed to the KOH solution, the silicon is etched and structures are damaged. Therefore, it is necessary to deposit a protective thin film on silicon structures before anodic bonding, so that it can resist the attack of the KOH solution and protect sidewalls of exposed silicon structures. In samples B-D, the silicon wafer is coated with different thin films and the glass wafer is 500- μm -thick. In sample B, the silicon wafer is coated with 1000 Å wet thermal SiO_2 . In sample C, the silicon wafer is coated with 1000 Å wet thermal SiO_2 , followed by 1000 Å silicon nitride (SiN) deposited using low pressure chemical vapor deposition (LPCVD). In sample D, the silicon wafer is coated with the same thin film as in sample C, and then is put in the wet oxidization furnace at 1000 °C for 1 hour to oxidize the SiN surface to silicon oxynitride (SiON). In samples E and F, the silicon wafers are coated with the same thin film as in sample B. The glass wafer is 500- μm -thick in sample B and 1-mm-thick in sample E. The resistivity of the silicon wafer is less than 10 $\Omega\cdot\text{cm}$ in sample B and more than 4000 $\Omega\cdot\text{cm}$ in sample F. Same bonding conditions - the bonding temperature of 400 °C, voltage of 800 V, piston force of 1800 N, chamber pressure of 3 mbar, and bonding time of 1 hour and 30 minutes, are used for all samples.

Chapter 5: Fabrication Technology

Table 5-1 Tabular sample preparation and tested average shear strength of anodic bonding.

Sample Type	Resistivity of silicon (Ω .cm)	Thin film on the silicon surface	Thickness of glass (μ m)	Average shear strength (MPa)
A	1-10	-	500	16.6
B	1-10	SiO ₂	500	13.9
C	1-10	SiO ₂ + SiN	500	1.6
D	1-10	SiO ₂ + SiN + SiON	500	11.2
E	1-10	SiO ₂	1000	13.0
F	> 4000	SiO ₂	500	13.6

5.2.3 Experimental results and discussions

After the anodic bonding, it is observed that samples A, B, D, E and F are bonded uniformly. All structures are bonded with the glass. There are some small colorful rings with diameters less than 4 mm at the bonding surface, which may be caused by the incomplete clean of silicon and glass wafer. However, for sample C, the bonding is relatively poor. There are some bubbles with diameters more than 3 cm in sample C. Many small structures with feature size less than 1 mm are un-bonded.

To quantitatively evaluate the bonding quality, the tensile strength measurement is conducted commonly [130-131]. The shear strength measurement has not been reported before. However, the shear strength measurement is relatively more important

Chapter 5: Fabrication Technology

when the bonding wafers need to be ground and polished. Failure usually occurs when the external shear stress exceeds the limitation of the shear bonding strength. Figure 5-3 shows the schematic of the shear test setup using Dage Series 4000 Bond Tester. The glass is faced down and the silicon is faced up. The shear height (the position of the test contact point) is set at 200 μm higher than the glass thickness. For instance, the shear height is set at 700 μm when the glass is 500 μm thick and 1200 μm when the glass is 1 mm thick. The bonded wafer pair is diced into dies with 2 mm $\times$ 2 mm in size. Seven test dies are prepared for each bonded wafer pair.

The experimental results of the shear strength are shown in Figure 5-4 and the average shear strength is summarized in Table 5-1. It reveals that the 1000 Å thermal oxide on silicon (sample B) reduces the average shear strength of the bonding pair from 16.6 MPa (sample A) to 13.9 MPa. The deposition of 1000 Å SiN on thermal oxide (sample C) decreases of the average shear strength to 1.6 MPa. This can be partly explained by the change of the electrostatic pressure, P . Multi-layer dielectric material coated on the silicon surface increases the ratio of g_d/ϵ_d and decreases the electrostatic pressure, P .

Figure 5-3 Schematic of the shear test setup.

Figure 5-4 Plot of measured shear strength of different samples.

However, wet thermal oxidization of SiN to SiON (sample D) increases the average shear strength to 11.2 MPa. This is lower than silicon-glass (sample A) and silicon- SiO₂-glass (sample B) bonding, but is much higher than silicon-SiO₂-SiN-glass bonding (sample C). Figure 5-5 shows SEM micrographs of the cross sectional view of samples C and D to evaluate their bonding interface between silicon and glass. Figure 5-5 (a) shows a distinct gap at the interface of sample C. This implies insufficient bond in sample C (silicon + SiO₂ + SiN). However, by oxidizing the surface of SiN into SiON, as in sample D, there is no any gap at the interface, as shown in Figure 5-5 (b). This means strong bond formed in sample D. In sample D, the surface refractive index of silicon with thin film is about 1.954 measured using a Rudolph-ellipsometer. That is between the refractive index $n = 1.46$ for 1000 Å thermal SiO₂ and $n = 2.02$ for 1000 Å LPCVD SiN.

Chapter 5: Fabrication Technology

(a) sample C: SiO₂ + SiN

(b) sample D: SiO₂ + SiN + SiON

Figure 5-5 SEM micrograph of the bonding interface region of silicon - thin film - glass bonding pair (a) Sample C and (b) Sample D.

Chapter 5: Fabrication Technology

This implies that the SiN surface has changed. Some oxygen (O) atoms have reacted with the SiN and formed a thin layer of silicon oxynitride (SiON). The thickness of SiON layer is about 30 Å. In [132], it is found that the SiN film is highly dense and the surface terminates with Si-N bond. The Si-N bond is too strong to be broken at 400 °C. Therefore, the Si-O-Si bond cannot be formed in the sample C. However, in the 1000 °C furnace condition, the nitrogen in the SiN surface layer can be substituted by the oxygen, and then the thin silicon oxide / oxynitride layer is formed. This layer contains a high density of H- and OH- groups at the surface, which help the interfacial chemical reactions. Therefore, Si-O-Si bond can be formed in the sample D effectively and causes a strong bonding.

The average shear strength of sample E (1000-μm-thick glass) is 13 MPa, slightly lower than sample B (500-μm-thick glass), which implies the bonding strength is slightly weakened when the thickness of the glass increases. This is because thicker glass has higher electrical resistance, causing more voltage drop on the glass. Therefore, the effective voltage, V_{eff} , at the interface is reduced, resulting in a lower electrostatic pressure and weaker bonding.

The average shear strength of the sample F ($\rho > 4000 \text{ } \Omega\cdot\text{cm}$) is 13.6 MPa, which is very close to 13.9 MPa of sample B ($\rho < 10 \text{ } \Omega\cdot\text{cm}$). That means the resistivity of the silicon wafer has little influence on the bonding shear strength.

The experiment of the grinding process shows that the bonding quality of the sample C is so poor that the pair collapses during the grinding process. Other samples (sample A, B, D, E and F) go through the grinding process successfully.

5.3 KOH Anisotropic Etching

Anisotropic chemical etching using the aqueous solution of KOH has long been used for the fabrication of the MEMS structures due to its excellent repeatability and uniformity in fabrication, and its low production cost. The etching conditions affect the surface properties of the structures, such as the flatness and the roughness. The aqueous solution of KOH starts to react with the exposed silicon immediately when it reaches the patterned silicon structures. Therefore, silicon structures without any protective thin film may damage immediately. Some protective thin film for the silicon structures, such as thermal oxide and thermal oxide/ SiN/ SiON can provide the effective protection to the sidewalls of the silicon structures. The experiment shows that the etching rate of thermal oxide in KOH aqueous solution with 35 wt.% concentration at 40 °C is approximately 300 Å/hr whereas the etching rate of LPCVD SiN is negligible. Therefore, the thermal oxide/ SiN/ SiON protective thin film is more favorable.

5.3.1 Layout design consideration

KOH is an anisotropic etchant of the silicon that exhibits a different etch rate on different crystal orientation planes, commonly $\{110\} > \{100\} > \{111\}$ [133-134]. The protective thin film can only be used to protect the sidewalls of the structures. The top surface is etched continuously by the KOH solution. When the layout of the structures is designed arbitrarily, a V-shape groove may form on the top of the structures. Therefore, the layout design should consider the KOH crystallography dependent etching. In KOH etching, the $\{111\}$ plane is an extremely slow etching plane and is accepted to be the non-etching plane. As the $\{111\}$ planes provide etching stops, it is better not to expose

Chapter 5: Fabrication Technology

them to the KOH solution during the wet etching so that the etching process can be controlled by adjusting the etching time and the sidewall will remain vertical. Which orientation plane is introduced initially depends on the geometry and the orientation of the mask feature. In this study, the normal (100) silicon wafers with $\langle 110 \rangle$ prime orientation flat is used. When a rectangular wire is accurately aligned with the prime orientation flat, i. e. the $\langle 110 \rangle$ direction, only $\{111\}$ planes are introduced as sidewalls from the very beginning of the KOH etching, which is 54.7° to $\{100\}$ planes. In this case, the cross section of the etching pit is a V-shaped groove with $\langle 110 \rangle$ edges and $\{111\}$ sidewalls, as shown in Figure 5-6 (a). There is one way to etch the silicon uniformly and produce vertical $\{100\}$ walls on the structures. As shown in Figure 5-6 (b), the structures are aligned in such a way that the straight trenches are in 45° angle with the prime orientation flat ($\langle 110 \rangle$ direction) of the (100) silicon wafer. There are $\{100\}$ planes perpendicular to the wafer surface and that their intersections with the wafer surface are $\langle 100 \rangle$ direction. Consequently, $\{100\}$ facets are initially introduced as sidewalls. As both the bottom and the sidewall planes belong to the same $\{100\}$ group, the lateral etching rate equals to the vertical etching rate. Hence, all the exposed silicon can be etched vertically, as shown in Figure 5-7 (b). The layout is turned 45° on the mask to accurately align straight wires with the $\langle 100 \rangle$ direction.

Figure 5-7 shows SEM micrographs of the cross-sectional view of the micromachined structures with different layout placement. When the straight wires are parallel (0°) or perpendicular (90°) to the $\langle 110 \rangle$ flat, a V-shaped groove is formed on the top, as shown in Figure 5-7 (a). However, if they are 45° to the $\langle 110 \rangle$ cut plane, the silicon is etched downward and the top etching surface is flat, as shown in Figure 5-7 (b).

Chapter 5: Fabrication Technology

Figure 5-6 Schematic top view and cross-sectional view showing the influence of the edges' orientation on the silicon etching profile (a) 0° or 90° , and (b) 45° to $\langle 110 \rangle$ prime orientation flat.

Chapter 5: Fabrication Technology

(a)

(b)

Figure 5-7 SEM micrographs showing cross section of the micromachined structures with different layout placement (a) 0° and (b) 45° to <110> prime orientation flat.

5.3.2 Etching temperature effect

KOH etching is a temperature dependent process, where the etching rate of silicon increases with the temperature. The etching rate of the silicon (100) in 35 wt.% KOH solution is summarized in Table 5-2. The stabilized etching temperature is $\pm 2\text{ }^{\circ}\text{C}$. The etching rate is approximately $3\text{ }\mu\text{m/hr}$ at the room temperature and $62.4\text{ }\mu\text{m/hr}$ at $70\text{ }^{\circ}\text{C}$. However, surface roughness changes with the etching temperature too, as shown in Figure 5-8. It shows that when the etching temperature increases from $40\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$, the surface roughness of the etching surface increases rapidly from 1.317 nm to 38.003 nm . In consideration of the etching rate and the surface roughness of the silicon etching, the silicon thinning of bonded wafers is carried out at $40\text{ }^{\circ}\text{C}$ in 35 wt.% KOH aqueous solution.

Table 5-2 The etching rate and surface roughness of silicon vs. etching temperature in 35 wt.% aqueous solution of KOH

Etching temperature ($^{\circ}\text{C}$)	Etching rate ($\mu\text{m/hr}$)	Surface roughness (nm)
23	2.95	-
40	12	1.317
50	29	6.005
60	40	19.687
70	62.4	38.003

(a) 1.317 nm @ 40 °C

(b) 6.005 nm @ 50 °C

(c) 19.687 nm @ 60 °C

(d) 38.003 nm @ 70 °C

Figure 5-8 Experimental results of the surface roughness of silicon etched by 35 wt.% KOH at different temperatures (a) 40 °C, (b) 50 °C, (c) 60 °C, and (d) 70 °C.

5.4 Self-Aligned Etching of the Glass

The self-aligned glass etching technique can be used to release the high-aspect-ratio suspended silicon structures or etch deep trenches in glass, as shown in Figure 5-1. The high-aspect-ratio silicon structures are patterned using the DRIE technique, followed by a protective thin film coating. Then, the silicon wafer is anodically bonded to a glass wafer, which is thinned by the grinding and polishing process. Next the KOH etching is used to expose small silicon structures. The stacks are then submerged in an aqueous solution of hydrofluoric acid (HF) for the glass self-aligned etching. The concentration of HF (49%): H₂O = 1:5 is chosen to etch the glass wafer smoothly.

Figure 5-9 SEM micrograph of the cross sectional view of a glass cavity after 30 mins self-aligned etching.

Chapter 5: Fabrication Technology

Figure 5-10 SEM micrograph of the high-aspect-ratio comb-drive actuator.

Figure 5-9 shows a SEM micrograph of the cross sectional view of a glass cavity etched by the aqueous solution of HF for 30 mins. It shows that the vertical etching depth of the glass is $6.55\ \mu\text{m}$ and the lateral etching width is $9.41\ \mu\text{m}$. The corresponding vertical etching rate of the Pyrex glass at this concentration is about $13.1\ \mu\text{m/hr}$. The lateral undercutting is nearly 1.44 times of the vertical etching depth. Ideally, the isotropic chemical wet etching of glass should result in an undercutting equal to the vertical etching depth. The larger undercutting here could be due to the presence of a thin layer of native oxide (SiO_2) at the interface, which is formed during the anodic bonding. In HF solution, the native oxide is etched faster than the glass. The HF solution then moves laterally from the bonding interface to attack the native oxide thereby increase the undercutting. The cross sectional view shown in Figure 5-7 represents the global views of the silicon mask which has straight wall due to the DRIE etch. The silicon mask is hanging over the glass substrate because of the HF isotropic etching of glass. Therefore,

Chapter 5: Fabrication Technology

the suspended structures can be released. Using this self-aligned glass-etching process, excellent mask accuracy is obtained due to the high-resolution DRIE process. Alignment problem is also prevented due to the self-aligned etching. Therefore, the advantages of this glass etching method are high accuracy and self alignment.

Figure 5-10 shows the SEM micrograph of the high-aspect-ratio comb-drive actuator fabricated using the proposed process. Both of the width and the space of comb fingers are 3 μm . The depth is 80 μm . Therefore, the aspect ratio of 26 is achieved using this substrate transfer fabrication process.

5.5 Shadow Mask Techniques

High-resolution patterning in deep holes is a common problem in the MEMS fabrication process [135] as normal photoresist spinning cannot be used on such a substrate. Shadow mask is useful in cases where normal patterning (lithography) is difficult [136]. In this section, the design, the fabrication and the usage of the shadow mask are discussed.

5.5.1 Design and fabrication of the shadow mask

The shadow mask is formed using a normal p-type (100)-oriented silicon wafer. The fabrication process flow is shown in Figure 5-11 (a)-(e). First, a 2- μm -thick photoresist is spun on the front side of the wafer and patterned. Then, the DRIE process is used to etch structures to approximately 50 μm deep using photoresist as the mask material. After stripping the photoresist, a dielectric layer consisting of 300-Å-thick thermal oxide and 1500-Å-thick LPCVD silicon nitride is deposited on both sides of the

Chapter 5: Fabrication Technology

Figure 5-11 Fabrication process flow of the shadow mask.

Chapter 5: Fabrication Technology

wafer. Then, the backside of the wafer is patterned using a double-side alignment photolithography technique via Electronic Vision EV Aligner. The pattern is transferred to the dielectric layer via RIE and the photoresist is stripped. Next, the wafer is anisotropically etched from the backside using 35 wt.% aqueous solution of KOH at 75 °C until the front pattern is visible from the backside clearly. Finally, the remaining silicon oxide and silicon nitride at both sides are etched using RIE.

Figure 5-12 shows a schematic cross sectional view of a shadow mask. High resolution shadow mask can be fabricated using this fabrication process since DRIE technique is utilized to etch the front side of the wafer. Both holes and distance between holes can be less than 5 μm . The back open of the wafer is etched using the aqueous solution of KOH. Due to the crystallography dependent etching of silicon in the aqueous solution of KOH, the rectangular opens, which are 0° (or 90°) to $\langle 110 \rangle$ prime orientation flat, have inclined $\{111\}$ sidewalls. The difference between the back open size and the front pattern size is $2X$, where X is expressed as

$$X = \frac{W - W_0}{2} = \frac{D - H}{\tan 54.74^\circ} \quad (5-7)$$

where W is the size of the back open, W_0 is the size of the front pattern, D is the thickness of the shadow-mask wafer and H is the etching depth of the front pattern. Generally, the wafer thickness, D , is 750 μm to 800 μm . The etching depth of the front pattern, H , is 50 μm . Hence, X is equal to 495 μm to 530 μm . The distance between two holes generated by the KOH etching should be larger than $2X$, that is about 1100 μm . Small holes or holes separated by small distance should be combined in one back open and supported by a silicon membrane. The thickness of the membrane is dependent on the etching depth of the front holes. On the other hand, if the distances between all holes are larger than 1 mm,

Chapter 5: Fabrication Technology

Figure 5-12 Schematic of the cross sectional view of the shadow mask.

the front process can be omitted. Only the KOH etching is used to etch through the wafer. Thus, separate through-holes are formed in the shadow mask. However, the simplified process is obtained at the cost of the resolution. The final hole size, W_0 , changes with the wafer thickness and the distance between two holes has to be larger than $2X$.

In the aqueous solution of KOH, large back opens are etched faster and are etched through earlier than small back opens. Approximately 30 minutes over-etching time is needed to etch through all patterns since the leakage of KOH solution. Thanks to the protection of SiO_2 / SiN , the front patterns do not change during the KOH over-etching.

Therefore, to shorten the over-etching time, the back opens should have a uniform design. In consideration of the membrane tension, the membrane size after the KOH etching should not be too large. Otherwise, the membrane may collapse after the KOH etching. Generally, the membrane size is less than $7 \times 7 \text{ mm}^2$. Figure 5-13 shows the optical photos of both the front side and the backside of a shadow mask for the single-beam SP2T switching circuit. It can be seen that the backside of the shadow mask is not as smooth as the front side due to the silicon anisotropic etching in the aqueous solution of KOH at the high temperature. The back open is shared by four irregular holes separated by three fixed-fixed beam-mass silicon structures.

Chapter 5: Fabrication Technology

(a) The front

(b) The back

Figure 5-13 Optical photos of the shadow mask (a) the front and (b) the back.

5.5.2 Metal deposition through a shadow mask

The metal patterns with high resolution are realized using E-beam evaporation of metal through a shadow mask. The device wafer is temporarily bonded to the shadow mask first. A small amount of photoresist is put at the edge of the wafers as an intermediate material of bonding. Then, the shadow mask is placed on top of the device wafer and aligned using the Electron Vision EV aligner. Next, the temporary bonding is implemented by the bonder - EVG520 of EV group. The wafers are bonded under pressure of 1000 N for 10 minutes at room temperature. After that, the bonded pair is placed in the evaporator and the desired metal (such as Cr/Au, where Cr acts as the adhesive layer of Au) is deposited at selected areas through the shadow mask. After the metal deposition, the shadow mask is de-bonded by heating up the two wafers at 150 °C and manually separating them when the photoresist turns soft. Finally, the photoresist residual on the device wafer and the shadow mask is wiped off using acetone. After removing the metal via wet etching, the shadow mask can be recycled.

The coated metal pattern is always larger than the pattern in the shadow mask due to the spread effect, as shown in Figure 5-14. The enlargement (E) can be calculated as

$$E = \frac{b}{a} = 1 + \frac{d_2}{d_1} \quad (5-8)$$

where a is the pattern size on the shadow mask, b is the pattern size of the metal on the device wafer, d_1 is the distance between the source and the shadow pattern; d_2 is the distance between the device wafer and the shadow pattern. In the E-beam evaporator, the distance between the source and the wafer holder, d_0 is 0.5 m and the gap between the device wafer and the shadow mask is less than 0.5 mm.

Chapter 5: Fabrication Technology

Figure 5-14 Schematic of the metal deposition through a shadow mask.

Figure 5-15 Two methods of the usage of a shadow mask (a) the backside of the shadow mask faces the device wafer, and (b) the front side of the shadow mask faces the device wafer.

Chapter 5: Fabrication Technology

Two methods can be used to combine the shadow mask and the device wafer, as shown in Figure 5-15 (a)-(b). The first method is to let the backside of the shadow mask face the device wafer. The second method is to let the front side of the shadow mask face the device wafer. Comparing the two methods, the distance between the shadow mask pattern and the device wafer, d_2 , for the first method is smaller by approximately 700 μm than the second method. Therefore, the enlargement, E , of the first method is 1.0024, that is significantly larger compared to the second method whose enlargement is 1.001. Hence, the second method is preferred to reduce the metal spreading. In consideration of the spread effect of the metal deposition through the shadow mask, the minimum distance between two holes in the shadow mask is designed to 70 μm .

Figure 5-16 shows the optical photo of a single-beam SP2T switching circuit after the metal deposition through a shadow mask. The bias line is sheltered from the metal deposition and remains high resistance. Device parts and pads are coated with metal, which guarantees the RF signal propagation and the bias voltage applying. It is also noted that the surface color of the device coated with metal is different due to the non-uniformity of metal deposition. This is because of the spread effect at the pattern edge.

Because of the nature of the evaporation process, the metal coated at sidewalls is thinner than that coated on the top surface. Figure 5-17 shows the SEM micrograph of the cross sectional view illustrating the step coverage of the metal deposition. The thickness of the gold coated on the top surface is 1.2 μm , while the thickness of the gold on the sidewalls is 0.45 μm . It is observed that the metal is tightly coated on the sidewalls and is uniformly covering the height of the entire structures.

Figure 5-16 Optical photo of a single-beam SP2T switching circuit after Al coating through the shadow mask.

Figure 5-17 SEM micrograph of cross sectional view illustrating the step coverage of the metal deposition through a shadow mask using E-beam evaporation.

5.6 Summary

This chapter focuses on the fabrication process development of a single-mask substrate transfer process for the fabrication of a high-aspect-ratio suspended silicon structure on the glass substrate. The process consists of a silicon DRIE etching process, a Si-thin film-glass anodic bonding, a silicon wafer thinning, a self-aligned glass etching and a metal deposition through a shadow mask. Every key step has been investigated in detail respectively. Through studying the Si-thin film-glass anodic bonding mechanism, the thermal oxide and silicon oxynitride are chosen as the intermediate layer of the Si-thin film-glass anodic bonding because these materials are found to provide sufficient bonding strength with shear strength larger than 11 MPa for the grinding and polishing process. These materials also are strong resistant to KOH etching. The variation of the glass thickness and the silicon resistivity only reduce the bonding strength slightly. The aqueous solution of KOH with concentration of 35 wt.% at 40 °C has been selected to thin the silicon wafer, which provides smooth etching surface of the silicon wafer. Based on the analysis of the crystallography dependent etching of the silicon in the KOH etching, the device layout is adjusted to be 45° to the <110> prime wafer flat in a (100) silicon wafer for the flat etching surface on the top of the device. The glass is etched using the silicon structures as the hard mask to release the suspended structures. This etching process is mask-less and self-aligned. High-resolution shadow mask is developed by etching an open window from the front side using the silicon DRIE process, followed by KOH etching-through process from the backside. The design and integration methods with the device wafer of the shadow mask have also been discussed.

Chapter 5: Fabrication Technology

This substrate transfer process has various advantages. First, high-aspect-ratio, deep silicon structures can be achieved since DRIE is done on the blank silicon wafer. These structures can produce large force for electrostatic actuators. Second, the silicon resistivity, the structure height, the glass thickness and the glass etch depth can be chosen with flexibility according to different applications. Third, the process provides low loss for RF applications when glass and high-resistivity silicon are chosen as the substrate and the device layer respectively. Fourth, the manufacturing cost is low since only 1-3 masks are needed in this process compared to 5-9 masks process of the metallic MEMS switch.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

This thesis presents a new design of the lateral micromachined RF switches, the Si-core CPW transmission lines and the integrated switching circuits. A glass-substrate single-mask substrate transfer fabrication process is developed. The major contributions and conclusions of the thesis are summarized in this Section.

Different lateral switches with bandwidth of 50 MHz to 25 GHz are designed and fabricated. These are the single-beam switch and the double-beam switch. In the lateral switch, the fixed electrode of the actuator can either be a part of the ground line or a separate structure. The electromagnetic design and modelling as well as the mechanical design and modelling of the lateral switches are presented. Comprehensive optimization of the lateral switches is experimentally verified. The optimized switches demonstrate low insertion loss of less than 1 dB, and high return loss and isolation of more than 20 dB from DC to 25 GHz. Additionally, its threshold voltage is less than 25 V and its switching speed is 35 μ s with more than one million switching cycles.

Design, modelling and EM simulation of the Si-core CPW transmission line are presented. Based on the RLGC model of the transmission line, the sources of attenuation

Chapter 6: Conclusions

related to substrate materials, core materials and process variations are identified and analyzed. The losses of the Si-core CPW are mainly due to the conductor loss and the dielectric loss, which are found to be dependent on both the substrate and the core materials. Additionally, core materials with high resistivity are more favorable to reduce the loss of the Si-core CPW transmission line. The process variations including the thickness of the silicon backbone and the undercut dimensions are found to have effects on the performance of the Si-core CPW transmission line. Therefore, these factors have to be controlled carefully. The experimental results also verify that the Si-core CPW transmission line supports quasi-TEM mode propagation up to 25 GHz with attenuation of less than 4 dB/cm. Based on the experiment and the simulation results, two basic guidelines to achieve a Si-core CPW transmission line with low loss are developed. First, thick metal is deposited with good step coverage. Second low loss substrate and high resistivity core materials are used.

Based on the development of the Si-core CPW transmission line and the lateral switches, integrated SPMT switching circuits are designed, fabricated and measured. An in-line SP2T switching circuit with two cantilever beams in a line is studied thoroughly through the circuit analysis and the EM simulation. The EM simulation and experimental results of the in-line SP2T switching circuit shows that the bond wires are essential to suppress the parasitic slot line mode since many discontinuities are found in the ground lines of the SPMT switching circuits. The in-line SP2T switching circuit with three bond wires has an insertion loss of less than 1 dB up to 20 GHz. Additionally, the parallel SP2T switching circuit with two cantilever beams arranged in parallel shows lowest

Chapter 6: Conclusions

insertion loss of less than 1 dB at 22 GHz. The single-beam SP2T switching circuit with only one cantilever beam to move in two directions has smallest circuit size of 0.92 mm².

Based on the design of these SP2T switching circuits, SP3T and SP4T switching circuits are designed and fabricated. The SP3T switching circuit has the insertion loss of 0.7 dB at 15 GHz. The return loss is 17 dB at 15 GHz. The isolation is larger than 20 dB up to 20 GHz. The SP4T switching circuit, on the other hand, has the insertion loss of less than 1 dB up to 10 GHz. Both the return loss and the isolation are higher than 22 dB at 10 GHz.

The full fabrication process flow of the single-mask substrate transfer process is discussed. This fabrication process is to first pattern the silicon back-bone structure in desired shapes using a silicon DRIE process. Then, the silicon back-bone structure is transferred to the glass substrate using a Si-thin film-glass anodic bonding process followed by a silicon thinning process. Finally, a glass self-aligned etching process is used to release the suspended structures and a layer of metal is coated on the circuits through a shadow mask. The advantages of this single-mask glass-substrate process are high-aspect-ratio, low loss, high flexibility and low manufacturing cost.

Based on the analysis of the Si-thin film-glass anodic bonding mechanism, thermal oxide and SiON are chosen as the intermediate layer of the Si-thin film-glass anodic bonding because these materials are found to provide sufficient bonding strength with shear strength larger than 11 MPa for the grinding and polishing process. These materials also have strong resistant to KOH etching. In terms of the etching rate and surface roughness, the aqueous solution of KOH with concentration of 35 wt.% at 40 °C

Chapter 6: Conclusions

has been selected to thin the silicon wafer, which provides smooth etching surface. Based on the analysis of the crystallography dependent etching of the silicon in the KOH etching, the device layout is adjusted to be 45° to the $\langle 110 \rangle$ prime wafer flat in a (100) silicon wafer for flat etching surface on the top of the device. The glass is etched through the silicon pattern of the device layer directly to release the movable structures of the switches. This process is mask-less and self-aligned. The high-resolution shadow mask is developed by etching the open window from the front using the silicon DRIE process, followed by the KOH etching-through process from the backside.

6.2 Recommendations

Based on this PhD project, some recommendations for future research are identified and summarized in this section.

First, it is important to improve the metal deposition process. The resistance is the main source of the loss of the Si-core CPW transmission line and the switching circuits. The resistance of the Si-core CPW and the circuits can be reduced through thicker metal deposition and better step coverage. The current step coverage of the metal deposition technique is less satisfactory for the sidewalls metal coating.

Second, the packaging of the lateral switches and the integrated switching circuits is important. The packaging methods for RF MEMS vertical switches can also be used for lateral switches and circuits [5]. A wafer-level packaging process is designed and shown in Figure 6-1. Through-wafer vias, feedthroughs and cavities are fabricated in a glass cap wafer. After release, the device is vacuum encapsulated by bonding the glass cap wafer with silicon using anodic bonding or eutectic bonding technology. The lateral

(a) Top view looking through the glass side

(b) Cross sectional view along A-A'

(c) Cross sectional view along B-B'

Figure 6-1 A schematic showing the wafer level packaging of the parallel SP2T switching circuit (a) Top view looking through the glass side (b) cross sectional view along A-A' and (c) cross sectional view along B-B'.

switch and the switching circuit are in the vacuum cavities. The Si-core CPW pads are connected to feedthroughs. Metal interconnections are used to replace the bond wires locating at the discontinuities of the ground plane. Bonding pads on top of the cap glass wafer are used to assemble the lateral switch with other RF circuits via wire bonding or flip chip bonding. Finally, the packaged components are diced to dies.

Third, based on the current development of the Si-core CPW transmission line and the lateral switch, an integrated circuit which integrates them and other RF components onto a single chip, such as a reconfigurable antenna and a phase shifter, will create technical impacts and have potential commercial markets in the near future.

APPENDIX A

EQUIVALENT CIRCUIT MODEL OF THE TRANSMISSION LINE

The Si-core CPW requires complex modeling because the conductor material is not lossless and the lines can be coupled both capacitively and inductively. The finite conductivity of the conductor results in a variation of the current density distribution in the conductor. Skin effect loss (conductor loss) and dielectric loss at high frequency make the resistance and capacitance of the CPW frequency dependent. The equivalent circuit model per unit length of the CPW for frequency dependency analysis is shown in Figure A-1, where R is the series resistance per unit length, L is the inductance per unit length resulting from the propagating electromagnetic field, G is the substrate shunt conductance per unit length, and C is the substrate capacitance per unit length.

The performance of a transmission line is reflected in the characteristic impedance, Z_0 , and the propagation constant, γ , which is expressed as

$$\gamma = \alpha + j\beta \quad (\text{A-1})$$

where α is the attenuation and β is the phase of the transmission line. In the quasi-TEM model, the propagation constant, γ , and the characteristic impedance, Z_0 , of the transmission line are expressed as

Figure A-1 The equivalent circuit model per unit length of the CPW.

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (\text{A-2})$$

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (\text{A-3})$$

Then, the RLGC parameters of the CPW transmission line can be extracted by

$$R = \text{Re}(\gamma Z_0) \quad (\text{A-4a})$$

$$L = \text{Im}(\gamma Z_0) / \omega \quad (\text{A-4b})$$

$$G = \text{Re}(\gamma / Z_0) \quad (\text{A-4c})$$

$$C = \text{Im}(\gamma / Z_0) / \omega \quad (\text{A-4d})$$

Generally, the S-parameters can be obtained either from the measurement using the vector network analyzer (VNA) or the simulation using Ansoft's HFSS. From the S-parameters, the propagation constant, γ , and the characteristic impedance, Z_0 , can be deduced through ABCD matrix, which is expressed as [27]

Appendix

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ \frac{\sinh(\gamma l)}{Z_0} & \cosh(\gamma l) \end{bmatrix} \quad (\text{A-5})$$

where l is the length of the transmission line. Hence, the propagation constant, γ , and the characteristic impedance, Z_0 , related to the ABCD parameters are derived as

$$\gamma = \frac{1}{l} \cosh^{-1}(A) \quad (\text{A-6})$$

$$Z_0 = \sqrt{\frac{B}{C}} \quad (\text{A-7})$$

The ABCD parameters can be expressed using the S-parameters as [27]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} & Z_c \frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \\ \frac{1}{Z_c} \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} & \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \end{bmatrix} \quad (\text{A-8})$$

where Z_c is the source and load reference impedance ($Z_c = 50 \, \Omega$). Once the two port S-parameters are measured or simulated, ABCD parameters, γ , Z_0 and RLGC parameters are deduced using Eqs. (A-8), (A-6) and (A-7) and (A-4), respectively.

APPENDIX B

RADIATION LOSS

The radiation loss for a CPW has been expressed in a simple form to fit the experimental data for the attenuation constant of a picosecond pulse [137]

$$\alpha_r = \frac{\epsilon_r^{3/2} f^3 (S + 2W)^2 \pi^5}{16c^3} \frac{(1 - \epsilon_{eff}(f) / \epsilon_r)^2}{\sqrt{\epsilon_{eff}(f) / \epsilon_r} K(k) K(k')} \quad (\text{B-1})$$

where

$$k' = \sqrt{1 - k^2} \quad (\text{B-2a})$$

$$k = \frac{S}{S + 2W} \quad (\text{B-2b})$$

where K is the complete elliptic integrals of the first kind, $\epsilon_{eff}(f)$ is the dispersion of the effective permittivity with frequency and is given by [138]

$$\sqrt{\epsilon_{eff}(f)} = \sqrt{\epsilon_{eff}(0)} + \frac{\sqrt{\epsilon_r} - \sqrt{\epsilon_{eff}(0)}}{1 + A(f / f_{TE})^{-1.8}} \quad (\text{B-3a})$$

where

$$A = e^{u \ln(S/W) + v} \quad (\text{B-3b})$$

$$u = 0.54 - 0.64p + 0.015p^2 \quad (\text{B-3c})$$

$$v = 0.43 - 0.86p + 0.54p^2 \quad (\text{B-3d})$$

$$p = \ln(S / H) \quad (\text{B-3e})$$

$\epsilon_{eff}(0)$ is the quasi-static value of effective permittivity given by Eq. (4-1b). f_{TE} is the cutoff frequency of the TE_0 surface wave mode for the substrate, which is given by

Appendix

$$f_{TE} = \frac{c}{4H\sqrt{\varepsilon_r - 1}} \quad (\text{B-3f})$$

The power leakage can be avoided if a sufficiently thin substrate is used to push the cutoff frequency above the operating frequency. For instance, if the substrate is a 500- μm -thick glass with $\varepsilon_r = 4.6$, then $f_{TE} = 79$ GHz, which is suitable for the applications below 40 GHz. However, for a 500- μm -thick silicon substrate with $\varepsilon_r = 11.9$, then $f_{TE} = 45$ GHz. Therefore, for silicon substrate the surface mode radiation can not be ignored above 45 GHz. Eq (4-15a) is accurate up to 5% for the following range of parameters

$$0.1 < S/W < 5; \quad 0.1 < S/H < 5; \quad 1.5 < \varepsilon_r < 50; \quad 0 < f/f_{TE} < 10 \quad (\text{B-3g})$$

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