A programmable switched capacitor filter for audio applications

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A Programmable Switched Capacitor Filter for Audio Applications

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Master of Engineering

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Statement of Originality

I hereby certify that content of this dissertation is the result of work done by me and has not been submitted for a higher degree to any other University or Institution.

12 June 2006

Date

Sang Chin

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ABSTRACT

Switched capacitor technique [1] is a well-developed technique for integrated filter design. It plays a critical role in integrated filters and mixed-signal circuit design. Well known of its advantages such as good accuracy and less external components required over its continuous-time counterpart, it is becoming increasingly popular in commercial application. With the advance in CMOS process, the possibility to achieve high accuracy capacitors makes switched capacitor filter's performance more reliable.

The objective of this project is to design a fully programmable 2nd order bi-quadratic switched capacitor bass equalizer. The proposed design allows parameters such as mid-band gain and center frequency to be digitally controlled. The designed switched capacitor filter has a high sampling clock frequency to center frequency ratio. This unfortunately requires an impractically large capacitance spread if conventional switched capacitor technique is engaged. Not only will there be a chipsize problem but also matching issue.

In this project, the main contribution is in realization of the abovementioned switched capacitor bass equalizer with reducing capacitance spread. A novel reduce capacitance spread technique has been proposed in this thesis. The dummy phase in conventional switched capacitor circuit is used as transition phase for redistributing the charges on the integrating capacitor. A much smaller capacitance spread requirement can be achieved by using this dummy phase approach.

CHAPTER 1 INTRODUCTION

1.1 Background

Switched capacitor circuits play critical role in the integrated filter application even though there are several other design techniques available in filter circuits design; for instance, the conventional resistor-capacitor (RC) active filter, transconductance-C (G_m -C) technique [2, 3], MOSFET-C technique [4, 5], switched capacitor technique [6], etc. The RC active filter is not suitable for integrated filter design due to its need of large silicon areas for resistor and capacitor to achieve a relatively large time constant (RC). Besides this, accurate performance is difficult to achieve in active RC filter since the performance is highly dependent on the time constant where accuracy is largely determined by the matching of the resistor and capacitor. Perfect matching is difficult as tracking of process variation for the resistor and capacitor during the diffusion process is not possible. The G_m -C technique [7] and the MOSFET-C technique [8] are also facing accuracy problem. Although the accuracy problem can be solved with extra tuning circuit, larger silicon area is required.

The switched capacitor technique is a suitable design technique for integrated filter design and it is also one of the most well established techniques in integrated filter design. The basic concept of switched capacitor is to replace large resistor value by periodically charging and discharging a capacitor. The resistance realized by switched capacitor is approximated as T/C , where T is the period of the sampling clock and C is the capacitance value. By using switched capacitor to replace a large resistor, it is possible to replace the large resistor with small capacitor. Comparing to other integrated filter techniques, it requires no tuning circuit to achieve good accuracy. It is

known for its high accuracy in analog filter design where its performance is very much determined by the capacitor ratio and sampling frequency.

In today's technology, the capacitor matching can be made as low as 0.1% using the CMOS process and the sampling frequency is normally adapted from the system clock, which is always accurate. By employing switched capacitor technique, external capacitance can be omitted to allow reduction of the number of necessary external components as well as the pins for an IC. These advantages have allowed the switched capacitor circuits to receive widespread commercial application for low cost requirement. Other than the accuracy of switched capacitor technique over other analog filter technique, the programmability is another advantage of switched capacitor filter [9].

1.2 Project Motivation

The objective of this project is to design a fully programmable bi-quadratic equalizer for audio application using the switched capacitor technique. As audio band is defined within the range of 20 Hz to 20 kHz, the sampling clock required will be of a frequency that is much higher than the highest signal frequency, which is 20 kHz in the audio band. The sampling clock used in this filter designed ought to be in several hundreds kHz to MHz range depending on the need.

The selection of sampling frequency affects many factors in the filter performance. The sampling frequency will affect the noise performance [10], op amp Gain-Bandwidth (GBW) requirement [11], and the capacitor spread [12]. The fully programmable audio filter was selected to operate under sampling clock of 400 kHz.

This is 10 times to the Nyquist frequency, which is defined as two times to the maximum audio frequency. For operation using a lower sampling frequency, the accuracy of the frequency response might be affected at high frequency. For higher sampling frequency, the accuracy and noise performance will be improved at the trade off i.e. the requirement for higher op amp gain bandwidth (GBW) as well as increased capacitance spread. The increase in spread of capacitance is the main disadvantage of switched capacitor filter with higher sampling frequency. For a sampling frequency of 400 kHz, with the conventional switched capacitor filter approach, the capacitance spread is more than a thousand and is impractical to be realized. The main impractical contribution of this project is therefore to explore technique for capacitance spread reduction and to implement the technique in audio filter design.

The programmability of the bi-quadratic filter is an advantage especially for changing the characteristics of frequency response or to obtain different performances that maybe required in many audio applications such as for tone control in a TV or Hi-Fi.

As mentioned above, the sampling frequency for the proposed design is selected as 400 kHz. When the center frequency of less than 100 Hz is required, for example in a bass boost application in audio applications, the capacitance spread that is determined by the ratio of the maximum and minimum capacitance will be high, and can be as high as 1000. This is undesirable as it is extremely difficult to realize due to the requirement for capacitance matching and the consideration for area consumption by the capacitors. Technique to reduce the capacitance spread is therefore critically essential in this case.

1.3 Contributions

In this project, the main contribution is the technique to reduce the capacitance spread for a switched capacitor filter design. This technique is important in low frequency for audio application. A paper has been published in ISIC 2004 (International Symposium of Integrated Circuits 2004). The title of the paper is “A Capacitance Spread Reduction, Switched Capacitance Filter”. In the paper, the capacitance spread reduction technique for switched capacitor filter is discussed, and will be provided in Section 3.2.3 and 3.2.4 of this thesis. An example on a biquadratic equalizer that is implemented using the proposed technique is presented also in Chapter 3. Furthermore, a gain offset compensation technique is proposed at the end of the thesis, providing a solution for the error cause by the op amp offset voltage and finite gain effect.

1.4 Thesis Outline

This thesis contains six chapters. In Chapter 1, the background of switched capacitor technique is first introduced with the discussion of the advantages of this technique as compared to the conventional RC filter technique. The motivation of using switched capacitor technique in this project has been briefly discussed in Section 1.2. The outline of this thesis is then presented in this section. Finally, in Chapter 1, the contributions of this project will be stated in Section 1.3.

In Chapter 2, the audio processing system is introduced. The difference between switched capacitor audio system and conventional audio processing system is compared. The application of switched capacitor in audio processing system and the

consideration of design and system are described. Block diagram showing some main building block is shown in this chapter. In Section 2.3, the capacitance spread required by conventional switched capacitor is revealed. Discussions on two existing capacitance spread reduction techniques are then presented.

Chapter 3 provides the design and simulation results of the building blocks used in this project, such as the op amp, switches, clock generator, smoothing filter, switched capacitor filter, etc. The main contribution in this project is the capacitance spread reduction technique for switched capacitor filter. The discussion of this proposed technique is included in this chapter. The design considerations for these building blocks are also described in details.

The layout for each building block and considerations such as layout of analog and digital signal are given in Chapter 4. The proposed design has been fabricated into a microchip. The overall layouts as well as its micrograph of the microchip are shown in the last part of the chapter.

In Chapter 5, the measurement results for the microchip are taken and plotted against the simulation result. These measurement results include: THD, frequency response, etc. A discussion on the implication of the results is provided at the end of each section. As there are problems with the microchip, some recommendations to overcome the problem have been given for future implementation. Finally, the conclusion of the project is given in Chapter 6. A gain offset compensation technique is also proposed for the improvement of the microchip.

CHAPTER 2 AUDIO SYSTEM OVERVIEW

2.1 Overview

An audio system is a system that processes audio signal such as music and song that comes with different effects from an audio source such as a CD player, or a TV transmission. From the signal point of view, the audio system can be classified to digital or analog system. With different systems, the design approaches are different.

In a digital audio system, the audio signal appears in the form of digital and is processed by a DSP (Digital Signal Processor); an ADC (Analog-Digital Converter) and a DAC (Digital-Analog Converter) are required at the front and back of the DSP [13], respectively.

An analog audio system is a system where the audio signal processed is in continuous form. It is classified into a continuous-time and a discrete-time system. A continuous-time signal is a signal that has a well-defined value at every point in the time interval. A continuous-time system processes continuous-time signal. Conventional active RC filter and discrete filter are typical continuous-time filters that have been used in the past decades. A discrete-time signal is a signal which is continuous in amplitude and discrete in time. The time instances are normally equally spaced. A discrete-time signal is obtained by sampling a continuous-time signal with regular sampling clock. A system processing discrete-time signal is known as discrete-time system. The difference between discrete-time system and digital system is that the signal processed is continuous in amplitude in discrete-time system while the amplitude of

digital signal is digitized. The discrete time system is also known as sampled-data system due to the fact that the data is sampled in the system.

The signal processed in switched capacitor filter is in discrete-time form, it is normally sampled before or at the front stage of the switched capacitor filter. The signal is sampled periodically by an accurate clock signal, which is important for the accuracy of filter. In this project an analog audio filter is designed using switched capacitor technique. The difficulty of designing a switched capacitor filter in audio application will be discussed in next section.

The design of an audio system becomes challenging as the demand from the user become high, the requirement for high quality and low cost is the general trend of the demand from the market. To fulfill the requirement mentioned above, the switched capacitor filter is one of the approaches and will be introduced in the next section.

2.2 Switched Capacitor Audio System Design

In this project, a switched capacitor filter type bass equalizer is designed for audio system. Requirements such as low total harmonic distortion (THD) and low noise are crucial since the circuit is to be used in an audio system. One advantage of the switched capacitor filter is its property of high programmability that makes it a better choice over its RC active filter counterpart. The parameters of the filter such as center frequency and the center frequency gain can be controlled by the selection of the capacitor value in the design. The effective value of capacitors in switched capacitor circuit is varied by capacitor bank. By selecting appropriate switches setting, the control of capacitor bank is done [14].

The filter designed in this project is a switched capacitor filter that can be used in audio processing for low frequency boosting with feature of varying center frequency, it is also known as a bass equalizer in audio application. To design the bass equalizer in switched capacitor filter, the capacitance spread is one of the concerns especially when it becomes very high, when the ratio between the sampling and the center frequencies become high. Detail of such concern will be discussed in next section. The equalizer designed in this project is a 2nd order switched capacitor filter. It is designed to be programmable in center frequency and center frequency gain.

Besides the advantage of programmability, the other reason for the choice of a switched capacitor filter in audio system instead of the active RC filter is because of its cost effectiveness. In commercial ICs, external components such as large capacitors impose higher cost for the design and the extra external pins required also limits the packages size to be used. For RC active filters that are used in audio processing, due to its use in an audio band of about 20 to 20 kHz, the time constant will be large. The time constant is determined by product of RC. The resistor used in an IC is normally chosen to be within 10 kohms for the consideration of accuracy and silicon area. Hence the required capacitor is as high in nano Farad or in micro Farad. It is impractical to be integrated into ICs and so the use of external capacitor is inevitable, which then cause the increase in cost as mentioned before.

For a filter, the cutoff frequency is determined by time constant RC. In switched capacitor filter, the capacitance is scaled down to the pico Farad range, so that it can be integrated while the resistance needed to be scaled up to a very large value. In the

concept of switched capacitor, a resistor is to be replaced by a switched capacitor that is of much smaller value.

The equivalent realized resistor [15] is:

$$R_{eq} \approx T / C, \quad \text{Eq[2-1]}$$

where T is the sampling clock period.

The basic structure for switched capacitor with periodically charged and discharged realizing a resistor is shown in Figure 2-1. With the sampling rate at a reasonable frequency (e.g. hundreds of kHz) and the capacitor in pico Farad range, it is possible to realize a large resistor and hence possible to make the filter integrated. In this case, all the capacitor required can be integrated into the ICs and this reduces the pin count as well as the cost of the ICs. The effect of the use of switched capacitor technique in commercialize ICs is significant.

Figure 2-1 A switched capacitor to realize a resistor

The implementation of switched capacitor filters in audio filter faces the large capacitance-spread problem, which is defined as the ratio between the maximum capacitance to minimum capacitance. This is approximated as in Eq[2-2] for conventional switched capacitor filter where f_s and f_0 are sampling frequency and center frequency respectively.

$$\text{Capacitance spread} = f_s / 2\pi f_0 \quad \text{Eq[2-2]}$$

As shown in Eq[2-2], the capacitance spread is directly proportional to the ratio of the sampling clock frequency to the center frequency. As mentioned before, a switched capacitor filter is a sampled data filter. The sampling frequency needed to be at least two times that of the maximum signal frequency so as to avoid aliasing of unwanted high frequency signal or noise. In actual case, the sampling frequency is required to be much higher, for instance ten times of the maximum signal frequency, for better approximation of filter response.

In audio application, the bandwidth is from 20 Hz to 20 kHz. Hence the requirement of sampling frequency is in hundreds kHz range. For the case of low frequency equalizer, the ratio of sampling clock frequency to the center frequency is even higher, making the capacitance spread high. It becomes difficult to be realized in real system as it is difficult to match two capacitors with so much difference and the chip size also becomes high. Hence, to implement a switched capacitor filter in audio system special technique is required to be implemented to reduce the capacitance spread. This technique will be discussed in detail in Chapter 3. The other advantage of this technique is to reduce the total area required by the switched capacitor filter.

SC filter circuits are analogue sampled-data systems, where the independent variable, time, is ideally discrete, while the dependent variable representing the signal is a voltage with continuous value. Hence, noise interference, for instance aliasing noise and thermal noise, and the corresponding limited dynamic range is one of the fundamental limitations for the application of the SC circuit technique. Therefore, an understanding of noise generation and transformation in SC filter circuits is crucial in

order to predict the noise performance of a proposed design as well as to optimize the designs of the existing SC filter circuits.

Noise interference from numerous sources always impairs the output signal of an SC circuit. Generally, these disturbances originate from three main sources [16]:

1. Clock signals inject charge into the signal path via parasitic capacitance associated with real switches. This type of interference is called clock feedthrough.
2. There are interference coupled directly or capacitively from power supply and ground lines to the circuit signals. This is especially so for SC circuits residing together with digital circuitry on a single chip. Special precautions are needed to reduce these effects.
3. Random noise that is physically generated inside the elements of SC circuits deteriorates the system performance. Switches and amplifiers realized by solid-state devices all exhibit random fluctuations in the voltages and currents at their terminals. These fluctuations make up the random noise in SC circuits.

There are other factors that will affect switched capacitor filter performance. Op amp imperfections, for instance finite op amp gain, dc offset and low-frequency noise will reduce the dynamic range of circuits [17]. Generally, three techniques are used in switched capacitor circuits to reduce the low frequency noise, DC offset, and finite low frequency gain. They are autozero (AZ), correlated double sampling (CDS), and chopper stabilization (CHS) techniques.

- **Autozero** [18]--- The idea of AZ is sampling the unwanted quantity and then subtracting it from the instantaneous value of the contaminated signal at either the input or output of the op amp. It requires at least two phases: (i) a sampling phase when the unwanted noise or offset is sampled and stored, and (ii) a signal processing phase when the previously stored noise or offset is subtracted from noise or offset at this phase. The process flow of autozeroing is shown in Figure 2-2. AZ technique can cancel the DC offset and reduce the low frequency noise. The low frequency noise is time varying and random. Hence, the AZ technique can only high pass filtered the noise but not canceling them completely.

Figure 2-2 Autozero Process Flow

- **Correlated double sampling** [19] --- It is a particular case of AZ with the noise sampled twice in each clock period. There are two sampling operation: (i) a sampling of V_{in} amplifier noise and offset. (ii) A second sampling on the signal and instantaneous noises of the amplifier.
- **Chopper stabilization** [20] --- Unlike the two methods mentioned above, the chopper stabilization technique is a modulation technique. The idea is to modulate

the signal to a high frequency where there is no low frequency noise, and then demodulate it back to the baseband after amplification.

As it will be shown in Chapter 5 that there are several problems exist in the proposed filter design without offset compensation technique. An offset compensation integrator with the capacitance spread reduction technique proposed was recommended at the end of this thesis as the future suggestion. This technique is based on the correlated double sampling technique as mentioned before.

The block diagram of Figure 2-3 is a general block diagram of a programmable switched capacitor filter, which can be used in audio system. The input in the figure is a continuous time audio signal that contains high frequency noise. As switched capacitor filter is a sampled data filter, the aliasing effect will cause the high frequency noise or signal with frequency higher than the sampling frequency to be folded to the audio band. The performance of the filter is degraded due to this and an anti-aliasing circuit is needed at the front end of the system. This anti-aliasing filter is realized with a continuous-time low pass filter. It is used to attenuate the undesired high frequency noise and signal to a reasonable level and hence to minimize the inevitable folding effect as mentioned above.

The output signal from the anti-aliasing filter is entered into the switched capacitor filter. The switched capacitor filter is the main functional block of this project; it processes the audio signal and provides the audio equalizer effect such as bass effect in this project. Some capacitors are made controllable. A sample and hold (S/H) circuit is placed at the end of the switched capacitor filter as the output block of the

switched capacitor filter. Only one of the phases at the output contains the desired signal, the function of the S/H circuit is to sample the output signal of the switched capacitor filter.

In a continuous-time system, it is necessary to convert the output discrete time signal from switched capacitor filter back to a continuous-time signal. In order to reconstruct the discrete-time signal from the sample and hold circuit, a low pass filter acting as a reconstruction filter is to be placed immediately after the S/H circuit. This filter has omitted the higher harmonic of the output signal and also known as smoothing filter.

Figure 2-3 General block diagram for switched capacitor filter

The sampling clock generator is the clock generator to provide all required clocks for the switched capacitor filter circuit. In this project, a multi-phase switched capacitor filter is designed and hence a clock generator is required to provide the multi-phase clocks as well as the inverting clock for the switches.

A parameter controller circuit is a logic circuit that generates the control signal to the capacitor bank in switched capacitor filter. It controls the equivalent capacitor values and hence changes the parameter of the filter such as the center frequency and the center frequency gain.

2.3 Literature Review of Existing Capacitance Spread Reduction

Switched Capacitor Filter

In this section, the capacitance spread required by a conventional switched capacitor integrator is derived and expressed in term of the cutoff frequency and sampling frequency to show the effect of these factors. This is followed by a review of two existing capacitance spread reduction technique for switched capacitor circuits.

Figure 2-4 RC integrator and conventional switched capacitor integrator

An active integrator is an important basic building block in an active filter design, either in RC-filter or switched capacitor filter. Shown in Figure 2-4 is the structure of a general RC integrator and a conventional switched capacitor filter. The cutoff frequency f_0 is $1/2\pi R_1 C_2$, which is dependent on the time constant $R_1 C_2$. For the case of the switched capacitor integrator, the resistor R_1 is replaced with a switched

capacitor C_1 of value T/R_1 or $1/f_s R_1$, where T and f_s represent the period and frequency of the sampling clock respectively. The cutoff frequency is hence:

$$f_0 = f_s C_1 / 2\pi C_2 \quad \text{Eq[2-3]}$$

and the capacitance spread will become:

$$C_2 / C_1 = f_s / 2\pi f_0 \quad \text{Eq[2-4]}$$

Eq[2-3] relates to the dependence of the integrator cutoff frequency to that of the sampling clock frequency as well as the capacitor ratio. From Eq[2-4], it can be seen that the capacitance spread is directly proportional to the ratio of the sampling clock frequency to the desired cutoff frequency. In this project, the center frequency is chosen to be 50 Hz and the sampling frequency is 400 kHz. The capacitance spread required in this project can be deduced from Eq[2-4] as 1273. It will be impractical to realize the switched capacitor filter on chip if no capacitance spread reduction technique is adopted. This is because of the capacitor matching issue and the final large chip size.

The transfer function for the conventional switched capacitor non-inverting integrator in z-domain can be found using the following equations:

$$H(z) = \frac{C_1}{C_2} * \frac{1}{1 - z^{-1}} \quad \text{Eq[2-5]}$$

or

$$H(z) = \frac{2\pi f_0}{f_s} * \frac{1}{1 - z^{-1}} \quad \text{Eq[2-6]}$$

upon substituting Eq[2-4] into Eq[2-5].

Eq[2-5] presents the transfer function of the switched capacitor integrator in z-domain, illustrating the spread of the capacitance. Eq[2-6], however, correlates the z-domain

transfer function with ratio of the sampling clock frequency and the cutoff frequency, by simply substituting Eq[2-4] into Eq[2-5].

There are two existing capacitance spread reduction techniques. In [21], Huang Qiuting proposed a capacitance spread reduction technique that made use of the dummy phase. The implementation of this technique on a non-inverting integrator is shown in Figure 2-5. The input signal is firstly sampled at C_I during clock phase 2. The input signal has no immediate effect on the output signal. During clock phase 1, capacitors C_I , C_{A1} and C_{A2} form an attenuator. The charges at C_{A2} are discharged to C_A through the inverting input of the op amp during the next clock phase 2, to be sampled at the output. The effect of an input signal is delayed by one clock period, as indicated in Eq[2-7] in the numerator term of z^{-1} . The z-domain transfer function of the non-inverting integrator is given in Eq[2-7].

$$H(z) = \frac{C_I \cdot C_{A2}}{C_{A1} \cdot C_A} \cdot \frac{z^{-1}}{1 - z^{-1}} \quad \text{Eq[2-7]}$$

Figure 2-5 Capacitance spread reduced non-inverting integrator by Huang

Note that, Eq[2-7] fields a z-domain transfer function that is similar to that of Eq[2-5] except for the capacitor ratio, as well as a delay of one cycle occur at the output with reference to the input. Cautious has to be taken when considering the timing of the signal during design. Comparing that capacitor ratio of Eq[2-7] and Eq[2-6], it can be seen that,

$$\frac{C_{A1}}{C_1} \cdot \frac{C_A}{C_{A2}} = \frac{f_s}{2\pi f_0} \quad \text{Eq[2-8]}$$

As discussed in this section before, the right hand term in Eq[2-8] gives 1273 for the design parameter of the switched capacitor filter design chosen for this project. Instead of using a simply capacitor pair, C_2/C_1 , to realize the large value of the conventional switched capacitor circuits, it is now achieved through multiplication of two capacitor pairs, C_{A1}/C_1 and C_A/C_{A2} . The capacitance spread is hence reduced to

$$\sqrt{\frac{f_s}{2\pi f_0}} \text{ or } 35.7.$$

In [22], Nagaraj proposed another capacitance spread reduction technique using the charge differencing technique. The non-inverting integrator implementation of this technique is illustrated in Figure 2-6. The z-domain transfer function is given as in Eq[2-9], where

$$H(z) = \frac{1}{1 + C_1/C_2} \cdot \frac{C_1 \cdot C_3}{C_2 \cdot C_2} \cdot \frac{z^{-1/2}}{1 - z^{-1}} \quad \text{Eq[2-9]}$$

Similarly, by comparing Eq[2-9] with Eq[2-6], Eq[2-10] can be obtained,

$$\frac{1}{1 + \frac{C_1}{C_2}} \cdot \frac{C_1 \cdot C_3}{C_2 \cdot C_2} = \frac{f_s}{2\pi f_0} \quad \text{Eq[2-10]}$$

The capacitance spread can be determined by C_2/C_1 and C_2/C_1 . By making C_1 and C_3

Figure 2-6 Capacitance spread reduced non-inverting integrator by Nagaraj

same, and assuming the first term, $\frac{1}{1 + C_1/C_2}$, of Eq[2-10] to be approximated as 1,

the capacitance spread required in this project using this second technique can be

approximated as $\sqrt{\frac{f_s}{2\pi f_0}}$, or 35.7; which is the same as the previous technique. The

advantage of this technique over the previous is that it requires only one large capacitance C_2 instead of two, C_{A1} and C_A .

2.4 System Specifications for the Switched Capacitor Filter Audio System

The switched capacitor filter designed in this project is a 2nd order audio filter and it is known as bass equalizer in audio band. This equalizer boosts the audio signal at 50

Hz. In this project, the particular cutoff frequency is at lower range of audio band. A sampling clock of 400 kHz is used as the sampling frequency for better for the response accuracy. The capacitance spread required, if conventional switched capacitor technique is used, is 1273 as given in last section.

As mentioned in the last section, switched capacitor filter is well known for its programmability allowing easy change of equivalent capacitance values via the logic control. The proposed filter’s midband frequency is designed to be variable so that the user can change the parameters of the filter. The midband gain for the filter is designed to be tunable at 6 and 12 dB. The specifications of the design are listed in Table 2.1.

Table 2.1 Design specifications for switched capacitor filter in the project

S/N	Parameter	Value	Units
1	Midband Frequency	50 and 150	Hz
2	Midband Gain	6 and 12	dB
3	Sampling Frequency	400	kHz
4	Signal to Noise Ratio (SNR) (At 1V _{rms} output)	80	dB
5	Total Harmonic Distortion (THD) (At 1V _{rms} output)	-60	dB

CHAPTER 3 CIRCUIT DESIGN AND SIMULATION

RESULTS

3.1 Introduction

The advances of MOS process allow high precision devices such as capacitor and resistor as well as internal compensated op amp design. This has enhanced the use of switched capacitor filter in integrated filter design [23]. In this project, a 5 V 0.8 μm BiCMOS process from PANASONIC is used. The threshold voltage for the PMOS and NMOS is $0.6 \pm 0.2\text{V}$ and $0.7 \pm 0.2\text{V}$ respectively. The process uses the twin well technology, and so the NMOS and PMOS are using different island, allowing minimum body effect to the threshold voltage.

Two types of resistor are employed in this process; SP (shallow P) resistor with highly doped P+ for higher sheet resistance and more sensitive to process variation, PS (poly silicon) resistor for lower resistance value and more accurate value. SP resistor has a negative temperature coefficient while the PS resistor has a positive temperature coefficient that mainly affects the temperature effect.

The main target for this project is to design a switched capacitor filter with lower capacitance ratio and chip area. The values and accuracies of the capacitor in this process are relatively important. This will affect the final chip area and the accuracy of the performance. In this process, the metal-poly (AL-PS) type capacitor is engaged [24]. The sheet capacitance of this AL-PS capacitor is 2000 pF/mm^2 .

The recommended range for accurate capacitance is 1 pF to 20 pF. For this range of capacitance, the required capacitance size is of dimension from 22 μm x 22 μm to 100 μm x 100 μm . Any capacitor with size lower than 1 pF may result in accuracy or matching problem due to the parasitic effect. Capacitor with capacitance higher than 20 pF will result in large chip area and hence is not cost effective. The cross-sectional view of the AL-PS capacitor and the equivalent circuit with parasitic effect is given in Figure 3-1. It shows the parasitic capacitors exist in the capacitor due to the overlapping of the bottom plate and the substrate parasitic capacitor C_{p2} as well as the top plate and the substrate parasitic capacitor C_{p1} . The capacitance of C_{p2} is about 5 % of the main capacitor C while C_{p1} is not given in process manual, it is, however, expected to be lower than C_{p2} . The effect of the parasitic capacitor C_{p2} to the performance of switched capacitor filter can be minimized by the use of stray-insensitive structure. As there is noise at substrate, the noise will be coupled to the circuits through the bottom capacitor C_{p2} , and contribute to the output noise at the output of the circuits.

Figure 3-1 (a) Layout of Metal-PS capacitor (b) Equivalent circuit of Metal-PS capacitor with parasitic capacitors

In this project the simulations were done in two ways for the switched capacitor filter. As switched capacitor filter is a discrete-time filter, the ac response is impossible to be done in conventional simulator. Simulator such as SWITCAP developed by Columbia University with ideal modeling of components is specially developed for discrete-time circuit such as switched capacitor filter in this case. The simulation in transistor level is still required as it provides more realistic result by including the non-ideal effect, which is not included in SWITCAP. The simulations in transistor level were done with conventional simulators such as Eldo of Mentor Graphics in transient mode. The introductions for the EDA tools including the simulators and layout tools were given in Appendix A. The simulation files for SWITCAP simulation were given in Appendix B.

While doing the simulation in transistor level with transient mode, the simulation might face problems such as lengthy simulation time due to the small time step (as small as 1/100 times of period of sampling clock for accuracy) at long simulation time (due to low frequency signal is interested in this project). It is possible that no result can be obtained due to the hardware limitations such as memory and database size. Some algorithms to shorten the simulation time are required. A userware developed in Accusim is given in Appendix C for this purpose.

In this project, the challenge is to implement an audio band switched capacitor equalizer with capacitor value constraint by the process, which is in the range of 1 pF to 20 pF. This means that the capacitance spread has to be limited to below 20 for a minimum capacitance of 1 pF.

The sampling clock frequency used in this project for switched capacitor filter is chosen to be 400 kHz. This is equivalent to 20 times to the maximum signal frequency of the audio band. This clock frequency is chosen to allow more accurate results but yet able to limit the capacitance spread to a reasonable value.

In this chapter, the building blocks of the switched capacitor filter used in this project are discussed in Section 3.2. The discussion of the building blocks includes the analysis and the simulation results. The building blocks discussed include some main components such as switch, op amp and etc. The switches and the op amp design are presented in Section 3.2.1 and 3.2.2. In Section 3.2.3, the proposed capacitance spread reduction switched capacitor technique is explained and the operation principle is illustrated with an integrator. The design of this project using the proposed technique in programmable switched capacitor bass equalizer is then explained in Section 3.2.4.

3.2 Circuit Design and Building Blocks

3.2.1 Switch

Switch is one of the important components in switched capacitor filter design. It samples the signal to capacitors. The importance of the switch is to make accurate sample for the signal. The simplest realization of a switch is a single MOS transistor with a control signal; however a transmission gate is normally used for its good input dynamic range. A transmission gate is made up of two parallel connected NMOS and PMOS transistor. The parallel connection of two transistors is used to ensure that the switch can work from rail-to-rail, to the full range of the power supply voltage. A clock signal connected to the gate of the NMOS switch while an inverted clock signal to the gate of PMOS switch. The circuit diagram of the switch used in this project is

shown in Figure 3-2. Besides the abovementioned switch transistors, two half-sized dummy switches are added at the two terminals of the switch circuit [25]. The function of these transistors will be discussed later in this section.

The aspect ratio of M_1 (PMOS) and M_2 (NMOS) is $15\mu\text{m}/0.8\mu\text{m}$ and $5\mu\text{m}/0.8\mu\text{m}$ respectively. The aspect ratio of PMOS is chosen to be three times to that of NMOS as the mobility of NMOS is about three times to PMOS; this help to improve the linearity of the ON-resistance of switch [26]. The absolute aspect ratio W/L is determined by the required ON-resistance to satisfy to requirement of settling time.

The non-ideal effect of the switch is affecting the accuracy of sampling through the switch and hence the performance of the overall system. The non-ideal effects of the switch include the charge injection effect, capacitance-coupling effect and the non-

Figure 3-2 Switch circuit with dummy transistor

linearity effect due to switch ON resistance [27, 28].

In switched capacitor filter, the signal is stored in the form of charges on a capacitor. Error charges on a capacitor can result in incorrect filter response. A MOS switch may also contain some non-ideal effect and one of such effects is the clock feedthrough effect, contributed by the coupling of charge from the clock signal to the capacitor. This coupling of charge is due to the overlapping capacitors between the gate to source and to drain in a MOS transistor, commonly called C_{gd} and C_{gs} . When transistor is used as a switch in a switched capacitor filter, one of its terminals is always connected to a capacitor while the other is connected to a signal of interest. Lastly, a clock signal is fed to the gate of the transistor. While clock signal changes from HIGH to LOW, the switch starts to turn off. The rising and falling of the clock signal cause the feedthrough of charges to the capacitor source or drain terminal through C_{gd} or C_{gs} . This induces error in the charges to the capacitors; and the error charge is dependent on the size of switch used. The smaller the switch size, the smaller the error in the charges is. The clock feedthrough effect for clock signal from LOW to HIGH can be neglected, as the charge at the capacitor will eventually be determined by the voltage source as the switch is ON. The clock feedthrough effect causes inaccuracy in the storage charge; and such effect is a major concern in switched capacitor design as the charge in a capacitor represents the signal in the system.

Another non-ideality caused by the switch is the channel charge injection effect [25] during the elimination of the channel. When a MOS transistor is turned ON, a channel is formed by the charge between the source and the drain terminals due to the clock signal at gate. As it is turning OFF, the channel is eliminated and the channel charge is redistributed to the components connected at the source and drain. The channel

charge injection effect causes error in the storage charge similar to the clock feedthrough effect. Both channel charge injection effect and clock feedthrough are affected by the switch transistor size. The bigger the size of transistor, the greater the overlapping capacitor C_{gs} and C_{gd} is. Similarly, channels charge becomes higher with bigger transistor size.

To minimize the effect of the channel charge injection and the clock feedthrough effect, dummy switch technique is applied to the switch as shown in the circuit diagram in Figure 3-2. Two transmission gates with half aspect ratio to the switch transistor are connected at both end of the switch. The input and output terminals of the half-sized transmission gate were shorted together; as these half-size transmission gates do not affect the function of the main switch, it is called dummy switch. The dummy switches are controlled by opposite clock as the main switch transistor. When the switch is turned OFF, the two dummy switches are turned ON at the same time. The injected charge from the switch transistor channel is redistributed to the two terminals. However, the two dummy switches at the terminals are also turned ON. The channel charge that is required to form the channel at the dummy switch is cancelled by the injected charge at the switch transistor. Similarly, the clock feedthrough charge during the switch transistor turn OFF transition is cancelled by the feedthrough charge to the clock signal when dummy switch is turning ON.

The ON-resistance of the switch affects the charge settling time and this limits the sampling period for the switched capacitor clock. The ON-resistance of the switch is controlled by the size of transistor used for the switch. The greater the size of

transistor, the lower the ON-resistance is. The trade off for this reduction is the increase of the non-ideal effect of the charge injection and the clock coupling effect.

The ON-resistance value is decided based on the maximum capacitor and the sampling clock used in this project. As mentioned before, a sampling clock frequency is decided to be 400 kHz, which means the half cycle time is 1.13 μ s. The maximum capacitance value is limited to less than 20 pF. To ensure less than 0.1 % of error for the charge transmission, the $R_{ON}C$ is designed to be 20 times less than 1.14 μ s. Hence the maximum R_{ON} is limited to be less than 2.85 k ohms. The R_{ON} is designed to be 2.75 kohms with the W/L ratio shown in the circuit diagram of Figure 3-2. The simulation result for R_{ON} versus V_{in} presented in Figure 3-3 illustrates non-linearity of

Figure 3-3 Switch R_{ON} vs V_{in}

the switch used in the system. As the ON-resistance is not constant, the linearity will be affected especially when V_{in} is very low or high.

3.2.2 Op Amp

Another main building block in switched capacitor filter is the op amp. Its performance limits the accuracy of the filter designed. Their non-ideal effects can

degrade the op amp performance and these imperfections include finite gain, finite linear range, offset voltage etc [11, 29].

The finite gain of op amp will affect the gain response and frequency response of a switched capacitor filter. For a practical op amp, the voltage gain is finite. The typical low frequency gain is 40 to 100 dB depending on the topology used. The open loop gain of the op amp is recommended to be higher than 60 dB, to maintain the accuracy of the filters.

The DC offset of an op amp is amplified and propagated through the circuits. This will eventually affect the DC voltage of the output, and the dynamic range of the output posing serious problem if no offset cancellation technique is employed. A correlated double sampling gain offset compensation technique was proposed in CHAPTER 6 to resolve such offset problem as a future recommendation.

The linear range of the op amp limits the output dynamic range of the circuit and may possibly affect the signal to noise ratio (S/N). The slew rate of an op amp is important in this design and will be mention in Section 3.2.3. The proposed design made use of two phases and other important parameters of concern for the op amp that will affect the switched capacitor filter performance are noise, gain bandwidth product (GBW), etc.

The op amp used in the switched capacitor filter design is shown in Figure 3-4. A simple 2 stages op amp is used. A PMOS transistor pair is used as the input differential pair with the aspect ratio given indicated in Figure 3-4. The simple rail-to-

MHz, which is 10 times more than the sampling frequency; this is to optimize the settling time and the wideband noise aliased by the sampling frequency. Simulation results obtained for the op amp circuit at Figure 3.4 is given in Table 3.1.

Table 3.1 Simulation results obtained for the op amp in Figure 3.4

Parameter	Value	Unit
Open loop Gain	80	DB
Gain Bandwidth (GBW)	4	MHz
Phase Margin (at 50 pF load)	70	Degree
Offset Voltage	15	mV
Slew Rate (SR)	10	V/us

3.2.3 Proposed Capacitance Spread Reduction Technique and Operation

Principle

In audio application, a large sampling frequency to cutoff frequency ratio switched capacitor filter is required; so as to allow the required capacitance spread to be large as mentioned in Chapter 2. With a conventional switched capacitor integrator used, the capacitance spread is approximated to be $f_s / 2\pi f_0$. In this project, the design is for application in low frequency range, in the audio band. Hence, it is also known as a bass equalizer. The desired center frequency in this case is 50 Hz and 150 Hz, while the sampling frequency is 400 kHz. Considering the case of a 50 Hz center frequency, the capacitance spread can be estimated using the equation provided above as 1273. This capacitance spread is impractical to be realized in any system, as it will lead to problems such as difficulty in matching and large chip area.

As mentioned in Section 2.3, the two existing capacitance spread reduction techniques

introduced can achieve a reduction of capacitance spread from $f_s/2\pi f_0$ to $\sqrt{f_s/2\pi f_0}$.

This causes the requirement of for capacitance spread reduce from 1273 to 35.7.

However, the ratio of 35.7 could be still too high for the process used. To further reduce the capacitance spread in this project, a multi-phase switched capacitor

Figure 3-5 Non-inverting integrator switched capacitor integrator

integrator is proposed to further reduce the large capacitance spread problem in audio applications. With this improved circuit, the ratio can be further reduced from the proposed circuit of [24] and [25]. The operation principle of the proposed improved capacitance spread reduction technique is illustrates by a non-inverting switched capacitor integrator. The circuit is given in Figure 3-5. The multi-phase sampling clock scheme is illustrated in Figure 3-6.

The non-inverting integrator presented in Figure 3-5 is a multiphase non-inverting integrator. The operation of the capacitor spread reduction technique will be explained

Figure 3-6 Multi-phase clock scheme for proposed switched capacitor integrator

next. The transfer function of the integrator and the effect of op amp offset voltage will be derived next.

(i) Operation principle of the proposed capacitor spread reduction technique

By applying the multi-phase structure, together with the use of the charge differencing technique, a further reduction of capacitance spread can be achieved. Two main phases, ϕ_1 and ϕ_2 of the sampling clock are used in the system with equal duty cycle and non-overlapping. For each main clock, it is divided into two sub-phases and hence the various phases are ϕ_{1a} , ϕ_{1b} , ϕ_{2a} , and ϕ_{2b} respectively.

In Figure 3-7, the connection of the integrator circuit at phase ϕ_{1a} has been given with the op amp offset voltage expressed in V_{OFF} , which is considered constant. Assumptions have been made such that input signal V_{IN} only changed at phase ϕ_2 and C_I and C_A are fully discharged before phase ϕ_{1a} , which will be shown later. During phase ϕ_{1a} , the input signal V_{IN} is sampled at C_I . The charges of value $C_I V_{IN}$ are

transferred to C_A and set the output voltage at this phase. With the capacitance of C_A selected to be bigger than C_I , the output voltage V_{oIa} at this phase will be the attenuation of the V_{IN} . Hence the output voltage will be small at this phase. The output signal at this phase can be derived as:

At $t = (n-1/2)T$, phase ϕ_{Ia}

$$V_{OUT}[(n-1/2)T] = -\frac{C_I}{C_A} * V_{in}[(n-1)T] + \frac{(C_I + C_A)}{C_A} * V_{OFF} \quad \text{Eq[3-1]}$$

Figure 3-7 Proposed switched capacitor integrator at ϕ_{Ia}

In the meantime, the output signal is sampled at C_B at this phase. The charges on C_B at this phase are $C_B * \{V_{OUT}[(n-1/2)T] - V_{OFF}\}$. There is no charge transferred in or out for C_{A2} at this phase, C_{A2} carries the memory of the output voltage from previous phase ϕ_2 , which is,

$$V_{CA2}[(n-1)T] = V_{CA2}[(n-1/2)T] = V_{OUT}[(n-1)T] - V_{OFF} \quad \text{Eq[3-2]}$$

Figure 3-8 Proposed switched capacitor integrator at ϕ_{1b}

The connection of integrator circuit at phase ϕ_{1b} is illustrated in Figure 3-8. The connection of C_B is disconnected from the output of op amp and it keeps the charge at ϕ_{1a} . Charges on C_{A2} remained unchanged at this phase. C_{A1} is connected in parallel with C_A and is connected to the output of the op amp and the inverting input of the op amp. There is no charge transfer from C_1 . Hence the charge at C_A is divided between the two capacitors C_A and C_{A1} , depending on the capacitance values. The output voltage at phase ϕ_{1b} is hence expressed as:

At $t = [(n-1/4)T]$, phase ϕ_{1b} ,

$$V_{OUT}[(n-1/4)T] = -\frac{C_1}{C_A + C_{A1}} * V_{in}[(n-1)T] + \frac{(C_1 + C_A + C_{A1})}{C_A + C_{A1}} * V_{OFF} \quad \text{Eq[3-3]}$$

There is no net charges difference at C_B and C_{A2} at ϕ_{1b} .

At phase ϕ_2 , the connection of circuit will be as that shown in Figure 3-9. C_I and C_A are discharged to ground and will have no effect to the output voltage during this phase. C_{A1} and C_B are discharged through the inverting input of the op amp to the integrating capacitor C_{A2} . The charge transferred to C_{A2} by C_{A1} and C_B is different in

Figure 3-9 Proposed switched capacitor integrator at ϕ_2

polarity due to the connection. The overall charge transferred to C_{A2} ΔQ is reduced due to the charge differencing in this phase as shown in Eq[3-4]. The output voltage at this phase is therefore found in Eq[3-5].

$$\Delta Q = \{ \{ V_{OUT} [(n-1/4)T - V_{OFF}] \} * C_{A1} - \{ V_{OUT} [(n-1/2)T] - V_{OFF} \} * C_B \}$$

Substituting Eq[3-1] and Eq[3-3] into equation above,

$$\begin{aligned} \Delta Q = & V_{IN} [(n-1)T] * \left(-\frac{C_I}{C_A + C_{A1}} * C_{A1} + \frac{C_I}{C_A} * C_B \right) \\ & + V_{OFF} * \left(C_B + \frac{C_I + C_A + C_{A1}}{C_A + C_{A1}} * C_{A1} - \frac{C_I + C_A}{C_A} * C_B \right) \end{aligned}$$

$$\begin{aligned}
 &= V_{IN}[(n-1)T] * \left(\frac{C_B C_1 * (C_A + C_{A1}) - C_A C_1 C_{A1}}{C_A * (C_A + C_{A1})} \right) \\
 &+ V_{OFF} * \left(\frac{C_A C_{A1} * (C_1 + C_A + C_{A1}) - C_B C_1 * (C_A + C_{A1})}{C_A * (C_A + C_{A1})} \right) \\
 V_{OUT}(nT) &= \frac{\Delta Q}{C_{A2}} + V_{CA2}[(n-1)T] + V_{OFF}
 \end{aligned} \tag{Eq[3-4]}$$

By substituting Eq[3-2] and Eq[3-4] into equation above,

$$\begin{aligned}
 V_{OUT}(nT) &= V_{IN}[(n-1)T] * \left(\frac{C_B C_1 * (C_A + C_{A1}) - C_A C_1 C_{A1}}{C_A * (C_A + C_{A1})} \right) / C_{A2} \\
 &+ V_{OFF} * \left(\frac{C_A C_{A1} * (C_1 + C_A + C_{A1}) - C_B C_1 * (C_A + C_{A1})}{C_A * (C_A + C_{A1})} \right) / C_{A2} \\
 &+ V_{OUT}[(n-1)T] - V_{OFF} + V_{OFF} \\
 &= V_{OUT}[(n-1)T] + V_{IN}[(n-1)T] * \frac{C_1 C_A * (C_B - C_{A1}) + C_B C_1 C_{A1}}{C_A C_{A2} * (C_A + C_{A1})} \\
 &+ V_{OFF} * \frac{C_1 C_A * (C_{A1} - C_B) + C_A C_{A1} * (C_A + C_{A1}) - C_B C_1 C_{A1}}{C_A C_{A2} * (C_A + C_{A1})}
 \end{aligned} \tag{Eq[3-5]}$$

Change Eq[3-5] into z-domain expression:

$$\begin{aligned}
 V_{OUT}(z) &= V_{IN}(z) * \frac{C_1 C_A * (C_B - C_{A1}) + C_B C_1 C_{A1}}{C_A C_{A2} * (C_A + C_{A1})} * \frac{z^{-1}}{1 + z^{-1}} \\
 &+ V_{OFF} * \frac{C_1 C_A * (C_{A1} - C_B) + C_A C_{A1} * (C_A + C_{A1}) - C_B C_1 C_{A1}}{C_A C_{A2} * (C_A + C_{A1})} * \frac{1}{1 + z^{-1}}
 \end{aligned} \tag{Eq[3-6]}$$

From Eq[3-6], it can be seen that, a z-domain integrator transfer function is obtained as well as the effect of the op amp offset voltage. When only input signal is considered, C_B is chosen to be of equal value as C_{A1} . This eliminates the first term in numerator and simplifies the overall equation. Hence, the above equation with only input signal considered becomes:

$$V_{OUT}(z) = V_{IN}(z) \frac{C_{A1} \cdot C_1 \cdot C_B \cdot z^{-1}}{C_A \cdot (C_A + C_{A1}) \cdot C_{A2} \cdot (1 - z^{-1})} \tag{Eq[3-7]}$$

By comparing Eq[3-7] with Eq[2-6], it can obtain

$$\frac{C_{A1} \cdot C_1 \cdot C_B}{C_A \cdot (C_A + C_{A1}) \cdot C_{A2}} = \frac{2\pi f_0}{f_s} \quad \text{Eq[3-8]}$$

From the above equation, by making C_{A1} , C_1 and C_B unit capacitance, and C_A and C_{A2} the largest size capacitors in the integrator design, it is possible to achieve a very large ratio and hence the capacitance spread can be reduced. The two capacitances are selected to be the same for the reason of better matching and ease of design. By assuming C_{A1} is to be much smaller than C_A , the term $(C_A + C_{A1})$ can be estimated as C_A . The capacitance spread can now be approximated as $\sqrt[3]{f_s / 2\pi f_0}$. This technique has further reduced the capacitance spread. To summarize, this structure has not only reduced the capacitance spread but also reduced the capacitance area required. The effect of this technique can be illustrated by the equalizer design in this project.

For a switched capacitor filter design with a clock frequency of 400 kHz and the center frequency of 50 Hz, the capacitance spread of this setting with conventional integrator structure will be $f_s / (2\pi f_0) = 1273$ using Eq[2-5]. With the previous capacitance spread reduction technique, the capacitance spread will be $\sqrt{f_s / 2\pi f_0} = 35.7$. However, using the proposed technique, the capacitance spread can be further reduced to approximately $\sqrt[3]{f_s / 2\pi f_0} = 11.2$, which is 70% less than previous capacitance spread reduction technique. This is a significant improvement in either capacitance spread reduction or area reduction.

For this technique, as the dummy phase ϕ_1 for the integrator has been used for attenuating the input signal; the output signal at ϕ_2 is the only desired integrator output. The output of op amp at different clock phase has large difference and hence

the slew rate of the op amp needs to be high enough for the fast change at op amp output from one phase to the other.

The abovementioned is a non-inverting switched capacitor integrator design using the capacitance spread reduction technique proposed. Similarly, an inverting multi-phase integrator can be obtained by simply changing the clock phases at the input sampling capacitor as shown in the Figure 3-5 with the clock phase replaced by that stated inside the parentheses. The transfer function for this inverting integrator can be found as Eq[3-9] using similar approach.

$$H(z) = -\frac{C_{A1} \cdot C_1 \cdot C_B \cdot z^{-1}}{C_A \cdot (C_A + C_{A1}) \cdot C_{A2} \cdot (1 - z^{-1})} \quad \text{Eq[3-9]}$$

(ii) Disadvantage of the proposed technique and design precaution

The disadvantage of this proposed design is the parasitic sensitivity to the parasitic capacitor C_p at node B, which is formed by the parasitic capacitor of top plate to substrate of C_B and the overlapping of the metal layer to the substrate. It will affect the performance of the integrator. Therefore, the connection to node B needed to be carefully designed so as to minimize the parasitic capacitor and hence the error to the system. As the capacitance C_B is chosen to be unit capacitance, the switches connected to it can be minimized. The minimum size transmission gates without dummy switches are used at this point as the voltage at this node is always closed to ground. The simulation file for the abovementioned integrator for SWITCAP simulation was given in Appendix B.

3.2.4 Switched Capacitor Equalizer Design Using Proposed Capacitance Spread Reduction Technique

The design of the 2nd order switched capacitor filter [30] starts with the biquadratic equation in s-domain as shown in Eq[3-10].

$$H(s) = -\frac{s^2 + \frac{\omega_{0z}}{Q_z}s + \omega_{0z}^2}{s^2 + \frac{\omega_{0p}}{Q_p}s + \omega_{0p}^2} \quad \text{Eq[3-10]}$$

where ω_{0p} and ω_{0z} are the center frequency of poles and zero respectively, Q_p and Q_z are the Q-factor of poles and zero respectively.

The s-domain transfer function is transformed into z-domain transfer function by bilinear s-z transformation [31]. The relationship between s and z can be expressed as in Eq[3-11].

$$s = \frac{2}{T} \cdot \frac{1-z^{-1}}{1+z^{-1}}, \quad \text{where } T = 1/f_{\text{sampling}} \quad \text{Eq[3-11]}$$

By substituting Eq[3-11] into Eq[3-10], the z-domain transfer function, $H(z)$, is obtained in Eq[3-12].

$$H(z) = -\frac{\left[\frac{4 + 2\frac{\omega_{0z}T}{Q_z} + (\omega_{0z}T)^2}{D} \right] z^2 + \left[\frac{2(\omega_{0z}T)^2 - 8}{D} \right] z + \left[\frac{4 - 2\frac{\omega_{0z}T}{Q_z} + (\omega_{0z}T)^2}{D} \right]}{\left[\frac{(\omega_{0p}T)^2 + 2\frac{\omega_{0p}T}{Q_p} + 4}{D} \right] z^2 + \left[\frac{2(\omega_{0p}T)^2 - 8}{D} \right] z + 1} \quad \text{.....Eq[3-12]}$$

$$\text{where } D = (\omega_{0p}T)^2 - 2\frac{\omega_{0p}T}{Q_p} + 4$$

Figure 3-10 Proposed biquadratic switched capacitor filter bass equalizer

Figure 3-11 Signal flow graph (SFG) of the switched capacitor bass equalizer

In this project, a switched capacitor second order audio filter with the center frequency of 50 Hz is to be designed. Using a sampling clock of 400 kHz, the capacitance spread required would be high. Hence, the technique proposed in last section has to be used in this design. The design of the filter is based on a conventional biquad filter with the integrator replaced by the integrator proposed in last section. The schematic for the biquad filter is given in Figure 3-10. The signal flow graph is given in Figure 3-11.

From the signal flow graph, the integrator function can be compared with that of the conventional integrator. The capacitance assignment for this improved switched capacitor filter can be approximated in Eq[3-13].

$$\begin{aligned}
 C_A &= C_{A2} = C_C = C_{C2} = 10.5 \\
 C_{A1} &= C_B = C_{C1} = C_D = 1 \\
 C_2 &= \frac{1}{Q_z} \\
 C_5 &= \frac{1}{Q_p} \\
 C_6 &= 10.5
 \end{aligned} \tag{Eq[3-13]}$$

The capacitance spread in this design is 10.5 and is actually slightly smaller than the value $\sqrt[1/3]{\frac{f_s}{2\pi f_0}}$ estimated before.

By implementing the proposed capacitance spread technique on the switched capacitor bass equalizer, the simulation output waveform can be shown in Figure 3-10. The waveform at the output of the switched capacitor bass circuit consists of signal at two main phases, one of them is so called dummy phase which contain undesired signal; while the other is the output phase.

From Eq[3-13], it can be seen that the mid-band gain and Q-factor can be controlled by changing capacitors C_2 and C_5 individually, whereas the center frequency is controlled by changing both C_A and C_C together. The value of capacitors is programmed using capacitor banks, by digitally switching on one or some switches.

Figure 3-10 Output waveform from simulation

With changing the values of C_2 and C_5 , the gain programmability can be achieved.

They are controlled with the capacitance bank. Figure 3-11 indicates the frequency

Figure 3-11 Frequency response of the proposed programmable switched capacitor biquad filter

response at four settings programmed for the switched capacitor bass equalizer. The settings are: 50 Hz center frequency with gain at 6 and 12 dB respectively; 150 Hz center frequency with gain at 6 dB and 12 dB. The programmability of the center

frequency can be done by changing C_A and C_C simultaneously. The two capacitors are set to be same for simplicity, and capacitors C_{A2} and C_{C2} are each set to fixed value of 10.5. For the center frequencies of 50 Hz and 150 Hz, the value for C_A and C_C are 10.5 and 5.9 respectively.

3.2.5 Bandgap and Biasing Circuit

The main power supply for the IC is 9 V while the V_{DD} for the MOSFET in the process used is 5 V. In the voltage reference design, a 5 V voltage is required for the voltage supply of switched capacitor filter; it is designed using a bandgap circuit. The biasing current generated from the bandgap circuit having the requirement of less temperature dependent.

From the schematic in Figure 3-12, the current at collector of Q_{12} and Q_{13} is designed

Figure 3-12 Bandgap circuit for biasing voltage and current

to be 50 μA that is determined by Eq[3-14] where resistor R_9 is chosen to be 930 ohms. It is known as current proportional to absolute temperature (I_{PTAT}) as the current is directly proportional to the temperature term in V_T as shown in Eq[3-14]. In the process used in this project, the I_S in the bipolar model is lower; V_{BE} is assumed to be 0.8 V in the equations below. The voltage reference V_{BG} is connected out from the base of Q_{12} , the voltage value is 1.25 V with R_{10} chosen to be 4000 ohms as shown in Eq[3-15].

$$I_{PTAT} = \frac{V_T}{R_9} \cdot \ln 6 = 50 \mu\text{A} \quad \text{Eq[3-14]}$$

$$V_{BG} = V_{BE} + I_{PTAT} \cdot R_9 + 2 \cdot I_{PTAT} \cdot R_{10} = 1.25 \text{V} \quad \text{Eq[3-15]}$$

$$I_{BIAS} = \frac{V_{BE18} + I_{PTAT} \cdot R_{11}}{R_{12}}$$

The estimated temperature dependence is shown in Eq[3-16],

$$\frac{\delta I_{BIAS}}{\delta T} \approx \frac{\frac{\delta V_{BE18}}{\delta T} + \frac{V_T}{T} \cdot \ln 6 \cdot \frac{R_{11}}{R_9}}{R_{12}} \quad \text{Eq[3-16]}$$

From Eq[3-15], the current I_{BIAS} of 50 μA is generated from I_{PTAT} by selecting R_{11} and R_{12} to be 12.5 k Ω and 28.5 k Ω respectively. The temperature dependency can be derived from Eq[3-16] where the temperature coefficient of V_{BE} is -2 mV .

The V_{BG} of 1.25 V is used to generate the voltage source of 5 V and the reference voltage of 2.5 V throughout the design of the switched capacitor filter design.

3.2.6 Sample and Hold Circuit

Figure 3-13 Switched capacitor S/H circuit

Base on the topology used for the proposed switched capacitor filter, the output signal of the designed filter consists of two different signals while only one is desired. The signal at one of the phase is attenuated and the other signal is the integrated signal, which is the desired signal. The output signal needs to be sampled at the phase with desired signal that is phase 1 in this project. A sample and hold circuit (S/H) using switched capacitor filter is employed after the switched capacitor filter. It is shown in Figure 3-13.

At clock phase ϕ_2 , the signal at input V_{in} is sampled at C_1 , while the voltage at C_2 is remained as the output voltage at previous clock phase. At the meantime, capacitor C_3 is charged to the output voltage at this phase. The connection is shown in Figure 3-16. The direction of the arrows in the figure shows the direction of the flow of charge.

At clock phase ϕ_1 as shown in Figure 3-17, the charge at C_1 , which contain the input signal at previous clock phase, is fully discharged through the inverting input of the op amp into C_2 . In the meantime, the charge at C_3 , which contain the output signal at previous clock, is fully discharged to C_2 too. Due to the connection of C_1 and C_3 , the

Figure 3-16 S/H circuit at phase ϕ_2

Figure 3-17 S/H circuit at phase ϕ_1

capacitors are discharged in opposite polarity, which cause the effective charge into capacitor C_2 become the different between current charge (or voltage) and previous

charge (or voltage). The direction of the charge flow is shown in the figure, indicating the different direction of charge flow from C_1 and C_3 . By selecting all three capacitors values same, the change in output voltage will follow the change in input voltage with half a cycle delay. The response can be derived as below.

Firstly, at $t = (n-1)T$, (clock phase 1)

$$\begin{aligned} V_{C1}[(n-1)T] &= V_{C3}[(n-1)T] = 0 \\ V_{C2}[(n-1)T] &= V_{out}[(n-1)T] \end{aligned} \quad \text{Eq[3-17]}$$

At $t = (n-1/2)T$, (clock phase 2)

$$\begin{aligned} V_{C1}[(n-1/2)T] &= V_{in}[(n-1/2)T] \\ V_{C2}[(n-1/2)T] &= V_{out}[(n-1/2)T] = V_{out}[(n-1)T] \\ V_{C3}[(n-1/2)T] &= V_{out}[(n-1/2)T] = V_{out}[(n-1)T] \end{aligned} \quad \text{Eq[3-18]}$$

At $t = (nT)$, (clock phase 1)

$$\begin{aligned} V_{C1}(nT) &= V_{C3}(nT) = 0 \\ V_{C2}(nT) &= V_{out}[(n-1)T] - \Delta Q(nT)/C_2 \end{aligned} \quad \text{Eq[3-19]}$$

where ΔQ is the overall charge into the negative terminal C_2 , and

$$\begin{aligned} \Delta Q &= C_3.V_{C3}[(n-1/2)T] - C_1.V_{C1}[(n-1/2)T] \\ &= C_3.V_{out}[(n-1)T] - C_1.V_{in}[(n-1/2)T] \end{aligned} \quad \text{Eq[3-20]}$$

Hence, by choosing same value for C_1 , C_2 and C_3 , the output voltage at phase 1 becomes,

$$V_{out}(nT) = V_{in}[(n-1/2)T] \quad \text{Eq[3-21]}$$

To express the output voltage in z-domain,

$$V_{out}(z) = V_{in}(z)z^{-1/2} \quad \text{Eq[3-22]}$$

The signal at the output of the sample and hold circuit is of a half cycle delay of the input voltage, at phase ϕ_1 , and hold for one cycle. As capacitor C_3 is sensitive to the parasitic capacitance, the parasitic capacitance will affect the performance of the sample and hold circuit, the layout of the junction for the capacitor C_3 and the switches is carefully drawn, with shortest distance and smallest possible MOSFET aspect ratio.

3.2.7 Lowpass Filter (AAF & SMF)

The anti-aliasing filter (AAF) and smoothing filter (SMF) are generally low pass filters to filter the high frequency noise for the input and the switched capacitor filter output. In fact, the switched capacitor filter outputs is going through a sample and hold circuit (S/H) before input to the smoothing filter.

Figure 3-18 LPF used as the smoothing filter (SMF) and anti-aliasing filter (AAF)

The low pass filter used here is a second order RC active filter with a cutoff frequency at 20 kHz. As the cutoff frequency is high enough, the derived resistor and capacitor can be integrated. A second order low pass filter is hence a reasonable choice for its

simplicity and higher cutoff rate at cutoff region. The schematic of the low pass filter used is given as in Figure 3-18, while the frequency response of the low pass filter is

Figure 3-19 LPF Response

plotted in Figure 3-19:

3.2.8 Non Overlapping Clock Generator

An external clock is used as the source of the sampling clock in this project. As a multi-phase sampling clock technique is proposed to reduce the capacitance spread, it is required that the sampling clock has two main phases namely ϕ_1 and ϕ_2 . Then two non-overlapping sub-phases are required for each main phase. A digital circuitry is needed to generate the sampling clock. The circuit is given in Figure 3-20.

The external clock frequency is 800 kHz for this project. The frequency is halved to 400 kHz by a frequency divider. Gone through the non-overlapping clock generator,

the two main clocks ϕ_1 and ϕ_2 are obtained. The non-overlapping clock generator circuit is depicted in Figure 3-21.

These two clocks are then mixed with input clock Clk_{in} and inverted input clock $\overline{\text{Clk}}_{\text{in}}$

Figure 3-20 Multi-phase non-overlapping clock generator

Figure 3-21 Multi-phase non-overlapping clock generator circuit

using AND gate to give the sub-phases ϕ_{1a} , ϕ_{1b} , ϕ_{2a} and ϕ_{2b} , which are used in the switched capacitor filter and sample-and-hold circuit. The multi-phase clocks response generated are referred to Figure 3-6.

CHAPTER 4 LAYOUT OF THE CIRCUITS

In this chapter, the layout of the building blocks described in Chapter 3 is shown. The building blocks are switches, op amp, low pass filter etc. The necessary precautions in the layout drawing such as the routing of the ground for the digital and the analog circuit; and the matching of transistor are discussed in detail in this chapter. [23]

4.1 Layout of Transmission Gate Switch

The layout of the transmission gate switch together with dummy switches described earlier in Section 3.2.1 is shown here in Figure 4-1. It is equivalent to the circuit

Figure 4-1 Layout of switch with dummy switch

illustrated in Figure 3-2. The PMOS transistors are drawn at the upper half of the switch while the NMOS transistors are drawn at the lower half of the switch. As mentioned in Chapter 3, for process that involves twin-well technology, it is necessary to have the island of the PMOS and NMOS transistor biased to the most positive potential, which is V_{DD} and the most negative potential, i.e. ground in this case, respectively.

The size of PMOS transistor is chosen to be three times to that of the NMOS transistor simply to match the mobility between the PMOS and NMOS. The dummy switch is designed to be of half the size of the main switch. For the purpose of better matching, the unit transistor is of the same size as that of dummy switch. Four transistors are provided for both the NMOS and PMOS each. M_1 and M_2 are the PMOS and NMOS transistor for the switch while MP_{dummy} and MN_{dummy} represent the dummy switches. The control signal Clock and /Clock are two digital control signal with opposite logic. It is used to control the ON and OFF of the switch.

4.2 Layout of Op Amp

The layout of the op amp described in Section 3.2.2 is presented in Figure 4.2. The input PMOS transistors $M1$ and $M2$ are layout in a way called interdigitation [33, 34]. The input transistors are divided into four transistors with smaller aspect ratio and connected alternatively; this is illustrated in Figure 4.3. By employing this layout technique, the matching of input transistors can be optimized and hence reduce op amp offset. $M3$ and $M4$ are the current source transistors for the input transistors pair and the output stage respectively. The active loads of the input stage are in bipolar

transistors indicated as $Q1$ and $Q2$ in Figure 4.2. These transistors are drawn to be symmetrical to each other to achieve better matching and reduce offset.

Figure 4-2 Layout of op amp used in switched capacitor filter

Figure 4-3 Interdigitated connection of the input transistor M_1 and M_2

4.3 Layout of Low Pass Filter

Figure 4.4 depicts the layout of the low pass filter discussed in Section 3.2.6. The resistors used for the low pass filter are the SP (shallow P) type resistor as its sheet

Figure 4-4 Layouy of LPF used in switched capacitor filter as SMF and AAF

resistance is higher than PS (poly-silicon) resistor of less process variant. The layout design of the low pass filter shown in Figure 4.4 is used for both the Anti-aliasing Filter and the Smoothing Filter in this project.

Figure 4-5 Cross-sectional view for SP resistor

As the SP resistor used in the LPF design is a diffusion type resistor, which is located in a resistor island of n-, island biasing is required (see in Figure 4.5) to avoid the

non-linearity effect due to the parasitic PN junction formed. As explain earlier in Figure 4.4 for the layout of the SP resistor used in the LPF is placed in a common island with the SP resistor island biased to the highest potential point, i.e. VDD of 5 V.

4.4 Layout of Non-overlapping Clock Generator

The non-overlapping clock generator for the sample and hold circuit is depicted in Figure 4.6. The input CLK_{in} is input from external clock generator. There are six outputs ϕ_1 , ϕ_{1a} , ϕ_{1b} , ϕ_2 , ϕ_{2a} and ϕ_{2b} , derived from CLK_{in} to the switched capacitor filter and sample-and-hold circuit.

Figure 4-6 Layout of non-overlapping clock generator

4.5 Layout of Sample-and-hold Circuit

The graph depicted in Figure 4.7 is the layout of the sample-and-hold circuit as mention Section 3.2.6. It is formed with switches, capacitors and an op amp. The capacitors C_1 , C_2 and C_3 used are the capacitors among the capacitors bank in the layout of bass equalizer. As it can be seen from the figure, the capacitors are placed

Figure 4-7 Layout of sample-and-hold circuit

far apart from the switches and op amp; it required long wire for the connection. This increases the capacitance effect to the circuit.

4.6 Switched Capacitor Bass Equalizer

In Figure 4.8 the switched capacitor bass circuit is provided. In a switched capacitor filter layout, in order to ease the layout and to reduce the complexity, the three main components: switches, capacitors and op amp, are grouped together. In this layout, the components at the first row are the switches. The sampling clock signal is connected to the switches from below. This is to prevent the crossing of the control signal with the input signal that can result in coupling noise of clock into the system.

The capacitor bank is placed at the top of the switches with signal lines between them. The capacitors are drawn identically for better matching [35] in unit size of 1pF. The non-overlapping clock generator is placed at the right part of the capacitor bank.

At the top of the capacitor bank, op amps OP1 and OP2 for the switched capacitor bass equalizer are placed. The sample and hold circuit is placed besides the op amps. The two low pass filters that function as the anti-aliasing and smoothing filter were placed above the op amps. Finally, the 5 V voltage reference generator is placed on top of the filters.

Figure 4-8 Layout of the switched capacitor bass equalizer

In Figure 4.9, the top view for part of the capacitor bank, with four capacitors, is illustrated. Each of the capacitors is isolated from each other and the isolation layer is biased to ground, the most negative potential, to prevent the substrate noise coupling to the capacitor, which may affect the performance. Signal path is routed on top of the

Figure 4-9 Top view for capacitor bank with four capacitors shown

isolation layer between capacitors and not on the capacitor area to prevent the crosstalk effect.

4.7 Layout of the Whole Chip and the Micrograph of the IC

As switched capacitor filter is a sampled data circuit, high frequency clock is required. This may then induce crosstalk problem, especially if the layout of the design is not done properly. The digital ground for the clock generator and the analog ground for circuits such as filter, op amp and switches are each using different pins. The layout of the analog ground is of a star-connection, with the ground of each building is separated but joined to the analog ground pin individually. This minimizes crosstalk effect due to ground. The capacitor island isolation mentioned in Section 4.5 is also one of the ways to prevent crosstalk. The layout for the ground is illustrated is Figure 4.10 [36].

The layout of the microchip is presented in Figure 4.11. The micrograph of the microchip fabricated is given also in Figure 4.11. In the whole chip, dummy

components such as extra switches and capacitors are included for future use. The measurement result will be discussed in next chapter.

Block diagram showing the layout plan and the pin assignment is depicted in Figure 4.12. The proposed circuit has been fabricated using Panasonic 0.8 mm BiCMOS process and assembled into microchip with 30 pins ceramic package. It can be seen that there are two 5 V Vdd pins for digital circuits and analog circuits. These voltages are generated by the bandgap circuit within the microchip and the connection to the output pin is for the purpose of evaluating the performance of the bandgap.

Figure 4-10 Ground line routing for the microchip

BSCTL1 and BSCTL2 are the digital control pins for the control of center frequency and gain at center frequency respectively. BSCTL3 is the digital control pin controlling the availability of the bass equalizer's op amp 1 output to BS1OUT of pin 11. Output signal of op amp can be measured at BS1OUT pin when BSCTL3 is made

HIGH. BSOUT pin is the output pin for op amp 2 of bass equalizer. SHIN and SHOUT are input and output for the sample-and-hold block. These pins are for the evaluation of sample-and-hold block. Similarly, SMFIN is the pin for the measurement of smoothing filter.

Figure 4-11 Layout of the whole chip and the micrograph of the IC

Figure 4-12 Microchip layout plan and pin assignment

CHAPTER 5 MEASUREMENT RESULTS

5.1 Overview

The circuit proposed in this project has been fabricated with the BiCMOS process as described in Section 3.1 and tested in ceramic package. The test chip consists of two low pass filters, switched capacitor bass equalizer, with two gain setting and two different center frequency, and sample and hold circuit as shown in Figure 5-1. Measurement has been done on each functional block for the performance. These blocks include the LPF(SMF), S/H circuit and the whole chip. The following is the block diagram of the microchip.

Figure 5-1 Block diagram for test chip

In Section 5.2, the measurement results for the low pass filter used as smoothing filter and anti-aliasing filter are given. The sample and hold circuit was measured and presented in Section 5.3. Finally, the measurement results for the whole chip are given in Section 5.4. The reasoning behind the problems encountered in low pass filter and the sample and hold circuit are given in respective section while the suggestion for the solutions to the problem encountered for the whole chip are given in CHAPTER 6.

5.2 Low Pass Filter (for SMF and AAF) Measurement Result

The frequency response of the 2nd orders low pass filter (LPF) was measured and shown in Figure 5-2. The measured frequency response is similar to the simulation result for this conventional RC active LPF as described in Section 3.2.7. The cutoff frequency for this filter obtained is about 19.5 kHz, which is closely matched to the designed value of 20 kHz.

Figure 5-2 LPF response (simulation vs measurement)

The total harmonic distortion (THD) result for the LPF is shown in Figure 5-3.

Figure 5-3 LPF THD result

From Figure 5.3, it can be seen that the THD is between the ranges of 0.1 % to 1 % for input voltage from 0.1 Vrms to 1.5 Vrms. For input voltage higher than 1.5 Vrms, clipping at the output voltage become obvious, which is normal as it is approaching

the power supply and ground potential. But the THD performance of the low pass filter is unsatisfactory as it is much higher than the simulation result, which is at about 0.02%.

The THD imperfection of the low pass filter is due to the epi island biasing for the resistor used. Referring to Figure 3.19 for the circuit of the low pass filter used, as the resistor value of 250 kohms is too large to be realized with a low resistivity polysilicon (PS) resistor, diffusion type shallow-P (SP) resistor was used. The used of this diffusion type resistor requires cautious island biasing, as the resistance is non-linear due to the voltage dependence of parasitic PN junction formed by the resistor body and the island biasing as shown in Figure 5.4. These large value resistors are shown in Figure 4.5 as R_2 , R_5 and R_6 . The SP island biasing is located at just one terminal of the resistor as depicted in Figure 5.4(a), which is not good enough to reduce the parasitic PN junction induced non-linearity effect. It was advisable to have the epi island biasing evenly distributed, for instance, the biasing put at both sides of the resistor

Figure 5-4 Top view of SP resistor (a) original of island biasing (b) Recommended placement of island biasing

body as illustrated in Figure 5.4. The approach depicted in Figure 5.4 (a) is adopted in this project, however, it is recommended to change to the layout of Figure 5.4 (b) to avoid the island biasing dependence affecting the result.

5.3 Sample and Hold (S/H) Circuit Measurement Result

As the switched capacitor filter in this project using multi-phase approach, the function of the sample and hold circuit is required to sample the output at the desired phase of the switched capacitor filter output. The sample and hold circuit is measured at S/H OUT with the signal input at S/H IN. The input voltage is a sine wave with amplitude of 0.2 Vrms. The frequency response of sample and hold circuit is shown in Figure 5-5 while the measured THD result is plotted in Figure 5-6 against the simulation result.

Figure 5-5 Sample and Hold Circuit Frequency Response

The THD performance of the sample and hold circuit is measured with input of sine wave of 1 kHz and varying input magnitude from 0.1 Vrms to 1.5 Vrms. The measured result is similar to the simulation except the simulation result shows worse THD response at higher input level from about 0.7 Vrms.

Figure 5-6 Sample and Hold Circuit THD Performance

The frequency response of the measured sample and hold circuit given in Figure 5.5 is shown to have lower gain magnitude than the simulation result of about -0.2 dB flat frequency response. In this case, an attenuation of $0.5 \sim 0.6$ dB is measured in the microchip. This deviation from the simulation is due to the parasitic capacitor C_p in the layout design, which occurs in parallel with C_3 as given in Figure 5.7 with respect to ground. The parasitic capacitance with respect to ground for the bottom plate of the capacitor in the process is about 5 % of the drawn capacitance as given in the diffusion process manual. The capacitor C_3 is a parasitic sensitive capacitor.

Figure 5-7 Sample and hold circuit with parasitic capacitor C_p

It can be seen from Eq[3-17] that at the output phase of sample and hold circuit, which is at phase 1,

$$V_{out}(nT) = V_{C_2}(nT) = V_{out}[(n-1)T] - \Delta Q(nT) / C_2 \quad \text{Eq[5-1]}$$

where ΔQ is the overall charge flow into the negative terminal of C_2 , and

$$\Delta Q = C_3 \cdot V_{out}[(n-1)T] - C_1 \cdot V_{in}[(n-1/2)T] \quad \text{Eq[5-2]}$$

Hence if the mismatch of the capacitance is considered,

$$\begin{aligned} V_{out}(nT) &= V_{out}[(n-1)T] - \{C_3 \cdot V_{out}[(n-1)T] - C_1 \cdot V_{in}[(n-1/2)T]\} / C_2 \\ &= V_{out}[(n-1)T] \cdot (1 - C_3 / C_2) + V_{in}[(n-1/2)T] \cdot C_1 / C_2 \quad \text{Eq[5-3]} \end{aligned}$$

From the equation above, as the used of C_1 and C_2 are insensitive to parasitic capacitance, it can be assumed well match, and hence the output become

$$V_{out} = V_{out}[(n-1)T] \cdot (1 - C_3 / C_2) + V_{in}[(n-1/2)T] \quad \text{Eq[5-4]}$$

The output voltage at phase 1 should follow the input voltage at phase 2 with a half period delay and an error voltage is introduced due the parasitic capacitance at C_3 .

The error of the output voltage is due to the parasitic capacitance of C_3 , which cause an error of about $-0.05 \cdot V_{out}[(n-1)T]$, an estimated of 5 % drop from expected result.

This is an error of about -0.45 dB.

5.4 Whole Chip Measurement Result

The switched capacitor bass equalizer fabricated in this microchip is programmable for a gain setting of 6 dB and 12 dB with the center frequency programmable at 50 Hz and 150 Hz. The measurement result overlapped with simulation result is shown in Figure 5-8. All the results are obtained at $Q = 1$.

Figure 5-8 Frequency Response for SCF (Measurement result vs simulation result)
(a) Setting: $A_0 = 12\text{dB}$ $f_0 = 150\text{Hz}$ (b) Setting: $A_0 = 6\text{dB}$ $f_0 = 150\text{Hz}$
(c) Setting: $A_0 = 12\text{dB}$ $f_0 = 50\text{Hz}$ (d) Setting: $A_0 = 6\text{dB}$ $f_0 = 50\text{Hz}$

The curves depicted in Figure 5.8 show the measured frequency response of the microchip at the four settings overlapping with the simulation results. At the setting of 150 Hz center frequency, the center frequency can be distinguished; however the center frequency gain has dropped significantly as compared with the designed value. For instance, the gain achieved for 12 dB setting is only about 8.5 dB in the microchip. At a setting of 50 Hz center frequency, the center frequency can still be distinguished from the 12 dB gain setting while not for the case of 6 dB gain setting.

In Figure 5.9 and Figure 5.10, the waveforms at the output of first and second op amp of the switched capacitor bass equalizer; the output of sampled and hold circuit and the main output were plotted. These output waveforms come from having an input signal of amplitude 1.2 Vpp at a frequency of 150 Hz.

As shown in Figure 5.9 (a), there exist an offset of about 0.8 V at phase 1 at the output of op amp 1 in the switched capacitor filter, which is unexpected and would limit the dynamic range and input level. The entire output waveform at phase 1 has been shifted below half V_{DD} .

In Figure 5.9(b), the output at phase 2 of op amp 2 of the switched capacitor filter shows a distorted waveform at the lower end of the signal as it approaches a value of 0.4 V. This would not have happened if the offset of 0.8 V is not present. The differences between the measured result and the simulation result in frequency response are due to a couple of factors such as skewing of clock signal and the offset problem.

Figure 5-9 Output at (a) Op amp 1 and (b) Op amp 2 of Switched Capacitor Bass Filter Circuit

In Figure 5.10, the output waveforms at sampled and hold circuit and the output of the microchip are given. The high frequency components can be seen at the output of the sample-and-hold circuit while these components are removed at the output of the microchip after the filtering effect of smoothing filter.

Figure 5-10 Output at Sample and Hold circuit and Smoothing Filter

As a summary for this section, the measurement results for the microchip fabricated have been done. There are some layout problems that cause some inconsistency of the measurement result to the simulation result such as the biasing of the SP resistor island and the effect of parasitic capacitance. For the measurement of the bass equalizer, it was found that the center frequency could be achieved in the microchip. However, there are several problems that exist and are listed below:

1. Offset problem
2. Gain level deviation from simulation result especially at low frequency for instance from DC to center frequency.

The analysis of the above problem can be found in Section 5.5.

5.5 Offset Problem

One of the problems faced by the fabricated test chip is the offset problem noted in Figure 5.9. There are two factors, which caused the problem, which are the lack of initializing state for the integrating capacitor and the intrinsic offset problem due to the op amp in the switched capacitor filter design.

Figure 5-11 Proposed bass equalizer that is implemented in this project

In the filter circuit on the test chip as shown in Figure 5.11, the integrating capacitors C_{A2} , C_{C2} and the feedforward capacitor C_6 were not initialized during startup time; the initial states of these capacitors are uncertain, and hence cause the dc voltage level change abruptly.

Secondly, the offset voltage from the op amp has also been amplified by the filter design. The op amp offset voltage effect for the non-inverting integrator has been derived in Eq[3-6] in Chapter 3. And the simulation result for the bass equalizer with the offset signal at the non-inverting input of op amp 1 and op amp 2, the DC gain is 27 dB and -9.2 dB respectively. The offset voltage at op amp 1 is amplified to the output of the filter.

A gain offset compensation technique is proposed at the end of this thesis as a future suggestion to resolve the offset problem. The proposed technique can be used to cancel the offset effect of the op amp and the finite gain effect at the op amp.

5.6 Frequency Response Deviation

As observed from Figure 5.8 and Figure 5.9, the whole chip evaluation showed the gain deviation for the frequency response. The gain response at the center frequency and at lower frequency differed from the simulation result. At setting of 12 dB gain and 150 Hz center frequency, the gain deviation is -3.5 dB from the ideal response. And at 20 Hz, the measured result of 3.5 dB is higher than that of 1.8 dB obtained from simulation.

From further simulation and troubleshooting, the root cause of the problem was identified. Two main factors have contributed to the drift of the frequency response. They are due to clock skewing and finite gain limitation of the op amp.

In the normal simulation, the clock-skewing problem cannot be observed. Hence to observe the effect due to the clock-skewing, a parasitic capacitor is added at the non-overlapping clock generator to introduce skewing clock phase. It causes the rising time and the falling time of the clock reduced, and hence results in overlapping of clock phases ϕ_1 and ϕ_2 which is undesired. Simulation was carried out with these skewed clock phases and the result was plotted in Figure 5.12. The two results are similar for the whole frequency range.

Figure 5-12 Frequency response for the measured result and the simulation result with a skewed clock phase

The finite gain problem for an op amp may affect the response curve. Even though the design of the op amp is with a gain of higher than 75 dB, the output of the op amp may be lower due to process tolerance. If the frequency response is considered at lower gain, the drift in the filter response can be observed. The result can be found in Figure 6.2 at the end of Chapter 6 by comparing with the frequency response with gain offset compensation technique.

CHAPTER 6 CONCLUSION AND RECOMMENDATIONS FOR FUTURE WORKS

6.1 Conclusion

In this thesis, a capacitance spread reduction switched capacitor technique for high sampling frequency to center frequency ratio has been proposed. The proposed technique was implemented in a bass equalizer with center frequency of 50 Hz and 150 Hz for audio application. This bass equalizer was fabricated with a 0.8 mm BiCMOS process.

The measurement results are documented in CHAPTER 5. The design target to reduce the capacitance spread for a switched capacitor bass equalizer with high sampling clock frequency has been achieved with the circuit proposed in Chapter 3. However, measurement also showed faulty results as compared to the simulation result at the gain level. The gain level is higher at center frequency and it deviated more at frequency lower than center frequency.

In this chapter, the reasons for the problems will be explained. Recommendations to improve circuit performance will also be provided. The main recommendation, which will be discussed in Section 6.2.1, made to resolve the problem faced is to implement gain offset compensation (GOC) to the switched capacitor filter. By doing this, the problem due to the non-ideal effect of op amp could be minimized as will be shown in

the following section. While in Section 6.2.2 the recommendation to eliminate the clock skewing effect to the performance will be given.

6.2 Recommendations for Future Works

6.2.1 Correlated double sampling gain offset compensation (GOC) technique

In this section, a correlated double sampling gain offset compensation technique is proposed to improve the performance and to resolve the existing problem as explained in this chapter.

As there are some problems exist in the microchip fabricated, and the problems have been discussed in Chapter 5. The problems are mainly caused by imperfection of the op amp such as finite gain and offset voltage. Gain offset compensation technique using correlated double sampling is proposed to countermeasure for the problems. It should be able to minimize the effect of the offset voltage as well as the effect of finite gain of the op amp to the output. The correlated double sampling (CDS) technique introduced in Section 2.2 is employed here. As mentioned before, the CDS technique first samples and holds the undesired signals, dc offset or noise, and the sampled signal is subtracted from the output containing the undesired signals. The part of circuit in the dashed box in Figure 6-1 acts as the CDS gain and offset compensated (GOC) circuit. The principle of operation is explained next.

Referring to Figure 6-1, by applying a multiphase clock scheme, the desired output of the non-inverting integrator will appear during phase ϕ_2 . During phase ϕ_{2a} , the bottom

plate of capacitor C_m is connected to ground, and the top plate of the capacitor is connected to the inverting input of the op amp, which would be virtual ground for an ideal case. In reality, the node would not be ground potential due to the effect of DC offset and the finite gain of the op amp. Hence, C_m would be charged to V_{off} (generated by DC offset of the op amp and finite gain error).

Figure 6-1 Proposed integrator with correlated double sampling gain offset compensation

At phase ϕ_{2b} , the bottom plate of C_m is switched to node A while the other terminal of the capacitor is connected to the inverting input of the op amp, there is no net charge flow (in or out) from the capacitor C_m . The voltage across the capacitor C_m would remain at V_{off} that is sampled at ϕ_{2a} . Hence the voltage at node A is equal to zero due to the cancellation of the offset voltage. Similarly, at phase ϕ_1 , voltage at node A can be assumed to be ground. The voltage at node A is derived as:

At phase ϕ_{2a} , $t = (n-1) T$,

$$V_{C_m}[(n-1)T] = V_{off}[(n-1)T] \quad \text{Eq[6-1]}$$

At phase ϕ_{2b} , $t = (n-1/2) T$,

$$V_{Cm}[(n-1/2)T] = V_{off}[(n-1)T] \quad \text{Eq[6-2]}$$

and $V_A[(n-1/2)T] = V_{off}[(n-1/2)T] - V_{off}[(n-1)T] \quad \text{Eq[6-3]}$

At phase ϕ_1 , $t = nT$,

$$V_{Cm}(nT) = V_{off}[(n-1)T] \quad \text{Eq[6-4]}$$

and $V_A(nT) = V_{off}(nT) - V_{off}[(n-1)T] \quad \text{Eq[6-5]}$

From Eq[6-3] and Eq[6-5], it can be seen that the voltage at node A is always equal to the difference between the offset voltage at inverting input of the op amp at the instance and that at phase ϕ_{2a} . For low frequency noise and DC offset at inverting input, these two equations can be estimated as zero.

Figure 6-2 Simulation result comparing the effect of GOC technique

Due to the GOC circuit, the node A at the bottom plate of C_m always sees a drop of V_{off} from inverting input of op amp, and so V_{off} could be cancelled at first order. By employing this method, the DC offset, which is considered as time-independent can be cancelled. Similarly, for low frequency noise (flicker noise), it is assumed the

change in noise is small and hence it can also be cancelled to certain extent. The simulation result comparing the result of op amp gain of 100 with and without the GOC circuit is depicted in Figure 6.2. It can be seen that, at low op amp gain, the frequency response deviated away from the ideal response at low frequency without employing the GOC technique. With the implementation of GOC technique, the gain response obtained can be made as close to the ideal frequency response. Hence, the GOC technique is necessary to be implemented in the proposed switched capacitor filter in this project to prevent the problem caused by op amp's imperfections such as offset and finite gain of the op amp.

6.2.2 Clock Skew Effect Reduction

As discussed in Section 5.6, the other factor causing the frequency response deviation is the clock skewing which result in overlapping of clocks. The method recommended to eliminate the effect of clock overlapping is to increase the designed non-overlapping time for the clock generator.

The non-overlapping clock generator circuit has been shown in Figure 3-21. The non-overlapping time is determined by the delay of the number of gates in the circuit. For the BiCMOS process adopted in this project, the delay time for each gate is about 10ps. And hence, the overall non-overlapping time for the clock generator in Figure 3-21 is approximately 40ps.

To prevent the clocks undesirably overlap, it is recommended to increase the number of buffer used in the clock generator. In this case, a total of 150ps non-overlapping

time is used in simulation with consideration of the clock skewing. The simulation result with increase non-overlapping time and the designed response is given in Figure 6-3. With increase of the non-overlapping time, the result is less affected by the clock skew effect and more closely matched to the design value.

Figure 6-3 Simulation result versus designed response

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APPENDIX A EDA Tools Used

The EDA tools are referring to the computer aided tools using for the IC design. These have included the schematic entry, simulation, layout and layout verification software. In this project, Mentor Graphics series EDA tools are the main simulation tools used. Analog and mixed signal ICs design tools are part of the products of Mentor Graphics.

The following is a list of the EDA tools used in this project:

1. Mentor Graphics:

(a) Design Architect

Software used in schematic entry and generating netlist for simulation and layout verification.

(b) Accusim

Software used for analog and mixed signal simulation. As switched capacitor filter is a discrete-time circuit, its simulation had to be done in transient mode instead of AC simulation.

(c) IC Station

Software used for IC layout. The layout was done with this software and following the provided layout rule for the process.

2. Switcap:

Switcap is software, which is developed by Columbia University, for general simulation of switched capacitor circuits. It provides ideal modeling simulation for switched capacitor filter allowing multiple clock phases simulation. It verifies the functionality for the switched capacitor

circuit proposed in this project in faster way than using the transient simulation in Accusim.

3. Dracula (Cadence):

Cadence is one of the suppliers for the EDA tools in IC design market similar to Mentor Graphics. The technology file for layout verification provided by the foundry of diffusion is in the format of Dracula, which is one of the layout verification tools provided by Cadence. Dracula is used as the layout verification tool in this project.

APPENDIX B Simulation Files for SWITCAP

As switched capacitor filter is a sampling data system, the simulation cannot be done with small signal simulation using conventional simulation tools for instance pspice, hspice and eldo. It can only be simulated in transient mode using the simulation tools abovementioned which is very tedious in this case and not suitable when only some changes were done. SWITCAP, which is developed by Columbia University is a simulation tool specially developed for switched capacitor network simulation. With the ideal op amps and switches modeled in the software, it provides rapid result to show the functionality of the switched capacitor network. However, the final result has to be verified through transistor level simulation in conventional simulator.

SWITCAP uses text based netlist file as the input file defining the connection of the circuit and the phases of the switches. It is possible to run for a multiple clock phases which is needed in this project. The input files used in this project are given below.

SWITCAP simulations file for proposed integrator in Figure 3.6

*Note: In the SWITCAP simulation files; clk1, clk2, clk3 and clk4 represent clock phase 1a, 1b, 2a and 2b respectively.

options; grid; number; width132; report; chkcclk; end;

Title: SC Integrator

```

timing;
period 2.5e-6;
clock clk1 1(0 1/4);
clock clk2 1(1/4 2/4);
clock clk3 1(2/4 3/4);
clock clk4 1(3/4 1);
end;
circuit;
CB (0 1) 1;
C1 (2 3) 1;
CA2 (4 5) 10.515;
CA1 (6 5) 1;
CA2 (7 2) 10.515;
A0500 (5 0 0 8) 10000;
S0105 (1 5) clk1 clk2;
S0801 (8 1) clk3;
S2 (3 0) clk1 clk2;
S3 (2 0) clk1 clk2;
S1 (3 9) clk3 clk4;
S4 (5 2) clk3 clk4;
S0804 (8 4) clk1 clk2;
S0600 (6 0) clk1 clk2;
S0708 (7 8) clk3 clk4;
S0706 (7 6) clk4;
S0700 (7 0) clk1 clk2;
V1 (9 0);
analyze sss;
infreq 1 20e3 log 100;
set v1 ac 1.0 0;
sample output hold 1 3/8+;
plot vdb(8) number ;
end;

```

SWITCAP simulations file for proposed switched capacitor equalizer in Figure 3.11.

*Note: In the switcap simulation files; clk1, clk2, clk3 and clk4 represent clock phase 1_a , 1_b , 2_a and 2_b respectively.

options; grid; number; width132; report; chkcclk; end;

Title: SC Bass Equalizer

```

timing;
period 2.5e-6;
clock clk1 1(0 1/4);
clock clk2 1(1/4 2/4);
clock clk3 1(2/4 3/4);
clock clk4 1(3/4 1);

```

```

end;

C3 (2 3) 10.515
C2 (4 5) 4
CB (7 6) 1
CD (0 8) 1
C1 (9 5) 1
C4 (4 10) 1
CA (11 12) 10.515
CC (13 14) 10.515
CC2 (15 14) 1
CA2 (16 9) 1
CA1 (17 9) 10.515
C6 (18 4) 1
CC1 (19 4) 10.515
C5 (18 9) 1
A1200 (12 0 0 20) 10000
A1400 (14 0 0 21) 10000
S1402 (14 2) clk1 clk2
SOUT (21 1) clk1
S15 (7 0) clk1
S16 (6 0) clk3 clk4
S14 (7 12) clk3 clk4
S17 (20 6) clk1
S18 (8 14) clk1 clk2
S19 (21 8) clk3
S2 (5 0) clk3 clk4
S3 (9 0) clk3 clk4
S6 (10 0) clk1 clk2
S7 (4 0) clk1 clk2
S1 (5 3) clk1 clk2
S4 (12 9) clk1 clk2
S5 (10 20) clk3 clk4
S8 (14 4) clk3 clk4
S13 (20 11) clk3 clk4
S24 (21 13) clk1 clk2
S20 (15 0) clk1 clk2
S9 (16 12) clk3 clk4
S23 (19 21) clk3 clk4
S10 (17 16) clk2
S11 (17 20) clk1 clk2
S12 (17 0) clk3 clk4
S21 (19 15) clk4
S22 (19 0) clk1 clk2
S25 (18 21) clk1 clk2
S26 (0 18) clk3 clk4
Vin (3 0)

analyze sss;
infreq 1 20e3 log 100;
set vin ac 1.0 0;
sample output hold 1 3/8+;
plot vdb(21) number ;
end;

```

SWITCAP simulations file for switched capacitor integrator with GOC in Figure 6.3.

*Note: In the switcap simulation files; clk1, clk2, clk3 and clk4 represent clock phase

I_a , I_b , 2_a and 2_b respectively.

options; grid; number; width132; report; chkcclk; end;

Title: Lossy Integrator small signal simulation;

```

timing;
period 2.5e-6;
clock clk1 1(0 1/4);
clock clk2 1(1/4 2/4);
clock clk3 1(2/4 3/4);
clock clk4 1(3/4 1);
end;

circuit;
CB (0 1) 1;
C1 (2 3) 1;
CA2 (4 5) 10.515;
CA1 (6 5) 1;
CA2 (7 2) 10.515;
A0500 (5 0 0 8) 100;
S0105 (1 5) clk1 clk2;
S0801 (8 1) clk3;
S0300 (3 0) clk1 clk2;
S0200 (2 0) clk1 clk2;
S0309 (3 9) clk3 clk4;
S0502 (5 2) clk3 clk4;
S0804 (8 4) clk1 clk2;
S0600 (6 0) clk1 clk2;
S0708 (7 8) clk3 clk4;
S0706 (7 6) clk4;
S0700 (7 0) clk1 clk2;
S0810 (8 10) clk3;
S0811 (8 11) clk1, clk2, clk4;
S1100 (11 0) clk3;
CM (10 11) 1;
V1 (9 0);
end;

analyze sss;
infreq 1 1e4 log 1000;
set v1 ac 1.0 0;
plot vdb(8) number vp(8) number;
end;

```

APPENDIX C Accusim Userware for Switched Capacitor

Simulation

As mentioned before, the result of the switched capacitor filter designed has to be verified with conventional simulator such as Eldo in Accusim after checking for the functionality. In switched capacitor simulation in transistor level is needed to see the non-ideal effect of op amp and switches, which have been mentioned in Chapter 3.

As a high frequency sampling clock is used, and the designed input signal is much lower comparing to the sampling clock, for instance in this project a sampling frequency of 400 kHz with the center frequency of 50 and 150 Hz. To obtain a reliable result, the maximum time step in the transient simulation mode has to be much smaller to the sampling period said 100. In this case the maximum time step is 25 ns and it is needed for the output to be simulated for few cycles to reach its stability. This makes the simulation of switched capacitor filter even more time consumed, the case for running out of database space is a common problem faced with a lengthy simulation. In order to increase the efficiency of the simulation and to prevent the error due to the database space, an userware was written by the author to provide simulation obtaining the result in transient mode with sweeping signal frequency as in the AC mode and periodically reset simulation database. The flowchart for the program is given in **Figure C. 1**:

The userware first prompt the user for setup data such as temperature, Vcc and tolerance simulation option. After setup the simulation data, the program starts the simulation.

As the system needs time to reach stable state before reliable result can be taken, it is always required more than few periods of the input frequency before the result to be obtained. However, the number of periods before the system becomes stable is hard to determined. In the userware developed, it will setup the simulation to be done in one period of the input frequency and detect if the result has became stable by comparing the result at starting time and ending time. The simulation will continue until the result becomes stable and hence the result will be taken for the last cycle, which is

reliable. The simulation will be repeated for different setup such as different temperature, Vcc or simulation model as requested by users. The following is the source code for the userware written.

File 1 of the userware written for simulation.

```
extern results,data,model,host,resultac;
function sw_form(), INVISIBLE
{
    data=$create_vector(30);
    data[25]=$create_vector(2);

    local ggt_note0 = $form_display_only($form_gadget_value($form_display_text_gadget(" AC/Transient Sweep
        Tolerance Simulation Setting", "helvetica-bold:20","wheat")));

    local ggt_end = $form_display_only($form_gadget_value($form_display_text_gadget(" Done by Wong Sang
        Chin", "helvetica-bold:4","wheat")));

    /// Column 1

    local ggt_scf = $form_action($form_gadget_value($form_click_button_gadget($form_item("SCF",
        "scf_sw()", "helvetica-bold:12", "Black"), @false, "Wheat")), 75);

    local ggt_measurement = $form_left_justified_column(@false, ggt_scf);

    local ggt_ok = $form_action($form_gadget_value($form_click_button_gadget($form_item("OK",
        "Sexecute()", "helvetica-bold:12", "Black"), @true, "Wheat")), 75);

    local ggt_reset = $form_action($form_gadget_value($form_click_button_gadget($form_item("Reset",
        "Sreset()", "helvetica-bold:12", "Black"), @false, "Wheat")), 75);

    local ggt_cancel = $form_action($form_gadget_value($form_click_button_gadget($form_item("Cancel",
        "Sforget()", "helvetica-bold:12", "Black"), @false, "Wheat")), 75);

    local ggt_proceed = $form_row(@false, ggt_ok, ggt_reset, ggt_cancel);

    /// Column 2

    local ggt_model_note = $form_display_only($form_gadget_value($form_display_text_gadget("Select
        Tolerance Model ( R PNP NPN )", "helvetica-bold:12","wheat")));

    local ggt_model1 =
        $form_named_argument_gadget(@model,
            $form_check_boxes_gadget( @column, "",
                $form_default_title_font, "Wheat",
                $form_item("CCC", "ccc"),
                $form_item("LLL", "lll"),
                $form_item("LLH", "llh"),
                $form_item("LHL", "lhl"),
                $form_item("LHH", "lhh"),
                $form_item("HLL", "hll"),
                $form_item("HLH", "hlh"),
                $form_item("HHL", "hhl"),
                $form_item("HHH", "hhh")
            ) // end of check boxes gadget
        ); // end of site definition

    local ggt_model1a=$form_row(@false, ggt_model1);

    local ggt_model2=$form_column(@false,ggt_model_note, ggt_model1a);

    /// Vcc Tolerance Setting

    local ggt_vcc_option =
        $form_named_argument_gadget(@vcc_option,
            $form_check_boxes_gadget( @column, "",
                $form_default_title_font, "Wheat",
```



```

        $form_item("VCC Tolerance", "vcc")
    ) // end of check boxes gadget
); // end of site definition

local ggt_vcc_low = $form_variable_gadget(@vcc_low,$form_string_entry_box_gadget("Minimum Vcc :
", "helvetica:14", "helvetica-bold:12", "Wheat"));

local ggt_vcc_typ = $form_variable_gadget(@vcc_typ,$form_string_entry_box_gadget("Typical Vcc :
", "helvetica:14", "helvetica-bold:12", "Wheat"));

local ggt_vcc_hi = $form_variable_gadget(@vcc_hi,$form_string_entry_box_gadget("Maximum Vcc:
", "helvetica:14", "helvetica-bold:12", "Wheat"));

local ggt_vcc_net = $form_variable_gadget(@vccnet,$form_string_entry_box_gadget("Vcc Net :
", "helvetica:14", "helvetica-bold:12", "Wheat"));

local ggt_column_vcc = $form_left_justified_column(@false, ggt_vcc_option, ggt_vcc_low,ggt_vcc_typ,
ggt_vcc_hi, ggt_vcc_net);

//// Temperature Tolerance Option
local ggt_temp_option =
    $form_named_argument_gadget(@temp_option,
        $form_check_boxes_gadget( @column, "",
            $form_default_title_font, "Wheat",
            $form_item("Temperature Tolerance", "temp")
        ) // end of check boxes gadget
    ); // end of site definition

local ggt_temp_low = $form_variable_gadget(@temp_low,$form_string_entry_box_gadget("Minimum
Temperature : ", "helvetica:14", "helvetica-bold:12", "Wheat"));

local ggt_temp_typ = $form_variable_gadget(@temp_typ,$form_string_entry_box_gadget("Typical
Temperature : ", "helvetica:14", "helvetica-bold:12", "Wheat"));

local ggt_temp_hi = $form_variable_gadget(@temp_hi,$form_string_entry_box_gadget("Maximum Temperature:
", "helvetica:14", "helvetica-bold:12", "Wheat"));

local ggt_column_temp = $form_left_justified_column(@false, ggt_temp_option, ggt_temp_low,ggt_temp_typ,
ggt_temp_hi);

local ggt_row_vcctemp=$form_row(@true, ggt_column_vcc, ggt_column_temp);

local ggt_sp_tol = $form_variable_gadget(@sp_tol,$form_string_entry_box_gadget("SP Resistor Absolute
Tolerance: ", "helvetica:12", "helvetica-bold:12", "Wheat"));

local ggt_ps_tol = $form_variable_gadget(@ps_tol,$form_string_entry_box_gadget("PS/PW Resistor Absolute
Tolerance: ", "helvetica:12", "helvetica-bold:12", "Wheat"));

local ggt_init_res = $form_column(@true, ggt_sp_tol, ggt_ps_tol);

local ggt_column_res = $form_column(@true, ggt_row_vcctemp, ggt_init_res);

local ggt_row_simu = $form_row(@true, ggt_measurement, ggt_model2, ggt_column_res);

local ggt_60= $form_navigator_entry(@init, "Initialize file : ", "$navigate_for_file",400,@row);

local ggt_70= $form_navigator_entry(@filepath, "Directory for the results :
", "$navigate_for_file",500,@row);

local ggt_column_menu1 = $form_column(@true, ggt_note0,ggt_row_simu,ggt_60,ggt_70,
ggt_proceed);

local ggt_column_menu = $form_right_justified_column(@false,
ggt_column_menu1,$form_right_justified_column(@false, ggt_end));

Screate_form("kernel", @sw, @true, $form_default_color, ggt_column_menu);
}

function sw(
    model                : vector{ default=["ccc"]},
    sp_tol                : real{ default="0.2"},
    ps_tol                : real{ default="0.1"},
    vcc_option            : vector{ default=[]},
    vcc_low               : real{ default="5.5"},
    vcc_typ               : real{ default="9"},
    vcc_hi                : real{ default="10.5"},
    vccnet                : string{ default=$last},
    temp_option           : vector{ default=[]},

```

```

temp_low      : real { default="-30"},
temp_typ      : real { default="27"},
temp_hi       : real { default="90"},
init          : string,
filepath      : string { default = $strcat($get_component_name(),"/results")}
)
{

  $set_multiple_variables(["sp"], ["1"], [@string], "/");
  $set_multiple_variables(["pd"], ["1"], [@string], "/");

  $load_userware("/users/scwong/macro_new/sw_run", "kernel", @ample);
  $load_userware("/users/scwong/macro_new/sw_plot", "kernel", @ample); //load macro
  $load_userware("/users/scwong/macro/thd_ac", "kernel", @ample); //load macro

  local i,j,k,x,y,z;

  data[1]=$create_vector(length(model));
  data[1]=model;
  data[2]=length(data[1]);
  data[3]=0;
  data[7]=0;
  data[10]=0;

  host = hostname;

  if(data[4]=="vcc" || data[8]=="vcc")
    data[11]=[];
  if(data[4]=="temp" || data[8]=="temp")
    data[15]=[];

  data[11]=vcc_option;
  data[12]=vccnet;

  if( $vector_search("vcc",data[11],0) != UNDEFINED)
  {
    data[13]=$create_vector(3);
    data[13][0]=vcc_low;
    data[13][1]=vcc_typ;
    data[13][2]=vcc_hi;
  }
  else
  {
    data[13]=$create_vector(1);
    data[13][0]=vcc_typ;
  }
  data[14]=0;

  data[15]=temp_option;

  if( $vector_search("temp",data[15],0) != UNDEFINED)
  {
    data[16]=$create_vector(3);
    data[16][0]=temp_low;
    data[16][1]=temp_typ;
    data[16][2]=temp_hi;
  }
  else
  {
    data[16]=$create_vector(1);
    data[16][0]=temp_typ;
  }

  data[17]=0;
  data[22]=$create_vector(6);
  data[22][0]=filepath;
  data[23]=$create_vector(2);
  data[23][0]=sp_tol;
  data[23][1]=ps_tol;
  data[25][0]=title;
  data[25][1]=init;

  if(data[4]==data[8])
    data[8]="no";

  if(data[8]=="no")
    data[9]="";

  if(data[4]=="vcc" || data[4]=="temp")
    data[5][3]="";

```

```

        if(data[8]=="vcc" || data[8]=="temp" )
            data[24]="";

        if(data[8]=="no" )
            data[24]="";

        results=Screate_vector(data[2]);
        for(i=0;i<data[2];i=i+1)
        {
            switch(data[0])
            {
                case "scf1":
                    results[i]=Screate_vector(1+5*length(data[9]));
                    for(j=0;j<length(results[i]);j=j+1)
                        results[i][j]=Screate_vector(length(data[6]));
                    break;
            }
        }

        if(data[4]=="freq")
            for(j=0;j<length(data[6]);j=j+1)
                data[6][j]=Sround_prec(data[6][j],2);

        for(i=0;i<data[2];i=i+1)
        {
            results[i][0]=data[6];
        }

        if(data[4]!="dcv" || data[4]!="dci")
            if(data[4]!="res")
                data[5][3]="";
        if(data[8]!="dcv" || data[8]!="dci")
            if(data[8]!="res")
                data[24]="";

        sw_run();
    }

function scf_sw_form(), INVISIBLE
{
    local ggt_note = $form_display_only($form_gadget_value($form_display_text_gadget("SCF Tolerance
    Simulation Setup", "helvetica-bold:20", "wheat")));

    local ggt_innet = $form_variable_gadget(@innet,$form_string_entry_box_gadget("Input Net Name :
    ", "helvetica:14", "helvetica-bold:12", "Wheat"),250);

    local ggt_outnet = $form_variable_gadget(@outnet,$form_string_entry_box_gadget("Output Net Name :
    ", "helvetica:14", "helvetica-bold:12", "Wheat"),250);

    local ggt_infreq = $form_variable_gadget(@infreq,$form_string_entry_box_gadget("Input Frequency :
    ", "helvetica:14", "helvetica-bold:12", "Wheat"),250);

    local ggt_inmag = $form_variable_gadget(@inmag,$form_string_entry_box_gadget("Input Magnitude :
    ", "helvetica:14", "helvetica-bold:12", "Wheat"),250);

    local ggt_indc = $form_variable_gadget(@indc,$form_string_entry_box_gadget("Input DC :
    ", "helvetica:14", "helvetica-bold:12", "Wheat"),250);

    local row_outnets=$form_column(@false, ggt_innet,ggt_outnet, ggt_infreq, ggt_inmag, ggt_indc);

    local ggt_primary =
        $form_named_argument_gadget(@primary_sw,
            $form_choice_buttons_gadget( @column, "Primary Sweep",
                $form_default_title_font, "Wheat",
                $form_item("VCC", "vcc"),
                $form_item("TEMPERATURE", "temp"),
                $form_item("VIN", "vin"),
                $form_item("FREQ", "freq"),
                $form_item("DC(V)", "dcv"),
                $form_item("DC(I)", "dci"),
                $form_item("RESISTOR", "res")
            ) // end of check boxes gadget
        ); // end of site definition

    local ggt_pvalues_note0 = $form_display_only($form_gadget_value($form_display_text_gadget("Primary
    Parameter( NET/RES) : ", "helvetica-bold:12", "Wheat")));

    local ggt_pri = $form_variable_gadget(@primary,$form_string_entry_box_gadget("
    ", "helvetica:14", "helvetica-bold:12", "Wheat"),200);

```

```

local ggt_pvalues_note = $form_display_only($form_gadget_value($form_display_text_gadget("Primary Sweep
Setting: ", "helvetica-bold:12", "Wheat")));

local ggt_start = $form_variable_gadget(@pstart,$form_string_entry_box_gadget("Start Value :
", "helvetica:14", "helvetica-bold:12", "Wheat"),200);

local ggt_end = $form_variable_gadget(@pend,$form_string_entry_box_gadget("End Valu :
", "helvetica:14", "helvetica-bold:12", "Wheat"),200);

local ggt_points = $form_variable_gadget(@ppts,$form_string_entry_box_gadget(" Step :
", "helvetica:14", "helvetica-bold:12", "Wheat"),200);

local row_pvalues=$form_column(@false, ggt_pvalues_note0, ggt_pri, ggt_pvalues_note,
ggt_start,ggt_end,ggt_points);

local ggt_secondary =
    $form_named_argument_gadget(@sec_sw,
        $form_choice_buttons_gadget( @column, "Secondary Sweep",
            $form_default_title_font, "Wheat",
            $form_item("VCC", "vcc"),
            $form_item("TEMPERATURE", "temp"),
            $form_item("VIN", "vin"),
            $form_item("FREQ", "freq"),
            $form_item("DC(V)", "dcv"),
            $form_item("DC(I)", "dci"),
            $form_item("RESISTOR", "res"),
            $form_item("No Secondary Sweep", "no")
        ) // end of check boxes gadget
    ); // end of site definition

local ggt_values_note0 = $form_display_only($form_gadget_value($form_display_text_gadget("Secondary
Parameter( NET/RES) : ", "helvetica-bold:12", "Wheat")));

local ggt_sec = $form_variable_gadget(@secondary,$form_string_entry_box_gadget("
", "helvetica:14", "helvetica-bold:12", "Wheat"),200);

local ggt_values_note = $form_display_only($form_gadget_value($form_display_text_gadget("Secondary
Values List: ", "helvetica-bold:12", "Wheat")));

local ggt_values = $form_variable_gadget(@sec_values,$form_string_entry_box_gadget("
", "helvetica:12", "helvetica-bold:12", "Wheat"));

local row_value = $form_repeat(@column, ggt_values);

local row_values=$form_column(@false, ggt_values_note0, ggt_sec, ggt_values_note, row_value);

local ggt_setup = $form_row(@true, row_outnets, ggt_primary, row_pvalues, ggt_secondary, row_values);

local ggt_ok = $form_action($form_gadget_value($form_click_button_gadget($form_item("OK",
"$execute()", "helvetica-bold:12", "Black"), @true, "Wheat")), 75);

local ggt_reset = $form_action($form_gadget_value($form_click_button_gadget($form_item("Reset",
"$reset()", "helvetica-bold:12", "Black"), @false, "Wheat")), 75);

local ggt_cancel = $form_action($form_gadget_value($form_click_button_gadget($form_item("Cancel",
"$forget()", "helvetica-bold:12", "Black"), @false, "Wheat")), 75);

local ggt_proceed = $form_row(@false, ggt_ok, ggt_reset, ggt_cancel);

local ggt_column_menu = $form_column(@true, ggt_note,ggt_setup, ggt_proceed );

Screate_form("kernel", @scf_sw, @true, $form_default_color, ggt_column_menu);

}

function scf_sw(
    inet          : string { default=$last},
    outnet        : string { default=$last},
    infreq        : real { default="1000"},
    inmag         : real { default="1"},
    indc          : real { default="2.5"},
    primary       : string,
    primary_sw    : string { default="vcc"},
    pstart        : real { default=$last},
    pend         : real { default=$last},
    ppts          : real { default=$last},
    secondary     : string,
    sec_sw        : string { default="no"},
    sec_values    : vector

```

```

    )
    {

        data[0]="scf";
        data[4]=primary_sw;
        data[5]=$create_vector(4);
        data[5][0]=pstart;
        data[5][1]=pend;
        data[5][2]=ppts;
        data[5][3]=primary;

        if(sec_sw==primary_sw)
            data[8]="no";
        else data[8]=sec_sw;
        data[9]=sec_values;
        data[18]=$create_vector(6);
        data[18][0]=innet;
        data[18][1]=infreq;
        data[18][2]=inmag;
        data[18][5]=indc;
        data[20]=outnet;
        data[24]=secondary;

        local inpri, no_of_pri, i,j,k;

        if(data[4]!="vin" && data[4]!="freq")
        {
            inpri=$create_vector(ceil((data[5][1]-data[5][0])/data[5][2])+1);
            no_of_pri=ceil((data[5][1]-data[5][0])/data[5][2])+1;
            k=0;
            for (j=0;j<no_of_pri-1;j=j+1)
            {
                inpri[k]=data[5][0]+j*data[5][2];
                k=k+1;
            }
            if (j< (data[5][1]-data[5][0])/data[5][2]+1)
                inpri[k]=data[5][1];
        }

        else
        {
            inpri = $create_vector(ceil(data[5][2]*log10(data[5][1]/data[5][0])+1));
            no_of_pri=ceil(data[5][2]*log10(data[5][1]/data[5][0])+1);
            k=0;
            for (j=0;j<=(log10(data[5][1]/data[5][0])-1);j=j+1)
            {
                for (i=0; i<data[5][2]; i=i+1)
                {
                    inpri[k]=data[5][0]*pow(10,j)*pow(10,i/data[5][2]);
                    k=k+1;
                }
            }
            if (j== (log10(data[5][1]/data[5][0])))
                inpri[k]=data[5][1];
            else
            {
                for (i=0;data[5][1]>data[5][0]*pow(10,j)*pow(10,i/data[5][2]);i=i+1)
                {
                    inpri[k] = data[5][0]*pow(10,j)*pow(10,i/data[5][2]);
                    k=k+1;
                }
                inpri[k]=data[5][1];
            }
        }

        data[6]=inpri;
    }

    function sw_run()
    {
        sw_vcc();
    }

    function sw_vcc()
    {
        local vcc_index;

        if(data[4]!="vcc" && data[8]!="vcc")

```



```

        for(vcc_index=0;vcc_index<length(data[13]);vcc_index=vcc_index+1)
        {
            data[14]=vcc_index;
            sw_temp();
        }
    else sw_temp();
}

function sw_temp()
{
    local temp_index;
    local i;

    if(data[4]!="temp" && data[8]!="temp")
        for(temp_index=0;temp_index<length(data[16]);temp_index=temp_index+1)
        {
            data[17]=temp_index;
            if(!$Sis_directory(data[22][0]))
                $Sadd_directory(data[22][0]);

            local date1=$date();
            local time1=$time();

            local file1= $Strcat(data[22][0],"/sw_",data[0],"_",data[4],"_",data[8]);

            if(!$Sis_directory(file1))
                $Sadd_directory(file1);

            local filepath1,filepath2;
            local stream_id1,stream_id2;

            if(data[4]!="vcc" && data[8]!="vcc")
                filepath1= $Strcat(file1,"/",date1[0],"_",$(date1[1], 2, ., @zero),"_",$(date1[2], 2, .,
                @zero),"_",$(time1[0], 2, ., @zero),"_",$(time1[1], 2, .,
                @zero),"_",data[13][data[14]]."V_",data[16][data[17]]."C",host);
            else
                filepath1= $Strcat(file1,"/",date1[0],"_",$(date1[1], 2, ., @zero),"_",$(date1[2], 2, .,
                @zero),"_",$(time1[0], 2, ., @zero),"_",$(time1[1], 2, .,
                @zero),"_",data[16][data[17]]."C",host);

            stream_id1 = $open_file($free_stream_id(),filepath1,@write);

            if(data[25][1]!="")
            {
                filepath2= $Strcat(filepath1,".ini");
                stream_id2 = $open_file($free_stream_id(),filepath2,@write);
                data[22][4]=filepath2;
                data[22][5]=stream_id2;
                $writes_file(data[22][5],$Strcat("dof",data[25][1]),".");
            }

            data[22][1]=filepath1;
            data[22][2]=stream_id1;

            $writes_file(data[22][2],"////////////////////////////////////");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2]," ( Start: ",data[5][0],"; Stop: ",data[5][1], " ;
            Step: ", data[5][2], " )\n");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2]," Secondary Mode :
            ",$format("%-50s",$super_string(data[8])));
            $writes_file(data[22][2]," ",data[24],"\n");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2],"////");
            $writes_file(data[22][2]," VCC Net :
            ",$format("%-50s",$super_string(data[12])),"\n");
            $writes_file(data[22][2]," Input Net: ",$format("%-50s",$super_string(data[18][0])),"\n");
            $writes_file(data[22][2]," Output Net: ",$format("%-50s",$super_string(data[20])),"\n");

            if(data[0]=="noise")
                for(i=0;i<length(data[21]);i=i+1)
                    $writes_file(data[22][2]," Measured Frequency ",i+1,"
                    : ",$format("%5s",$super_string(data[21][i])), "Hz\n");

```

```

$writes_file(data[22][2], "/// Start Simulation Time: ", date1[0], "-", $i(date1[1],
2, , @zero), "-", $i(date1[2], 2, , @zero), " ", $i(time1[0], 2, , @zero), ":", $i(time1[1], 2, ,
@zero), "\n");

if(data[4]=="vcc" && data[8]!="temp")
    $writes_file(data[22][2], "/// Vcc : Primary \n");
else if(data[8]=="vcc")
    $writes_file(data[22][2], "/// Vcc : Secondar \n");
else
    $writes_file(data[22][2], "///Vcc : ", data[13][data[14]], " V\n");
    $writes_file(data[22][2], "///Temperature: ", data[16][data[17]], " C\n");
if(data[25][1]!="")
    $writes_file(data[22][2], "///Initialize file: ", $format("%60s", data[25][1])
, "\n");

$writes_file(data[22][2], "/// Simulated at: ", $format("%-50s", host), "\n");
$writes_file(data[22][2], "//////////////////////////////////////\n");

sw_model();

local edate1=$date();
local etime1=$time();

$writes_file(data[22][2], "///", $supper_string(data[4]), " SWEEP SIMULATION\n");
$writes_file(data[22][2], "///", $format("%-50s", data[25][0]), "\n");
$writes_file(data[22][2], "///End Simulation Time: ", edate1[0], "-", $i(edate1[1], 2, , @zero), "-", $i(edate1[2], 2, ,
@zero), " ", $i(etime1[0], 2, , @zero), ":", $i(etime1[1], 2, , @zero), "\n");
$writes_file(data[22][2], "//////////////////////////////////////\n");

sw_plot(data, results);
}

else
{
if(!$Sis_directory(data[22][0]))
    $Sadd_directory(data[22][0]);

local date1=$date();
local time1=$time();

local file1 = $strcat(data[22][0], "/sw_", data[0], "_", data[4], "_", data[8]);

if(!$Sis_directory(file1))
    $Sadd_directory(file1);

local filepath1, filepath2;
local stream_id1, stream_id2;

if(data[4]!="vcc" && data[8]!="temp")
    filepath1 = $strcat(file1, "/", date1[0], "-", $i(date1[1], 2, , @zero), "-", $i(date1[2], 2, ,
@zero), " ", $i(time1[0], 2, , @zero), "-", $i(time1[1], 2, , @zero), "_", data[13][data[14]], "V", host);
else
    filepath1 = $strcat(file1, "/", date1[0], "-", $i(date1[1], 2, , @zero), "-", $i(date1[2], 2, ,
@zero), " ", $i(time1[0], 2, , @zero), "-", $i(time1[1], 2, , @zero), host);
stream_id1 = $open_file($free_stream_id(), filepath1, @write);

if(data[25][1]!="")
{
    filepath2 = $strcat(filepath1, ".ini");
    stream_id2 = $open_file($free_stream_id(), filepath2, @write);
    data[22][4]=filepath2;
    data[22][5]=stream_id2;
    $writes_file(data[22][5], $strcat("dof ", data[25][1]), ".");
}

data[22][1]=filepath1;
data[22][2]=stream_id1;

$writes_file(data[22][2], "//////////////////////////////////////\n");
$writes_file(data[22][2], "///", $supper_string(data[4]), " SWEEP SIMULATION \n");
$writes_file(data[22][2], "/// Title : ", $format("%-50s", data[25][0]), "\n");

$writes_file(data[22][2], "/// Simulation File Name: ", $format("%50s", $get_component_name()),
\n");

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$writes_file(data[22][2], "/// Primary Mode:", $format("%15s", $supper_string(data[4])));
$writes_file(data[22][2], " ", data[5][3], " ( Start: ", data[5][0], "; Stop: ", data[5][1], "; Step: ", data[5][2], " )\n");
$writes_file(data[22][2], "/// Secondary Mode:", $format("%-50s", $supper_string(data[8])));
$writes_file(data[22][2], " ", data[24], "\n");
$writes_file(data[22][2], "///VCC Net:", $format("%-50s", $supper_string(data[12])));
$writes_file(data[22][2], "///Input Net:", $format("%-50s", $supper_string(data[18][0])));
$writes_file(data[22][2], "///Output Net:", $format("%-50s", $supper_string(data[20])));

if(data[0]=="noise")
    for(i=0;i<length(data[21]);i=i+1)
        $writes_file(data[22][2], "///Measured Frequency ", i+1, ":",
            $format("%5s", $supper_string(data[21][i])), "Hz\n");

    $writes_file(data[22][2], "///Start Simulation Time:", date1[0], " ", $i(date1[1], 2, , , @zero), " ", $i(date1[2],
        2, , , @zero), " ", $i(time1[0], 2, , , @zero), ":", $i(time1[1], 2, , , @zero), "\n");

if(data[4]=="vcc") // && data[8]=="temp"
    $writes_file(data[22][2], "///Vcc : Primary \n");

else if(data[8]=="vcc")
    $writes_file(data[22][2], "///Vcc : Secondary \n");
else $writes_file(data[22][2], "/// Vcc: ", data[13][data[14]], " V \n");

$writes_file(data[22][2], "///Temperature: ", data[16][data[17]], " C \n");

if(data[25][1]!="")
    $writes_file(data[22][2], "///Initialize file:", $format("%-60s", data[25][1]), "\n");
$writes_file(data[22][2], "///Simulated at : ", $format("%-50s", host), "\n");
$writes_file(data[22][2], "////////////////////////////////////\n\n");

sw_model();

local edate1=$date();
local etime1=$time();

$writes_file(data[22][2], "\n\n\n////////////////////////////////////\n");
$writes_file(data[22][2], "///", $supper_string(data[4]), " SWEEP SIMULATION \n");
$writes_file(data[22][2], "/// ", $format("%-50s", data[25][0]), "\n");
$writes_file(data[22][2], "///End Simulation Time: ", edate1[0], " ", $i(edate1[1], 2, , , @zero), " ", $i(edate1[2],
    2, , , @zero), " ", $i(etime1[0], 2, , , @zero), ":", $i(etime1[1], 2, , , @zero), "\n");
$writes_file(data[22][2], "////////////////////////////////////\n\n");

sw_plot(data, results);
}

function sw_model()
{
    local mod_index;
    local i;

    for(mod_index=0;mod_index<length(data[1]);mod_index=mod_index+1)

        data[3]=mod_index;
        switch(data[1][data[3]])

            case "ccc": break;
            case "lll":
                $set_multiple_variables(["sp"], [1/(1-data[23][0])], [@number], "/");
                $set_multiple_variables(["pd"], [1/(1-data[23][1])], [@number], "/");
                break;
            case "llh":
                $set_multiple_variables(["sp"], [1/(1-data[23][0])], [@number], "/");
                $set_multiple_variables(["pd"], [1/(1-data[23][1])], [@number], "/");
                break;
            case "lhl":
                $set_multiple_variables(["sp"], [1/(1-data[23][0])], [@number], "/");
                $set_multiple_variables(["pd"], [1/(1-data[23][1])], [@number], "/");
                break;
            case "lhh":
                $set_multiple_variables(["sp"], [1/(1-data[23][0])], [@number], "/");
                $set_multiple_variables(["pd"], [1/(1-data[23][1])], [@number], "/");
                break;
            case "hll":
                $set_multiple_variables(["sp"], [1/(1+data[23][0])], [@number], "/");
                $set_multiple_variables(["pd"], [1/(1+data[23][1])], [@number], "/");
                break;
            case "hlh":
                $set_multiple_variables(["sp"], [1/(1+data[23][0])], [@number], "/");

```

```

        $set_multiple_variables(["pd"], [1/(1+data[23][1])], [@number], "/");
        break;
    case "hhl":
        $set_multiple_variables(["sp"], [1/(1+data[23][0])], [@number], "/");
        $set_multiple_variables(["pd"], [1/(1+data[23][1])], [@number], "/");
        break;
    case "hhh":
        $set_multiple_variables(["sp"], [1/(1+data[23][0])], [@number], "/");
        $set_multiple_variables(["pd"], [1/(1+data[23][1])], [@number], "/");
        break;
}

$writes_file(data[22][2], "\n\n////////////////////////////////\n");
$writes_file(data[22][2], "/// MODEL", $supper_string(data[1][data[3]]), "\n");
$writes_file(data[22][2], "////////////////////////////////\n");

sw_sec();

//////// Reset the resistor values if changed
}

$set_multiple_variables(["sp"], ["1"], [@number], "/");
$set_multiple_variables(["pd"], ["1"], [@number], "/");
}

function sw_sec()
{
    local i,j,k;
    for(i=0;i<length(data[9]);i=i+1)
    {
        data[10]=i;
        if(data[8]!="no")
        {
            $writes_file(data[22][2], "\n////////////////////////////////\n");
            $writes_file(data[22][2], "/// Secondary ( ", $supper_string(data[8]), " ) ", data[9][data[10]], " ",
                data[24], "\n");
            $writes_file(data[22][2], "////////////////////////////////\n\n");
        }

        $writes_file(data[22][2], " Start Time : ", $date()[0], "-
        ", $i($date()[1], 2, .., @zero), "-", $i($date()[2], 2, .., @zero), " ", $i($time()[0], 2, .., @zero), ":",
        $i($time()[1], 2, .., @zero), "\n");

        $writes_file(data[22][2], $format("%-14s", "Primary"));
        $writes_file(data[22][2], "\n");
    }

    if(data[0]!="noise")
    {
        if(data[4]!="freq" && data[8]!="freq")
            $writes_file(data[22][2], "\n", "Freq = ", data[18][1], " Hz\n");
        if(data[4]!="vin" && data[8]!="vin")
            $writes_file(data[22][2], "\n", "Magnitude = ", data[18][2], " Vrms\n");
        switch(data[4])
        {
            case "vin":
                $writes_file(data[22][2], $format("%5s%3s%-5s", "VIN(/ ", data[18][0], " )"));
                break;
            case "freq":
                $writes_file(data[22][2], $format("%5s%3s%-5s", "Freq(/ ", data[18][0], " )"));
                break;
        }

        switch(data[0])
        {
            case "scf":
                $writes_file(data[22][2], "VOUT(Vrms) Gain(dB) THD(%) t (stable)
                DC(V)");
                $writes_file(data[22][2], "\n");
                break;
        }

        switch(data[8])
        {
            case "vin":
                data[18][2]=data[9][data[10]];
                break;
        }
    }
}

```



```

        case "freq":
            data[18][1]=data[9][data[10]];
            break;
    }

    sw_pri();

    $writes_file(data[22][2], "\n End Time : ", $date()[0], "-", $date()[1], 2, , , @zero, "-", $date()[2],
    2, , , @zero, ", ", $date()[0], 2, , , @zero, ", ", $date()[1], 2, , , @zero, "\n");
}

}

function sw_pri()
{
    local i;

    for(data[7]=0; data[7]<length(data[6]); data[7]=data[7]+1)
    {
        switch(data[4])
        {
            case "vin":
                data[18][2]=data[6][data[7]];
                break;
            case "freq":
                data[18][1]=data[6][data[7]];
                break;
        }

        switch(data[0])
        {
            case "scf":
                sw_scf();
                $writes_file(data[22][2], $format("%12.2e%12.2e%12.2e%12.2e%12.2e%12.2e", data[6][data[7]],
                results[data[3]][1+5*(data[10])][data[7]], results[data[3]][2+5*(data[10])][data[7]], results[dat
                a[3]][3+5*(data[10])][data[7]], results[data[3]][4+5*(data[10])][data[7]], results[data[3]][5+5*(d
                ata[10])][data[7]]), "", $date()[0], "-", $date()[1], 2, , , @zero, "-", $date()[2], 2, , @zero, "
                ", $date()[0], 2, , , @zero, ", ", $date()[1], 2, , , @zero);
                $writes_file(data[22][2], "\n");
                break;
        }
    }
}

function sw_scf()
{
    local t, cycle;
    t=scf_init();

    local period = (1/data[18][1]);
    local time_step= 1/(400e3*100);

    cycle = (period)+t*2*period;

    $setup_checkpoint(cycle, $strcat(data[22][1], ".sav1"), @overwrite, @false);

    $setup_restart($strcat(data[22][1], ".sav2"));

    $add_analog_trace(data[20]);
    $force_dc(data[12], data[13][data[14]], @v, "//ground");
    $force_sinusoidal(data[18][0], data[18][5], data[18][2]*1.414, data[18][1], "0", "0", @v, "//ground");

    $setup_transient_analysis(time_step, cycle, time_step, @nouic, "", @nonoise, @nochecksoa);
    $set_temperature(data[16][data[17]], 27);
    kernel@@$as_run_synonym = "";
    $add_keeps(@nowindow, @nofull, data[18][0], data[20]);

    if(data[25][1]!="")
        $dofile(data[22][4]);

    $run();

    local level=($tmax(data[20],...cycle-period,cycle)-$tmin(data[20],...cycleperiod,
    cycle))/(2*1.414);
    local input=data[18][2];
    local gvc = 20*(log10((level/input)));
    local thd = thd3(data[20], @per, 1024, @linear, cycle-period, cycle, data[18][1]);
    local dc=($tmax(data[20],...cycle
    period,cycle)+$tmin(data[20],...2*cycle+0.01*period,cycle+0.01*period))/2;

```



```

results[data[3]][1+5*(data[10])][data[7]]=level;
results[data[3]][2+5*(data[10])][data[7]]=gvc;
results[data[3]][3+5*(data[10])][data[7]]=thd;
results[data[3]][4+5*(data[10])][data[7]]=cycle;
results[data[3]][5+5*(data[10])][data[7]]=dc;
}

function scf_init()
{

local i=0;
local in;//=data[18][2];
local freq;//=data[18][1];
local period, cycle, time_step;

do{
////////// Reset setup and delete keeps and runs //////////
del runs -a;
del keeps -a;
rese se -d;

switch(data[1][data[3]])
{
    case "ccc": dof modcc;break;
    case "lll": dof modll;break;
    case "llh": dof modlh;break;
    case "lhl": dof modhl;break;
    case "lhh": dof modhh;break;
    case "hll": dof modll;break;
    case "hlh": dof modlh;break;
    case "hhl": dof modhl;break;
    case "hhh": dof modhh;break;
}

in = data[18][2];
freq=data[18][1];
time_step= 1/(400e3*20); // Original 100;
period = (1/freq);
cycle=period;

$setup_checkpoint(cycle, $strcat(data[22][1], ".sav1"), @overwrite, @false);

if(i!=0)
{
    $setup_restart($strcat(data[22][1], ".sav2"));
}

$setup_transient_analysis(time_step, (2*i+1)*cycle+0.01*period, time_step, @nouic, "", @nonoise, @nochecksoa);
$set_temperature(data[16][data[17]], 27);
kernel@@$as_run_synonym = "";
$sadd_keeps(@nowindow, @nofull, data[20]);

$force_dc(data[12], data[13][data[14]], @v, "//ground");
$force_sinusoidal(data[18][0], data[18][5], data[18][2]*1.414, data[18][1], "0", "0", @v, "//ground");

$sadd_analog_trace(data[20]);

if(data[25][1]!="")
    $dofile(data[22][4]);

$sset_active_window("Chart");

$create_double_formatter("1", @f, 20, 9, @replace, "none");
$create_double_formatter("2", @f, 20, 9, @replace, "milli");

extern simview@@$current_chart_attrs = [data[20], "SandyBrown", "helvetica", 12, "bottom_left", "SandyBrown", "helvetica",
10, "bottom_left", "0", "100", "LightGray", "solid", 1, 0, 4, "off", 0, "analog_default_formatter"];
$$change_chart_axis_attributes([data[20], "SandyBrown", "helvetica", 12, "bottom_left", "SandyBrown", "helvetica", 10,
"bottom_left", 0, 100, "LightGray", "solid", 1, 0, 4, "off", 0, "1"]);

local x;

for(x=0;x<=10;x=x+1)
    $add_cursor("", (x)*period+i*10*period);

$run();

$setup_checkpoint(cycle, $strcat(data[22][1], ".sav2"), @overwrite, @false);

```

```

$setup_restart($strcat(data[22][1], ".sav1"));

$setup_transient_analysis(time_step, 2*(i+1)*cycle+0.01*period, time_step, @nouic, "", @nonoise, @nochecksoa);

if(data[25][1]!="")
    $dofile(data[22][4]);

$run();

i=i+1;

} while(abs($tvalue(data[20], (2*i-1)*cycle)-$tvalue(data[20], (2*i)*cycle))>3e-3);

return i;
}

```

End of file 1.

File 2 for plotting of the results of the userware

```

////////// Gain, THD vs Vin function //////////

function sw_plot( data:vector, results:vector
)

////////// Initialization //////////

{

local in1,in2,in3;

////////// Curve plotting //////////
////////// Initialization //////////

local no_of_curves = 3;
local w=$create_vector(length(data[6]));
local x=length(data[6]); // Primary Length
local y;

switch(data[0])
{
    case "scf":
    {
        y=5;
        break;
    }
}

local z=length(data[9]);
local pt = 0;
local xy = $create_vector(2); // Output
local curve1 = $create_vector(1);

// to create 1 curve, your_curve1
curve1[0] = $create_vector(x);
// to create 3 pts in the your_curve1
w =results[0][0];

local h,i,j,k;

for(h=0;h<length(data[1]);h=h+1) ///// MODEL
{
    for(i=0;i<z;i=i+1) ///// Secondary
    {
        for(j=0;j<y;j=j+1) ///// Output Net
        {
            for(k=0;k<x;k=k+1) ///// Primary
            {
                xy[0]=w[k]; // xy[0] = 1st data read
                xy[1]=results[h][1+j+i*y][k];
                curve1[0][k]=xy;
            }

            if(i==0 )
            {
                if(j==0)
                {
                    $open_chart($strcat($upper_string(data[0])," Sweep Simulation Primary
                    ( ",$upper_string(data[4])," ); Secondary ( ",$upper_string(data[8]),

```

```

    "));

    Sset_active_window($strcat("Chart#",2+h));

    $$add_curves($strcat("Sec_",data[8],"_",data[9][i]), "", @line, @data,
    @nooverlay, @nonewaxis,curve1);
}
else
{
    Sset_active_window($strcat("Chart#",2+h));

    $$add_curves($strcat("Sec_",data[8],"_",data[9][i]), "", @line, @data,
    @nooverlay, @newaxis,curve1);
}
else
{
    if(j==0)
    {
        Sset_active_window($strcat("Chart#",2+h));

        $$add_curves($strcat("Sec_",data[8],"_",data[9][i]), "Y", @line,
        @data,@overlay, @nonewaxis,curve1);
    }
    else
    {
        Sset_active_window($strcat("Chart#",2+h));
        $$add_curves($strcat("Sec_",data[8],"_",data[9][i]),
        $strcat("Y",j+1),@line, @data, @overlay, @nonewaxis,curve1);
    }
}
}

////////// Create Chart //////////

local a,b,c;

Sset_active_window($strcat("Chart#",2+h));

$change_axis_title($strcat($supper_string(data[4])," ",$supper_string(data[5][3])), "X");

switch(data[0])
{
    case "scf":
    {
        $change_axis_title("Output (Vrms)", "Y");
        $change_axis_title("Gain (dB)", "Y2");
        $change_axis_title("THD (%)", "Y3");
        $change_axis_title("attack time(s)", "Y4");
        $change_axis_title("DC (V)", "Y5");
        break;
    }
}

$smaximize_window();

$$add_text($strcat("Simulation File : ", $get_component_name()), [154, 700, $strcat("Chart#",2+h)], @data);

$$add_text($strcat("Tolerance ( R PNP NPN ) : ", $supper_string(data[1][h][0])," ",$supper_string(data[1][h][1]),"
", $supper_string(data[1][h][2])),[154, 680, $strcat("Chart#",2+h)], @data);

Sset_active_window($strcat("Chart#",2+h));

$$save_window($strcat(data[22][1],"_", $supper_string(data[1][h]),".wav"), @replace, @data, void, @nosetuponly);
}
}

////////// End of "gvc_vcc" //////////

```