Control of ultra-capacitor based power electronic converters

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Control of Ultra-capacitor Based Power Electronic Converters

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School of Electrical & Electronic Engineering

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SUMMARY

The performance and properties of power converters operating with constant voltage sources, such as batteries and rectifiers, have been thoroughly analysed in the existing power converter literature. However the same has not been done for power converters supplied by capacitors. This may be because the energy densities of conventional capacitors have not been sufficiently high to use them widely as replacements for batteries. However with the development of ultra-capacitors having moderate energy densities, this situation has now changed.

Ultra-capacitor is an emerging low voltage energy storage device that shows a very high potential as a short-term energy storage in many industrial applications. Ultra-capacitor is maintenance-free and easy to use compared to a battery, yet has a much higher power density. However, due to the low voltage rating of a single ultra-capacitor cell, a number of such cells are needed to be connected in series in order to make an ultra-capacitor bank that has a voltage rating sufficient for practical applications. Furthermore, the terminal voltage of ultra-capacitors varies in a wide range when they are charged or discharged. Therefore, a DC-DC converter or a DC-AC inverter is also required as an interface between the ultra-capacitor bank and a load that demands a constant voltage at its terminals.

Despite the growing use of power converters supplied by banks of ultra-capacitors, there is very little work done in analyzing the control characteristics of such systems. Therefore, the main focus of this thesis is to analyze the control characteristics of these ultra-capacitor based power converter systems.

It is shown in this thesis that the capacitor based DC-DC converter systems are characterized by an additional low frequency pole zero pair in its transfer functions compared to equivalent battery based systems. In the duty-ratio to output voltage transfer function, the additional zero lies extremely close to the origin in the right half plane while the additional pole lies close to the origin in the left half plane.

It is shown that the low frequency pole zero-pair exists in the ultra-capacitor based system transfer functions due to the finite capacitance of the ultra-capacitor banks. Hence it is practically impossible to prevent the occurrence of them in ultra-capacitor based systems. However, by varying the DC-DC converter configurations and also by varying their control configuration, the position of this pole-zero pair may be varied. By analyzing three of the common DC-DC converter configurations that can be used with ultra-capacitor based systems, namely the classical boost converter, fly-back converter and the tri-state boost converter, it is shown that the effect of the low frequency pole-zero pair is slightly different in different DC-DC converter configurations.

Furthermore, when the ultra-capacitor based DC-DC converter systems are controlled using voltage-mode control, which is the simplest method of control, the steady state output voltage of the system decays continuously with time, unless the controller is designed to compensate the low frequency pole and the low dc gain. It is shown that in order to eliminate these effects of the pole-zero pair, the pole and the zero should be pushed towards origin so that they are effectively cancelled with each other. Both peak current-mode control and sliding-mode control are shown to be capable of achieving this objective. Furthermore, the cancellation obtained with peak current-mode control is shown to be only approximate while the cancellation obtained with sliding-mode control is relatively more accurate. Therefore, controllers for ultra-capacitor based power converters, controlled using peak current mode control or sliding mode control, may be designed similar to equivalent battery based systems, without considering the effects of the low frequency pole zero pair.

The recently introduced Z source inverter is suitable for interfacing a variable DC voltage source directly with an ac load demanding a constant voltage. Hence it appears to be an excellent candidate for the use with ultra-capacitor banks.

In this thesis, it is shown that the Z source inverter can have three additional operating states, other than its three widely considered operating states. Moreover, this thesis presents a clear steady state analysis for all these operating states, and provides simple guidelines to design Z source inverter's unique impedance network, so that the three additional operating states are suppressed. Two methods of design are discussed, a non linear method and a simplified linear method. These design guidelines can be used to design the impedance network of a Z source inverter to match a given voltage source with a specified load.

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CHAPTER 1

INTRODUCTION

Power electronic converters supplied by dc power sources can be broadly divided into two categories as DC-DC converters and DC-AC converters (Inverters) depending on their output voltage waveform. The control and the characteristics of these converters are well documented in the literature [1-8]. However, in all such analysis, the dc source voltage is assumed to be constant by considering possible sources such as batteries, rectifiers or generators. Due to the recent technological developments in short term energy storage devices such as ultra-capacitors and energy sources such as fuel cells, a need has arisen to re-investigate the performance of these converters with variable voltage dc sources.

Ultra-capacitor is one of these emerging low voltage energy storage devices that show a very high potential as a short-term energy storage for power quality applications [9-14]. Ultra-capacitor is maintenance-free and easy to use compared to a battery, yet has a much higher power density. However, due to the low voltage rating of a single ultra-capacitor cell, a number of such cells are needed to be connected in series in order to make an ultra-capacitor bank that has a voltage rating sufficient for practical applications. Furthermore, the terminal voltage of ultra-capacitors varies in a wide range when they are charged or discharged. Therefore, a DC-DC converter or a DC-AC inverter is also required as an interface between the ultra-capacitor bank and a load that demands a constant voltage at its terminals. This means the DC-DC converter or the DC-AC inverter is required to operate with a variable voltage source. Among the numerous possible applications of ultra-capacitors, one promising application is in ride through systems for Adjustable Speed Drives (ASDs).

ASDs are widely used in commercial and industrial facilities due to their improved efficiency and energy savings. However, they are sensitive to power system disturbances, especially

voltage sags and momentary interruptions. Hence they could cause nuisance and costly tripping on industrial processes under such disturbances [15].

The general configuration of an ASD is given in Fig. 1.

Fig. 1. General configuration of an ASD

In the general ASD configuration, shown in Fig. 1, the power demands of the Voltage source inverter (VSI) and the motor loads are entirely or partially supplied by the stored energy in the dc link capacitance, during a momentary power interruption or a voltage sag. This causes a reduction in dc link voltage, which in turn results in tripping of the motor loads if the magnitude of the dc link voltage falls below a set threshold voltage.

Therefore, the ride through time of the basic ASD is dependant on the energy stored in the dc link capacitance. However the energy stored in the dc link is usually only sufficient to provide ride through for a few milliseconds, and hence is not sufficient to ride through most of the common voltage sags or interruptions [15].

For small voltage sags, methods such as Integrated boost converter approach or an inverter with boosting capability [16-18] can be used to boost up the dc link voltage or the voltage at the motor loads, after some modifications to the existing circuit in the general ASD configuration without the use of a separate energy storage. However these methods cannot handle deep voltage sags or momentary interruptions that completely cut off the source from

the load. Therefore, a ride through system that employs a separate energy storage that has the capability to handle all possible system disturbances, including small or deep voltage sags and momentary interruptions, should be used in such cases. (It should be noted here that the ride through systems discussed in this thesis are the ride through systems that has the capability to supply full power to the load during the supply disturbance. However, the ASD may be able to ride through the disturbance by other means such as the use of load inertia and operating at reduced speed [19], if the load can tolerate such conditions. These solutions can be implemented with almost no additional cost).

Apart from ultra-capacitors, flywheels and batteries are also widely considered as this energy storage for ride through systems [20]. However, Flywheel systems are bulkier and they involve moving parts that requires considerable maintenance. Hence they are mostly used at high power levels where the batteries or ultra-capacitors cannot be used. On the other hand, batteries are used at low to medium power levels but they also needed to be maintained frequently while their life time and the number of charge/discharge cycles are less compared to both flywheels and ultra-capacitors. Therefore, ultra-capacitors, which are maintenance-free and having a superior power density compared to batteries, are ideally suited as the short term energy storage in the ride through applications at low and medium power levels [10, 13, 20]. Ultra-capacitors also have a number of properties that make them very attractive to these ride through applications, such as, fast charge discharge capability, smaller size and environmental friendliness due to no harmful emissions etc [13]. In addition to the use in ride through systems, ultra-capacitors also find applications in other power quality solutions such as Dynamic Voltage Restorers (DVR) and Distribution Static Compensators (DstatCom) [21], as well as in uninterruptible power supply systems (UPS) as a replacement for the Battery [13]. A single ultra-capacitor cell has a very low voltage rating of the order of 2.5V. Therefore, a number of them are required to be connected in series to construct an ultra-capacitor bank that

is having a suitable voltage rating for practical applications. Moreover, a boost type DC-DC converter is required as the power converter to interface ultra-capacitors to the rest of the system to regulate the voltage at the dc link against continuously decreasing ultra-capacitor terminal voltage during the ride through period.

A number of boost type DC-DC converters can be used as the power converter in ultra-capacitor based ride through systems. However, if galvanic isolation is not required, the simplest form of the converter that can be used is the classical boost converter. A separate buck converter is also required to recharge the ultra-capacitors once their charge is depleted after one or more ride through cycles [11]. However, the buck converter operates only when the system is healthy and its operation is, therefore, not very time critical. An alternative arrangement is the two quadrant DC-DC converter, which has both boost and buck capabilities [12]. However, this system also operates similar to the above, i.e. boost operation to provide ride through for the load and buck operation to charge the ultra-capacitors. If galvanic isolation is required, then fly-back converters can be employed as the power converter between the ultra-capacitors and the dc link [15].

1.1 Motivation

Applications involving ultra-capacitors, such as the ride through systems for an ASD, are expected to grow in the near future [9, 22, 23]. With more and more ultra-capacitors having moderate energy densities being developed, they also have a considerable promise to be used as replacements for batteries or used together with batteries in a wide variety of applications [9, 13, 23-25].

Because of the low voltage rating of the ultra-capacitors and widely varying terminal voltage, it is necessary to use a DC-DC converter to interface ultra-capacitor banks to the rest of the system. As mentioned earlier, the control characteristics of DC-DC converters supplied with

batteries have been analyzed thoroughly in recent times [1, 8, 26-28]. However, the same has not been widely done for DC-DC converters supplied with capacitors. This is the main motivation for the detailed studies and analysis of this thesis.

When a dc voltage source with a varying terminal voltage, such as a bank of ultra-capacitors, is used to power an ac load, the usual practice is to use a DC-DC converter and an inverter between the voltage source and the ac load. The DC-DC converter is used to maintain a constant dc supply at the input of the inverter while the inverter transforms dc to ac. The recently proposed Z-Source inverter [17], however, is capable of interfacing such variable voltage sources to ac loads directly, without the use of the DC-DC converter. The Z-Source inverter achieves this goal by modifying the dc link of the conventional voltage source inverter and modifying its switching pattern. Currently, most of the research work in Z-Source inverters is focused on methods to optimize the performance of the Z-Source inverter output by optimizing the switching pattern [29-31]. However the Z-Source inverter has a unique LC impedance network, and, very little attention has been given to design this impedance network for a given ac load and for a given variable voltage dc source.

Prior to analyzing the performance or control characteristics in detail, it is very vital to design this impedance network properly so that this complex impedance network performs as required. As the use of Z-Source inverters in power quality and power supply applications is also expected to grow, it is necessary to derive simple guidelines to design the impedance network of a Z-Source inverter. This is the motivation behind the final sections of this thesis.

1.2 Objectives

The main objectives of this research are as follows.

1. Analyzing special properties of ultra-capacitors and their applications. This involves a detailed literature review to identify the potential of ultra-capacitors for practical applications and their limitations.
2. Analyzing control characteristics of an ultra-capacitor based ride through system in comparison to those of a battery based ride through system. Classical boost converter is mainly used for this initial analysis as it is the most widely used converter for ultra-capacitor based applications at present.
3. Extending the analysis of control characteristics to a number of other commonly used power converter topologies for ultra-capacitor based applications. The power converter topologies considered in this thesis are the tri-state boost converter, fly-back converter and the Z-Source inverter.
4. Investigating the effects of more advanced control methods such as peak current-mode control and sliding-mode control in alleviating the difficulties found with voltage-mode control in ultra-capacitor based systems.
5. Designing the impedance network for a Z-Source inverter to interface a given dc voltage source with a specified ac load.

1.3 Major Contributions of the Thesis

The following contributions have been made as a result of this research work.

1. Identifying the existence of an additional low frequency pole-zero pair and the low dc gain in the transfer functions of ultra-capacitor based converter systems in comparison to those of a battery based system. It is shown that the control systems for voltage-mode controlled ultra-capacitor based systems should be designed considering the presence of this additional pole-zero pair and the low dc gain.

2. Demonstrating that the low frequency pole-zero pairs in the transfer functions of the ultra-capacitor based systems are caused by the finite capacitance of ultra-capacitor banks.

It is shown that the low frequency pole-zero pairs cannot be eliminated from ultra-capacitor based system transfer functions because of the finite capacitance of ultra-capacitor banks. However, it is shown that the converter configuration and the other converter parameters affect their individual positions to a certain extent. During this analysis, the positions of the low frequency pole-zero pairs of several converter configurations that can be used with ultra-capacitor based applications, such as the classical boost converter, tri-state boost converter, fly-back converter and the Z-Source inverter, were derived.

3. Demonstrating that by employing some more advanced control strategies, the effect of the low frequency pole-zero pairs of ultra-capacitor based systems can be minimized.

Through a detailed analysis of the transfer functions under peak current-mode control and sliding-mode control, it is shown that both of them have the capability to drive the low frequency pole and zero towards each other considerably. This in turn approximately cancels the effects of both the pole and the zero with each other so that their effect on the closed loop response is negligible. Therefore, it is shown that the control systems that use these control methods can be designed without considering the low frequency pole zero pair. Sliding-mode control is shown to be the more effective of the two methods to control ultra-capacitor based ride through systems. However, considering the fact that the useful operating period of the ride through systems is only a few seconds, the improvement obtained with peak current-mode control is also shown to be adequate in practical applications.

4. Identifying the six possible operating states of the Z-Source inverter and deriving methods to design its impedance network.

The Z-Source inverter has the unique capability to directly interface a variable dc voltage source, such as an ultra-capacitor bank, to an ac load demanding a constant voltage at its terminals. This thesis shows that, in general, the Z-Source inverter can be operated in six different circuit states, rather than the three circuit states that are widely discussed. The thesis also provides simple guide lines to design the impedance network, which is unique for Z-Source inverters, to interface a given load with a given dc voltage source. Two methods of design are demonstrated that design the impedance networks to operate with large or small ripples.

1.4 Organization of the Thesis

In Chapter 2, the development of ultra-capacitors and their applications are discussed. Ultra-capacitors are known to possess slightly different properties than the normal capacitors. The models available to describe these unique properties of ultra-capacitors and the methods adopted to derive their parameters are also discussed in this chapter.

Chapter 3 presents a summarized literature review on some of the power converters that can be used with ultra-capacitor banks and their control characteristics with a constant emf dc source. The classical boost converter, fly-back converter, tri-state boost converter and the Z-Source inverter are selected as the possible converters. Three of the control methods that are commonly used to control DC-DC converters, namely voltage-mode control, current-mode control and sliding-mode control, are also presented in this chapter.

Chapter 4 extends the analysis in Chapter 3 to capacitor based DC-DC converters. This analysis shows the existence of a low frequency pole-zero pair in the capacitor based DC-DC converter transfer functions.

The analysis in Chapter 4 also shows that the low frequency pole-zero pair is in fact a result of the finite capacitance of capacitor banks and hence cannot be avoided by changing the converter configuration.

Chapter 5 analyses the ultra-capacitor based ride through system for an ASD that employs a classical boost converter as the interfacing DC-DC converter, which is the most common power quality application of the ultra-capacitors. Main attention is given to highlight the control properties of the system and to demonstrate the existence of the low frequency pole-zero pair in the ultra-capacitor based system transfer functions. It is shown that in voltage-mode control, the low frequency pole and the low dc gain should be considered when designing the control system of the ride through system. Simulation and experimental results are presented for an illustrative example to aid the discussions.

Chapter 6 discusses how the effect of the low frequency pole-zero pair can be minimized by adopting peak current-mode control and sliding-mode control. Hence, it is shown that control systems under these control methods can be developed without considering the effects of the low frequency pole zero pair. Both simulation and experimental results are presented to verify the conclusions for selected illustrative examples.

The recently proposed Z-Source inverter, which shows promise for ultra-capacitor based applications, is investigated in Chapter 7. It is shown that, in addition to the three circuit states commonly discussed, the Z-Source inverter can operate with three more circuit states. It is shown that these additional circuit states degrade the performance of the Z-Source inverter. Guidelines to design the impedance network of the Z-Source inverter for a given source and a load, so that these additional circuit states are suppressed, are described in this chapter. Two methods of design are demonstrated so that the impedance network operates with large or small ripples in its currents and voltages. Simulation results are given to validate the design

guidelines. Special considerations that should be noted when designing the Z-Source inverter in ultra-capacitor based applications are also discussed.

Finally, Chapter 8 summarizes the main findings of the research and presents recommendations for future work.

CHAPTER 2

ULTRA-CAPACITORS

2.1. Introduction

Ultra-capacitors are a new type of capacitors developed during the last few decades [9]. The most striking feature of these capacitors is their very high capacitance. While the capacitances of normal capacitors are in milli Farads or micro Farads range, the capacitances of ultra-capacitors generally lie in the Farrads range with some having capacitances even up to several thousands of Farads. In fact the term ‘ultra-capacitors’ is used for these capacitors due to their very high capacitance. ‘Supercapacitors’ and ‘Electrochemical capacitors’ are two of the other names used frequently for these devices [9].

Ultra-capacitors have intermediate properties between those of the normal capacitors and batteries. Hence they are widely being considered in short term energy storage applications as a replacement for batteries or to operate in tandem with batteries to reduce the burden on batteries. This chapter presents a detailed literature review of the properties and applications of the ultra-capacitors. Moreover, the attempts to develop an electrical equivalent circuit for the ultra-capacitors to describe their unique properties, are also discussed.

2.2. Historical Developments of Ultra-capacitors

The principle that the electrical energy can be stored in a charged capacitor has been known since 1745 [9]. The amount of energy stored is $\frac{1}{2}C\nu^2$ where, C is the capacitance of the capacitor and ν is the voltage difference between the plates accommodating the charge.

The utilization of the same principle to store electrical energy for practical purposes, as in a cell or a battery seems to have been first proposed and claimed as an original development in

the patent granted to H.E. Becker in 1957 [9]. The patent described electrical energy storage by means of the charge held in the interfacial double layer at a porous carbon material perfused with an aqueous electrolyte. The principle involved was charging the capacitance, of the double layer that arises at all solid / electrolyte interfaces and therefore, the capacitors developed were known as double layer type capacitors. After Becker, the SOHIO Corporation in Cleveland, Ohio, USA, also utilized the double layer capacitance of the high area carbon materials, but in a nonaqueous electrolyte to develop similar type of capacitors [9].

A different principle called a “pseudocapacitance” was utilized and developed from 1975 onwards as the basis for the energy storage in a new type of capacitor [9, 32]. Pseudocapacitance arises whenever, for thermodynamic reasons, there is some continuous dependence of a charge, q , passed Faradically in Oxidation or Reduction, upon the electrode potential, V . Thus, a derivative dq/dV can arise that corresponds to a pseudocapacitance that is directly measurable, or utilizable, as a capacitance. However, the materials showing pseudocapacitance are still too expensive to develop large-scale capacitors of high energy [9]. Hence, almost all of the ultra-capacitors being used in high power applications are of the double layer type.

The large capacitances, on the order of several Farads per gram, that can be achieved with pseudocapacitors or double layer type capacitors led to the terms “supercapacitors” or “Ultra-capacitors” being used widely for these capacitive devices. But recently, a more general term “electrochemical capacitors” is also being used to describe them [9].

2.3. Construction of the Ultra-capacitor

A rough sketch of the construction of a double layer type ultra-capacitor is given in Fig 2.1 [33]. Activated Porous Carbon materials having a high specific area in the range of 1000-2000 m^2/g are used as the electrode material of the double layer type ultra-capacitors. They have a

complex pore structure distributed in a three dimensional space in which the liquid electrolyte can penetrate and fill in [9]. The diameter of a pore of the porous structure is in nanometer range. The current collector in Fig 2.1 is a metallic sheet that is used to connect the positive and negative external leads of the capacitor to the corresponding porous electrodes inside capacitor. The porous insulating membrane separates the positive and negative electrodes but allows positive and negative ions of the electrolyte to pass through [9, 34].

Fig 2.1. Construction of the ultra-capacitor

The key factor that enables double layer type ultra-capacitors to have a very high capacitance in a small volume is the utilization of electrode materials with high specific surface area such as activated porous carbons. Similarly, the materials used to develop pseudocapacitive ultra-capacitors have a quasi-3-dimensional, electronically conducting structure, giving accessibility to protons and electrons that are involved in two or three successive, reversible oxidation or reduction steps in charge or discharge, respectively [9].

Although ultra-capacitors are categorized as double layer type and pseudocapacitive type, it is now known that the actual capacitance of a certain ultra-capacitor has a mixture of both. About 1% – 5% of the total capacitance of double layer type ultra-capacitors consists of pseudocapacitance due to the faradic reactivity or certain surface (edge) functionalities due to the impurities present on carbon. On the other hand, pseudocapacitive type ultra-capacitors

also exhibit a double layer type capacitance proportional to their electrochemically accessible interfacial areas, about 5% to 10% [9].

At present, ultra-capacitors are manufactured in a number of sizes ranging from about 0.01 F to 5000F [13]. Typical voltage rating of a single ultra-capacitor cell is approximately about 2-3V. A selection of currently available commercial ultra-capacitors is shown in Fig 2.2.

Fig. 2.2. Commercial electrochemical capacitors and toy equipped with an electrochemical capacitor [13]

Currently, there are a number of ultra-capacitor manufacturers in the world. Some of the leading manufacturers are Maxwell Technologies in San Diego, USA; Epcos in Munich, Germany; Panasonic in Osaka, Japan and Nesscap in Yongin, Republic of Korea.

2.4. Properties of Ultra-capacitors

The main property of the ultra-capacitors is the high capacitance [9]. Now even 5000 F capacitors are available in the market, which have very small volumes and weights. However,

the voltage rating of a single ultra-capacitor cell is still low, around 2.5 V for capacitors utilizing non-aqueous electrolytes and about 1 V for capacitors utilizing aqueous electrolytes. Ultra-capacitors have about 20 times higher energy density compared to the normal capacitors. But compared to a conventional battery, its energy density is lower – about $1/10^{\text{th}}$ of a conventional battery. On the other hand, ultra-capacitors have a superior power density compared to batteries, but it is seen to be lower than that of normal capacitors [9],[13, 35]. Hence, as illustrated in Fig. 2.3 [13], ultra-capacitors bridge the gap between the normal capacitors and batteries in the power-energy spectrum, and thereby create opportunities for a number of small scale energy storage applications that were not possible before.

Fig 2.3. Ragone plot for various energy storage and conversion devices

An ultra-capacitor can be charged or discharged in about 0.3 – 30 seconds. Although this is very much larger than normal capacitors, it is much faster compared to batteries, which usually take about 1000 Seconds to charge or discharge [34]. Furthermore, the ultra-capacitors do not explode like normal capacitors even if their terminals are short circuited [17]. This makes ultra-capacitors more suitable for applications that require fast and safe energy transfers.

Moreover, the ultra-capacitor can be cycled about 1000000 times during its lifetime, which is about 30 years [31]. Although this value is less than the conventional capacitors, it is very

much higher than that of the batteries. Furthermore, there is no “memory effect” as that of Ni-Cd batteries in the ultra-capacitors and also they don’t show parasitic life limiting irreversible chemical reactions [9, 34]. Due to this reason, the ultra-capacitors are maintenance-free, similar to the normal capacitors, and also are safer and environmentally friendly.

2.5 Applications of Ultra-capacitors

The properties discussed in section 2.4 suggests that the ultra-capacitor is more suitable for applications as a power supply and as an energy storage [14, 21, 36]. The ideal applications include all those demanding energy for a duration in the time range 0.01 seconds to 100 seconds. Also the lower energy density of low voltage capacitors makes them very attractive for pulse power applications in the millisecond range. However the present ultra-capacitors are not suitable for AC applications and for applications involving a high ripple current. This is because the internal resistance of the ultra-capacitors is higher than that of the normal capacitors and under AC applications thermal degradation can occur. Moreover, some manufacturers use asymmetric electrode systems or have special treatments on one of the electrodes so that the two electrodes become non identical [16]. This results in a polarity of the devices [22].

Currently, the ultra-capacitors are used in the following application areas.

(a) Power supplies or back up power supplies.

Ultra-capacitors have been used as Memory backup power supplies for computers for about 30 years now [9]. Ultra-capacitors also find applications as backup power supplies of video recorders, TV satellite receivers, alarm clocks, radios and process controllers. Typical backup durations provided by the ultra-capacitors in these applications vary from few hours to weeks. However, in cameras, programmable pocket calculators, mobile phones etc. they are used to provide backup for a few minutes during the replacement of the battery. Other than these,

ultra-capacitors are also being used as power supplies of toys, smoke detectors, emergency lights, starters, igniters and actuators.

(b) Alternating power sources

Ultra-capacitors are also used as “alternating power sources”, for example with solar power. In the day solar cells power the electric load while charging the ultra-capacitor and in the night ultra-capacitor takes over the electric load. Examples are solar watches, solar lanterns, road marking lanterns, traffic warning lights etc.

(c) Voltage regulation in distribution systems

Voltage regulation in distribution systems such as in Aircraft power systems, transportation networks etc, under variable load conditions [33, 35, 37].

(d) Electric vehicles, Hybrid electrical vehicles and fuel cell vehicles

Ultra-capacitors are also used in Electric vehicles (EV), Hybrid electrical vehicles (HEV) and fuel cell vehicles. All these are more or less at research level at present but are likely to be improved in near future. In these applications the ultra-capacitor is used as a power source and an energy storage device. Typical functions of the ultra-capacitors are, storing the energy obtained from regenerative braking and provide accelerating power to the vehicle. In these applications, generally, the ultra-capacitor takes the “varying load” while the primary power source (Battery (in EV), internal combustion engine(in HEV) and fuel cell (in fuel cell vehicle)) is providing the “constant or base load”. Similar applications are also possible in elevators, cranes etc [38-44].

(e) Ride through systems for adjustable speed drives

Ultra-capacitors are also used to provide short-term ride through power for adjustable speed drives (ASD). Also the Varying power requirements of the ASD can be provided by the ultra-capacitors, thereby reducing the burden on the utility and also reducing the power quality

problems associated with ASDs. Again this application is also at research level at present [11, 20].

(f) Energy storage in uninterruptible power supplies

Some industrial processes / equipment are very sensitive to short interruptions and disturbances of mains supply. Power Quality and UPS (Uninterruptible power supplies) devices employing batteries and normal capacitors are used these days to protect them. Considering the energy and power capabilities of the ultra-capacitor, it can be used in place of the batteries in such applications. This will reduce the size and cost of these equipment [45].

2.6. The Electrical Double Layer

Most of the ultra-capacitors used in high power applications at present are double layer type ultra-capacitors [9]. This section describes both the physical and the electrical model of the electrical double layer, which is responsible for the high capacitances exhibited by these ultra-capacitors.

2.6.1 Physical Model of the Electrical Double Layer.

Charged electrode / solution interfaces have electrical double layers that have very high capacitances of about $16 \mu\text{F}/\text{cm}^2$ to $50 \mu\text{F}/\text{cm}^2$ [9]. This high double layer capacitance is the major component in the high capacitance of the (double layer type) ultra-capacitors.

Currently the best model that describes the electrical double layer is the Grahame model [9] shown in Fig. 2.4. Note that the figure shows only a negatively charged electrode.

Fig 2.4. Electrical double layer at the charged electrode solution interface

In Fig. 2.4, ψ_M , ψ_s and ψ_l represents the absolute potentials of the electrode, bulk electrolyte and the outer Helmholtz layer.

The Grahame model, shown in Fig. 2.4, consists of three distinguishable regions, namely, the inner Helmholtz layer, the outer Helmholtz layer and a diffuse ion distribution region. The inner and the outer Helmholtz layers correspond to the difference distances of closest approach that can arise for anions compared to the cations at the electrode surface. At extremes of polarization, (i.e. for high positive or high negative charge densities), one or the other of the Helmholtz layer regions dominates, with a population of anions or cations, depending on the polarization. Because anion distances of closest approach are usually smaller than hydrated cation distances of closest approach, the inner layer capacitance at positively charged electrode surfaces is usually higher than that of the corresponding negatively charged surface. These aspects of double layer capacitance behavior are of great significance to the understanding of the properties of the double layer type ultra-capacitors and the magnitude of capacitance that can be achieved per unit area over various ranges of potential and various electrode materials [9].

Note that the electron density on the electrode side is assumed to lie within the electrode in the Grahame model. However, at the electrode surface the electrons tend to overspill towards the electrolyte solution, as described by the Gellium model, in practical electrode to solution interfaces [9].

2.6.2 Approximate Electrical Equivalent Circuit Model of the Double Layer

Section 2.6.1 above, briefly describes the physical shape of the electrical double layer at the electrode electrolyte interface and its complexity. The corresponding electrical behaviour is approximately represented by the electrical equivalent circuit shown in Fig 2.5 [46].

Fig. 2.5 Approximate electrical equivalent circuit of the double layer

In Fig. 2.5, C_{dl} represent the capacitance of the double layer, which is the series combination of the Helmotz layer capacitance (C_H) and the diffuse layer capacitance (C_{diff}). R_{ct} and R_s represent the charge transfer resistance at the electrode-solution interface and the resistance of the electrolyte respectively. The Warburg (frequency dependant) impedance (W) represents the diffusion in the electrode processes [9].

C_{diff} is not a constant value. It is a function of absolute electrode and bulk electrolyte potentials, absolute temperature, bulk electrolyte concentration, mean value of dielectric constant of electrolyte and the charge number of positive and negative ions[9, 46]. Similarly C_H also varies as a function of surface area of the electrodes, dielectric constant of the solvent

and the distance between the charge layers in the electrode and the Helmholtz layers [9, 46].

Therefore, the double layer capacitance C_{dl} also varies accordingly.

The impedance, $R_{ct} + W = Z_f$, represents the impedance of faradic processes involved in the over-charging of the double layer capacitance and self-discharging. In fact, the electrolyte concentration is very high in the practical ultra-capacitor, and therefore, the thickness of the diffuse layer is very small due to nanometer dimensions of the porous electrodes [9]. Therefore, the effect of C_{diff} and also the effect of W are quite small in a practical ultra-capacitor.

2.7. Electrical Model of the Ultra-capacitor

The behavior of an ultra-capacitor is quite different from a normal capacitor. Other than the various properties described above, the most significant property is that its capacitance varies with voltage, frequency, magnitude of charging current and temperature [9]. Therefore, several attempts have been made to approximately model this complex device in terms of simple electrical components (resistors, capacitors and inductors), in order to understand it better and predict its properties [9, 46-53].

The porous electrodes used in the ultra-capacitors have a complex pore structure. In most of the approximate models that involve calculations related to pores and pore structure of the electrode, the pores have been assumed to have a cylindrical shape having a constant diameter. However the calculations related to a cylindrical shaped pore filled with electrolyte and its charge distribution under the influence of an applied potential, relates to a semi infinite transmission line charging under the influence of a potential applied to it from one end [9]. The measured frequency response of the ultra-capacitor also shows a behavior similar to a transmission line [9], and therefore, the assumption that the pores are actually of cylindrical shape does not lead to a significant error.

Note that a practical double layer type ultra-capacitor is constructed as shown earlier in Fig. 2.1. Due to this construction, the ultra-capacitor always comes with two double layer capacitances in series, the capacitance of the positive electrode and that of the negative electrode. However, the ultra-capacitor models described below represent the equivalent capacitance between the terminals of the ultra-capacitor and hence they necessarily represent the series equivalent capacitance of the positive and negative electrode capacitances.

2.7.1 Model Describing Dynamic Behavior of Ultra-capacitor

The dynamic behaviour of the ultra-capacitor is more accurately represented by the advanced equivalent circuit shown in Fig. 2.6 which was proposed by S. Buler *et al.* [49].

Fig. 2.6. Model describing the dynamic behavior of the Ultra-capacitor

In this model, L_{lead} and esr represent the ultra-capacitor lead inductance and the equivalent series resistance respectively. The complex pore impedance, Z_p , models the porosity of the ultra-capacitor electrodes. Its expanded model is given in Fig. 2.7 [9, 49]. Note here that Fig. 2.7 also represents a uniform semi-infinite transmission line, mathematically expanded to a different configuration [48, 49].

Fig. 2.7. Representation of complex pore impedance Z_p

This model approximates the behavior of ultra-capacitors very closely at high frequencies although it deviates slightly from the actual behavior at low frequencies. This is because Z_p is identical to the uniform semi-infinite transmission line [49] and, as already mentioned, the semi-infinite transmission line accurately describes only the high frequency (transient) behavior of the ultra-capacitor.

Nevertheless, the model has several advantages, including the reasonable accuracy and the fact that the number of parameters needed to calculate are less, compared to most of the other detailed models described below [9, 49]. Apart from L_{lead} and esr , only 2 parameters need to be calculated to determine the complete ultra-capacitor model, namely τ and C_{uc} [49]. Moreover, it is shown in [49] that the model approximates the practical behavior of ultra-capacitor quite well if the number of RC branches is selected to be at least 10, i.e. $n \geq 10$.

2.7.2 Transmission Line Model

The model proposed by F. Belhachemi *et al.* [48] is shown in Fig. 2.8.

Fig. 2.8. Transmission Line Model

In this model, a transmission line is used to represent the short term transient behavior of the ultra-capacitor. A set of RC elements are added to describe its behavior in longer time [48].

Although the model is quite accurate, the number of parameters needed to determine the complete model increases with the increase of number of parallel branches 'n'.

2.7.3 Ladder Circuit Model

The ultra-capacitor frequency response, which is similar to the frequency response of a semi infinite transmission line [9], can be approximated by a ladder circuit [9, 47] consisting of several RC branches with different time constants, as shown in Fig. 2.9. L_{lead} is used to represent the inductance of the capacitor leads. For higher accuracy, however, the number of branches has to be increased. Therefore, the number of parameters to be determined in this model is higher when aiming for higher accuracy [9].

Fig. 2.9. Ladder Equivalent Circuit

2.7.4 Three-Branched Model

Three-branch model proposed by Zubeita and Bonert [51] is shown in Fig. 2.10. This model takes into account the energy evolution during and after the fast transients as well as the dependence of the capacitance on voltage. The first branch, consisting of the R_i , C_{i0} and the variable capacitance KV_{ci} , describes the energy evolution during charging and discharging of the ultra-capacitor, while the other two branches, known as the delayed branch (R_d and C_d) and the long term branch (R_l and C_l), describes the internal redistribution of energy following charging or discharging in the time range of minutes and above [51]. The equivalent parallel resistance (epr) represents the self discharge of the ultra-capacitor.

Fig 2.10. Three-Branch Model

Therefore, to determine the complete model, a total of ten parameters need to be determined as per the three-branch model. However, the second and the third branches, as well as *epr*, may be omitted from the model if the interested time duration is only a few seconds, in which case, the number of parameters to be determined reduces to five.

2.7.5 Classical Equivalent Circuit

This classical model, shown in Fig. 2.11, considers the ultra-capacitor simply as a normal capacitor [9, 50, 54].

Fig. 2.11. Classical Equivalent Circuit

In Fig. 2.11, *esr* and *epr* represent the equivalent series resistance and the equivalent parallel resistance respectively, while *C_{eq}* represent the equivalent capacitance of the ultra-capacitor. *L_{lead}* represent the inductance of the ultra-capacitor leads. The Classical equivalent circuit is capable of approximately representing the ultra-capacitor behavior under slow charge / slow

discharge conditions. It is not suitable for analyzing fast transients in time domain. Unlike the other ultra-capacitor models described above, the classical model parameters are easy to derive, and in most cases, are provided in the manufacturer's data sheets.

2.8. Comparison of Existing Ultra-capacitor Models

All the commonly used ultra-capacitor models, described above in section 2.6, represent some form of a ladder model with varying number of RC ladder branches. The model accuracy is only proven in time domain for the classical model, the three-branch model and the transmission line model [9, 48, 51]. However the accuracy of the ladder model and the model describing dynamic behavior is proven both in time domain and frequency domain [49].

Although no model is universally accepted yet as the correct ultra-capacitor model, the available experimental results, both in frequency domain and time domain, suggest that the ultra-capacitor is accurately represented by a uniform transmission line model or by a ladder model with a sufficiently high number of ladder branches [9]. In ladder model, the model accuracy and the model complexity increase, as the number of ladder branches is increased. A reasonable compromise between the accuracy and the complexity may be obtained by reducing the number of ladder branches, as shown with the ladder model [9] and the three-branch model [51].

The model describing the dynamic behavior of the ultra-capacitor [49] has a complexity equivalent to a uniform transmission line model. But the model is represented in a very simple configuration so that the number of model parameters needed to be determined is minimized. Because of this simplicity and also due to its proven accuracy, this model can be considered as one of the most advanced and accurate models for the ultra-capacitor at present.

2.9. Model Parameter Extraction of Existing Models

The classical model, the three-branch model and the physical based model use time domain techniques to derive the model parameters while the other two models use frequency domain techniques. In time domain techniques, the capacitor is charged and discharged with a constant current to derive the model parameters. Pulse charging and the time domain response are also used to derive some of the complex parameters in these techniques. In frequency domain techniques, the capacitor frequency response is measured for a wide frequency band and the parameters are extracted by analyzing the changes in the terminal input impedance. However in most of the frequency domain techniques, specialized computer programs are also used to derive the model parameters. These computer programs allow the user to specify a certain model, generally of ladder type, and derive parameters for that model. Some of these software first determines the transfer function from the frequency response data and then calculate the model parameters which minimizes the error between the model predicted response and the actual response [55]. The user can change the order (and hence the number of branches of the ladder circuit) of the transfer function and then determine the parameters from the software to obtain the optimum equivalent circuit.

Most of the other Impedance spectroscopy software uses nonlinear least squares fitting techniques to obtain the model parameters. These techniques allow the user to input a certain model and some initial parameter values for the model. Then, after some iterations, the program finds the optimum values for those parameters so that the overall error between the actual response and the calculated response is minimized.

2.10 Selection of an Ultra-capacitor Bank for Practical Applications

Ultra-capacitors have considerable promise as short term energy storage in power quality applications [9, 15, 34], Uninterruptible power supply applications [43] etc. When selecting the size and the ratings of an ultra-capacitor bank for such an application, the following factors need to be considered.

- 1) Maximum power demanded by the load and the required ride through time.
- 2) The maximum and the minimum allowable terminal voltage of the ultra-capacitor bank.
- 3) Maximum current that can be drawn from the ultra-capacitor bank

The size of the ultra-capacitor bank is primarily determined by the first two conditions given above while the last condition is needed when selecting a particular ultra-capacitor cell for the already designed bank. For simplicity and also because an approximate value is sufficient at this stage, the classical model is usually used for the ultra-capacitor in these calculations [42, 56].

Assume that the fully charged terminal voltage of the ultra-capacitor bank is $V_{uc\max}$, and that it has a useful terminal voltage range down to $V_{uc\min}$. If the capacitance of the capacitor bank is C_{uc} , Then the total useful energy stored in the capacitor bank, E_{uc} , is given by

$$E_{uc} = \frac{1}{2} \cdot C_{uc} \cdot (V_{uc\max}^2 - V_{uc\min}^2) \quad (2-1)$$

Assume that the rated load voltage and current are given by V_{load} and I_{load} respectively.

Then, the energy requirement of the load to run for t_{ride} seconds is given by,

$$E_{load} = V_{load} \cdot I_{load} \cdot t_{ride} \quad (2-2)$$

By equating (2-1) and (2-2), the capacitance of the ultra-capacitor bank can be obtained so that it can support the load for t_{ride} seconds, neglecting losses.

$$C_{uc} = \frac{2 \cdot V_{load} \cdot I_{load} \cdot t_{ride}}{V_{uc\max}^2 - V_{uc\min}^2} \quad (2-3)$$

If the efficiency of the system connecting the ultra-capacitor bank and the load, η , is known, then the losses may also be incorporated into (2-3) and the value of C_{uc} will then be changed to,

$$C_{uc} = \frac{2 \cdot V_{load} \cdot I_{load} \cdot t_{ride}}{\eta (V_{uc \max}^2 - V_{uc \min}^2)} \quad (2-4)$$

Since ultra-capacitor cells have a very small voltage rating, a number of cells are required to be connected in series to obtain the voltage rating $V_{uc \max}$. This creates some additional problems related to cell balancing [57-64], i.e. to equalize the voltage distribution across each and every cell in the series connection. These cell balancing circuits reduce the efficiency of the ultra-capacitor bank due to the power losses in these balancing circuits. Usually, a number of these series ultra-capacitor banks are needed to be connected in parallel to meet the current rating requirements of the load.

2.11. Summary

The phenomenon of the electrical double layer at an electrode-electrolyte interface that contributes to the high capacitance of the double layer type ultra-capacitors was introduced. This was followed by a description of the physical model of the double layer. Some descriptions of the existing models proposed for the ultra-capacitors, and the methods used to derive their parameters were also described. The two methods that are used to derive the parameters of various models, namely, the time domain and frequency domain techniques, were also briefly discussed.

The model describing the dynamic behaviour and the transmission line model are more suitable for describing the transient behaviour of the ultra-capacitors. The three-branch model and the ladder model can be used to approximately describe transient behaviour as well as the behaviour in longer time, depending on the number of branches used. But the classical model,

which is the simplest model that can be used for the device, is only suitable to describe the behaviour in longer times or in steady state. However, it should be noted that none of the above models have yet been universally accepted as the correct model for the ultra-capacitor.

When the size of the ultra-capacitor bank is calculated for a particular application, the usual practice is to use the classical model of the ultra-capacitor [42]. This is mainly because of its simplicity. However, the value obtained is also seen to be reasonably accurate in practical short term energy storage applications [42].

The next chapter presents a literature review of the control characteristics of the power converters that can be used with ultra-capacitor banks and the closed loop control methods available for their control.

CHAPTER 3

Power Converters and Their Control

3.1 Introduction

As a low cost and maintenance-free substitute for batteries, ultra-capacitors show considerable promise in power quality applications. However, the rated voltage of an ultra-capacitor cell is still very small, of the order of 2-3V [9], and hence a number of ultra-capacitor cells are needed to be connected in series in order to make an ultra-capacitor bank having a sufficient voltage rating applicable to high power loads. Apart from this the terminal voltage of an ultra-capacitor also varies in a wide range when they are charged or discharged. Therefore, in order to interface the ultra-capacitor bank with a load demanding a constant voltage, a DC-DC converter is required between the load and the ultra-capacitor bank. To optimize the cost, the usual practice is to construct the ultra-capacitor bank so that its voltage rating is less than the voltage rating of the load and to interface it with the load with a boost type DC-DC converter [11, 15, 39, 42, 65, 66].

When no galvanic isolation is required between the load and the source, the most widely used form of the boost converter to interface ultra-capacitor banks is the classical boost converter. In fact this is the simplest form of the boost converter that can be used for the application. Alternatively, the fly-back converter is used for ultra-capacitor based applications in cases where galvanic isolation is required.

In fact, since the ultra-capacitors are required to be recharged frequently, a two quadrant DC-DC converter is used as the interface in almost all of the ultra-capacitor based power quality applications. However, the buck operation of the DC-DC converter, which is used to recharge the ultra-capacitor bank is not time critical as recharging is carried out when the main source is healthy. Hence, the analysis in this thesis will be focused entirely on the boost operation of the

interfacing DC-DC converter. Therefore, the converter will simply be referred to as a boost type DC-DC converter rather than a two quadrant DC-DC converter throughout this thesis.

This chapter presents a summarized literature review on the control characteristics of the above mentioned converters that are used frequently to interface ultra-capacitor banks. The main attention is given to the control to output transfer function and its pole-zero map. Moreover, it is well known that both the classical boost converter and the fly-back converter have a right half plane (RHP) zero in their control to output transfer functions when operated with continuous inductor current [8]. Due to this reason, both these converters show inverse response and also have a limited stable control bandwidth [67].

The tri-state boost converter is a recently proposed converter, which is capable of eliminating the RHP zero of the classical boost converter [68]. Hence it may be used as an alternative to the classical boost converter in situations where the RHP zero needs to be avoided. Therefore, this chapter also gives a summarized literature review on the tri-state boost converter.

Control techniques that are used to control DC-DC converters can be broadly categorized as voltage-mode (duty ratio) control and current-mode control [8]. Although not very popular as these two methods, sliding-mode control [69] is also another control method that is widely used to control DC-DC converters in some of the current applications. This chapter introduces these three control methods briefly in the latter sections.

Variable voltage sources such as ultra-capacitor banks are usually interfaced to ac loads that demand a constant voltage through a DC-DC converter and a Voltage source inverter (VSI). The DC-DC converter is used to regulate the dc link voltage of the VSI while the VSI transforms dc to ac. This is mainly because the conventional VSI is essentially a buck converter and hence it cannot boost the voltage when its dc link voltage is low [17]. However, the recently proposed Z-Source inverters is capable of performing both buck and boost operations, and therefore, is suitable for directly interfacing variable dc voltage sources such as

ultra-capacitor banks to ac loads. The final sections of this chapter introduce the Z-Source inverter and its operating principle.

3.2. Classical Boost Converter

Classical boost converter is the simplest DC-DC converter that can be used for voltage boosting applications [8, 26]. It is found in most regulated dc power supplies and regenerative braking of dc motors [1].

3.2.1 System Poles and Zeros

Fig. 3.1 illustrates the classical boost converter supplying a resistive load, which has widely been analyzed in a number of literature [1, 8, 26]. In these converters, the source E_b is a constant emf source with negligible internal resistance. E_b can be approximated by a battery in practice.

Fig. 3.1 Classical boost converter

In Fig. 3.1, X_1 and X_2 represents the current in the boost converter inductance (L_i) and the voltage across the output filter capacitance (C_f) respectively. The two resistances R_i and R_L represent the parasitic resistance of the boost inductor and the load resistance respectively.

Assuming the steady state duty ratio as d_0 , the steady state values of the two variables can be determined as [8],

$$\bar{X}_1 = E_b / (R_i + (1-d_0)^2 R_L), \quad \bar{X}_2 = \bar{V}_{dc} = \frac{E_b}{(1-d_0)} \left[1 / \left(1 + \frac{R_i}{(1-d_0)^2 R_L} \right) \right] \quad (3-1),$$

It is well known that this battery based classical boost converter contains a right half plane (RHP) zero in its duty ratio (control) to output voltage transfer function when operated with continuous inductor current [8]. The expressions for the duty ratio to output voltage transfer function $G_{Vdb}(s)$ and its RHP zero Z_{1b} are given in (3-2) and (3-3) respectively [8]. These transfer functions are derived from Middlebrook's state space averaging theory. The major steps of derivation are also given in Appendix A.

$$G_{Vdb_classic}(s) = \frac{-\bar{X}_1 \left[s - \left(\frac{\bar{X}_2(1-d_0) - R_i \bar{X}_1}{L_i \bar{X}_1} \right) \right]}{C_f \left[s^2 + \left(\frac{R_i}{L_i} + \frac{1}{C_f R_L} \right) s + \left(\frac{(1-d_0)^2}{L_i C_f} + \frac{R_i}{L_i C_f R_L} \right) \right]} \quad (3-2)$$

$$Z_{1b_classic} = (\bar{X}_2(1-d_0) - R_i \bar{X}_1) / (L_i \bar{X}_1) \quad (3-3)$$

Using (3-1), the RHP zero position may also be written as,

$$Z_{1b_classic} = ((1-d_0)^2 R_L - R_i) / L_i \quad (3-4)$$

Therefore, it is clear that the system RHP zero depends on the operating duty ratio of the boost converter. Since the battery emf, E_b , is fixed, d_0 will remain constant when supplying a load demanding a constant voltage V_{dc} . Therefore, if the load is also constant, then the position of the RHP zero will remain constant for a given battery based boost converter and for a given load.

The poles of the battery based classical boost converter can be derived from the denominator of (3-2) as,

$$P_{1b_classic}, P_{2b_classic} = -\frac{1}{2} \left(\frac{R_i}{L_i} + \frac{1}{C_f R_L} \right) \pm \frac{1}{2} \sqrt{\left(\frac{R_i}{L_i} - \frac{1}{C_f R_L} \right)^2 - 4 \left(\frac{(1-d_0)^2}{L_i C_f} \right)} \quad (3-5)$$

In most practical converters, the term within the square root sign in (3-5) is negative and hence $P_{1b_classic}$ and $P_{2b_classic}$ form a complex conjugate pair, with a negative real part. Hence the system is seen to be stable.

Relative positions of these poles and zeros are illustrated in Fig. 3.2 below.

Fig. 3.2. Pole-zero map for classical boost converter

Note, however, that the two poles in (3-5) become real and the zero moves to the LHP when $d_0 \cong 1$, which is the condition used to derive some of the approximate equations in

Chapter 4. The two poles are then seen to be located approximately at $-\frac{R_i}{L_i}$ and $-\frac{1}{C_f R_L}$.

3.2.2 RHP Zeros in Control to Output Transfer Function

The RHP zeros in the control (duty ratio) to output voltage transfer function impose fundamental limitations on the control bandwidth [67, 70-73], as they force an upper limit on the achievable gain cross over frequency for stable operation [67, 73]. Moreover, the RHP

zeros cause inverse response [74, 75] and complicate the control system designs [76-79].

It is shown in [67] that for systems with one RHP zero at z , which lies significantly away from the system poles, the maximum achievable gain cross over frequency ω_{gc} of the open-loop compensated system is limited to (Appendix F),

$$\omega_{gc} \leq z \tan \alpha \quad (3-6)$$

where $\alpha = \frac{\pi}{2} - \frac{\varphi_m}{2} + n_{gc} \frac{\pi}{4}$, φ_m = phase margin in radians, n_{gc} = slope of the Bode plot of compensated minimum phase part of control to output voltage transfer function at ω_{gc} . Typically, for minimum phase systems $-1.7 < n_{gc} < -1.3$. However, with non minimum phase systems slightly higher values are used such as $n_{gc} = -0.5$ or $n_{gc} = -1$ [67].

These limitations associated with the RHP zero impose restrictions on the performance of the battery based classical boost converter described above [8]. Therefore, if the performance of the boost converter is to be improved, these restrictions should be minimized by utilizing suitable means.

As seen from (3-6), the effect of RHP zeros on the controller bandwidth become more severe as the RHP zero approaches the origin [67]. Therefore, if the RHP zero can be pushed towards positive infinity by proper selection of the system parameters, then the effect of the RHP zero can be minimized. As can be seen from (3-4), this can be achieved by reducing L_i [80].

However, reducing L_i increases the inductor current ripple and thereby the converter losses.

Alternatively, the system performance can also be improved by eliminating the RHP zero from the system altogether. Several techniques can be employed to achieve this objective.

Although it is not seen from (3-4), since it is derived from small signal approximations, reducing the switching period (T_s) of the converter is capable of pushing the zero from the RHP to the LHP, as described using injected absorbed current (IAC) model in [80].

For this, the necessary condition is,

$$\frac{2L_i}{R_L d_0 (1-d_0)^2} > T_s > \frac{2L_i}{R_L (2-d_0)(1-d_0)^2} \quad (3-7)$$

Another technique that can be used to eliminate the RHP zero is the leading edge modulation of output voltage [81]. However, this method requires the equivalent series resistance of the filter capacitance (R_f) to be larger than a minimum value [80, 81] so that,

$$R_f C_f > \frac{L_i}{R_L (1-d_0)} \quad (3-8)$$

The switching ripple also must not be integrated by the control loop to achieve the desired objective in this method [81].

Therefore, both the above methods tend to increase the power losses of the boost converter and the magnitudes of L_i and C_f [81, 82].

Another method that can be used is the operation of the boost converter in discontinuous conduction mode. However, while this does not address the problem of the RHP zero in continuous conduction mode, it increases the system losses and reduces the converter efficiency [68].

The recently proposed tri-state boost converter [68], is capable of eliminating the RHP zero of the continuous current boost converter avoiding most of the above disadvantages.

3.3. Tri-State Boost Converter

The schematic diagram of one form of the tri-state boost converter [68] is given below.

Fig. 3.3 Tri-state boost converter

As explained above, the classical boost converter exhibits inverse response [67, 83] due to its RHP zero in the control (duty ratio) to output voltage transfer function. i.e., whenever the duty ratio is increased to boost the load voltage, the output capacitor discharging period is increased resulting in an initial drop of load voltage until the inductor current is built up sufficiently to recharge the output capacitor [68].

The tri-state boost converter in Fig. 3.3 has an additional control freedom compared to the classical boost converter since it has two controlled switches compared to the one in the classical boost converter. The two states that can be obtained with both T_m and T_f on and with both T_m and T_f off are the switch on (boost) state and the switch off (capacitor charging) state of the classical boost converter. The third state of the tri-state boost converter is obtained by turning on T_f and turning off T_m . This forces the current in the inductor L_i to freewheel through the diode D_f .

These three states of the tri-state boost converter are known as the boost interval (when both T_f and T_m are on), the capacitor charging interval (when both T_f and T_m are off) and the freewheeling interval (when T_f on and T_m off). If the duty ratios of the three intervals are taken as d_b , d_o and d_f respectively, then it is seen that,

$$d_f + d_b + d_o = 1 \quad (3-9)$$

The steady state of the tri-state boost converter can be obtained from state space averaging [8, 28] as,

$$\bar{X}_1 = \frac{(d_b + d_o)}{(R_i + d_o^2 R_L)} E_b \text{ and } \bar{V}_{dc} = \bar{X}_2 = \frac{(d_b + d_o)}{(R_i + d_o^2 R_L)} d_o R_L E_b \quad (3-10)$$

From (3-9) and (3-10) it is seen that if $d_f = 0$, then the tri-state boost converter will approach the classical boost converter.

As can be seen from (3-9), the three state operation allows changing the boost interval, $d_b T_s$, without affecting the capacitor charging interval, $d_o T_s$, by suitably varying the freewheeling interval $d_f T_s$, where T_s represents the switching period. This results in the absence of the RHP zero in the tri-state boost converter.

The control (boost interval duty ratio) to load voltage transfer function for the tri-state boost converter can be derived using the guidelines described in [68] as,

$$G_{Vdb_3state}(s) = \frac{\tilde{V}_{dc}(s)}{\tilde{d}_b(s)} = \frac{d_o E_b}{L_i C_f \left[s^2 + \left(\frac{1}{R_L C_f} + \frac{R_i}{L_i} \right) s + \left(\frac{d_o^2}{L_i C_f} + \frac{R_i}{R_L L_i C_f} \right) \right]} \quad (3-11)$$

Note that the RHP zero is eliminated from the transfer function. Comparing denominators of (3-2) and (3-11) it can also be seen that the poles of the tri-state boost converter coincide with the poles of the classical boost converter if $d_f = 0$. The two poles of the tri-state boost converter are located at,

$$P_{1b_3state}, P_{2b_3state} = -\frac{1}{2} \left(\frac{R_i}{L_i} + \frac{1}{C_f R_L} \right) \pm \frac{1}{2} \sqrt{\left(\frac{R_i}{L_i} - \frac{1}{C_f R_L} \right)^2 - 4 \left(\frac{d_o^2}{L_i C_f} \right)} \quad (3-12)$$

Similar to the classical boost converter, these two poles are also complex conjugates in most practical tri-state boost converters.

3.4. Fly-Back Converter

The classical boost converter or the tri-state boost converter mentioned above does not provide galvanic isolation between the load and the input source. Hence, the fly-back converter is also widely considered in ultra-capacitor applications where the galvanic isolation is required.

Fly-back converters are derived from the buck boost converter by placing a second winding on the buck boost converter inductance [1]. By this way it is possible to have galvanic isolation between the load and the source. The schematic diagram of the fly-back converter is given below in Fig. 3.4.

Fig 3.4 Fly-back converter

In Fig. 3.4, L_m represents the magnetizing inductance of the two winding inductor while $N_1:N_2$ represents its turns ratio.

The duty ratio to load voltage transfer function and the steady state relationships of the fly-back converter can be derived using the guidelines described in [1, 28] as shown below in (3-13) and (3-14). The turns ratio for the two winding inductor is assumed to be unity when deriving this transfer function.

$$G_{Vdb_flyback}(s) = \frac{-\bar{X}_1 \left[s - \left(\frac{(\bar{X}_2 + E_b)(1-d_0) - R_i \bar{X}_1}{L_m \bar{X}_1} \right) \right]}{C_f \left[s^2 + \left(\frac{d_0 R_i}{L_m} + \frac{1}{C_f R_L} \right) s + \left(\frac{(1-d_0)^2}{L_m C_f} + \frac{d_0 R_i}{L_m C_f R_L} \right) \right]} \quad (3-13)$$

$$\bar{X}_1 = \frac{d_0}{d_0 R_i + (1-d_0)^2 R_L} E_b, \quad \bar{X}_2 = \frac{d_0 (1-d_0) R_L}{d_0 R_i + (1-d_0)^2 R_L} E_b \quad (3-14)$$

Fly-back converters also contain a RHP zero in their control to output transfer function as can be observed from (3-13). Hence they also have a limited control bandwidth and inverse response as discussed in section 3.2 for classical boost converters.

From (3-13) and (3-14), the position of the fly-back converter RHP zero can be derived as,

$$Z_{lb_flyback} = \frac{(1-d_0)^2 R_L - d_0^2 R_i}{L_m d_0} \quad (3-15)$$

while the poles of the system can be derived as,

$$P_{1b_flyback}, P_{2b_flyback} = -\frac{1}{2} \left(\frac{d_0 R_i}{L_m} + \frac{1}{C_f R_L} \right) \pm \frac{1}{2} \sqrt{\left(\frac{d_0 R_i}{L_m} + \frac{1}{C_f R_L} \right)^2 - 4 \left(\frac{(1-d_0)^2}{L_m C_f} + \frac{d_0 R_i}{L_m C_f R_L} \right)} \quad (3-16)$$

These two poles can also be complex in most practical systems similar to the classical boost converter poles given in (3-5).

The effects of the RHP zero given in (3-15) can be minimized by adopting the techniques discussed in section 3.2.2. Moreover, it is also possible to eliminate the fly-back converter RHP zero by adopting the leading edge modulation technique [81] discussed in the same section.

3.5. Control of DC-DC Converters

Among the many control methods that have been proposed and analyzed for DC-DC converters, the most popular are voltage-mode control (duty ratio control) and current

programmed control (current-mode control) [8]. Current-mode control is further divided into two categories as peak current-mode control and average current-mode control [8, 84]. In peak current-mode control, the peak switch current or the peak inductor current is controlled while in average current-mode control it is the average inductor current which is controlled. The main reasons for the popularity of these methods are the simple design and simple implementation procedures [8, 69].

3.5.1 Voltage-mode Control

In voltage-mode control (duty ratio control), only the converter output voltage is sensed, which is then compared with a reference voltage to produce the error signal that is fed to a compensator to adjust the converter duty ratio. Therefore, the converter output voltage is directly controlled by controlling the duty ratio in voltage-mode control [8]. The schematic diagram of voltage-mode control applied to a classical boost converter is given below.

Fig 3.5. Schematic diagram of voltage-mode control of classical boost converter

If the compensator $G_{cd}(s)$ is only a gain, then it is seen that voltage-mode control does not alter the pole-zero pattern of the open loop transfer functions of the converter [8]. This is because the voltage-mode control structure, shown in Fig 3.5 above, is only capable of modifying the gain of the original plant transfer functions. Hence for the classical boost converter, shown above in Fig 3.5, the pole-zero pattern of the control to output transfer function will be the same as the pole-zero pattern discussed in section 3.2.1.

3.5.2 Current-mode Control

In current-mode control either a switch current or an inductor current is measured in addition to the output voltage. Therefore, current-mode control has two feedback loops, an outer voltage loop and an inner current loop, operating in cascade. The schematic diagram for peak current-mode control is shown in Fig 3.6. The outer voltage loop produces the reference for the inner current loop which sets the switching times directly. A simple control network switches the transistor on and off such that the peak transistor current or the inductor current follows the reference as shown in Fig 3.6 [8]. Therefore, the converter duty cycle is not directly controlled but depends on the reference current and other currents and voltages of the converter [8].

Fig. 3.6 Schematic diagram of peak current-mode control of classical boost converter

Current-mode control has several advantages over the simpler voltage-mode control described earlier [8]. One of the main advantages is the simple first order response compared to the second order response of the voltage-mode control. Another advantage is the inbuilt over-current protection since the switch current or the inductor current is being controlled [8]. A major problem that is associated with current-mode controlled converters is the sub-harmonic oscillation that occurs for duty ratios larger than 0.5 [8, 84]. However, although difficult, this problem can be solved by employing an external ramp (m_a) in peak current-mode control [8], as shown in Fig 3.6, or using a suitable gain in the current loop in average current-mode control [84].

For peak current-mode control, the controller model can be developed as described in [8], considering the relationship between the control input I_c , and the inductor current X_1 as,

$$X_1 = I_c - m_a d T_s - (m_1 d^2 T_s / 2) - (m_2 (1-d)^2 T_s / 2) \quad (3-17)$$

Where T_s represent the switching period, while $m_1 = V_g / L_i$ and $m_2 = -(V_g - X_2) / L_i$. Note that $V_g = E_b - R_i X_1$.

The small signal current-mode controller model can be found by perturbation and linearization of (3-17) as described in [8]. The result is given below in (3-18). Note that m_a and T_s are not perturbed as they are assumed constant.

$$\tilde{d}(s) = F_m [\tilde{i}_c(s) - \tilde{X}_1(s) - F_g \cdot \tilde{V}_g(s) - F_v \cdot \tilde{X}_2(s)] \quad (3-18)$$

Where,

$$F_g = [T_s (2d_0 - 1) / (2L_i)], \quad F_v = [(1-d_0)^2 T_s / (2L_i)], \quad F_m = 1 / [m_a T_s] \quad \text{and}$$

$\tilde{V}_g(s) = E_b(s) - R_i \tilde{X}_1(s)$ is the input dc voltage for the boost converter.

The relationship given in (3-18) is shown within the dashed lines in Fig 3.7. However, when the parasitic resistance of the inductor, R_i , is included, the block diagram can be completed for the system shown in Fig 3.6 as given in Fig 3.7.

Fig. 3.7 small signal open loop control block diagram for peak current-mode control

Hence the open loop control to output transfer function in peak current-mode control can be shown to be given by [8],

$$G_{V_c}(s) = \frac{\tilde{X}_2(s)}{\tilde{i}_c(s)} = \frac{F_m G_{V_d}(s)}{1 + F_m (G_{X_{1d}}(s) + F_v G_{V_d}(s))} \quad (3-19)$$

Therefore, since the numerator of G_{V_c} contains G_{V_d} , the current-mode control does not affect the open loop zeros of the control to output transfer function of the original system. However, it is seen to modify the denominator and hence the positions of system poles. As it is well known, this modification results in pushing the pole resulting from inductor L_i to very high frequencies [8]. Hence, the peak current-mode controlled DC-DC converters are known to exhibit first order responses compared to the second order responses of voltage-mode controlled converters.

The parameters of both voltage-mode and current-mode control methods depend on the operating point. Moreover, achieving large signal stability is difficult without affecting the system performance in these control methods. Furthermore, the design and stabilization of the system becomes more complex when applied to higher order converters such as cuk or sepic converters [69]. Therefore, in cases where these problems need to be avoided, sliding-mode control can be employed instead of voltage-mode or current-mode control to control DC-DC converters [69, 85, 86].

3.5.3 Sliding-mode Control

Sliding-mode control is based on control techniques derived from variable structure theory described in [87]. In general sliding-mode control theory, all system state variables are sensed and the corresponding error signals with respect to their steady state values, are multiplied by suitable gains and added together to form the sliding function. Then, a hysteresis block keeps this sliding function near zero by switching the converter switching device on and off [85].

This means the general sliding-mode control acts on all system states simultaneously and tries to bring them all to the steady state. This behavior leads to fast response in sliding-mode controlled systems compared to voltage-mode or current-mode controlled systems. Moreover, reduced order sliding-mode controllers, i.e. sliding-mode controllers utilizing only some of the system states, are also shown to possess equally good system properties [69]. The main disadvantages of the sliding mode control are the chattering and variable frequency switching [67]. However, these problems can be easily avoided by utilizing suitable means [67].

The derivation of small signal transfer functions for sliding-mode controlled DC-DC converters is illustrated in Appendix D1 [85].

3.6. Z-Source Inverter

The Z-Source inverter is a recently introduced power converter that is capable of directly interfacing a variable DC voltage source to an ac load demanding a constant voltage at its terminals, without the use of a separate DC-DC converter [17, 88]. Therefore, the Z-Source inverter shows considerable promise for future ultra-capacitor based power quality applications.

The principle of Z-Source converter, in general, can be applied to all types of converters such as, DC to AC, AC to DC, AC to AC and DC to DC. Furthermore, it can be applied to both voltage source or current source converters [17]. However, the Z-Source inverter given in Fig 3.8 is the most researched type of converter up to now.

Fig 3.8 Voltage source Z-Source inverter

The Z-Source inverter (ZSI) differs from the conventional voltage source inverter (VSI) due to the presence of the impedance network and diode D_s as shown in Fig. 3.8. The impedance network shown, changes the circuit configuration from that of a voltage source to an impedance source (i.e. Z-Source). The inductive and capacitive elements in the impedance network need not necessarily be identical as shown in the symmetrical impedance network in Fig 3.8 [17]. However, almost all the work reported in literature uses symmetrical impedance networks for convenience.

The presence of this unique impedance network allows the ZSI to be operated in a new circuit state called the shoot through state in which both the switching devices on a single VSI leg are switched on to effect a short circuit of the dc link. During this state, energy is transferred from the capacitors to the inductors in the impedance network, thereby giving rise to the voltage boosting capability of the ZSI. Since the conventional VSI is capable of performing buck operation, the Z-Source inverter shown in Fig. 3.8 can be operated as a buck or boost inverter [17]. It is due to this buck-boost capability that the ZSI is suitable for direct interfacing of variable voltage sources to constant voltage ac loads.

Currently, available literature on ZSI [17, 30, 88, 89] mainly focuses on how to control the switching devices of the VSI, with the additional degree of freedom brought in by the shoot-through state. However little or no effort have been made to study the operating states of the impedance network and to provide any guidelines to size its components.

In this thesis a detailed analysis of the steady state operation of the ZSI is carried out in order to provide design guidelines for the sizing of the impedance network.

3.7 Summary

The most common types of DC-DC converters used for ultra-capacitor based applications are the classical boost converter and the fly-back converter. It is well known that the battery based

(constant emf) classical boost converter and the fly-back converter contain a RHP zero in their duty ratio to output voltage transfer functions in continuous inductor current-mode. Both of these converters therefore, show inverse response and a limited control bandwidth [67, 90]. It is possible to eliminate the RHP zero from the transfer functions of both these converters by adopting the leading edge modulation described in [81]. However this technique requires maintaining the equivalent series resistance of the output filter capacitor (R_f) above a minimum value. In some cases, additional resistance may need to be added to meet this requirement. This increases the circuit losses as well as the ripple of the output load voltage. Moreover, the success of the method depends on the accuracy of the estimation of R_f , which is dependant on the temperature [68]. The tri-state boost converter, described in [68], is capable of eliminating the RHP zero of the classical boost converter, without these disadvantages. It achieves this objective by introducing a third circuit state to the existing classical boost converter after a simple modification to the circuit. However the additional circuit state introduces additional power losses and hence the tri-state boost converter efficiency is seen to be lower than that of the classical boost converter [91]. Furthermore, the generation of switching signals also becomes more complex.

This chapter also briefly explored the methods that are used to control DC-DC converters. Currently, the most popular control methods are voltage-mode control and current-mode control [8]. In voltage-mode control, only the output load voltage is used as the feedback signal while in current-mode control the switch current or an inductor current is also used in addition to the measured voltage signal. Compared to voltage-mode control, the current-mode controlled DC-DC converters show simple first order system dynamics and hence are generally preferred [8]. A major disadvantage of both voltage-mode and current-mode controlled systems is the dependence of the designed controllers on the system parameters.

Although not as popular as voltage-mode and current-mode control, sliding-mode control is another control method that can be applied to control DC-DC converters [69, 92, 93]. Sliding-mode control is derived from the variable structure systems theory [87], and it complies with the non-linear nature of the DC-DC converters. Sliding-mode control has several advantages such as large signal stability, good dynamic response and robustness [69].

Finally this chapter introduced the Z-Source inverter [17], which is a new power converter introduced during recent years. Unlike the conventional voltage source or current source inverters, which can only operate as buck or boost converters, the Z-Source inverters are capable of operating as buck-boost converters [17]. This unique feature makes them ideally suited to directly interface variable voltage or current sources to ac loads without using a separate DC-DC converter in between. Hence the Z-Source inverters show considerable promise towards future ultra-capacitor based power quality applications.

The next chapter analyses the operation of these DC-DC converters with a bank of ultra-capacitors as the dc source. The effect of the variable dc source on the control characteristics is the main focus in this analysis.

CHAPTER 4

CAPACITOR BASED POWER CONVERTERS

4.1 Introduction

As discussed in Chapter 3, the power converters operating with batteries with a constant emf have been widely analyzed in the literature [1, 4, 8, 27]. However the same has not been done for power converters supplied by capacitors. This may be because the capacitors did not have sufficient energy density to use them widely as power sources for converters until the recent development of the ultra-capacitors.

Unlike the constant emf batteries used in the analysis presented in Chapter 3, the terminal voltage of the capacitors continuously decreases when they are used to power a load. (It should be noted that the emf of the batteries also decrease with time, but the decrease is negligible in the useful operating period). Therefore, in order to maintain a constant voltage at the load, the duty ratio of a DC-DC converter should be continuously adjusted against the variation of the capacitor terminal voltage. This means that a capacitor based power converter should always be operated with closed loop control when the load voltage needs to be kept constant. However, the open loop behaviour discussed in this chapter also gives valuable insight into the properties of capacitor based converters.

One of the main differences between constant emf battery based power converters and capacitor based power converters is the steady state behaviour. While the former reaches a clear steady state after initial transients, the latter does not show such a steady state. In fact the capacitor based systems do not have a steady state in strict terms because its terminal voltage will be always decreasing during its useful operating period. However, if this terminal voltage decay is small, then an approximate steady state may be assumed by treating the capacitor

voltage as constant for a small period of time. The transfer functions for the capacitor based systems are derived using small signal perturbation around this steady state.

It should be noted that the same transfer function expressions can be obtained by assuming a linear decay of the capacitor terminal voltage as discussed under the ‘second method’ in Appendix A3. However, the steady state values, X_0 , derived from the two methods are different. Nevertheless, from (A3-10), this difference in X_0 values are seen to be due to the rate of change of state variables (k_1, k_2, k_3 and k_4), as the capacitor terminal voltage decays with time. Therefore, if the magnitude of these rates are small, then both methods results in almost the same transfer functions for the system. Moreover, the small difference in X_0 values only affect the positions of zeros and the gain of the transfer function. It does not affect the positions of poles. Therefore, the transfer functions for the capacitor based systems analyzed in this thesis will be derived from the first method given in appendix A3, for simplicity.

This chapter analyses the control characteristics, such as poles and zeros of the transfer functions, for the three DC-DC converters discussed in Chapter 3, when supplied by capacitors. These converters are the classical boost converter, fly-back converter and the tri-state boost converter. The results of the analysis are then compared with the results of the equivalent constant emf battery based converters discussed in Chapter 3.

4.2. Capacitor Based Classical Boost Converter

The classical boost converter operating with capacitors and supplying a resistive load is given in Fig 4.1. Note that in this analysis the terminal voltage of the energy storing capacitor bank is denoted as X_1 , the inductor current is denoted as X_2 and the output filter capacitor voltage is denoted as X_3 . The capacitance of the energy storing capacitor bank is taken as C_{uc} . The

equivalent series parasitic resistance of both capacitor bank and the boost converter inductance is denoted as R_i .

Fig 4.1. Capacitor based classical boost converter operating with a resistive load

The transfer functions for this standalone system are derived using Middlebrook's steady state averaging theory [28] as shown in Appendix A. The resulting expressions for system steady state and the control to output transfer function are given in (4-1) to (4-3).

Note that, the steady state given is strictly valid only at the initial state of a charging or discharging process of the capacitor bank. However, if the rate of decay of capacitor voltage is small or linear, it can be used to describe a steady state for the capacitor based converter at any stage of charging / discharging for a small time period without much error, as shown in appendix A3.

$$\bar{X}_2 = \bar{X}_1 / (R_i + (1-d_0)^2 R_L) \quad (4-1)$$

$$\bar{X}_3 = \bar{V}_{dc} = \frac{\bar{X}_1}{(1-d_0)} \left[1 / \left(1 + \frac{R_i}{(1-d_0)^2 R_L} \right) \right] \quad (4-2)$$

$$G_{Vdu}(s) = \frac{-\bar{X}_2 \left[s^2 - \left(\frac{\bar{X}_3(1-d_0) - R_i \bar{X}_2}{L_i \bar{X}_2} \right) s + \frac{1}{C_{uc} L_i} \right]}{C_f \left[s^3 + \left(\frac{R_i}{L_i} + \frac{1}{C_f R_L} \right) s^2 + \left(\frac{(1-d_0)^2}{L_i C_f} + \frac{1}{L_i C_{uc}} + \frac{R_i}{L_i C_f R_L} \right) s + \frac{1}{C_{uc} L_i C_f R_L} \right]} \quad (4-3)$$

4.2.1 System RHP Zeros

From the numerator of (4-3) it is seen that the system has two RHP zeros and they are located at,

$$Z_{1u_classical} = [(\bar{X}_3(1-d_0) - R_i \bar{X}_2)/(2L_i \bar{X}_2)] - (Z_d / 2) \quad (4-4)$$

$$Z_{2u_classical} = [(\bar{X}_3(1-d_0) - R_i \bar{X}_2)/(2L_i \bar{X}_2)] + (Z_d / 2) \quad (4-5)$$

Where, $Z_d = \sqrt{[(\bar{X}_3(1-d_0) - R_i \bar{X}_2)/(2L_i \bar{X}_2)]^2 - [1/(L_i C_{uc})]}$

For Z_d to be real, C_{uc} should be large enough to satisfy the inequality,

$$C_{uc} > L_i [(2\bar{X}_2)/(\bar{X}_3(1-d_0) - R_i \bar{X}_2)]^2 \quad (4-6)$$

For high capacitance ultra-capacitor based systems, this inequality is normally satisfied and hence both the zeros given in (4-4) and (4-5) are found as real.

From the two zeros given in (4-4) and (4-5), $Z_{1u_classical}$ given in (4-4), is seen to have a much smaller magnitude compared to $Z_{2u_classical}$, given in (4-5). This is because C_{uc} is very high, in the range of Farads, for the high capacitance capacitor banks considered in this analysis. Hence $Z_{1u_classical}$ is seen to be located closer to the origin than $Z_{2u_classical}$. Therefore, $Z_{1u_classical}$ represents the dominant RHP zero of the capacitor based classical boost converter. The expression of $Z_{1u_classical}$, given in (4-4), can be further simplified using (4-1) and (4-2) as,

$$Z_{1u} = Z_{1u_classical} = p - p \sqrt{1 - \frac{1}{C_{uc} L_i p^2}} \quad (4-7)$$

$$\text{where, } p = \frac{\bar{X}_3(1-d_0) - R_i \bar{X}_2}{2L_i \bar{X}_2} = \frac{(1-d_0)^2 R_L - R_i}{2L_i}$$

$$\text{Moreover, } \frac{1}{C_{uc} L_i p^2} = \frac{4L_i}{C_{uc} [(1-d_0)^2 R_L - R_i]} \quad (4-8)$$

In practical classical boost converter systems, L_i is in the range of few milli Henries and

$[(1-d_0)^2 R_L - R_i]$ is in the range of several Ohms. Therefore, the term $\frac{1}{C_{uc} L_i p^2}$ given in (4-8) is in the order of L_i and therefore, it is much less than 1 in general.

Therefore, by using the approximation $\sqrt{1-x} \cong 1 - \frac{x}{2}$ for $x \ll 1$, (4-7) can be simplified further as,

$$Z_{1u} = Z_{1u_classical} \cong \frac{1}{C_{uc} [(1-d_0)^2 R_L - R_i]} \quad (4-9)$$

Therefore, apart from R_L and R_i , the low frequency RHP zero, i.e. the dominant RHP zero, of the capacitor based classical boost converter depends on the capacitance of the capacitor bank. It also depends on the duty ratio d_0 at the selected steady state operating point of the capacitor based classical boost converter, which in turn depends on the terminal voltage of the capacitor bank. As the terminal voltage of the capacitor bank decreases, d_0 has to be increased. This results in Z_{1u} moving away from the origin.

4.2.2 System Poles

It is not convenient to derive similar simple expressions for the system poles from the denominator of (4-3). However if the three system poles are taken as α_1 , α_2 and α_3 then the following relationships can be derived as shown in the Appendix E from the coefficients of the denominator.

$$\alpha_1 + \alpha_2 + \alpha_3 = -\left(\frac{R_i}{L_i} + \frac{1}{C_f R_L}\right) \quad (4-10)$$

$$\alpha_1 \alpha_2 + \alpha_1 \alpha_3 + \alpha_2 \alpha_3 = \left(\frac{(1-d_0)^2}{L_i C_f} + \frac{1}{L_i C_{uc}} + \frac{R_i}{L_i C_f R_L}\right) \quad (4-11)$$

$$\alpha_1 \alpha_2 \alpha_3 = -\frac{1}{C_{uc} L_i C_f R_L} \quad (4-12)$$

Comparing (4-11) and (4-12), it is seen that in most practical converters, $(\alpha_1\alpha_2 + \alpha_1\alpha_3 + \alpha_2\alpha_3) > \alpha_1\alpha_2\alpha_3$. This is because C_f and L_i represent very small values (C_f is mostly in micro Farads range and L_i is in milli Henry range), while C_{uc} and R_L represent high values in the range of Farads and Ohms. From the denominator of (3-2), it can be seen that for the constant emf battery based system, the summation of the two poles are given by

$$-\left(\frac{R_i}{L_i} + \frac{1}{C_f R_L}\right) \text{ while the product of the two poles are given by } \left(\frac{(1-d_0)^2}{L_i C_f} + \frac{R_i}{L_i C_f R_L}\right).$$

Therefore, it is seen that the additional pole added due to C_{uc} in the capacitor based system does not change the summation of the poles but it slightly increases the summation of the double pole product given in (4-11). Moreover, the product of all three poles in capacitor based system given in (4-12) is seen to be less than the product of the two poles in the constant emf battery based system. This behaviour suggests that the additional pole added in the capacitor based system is located very close to the origin.

Therefore, the pole-zero map of the capacitor based classical boost converter will approximately be as shown below in Fig 4.2.

Fig. 4.2. Typical pole-zero map of a capacitor based classical boost converter (not to scale)

4.2.3 Approximate System Poles

If $d_0 \cong 1$ is assumed, then the following approximate expressions can be derived for the three system poles from the denominator of (4-3),

$$P_{1u} = P_{1u_classical} \cong \frac{-R_i}{2L_i} + \sqrt{\left(\frac{R_i}{2L_i}\right)^2 - \left(\frac{1}{L_i C_{uc}}\right)} \quad (4-13)$$

$$P_{2u} = P_{2u_classical} \cong \frac{-R_i}{2L_i} - \sqrt{\left(\frac{R_i}{2L_i}\right)^2 - \left(\frac{1}{L_i C_{uc}}\right)} \quad (4-14)$$

$$P_{3u} = P_{3u_classical} \cong -\frac{1}{C_f R_L}, \quad (4-15)$$

For high capacitance ultra-capacitor based systems, the term within the square root sign in (4-13) and (4-14) is positive. This is because C_{uc} is typically in the Farads range while R_i has a magnitude of several hundreds of miliOhms. Therefore, since C_f is in microFarads and L_i is in milliHenries, P_{2u} and P_{3u} in (4-14) and (4-15) will have a reasonably high magnitude compared to P_{1u} in (4-13). Furthermore, P_{1u} is seen to be located very close to the origin since its magnitude is very small due to the high capacitance of C_{uc} . The exact position of the dominant pole $P_{1u_classical}$ is conveniently obtained only with numerical results. However an approximate position for $P_{1u_classical}$ may be obtained as described in Appendix E3, since $P_{1u_classical}$ is much smaller in magnitude compared to other poles in the system. This approximate position of $P_{1u_classical}$ may be obtained by taking the limiting value of (E4-1) when $L_s \rightarrow \infty$ and substituting $L_L = 0$.

$$P_{1u_classical} = \frac{-1}{((1-d_0)^2 R_L + R_i)C_{uc} + C_f R_L} \quad (4-16)$$

Since C_f is very small, (4-16) may be further simplified to,

$$P_{1u_classical} = \frac{-1}{((1-d_0)^2 R_L + R_i) C_{uc}} \quad (4-17)$$

From (4-9) and (4-17), it is seen that $P_{1u_classical}$ is slightly smaller than $Z_{1u_classical}$ for a standalone converter. Moreover, the difference between $P_{1u_classical}$ and $Z_{1u_classical}$ is seen to be due to the presence of R_i . Otherwise the two are identical.

Note that the poles that are denoted as P_{1u} , P_{2u} and P_{3u} correspond to the poles α_1 , α_2 and α_3 given above in section 4.2.2.

4.2.4 Comparison with the Constant emf Battery based system.

Comparing the pole-zero maps in Fig 3.2 and Fig 4.2, it is seen that the capacitor based classical boost converter contains an additional low frequency pole-zero pair very close to the origin in its control to output transfer function.

In fact, a battery with a constant emf may be assumed as a capacitor with infinite capacitance. By taking the limiting expressions when $C_{uc} \rightarrow \infty$, it can be seen that both P_{1u} and Z_{1u} in the capacitor based system moves to the origin, which effectively cancels each other out. Moreover, all other poles and zeros of the capacitor based system derived in (4-5), (4-14) and (4-15) moves to the corresponding positions of the constant emf battery based system, which were given in (3-3) and (3-5). Note that $d_0 \cong 1$ should be substituted in (3-5) to obtain the equivalent estimates for the poles of the battery based system that agrees with P_{2u} and P_{3u} .

This shows that the low frequency pole-zero pair, P_{1u} and Z_{1u} , exist in capacitor based systems due to the finite capacitance of the capacitor banks. Therefore, it is not possible to eliminate them entirely from the transfer functions of the capacitor based systems. The effects of this pole zero pair is further investigated in detail in Chapter 5.

4.3 Capacitor based tri-state boost converter

The tri-state boost converter operating with a capacitor bank and supplying a resistive load is shown in Fig. 4.3.

Fig 4.3 Capacitor based tri-state boost converter operating with a resistive load

The operation of the battery based tri-state boost converter and its ability to eliminate the RHP zero of the classical boost converter was discussed in section 3.3 of Chapter 3. Compared to the classical boost converter, the tri-state boost converter has one additional switching device and one additional diode, making it possible to operate the converter in three states as described in that section.

The state matrices for the capacitor based tri-state boost converter are given in Appendix C1. Expressions for the steady state of the system and the control to output transfer function, which are given below, are also derived in Appendix C1.

$$\bar{X}_2 = \frac{(d_{b0} + d_{o0})}{(R_i + d_{o0}^2 R_L)} \bar{X}_1 \quad (4-18)$$

$$\bar{V}_{dc} = \bar{X}_3 = \frac{(d_{b0} + d_{o0})}{(R_i + d_{o0}^2 R_L)} d_{o0} R_L \bar{X}_1 \quad (4-19)$$

$$G_{Vdu}(s) = \frac{\tilde{V}_{dc}(s)}{\tilde{d}_b(s)} = \left\{ \frac{d_{o0} \bar{X}_1 \left[s - \frac{\bar{X}_2 (d_{o0} + d_{b0})}{C_{uc} \bar{X}_1} \right]}{L_i C_f \left[s^3 + \left(\frac{1}{R_L C_f} + \frac{R_i}{L_i} \right) s^2 + \left(\frac{(d_{o0} + d_{b0})^2}{C_{uc} L_i} + \frac{d_{o0}^2}{L_i C_f} + \frac{R_i}{R_L L_i C_f} \right) s + \frac{(d_{o0} + d_{b0})^2}{C_{uc} L_i C_f R_L} \right]} \right\} \quad (4-20)$$

Note that d_{b0} represents the duty ratio of the boost interval and d_{o0} is the duty ratio of the output capacitor (C_f) charging interval.

4.3.1 System RHP Zeros

From the numerator of (4-20) it is seen that the tri-state boost converter has one RHP zero in the control to output transfer function of the capacitor based system, although the corresponding battery based system did not have any, as described in section 3.3 of Chapter 3.

The RHP zero is seen to be located at,

$$Z_{lu} = Z_{lu_tri-state} = \frac{\bar{X}_2 (d_{o0} + d_{b0})}{C_{uc} \bar{X}_1} \quad (4-21)$$

Using the steady state values given in (4-18) and (4-19), (4-20) may be further simplified as,

$$Z_{lu} = Z_{lu_tri-state} = \frac{(d_{b0} + d_{o0})^2}{C_{uc} [d_{o0}^2 R_L + R_i]} \quad (4-22)$$

Since the maximum possible value of $d_{o0} + d_{b0}$ is 1, it is seen that (4-22) represents a smaller value compared to (4-9). Therefore, it is seen that the tri-state boost converter pushes the low frequency RHP zero closer to the origin compared to the classical boost converter.

Hence, the tri-state boost converter is only capable of removing the high frequency RHP zero of the ultra-capacitor based system, which is the RHP zero closer to the RHP zero of a classical battery based boost converter. It is not capable of eliminating the low frequency RHP zero. However, the tri-state boost converter has influenced the position of the low frequency RHP

zero as it has moved it from the position given in (4-4) of the classical boost converter, to the position given in (4-21).

4.3.2 Approximate System Poles

To derive the approximate pole positions, assume that R_L is very large. Then the approximate pole positions are found as,

$$P_{1u} = P_{1u_tri-state} \cong 0 \quad (4-23)$$

$$P_{2u} = P_{2u_tri-state} \cong \frac{-R_i}{2L_i} + \sqrt{\left(\frac{R_i}{2L_i}\right)^2 - \left(\frac{(d_{o0} + d_{b0})^2}{C_{uc}L_i} + \frac{d_{o0}^2}{L_iC_f}\right)} \quad (4-24)$$

$$P_{3u} = P_{3u_tri-state} \cong \frac{-R_i}{2L_i} - \sqrt{\left(\frac{R_i}{2L_i}\right)^2 - \left(\frac{(d_{o0} + d_{b0})^2}{C_{uc}L_i} + \frac{d_{o0}^2}{L_iC_f}\right)} \quad (4-25)$$

Equation (4-23) to (4-25) suggests that the tri-state boost converter also has one pole very close to the origin while the other two are relatively far away from the origin. Therefore, the tri-state boost converter also has the low frequency pole-zero pair very close to the origin when it is operated with ultra-capacitors.

Note that, the poles in (4-24) and (4-25) form a complex conjugate pair in most practical applications.

Furthermore, an approximate expression for $P_{1u_tri-state}$ may be obtained from (4-20) as shown below, following the same procedure discussed in section 4.2.3.

$$P_{1u} = P_{1u_tri-state} = \frac{-(d_{b0} + d_{o0})^2}{C_{uc}[d_{o0}^2 R_L + R_i] + C_f R_L (d_{b0} + d_{o0})^2} \quad (4-26)$$

Comparing (4-22) and (4-26), it can be seen that $P_{1u_tri-state}$ is slightly smaller than $Z_{1u_tri-state}$.

Since $d_{b0} + d_{o0}$ is less than 1, it can also be seen that $P_{1u_tri-state}$ is smaller than $P_{1u_classical}$.

4.3.3 Exact System Poles

Deriving simple expressions for the exact poles is again difficult. However if the poles of the system are taken as β_1 , β_2 and β_3 then the following relationships can be derived from the denominator of (4-20).

$$\beta_1 + \beta_2 + \beta_3 = -\left(\frac{R_i}{L_i} + \frac{1}{C_f R_L}\right) \quad (4-27)$$

$$\beta_1\beta_2 + \beta_1\beta_3 + \beta_2\beta_3 = \left(\frac{(d_{o0} + d_{b0})^2}{C_{uc}L_i} + \frac{d_{o0}^2}{L_i C_f} + \frac{R_i}{R_L L_i C_f}\right) \quad (4-28)$$

$$\beta_1\beta_2\beta_3 = -\frac{(d_{o0} + d_{b0})^2}{C_{uc}L_i C_f R_L} \quad (4-29)$$

Note that the poles that are denoted as β_1 , β_2 and β_3 corresponds to the poles given in (4-23) to (4-25).

Comparing (4-10) to (4-12) with (4-27) to (4-29), it is seen that,

$$|\beta_1 + \beta_2 + \beta_3| = |\alpha_1 + \alpha_2 + \alpha_3| \quad (4-30)$$

$$|\beta_1\beta_2 + \beta_1\beta_3 + \beta_2\beta_3| < |\alpha_1\alpha_2 + \alpha_1\alpha_3 + \alpha_2\alpha_3| \quad (4-31)$$

$$|\beta_1\beta_2\beta_3| < |\alpha_1\alpha_2\alpha_3| \quad (4-32)$$

Therefore, under tri-state conditions the positions of the system poles have shifted, but the summation of the poles, given by (4-30), remains the same as that of the classical boost converter. However from the approximate pole positions derived above, it was seen that one of the poles represented by α_1 , α_2 and α_3 and β_1 , β_2 and β_3 is located very close to the origin (low frequency pole) while the other two poles are located further from the origin (high frequency poles). Considering the fact that the two high frequency poles are in most cases complex, the inequalities in (4-31) and (4-32) can only be met if the low frequency pole has shifted towards the origin while the two high frequency poles have shifted away from the

origin. More importantly, the shift in poles is seen to be very small since the summation of the poles remains the same as per (4-30).

Therefore, this result suggests that in the tri-state boost converter, the low frequency left half plane pole is located slightly closer to the origin than that of the classical boost converter.

4.3.4 Comment on the Low Frequency Pole-zero Pair Compared to Capacitor based classical boost converter

As shown above, the low frequency pole-zero pair in the capacitor based tri-state boost converter is located slightly closer to the origin compared to the capacitor based classical boost converter. However, the above analysis assumes same $\bar{X}_1$ for both tri-state boost converter and the classical boost converter. Although this may be true at the start of the converter operation, it does not hold during the converter operation. This is due to the difference in efficiencies of the two converters. The additional freewheeling state of the tri-state boost converter increases the tri-state boost converter losses and hence its efficiency is lower than that of the classical boost converter [91]. Therefore, the capacitor bank discharges faster when operating with a tri-state boost converter.

4.3.5 Numerical Results

Consider a numerical example with the following parameters for both the capacitor based tri-state and classical boost converters. Note that X_{10} represents the initial terminal voltage of the capacitor bank.

$$C_{uc} = 1F, \quad L_i = 2.4mH, \quad R_i = 0.5\Omega, \quad C_f = 2200\mu F, \quad R_L = 120\Omega, \quad V_{dc} (rated) = 650V, \\ X_{10} = 325V$$

These numerical values correspond to a boost converter having a load of about 3.5 kW. The value of the ultra-capacitor bank was selected as described in section 2.10, considering a

minimum useful ultra-capacitor terminal voltage of about 250 V and a ride through time of more than 6 seconds.

Initial duty ratios of the two can be obtained from (A3-10) in Appendix A and (4-18) and (4-19) as,

$$d_0 = 1 - \frac{\bar{X}_1}{2\bar{V}_L} \pm \sqrt{\frac{\bar{X}_1^2}{4\bar{V}_L^2} - \frac{R_i}{R_L}} \quad (\text{for classical boost converter}) \quad (4-33)$$

$$d_{b0} = \left(\frac{\bar{X}_3(R_i + d_{o0}^2 R_L)}{d_{o0} R_L \bar{X}_1} - d_{o0} \right) \quad (\text{for tri-state boost converter}) \quad (4-34)$$

As per (4-33) and (4-34) the converter duty ratios for the numerical calculations were performed as $d_0 = 0.51$ and $d_{b0} = 0.45$. Note that d_{o0} , in (4-34), was assumed as 0.43.

With these parameters, $P_{1u_classical} = -0.0342$, $Z_{1u_classical} = 0.0345$ and $P_{1u_tri-state} = -0.0338$, $Z_{1u_tri-state} = 0.0341$ (Exact positions). Therefore, although the tri-state boost converter pushes the low frequency pole and zero towards the origin, the shift is seen to be negligibly small and hence the improvement gained from the tri-state boost converter over the classical boost converter is negligible when it comes to the low frequency pole-zero pair.

When the approximate expressions given in (4-9), (4-17), (4-22) and (4-26) is used to calculate the above positions, the results are as follows.

$$P_{1u_classical} = -0.03412, Z_{1u_classical} = 0.0353, P_{1u_tri-state} = -0.0338, Z_{1u_tri-state} = 0.0341$$

Therefore, both the exact analysis and the approximate analysis results in almost the same positions for the low frequency pole zero pair.

4.4. Capacitor based fly-back converter

A Fly-back converter is another DC-DC converter, which is widely used to interface ultra-capacitor banks in some power quality applications [15]. Unlike the classical boost converter, a

fly-back converter is capable of offering galvanic isolation between the source and the load.

The schematic diagram of a capacitor based fly-back converter supplying a resistive load is given in Fig 4.4.

Fig 4.4. Capacitor based fly-back converter operating with a resistive load

In the above figure, L_m represents the magnetizing impedance of the two winding inductor of the fly-back converter.

The system state matrices for the capacitor based fly back converter are given in the Appendix C2. Similar to the cases described above, the steady state and the open loop control to output transfer function can be derived as shown below.

$$\bar{X}_2 = \frac{d_0}{d_0 R_i + (1-d_0)^2 R_L} \bar{X}_1 \quad (4-35)$$

$$\bar{X}_3 = \frac{d_0 (1-d_0) R_L}{d_0 R_i + (1-d_0)^2 R_L} \bar{X}_1 \quad (4-36)$$

$$G_{Vdu}(s) = \frac{-\bar{X}_2 \left[s^2 - \left(\frac{(\bar{X}_3 + \bar{X}_1)(1-d_0) - R_i \bar{X}_2}{L_m \bar{X}_2} \right) s + \frac{d_0}{C_{uc} L_m} \right]}{C_f \left[s^3 + \left(\frac{d_0 R_i}{L_m} + \frac{1}{C_f R_L} \right) s^2 + \left(\frac{(1-d_0)^2}{L_m C_f} + \frac{d_0^2}{L_m C_{uc}} + \frac{d_0 R_i}{L_m C_f R_L} \right) s + \frac{d_0^2}{C_{uc} L_m C_f R_L} \right]} \quad (4-37)$$

4.4.1 System RHP Zeros

From the numerator of (4-37) it is seen that the fly-back converter also has two RHP zeros in the control to output transfer function when used with ultra-capacitors. The two RHP zeros are located at,

$$Z_{1u} = Z_{1u_flyback} = \left(\frac{(\bar{X}_3 + \bar{X}_1)(1-d_0) - R_i \bar{X}_2}{2L_m \bar{X}_2} \right) - \sqrt{\left(\frac{(\bar{X}_3 + \bar{X}_1)(1-d_0) - R_i \bar{X}_2}{2L_m \bar{X}_2} \right)^2 - \frac{d_0^2}{L_m C_{uc}}} \quad (4-38)$$

$$Z_{2u} = Z_{2u_flyback} = \left(\frac{(\bar{X}_3 + \bar{X}_1)(1-d_0) - R_i \bar{X}_2}{2L_m \bar{X}_2} \right) + \sqrt{\left(\frac{(\bar{X}_3 + \bar{X}_1)(1-d_0) - R_i \bar{X}_2}{2L_m \bar{X}_2} \right)^2 - \frac{d_0^2}{L_m C_{uc}}} \quad (4-39)$$

The low frequency RHP zero associated with the ultra-capacitor based fly-back converters is given in (4-38). Following a similar procedure as in the case of (4-9), (4-38) can be simplified to,

$$Z_{1u} = Z_{1u_flyback} = \frac{d_0^3}{C_{uc}[(1-d_0)^2 R_L - d_0^2 R_i]} \quad (4-40)$$

Since the conversion ratio of the fly-back converter is quite different from that of the classical boost converter or the tri-state boost converter, the comparison of $Z_{1u_flyback}$ with $Z_{1u_classical}$ and $Z_{1u_tri-state}$ is not very straightforward. In practice, d_0 of the classical boost converter or the d_b of the tri-state boost converter is less than the d_0 of the fly-back converter for the same boost ratio. Therefore, the low frequency RHP zero of the capacitor based fly-back converter may sometimes be located further from the origin compared to the capacitor based classical boost converter or the capacitor based tri-state boost converter as can be seen from (4-9), (4-22) and (4-40).

The other RHP zero given in (4-39) is seen to be located far away from the origin and, as in the case of the classical boost converter, it can also be shown that this high frequency RHP zero is located closer to the RHP zero of a constant emf battery based fly-back converter.

4.4.2 Approximate System Poles

In order to derive the approximate pole positions, assume that R_L is very large. The approximate pole positions of the fly-back converter can then be found after simplifications as,

$$P_{1u} = P_{1u_flyback} \cong 0 \quad (4-41)$$

$$P_{2u} = P_{2u_flyback} \cong \frac{-d_0 R_i}{2L_m} + \sqrt{\left(\frac{d_0 R_i}{2L_m}\right)^2 - \left(\frac{d_0^2}{C_{uc} L_m} + \frac{(1-d_0)^2}{L_m C_f}\right)} \quad (4-42)$$

$$P_{3u} = P_{3u_flyback} \cong \frac{-d_0 R_i}{2L_m} - \sqrt{\left(\frac{d_0 R_i}{2L_m}\right)^2 - \left(\frac{d_0^2}{C_{uc} L_m} + \frac{(1-d_0)^2}{L_m C_f}\right)} \quad (4-43)$$

Equation (4-41) to (4-43) suggests that the fly-back converter also has one pole very close to the origin while the other two poles are relatively far away from the origin. This means the fly-back converter also has a low frequency pole-zero pair when it is operated with ultra-capacitors.

Note that, as in (4-25), the poles in (4-42) and (4-43) also form a complex conjugate pair in most practical applications.

Furthermore, an approximate expression for $P_{1u_flyback}$ may be obtained from (4-20) as shown below, following the same procedure discussed in section 4.2.3.

$$P_{1u} = P_{1u_flyback} = \frac{-(d_0)^2}{C_{uc}[(1-d_0)^2 R_L + d_0 R_i] + C_f R_L (d_0)^2} \quad (4-44)$$

Comparing (4-40) and (4-44), it can be seen that $P_{1u_flyback}$ is slightly smaller than $Z_{1u_flyback}$.

4.4.3 Exact System Poles

Deriving simple expressions for the exact poles is again difficult. However if the poles of the system are taken as γ_1 , γ_2 and γ_3 then the following relationships can be derived from the denominator of (4-37).

$$\gamma_1 + \gamma_2 + \gamma_3 = -\left(\frac{d_0 R_i}{L_m} + \frac{1}{C_f R_L}\right) \quad (4-45)$$

$$\gamma_1 \gamma_2 + \gamma_1 \gamma_3 + \gamma_2 \gamma_3 = \left(\frac{d_0^2}{C_{uc} L_m} + \frac{(1-d_0)^2}{L_m C_f} + \frac{d_0 R_i}{R_L L_m C_f}\right) \quad (4-46)$$

$$\gamma_1 \gamma_2 \gamma_3 = -\frac{d_0^2}{C_{uc} L_m C_f R_L} \quad (4-47)$$

Note that the poles that are denoted as γ_1 , γ_2 and γ_3 corresponds to the poles given in (4-41) to (4-43).

Comparing (4-10) to (4-12) with (4-45) to (4-47), it is seen that,

$$|\gamma_1 + \gamma_2 + \gamma_3| < |\alpha_1 + \alpha_2 + \alpha_3| \quad (4-48)$$

$$|\gamma_1 \gamma_2 + \gamma_1 \gamma_3 + \gamma_2 \gamma_3| < |\alpha_1 \alpha_2 + \alpha_1 \alpha_3 + \alpha_2 \alpha_3| \quad (4-49)$$

$$|\gamma_1 \gamma_2 \gamma_3| < |\alpha_1 \alpha_2 \alpha_3| \quad (4-50)$$

Therefore, as per (4-48) to (4-50), all the poles of the fly-back converter can be smaller in magnitude compared to the poles of an equivalent classical boost converter. This result suggests that the low frequency left half plane pole of the fly-back converter can be located closer to the origin compared to that of the classical boost converter. But this may not always be guaranteed as other pole combinations can also satisfy these inequalities.

4.4.4 Comment on the Low Frequency Pole-zero Pair Compared to Capacitor based classical boost converter

It is seen that the direction of movement of the low frequency pole-zero pair is not very conclusive in the fly-back converter. However, comparing (4-10) to (4-12) and (4-45) to (4-47) it can be seen that the variation of γ_1 , γ_2 and γ_3 from the corresponding poles of classical boost converter, α_1 , α_2 and α_3 , should be very small. Thus, the ultimate variation of the low frequency pole-zero-pair is very small compared to the classical boost converter. Therefore, a significant improvement of the performance cannot be expected from the fly-back converter compared to the classical boost converter. Moreover, the efficiency of the fly-back converter is less compared to the classical boost converter, leading to faster discharge of capacitor bank.

4.4.5 Numerical Results

To verify these conclusions, consider the same numerical example that was used to compare classical and tri-state boost converters.

The system parameters for the fly-back converter are selected as,

$$C_{uc} = 1F, \quad L_m = 2.4mH, \quad R_i = 0.5\Omega, \quad C_f = 2200\mu F, \quad R_L = 120\Omega, \quad V_{dc} \text{ (rated)} = 650V, \\ X_{10} = 325V$$

The fly-back converter duty ratio for this case was calculated as $d_0 = 0.68$, from (4-35) and (4-36).

With these parameters, the exact analysis results in $P_{1u_flyback} = -0.0339$ and $Z_{1u_flyback} = 0.0261$, while the approximate analysis results in $P_{1u_flyback} = -0.0363$ and $Z_{1u_flyback} = 0.0261$. Hence, $P_{1u_flyback}$ is seen to be located slightly closer to the origin compared with capacitor based classical boost converter while $Z_{1u_flyback}$ is located slightly

away from origin. However the movement of the pair is still seen to be negligible for any practical purpose.

Therefore, it can be seen that both the tri-state boost converter and the fly-back converter give inferior performance than the classical boost converter when operated with ultra-capacitors. However, the difference in performance is seen to be very small to make any impact on the converter performance.

4.5 Summary

Currently, the most widely used DC-DC converters to interface ultra-capacitor banks are the classical boost converter and the fly-back converter. It was shown that both these converters contain a low frequency pole-zero pair in their transfer functions when capacitors are used as the source. Moreover, the low frequency pole-zero pair is shown to exist in addition to the poles and zeros found in equivalent constant emf battery based converter transfer functions. When control to output transfer function is considered, the zero of the low frequency pole-zero pair is shown to be located on the right half plane (RHP) while the pole is located in left half plane (LHP).

As explained in Chapter 3, the tri-state boost converter is capable of eliminating the RHP zero that is known to exist in the control to output transfer function of the classical boost converter. However, it is not capable of eliminating the low frequency RHP zero of a capacitor based system. This is because the existence of the low frequency pole-zero pair is, in fact, a direct result of the finite capacitance of the capacitor bank. Hence, it is not possible to eliminate the low frequency pole-zero pair from the transfer functions of the capacitor based systems.

The efficiencies of both fly-back converter and the tri-state boost converter are less than that of an equivalent classical boost converter. Although it does not have a significant effect on the performance of a constant emf battery based system, it has a noticeable influence on the

performance of a capacitor based system. This is because a less efficient converter discharges the capacitor bank faster, thereby causing a faster decay of the capacitor terminal voltage. Therefore, from the three converters analyzed in this chapter, the classical boost converter is seen to be more suitable for capacitor based applications in this aspect.

Since ultra-capacitors can also be approximately represented as normal capacitors, descriptions in this chapter are also seen to be applicable for ultra-capacitor based systems.

Voltage-mode control is the simplest form of closed loop control that can be applied to control DC-DC converters. However, it does not significantly alter the closed loop system transfer functions from the open loop system transfer functions [8]. Therefore, the adverse effects of the low frequency pole-zero pair should be dominant in voltage-mode controlled ultra-capacitor based DC-DC converters, if not properly compensated. These aspects will be analyzed in more detail in the next chapter. The analysis is based on an ultra-capacitor based ride through system, which is the most common application involving ultra-capacitors at present.

CHAPTER 5

VOLTAGE-MODE CONTROL OF ULTRA-CAPACITOR BASED RIDE THROUGH SYSTEM

5.1. Introduction

Ultra-capacitor based ride through systems are suitable to provide ride through for Adjustable Speed Drives (ASD), which is currently a significant load component in large power systems. An ASD drives a process at a variable-speed. In the commonly used ac induction motor drives, power electronic devices are switched at high frequencies to generate the variable-frequency variable-voltage power supply needed for the motor [20, 94].

ASDs are sensitive to power system disturbances and the most disruptive disturbances for them are the voltage sags and the momentary interruptions of the power source [20]. A voltage sag is defined as a decrease in rms voltage between 10% and 90% of nominal voltage, for periods from a half cycle to a minute, whereas a momentary interruption is a decrease in rms voltage of greater than 90% [20]. However, the majority of the sags or momentary interruptions last up to a few seconds [15, 20]. Survey results have shown that, in order to make the ASD immune to the most common sags, ride through for sags with a magnitude of up to 40% and duration of up to 60 cycles should be provided. To provide immunity for the most common momentary interruptions, the ride through should be provided for at least 3 seconds for a complete loss of input power source [15, 20].

For most of the common voltage sags, the ride through performance of the ASD can be improved from the integrated boost converter approach [18] without using an additional energy storage. In this method, a boost converter is employed between the source and the dc link of the ASD. This boost converter is operated to boost up the dc link voltage once the source

voltage is reduced. However this approach is not applicable for momentary interruptions where the source is not available during the disturbance. Ultra-capacitor based ride through systems are particularly suitable to provide ride through during these momentary interruptions of the source [15].

The general configuration of an ASD without a ride through mechanism is given in Fig. 5.1.

Fig 5.1. General configuration of an Adjustable Speed Drive

In general, the dc link of the ASD is supplied by a three-phase controlled or uncontrolled rectifier, although the uncontrolled rectifier type, shown in Fig 5.1, is more common due to its lower cost. When the source is tripped or when the source voltage is reduced considerably due to a power system fault, the ride through time of this general ASD configuration is determined primarily by the size of the dc link capacitance. However, in practice the existing dc link capacitance of an ASD is only capable of providing ride through for a few milliseconds, which is too small considering the fact that a momentary interruption can last for as long as a few seconds [15].

An ultra-capacitor bank can be connected to the dc link as shown in Fig 5.2 to improve the ride through performance of the ASD.

Fig 5.2. Ultra-capacitor based ride through system for an ASD

In Fig 5.2, the simplest form of the boost converter, which is the classical boost converter, is used as the interface between the ultra-capacitor bank and the dc link. In fact this is the most widely used form of the boost converter for this application, when galvanic isolation is not required. If a deep voltage sag occurs in the grid so that the peak line to line voltage is less than the dc link voltage, all the diodes become reverse-biased at all times, effectively isolating the dc link from the grid causing a momentary interruption. During this period, the bank of ultra-capacitors injects power through the DC-DC converter to maintain the dc link voltage within a selected range. The ride-through system should also initiate its remedial action quickly to ensure that the immediate fall of dc link voltage following the sag does not drop below a certain set minimum level in order to prevent undesirable tripping of the ASD. Upon the recovery of the grid voltage, the normal operation resumes and the bank of ultra-capacitors is charged back to its full charged level, drawing power either from the ac or dc side of the rectifier through its charging circuit which is not shown in Fig 5.2.

5.2. System Analysis

The equivalent circuit of the system shown in Fig 5.2 is shown in Fig 5.3.

Fig 5.3. Equivalent circuit of the ride through system for the ASD

The source is modeled by the average value of the rectified voltage E_s in series with a resistor R_s and an inductor L_s representing the line impedance. Diode D_s indicates the unidirectional power flow from the source. The voltage source inverter and the motor load of the ASD is modeled as a constant dc current source as described in [94]. Although a harmonic current source is more appropriate, extensive sensitivity studies had suggested that there is little need to model it in such a way [94]. This is because the dc link capacitance, C_f , bypasses most of the inverter harmonics and hence their effect on the rest of the system is minimized [94].

As explained in Chapter 2, an ultra-capacitor can be represented with a very good accuracy from the advanced model describing the dynamic ultra-capacitor behavior having about ten RC elements [49]. However this model increases the order of the system considerably as it introduces ten more states to the system. This makes it inconvenient to analyze the system transfer functions. On the other hand, the classical model for the ultra-capacitor, described in section 2.7, results in the simplest system transfer functions for the ride through system although the model is less accurate.

The following two sections analyze the ride through system transfer functions with these two models of the ultra-capacitor.

5.2.1. System Transfer Functions with Classical Model for the Ultra-capacitor

The equivalent circuit of the ride through system with classical model for the ultra-capacitors is shown in Fig 5.4.

Fig 5.4. Equivalent circuit of the ride through system and the load

The small signal system transfer functions for this system can be derived from Middlebrook's state space averaging theory [28] as described in Appendix A.

The control to output transfer function $G_{Vdu}(s)$ and the source disturbance to output transfer function $G_{VUu}(s)$ are given in (A3-5) and (A3-6) respectively, in Appendix A. By factorizing the numerator of $G_{Vdu}(s)$, it can be shown that it has one LHP zero and two right half plane (RHP) zeros. The LHP zero is located at $Z_{3u} = -R_S / L_S$ while the two RHP zeros are located at,

$$Z_{1u} = [(\bar{X}_3(1-d_0) - R_i \bar{X}_2) / (2L_i \bar{X}_2)] - (Z_d / 2), Z_{2u} = [(\bar{X}_3(1-d_0) - R_i \bar{X}_2) / (2L_i \bar{X}_2)] + (Z_d / 2) \quad (5-1)$$

$$\text{Where, } Z_d = \sqrt{[(\bar{X}_3(1-d_0) - R_i \bar{X}_2) / (2L_i \bar{X}_2)]^2 - (1 / (C_{uc} L_i))}$$

For Z_d to be real, C_{uc} should be large enough to satisfy the inequality,

$$C_{uc} > L_i [(\bar{X}_3(1-d_0) - R_i \bar{X}_2) / (2L_i \bar{X}_2)]^2 \quad (5-2)$$

For practical ultra-capacitor based ride-through systems, this inequality is normally satisfied and Z_{1u} and Z_{2u} are found as real. Furthermore, it can also be seen that $Z_{2u} \gg Z_{1u}$. Therefore, an approximate expression for Z_{1u} may be obtained as explained in appendix E3 by evaluating the numerator of (A3-5). This approximate position of Z_{1u} is given in (E5-3) in Appendix E5.

It is difficult to derive exact expressions for the four poles of the system in the same way. However approximate solutions for all the system poles may be obtained as follows, if $d_0 \cong 1$ is substituted in (A3-7) in Appendix A.

$$P_{1u} = \left[- (R_i / L_i) + \sqrt{(R_i / L_i)^2 - (4 / (L_i C_{uc}))} \right] / 2 \quad (5-3)$$

$$P_{2u} = \left[- (R_i / L_i) - \sqrt{(R_i / L_i)^2 - (4 / (L_i C_{uc}))} \right] / 2 \quad (5-4)$$

$$P_{3u}, P_{3u}^* = \left[- (R_S / L_S) \pm \sqrt{(R_S / L_S)^2 - (4 / (L_S C_f))} \right] / 2 \quad (5-5)$$

Note that the relationships given in (5-3) – (5-5) are only accurate when $d_0 \cong 1$, and they can not be considered as general expressions for the poles of the system. However, these expressions may be used to derive the relative magnitudes of the poles.

From (5-3), (5-4) and (5-5) it is seen that $P_{1u} \ll P_{2u} < P_{3u}, P_{3u}^*$ since $C_{uc} \gg C_f$. Hence a more accurate approximate expression for P_{1u} may be obtained as described in appendix E3 and using the denominator expression in (A3-7). This approximate expression of P_{1u} , which is repeated below, is derived in appendix E5.

$$P_{1u} \cong \frac{-1}{R_S \left((1 - D_0)^2 C_{uc} \right) + R_i C_{uc}} \quad (5-6)$$

Such an accurate estimation of the other system poles is not possible since all these poles can have comparable magnitudes. Nevertheless, few important observations can be made about these poles from the expressions given in (5-4) and (5-5).

P_{2u} in (5-4) represents an approximate position of the pole which is primarily associated with the boost converter inductance, L_i . The approximate positions of the other two poles, which are associated mainly with the load side parameters of the converter, are denoted as P_{3u} and P_{3u}^* in (5-4), since they are complex in almost all cases. Note that, P_{2u} and P_{1u} , are real in almost all ultra-capacitor based systems since C_{uc} is a high value, which is in the order of a few Farads.

For practical systems, the (R_S/L_S) ratio can be quite small. Therefore, P_{3u} and P_{3u}^* has very small damping coefficients and they lie closer to the origin. Therefore, the position of P_{2u} , which depends more on the (R_i/L_i) ratio, will have a significant influence on the damping of the response of the ride through system.

The pole-zero map depicting these approximate pole and zero positions are given in Fig 5.5.

Fig 5.5. Typical pole-zero map of the control to output transfer function of a classical boost converter operating with ultra-capacitors modeled by classical model (not to scale)

Note that the pole-zero map of a constant emf battery based classical boost converter does not

have the low frequency pole-zero pair shown in Fig 5.5, although it has all the other system poles and zeros shown. The separation between the low frequency pole-zero pair is dependant mainly on the value of C_{uc} as can be seen from (5-1) and (5-6).

5.2.2. System Transfer Functions with Advanced Ultra-capacitor Model for the Ultra-capacitor

The equivalent circuit of the ride through system with the advanced ultra-capacitor model [49] is shown in Fig 5.6.

Fig 5.6. Equivalent circuit of the ride through system for the ASD with advanced ultra-capacitor model with ten capacitive elements

Small signal transfer functions can be derived in the same way for this system as shown in Appendix A. However it is not convenient to derive expressions for the approximate pole-zero positions as was done above in section 5.2.1 for the classical model.

The simplest case with one ladder branch added to the classical model is evaluated in Appendix B. It is shown that the additional pole that is added to the transfer functions due to the added ladder branch lies to the left of the dominant pole added, due to the capacitive element in the classical model. However, when the number of ladder branches increase, this

analysis is not convenient to extend, and hence only a numerical evaluation is possible. Fig 5.7 illustrates a typical pole-zero map that is derived from numerical calculations for a practical system.

Fig 5.7. Typical pole-zero map of the control to output transfer function of a classical boost converter operating with ultra-capacitors modeled by advanced ultra-capacitor model (not to scale)

Numerical investigation shows that for every RC branch that is added to the ultra-capacitor model, a pole-zero pair is added to the pole-zero map. The additional pole-zero pairs are in the Left Half Plane (LHP), and, each pair that is added with every additional RC branch is located to the left of all the previous pairs. However, the dominant pole-zero pair shown in Fig 5.7 is added due to the capacitive element C_{uc} in Fig 5.6 and it is located very close to the position of the low frequency pole-zero pair shown in Fig 5.5. Moreover, the pole and zero of the additional pole-zero pairs added to the LHP are close to each other and are also relatively far away from the origin compared to the dominant pole-zero pair. This further reduces the effect of these additional pole-zero pairs on the control to output transfer function of the system.

Nevertheless in higher order systems, only the dominant poles and zeros need to be considered when designing its closed loop control system to obtain acceptable performance [8]. Therefore,

it is seen to be sufficient to model the ultra-capacitor from its classical model when designing control system of the ride through system. Hence, all the analysis of the ultra-capacitor based ride through system that follows will use the classical model of the ultra-capacitor, similar to the analysis in section 5.2.1.

This means that the analysis performed for capacitor based systems in Chapter 4 is applicable even for the ultra-capacitor based systems considered in this chapter.

5.3. Ultra-capacitor Based Ride Through System for a Linear RL Load

By replacing the current source load in Fig 5.4 with a series combination of a resistance R_L and an inductance L_L , the above analysis can be repeated, the results of which will be valid for any general RL load. With the exception of an additional high frequency pole-zero pair corresponding to the load parameters R_L and L_L , this analysis would also result in the same conclusions that were reached under the constant current source load above. This means that the main conclusions made with respect to the low frequency pole-zero pair will remain valid for all types linear loads in general.

The system matrices corresponding to the RL load are also given in Appendix A.

5.4 Variation of Low Frequency Pole-zero Pair with System Parameters

As mentioned earlier, it is not convenient to derive simple expressions for the exact positions of the low frequency pole and the zero of ultra-capacitor based systems. However it's worthwhile to identify how this pole-zero pair varies with each and every parameter of the ride through system depicted above, in order to obtain a better insight into the system properties.

Hence, a numerical example, with a RL load, is considered in this section to analyze these variations. The RL load is used here to enable the analysis to be extended to the variations of linear load parameters.

The variation of the low frequency pole-zero pair in the control to output transfer function with variation of system parameters is analyzed here.

The nominal system parameters used for the analysis are given below. Only one of these parameters is varied at a time around its nominal value while the others remain constant at the given values.

$$C_{uc} = 3.5F, R_i = 0.192\Omega, L_i = 2.4mH, C_f = 2200\mu F, L_S = 2.4mH, R_S = 0.3\Omega, E_S = 660V, \\ V_{dc} = 650V, R_L = 25\Omega, L_L = 10mH$$

As per the results shown in Fig 5.8, three parameters, namely the capacitance (C_{uc}), the parasitic series resistance (R_i) and the source resistance (R_S) can be identified as the parameters that mostly influence the positions of the low frequency pole-zero pair. All the other parameters do not show a significant effect.

As expected, the capacitance of the ultra-capacitor bank, C_{uc} , is seen to be the most influential. The separation between the pole and the zero of the pair is seen to increase when the magnitude of C_{uc} is decreased. Similar patterns for the variation of the low frequency pole-zero pair is also seen with R_i and R_S . These results agree with the conclusions made from the approximate pole-zero analysis earlier in this chapter and in appendix E4 and E5.

The capacitance C_{uc} is directly dependant on the ultra-capacitor bank. Furthermore, R_i also partially depends on the ultra-capacitor bank. Hence, it is seen that, while the finite capacitance of the ultra-capacitor bank is responsible for the existence of the low frequency pole-zero pair, the ultra-capacitor bank also has the most influence on their positions, although the effect of the source resistance is also significant. In general, as the size of the capacitor bank increases, the effects of the low frequency pole-zero pair will diminish as the pole-zero pair almost cancels with each other.

From the graphs of fig 5.8 and also from the approximate analysis given in appendix E4 and E5, it can be seen that $P_{1u} \gg Z_{1u}$, and the magnitude of Z_{1u} almost always very close to zero. Furthermore, compared to all the other poles and zeros of the system, both P_{1u} and Z_{1u} have very small magnitudes and are seen to be relatively close to each other.

The stability limit given in (3-6) in chapter 3 is derived assuming no poles at the vicinity of the RHP zero [67]. Therefore this stability limit, does not strictly apply to RHP zeros like Z_{1u} , where a pole can always be found close by. Furthermore, an additional open loop pole zero pair, similar to P_{1u} and Z_{1u} , generates an additional branch in the root locus that results in an additional closed loop pole [95]. Since Z_{1u} is in RHP, part of this additional root locus branch will be in RHP. Therefore, once a certain limit is exceeded (by the controller), the additional closed loop pole will move to the RHP making the system unstable. However, since Z_{1u} has a small magnitude, the closed loop pole that is pushed to the RHP will also have a small magnitude and hence a large time constant in most cases. Therefore, it will not have a significant influence on the system response in the first few seconds of operation. Hence, the stability limit imposed by Z_{1u} , if any, can be ignored when designing control systems that intend to operate only for a few seconds, like ultra-capacitor based systems.

Hence, Z_{1u} can be considered as located on the origin, (i.e. it is not considered as a RHP zero) to simplify the controller design process for ultra-capacitor based ride through systems. It should also be noted that the expressions for Z_{1u} are only approximate expressions that are dependant on the assumptions made regarding the steady state of the system. However, the magnitude of P_{1u} can not be assumed as negligible in the same way, since it generally has a sufficiently large magnitude to influence the system response even within a few seconds.

Fig 5.8: Variation of the positions of low frequency pole-zero pair with system parameters (a) With capacitance, (b) With parasitic inductor resistance, (c) Boost converter inductance, (d) Output filter capacitance, (e) Source resistance, (f) Source inductance, (g) Load resistance and (h) Load inductance

5.5. Comparison of Ultra-capacitor Based and Battery Based Ride Through Systems.

As explained in Chapter 4, the low frequency pole zero pair exists in ultra-capacitor based ride through system transfer functions due to the finite capacitance of the ultra-capacitor banks. A ride through system based on a battery with a constant emf will not show this low frequency pole-zero pair in its transfer functions.

It was shown in Chapter 4 that a battery based system can be considered as a limiting system for capacitor based systems. Since the conclusions in Chapter 4 also applies to ultra-capacitor based systems, this shows that the ultra-capacitor based systems can be made identical to battery based systems only when C_{uc} is infinite. (Assuming battery emf is constant during the useful operating period). Nevertheless, the results in Chapter 4 also show that the properties of the ultra-capacitor based system can be made closer to the properties of a constant emf battery based system by increasing C_{uc} . However, this would also increase the cost and the size of the ultra-capacitor bank considerably.

As shown above, the ultra-capacitor based ride through system has two RHP zeros in its control to output transfer function. However, the low frequency RHP zero can be assumed to be located on the origin when designing control systems for ultra-capacitor based systems as described above in section 5.4. Therefore, ultra-capacitor based systems will also have the same effective RHP zero as that of battery based systems.

RHP zeros impose fundamental limitations on the control bandwidth, as they force an upper limit to the achievable gain cross over frequency for stable operation as described in chapter 3 [67, 90]. Since the effective RHP zero of ultra-capacitor based system is very close to the RHP zero of the battery based system, both these systems is seen to have almost the same stable control bandwidth.

However, the additional low frequency pole, P_{1u} , in the ultra-capacitor based system can

degrade its performance unless P_{1u} is properly compensated by the controller. Also from (A2-2) and (A3-5), it is seen that the control to output transfer function of the ultra-capacitor based systems have a smaller DC gain compared to the equivalent battery based system. This also helps to degrade the steady state performance of the ultra-capacitor based system. This possibility of performance degradation is one of the main distinctions between the ultra-capacitor and the battery based systems.

Moreover, the positions of the poles and zeros of the battery based systems can be assumed as fixed during its useful operating period. But the same can not be assumed for an ultra-capacitor based system since ultra-capacitor terminal voltage, X_1 , always decreases when the system operates. This variation of X_1 in turn causes the variation of all the other states of the system, which means that in strict terms the ultra-capacitor based systems do not have a steady state. Hence the ultra-capacitor based system can only be assumed as reaching a quasi steady state.

Since X_1 varies, the quasi steady state also varies with time causing the system poles and zeros to vary as shown in the Fig 5.9. The variation of the system zeros depicted in Fig 5.9 may also be visualized from the equations derived for them in section 5.2 although the variation of poles can only be conveniently obtained from numerical results.

Fig 5.9. Typical variation of poles and zeros of the control to output transfer function with the decreasing terminal voltage of the ultra-capacitor bank (not to scale)

All the factors described above affect the ultra-capacitor based ride through system's response adversely and hence the performance, especially the steady state performance, can be very poor compared to the steady state performance of an equivalent constant emf battery based system, unless the low frequency pole and the low dc gain is compensated.

5.6. Voltage-mode Controller Design

Voltage-mode control is the simplest form of control that can be applied to control ride through systems. It uses only one feedback signal, the output capacitor voltage or the output load voltage, in its control loop. Fig 5.10 depicts the small-signal block diagram of the closed-loop feedback control of voltage-mode control. It controls the dc link voltage $\tilde{V}_{DC}(s)$ of the ride-through system.

In the figure, $\tilde{V}_{dc,ref}(s)$ represents small changes in reference voltage, $\tilde{U}_s$ represents the small variations of the source voltage and H represents the feedback gain. $G_{VU}(s)$ represent either

$G_{VUu}(s)$ or $G_{VUb}(s)$ depending on whether the system is ultra-capacitor-based or battery-based. Similarly, $G_{Vd}(s)$ represents either $G_{Vdu}(s)$ or $G_{Vdb}(s)$.

Fig 5.10. Small signal control block diagram for Voltage-mode control

The loop gain of the system in Fig 5.10, which is defined as the product of the gains of the forward and feedback paths of the loop [8], is given by,

$$L(s) = Hk_p G_{cv}(s)G_{Vd}(s) \quad (5-7)$$

where k_p is the gain of the PWM signal generator, H is the gain of the voltage sensor and $G_{cv}(s)$ is the transfer function of the compensator (controller) to be designed. $L(s)$ is controllable via $G_{cv}(s)$ and can be used to modify the closed-loop disturbance rejection properties of the system. The dc gain of $G_{cv}(s)$ is selected to make the dc gain of $L(s)$ positive.

Due to the limitations of control bandwidth imposed by the RHP zeros, the controller should be designed to satisfy the condition given in (3-6). Note that, since the limitations due to Z_{1u} can largely be ignored, Z_{2u} should be used to calculate the bandwidth limitation from (3-6). Therefore, it can directly be seen that the ω_{gc} for ultra-capacitor based systems is almost equal to that of the battery-based systems because Z_{2u} is almost equal to Z_{1b} , the RHP zero of the battery based system. The limiting controller that compensates the system to agree with (3-

6) guarantees the specified stability margins. Increasing the controller gain beyond this value will reduce the stability margins and ultimately will force the system to be unstable.

Since the controller design procedure involves n_{gc} , the slope of the minimum phase component of $L(s)$, it is necessary to separate the minimum and non-minimum phase parts of $L(s)$ as $L_{mp}(s)$ and $L_{nmp}(s)$ respectively [67].

For the ultra-capacitor based system, the numerator of $G_{Vdu}(s)$ given in (A3-5) in Appendix A can be rearranged to reflect its RHP zeros as,

$$N_{du}(s) = -C_{uc}L_i\bar{X}_2(sL_s + R_s)(s - Z_{1u})(s - Z_{2u}) \quad (5-8)$$

Since Z_{1u} can be considered as located on the origin, (5-8) may be simplified as shown below.

$$N_{du}(s) = C_{uc}L_i\bar{X}_2(s)(sL_s + R_s)(Z_{2u} - s) \quad (5-9)$$

Considering the fact that there are no other non-minimum phase components in the denominator of $G_{Vdu}(s)$ and in the compensator $G_{cv}(s)$, $L_{nmp}(s)$ and $L_{mp}(s)$ are separated as [67], (Appendix F)

$$L(s) = L_{nmp}(s)L_{mp}(s) \quad (5-10)$$

$$|L_{nmp}(s)| = [(Z_{2u} - s)] / [(Z_{2u} + s)] \quad (5-11)$$

$$|L_{mp}(s)| = |[G_{cv}(s)(C_{uc}L_i\bar{X}_2)(sL_s + R_s)(Z_{2u} + s)HK_p] / D_{du}(s)| \quad (5-12)$$

The sign of $L_{nmp}(s)$ is chosen to satisfy the requirement of encirclements by the Nyquist stability criterion [67]. The sign of $L_{mp}(s)$ should then be selected such that the sign of $L(s)$ is unchanged. The slope n_{gc} refers to the slope of $L_{mp}(s)$ at the cross over frequency ω_{gc} . Note that both n_{gc} and ϕ_m are selectable by the designer and are dependant on the choice of $G_{cv}(s)$. The right hand side of (3-6), which is the limit of ω_{gc} for stability, will change depending on these parameters.

The closed-loop disturbance rejection transfer function of the overall system can be derived from Fig 5.10 as,

$$G_{VU}(s)|_{closedloop} = \tilde{V}_{DC}(s)/\tilde{U}(s) = G_{VU}(s)/(1 + L(s)) \quad (5-13)$$

To describe the controller design procedure for an ultra-capacitor based ride through system for an ASD and to demonstrate the effect of the low frequency pole-zero pair on the system response, numerical values and computer simulation results for two selected systems are presented next.

5.7. Illustrative Examples

5.7.1 System Description.

In the examples, the voltage at the dc link of an ASD is treated as healthy if it remains between a set minimum value V_{min} and a maximum value V_{max} around the rated dc link voltage, V_{rated} , which is the rated value of V_{dc} . The ultra-capacitor based ride-through system is activated only after the dc link voltage drops below V_{min} due to the occurrence of a deep voltage sag or a momentary interruption in the ac supply voltage. Therefore, the dc link voltage will continue to drop until the power transferred through the boost converter increases to the level of power demanded by the load during a disturbance. However, since there is usually a set voltage V_{trip} at which the ASD will be tripped by under-voltage protection relays, the ride through system must quickly avoid reaching this critical voltage. The dc link voltage should then be brought back to the acceptable range with no overshoot beyond V_{max} and maintained preferably at V_{rated} during the entire period of disturbance.

Note that V_{trip} is generally taken as 87% of the rated dc link voltage in most practical ASD systems [15, 18].

5.7.2 Example 1

Consider the system with following parameters. Apart from $V_{\min}$, $V_{\max}$, V_{trip} and V_{dc} , all the other parameters correspond to the equivalent circuit shown in Fig 5.4 and the control block diagram shown in Fig 5.10.

$C_{uc} = 0.35F$, $R_i = 0.5\Omega$, $L_i = 5mH$, $C_f = 1000\mu F$, $L_s = 0.75mH$, $R_s = 0.3\Omega$, $E_s = 650.9V$, $I = 3A$, $V_{dc} = 650V$, $V_{\min} = 0.95V_{dc} = 617.5V$, $V_{\max} = 1.1V_{dc} = 715V$, $V_{trip} = 0.87V_{dc} = 565.5V$, $K_p = 0.02$ and $H = 0.085$. The ride-through period specification is taken as $t_{ride} = 3$ sec [15, 18].

In this case the full charged voltage of the ultra-capacitor bank, i.e. $V_{uc\max}$, is taken as 325V, which is 50% of the rated dc link voltage, V_{dc} . The minimum useful voltage of the ultra-capacitor bank, i.e. $V_{uc\min}$, is taken as 60% of $V_{uc\max}$, i.e. 195V. Hence, the boost converter that interfaces the ultra-capacitor bank with the load should have a boost ratio range from 2 to 3.3 in order to have 650V at the load. Substituting these values in (2-3) the minimum capacitance that is required to provide successful ride through for the load can be obtained as $C_{uc} = 0.23F$. To allow for the converter losses, the size of the ultra-capacitor bank was chosen as 0.35F, which is approximately 2 times the minimum value given above.

The parameters of the source, i.e. L_s , R_s and E_s , were chosen to be compatible with practical adjustable speed drive systems as per [18]. The magnitudes of L_f and C_f were chosen so that the ripple in boost inductor current and the output load voltage to be 5% of the rated value as per [26]. The peak value of the saw-tooth waveform of the PWM generator was assumed as 50V. The values of H and K_p were chosen to match with this peak value [8].

The tripping voltage V_{trip} is taken as 565.5V which is 87% of $V_{L,rated}$, corresponding to the value for a commercial adjustable-speed drive [15].

5.7.2.1 Analysis of the Pole-zero Positions

From the above data, the duty ratio to output voltage transfer function may be obtained from (A2-4) and (A3-5) for the ultra-capacitor based ($G_{du}(s)$) and battery based ($G_{db}(s)$) ride through systems respectively. Note that the emf of the equivalent battery based system (E_b) is taken as 325V. The pole-zero pattern for $G_{du}(s)$ are given in Table 5-1 for two initial ultra-capacitor charge levels together with the corresponding values for the equivalent $G_{db}(s)$. The corresponding DC gains of the transfer functions is also given in table 5-1.

TABLE 5-1

Pole-zero positions of open-loop duty-ratio to dc link voltage transfer function

– Example 1

Initial Charge	Ultra-capacitor Bank			Battery	
		$\bar{X}_1 = 325 \text{ V}$	$\bar{X}_1 = 250 \text{ V}$		$E_b = 325 \text{ V}$
Poles	P_{1u}	-5.2	-5.5	P_{1b}	$-208.6 \pm 1196i$
	P_{2u}	-106.2	-101.3	P_{2b}	-111.4
	P_{3u}	$-208.6 \pm 1196i$	$-211 \pm 1188i$	-	
Zeros	Z_{1u}	0.0029	0.005	Z_{1b}	324700
	Z_{2u}	194700	115100	Z_{2b}	-428.6
	Z_{3u}	-428.6	-428.6	-	
DC gain magnitude		0.1	0.13	169	

It is seen from Table 5-1 that, apart from the low frequency pole-zero pair, almost all the other high frequency system poles and zeros are almost equal in battery based and ultra-capacitor based systems. This is approximately true for all ultra-capacitor charge levels.

Due to this reason, the initial (transient) response of both ultra-capacitor based and battery based ride through systems will be almost equal. However, the presence of the low frequency pole-zero pair (especially the low frequency pole) and the low dc gain, will significantly change the latter parts of the waveform of the ultra-capacitor based system from that of the equivalent battery based system.

The magnitude of the low frequency pole (P_{lu}) is seen to be quite large compared to the magnitude of the low frequency RHP zero (Z_{lu}). (Note also that Z_{lu} was considered as located on the origin for controller design process). Hence the pair can not simply be considered as canceling each other. Also the magnitude of P_{lu} is seen to be large enough to affect the response of the ride through system even within a short time period of the order of few seconds. Therefore, if the performance of ultra-capacitor based systems is to be made equal to the performance of an equivalent battery based system, then this low frequency pole (P_{lu}) and the low dc gain should be compensated by the controller.

5.7.2.2. Controller Design and Simulation Results

As per (3-6) it is seen that the gain cross over frequency, ω_{gc} , of the open loop compensated system has an upper limit of 134500 rad/sec for $\varphi_m \geq \pi/4 \text{ rad}$ and $n_{gc} = -1$ for both ultra-capacitor and battery based systems.

Therefore, a suitable Proportional-Integral (PI) type compensator that lies within the above stability conditions, can be determined as described earlier in section 5.4 as,

$$G_{cv} = \left(4 + \frac{24}{s}\right) \quad (5-14)$$

Note that this compensator is selected to approximately cancel the low frequency pole of the ultra-capacitor based system and to improve its dc gain, so that both the ultra-capacitor based and battery based systems can have almost equal performance.

The bode plots of the compensated stable system is given in Fig 5.11. In the figure, $L(s)$ denotes the open loop compensated Bode plot of the complete system, while $L_{mp}(s)$ and $L_{nmp}(s)$ denotes its minimum phase and non minimum phase parts.

Fig 5.11. Bode Plot of the compensated ultra-capacitor based ride through system at initial ultra-capacitor terminal voltages of 250V and 325V.

Note that the system has more than one gain cross over frequency. Therefore, the Bode stability criterion cannot be directly applied to check the stability of the system [96]. The revised Bode stability criterion, given in [96], is employed to check the stability of the system. The revised Bode stability criterion states that a closed-loop system is stable if the open-loop system is stable and the frequency response of the open-loop transfer function has an amplitude ratio of less than unity at all frequencies corresponding to the phase $\phi = -\pi - 2n\pi$, where $n = 0, 1, 2, \dots, \infty$ [96]. From fig 5.11 it is seen that the system has a minimum phase margin of 45 degrees at a gain cross over frequency of 1370 rad/sec, when the initial ultra-capacitor terminal voltage is 325V. The gain cross over frequency changes to 1250 rad/sec and the minimum phase margin becomes 64 degrees when the initial ultra-capacitor terminal voltage reduces to 250V. At all the other initial ultra-capacitor terminal voltages between 325V and 250V, the

system bode plot will lie between these two bode plots given in fig 5.11. Therefore, this system will always have a phase margin over 45 degrees and a gain cross over frequency above 1250 rad/sec in its useful operating region.

Moreover, the system is seen to have three more cross over points, which are stable. Therefore, all four cross over points are stable in the given system at all the useful ultra-capacitor terminal voltage levels. This means the system depicted in fig 5.11 is stable under the revised bode stability criterion.

The simulation results, obtained with MATLAB/SIMULINK software, for the closed loop operation of the system with this compensator under the influence of a loss of supply fault are given in Fig 5.12. Simulation results for an equivalent battery based system operating with a compensator having the same magnitude are also given for comparison.

Fig 5.12. Variation of (a) dc link Voltage (b) Terminal voltage of the energy storage, for initial terminal voltages of 325V and 250V, when controlled using controller $G_{cv}(s)$

The simulation procedure was to maintain the healthy system conditions initially and then to disconnect the source at 0.1 seconds to simulate the isolation of the dc link from the ac source due to a loss of supply fault. When the dc link voltage drops to 617.5 V (V_{min}), gate pulses are applied to the transistor T_1 in Fig 5.4 to start the ride-through operation.

Note that both the ultra-capacitor based (When Initial terminal voltage is 325V) and battery based systems show almost equal transient and steady state responses. The lowest dc link voltage observed immediately after the loss of supply fault is about 615V in both the systems, which is well above the tripping voltage (V_{trip}) of 565.5V. Also the initial overshoot of the battery based and the ultra-capacitor based systems are seen to be almost identical and within the limit of $V_{max} = 715V$. This result is expected as explained in section 5.7.2.1 since the high frequency poles and zeros that govern the transient response of a system are almost identical in the battery based and the ultra-capacitor based systems.

The simulation results for the ultra-capacitor based system when its initial terminal voltage is 250V is also given in fig 5.12. It also shows acceptable response in both transient and steady state conditions. When the ultra-capacitor terminal voltage reaches 195V (minimum ultra-capacitor terminal voltage considered in this example), the duty ratio is held constant, causing the load voltage to decay as shown in fig 5.12.

As a second case, consider the performance of the system given in fig 5.13, when the controller is designed so that it does not compensate the low dc gain and the low frequency pole. The controller used for this simulation is given in (5-15)

$$G_{cv1} = \left(1 + \frac{3}{s}\right) \quad (5-15)$$

Fig 5.13. Variation of (a) dc link Voltage (b) Terminal voltage of the energy storage, for initial terminal voltages of 325V and 250V, when controlled using controller $G_{cv1}(s)$

Note that the initial response of the dc link voltage is again almost identical in both the battery based and the ultra-capacitor based (at 325V) systems. The lowest dc link voltage observed immediately after the loss of supply fault is about 616V in both the systems, which is well above the tripping voltage (V_{trip}) of 565.5V. Also the initial overshoot of the battery based and the ultra-capacitor based systems are seen to be almost equal (about 673V) and within the limit of $V_{max} = 715V$. This result is expected as explained above since the high frequency poles and zeros that govern the transient response of a system are almost identical in the battery based and the ultra-capacitor based systems.

However, in steady state the behaviour of the two systems are drastically different: the ultra-capacitor based system shows a gradually decreasing dc link voltage while the battery based system shows a nearly constant dc link voltage at the rated level (650V). The poor steady state response of the ultra-capacitor based system can be attributed to the presence of the low frequency pole-zero pair and the low dc gain of the ultra-capacitor based system as explained in section 5.4. Moreover, the low frequency closed loop pole associated with P_{1u} causes a slowly decaying transient, which is responsible for the voltage decay observed in the ultra-capacitor based system in Fig 5.13 (a).

Simulation results for the ultra-capacitor based system when the initial terminal voltage is 250V are also given in fig 5.13 for comparison.

5.7.3 Example 2

This example is aimed to demonstrate experimentally that the load voltage slowly decays if the controller is not designed to compensate the low frequency pole and the low dc gain. The equivalent circuit of the experimental setup is similar to the ultra-capacitor based ride through system shown in Fig 5.2, except for the load. Instead of the VSI and the motor load in Fig 5.2, the load consists of an inductance and a resistance in series. The corresponding circuit parameters are given below.

$$C_{uc} = 5F, \quad R_i = 1.6\Omega, \quad L_i = 3mH, \quad C_f = 200\mu F, \quad L_S = 1.8mH, \quad R_S = 5\Omega, \quad E_S = 121.5V, \\ R_L = 120\Omega, \quad L_L = 90mH, \quad E_L = 0V, \quad k_p = 1/24, \quad H = 0.1.$$

The experimental setup is shown in Fig 5.14. The figure shows the combined circuit as well as the enlarged views of boost converter components, ultra-capacitor bank and the load.

Boost Converter Components

Fig. 5.14. Laboratory prototype used for Experiments

An Insulated Gate Bipolar Transistor (IGBT) with a collector to emitter breakdown voltage of 1200V and a continuous collector current rating of 45A was used as the switching device of the boost converter. This switching device is operated at 5kHz to transfer energy from the ultra-

capacitors to the load during the ride through period. A diode with a peak repetitive reverse voltage of 600V and a continuous forward current rating of 22A was used as the diode D_1 of the boost converter. These two components and the output filter capacitance were mounted very close to each other as shown in Fig 5.14, to minimise stray inductance effects.

The 5F ultra-capacitor bank consists of twenty 100F NESSCAP ultra-capacitors connected in series. The voltage rating of a single ultra-capacitor cell is 2.7V. Each ultra-capacitor cell has a continuous current rating of 21.4A. However, they are capable of handling more than 58A when the ultra-capacitors are discharged to half of its terminal voltage within one second.

Hall effect current and voltage transducers, types CSNP661 from Honeywell and LV25-P from LEM, were used to measure the ultra-capacitor current, ultra-capacitor terminal voltage and the load voltage. The measured data is stored in a digital computer and subsequently used for plotting using MATLAB software. The whole process of controlling the converter and data acquisition is performed from DSP (Digital Signal Processor) controller board DS1104, using dSPACE real time test platform which operates in conjunction with MATLAB / SIMULINK software.

The rated load voltage in this setup is 120V. Therefore, based on similar guide lines mentioned under system parameters in section 5.7.1, $V_{\min} = 114V$, $V_{\max} = 126V$ and $V_{trip} = 104.4V$. The fully charged voltage of the ultra-capacitor bank is taken as 48V, and it is assumed to have a useful operating voltage range down to 60% of the full charge value (i.e. 28.8V). The ride-through time specification is again taken as 3 seconds [15]. In order to provide successful ride through for the load, the terminal voltage of the ultra-capacitor bank should be approximately at least 35V prior to the start of any ride through operation.

From the above data, it is seen that the ultra-capacitor bank, once fully charged, is capable of supporting more than 10 ride-through cycles for the load. Therefore, compared to the first example, in which only one and half ride-through cycles were possible, the ultra-capacitor

bank in this example is oversized. Therefore, the low frequency pole-zero pair, P_{1u} and Z_{1u} given in Table 5-2, is seen to be closer to each other compared to the previous example.

TABLE 5-2

Pole-zero positions of open-loop duty-ratio to dc link voltage transfer function

– Example 2

Initial Charge	Ultra-capacitor bank			Battery	
		$\bar{X}_1 = 48 \text{ V}$	$\bar{X}_1 = 35 \text{ V}$		$E_b = 48 \text{ V}$
Poles	P_{1u}	-0.085	-0.1	P_{1b}	$-1131 \pm 993.5i$
	P_{2u}	-903.7	-724.0	P_{2b}	-903.6
	P_{3u}	$-1131 \pm 993.6i$	$-1237 \pm 959.1i$	P_{3b}	-1478.6
	P_{4u}	-1478.7	-1446.7	-	
Zeros	Z_{1u}	0.001	0.002	Z_{1b}	62395
	Z_{2u}	62395	32419	Z_{2b}	-1334
	Z_{3u}	-1333.3	-1333.3	Z_{3b}	-2778
	Z_{4u}	-2778	-2778	-	
Dc gain magnitude		1.2	1.67	96.2	

A compensator for this laboratory setup that satisfies the criterion given in (3-6), but does not compensate the low frequency pole or the low dc gain, can be found as, $G_{cv}(s) = [0.1 + (0.11/s)]$, following the same procedure described in Example 1. The simulation and experimental results obtained for this compensator under a loss of supply fault condition are given below in Fig 5.15. The simulation and experimental procedure was to maintain the healthy dc link voltage and then to disconnect the source at 0 seconds to simulate the isolation of the dc link from the ac source due to a loss of supply fault. When the dc link voltage drops to 114V (V_{min}), gate pulses are applied to the switching device to start the ride trough operation.

(a) Simulation

(a) Experimental result

(b) Simulation

(b) Experimental result

(c) Simulation

(c) Experimental result

Fig 5.15. Simulated and experimental variation of (a) Terminal voltage of the ultra-capacitor bank, (b) Load Voltage for ultra-capacitor based system, (c) Load voltage for constant emf battery based system.

The simulation results are given only for 3 seconds, which is the required ride through time, although the experimental waveforms were captured for more than 7 seconds. Moreover, the load is supplied by a diode rectified dc voltage in the experimental setup, which is similar to the source for a practical ASD.

Both simulation and experimental results given in Fig 5.15, approximately agree with each other. Note that the dc link voltage of the ultra-capacitor based system decays with time in both simulation and experiment, since the low frequency pole and the low dc gain is not compensated, although it stays constant with an equivalent battery based system even for the compensator $G_{cv}(s) = [0.1 + (0.11/s)]$. However the load voltage decay in the ultra-capacitor based system is smaller compared to the previous example since the ultra-capacitor bank is oversized and hence the low frequency pole-zero pair is closer to each other.

As mentioned in Example 1, the steady state behaviour of the ultra-capacitor based system may be improved by employing a compensator that is capable of compensating for the low frequency pole and the low dc gain.

5.8. Minimizing the Effect of the Low Frequency Pole-zero Pair

An open loop pole-zero pair creates an additional branch in the root locus that results in an additional closed loop pole [95]. However, the effects of such closed loop poles on the closed loop response can be minimized by reducing the separation between the open loop pole-zero pair [95].

Hence, if the separation between the low frequency pole-zero pair of the ultra-capacitor based systems can be made smaller, then the influence of the pair on the closed loop system will also be reduced.

Therefore, since the low frequency pole-zero pair cannot be avoided in an ultra-capacitor based system having finite capacitance, the separation between this pair should be minimized by

choosing a suitable control method in order to improve its response closer to the level of an equivalent battery based system.

5.9. Summary

A typical ultra-capacitor based ride through system for an ASD was introduced and analyzed in detail. The ride through system uses a classical boost converter as the interface between the load and the ultra-capacitor bank. Based on an approximate pole-zero analysis and numerical results, it was shown that for designing the controller for the ride through system, the classical model of the ultra-capacitor is sufficient. This is because the classical model is capable of approximately describing the dominant pole and zero of the system, which are the most important roots when designing the closed loop control for any system.

The detailed analysis of the ride through system with the classical model for the ultra-capacitor confirmed the existence of an additional low frequency pole-zero pair in the control to output transfer function. The additional zero (Z_{lu}) is located in the right half plane (RHP) while the additional pole (P_{lu}) is located in the left half plane (LHP). It is also seen that Z_{lu} is much smaller compared to P_{lu} , and hence it may be considered as located on the origin for controller design process.

Therefore, it was shown that the effect of the low frequency pole-zero pair needs to be minimized by some means if the response of the ultra-capacitor based systems are to be improved, perhaps to the level of the constant emf battery based systems. It is seen that, in voltage mode control, this can be achieved by compensating the low frequency pole and the low dc gain of the control to dc link voltage transfer function.

The chapter also analyzed the positions of the low frequency pole-zero pair when the parameters of the ride through system are varied. It was shown that these positions are mainly dependant on the size of the ultra-capacitor bank, the magnitude of the series parasitic

resistance of the boost inductance and the resistance of the source. Moreover, it was also shown that if the size of the capacitor bank is increased, then the low frequency pole-zero pair moves closer to each other, approximately canceling their effects.

Consequently, it can be concluded that if the capacitance of the ultra-capacitor banks were increased, then the systems will approach the behavior of the battery based systems. This will simplify the controller design process, as the controller can be designed assuming an equivalent battery based system, without considering the low frequency pole and the low dc gain. However this would offset some of the cost advantages of using the ultra-capacitors over the batteries, which was in fact the main reason for choosing the ultra-capacitors in the first place. Therefore, the only remaining alternative, to push the ultra-capacitor based system closer to an equivalent battery based system, is to use a different control method, which is capable of minimizing the separation of the low frequency pole-zero pair.

Hence the next chapter looks at two different control configurations that are widely used, the peak current-mode control and the sliding-mode control, and how they affect the low frequency pole-zero pair of the ultra-capacitor based systems. The classical boost converter, which is the simplest and the most efficient converter configuration, is used through out the analysis in order to entirely focus on the benefits of the control configurations.

CHAPTER 6

PEAK CURRENT-MODE CONTROL AND SLIDING-MODE CONTROL OF ULTRA-CAPACITOR BASED RIDE THROUGH SYSTEMS

6.1 Introduction

As concluded in the previous chapters, the low frequency pole and the low dc gain of the ultra-capacitor based systems should be compensated to achieve acceptable steady state performance, when the ultra-capacitor based ride through system is controlled in voltage mode. However, it becomes much easier for the designer, if the control system for the ultra-capacitor based system can be designed similar to an equivalent battery based system, without considering the effects of the low frequency pole zero pair. This is because the control system designs for battery based systems are well established and the relevant literatures are widely available [1, 4, 6-8, 26-28, 97, 98]. This chapter explores the improvements that can be obtained with two control methods towards this objective, namely the peak current-mode control [8] and sliding-mode control [87, 92, 99-101].

As discussed in Chapter 3, peak current-mode control is known to have a number of advantages over the voltage-mode control [8]. The main advantages are the simpler dynamics resulting from the movement of the inductor pole to high frequencies and the in-built over-current protection. In order to implement peak current-mode control, an additional current sensor is required to monitor the inductor current. However, this is not considered as a disadvantage because a current sensor is required even in voltage-mode control to implement over-current protection for the transistor [8].

Apart from the more popular voltage-mode and current-mode control methods, sliding-mode control is another approach that is widely used to control DC-DC converters [69, 85, 86, 93, 102]. Sliding-mode control is based on control techniques derived from variable structure systems theory [87] and it complies with the non-linear nature of DC-DC converters [93]. Sliding-mode control has several advantages such as large signal stability, robustness, good dynamic response and simpler implementation [69].

6.2 Peak Current-mode Control

The schematic diagram of the peak current-mode control of the ultra-capacitor based ride through system is given below in Fig 6.1.

Fig 6.1. Schematic diagram of peak current-mode control of the ultra-capacitor based ride through system

The outer voltage control loop and the inner current control loops of the complete peak current-mode control system are separately shown in Fig 6.1. The output of the voltage loop is used as the reference signal for the inner current loop, and, the transistor T is switched on and off depending on whether the inductor current is below or above this reference.

A well known problem with the peak current-mode control scheme is the instability that is observed for duty ratios greater than 0.5 [8]. A suitably selected artificial ramp signal (m_a) is added to the measured inductor current to eliminate this instability as shown in Fig 6.1 [8].

6.2.1 Peak Current-mode Controller Model and Transfer Functions for an Ultra-capacitor based system

A small signal model for the peak current-mode controller can be developed following the guide lines given in [8] for the ultra-capacitor based ride through system described above. In this analysis the boost inductor current (X_2) was taken as the current feedback signal.

The peak current-mode controller model can be developed as described in [8], considering the relationship between the control input I_c , and the inductor current X_2 as,

$$X_2 = I_c - m_a d T_s - (m_1 d^2 T_s / 2) - (m_2 (1 - d)^2 T_s / 2) \quad (6-1)$$

Where m_a and T_s represent the artificial ramp added to stabilize the control loop and the switching period, respectively, while $m_1 = (X_1 - X_2 R_i) / L_i$ and $m_2 = -(X_1 - X_3 - X_2 R_i) / L_i$.

The small signal current-mode controller model can be found by perturbation and linearization of (6-1) as described in [8]. The result is given in (6-2). Note that m_a and T_s are not perturbed as they are assumed as constant.

$$\tilde{d}(s) = F_m [\tilde{i}_c(s) - \tilde{X}_2(s) - F_g \cdot \tilde{V}_g(s) - F_v \cdot \tilde{X}_3(s)] \quad (6-2)$$

Where,

$$F_g = [T_s (2d_0 - 1) / (2L_i)], \quad F_v = [((1 - d_0)^2 T_s) / (2L_i)], \quad F_m = 1 / [m_a T_s] \quad \text{and}$$

$\tilde{V}_g(s) = \tilde{X}_1(s) - R_i \tilde{X}_2(s)$ is the input dc voltage for the boost converter. This relationship is shown by the dashed lines in Fig. 6.2. The small signal model for the ultra-capacitor based ride through system can now be completed as shown in Fig. 6.2. Note that, H and $G_{cc}(s)$ denote the feed back gain of the dc link voltage and the transfer function of the compensator, respectively. The open loop system transfer functions, $G(s)$, are given in Appendix A.

Fig 6.2. Small signal control block diagram for the ultra-capacitor based ride through system with peak current-mode control.

From this block diagram, the open loop control to output transfer function and the source disturbance to output transfer function can be derived as given in (6-3) and (6-4) respectively.

$$G_{Vcu}(s) = \tilde{V}_{dc}(s) / \tilde{i}_c(s) = \{[F_M G_{Vdu}(s)] / [1 + F_M (G_{X2du}(s) F_I + G_{Vdu}(s) F_v)]\} \quad (6-3)$$

$$G_{Scu} = \frac{\tilde{V}_{dc}(s)}{\tilde{U}(s)} = \frac{[G_{Sdu} - F_M F_g G_{Vdu}(s) G_{X1Uu}(s) + F_M F_I (G_{X2du}(s) G_{Sdu}(s) - G_{Vdu}(s) G_{X2Uu}(s))]}{[1 + F_M (G_{X2du}(s) F_I + G_{Vdu}(s) F_v)]} \quad (6-4)$$

$$\text{Where, } F_I = 1 - \frac{(2d_0 - 1)R_i T_s}{2L_i} \text{ and } F_M = \frac{F_m}{1 + F_m F_g G_{X1d}(s)}$$

General expressions for poles of (6-3) are difficult to derive. However the behavior of the poles under current-mode control can be identified by assuming $L_S \cong 0$ and $d_0 \cong 1$, which are the same conditions under which the first expression for P_{1u} was derived in chapter 5, in voltage-mode control. Under these assumptions, the denominator of (6-3), D_{cu} , can be simplified as given below.

$$D_{cu}(s) = s^3 + a_2 s^2 + a_1 s + a_0 \quad (6-5)$$

Where,

$$\begin{aligned} a_2 &= \left[\frac{R_i}{L_i} + \frac{1}{C_f R_S} \right] + \left\{ \frac{\bar{X}_3 F_m (1 - R_i F_g)}{L_i} - \frac{\bar{X}_2 F_m F_v}{C_f} \right\}, \\ a_1 &= \left[\frac{R_i}{L_i R_S C_f} + \frac{1}{L_i C_{uc}} \right] + \left\{ \left(\frac{\bar{X}_3 F_m (1 - R_i F_g)}{L_i C_f R_S} \right) - \frac{\bar{X}_2 R_i F_m F_v}{L_i C_f} - \frac{\bar{X}_3 F_m F_g}{L_i C_{uc}} \right\}, \\ a_0 &= \left[\frac{1}{C_{uc} L_i C_f R_S} \right] - \left\{ \frac{F_m (F_g \bar{X}_3 + R_S \bar{X}_2 F_v)}{C_{uc} L_i C_f R_S} \right\} \end{aligned}$$

Note that from (6-2), $F_m = \frac{1}{m_a T_s}$, $F_g = \frac{T_s}{2L_i}$ and $F_v = 0$ when $d_0 \cong 1$.

The terms within the '[]' in (6-5) represent the terms that exist even under voltage-mode control. This can be verified by substituting $L_S \cong 0$ and $d_0 \cong 1$ in (A3-7). The other terms within the '{ }' represent the terms added due to current-mode control. Note that, since T_s is very small, F_g can be assumed to be very small and F_m can be assumed as a very high value [8]. Substituting these values in (6-5) results in the following expressions for a_2, a_1 and a_0 .

$$\left. \begin{aligned} a_2 &\approx \left[\frac{R_i}{L_i} + \frac{1}{C_f R_S} \right] + \left\{ \frac{\bar{X}_3 F_m}{L_i} \right\} \\ a_1 &\approx \left[\frac{R_i}{L_i R_S C_f} + \frac{1}{L_i C_{uc}} \right] + \left\{ \left(\frac{\bar{X}_3 F_m}{L_i C_f} \right) \left(\frac{1}{R_S} \right) \right\} \\ a_0 &\approx \left[\frac{1}{C_{uc} L_i C_f R_S} \right] \{ 1 - F_m F_g \bar{X}_3 \} \end{aligned} \right\} \quad (6-6)$$

Note that, in the third order polynomial, a_2 represent the negative of the sum of the roots (summation of poles), a_1 represents the summation of all the possible products of the roots taken two at a time (double pole product) and a_0 represents the negative of the product of all three roots (all pole product) as described in Appendix E1 and E2. Therefore, (6-6) shows that, compared to the voltage-mode control, the magnitude of the summation of the poles and the summation of the double pole product have increased. However, the product of all three poles is seen to be reduced since $0 < (1 - F_m F_g \bar{X}_3) < 1$ should be satisfied for system stability. As was shown in chapter 5, one of the poles in the voltage-mode control was very close to the origin, (P_{1u}), while the other two poles were comparatively far away from the origin. Therefore, the condition in (6-6) can only be met if P_{1u} is made even smaller while the other two poles or one of those poles is pushed far into the LHP. Therefore, current-mode control increases the separation between the system poles and pushes P_{1u} closer to the origin than in voltage-mode control.

Therefore, the separation between P_{1u} and Z_{1u} is smaller in current-mode control than that of voltage-mode control. This means the converter behaviour is closer to an equivalent battery based system under peak current mode control. Therefore, the adverse effects of the low frequency pole zero pair is significantly reduced in peak current-mode control, which can be considered as an advantage when it comes to ultra-capacitor based ride through systems.

However, both voltage-mode and peak current-mode control have several disadvantages including the dependence of the design on circuit parameters and the difficulty in achieving large signal stability without reducing the useful bandwidth. Also design and stabilization of control systems for higher order DC-DC converters is not convenient with these techniques [69].

6.3 Sliding-mode Control

The schematic diagram of the sliding-mode controlled ultra-capacitor based ride through system is given in Fig 6.3. The order of the circuit states is changed here as suggested in [85], so that the currents appear first in the state vector followed by the voltages. The system state matrices for the rearranged state vector are given in Appendix D.

Fig 6.3. Sliding-mode control of ultra-capacitor based ride through system

According to the general sliding-mode control theory, all state variables are sensed, and the corresponding state variable errors are multiplied by proper gains k_n , and added together to form the sliding function ψ . i.e. for a system with N state variables the sliding function is defined as,

$$\psi = \sum_{n=1}^N k_n (X_n - X_{n,ref}) = 0 \quad (6-7)$$

where $X_{n,ref}$ denotes the reference value of n^{th} state.

However as shown in [102], reduced order sliding-mode controllers can also be designed to achieve good system performance in DC-DC converters. Accordingly, Fig 6.3 illustrates a reduced order sliding-mode controller that uses the same number of sensors as of the peak current-mode control [85].

For this system, $N = 4$, $k_1 = k_i$, $k_2 = k_3 = 0$ and $k_4 = k_u$, Therefore,

$$\psi = k_i(X_1 - X_{1,ref}) + k_u(X_4 - X_{4,ref}) = 0 \quad (6-8)$$

The reference for the dc link voltage $X_{4,ref}$ is generated externally. One first order low pass filter (LPF) is added to the system in Fig 6.3 to internally generate the other reference signal $X_{1,ref}$ for the inductor current X_1 . Dynamic equation for this additional state is given by,

$$\dot{X}_{1,ref} = -(1/\tau)X_{1,ref} + (1/\tau)X_1 \quad (6-9)$$

Where τ is the time constant of the first order low pass filter.

Therefore, the addition of the LPF increase the system order by one and the new system state vector becomes,

$$X_{new1} = [X_1, X_2, X_3, X_4, X_{1,ref}]^T \quad (6-10)$$

Prior to the addition of the LPF, the system state vector was given by $X = [X_1, X_2, X_3, X_4]^T$ and the perturbed (ac) state space equation was given in (A1-1) in the Appendix A as,

$$\dot{\tilde{X}} = A \tilde{X} + [(A_1 - A_2)X_0 + (B_1 - B_2)U_0] \tilde{d} + B \tilde{U} \quad (6-11)$$

Therefore, after perturbation and linearization, the perturbed state space equations for the new system with the LPF filter can be derived as [85],

$$\dot{\tilde{X}}_{new1} = A_c \tilde{X}_{new1} + B_c \tilde{U} + D_c \tilde{X}_{4,ref} \quad (6-12)$$

The derivation of (6-12) and the new system matrices A_c , B_c and D_c are given in Appendix D.

However considering the constraint (6-8) , one state variable may be eliminated from (6-12) and hence the final perturbed state space equations for the system can be shown to be given by [85],

$$\dot{\tilde{X}}_{new} = A_T \tilde{X}_{new} + B_T \tilde{U} + D_{T1} \tilde{X}_{4,ref} + D_{T2} \dot{\tilde{X}}_{4,ref} \quad (6-13)$$

Assuming X_1 is eliminated, $X_{new} = [X_2, X_3, X_4, X_{1,ref}]^T$. The matrices A_T , B_T , D_{T1} and D_{T2} in (6-13) are defined in Appendix D. Therefore, the final system order still remains four for the system shown in Fig 6.3. The necessary closed loop transfer functions for sliding-mode control can be derived by taking the Laplace transform of (6-13).

The closed loop control to output transfer function and the disturbance rejection transfer function are given by the element in the fourth row of the following transfer function vectors,

$$G_{XX_{4ref}}(s) = \frac{\tilde{X}(s)}{\tilde{X}_{4,ref}(s)} = (sI - A_T)^{-1} (D_{T1} + sD_{T2}) \quad (6-14)$$

$$G_{XU}(s) = \frac{\tilde{X}(s)}{\tilde{U}(s)} = (sI - A_T)^{-1} B_T \quad (6-15)$$

The open loop system transfer functions remains the same as that of the voltage-mode controlled systems, and hence are not derived here.

6.3.1 Positions of the Low Frequency Pole-zero Pair with Sliding-mode Control

Due to the complexity of the transfer function expressions derived, it is difficult to simplify them further to obtain simple expressions for poles and zeros for the complete ride through system. However, simpler expressions for the system poles and zeros may be derived for the standalone operation of the ride through system (when the source is completely cut off) as shown below.

6.3.1.1 Standalone Transfer Functions and the Low Frequency Pole-zero Pair

The control to output transfer function for the standalone system, which is of order three, can be derived by letting $L_S \rightarrow \infty$ in (6-14) and expanding the equation. The resulting expression for the control to output transfer function can be simplified to a certain extent as shown below.

$$G_{Vd}(s) = K_S \frac{s \left(s + \frac{(1-d_0)^2 I}{C_f (\bar{X}_4 (1-d_0) - IR_i)} \right)}{(s^3 + a_2 s^2 + a_1 s + a_0)} \quad (6-16)$$

Where, $K_S = \frac{-\tau k_u C_f ((1-d_0)\bar{X}_4 - IR_i)}{k_{den}}$ and,

$$a_2 = \frac{(1-d_0)((1-d_0)(k_u \bar{X}_4 + I k_i) - 2k_u IR_i)}{k_{den}} + \frac{(1-d_0)L_i k_u I \tau}{k_{den}}, \quad a_1 = \frac{num_a_1}{(1-d_0)^3 C_{uc} C_f^2 L_i k_{den}},$$

$$a_0 = \frac{(1-d_0)I k_u \tau}{k_{den} C_{uc}}, \quad k_{den} = k_i C_f (\bar{X}_4 (1-d_0) - IR_i) - k_u I L_i (1-d_0),$$

$$num_a_1 = k_u (b_5 + b_4 + b_3 + b_2 + b_1 + b_0),$$

where, $b_5 = C_{uc} \tau L_i C_f^2 (1-d_0)^4 (\tau L_i + (1-d_0)\bar{X}_4),$

$$b_4 = -2C_{uc} \tau^2 k_u k_i I^2 L_i C_f (1-d_0)((1-d_0)\bar{X}_4 - IR_i),$$

$$b_3 = C_{uc} \tau^2 k_i^2 I C_f^2 \bar{X}_4 (1-d_0)((1-d_0)\bar{X}_4 - 2IR_i),$$

$$b_2 = C_{uc} \tau L_i I (1-d_0)^2 (2C_f^2 R_i (1-d_0)^2 + \tau k_u^2 I^2 L_i), \quad b_1 = -I L_i C_f^2 (1-d_0)^4,$$

$$b_0 = C_{uc} \tau^2 k_i^2 I^3 C_f^2 R_i^2.$$

From the expressions of a_2 , a_1 and a_0 it is seen that $k_{den} > 0$ and $num_a_1 > 0$ must be satisfied for system stability. (Otherwise at least one closed loop pole will be located in RHP).

From the numerator of (6-16), it is seen that the low frequency zero of the sliding-mode controlled standalone ultra-capacitor based system is located on the origin. However, numerical results confirm that this zero is always located on the origin even in the sliding mode controlled ultra-capacitor based ride through system.

From the denominator it is seen that by selecting a very small τ , the product of the system poles, which corresponds to the magnitude of a_0 , can be made very small compared to the sum of the poles, which corresponds to the magnitude of a_2 . This means $a_2 \gg a_0$. Moreover, since C_f and L_i are in general in micro Farads and milli Henries, a_1 is usually higher than a_2 . Therefore, the general relationship between the denominator coefficients of (6-16) is $a_1 > a_2 \gg a_0$. Note that, a_1 corresponds to the summation of all possible products of the poles taken two at a time, as explained in Appendix E1 and E2.

Therefore, it is seen that the above relationship of the coefficients can only be achieved if one of the three system poles is located very close to the origin while the other two poles are far away from the origin. This shows that by selecting a suitably small τ , the low frequency pole of the sliding-mode controlled ultra-capacitor based systems can be pushed closer to the origin. Since the low frequency zero is exactly located on the origin, this shows that the sliding-mode controlled ultra-capacitor based systems are capable of canceling out the low frequency pole-zero pair with a higher accuracy. This makes the sliding mode controlled ultra-capacitor based systems almost identical to equivalent battery based systems.

However, the selected k_u , k_i and τ should satisfy $k_{den} > 0$ and $num_a_1 > 0$ to ensure system stability.

6.3.1.2. Comment on the Low Frequency Pole-zero Pair

The analysis shows that the low-frequency zero of the control to output transfer function of the ultra-capacitor based ride through system is located on the origin.

It also shows that the standalone system has three LHP closed loop poles. One of these poles lies very close to the origin compared to the other two. Furthermore, it is also seen that the position of this low frequency pole may be shifted very close to the origin by selecting a suitably small time constant, τ , for the first order low pass filter. However the selection of τ is

not arbitrary, as τ and also the sliding-mode coefficients k_u and k_i , should satisfy the two inequalities mentioned above in section 6.3.1.1 to ensure closed loop system stability.

Therefore, the low frequency pole of the system is in general pushed closer to the origin with sliding-mode control compared to the peak current-mode control. Since the low frequency zero is also exactly located on the origin, the cancellation of the low frequency pole-zero pair in closed loop is achieved with relatively higher accuracy under sliding-mode control compared to peak current-mode control. This significantly improves the properties of the ultra-capacitor based ride through systems to the level of battery based systems. Hence the controllers for sliding mode controlled systems can be designed similar to an equivalent battery based system.

6.4 Illustrative Examples

To demonstrate the differences in the performance of the ultra-capacitor based ride through system with the three control methods, namely voltage-mode, peak current-mode and sliding-mode, two examples are presented in this section. In these examples, the functioning of the ride through system during a fault in the ac source is the same as described in section 5.5.

6.4.1 Illustrative Example 1:

Consider an ultra-capacitor based ride through system with the following numerical values for the circuit components and for the various parameters of the three control methods described above.

$$C_{uc} = 1F, \quad R_i = 0.5\Omega, \quad L_i = 2.4mH, \quad C_f = 2200\mu F, \quad L_S = 0.735mH, \quad R_S = 0.077\Omega, \\ E_S = 650.5V, \quad I = 5.42A, \quad V_{dc} = 650V, \quad k_p = 1/50, \quad H = 0.17/2, \quad T_s = 1/5000, \quad k_i = 0.6, \quad k_u = 0.5, \\ \tau = 0.015.$$

The full charge ultra-capacitor bank voltage is taken as 325V. It is assumed that the ultra-capacitor bank has a useful voltage range of 40% of the fully charged voltage. Therefore the minimum allowable voltage of the ultra-capacitor bank is 195V. The external ramp m_a of peak current-mode control was assumed as half of m_2 to ensure stability for duty ratios greater than 0.5 [8]. A fully charged ultra-capacitor bank is assumed when calculating m_2 to determine this m_a .

The ride through specification for the system is assumed as 3 seconds [15]. Therefore, by considering the remaining energy on the ultra-capacitor bank, it can be seen that in order to provide successful ride through for the load, the terminal voltage of the ultra-capacitor bank should be more than 250V prior to the start of any ride through operation. It is also seen that the given ultra-capacitor bank could support about 1.5 ride through cycles to the load without recharging.

The positions of P_{1u} and Z_{1u} of the ride through systems can be obtained for the three control methods using the above parameters, from the procedures described earlier in section 5.2.1, 6.2.1 and 6.3.1. Although P_{1u} and Z_{1u} can be calculated using approximate expressions for voltage-mode control, they can only be calculated numerically for the other two methods. The results for the open loop systems for the maximum and minimum initial ultra-capacitor voltages are given in Table 6.1.

Table 6.1: Positions of P_{1u} and Z_{1u} in open loop system for Example 1

Initial ultra-capacitor (V)	Voltage-mode		Peak current-mode		Sliding-mode	
	P_{1u}	Z_{1u}	P_{1u}	Z_{1u}	P_{1u}	Z_{1u}
325	-1.95	0.018	-0.02	0.018	-1.95	0.018
250	-1.98	0.03	-0.015	0.03	-1.98	0.03

Note that in voltage-mode, P_{1u} is about hundred times away from the origin compared to Z_{1u} . This means the ratio, $K_{pz} = \left| \frac{P_{1u}}{Z_{1u}} \right|$, is about 100. The ratio remains almost the same from the maximum initial ultra-capacitor voltage (325V) down to the minimum (250V). But in peak current-mode, P_{1u} is pushed significantly closer to the origin although Z_{1u} remains at the same position for all useful initial ultra-capacitor charge levels. Therefore K_{pz} is reduced significantly and it is seen to lie between 1 and 2 for the entire ultra-capacitor terminal voltage range from 250V to 325V. Since the other poles and zeros of the system (not shown), are located very far from the origin and, P_{1u} and Z_{1u} itself have very small magnitudes, the two may be assumed as canceling each other for all practical purposes in peak current-mode control. Therefore, the ultra-capacitor based ride through systems operated with peak current-mode control should behave similarly to their battery based counterparts. On the other hand, the open loop system in sliding-mode control is the same system observed in voltage-mode control. Therefore, there is no difference in the pole-zero positions of those two in open loop. The positions of the dominant pole and zero in the closed loop system are given in Table 6.2.

Table 6.2 Positions of dominant poles and zeros in the closed loop system for Example 1

Initial ultra-capacitor (V)	Voltage-mode		Peak current-mode		Sliding-mode	
	P_{dom}	Z_{dom}	P_{dom}	Z_{dom}	P_{dom}	Z_{dom}
325	-1.8	0.018	-0.02	0.018	-1.5E-6	0
250	-1.86	0.03	-0.015	0.03	-1.5E-6	0

Both Voltage-mode and peak current-mode have a compensator in their closed loop control system. These compensators alter the pole-zero map of the system by adding poles and zeros to the system. However sliding-mode control does not use such a compensator. In order to make a

fair comparison with sliding-mode control these compensators of voltage-mode and peak current-mode were assumed to be unity in deriving Table 6.2.

From Table 6.2 it is seen that the separation between the dominant closed loop pole and zero in voltage-mode control is still large. The time constant of the dominant closed loop pole, which is given by $1/P_{dom}$, is seen to be 0.55 sec when the ultra-capacitor terminal voltage is 325V while it is 0.54 sec when the ultra-capacitor terminal voltage is 250V. Therefore, the decaying response of this pole will still be significant even within a small ride through period of a few seconds. Therefore, the closed loop steady state performance of the ride through system can be affected by the low frequency pole-zero pair under voltage-mode control, unless its effects are not properly compensated.

The dominant closed loop pole and zero in peak current-mode control given in Table 6.2 are almost identical to the positions of P_{1u} and Z_{1u} for the same control method in Table 6.1. Note that a transient having a very small magnitude still exists in peak current-mode control. However it has a very large time constant of about 50 seconds, which is much larger than the required ride through time. Hence, even if this pole is left uncompensated by the controller, the decay in voltage within the ride through time may not be very significant.

For sliding-mode control, the closed loop dominant pole is almost on the origin while the zero is exactly on the origin. Therefore, the pair can be assumed as cancelled more accurately than in peak current-mode control. Consequently, the response of the closed loop system should be identical to the equivalent battery based system.

Therefore, the ultra-capacitor based ride through systems controlled with peak current-mode and sliding-mode control may be designed in the same way as designing an equivalent battery based systems, without considering the effects of P_{1u} and Z_{1u} , caused by the finite capacitive effects of the ultra-capacitors.

6.4.1.1 Simulation Results

The following simulation results were obtained using MATLAB / SIMULINK software to verify the conclusions made above. For Voltage-mode control simulations, a stable PI compensator, $G_{cv}(s) = [1 + (4.5/s)]$ that do not compensate the low frequency pole or the low dc gain, was designed as described in Chapter 5. For peak current-mode control, the compensator $G_{cc}(s) = [20 + (400/s)]$, was designed in the usual way by assuming an equivalent battery based system [8].

For sliding-mode control, the values of k_i , k_u and τ were given under system parameters above. The width of the hysteresis band was selected as 2. Note that the width of the hysteresis band affects the switching frequency and the ripple in voltage and current waveforms [85].

The simulation procedure was to maintain the healthy system and then to disconnect the source circuit to simulate a loss of supply fault. When the dc link voltage drops below 95% of the rated value (617.5V) the ride through system is triggered and the gate pulses are applied to the switch to start the ride through operation.

Fig 6.4 and Fig 6.5 show the system performance for the three control methods when the initial ultra-capacitor voltage is 325V and 250V respectively, while Fig 6.6 shows the corresponding ultra-capacitor terminal voltage variations. In both Fig 6.4 and 6.5, Fig (a) compares voltage-mode control with peak current-mode control while Fig (b) compares voltage-mode control with sliding-mode control.

As seen in Fig 6.4 and 6.5, the dc link voltage shows an increasing error with time in voltage-mode control, since the low frequency pole or the low dc gain is not properly compensated. This behaviour holds for both initial ultra-capacitor terminal voltages of 325V and 250V. However in peak current-mode control and sliding-mode control the dc link voltage is almost maintained constant throughout the ride through period, similar to the response of an equivalent battery based system, although the ultra-capacitor terminal voltage drops with time

as shown in Fig 6.6. This is because the low frequency pole-zero pair caused by the finite capacitive effects of the ultra-capacitors is almost cancelled at all ultra-capacitor terminal voltage levels in these two control methods.

These observations agree with the conclusions made earlier in section 6.4.1.

Fig 6.4. Comparison of dc link voltage vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 325V

Fig 6.5. Comparison of dc link voltage vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 250V

Fig 6.6. Comparison of ultra-capacitor terminal voltages under Voltage-mode, Peak Current-mode and Sliding-mode control

The system with peak current-mode control does not show any overshoot while the sliding-mode and voltage-mode controlled system shows an overshoot. The system controlled by sliding-mode control is also seen to be faster than peak current-mode system. However all these transient properties are attached to the high frequency behavior of the systems and hence are not related to the forgoing discussion on low-frequency behaviour.

The corresponding ultra-capacitor current variations are given below in Fig 6.7 and Fig 6.8. The waveforms in Fig 6.7 correspond to initial ultra-capacitor terminal voltage of 325V while Fig 6.8 shows the waveforms for the initial ultra-capacitor terminal voltage of 250V. The current in voltage-mode control varies as per the variations in the load voltage shown in the above figures. The current in peak current-mode and sliding-mode control show a smooth response although it increases with time due to the decreasing terminal voltage of the ultra-capacitors.

Fig 6.7. Comparison of ultra-capacitor current vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 325V

Fig 6.8. Comparison of ultra-capacitor current vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 250V

The equivalent battery based ride through system for this example will have a battery with a constant emf of 325V in place of the ultra-capacitors. The simulation results for such a battery based ride through system with all the other parameters unchanged are given below in Fig 6.9 and Fig 6.10.

Fig 6.9. Comparison of dc link voltage vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, for a battery with a constant emf of 325V

The load voltage waveform of the constant emf battery based system is identical with the corresponding load voltage waveforms of the ultra-capacitor based system shown for the peak current-mode and sliding-mode control. However there is a significant difference in the load voltage waveforms of the battery based and ultra-capacitor based systems under voltage-mode control. In the battery based system the terminal voltage under voltage-mode control remains at the rated voltage (650V) during the ride through time. In contrast, it was seen decaying continuously in the equivalent ultra-capacitor based system.

6.4.2 Illustrative Example 2:

This example is based on the laboratory experimental setup described in section 5.6.2 in Chapter 5. The equivalent circuit of the experimental setup is similar to the ultra-capacitor based ride through system shown in Fig 5.2, except for the load. Instead of the VSI and the motor load in Fig 5.2, the load in this example is a series RL load. The corresponding circuit parameters are given below.

$C_{uc} = 5F$, $R_i = 1.6\Omega$, $L_i = 3mH$, $C_f = 200\mu F$, $L_S = 1.8mH$, $R_S = 5\Omega$, $E_S = 121.5V$,
 $R_L = 120\Omega$, $L_L = 90mH$, $k_p = 1/24$, $H = 0.1$, $T_s = 1/5000$, $k_i = 2.5$, $k_u = 2$, $\tau = 0.015$

All these parameters, except the source parameters, (i.e. L_S , R_S and E_S), are measured or set values of the experimental setup. The source parameters were estimated based on the guidelines given in [18]. The value of R_S also includes an added resistance in the experimental setup to limit charging currents of C_f at the start up.

The rated load voltage in this example is 120V. Therefore, based on the same guidelines adopted in section 5.5 , different voltage levels are selected as, $V_{min} = 114V$, $V_{max} = 126V$ and $V_{trip} = 104.4V$. The fully charged voltage of the ultra-capacitor bank is 48V. The ultra-capacitor bank is assumed to have a useful operating voltage range down to 60% of the full charge value, which is 28.8V. The ride-through time specification is again taken as 3 seconds [15]. In order to provide successful ride through for the load, the terminal voltage of the ultra-capacitor bank should be approximately at least 35V prior to the start of any ride through operation.

From the above data, the positions of P_{1u} and Z_{1u} of the open-loop ride through system for the three control methods can be obtained as given in Table 6.3.

Table 6.3 Positions of P_{1u} and Z_{1u} in open loop system for Example 2

Initial ultra-capacitor (V)	Voltage-mode		Peak current-mode		Sliding-mode	
	P_{1u}	Z_{1u}	P_{1u}	Z_{1u}	P_{1u}	Z_{1u}
48	-0.085	0.0013	-0.0025	0.0013	-0.085	0.0013
35	-0.1	0.0025	-0.0018	0.0025	-0.1	0.0025

It is seen that both P_{1u} and Z_{1u} are smaller under all control methods compared to the previous example. This is because the ultra-capacitor bank in this system is oversized and

therefore it behaves closer to an equivalent battery based system. However, in voltage-mode control it is seen that $|P_{1u}| \gg |Z_{1u}|$, while in peak current-mode control P_{1u} and Z_{1u} are of the same order. The poles and zeros are the same for sliding-mode and voltage-mode control in open loop.

The corresponding positions of the dominant poles and zeros in the closed loop system for the three methods are given in Table 6.4.

Table 6.4 Positions of dominant poles and zeros in closed loop system for Example 2

Initial ultra-capacitor (V)	Voltage-mode		Peak current-mode		Sliding-mode	
	P_{1u}	Z_{1u}	P_{1u}	Z_{1u}	P_{1u}	Z_{1u}
48	-0.063	0.0013	-0.002	0.0013	-4.50E-07	0
35	-0.074	0.0025	-0.0014	0.0025	-4.50E-07	0

The separation between the dominant pole and the zero in the closed loop system using voltage-mode control is seen to be lower than in open loop system. But the separation still remains large since $30 < K_{pz} < 50$ for all ultra-capacitor charge levels from 35V to 48V. Therefore, a small decaying transient having a varying time constant between 13.5 and 15.9 sec should prevail in the output load voltage, if not properly compensated. In peak current-mode control, the separation between P_{1u} and Z_{1u} has been reduced only slightly. The time constant of a possible low frequency transient is therefore seen to be very large in peak current-mode control, of the order of 500 seconds. Under sliding-mode control, both P_{1u} and Z_{1u} remain almost on the origin, therefore their effects are almost cancelled with each other. This shows that, although the effect of the dominant pole-zero pair prevails under the voltage-mode control, the effect may be assumed negligible under the peak current-mode control and the sliding-mode control. These results agree with the conclusions derived from the illustrative example 1.

6.4.2.1 Simulation Results

The following simulation results were obtained using MATLAB / SIMULINK software for this example. For Voltage-mode control a stable PI compensator, $G_{cv}(s) = -[0.1 + (0.11/s)]$, was designed as described in Chapter 5, so that it does not compensate for the low frequency pole or the low dc gain. For peak current-mode control, the compensator $G_{cc}(s) = -[8 + (300/s)]$ was designed in the usual way by assuming an equivalent battery based system [8].

The simulation procedure was to maintain the healthy system and then to disconnect the source circuit to simulate a loss of supply fault. When the dc link voltage drops below 95% of the rated value (114V) the ride through system is triggered and gate pulses are applied to the switch to start the ride through operation.

Fig 6.10 and Fig 6.11 show the load voltage waveforms for the three control methods when the initial ultra-capacitor voltage is 48V and 35V respectively, while Fig 6.12 shows the variation of terminal voltage of ultra-capacitor bank. As shown in Fig 6.10 and Fig 6.11, the dc link voltage gradually decays with time in voltage-mode control, because the low frequency pole or the low dc gain is not properly compensated. Note that the decay is seen to be smaller compared to the first example since the ultra-capacitor bank is oversized. However in peak current-mode control and sliding-mode control, the dc link voltage is almost maintained constant throughout the ride through period, similar to the response of an equivalent battery based system. This is because the low frequency pole due to the ultra-capacitors is almost cancelled with the low frequency zero in these two control methods. These observations agree with the conclusions made above in example 1.

Fig 6.10. Comparison of dc link voltage vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 48V

Fig 6.11. Comparison of dc link voltage vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 35V

Fig 6.12. Comparison of ultra-capacitor terminal voltages under Voltage-mode, Peak Current-mode and Sliding-mode control

The corresponding ultra-capacitor current variations are given below in Fig 6.13 and Fig 6.14. The variation of the ultra-capacitor current follows the same pattern described above in Example 1.

Fig 6.13. Comparison of ultra-capacitor current vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 48V

Fig 6.14. Comparison of ultra-capacitor current vs time for (a) Voltage-mode and Peak current-mode control (b) Voltage-mode and Sliding-mode control, at the initial ultra-capacitor terminal voltage of 35V

The equivalent battery based ride through system for this example will have a battery with a constant emf of 48V in place of the ultra-capacitors. The simulation results for such a battery based ride through system with all the other parameters unchanged are given below in Fig 6.15.

Fig 6.15. Comparison of load voltage vs time for Voltage-mode, Peak Current-mode and Sliding-mode control for a battery with a constant emf of 48V

Note that, similar to the results in Example 1, the equivalent voltage-mode controlled battery based system in Example 2 also reaches the rated load voltage of 120V without showing load voltage decay as in voltage-mode controlled ultra-capacitor based systems.

The steady state load voltage waveform for battery based and ultra-capacitor based systems are almost equal under sliding-mode and peak current-mode control methods, since in these methods the low frequency pole-zero pair found in ultra-capacitor based systems is almost cancelled.

6.5. Comment on the Results of Illustrative Examples

The output load voltage of the voltage-mode controlled ultra-capacitor based ride through systems show a gradual decay with time, unless the low frequency pole and the low dc gain is properly compensated. However the equivalent battery based ride through systems does not show such decay and it is seen that they always maintain the expected output voltage in steady state. This behavior can be explained by the low frequency pole-zero pair that is present only in ultra-capacitor based systems as discussed in Chapter 5.

The separation between the low frequency pole-zero pair is highest under voltage-mode control. The separation also increases when the size of the ultra-capacitor bank is minimized due to cost considerations. Therefore, the low frequency transient associated with the low frequency closed loop pole added due to the pole-zero pair, can be significant in steady state in most of the practical ultra-capacitor based systems. However the equivalent battery based systems do not contain such a low frequency pole-zero pair that affects its steady state. Therefore, they do not show such a decaying response with time at its output.

Peak current-mode control and sliding-mode control push the low frequency pole-zero pair of the ultra-capacitor based systems closer to the origin as explained earlier, so that they can be considered as cancelled under practical conditions. The cancellation is almost exactly achieved

in closed loop with sliding-mode control although in peak current-mode control the cancellation can only be considered as approximate. However the time constant of the low frequency transient associated with peak current-mode control is very large. Therefore, it does not affect the system output within the required ride through time, which is in the order of a few seconds. As explained earlier in Chapter 5, once the low frequency pole-zero pair is cancelled, the transfer functions of the ultra-capacitor based systems are identical to battery based systems and hence the two systems should behave in the same way. This is the reason for almost identical output load voltage waveforms for the ultra-capacitor based and battery based ride through systems under peak current-mode control and sliding-mode control in the above illustrative examples.

6.6 Experimental Results

Experimental results were obtained for the laboratory setup that has the same parameters mentioned for illustrative example 2. The details of the experimental setup were given in section 5.6.3 in Chapter 5. The control signals for the converter were generated from the dSPACE1104 real time test platform, which operates in conjunction with MATLAB/SIMULINK software. The experimental procedure is identical to the simulation procedure described above.

6.6.1 Experimental Results for Voltage-mode Control

Fig 6.16, Fig 6.17 and Fig 6.18 show the experimental waveforms obtained for voltage-mode control. The maximum duty ratio of the switching device in the experimental setup was set at 0.9 for safety. The ultra-capacitor terminal voltage waveforms given in Fig 6.16 include the voltage drop across its equivalent series resistance. This resistance was considered together

with R_i in the analysis performed in the preceding chapters. The experimental waveforms also show high frequency spikes, which are due to parasitic inductances in circuit wiring.

Fig 6.16. Experimental ultra-capacitor terminal voltage variation for voltage-mode control

Fig 6.17. Experimental load voltage variation for voltage-mode control

Fig 6.18. Experimental ultra-capacitor current variation for voltage-mode control

The inductive load in the experimental setup is supplied by a diode rectifier and its output voltage contains a ripple of about 5V as shown in Fig 6.17. At $t = 0$ seconds, the source to this diode rectifier is tripped to simulate a loss of supply fault. As can be seen from Fig 6.17 the load voltage maintained by the voltage-mode controlled ride through system subsequently decays with time as observed in simulation results given in Fig 6.10 and Fig 6.11.

6.6.2 Experimental Results for Peak Current-mode Control

Fig 6.19, Fig 6.20 and Fig 6.21 show the experimental waveforms obtained for the same system when peak current-mode control is used.

At $t = 0$ seconds, the source to the diode rectifier is tripped to simulate the loss of supply fault. As can be seen from Fig 6.20 the subsequent load voltage, which is maintained by the peak current-mode controlled ride through system, does not decay with time as the voltage-mode controlled system described in section 6.6.1. Moreover, the constant load voltage behaviour holds for both the initial ultra-capacitor terminal voltages 35V and 48V.

Fig 6.19. Experimental ultra-capacitor terminal voltage variation for Peak current-mode control

Fig 6.20. Experimental load voltage variation for Peak current-mode control

Fig 6.21. Experimental Ultra-capacitor current variation for Peak current-mode control

Peak current-mode control is highly sensitive to the high frequency noise in the current measurement circuits. Due to this, the waveforms given in Fig 6.19 to Fig 6.21 is seen to contain more high frequency distortion compared to the voltage-mode control waveforms given in Fig 6.16 to Fig. 6.18. These additional high frequency components discharge the ultra-capacitor bank faster compared to voltage-mode control. As a result, the ride through time is less than 3 seconds when initial ultra-capacitor bank terminal voltage is 35 V for this experimental setup. Apart from these deviations, the experimental results given above approximately agree with the simulation results for the peak current-mode control given in Fig 6.10 and Fig 6.11.

6.6.3 Experimental Results for Sliding-mode Control

The response of the same system when controlled with sliding-mode control is shown below in Fig 6.22, Fig 6.23 and Fig 6.24. It is seen from Fig 6.23 that the load voltage is maintained constant throughout the ride through time without showing any decay. Moreover, the steady

state load voltage waveforms are seen to be superior compared to the peak current-mode waveforms given in Fig. 6.20.

These results agree with the conclusions made earlier from simulation results.

Fig 6.22. Experimental ultra-capacitor terminal voltage variation for sliding-mode control

Fig 6.23. Experimental load voltage variation for sliding-mode control

Fig 6.24. Experimental ultra-capacitor current variation for sliding-mode control

The switching frequency under sliding-mode control varies with time while it remains constant in voltage-mode control. As a result, the converter under sliding-mode control operates with a lower switching frequency than in voltage-mode control or peak current-mode control during the initial period. Due to this reason the initial response of the sliding-mode controlled system shown in Fig 6.22 to Fig 6.24 shows a higher ripple in the waveforms compared to voltage-mode waveforms. This causes fast discharge of the ultra-capacitors as it draws additional energy from the ultra-capacitors. Therefore, the ride through period observed when initial ultra-capacitor voltage is 35V is less than 3 seconds in sliding-mode control, although it was exactly 3 seconds under voltage-mode control.

6.7 Summary

In this chapter, two control methods, namely the peak current-mode control and sliding-mode control, were analyzed when used to control ultra-capacitor based systems. Ultra-capacitor

based ride through system introduced in Chapter 5 was used for the analysis.

The analysis has shown that both peak current-mode control and sliding-mode control are capable of reducing the separation between the low frequency pole-zero pair of the ultra-capacitor based systems considerably, so that their effect on the closed loop system is minimized.

With peak current-mode, however, it is seen that only the low frequency LHP pole is pushed towards the origin while the low frequency RHP zero remains at the same position as of the voltage-mode controlled system. However, since RHP zero is, in any case, very close to the origin than the LHP pole, the movement of the LHP pole has a very significant effect when minimizing the effect of the low frequency pole-zero pair. On the other hand, sliding-mode control pushes the low frequency zero to the origin while the LHP pole is pushed almost to the origin. Therefore, the low frequency pole-zero pair cancellation is almost exactly achieved with sliding-mode control than peak current-mode control. Therefore, the sliding-mode control can be considered more suitable for ultra-capacitor based systems than the peak current-mode control.

Since the low frequency pole zero pair is almost cancelled, the ultra-capacitor based ride through systems are almost identical to their equivalent battery based systems. Hence the controllers for the peak current mode controlled or the sliding mode controlled ultra-capacitor based ride through systems may be designed considering an equivalent battery based system, without considering the effects of the low frequency pole zero pair.

Two important advantages that peak current-mode control has are the inbuilt peak current limiting and the fixed switching frequency. Although they can not be considered as specific advantages for ultra-capacitor based systems, these features are preferable in any power electronic converter for the safety of the switching devices and for to the considerations of

acoustic noise and filter designing [1]. The sliding-mode controlled system described above does not have these features, although they may be easily incorporated as described in [69].

When ride through systems are considered, a very important advantage of sliding-mode control over the peak current-mode control is the fast response. This is because sliding-mode controllers act on all the controlled system states simultaneously [69], and try to bring all of them close to their respective reference values. Therefore, the system reaches its steady state faster than other control methods. On the other hand peak current-mode control tries to bring the output load voltage to the reference value while limiting the inductor current to a set maximum value. Therefore, it takes a longer time to reach steady state compared to sliding-mode control. This behavior of the two control methods is evident from the comparison simulation results given above in this chapter.

The recently introduced Z-source inverters are ideally suited for ultra-capacitor based applications since they are capable of interfacing variable voltage sources to ac loads demanding a constant voltage at its terminals. The next chapter gives a detailed description of all the possible operating states of these Z-source inverters. It also describes two methods that can be used to design the unique impedance network of the Z-source inverters for a given variable voltage source and a given load.

CHAPTER 7

DESIGNING A SYMMETRICAL IMPEDANCE NETWORK FOR Z-SOURCE INVERTERS

7.1 Introduction

During recent years the use of variable voltage sources such as fuel cells and ultra-capacitors have increased significantly in power quality applications. Consequently, a need has arisen to design inverters which can operate successfully with these variable voltage sources. The conventional Voltage Source Inverter (VSI), which is the most commonly used inverter, suffers from the drawback that it cannot boost the voltage of the input source. Thus, a separate voltage-boosting DC-DC converter is needed to interface the variable-voltage source with the conventional VSI. This cascaded arrangement of two power converters increases not only the complexity of circuitry and control but also the cost and the space requirement. In order to satisfy the pressing needs for a single converter capable of both voltage boosting and inversion, many new inverter topologies have been proposed in the recent past [17, 103]. Among these new topologies, Z-Source Inverter (ZSI) appears to be gaining popularity over the others mainly because it continues to employ a conventional VSI as the power converter yet with a modified dc link stage [17, 104]. Although ZSI is the most widely researched Z-Source converter configuration at present, the Z-Source principle can be applied to all converter types such as, DC-DC, DC-AC, AC-DC and AC-AC, operating with either voltage sources or current sources [17].

As illustrated in Fig. 7.1, a diode (D_s) and an impedance network connected between the variable dc voltage source and the conventional VSI are the main differences in the power circuit of a ZSI. As seen in Fig. 7.1, the impedance network of the ZSI consists of two identical inductors and two identical capacitors connected in a specific manner. This impedance network

need not necessarily be symmetrical, although a symmetrical impedance network is considered in most cases for simplicity [17].

The impedance network changes the circuit configuration from that of a voltage source to an impedance source (i.e. Z-source). It allows the VSI to be operated in a new state called the shoot-through state in which the two switching devices in the same inverter leg are simultaneously switched-on to effect a short-circuit of the dc link. During this state, energy is transferred from the capacitors to inductors, thereby giving rise to the voltage-boost capability of the ZSI. As the capacitors may be charged to higher voltages than the input source voltage, the diode D_s is necessary to prevent discharging of them back through the input source.

Fig.7.1. Z-source inverter with an input voltage source.

Currently available literature on ZSI [17, 29-31, 88, 89, 105-107], mainly focuses on the control of the switching devices of the VSI to maximize the voltage-boost ratio while minimizing the device stresses. However, little or no effort has been made to study the behaviour of the impedance network and to provide any guidelines to size its components. The objective of this chapter is to provide a clear analysis of the steady-state operation of the impedance network of the ZSI and to provide simple design guidelines to size this inductor and the capacitor.

The next section of this chapter provides a detailed analysis of all the possible states of ZSI. Since the main attention is given to design the impedance network, a battery based Z-source inverter is considered for this initial analysis. The equations derived in this section are then used to accurately design the impedance network for a ZSI that is operating with only two circuit states. However, due to the resulting mathematical complexity in solving these equations, an approximate, yet much simpler method of designing the impedance network is also presented. Computer simulations are used to verify the accuracy of the design process for an illustrative example.

Finally, the analysis is extended to the Ultra-capacitor based Z-source inverter, mainly to study the positions of the low frequency pole-zero pair and the methods that can be adopted to minimize its effects on the Ultra-capacitor based Z-source inverter performance.

7.2 Operating states of the impedance network

The operating state of the impedance network is decided by the switching states of the semiconductor devices on its input and output terminals. As illustrated in Fig. 7.2, the diode D_s on its input side has two switching states as 'On' and 'Off' and the VSI on its output side has three switching states as 1, 2 & 3. In the state 1, which is known as 'Open' state [17, 30], VSI applies one of the two zero switching vectors to the load while open circuiting its input terminals. Similarly, in the state 2, known as 'Active' state [17, 29, 30], VSI applies one of the six non-zero switching vectors to the load while drawing a load dependant current from its input source. Assuming the load impedance to be inductive, the current drawn from the impedance network during this state can be represented by a constant current source I_0 [1, 17]. A conventional VSI can only be operated in these two input states. However with the impedance network on the dc link, the VSI of the Z-source inverter can be operated in a third input state, which is known as the 'Shoot-Through' state [17, 29, 30]. During this state, input

terminals of the VSI are effectively short-circuited by switching on the devices at the top and bottom of at least one of its three legs.

Fig. 7.2 Switching equivalent of Z-source inverter.

Thus, in general, the impedance network of the ZSI at a given time can operate in any one of the six possible states given in Table 7.1.

TABLE 7.1

Possible operating states of the impedance network

VSI Input State	Open		Active		Shoot-Through	
Diode Ds	On	Off	On	Off	Off	On
State of Impedance Network	Open-1	Open-2	Active-1	Active-2	Shoot Through-1	Shoot Through-2

During a switching cycle of the VSI, the impedance network may operate in up to a maximum of six states. However, as it will be seen later, the Open-1, Active-1 and Shoot-Through-1 states are the desired states in practical applications. The three states, Open-2, Active-2 and Shoot-Through-2 are undesirable and are to be avoided by proper sizing of the inductors and capacitors of the impedance network.

Prior to analyzing the voltage-current variations in each of the six possible states, the common equations that describe the impedance network in general can be identified as,

$$V_L = L(dI_L / dt); \quad I_C = C(dV_C / dt) \quad (7-1)$$

$$V_s = V_c + V_L; \quad I_s = I_c + I_L \quad (7-2)$$

$$V_i = V_c - V_L; \quad I_i = I_L - I_c \quad (7-3)$$

where V_L and I_L are the voltage across and current through any of the two inductors, V_c and I_c are the voltage and current of any of the capacitors, V_s and I_s are the voltage and current at the input terminals of the impedance network connected to the source through the diode and V_i and I_i are the voltage and current at the output terminals connected to the VSI. The characteristics of the six operating states can be described separately as given in the following subsections.

7.2.1 Open-1 State

The equivalent circuit of the ZSI during the Open-1 state is shown below in Fig. 7.3.

Fig. 7.3. Equivalent circuit of Z-source inverter during Open-1 state.

The equations that define the Open-1 state are given by,

$$V_s = E_s \text{ and } I_i = 0 \quad (7-4)$$

By substituting (7-4) in (7-1)-(7-3), the voltage across the capacitor and its current can be expressed as given in (7-5), by solving the resulting second order differential equation

$$\frac{d^2 V_c}{dt^2} + \frac{V_c}{LC} = \frac{E_s}{LC}.$$

$$V_c = E_s + X_o \cdot \sin(\omega t + \phi_o) \quad (7-5)$$

$$I_c = I_l = I_s / 2 = X_o \omega C \cdot \cos(\omega t + \phi_o) \quad (7-6)$$

$$\text{where } \omega = \sqrt{LC} \quad (7-7)$$

$$X_o = \sqrt{(V_{cio} - E_s)^2 + [I_{lio} / (C\omega)]^2} \quad (7-8)$$

$$\phi_o = \tan^{-1}((V_{cio} - E_s)\omega C / I_{lio}) \quad (7-9)$$

with the initial values of capacitor voltage and inductor current in Open-1 state denoted by V_{cio} and I_{lio} respectively. With positive values of V_{cio} and I_{lio} , the range of the initial angle is $\phi_o < \pi/2$. As a result, capacitor voltage will increase in a sinusoidal manner with time. Furthermore, the inductor voltage and output voltage in this state are given by ,

$$V_l = E_s - V_c \text{ and } V_i = 2V_c - E_s \quad (7-10)$$

At $\omega t + \phi_o = \pi/2$, capacitor voltage achieves its peak value and the inductor and source currents drop to zero. If the VSI is operated in Open state beyond the limiting time of $t_{o,\max} = (\pi/2 - \phi_o) / \omega$, the diode D_s would turn off as the source current tries to flow in the reverse direction. This signifies the end of Open-1 state and the beginning of Open-2 state.

7.2.2 Open-2 State

In the Open-2 state, the diode remains in the Off state and the VSI in the Open state. Therefore, the state defining equations are given as,

$$I_s = 0 \text{ and } I_i = 0 \quad (7-11)$$

Hence, the impedance network remains electrically isolated from the source and the load. All the system variables remain constant during this state. In order to avoid this state, the necessary condition can be seen as,

$$I_{lo \min} > 0 \quad (7-12)$$

7.2.3 Active-1 State

The equivalent circuit of the ZSI during the Active-1 state is given below in Fig. 7.4.

Fig. 7.4. Equivalent circuit of Z-source inverter in Active-1 state.

As seen in Fig. 7.4, the only difference between Open-1 state and Active-1 state is the presence of the constant current source I_0 across the input terminals of the VSI.

The state defining equations for Active-1 state are,

$$V_s = E_s \text{ and } I_i = I_0 \quad (7-13)$$

Substituting (7-13) in (7-1)-(7-3), the capacitor voltage and system currents can be derived as,

$$V_c = E_s + X_A \cdot \sin(\omega t + \phi_A) \quad (7-14)$$

$$I_c = I_L - I_0 = (I_s - I_0) / 2 = X_A \omega C \cdot \cos(\omega t + \phi_A) \quad (7-15)$$

$$\text{where } X_A = \sqrt{(V_{ciA} - E_s)^2 + [(I_{liA} - I_0)/(C\omega)]^2} \quad (7-16)$$

$$\phi_A = \tan^{-1}((V_{ciA} - E_s)\omega C / (I_{liA} - I_0)) \quad (7-17)$$

with the initial values of the capacitor voltage and inductor current in Active-1 state given by V_{ciA} and I_{liA} respectively. Note that the expressions for V_I and V_i given in (7-10) holds true even for the Active-1 state.

Comparing (7-14) and (7-15) with those for the Open-1 state given in (7-5) and (7-6), it can be seen that Open-1 state is a special case of Active-1 state where $I_0 = 0$. As the load current I_0 increases from zero, the peak value of the sinusoidal components of both capacitor voltage and inductor current will decrease and reach a minimum when $I_0 = I_{lA}$. Furthermore, the initial angle ϕ_A will increase with increasing I_0 and reach a value of $\pi/2$ at $I_0 = I_{lA}$.

With increasing time, the capacitor voltage will increase towards the peak value in a sinusoidal manner. However, if the same initial conditions were assumed, the peak value in Active-1 state would be less than that for the Open-1 state and the initial operating point would be closer to its peak point on the sinusoidal waveform.

From (7-15), it can be seen that the current through the diode, I_s , will be zero and the diode will turn off when, $I_l = -I_c = I_0/2$. It is interesting to note here that the capacitor voltage charges to the peak value and then discharges before approaching the above operating point which marks the end of Active-1 state and the beginning of Active-2 state. If the duration of the Active-1 period is t_A , the final values of the two state variables can be written as,

$$V_{cfA} = E_s + X_A \cdot \sin(\omega t_A + \phi_A) \quad (7-18)$$

$$I_{lfA} = I_0 + X_A \omega C \cdot \cos(\omega t_A + \phi_A) \quad (7-19)$$

7.2.4 Active-2 State

The state defining equations for Active-2 state are

$$I_i = I_0 \text{ and } I_s = 0 \quad (7-20)$$

Substituting (7-20) in (7-2) and (7-3), it can be seen that the currents remain constant at $I_l = -I_c = I_0 / 2$ and the capacitor discharges linearly with time at the rate of $I_0 / (2C)$.

In order to avoid Active-2 state in appearing during operation, the necessary condition is

$$I_{LA\min} > I_0 / 2 \quad (7-21)$$

However, it is important to note that the avoidance of Active-2 state does not eliminate the capacitor charging to its peak voltage. In order to avoid the capacitor charging to its peak value, the necessary condition according to (7-14) and (7-15) is

$$I_{LA\min} > I_0 \quad (7-22)$$

7.2.5 Shoot-Through-1 State:

The equivalent circuit for the Shoot-Through-1 state of the ZSI is given below in Fig.7.5.

Fig. 7.5. Equivalent circuit of Z-source inverter in Shoot-Through-1 state.

The state defining equations for shoot-through-1 state are,

$$I_s = 0 \text{ and } V_i = 0 \quad (7-23)$$

Substituting (7-23) in (7-1)-(7-3), the capacitor voltage and its current can be found as,

$$V_c = V_l = V_s / 2 = X_S \cdot \sin(\omega t + \phi_S) \quad (7-24)$$

$$I_c = -I_l = X_S \omega C \cdot \cos(\omega t + \phi_S) \quad (7-25)$$

$$\text{where } X_S = \sqrt{(V_{ciS})^2 + [(-I_{liS}) / (C\omega)]^2} \quad (7-26)$$

$$\phi_S = \tan^{-1}(-V_{ciS} \omega C / I_{liS}) \quad (7-27)$$

with the initial values of capacitor voltage and inductor current in Shoot-Through-1 state given by V_{ciS} and I_{liS} respectively. Since $\pi/2 < \phi_S < \pi$, with positive capacitor voltages and inductor currents found in practical converters, capacitor voltage given by (7-24) drops from its initial value in a sinusoidal manner with increasing time in this state. Simultaneously, the inductor current given by (7-25), increases towards its peak value in a sinusoidal manner with increasing time. This indicates that the energy stored in the capacitors during Open and Active states is transferred to inductors during the Shoot-Through state, thereby allowing the boosting of the voltage applied to the VSI. The Shoot-Through-1 state ends and the Shoot-Through-2 state begins when the diode D_s gets forward-biased and comes into conduction. This occurs when V_s drops to the level of E_s . Thus, from (7-24), it can be seen that $V_c = E_s / 2$ at the end of Shoot-Through-1 state. If the period of Shoot-Through-1 period is t_S , the final values of the two state variables can be written as,

$$V_{cfS} = X_S \cdot \sin(\omega t_S + \phi_S) \quad (7-28)$$

$$I_{lfS} = -X_S \omega C \cdot \cos(\omega t_S + \phi_S) \quad (7-29)$$

7.2.6 Shoot-Through-2 State:

The defining equations of Shoot-Through-2 state can be written as,

$$V_s = E_s \text{ and } V_i = 0 \quad (7-30)$$

Substituting (7-30) in (7-1)-(7-3) it can be seen that $V_c = V_l = E_s / 2$ and $I_c = 0$ in this state. Moreover, the inductor current ramps up linearly at a rate of $E_s / (2L)$ with time. Thus, it is unsafe to let the converter operate for long periods in this state, as the increasing currents could

soon damage the diode D_s and the switching devices of the VSI. In order to prevent Shoot-Through-2 state during operation, the necessary condition is

$$V_{c\min} > E_s / 2 \quad (7-31)$$

7.2.7 Overview of Operating States:

From the preceding discussion it is clear that the Open-2, Active-2 and Shoot-Through-2 states do not contribute to the power conversion process and should be avoided. Thus, they can be termed as ‘static states’. Practical converters are operated only in two or three of the Open-1, Active-1 and Shoot-Through-1 states. They are hereby named as ‘dynamic states’.

The three static states appear only when the capacitor voltage and inductor current fluctuate in a wide range leading to the violation of conditions given in (7-12), (7-21) and (7-31). Therefore, it is necessary to limit the ripples of the related voltages and currents by increasing the sizes of the inductors and capacitors appropriately. Thus, after designing the impedance network, a check can be made with these three conditions to ensure the limitation of operation only to the three dynamic states.

7.3 Designing of impedance Network for Operation with two Dynamic States

7.3.1 Non-Linear Method

Since the Open-1 period is not essential for the conversion process and Open-1 and Active-1 states behave in a similar manner, the Open-1 period can be considered as part of the Active-1 period, as proposed in [17]. Thus, a ZSI operating only in the Active-1 and Shoot-Through-1 states as depicted in Fig. 7.6, is considered for the analysis in this section. Since the final value of a variable in one state is the initial value of the same variable in the other state, the boundary conditions can be defined as,

$$V_{ifA} = V_{cfS} ; V_{ciS} = V_{cfA} \quad (7-32)$$

$$I_{liA} = I_{lfS} ; I_{liS} = I_{lfA} \quad (7-33)$$

Furthermore, since one switching cycle of VSI has only the Active-1 and Shoot-Through-1 period,

$$t_S = d_s T_s, \quad t_A = (1 - d_s) T_s \quad (7-34)$$

where T_s is the period of switching cycle at the dc link and d_s is the duty ratio of the shoot-through-1 state. Note here that T_s is only one half of the period of the switching cycle of VSI because the dc link experiences two similar switching cycles in one switching cycle of VSI.

Fig. 7.6. Steady-state waveforms of (a) capacitor voltage (b) inductor current for the operation with two dynamic states.

Since the equivalent dc link voltage applied to the VSI is given by the average value of V_i during the Active-1 state ($\bar{V}_{iA}$), it can be expressed using (7-10), (7-14) and (7-15) as,

$$\bar{V}_{iA} = \frac{1}{t_A} \int_0^{t_A} V_i \cdot dt = E_s + 2[I_{liA} - I_{lfA}]/[\omega^2 C(1 - d_s)T_s] \quad (7-35)$$

For a 3-phase VSI operating with sinusoidal PWM, the peak value of fundamental line to neutral output voltage (V_m) is given by, $M\bar{V}_{iA}/2$, where M is the modulation index [1].

Therefore, $\bar{V}_{iA}$ can also be expressed as,

$$\bar{V}_{iA} = 2V_m / M \quad (7-36)$$

Moreover, the average values of V_c and I_l , ($\bar{V}_c$ and $\bar{I}_l$) can be determined from the waveforms in Fig. 7.6 as,

$$\bar{V}_c = E_s(1 - d_s) + \frac{2(I_{liA} - I_{lfA})}{\omega^2 C T_s} \quad (7-37)$$

$$\bar{I}_l = I_0(1 - d_s) + \frac{2C(V_{cfA} - V_{ciA})}{T_s} \quad (7-38)$$

By setting the ratios of peak to average values of both capacitor voltage and inductor current to be the same value k ,

$$V_{cfA} = (1 + k)\bar{V}_c \quad (7-39)$$

$$I_{liA} = (1 + k)\bar{I}_l \quad (7-40)$$

where $0 < k < 1$ in practical converters.

By neglecting the power losses in the inverter and the effects of harmonics on the ac side, the average power transferred from the dc link can be equated to the power delivered to the ac load over one ac cycle as [1],

$$\bar{V}_{iA} I_0 (1 - d_s) = (3/2) V_m I_m \cos \phi \quad (7-41)$$

where, I_m is the peak phase current on the ac side and ϕ is the power factor angle of the load on the ac side of the inverter. As shown in [1, 108, 109], the instantaneous voltage and current at the dc link and the duty cycle d_s vary in a wide range from one switching cycle to another. However, for simpler calculations, the ripples of $\bar{V}_{iA}$, I_0 and d_s have been neglected and their values have been assumed as constants in (7-41).

By equating $\bar{V}_{iA}$ in (7-35) and (7-41), a relationship can be found as,

$$(3/2) V_m I_m \cos \phi / [(1 - d_s) I_0] = E_s + 2(I_{liA} - I_{lfA}) / (\omega^2 C (1 - d_s) T_s) \quad (7-42)$$

Similarly by equating $\bar{V}_{iA}$ in (7-36) and (7-41), another equation can be derived as,

$$I_0 = (3/4)MI_m (\cos \phi)/(1 - d_s) \quad (7-43)$$

Finally, the relationship between M and d_s is a result of the control strategy that is adopted to switch the VSI. For example, in simple boost control [17] and maximum constant boost control [30], d_s is kept constant at $(1 - M)$ and $(1 - \sqrt{3}M/2)$ respectively. Therefore, in general M can be written as a function of d_s as ,

$$M = f(d_s) \quad (7-44)$$

In order to determine the required values of C , ω and d_s that would yield the required output ac voltage and current, it is necessary to solve (7-16)-(7-19), (7-26)-(7-29), (7-32)-(7-40) and (7-42)-(7-44) simultaneously by using a numerical method. Finally, the required inductance can be determined using (7-7).

However, due to the large number of non linear equations involved, the possibility of finding a correct solution for the above set of equations is highly dependant on the accuracy of the initial values used for the numerical method. The approximate method of design described in the following section can be used to estimate the initial values of the variables used in the nonlinear method.

7.3.2 Linear Method

As it can be observed from the number of non linear equations involved, it is not a simple task to accurately design the impedance network even for the simplest case of operation with two dynamic states. Hence a less accurate, yet a much simpler method is proposed in this section for the sizing of the impedance network.

A ripple in the capacitor voltage in turn appears as a ripple in the dc link voltage applied to the VSI. A large ripple in the dc link voltage degrades the waveform of the ac voltage by giving rise to unexpected harmonics in addition to increasing the voltage rating of the VSI. As a consequence, the ripple of the capacitor voltage in practical converters is limited by these

concerns and leads to a much smaller ripple than the one allowed by (7-31). Similarly, the ripple of the inductor current in turn appears as a ripple in the current through the diode and the source. In order to limit the current rating of the diode and the source, the ripple of the inductor current is constrained to a range which is much smaller than that allowed by the condition in (7-21). Due to the smaller ripples allowed, the changes in the capacitor voltage and inductor current can be assumed as linear, instead of sinusoidal, for simpler analysis and designing of the ZSI.

Fig. 7.7 illustrates the waveforms of the capacitor voltage and inductor current under this condition. The peak value of the ripples of capacitor voltage and inductor current are given as ΔV_c and ΔI_l respectively.

With linear variations of waveforms, from (7-1), ΔV_c and ΔI_l can be expressed as,

$$\Delta V_c = (\bar{I}_l \Delta t) / C ; \Delta I_l = (\bar{V}_l \Delta t) / L \quad (7-45)$$

Considering the Shoot-Through-1 period,

$$C = (\bar{I}_l d_s T_s) / (2\Delta V_c) ; L = (\bar{V}_c d_s T_s) / (2\Delta I_l) \quad (7-46)$$

(a)

(b)

Fig. 7.7 Variations of (a) capacitor voltage and (b) inductor current with time for small ripples around their average values.

Since the average inductor voltage and average capacitor current over a complete switching cycle in steady-state are zero [17],

$$\bar{V}_c / \bar{E}_s = \bar{I}_l / I_0 = \lambda \quad (7-47)$$

where $\lambda = (1 - d_s) / (1 - 2d_s)$.

By taking $\Delta \bar{V}_c / V_c = \Delta \bar{I}_l / \bar{I}_l = k$ where $k \ll 1$ is a design variable, (7-46) and (7-47) can be combined as, $C = (\bar{I}_0 d_s T_s) / (2kE_s)$; $L = (E_s d_s T_s) / (2kI_0)$ (7-48)

By substituting for I_0 from (7-43) into the above equations,

$$C = \frac{3d_s T_s M I_m \cos \phi}{8kE_s (1 - d_s)}; \quad L = \frac{2E_s d_s T_s (1 - d_s)}{3kM I_m \cos \phi} \quad (7-49)$$

Thus, if E_s, I_m, ϕ, d_s, T_s and M are known, C and L for any control strategy can be calculated from (7-48) to result in a desired level of ripples k .

Furthermore, by using (7-10) and (7-47),

$$\bar{V}_{iA} = (2\lambda - 1)E_s \Rightarrow \bar{V}_{iA} = E_s / (1 - 2d_s) \quad (7-50)$$

7.3.2.1 Simple Boost Control

For simple boost control, the relationship between M and d_s is [17],

$$M = 1 - d_s \quad (7-51)$$

Substituting this into (7-43),

$$I_0 = (3/4)I_m \cos \phi \quad (7-52)$$

By equating (7-36) to (7-50) and substituting for M from (7-51),

$$\lambda = 2V_m / E_s \Rightarrow d_s = (2V_m - E_s) / (4V_m - E_s) \quad (7-53)$$

With the substitution of λ and d_s from (7-53) in (7-47) and (7-49) respectively, it can be found that

$$\bar{V}_c = 2V_m; \quad \bar{I}_l = 2V_m I_0 / E_s \quad (7-54)$$

$$C = \frac{3T_s I_m \cos \phi (2V_m - E_s)}{8kE_s (4V_m - E_s)}; \quad L = \frac{2E_s T_s (2V_m - E_s)}{3kI_m \cos \phi (4V_m - E_s)} \quad (7-55)$$

Hence, the sizing of capacitance and inductance can be easily done with (7-55) for simple-boost control.

The voltage and current ratings of the diode for control strategy can be determined using (7-24) and (7-15) as,

$$V_{Ds} = 2(1+k)\bar{V}_c; \quad I_{Ds} = 2(1+k)(\bar{I}_l - I_0) \quad (7-56)$$

and the voltage rating of VSI can be derived using (7-10) as,

$$V_{VSI} = 2(1+k)\bar{V}_c - E_s \quad (7-57)$$

7.3.2.2 Maximum Boost Control

For maximum boost control, the relationship between M and d_s is [30],

$$M = 2(1 - d_s) / \sqrt{3} \quad (7-58)$$

With this as the only change, corresponding equations of (7-52)-(7-55) can be written as (7-59)-(7-62) respectively.

$$I_0 = (\sqrt{3}/2)I_m \cos \phi \quad (7-59)$$

$$\lambda = \sqrt{3}V_m / E_s \Rightarrow d_s = (\sqrt{3}V_m - E_s) / (2\sqrt{3}V_m - E_s) \quad (7-60)$$

$$\bar{V}_c = \sqrt{3}V_m; \quad \bar{I}_l = \sqrt{3}V_m I_0 / E_s \quad (7-61)$$

$$C = \frac{\sqrt{3}T_s I_m \cos \phi (\sqrt{3}V_m - E_s)}{4kE_s (2\sqrt{3}V_m - E_s)}; \quad L = \frac{E_s T_s (\sqrt{3}V_m - E_s)}{\sqrt{3}kI_m \cos \phi (2\sqrt{3}V_m - E_s)} \quad (7-62)$$

7.4 Design Example and Simulation Results

Let a 3-phase, 50 Hz, 400 V (line-line), 25A, Y-connected unity power factor load with an LC filter be supplied by a ZSI operating at 5 kHz under simple-boost control with a constant input

dc source voltage of 200 V. For this case, the known operating parameters of the circuit can be listed as, $T_s = 10^{-4} \text{ s}$; $E_s = 200 \text{ V}$; $V_m = 400\sqrt{2/3} = 326.6 \text{ V}$; $I_m = 25\sqrt{2} \text{ A}$ and $\phi = 0$.

7.4.1 Design Based on Linear Method

Since this method assumes linear waveforms, it is reasonably accurate only for waveforms with small ripple factors, i.e. small values of k .

Substituting V_m and E_s in (7-53) (simple boost), it can be found that $\lambda = 3.266$, $d_s = 0.41$ and from (7-51), $M = 0.59$. Furthermore, the dc link current I_0 is given by (7-52) as $I_0 = 26.52 \text{ A}$. Using (7-54), it can be found that $\bar{V}_c = 653.2 \text{ V}$ and $\bar{I}_l = 86.66 \text{ A}$. The equivalent dc link voltage can then be found from (7-50) as, $\bar{V}_{iA} = 1106.4$. The sizes of capacitors inductors are then given by (7-55) as $C = 2.72/k \text{ } \mu\text{F}$ and $L = 0.154/k \text{ mH}$, where k is the design variable chosen to limit the ripples of capacitor voltage and inductor current.

For the ripples to be 5% of their average values, $k = 0.05$ and then $C = 54.4 \text{ } \mu\text{F}$ and $L = 3.09 \text{ mH}$. The voltage and current rating of the diode from (7-56) are 1371.7V and 126.3A respectively and the voltage rating of VSI from (7-57) is 1171.7V.

The waveforms of V_c , V_i , I_l and I_i as achieved from the computer simulation performed using MATLAB/SIMULINK for the design with $k = 0.05$ are illustrated in Fig. 7.8. As can be seen in Fig. 7.8(a), capacitor voltage has an average value about 645 V and a peak ripple of 5%. The drop in the average value from the expected 653 V can be attributed as due to the resistance of the inductor used in the simulation. The inductor current shown in Fig. 7.8(b) has an average value of 86A and a peak ripple of 5%. The excellent matching of the simulation results with the expected values verifies the accuracy of the design process.

(a)

(b)

Fig. 7.8. Waveforms of (a) V_c and V_i (b) I_l and I_i as resulted from the simulation for the design with $k = 0.05$.

(a)

(b)

Fig. 7.9. Waveforms of (a) V_c and V_i (b) I_l and I_i as resulted from the simulation for the design with $k = 1$.

In order to demonstrate the possibility of appearance of static states when the impedance network is designed for larger ripples, simulation was repeated for the same case with $k = 1$. Both in Fig. 7.9(a) and 7.9(b), it can be clearly seen that there are two additional states, namely Active-2 and Shoot-Through-2. The sinusoidal variations of V_c and I_l during Active-1 and Shoot-Through-1 states are clearly visible from these figures. Furthermore, V_c remains

constant at $E_s / 2 = 100V$ in Shoot-Through-2 state and drops linearly in Active-2 state. Similarly, I_l remains constant at $I_0 / 2 = 13.3A$ during Active-2 state and increases linearly in Shoot-Through-2 state. Thus, the analysis of states presented in section 5.2 accurately predicts the behaviour of the ZSI for any operating condition. However, since the C and L values were calculated on the basis of the linearized waveforms, the average values of both V_c and I_l have deviated significantly from the expected values.

7.4.2 Comparison of Accuracy of Linear and Nonlinear Methods

In order to demonstrate the decreasing accuracy of linear method with increasing ripple factor k and the improvements that can be made by using the nonlinear method, two case studies are made here for two large values for k .

7.4.2.1 Case Study 1: $k=0.25$

The circuit variables as calculated from the linear method and the nonlinear method are compared in Table 7.2. The parameters from the linear method were used as the initial values in the nonlinear method that used ‘fsolve’ function of MATLAB optimization toolbox with Levenberg-Marquardt algorithm as the method of solving of simultaneous nonlinear equations.

TABLE 7.2

Circuit variables calculated from linear and nonlinear methods for $k = 0.25$

Variable	Linear	Nonlinear	Variable	Linear	Nonlinear
L (mH)	0.62	0.55	V_{ciA} (V)	489.9	445.3
C (μF)	10.88	9.61	V_{cfA} (V)	816.5	816.5
d_s	0.410	0.413	I_{liA} (A)	108.3	108.2
I_0 (A)	26.52	26.52	I_{lfA} (A)	65.0	59.0

It is interesting to note here that the values of L and C as obtained with the nonlinear method are smaller compared to those resulted from the linear method. Furthermore, the value of d_s predicted by the nonlinear method is higher than that predicted by the linear method.

Fig. 7.10 and 7.11 show the simulation results, obtained with MATLAB/SIMULINK software for $k = 0.25$. In order to facilitate the simulation, parasitic resistances of elements such as capacitors, inductors and the source were included. The VSI consisted of six Insulated Gate Bipolar Junction Transistors (IGBT) with high resistive snubbers. A low pass filter having $L_f = 10\text{mH}$ and $C_f = 10\mu\text{F}$ was used on the ac side between the inverter and the load to filter out high frequency components. This results in a reduction in the fundamental component of load voltage and load current by about 4.74%. Hence, the expected load voltage and load current are 220V (line-neutral) and 23.8 A respectively when the corresponding values at the inverter terminals are at their rated values, i.e. 231V and 25A respectively.

Fig. 7.10: Simulated waveforms of (a) V_c , (b) I_l , for the designs based on non linear and linear methods, for $k = 0.25$.

Fig 7.11: Simulated waveforms of (a) load voltage (line-neutral), (b) load current, for the designs based on non linear and linear methods, for $k = 0.25$.

A comparison of the performances of the two inverters designed using nonlinear and linear method is given in Table 7.3. The percentage ripple factors given in the table are calculated using the starting and ending values of V_c and I_l during the Active-1 state. For example, $\Delta V_{cfA} = (V_{cfA} - \bar{V}_c) \cdot 100 / \bar{V}_c$ %. As can be seen in the last two columns of the table, percentage errors between calculated and simulated results are exactly the same in both inverters for this case with $k = 0.25$. The small reduction in the ac side voltage and current from the expected values can be attributed to the parasitic resistances used in the simulation.

TABLE 7-3

Performance comparison of ZSIs designed using linear and nonlinear methods, for $k = 0.25$

		$\bar{V}_c$ (V)	$\bar{I}_l$ (A)	ΔV_{cfA} (%)	ΔV_{ciA} (%)	ΔI_{liA} (%)	ΔI_{lfA} (%)	V_{LN} rms (V)	I_{load} rms (A)
Linear	Calculated	653.2	86.66	25	25	25	25	220	23.8
	Simulated	620	92	22.5	33.9	20.6	23.9	216	23.5
	% error	5.1	-5.8	10	-35.6	17.6	4.4	1.8	1.3
Nonlinear	Calculated	653.2	86.60	25	32	25	32	220	23.8
	Simulated	645	91	26.3	39.5	25.2	28.6	216	23.5
	% error	1.25	5.1	-5.2	-23.4	-0.8	10.6	1.8	1.3

However, the corresponding errors in the average, maximum and minimum values of the capacitor voltage and inductor current are, in general, much smaller in the inverter designed using the nonlinear method.

As can be observed from the simulated waveforms of V_c and I_l in Fig. 7.10, waveforms deviate from linearity at high values of k . As a result, the average value of any of the two waveforms is higher than the corresponding average of the maximum and minimum values of the waveforms. In another words, the peak ripples calculated using the maximum values, i.e. ΔV_{cfA} , ΔI_{liA} , are smaller than the ripples calculated using the minimum values, i.e. ΔV_{ciA} , ΔI_{lfA} . This is clearly evident from the Table 7.3.

7.4.2.2 Case Study 2: $k=0.4$

The circuit variables calculated using linear and nonlinear methods for $k = 0.4$ are given in Table 7.4. The waveforms as resulted from computer simulation are given in Fig. 7.12 and 7.14. A performance comparison of the two inverters based on the two design methods is given in Table 7.5. Note that the nonlinear method results in smaller values for L and C , as observed in case study 1. It also predicts a higher d_s than the linear method, and the % error of the results of the non linear method are lower than that of the linear method. This means that the simulation results agree reasonably well with the non linear method calculations while the calculated values from the linear method are seen to be far away in general. This is more evident from the waveform magnitudes in the ac side, which is the final desired output from the system. The magnitudes of the ac side waveforms are reasonably accurate for the nonlinear design, while the results obtained with the linear design are far from acceptable.

A comparison of results in Table 7.3 and 7.5 confirms that the design based on non linear method leads to acceptable performance irrespective of the levels of the ripples whereas the design based on the linear method is accurate only when the levels of ripples are small.

Furthermore, non-linear method results in smaller L and C values as can be seen in Table 7.2 and 7.4.

Fig. 7.12: Simulated waveforms of (a) V_c , (b) I_l , for the designs based on non linear and linear methods, for $k = 0.4$.

TABLE 7-4

Circuit variables calculated from linear and nonlinear methods for $k = 0.4$

Variable	Linear	Nonlinear	Variable	Linear	Nonlinear
L (mH)	0.38	0.31	V_{ciA} (V)	392.0	245.0
C (μ F)	6.80	5.32	V_{cfA} (V)	914.5	914.5
d_s	0.41	0.42	I_{liA} (A)	121.3	121.2
I_0 (A)	26.52	26.52	I_{lfA} (A)	52.0	32.5

Fig 7-13: Simulated waveforms of (a) load voltage (line-neutral), (b) load current, for the designs based on non linear and linear methods, for $k = 0.4$.

TABLE 7.5

Performance comparison of ZSIs designed using linear and nonlinear methods, for $k = 0.4$

		$\bar{V}_c$ (V)	$\bar{I}_l$ (A)	ΔV_{cfA} (%)	ΔV_{ciA} (%)	ΔI_{liA} (%)	ΔI_{lfA} (%)	V_{LN} rms (V)	I_{load} rms (A)
Linear	Calculated	653.2	86.66	40	40	40	40	220	23.8
	Simulated	590	84	35.6	54.2	29.8	40.5	194	21
	% error	9.7	3.1	11	-35.5	25.5	-1.2	11.2	11.8
Nonlinear	Calculated	653.2	86.60	40	62	40	62	220	23.8
	Simulated	620	89	43.5	58.9	36.5	49.4	212	23
	% error	5.1	-2.8	-8.7	5	8.7	20.3	3.6	3.4

7.5 Effects of Non Idealities

In the design methods described in section 5.3, a number of assumptions were made to simplify the calculations. However, in a practical converter, the effects of these non-idealities become apparent. The differences in the calculated and simulated results given in Tables 7.3

and 7.5 are partly due to these non-idealities. Three of the main non-idealities are described below.

1. Representation of load current in active state by a constant Current source (I_0)

The dc link current of a VSI contains a strong harmonic at six times the fundamental frequency of the ac load current, in addition to the dominant dc component and the high frequency harmonics at inverter switching frequency [1]. Therefore, the instantaneous dc link current changes in a large range. Due to the high switching frequency of VSI, the duration of the Active-1 period is very small and hence it is reasonably accurate to assume I_0 as constant during the period of one Active-1 state. However, the value of I_0 varies from one Active-1 state to another as the instantaneous dc link current changes its value. Due to the strong sixth harmonic, the magnitude of I_0 is seen to be varying approximately at six times the inverter output frequency. Although this variation of I_0 does not affect the average values, it does affect the ripple of the inductor current and the capacitor voltage. In order to account for the increased ripple content, the inductor and capacitor designed using the assumption of constant I_0 need to be increased by a certain percentage that corresponds to the percentage of sixth harmonic current in the dc link. However, assuming sufficient filtering is available at the inverter output side, the effect of the increased ripples of V_c and I_l on the ac load can be neglected.

2. Parasitic resistances of the Z network and the source

The main effect of parasitic resistances is to reduce the voltage boost of the Z inverter. The effect of the parasitic resistances can be easily determined from the linear method for the case where the ripples are small.

Let the parasitic resistances of the source, inductor and capacitor be R_s , R_l and R_c . By following the same method of derivation as in section 7.3.2, it can be shown that,

$$\bar{V}_c = \frac{1-d_s}{1-2d_s} E_s - (R_s + R_l + 2d_s R_c) I_0 \frac{1-d_s}{(1-2d_s)^2} \quad (7-63)$$

$$\bar{I}_l = \frac{(1-d_s)}{1-2d_s} I_0 \quad (7-64)$$

Therefore, the effect of the parasitic resistances is to drop the average capacitor voltage $\bar{V}_c$. This in turn reduces the dc link voltage and the output ac voltage. However, average inductor current $\bar{I}_l$ remains unaffected.

If the parasitic resistances are known, then they can be included in the design calculations to improve the design. However, although this is simple in linear design, the calculations and the equations become more complex in the nonlinear design.

3. Presence of Open-1 State with Simple-Boost Control

When simple-boost control with constant d_s is applied to a VSI operating with sinusoidal PWM all three dynamic states, including the Open-1 state appear during one switching cycle [17]. As discussed in section 7.2, the performance of ZSI inverter is different from Active-1 state to Open-1 state. However, in design methods described in section 7.3, operation in only two states were considered by assuming that there are no periods of Open-1 state. Therefore, the equations derived in section 7.3 are valid only if these open-1 periods are negligibly small compared to other states.

The error in design due to this open 1 state may be reduced by adopting control strategies that eliminates or minimizes the open 1 state in a switching cycle, such as maximum boost control.

7.6. Ultra-capacitor based Z-source inverters.

The previous analysis was based on a battery based Z-source inverter, and the main objective was to design its impedance network. However when the Z-Source inverter is used to interface an ultra-capacitor bank, some of the above conclusions may not be directly applicable. As with

the other converters described in Chapters 3 and 4, the main attention should be given to the minimization of the effects of the low frequency pole-zero pair that exists in all the ultra-capacitor based converter systems, when designing a Z-Source inverter to interface ultra-capacitor banks. Therefore, this section focuses on the low frequency pole-zero pair of the Ultra-capacitor based Z-source inverters and the means that can be adopted to minimize their adverse effects.

Ultra-capacitors usually have a higher series resistance compared to the batteries [9]. Therefore, this series resistance, R_{uc} , was also included in the analysis in this section. The switching equivalent of the Ultra-capacitor based Z-source inverter is shown in Fig 7.14. The system state matrices for this Ultra-capacitor based Z-source inverter is given in Appendix C3.

Fig 7.14. Switching Equivalent of Ultra-capacitor based Z-source inverter

Following the procedure described in Appendices A and C3, the open loop control to output transfer function for the Z-Source inverter can be derived as shown below. The shoot through state 1 duty ratio, d_s , was taken as the control variable while the peak dc link voltage (V_i in Fig 7.14) was taken as the output variable for the Z inverter.

$$G_{Vdu_Z}(s) = \frac{num_Z}{den_Z} \quad (7-65)$$

Where, $num_Z = (b_3s^3 + b_2s^2 + b_1s + b_0)(-C_{uc}LC((1-2d_s)\bar{X}_1 - 4d_sR_{uc}L))$ and

$$den_Z = s(a_2s^2 + a_1s + a_0)(C_{uc}CL)(1-2d_s)^2$$

$$a_2 = 1, a_1 = 2\frac{R_{uc}}{L}(1-d_s), a_0 = \frac{2(1-d_s)^2}{C_{uc}L} + \frac{(1-2d_s)^2}{CL}$$

$$b_3 = 1, b_2 = (2(1-d_s)(1-2d_s)(C + 2C_{uc})d_aI_0)/(C_{uc}C((1-2d_s)\bar{X}_1 - 4d_sR_{uc}L)),$$

$$b_1 = -((1-2d_s)((1-2d_s)\bar{X}_1 - 4d_aR_{uc}I_0))/(LC((1-2d_s)\bar{X}_1 - 4d_sR_{uc}L)),$$

$$b_0 = (d_aI_0(1-2d_s)(1-d_s))/(C_{uc}LC((1-2d_s)\bar{X}_1 - 4d_sR_{uc}L))$$

Therefore, it is seen that both the numerator and the denominator of this Z inverter control to output transfer function has the same order.

7.6.1 System RHP Zeros

It is not convenient to derive simple expressions for the system zeros from (7-65). However as described in Appendix E, it is seen that the system should have two RHP zeros and one LHP zero. Moreover, the LHP zero should be real and it should have the highest magnitude of the three zeros in order to meet the signs of the numerator coefficients given in (7-65), as described in Appendix E. Therefore, it can be concluded that the system LHP zero should be located at high frequencies.

As described in Appendix E, the signs in the numerator coefficients can be met if the RHP zeros were real and one of them is very small. Therefore, there is a possibility to have one low frequency RHP zero and one high frequency RHP zero in the ultra-capacitor based Z inverter. However the exact positions of these RHP zeros are dependant on the system parameters, and, may only be conveniently evaluated with numerical values.

7.6.2 System Poles

From (7-65) it is seen that the open loop control to output transfer function of the Z inverter has one pole at the origin and two poles at,

$$P_{2u_Z}, P_{2u_Z}^* = -\frac{R_{uc}}{L}(1-2d_s) \pm \sqrt{\left(\frac{R_{uc}}{L}(1-2d_s)\right)^2 - \left(\frac{2(1-d_s)^2}{C_{uc}L} + \frac{(1-2d_s)^2}{CL}\right)} \quad (7-66)$$

These two poles in (7-66) are complex conjugates in most cases since R_{uc} is very small. Moreover, due to the small R_{uc} , the real part of these two poles are also small. Therefore, it is seen that the Z inverter has all its poles very close to the origin, and hence the system is seen to be lightly damped.

7.6.3 Pole-zero Map of Battery based Z-source inverter

By letting $C_{uc} \rightarrow \infty$ in (7-65) the equivalent battery based Z inverter control to output transfer function can be obtained as given below.

$$G_{Vdb_Z}(s) = \frac{-\left(s^2 + \frac{4d_a(1-d_s)(1-2d_s)I_0}{CL(E_b(1-2d_s) - 4d_a d_s R_{uc} I_0)}s - \frac{E_b(1-2d_s)^2 - 4d_a R_{uc} I_0(1-2d_s)}{CL(E_b(1-2d_s) - 4d_a d_s R_{uc} I_0)}\right)(CL(E_b(1-2d_s) - 4d_a d_s R_{uc} I_0))}{\left(s^2 + 2\frac{R_{uc}}{L}(1-d_s)s + \frac{(1-2d_s)^2}{LC}\right)((1-2d_s)^2 LC)} \quad (7-67)$$

From (7-67), it is seen that the battery based system do not have a pole on the origin. Also by comparing the denominator of (7-67) with the denominator of (7-65) it is seen that the battery based system has two poles, which are almost located at the same position of the two complex conjugate poles of the ultra-capacitor based system given in (7-66).

By analyzing the numerator of (7-67), it is seen that the battery based system has two zeros, one in the RHP and the other in the LHP. Since C and L represent values in micro or milli range, the numerator coefficients of the quadratic term in (7-67) suggests that these two zeros must have large magnitudes. Hence it is clear that both the LHP and RHP zero in the battery

based Z inverter are located at high frequencies for practical Z inverters. Therefore, there is no possibility to have a low frequency RHP zero in practical battery based Z inverters.

7.6.4 Comments on the Low Frequency Pole-zero Pair

It is seen that the ultra-capacitor based Z inverter has a pole at the origin and it also has a possibility to have a RHP zero very close to the origin. However in case of the battery based Z inverter there is no pole on the origin and also there is no possibility to have a RHP zero close to the origin.

The numerical results that follows also are in agreement with these conclusions and they also show that there is always a RHP zero very close to the origin in practical ultra-capacitor based Z inverters. Therefore, similar to the conclusions made for the other converters above, the main difference between the battery based and ultra-capacitor based Z inverter transfer functions is the low frequency pole-zero pair. However with the Z inverter transfer functions, the low frequency pole is seen to be located exactly on the origin. The position of the low frequency RHP zero varies with other system parameters. Hence, it should be noted here that the additional root locus branch added due to the low frequency pole-zero pair of the Ultra-capacitor based Z-source inverter is entirely in the RHP, as shown in fig 7.15, unlike in all the other converters described above.

Fig. 7.15. Typical root locus plot for the Ultra-capacitor based Z-source inverter when the feedback gain is varied - obtained with numerical results in section 7.6.5 (not to scale)

Therefore, the closed loop system response of all the Ultra-capacitor based Z-source inverters will be unstable. But if the low frequency RHP zero can be made reasonably close to the origin by suitably selecting other system parameters, then the closed loop system response can be made less sensitive to the effects of this unstable closed loop pole [95].

Therefore, a suitably designed Z inverter, which is capable of minimizing the effects of the low frequency pole zero pair, can be used for applications involving ultra-capacitors without significant performance degradation.

7.6.5 Numerical Results

The pole-zero positions of the three impedance networks that were designed in section 7.4, are analyzed below. The parameters corresponding to the three impedance networks, which were designed for a 3-phase 400V, 25A unity power factor load and a 200 V (fixed) source, are given in Table 7.6.

Table 7.6: Parameters for three impedance networks designed in section 7.4

	Case 1 Small ripple design	Case 2 Medium ripple design	Case 3 High ripple design
L (mH)	3.09	0.55	0.31
C (μF)	54.4	9.61	5.32
d_s	0.41	0.413	0.42
I_0 (A)	26.52	26.52	26.52
R_{uc} (Ω)	0	0	0

The positions of P_{1u} and Z_{1u} observed in these three cases are as given below in Table 7.7.

Table 7.7: Low frequency pole zero pair of Ultra-capacitor based Z-source inverter for three impedance network designs

	Low frequency pole / zero	Capacitance of Ultra-capacitor bank (C_{uc})		
		3 F	5 F	10 F
Case 1	P_{1u}	0	0	0
	Z_{1u}	0.1709	0.1025	0.0513
Case 2	P_{1u}	0	0	0
	Z_{1u}	0.1754	0.1052	0.0526
Case 3	P_{1u}	0	0	0
	Z_{1u}	0.1862	0.1117	0.0559

Results in Table 7.7 shows that the effects of the low frequency pole-zero pair of the Ultra-capacitor based Z-source inverter can be minimized by designing the impedance network to operate with small ripples, i.e. by increasing the size of the elements of the impedance network. The effect of the low frequency pole-zero pair can be further suppressed also by using a larger ultra-capacitor bank, as concluded earlier in Chapter 5. The results in Table 7.6 shows that the size of the ultra-capacitor bank has the largest effect on the position of the low frequency RHP zero.

7.7 Summary

The Z-Source inverter (ZSI) is a recently introduced power converter that is capable of directly interfacing a variable voltage source such as an ultra-capacitor bank to an ac load that demands a constant voltage at its terminals. Although most of the current literature on the ZSI focuses on the control of the inverter in order to utilize its unique advantages, none of them give sufficient guidelines to design a ZSI for a given application.

In this chapter all possible operating states of the ZSI were analyzed and the equations were derived to predict the behaviour of ZSI in steady-state. Through the analysis it was shown that as the ripples of the capacitor voltage and inductor current become large, three additional static states appear in addition to the commonly used three dynamic states. Based on the equations derived, a method was proposed to design the impedance network accurately for any operating condition by considering the nonlinearity of waveforms. However, as the mathematical complexity of the proposed design method is high, a simpler design method was also presented by assuming the ripples to be small and linear.

The design method involving non linear equations, although complex, is suitable for designing Z networks with smaller capacitors and inductors that allow larger ripples in capacitor voltage and inductor currents. However large ripples in the inductor current and capacitor voltages results in large ripples in the dc link voltage, which in turn results in unexpected harmonics at the ac load voltage. However, assuming sufficient filtering is available at the inverter output, this effect may be neglected.

On the other hand the approximate linear method is simple, but it results in a larger impedance network than the non linear method. However it offers some other advantages such as reduced circuit losses and less harmonic considerations on the ac side.

The accuracy of the non linear design method and the linear design method were verified by computer simulations using illustrative examples. Furthermore, the appearance of static states

was also demonstrated and the analysis presented was verified by considering a case where the ripples are allowed to be large.

However, these two design methods assume the steady state operation of a battery based Z-source inverter. Therefore, the conclusions derived are not directly applicable for Ultra-capacitor based Z-source inverters, since it neglects the possible adverse effects of the low frequency pole-zero pair that is present in all ultra-capacitor based converter systems.

The final sections of this chapter investigated the variation of the low frequency pole-zero pair of the control to output transfer function of the Ultra-capacitor based Z-source inverter when the Z network parameters and the size of the ultra-capacitor bank were varied. The shoot through duty cycle was chosen as the control variable, while the peak dc link voltage was chosen as the output variable.

It was shown that the low frequency pole always lies on the origin while the low frequency zero lies very close to the origin on the RHP. Hence, in order to improve the steady state performance of the Ultra-capacitor based Z-source inverters, it is necessary to select the system parameters so that the RHP zero is moved sufficiently close to the origin. It was shown that the RHP zero can be moved closer to the origin by selecting a large impedance network for the Z network and also by using a larger ultra-capacitor bank.

The linear design method, which designs the Z network to operate with smaller ripples, is thus more suitable for Ultra-capacitor based Z-source inverter applications, since it results in larger impedance networks. However, if a very large variation of the low frequency RHP zero is desired, then it may be necessary to increase the size of the ultra-capacitor bank also, as it has the most significant influence on the low frequency RHP zero position.

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

8.1 Conclusions

The ultra-capacitor is an emerging energy storage device that is ideally suited for short term energy storage applications. It has a superior power density but a lower energy density compared to batteries. However, ultra-capacitors are maintenance free and also have the capability to withstand a large number of charge discharge cycles compared to batteries. Also they can be charged or discharged much faster than the batteries, making them very attractive to applications that require fast energy transfers. Due to these unique and attractive properties, ultra-capacitors are being considered in short term power quality applications as a replacement for batteries.

Currently ultra-capacitors are mostly considered for ride through systems for adjustable speed drives (ASD), which is an integral part of modern industrial processes. Therefore, the main analysis in this thesis was based on an ultra-capacitor based ride through system for an ASD, although the conclusions derived are shown to be equally applicable to other types of ultra-capacitor based applications.

Due to the low voltage rating of the ultra-capacitors, a number of ultra-capacitor cells are needed to be connected in series / parallel to construct an ultra-capacitor bank that is having a suitable voltage rating / current rating for practical applications. Since the terminal voltage of any capacitor vary in a very wide range when they are charged or discharged, a DC-DC converter is also required as the interface between the ultra-capacitor bank and rest of the system. The DC-DC converter typically has both buck and boost capability: buck operation to

recharge the ultra-capacitors and boost operation to supply power to a load operating at a higher voltage than the terminal voltage of the ultra-capacitor bank.

The ultra-capacitor based ride through system needs to operate and supply power to the ASD during short disturbances to the source. These short term disturbances can last from a few cycles up to a minute, but the most common disturbances usually last only for a few seconds. When providing power to the ASD during a short disturbance, the ultra-capacitor based ride through system should operate fast in order to prevent a collapse of dc link voltage beyond a certain set value to prevent the tripping of the ASD. The DC-DC converter that interfaces the ultra-capacitor bank needs to be operated in boost mode during this ride through time. Hence the boost mode operation of the DC-DC converter is seen to be time critical, compared to the buck operation that is used to recharge the ultra-capacitors when the source is healthy. Therefore, the analysis in this thesis was entirely focused on the boost operation of the interfacing DC-DC converter.

If galvanic isolation is not required, the simplest form of the boost converter that can be used for the ultra-capacitor based ride through system is the classical boost converter. In applications where the galvanic isolation is required the fly-back converter can be used instead. In fact these two are the commonly used DC-DC converters to interface ultra-capacitor banks in current applications. The main analysis in this thesis, however, is based on the classical boost converter although the analysis was also extended for the fly back converter. Two other DC-DC converter topologies, namely the tri-state boost converter and the Z-Source inverter, are also examined during this thesis.

Since the ultra-capacitors are widely considered as a replacement for batteries, the performance of the ultra-capacitor based system is mainly compared with equivalent battery based systems in this thesis. The main attention was given to the analysis of the control characteristics as this is an area that is not widely reported in the current literature.

Although the ultra-capacitor is modeled accurately by a ladder circuit of RC elements, it is shown in this thesis that the classical model for the ultra-capacitor is sufficient to analyze control characteristics. This is mainly because the classical model is capable of approximately predicting the dominant poles and zeros of the ultra-capacitor based system transfer functions, which are the necessary roots in analyzing any higher order system. The ladder circuit models, when used for the analysis, results in a large number of non dominant pole-zero pairs, which increases the system complexity and obscure symbolical analysis. Hence, the system analysis with ladder model for ultra-capacitors is only seen to be convenient in a numerical analysis.

When the classical model is used for the analysis, the system transfer functions of the ultra-capacitor based ride through systems for the ASD is seen to contain an additional low frequency pole-zero pair compared to the battery based systems. In duty ratio to dc link voltage transfer function, the zero is seen to be located within RHP and the pole is seen to be located within the LHP. The magnitude of the RHP zero is seen to be much smaller compared to the LHP pole. The existence of this pole zero pair also reduces the dc gain of the ultra-capacitor based system transfer functions compared to the battery based equivalents. Apart from this dominant pole-zero pair that lie very close to the origin, all the other poles and zeros of the transfer function are seen to be located approximately at the similar positions of the poles and zeros of an equivalent battery based system. Hence, the main difference in the transfer functions of the battery and ultra-capacitor based systems is seen to be the existence of the dominant low frequency pole-zero pair very close to the origin, in ultra-capacitor based systems. The additional low frequency pole-zero pair was shown to exist in ultra-capacitor based systems due to the finite capacitance of ultra-capacitors.

The RHP zeros in the open loop control to output transfer function of a system limits the stable control bandwidth of that system. This limit is obtained assuming that all the other LHP poles of the system lies far away from these RHP zeros. However, in an ultra-capacitor based

system, the additional low frequency RHP zero is always found with the nearby additional low frequency LHP pole. Therefore the limitations associated with this low frequency RHP zero does not affect the system performance severely as the effects of an isolated RHP zero. Therefore, the stability limitation associated with the low frequency RHP zero can largely be neglected when designing control systems for ultra-capacitor based systems. Nevertheless, an un-cancelled open loop pole-zero pair near the origin, similar to this pole zero pair of an ultra-capacitor based system, places an additional dominant closed loop pole near the origin. However, the response of this dominant closed loop pole will have a very large time constant, larger than 100 secs in general. Therefore, even if the system becomes unstable because of exceeding a stability limit associated with the low frequency RHP zero, it is not felt within a short period of few seconds, which is the useful operating period of an ultra-capacitor based system.

Therefore, when designing control systems for ultra-capacitor based systems, the low frequency RHP zero should be treated as on the origin. As a result, any stability limitation associated with RHP zeros occurs due to the high frequency RHP zero of the ultra-capacitor based system, which is approximately located at the position of the RHP zero of an equivalent battery based system. However the low frequency RHP pole, which has a much larger magnitude compared to the low frequency RHP zero, and the low dc gain of the ultra-capacitor based system, should be compensated when designing voltage mode controlled ultra-capacitor based systems, to achieve acceptable steady state performance.

By analyzing both the classical boost converter and the fly-back converter, which are the two converters that are widely used for the ultra-capacitor based ride through systems, it is shown that both these converters are affected by the low frequency pole-zero pair. The effect is shown to be slightly different for the two converters. The analysis is also extended to the tri-state boost converter, which is capable of eliminating the RHP zero from the classical battery based

boost converter control to output transfer function. However it is shown that the tri-state boost converter is also not capable of eliminating the low frequency RHP zero or the effect of the low frequency pole-zero pair of the ultra-capacitor based systems.

By deriving approximate expressions for the low frequency pole-zero pair, it was shown that the low frequency pole-zero pair always cancels each other at the origin when the capacitance approaches infinity. This explains the absence of the low frequency pole-zero pairs from the battery based system transfer functions and at the same time shows that by reducing the separation between the pole and the zero of the pair, the adverse effects of both the low frequency pole and the zero on the ultra-capacitor based system response can be minimized.

Therefore, such systems should behave similar to equivalent battery based systems. This makes it convenient to design controllers for the ultra-capacitor based system, since only an equivalent battery based system needs to be considered for the design. It is not required to pay special attention to the low frequency pole zero pair or the low dc gain of the ultra-capacitor based systems.

The peak current-mode control configuration is shown to be capable of pushing the low frequency pole of the ultra-capacitor based system very close to the origin compared to the voltage-mode control. However, it is not capable of moving the low frequency RHP zero from the position of the voltage-mode controlled system. Since the separation between the pole and the zero is reduced, the peak current-mode control is capable of pushing ultra-capacitor based systems closer to equivalent battery based systems. For systems that has the low frequency RHP zero very close to the origin, the improvement obtained with peak current-mode control in this respect, is seen to be very significant.

Simulation and experimental results were given to verify these conclusions and to show that the controllers for the with peak current-mode controlled ultra-capacitor based system can be designed considering an equivalent battery based system.

Application of sliding-mode control for the ultra-capacitor based ride through system was also investigated in this thesis. A sliding-mode control configuration that matches the peak current-mode control configuration in complexity and in the number of the sensors was used for the analysis. It was shown that the sliding-mode control configuration is capable of pushing the low frequency zero to the origin and the low frequency pole almost to the origin, thereby effectively canceling the low frequency pole-zero pair of the ultra-capacitor based ride through system in closed loop. The cancellation is seen to be almost exact for all practical purposes and the cancellation can be made more accurate by selecting a smaller time constant for the low pass filter that generates the reference for the inductor current. Simulation and experimental results were given to verify that the response of the ultra-capacitor based system is almost identical to an equivalent battery based system, and the controllers can be designed by considering an equivalent battery based system without considering the low frequency pole zero pair or the low dc gain associated with ultra-capacitor based systems.

In comparison, this analysis shows that the sliding-mode control is more suitable to control ultra-capacitor based ride through systems in view of achieving better steady state waveforms. The peak current-mode control is also seen to be adequate especially in cases where the low frequency RHP zero is very close to the origin in the open loop system.

The Z-Source inverter, which is a new inverter configuration proposed in recent years, is capable of directly interfacing a variable voltage source to an ac load that operate from a fixed rms voltage. Therefore, Z-Source inverter shows a considerable promise towards ultra-capacitor based power quality applications. However, the currently available literature does not give sufficient insight into the operation of the Z-Source inverters or to design them for a particular application.

In this thesis a detailed analysis on the Z-Source inverter and all its possible operating states was presented. Through this analysis it was shown that there can be a maximum of six possible

operating states for the Z source inverter. Up to now only three of these states had been identified in the available literature. These already identified states were termed as dynamic states, while the new states were termed as static states, in this thesis. Based on this analysis, two methods to design the Z-Source inverter to interface a given voltage source to a given load was introduced. The first method, i.e. the non linear method, is seen to be rather complex since a large number of non linear equations need to be solved. But it results in smaller values for the impedance network of the Z-Source inverter. The other method, i.e. the linear method, gives simple design guidelines based on small ripple approximation of the waveforms. However this method results in higher values for the components in the impedance network than the nonlinear method.

The nonlinear method and the linear method were based on the analysis of a battery based Z-source inverter. Therefore, they do not consider the effect of the low frequency pole-zero pair that is degrading the performance of the Ultra-capacitor based Z-source inverters. If this is also taken into consideration, then, it was shown that the Z-Source inverters designed using the linear method is more appropriate for ultra-capacitor based applications since the method results in larger impedance networks that minimize the separation between the low frequency pole-zero pair. Increasing the size of the ultra-capacitor bank can also be considered as an option to minimize the effects of the low frequency pole-zero pair, if the cost considerations allow.

In the control to output transfer function of the Ultra-capacitor based Z-source inverter, the low frequency pole is located on the origin and the low frequency zero is located very close to the origin in the RHP. This results in a RHP pole very close to the origin in closed loop system. Therefore the Ultra-capacitor based Z source inverter always operates in unstable mode. However, this instability is not very severe provided the RHP zero of the open loop system is

sufficiently close to the origin and the system is only intended to be operated for a small time duration.

8.2 Recommendations for Future Work

Ultra-capacitor based systems are intended to be operated only for a few seconds, which is a significant difference from their battery based counterparts, which are usually designed considering continuous operation. When a system is designed for continuous operation it is mandatory that it should always stay stable. However for a system that is intended to operate only for a few seconds, stability in the manner necessary for continuous systems may not be a critical issue provided the system response can be maintained within specified limits during the intended operating period.

In this thesis a detailed analysis on the above aspect was not done. Hence the characterization of stable and unstable ultra-capacitor based systems was done based on the existing theory applicable to continuous systems. However, deriving dedicated guidelines for designing control systems for systems that are intended to operate only for a limited period is a challenging task that can be useful for the optimization of control systems in short term applications such as ultra-capacitor based ride through systems.

Ultra-capacitor is best represented by a ladder model rather than the classical model. As shown in this thesis, the ladder model introduces several non dominant pole-zero pairs to the system transfer functions, which tends to modify the system transient properties. These additional pole-zero pairs added were neglected in the analysis in this thesis since they do not represent the dominant poles or the zeros of the system. However their effect on the transient response of the ride through system appears to be an interesting subject for further analysis.

The design of ultra-capacitor banks are mostly carried out considering the classical model for the ultra-capacitor. This is mainly due to simplicity and also since an approximate design is

sufficient for most of the current applications. However design of ultra-capacitor banks considering its more advanced models may lead to optimization of the transient performance of ultra-capacitor based systems.

In this thesis the most challenging operation of the ultra-capacitor based ride through system is considered as the boost operation in which the ultra-capacitor bank supplies power to the load during a source disturbance. It is assumed that the charging of ultra-capacitors, i.e. the buck operation of the interfacing DC-DC converter, is not very time critical since it is carried out when the source is healthy. However when the size of the ultra-capacitor bank is optimized due to cost considerations, the number of ride through cycles it can perform before recharging again is intentionally reduced. Under such conditions it may be necessary to bring the ultra-capacitor bank to full charge again within a set time frame. This subject also can be considered as an important area for future research.

The main attention in this thesis was given to classical control methods such as voltage-mode control and peak current-mode control, which are widely employed for ultra-capacitor based ride through applications. Sliding-mode control was also analyzed in addition to these two methods. However the effect of more advanced control methods such as fuzzy logic and neural methods or optimal control is another interesting area for future research.

Ultra-capacitors also find a wide range of power quality applications other than ride through systems. Two of the popular applications are the dynamic voltage restorers and distribution static compensators. Other than this, they are also suitable to use together with another power source, such as a fuel cell or a battery, to enhance the lifetime of these power sources. Investigating these ultra-capacitor based applications can also be considered as an important subject for future research.

Only the open loop analysis of the ultra-capacitor based Z-source inverter was performed in this thesis. The analysis of the properties of the closed loop ultra-capacitor based Z-source inverters can also be highlighted as a significant area for future research.

Author's Publications

1. Y. R. L. Jayawickrama and S. Rajakaruna, "Ultracapacitor supplied ride-through system for a DC load", IEEE International Conference on Power System Technology, 2004, vol. 1, pp. 232-237.
2. S. Rajakaruna and Y. R. L. Jayawickrama, "Designing Impedance Network of Z-Source Inverters", Seventh International Power Engineering conference, IPEC2005, Nov 29 – Dec 2, 2005, Singapore.
3. Y. R. L. Jayawickrama and R. M. A. S. Rajakaruna, "Control of ultra-capacitor based ride through systems in adjustable speed drives", EEE research bulletin, 2005.
4. S. Rajakaruna, Y.R.L. Jayawickrama and N.N. Maw, "Steady-State Analysis and Designing of a Symmetrical Impedance Network for Z-Source Inverters", *IEEE Transactions on Industrial Electronics*, accepted for publication in Aug. 2006

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APPENDICES

Appendix A

A1. Derivation of the Linearised System Transfer Functions from Middlebrook's State Space Averaging Theory

Assume that the state space equations for a power converter can be written as given below. In these expressions X is the vector of state variables, U is the vector of independent sources and Y is the vector of output variables. The matrices A_1 , B_1 , A_2 , B_2 , C_1 , D_1 , C_2 and D_2 represents the respective system matrices in each of the two switched networks.

When the switching device is on,

$$\text{System state equation, } \dot{X} = A_1 X + B_1 U$$

$$\text{Output equation, } Y = C_1 X + D_1 U$$

When the switching device is off,

$$\text{System state equation, } \dot{X} = A_2 X + B_2 U$$

$$\text{Output equation, } Y = C_2 X + D_2 U$$

Based on these equations, the average state space model for the system is derived as below.

(d denotes the duty ratio in the following equations)

$$\text{Average system state equation, } \dot{X} = A' X + B' U$$

$$\text{Average output equation, } Y = C' X + D' U$$

Where, $A' = A_1 d + A_2 (1 - d)$, $B' = B_1 d + B_2 (1 - d)$, $C' = C_1 d + C_2 (1 - d)$ and $D' = D_1 d + D_2 (1 - d)$

Let $d = d_0 + \tilde{d}$,

Where d_0 = steady (dc) part of the duty ratio and $\tilde{d}$ = small perturbations of d around d_0 .

Similarly, let $X = \bar{X} + \tilde{X}$, $Y = \bar{Y} + \tilde{Y}$ and $U = \bar{U} + \tilde{U}$, with the index '-' above a particular variable representing the steady state of that variable.

These perturbed values of d , X , Y and U are substituted in the average state space equations above, to get the perturbed and steady state equations. In simplifications, it is assumed that second or higher order multiplications of small perturbations are negligible

Perturbed (ac) equations:

$$\dot{\tilde{X}} = A \tilde{X} + [(A_1 - A_2)\bar{X} + (B_1 - B_2)\bar{U}] \tilde{d} + B \tilde{U} \quad (A1-1)$$

$$\tilde{Y} = C \tilde{X} + [(C_1 - C_2)\bar{X} + (D_1 - D_2)\bar{U}] \tilde{d} + D \tilde{U} \quad (A1-2)$$

Steady state (dc) equations:

$$A \bar{X} + B \bar{U} = \dot{\bar{X}} \Rightarrow \bar{X} = A^{-1} (\dot{\bar{X}} - B \bar{U}) \quad (A1-3)$$

$$\bar{Y} = C \bar{X} + D \bar{U} \quad (A1-4)$$

Where, $A = A_1 d_0 + A_2 (1 - d_0)$, $B = B_1 d_0 + B_2 (1 - d_0)$, $C = C_1 D + C_2 (1 - d_0)$ and $D = D_1 d_0 + D_2 (1 - d_0)$

In steady state, $\dot{\bar{X}} = 0$, for power converters supplied by constant emf batteries. However, this is not the case with ultra-capacitor based converters.

In ultra-capacitor based converters, the ultra-capacitor terminal voltage always drops with time in open loop. As a result all the other circuit states will also show a decay with time.

Output Transfer Functions:

By taking the Laplace transforms of equations (A1-1) and (A1-2), the following small signal transfer functions can be obtained for the output of the system. In these equations, s is the Laplace variable and I is the identity matrix.

$$\frac{\tilde{Y}(s)}{\tilde{d}(s)} = G_{Vd}(s) = \left(C (sI - A)^{-1} [(A_1 - A_2)\bar{X} + (B_1 - B_2)\bar{U}] + [(C_1 - C_2)\bar{X} + (D_1 - D_2)\bar{U}] \right) \quad (A1-5)$$

$$\frac{\tilde{Y}(s)}{\tilde{U}(s)} = G_{VU}(s) = C (sI - A)^{-1} B + D \quad (A1-6)$$

These small signal output transfer functions are valid around the steady state, $\bar{X}$, calculated above.

The subscript u or b is used with G_{Vd} and G_{VU} to distinguish between ultra-capacitor based system transfer functions and battery based system transfer functions respectively.

State Transfer Functions:

From (A1-1) the state transfer functions can be obtained as,

$$\tilde{X}(s) = G_d(s) \cdot \tilde{d}(s) + G_U(s) \cdot \tilde{U}(s) \quad (A1-7)$$

Where, $G_d(s) = (sI - A)^{-1} (A_1 - A_2) \bar{X}$ and $G_U(s) = (sI - A)^{-1} B$

$$\text{Define } G(s) \text{ as, } G(s) = \begin{bmatrix} G_d(s) & G_U(s) \end{bmatrix} = \begin{bmatrix} G_{X1d} & G_{X1U} \\ G_{X2d} & G_{X2U} \\ G_{X3d} & G_{X3U} \\ G_{X4d} & G_{X4U} \end{bmatrix} \quad (A1-8)$$

A2. System Matrices and Transfer Functions of Battery based ride through system

For the battery based ride through system, the state matrices and vectors are given by,

$$\left. \begin{aligned} A_k &= \begin{bmatrix} -R_i/L_i & b_k & 0 \\ a_k & 0 & 1/C_f \\ 0 & -1/L_S & -R_S/L_S \end{bmatrix}, \begin{cases} \text{for } k=1, a_k = b_k = 0 \\ \text{for } k=2, a_k = 1/C_f, b_k = -1/L_i \end{cases} \\ B &= \begin{bmatrix} 0 & 1/L_i & 0 \\ -1/C_f & 0 & 0 \\ 0 & 0 & 1/L_S \end{bmatrix} \text{ and } C = [0 \ 1 \ 0], U = [I \ E_b \ E_S]^T \end{aligned} \right\} \quad (A2-1)$$

Assume that the steady state is given by $X_0 = [\bar{X}_2 \ \bar{X}_3 \ \bar{X}_4]^T$.

The necessary transfer functions can be derived by substituting these matrices in (A1-5) and (A1-6) as,

$$G_{Vdb}(s) = \frac{(s L_S + R_S)[(\bar{X}_3(1-d_0) - R_i \bar{X}_2) - L_i \bar{X}_2 s]}{D_b(s)} \quad (A2-2)$$

$$G_{Sdb}(s) = \frac{(L_i s + R_i)}{D_b(s)} \quad (A2-3)$$

Where $D_b(s)$ denotes the denominator of the transfer functions, which is given by,

$$D_b(s) = (a_3 s^3 + a_2 s^2 + a_1 s + a_0) \cdot (L_i C_f L_S) \quad (A2-4)$$

where, $a_3 = 1$, $a_2 = \frac{R_i}{L_i} + \frac{R_S}{L_S}$, $a_1 = \frac{(1-d_0)^2}{L_i \cdot C_f} + \frac{R_i R_S}{L_i L_S} + \frac{1}{C_f L_S}$ and

$$a_0 = \frac{(1-d_0)^2 R_S}{L_i \cdot C_f L_S} + \frac{R_i}{L_i \cdot C_f L_S}$$

A3 System matrices and Transfer Functions of Ultra-capacitor based ride through System with Classical Model of Ultra-capacitors

A3.1. Load represented by a constant current source

For the system shown in Fig 5.4, the system matrices and the vectors are given by,

$$\left. \begin{aligned} A_k &= \begin{bmatrix} 0 & -1/C_{uc} & 0 & 0 \\ 1/L_i & -R_i/L_i & b_k & 0 \\ 0 & a_k & 0 & 1/C_f \\ 0 & 0 & -1/L_S & -R_S/L_S \end{bmatrix}, \begin{cases} \text{for } k=1, a_k = b_k = 0 \\ \text{for } k=2, a_k = 1/C_f, b_k = -1/L_i \end{cases} \\ B_1 = B_2 &= \begin{bmatrix} 0 & 0 & -1/C_f & 0 \\ 0 & 0 & 0 & 1/L_S \end{bmatrix}^T, C_1 = C_2 = [0 \quad 0 \quad 1 \quad 0] \text{ and } D_1 = D_2 = [0 \quad 0]^T. \\ U &= [I \quad E_S]^T \text{ and } X = [X_1 \quad X_2 \quad X_3 \quad X_4]^T, Y = V_{dc}. \end{aligned} \right\} \quad (A3-1)$$

First method: Assuming a constant $\bar{X}_1$ to calculate steady state and deriving transfer functions

By replacing the ultra-capacitor bank with a battery having a constant emf $\bar{X}_1$, the relationships at the steady state $X_0 = [\bar{X}_1 \ \bar{X}_2 \ \bar{X}_3 \ \bar{X}_4]^T$, can be derived using (A1-3) as,

$$\bar{X}_2 = [\bar{X}_1 - (1-d_0)(\bar{E}_S - IR_S)] / (R_i + (1-d_0)^2 R_S) \quad (A3-2)$$

$$\bar{V}_{DC} = \bar{X}_3 = [(1-d_0)R_S \bar{X}_1 + R_i(\bar{E}_S - IR_S)] / (R_i + (1-d_0)^2 R_S) = (1-d_0)R_S \bar{X}_2 + (\bar{E}_S - IR_S) \quad (A3-3)$$

$$\bar{X}_4 = [(1-d_0)^2 \bar{E}_S - ((1-d_0)\bar{X}_1 - IR_i)] / (R_i + (1-d_0)^2 R_S) = \bar{I} - (1-d_0)\bar{X}_2 \quad (A3-4)$$

where, $\bar{V}_{DC} = \bar{X}_3$ is the average dc link voltage.

Note that the ultra-capacitor based systems have no steady-state during operation and the ultra-capacitor voltage will be either increasing or decreasing during operations. Therefore the desired relationships are strictly valid only at initial state before charging or discharging.

Assume that this steady state is given by $X_0 = [\bar{X}_1 \ \bar{X}_2 \ \bar{X}_3 \ \bar{X}_4]^T$.

The necessary transfer functions can be derived by substituting the system matrices and vectors given in (A2-1) in (A1-5) and (A1-6) as,

$$G_{Vdu}(s) = \frac{-(sL_S + R_S)[C_{uc}L_i\bar{X}_2s^2 - C_{uc}(\bar{X}_3(1-d_0) - R_i\bar{X}_2)s + \bar{X}_2]}{D_{du}(s)} \quad (A3-5)$$

$$G_{VUu}(s) = \frac{(L_i C_{uc} s^2 + R_i C_{uc} s + 1)}{D_{du}(s)} \quad (A3-6)$$

Where $D_{du}(s)$ denotes the denominator of the transfer functions, which is given by,

$$D_{du}(s) = (a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0) \cdot (C_{uc}L_iC_fL_S) \quad (A3-7)$$

where, $a_4 = 1$, $a_3 = \frac{R_i}{L_i} + \frac{R_S}{L_S}$, $a_2 = \frac{(1-d_0)^2}{L_i \cdot C_f} + \frac{R_i R_S}{L_i L_S} + \frac{1}{C_f L_S} + \frac{1}{L_i \cdot C_{uc}}$

$$a_1 = \frac{(1-d_0)^2 R_S}{L_i \cdot C_f L_S} + \frac{R_S}{L_i \cdot C_{uc} L_S} + \frac{R_i}{L_i \cdot C_f L_S} \text{ and } a_0 = \frac{1}{C_{uc} \cdot L_i \cdot C_f \cdot L_S}$$

Second Method: Estimating X_0 for a linear decay of ultra-capacitor terminal voltage and deriving transfer functions

As mentioned after the steady state equations ((A1-3) and (A1-4)) in appendix A1, the ultra-capacitor terminal voltage always drops with time together with other state variables, when the converter is operated in open loop. Moreover, if the rate of decay of ultra-capacitor terminal voltage is small, then the rate of decay of all the other state variables can be assumed as small in open loop. Under these conditions, the rate of decay of the state variables can be assumed as constant. i.e. $\dot{\bar{X}}_1 = k_1$, $\dot{\bar{X}}_2 = k_2$, $\dot{\bar{X}}_3 = k_3$, $\dot{\bar{X}}_4 = k_4$ (A3-8)

where, k_1, k_2, k_3, k_4 are negative constants.

Therefore, $\dot{\bar{X}}$ in (A1-3) may be written as, $\dot{\bar{X}} = [k_1, k_2, k_3, k_4]$ (A3-9)

Substituting (A3-9) and (A3-1) in (A1-3), the following expression can be derived for the approximate steady state of the ultra-capacitor based converter.

$$\bar{X} = X_0 = \begin{bmatrix} \bar{X}_1 \\ \bar{X}_2 \\ \bar{X}_3 \\ \bar{X}_4 \end{bmatrix} = \begin{bmatrix} -C_{uc} k_1 [R_S (1-d_0)^2 + R_i] + k_2 L_i + (1-d_0) \{(\bar{E}_S - \bar{I} R_S) - \rho\} \\ -C_{uc} k_1 \\ -C_{uc} R_S (1-d_0) k_1 + (\bar{E}_S - \bar{I} R_S) - \rho \\ C_{uc} (1-d_0) k_1 + \bar{I} + C_f k_3 \end{bmatrix} \quad (A3-10)$$

Where, $\rho = [L_S k_4 + R_S C_f k_3]$.

The first term in (A3-10) describes how $\bar{X}_1$ changes with the converter duty ratio.

The expression in (A3-10) can be further simplified as,

$$\bar{X} = X_0 = \begin{bmatrix} \bar{X}_1 \\ \bar{X}_2 \\ \bar{X}_3 \\ \bar{X}_4 \end{bmatrix} = \begin{bmatrix} \bar{X}_1 \\ \frac{(\bar{X}_1 - (1-d_0)(\bar{E}_S - \bar{I} R_S) - L_i k_2 + [L_S k_4 + R_S C_f k_3](1-d_0))}{\left(\frac{R_i + (1-d_0)^2 R_S}{R_S (1-d_0) \bar{X}_2 + (\bar{E}_S - \bar{I} R_S) - [L_S k_4 + R_S k_3]} \right)} \\ \bar{X}_3 \\ \bar{X}_4 \end{bmatrix} \quad (A3-11)$$

There after, deriving the transfer functions as described in the first method, results in exactly the same transfer function expressions given in (A3-5) and (A3-6) for the ultra-capacitor based converter. However, the transfer functions derived from this method are different from the transfer functions of the first method, since the values of $\bar{X}$ are different as can be seen from (A3-2) – (A3-4) and (A3-11). Nevertheless, the transfer functions of the first method and the second method will approximately be equal for small k_1, k_2, k_3 and k_4 values.

Therefore, both these methods are seen to be equally good to determine the transfer functions of the ultra-capacitor based converter.

A3.2. Load represented by a general RL load

When the constant current load shown in Fig 5.4, is replaced by a RL load the system matrices and vectors are given by,

$$\left. \begin{aligned} A_k &= \begin{bmatrix} 0 & -1/C_{uc} & 0 & 0 & 0 \\ 1/L_i & -R_i/L_i & b_k & 0 & 0 \\ 0 & a_k & 0 & 1/C_f & -1/C_f \\ 0 & 0 & -1/L_S & -R_S/L_S & 0 \\ 0 & 0 & 1/L_L & 0 & -R_L/L_L \end{bmatrix}, & \begin{cases} \text{for } k=1, a_k = b_k = 0 \\ \text{for } k=2, a_k = 1/C_f, b_k = -1/L_i \end{cases} \\ B &= [0 \ 0 \ 0 \ 1/L_S \ 0], \ C = [0 \ 0 \ 1 \ 0 \ 0], \ U = [E_S], \\ X &= [X_1 \ X_2 \ X_3 \ X_4 \ X_5]^T \text{ and } Y = V_{dc}. \end{aligned} \right\} \quad (A3-12)$$

By taking the steady state as $X_0 = [\bar{X}_1 \ \bar{X}_2 \ \bar{X}_3 \ \bar{X}_4 \ \bar{X}_5]^T$, the steady state relationships of this system can be obtained by using (A1-3) as follows.

$$\bar{X}_2 = \bar{X}_1 / (R_i + (1-d_0)^2 R_L) \quad (A3-13)$$

$$\bar{X}_3 = \bar{V}_{dc} = \frac{\bar{X}_1}{(1-d_0)} \left[1 / \left(1 + \frac{R_i}{(1-d_0)^2 R_L} \right) \right] \quad (A3-14)$$

$$\bar{X}_4 = \bar{X}_5 = \frac{\bar{E}_s}{R_L + R_S} \quad (A3-15)$$

The necessary transfer functions can be derived by substituting the above matrices in (A1-5) and (A1-6) as,

$$G_{Vdu}(s) = \frac{-(sL_S + R_S)(sL_L + R_L)[C_{uc}L_i\bar{X}_2s^2 - C_{uc}(\bar{X}_3(1-d_0) - R_i\bar{X}_2)s + \bar{X}_2]}{D_{du}(s)} \quad (A3-16)$$

$$G_{VUu}(s) = \frac{(sL_L + R_L)(L_iC_{uc}s^2 + R_iC_{uc}s + 1)}{D_{du}(s)} \quad (A3-17)$$

where, $D_{du}(s) = (a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0) \cdot (C_{uc}L_iC_fL_SL_L)$,

$$a_5 = 1, \quad a_4 = \frac{R_i}{L_i} + \frac{R_S}{L_S} + \frac{R_L}{L_L}, \quad a_3 = \frac{(1-D_0)^2}{L_iC_f} + \frac{R_i}{L_i} \left[\frac{R_S}{L_S} + \frac{R_L}{L_L} \right] + \frac{1}{C_f} \left[\frac{1}{L_L} + \frac{1}{L_S} \right] + \frac{R_S \cdot R_L}{L_S \cdot L_L} + \frac{1}{L_i \cdot C_{uc}}$$

$$a_2 = \frac{(1-D_0)^2}{L_iC_f} \left[\frac{R_S}{L_S} + \frac{R_L}{L_L} \right] + \frac{1}{L_iC_{uc}} \left[\frac{R_S}{L_S} + \frac{R_L}{L_L} \right] + \frac{R_S + R_L}{C_f \cdot L_S \cdot L_L} + \frac{R_i}{L_iC_f} \left[\frac{1}{L_S} + \frac{1}{L_L} \right] + \frac{R_i \cdot R_S \cdot R_L}{L_i \cdot L_L \cdot L_S},$$

$$a_1 = \frac{R_S \cdot R_L \cdot (1-D_0)^2}{L_iC_f \cdot L_S \cdot L_L} + \frac{R_i \cdot (R_S + R_L)}{L_iC_f \cdot L_S \cdot L_L} + \frac{R_S \cdot R_L}{C_{uc} \cdot L_i \cdot L_S \cdot L_L} + \frac{1}{C_{uc} \cdot L_i \cdot C_f \cdot L_L} + \frac{1}{C_{uc} \cdot L_i \cdot C_f \cdot L_S} \text{ and}$$

$$a_0 = \frac{R_S + R_L}{C_{uc} \cdot L_i \cdot C_f \cdot L_S \cdot L_L}$$

A3.3 Capacitor Based Classical Boost Converter

The control to output transfer function for the standalone capacitor based classical boost converter, which is given below, can be obtained from (A3-16) by taking the limiting transfer function when $L_S \rightarrow \infty$ and $L_L \rightarrow 0$.

$$G_{Vdu}(s) = \frac{-[C_{uc}L_i\bar{X}_2s^2 - C_{uc}(\bar{X}_3(1-d_0) - R_i\bar{X}_2)s + \bar{X}_2]}{D_{du}(s)} \quad (A3-18)$$

where, $D_{du}(s) = (a_3s^3 + a_2s^2 + a_1s + a_0) \cdot (C_{uc}L_iC_f)$,

$$a_3 = 1, \quad a_2 = \frac{R_i}{L_i} + \frac{1}{C_fR_L}, \quad a_1 = \frac{(1-D_0)^2}{L_iC_f} + \frac{R_i}{L_iC_fR_L} + \frac{1}{L_iC_{uc}} \text{ and } a_0 = \frac{1}{C_{uc}L_iC_fR_L}$$

The steady state of this system can be obtained by substituting $R_S \rightarrow \infty$ in (A3-13) to (A3-15) as,

$$\bar{X}_2 = \bar{X}_1 / (R_i + (1 - d_0)^2 R_L) \quad (\text{A3-19})$$

$$\bar{X}_3 = \bar{V}_{dc} = \frac{\bar{X}_1}{(1 - d_0)} \left[1 / \left(1 + \frac{R_i}{(1 - d_0)^2 R_L} \right) \right] \quad (\text{A3-20})$$

A4 System Matrices for Ultra-capacitor Based Ride Through System with Advanced Ultra-capacitor Model

For the system shown in Fig. 5.6, the system matrices and the state and source vectors are given by,

$$\begin{aligned}
 A_k = & \left[\begin{array}{cccccccccccc} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_{uc}} & 0 & 0 \\ 0 & \frac{-2}{RC_{uc}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & \frac{-8}{RC_{uc}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & 0 & \frac{-18}{RC_{uc}} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-32}{RC_{uc}} & 0 & 0 & 0 & 0 & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-50}{RC_{uc}} & 0 & 0 & 0 & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-72}{RC_{uc}} & 0 & 0 & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-98}{RC_{uc}} & 0 & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-128}{RC_{uc}} & 0 & \frac{-2}{C_{uc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-162}{RC_{uc}} & \frac{-2}{C_{uc}} & 0 & 0 \\ \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{1}{L_i} & \frac{-R_i}{L_i} & b_k & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & a_k & 0 & \frac{1}{C_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_s} & \frac{-R_s}{L_s} \end{array} \right] \quad (A4-1) \\
 & \left. \begin{aligned} & \text{for } k = 1, a_k = b_k = 0 \\ & \text{for } k = 2, a_k = 1/C_f, b_k = -1/L_i \end{aligned} \right\} \\
 B_1 = B_2 = & \left[\begin{array}{cccccccccccc} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_f} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_s} \end{array} \right]^T, \\
 C_1 = C_2 = & [0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0], \\
 D_1 = D_2 = & [0 \ 0]^T
 \end{aligned}$$

Assume that the steady state is given by,

$$X_0 = [\bar{X}_1 \ \bar{X}_2 \ \bar{X}_3 \ \bar{X}_4 \ \bar{X}_5 \ \bar{X}_6 \ \bar{X}_7 \ \bar{X}_8 \ \bar{X}_9 \ \bar{X}_{10} \ \bar{X}_{11} \ \bar{X}_{12} \ \bar{X}_{13}]^T.$$

As explained as explained, this steady state is also strictly accurate only at the initial state of a discharging or charging process of the ultra-capacitor bank.

System transfer functions can be derived in the same way as above by substituting these matrices in (A1-5) and (A1-6). However as expected, it is difficult to simplify the transfer functions.

Appendix B

Comparison of Pole-zero Map of Ladder Model and Classical Model of the Ultra-capacitor

To compare the effect of using the ladder model or the classical model for the ultra-capacitor on the ride through system transfer functions, consider the stand alone ride through system (i.e. without the source) with a resistive load.

For the ladder model, only the two branch ladder model, which is shown in Fig B, is considered here to simplify the analysis. The lead inductance and the lead resistance shown are considered together with L_i and R_i of the boost converter when deriving system transfer functions.

Fig. B: Two branch ladder model for the ultra-capacitor

The standalone system transfer functions can be obtained by taking the limiting transfer functions by allowing $L_S \rightarrow \infty$ in the transfer functions derived as described in Appendix A. Only the control to output transfer function is considered for the comparison. Similar comparisons are also possible for all the other system transfer functions.

B1. Control to Output Transfer Function with Classical Model:

The control to output transfer function with classical model can be obtained as,

$$G_{vdu}(s)_{\text{classical}} = \frac{N_{du}(s)_{\text{classical}}}{D_{du}(s)_{\text{classical}}} \quad (\text{B1-1})$$

Where, $D_{du}(s)_{\text{classical}} = (a_{3c}s^3 + a_{2c}s^2 + a_{1c}s + a_{0c}) \cdot (C_{uc}L_iC_fR_L)$ and

$$N_{du}(s)_{\text{classical}} = -(R_L C_{uc} L_i \bar{X}_2) [b_{2c}s^2 + b_{1c}s + b_{0c}]$$

$$a_{3c} = 1, a_{2c} = \frac{R_i}{L_i} + \frac{1}{C_f R_L}, a_{1c} = \frac{(1-d_0)^2}{L_i C_f} + \frac{R_i}{L_i R_L C_f} + \frac{1}{L_i C_{uc}}, a_{0c} = \frac{1}{L_i C_{uc} R_L C_f}$$

$$b_{2c} = 1, b_{1c} = -\frac{(\bar{X}_3(1-d_0) - R_i \bar{X}_2)}{L_i \bar{X}_2}, b_{0c} = \frac{\bar{X}_2}{C_{uc} L}$$

Note that all the coefficients on the denominator are positive, and Therefore, all the system poles are on the LHP as explained in Appendix C below. In order to obtain simple expressions for system poles, assume that R_L is very large. Under this condition the effect of the load is minimized and the denominator can be simplified to,

$$D_{du}(s)_{\text{classical}} = s \left[s^2 + \frac{R_i}{L_i} s + \left(\frac{(1-d_0)^2}{L_i C_f} + \frac{1}{L_i C_{uc}} \right) \right] \cdot (C_{uc} L_i C_f) \quad (\text{B1-2})$$

Therefore, the approximate system poles are obtained as,

$$P_{1u_classical} \cong 0, \quad (\text{B1-3})$$

$$P_{2u_classical} \cong \frac{-R_i}{2L_i} + \sqrt{\left(\frac{R_i}{2L_i} \right)^2 - \left(\frac{(1-d_0)^2}{L_i C_f} + \frac{1}{L_i C_{uc}} \right)} \quad (\text{B1-4})$$

$$P_{3u_classical} \cong \frac{-R_i}{2L_i} - \sqrt{\left(\frac{R_i}{2L_i} \right)^2 - \left(\frac{(1-d_0)^2}{L_i C_f} + \frac{1}{L_i C_{uc}} \right)} \quad (\text{B1-5})$$

This means that one of the system poles is located very close to the origin in the LHP while the other two are relatively far away from the origin.

B2. Control to Output Transfer Function with Two Branch Ladder Model:

The control to output transfer function with two branch ladder model can be obtained as,

$$G_{vdu}(s)_{ladder} = \frac{N_{du}(s)_{ladder}}{D_{du}(s)_{ladder}} \quad (B2-1)$$

Where, $D_{du}(s)_{ladder} = -(a_{4l}s^4 + a_{3l}s^3 + a_{2l}s^2 + a_{1l}s + a_{0l}) \cdot (C_{uc0}C_{uc1}L_iR_1R_LC_f)$

$$N_{du}(s)_{ladder} = -(C_{uc0}C_{uc1}L_iR_1R_L\bar{X}_2)[b_{3l}s^3 + b_{2l}s^2 + b_{1l}s + b_{0l}]$$

$$a_{4l} = 1, a_{3l} = \frac{R_i}{L_i} + \frac{1}{C_fR_L} + \frac{1}{R_1} \left(\frac{1}{C_{uc0}} + \frac{1}{C_{uc1}} \right),$$

$$a_{2l} = \frac{(1-d_0)^2}{L_iC_f} + \frac{R_i}{L_iR_LC_f} + \frac{1}{L_iC_{uc0}} + \frac{1}{R_1} \left[\left(\frac{1}{C_{uc0}} + \frac{1}{C_{uc1}} \right) \left(\frac{R_i}{L_i} + \frac{1}{R_LC_f} \right) \right],$$

$$a_{1l} = \frac{1}{C_{uc0}L_iR_LC_f} + \frac{1}{R_1} \left[\frac{1}{L_iC_{uc0}C_{uc1}} + \left(\frac{1}{C_{uc0}} + \frac{1}{C_{uc1}} \right) \left(\frac{R_i}{L_iR_LC_f} + \frac{(1-d_0)^2}{L_iC_f} \right) \right],$$

$$a_{0l} = \frac{1}{C_{uc0}C_{uc1}L_iR_1R_LC_f}$$

$$b_{3l} = 1, b_{2l} = - \left[\frac{(\bar{X}_3(1-d_0) - R_i\bar{X}_2)}{L_i\bar{X}_2} - \frac{1}{R_1} \left(\frac{1}{C_{uc0}} + \frac{1}{C_{uc1}} \right) \right],$$

$$b_{1l} = \frac{1}{L_iC_{uc0}} + \frac{1}{R_1} \left[\frac{1}{L_i} \left(\frac{1}{C_{uc0}} + \frac{1}{C_{uc1}} \right) \left(R_i - \frac{\bar{X}_3(1-d_0)}{\bar{X}_2} \right) \right], b_{0l} = \frac{1}{R_1C_{uc0}C_{uc1}L_i}$$

Note that all the coefficients on the denominator are positive, and therefore, all the system poles are on the LHP as explained in Appendix C below. Again, in order to obtain simple expressions for system poles, assume that R_L is very large. Under this condition the denominator can be simplified to,

$$D_{du}(s)_{ladder} = s \left[s^3 + \left(\frac{R_i}{L_i} + \frac{k}{R_1} \right) s^2 + \left(\frac{(1-d_0)^2}{L_iC_f} + \frac{1}{L_iC_{uc0}} + \frac{kR_i}{R_1L_i} \right) s + \frac{1}{R_1} \left(\frac{1}{L_iC_{uc0}C_{uc1}} + \frac{k(1-d_0)^2}{L_iC_f} \right) \right] (C_{uc}L_iC_f) \quad (B2-2)$$

$$\text{Where, } k = \left(\frac{1}{C_{uc0}} + \frac{1}{C_{uc1}} \right).$$

Therefore, from (B2-2), it is seen that one of the poles is again located very close to origin. Therefore,

$$P_{lu_ladder} \cong 0 \quad (B2-3)$$

Furthermore, it is seen that if R_1 is infinite (i.e. similar to classical model), the terms within the square brackets in (B1-2) and (B2-2) coincides, provided $C_{uc} = C_{uc0}$. When $R_1 \rightarrow \infty$, a pole-zero cancellation occurs with the numerator at the origin in (B2-1), transferring (B2-2) also to a third order polynomial. Therefore, it can be determined that the additional pole due to the ladder branch R_1, C_{uc1} , is represented by the expression within square brackets in (B2-2). Therefore, the dominant pole given in (B2-3) should correspond to the dominant pole given in (B1-3), or more accurately, it should be the pole associated with C_{uc0} .

Also from (B1-2) and (B2-2) it is seen that the additional pole increases the summation of poles from $-\frac{R_i}{L_i}$ to $-\left(\frac{R_i}{L_i} + \frac{k}{R_1}\right)$. For practical ultra-capacitors, k is in the range of few Farads and R_1 is in the range of milliohms. Therefore, this indicates a substantial increase in the summation of poles due to the added pole. This shows that the pole added due to the ladder branch R_1, C_{uc1} is in fact located somewhat far from the origin and not very close to the origin like the dominant poles described in (B1-3) and (B2-3).

Moving onto the numerator coefficients in (B2-1), it is seen that b_{0l} is always positive while b_{1l} is always negative. Note that both the zeros in (B1-1), i.e. when classical ultra-capacitor model is used, were positive. Therefore, the zero due to the ladder branch R_1, C_{uc1} , should be a negative (LHP) zero and it should at least have the medium magnitude of the three roots. Furthermore, by comparing expressions for b_{1c} and b_{2l} , it is seen that the summation of the roots of the numerator has reduced significantly due to the added zero under the ladder model. This means that the magnitude of the added LHP zero should also be high, indicating that it should be located reasonably far away from the origin in general.

In summary, this analysis shows that when one ladder branch, R_1, C_{uc1} , is added to the classical model of the ultra-capacitor, an additional pole-zero pair is added to the control to output transfer function of the ride through system. Furthermore, the added pole-zero pair is located in the LHP and its position is not very close to the origin as of the dominant pole and zero described in section 3.2.1. The exact position of the added pair depends on the value of R_1 . Comparing b_{1c} , b_{1l} , a_{2c} and a_{3l} further, it is also seen that the change in the summation of zeros and poles when the ladder branch is added is approximately the same and is equal to $\frac{k}{R_1}$. This also shows that the added LHP pole and the zero in the pole-zero pair is also located very close to each other.

For ultra-capacitor models with more than two ladder branches, this procedure can be repeated for each additional of ladder branch. For every addition, it can be shown that a pole-zero pair is added to the pole-zero map and they are always located away from the origin in LHP. They do not represent the dominant pole or the zero of the system. The dominant pole-zero pair of the ultra-capacitor systems is associated with the first capacitive element of the ladder and it can approximately be obtained using the classical model of the ultra-capacitor that uses only one capacitive element in the model.

Therefore, in order to estimate the position of the dominant pole-zero pair, the classical ultra-capacitor model is seen to be sufficient.

Appendix C

C1. Tri-state Boost Converter

System state matrices for the standalone tri-state boost converter operating with a resistive load are given below.

$$\left. \begin{aligned}
 A_k &= \begin{pmatrix} 0 & -1/C_{uc} & 0 \\ 1/L_i & -(R_i + R_{uc})/L_i & b_k \\ 0 & a_k & -1/(C_f R_L) \end{pmatrix} \begin{cases} \text{for } k=1, a_k = b_k = 0 \\ \text{for } k=2, a_k = 1/C_f, b_k = -1/L_i \end{cases} \\
 A_3 &= \begin{pmatrix} 0 & 0 & 0 \\ 0 & -R_i/L_i & 0 \\ 0 & 0 & -1/(C_f R_L) \end{pmatrix} \\
 B_1 = B_2 = B_3 &= (0 \ 0 \ 0)^T, \ C_1 = C_2 = C_3 = (0 \ 0 \ 1), \ D_1 = D_2 = D_3 = (0).
 \end{aligned} \right\} \quad (C1-1)$$

The matrices denoted by subscript 1 correspond to the boost interval (when both T_f and T_m are on), matrices denoted with subscript 2 correspond to the capacitor charging interval (when both T_f and T_m are off) and the matrices denoted by subscript 3 correspond to the freewheeling interval (when T_f on and T_m off).

The system perturbation and the linearization are performed similar to the procedure described in Appendix A. The only difference being the number of states involved, three, while it was two for the case described in Appendix A.

If the boost interval duty ratio is denoted as d_b and the capacitor charging interval duty ratio is denoted as d_o , then the average system matrix A is defined as, $A = A_1 d_{b0} + A_2 d_{o0} + A_3(1 - d_{b0} - d_{o0})$. The subscript '0' denotes the steady state. The other average matrices B , C and D are defined similarly.

The steady state expressions for the for the ultra-capacitor based tri-state boost converter can be obtained as follows under the same assumptions made for the classical boost converter.

$$\bar{X}_2 = \frac{(d_{b0} + d_{o0})}{(R_i + d_{o0}^2 R_L)} \bar{X}_1 \text{ and } \bar{V}_{dc} = \bar{X}_3 = \frac{(d_{b0} + d_{o0})}{(R_i + d_{o0}^2 R_L)} d_{o0} R_L \bar{X}_1 \quad (C1-2)$$

C2. Fly-back Converter

System state matrices for the standalone fly-back converter operating with a resistive load are given below.

$$\left. \begin{aligned} A_1 &= \begin{pmatrix} 0 & -1/C_{uc} & 0 \\ 1/L_m & -R_i/L_m & 0 \\ 0 & 0 & -1/(C_f R_L) \end{pmatrix}, A_2 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & -1/L_m \\ 0 & 1/C_f & -1/(C_f R_L) \end{pmatrix} \\ B_1 &= B_2 = (0 \ 0 \ 0)^T, C_1 = C_2 = (0 \ 0 \ 1), D_1 = D_2 = (0). \end{aligned} \right\} \quad (C2-1)$$

The system perturbation and the linearization are performed similar to the procedure described in Appendix A. The average system matrices A , B , C and D are also defined as described in Appendix A.

The steady state expressions for the for the ultra-capacitor fly-back converter can be obtained as follows under the same assumptions made for the classical boost converter.

$$\bar{X}_2 = \frac{d_0}{d_0 R_i + (1-d_0)^2 R_L} \bar{X}_1, \bar{X}_3 = \frac{d_0(1-d_0)R_L}{d_0 R_i + (1-d_0)^2 R_L} \bar{X}_1 \quad (C2-2)$$

C3. Z-Source Inverter

System state matrices for the Z-Source inverter operating with an ultra-capacitor bank is given below. It is assumed that the Z inverter is only operating in active 1, open 1 and the shoot through 1 states. The matrices given below were derived as per the equivalent circuit depicted in Fig 7.14.

$$\left. \begin{aligned} A_1 &= A_2 = \begin{pmatrix} 0 & -2/C_{uc} & 0 \\ 1/L & -(2R_{uc})/L & -1/L \\ 0 & 1/C & 0 \end{pmatrix}, A_3 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 1/L \\ 0 & -1/C & 0 \end{pmatrix}, \\ B_1 &= (1/C_{uc} \ R_{uc}/L \ -1/C)^T, B_2 = B_3 = (0 \ 0 \ 0)^T, C_1 = C_2 = (-1 \ 2R_{uc} \ 2), \\ C_3 &= (0 \ 0 \ 0), \\ D_1 &= (-R_{uc}), D_2 = D_3 = (0), U = (I_0) \end{aligned} \right\} \quad (C3-1)$$

The system perturbation and the linearization are performed similar to the procedure described in Appendix C1 for the tri-state boost converter.

If the active 1 state duty ratio is denoted as d_a and the shoot through 1 state duty ratio is denoted as d_s , then the average system matrix A is defined as, $A = A_1 d_{a0} + A_2(1 - d_{b0} - d_{o0}) + A_3 d_{s0}$. The subscript '0' denotes the steady state. The other average matrices B , C and D are defined similarly.

The steady state expressions for the for the Ultra-capacitor based Z-source inverter can be obtained as follows.

$$\bar{X}_2 = \frac{(d_{a0})}{(1-2d_{s0})} I_0 \text{ and } \bar{X}_3 = \frac{(1-d_{s0})}{(1-2d_{s0})} \bar{X}_1 - \frac{d_{a0} R_{uc}}{(1-2d_{s0})^2} I_0 \quad (C3-2)$$

Appendix D

D1. Small Signal Model Derivation and Closed Loop Transfer Functions for Sliding-mode Control

As derived in Appendix A, the perturbed state equation for the original system is given by,

$$\dot{\tilde{X}} = A' \tilde{X} + C' \tilde{d} + B \tilde{U} \quad (D1-1)$$

Where, $C' = (A_1 - A_2) \bar{X} + (B_1 - B_2) U_0$.

According to the general sliding-mode control theory, all the system state variables are sensed, and the corresponding state variable errors are multiplied by proper gains k_i and added together to form the sliding function ψ . i.e. for a system with N state variables, the sliding function is defined as,

$$\psi = \sum_{n=1}^N k_n (X_n - X_{n,ref}) = 0 \quad (D1-2)$$

Where $X_{n,ref}$ denotes the reference value of n^{th} state.

In general only some of the reference values $X_{n,ref}$ are fed externally. The other references are derived internally to the controller, normally by low pass filtering of the corresponding variables. This creates M additional state variables X_{int}^* whose dynamics are described by,

$$\dot{X}_{int}^* = -\frac{1}{\tau_i} X_{int}^* + \frac{1}{\tau_i} X_i \Rightarrow \dot{\tilde{X}}_{int}^* = T_1 X_{int}^* - T_2 X, \quad i=1,2,\dots,M \quad (D1-3)$$

where τ_i are the corresponding filter time constants. Note that T_1 is a diagonal $M \times M$ matrix, while T_2 is a $M \times N$ matrix given by, $T_2 = [T_1 \quad 0]$.

Thus the system order increases by M . The remaining $N - M$ state variable references are additional inputs. Note that the linear equation in (D1-3) holds even for perturbed variables.

Define the vector of all these state variables (small perturbations) as,

$$\tilde{X}' = \begin{bmatrix} \tilde{X} \\ \tilde{X}_{int}^* \end{bmatrix} \quad (D1-4)$$

Assuming that the converter operates in the sliding-mode, constraint (D1-2) implies that $\dot{\psi} = 0$.

Thus, considering the perturbed signals,

$$\dot{\tilde{\psi}} = K^T (\dot{\tilde{X}} - \dot{\tilde{X}}^*) = K^T \dot{\tilde{X}} - K_{int}^T \dot{\tilde{X}}_{int}^* - K_{ext}^T \dot{\tilde{X}}_{ext}^* = 0 \quad (D1-5)$$

in which the vector of sliding coefficients, K , is divided into two terms K_{int} and K_{ext} .

Therefore, from (D1-1) and (D1-3), the small perturbations of the converter duty cycle d can be expressed as,

$$\tilde{d} = D_{s1} \tilde{X}' + D_{s2} \tilde{U} + D_{s3} \tilde{X}_{ext}^* \quad (D1-6)$$

where, $D_{s1} = [D_{s11} \quad D_{s22}]$, $D_{s2} = -(K^T C')^{-1} \cdot (K^T B)$, $D_{s3} = -(K^T C')^{-1} \cdot (K_{ext}^T)$ with

$$D_{s11} = -(K^T C')^{-1} \cdot (K^T A + K_{int}^T T_2) \text{ and } D_{s22} = -(K^T C')^{-1} \cdot (K_{int}^T T_1).$$

Substituting (D1-6) in (D1-1) and using (D1-3), the linear system equation is obtained as,

$$\dot{\tilde{X}}' = A_c \tilde{X}' + B_c \tilde{U} + D_c \tilde{X}_{ext}^* \quad (D1-7)$$

$$\text{Where, } A_c = \begin{bmatrix} A + C'D_{s11} & C'D_{s22} \\ -T_2 & T_1 \end{bmatrix}, B_c = \begin{bmatrix} B + C'D_{s2} \\ 0 \end{bmatrix}, D_c = \begin{bmatrix} C'D_{s3} \\ 0 \end{bmatrix}$$

Considering the constraint (D1-2), the system order can be reduced by one. The final small signal model has order $(N + M - 1)$ and is given by,

$$\ddot{\tilde{X}}'' = A_T \tilde{X}'' + B_T \tilde{U} + D_{T1} \tilde{X}_{ext}^* + D_{T2} \dot{\tilde{X}}_{ext}^* \quad (\text{D1-8})$$

Assuming (D1-2) is solved for first state variable and substituted in (D1-7), the four matrices in (D1-8) are given by,

$$A_T = A_c(2:N + M, 2:N + M) + A_c(2:N + M, 1) \cdot F_1, B_T = B_c(2:N + M, :),$$

$$D_{T1} = A_c(2:N + M, 1) \cdot F_2, D_{T2} = D_c(2:N + M, :).$$

$$F_1 = (-1/k_1) \cdot [K^T(2:N) - K_{int}^T], F_2 = (1/k_1) \cdot K_{ext}^T.$$

(The notation $A(n:m, j:k)$ means the sub matrix obtained from matrix A taking rows from index $n-m$ and columns from index $j-k$. The symbol $:$ alone means all).

The necessary closed loop transfer functions can be obtained by taking the laplace transform of (D1-8).

D2. State Matrices and Closed Loop Transfer Functions for Ultra-capacitor Based System Under Sliding-mode Control

The general procedure for obtaining the closed loop transfer functions for DC-DC converters operating with sliding-mode control is given in [85]. Descriptions given below are applicable to the sliding-mode control of the ultra-capacitor based ride through system given in Chapter 6. System matrices under sliding-mode control for the ultra-capacitor based ride through system are given below. These are the same matrices given in Appendix A, but with the state order rearranged as shown in section 6.3.

$$A_k = \begin{bmatrix} -R_i/L_i & 0 & 1/L_i & b_k \\ 0 & -R_S/L_S & 0 & -1/L_S \\ -1/C_{uc} & 0 & 0 & 0 \\ a_k & 1/C_f & 0 & 0 \end{bmatrix}, \begin{cases} \text{for } k=1: \\ a_k = b_k = 0 \end{cases}, \begin{cases} \text{for } k=2: \\ a_k = 1/C_f, b_k = -1/L_i \end{cases}$$

$$B = \begin{bmatrix} 0 & 0 & 0 & -1/C_f \\ 0 & 1/L_S & 0 & 0 \end{bmatrix}^T, C = [0 \ 0 \ 0 \ 1], U = [I \ E_S]^T$$

Therefore, for this system, the order is 4, i.e $N = 4$.

Small signal model and the closed loop transfer functions for the ultra-capacitor based system are derived similar to the procedure discussed in Appendix D1 [69, 85]. The main equations are given below.

One LPF filter is added to the ultra-capacitor based system, to internally generate the reference, $X_{1,ref}$, for X_1 . Therefore, for this system, $M = 1$. Dynamic equation for this additional state is given by, $\dot{X}_{1,ref} = -(1/\tau)X_{1,ref} + (1/\tau)X_1$, which can be rewritten as,

$$\dot{X}_{1,ref} = T_1 X_{1,ref} - T_2 X \quad (D2-1)$$

where $T_1 = [-1/\tau]$ and $T_2 = [(-1/\tau), 0, 0, 0]$. τ represent the time constant of the first order LPF filter.

Therefore, the new total system state vector becomes,

$$X_{new} = [X_1, X_2, X_3, X_4, X_{1,ref}]^T \quad (D2-2)$$

System in Fig 6.4 has one external reference for dc link voltage, $X_{4,ref}$.

Also define the internal reference gain vector and the external reference gain vector as, $K_{int} = k_i$ and $K_{ext} = k_u$.

The new system state matrix of the total system can be obtained by including (D2-1) into the original system state equations given in Appendix A or (D1-1). After perturbation and linearization of these new set of equations in the same way as earlier [27, 28], the converter duty cycle and the linear system equations are obtained as,

$$\tilde{d} = D_1 \tilde{X}_{new1} + D_2 \tilde{U} + D_3 \tilde{X}_{4,ref} \quad (D2-3)$$

$$\tilde{X}_{new1} = A_c \tilde{X}_{new1} + B_c \tilde{U} + D_c \tilde{X}_{4,ref} \quad (D2-4)$$

Where, $D_1 = [D_{11} \quad D_{22}]$

$$D_{11} = [-K^T C']^{-1} [K^T A' + K_{int}^T T_2], \quad D_{22} = [-K^T C']^{-1} [K_{int}^T T_1], \quad D_2 = [-K^T C']^{-1} [K^T B'],$$

$$D_3 = [-K^T C']^{-1} [K_{ext}^T], \quad A_c = \begin{bmatrix} A' + C'D_{11} & C'D_{22} \\ -T_2 & T_1 \end{bmatrix}, \quad B_c = \begin{bmatrix} B' + C'D_2 \\ 0 \end{bmatrix}, \quad D_c = \begin{bmatrix} C'D_3 \\ 0 \end{bmatrix}$$

Now taking into constraint (6-8) (or in general, (6-7)), one state can be eliminated from the system, reducing the system order by one. Therefore, the final small signal model of the sliding-mode controlled system is,

$$\tilde{X}_{new} = A_T \tilde{X}_{new} + B_T \tilde{U} + D_{T1} \tilde{X}_{4,ref} + D_{T2} \tilde{X}_{4,ref} \quad (D2-5)$$

Note that by assuming X_1 is eliminated, X_{new} is given by, $X_{new} = [X_2, X_3, X_4, X_{1,ref}]^T$.

Then, $B_T = B_c(2:5, :)$

$$A_T = A_c(2:5, 2:5) + A_c(2:5, 1) \cdot F_1, \quad D_{T1} = A_c(2:5, 1) \cdot F_2, \quad D_{T2} = D_c(2:5, :).$$

$$F_1 = (-1/k_1) \cdot [K^T(2:4) - K_{int}^T], \quad F_2 = (1/k_1) \cdot K_{ext}^T.$$

(The notation $A(n:m, j:k)$ means the sub matrix obtained from matrix A taking rows from index $n-m$ and columns from index $j-k$. The symbol $:$ alone means all).

The necessary closed loop transfer functions can be obtained by taking the laplace transform of (D2-5).

Appendix E

E1. Roots of a Third Order Polynomial

Assume a third order polynomial given by,

$$s^3 + a_2 s^2 + a_1 s + a_0 = 0 \quad (E1-1)$$

If the roots of the polynomial are given by α_1 , α_2 and α_3 , then

$$(s - \alpha_1)(s - \alpha_2)(s - \alpha_3) = 0 \quad (\text{E1-2})$$

Therefore, by comparison,

$$\alpha_1 + \alpha_2 + \alpha_3 = -a_2 \quad (\text{E1-3})$$

$$\alpha_1\alpha_2 + \alpha_1\alpha_3 + \alpha_2\alpha_3 = a_1 \quad (\text{E1-4})$$

$$\alpha_1\alpha_2\alpha_3 = -a_0 \quad (\text{E1-5})$$

Note that if all a_2 , a_1 and a_0 are positive, then the equations in (E1-3) – (E1-5) are satisfied only by negative α_1 , α_2 and α_3 . This means all the roots of (E1-1) should have negative real parts.

On the other hand, if $\alpha_1, \alpha_3 > 0$, $\alpha_2 < 0$ and $|\alpha_1| < |\alpha_2| < |\alpha_3|$, from (E1-4) it is seen that a_1 and a_2 should be always negative and a_0 should be always positive. However if a_2 is positive while signs of a_1 and a_0 remains as above, it indicates that the negative root, i.e. α_2 , has the highest magnitude.

In summary, if $a_1 < 0$ and $a_0 > 0$, then it can be concluded that the negative root of the polynomial has the medium or the highest magnitude of the three roots, regardless of the sign of a_2 .

E2. Roots of a Fourth Order Polynomial

Similarly a fourth order polynomial given by $s^4 + b_3s^3 + b_2s^2 + b_1s + b_0 = 0$ and having the roots given by β_1 , β_2 , β_3 and β_4 has the following relationships.

$$\beta_1 + \beta_2 + \beta_3 + \beta_4 = -b_3 \quad (\text{E2-1})$$

$$\beta_1\beta_2 + \beta_1\beta_3 + \beta_1\beta_4 + \beta_2\beta_3 + \beta_2\beta_4 + \beta_3\beta_4 = b_2 \quad (\text{E2-2})$$

$$\beta_1\beta_2\beta_3 + \beta_2\beta_3\beta_4 + \beta_1\beta_2\beta_4 + \beta_1\beta_3\beta_4 = -b_1 \quad (\text{E2-3})$$

$$\beta_1\beta_2\beta_3\beta_4 = b_0 \quad (\text{E2-4})$$

Note that if all b_3 , b_2 , b_1 and b_0 are positive, then the equations in (E2-1) – (E2-4) are satisfied only by negative β_1 , β_2 , β_3 and β_4 . This means all the roots of the fourth order polynomial should have negative real parts.

E3. Approximate Roots of an Arbitrary Degree Polynomial

Assume an arbitrary degree polynomial $P(s)$,

$$P(s) = 1 + \lambda_1 s + \lambda_2 s^2 + \dots + \lambda_n s^n \quad (\text{E3-1})$$

Also assume that it can be factorized as given in (E3-2) below.

$$P(s) = (1 + \tau_1 s)(1 + \tau_2 s) \dots (1 + \tau_n s) \quad (\text{E3-2})$$

If all time constants (τ_i , $i = 1 \dots n$) are real and well separated in value, i.e.

$|\tau_1| \gg |\tau_2| \gg \dots \gg |\tau_n|$, then [8],

$$\tau_1 \cong \lambda_1, \tau_2 \cong (\lambda_2 / \lambda_1), \dots, \tau_n \cong (\lambda_n / \lambda_{n-1}) \quad (\text{E3-3})$$

Therefore, if $|\lambda_1| \gg |(\lambda_2 / \lambda_1)| \gg |(\lambda_3 / \lambda_2)| \gg \dots \gg |(\lambda_n / \lambda_{n-1})|$, then,

$$P(s) = (1 + \lambda_1 s)(1 + (\lambda_2 / \lambda_1)s) \dots (1 + (\lambda_n / \lambda_{n-1})s) \quad (\text{E3-4})$$

Note that if the k^{th} root (or k^{th} time constant) is not well separated in value, i.e.

$|\tau_1| \gg |\tau_2| \gg \dots \gg |\tau_k| \cong |\tau_{k+1}| \gg \dots \gg |\tau_n|$, then

$$P(s) = (1 + \lambda_1 s)(1 + (\lambda_2 / \lambda_1)s) \dots (1 + (\lambda_k / \lambda_{k-1})s + (\lambda_{k+1} / \lambda_{k-1})s^2) \dots (1 + (\lambda_n / \lambda_{n-1})s) \quad (\text{E3-5})$$

Equation (E3-5) holds even for complex conjugate pairs of τ_k and τ_{k+1} .

Therefore, if a polynomial contains a root that is very small compared to all the other roots of the polynomial, then it may be estimated by $-1 / \lambda_1$.

E4. Estimating Approximate Positions of P_{1u} and Z_{1u} for the Case with an RL Load

From the denominator of (A3-15) and the clarification in appendix E3, the pole with the smallest magnitude, i.e. P_{1u} , may be estimated as,

$$P_{1u} \cong \frac{-(R_S + R_L)}{R_S R_L ((1 - d_0)^2 C_{uc} + C_f) + R_i C_{uc} (R_S + R_L) + L_L + L_S} \quad (\text{E4-1})$$

Since C_f , L_L and L_S represent very small values and also since R_L is much larger than R_i or R_S , (E4-1) may be further simplified to,

$$P_{1u} \cong \frac{-(1 + (R_S / R_L))}{R_S ((1 - d_0)^2 C_{uc}) + R_i C_{uc} (1 + (R_S / R_L))} \cong \frac{-1}{R_S ((1 - d_0)^2 C_{uc}) + R_i C_{uc}} \quad (\text{E4-2})$$

Similarly, from the numerator of (A3-15) and the descriptions in appendix E3, the RHP zero with the smallest magnitude, i.e. Z_{1u} , may be estimated as,

$$Z_{1u} \cong \frac{\bar{X}_2}{C_{uc} (\bar{X}_3 (1 - d_0) - R_i \bar{X}_2)} \quad (\text{E4-3})$$

Using (A3-12) and (A3-13), this can be further simplified to,

$$Z_{1u} \cong \frac{\bar{X}_2}{C_{uc} (\bar{X}_3 (1 - d_0) - R_i \bar{X}_2)} \quad (\text{E4-4})$$

Since $R_L \gg R_S, R_i$, it can therefore be seen that $|P_{1u}| \gg |Z_{1u}|$.

However, as discussed in chapter 5, all the other poles and zeros of the system have much larger magnitudes than P_{1u} and Z_{1u} .

From (E4-2) and (E4-4) it can be seen that P_{1u} mainly depends on R_S, R_i and C_{uc} while Z_{1u} depends mainly on R_L, R_i and C_{uc} .

E5. Estimating Approximate Positions of P_{1u} and Z_{1u} for the Case with an Constant Current source Load

From (A3-7) and the clarification given in appendix E3, the pole with the smallest magnitude, i.e. P_{1u} , may be estimated as,

$$P_{1u} \cong \frac{-1}{R_S(1-d_0)^2 C_{uc} + R_i C_{uc} + C_f R_S} \quad (\text{E5-1})$$

Since C_f represent a very small value, (E5-1) may be further simplified to,

$$P_{1u} \cong \frac{-1}{R_S((1-d_0)^2 C_{uc}) + R_i C_{uc}} \quad (\text{E5-2})$$

Similarly, from the numerator of (A3-5) and the descriptions in appendix E3, the RHP zero with the smallest magnitude, i.e. Z_{1u} , may be estimated as,

$$Z_{1u} \cong \frac{\bar{X}_2}{C_{uc}(\bar{X}_3(1-d_0) - R_i \bar{X}_2)} \quad (\text{E5-3})$$

Using (A3-2) and (A3-3), this can be further simplified to,

$$Z_{1u} \cong \frac{\bar{X}_1 - (1-d_0)(E_S - IR_S)}{C_{uc}((\bar{X}_1 R_S(1-d_0)^2 - R_i \bar{X}_1) + 2R_i(1-d_0)(E_S - IR_S))} \quad (\text{E5-4})$$

$$Z_{1u} \cong \frac{1 - \frac{(1-d_0)(E_S - IR_S)}{\bar{X}_1}}{C_{uc}\left((R_S(1-d_0)^2 - R_i) + \frac{2R_i(1-d_0)(E_S - IR_S)}{\bar{X}_1}\right)} \quad (\text{E5-5})$$

Note that $(E_S - IR_S)$, represents a value very close to $\bar{V}_{DC}$ and $(1-d_0)(E_S - IR_S)$ approximately represents a value very close to (but less than) $\bar{X}_1$.

Therefore, $1 - \frac{(1-d_0)(E_S - IR_S)}{\bar{X}_1} \cong 0$.

Therefore, by comparing (E5-2) and (E5-5), it can be seen that $|P_{1u}| \gg |Z_{1u}|$.

However, as discussed in chapter 5, all the other poles and zeros of the system have much larger magnitudes than P_{1u} and Z_{1u} .

Both P_{1u} and Z_{1u} are seen to be mainly dependant on R_s, R_i and C_{uc} . Z_{1u} is also seen to be dependant slightly on E_s, R_s, I and $\bar{X}_1$.

Appendix F

As per the basic root locus theory, the locus of closed loop poles of a feedback system, i.e. root locus, start from the open loop poles and ends at the open loop zeros or at infinity. This directly shows that if a system has a RHP zero in open loop, then a section of the root locus of that system should lie in the RHP. This means the system should become unstable under certain conditions or once a certain limit is exceeded. The gain cross over frequency inequality, derived in [67], gives a formal relationship for this design limit.

Gain Crossover Frequency inequality for non minimum phase systems with one open loop RHP zero:

i) Bode's ideal loop transfer function:

Bode proposed that the ideal shape of the loop transfer function ($L(s)$), should have the form [67],

$$L(s) = \left(\frac{s}{\omega_{gc}} \right)^n \quad (F-1)$$

Where, s is the laplace variable, ω_{gc} is the gain cross over frequency and n is a negative real number.

The loop transfer function given in (F-1) always has a phase margin of $\varphi_m = \pi(1 + n/2)$ for all values of gain. Therefore, although the changes in the gain of $L(s)$ change the cross over frequency, the phase margin of the closed loop system remains unaffected.

Bode also showed that that it was sufficient to approximate $L(s)$ over a frequency range around the desired cross over frequency ω_{gc} [67].

ii) Derivation of stability limit

Consider a non minimum phase system, $P(s)$, with one RHP zero at z . Also assume that $P(s)$ can be factorized into its minimum phase part ($P_{mp}(s)$) and non minimum phase part ($P_{nmp}(s)$), i.e.

$$P(s) = P_{mp}(s) \cdot P_{nmp}(s) \quad (F-2)$$

Where, $P_{nmp}(s)$ is selected so that $|P_{nmp}(s)| = 1$ and it satisfies the requirement of encirclements by the nyquist stability criterion [67].

Since, $P(s)$ has only one RHP zero in this case, $P_{nmp}(s) = \frac{z-s}{z+s}$ (F-3)

Assume that the controller that is used to control $P(s)$ is $C(s)$, and $C(s)$ does not contain any non minimum phase zeros or poles. Therefore, if the loop transfer function $L(s) = P(s)C(s)$ is stable and it has a phase margin φ_m at the cross over frequency ω_{gc} , then,

$$\angle L(j\omega_{gc}) = \angle P_{nmp}(j\omega_{gc}) + \angle P_{mp}(j\omega_{gc}) + \angle C(j\omega_{gc}) \geq -\pi + \varphi_m \quad (F-4)$$

Assuming that the controller $C(s)$ is selected so that $P_{mp}(s)C(s)$ is equal to the Bode's ideal loop transfer function given in (F-1) at the cross over frequency, then

$$\angle P_{mp}(j\omega_{gc}) + \angle C(j\omega_{gc}) = n_{gc} \frac{\pi}{2} \quad (F-5)$$

(Note that the n around the cross over frequency is denoted as n_{gc})

From (F-4) and (F-5) it can therefore be seen that,

$$\angle P_{nmp}(j\omega_{gc}) \geq -\pi + \varphi_m - n_{gc} \frac{\pi}{2} \quad (F-6)$$

From (F-3), $\angle P_{nmp}(j\omega_{gc}) = -2 \tan^{-1}(\frac{\omega_{gc}}{z})$ (F-7)

Therefore, if $\alpha = -\frac{\pi}{2} + \frac{\varphi_m}{2} - n_{gc} \frac{\pi}{4}$, then from (F-6) and (F-7),

$$\omega_{gc} \leq z \tan \alpha \tag{F-8}$$