A monolithic capacitive transducer for electrical capacitance tomography

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A Monolithic Capacitive Transducer for Electrical Capacitance Tomography

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2010

STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

26 July 2010
Date

Cui Jie
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ABSTRACT

This thesis presents a new high-resolution, fully-integrated monolithic capacitive transducer for portable electrical capacitance tomography (ECT) applications. This mixed-signal chip comprises a new switched-capacitor (SC) capacitance-to-voltage (CV) convertor with a stray immunity, a new offset-reduced chopping differential difference amplifier (DDA) for post amplification and a digital control module for generating a series of control clocks. The CV convertor, being a critical building block, adopts correlated double sampling (CDS) to minimize the $1/f$ noise and cancel the dc offset arising from the dedicated op-amp having a high power-bandwidth efficiency. Moreover, it realizes a new instrumentation-based methodology through additional auto-zero (AZ) operations to sample and cancel the front-end circuit level switch errors. A detailed analysis is conducted on the proposed switched-capacitor interface as well as for the conventional chopping amplifier with respect to the imperfections. Analytical modeling of the imperfections on the chopping amplifiers is then presented. A new resistance balancing technique is proposed for the further reduction of dc offsets in chopping amplifiers. With a high resolution design objective, design-for-test methodologies are also proposed. These include the parasitic balancing technique and the charge lever mechanism. The simulation and measurement results validate the proposed methodologies and new circuits. Several figures-of-merit are devised for a fair comparison with the reported prior art works. The experimental results show that the chip is able to sense the range of capacitance from 0.26fF to 2pF at a heavy parasitic capacitance of 150 pF, leading to a dynamic range of 77.8 dB at a single 3V while consuming a total of 4.5 mW. No apparent dc offset was observed. Compared with the reported works, the IC prototype offers significant technical merits in terms of monolithic integration, a reduced power supply, low-power consumption, high resolution and a high dynamic range, thus demonstrating advanced state-of-art performance.

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CHAPTER 1

1 INTRODUCTION

1.1 Motivations

With the advanced pace of the development of integrated circuits (IC) and microsystem technology, the use of on-silicon precision sensor applications has expanded towards multiple new transducer applications. A large variety of on-silicon sensors have been created, and capacitance-voltage (CV) transducers have become important in many situations in which capacitance variation are converted into voltage electrical signals measurable and controllable by electric instruments directly.

One of these applications is electrical capacitance tomography (ECT). Tomography is a technology that allows for real-time cross-sectional images of the distribution of materials without invasion and direct contact. Within the last twenty years, ECT systems have drawn much attention for their advancing industrial and medical applications. ECT systems are attractive because they are highly sensitive, demonstrate low drift with changes in temperature and time, have low static offset and electrical drift, display high integrity, are low in cost, and their mechanical structure is both simple and compatible with backend signal processing. These characteristics are very important when the systems are applied in an industrial environment. ECT systems are capable of visualizing mixed contents inside a container to the level of a few hundred frames per second, and stably display femto farad order resolutions. These characteristics make ECT systems popular and raise the general demand for even higher image resolutions at lower costs.

The ECT system can be said to consist of two parts, the front end and the back end. As the back-end digital signal processor works to convert collected signals into real-time images, the front end capacitive transducer critically controls and shapes the characteristics of the whole system. Such a fully-integrated capacitive transducer makes the ECT system portable and suitable for external environments. The complementary requirements for the design of a qualified ECT capacitive transducer sensor chip are as follows:

- 1) Low baseline drift
- 2) Strong environmental immunity, such as stray capacitance immunity, low drift and insensitive to temperature fluctuation
- 3) Low power consumption and portable
- 4) Fast data acquisition speed
- 5) Wide dynamic range of measurement
- 6) High sensitivity and precision
- 7) Extendable for portable applications

There are two main types of ECT system, the switched-capacitor (SC) ECT and the AC based ECT. The SC based ECT deals with the sample-data technique. Although it is successfully built using a real-time ECT system with a capacitor charging-discharging circuit, it works with circuit and system techniques to counteract the presence of heavy parasitic capacitances, non-ideal switch error effects, potentially large baseline offset, drift over time and temperature. This is a promising approach since the foundation switched-capacitor technique has the intrinsic advantage of cancelling low-frequency noise and offset, which benefits the circuit baseline stability. The second method employs a continuous-time technique that has high dependence on the linearity, accuracy and offset of the analog processing circuits such as the rectifier and multiplier. However, such a front-end design requires that transducer circuits have low-noise and low-drift, which presents a great design challenge to transducers using CMOS technology for both signal conversion and

signal processing tasks. On the one hand, such a technique eliminates the switch error. On the other hand, its power-noise performance may not compare well with its switched-capacitor counterpart because it needs very low-noise low-offset front-end components. Nonetheless, the main advantage of the switched-capacitor based ECT system is the simplicity of the transducer's electronics which enables easy integration.

This study aims to develop a switched-capacitor based transducer design for ECT systems as it is thought that such a design offers significant potential as a high-performance, low-cost solution for sensory systems using popular CMOS technology. Given the general trend toward portable, integrated systems rather than circuits with discrete components, an integrated design is desirable. However, such an integrated transducer design presents two main challenges. One is the requirement of strong immunity over heavy parasitic levels, while the other is the low noise requirement arising from the fact that noise will limit the minimum detectable capacitance of the transducer. The discrete component CV convertor typically uses a much higher power supply (± 15 V or ± 18 V) than CMOS integrated circuits which usually use between 5 or 3V. However, at lower power levels, CMOS integrated circuits are prone to higher noise levels than discrete component circuits because of their low-frequency flicker noise component. Thus, another aim of this paper is to design a high-resolution transducer that will allow for a high-performance low-cost solution ECT system that makes use of popular CMOS technology.

1.2 Objectives

The objective of this thesis is to investigate circuit techniques for the design of a new highly-sensitive capacitance-to-voltage transducer, taking into account the heavy parasitic capacitances of electrical capacitance tomography applications, and to realize a low-cost integrated circuit prototype. The scope of the research project is as

follows:

1. To use a modeling approach to analyze and study the effect of imperfections such as non-ideal chopper switches, switch errors, non-ideal op-amps, and parasitic capacitances in precision analog design environments. This will facilitate the design of a larger mixed-signal transducer system and improve the precision of its sensory circuits and systems.
2. To investigate novel circuit techniques and a new circuit topology that can counteract the error arising from a switched-capacitor circuit and thus permit the realization of a high quality capacitive transducer that has a wide capacitance detection dynamic range, a high image capturing speed, low temperature drift, and most importantly, lower power demands to reduce consumption and allow for portable applications.
3. To support a design-for-test strategy and provide an on-chip testing circuit design which permits easy verification of the functionality of the fabricated mixed-signal chips. This is to benefit the manufacturing test environment and reduce the overall cost of testing.

1.3 Major Contributions of the Thesis

The major contributions of this research work are summarized as follows:

1. The major non-ideal effects that occur in the precision analog environment will be thoroughly studied. These include imperfect chopper switches, switch errors, non-idealities in the op-amps and parasitic capacitances. Modeling approaches appropriate for each individual non-ideal effect will be investigated and included in the detailed analysis of a conventional chopper-stabilized amplifier. Taking into

account the dominant non-perfection factors impacting the amplifier design, a new chopper-stabilized amplifier with reduced offset will be proposed from results of the foundational study and fundamental analysis. Experimental results will demonstrate the reduction in dc offset by applying the methodology in the fabricated chopper-stabilized amplifier chips. This new offset reduction technique is a useful addition to the new switched-capacitor ECT transducer design.

2. A low-cost, high-performance ECT transducer chip will be designed which comprises a new front-end sample-data transducer circuit and a back-end continuous-time scaling amplifier for signal-conditioning. The switched-capacitor transducer will further incorporate dual offset reduction strategies. The first strategy involves instrumentation based offset reduction for the front-end transducer architecture, while the second strategy makes use of the proposed offset reduction from the foundation study to further minimize the offset arising from imperfections in the chopper-stabilized scaling amplifier. In combination, a ECT chip with low baseline drift will be realized for a favorable ECT system. The ECT transducer chip will be designed using the Cadence software suite, and realized using TSMC 0.25 μ m CMOS process technology. It will be validated by the chip measurements. The ECT transducer chip will show significant improvement results over previously reported results, with the following key performance metrics:

- Measurement range 0.26 fF $\sim$ 2 pF
- Data acquisition speed of 300 μ S
- Immunity of parasitic capacitance up to 150 pF
- Power consumption of 4.5 mW at a single 3V supply

3. A “design-for-test” circuit topology has been proposed for practical test and measurement conditions. The methodology provides a thorough understanding of the integrated circuit design process from design and layout to packaging and

measurement.

1.4 Organization of the Thesis

Subsequent chapters are organized as follows:

Chapter 2 presents a review of tomography system. It begins with a history of tomography in general before looking at electrical capacitance tomography (ECT) in particular. The applications of ECT will be reviewed along with current research concerns. The chapter further compares prior-art tomography system architectures with different implementations.

Chapter 3 reviews the circuit design methods employed to build high quality blocks for precise and stable transducers. These include Auto-zero (AZ), Correlated Double Sampling (CDS) and Chopper Stabilization (CHS). This review is followed by a further examination of the literature pertaining to three major switched-capacitor based capacitance measuring circuits. These circuits were developed in the University of Manchester Institute of Science and Technology (UMIST), Zhejiang University and Nanyang Technological University (NTU). Other continuous-time AC-based capacitance measuring circuits will also be discussed before we conclude our general classification of transducers.

Chapter 4 proposes the methodology for incorporating AZ or CDS techniques in an alternative circuit that suppresses switch errors, $1/f$ noise and offsets of the op-amp. The switched-capacitor design technique has the key advantage of stray immunity, therefore, these efforts pertain to the front-end switched-capacitor transducer. The second electronic part of the transducer adopts a chopper stabilization technique which has the advantage of not producing any folded back noise and is thus suitable

for signal-processing in a low parasitic environment. An analysis of the imperfections of a chopper-stabilized op-amp is provided in Chapter 2. A new resistance balancing method is then proposed to further reduce the dc offset in conventional chopper-stabilized amplifier topologies. Illustrative examples are given on how to apply the new offset reduction method to the chopping op-amp and chopping DDA.

Chapter 5 describes the proposed ECT tomography system architecture. This is then followed by a demonstration of the instrumentation methodology involved in the design of a precision switched-capacitor sample-and-hold circuit. Again, the methodology incorporating AZ and CDS technique is extended to the foundation switched-capacitor transducer comprising a switched-capacitor front-end interface and a differential difference amplifier (DDA) which serves as the back-end signal-conditioning circuit. Circuit improvements resulting from the inclusion of the foundation transducer are presented in detail. These involve (i) additional switched-capacitor input circuitries that deal with practical capacitance measurement issues, (ii) instrumentation based front-end SC transducers that incorporate feedback architecture to improve circuit stability as well as reduce the error and noise arising from the sample-and-hold circuits, (iii) the replacement of the DDA by chopper-stabilized DDA to achieve low-noise and precise back-end signal processing stages and (iv) the introduction of test methodology on the basis of a parasitic balancing and charge lever mechanism that facilitates the testing of the switched-capacitor transducer when dealing with very small sensing capacitance values.

Chapter 6 describes the digital logic design dedicated to the transducer, such as non-overlapping clock phase generator, digital controlled signal generator, basic circuits and so on.

Chapter 7 discusses the mixed-signal layout issues of the transducer system. Layout techniques pertaining to low noise shielding and matching are presented. The system

floor plan and I/O pad layout are provided on a standard DIL 28 package.

Chapter 8 presents the results of the simulation and experimental validation of the proposed methodologies, including the outcome of the new circuit elements, specifically the S/H circuits, the chopper-stabilized DDA and the switched-capacitor capacitive transducer. This new design will be compared to prior-art transducers that were earlier discussed.

Chapter 9 gives a summary of the research work as well as recommendations for future work.

CHAPTER 2

2 ELECTRICAL CAPACITANCE TOMOGRAPHY

2.1 ECT Systems and Their Applications

Electrical capacitance tomography (ECT) came into being in the late 1980's. ECT is used to visualize the internal behavior of industrial processes that use dielectric components. ECT is especially useful for obtaining information about the distribution of the contents of closed pipes or vessels. It does this by non-invasively and non-intrusively measuring the variations in the dielectric properties of the materials inside the vessel. After many years of research in university laboratories, ECT systems have recently begun to be used in real-life industrial environments.

ECT can be used in two different domains. The first domain it can be used in, which is also the one where its use is the most mature, is industrial application [Z. Y. Huang, 2003]. Besides this domain, ECT can also be used in the construction of medical images. Recently, there has been considerable success in this area with, for example, tumor identification [A. Kimoto, 2005]. Ordinarily, the excitation frequency of ECT is considered to be a "low" frequency, up to about 1MHz [T. York, 2001]. Therefore, the speed at which images are constructed in for industry applications is around a hundred frames per second. ECT can also be used to detect four kinds of non-conducting materials. They are solids [D. Sankowski, 2005], liquids [W. Q. Yang, 1996], gases [R. He, 1994], and mixtures of any two kinds of dielectric materials [D. L. Xie, 2004]. This is because the permittivity distribution corresponds to the concentration of

materials [P. M. Williams, 1998].

ECT is used in various industries, such as petrochemicals, food processing, plastic production, and chemical engineering. Amongst the various modes of image reconstruction tomography, ECT was the first to be developed. It offers many advantages over its counterparts, such as Electrical Resistance Tomography (ERT), Electromagnetic Tomography (EMT), and Electrical Impedance Tomography (EIT). It is low-cost with a straightforward processing system, interface, circuit, controller and sensor electrodes. It has a high response speed and does not emit any radiation. ECT systems can deliver reconstructions of cross-sectional images at 100 frames per second, which is a very attractive speed for online control applications. In the future, portable ECT systems will be developed which will be robust in different environments. Its current properties make it adequate for most industry applications.

TABLE 2.1.1 SUMMARY OF REPORTED ELECTRICAL CAPACITANCE TOMOGRAPHY SYSTEMS

Reference	Characteristics
S. M. Huang [1988]	Charge transfer device and the switched guard method, 8 electrodes, 200 frames/second
G. E. Fasching [1991]	400 kHz sinusoidal excitation at up to 250V, 4 planes for 16 electrodes, 30 frames/second
G. A. Johansen [1996]	Radio arm bridge, gamma ray system is conjunctly used, 8 electrodes, 5 frames/second
W. Q. Yang [1997]	Commercialized, charge-discharge circuit, 1 MHz, 12 electrodes
W. K. Harteveltd [1999]	New fast active differentiator circuit, promising high data rates
R. Deloughry [1999]	Driven guard, modified ac bridge, 100 kHz DDS sinusoidal source, hardware conditioning, 12 electrodes, 1.9 V/pF
Z. Y. Huang [2003]	Hybrid image reconstruction algorithm, 12 electrodes, 150 frames/second, 1.0fF resolution
D. L. Xie [2004]	Switched-capacitor circuit, 12 electrodes, 600 frames/second

As mentioned earlier, a CV transducer forms the core of the front-end data collection

for an ECT system. A comparison of CV transducers used in ECT systems is shown in Table. 2.1.2. The Table indicates that the development trajectory of transducers has followed a path of increasing sensitivity and finer resolution. This may be accomplished by miniaturizing ECT systems. The increase in speed obtained by significantly reducing the external heavy parasitic capacitances contributes to a high noise gain factor in the typical transducer circuit. Another trend in the development of ECT systems is the use of integrated, rather than discrete, circuits. At the same time, the supply voltage is significantly reduced because of the use of low-supply CMOS ICs technology. This greatly limits the dynamic range of transducers. In addition, the noise problem associated with CMOS technology becomes a major concern.

TABLE 2.1.2. DETAILED SUMMARY OF REPRESENTATIVE CV TRANSDUCER

Parameter	W. Q. Wang [1999]	D. L. Xie [2004,2006]	S. M. Huang/ X. H. Hu [1992]/[2007]	T.N. Phua [2008]
Type of Transducer	AC-based	Differential sampling	Charge and discharge	Switched-Current Super Current Mirror IV Conversion
Component	Discrete	Discrete	Discrete	IC
Electrode no.	12	12	12	8
Cf	10 pF	NA	4.7 nF	NA
Rf	—	—	15 kΩ	—
Cs	150 pF	NA	150 pF	1.2 pF
Power supply	+/-15 V	+/- 18 V	+/- 15 V	3 V
Cxmin(pk)	10 fF	0.5 fF	0.3 fF	0.91 fF
Sensitivity	2.0 V/pF	4.8 V/pF	0.5V/pF	40 V/pF
Speed	100 f/s	600 f/s	100 f/s	6250 f/s

The circuit techniques used should take these limitations into account. Although the switched-current approach aims to reduce power consumption, the high noise content

arising from the finite gm of weak inversion transistors counteracts any improvements in resolution. More importantly, the wide variation in the process parameters of weak-inversion based switched-current circuits can lead to a significant reduction in the performance of the integrated electrode electronics. This design trade-off is directly linked to the yield of micropower integrated circuits. There is, therefore, the need for a new type of robust capacitive transducer that can provide a fully-integrated solution with high resolutions in reduced supply conditions.

2.2 ECT System Working Principles

Capacitive tomography is defined as the detection, sensing, or imaging of physical structures by the detection and analysis of variations or perturbations in electric field parameters. These changes in electric field parameters result from changes in the relative electrical permittivity of the physical structures that reside in the physical space that is being sensed. Every mixture corresponds to a certain dielectric constant. The mixture used herewith is a dielectric material of unknown capacitance. The capacitance value [L. K. Baxter, 1997] will vary with the variation of the mixture component. Governed by physical parameters, it is expressed as

$$C = \frac{\epsilon_0 \times \epsilon_r \times s}{d} \quad (2.2.1)$$

where, C= capacitance in farads,

$\epsilon_0 = 8.854 \times 10^{-12}$ farad/meter, dielectric constant for vacuum,

ϵ_r = relative dielectric constant, 1 for vacuum,

s = area in square meter,

d = spacing in meter

When the first ECT system was successfully demonstrated [S. M. Huang, 1988], the generic architecture suggested that a basic capacitance-based ECT system was subdivided into three parts. These are: (i) the primary sensor (the capacitive

transducer), (ii) the capacitance measuring unit (the digital controller), and (iii) an image reconstruction computer as shown in Fig. 2.1.1. The sensor primarily detects the change of capacitance C_x . The associated electronic sensor aims to transform the detected capacitance value into a corresponding voltage value, while the image reconstruction computer uses the large amount of data that is captured to reconstruct an image of the mixture inside the vessel.

In early work in this field, ECT sensors consisted of a certain number of electrodes, typically 8 [S. M. Huang, 1988] or 12 [R. A. Williams, 1995], that surrounded the cross-section of the vessel or pipe being investigated. The functions of the capacitive transducer and the digital controller include the selection of electrode-pair combinations, the measurement of capacitances between all possible combination pairs of electrodes (and by doing so, interrogating different areas in the sensing volume), the conversion of the measured capacitance values into digital signals, and acting as an interface between the data acquisition component and the image reconstruction computer.

Fig. 2.2 Electrical capacitance tomography system

The digital controllers that process the sampled data and construct cross-sectional images in the computer screen are another critical part of the system. The full permittivity distribution requires some signal sampling channels, such as 8 or 12 electrodes. The different capacitance values between each two-electrode pair need to be collected and stored for processing. Consider an example of an 8-electrode ECT

system. The electrodes are numbered from 1 to 8. The measurement protocol in the sensors first measures the capacitance between the electrode pair 1 and 2, then between pair 1 and 3, and until pair 1 and n , where n equals to 8 here. The sensor next continues measuring the capacitance between electrodes 2 and 3, $\dots$, until pair 2 and n . The sampling procedure is repeated until it reaches pair $(n-1)$ and n , and when all inter-electrode capacitance values have been measured. These capacitance values can be expressed in a matrix format as follows:

$$\begin{bmatrix} C_{12} & C_{13} & \cdots & C_{1,n-1} & C_{1,n} \\ C_{23} & C_{24} & \cdots & C_{2,n} & \\ \vdots & \vdots & \vdots & & \\ C_{n-2,n-1} & C_{n-2,n} & & & \\ C_{n-1,n} & & & & \end{bmatrix} \quad (2.2.2)$$

It is symmetric with respect to the diagonal since $C_{ij} = C_{ji}$, $i, j \in [1, n]$. With n electrodes, one can obtain a universal equation for total independent capacitance measurements M .

$$M = \frac{n(n-1)}{2} \quad (2.2.3)$$

For an 8-electrode system it gives a total of 28 capacitance values in total. Since the capacitance value C_{ij} is singly dependent on the permittivity distribution ϵ inside the measured pipeline, the permittivity can be expressed with inversing relationship as follows:

$$\epsilon(x, y) = f^{-1}(C_{12}, C_{13}, \dots, C_{ij}, \dots, C_{n-1,n}) \quad (2.2.4)$$

Based on (2.2.4), the permittivity distribution can theoretically be obtained under any circumstances. Unfortunately, a close-form analytical and unique expression for (2.2.4)

can not be found all the time. This is mainly because the relationship between the capacitance and the distribution of the dielectric constant is nonlinear and ill-posed inverse. It is thus impossible to establish an explicit expression. Researchers have been applying approximate numerical techniques to find the approximate solution in (2.2.4) for a given set of capacitance measurement values. Much effort has been committed to the reconstruction algorithm, and many mathematical approaches have been proposed for high-precision image reconstruction.

Among these approaches, the dominant method today is the linear back projection (LBP) [Ø. Isaksen, 1996]. The LBP technique adapts a simple matrix multiplication, such as the procedure of converting (2.2.2) to (2.2.4). It needs comparatively less mathematical effort and an essentially representative distribution of materials can be obtained with low spatial resolution. While the resolution is adequate for most industry applications, its advantage is its high speed, which makes it possible to obtain “real-time” visualization. Although techniques based on linear approximations are fast, they are not adequate for all applications. Other mathematical algorithms mostly deal with different kinds of iterative regularization methods, such as singular value decomposition, Tikhonov regularization, Newton-Raphson, the regularized Gauss-Newton scheme [M. Soleimani, 2005], the Levenburg-Marquard method, iterative Tikhonov, the steepest descent method, Landweber iteration, the conjugate gradient method, algebraic reconstruction techniques, simultaneous iterative reconstruction techniques, total-variation image reconstruction [W. F. Fang, 2004] and model-based reconstruction. While iterative approaches typically provide more accurate images, the process is time-consuming and there might be convergence problems. There is always a trade-off between these two types of image reconstruction methods. The algorithms are reported in the review papers [N. Reinecke, 1996] [W. Q. Yang, 2003].

Apart from effective algorithms and high-speed back-end signal-processing unit, a high quality ECT system indeed requires a quality front-end transducer. This ensures

not to deteriorate the analog performance during a process of detection of minute capacitance change whilst without influencing by other critical non-ideal effects arising from imperfection of sensory circuit or system in mixed-signal environment. As a focus, the research, design and implementation of front-end sensor interface circuit (capacitive transducer) becomes the key objectives in this dissertation. The relevant topics will be further discussed from Chapter 3 to Chapter 9.

CHAPTER 3

3 REVIEW OF CAPACITIVE TRANSDUCERS IN TOMOGRAPHY

In this chapter, different circuit techniques applicable to the design of a high quality transducer for ECT applications are reviewed. This is then followed by the review of representative types of transducers in tomography.

3.1 Circuit Techniques for Switched-capacitor Circuit: Auto-zero (AZ) and Correlated Double Sampling (CDS)

Auto-zero and correlated double sampling are usually viewed as circuit techniques for designing precision-awareness in the context of high precision switched-capacitor transducers. They have their own advantages and disadvantages. Understanding their fundamental limitations will help in designing a high-quality transducer.

The versatile applications of op-amps in precision analogue modules makes it very important that the effects of narrow-band low frequency noise sources be eliminated at the virtual ground point of op-amps [C. C. Enz, 1996]. AZ is a sampling method which came into being in the 1970's. Utilizing the sample-and-hold idea, the AZ technique automatically subtracts the sampled errors from the contaminated signal. That is the origin of the name "auto-zero": the technique can sample and zero the errors continuously. The AZ technique is particularly useful for the application of switched-capacitor circuits which have the same underlying sample-and-hold

principle.

Fig. 3.1.1 Basic principle of auto-zero technique

The basic principle of AZ is sampling and subtracting the errors and noise from the contaminated signal at the input, intermediate node, or output of the op-amp. It consists of two working phases, as shown in Fig. 3.1.1: i) the sampling ($\phi 1$) of errors and noise, and ii) the processing of the signals ($\phi 2$) for cancellation and the preparation of offset-free signals for further operation. The precision of the subtraction depends heavily on the time variation of the offset error and the noises. The input-referred offset voltage of op-amps is normally a DC or low-frequency error. The cancellation to this component is comparatively precise. However, noises are different since they are randomly vibrating sources. The correlation between the noise sampled at the first stage and the instantaneous noise value at the second stage has a large impact on the efficiency of the AZ process in reducing low-frequency noise. Compared to white noise, the auto-correlation of a $1/f$ noise decreases at a slower pace with increasing time intervals. The AZ process is thus more efficient for dealing with flicker noise than broadband white noises, such as the thermal noise of components. Using the AZ technique effectively will help design a quality switched-capacitor capacitive transducer. The thesis focuses on this aspect.

Fig. 3.1.2 Frequency characteristic of CDS analog processor with $\tau = T/2$

The CDS technique was originally introduced to reduce the noise produced in charge-coupled devices, and can be viewed as an AZ operation followed by an S/H. The correlated double sampling (CDS) technique is a particular case of the AZ technique where the amplifier noise and offset are sampled twice in each clock period. It is widely used in switched-capacitor circuits. Although the signal at the output of a circuit using CDS is S/H, the effect on the amplifier offset and noise is very similar to that of the AZ process. The baseband transfer function still imposes a zero at the origin of the frequency that cancels any offset and strongly reduces the $1/f$ noise in the same way that the AZ technique does. The foldover component due to aliasing is comparable since the wideband noise has already been sampled once. Fig. 3.1.2 shows the frequency filter characteristic of CDS with $\tau = T/2$ [M. H. White, 1974].

3.2 Switched-Capacitor Transducers

The switched-capacitor circuit is most popular approach for applying the analog signal processing technique in MOS integrated circuits. This circuit was well-known from as early as the 1960s and 1970s, because of its accurate frequency response, good linearity and dynamic range. A switched-capacitor circuit is based on some basic building blocks, such as op-amps, capacitors, switches, and non-overlapping clocks. Switched-capacitor circuits are often used for filtering functions and to realize a variety of signal-processing blocks, such as gain-stages, voltage-controlled oscillators, and modulators, and switched-capacitor transducer, where switched-capacitor circuits are used as gain circuits.

A switched-capacitor transducer is used in many industrial applications, particularly to measure physical quantities, such as humidity, pressure or flow. These are sensed as capacitance values, which are then converted into electrical signals for further

signal processing. Capacitance measurement can also be extended to an electrical capacitance tomography system.

3.2.1 Charge-Discharge Capacitance Measuring Circuit

Sensor electronics topologies that use switched-capacitor transducers as a means of capacitance measurement have been published [S. M. Huang, 1992], [P. M. Williams, 1996, 1998]. Among them, Huang *et al.* were the first to implement an ECT system with the switched-capacitor approach in UMIST. The principle of the basic capacitance measuring circuit can be explained with reference to Fig. 3.2.1.

Fig. 3.2.1 The capacitance measurement circuit proposed by Huang *et.al.* in 1992

One electrode of unknown capacitance (the source electrode) is connected with a pair of MOS switches, S_1 and S_2 , while the other electrode (the detecting electrode) is connected with switches S_3 and S_4 . In a typical operating cycle, switches S_1 and S_3 are first closed (while S_2 and S_4 are open) to charge the unknown capacitance, C_x , to voltage V_c . The charging current flows into the input channel (at virtual earth

potential) of the current detector in the upper circuit (CD1), where it is converted into negative voltage output. In the second half of the cycle, switches S2 and S4 are closed (while S1 and S3 are open) to discharge C_x to earth potential. The discharging current flows out of the current detector in the lower circuit (CD2), producing a positive voltage output. This typical charge/discharge cycle repeats at a frequency, f , and the successive charging and discharging current pulses are averaged in the two current detectors, producing two DC output voltages.

$$V_1 = -f \times V_c \times R_f \times C_x + e_1 \quad (3.2.1)$$

$$V_2 = f \times V_c \times R_f \times C_x + e_2 \quad (3.2.2)$$

where R_f and C_f are the values of the feedback resistors and capacitors of the current detectors, and e_1 and e_2 represent the output offset voltages of CD1 and CD2, which are caused mainly by the charge injection effect of the MOS switches. The offset voltages of the operational amplifiers, A1 and A2, have only some minor contribution of offsets to e_1 and e_2 compared with the charge injection effect. The capacitors C_{in} (0.1 μ F) are added to ensure that the virtual earth potentials at the inputs of CD1 and CD2 remain stable during the high-speed charging and discharging operation. Since, during the operation, the source electrode is always connected with low impedance supplies (V_c and earth), and the detecting electrode is always at virtual earth potential, stray capacitances have virtually no effect on the measurement.

The dynamic characteristics of the current detectors are similar to that of a first-order low-pass filter with a time constant T determined by $R_f C_f$. The time constant is chosen so that the switching frequency f is sufficiently attenuated and the bandwidth of the amplifier noise is limited, while the required data capture speed is satisfied.

The differential output voltage $V_2 - V_1$ is taken as the output signal of the basic circuit. From equations (3.2.1) and (3.2.2), we have

$$V_2 - V_1 = 2 \times f \times V_c \times R_f \times C_x + e_2 - e_1 \quad (3.2.3)$$

Compared with equations (3.2.1) or (3.2.2), equation (3.2.3) shows that the differential structure has gained two advantages. First, the sensitivity of the measurement has doubled to $2fV_cR_f$. Second, the output offset voltages e_1 and e_2 tend to cancel each other out, provided that S3 and S4 have similar charge injection effects and the two operational amplifiers have matched offset voltages (from a dual amplifier package, for instance). Another advantage of this differential structure can be gained when the measurement is applied to fluids carrying electrostatic charges, as in the case of pneumatically-conveyed solids. The electrostatic charges induce a noise current flowing into the detecting electrode and produce noise voltages at the detector outputs. Since the frequency of the noise current is much lower (usually less than 100 Hz) than the switching frequency of the noise current flowing into CD1 and CD2 during two successive switching intervals (charge and discharge) they can be treated as being of equal amplitude. Therefore the two noise voltages cancel each other out in the differential output.

Although the differential structure reduces the output-offset voltage caused by the charge injection effect, some 20 to 30% of this effect still remains. More importantly, the temperature drifts of the charge injection on two different switches cannot match each other very well even when the switches are fabricated on the same IC chip. Considering the minimum resolution as being less than or equal to 1 femto farad, the baseline drift must be corrected by the arrangement described below.

The idea is to check the baseline regularly and correct the drift by subtracting the baseline from the values measured later. To implement this, a baseline-checking mode is incorporated into the circuit operation. In this mode, the source electrode is earthed while switches S3 and S4 remain operational, and the output offset due to the charge injection is measured. Then, the measurement is restarted by enabling the

charge/discharge control signal connecting to S1 and S2, and the offset value obtained in the checking period is subtracted from each measurement value obtained after the check. The time period needed for the checking is short. For a 12-electrode system with 11 measurement channels, the baseline checking operation needs about 1 ms, which is about one-tenth of the time required for capturing a complete set of measurement data. The frequency of the checking can be determined arbitrarily. If performed once per second, approximately 100 frames of imaging data can be obtained between two checking intervals. Considering the length of the measurement mode, the short checking interval will have little influence on the data acquisition process.

In summary, the baseline drift arising from the switch charge injection of the switched-capacitor circuit needs extra periodic calibration time to be cancelled out via digital signal processing. This is the main disadvantage of this solution. A second limitation of the circuit is that the circuit architecture requires a low-offset low-noise op-amp, which may not be suitable for CMOS implementations because of the absence of cancellation techniques. Finally, matching the offsets of the two op-amps is another critical issue. Absolute matching between op-amps is almost impossible in practical fabrication. This disadvantage will introduce random error to the circuit.

3.2.2 Differential Sampling Capacitance Measuring Circuit

A team at the National Laboratory of Industrial Control Technology in Zhejiang University has examined the use of discrete implementations of switched-capacitor capacitance measuring circuits in ECT systems [Z.Y. Huang, 2003] [D.L. Xie, 2004] [B.L. Wang, 2005] [D.L. Xie, 2006]. The simplified circuit as shown in Fig. 3.2.2 is a straightforward signal path consisting of charge-to-voltage conversion, sample-and-hold stage and final differential amplification.

Fig. 3.2.2(a) Discrete switched-capacitor capacitance measuring circuit

Fig. 3.2.2(b) Discrete switched-capacitor capacitance measuring circuit working clock phases

The capacitance measuring circuit operates under the control of working clock phases as shown in Fig. 3.2.2 (b). At the beginning, the charge transfer is stimulated with null input voltage. The charge caused by switch S1 turning off generates a voltage V_L . This pure error voltage is sampled and held by the sample-and-hold O3 to be cancelled later. The voltage of the excitation source V_i changes from high to low at time t_3 . The charge transferred through the capacitance to be measured C_x can be expressed as

$$Q = -\Delta V_i C_x \quad (3.2.2.1)$$

Hence, the output of O1 is

$$V_H = V_L + \frac{Q}{C_f} \quad (3.2.2.2)$$

This voltage value is held by sample-and-hold O2. The differential amplifier O4 subtracts the voltages at two input terminals, and the final output is

$$V_{out} = V_H - V_L = \frac{-\Delta V_i C_x}{C_f} \quad (3.2.2.3)$$

This result is linearly proportional to the measured capacitance C_x . The differential topology largely suppresses the influence of the biasing current and the offset voltages of the op-amps. Since the parasitic capacitors associated with the two panels of C_x are always connected to absolute earth or virtual earth, they have no effect on the measurement of capacitance. Therefore, this capacitance measuring circuit has parasitic immunity.

This switched-capacitor capacitance measuring circuit, which is based on differential sampling methods for ECT, only charges and discharges the measured capacitance once. It has two main advantages over AC-based circuits. One is its high speed. The speed of the system is determined by the time required for setting up the op-amp and S/Hs. The time for setting up the programmable gain amplifier, offset voltage, A/D conversion and data transmission in the back-end take up most of the data acquisition process, instead of capacitance measurement. Furthermore, the circuit's final voltage is proportional to its measured capacitance. However, the circuit has some disadvantages. There is no CDS action in the first stage switched-capacitor circuit. There are no offsets or $1/f$ noise cancellations in the S/H circuits and the same goes for the differential amplifier. Finally, the circuit relies on a good match between the two S/H amplifiers and very low-noise op-amps.

3.2.3 Correlated-Double Sampling Capacitance Measuring Circuit

The sensor interface circuit research team has proposed a transducer incorporating the CDS technique as shown in Fig. 3.2.3 [J. Peng, 2007]. This interface circuit for ECT applications has four phases in its operation which are controlled by non-overlapping clocks: the reset phase, the auto-zero phase, the charge transfer phase and the hold

phase. They are described in the following discussion.

The transducer incorporating the CDS technique is shown in Fig. 3.2.3 (a). The use of CDS takes advantage of the cancellation of dc offsets and $1/f$ noise arising from the CMOS op-amps. This applies especially because the dc offsets tend to drift with time and temperature and the $1/f$ noise reduces the SNR dynamic range of the transducer. Fig. 3.2.3 (a) consists of two capacitance detectors: Capacitance Detector 1 (CD1) and Capacitance Detector 2 (CD2) arranged in a circuit with pseudo-differential architecture. Each capacitance detector comprises one high-speed op-amp, with its positive input tied to the virtual ground and its negative input tied to a CDS switched-capacitor network. To measure C_x , the source electrode is switched in a sequence to sources (V_{ref1} , V_{ref2} and V_Q), respectively. These sources are controlled by three MOS switches $S1$, $S2$, and $SGNDA$, while the detecting electrode is alternatively connected with each op-amp's virtual earth through the switch control signals $SN1$ and $SN2$. Fig. 3.2.3 (b) shows the waveforms of the switch control signals. The front-end sensor consists of four operation phases derived from the non-overlapping biphasic clock signals $\Phi1$ and $\Phi2$, namely the reset phase, the auto-zero phase, the charge transfer phase, and the hold phase. In the reset phase, the op-amp in the detector is configured in a unity-gain configuration while the feedback capacitor is connected to the analog ground. In the auto-zero phase, the op-amp retains the same configuration but both the sensing and feedback capacitors must be switched to analogue ground to sample the op-amp offset. In the charge transfer phase, the sensing capacitance is applied with a reference voltage source (either a ground reference or alternative reference source) whilst the feedback capacitor forms the feedback loop for capacitance-to-voltage conversion. It is noted that the two reference sources are designed to be symmetrical with respect to the analogue ground. When the sensing capacitance is isolated in the final hold phase, the detected voltage will be held by the feedback capacitor.

(a). NTU SC CDS ECT transducer circuit

(b). Clocks of NTU SC CDS ECT transducer circuit

Fig. 3.2.3 NTU SC CDS ECT transducer circuit (a) and its clocks (b)

During phase 1, CD1 resets, and CD2 transfers charges. Switches S1, S6, SN1, SGND, S7 and S8 are open, and switches S2, S4, S5, SN2 and S9 are closed. In this phase, A1 is operated as a unity-gain amplifier, while A2 transfers the charge only since the dc offset of A2 has been stored in the feedback capacitor Cf2 in previous phase 4 and is cancelled in current phase 1. The output voltages of these two op-amps are

$$V_{out1} = V_Q + V_{os1} \quad (3.2.3.1)$$

$$V_{out2} = V_Q + (C_x / C_{f2}) \Delta V_{ref} \quad (3.2.3.2)$$

During phase 2, CD1 is operating auto-zero and CD2 is holding the transferred charge in phase 1. Therefore, the output of A1 and A2 remain the same values as phase 1. Switches S4, S5, SN1, SGND, and S9 are open, and switches S1, S2, S6, SN2, S7 and S8 are closed.

During phase 3, which is the counterpart of phase 1, CD2 is resetting, and CD1 is transferring charges. Switches S1, S6, SN1, SGND, S7 and S8 are closed, and switches S2, S4, S5, SN2 and S9 are open. In this phase, A2 is operated as a unity-gain amplifier, while A1 transfers the charge since the dc offset of A2 has been stored in the feedback capacitor Cf1 in previous phase 2 and is cancelled in current phase 3. Simultaneously, the output voltages of these two op-amps are,

$$V_{out2} = V_Q + V_{os2} \quad (3.2.3.3)$$

$$V_{out1} = V_Q - (C_x / C_{f1}) \Delta V_{ref} \quad (3.2.3.4)$$

Phase 4 is the counterpart of phase 2 exactly. During this phase, CD1 is holding the voltage of phase 3, and CD2 is operating auto-zero. Switches S6, SGND, SN2, S7 and S8 are open, and S1, S2, S4, S5, SN1 and S9 are closed. Quite similar with the phase 2 operations, the outputs of A1 and A2 keep the same values as phase 3. They follow the values of (3.2.3.3) and (3.2.3.4).

The proposed SC CDS ECT transducer shows a highly suppressed baseline dc offset, a low operation temperature coefficient, and a detection range from 1 fF to 2 pF. Due

to the low baseline dc offset, the baseline correction operation can be introduced with lower frequency, thus enhancing the system's speed.

3.3 Circuit Technique for Continuous-time Measuring Circuits: Chopper Stabilization

In current analogue integrated circuit modules, the variety of op-amp applications focuses our attention to their input offset voltage. Chopper stabilization (CHS), which has been proposed since the 1940's, provides a stand-alone op-amp with an advanced effective input offset characteristic. It can be used both in continuous time and discrete time integrated applications, such as chopper-stabilized switched-capacitor filters [Z. Ignjatovic, 2004] [P. R. Gray,1981], analogue-digital converters (ADC) [W. Lee, 1996] [C. B. Wang, 2001], and biasing circuits [L. Hebrard, 2005].

Fig. 3.5 Chopping principle in frequency and time domain

The underlying working principle of CHS is shown in Fig. 3.5 [C. C. Enz, 1987]. Suppose the input signal spectrum is limited within $f_{chop}/2$ under the communication aliasing-immune constraint. After the first chopper, the input signal is modulated up to the chopping frequency f_{chop} . Odd harmonics will be at 3 f_{chop} , 5 f_{chop} , 7 f_{chop} , and so on. While at this stage, the low-frequency 1/f noise and dc offset voltage stay at their basebands, and they add up together with a modulated signal. After being

amplified, at the second chopper, the mixer is demodulated. The signal is transposed back to the baseband after amplification, while the low frequency noise and dc offset are transposed to a higher frequency. Through these two chopping stages, the original low frequency signal and noise, offset are distinguished and set apart from each other at frequency domain. After a low-pass filter (LPF) with $f_{\text{chop}}/2$ cutoff frequency, the higher frequency imperfection is largely eliminated from the signal path.

Nevertheless, the CHS technique has its own drawbacks. The nonidealities of the chopping modulators, specifically the input chopping modulator, introduce a residual offset to the amplification. Normally the multiplication chopper can be implemented using cross-coupled switches which are constructed by MOS transistors. These nonidealities mainly come from the mismatches of the clock feedthrough and the switch charge injection of the MOS switch transistor chopper. They may introduce input-signal-dependent and temperature-dependent nonlinear components to the applied system. This residual offset exists in the form of very high frequency glitches or spikes. Therefore, it is desirable to investigate circuit techniques for further improving the performance of CHS amplifiers. This will be a focus of this thesis.

3.4 AC-based Capacitance Measuring Circuit

Instead of the switched-capacitor technique, the performance of an ECT system can be improved [W. Q. Yang, 1999] by using an AC-based capacitance measuring circuit. Such a circuit does not have any MOS switches directly connected to sensor electrodes. Therefore, it does not suffer from charge injections. The front-end circuit for capacitance measurements is shown in Fig. 3.3.1.

Fig. 3.3.1 The AC-based capacitance measurement circuit [H. Hahnel *et.al.* 1995]

The op-amp is configured as a non-inverting amplifier. An amplitude-controllable sine-wave voltage source is applied to its non-inverting input. By means of op-amp feedback, the inverting input to which the electrode is connected is kept at the same potential as the non-inverting input. The left-side electrode is used as an excitation electrode. A sine-wave voltage (V_i) is applied to the non-inverting input, the inverting input is kept at the same potential and hence the left-side electrode is excited by the sine wave. The right-side electrode is used as a detection electrode. The amplitude of the sine wave voltage source is set to zero, i.e. the non-inverting input is effectively connected to the earth, and the potential of this electrode is zero. By this arrangement, an electrode can be used as either an excitation electrode or a detection electrode, and there are no switches connected to sensor electrodes directly. The output of the right side is

$$V_{o2} = -\frac{(j \times \omega \times C_x \times R_f) \times V_i}{j \times \omega \times C_f \times R_f + 1} \quad (3.3.1)$$

where C_x is the measured capacitance

R_f is the feedback resistance

C_f is the feedback capacitance

ω and V_i are the angular frequency and amplitude of the excitation

voltage.

The capacitor (C_f) is made small value of a few pF, and the feedback path is dominated by the resistor (R_f) at the intended excitation frequency. Hence,

$R_f \ll \frac{1}{\omega \times C_f}$, and equation (3.3.1) is simplified as

$$V_{o2} = -j \times \omega \times C_x \times R_f \times V_i \quad (3.3.2)$$

The output of the front-end circuit is linear with the measured capacitance. The sensitivity is proportional to the frequency, amplitude of the excitation voltage and the feedback resistance. To increase the circuit's sensitivity, a high frequency, large amplitude excitation signal and a high feedback resistance are desirable. It is also necessary to employ a high excitation frequency for a high imaging rate. However, the frequency of the applied excitation signal and the resistance value is limited by the op-amp's gain bandwidth, and the amplitude of the excitation signal is limited by the op-amp's power supply, usually $\pm 15V$. This results in a very high gain bandwidth product of the op-amp, leading to significant power consumption by the transducer. Besides, the usual high stability of the voltage reference source in other transducers is now translated as the requirement of a highly-stable excitation ac source. Obviously, for stability control, the digital sine wave signal generator is an extra circuit block that is required by the system, compared to its switched-capacitor counterpart. This is an expensive, inefficient and space-consuming option for implementing integrated circuits. Although the AC-based capacitive measurement system eliminates switch charge injection, it is complex, and the nonlinearity arising from the non-ideal analogue multiplier and the rectifier limits the minimum resolution to only 10 fF [H. Hahnel *et.al.* 1995]. Therefore, the signal's dynamic range is significantly reduced in such implementations.

Fig. 3.3.2 Complete capacitance measurement channel for one electrode in AC-based ECT system

3.5 Comments on Capacitance Measuring Circuits

The sample-data circuit technique has become one of the most promising approaches for developing high-dynamic range transducers, because the natural sample-and-hold process makes it easy to reduce low-frequency flicker noise and offset using typical CMOS amplifiers, instead of very low-noise BJT or BiFET based amplifiers. The reset feature favors a high parasitic operation environment, because of the stray immune property of switched-capacitor circuits. As can be seen, the chopping technique employed in ac based transducers does not lead to a high dynamic range, despite the ac based structure having many stray immune properties. However, the chopper stabilization circuit technique offers significant benefits for the design of low-noise integrated circuits in the context of no folded-back noise. This is particularly suitable for signal-conditioning based applications.

Based on these observations, the sample-data circuit is suitable for the design of front-end transducers, whereas the chopper stabilization circuit is suitable for the design of back-end signal-conditioning circuits. From here on, this study examines both options to devise a high-quality transducer so as to take advantage of the technical merits of both schemes.

In addition, the technology platform is suitable for monolithic integration despite prior work at UMIST or Zhejiang University where ECT systems were implemented as discrete components. Recently, the NTU CDS capacitance measuring circuit has demonstrated that ECT systems are flexible enough to be fully integrated, that time-constant setting can easily be used, and that the switched-capacitor technique can be used to reduce the number of external components used. Another advantage is that the sample-data based ADC is a natural interface with the switched-capacitor transducers.

When transducers are compared in terms of their capacitance-measuring circuits, switched-capacitor transducers tend to be simpler as they are made up of straightforward building blocks. On the contrary, circuits based on the standalone continuous-time ac-based counterpart rely on the peculiar multiplier component, where linearity is an issue, or the digital sine wave signal generator block, where cost is a concern. Thus, ac-based architecture may not be optimal in the context of design complexity and performance.

This research project represents an ongoing effort to focus on new circuit techniques and new transducer circuit architectures, so as to further improve the design of capacitive measuring circuit, based on the relative advantages and disadvantages of two categories of transducers. The project aims to design and implement a monolithic capacitive transducer using the sample-data and the continuous-time chopper-stabilization as a hybrid approach, because the hybrid circuit architecture can improve the performance of transducers.

CHAPTER 4

4 PROPOSED CIRCUIT TECHNIQUES FOR PRECISION ANALOG CIRCUITS

4.1 Instrumentation-based Circuit Design Technique

By reviewing both the advantages and disadvantages of previously reported representative works in realizing capacitance-voltage conversion, it is desirable to cancel further non-ideal effects as much as possible for the implementation of the precision transducer. Traditional approaches use AZ or CDS to cancel the dc offset and to reduce $1/f$ noise in switched-capacitor sensory systems. However, the switch errors are reduced through other means, such as through a differential approach in a differential circuit based transducer or through a dummy transistor approach in a single-ended circuit based transducer. For the sake of compactness and because of the potential involvement of a large number of integrated channels, the single-ended transducer is preferred because of the reduced number of external components, reduced size, cost and power consumption. Although classical switch error cancellation techniques can be employed, it is possibly reduced by another means of storage on circuit switch errors using the additional AZ phase of the transducer circuit system and subtracts it through the differential operation in the later stage of the scaling amplifier. In this way, multiple operation cycles on the switched-capacitor transducer system are executed; this does not jeopardize the speed because the switched-capacitor circuits can easily be run more quickly to compensate for the additional operation phase. From a system level point of view, sampling the front-end transducer system level errors looks promising. It is performed like the calibration

process in an instrumental way. Fig. 4.1 provides a conceptual flow chart of the methodology.

Fig. 4.1 Instrumentation methodology of switched-capacitor sensory system

4.2 Analytical Study of Non-ideal Effects in a Classical Precision Amplifier

Fig. 4.2 Error sources and parasitics of a conventional chopping amplifier

The scaling amplifier in the ECT transducer also plays another critical role in sensor signal processing because it serves as the post-amplification stage whilst still requiring precision, low-noise characteristics and low drift against time and temperature. When dealing with heavy parasitic capacitance with stray immunity as the top priority, the switched-capacitor is the best approach, particularly suitable for the front-end transducer design. However, the folded-back noise of the switched-capacitor circuits may not be advantageous in comparison to the CHS amplifier because it can offer lower thermal noise performance. As a result, the CHS amplifier becomes the suitable amplifier topology for the back-end processing stage of the ECT transducer.

Fig. 4.2 highlights summarized scenario of a conventional non-inverting chopping amplifier configuration associated with numerous error sources and parasitics that may cause potential impact on the circuit performance in analog signal-processing task. In theory, the CHS technique applies modulation to transpose the signal to a higher frequency which has no $1/f$ noise, and then modulates it back to the baseband after amplification. As a result, the dc offset source in association with the intrinsic $1/f$ noise will be canceled in principle. Of particularly interest, the common mode rejection of the amplifier is simultaneously enhanced because the input-referred common mode error source, being treated similar to the offset source, is also minimized by the chopping technique simultaneously. Hence, this relaxes the transistor matching requirements in the chopping op-amp design. However, the switch charge injection and clock feedthrough of input chopper switches together with mismatch effect of switches contributes well-known dc and signal-dependent errors (if input signal is large) to the chopping op-amp. More importantly, the unbalance impedances (Z_{in+} and Z_{in-}), as observed from the viewpoint of the effective resistance and effective parasitic capacitance, associated with each input node to op-amp causes uneven split ratio of switch charge, leading to unexpected larger dc error on the basis of uneven cancellation of charge injection in an asymmetry circuit structure. All of

these non-ideal effects are combined to appear in a form of total residual dc error, which is equivalently caused by the average values of spikes over a chopping period. It is also noted the spikes depends on the chopping frequency and the matching characteristic of the circuit. The larger the mismatch, the larger is the spikes in the context of peak amplitude.

In section 4.2.1, the fundamental error sources in a chopping op-amp are modeled. In section 4.2.2, the error models are extended to a chopping DDA and a new resistance balancing technique is introduced for compensation of the unbalanced resistive gain network so as to obtain better offset reduction. In later chapter VIII of results and discussions, the simulation results for compensated chopping amplifier and chopping DDA are compared with their respective second-order analytical results from the error source models. Their implications are discussed in details. Furthermore, the experimental results are conducted on a previously published chopping DDA to validate the effectiveness of the proposed resistance compensation methodology.

4.2.1 Switch Charge Injection in Chopping Network of the Single-ended Chopping Op-amp

Fig. 4.2.1.1 Simplified schematic of a single-ended chopping op-amp

A typical single-ended chopping op-amp is shown in Fig. 4.2.1.1. The input chopper S_1 transposes the signal to a higher frequency, the internal chopper S_2 demodulates it back to the baseband after amplification by the first gain stage (formed by transistors M_1 - M_9). The non-ideal effects of the first chopper have been discussed in prior section. On the other hand, regardless of the gain of second stage (formed by transistors M_{10} - M_{16}), the errors of internal chopping switches are reduced by the first stage gain, thus they are negligibly small when compared with that of input counterpart. For driving lower resistive load, a source-follower buffer (M_{17} - M_{18}) can be added as an option but at the expense of reduced output swing. Since a multistage topology is used, the nested-Miller frequency compensation is adopted. Due to very high gain structure, the gain error can be reduced significantly, which improves precision ultimately.

Fig. 4.2.1.2 Switch charge injection analytical model

One of the non-ideal effects of MOS transistor switch is the switch charge injection. Fig. 4.2.1.2 depicts the analytical model for analyzing charge injection error voltage. The source terminal is assumed to have finite source resistance R_s and parasitic capacitance C_{ps} whilst the other terminal has a load capacitance C_{eff} , which is mainly contributed by the input capacitance of op-amp. When the transistor switch turns from on to off, part of the injected charge is absorbed by the driving source whereas the other part flows towards the capacitive load. As a result, the charge split ratio is defined as

$$\eta = Q_{ch,eff} / Q_{ch,total} \quad (4.2.1.1)$$

Where $Q_{ch,eff}$ is the charge dump at C_{eff} side whereas $Q_{ch,total}$ is the total switch charge

injection. η is dependent upon terminal impedance. Based on the prior work [J. Shieh, 1987], the error charge at the C_{eff} node with finite R_S and C_{ps} is

$$Q_{ch,eff} = -C_{eff} \frac{UC_G}{2C_{eff}} \exp\left(-\frac{V_{HT}}{UC_{eff}R_S}\right) \times \int_0^{V_{HT}} \left[\mu_n C_{ox} \left(\frac{W}{L}\right) R_S (V_{HT} - U\xi) + 1\right]^{\frac{1}{C_{eff}\mu_n C_{ox} \left(\frac{W}{L}\right) R_S^2 U}} \\ \times \exp\left(\frac{\xi}{C_{eff}R_S}\right) \left(2 - \frac{1}{1 + \mu_n C_{ox} \left(\frac{W}{L}\right) R_S (V_{HT} - U\xi)}\right) d\xi \quad (4.2.1.2)$$

where U denotes the falling rate of the chopping clock, C_G is the total gate capacitance of switch transistor and ξ is the integral variable. The gate-overdrive voltage of the switch transistor is defined as

$$V_{HT} = V_H - V_S - V_{th} \quad (4.2.1.3)$$

where V_H is the ON gate voltage, V_S is the source voltage and V_{th} is transistor effective threshold voltage including the body effect.

For a normal NMOS switch, the total switch charge injection is

$$Q_{ch,total} = -WLC_{ox}(V_{GS} - V_{th}) \quad (4.2.1.4)$$

η can be obtained from (4.2.1.1) - (4.2.1.4) for practically applicable chopping op-amp condition. Fig. 4.2.1.3(a) shows the biphasic clocks with dedicated turn-off times Δt_1 and Δt_4 , non-overlapping times Δt_2 and Δt_5 and turn-on times Δt_3 and Δt_6 . In the first half cycle, the clock ϕ_1 goes from high to low and the complementary clock ϕ_2 goes from low to high, and vice versa for these biphasic clock signals in the second case. Fig. 4.2.1.3(b) shows the first circuit case that two switch transistors M_1 and M_3 start to turn off whereas the other two transistor switches turn on at an elapse of time.

(a) Biphasic non-overlapping control clock signals ϕ_1 and ϕ_2 (b) M_1 - M_3 start turning off but M_2 - M_4 turn on at $\Delta t_1 + \Delta t_2 + \Delta t_3$ later

Fig. 4.2.1.3 Switch charge injection voltage errors sampled by capacitive loads

For lumped resistance modeling, the switch admittance is $2G_{on}$ (equivalent to $2/R_{on}$) for a half switch. The G_{on} is the on-conductance of a triode switch which is defined as

$$G_{on} \approx \mu C_{ox} (W/L)(V_{GS} - V_{th}) \quad (4.2.1.5)$$

Refer to the middle points N_1 and N_3 nodes of lumped resistor model for on switches, they exhibit high impedance with respect to the substrate. When the switches turn from ON to OFF, the channels disappear. N_1 and N_3 become ground since the switch channels merge with the substrate at the instant. This process emulates a sample-and-hold action, with channel on-off phenomenon being treated as sampling switch behavior and lumped parasitic capacitors C_{eff+} and C_{eff-} being treated as the sampling capacitors with reference to ground. Note that $C_{eff+} \approx C_{p+}$, $C_{eff-} \approx C_{p-}$, and

assuming that the effective parasitics are dominated by the input capacitances of amplifier and the routing parasitics are negligible.

Finally, potentials induced in each half switch channel of M_1 and M_3 will be sampled by the two lumped parasitic capacitors. Since the channel admittance changes from on state to off state of the switch, the average change of half switch admittance in transition time Δt_1 is estimated to be $G_{on(average)} = 1/R_{on}$. This leads to the sampled charge injection error voltage $V_{ch,M_1} = \frac{\Delta Q_{ch,M_1}}{\Delta t_1} R_{on,M_1}$ in M_1 and $V_{ch,M_3} = \frac{\Delta Q_{ch,M_3}}{\Delta t_1} R_{on,M_3}$ in M_3 , respectively. However, they are further averaged by a factor $\frac{\Delta t_1}{T/2 - \Delta t_2 - \Delta t_3}$ due to the channel voltage induced in finite turning-off time Δt_1 for given half clock cycle. These charge injection error voltages appear in a form of common-mode dc signals superimposed on either an input signal potential (using non-inverting amplifier configuration like the case in Fig. 4.2) or a virtual analog ground potential (using inverting amplifier configuration) in C_{eff+} and C_{eff-} . Based on the relationship that $I = Q/t = V/R$, the mean channel dc charge injection error voltages are written as

$$V_{ch,M_1} = \frac{\Delta Q_{ch,M_1}}{\Delta t_1} R_{on,M_1} \frac{\Delta t_1}{T/2 - \Delta t_2 - \Delta t_3} \quad (4.2.1.6)$$

$$V_{ch,M_3} = \frac{\Delta Q_{ch,M_3}}{\Delta t_1} R_{on,M_3} \frac{\Delta t_1}{T/2 - \Delta t_2 - \Delta t_3} \quad (4.2.1.7)$$

Since $(T/2) \gg \Delta t_2$ and Δt_3 , we have

$$V_{ch,M_1} \approx \Delta Q_{ch,M_1} \frac{R_{on,M_1}}{T/2} \quad (4.2.1.8)$$

$$V_{ch,M_3} \approx \Delta Q_{ch,M_3} \frac{R_{on,M_3}}{T/2} \quad (4.2.1.9)$$

Using (4.2.1.1)-(4.2.1.5), (4.2.1.8) and (4.2.1.9), the charge injection error voltage source, arising from the M_1 and M_3 in differential input of amplifier, is derived as follows:

$$\begin{aligned}
\Delta V_{ch,M_1 \& M_3} &= V_{ch,M_1} - V_{ch,M_3} \\
&\approx \eta_1 Q_{ch,M_1} R_{on,M_1} / (T/2) - \eta_3 Q_{ch,M_3} R_{on,M_3} / (T/2) \\
&\approx -\eta_1 (WL)_1 C_{ox} (V_{GS1} - V_{th1}) R_{on,M_1} / (T/2) \\
&\quad + \eta_3 (WL)_3 C_{ox} (V_{GS3} - V_{th3}) R_{on,M_3} / (T/2)
\end{aligned} \tag{4.2.1.10}$$

Note that the differential operation in Fig. 4.2.1.3(b) also subtracts the almost identical analog signals at B and D due to feedback in non-inverting configuration or the almost identical analog ground potentials at B and D due to feedback in inverting configuration. This leads to the residual charge injection dc defined in (4.2.1.10).

At the instant that the transistors, M_1 and M_3 , switch from on to off, the respective gate-to-source voltage is signal-dependent and given by

$$V_{GS,i} = V_G - V_{S,i} = V_{DD} - V_{S,i} = V_{DD} - (V_Q + v_{in}) \tag{4.2.1.11}$$

with $i = 1,3$ and V_Q is the quiescent voltage at node A, B, C and D in Fig. 4.2.1.3(b). Due to the body effect, each threshold voltage of the MOS transistor switch will be modulated by the input signal. Further mismatch in threshold voltages also contributes additional error. For simplicity, the short channel length and narrow width effects are ignored. The threshold voltage pertaining to the above two effects can be modeled as

$$V_{th,i} \approx V_{th0} + K1(\sqrt{2\Phi_f + V_{SB,i}} - \sqrt{2\Phi_f}) + K2V_{SB,i} + \Delta V_{th,i} \tag{4.2.1.12}$$

whereas the source-to-bulk voltages in the bulk-modulated transistors are

$$V_{SB,i} = V_{S,i} - V_B = V_{S,i} - 0 = V_Q + v_{in} \tag{4.2.1.13}$$

with $i = 1,3$. It is assumed that V_{th0} is the nominal reference threshold voltage at zero source-bulk voltage. $\Delta V_{th,i}$ is the lumped deviation of threshold voltage in a single MOS switch transistor with respect to the nominal V_{th} , ranging from -5mV to +5mV

in a typical process. $K1$ and $K2$ denote the first-order and second-order body effect coefficients, respectively in the BSIM3 model.

Furthermore, a mismatch in switch area contributes another error. If the ideal dimension is treated as WL, α can be introduced to a MOS switch transistor as the relative mismatch coefficient with respect to the ideal case. They represent the percentage of mismatch from the nominal value of the gate area of the four switch transistors respectively. In practical processes, α ranges from -2% to 2%. Assuming α_1 , α_2 , α_3 and α_4 represent the percentage of mismatch from the nominal value of the gate area of M_1 , M_2 , M_3 and M_4 , substituting (4.2.1.11)-(4.2.1.13) into (4.2.1.10), we obtain (4.2.1.14). For the clock transition case in second half cycle, there is also a similar result (4.2.1.15) for the signal-dependent charge injection error voltage source $\Delta V_{ch,M_2 \& M_4}$ caused by M_2 - M_4 switch pair in the complementary operation.

$$\begin{aligned} \Delta V_{ch,M_1 \& M_3} &= V_{ch,M_1} - V_{ch,M_3} \\ &= \eta_3(WL)(1+\alpha_3)C_{ox}[V_{DD} - V_Q - v_{in} - V_{th0} - K1(\sqrt{2\Phi_f + V_Q + v_{in}} - \sqrt{2\Phi_f}) - K2(V_Q + v_{in}) - \Delta V_{th,3}]R_{on,M_3} / (T/2) \\ &\quad - \eta_1(WL)(1+\alpha_1)C_{ox}[V_{DD} - V_Q - v_{in} - V_{th0} - K1(\sqrt{2\Phi_f + V_Q + v_{in}} - \sqrt{2\Phi_f}) - K2(V_Q + v_{in}) - \Delta V_{th,1}]R_{on,M_1} / (T/2) \end{aligned} \quad (4.2.1.14)$$

$$\begin{aligned} \Delta V_{ch,M_2 \& M_4} &= V_{ch,M_2} - V_{ch,M_4} \\ &= \eta_4(WL)(1+\alpha_4)C_{ox}[V_{DD} - V_Q - v_{in} - V_{th0} - K1(\sqrt{2\Phi_f + V_Q + v_{in}} - \sqrt{2\Phi_f}) - K2(V_Q + v_{in}) - \Delta V_{th,4}]R_{on,M_4} / (T/2) \\ &\quad - \eta_2(WL)(1+\alpha_2)C_{ox}[V_{DD} - V_Q - v_{in} - V_{th0} - K1(\sqrt{2\Phi_f + V_Q + v_{in}} - \sqrt{2\Phi_f}) - K2(V_Q + v_{in}) - \Delta V_{th,2}]R_{on,M_2} / (T/2) \end{aligned} \quad (4.2.1.15)$$

Since the input signal and feedback signal swap with each other at the input terminals of op-amp in every half cycle, the average effective charge injection error voltage in one clock cycle is thus obtained as

$$V_{ch\_eff} = \frac{\Delta V_{ch,M_1 \& M_3} + \Delta V_{ch,M_2 \& M_4}}{2} \quad (4.2.1.16)$$

As a result, the charge injection effect in the non-ideal chopper model can be

separated into an ideal chopper plus an input-referred error voltage source which represents effective switch charge injection as shown in Fig. 4.2.1.4

Fig. 4.2.1.4 Input-referred switch charge injection error voltage source

4.2.2 Clock Feedthrough in Chopping Network

Fig. 4.2.2.1 Clock feedthrough errors induced by chopping switches at first half cycle

A MOSFET switch in the chopper couples the clock transitions through its gate-source and gate-drain overlap capacitances and introduces the clock feedthrough error to the capacitance associated with the node. Although the ideal differential operation can cancel the clock feedthrough effect, the practical mismatch of switch transistors will lead to a residual dc error.

Assuming the overlap capacitance is constant, for an n-channel transistor switch, the induced error voltage in the effective parasitic capacitor C_{eff} is given by

$$V_{cf} = -\Delta V_{ck} \frac{(WL)(1 + \alpha_i)C_{ov}}{(WL)(1 + \alpha_i)C_{ov} + C_{eff}} \quad (4.2.2.1)$$

where $i = 1, 2, 3, 4$, ΔV_{ck} is the change of clock voltage that is positive from V_{DD} to V_{SS} and negative from V_{SS} to V_{DD} , C_{ov} is the overlap capacitance per unit area of gate-drain or gate-source. Refer to Fig. 4.2.2.1, in first half cycle, the clock feedthrough errors including mismatch with respect to ideal switch area WL are

$$V_{cf,M_1} = -(V_{DD} - V_{SS}) \frac{(WL)(1 + \alpha_1)C_{ov}}{(WL)(1 + \alpha_1)C_{ov} + C_{eff}} \quad (4.2.2.2)$$

$$V_{cf,M_2} = -(V_{SS} - V_{DD}) \frac{(WL)(1 + \alpha_2)C_{ov}}{(WL)(1 + \alpha_2)C_{ov} + C_{eff}} \quad (4.2.2.3)$$

$$V_{cf,M_3} = -(V_{DD} - V_{SS}) \frac{(WL)(1 + \alpha_3)C_{ov}}{(WL)(1 + \alpha_3)C_{ov} + C_{eff}} \quad (4.2.2.4)$$

$$V_{cf,M_4} = -(V_{SS} - V_{DD}) \frac{(WL)(1 + \alpha_4)C_{ov}}{(WL)(1 + \alpha_4)C_{ov} + C_{eff}} \quad (4.2.2.5)$$

Hence, the input-referred clock feedthrough error voltage source for the first half cycle becomes

$$\begin{aligned} \Delta V_{cf,1} &= V_{cf,M_1} - V_{cf,M_3} + V_{cf,M_4} - V_{cf,M_2} \\ &= -(V_{DD} - V_{SS}) \frac{1}{1 + C_{eff} / [(WL)(1 + \alpha_1)C_{ov}]} \\ &\quad + (V_{DD} - V_{SS}) \frac{1}{1 + C_{eff} / [(WL)(1 + \alpha_3)C_{ov}]} \\ &\quad - (V_{SS} - V_{DD}) \frac{1}{1 + C_{eff} / [(WL)(1 + \alpha_4)C_{ov}]} \\ &\quad + (V_{SS} - V_{DD}) \frac{1}{1 + C_{eff} / [(WL)(1 + \alpha_2)C_{ov}]} \end{aligned} \quad (4.2.2.6)$$

Since there is a reversal of input terminals and the opposite clock transitions occur in the chopping network during the second half cycle, the induced clock feedthrough error $\Delta V_{cf,2}$ is identical to that of the first half cycle. Consequently, the effective clock feedthrough error in one clock cycle is obtained as

$$V_{cf\_eff} = (\Delta V_{cf,1} + \Delta V_{cf,2}) / 2 \quad (4.2.2.7)$$

The input-referred error source model for standalone clock feedthrough effect is illustrated in Fig. 4.2.2.2.

Fig. 4.2.2.2 Input-referred clock feedthrough error voltage source

4.2.3 Non-ideal Effects in Op-amp

Fig. 4.2.3.1 Non-inverting gain circuit with finite open-loop gain chopping op-amp

The finite open-loop gain of op-amp affects the precision of the feedback system. Therefore, the finite gain error in Fig. 4.2.3.1 can be derived as

$$\Delta V_{\varepsilon} = v_{in} \left(-\frac{R_1 + R_2}{R_2} \times \frac{1}{A} \right) \quad (4.2.3)$$

Besides finite gain error, other contributions come from dc offset and common-mode error. Their models are illustrated also in Fig. 4.2.3.2. The common-mode error voltage source equals to the division of the input common mode voltage V_{CM} over the common-mode rejection ratio (CMRR). Like the dc offset, the common-mode error will be reduced by the CHS technique. This explains why the chopping amplifier has improved common mode rejection ratio when compared to the conventional counterpart without using CHS technique.

Fig. 4.2.3.2 Finite gain error, dc offset error and common mode error in a chopping op-amp

4.2.4 Complete Error Source Models of Single-ended Chopping Op-amp

Taking into account of error source models including switch charge injection, clock feedthrough, finite gain error, common-mode error and dc offset, these lead to the input-referred voltage sources in Fig. 4.2.4. Since the common-mode error as well as the dc offset will be substantially reduced by the chopping op-amp, the effective offset error source can be further simplified as follows:

$$v_{error,OpAmp} \approx V_{cf\_eff} + V_{ch\_eff} + \Delta V_{\epsilon} \quad (4.2.4)$$

Fig. 4.2.4 Input-referred error voltage sources in a chopping op-amp

4.2.5 Complete Error Source Models of Chopping DDA

The concept of chopper stabilization can be incorporated into DDA for obtaining further low-noise low-offset characteristics. Like conventional operation, the DDA forces the voltage difference between two floating input ports to the same value in a closed-loop environment such that the chopping DDA becomes a useful instrumentation amplifier for handling floating input signal whilst preserving good accuracy.

Fig. 4.2.5.1 Simplified schematic of a single-ended chopping DDA

Fig. 4.2.5.1 shows the circuit schematic of a single-ended chopping DDA [P. K Chan, 2004]. It is somewhat similar to that of Fig. 4.2.1.1 except with the addition of second input port. Each input port of DDA is identically designed (M_1 , M_2 , M_5 and input chopping switch network S_1 , or M_1' , M_2' , M_5' and S_1'). The floating input signals are transposed to the chopping frequency through the two input chopping switch networks, S_1 and S_1' whereas the differential pairs $M_1'-M_2'$ and M_1-M_2 perform the V-I conversion at high frequency simultaneously. First stage gain is achieved by I-V conversion in the active load formed by transistors M_3-M_4 and M_6-M_9 . Through the use of chopper S_2 , the signal is demodulated back to the baseband frequency but the $1/f$ noise, input common error and dc offset of the first stage are shifted to high frequency simultaneously. The recovered signal is further amplified by the next two-stage amplifier ($M_{10}-M_{16}$) with source follower ($M_{17}-M_{18}$).

Fig. 4.2.5.2 Input-referred voltage sources in a chopping DDA

Fig. 4.2.5.2 shows the input-referred error voltage source models in a chopping DDA.

Since the respective dc offsets and common-mode errors will be suppressed by the CHS action, the effective offset error in a chopping DDA can be further simplified as follows:

$$v_{error,DDA} \approx V_{cf\_eff} + V_{ch\_eff} + \Delta V_{\varepsilon} - V_{cf\_eff}' - V_{ch\_eff}' \quad (4.2.5.1)$$

Based on identically-designed input chopping ports, similar error sources and voltage error equations can be established with respect to that of a chopping op-amp as discussed before. Arising from different circuit configurations, the analysis method on switch charge injection is slightly revised. If the chopping switches were connected to either the input source or non-inverting feedback point, the signal-dependent charge injection error equations are similar to that of (4.2.1.14) and (4.2.1.15), else dropping the “ v_{in} ” terms in the relevant equations if the switches are connected to the analog ground in the DDA closed-loop topology for the case without bulk modulation. Except the gain error, it is interesting to observe in (4.2.5.1) that the combined effects of charge injection and clock feedthrough errors in one input port tend to counteract the corresponding errors in the other input port. However, random errors may be cancelled but dependent upon the matching in layout.

4.3 Precision Amplifier in Capacitive Transducer

Fig. 4.3.1 Adding a resistor for resistance balancing an intrinsic asymmetrical structure in a non-inverting amplifier using chopping op-amp

From preceding analysis, the first offset contribution comes from the dc input-referred

error voltage sources arising from various mismatching effects in MOS device parameters. The second offset contribution, which is one of key suggestions in this work, comes from the uneven split ratio of channel charge caused by mismatch of impedance associated with the driving source terminal and effective impedance of the feedback network as illustrated in Fig. 4.2. However, for low-frequency sensor signal-processing condition, the impedances contributed by parasitic capacitors are usually high and can be ignored for simplicity in analysis. Besides, due to the nonlinear charge dump in (4.2.1.2), the charge split ratio is nonlinear nature. Even $C_{ps} \neq C_p$, the output error is increased slightly. As a result, the resistive level balancing for impedance matching becomes the prime importance. Hence, it is adequately to compensate an unbalancing DDA structure by adding a simple balancing resistor R_b so as to fulfill the approximated condition that $(Z_{in+} \approx R_{in+}) \approx (Z_{in-} \approx R_{in-})$. This phenomenon will be validated in Chapter 8.

Fig. 4.3.1 illustrates the application of the resistance balancing method in an asymmetrical structure of a non-inverting amplifier using a chopping op-amp. For example of $C_L = 25\text{pF}$, $C_{ps} = 5\text{pF}$, $C_p = 3\text{pF}$ and a typical frequency range from dc to kHz in sensor applications, one can exclude the effect of parasitic capacitances because their values are much larger than resistive values at the frequencies of interest. Therefore, we have

$$R_3 = R_S + R_b = R_S + \frac{R_1(R_2 + R_{out})}{R_1 + R_2 + R_{out}} \approx R_1 \quad (4.3.1)$$

with $R_1 < R_2 + R_{out}$. Note that R_{out} is the effective output resistance of op-amp. From (4.3.1), we have

$$R_b = R_1 - R_S \approx R_1 \quad (4.3.2)$$

Fig. 4.3.2 Adding a resistor for resistance balancing an intrinsic asymmetrical structure in a non-inverting amplifier using chopping DDA

Following similar methodology, it can be applied for chopping DDA in Fig. 4.3.2 as well. Through adding one balancing resistor R_b , the two input chopping networks S_1 and S_1' for floating inputs are now balanced to each other, the result of which shares similar advantages in the chopping op-amp.

CHAPTER 5

5 PROPOSED CAPACITIVE TRANSDUCER

5.1 System Architecture and Its Design Considerations

In order to realize the ECT function as a system as discussed in Chapter 2, a particular system architecture of an ECT system is required (shown in Fig. 5.1.1). The proposed capacitive transducer is located at the front portion of the ECT system. This interface chip senses the subtle changes of the external capacitances and the CV convertor converts these changes into DC voltage outputs. This measured output is sampled by a data acquisition card, which is interfaced with the personal computer (PC). It is a convenient setup because the card has a built-in ADC component. Besides, the data acquisition card can be made with a feedback control signal dedicated to the front-end interface. Such a control signal can be a programmable reference voltage to dynamically scale the input reference of the transducer in order to cater to various full-scale ranges of capacitance values. Another key function of the data acquisition card is to establish a communication link in order to transfer the data to the PC for data storage, analysis and image construction. As a result, the image can be displayed on the PC screen.

Fig. 5.1 General system architecture of an ECT system

The sensor electronic (capacitive transducer) is thus the first part of the entire system. The capacitive transducer determines the resolution, sensitivity and efficiency of the whole process. If errors and noise cannot be reduced effectively at the front-end, they will be amplified and propagated stage by stage, hence causing unacceptable results in the final output. Thus, the performance of the capacitive transducer at the front-end interface design is crucial to the performance of the entire imaging system. The requirements [W. Q. Yang, 1999] for an industrial capacitive transducer intended for real time visualization and image construction are as follows:

- (a) compatibility with primary sensors with up to 12 electrodes
- (b) high measurement resolution
- (c) low noise level
- (d) low baseline drift refer to time and temperature
- (e) wide dynamic range of measurement from sub femto- Farad to 2 pico- Farad
- (f) fast data capture rate
- (g) fully software-controlled circuit setting
- (h) communication capability with image reconstruction computer located at remote distance up to 250 meters.

In the ECT application, the external capacitance to be measured for a resolution of less than 1 femto farad under external heavy parasitic capacitances is rather

challenging. For instance, the finite capacitance measurement in the tomography environment is constrained by the heavy stray capacitance (100-200 pF) to the earth of an ECT sensor.

In an ECT sensor, stray capacitance arises mainly from three sources [S. M. Huang, 1992]. They are

- (i) the capacitance between the measurement electrode and the earthed screen;
- (ii) the capacitance of the shielding cable connecting the electrode to a capacitance measuring circuit, typically 1 pF/cm (i.e. 100 pF for a cable of 1 m);
- (iii) the input capacitance of the MOS switches in the capacitance measuring circuit.

This heavy parasitic capacitance raises rigorous requirements to the capacitive transducer in the context of parasitic capacitance immune. That is the reason why the stray immunity on the basis of switched-capacitor circuit topologies must be utilized in the design. In addition, the sensor should have high signal-to-noise ratio (SNR), low drift against time and temperature and high processing rate.

5.2 Proposed Instrumentation-based Switched-capacitor Capacitance Measuring Circuit

5.2.1 Proposed Instrumentation SC Technique with S/H Design Example

The instrumentation based SC methodology described in Chapter 4 has the advantages of sampling and storing multiple parameters such as 1/f noise, offset and switch errors of the SC circuit for cancellation instead of the traditional method of SC circuits, which solely makes use of AZ or CDS to cancel the 1/f and offset noise only. The remaining charge-injection issue relies on either the differential technique or the

dummy compensation switch with a single-ended structure. Here, the circuit means of using the instrumentation based SC approach to cancel switch errors of MOS switches becomes the key technical merit in the proposed single-ended capacitive transducer. Prior to discussing the new capacitance measuring circuit, the use of the instrumentation based SC approach on the design of a high precision sample-and-hold (S/H) is first presented, so as to illustrate the evolution of the methodology to other proposed circuit architectures in subsequent sections.

Sample-and-hold (S/H) circuit is a key analog building block. The basic function is to transform a continuous-time signal into a quasi-analog signal. Therefore, it serves as important front-end data acquisition device in data converter architectures. Hence, the accuracy dictates the overall static or dynamic performance in converters. In integrated transducer environment [S. Ogawa, 2001], the sample-and-hold circuit can be utilized in the form of analog memory to hold the acquired intermediate analog signal for sensor analog signal processing or used in analog-to-digital converter (ADC) for sensor data acquisition. Based on sensor applications, not only does the sample-and-hold circuit provide precision, but it is also required to achieve low drift in terms of time and temperature.

The design of accurate S/H circuits is not straightforward. This stems from the fact that the practical S/H circuits suffer from various linear and nonlinear effects, which greatly limit their performance. In CMOS low-frequency implementations, the major error sources [B. J. Sheu, 1997] [D. A. Johns, 1996] are principally contributed by switch charge injection, switch clock-feedthrough effect, dc offset of op-amp and finite open-loop gain of op-amp. More importantly, the intrinsic $1/f$ noise, arising from MOS devices in CMOS op-amp, appears as the dominant noise source that reduces the dynamic range of the S/H circuit significantly. All these problems motivate the search for robust circuit techniques that can solve the shortcomings.

Fig. 5.2.1.1 A conventional sample-and-hold circuit

The closed-loop S/H design approach is of particular attention in integrated transducer because of potential better accuracy although there is a penalty on speed. A well-known popular S/H circuit [D. A. Johns, 1997] is implemented by including a buffer-based sample-and-hold network in the feedback loop of an op-amp as depicted in Fig. 5.2.1.1. During clock phase ϕ_1 in sample mode, the circuit is configured as a closed-loop unity-gain op-amp. At the end of clock phase ϕ_2 in hold mode, the input voltage sampled at that time is then stored in capacitor C. Refer to the prior-art circuit, the key advantages are identified as (i) simple topology, (ii) no loading effect because of infinite the input impedance at low frequency (iii) the dc error due to the buffer being divided by high open-loop gain and hence it is of little concern. However, there are several disadvantages: (i) the input offset and $1/f$ noise of the op-amp will remain, (ii) the signal-dependent switch charge injection as well as the clock-feedthrough effect deteriorates the sampling precision and (iii) the circuit displays temperature dependent characteristic since offset and switch charge-injection are sensitive to temperature.

Fig. 5.2.1.2 Proposed high-precision low-drift S/H circuit

Fig. 5.2.1.2 shows the proposed high-precision low-drift S/H circuit topology. It consists of one op-amp (two-stage topology), two sample-and-hold networks with bootstrap sampling switches, two source-follower-based buffers and one chopper-stabilized differential difference amplifier (CHSDDA). The sequential operation of the S/H circuit is controlled via associated timing control signals, which are derived from the four-phased non-overlapping clocks ϕ_1 , ϕ_2 , ϕ_3 and ϕ_4 .

The operation algorithm is based on auto-zero (AZ) process [C. C. Enz, 1996] combined with critical bootstrap switches [X. P. Fan, 2002] for accurate error sampling and makes use of differential operation for error subtraction via a highly accurate differential-to-single-ended CHSDDA. The circuit operation can be separated into four phases: reset phase, offset and switch charge injection sample phase, signal sample phase and signal hold phase. Different topologies of the circuit at different clock phases are illustrated in Fig. 5.2.1.3.

Fig. 5.2.1.3 Circuit topologies at different clock phases: ϕ_1 , ϕ_2 , ϕ_3 and ϕ_4

During ϕ_1 (reset phase), S2, S6 and S7 are closed and other switches are open. A feedback loop is formed. The capacitor C1 is charged up to input-referred offset voltage, V_{os} , of the op-amp.

During ϕ_2 (offset and switch charge injection sample phase), S2 and S4 remain closed whilst other switches remain open. Since S6 changes from on mode in ϕ_1 to off mode in ϕ_2 , the switch channel charge as well as clock-feedthrough charge arising from this action flows in the holding capacitor C1. Therefore, C1 holds the residual dc offset (being sampled in ϕ_1) together with the switch charge injection error and clock-feedthrough error, $V_{out1} = (V_{offset} + V_{inj} + V_{clk})$, waiting for the subsequent subtracting operation at ϕ_4 . Meanwhile, the buffer drives CHSDDA with the error voltage.

During ϕ_3 (signal sample phase), S1, S3 and S5 are then closed but S2 and S4 are now open. C3 samples the input signal V_{in} plus dc offset of the op-amp. The buffer associated with the capacitor C3 drives the other input terminal of CHSDDA with signal plus error voltage.

During ϕ_4 (signal hold phase), S2 and S4 are closed again whilst other switches are switched off. The op-amp is now configured with unity-gain topology with the non-inverting input being shorted to analog ground. Since S5 is switched from on mode to off mode, the switch channel charge as well as clock-feedthrough charge arising from this action flows in the holding capacitor C3. Of particular interest, the switch charge injection in ϕ_4 is similar to that of ϕ_2 . As a result of ϕ_3 and ϕ_4 operations, the voltage developed in C3 comprises the sampling signal and the error voltage that is made up of dc offset of op-amp, switch charge injection and clock-feedthrough effect. Ultimately, the capacitor C3 holds the value of $V_{out2} = (V_{in} + V_{offset} + V_{inj} + V_{clk})$.

The two error voltages stored in C1 and C3 respectively, which are regarded as the common-mode components, will be cancelled by the subsequent differential operation in CHSDDA as shown in Fig. 5.2.1.2. It should be noted that the chopper stabilization (CHS) technique, being applied to DDA, aims at eliminating the dc offset and $1/f$ noise in conventional DDA [S.C. Huang, 1993].

Although the AZ technique samples the unwanted quantities such as offset and switch error voltages that can be cancelled via subtraction, there still exists error sampling issue on the basis of signal-dependent characteristic of single MOS switch. Refer to Fig. 5.2.1.2, S5 and S6 are the key switches that cause the signal-dependent charge injection arising from different developed voltages across capacitors C1 and C3, respectively.

Consider a common MOS switch switching from on to off, the switch channel charge is given as

$$Q_{ch} = -W \times L \times C_{ox} \times (V_{DD} - V_{in} - V_T) \quad (5.2.1.1)$$

where W is the channel width, L is the channel length, C_{ox} is the gate oxide per unit area, and V_{TH} is the threshold voltage of MOS transistor. It can be seen that the channel charge can be input signal dependent through body effect on the threshold term.

There are several bootstrap schemes [X. P. Fan, 2002] [H. Kobayashi, 2001] that are able to minimize signal-dependent charge injection. Herewith, a parallel bootstrap switch is employed since it offers better resolution as well as low temperature sensitivity.

Fig. 5.2.1.4 Switched-capacitor parallel bootstrap switch

Refer to Fig. 5.2.1.4, two bootstrap transistors are connected in a parallel topology. In CLK2, the battery capacitors C_b and C_b' are charged up to differential voltage of V_{dd}' .

and analog ground. In CLK1, these two battery voltages are applied for the gate-to-source terminals of the two switch transistors, MN1 and MN1' respectively. To the first order, the currents flowing through the two switch transistors in triode region are

$$i_1 \approx \mu_n C_{ox} \frac{W}{L} [(V_S + V_C - V_S - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (5.2.1.2)$$

$$\therefore i_1 \approx \mu_n C_{ox} \frac{W}{L} [(V_C - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (5.2.1.3)$$

$$i_2 \approx \mu_n C_{ox} \frac{W}{L} [(V_D + V_C - V_S - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (5.2.1.4)$$

$$\therefore i_2 \approx \mu_n C_{ox} \frac{W}{L} [(V_C - V_T)V_{DS} + \frac{1}{2}V_{DS}^2] \quad (5.2.1.5)$$

where V_C is defined as the constant floating voltage source being applied between gate-to-source terminals, and the other symbols have their usual meaning. Using Eqn. (5.2.1.2) and Eqn. (5.2.1.4), the total current can be written as

$$i = i_1 + i_2 \approx 2\mu_n C_{ox} \frac{W}{L} (V_C - V_T)V_{DS} \quad (5.2.1.6)$$

From (5.2.1.6), the effective resistance is obtained as

$$R_{on} \approx \frac{1}{2\mu_n C_{ox} \frac{W}{L} (V_C - V_T)} \quad (5.2.1.7)$$

The bootstrap technique brings in significant advantages that the conducting current and the on-resistance of the switch are signal-independent. Besides, the charge injection of this switch is also independent of the input signal to the first order since the effective gate-to-source voltage is kept constant.

The chopper stabilized differential difference amplifier is configured as a unity-gain differential amplifier. The first input chopper translates the differential input signal up to higher frequency in amplified form while the offset of the chopping DDA remains in the baseband and is amplified by the first gain stage. The second chopper in the intermediate stage demodulates the amplified ac signal into baseband whereas the offset of the first stage amplifier is modulated to chopping frequency. Hence, the intrinsic offset or 1/f noise is reduced significantly. More importantly, the CHSDDA

can provide voltage gain on the input signal through adding gain-defined resistive network.

5.2.2 Foundation Switched-Capacitor Transducer Circuit

A foundational switched-capacitor transducer circuit based on the proposed instrumentation SC methodology is shown in Fig. 5.2.2.1.

Fig. 5.2.2.1 Topology of proposed capacitive transducer

The capacitance measurement circuit consists mainly of two parts, where the first part

is the CDS capacitive capacitance-to-voltage (CV) measuring circuit with one op-amp and two sample-and-holds while the second part is the differential difference amplifier (DDA) for the differential-to-single-ended operation. It is called an instrumentation based SC CDS capacitive transducer that has switch charge injection sampling by an additional AZ operation and its cancellation by differential subtraction. In the following sub-sections, two main points are discussed in detail.

The first stage op-amp serves as a CV converter that generates the desired output voltage signal whilst minimizing $1/f$ noise as well as the dc offset voltage of the op-amp and charge injection due to MOS switches. The system proposed here makes use of both the Auto Zero (AZ) process and the Correlated-Double-Sampling (CDS) technique. The AZ process samples the unwanted circuit charge injection first and subtracts it from the subsequent operation. The CDS is aimed at removing the $1/f$ noise and offset of the op-amp.

Fig. 5.2.2.2(a) A CDS capacitance measuring circuit with switch charge injection sampling by AZ operation

Fig. 5.2.2.2(b) Clock phases used in the capacitance measuring circuit

Fig. 5.2.2.3 Circuit topologies at clock phase of 1, 2, 3, 4

Fig. 5.2.2.2(a) shows the front-end capacitance detection circuit with both AZ and CDS techniques with the operation clock phases as depicted in Fig. 5.2.2.2(b). Different topologies of the circuit at different clock phases are illustrated in Fig. 5.2.2.3. They are reset, switch charge injection measurement, offset sampling and sensing phases respectively.

During ϕ_1 (reset phase), C_x and C_f are both connected to virtual ground and charged to V_{os} to emulate the topology of offset sampling phase.

During ϕ_2 (switch charge injection measurement phase), one side of C_f is tied to the output node of the op-amp to realize the feedback loop, but the other side of C_x remains the connection to virtual ground. This leads to the offset independent transfer function as

$$V_{out1} = \frac{-C_x}{C_f} \times V_{input} + e_l \quad (5.2.2)$$

where e_l is the voltage error due to circuit charge injection, while the input voltage V_{input} is virtual ground at this phase. The switch error voltage arising from the open of MOS switch is then stored in S/H 1 at the end of ϕ_2 , waiting for the subsequent subtraction operation at ϕ_4 .

During ϕ_3 (offset sampling phase), M2, M3 and M5 are closed. C_x and C_f are charged to V_{os} of the op-amp. Thus, V_{os} is sampled in C_f at this clock phase again. Circuit topology of ϕ_3 can be seen as another copy of circuit topology at ϕ_1 but only focusing on sampling offset error of op-amp.

During ϕ_4 (sensing phase), C_x is configured to connect to V_{in} , M2, M3 and M5 are open. M4 is ON for establishing the feedback. Except that C_x is connecting to V_{in} instead of virtual ground, the circuit is the exact configuration as that in ϕ_2 . This operation ensures the switch charge injection in ϕ_4 is identical to that of ϕ_2 , and the error voltage being produced is also the same. The ϕ_3 and ϕ_4 operations result in the output voltage comprising measured signal as well as switch error as described by equation (5.2.1). Consequently, the circuit injection will be cancelled by the subsequent differential operation through DDA.

In addition, M3 is the key switch that causes the charge injection. It is important to turn on M3 slightly before other switches so as to minimize switch charge injection incurred by M1 and M2.

5.2.3 Improved Switched-Capacitor Transducer Circuit

The foundation instrumentation SC CDS capacitive transducer is based on an open-loop configuration. In order to reduce errors and noise components come from S/H blocks, a feedback approach is utilized in order to improve upon the precision of the capacitive transducer. Although the closed-loop configuration reduces the speed of the sensory system, it will not jeopardize speed in the ECT system because the signal bandwidth is generally not broad. The switched-capacitor circuits can be made to run adequately fast in typical CMOS technology today. With a monolithic design rather than discrete component implementation, this further relaxes the speed tradeoff. Besides, the differential difference amplifier also suffers from $1/f$ noise and dc offset problems. It can be improved by means of adding chopper stabilization.

Fig. 5.2.3.1 Proposed switched-capacitor transducer for electrical capacitance tomography

The proposed switched-capacitor transducer is shown in Fig. 5.2.3.1. It comprises a CV convertor (the part covered by two dashed boxes) and a high-precision gain

amplifier (the part outside the dashed box). Here, the CV convertor is also divided into two portions. The left portion in the dashed box is dedicated to the sensing capacitance C_x with a built-in design-for-test circuitry. For measurement or testing on small C_x values in a high resolution capacitive transducer operation environment, the concepts of “parasitic balancing” and “lever mechanism” are proposed. These are discussed in a later part of this section. The right portion deals with the feedback capacitor C_f together with one op-amp and two sample-and-hold circuits. They are able to be configured in different feedback topologies via the control logic on the associated switches. The instrumentation based SC methodology plus CDS technique is used in the first CV converter. It is a stray insensitive circuit architecture. The post-amplification is performed in the second CHSDDA stage, incorporating the proposed resistance balancing technique. Not only does the combined circuit architecture support the usual reduction of dc offsets and $1/f$ noise, it also provides good precision as well as the circuit switch error cancellation. This is similar to the case of the precision S/H design example described in Section 5.2.1.

5.2.3.1 Design-for-test issues

a) Voltage shifting

Although the closed-loop topology slows down the speed of the CV conversion, the flowing speed of the mixture inside the measured pipeline may not be high. Hence, the image construction specification can still be met. More importantly, the closed-loop design reduces the errors or noise contributed by the internal blocks such as the S/H circuits. The feedback mechanism also assists with maintaining circuit stability in terms of drift against temperature and time. As a result, these can be regarded as the technical merits of the circuit architecture. A level-shifting technique is used to reduce the on-resistance of the switches for the charging and discharging operation in heavy parasitic capacitors. Therefore, 1 V virtual ground is employed

instead of a mid-point 1.5V for a 3V single supply. Another advantage of this is that the virtual ground level-shifting increases the output headroom of the system. For instance, the transducer output dc voltage is linear with respect to the detected capacitance, from 1V to 2.4V at a full scale of 2pF detecting capacitance. In comparison to other previously reported switched-capacitor transducers, another apparent merit of this topology is its simplicity by means of using a single op-amp in the front-end CV converter design, leading to a reduction in the number of components, the silicon area and power consumption, as well as relaxing the matching issues arising from the component pairs.

b) Dummy pin balancing technique

When testing the function of the high-resolution capacitive transducer, it is difficult to test small capacitance. Therefore, the dummy pin balancing topology and the lever mechanism dedicated to design for the test are proposed.

Fig. 5.2.3.2 Parasitic capacitance situation without/with reference capacitor C_{R1} and C_{R2} for balancing

As shown in Fig. 5.2.3.2 (a), the parasitic capacitance C_{PX} associated with the two IC pins of the transducer can create a significant offset effect if the sensing capacitor C_X is small. The typical value of the C_{PX} is a few hundred fF. This reduces the headroom

for the test range of C_X under a high sensitivity circuit design. In order to overcome this problem, the dummy balancing topology is proposed in Fig. 5.2.3.2 (b). As can be seen from the figure, two additional reference capacitors, C_{R1} and C_{R2} , are added to stabilize the capacitances across the pins without the dominance of the fringing field parasitic capacitances C_{PX} and $C_{PXdummy}$. This resulting capacitor network balances the associated parasitic capacitances, C_{PX} and $C_{PXdummy}$. As a result, when the capacitor network is operated in the form of a differential capacitor, the original offset value of C_{PX} is now reduced to $|C_{PX} - C_{PXdummy}|$. The capacitors C_{R1} and C_{R2} can be ensured to have a size of 1pF by matching 0.1% under careful layout. Throughout this balance design, the parasitic capacitance caused by the adjacent pins of a transducer chip is minimized significantly. This suggests that the methodology translates the single sensing capacitor structure into differential means.

c) Lever mechanism

Another test problem in realistic external capacitor measurement is the availability of minute C_x values for CV verification. For instance, precise capacitors of 2 pF and 1 pF are hardly ever found in off-the-shelf components. In order to validate the resolution of the proposed transducer, a concept of differential capacitance is proposed as follows:

$$C_X = C_X' - C_{Xdummy} \quad (5.2.3.1)$$

According to the differential concept, the actual capacitance, C_x , to be measured is the difference between C_x' and C_{Xdummy} , as illustrated in Fig. 5.2.3.1. By varying the two values from external capacitors, various minute values of differential capacitance can be synthesized for verification of the CV convertor. Besides, the capacitor C_p is internally added to emulate the very heavy parasitic capacitance in an ECT system. In the real ECT tomography application, C_x' , C_{Xdummy} and C_p

components are not required, and the actual capacitance measurement situation is illustrated in Fig. 5.2.3.3(a) and (b).

Fig. 5.2.3.3(a) Actual measurement situation of capacitors connecting to pins dedicated to design-for-test

Fig. 5.2.3.3(b) Proposed switched-capacitor network dedicated to design-for-test

In the proposed switched-capacitor design-for-test network shown in Fig. 5.2.3.3(b), the switch transistor represents M_i and the control signal Φ_{ij} represents the fact that the signal is activated during the clock ϕ_i or ϕ_j is asserted as being high. M_3 , M_4 , M_5 and M_6 are the four switches that control the charging or discharging process of C_{R1} , C_{R2} , C_X' and C_{Xdummy} . For the charge-and-discharge route, the upper terminal is connected to either analog ground or V_{ref} , while the lower terminal is always connected to the analog ground. In ϕ_1 and ϕ_2 , the upper terminal voltage is analog ground. In ϕ_3 and ϕ_4 , V_{ref} connects to the upper terminal. C_{R1} and C_{R2} are capacitors that are added intentionally for the balancing as well as the stabilization of

capacitance values across the pins, as mentioned previously. C_X' and $C_{X\text{dummy}}$ generate an equivalent differential capacitor C_X that has a target range from 2pF to the order of sub-femto. For example, in $\phi 1$, the virtual current flow sets out from the analog ground, passing by M_5 , C_{R2} and $C_{X\text{dummy}}$, C_{R1} and C_X' , M_1 , in sequence, finally sinking back to the analog ground. In this way, $\phi 1$ actually becomes a reset phase and any extra charge in capacitors is cleared up. The current flows for other working phases can be derived in a similar manner.

The other proposed method is based on the lever mechanism dedicated to design-for-test in the switched-capacitor circuit. The design equation for lever mechanism is given as follows:

$$F_1 * L_1 = F_2 * L_2 \quad (5.2.3.2)$$

where F_1 , L_1 represent the length and force, respectively in the left hand side of the lever whereas F_2 , L_2 represent the length and force, respectively in the right hand side of the lever. Following the similar concept, one can relate the total charge in the following relationship as

$$Q = C_1 \Delta V_1 = \left(\frac{1}{n} C_1\right) (n \Delta V_1) = C_2 \Delta V_2 = C_1 (V_{ag} - V_{ref1}) = C_2 (V_{ag} - V_{ref2}) \quad (5.2.3.3)$$

where the symbols have their usual meanings.

For example, the total charge for $C_X=1\text{fF}$ with 1V differential voltage is equal to the total charge for $C_X=1\text{pF}$ with 1mV differential voltage according to (5.2.3.13). Based on this theory, several conservation charge equations from the CV converter can be established as follows:

$$\Delta V_{\text{out}} C_f = (V_{\text{out},\phi 4} - V_{\text{out},\phi 2}) C_f = C_{X\text{-actual}} (V_{\text{ang}} - V_{\text{ref-actual}}) = C_{X\text{-virtual}} (V_{\text{ang}} - V_{\text{ref-virtual}})$$

(5.2.3.4)

By varying the external V_{ref} value, the $\Delta V = (V_{\text{ang}} - V_{\text{ref}})$ can be easily controlled. The reason to do so is to enable the test on the resolution of the transducer chip because the minimum C_x values can reach 1fF or even less and it is difficult to acquire such small values from the off-the-shelf components. Through the lever mechanism of charge, it is able to test the small capacitance change through the change in the small differential voltage based on the level mechanism concept. More importantly, this voltage difference, such as in the 1mV example, is feasible for practical measurements.

5.2.3.2 Four working phases

The CV convertor works like a switched-capacitor gain amplifier with two embedded sample-and-hold circuits arranged to operate in multiple cyclic operations. It is operated at four different phases in one single measurement cycle to process and output the measurement result of the detected capacitance. Table 5.2.3 summarizes the status of all the switches and circuit operation modes on the basis of the complete transducer circuit shown in Fig. 5.2.3.1 in the four phases.

TABLE 5.2.3 THE STATUS OF ALL SWITCHES AND CIRCUIT AT FOUR WORKING PHASES

phase	M ₁	M ₂	M ₃	M ₄	M ₅	M ₆	Circuit Mode
$\phi 1$	ON	OFF	OFF	ON	ON	OFF	Reset
$\phi 2$	ON	OFF	ON	OFF	OFF	ON	S/H
$\phi 3$	OFF	ON	OFF	ON	ON	OFF	Reset
$\phi 4$	OFF	ON	ON	OFF	OFF	ON	S/H
phase	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	Input voltage
$\phi 1$	ON	ON	OFF	OFF	OFF	OFF	V_{ang}

$\phi\ 2$	OFF	OFF	OFF	ON	OFF	ON	V_{ang}
$\phi\ 3$	ON	ON	OFF	OFF	OFF	OFF	V_{ref}
$\phi\ 4$	OFF	OFF	ON	OFF	ON	OFF	V_{ref}

The four operation phases are given as follows: $\phi 1$ is the reset phase for analog ground, $\phi 2$ is error sampling phase, $\phi 3$ is reset phase for reference voltage input, and $\phi 4$ is signal plus error measurement phase.

The simplified topologies of the CV convertor in the different phases are illustrated in Fig. 5.2.3.4. In phase $\phi 1$, the CV convertor samples the amplifier’s dc offset and 1/f noise. In phase $\phi 2$, the dc offset and 1/f noise are subtracted by the CDS action while the switch error is simultaneously sampled and stored in the S/H 1 circuit. In phase $\phi 3$, the CV convertor samples the amplifier’s dc offset and 1/f noise again but the measurement capacitor C_x is charged up for charge transfer in the next clock phase. In phase $\phi 4$, the CV convertor transforms the measured capacitance to voltage and stores it in the S/H 2 circuit while the non-ideal switch errors are maintained as being similar to those in S/H 1. It is noted that the CDS structure does not translate any offset or 1/f noise of the amplifier to the S/H circuits. The final error sources come from the switch errors. These S/H circuit outputs are further processed to obtain a quality signal for the final measurement result.

Fig. 5.2.3.4 Simplified circuit topologies at four working phases: ϕ_1 , ϕ_2 , ϕ_3 and ϕ_4

The four separated phases are: ϕ_1 is reset phase, ϕ_2 is switch error sample and hold phase, ϕ_3 is reset phase with reference voltage ready for next phase of capacitance measurement, and ϕ_4 is signal and switch error sample and hold phase.

During ϕ_1 , M1, M4, M5, S4, and S5 remain closed whilst other switches remain open. C_X and C_f are connecting between analog ground and virtual analog ground. The $1/f$ noise and dc offset of amplifiers are sampled to both the capacitors.

During ϕ_2 , M1, M3, M6, S7 and S9 close. The charge transfer process in the CDS structure subtracts the $1/f$ noise and dc offset components that are sampled from ϕ_1 but the switch error of the circuit is referred back to the hold capacitor C_{h1} when the switch S5 turns off. The transfer function of this gain amplifier is

$$v_{out,\phi_2}' = \left(\frac{C_X' + C_{R1} - C_{Xdummy} - C_{R2}}{C_f} \right) \Delta V_{in,\phi_2} + \Delta_{\phi_1} \approx \left(\frac{C_X}{C_f} \right) (V_{ag} - V_{ag}) + \Delta_{\phi_1} = \Delta_{\phi_1} \quad (5.2.3.5)$$

$$\text{where } \Delta_{\phi_1} \approx V_{cf,\phi_1} + V_{ch,\phi_1} \quad (5.2.3.6)$$

Here, $V_{out,\phi 2}$ denotes the output of the main op-amp output. It is also assumed that the gain error of the op-amp is negligible for a very high open-loop gain op-amp. C_X is the equivalent model of external measurement capacitance. C_f is the feedback capacitance, which is 10 pF in this design. $\Delta_{\phi 1}$ represents the lumped circuit error arising from the switching action that originated from the circuit level charge injection $V_{ch,\phi 1}$ error and the circuit level clock-feedthrough error $V_{cf,\phi 1}$ from the previous phase $\phi 1$. However, when S7 and S9 change from ON to OFF at the end of $\phi 2$, the switch channel charge as well as clock-feedthrough error arising from the switch S7 cause an additional switch error to C_{h1} . The error from S9 is negligible because the buffer has a low output impedance. This leads to

$$V_{out,\phi 2} = \Delta_{\phi 1} + \Delta_{\phi 2} \quad (5.2.3.7)$$

$$\text{where } \Delta_{\phi 2} \approx V_{cf,\phi 2} + V_{ch,\phi 2} \quad (5.2.3.8)$$

As a result, C_{h1} holds the summing switch errors which will be used for the subsequent subtracting operation at $\phi 4$. The source-follower based buffer inside the feedback loop drives the CHSDDA with this error voltage.

During $\phi 3$, the circuitry resets again. M2, M4, M5, S4 and S5 are close. The only difference between $\phi 1$ and $\phi 3$ is that C_X is now connecting to V_{ref} , which is absolute ground (0V). The charge stored in C_X becomes $C_X \times (V_{ag} - 0)$. In this phase, the 1/f noise and dc offset of amplifiers are sampled again to both the capacitors.

During $\phi 4$, M2, M3, M6, S6 and S8 are close. The charge transfer process in the CDS structure subtracts the 1/f noise and dc offset components that are sampled from the previous $\phi 3$ but the switch error of the circuit is referred back to the hold capacitor C_{h2} when the switch S5 turns off. The transfer function of this gain amplifier is similar with (5.2.3.2). Substituting ΔV_{in} with $(V_{ag} - V_{ref}) = (V_{ag} - 0)$, we obtain

$$v'_{out,\phi4} = \left(\frac{C_X' + C_{R1} - C_{Xdummy} - C_{R2}}{C_f} \right) \Delta V_{in,\phi4} + \Delta_{\phi3} \approx \left(\frac{C_X}{C_f} \right) (V_{ag} - V_{ref}) + \Delta_{\phi3} \quad (5.2.3.9)$$

$$\Delta_{\phi3} \approx V_{cf,\phi3} + V_{ch,\phi3} \quad (5.2.3.10)$$

where the symbols have their usual meanings. Herewith, it is also assumed that the amplifier has a very large open-loop gain to minimize the contribution from finite gain error of op-amp. At the end of $\phi4$, when S6 and S8 changes from ON to OFF, the additional switch channel charge as well as clock-feedthrough error arising from S6 cause C_{h2} to hold the lumped error plus the signal as follows:

$$v_{out,\phi4} \approx \left(\frac{C_X}{C_f} \right) (V_{ag} - V_{ref}) + \Delta_{\phi3} + \Delta_{\phi4} \quad (5.2.3.11)$$

$$\Delta_{\phi4} \approx V_{cf,\phi4} + V_{ch,\phi4} \quad (5.2.3.12)$$

It is noted that the error from S8 is negligible because of the low-impedance of second source follower buffer. This buffer inside the feedback loop drives another input of CHSDDA with this signal and error.

Finally, the subtraction function operates at the two input terminals of CHSDDA. It gives the following:

$$V_{out,\phi4} - V_{out,\phi2} = \left(\frac{C_X}{C_f} \right) (V_{ag} - V_{ref}) + \Delta_{\phi3} + \Delta_{\phi4} - \Delta_{\phi1} - \Delta_{\phi2} \quad (5.2.3.13)$$

After amplifying by the precision CHSDDA, the final output of the ECT transducer is

$$V_{out} = \left(\left(\frac{C_X}{C_f} \right) (V_{ag} - V_{ref}) + \Delta_{\phi3} + \Delta_{\phi4} - \Delta_{\phi1} - \Delta_{\phi2} \right) \left(1 + \frac{R_2}{R_1} \right) \quad (5.2.3.14)$$

Viewing from the final dc output voltage shown in (5.2.3.14), it is obvious that the non-ideal sources tend to cancel each other to yield a final residual term

$$\Delta_{\varphi 3}+\Delta_{\varphi 4}-\Delta_{\varphi 1}-\Delta_{\varphi 2} .$$

5.3 Building Blocks Design

5.3.1 Main Op-amp Design

The op-amp serves as the main core of the CV converter and its performance dictates the ECT system performance. Design concerns are addressed by several critical op-amp parameters. The op-amp must be carefully designed to meet the necessary requirements.

Fig. 5.3.1 Designed high gain two-stage main op-amp

Fig. 5.3.1 shows the simplified schematic of the circuit architecture of the op-amp. Since an inverting amplifier configuration is used in the capacitive transducer topology, the input common mode range is relaxed. Therefore, the input cascode differential stage is employed in conjunction with a second class-A inverting cascode amplifier for high-swing output. The complete amplifier can achieve a very high gain with only two gain stages. This not only benefits the reduction of the gain error of the op-amp, which is favorable for instrumentation based applications, but also improves the common mode rejection ratio under a very high differential gain and

permits a fast-settling op-amp design. Moreover, the cascode frequency compensation technique using the current mirror structure [P. R. Gray, 2001] is employed. The main reasons for this are (i) to have wide unity gain-bandwidth for fast settling while consuming low power for driving a reasonable capacitive load (ii) to obtain a high power supply rejection ratio (PSRR) because the op-amp is operated in a mixed-signal environment and (iii) to obtain better noise performance in comparison to other types of cascode compensated amplifiers [B. K. Ahuja, 1983] because it suffers from a higher amount of noise arising from the current source in the current buffer. Since the switched-capacitor CDS is applied for the front-end CV converter, the flicker noise effect is of little concern but the thermal noise should be made low.

5.3.2 Chopping DDA Design

Fig. 5.3.2 Simplified schematic of a single-ended chopping DDA

Fig. 5.3.2 shows the circuit schematic of a single-ended chopping DDA based on previous work [P. K Chan, 2004]. Each input port of DDA is identically designed (M_1 , M_2 , M_5 and input chopping switch network S_1 , or M_1' , M_2' , M_5' and S_1'). The floating input signals are transposed to the chopping frequency through the two input chopping switch networks, S_1 and S_1' while the differential pairs $M_1'-M_2'$ and M_1-M_2 simultaneously perform the V-I conversion at a high frequency. First stage

gain is achieved by I-V conversion in the active load formed by transistors M3-M4 and M6-M9. Through the use of chopper S2, the signal is demodulated back to the baseband frequency but the $1/f$ noise, input common error and dc offset of the first stage are simultaneously shifted to a high frequency. The recovered signal is further amplified by the next two-stage amplifier (M₁₀-M₁₆). A source follower (M₁₇-M₁₈) is added in to improve the driving ability of the external loading.

CHAPTER 6

6 DIGITAL CONTROL LOGIC DESIGN

6.1 Control Functions

In order to control the whole CV convertor and ensure that it is working correctly under different operation modes and cycles, a digital control logic block is required. Basically, the working principle of the digital control logic block is to generate many non-overlapping clocks at different frequencies based on one pair of non-overlapping clocks, i.e., the chopping and the non-chopping clocks. Fig. 6.1.1 shows all the waveforms of the final output signals from the digital to the analog section for the full control of every operation.

Fig. 6.1.1 Waveforms of clocks generated according to defined period of the system

Firstly, one pair of non-overlapping clocks, the chopping clock and the non-chopping clock, are generated based on the input of the main frequency to control the chopping DDA, and are named V_{chop} and V'_{chop} . There are other two pairs of non-overlapping clocks. One pair is ϕ_{13} and ϕ_{24} , and the other pair is ϕ_{12} and ϕ_{34} . All of these are illustrated in Fig. 6.1.1.

In addition, the digital control logic generates hold non-overlapping clocks, ϕ_{1hold} , ϕ_{2hold} , ϕ_{4hold} and ϕ_{13hold} , which are the AND results of clocks and the system S/H signal. Apparently, they are non-overlapping signals and used in the feedback gain loop of the CV convertor. The S/H signal is used to govern the measurement cycle and the data transfer cycle. The digital logic is built up basically by delay cell, inverters, AND gate, OR gate, XOR gate, D flip-flop and the power-on circuit.

The T stands for a period to complete a four-phase operation for the switched-capacitor transducer, which is fixed at $100\ \mu\text{S}$. A complete sample-and-hold cycle consists of three T s, with the first sample phase dedicated to sampling and measurement while the two subsequent hold cycles are dedicated to holding the measurement data for data acquisition. Within a $300\ \mu\text{S}$ time frame, the system completes a whole capacitive measurement procedure, including one capacitance signal sampling and signal conversion from C to V in first T time and holding it in second $2T$ time for the signal processing done by the data acquisition card in the ECT tomography system. The slow changing speed of the external capacitance of the ECT application relaxes the requirement of the chopping frequency of the chopping DDA. In this design, $80\ \text{kHz}$ is chosen as the main chopping frequency of the chopping DDA. Based on the master frequency, ϕ_{13} and ϕ_{24} become $40\ \text{kHz}$ signals, and ϕ_{12} and ϕ_{34} become $20\ \text{kHz}$ signals.

Fig. 6.1.2 Digital control logic design

Referring to Fig. 6.1.2, the whole digital control logic design is introduced in the following. There are two input signals in the logic generator, the 80 kHz main clock ϕ_0 and the control signal. They are used for control of the sampling and holding actions of the system for verification of the functionality of the transducer. The 80 kHz main clock could be generated from an external instrument or an internal oscillator. For the sake of flexibility, ϕ_0 is obtained from an external frequency generator through a pin. The main frequency goes through a two-phased non-overlapping block first in order to generate two 80 kHz non-overlapping chopping signals for two choppers of the chopping DDA. The chopping signal is then divided by a D flip-flop to yield a 40 kHz signal for further processing. Based on this 40 kHz signal, a non-overlapping clock generator produces two-phased non-overlapping clocks. The first is further divided to get a 20 kHz signal which supplies to three subsequent blocks simultaneously. There are three purposes for generating the 20 kHz signal. The first is to generate the system sample-and-hold signal together with an external control signal called “Control”. This sample-and-hold signal generator is elaborated upon in Section 6.2.4. The second purpose is to generate two-phased non-overlapping clocks called ϕ_{12} and ϕ_{34} . The third is to generate other controlling signals together with the help of a 40 kHz clock through a gate logic module that consists of AND, OR, INV, delay, as well as the aforementioned S/H signal. The input “Control” ultimately provides a master enable function for controlling clock signals to the whole CV convertor. Finally, one master clock, eight

controlling clocks and one control signal are used in the SC system.

6.2 Logic Circuits

6.2.1 Two-phased non-overlapping clock generator

As discussed above, the non-overlapping clocks are essential to the control signal generator. They determine when charge transfers occur and they must be carefully designed to be able to realize the non-overlapping period in order to guarantee that the charge is not inadvertently lost or causes severe open-loop or a false action on the part of the analog section. The simplest way to generate two non-overlapping clocks is shown in Fig. 6.2.1. Here, the delay blocks are used to ensure that the clocks remain non-overlapping and to determine the slot time for how long they are non-overlapping. ϕ_0 is the main frequency of the system, which is an 80 kHz square wave with a 50% duty cycle. The generated ϕ_1 and ϕ_2 are both also 80 kHz square waves with a near 50% duty cycle, but at no time are both signals high.

Fig. 6.2.1 Circuit implementation of two non-overlapping clocks from a single clock

6.2.2 Power-on reset circuit

There are always two possible output states of D flip-flop initially. To guarantee the beginning state of the digital logic, a start-up circuit as shown in Fig. 6.2.2 must be provided. The NMOS functions as a capacitor when its source and drain terminals are shorted and connected to the ground, which saves the area compared with its poly counterpart. The PMOS is biased to act as a resistor. When the circuit is powered up, the gate capacitor of the NMOS will be charged up. When the gate capacitor is charged to a certain potential, the NMOS of the inverter begins to operate and the output voltage of the power-on reset circuit is forced to be low. This single pulse causes the D flip-flop to be reset and consequently start.

Fig. 6.2.2 Power-on reset circuit for digital logic start up

6.2.3 D Flip-flop

Fig. 6.2.3 D flip-flop with reset terminal

Fig. 6.2.3 shows the D flip-flop with reset terminal. A few D flip-flop blocks are utilized in the digital control logic to divide the provided signal to a half frequency signal. The reset signal comes from the power-on reset block and provides a clean up and start up for the whole digital logic which includes the D flip-flops.

6.2.4 System Sample-and-hold Signal Generator

Fig. 6.2.4 Sample-and-hold signal generator and the generated S/H signal

Fig. 6.2.4 shows the system sample-and-hold signal generator having a S/H monitoring signal. It is a waveform with 300 μ s cycle and 1/3 duty cycle as indicated by the “S/H” signal. The generator is driven by the output clock of the second divider. The system sample-and-hold signal generator is used to sample the measured result from the CV converter through a form of DC voltage (during S/H High) and hold the sampled DC voltage for a certain period (during S/H Low) for further back-end processing. Under normal operations, the “Control” input is applied with logic 1, which is 3V. For the system reset, the “Control” input is applied with logic 0, which is

0V.

CHAPTER 7

7 LAYOUT CONSIDERATIONS

7.1 Mixed-signal Layout Issues

When design considerations for circuits and systems are finalized and circuits are validated through realistic transistor-level simulations, the layout of circuits and systems should be addressed along with the circuit design work, with the philosophy of “design for layout” and “design for manufacture”. The proper layout ensures that circuits sustain performance or maximize the IC yield after manufacture since there are many pitfalls in the practical fabrication environment in the context of process variation, the matching characteristic, parasitic effects, etc. A properly planned layout plus layout techniques form the basis for a successful prototype. This aims to maintain the realistic results as much as possible to the circuit designers in the phase of post-layout simulation. For the mixed-signal CV transducer that is applied in the tomography field, the critical factors such as noise coupling, matching and the system floor plan are important considerations for the layout.

7.1.1 Low Noise

The digital clock generator generates four-phase non-overlapping control clocks and other control signals for measurement, advanced controlling clocks, and so on. The digital part is naturally prone to being highly noisy because of its switching frequency. This kind of noise does not affect the function of the digital part itself as the digital circuit normally has a good level of toleration to noise. However, if this noise is not isolated from the analog blocks, it easily degrades the system performance since

resolution is of primary concern. The high frequency digital noise couples to the analog section from the power supply, common substrate and control signal lines.

Fig. 7.1.1.1 Guard ring arrangement for analog and digital sections (not according to scale)

There are several layout methods for minimizing the influences of these three types of coupling sources. In order to block digital noise from being injected into a highly sensitive analog core from the common P substrate, they should be kept away from each other as far as possible. A guard ring circles each part for isolation as shown in Fig. 7.1.1.1. A guard ring consists of a few parallel n and p type power contact lines, in which p-substrate contacts are connected to the absolute ground and N well contacts are connected to the highest voltage in the circuit (V_{DD} here). This improves immunity to parasitic diode current leakage.

Fig. 7.1.1.2 Cross section of guard ring

Fig. 7.1.1.2 shows the cross section of a guard ring. If the process has a deep N well, or if a few more parallel rings are used, the overall effect would be better. This guard ring shielding method is also applied to all the switch transistors. This is mainly

because the comparatively high digital control signal frequencies would otherwise impact on other parts of the analog section through these switch transistors.

The second source of noise coming into the analog section is the power supply. This is because the noise of the digital section refers back to the power supply and ground. If the analog part shares the power supply and ground with the digital part, the noisy power would be already large enough to limit system resolution. It is thus preferable to use a separate power supply for the digital and analog sections. The supplies are VDDD (digital power), VSSD (digital ground), VDDA (analog power) and VSSA (analog ground). They should be connected to each individual pad, and their widths depend on the total current in the worst situation. Furthermore, full attention should be paid to the locations of the pins for the four power supplies.

In addition, in order to shield sensitive lines, an intermediate metal layer is chosen to transfer sensitive signals, and the upper and lower metal layers are grounded to shield this intermediate layer. Through this means, the intermediate signal is fully isolated from the external environment. Fig. 7.1.1.3 provides an exemplary case.

Fig. 7.1.1.3 Shielding sensitive line with neighbor lines

7.1.2 Matching

Matching is another critical issue for the high precision analog circuit layout. Many circuit building blocks require precise matching, such as current mirrors, input differential pairs, current mirror active load, and so on. In order to reduce the mismatching offset due to the fabrication process as much as possible, an interdigitized technique in conjunction with a common-centroid technique is utilized for the critical matched component pair, differential pair, and so on. Fig. 7.1.2 provides a sketch map of an exemplary symmetrical layout technique. Devices 1 and 2 are interleaved at the top, and are ordered in reserve at the bottom. This provides independence of process in one gradient direction. In order to reduce the lateral etching effect, dummy transistors are added on both sides.

Fig. 7.1.2 Sketch map of common-centroid layout

Moreover, the common-centroid technique is also adopted for the matching of passive devices such as resistors and capacitors. The precise ratio of some resistors and capacitors is critical for ensuring system accuracy and dc offset.

7.2 Floor Planning and Chip Layout

Based on the preceding layout considerations and careful arrangement of the whole architecture, the top-level floor plan of the CV convertor is illustrated in Fig. 7.2.

Fig. 7.2 Floor plan of the CV convertor

The critical issues to be addressed include the routing of the critical path, the floor plan and isolation of the power supplies and ground, decoupling of the noise of the digital section to the analog section. The floor plan employs mixed-signal layout techniques to minimize the digital signals from disturbing the sensitive analog signals, as discussed previously. In addition, the floor plan of the CV convertor is highly relative to the PADs arrangement and placement, as well as the input/output signals routing. It serves as an indication for the placement, location, shape and dimension of every building block during the entire layout process. In the floor plan, the digital section is arranged at the bottom-left, with an input main clock signal and output the generated control clocks which are distributed to the rest of the mixed-signal blocks. Finally, the analog signals are arranged at the right-most end of the floor plan.

7.2.1 Star Layout

Another key issue is the distribution of power and the ground in the layout. When the power and ground are not distributed properly, noise can be coupled from the digital part into the analog part. Fig. 7.2.1 shows the star layout methodology of the power buses. Between the power buses, the cells draw power naturally from the top V_{dd} and bottom V_{ss} .

Fig. 7.2.1 Star layout of power and ground

7.2.2 Arrangements of PADs and pins

Fig. 7.2.2.1 PADs and pins layout arrangements

The signals paths are arranged to be compatible with PADs and pins as shown in Fig. 7.2.2.1. Table 7.2.2 lists the pin functions associated with the DIP 28 package of the test chip as shown in Fig. 7.2.2.2.

TABLE 7.2.2 SUMMARY OF PIN FUNCTION

Pin no.	I/O	Name	Function
I1	Input	CP	main frequency digital signal
I2	Input	V _{ddd}	power supply of digital section
I3	Input	V _{ssd}	ground of digital section (0V)
I4	Input	V _{dda}	power supply of analog section
I5	Input	V _{ssa}	ground of analog section (0V)
I6	Input	V _{ref}	reference voltage
I7	Input	C _{x-}	negative terminal of external measured capacitor
I8	Input	C _{x+}	positive terminal of external measured capacitor
I9	Input	C _{x-} dummy	dummy negative terminal of external measured capacitor for balance
I10	Input	Control	system sample-and-hold control input
I11	Input	V _{ang}	analog ground (1V)
O1	Output	V _{out}	output voltage
O2	Output	S/H	system sample-and-hold monitoring signal

Fig. 7.2.2.2 Pin arrangement of the capacitive transducer chip

In order to facilitate the connection of off-chip decoupling capacitors as quickly as possible, a decoupling capacitor can be placed between I2 and I3 close to each other. As resolution and stability are crucial for the successful use of this application, noise isolation of the power and ground have also been considered in this aspect of the pin and pad package. The common method utilized to suppress interruptions between the analog and digital sections is to use a separate pad and pin. As shown in Fig. 7.2.2.2, I4 and I5 (V_{dda} and V_{ssa}) are far way from I2 and I3 (V_{ddd} and V_{ssd}). All of the supply pins are far away from the other signal lines. The separate capacitive decoupling capacitor is illustrated in Fig. 7.2.2.3.

Fig. 7.2.2.3 Separate pin and pad arrangement for digital and analog power

CHAPTER 8

8 RESULTS AND DISCUSSIONS

In order to verify the proposed instrumentation based SC methodology, resistance balancing methodology and new designs of the sample-and-hold circuit, the chopper-stabilized amplifiers and capacitive transducer on the basis of the respective methodology, a series of simulation and experimental results are presented and discussed. Finally, a comparison is made to show the performance of the proposed monolithic capacitive transducer with respect to that of the prior art works. Prior to the presentation, a list of equipment used to evaluate the integrated circuit prototypes is provided in Table 8.1.

TABLE 8.1 INSTRUMENTS USED TO EVALUATE THE IC PROTOTYPES

Experimental instrument	Model and specifications
Power supply	Hewlett Packard E3631A 0-6V, 5A / 0-+/-25V, 1A Triple Output DC power supply
Precision Digital Multimeter	Hewlett Packard 34401A
Multimeter for rough Cx detection	Metex M-3650CR
Function Generator	Stanford Research Systems DS360 ultra low distortion function generator
Oscilloscope	Hewlett Packard 54645D 100MHz 2.+16 channels Mega Zoom Mixed Signal Oscilloscope
Precision capacitor measurement meter	Meguro Electronics Corp. VHF Q meter MQ-171
FFT network analyzer	Stanford Research Systems Model SR770 FFT network analyzer

8.1 Instrumentation-based SC S/H Circuit

In order to evaluate the system performance, the transistor-level HSPICE simulation was carried out using realistic BSIM3 model parameters of AMS 0.6 μm CMOS process. The specified parameters for simulation are listed in Table 8.1.1.

In response to the 1.0Vpp 1 kHz input sine wave signal, the simulated output responses of the conventional S/H circuit and the proposed S/H circuit are illustrated in Fig. 8.1.1. It is noted that the aspect ratio is $10\mu\text{m}/0.6\mu\text{m}$ for each main switch transistor in parallel bootstrap switch topology and $20\mu\text{m}/0.6\mu\text{m}$ for normal bootstrap switch transistor under identical on-resistance implementation. The typical hold errors are obtained as 0.2 mV and 2.3 mV respectively from the zoom-in views in Fig. 8.1.1. It can be seen that the precision of the proposed S/H circuit is one order better than the conventional S/H circuit.

TABLE 8.1.1 SPECIFIED SIMULATION PARAMETERS

Parameter	Value
Power Supply	+5 V
Holding Capacitor	10 pF
Input Signal Frequency	1 kHz
S/H Frequency	10 kHz
Chopping Frequency	20 kHz

(a) the proposed S/H

(b) the conventional S/H

Fig. 8.1.1 Simulated output response of the two S/H circuits

For accessing the immunity to op-amp offset error, an intentional 5mV offset is added in series with the input of the op-amp in Fig. 5.2.1.1 and Fig. 5.2.1.2, respectively. Besides, another intentional 5mV offset is also inserted in one of the buffers so as to create a 5mV offset difference between the buffer pair in Fig. 5.2.1.2. As can be seen from the simulation results in Fig. 8.1.2, the output voltage of the proposed circuit is almost close to ideal response whereas the prior-art circuit deviates from the ideal

response with the offset error. Hence, it is confirmed that the proposed circuit is independent of the mismatch offset of the op-amp and the buffer pair.

Fig. 8.1.2 Comparison of offset effect in the two S/H circuits

Fig. 8.1.3 Comparison of temperature drift in the conventional and proposed S/H circuits using identical parallel bootstrap switch

Fig. 8.1.4 Comparison of temperature drift using different switches in the proposed S/H circuit

TABLE 8.1.2 PERFORMANCE COMPARISON

Parameter	Conventional S/H	Proposed S/H
Holding Error (mV)	2.3	0.2
Temperature Drift (uV/°C)	27.46	0.846

For a constant 2.5V dc input, the output voltages of the two topologies versus variation of temperature from -40°C to 90°C are illustrated in Fig. 8.1.3. Further comparison in Fig. 8.1.4 has revealed that the proposed S/H circuit exhibits the lowest temperature drift when using parallel bootstrap switch topology. Table 8.1.2 summarizes the performances of the conventional and the proposed work. Hence, the simulation result has validated that the proposed circuit technique, which makes use of proposed instrumentation SC method, AZ process, parallel bootstrap switch and CHSDDA, can achieve highly stable dc output voltage against broad range of temperature. The characteristic of low temperature drift offers significant performance improvement in the context of S/H circuit design in integrated transducers. As a final remark, the instrumentation SC circuit technique in this S/H circuit can be applied to the design of capacitive transducer. The measurement results of which will be further discussed in Chapter 8, section 8.3.

8.2 Resistance-Balanced Chopper-Stabilized Amplifiers

8.2.1 Calculation and Simulation Results of the Input-referred Errors in Chopping Amplifiers

The simulation topologies are based on Fig. 4.3.1. and Fig. 4.3.2, with the assumption that R_S is much smaller than R_b whereas the analog ground output resistance is negligible small in comparison to R_1 and R_2 , $C_{ps} = 5$ pF and $C_p = 3$ pF. Table 8.2.1.1 illustrates two exemplary cases of the devices random mismatch in each type of amplifier, with ± 5 mV for the threshold voltages in the input choppers S_1 , S_1' , differential pairs M_1-M_2 , $M_1'-M_2'$ and active load transistor pairs M_3-M_6 , based on 2.5V V_Q and small input signal. All the mismatches of aspect ratios in the critical matching pairs are assumed with $\pm 2\%$ except that of $\pm 5\%$ for the input choppers that deal with small transistor size. For a closed-loop gain factor of 10, with a choice of $R_1 = 1$ k Ω , $R_2 = 9$ k Ω , $C_L = 25$ pF and the assumption of $R_b \gg R_s$, we can find that $R_3 \approx R_b \approx 1$ k Ω from (5.2.1)-(5.2.2). Therefore, using (5.1.1.1)-(5.1.1.5) and typical values of process and design parameters for computation in MATLAB, the charge split ratio for 1 k Ω is 60.4% in the chopping op-amp, whereas in the chopping DDA, the charge split ratio is 60.4% for 1 k Ω and 35.7% for negligible source resistance value of analog ground reference. Starting from -50 mV with respect to an analog ground reference 2.5 V, an incremental input step of 10 mV dc was applied to each circuit until +50 mV. The dc output of each amplifier was extracted using a 150 Hz RC low-pass filter under a chopping clock frequency of 64 kHz. This ensures harmonics as well as high-frequency noise are rejected substantially. Using realistic Level 49 BSIM3 model from AMS 0.6 μ m CMOS process and a single supply of 5V, the simulated equivalent input-referred errors of each amplifier were obtained against different output voltages in Fig. 8.2.1.1 and Fig. 8.2.1.2, respectively. As can be observed, the predicted results are close to the simulation results. Mismatch effect in

chopping amplifiers deteriorate the dc precision. Improving matching of critical transistor matching pair will reduce the dc offset. The DDA suffers from relatively higher dc offset than the op-amp counterpart because of the increase in complexity. Refer to the calculated results in Table 8.2.1.2 and Table 8.2.1.3, the contributions arising from the charge injection (V_{ch_eff}), clock feedthrough (V_{cf_eff}) and finite gain error (ΔV_e) are summed to obtain the equivalent input-referred error, which gives the insight on how individual error source makes an impact to the final error. Since the estimated equivalent input-referred error is close to the simulation result, it has confirmed that other error sources such as dc offset and dc common-mode error are suppressed effectively. This also validates the dominant error source models as discussed above. In order to predict the effectiveness of the proposed technique, the same simulations without R_b are done for both chopping op-amp and DDA. Fig. 8.2.1.3 and Fig. 18.2.1.4 show the respective comparative simulation result. It can be seen that there are about 2 to 3 times in improvement on the dc offsets.

Fig. 8.2.1.1 Input-referred error of the chopping op-amp

Fig. 8.2.1.2 Input-referred error of the chopping DDA

Fig. 8.2.1.3 Simulated input-referred errors of the balanced and unbalanced chopping op-amp

Fig. 8.2.1.4 Simulated input-referred errors of the balanced and unbalanced chopping DDA

TABLE 8.2.1.1 SIMULATION PARAMETERS FOR EXEMPLARY MISMATCHED CASES

Parameter Variation	Chopping Op-amp Case 1	Chopping Op-amp Case 2	Chopping DDA Case 1	Chopping DDA Case 2
Vth,S1-M1	-5 mV	+5 mV	-5 mV	+5 mV
Vth,S1-M2	+5 mV	-5 mV	+5 mV	-5 mV
Vth,S1-M3	-5 mV	+5 mV	-5 mV	+5 mV
Vth,S1-M4	+5 mV	-5 mV	+5 mV	-5 mV
Vth,S1'-M1	-	-	+5 mV	-5 mV
Vth,S1'-M2	-	-	-5 mV	+5 mV
Vth,S1'-M3	-	-	-5 mV	+5 mV
Vth,S1'-M4	-	-	+5 mV	-5 mV
(W/L)M1	-2%	+2%	-2%	+2%
(W/L)M2	+2%	-2%	+2%	-2%
(W/L)M1'	-	-	+2%	-2%
(W/L)M2'	-	-	-2%	+2%
(W/L)S1-M1	-2%	+2%	-2%	+2%
(W/L)S1-M2	+2%	-2%	+2%	-2%
(W/L)S1-M3	+2%	-2%	+2%	-2%
(W/L)S1-M4	-2%	+2%	-2%	+2%
(W/L)S1'-M1	-	-	+2%	-2%
(W/L)S1'-M2	-	-	-2%	+2%
(W/L)S1'-M3	-	-	-2%	+2%
(W/L)S1'-M4	-	-	+2%	-2%

TABLE 8.2.1.2 CALCULATION OF INDIVIDUAL INPUT-REFERRED ERROR IN CHOPPING OP-AMP AND COMPARISON OF THE SUMMED ERRORS WITH SIMULATED RESULTS

Input voltage (V)	Ideal Output Voltage (V)	Mismatch Case 2		No mismatch		Mismatch Case 1	
		Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)
2.55	3.0	$V_{\text{ch\_eff}}$: 29.6 $V_{\text{cf\_eff}}$: -23 ΔV_{ϵ} : -6.3 total : 0.3	1	$V_{\text{ch\_eff}}$: 0 $V_{\text{cf\_eff}}$: 0 ΔV_{ϵ} : -6.3 total : -6.3	-5.1	$V_{\text{ch\_eff}}$: -27.8 $V_{\text{cf\_eff}}$: 23 ΔV_{ϵ} : -6.3 total : -11.1	-10.8
2.52	2.7	$V_{\text{ch\_eff}}$: 24.6 $V_{\text{cf\_eff}}$: -23 ΔV_{ϵ} : -2.5 total : -0.9	-0.4	$V_{\text{ch\_eff}}$: 0 $V_{\text{cf\_eff}}$: 0 ΔV_{ϵ} : -2.5 total : -2.5	-2.4	$V_{\text{ch\_eff}}$: -24.3 $V_{\text{cf\_eff}}$: 23 ΔV_{ϵ} : -2.5 total : -3.8	-4.5
2.5	2.5	$V_{\text{ch\_eff}}$: 15.9 $V_{\text{cf\_eff}}$: -23 ΔV_{ϵ} : 0 total : -7.1	-7.2	$V_{\text{ch\_eff}}$: 0 $V_{\text{cf\_eff}}$: 0 ΔV_{ϵ} : 0 total : 0	0.55	$V_{\text{ch\_eff}}$: -15.9 $V_{\text{cf\_eff}}$: 23 ΔV_{ϵ} : 0 total : 7.1	7.6
2.48	2.3	$V_{\text{ch\_eff}}$: 13.8 $V_{\text{cf\_eff}}$: -23 ΔV_{ϵ} : 2.5 total : -6.5	-6.9	$V_{\text{ch\_eff}}$: 0 $V_{\text{cf\_eff}}$: 0 ΔV_{ϵ} : 2.5 total : 2.5	2.1	$V_{\text{ch\_eff}}$: -14 $V_{\text{cf\_eff}}$: 23 ΔV_{ϵ} : 2.5 total : 11.5	11
2.45	2.0	$V_{\text{ch\_eff}}$: 12.8 $V_{\text{cf\_eff}}$: -23 ΔV_{ϵ} : 6.3 total : -3.9	-5	$V_{\text{ch\_eff}}$: 0 $V_{\text{cf\_eff}}$: 0 ΔV_{ϵ} : 6.3 total : 6.3	5.2	$V_{\text{ch\_eff}}$: -14.2 $V_{\text{cf\_eff}}$: 23 ΔV_{ϵ} : 6.3 total : 15.1	14

TABLE 8.2.1.3 CALCULATION OF INDIVIDUAL INPUT-REFERRED ERROR IN CHOPPING DDA AND COMPARISON OF THE SUMMED ERRORS WITH SIMULATED RESULTS

Input Voltage (V)	Ideal Output voltage (V)	Mismatch Case 2		No mismatch		Mismatch Case 1	
		Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)
2.55	3.0	$V_{\text{ch\_eff}}: 56.5$ $V_{\text{cf\_eff}}: -46$ $\Delta V_{\epsilon}: -5$ total : 5.5	6.9	$V_{\text{ch\_eff}}: 0.8$ $V_{\text{cf\_eff}}: 0$ $\Delta V_{\epsilon}: -5$ total : -4.2	-5.2	$V_{\text{ch\_eff}}: -55.5$ $V_{\text{cf\_eff}}: 46$ $\Delta V_{\epsilon}: -5$ total : -14.5	-13.2
2.52	2.7	$V_{\text{ch\_eff}}: 49.3$ $V_{\text{cf\_eff}}: -46$ $\Delta V_{\epsilon}: -2$ total : 1.3	2.5	$V_{\text{ch\_eff}}: 0.5$ $V_{\text{cf\_eff}}: 0$ $\Delta V_{\epsilon}: -2$ total: -1.5	-2.4	$V_{\text{ch\_eff}}: -48.2$ $V_{\text{cf\_eff}}: 46$ $\Delta V_{\epsilon}: -2$ total : -4.2	-3
2.5	2.5	$V_{\text{ch\_eff}}: 32.4$ $V_{\text{cf\_eff}}: -46$ $\Delta V_{\epsilon}: 0$ total: -13.6	-12.7	$V_{\text{ch\_eff}}: 0$ $V_{\text{cf\_eff}}: 0$ $\Delta V_{\epsilon}: 0$ total : 0	0.1	$V_{\text{ch\_eff}}: -31.9$ $V_{\text{cf\_eff}}: 46$ $\Delta V_{\epsilon}: 0$ total : 14.1	13
2.48	2.3	$V_{\text{ch\_eff}}: 29.8$ $V_{\text{cf\_eff}}: -46$ $\Delta V_{\epsilon}: 2$ total: -14.2	-15	$V_{\text{ch\_eff}}: 0.2$ $V_{\text{cf\_eff}}: 0$ $\Delta V_{\epsilon}: 2$ total : 2.2	2.2	$V_{\text{ch\_eff}}: -27.9$ $V_{\text{cf\_eff}}: 46$ $\Delta V_{\epsilon}: 2$ total : 20.1	20
2.45	2.0	$V_{\text{ch\_eff}}: 29$ $V_{\text{cf\_eff}}: -46$ $\Delta V_{\epsilon}: 5$ total : -12	-11	$V_{\text{ch\_eff}}: 0.4$ $V_{\text{cf\_eff}}: 0$ $\Delta V_{\epsilon}: 5$ total : 5.4	4.5	$V_{\text{ch\_eff}}: -27.1$ $V_{\text{cf\_eff}}: 46$ $\Delta V_{\epsilon}: 5$ total : 21.9	23.3

Monte Carlo simulation of the chopping DDA is also conducted to observe the input-referred dc offset of the chopping DDA at 3V power supply and 64 kHz chopping frequency. Fig. 8.2.1.5 shows the histogram of Monte Carlo simulation result.

Fig. 8.2.1.5 Histogram of Monte Carlo simulation result of input-referred errors of 50 balanced chopping DDA samples at 3V and 64 kHz chopping frequency

Refer to Fig. 8.2.1.5, the 50 samples show the input-referred offset having a mean of 10.52 μV , and a standard variation of 7.48 μV . The results of Monte Carlo simulation will be compared with the measurement results of fabricated chopping DDA chips.

8.2.2 Effect of Variation of Parasitic Capacitance and Compensation Resistance

Fig. 8.2.2 Output errors of chopping amplifiers with variation of parasitic capacitance and compensation resistance values at no mismatch condition

It is interesting to examine the effect of unbalanced parasitic capacitance on the output

error voltage. Assume all source resistances are negligible small using buffered output, C_{ps} is 5pF, $C_L = 25$ pF and C_p steps from 0 to 2.5 pF and to 5 pF, For $V_Q = 2.5V$ and $V_{in} = 0V$, the output error voltage for each type of amplifier is shown in Fig. 8.2.2. Even for variation of ± 0.5 k Ω in the nominal compensation resistor R_3 of 1 k Ω , the change of output error voltage gives no more than ± 1 μV , this indicates the insensitivity of both amplifier structures. In overall observation, for higher R_3 values due to over compensation, the sensitivity of error output voltage with respect to the change of unbalanced parasitic capacitance in dual input ports chopping DDA offers relatively less change when compared to that of single input port chopping op-amp.

8.2.3 Measured Results of Chopping DDA

Fig. 8.2.3.1 Microphotography of the chopping DDA [P. K Chan, 2004]

The core chopping DDA had been fabricated by AMS 0.6 μm CMOS technology, with an active area of 0.24 mm² shown in Fig. 8.2.3.1. For offset measurement setup, the amplifier output was connected with a 150 Hz RC low-pass filter to reject the chopping noise. A precision HP 3486 multi-meter was used to record the dc offset. Precision power supplies having 1 mV tuning resolution were programmed to provide the analog ground of 1.5V and different dc inputs with reference to the analog ground of 1.5V. The input-referred dc offset was then calculated for each input case. Care must be taken that the closed-loop gain is chosen not to saturate the amplifier with a given 3V supply. For validating the resistance balancing technique, 10 chopping DDA

chips were measured at a non-inverting gain of 10 and a single 3V supply. The results are depicted in Fig. 8.2.3.2. It is evident that the compensation causes reduction of dc offsets, regardless of the chopping frequencies. The dc offset performance is further evaluated through the histograms as plotted in Fig. 8.2.3.3 and Fig. 8.2.3.4. With 10 kHz and 64 kHz chopping frequency, the mean value of input-referred offset voltage for compensated chopping DDAs is obtained correspondingly as 10.3 μ V and 11.5 μ V. More importantly, it is observed a shift in the redistribution of offsets in both histograms. With balancing technique, 4 out of 10 samples move towards lower offset range, with less than 3 μ V and 5 μ V offsets at 10 kHz and 64 kHz, respectively, demonstrating the effectiveness of the compensation scheme. Compared with the Monte Carlo simulation results shown in Fig. 8.2.1.5, the measurement results worsens slightly from mean value of 10.52 μ V to 11.5 μ V, and standard variation from 7.48 μ V to 8.1 μ V, yet these could come from the less samples of measurement and are acceptable difference between simulation and measurement.

Fig. 8.2.3.2 Measured dc offset results of the balanced/unbalanced chopping DDAs at 10 kHz and 64 kHz chopping frequency and 3V supply

Fig. 8.2.3.3 Histogram of the measured results of balanced/unbalanced chopping DDAs at 3V and 10 kHz

Fig. 8.2.3.4 Histogram of the measured results of balanced/unbalanced chopping DDAs at 3V and 64 kHz

As noise is another critical performance parameter, measurements have been conducted to examine the impact of resistance balancing technique to noise performance. The measured results are depicted in Fig. 8.2.3.5. As can be seen, the input-referred noise root spectral densities based on the closed-loop gain of 10 are 59 $\text{nV}/\sqrt{\text{Hz}}$ @10Hz and 52 $\text{nV}/\sqrt{\text{Hz}}$ @6kHz without balanced resistor whereas 62 $\text{nV}/\sqrt{\text{Hz}}$ @10Hz and 55 $\text{nV}/\sqrt{\text{Hz}}$ @6 kHz with balanced resistor. The result suggests

an increase of $3 \text{ nV}/\sqrt{\text{Hz}}$, which is sufficiently low to be acceptable. Finally, the almost flat response of noise floor indicates that the $1/f$ noise is suppressed, demonstrating the effectiveness of the proposed scheme.

The experimental results have indicated that the resistance balancing technique is useful to further reduce the dc offset of chopping DDA which is applied in the design of post amplification of capacitive transducer and the noise penalty is negligible.

Fig. 8.2.3.5 Input-referred noise with and without balancing resistor from dc to 6 kHz

8.3 Instrumentation-Based SC Capacitive Transducer

8.3.1 Simulation Results of the Proposed Capacitive Transducer

The statistical method is the best way to verify the efficiency of designed circuitry under mass production. The simulation of the whole circuitry aims to ensure the accuracy and stability of the design in the practical environment. The whole circuitry defined here includes the front-end CV converter with an external parasitic capacitor as heavy as 150 pF and the back-end amplification stage chopped at 64 kHz. A Monte Carlo simulation was run with 50 samples on the basis of $C_x=2\text{pF}$, a typical supply condition, at room temperature and through a TSMC 0.25 μm CMOS process.

Fig.8.3.1.1(a) Histogram of Monte Carlo simulation result of error percentage of 50 capacitive transducer samples at $C_x=2\text{pF}$

Fig.8.3.1.1(b) Histogram of Monte Carlo simulation result of error percentage of 50 capacitive transducer samples at $C_x=0.25$ fF

Fig.8.3.1.1 shows a histogram of the Monte Carlo simulation results for (a) $C_x=2$ pF, which represents a large C_x measurement, and (b) $C_x=0.25$ fF, which represents a small C_x measurement. It is clear that the majority of the samples range from having a 0.36% - 0.40% error in the 2pF case. For the case of $C_x=0.25$ fF in a small capacitance measurement, the distribution shows about a 20% error. This is apparently larger than that of a large C_x measurement. Although it is more sensitive to process-related parameters, the errors in the small C_x measurement are acceptable. These Monte Carlo simulation results are compared with the measured results of the fabricated chips to show consistency between simulation and measurement.

8.3.2 Measured Results of the Proposed Capacitive Transducer

The entire CV converter was fabricated using TSMC (Taiwan Semiconductor Manufacturing Co., LTD) 0.25 μ m mixed-signal 2P5M/1P5M+ salicide 2.5V/3.3V process. The chip is bounded to a 28-pin DIL package. The microphotography of the CV transducer is shown in Fig. 8.3.2.1. The die size is of 1.5 mm width and 1.3 mm length.

Fig. 8.3.2.1 Microphotography of the capacitive transducer IC

In a standard laboratory environment, the measurement setup was constructed as shown in Fig. 8.3.2.2. An RC passive filter with a cut-off frequency of 5 kHz was inserted between the output of transducer IC and the measuring instruments. The main purpose was to suppress spikes or high-frequency components arising from the chopping DDA.

Fig. 8.3.2.2 Measurement setup diagram

Five chips were measured to validate the CV converter design. Prior to the measurements, the capacitors $C_{X'}$ and C_{Xdummy} were measured by the precision capacitance measurement meter. Powered at 3V supply, each chip was taken as a measurement for the representative reference values of 2 pF, 2 fF and 0.25 fF, and the error variations were observed to be less than 0.42% for 2 pF, 3.98% for 2 fF, and 21.60% for 0.25 fF. Table 8.3.2(a) shows the measurement errors of the five chips for the three C_x values. Compared with the Monte Carlo simulation results shown in Fig. 8.3.1.1(a) and (b), the error percentages of the five chips at $C_x=2$ pF and 0.25 fF all fall within the simulated range and logically show those error percentages with a higher occurrence possibility.

TABLE 8.3.2(A) MEASUREMENT ERRORS OF 5 CHIPS

Chip no.	$C_x=2$ pF	$C_x=2$ fF	$C_x=0.25$ fF
1	0.39%	3.42%	20.78%
2	0.42%	3.98%	21.60%
3	0.35%	2.84%	15.34%
4	0.40%	3.84%	20.05%

5	0.38%	3.68%	19.74%

TABLE 8.3.2(B) DETAILED EXEMPLARY DETECTION RANGE OF CHIP 1

C_X' (pF)	C_{Xdummy} (pF)	C_X	V_{ref} (V)	V_{ang} (V)	V_{out} (V)	Measured C_X	Error
5.015	3.065	1.95pF	0	1.00197	2.37500	1.95761pF	0.39%
5.015	4.065	0.95pF	0	1.00197	1.67095	0.95381pF	0.40%
5.015	3.065	195fF	0.90185	1.00197	1.13940	196.093fF	0.56%
5.015	3.055	19.60fF	0.99189	1.00197	1.01588	19.714fF	0.58%
5.015	3.145	1.870fF	1.00101	1.00197	1.00327	1.934fF	3.42%
5.015	4.585	0.430fF	1.00101	1.00197	1.00228	0.461fF	7.21%
5.015	4.730	0.285fF	1.00101	1.00197	1.00219	0.327fF	14.73%
5.015	4.760	0.255fF	0.99949	1.00051	1.00073	0.308fF	20.78%

Table 8.3.2(b) is the detailed exemplary raw data of chip 1, from which the plot for Fig. 8.3.2.3(a) is derived. With controllable biasing reference sources, the measured and calculated data are listed.

Fig. 8.3.2.3(a) Error percentage of chip no. 1

Based on the observation in Fig. 8.3.2.3(a), the absolute error values are becoming smaller as C_x decreases from 2 pF until 2 fF. The absolute error values are maintained to be relatively stable at the femto farad level. As the C_x enters the sub-femto farad level, the effect of even the last digit value of the instruments starts displaying a variation in the measurement results. The resolution limit of the measurement instruments also contributes to the stability.

Fig. 8.3.2.3(b) Error percentage of 5 chips

Fig. 8.3.2.3(b) shows the small variation in error percentages among the other four chips with respect to the chip no. 1. This confirms the consistency of the measured results from the different chips and the functionality of all five chips.

Fig. 8.3.2.4(a) Output waveform of one chip at $C_X = 1.95 \text{ pF}$

Fig. 8.3.2.4(b) Output waveforms of four chips at $C_X = 1.95 \text{ pF}$

An approximate full scale capacitance with $C_X = 1.95 \text{ pF}$ is shown in Fig. 8.3.2.4 (a). The oscilloscope displayed 2.375V and the value was identical to that of the precision digital multimeter. This is translated into the change in output voltage of 1.37303V with respect to the analog ground, which corresponds to the measured C_X value of 1.95761 pF. The closed-loop gain of the chopping DDA is 7. The calculation of the

measured C_X is based on the following two equations:

$$C_X * (V_{ang} - V_{ref}) = C_f * \Delta V_{out} \quad (8.3.1.1)$$

$$V_{out} = V_{ang} + \Delta V_{out} * 7 \quad (8.3.1.2)$$

where C_X has the unit of pF.

In another aspect, Fig. 8.3.2.4 (a) shows the different working phases of the CV convertor. During the preliminary stage, the digital section works to generate all necessary signals to operate the analog section and the CV convertor has not been triggered to work yet. Until all the operating signals are ready, the CV convertor starts functioning with the cycle of every 300 μ S. The first 100 μ S is T1 and the sample-and-hold signal functions in the sample status to allow the CV convertor to execute the four phase working cycle. Sequentially, the front-end CV convertor $\phi 1$ is the reset phase for the analog ground, $\phi 2$ is the error sampling phase, $\phi 3$ is the reset phase for the reference voltage input, and $\phi 4$ is the signal plus error measurement phase accordingly. After that, T2 and T3 are the holding status for the whole circuitry and the front end CV convertor holds the two differential output voltages for later stage high-precision gain amplifying. At the later stage of T2, the output of the high-precision gain amplifier shows a stable value which is desired for the measurement of C_X . Then, another T1 of another 300 μ S cycle arrives and the working phases repeat. It can be observed that the oscilloscope waveform echoes the detailed working principle of each phase depicted in Chapter 4. Fig. 8.3.2.4 (b) shows the output waveforms of the other four chips with 1.95 pF C_X . All of the five chips show similar results.

For the approximate middle value of $C_X=0.95$ pF, the oscilloscope displayed 1.670V in Fig. 8.3.2.4(c) while the digital multimeter showed 1.67095V. This indicates that the meter exhibited a more precise measurement than the oscilloscope. For the small

capacitance measurement starting from a few hundred fF and below, the proposed charge lever mechanism was applied. Finally, for the ultimate small capacitance measurement in the case of $C_X=0.255$ fF, the oscilloscope was not able to reflect the change in Fig. 8.3.2.4(d) but the digital multimeter showed a value of 1.00073V, suggesting a change in output voltage of 0.22 mV with respect to the analog ground. The result demonstrates that the proposed capacitive transducer can achieve the limit of 0.255 fF resolution. It is also observed that when the capacitance value in the measurement is decreased, the amount of error is increased. This phenomenon is probably due to the unbalanced fringing field effect or the environmental electric field that existed across the pins and PCB board. The dc offsets in all the measurement cases were negligibly small, thus validating the effectiveness of the proposed precision circuit design techniques, which are based on the SC Instrumentation-based circuit technique for the front-end interface circuit design and resistance balancing circuit technique for the back-end chopper stabilization DDA circuit design.

Fig. 8.3.2.4(c) Output waveform of the chip at $C_X=0.95$ pF

Fig. 8.3.2.4(d) Output waveform of the chip at $C_x=0.255$ fF

Fig. 8.3.2.4(e) Output system sample-and-hold signal

The other output signal is the sample-and-hold signal, with a square wave having a 300 μ S period and 1/3 duty cycle, as shown in Fig. 8.3.2.4(e), which serves as a reference signal for monitoring the output voltage. From the overall measurement results, it is confirmed that the capacitive transducer IC can measure from 0.26 fF to a full scale of 2 pF, with a maximum error of about 20% in the smallest capacitance detection.

8.4 Comparison with Prior-Art Works

In order to make a comparison with different reported capacitance measuring circuits in a fair manner, the focus is on the fundamental front-end CV interface circuit. The reason for this is that in most of the cases, the front-end interface dictates the resolution and sensitivity in the context of sensing small capacitances under heavy parasitic capacitances. The post-amplification stage can be realized in many circuit techniques, and it should hence be removed in order to permit an examination of the standalone performance of each front-end interface. Due to different operation conditions such as different values of the power supply, voltage reference source and parasitic capacitance, this leads to a different level of performance. In this issue, different figures-of-merit are established to normalize their performance parameters in order to have a realistic comparison in the respective circuit architecture. All the performance parameters of each capacitance measuring circuit are summarized in Table 8.4.1.

The first FOM is the parasitic noise gain, as most of the structures, which are based on the op-amp structure, form a parasitic network arising from the effective impedance of the feedback network and the effective impedance of the network shunting the inverting input of the op-amp to the ground. The feedback network and shunt inverting input network form a non-inverting parasitic gain for noise from an op-amp design model. This is generalized as follows:

$$GAIN_{Noise} = 1 + Z_f / Z_i \quad (8.4.1)$$

It is noted that the noise gain is frequency dependent. The impedance network can be either a pure capacitor or a capacitor in parallel to a resistive component, dependent on the type of circuit architecture. In ECT, the signal bandwidth is typically restricted to 5 kHz. Hence, the effective noise gain for each transducer is calculated based on

the specific frequency. From the table, it can be seen that the circuit architecture with a feedback resistor component reduces the parasitic noise gain. It is apparent because the resistor tends to shoulder output and input to form a voltage follower like structure. Therefore, this is the main benefit of this group of circuits. In SC transducers, they suffer from this kind of drawback because the pure capacitor is the feedback element.

The second is the sensitivity FOM. As observed, the sensitivity of a CV transducer depends on the circuit architecture, reference source potential and the degree of parasitic capacitance. It is common to mention that the higher the supply, the higher the reference source value, while the larger the parasitic capacitance, the smaller the overall sensitivity. As a result, the normalization leads to

$$\text{Normalized Sensitivity FOM} = \frac{S}{\text{Total Supply}} C_s \quad (8.4.2)$$

where S stands for the sensitivity, C_s is the parasitic capacitance and Total Supply represents the absolute value of the supply voltage. From the table, it can be seen that the SC based transducer has a moderate sensitivity factor. This is still not the major limiting factor for the capacitance measuring circuits that make use of switched-capacitor circuit techniques, because the switched-capacitor circuits can employ the CDS technique to reduce the low-frequency noise.

The third FOM refers to the C_x dynamic parameter which is defined as

$$C_x \text{ dynamic} = \frac{C_x(\text{max})}{C_x(\text{min})} \quad (8.4.3)$$

This is the actual performance index of the capacitance measuring circuits in terms of a realistic dynamic range. It is interesting to observe that despite the fact that the switched-capacitor circuits suffer from higher parasitic noise gain, the overall

resolution performance outperforms that of others. This is mainly because the switched-capacitor technique permits a low-frequency noise reduction and the fully integration approach benefits from low-noise implementation. More importantly, a very high gain-bandwidth op-amp is not required, which could be noisy due to the broadband design. Finally, the lower clock frequency in the switched-capacitor circuit design also brings in the key advantage of a better supply rejection performance of the op-amp.

As a final remark, compared to all the reported capacitance measuring circuit results, the proposed instrumentation-based SC CDS capacitive transducer offers the best dynamic result while detecting a very small capacitance under very heavy parasitic capacitance, dissipating low power, operating in much lower supply and supporting monolithic integration as the key technical merits. This is thanks to (i) the instrumentation based SC technique to reduce system-level switch errors, (ii) the CDS technique to reduce $1/f$ noise and dc offsets of the op-amp, (iii) the transducer feedback loops to reduce the noise and errors arising from the two S/H circuits and improve the stability of the transducer against time drift and temperature fluctuation, (iv) the resistance-balancing techniques to further reduce the dc offset which is beneficial for improving precision as well as reducing the drift against time and temperature and (v) the chopper-stabilization DDA circuit technique for achieving a stable and low-noise post amplification for a quality back-end signal processing stage.

TABLE 8.4.1 PERFORMANCE COMPARISON OF PRIOR-ART BASIC FRONT-END
TRANSDUCER INTERFACES WITHOUT POST AMPLIFICATION STAGE OR
DIFFERENTIAL-TO-SINGLE-ENDED STAGE

Parameter	W. Q. Yang [1999/2003]	D. L. Xie [2004,06]	S. M. Huang/ X. H. Hu [1992]/[2007]	J. Peng [2007]	T.N. Phua [2008]	This work
Circuit Technique	AC-based	SC Diff. Sampling	Charge and Discharge	SC CDS	Switched- Current (S.I.)	Instrumentation -based SC CDS
Comp. Type	Discrete	Discrete	Discrete	IC	IC	IC
Technology	BJT	BiFET	BJT	CMOS 0.6 μ m	CMOS 0.35 μ m	CMOS 0.25μm
Supply Voltage	+/- 15 V	+/- 18 V	+/- 15 V	5 V	3 V	3 V
Power Dissipation	300 mW Op-amp LM6364 $\times$ 2	2040 mW Op-amp TL082C $\times$ 3	300 mW Op-amp LM6361N $\times$ 2	10 mW 2-stage, folded- cascode input stage	N. A. S.I. Super Mirror	1.2 mW 2 stage, cascode input stage
Switching Freq. f	500 kHz	100 kHz	1 MHz	250 kHz	N.A.	80 kHz
Op-amp GBW	175 MHz	4 MHz	50 MHz	43 MHz	—	30 MHz
C _f	22 pF	—	4.7 nF	8 pF	—	10 pF
R _f	0.22 M Ω	—	15 k Ω	—	—	—
C _s	150 pF	N.A.	150 pF	150 pF	1.2 pF	150 pF
Virtual Earth C _{in}	—	—	0.1 μ F	—	—	—
Parasitic Noise Gain @ 5kHz	1.91 Single-side	N.A.	3.04 Single-side	19.7 Single-side	N.A.	16 Single-side
Sensitivity, S	2 V/pF	2.4 V/pF	450 mV/pF	250 mV/pF	~14.8 V/pF	100 mV/pF
Reference Source	V _s = 10Vp sinewave	N.A.	V _r = 15 V	V _r = 1 V	—	V_r = 1 V
Output Expression	$\sim 2V_s \times (C_x/C_f)$	$V_r \times (C_x/C_f)$	$2V_r R_f C_x f$	$2V_r \times (C_x/C_f)$	$\sim k_1 \times [k_2 - V_1 \times \ln[1 - (\omega C_x f / I_{bias})]]$	$V_r \times (C_x/C_f)$
Sensitivity FOM (S/supply) $\times$ C _s	~ 10	N.A.	2.25	7.5	5.92	5
* C _{xmax} (pk)	2 pF	2 pF	2 pF	2 pF(not mea. value)	~ 67.5 fF	2 pF
*C _{xmin} (pk)	10 fF	0.5 fF	0.3 fF	1 fF (not mea.value)	0.91 fF	0.26 fF
*C _x Dynamic C _{xmax} /C _{xmin}	46 dB	72 dB	76.5 dB	N.A.	~ 37.4 dB	77.8dB

*Denote the measured data from the whole capacitance measuring circuit but not from the front-end CV converter.

CHAPTER 9

9 CONCLUSIONS AND RECOMMENDATIONS

9.1 Conclusions

This thesis has reviewed different approaches to state-of-art ECT systems and has compared the advantages and disadvantages of each circuit approach. This was followed by a review of both the key switched-capacitor circuit technique and the chopper-stabilization circuit technique that support the precision and low-noise design simultaneously. The relative advantages and disadvantages are now better understood so as to permit the identification of problems, the formulation of the circuit and system research strategy together with design and realization of a new capacitance measuring circuit in order to meet the ultimate objectives.

Prior to the design, the thesis presented a new instrumentation SC design methodology to cancel the non-ideal effects such as $1/f$ noise, dc offset and circuit level switch error in an economical way. This was applied to the switched-capacitor circuit design incorporating the usual CDS technique for making further improvements to the circuit performance. To address the practical problems arising from the chopper-stabilized amplifiers, the thesis presented an analysis of the main non-ideal sources such as charge injection, clock feedthrough, mismatches of components, and so on, in a precision analog design approach. The models of non-ideal effects were proposed to predict the imperfection of the output from the precision amplifier. This led to a better understanding of the fundamental limitations

to the chopping amplifiers. As a result, a new resistance balancing circuit technique was proposed to further reduce the dc offset of the amplifier. The proposed technique has a technical merit that it can be applied to the SC capacitive transducer design. Minimizing the dc offset leads to the benefit of precision and output stability against time and temperature fluctuation. This is an essential attribute for a precision analog design.

Based on the study, the instrumentation based SC approach was proposed in a new S/H circuit design example to demonstrate the usefulness of the methodology. This was then applied to the foundation SC capacitive transducer design with basic instrumentation based SC CDS front-end capacitive transducer followed by the DDA circuit as the post-amplification stage. The circuit was further extended to the new SC capacitive transducer incorporating SC instrumentation based methodology, CDS circuit technique, additional feedback loops to reduce noise and errors from the storing devices used by the instrumentation-based methodology and high precision chopping DDA incorporating the resistance balancing technique for quality post amplification. At this juncture, design-for-test strategies were also devised. This included the parasitic balancing technique for use in either test or Cx measurement, a method of generation of minute capacitance for testing and the concept of a charge lever mechanism to facilitate minute capacitance testing.

As the IC prototype was geared towards a mixed-signal circuit and system design, the digital blocks were discussed and their functions were explained in detail. Moreover, the control waveforms were also illustrated. Since the design-for-test strategy was applied throughout the chip, the digital circuit that was dedicated to this purpose was also mentioned.

The layout is also crucial to the mixed-signal circuit system design. Therefore, the design-for-layout strategies were discussed. This included low-noise layout methods and the matching strategies for precision analog. Moreover, the floor plan is important

for mixed-signal silicon IC. It was highlighted how the system block is located and how the pins are allocated for packaging. All of these are important layout considerations for a successful mixed-signal IC prototype.

The final work was dedicated to both the simulation and measurement results to validate all the proposed methodologies and new circuit designs. The proposed SC instrumentation based methodology using the S/H circuit was demonstrated as the first example. Better precision can be obtained compared to the classical circuit method. This was then followed by the validation of the resistance balancing technique on the design of the chopper-stabilized DDA. The measured results have confirmed a better yield on lower dc offsets of amplifiers and reduced dc offsets when compared to the conventional chopping DDA while the input-referred noise is only increased very slightly. Therefore, the proposed precision analog circuit technique is validated and it is applied to the proposed SC capacitive transducer. Finally, different figures-of-merit were established to compare the measured results of the proposed SC capacitive transducer with the reported results of their counterparts. It turns out that the new SC capacitive transducer offers the best performance metrics. This suggests that the combination of all new circuit techniques and methodologies leads to a high quality IC prototype that achieves advanced state-of-art performance.

9.2 Recommendations

The ECT system is consistently pushed for portability, small size, low power consumption, and low supply voltage for on-site industrial applications. All these requirements are directed to the integrated solution while addressing the matching among electrode pairs, the possible reduction of parasitic capacitance arising from the measurement setup or test fixture.

With the fabrication dimension being continuously scaled down from the advancement of process technologies, this naturally leads to a decrease in power supply voltage in the sensor interface. In order to stay in line with the development of process technology and to facilitate the realization of a fully integrated, portable ECT system with a capacitive transducer sensor incorporated, the capacitive transducer is bound to adopt a low-voltage CMOS design with a further reduced power supply, such as 2.2 V or 1.8 V or even lower. The current research has shown many circuit techniques incorporating multiple methodologies and circuit techniques for achieving a quality ECT capacitive transducer. The adoption of a low-voltage CMOS design to the capacitive transducer introduces possibilities for future research in the domain of the low-voltage integrated circuit design field.

It is clear that the reduced power supply voltage increases the challenging issues for the monolithic capacitive transducer design. This resorts to architectural modifications together with new circuit techniques in order to alleviate problems such as leakage current, headroom issue, reliability issue on bootstrapped switch under low-voltage operation, and so on, in the context of advanced process technologies. Possible design directions may include the adoption of a full differential design instead of single ended topology so that the diode transistor design could be removed to expand on dynamic ranges. In keeping with a reduction in supply, one of the most important issues is the tolerance of noise from circuitries under low-voltage design. Low-noise

design techniques are to be continuously explored in order to ensure the proper functionality of the capacitive transducer maintained at a good dynamic range in low-voltage operations.

Another challenge is how to further improve the resolution of the transducer. The resolution enhancement could be handled from several angles. These include the circuitry configuration, the dedicated layout techniques, the measurement methodologies, and so on. Finally, another problem is in tackling robustness under process sensitive parameters.

All these recommendations suggest future work on the ultra low-power ECT transducer.

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LIST OF PUBLICATIONS

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