Design of multi-standard and wideband delta-sigma modulator

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2010

Du, Y. (2010). Design of multi-standard and wideband delta-sigma modulator. Master's thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/46990>

<https://doi.org/10.32657/10356/46990>

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**DESIGN OF MULTI-STANDARD
AND
WIDEBAND DELTA-SIGMA MODULATOR**

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School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Master of Engineering

2010

Acknowledgement

I wish to express my appreciation and thankfulness to my supervisor, Dr. Tiew Kei Tee and Prof. Siek Liter for their guidance, advice and support to my research. It is a great opportunity to study and work with their supervision. In addition, I would like to thank the members of my thesis examination committee for their time and feedback to improve the quality of my thesis.

I also want to thank the members of my laboratory mates for their helping on technical problems for my project. Thanks to my friends in Center of Integrated Circuits and Systems (CICS). I appreciate the friendships and support from them.

Thanks to CICS for workstation of CADENCE and Nan Yang Technological University for funding this project.

Finally, I am very grateful to my family for their encouragement, understanding and moral support, which made this work into a completed endeavor. Especially, I would like to express my deep appreciation to my husband, Wang KaiFei who has accompanied me with his strong encouragement and support in these years. I also thank my daughter YaXin for the joy she has added to my life.

Abstract

A growing number of products in communication area now require high-precision analog-to-digital conversion. In addition, there are increasing requirements for emerging products to extend their features into programmable and reconfigurable applications for multiple frequency operations. Delta-sigma modulation, first proposed by Cutler and Inose in the 1950's and early 1960's, offers a more practical alternative to high-precision analog-to-digital conversion. In addition to advantages such as relaxed anti-aliasing filtering and analog building blocks requirements, delta-sigma ($\Delta\Sigma$) modulation with its inherent dynamic range versus bandwidth trade-off serves as an ideal candidate for the design of a multi-standard capable analog-to-digital (A/D) interface which is adaptable to different dynamic range and bandwidth requirements. Conventionally, delta-sigma analog to digital converters are adopted to achieve high resolution (>15 bits) for low signal bandwidth (<100 kHz). Recently, much work has been devoted to the approaches that overcome the limitations such as low speed in delta-sigma data conversion. This is due to the increasing demand for high-resolution and wide bandwidth combined with high sampling rate and low supply voltage of ADCs.

In this work, a multi-standard wideband 6th-order delta-sigma modulator operating at 64MHz sampling frequency has been implemented for operating at five different low oversampling ratios of 4, 6, 8, 12 and 16. The prototype is implemented in a 0.18- μ m CMOS process with 1.8-V power supply. For a sampling frequency of 64MHz, the power consumption of the modulator is 32mW. By inserting the proposed PCA (programmable capacitor array) blocks into the cascade architecture, the modulator can achieve the signal bandwidth from 2MHz to 8MHz. In contrast to the multi-standard modulators reported in which more than one sampling rates are used to obtain different signal bandwidths with an achievable Nyquist rate bandwidth of less than 2MHz., the proposed modulator architecture achieves multiple bandwidth using a PCA at a constant sampling frequency and the achievable Nyquist rate bandwidth is larger than 2MHz. Our proposed $\Delta\Sigma$ modulator supports wide band analog-to-digital conversion and allows operation at oversampling ratio as low as 4. So far, some of the previous wideband delta-sigma modulators also use low oversampling ratio (M). But this is one of the first $\Delta\Sigma$ modulators that uses an M equals to 4 with no multi-bit quantizer and dynamic element matching (DEM) algorithm which limits the achievable sampling rate.

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Nomenclature

$\Delta\Sigma$	Delta-sigma
A/D	Analog-to-digital
PCA	Programmable capacitor array
DEM	Dynamic element matching
ADC	Analog-to-digital conversion/converter
VLSI	Very-large-scale integration
CMOS	Complementary metal–oxide–semiconductor
MASH	Multi-stage noise shaping
M	Oversampling ratio
f_s	Sampling frequency
f_B	Input frequency of interest
f_N	Nyquist rate frequency
$P_d(f)$	Power spectral density
STF	Signal transfer function
NTF	Noise transfer function
DAC	Digital-to-analog conversion/converter
$P_{Q,Nyquist}$	Quantization noise power of a Nyquist rate converter
L	Order of the delta-sigma modulator
PSD	Power spectral density
DR	Dynamic range
SNR	Signal to noise ratio
$SNDR$	Signal to noise and distortion ratio
FFT	Fast Fourier transform
FOM	Figure of merit
P	Power dissipation
b	Effective resolution
BW	Nyquist rate output bandwidth
$X(z)$	Analog input signal
$Y(z)$	Final digital output of the whole system

$Y_1(z), Y_2(z), Y_3(z)$	Digital outputs of individual stage
$H_1(z), H_2(z), H_3(z)$	Digital error cancellation network
ECN	Error cancellation network
WDSM	Wideband delta sigma modulator
CT	Continuous-time
SC	Switched-capacitor
SI	Switched-current
RC	Resistor and capacitor
OTA	Operational transconductance amplifier
opamp	Operational amplifier
GBW	Gain bandwidth
SR	Slew rate
DSM	Delta sigma modulator
PCA	Programmable capacitor arrays
CMFB	Common mode feedback
IC	Integrated circuit
DUT	Device under test
PCB	Printed circuit board

Chapter 1

Introduction

1.1. Scope of Thesis

By virtue of advantages such as insensitivity to noise and ease of design, more and more signal processing is implemented in the digital domain. However, most of the time input signals are only available in analog forms. There is a ubiquitous need for interface circuits converting the real world analog signal to digital signal. In addition, the rapid growth in communications also stimulated the development of analog-to-digital conversion (ADC) technology. The basic operation of an analog-to-digital converter is to sample the input signal in time and quantize the amplitude to a series of digital codes representing the signal amplitude level. Various techniques have been proposed to perform analog-to-digital (A/D) conversion [1]. One of the approaches is delta-sigma modulation [2].

Among all the analog-to-digital conversion (ADC) techniques, delta-sigma modulation is widely adopted in the high precision applications with moderate signal bandwidth. A qualitative illustration of bandwidth and resolution for some of the ADC techniques given by [3] is shown in Figure 1.1. Obviously, delta-sigma A/D converters can obtain very high resolution with relatively low signal bandwidth. Flash converters, on the other hand, can achieve very high sampling rate with limited resolution of about 8 or 10 bits. There are also candidates like subranging/pipelined and successive approximation etc, which offer moderate resolution with moderate signal bandwidth as well. The choice of ADC architectures depends on the application and the performance requirements of a certain application.

Figure 1.1 Illustration of bandwidth vs. resolution

With the development of modern communication systems, the wireless and data communications areas coupled with the advancement in VLSI technology have stimulated the use of analog to digital interface for wideband applications. Oversampled delta-sigma modulators are popular for their ability to implement high performance analog-to-digital converters (ADCs). Furthermore, delta-sigma modulation with its inherent dynamic range versus bandwidth trade-off serves as an ideal candidate for the design of a multi-standard capable A/D interface adaptable to different dynamic and bandwidth requirements [4].

The delta-sigma modulator in this work can be programmed to achieve five different sets of signal bandwidth and resolution. This is realized by the programmable capacitor array (PCA) which is located at the second and third stage modulators. With the speed of digital circuits increasing up to the gigahertz range, there is simultaneously increasing demands on the analog-to-digital converters in terms of resolution and bandwidth. Another desired performance of ADCs is the conversion rate from audio range to megahertz in the communication systems to

meet the growing needs of the high-capacity and high-speed data transfer. To meet the multi-standard requirement, one straightforward way is to change the sampling rate so as to get different signal bandwidth at a certain oversampling ratio. While in practical implementation, the different sampling rate will require different characteristic of the operational amplifier. When the sampling rate is increased to very high, it is difficult to design a proper opamp to meet the fast operating speed. Also, a CMOS technology will be an upper limit on the analog circuit performance and sampling speed. In this work, a PCA was introduced to obtain the multi-standard functionality. In oversampling ADC theorem, the signal bandwidth is proportional to the sampling frequency and inversely proportional to the oversampling ratio [5], achieving wideband conversion implies low oversampling ratio. Cascade or MASH $\Delta\Sigma$ architectures can combine high order noise shaping with the stability of a second-order modulator, and are suited for high-speed ADCs with low oversampling ratio (M).

The focus of this work is to design and implement a delta-sigma modulator capable of operating at an M equal to 4, 6, 8, 12 and 16 respectively for multi-standard and wideband applications. System and circuit level simulations and evaluations have demonstrated that the proposed modulator is capable of achieving high speed and high resolution in analog-to-digital conversion. The detailed design considerations in circuit implementation of the proposed modulator are also analyzed and discussed. The prototype is fabricated in a 0.18- μm CMOS process with 1.8-V power supply. Besides the property of wide signal band, the designed delta-sigma modulator can meet the multi-standard requirement by switching three external control signals according to different oversampling ratios.

Figure 1.2 Illustration of the objective performance

As illustrated in Figure 1.2, the performance of the proposed delta-sigma A/D converter can be used in the high speed and medium resolutions area, which is traditionally dominated by pipelined A/D converters. The signal bandwidth that can be achieved ranges from 2MHz to 8MHz with dynamic range ranging from 47dB to 74.5 dB respectively.

1.2 Thesis Organization

This thesis is divided into 7 chapters and organized as follows: Chapter 2 provides the concept overview and basic architectures of delta-sigma modulation. The operating principle and fundamental architectures of the delta-sigma modulator are introduced. The advantages and disadvantages of each different structure are investigated to determine the suitable one that is established in the followed sections of the thesis.

Chapter 3 describes the system level architecture of the implemented delta-sigma modulator that can provide variable resolution (i.e. multi-standard) for high frequency (i.e. wideband) applications. The integrators' gain factors are given in

this chapter and the overall system transfer function is explored. The simulation results reveal the desired ideal performance of the modulator.

Chapter 4 presents a detailed study of the design methodology in the practical implementation of the proposed MASH delta-sigma modulator. Firstly, the non-idealities such as finite DC gain, linear settling, slew rate and etc. in the major building block of a switched-capacitor integrator --- opamp are investigated. Next, the circuit noise sources such as sampling noise, thermal noise, flicker noise and etc are studied as well. Parameter mismatch which is essentially critical in the cascade delta-sigma architectures is also thoroughly considered as another precaution. These parameter mismatch effects can be related through the capacitor ratio mismatches and thus can be quantified for analysis purpose. Having considered the effects of these non-idealities, the non-linear model for the real implementation of SC integrators is also given in this chapter.

Chapter 5 presents the detailed switched-capacitor circuit implementation in a 0.18 μ m CMOS process of the proposed modulator based on the architecture introduced in Chapter 3 and the methodology described in Chapter 4. The design for different component blocks, including operational amplifier, quantizer, programmable capacitor array (PCA), clock generator and clock booster, as well as an analysis of the circuit noise, are covered in this chapter.

Chapter 6 examines the prototype layout of the proposed delta-sigma modulator. Test setup and post-layout simulation results are detailed in this chapter. Discussion and comparison against state-of-the-art designs are also provided.

Chapter 7 contains the comments of contribution and suggestion for future work.

Chapter 2

Overview of Delta-Sigma ADC

As one of the ADC technologies, delta-sigma ($\Delta\Sigma$) modulation technique has become very popular and also acquires distinguished development in recent years. It can achieve high resolution performances while avoiding many of the difficulties encountered with conventional methods for analog-to-digital conversion such as relaxed anti-aliasing filtering and analog building blocks requirements. The main concept of the delta-sigma modulation is based on oversampling and quantization noise shaping. In this chapter, beginning with an introduction to these two operations, the discussion contains different delta-sigma architectures from first-order to higher-order, cascade and multi-bit etc. At the end of this chapter, a comparison of different architectures of delta-sigma modulator is presented.

2.1 Oversampling Conversion

It is well known that the sampling frequency (f_s) must be at least twice the maximum input frequency of interest (f_B) so that the signal can be re-constructed. This frequency is known as the Nyquist rate frequency f_N , which is equal to $2 \cdot f_B$. Oversampling means to sample the signal at a sampling frequency f_s that is larger than the Nyquist rate, $2f_B$. The oversampling ratio (M) is defined as the ratio between the sampling frequency f_s and the Nyquist rate $2f_B$ [5].

$$M = \frac{f_s}{2f_B} \quad (2.1)$$

To simplify the analysis of the noise from the quantizer, the quantization noise is temporarily treated as a white noise that distributes in the range $\pm f_s/2$ and the quantization gain as unity under certain assumptions [6]. Figure 2.1 depicts a qualitative analysis to the power spectral density $P_d(f)$ of the quantization noise for Nyquist rate conversion and oversampling conversion respectively. The total power of the quantization noise is identical for these two conversions, but the noise power spectra distribution within the signal band is different for different conversion technique used. There is much less noise power falling into the signal bandwidth $[-f_B, +f_B]$ for oversampling conversion than that of Nyquist rate conversion. Owing to this property, oversampling conversion has been widely used to get high signal to noise ratio [7] [8]. Using oversampling alone, each doubling of M only improves the signal-to-noise ratio by about 3dB, which is still not effective for some of the high-resolution applications. To obtain even higher resolution, noise shaping technique must be used which will be discussed in the next section.

Figure 2.1 $P_d(f)$ of the quantization noise for Nyquist rate and oversampling conversion

2.2 Quantization Noise Shaping

The output signal of a general delta-sigma modulator contains two components: the input analog signal and the quantization noise. The input signal is usually shaped by an all-pass or low-pass signal transfer function (*STF*) that preserves the original signal characteristics. The quantization noise is shaped by a high-pass noise transfer function (*NTF*) in the delta-sigma modulator. Figure 2.2 illustrates a qualitative analysis to the noise shaping spectra of a delta-sigma modulator within $[0, +f_s/2]$. The other half part of frequency range between $[-f_s/2, 0]$ is the symmetric mirror of $[0, +f_s/2]$ as Y axis. Without noise shaping, the quantization noise will uniformly distribute within $[-f_s/2, +f_s/2]$. The noise power located within the signal band $[-f_B, +f_B]$ is still quite large. After shaping by a certain noise transfer function (*NTF*) of a delta-sigma modulator, the power spectral density of the quantization noise is greatly suppressed in the signal band and most of them are pushed towards the high frequency region beyond the signal band, which can then be removed by a digital low pass filter. The form of *NTF* is determined by the structure of the delta-sigma modulator. More detailed information on *NTF* will be explained in the following sections.

Figure 2.2 Illustration of quantization noise shaping

2.3 Basic Architecture of $\Delta\Sigma$ Modulators

In delta-sigma A/D converters, the main idea is to oversample the analog input signal at a sampling rate that is higher than the Nyquist rate and combine with negative feedback and digital filtering to obtain high resolution. Figure 2.3 represents a basic block diagram of a delta-sigma ($\Delta\Sigma$) ADC. The system consists of an anti-aliasing filter, a loop filter $I(z)$, an n -bit internal ADC, an n -bit DAC in the feedback path and a digital decimator with down sampler.

Figure 2.3 Basic scheme of a delta-sigma ADC

In order to avoid aliasing effects, the input signal is usually band-limited by an anti-aliasing filter before feeding into the modulator. The digital low pass filter is used to remove the noise power outside the signal band and the purpose of the down-sampler is to down sample the signal to the Nyquist rate. One of the major advantages of $\Delta\Sigma$ A/D converter is the relaxed requirement on the anti-aliasing filter used to band-limit the analog input signal. Since the sampling frequency is much higher than the Nyquist Rate, only low order low-pass filter such as RC low-pass filter may be used. The decimator is a pure digital system and can be designed by following some well-documented approaches [9]. So the main challenge of a delta-sigma ADC is generally on the design of the modulator.

Figure 2.4 (a) highlights the delta-sigma modulator portion of the overall delta-sigma ADC. It consists of a loop filter $I(z)$ and a quantizer. The quantizer refers to the conventional ADC and DAC used in the modulator. If a one bit ADC is used, the delta-sigma modulator can be modeled by replacing the quantizer with a gain factor g_q and an additive noise source $E(z)$ as shown in Figure 2.4 (b). The value of g_q depends on the scaling factor of the loop filter. If one-bit quantizer is used, it can be set to 1.

Figure 2.4 (a) Delta-sigma modulator (b) Quantizer model

Analyzing the model in Figure 2.4, one can obtain the z -domain transfer function between the input and output of the delta-sigma ($\Delta\Sigma$) modulator:

$$Y(z) = \frac{I(z)}{1 + I(z)} \cdot X(z) + \frac{1}{1 + I(z)} \cdot E(z) \quad (2.2)$$

So the $\Delta\Sigma$ modulator in Figure 2.4 (a) has the following noise transfer function (NTF) and signal transfer function (STF):

$$\begin{aligned} NTF(z) &= \frac{1}{1 + I(z)} \\ STF(z) &= \frac{I(z)}{1 + I(z)} \end{aligned} \quad (2.3)$$

A simple loop filter $I(z)$ is

$$I(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (2.4)$$

which is an integrator and effectively a low-pass filter. It can be implemented as an accumulator using a unit delay as shown in Figure 2.5. The large gain ($I(z) \rightarrow \infty$) of the integrator at low frequencies ($z \rightarrow 1$) results in the suppression of the quantization noise in the low frequency region i.e. the signal base band region.

Figure 2.5 Integrator implementation

The resulting transfer function for the modulator is

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) \quad (2.5)$$

where the *NTF* and *STF* are

$$\begin{aligned} NTF(z) &= 1 - z^{-1} \\ STF(z) &= z^{-1} \end{aligned} \quad (2.6)$$

Since the transfer function is given by $(1 - z^{-1})$, the noise is shaped by a high pass filter characteristic. This suppressed in-band noise power is given by

$$P_Q = \int_{f_B}^{f_s} \frac{P_{Q,Nyquist}}{f_s} \left| 1 - e^{-j2\pi \frac{f}{f_s}} \right|^2 df = \frac{P_{Q,Nyquist}}{M^3} \cdot \frac{\pi^2}{3} \quad (2.7)$$

where $P_{Q,Nyquist}$ is the quantization noise power for a Nyquist rate converter, f_s is the sampling frequency and M is the oversampling ratio of the delta-sigma modulator.

In the time domain, the signal transfer function is just a unit delay of the input signal. The quantization noise is shaped by the high-pass $NTF(z) = 1 - z^{-1}$ and will be pushed to the high frequency region. This structure forms exactly a first-order delta-sigma modulator, which is the most elementary architecture. The other architectures can all be an extension of this one. Residual tones generated due to the close correlation between the input signal and the quantization noise are the main

drawback of first order delta sigma modulators. This problem could be solved by using second or higher order modulators.

2.4 Second and Higher Order Single-loop $\Delta\Sigma$ Modulators

2.4.1 Conventional 2nd-order $\Delta\Sigma$ Modulator

Figure 2.6 Second-order delta-sigma modulator

To further improve the performance of a modulator, an intuitive idea is to replace the ADC in Fig. 2.4(a) as a first order $\Delta\Sigma$ ADC. The resulting modulator becomes a second-order $\Delta\Sigma$ modulator. A conventional structure of the second-order $\Delta\Sigma$ modulator is shown in Figure 2.6. By choosing the coefficients properly, the *NTF* and *STF* of the modulator in Figure 2.6 are given by equation (2.8).

$$\begin{aligned} NTF(z) &= (1 - z^{-1})^2 \\ STF(z) &= z^{-2} \end{aligned} \quad (2.8)$$

Extending equation (2.6) and (2.8), one can obtain the *NTF* and *STF* of an L^{th} -order single-loop $\Delta\Sigma$ modulator as shown in equation (2.9).

$$\begin{aligned} NTF(z) &= (1 - z^{-1})^L \\ STF(z) &= z^{-L} \end{aligned} \quad (2.9)$$

It can be seen that the noise transfer function of higher order modulator is given by $(1-z^{-1})^L$, where L is the order of the delta-sigma modulator. Subsequently, the in-band quantization noise power is given by

$$P_{Q,\Delta\Sigma} = \int_{f_B}^{f_B} \frac{P_{Q,Nyquist}}{f_s} \left| 1 - e^{-j2\pi \frac{f}{f_s}} \right|^{2L} df = \frac{P_{Q,Nyquist}}{M^{2L+1}} \cdot \frac{\pi^{2L}}{2L+1} \quad (2.10)$$

By setting L equal to 1, 2 and 3 respectively, the plot of the frequency response of the 1st-order, 2nd-order and 3rd-order *NTF* are shown in Figure 2.7. It is obvious that the higher the modulator order, the more the quantization noise will be suppressed in the low frequency region and the more amplified in the high frequency region.

Figure 2.7 Frequency response of the 1st, 2nd and 3rd order *NTF*

2.4.2 Placement of the *NTF* Zeros of 2nd-order $\Delta\Sigma$ Modulator

Compared with first-order architecture, the second-order architecture has more design parameters available: the integrator gain factors in the feedback paths [4].

The resolution can be improved by adding additional feedback loops to the conventional architecture shown in Figure 2.6. Figure 2.8 depicts a second-order modulator with additional feedback loops. For a given oversampling ratio, there are optimum values for “ r_1 ” and “ r_2 ” that maximize the in-band quantization noise suppression. The use of “ r_1 ” and “ r_2 ” will shift the locations of the *NTF* zeros providing further suppression to the quantization noise, thereby improving the

resolution of a modulator. The detailed principle and methodology can be referred to [4].

Figure 2.8 Second-order modulators with additional feedback loops

The transfer function for the modulator is

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E(z) \quad (2.11)$$

where the NTF and STF are

$$NTF(z) = \frac{1 + (a_2 r_2 - 2) \cdot z^{-1} + (a_1 a_2 r_1 - a_2 r_2 + 1) \cdot z^{-2}}{1 + (a_2 b_2 + a_2 r_2 - 2) \cdot z^{-1} + (a_1 a_2 b_1 + a_1 a_2 r_1 - a_2 b_2 - a_2 r_2 + 1) \cdot z^{-2}}$$

$$STF(z) = \frac{a_1 a_2 \cdot z^{-2}}{1 + (a_2 b_2 + a_2 r_2 - 2) \cdot z^{-1} + (a_1 a_2 b_1 + a_1 a_2 r_1 - a_2 b_2 - a_2 r_2 + 1) \cdot z^{-2}} \quad (2.10)$$

when $a_1 = a_2 = 1$ and $r_1 = r_2 = r$, the NTF zeros can be obtained by solving

$$1 - (2 - r) \cdot z^{-1} + z^{-2} = 1 - 2 \cdot \cos \theta \cdot z^{-1} + z^{-2} = (1 - e^{-j\theta} \cdot z^{-1}) \cdot (1 - e^{j\theta} \cdot z^{-1}) = 0 \quad (2.12)$$

where r is equal to $2 \cdot (1 - \cos \theta)$. For example, $r=0.03843$ corresponds to a $\theta = \pi/16$.

Comparing the NTF in Eq. (2.12) with the one in Eq. (2.8), it can be seen that the zero location of the NTF is moved away from $z = 1$ to $z = e^{\pm j\theta}$. The PSD (power spectral density) of the modulators in Figure 2.6 and 2.8 using MATLAB simulation tools [10] are plotted in Figure 2.9.

Figure 2.9 PSD of the modulators in Figure 2.6 & 2.8

In a switched-capacitor implementation of the delta-sigma modulator, noise sources such as kT/C noise together with the input-referred opamp noise including the flicker noise ($1/f$) are present at the input of the modulator. These noise sources normally dominate the noise floor level at the low frequency region where the quantization noise is suppressed by multiple NTF zeros at DC of a high-order low-pass delta-sigma modulators. As a consequence, for wideband application the performance of the modulator will be limited by all those noises and it is intuitively better to spread the *NTF* zeros away from z -plane origin within the signal band.

2.4.3 High-order, Single-loop $\Delta\Sigma$ Modulator

The design of high-order, single-loop modulators can adopt the technique introduced in [11] [12] [13]. The coefficients of the transfer functions are usually

synthesized with traditional low-pass filter functions such as Butterworth or Chebyshev etc. This approach is an efficient way to design a high-order modulator with relatively guaranteed stability by the zero and pole locations in the unit circle. However, the coefficients of those transfer functions are normally difficult to make real implementation because of a large minimum to maximum ration.

It is well known that single-loop L^{th} -order ($L > 2$) $\Delta\Sigma$ modulators will probably run into instability problems [14] [15]. A $\Delta\Sigma$ modulator is considered stable when for a certain class of input signals, the states of the systems are bounded and the modulator is free from large signal limit cycles [16] [17]. Simulation results show that for single loop 1-bit quantization $\Delta\Sigma$ modulator, the 1st-order modulator will be always stable; the 2nd-order modulator will be conditionally stable [18], while the modulators with $L > 2$ will likely suffer from the stability problems [8] [19].

There are two kinds of stability considerations [20]. One is small signal stability and the other is large signal stability. For small signal stability, the loop is stable as long as all the poles are located inside the unit circle in the z-domain, which can be easily achieved by choosing appropriate coefficients for the *NTF*. However, the modulator may not work well even with the proper pole locations if any integrator is saturated or overloaded due to the effects of the feedback loop. In fact, this happens for most single-bit high-order modulators that have improper integrator gains. The question “Is my modulator stable?” still needs to be addressed by extensive behavioral simulation and some approximation methods [5]. Many analyses and studies [21] [22] [23] [24] [25] have been done in this field.

The stability problem can be effectively alleviated in the cascade and/or multi-bit delta-sigma modulators with well-defined integrator gains.

2.5 Cascade / Multi-stage / MASH $\Delta\Sigma$ modulators

As the order of the $\Delta\Sigma$ modulator is increased, stability becomes a significant problem. Robust stability of a 1st or 2nd order delta-sigma modulator is very desirable, while the performance is not as good as that needed in most of the applications. One solution to the stability problems of higher order $\Delta\Sigma$ modulator is to cascade several stages instead of a single loop, which is known as the cascade / multi-stage / MASH architecture [5] [8] [26]. One important merit of cascade topology is that it can be absolutely stable. Cascading first and second order modulators form a stable high-order modulator. Therefore, MASH architecture is often used for the design of high-order $\Delta\Sigma$ systems. The architecture shown in Figure 2.10 demonstrates the cascade or multi-stage (MASH) $\Delta\Sigma$ modulators. Each stage in Figure 2.10 is an L^{th} -order (usually $L=1$ or 2) single loop modulator with its own quantizer and feedback loops. The quantization error from the preceding stage of modulator is converted and fed into the next one. The digital outputs of each stage modulators are combined and processed in a digital error cancellation network to produce the final digital output. The quantization errors from all stages except the last one are cancelled in the final digital output after going through the digital error cancellation network. With perfect matching, the final output $Y(z)$ contains only the input signal $X(z)$ and the noise-shaped last stage quantization error $E_N(z)$.

Figure 2.10 Cascade delta-sigma architecture

To get the proper transfer functions of ECN that can meet these requirements, an example of three-stage cascade delta-sigma modulator is as shown in Figure 2.11.

Figure 2.11 Block diagram of the three-stage cascade $\Delta\Sigma$ modulator

Where each stage input X_N is given by

$$\begin{aligned}
 X_n(z) &= X(z), & n &= 1 \\
 &= g_{(n-1)} \cdot \left[(1 - l_{(n-1)}) \cdot Y_{(n-1)}(z) - E_{(n-1)}(z) \right], & n &= 2, 3
 \end{aligned} \tag{2.13}$$

The transfer function of each stage delta-sigma modulator is given by

$$\begin{aligned}
 Y_n(z) &= STF(z) \cdot X_n(z) + NTF(z) \cdot E_n(z) \\
 &= \frac{S_n(z)}{D_n(z)} \cdot X_n(z) + \frac{N_n(z)}{D_n(z)} \cdot E_n(z)
 \end{aligned}
 \tag{2.14}$$

where $n = 1, 2, 3$.

Except for the first stage input which is the overall modulator input signal $X(z)$, the input of each stage $X_n(z)$ is related to the previous stage output $Y_{(n-1)}(z)$ and quantization noise $E_{(n-1)}(z)$ and it is scaled by a gain factor of $g_{(n-1)}$ except the first stage input is the overall modulator input signal $X(z)$. The parameter $g_{(n-1)}$ is introduced to scale the input signals of the second and third stage so as to prevent overloading of the integrators. $S_n(z)$ and $N_n(z)$ are the numerators of the STF and NTF respectively. $D_n(z)$ represents the denominator of the STF and NTF . The quantizer is modeled as a gain of one and an additive noise source $E_n(z)$ as illustrated in previous section.

To cancel the quantization noises $E_1(z)$ and $E_2(z)$, the digital error cancellation network should be suggested as:

$$\begin{aligned}
 H_1(z) &= S_2(z) \cdot S_3(z) \cdot [D_1(z) + (l_1 - 1) \cdot N_1(z)] \\
 H_2(z) &= \frac{1}{g_1} \cdot z^{-2} \cdot (1 - z^{-1})^2 \cdot [D_2(z) + (l_2 - 1) \cdot N_2(z)] \\
 H_3(z) &= \frac{1}{g_1 \cdot g_2} \cdot (1 - z^{-1})^2 \cdot N_2(z) \cdot D_3(z)
 \end{aligned}
 \tag{2.15}$$

Actually, the above equations provide a general ECN transfer function for the cascade delta-sigma modulator built as shown in Figure 2.11 regardless of the values of the inherent coefficients. The quantizers can be any bit one and each stage can be any order modulators.

The major advantage of the cascade architecture over a single loop one is its stability. Since cascade modulator architecture contains only feed forward paths and no feed back path between the individual stages, it will be stable if the individual stages are stable. Therefore, the cascade of several existing first-order or second-order modulators can be made inherently stable for any stages of modulators theoretically. The modulator requires scaling of internal signals to achieve better performance without overloading.

The order of the cascade modulators is the sum of the order of each stage. The performances and stabilities of the cascade modulators are generally better than the corresponding single-loop ones. For example, the performance of the two-one-one, two-two and three-one cascade structures described in [27] are better than the performance of a fourth-order single-loop modulator described in [28].

The performance of MASH modulators based on first or second-order integrator is compared here in the form of a fifth-order example. The design of a fifth-order MASH modulator can be accomplished in several different ways such as $1-2-2$, $2-1-2$ and $2-2-1$. Each provides fifth-order noise shaping while the level of the overall noise floor is different as can be seen from Figure 2.12. The architectures of $1-2-2$, $2-1-2$ and $2-2-1$ give SNDR of 92dB, 111dB and 119dB respectively when sampling frequency is 32MHz and oversampling ratio is 16.

Figure 2.12 PSD comparison of different architecture of 5th-order cascade $\Delta\Sigma$ modulator

Table 2.1 summarizes the results of various MASH designs realized using the first and second order $\Delta\Sigma$ modulators. From this table, a modulator can be chosen that has the properties required to meet.

Table 2.1 Summary of modulator structures and performances

Modulator Structure	NTF Order	SNDR (dB) at $M=16$
1 DSM	1	42
2 DSM	2	51
1-1 MASH	2	55
1-2 MASH	3	67

1-1-1 MASH	3	71
2-1 MASH	3	76
2-2 MASH	4	80
1-2-2 MASH	5	92
2-1-2 MASH	5	111
2-2-1 MASH	5	119
2-2-2 MASH	6	125.3

As mentioned before, for delta-sigma ADCs, the requirements on the accuracy of the analog components are not as severe as for a Nyquist rate ADCs. However, in cascade architectures, the performance is slightly more sensitive to the imperfections of the analog components. The reason is that in cascade modulators, the quantization errors are all theoretically cancelled in the error cancellation network. But in practice, the extent of quantization errors cancellation depends on how well the analog implementation of the integrator gain factors match with their counterpart in the digital error cancellation network. The imperfect cancellation caused by analog circuits' inherent non-idealities results in the quantization errors from the intermediate stages to leak to the final output of the ADCs. This noise leakage usually limits the overall performance of the cascade delta-sigma ADCs and makes it worse than expected [29]. If there is imperfect implementation in the first stage, the un-cancelled quantization error leaks to the output directly and is suppressed by the 1st-stage *NTF* only, so it could cause severe degradation in the quantization noise suppression.

2.6 Multi-bit $\Delta\Sigma$ modulators

Besides the cascade architectures, using multi-bit or multi-level ADC and DAC components instead of the single-bit quantizer could also potentially solve the

stability problem. The more stable a system, the larger is the allowable signal that can be applied to the input. Multi-bit modulators also lower the level of quantization noise in the output spectrum and further enhance the resolution of the $\Delta\Sigma$ modulators. The multibit $\Delta\Sigma$ modulator requires a multibit DAC feedback path as shown in Figure 2.13. It has typically 6dB increase of the system dynamic range for each additional one-bit increment of the quantizer. The popular use of single-bit quantizer results from the inherent linearity they offer. In 1-bit quantizer or comparator, there are only two output levels representing the input signal magnitude. While in an N -bit quantizer, the input signal is compared with 2^N-1 threshold simultaneously so that they track the input signal more accurately. However, this advantage is at the expense of component (especially DAC) accuracy, design complexity, and higher power consumption [30] [31].

Figure 2.13 A multibit $\Delta\Sigma$ modulator

One important problem that needs to be addressed in multi-bit $\Delta\Sigma$ modulator is the nonlinearity of the feedback DAC. The inherent linearity property is lost when using a multi-bit quantizer instead of a single-bit one. The amount of DAC errors in a modern VLSI process is no less than 0.1% [32] [33], limiting the implementation of a high-resolution system without adopting any correction techniques. The errors due to the DAC nonlinearity remain unshaped and enter the modulator at its input and will degrade the resolution of the $\Delta\Sigma$ modulator. Consequently, the signal-to-noise ratio suffers from the quantization nonlinearity due to the multi-bit

DAC. Numerous attempts to reduce the sensitivity to the DAC nonlinearities have been made. The requirement of a highly linear multi-level DAC demands extra precautions such as precisely matched components or additional trimming, calibrating, element matching schemes. Larson et al. proposed the use of digital correction to cancel it [30]. In recent years, various forms of dynamic element matching techniques have been used to alleviate the quantization non-idealities [30] [31] [34] [35] [36] [37] [38]. For multi-bit quantizer, the errors contain not only the unavoidable inherent quantization noise but also other errors such as offset, gain or non-linearity and so on [39]. Considering that the required accuracy of the multi-bit quantizer should be at least the same as the required dynamic range (DR) since the DAC errors directly add to the input without any noise shaping, linear quantizers such as 1-bit or 3-level quantizer is chosen to be the candidates in this work. The detailed model and information of 3-level quantizer can be found in chapter 3.

2.7 Design Rationale and Summary

The basic concepts of oversampling and noise shaping are briefly presented in this chapter. More detailed and thoroughly analysis can be found in [5] [8] [40].

As described in previous sections, there exists a large variety of architectures that can be chosen for delta-sigma modulators. Each structure has its own advantages and disadvantages. Table 2.1 provides the comparison of different types of $\Delta\Sigma$ architectures. A specific architecture can be chosen based on the requirements on oversampling ratio, resolution, circuit complexity, and circuit tolerances etc.

From equation (2.1), the signal bandwidth is given as $f_B = f_s / (2 \cdot M)$. It can be seen that to get wide signal bandwidth, the only way is to use lower oversampling ratio (M) for a certain decided sampling frequency.

For low M , high order, cascade and multi-bit architectures are preferred according to the comparison listed in Table 2.2. The MASH structures significantly lessen the constriction on the stability of high-order loop, so they are the good candidates for high accuracy and high speed performance. The multi-bit structures have more complex circuitry and are very sensitive to the imperfections of component DAC. Since the multi-bit architectures have the DAC errors that need extra efforts to eliminate, 1-bit or 3-level quantizers that are inherently linear will be used. 3-level instead of 1-bit quantizer was used in each stage of the modulator to obtain better performance while maintaining the linearity. On the other hand, the second-order delta-sigma architecture is insensitive to circuit non-idealities and parameter variations. Its stability is also guaranteed over the full analog input range. In this work, a 6th-order three-stage cascade with 3-level quantizer delta-sigma modulator is proposed for operation at low oversampling ratio of 4, 6, 8, 12 and 16. Together with varying some of the parameters in tandem with different oversampling ratios, this modulator is suitable for multi-standard and wideband applications.

In this work, cascade architecture with 3-level quantizer is used to achieve multiple and wide bandwidth $\Delta\Sigma$ modulator. It is believed that if the multi-bit quantizer is adopted in this proposed programmable modulator, the resolution for each signal bandwidth will be improved. The sacrifices are high power consumption and more circuit design complexity. How to trade-off these factors and improve the performance of the overall system can be one of the future works need to be investigated.

The detailed architecture of the proposed delta-sigma modulator will be presented in the next chapter. The comparison of our modulator and other state-of-the-art modulators can be found in chapter 6 in terms of overall performance.

Table 2.2 Comparison of $\Delta\Sigma$ architectures

	ADVANTAGES	DISADVANTAGES
Single-loop, 1-bit low order	<ul style="list-style-type: none">• Stability• Simple circuit• Large input signal range	<ul style="list-style-type: none">• Very high M needed• Limited resolution obtained
Single-loop, 1-bit high order	<ul style="list-style-type: none">• Good performance for low M• Simple quantization component	<ul style="list-style-type: none">• Poor stability• Small input signal range
Cascade / Multi-stage / MASH	<ul style="list-style-type: none">• Good performance for low M• Guaranteed stability• Large input signal range	<ul style="list-style-type: none">• Sensitivity to the component mismatch
Multi-bit	<ul style="list-style-type: none">• Good performance for low M• Good stability	<ul style="list-style-type: none">• Sensitivity to the non-linearity of the DAC component• Complexity of both the digital and the analog circuit

Chapter 3

System Level Design

Based on the previous literature review, a 6th-order cascade delta-sigma analog-to-digital converter (ADC) is chosen for operating at low oversampling ratios (M) of 4, 6, 8, 12 and 16. In the 6th-order $\Delta\Sigma$ architecture, 3-level quantizer will be used in each of the stage. This chapter focuses on the system level design of the proposed multi-standard and wideband $\Delta\Sigma$ modulator and it provides the basic foundation to the following IC design implementation works.

3.1 Introduction

The performance of an ADC can be described by a number of specifications [41]. Some of the most important specifications used to specify the behavior of a delta-sigma modulator are briefly discussed here [42].

- Signal to Noise Ratio (SNR). The SNR of a converter is the ratio of the signal power to the noise power, measured at the output of the converter for certain input amplitude. The maximum SNR is called the peak signal-to-noise ratio.
- Signal to Noise and Distortion Ratio ($SNDR$). The $SNDR$ of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for certain input amplitude. The maximum $SNDR$ a converter can achieve is called the peak signal-to-noise-and-distortion ratio.
- Dynamic Range (DR). The DR is the ratio between the power of the maximum input signal that can be applied and the minimum input signal that can be detected. For an ideal delta-sigma analog to digital converter

with a full scale input range of $\pm\Delta$, relationship among the dynamic range (DR), oversampling ratio (M), order of the modulator (L), number of quantizer bits (B) can be approximated as [43]:

$$DR = \frac{\frac{\Delta^2}{2}}{\frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{M}\right)^{2L+1} \cdot \frac{\Delta^2}{3} \cdot \left(\frac{1}{2^B - 1}\right)^2} \quad (3.1)$$

$$= \frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}} \cdot M^{2L+1} \cdot (2^B - 1)^2$$

- Effective resolution. The effective resolution of an A/D converter is a number of bits (b) that indicates the same performance of an ideal quantizer. It can be calculated as

$$b = \frac{SNDR_{\max} - 1.76}{6.02} \quad (3.2)$$

Figure 3.1 Illustration of SNR, SNDR and DR

These specifications can be obtained from spectral analysis of the measured ADC output by performing a fast Fourier Transform (FFT) to the captured digital output data. Figure 3.1 illustrates some of the frequently used performance metrics such as the *SNR*, *SNDR* and *DR*.

To provide an insight to the evaluation of the performance of state-of-the-art delta-sigma modulator with experimental results published in literature, one of the factors named as figure of merit (*FOM*) is introduced as:

$$FOM = \frac{P}{2^b \cdot BW} \quad (3.3)$$

where P is the power dissipation, b is the effective resolution which can be obtained from Eq. (3.2) and BW is the Nyquist rate output bandwidth.

In the delta-sigma modulation, the sampling rate is usually much higher than the Nyquist rate as presented in chapter 2. Considering power consumption and technology used, the sampling rate cannot be too high. Hence for wideband application, low M is used for a given certain sampling frequency. There are only two choices left to achieve high dynamic range. For low M , it has been studied that using a single-loop single-bit delta-sigma modulator cannot obtain satisfactory results [44]. The peak *SNDR* of an L^{th} order delta-sigma modulator improves by $(6L+3)$ dB or $(L+0.5)$ bits per octave increase in the oversampling ratio M . In addition, there are stability issues associated with a high order single loop architecture which makes a second-order modulator more appropriate. Furthermore, multi-bit structures have more complex circuitry and are less tolerant to circuit imperfections especially the errors due to the multi-bit DAC. Comparing with 1-bit quantizer, 3-level quantizer can improve the modulator performance while maintaining the linearity characteristic. Therefore, the proposed modulator is 2-2-2 cascade with 3-level quantizer delta-sigma modulator. The stability of the modulator is effectively guaranteed by using multiple stage cascades of 2nd-order architectures inside. Moreover, each of the stage has the additional feedback to

optimize the *NTF* zero so as to provide more suppression of the noise level as described in section 2.4.2.

3.2 The proposed 2-2-2 Cascade Architecture

The whole block diagram of the 2-2-2 cascade architecture is illustrated in Figure 3.2. For all the signals presented in the z -domain, $X(z)$ is the analog input signal. $Y(z)$ is the final digital output of the whole system and $Y_1(z)$, $Y_2(z)$, $Y_3(z)$ are the digital outputs of individual stage. There are three stages in this modulator and every stage is a second-order delta-sigma modulator with its own quantizer inside. Three-level quantizer is used in all the 1st, 2nd and 3rd stage. The digital output of each stage $Y_1(z)$, $Y_2(z)$, $Y_3(z)$ will then be passed through a digital error cancellation network to come up with the final digital output $Y(z)$ of the whole system. The digital error cancellation network is formed by $H_1(z)$, $H_2(z)$ and $H_3(z)$. The detailed information of each component of the system will be presented in the following sections.

For the cascade 2-2-2 MASH delta-sigma modulator, a series of simulation has been performed to ascertain the proposed modulator can obtain the best performance while avoiding the overloading problem in each subsequent stage. Besides the tradeoff between good performance and non-overloading of the whole system, the ease of implementing the digital error cancellation network must also be considered. The final choices of parameter values are presented in Table 3.1. As can be seen from the table, the values of the parameters are chosen as 2's power so as to ease the implementation in the digital domain.

Figure 3.2 Block diagram of the proposed 2-2-2-cascade $\Delta\Sigma$ modulator

Table 3.1 Coefficients settings of the modulator in Fig. 3.2

M	r_2	r_3	g_1	g_2	l_1	l_2	$b_1 = b_2 = b_3$
4	2^{-2}	2^{-1}	0.5	1	2	1	2
6	2^{-3}	2^{-2}					
8	2^{-4}	2^{-3}					
12	2^{-5}	2^{-4}					
16	2^{-6}	2^{-5}					

3.2.1 Three-level Quantizer

Before going into each stage of the modulator, it is appropriate to first describe the three-level quantizer used.

To analyze any quantizer, one of the crucial issues is the quantization noise. Many of the insights have been presented in [6]. One-bit quantizer has been widely used in delta-sigma modulators due to its inherent linearity [45] [46]. Many different approaches have been proposed to model the one-bit quantizer to better understand the behavior of the modulator [40] [47] [48]. The most commonly used approach is the linear model method which models the quantizer as a gain of one and an additive noise source $E(z)$. In one-bit quantizer or comparator, there are only two fixed output levels representing the input signal magnitude. Therefore, it can be modeled as a gain of one and an additive noise source $E(z)$ that symbolizes the unavoidable inherent quantization noise. In order to make the input signal to be tracked more accurately while maintaining linearity, it is suggested to use a three-level quantizer instead of one-bit one in each stage of the proposed delta-sigma modulator [49]. Now, just like one-bit quantizer, the output of three-level quantizer have the fixed three analog output levels whose middle-level output is the average of two extreme outputs and therefore it is also inherently linear.

Normally, the three output voltage levels are $+V_{dd}$, $-V_{dd}$ and ground for fully-differential circuits. Therefore the three-level quantizer can be likewise modeled as a gain of one and an additive noise source $E(z)$ [50] as shown in Figure 3.3.

Figure 3.3 Linear model of 3-level quantizer in a 1st-order $\Delta\Sigma$ modulator

In contrast to this, if multi-bit DAC is used, one has to consider the linearity issues as the resolution of the modulator is limited by the accuracy of the multi-bit DAC in the feedback path. As will be shown in the circuit implementation, the modulator can employ a 3-level DAC without linearity problem.

3.2.2 Error Cancellation Network (ECN)

To get the final output of the modulator Y , the output of each stage Y_1 , Y_2 and Y_3 need to pass through the digital error cancellation network (ECN) before being summed up together to form the final output. This network includes three digital circuit building blocks H_1 , H_2 and H_3 . As presented in chapter 2, the main purpose of this digital error cancellation network is to cancel the quantization noises E_1 and E_2 generated from first and second stage while remain the quantization noise E_3 produced from the last stage.

The transfer function of each stage delta-sigma modulator is given by

$$\begin{aligned}
 Y_n(z) &= STF(z) \cdot X_n(z) + NTF(z) \cdot E_n(z) \\
 &= \frac{S_n(z)}{D_n(z)} \cdot X_n(z) + \frac{N_n(z)}{D_n(z)} \cdot E_n(z) \\
 &= \frac{g_{n-1}z^{-2}}{1+(r_n+b_n-2)z^{-1}+(2-b_n)z^{-2}} \cdot X_n(z) + \frac{1+(r_n-2)z^{-1}+z^{-2}}{1+(r_n+b_n-2)z^{-1}+(2-b_n)z^{-2}} \cdot E_n(z)
 \end{aligned} \tag{3.4}$$

where $n = 1, 2, 3$ and $r_1 = 0$.

According to the method introduced in section 2.5 and extending the Eq. 2.15, one can get the ECN equations for the proposed 2-2-2-cascade modulator:

$$\begin{aligned}
 H_1(z) &= z^{-4}[(l_1 - 1)(1 - z^{-1})^2 + 1] \\
 &= 2 \times z^{-4} - 2 \times z^{-5} + z^{-6}
 \end{aligned} \tag{3.5}$$

$$\begin{aligned}
 H_2(z) &= \frac{1}{g_1} z^{-2} (1 - z^{-1})^2 \{(l_2 - 1)[1 - (2 - r_2)z^{-1} + z^{-2}] + r_2 z^{-1} + 1\} \\
 &= 2 \times [z^{-2} + (r_2 - 2) \times z^{-3} + (1 - 2 \times r_2) \times z^{-4} + r_2 \times z^{-5}]
 \end{aligned} \tag{3.6}$$

$$\begin{aligned}
 H_3(z) &= \frac{1}{g_1 g_2} (1 - z^{-1})^2 (1 + r_3 z^{-1}) [1 - (2 - r_2)z^{-1} + z^{-2}] \\
 &= 2 \times [(r_2 + r_3 - 4) \times z^{-1} + (r_2 \times r_3 - 2 \times r_2 - 4 \times r_3 + 6) \times z^{-2} + \\
 &\quad (-2 \times r_3 \times r_2 + r_2 + 6 \times r_3 - 4) \times z^{-3} + (r_2 \times r_3 - 4 \times r_3 + 1) \times z^{-4} + r_3 \times z^{-5}]
 \end{aligned} \tag{3.7}$$

This error cancellation network is the only pure digital part of the whole system. Besides the tradeoff between good performance and non-overloading, we also consider the convenience of implementing the digital error cancellation network by using the integer power of 2 factors. b_1 to b_2 are chosen to be 2 as in a typical 2nd-order delta-sigma modulator [45]. r_2 and r_3 determine the locations of the noise

transfer function zeros and their values are different for each different oversampling ratio which are given in Table 3.1.

3.2.3 System Transfer Function

Combining the three stage outputs with the digital cancellation network transfer functions and synthesizing all the equations, one can obtain the overall output of the system $Y(z)$.

$$\begin{aligned}
 Y(z) &= H_1(z) \cdot Y_1(z) + H_2(z) \cdot Y_2(z) + H_3(z) \cdot Y_3(z) \\
 &= STF(z) \cdot X(z) + NTF(z) \cdot E(z) \\
 &= z^{-6} \cdot X(z) \\
 &\quad + \frac{1}{g_1 g_2} (1 - z^{-1})^2 [1 - (2 - r_2)z^{-1} + z^{-2}] \cdot [1 - (2 - r_3)z^{-1} + z^{-2}] \cdot E_3(z)
 \end{aligned} \tag{3.8}$$

From equation (3.10), it can be found that the final digital output of the system only consists of a delayed version of the analog input $X(z)$ and the 6th-order noise shaped quantization noise $E_3(z)$. With ideal matching, the quantization noises $E_1(z)$ and $E_2(z)$ generated from the 1st-stage and 2nd-stage are completely eliminated from the final output.

It should be noticed that there is a gain factor of $1 / (g_1 \cdot g_2)$ in front of the desired 6th order NTF . In this design, $g_1 = 0.5$ and $g_2 = 1$, the quantization noise will be boosted by a factor of 2.

3.3 Parameter Settings

To facilitate the implementation of the digital error cancellation network as described in section 3.2.2, it is convenient to choose all the parameters as 2's power

of integer number. In this section, the system is considered under linear condition and only quantization noise is taken into account. The input signal level is set to -3dBFS , which is normalized to the full scale of the feedback level $[-0.5, 0.5]$.

For multi-standard applications, the proposed WDSM is able to operate at different oversampling ratio M so as to get various signal bandwidth and resolution. Based on the optimum quantization noise shaping [51] and the system transfer function (3.11), the values of r_2 and r_3 can be determined by dividing or multiplying 2's power for different M . The concept of spreading the *NTF* zeros within the signal bandwidth to better suppress the quantization noise for better *SNDR* performances is presented in [4]. b_1 , b_2 and b_3 are set as $b_1 = b_2 = b_3 = 2$ in this work.

In order to maximize the signal ranges available within the entire system, it is necessary to apply internal signal scaling before saturation or overloading to avoid internal state information loss. The 2-2-2-cascade architecture has been mapped to an equivalent structure as shown in Figure 3.4 that can be implemented using switched-capacitor circuits. It can be seen that the scaled version of the modulator shown in Figure 3.4 is functionally identical to the original version shown in Figure 3.2 once the parameters satisfy the expressions provided in Eq. (3.9).

Figure 3.4 2-2-2-cascade architecture implementation

$$a_{bn} = b_n a_{n1} a_{n2} \qquad , n = 1,2,3$$
$$a_{m1} = \frac{r_n}{a_{n2}} \qquad , n = 1,2,3$$
$$a_{m2} = r_n \qquad , n = 1,2,3$$
$$a_{v1} = \frac{g_1 a_{21}}{a_{11} a_{12}} \tag{3.9}$$
$$a_{v2} = \frac{g_2 a_{31}}{a_{21} a_{22}}$$
$$a_{y1} = l_1 g_1 a_{21}$$
$$a_{y2} = l_2 g_2 a_{31}$$

Using the parameter values listed in Table 3.1 and Eq. (3.9), the integrator gain factors for the actual implementation can be determined following a simulation procedure similar to [52]. Table 3.2 summarizes the integrator gain factors for the switched-capacitor implementation of the proposed 2-2-2 MASH delta-sigma modulator as shown in Fig.3.4. It is worth noting that the scaling coefficients should be made as large as possible for larger signal-to-noise ratio.

Table 3.2 Final choice of integrator gain factors for the proposed delta-sigma modulator

M	a_{r21} = a_{r32}	a_{r22}	a_{r31}	a_{v1}	a_{y1}	a_{v2}	a_{y2}	$a_{11} = a_{21}$ = a_{31}	$a_{12} = a_{22}$ = a_{32}	$a_{b1} = a_{b2}$ = a_{b3}
4	2^{-1}	2^{-2}	2^0	1	0.2	2	0.2	0.2	0.5	0.2
6	2^{-2}	2^{-3}	2^{-1}							
8	2^{-3}	2^{-4}	2^{-2}							
12	2^{-4}	2^{-5}	2^{-3}							
16	2^{-5}	2^{-6}	2^{-4}							

Altering the values of a_{r21} , a_{r22} , a_{r31} and a_{r32} shifts the zeros location of NTF according to different M .

Upon performing internal signal scaling as shown in Figure 3.4, the probability distribution of each integrator output are plotted in Figure 3.5. The input level is set to -3dBFS, equivalent to the input level at which peak SNDR of the real implementation occurs. From these plots, it can be seen that the signal range of each integrator output is well controlled within the full scale of the quantizer feedback level which was normalized to $[-1, 1]$.

(a)

(b)

(c)

(d)

Figure 3.5 Probability distribution of each integrator output at -3dBFS input level

3.4 Simulation Results of the Ideal System

In this section, the simulation results are based on ideal condition and only quantization noise is considered. The input signal level is -3dBFS , which is normalized to the full scale of the quantizer feedback level.

The full SIMULINK model of the proposed delta-sigma modulator is as shown in appendix A1. By setting all the parameters as shown in Table 3.2, the frequency responses and zero-pole plot of the proposed WDSM *NTF* are shown in Figure 3.6 (a) and (b). It is obvious that the noise shaping is as desired and the zeros of the *NTF* are spreading along the unit circle achieving better noise suppression within the signal band. Each oversampling ratio corresponds to six different pairs of zeros. With a sinusoidal input frequency of 250 kHz , the power spectral density of the modulator's output for different values of M is plotted in Figure 3.7. The input magnitude is at -3dBFS and 65536 numbers of samples are collected. The sampling frequency is 64 MHz . It can also be seen from Figure 3.7 that the desired quantization noise shaping is obtained for different oversampling ratio M . The noise level is higher for smaller M with wider signal bandwidth. The maximum signal band that can be achieved is $(0.25 \times f_s / 2)$ when M is equal to 4.

(a)

(b)

Figure 3.6 (a) Frequency responses and (b) zero-pole plot of the *NTF*

Figure 3.7 PSD of the modulator for different M for input rate of 250 kHz

Figure 3.8 Simulated $SNDR$ vs. input level of the proposed delta-sigma modulator for different M

The simulated dynamic range (DR) including only quantization noise of this architecture for different M are 53dB, 74dB, 94dB, 115dB and 132 dB respectively as shown in Figure 3.8. The rest of the noise budget for the modulator will be reserved for thermal noise and various non-idealities such as mismatch, amplifier settling and slew rate which will be discussed in chapter four.

Table 3.3 Modulator performance including only quantization noise

M	4	6	8	12	16
DR	53.3 dB	74.2 dB	93.8 dB	115 dB	131.5 dB
Overload input level	-1 dBFS	-1 dBFS	-1 dBFS	-1 dBFS	-1 dBFS
Peak $SNDR$	51.7 dB	73.3 dB	92.5 dB	112.7 dB	125.3 dB

3.5 Summary

This chapter presents the detailed system level information of the proposed 6th-order MASH delta-sigma modulator that can support both the multi-standard and wide signal band applications. To prevent the excessive signal growth at the integrator outputs, the internal signal scaling in the form of integrator gain scaling is performed and final choice of values for the actual switched-capacitor circuit implementation is given. After introducing each component and coefficients of the proposed WDSM, the resulting final system transfer function is furnished. The simulation results for the linear system established so far are also provided to assure the desired performance of the proposed delta-sigma modulator.

Based on the system structure described in this chapter, the design methodology and the consideration for transistor level implementation of the proposed modulator will be given in the following chapters.

Chapter 4

Modulator Design Considerations

The integrators or loop-filters within a delta-sigma modulator can be implemented either by a discrete sampled-data system or in the continuous-time (CT) domain. A discrete sampled-data system can either be implemented using switched-capacitor (SC) or switched-current (SI) [53] techniques. The performance of SI circuits is limited by the non-idealities such as charge injection, non-linear settling, channel length modulation and transistor noise sources [54]. In addition, it has been shown in [55] that SI circuits have inferior power efficiency especially in low-voltage design compared to circuits implemented using SC technique. For CT implementation, normally a linear RC integrator is required. The on-chip resistors with very high linearity are difficult to achieve in standard CMOS process. The time-constant of CT integrator is a product of the resistor and capacitor, which will suffer from process variations. To minimize the thermal noise, the resistors in CT circuit need to be kept as small as possible. For the same time constant, reducing resistor necessitates the use of large capacitors. Consequently, the chip area and power consumption are also increased. As such, the modulator in this work was decided to be implemented by using the SC technique [56] [57].

To transfer the modulator from schematic to switched-capacitor circuit, the effects of circuits' non-idealities must be considered in advance. These non-idealities include various circuit noise sources, integrator non-idealities and parameters mismatches. They can be modeled using Verilog-A when doing circuit simulation. In this chapter, the methodology used in the design of a delta-sigma ADC will be discussed in detail.

4.1 Operational Amplifier Requirements

One of the most important components in the switched-capacitor implementation of a delta-sigma modulator is the operational transconductance amplifier (OTA). The main characteristic of an operational amplifier in linear active operation is that of creating a virtual ground, a node with constant dc voltage that does not draw any current. This requires a linear, low-noise, high open loop DC gain amplifier. Moreover, the amplifier time constant has to be low enough to ensure settling within the specified accuracy.

4.1.1 DC Gain

The transfer functions obtained in chapter 3 have been derived based on the assumption that the opamp has infinite DC gain. In the actual circuit implementation, the opamp cannot have infinite dc-gain. The finite DC gain of OTA results in integrator noise leakage, which degrades the noise-shaping performance of the delta-sigma modulator. The finite DC gain of the opamp in integrators has the effect of providing only a finite suppression of quantization noise at lower frequencies, resulting in flattening of the noise floor as shown in Figure 4.1.

Figure 4.1 Illustration of the effect of integrator leakage on the *NTF*

A single ended switched-capacitor integrator is shown in Figure 4.2. The integrator consists of one operational amplifier (opamp), four switches and two capacitors. Capacitor labeled C_p represents the input parasitic capacitance. The circuit operating principle is as follows: when ϕ_1 is high, capacitor C_s is charged to $C_s \times V_{in(n)}$. When ϕ_2 is high, the charge stored on C_s is transferred to C_f . Assuming that all the analog components used in this integrator are ideal, the integrator has a transfer function in the z -domain as:

$$H(z) = \frac{C_s}{C_f} \cdot \frac{z^{-1}}{1 - z^{-1}} \quad (4.1)$$

Figure 4.2 A single ended switched-capacitor integrator

Suppose an OTA with a dc-gain of A_0 is used, this finite dc-gain prevents the charge sampled on C_s from being completely transferred to the integrating capacitor C_f . As a consequence, this results noise leakage and distortion. The integrator transfer function derived based on charge conservation in z -domain is as follow:

$$I(z) = \frac{C_s}{C_f} \cdot \frac{(1 - \epsilon_m) \cdot z^{-1}}{1 - (1 - \epsilon_p) \cdot z^{-1}} \quad (4.2)$$

where

$$\begin{aligned}
\varepsilon_m &= \frac{1 + a_1 + a_p}{1 + a_1 + a_p + A_0} \\
\varepsilon_p &= \frac{a_1}{1 + a_1 + a_p + A_0} \\
a_1 &= \frac{C_s}{C_l} \\
a_p &= \frac{C_p}{C_l}
\end{aligned} \tag{4.3}$$

The resulting effect of the finite dc-gain is to introduce a gain error and to shift the pole slightly off the unit circle. The noise shaping is degraded from the ideal shaping $(1 - z^{-1})^{-1}$ and hence the quantization noise level in the signal band is increased. Figure 4.3 shows the MATLAB simulated output power spectral densities of a 2nd-order modulator when the amplifiers have a DC gain of 30dB and 100dB. The effect of the DC gain of the amplifiers on the noise floor is obvious.

Figure 4.3 Simulated quantization noise leakage due to opamp finite DC gain for a 2-2 cascade modulator. The input signal is a -10dBFS, 250 kHz sine wave, and the sampling frequency is 64MHz.

Taking into account the finite DC gain of the operational amplifier, the output transfer function of the first order delta-sigma modulator shown in Eq. (2.5) can be rewritten as:

$$\begin{aligned} Y(z) &= z^{-1} \cdot X(z) + [1 - (1 - \varepsilon_p) \cdot z^{-1}] \cdot E(z) \\ &= z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) + \varepsilon_p \cdot z^{-1} \cdot E(z) \end{aligned} \quad (4.4)$$

where the last term of Eq. (4.4) shows that there is an unshaped quantization noise leakage with a gain factor of ε_p proportional to the reciprocal of A_0 at the final output expression.

4.1.2 Linear Settling and Slew Rate

In SC circuits, the SC integrator should completely settle down during the integration phase so that the settling error will not degrade the modulator performance. The settling speed performance is usually specified for a small input signal and large input signal with gain bandwidth (GBW) and slew rate (SR). The parameters GBW and SR are directly related to the drawn current. SR is the maximum rate at which an amplifier output can be driven between limits in response to a step change in input voltage while accurately reproducing the input waveform.

Considering the switched-capacitor integrator as shown in Figure 4.2 including the input parasitic capacitor C_P and output load capacitor C_L , during the charge transfer phase the speed of the charge transfer is limited by a maximum rate of change known as the slew rate as well as an exponential response normally referred to as the linear settling of the opamp. Normally, the change of the output is first limited by the slew rate and followed by the linear settling period. It should be pointed out that the capacitive load seen during slewing is always smaller than the capacitive load seen during linear settling. The exact settling and slew rate depend on the implementations of the opamp and integrator. For simplification, the opamp can be

modeled as a single transistor with a transconductance of g_m in the SC integrator as shown in Figure 4.4.

Figure 4.4 Opamp modeled as a single transistor in a SC integrator

Assuming the time constant formed by the switch on-resistance and the sampling capacitor during sampling period is much smaller than the reciprocal of the opamp bandwidth, the transfer function of the circuit in Figure 4.4 can be derived in s -domain as:

$$\frac{V_o(s)}{V_i(s)} = \frac{C_s}{C_l} \cdot (1 - \varepsilon_m) \cdot \frac{1 - \frac{s}{z}}{1 + \frac{(1 - \varepsilon_m) \cdot s}{p}} \quad (4.5)$$

where

$$\begin{aligned}
 z &= \frac{g_m}{C_I} \quad ; \\
 p &= \frac{g_m}{C_S + C_P + C_L \cdot \left(1 + \frac{C_S}{C_I} + \frac{C_P}{C_I}\right)} \quad ; \\
 \varepsilon_m &= \frac{C_I + C_S + C_P}{C_I + C_S + C_P + C_I \cdot A_0}
 \end{aligned} \tag{4.6}$$

If a step input is applied, there is a right half plane zero z that will provide a direct feed through path and will degrade the settling behavior of the circuit. The pulse response of the integrator can be derived in the time domain as:

$$V_o(t) = \frac{C_S}{C_I} \cdot (1 - \varepsilon_m) \cdot \left[1 - \left(1 + \frac{p}{(1 - \varepsilon_m) \cdot z} \right) \cdot e^{-\frac{pt}{(1 - \varepsilon_m)}} \right] \tag{4.7}$$

$$\text{when } t = 0, \quad V_o(0) = -\frac{C_S}{C_I} \cdot \frac{p}{z}$$

$$\text{when } t \rightarrow \infty, \quad V_o(\infty) = \frac{C_S}{C_I} \cdot (1 - \varepsilon_m)$$

It is obvious that the presence of z will introduce larger signal swing requirement of $(C_S/C_I) \cdot (1 + p/z)$ instead of (C_S/C_I) which means that the output will take longer time to get to the desired value.

The next non-ideality that needs to be considered is the effect of opamp slew rate (SR). Using similar method introduced in [47], the asymptotic step change of the output voltage of Figure 4.4 during charge transfer phase ϕ_2 can be derived using the following expression:

$$Y_a = V_o(\infty) - V_o(0) = \frac{C_S}{C_I} \cdot (1 - \varepsilon_m) \cdot \left[1 + \frac{p}{(1 - \varepsilon_m) \cdot z} \right] \cdot V_i \tag{4.8}$$

At the end of charge transfer phase $t = t_s$,

$$V_o(t_s) = \begin{cases} V_o(0) + Y_a \cdot \left(1 - e^{-\frac{t_s}{\tau}}\right) & , |Y_a| \leq \tau \cdot SR \\ V_o(0) + Y_a - \text{sgn}(Y_a) \cdot \tau \cdot SR \cdot e^{\left(\frac{|Y_a|}{\tau \cdot SR} - \frac{t_s}{\tau}\right)} & , \tau \cdot SR < |Y_a| \leq (\tau + t_s) \cdot SR \\ V_o(0) + \text{sgn}(Y_a) \cdot \tau \cdot SR & , |Y_a| > (\tau + t_s) \cdot SR \end{cases} \quad (4.9)$$

where sgn is the sign function, SR is the opamp slew rate and τ is the circuit settling time constant inferred in the exponential term of Eq. (4.7). The charge transfer phase duration t_s is normally less than half of the sampling period as there are two non-overlapping clock phases ϕ_1 and ϕ_2 required in the implementation of the circuit.

Taking into account the finite DC gain A_0 as well as the opamp settling speed effects and applying superposition principle, the overall sampled data output voltage can be expressed as:

$$V_o(n) = \begin{cases} V_{io}(n-1) + Y_a \cdot \left(1 - e^{-\frac{t_s}{\tau}}\right) & , |Y_a| \leq \tau \cdot SR \\ V_{io}(n-1) + Y_a - \text{sgn}(Y_a) \cdot \tau \cdot SR \cdot e^{\left(\frac{|Y_a|}{\tau \cdot SR} - \frac{t_s}{\tau}\right)} & , \tau \cdot SR < |Y_a| \leq (\tau + t_s) \cdot SR \\ V_{io}(n-1) + \text{sgn}(Y_a) \cdot \tau \cdot SR & , |Y_a| > (\tau + t_s) \cdot SR \end{cases} \quad (4.10)$$

where $(n-1)$ denotes the previous sample and

$$V_{io}(n-1) = V_o(n-1) - \frac{C_s}{C_i} \cdot \frac{p}{z} \cdot V_i(n-1) \quad (4.11)$$

The simulation results in [52] have shown that high-resolution performance may be obtained in two possible settling regimes: the slow regime and fast regime. In the slow regime, no slew limiting occurs, and the settling time constant acts as an equivalent gain error. There is a lower limit on both the SR and τ . The slow regime depends on the settling being linear, and any deviation from linear setting degrades

the modulator's performance. While in fast regime, although the integrator is strongly slew rate limited, the amplifier settling is sufficiently fast to cancel the nonlinear effects of the slew limiting to negligible levels.

When a fully differential folded cascode opamp is used to construct an integrator, the slew rate and settling time constant are related by:

$$\tau \cdot SR = \left(1 + \frac{C_S}{C_I} + \frac{C_p}{C_I}\right) \cdot \frac{V_{gs} - V_{th}}{2} \quad (4.12)$$

where C_p , C_S and C_I are the parasitic capacitance, sampling capacitance and integration capacitance respectively. V_{gs} is the gate-to-source voltage and V_{th} is the threshold voltage of the input transistors. It is obvious that in order to achieve high slew rate and large settling time constant simultaneously, it is necessary to employ large value of the overdrive voltage ($V_{gs} - V_{th}$) which is especially difficult in a low supply voltage implementation such as the work in this thesis. In this design, an overdrive voltage of 0.15-V was chosen to provide large enough slew rate and wide output swing.

It is convenient to define the normalized slew rate and the number of settling time constants as:

$$SR_n = \frac{SR}{F} \cdot \frac{T_S}{2} \quad (4.13)$$

$$n_\tau = \frac{1}{\tau} \cdot \frac{T_S}{2} = p \cdot \frac{T_S}{2} \quad (4.14)$$

where T_S is the sampling period and F is the feedback level magnitude from modulator output, p is the closed loop pole given in Eq. (4.6).

In a switched-capacitor implementation, the effects of finite DC gain and limited settling time of the operational amplifier were revealed to directly degrade the noise transfer function of the modulator. Thus it will cause the out-of-band quantization noise leak into the signal band.

4.2 Circuit Noise Considerations

In practice, a number of noise sources and non-idealities have to be taken into account. There are two types of noise that are dominant in a delta-sigma modulator implementation: thermal and flicker noise (also known as $1/f$ noise). The former can be treated as a white noise with a power spectral density that is constant with frequency. The gate-referred thermal noise spectral density of a MOSFET with transconductance of g_m in saturation is $N_T = 8kT/(3g_m)$. Flicker noise has a power spectral density that is inversely proportional to frequency, depending on the bandwidth of interest and the implementation. It displays a spectral density that varies inversely with frequency. Thus the energy is concentrated at low frequencies. Some circuit techniques such as correlated double sampling [58] and chopper stabilization [59] [60] can be used to reduce $1/f$ noise. In general, $1/f$ noise is less of a concern for circuit designed for wideband applications.

4.2.1 Thermal Noise

Thermal noise is generated by a random thermal motion (Brownian motion) of carriers (electron, hole) in device. In SC circuit, the thermal noise is mainly generated by on-channel resistance of the switches. The spectral density of the thermal noise across a resistor R can be expressed as [61]:

$$V_{TR}(f) = 4kTR \quad , f \geq 0 \quad (4.15)$$

where k is Boltzmann constant ($k=1.38 \times 10^{-23} \text{ J/K}^{-1}$) and T is absolute temperature. During the sampling phase of the circuit shown in Figure 4.2, the circuit is modeled as a simple RC circuit connected to the noise source as in Figure 4.5.

Figure 4.5 Equivalent circuit during sampling phase of SC integrator

The spectral density noise output of the circuit, which is also the input noise of the integrator, is equal to:

$$\begin{aligned} S_o(f) &= S_R(f) \left| \frac{1}{1 + sRC_s} \right| \\ &= \frac{4kTR}{1 + \omega^2 R^2 C_s^2} \end{aligned} \quad (4.16)$$

Thus the total thermal noise power at the integrator input is

$$\begin{aligned} V_T &= \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{4kTR}{1 + \omega^2 R^2 C_s^2} d\omega \\ &= \frac{2kT}{\pi C_s} \tan^{-1}(\omega RC_s) \Bigg|_{\omega=0}^{\omega=\infty} \\ &= \frac{kT}{C_s} \end{aligned} \quad (4.17)$$

where C_s is the capacitance of the sampling capacitor.

It can be seen that the input noise power is independent of the resistor R . This is because even though R increases the noise power density, it also decreases the noise power bandwidth by the same amount.

Above, only the contribution from a single switch has been considered. In a practical SC integrator, several switches each contribute to the total noise generated by the integrator. Since their noise sources are uncorrelated, their powers add. Then the capacitor values should be as shown in the following equation.

$$V_T = N \cdot \frac{kT}{C_s} \quad (4.18)$$

where N is a constant for certain design. One can refer to [62] for details.

In the delta-sigma modulator, the total input-referred noise is dominated by the thermal noise at the first stage input node. As a consequence, the capacitor used in the first stage should be large enough to satisfy the dynamic range specification. The capacitor used in the subsequent stages can be downscaled, which can result in significant power saving. These capacitors are determined by matching

consideration rather than noise consideration, because the in-band thermal noise injected into the subsequent stage is suppressed by the high loop-gain [52].

The in-band thermal noise at the input node of a delta-sigma modulator is approximately given by:

$$V_T = \frac{N}{M} \cdot \frac{kT}{C_s} \quad (4.19)$$

where M is oversampling ratio.

4.2.2 Flicker Noise

Flicker noise is due to the irregular absorption and release of carriers in the traps that are formed by contamination, crystalline defects, etc within the emitter base depletion region. It is also known as $1/f$ noise because it has a power spectral density that is inversely proportional to the frequency. The flicker noise in a MOSFET device can be modeled by a voltage source connecting between the gate and source terminals of the transistor. The power spectral density of the source is given by:

$$N_F = \frac{K_f}{W \cdot L} \cdot \frac{1}{f} \quad (4.20)$$

where K_f is an experimental constant. The equivalent flicker noise is usually modeled as an independent noise with other noise sources such as thermal noise and it is independent of biasing conditions as well. The experimental constant K_f is highly process dependent and it is different for PMOS and NMOS device. Because it is believed that the $1/f$ noise is caused by a fluctuation in the number of carries in the active channel, a device with no current flowing through it has no $1/f$ noise. In SC circuit, those devices working as switches contribute negligible $1/f$ noise. As a consequence, in a SC circuit, $1/f$ noise is mainly considered in the opamps. The input-referred $1/f$ noise of a delta-sigma modulator is very close to the input-referred $1/f$ noise of the opamp in the first integrator. Due to the noise shaping argument, the contribution of opamps in the succeeding integrators to the overall $1/f$

noise of the delta-sigma modulator can be neglected. From Eq. 4.22, it is suggested to use large area MOSFET devices to reduce the $1/f$ noise. Owing to the large transistor sizes of the differential input pair of opamps, the $1/f$ noise contribution can be neglected. In addition, the wide input bandwidth relaxes the $1/f$ noise limits as compared to the modulators for lower frequency applications. Hence, the focus is to trade off the quantization noise and the thermal noise when designing and implementing the wide-band delta-sigma modulators.

4.2.3 Amplifier Noise

In addition to KT/C noise from the sampling switches, noise from the transistors used in the operational amplifier can also degrade the performance of the integrator. The input referred amplifier noise in the SC integrator can be modeled as shown in Figure 4.6.

Figure 4.6 Input referred amplifier noise in the SC integrator

Since ϕ_1 and ϕ_2 are two non-overlapping clock phases, the z -domain output of the integrator in Fig. 4.6 is

$$V_{out}(z) = \frac{1}{1-z^{-1}} \frac{C_s}{C_I} \left[z^{-1} V_{in}(z) + \Xi_{OTA}(z) + (1-z^{-1}) \frac{C_I}{C_s} \Xi_{OTA}(z) \right] \quad (4.21)$$

where $\Xi_{OTA}(z)$ represents the z -transform of the total amplifier noise σ_{OTA} , which will be derived in chapter 5.2. The first part of the equation is first-order spectrally shaped, so it does not significantly increase the noise floor as compared with the second and third portion.

With $1/f$ noise contribution neglected, the integrator in-band amplifier noise power referred to the input of the integrator is [62]

$$V_N^2 = \left[\frac{1}{M} + \left(\frac{C_I}{C_s} \right)^2 \cdot \frac{\pi^2}{3M^3} \right] \cdot \sigma_{OTA}^2 \quad (4.22)$$

where M is the oversampling ratio. It can be seen from (4.22) that for an oversampling ratio of 16 and an integrator gain equal to $1/4$, the second term causes an increase of the total input-referred noise by approximately 20%. With even smaller M is used, the noise contribution of the operational amplifier is aggressively increased.

4.2.4 Noise Calculation in SC Circuits

As described in the previous sections, two kinds of noise flicker noise or $1/f$ noise and thermal noise exist in MOSFET. Since the flicker noise is dominant in the low frequency end. Only the thermal noise in the sampling switch and the first integrator is considered.

The total input referred noise power can be calculated by adding KT/C noise and op-amp noise together by assuming the two noise sources are uncorrelated. The total input referred noise thus given by

$$V_{Total}^2 = \left[\frac{1}{M} + \left(\frac{C_I}{C_s} \right)^2 \cdot \frac{\pi^2}{3M^3} \right] \cdot \sigma_{OTA}^2 + \frac{N}{M} \cdot \frac{kT}{C_s} \quad (4.23)$$

For fully differential implementation of the circuit, the input referred noise voltage increases by a factor of two assuming no correlation between the noises from the positive side and negative side of the circuit. The total noise voltage can be derived as

$$V_{Total,diff}^2 = \left[\frac{1}{M} + \left(\frac{C_I}{C_S} \right)^2 \cdot \frac{\pi^2}{3M^3} \right] \cdot 2\sigma_{OTA}^2 + \frac{N}{M} \cdot \frac{2kT}{C_S} \quad (4.24)$$

As can be seen from the measurement results in chapter 6, besides the noise predicted during noise analysis there are quite a number of other noise sources making the noise floor much higher than the simulation results. This is due to some of the noise sources are directly added to the system such as external noise from PCB board and the external components.

4.3 Effects of Parameter Mismatch

The parameter mismatch is due to the process imperfection of the current technology. The effect on the modulator performance will be studied in this section.

In a typical switched-capacitor integrator as shown in Figure 4.2, the integrator gain is implemented with the ratio between the sampling capacitor and the integration capacitor C_S/C_I . If the matching between two capacitors [63] [64] is not perfect due to reasons such as process variation, it will directly cause the integrator gain to become a random variable distributed near the targeted value. As a consequence, the integrator gain unavoidably has random mismatch.

The coefficients mismatch refers to the mismatch of the coefficients between the analog and digital domains. For a coefficient with a value of x , the actual achieved value after implementation can be expressed as $(x+\Delta x)$ where the additional factor Δx can be positive or negative values. The gain mismatch is mainly determined by the accuracy of the capacitor ratio in a switched-capacitor circuit. Capacitor matching is important for cascade delta-sigma modulators. Parameter mismatch causes the noise leakage from all the stages degrading the overall SNDR of the

cascade delta-sigma modulator. It requires careful layout techniques and typically imposes a lower limit on the capacitance. The achievable matching accuracy is dependent on the process of the semiconductor foundry.

For the proposed 2-2-2 MASH delta-sigma modulator, the output taking into account the mismatch can be written as:

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E_3(z) + \Delta E_1(z) + \Delta E_2(z) + \Delta E_3(z) + \Delta Y_1(z) + \Delta Y_2(z) \quad (4.25)$$

where

$$STF(z) = z^{-6}$$

$$NTF(z) \approx \frac{1}{g_1 g_2} \cdot N_1(z) \cdot N_2(z) \cdot N_3(z)$$

$$\Delta E_1(z) \approx z^{-4} \left\{ \Delta N_1(z) - \left[\frac{\Delta g_1}{g_1} + \frac{\Delta D_1(z)}{D_1(z)} - \frac{\Delta D_2(z)}{D_2(z)} \right] \cdot N_1(z) \right\} \cdot E_1(z)$$

$$\Delta E_2(z) \approx z^{-2} \cdot \frac{N_1(z)}{g_1} \cdot \left\{ \Delta N_2(z) - \left[\frac{\Delta g_2}{g_2} + \frac{\Delta D_2(z)}{D_2(z)} - \frac{\Delta D_3(z)}{D_3(z)} \right] \cdot N_2(z) \right\} \cdot E_2(z)$$

$$\Delta E_3(z) \approx \frac{1}{g_1 g_2} \cdot N_1(z) \cdot N_2(z) \cdot \Delta N_3(z) \cdot E_3(z)$$

$$\Delta Y_1(z) \approx (l_1 - 1) \cdot N_1(z) \cdot S_2(z) \cdot \left[\frac{\Delta D_2(z)}{D_2(z)} - \frac{\Delta g_1}{g_1} - \frac{\Delta l_1}{l_1 - 1} \right] \cdot Y_1(z)$$

$$\Delta Y_2(z) \approx (l_2 - 1) \cdot N_2(z) \cdot S_3(z) \cdot \left[\frac{\Delta D_3(z)}{D_3(z)} - \frac{\Delta g_2}{g_2} - \frac{\Delta l_2}{l_2 - 1} \right] \cdot Y_2(z) \quad (4.26)$$

The expressions for $S_n(z)$, $N_n(z)$, $D_n(z)$ are given in Eq. (3.4) in chapter 3. The assumption is higher order terms are neglected. The noise leakages can be derived and approximately expressed as:

$$\Delta N_1(z) \approx (\varepsilon_{p11} + \varepsilon_{p12}) \cdot (1 - z^{-1}) \cdot z^{-1} + \varepsilon_{p11} \cdot \varepsilon_{p12} \cdot z^{-2} \quad (4.27)$$

$$\Delta N_n(z) \approx (\varepsilon_{pn1} + \varepsilon_{pn2} + \Delta r_{n2} - r_n \cdot \varepsilon_{pn2}) \cdot (1 - z^{-1}) \cdot z^{-1} + (\Delta r_{n1} - r_n \cdot \varepsilon_{pn2}) \cdot z^{-2}, n = 2, 3 \quad (4.28)$$

$$\frac{\Delta D_n(z)}{D_n(z)} \approx \{(\varepsilon_{pn1} + \varepsilon_{pn2} + \Delta r_{n2} - r_n \cdot \varepsilon_{pn2} + \Delta b_n) \cdot (1 - z^{-1}) \cdot z^{-1} + [(2r_n + b_n) \cdot \varepsilon_{pn1} + r_n \cdot \varepsilon_{pn2} + \Delta r_{n1}] \cdot z^{-2}\} \div [(1 - z^{-1})^2 + (r_n + b_n) \cdot (1 - z^{-1}) \cdot z^{-1} + (1 + r_n) \cdot z^{-2}], n = 1, 2, 3 \quad (4.29)$$

It can be seen that ΔN_1 given in Eq. (4.27) has the lowest noise shaping order and hence has the largest noise leakage power. The extra in-band quantization noise leakage power due to ΔE_1 is therefore given by:

$$\Delta P_{E1} = \left[\frac{\pi^2}{3M^3} \cdot (\varepsilon_{p11} + \varepsilon_{p12})^2 + \frac{1}{M} \cdot (\varepsilon_{p11} \cdot \varepsilon_{p12})^2 \right] \cdot \sigma_{E1}^2 \quad (4.30)$$

where σ_{E1}^2 is the quantization noise power of E_1 .

For an opamp with DC gain A_{o11} and A_{o12} implementing the SC integrators as shown in Eq. (4.2), the parameters involved should satisfy the following condition:

$$\frac{1}{\varepsilon_{p11}} + \frac{1}{\varepsilon_{p12}} \gg \sqrt{3} \cdot \frac{M}{\pi} \quad (4.31)$$

where M is the oversampling ratio. The term of $(\varepsilon_{p11} \cdot \varepsilon_{p12})$ will be very small and it can be ignored. If this noise leakage is controlled to have less than 1dB degradation of the ideal SNDR, the following condition must be satisfied:

$$(\varepsilon_{p11} + \varepsilon_{p12}) < \frac{1}{g_1 \cdot g_2} \cdot \left(\frac{\pi}{M} \right)^5 \cdot \sqrt{\frac{3 \cdot (10^{0.1} - 1)}{13 \cdot 10^{G/10}}} \quad (4.32)$$

where G is factor to include the additional noise suppression due to the optimum NTF zeros location. For 6th-order 2-2-2 cascade architecture, G is approximately equal to 22dB [4]. For DC gain A_{o11} and A_{o12} are all equal to 68dB, the degradation of ideal SNDR is roughly 10dB when $M=16$. With ideal peak SNDR of 126dB, this degradation is still within the acceptable performance range.

The most stringent capacitor matching requirement happens to coefficient g_1 . The matching requirement for g_1 introducing less than 1dB degradation of the ideal SNDR is given by:

$$\frac{\Delta g_1}{g_1} < \frac{1}{g_1 \cdot g_2} \cdot \left(\frac{\pi}{M} \right)^4 \cdot \sqrt{\frac{5 \cdot (10^{0.1} - 1)}{13 \cdot 10^{G/10}}} \quad (4.33)$$

In the switched-capacitor implementation of the proposed architecture, the parameters such as g_1 are related by several integrator gain factors as shown in Figure 3.5 and Eq. (3.11). g_1 can be rewritten as:

$$g_1 = \frac{a_{11} \cdot a_{12} \cdot a_{v1}}{a_{21}} = a_{12} \cdot a_{v1} \quad (4.34)$$

Meanwhile, the integrator gain factors are realized by the ratio of the sampling capacitor and the integration capacitor.

To improve capacitor matching properties against process variations, it is desired to parallel-connect n unit capacitance of C_0 to form the capacitance of $(n \cdot C_0)$. The sampling and integration capacitors can be implemented using an array of unit capacitors because the process variation will affect them by the same factor. In the proposed MASH delta-sigma modulator, the smallest feedback “ r ” values are implemented by parallel-connecting or series-connecting the unit capacitance of C_0 . The detailed information will be given in Chapter five.

A variable $\varepsilon(x)$ is introduced here to signify the percentage of the mismatch between the analog and digital domains for coefficient x . They are related through the following equation:

$$x_a = x_d \cdot [1 + \varepsilon(x)] \quad (4.35)$$

The simulation results of the SNDR degradation resulting from different parameter mismatches $\varepsilon(x)$ for different M are tabulated in Table 4.1 - 4.6. Term “Neg.” represents the value of less than 0.001dB which is negligible. These tables show that the parameters at larger oversampling ratios present much more severe matching requirements than the ones at lower oversampling ratios for the proposed 2-2-2 MASH delta-sigma modulator.

Table 4.1 SNDR degradation (dB) due to the a_{n1} -coefficients mismatch

$\mathcal{E}(a_{11}),$ $\mathcal{E}(a_{21}),$ $\mathcal{E}(a_{31})$	+0.1%	-0.1%	+0.5%	-0.5%	+1%	-1%
$M=4$	Neg.	Neg.	Neg.	Neg.	Neg.	0.1
$M=6$	0.30	0.13	0.33	0.45	0.67	1.08
$M=8$	0.35	0.28	0.84	0.82	2.01	2.65
$M=12$	0.13	0.26	2.33	2.21	5.24	5.49
$M=16$	Neg.	Neg.	5.40	4.84	9.71	9.6

Table 4.2 SNDR degradation (dB) due to the a_y -coefficients mismatch

$\mathcal{E}(a_{y1}),$ $\mathcal{E}(a_{y2})$	+0.1%	-0.1%	+0.5%	-0.5%	+1%	-1%
$M=4$	Neg.	Neg.	Neg.	Neg.	0.04	0.09
$M=6$	0.02	0.17	0.29	0.35	0.79	0.82
$M=8$	0.31	0.53	1.03	1.11	3.37	2.62
$M=12$	0.65	0.58	2.47	2.41	6.01	6.05
$M=16$	Neg.	Neg.	5.03	5.05	10.62	10.52

Table 4.3 SNDR degradation (dB) due to the a_v -coefficients mismatch

$\mathcal{E}(a_{v1}),$ $\mathcal{E}(a_{v2})$	+0.1%	-0.1%	+0.5%	-0.5%	+1%	-1%
$M=4$	0.12	0.06	Neg.	Neg.	0.15	0.20
$M=6$	0.10	0.17	0.90	0.90	2.09	2.31
$M=8$	0.73	0.56	5.14	5.19	10.29	10.00
$M=12$	4.41	4.34	16.31	16.28	22.29	22.31
$M=16$	12.77	12.67	26.42	26.42	32.45	32.47

Table 4.4 SNDR degradation (dB) due to the a_{bn} -coefficients mismatch

$\mathcal{E}(a_{b1}),$ $\mathcal{E}(a_{b2}),$ $\mathcal{E}(a_{b3})$	+0.1%	-0.1%	+0.5%	-0.5%	+1%	-1%
$M=4$	Neg.	Neg.	Neg.	Neg.	0.17	0.05
$M=6$	0.26	0.26	0.39	0.30	0.69	0.49
$M=8$	0.28	0.27	0.43	0.01	1.8	1.38
$M=12$	Neg.	Neg.	0.54	0.61	2.07	1.98
$M=16$	Neg.	Neg.	0.45	0.28	2.73	3.58

Table 4.5 SNDR degradation (dB) due to the a_{n2} -coefficients mismatch

$\mathcal{E}(a_{12}),$ $\mathcal{E}(a_{22}),$ $\mathcal{E}(a_{32})$	+0.1%	-0.1%	+0.5%	-0.5%	+1%	-1%
$M=4$	Neg.	Neg.	Neg.	Neg.	Neg.	Neg.
$M=6$	0.13	0.11	0.69	0.79	1.89	1.87
$M=8$	0.14	0.83	4.65	4.75	9.11	9.23
$M=12$	4.12	4.06	15.90	16.06	21.84	21.86
$M=16$	12.35	12.35	26.33	26.36	32.30	32.44

Table 4.6 SNDR degradation (dB) due to the a_r -coefficients mismatch

$\mathcal{E}(a_{r21}),$ $\mathcal{E}(a_{r22}),$ $\mathcal{E}(a_{r31}),$ $\mathcal{E}(a_{r32})$	+0.1%	-0.1%	+0.5%	-0.5%	+1%	-1%
$M=4$	Neg.	Neg.	Neg.	Neg.	Neg.	Neg.
$M=6$	0.22	0.28	0.19	0.36	0.66	0.47
$M=8$	0.66	0.38	0.64	0.47	1.18	1.52
$M=12$	0.22	0.02	1.87	1.81	4.86	5.18
$M=16$	Neg.	Neg.	3.42	2.64	7.87	7.64

The output spectrum of the modulator with $\varepsilon(a_{y1})$ and $\varepsilon(a_{y2})$ of -0.5% for $M = 12$ at -20dBFS input level is plotted in Figure 4.7. The $SNDR$ is degraded by about 6dB compared to the ideal case. It can be seen from Figure 4.7 that due to the gain mismatch, the quantization noise has leaked into the signal band and masked the NTF notches which causes the degradation of $SNDR$.

Figure 4.7 PSD of the modulator with coefficients a_{y1} and a_{y2} mismatch

4.4 Non-linear Model for the SC Integrators

For the single ended switched-capacitor integrator as shown in Figure 4.2, a complete expression of the transfer function $H(z)$ with consideration of the non-idealities, such as finite opamp DC gain, capacitor mismatch error and incomplete opamp settling is given by:

$$H(z) = \frac{C_s}{C_I} \cdot \frac{k(1-\sigma)z^{-1}}{1 - (1 - \frac{C_s}{C_I} A_o^{-1})z^{-1}} \quad (4.36)$$

where A_o is the dc gain of the opamp, C_I and C_s are the values of the sampling and integration capacitors and $\sigma = A_o^{-1} + C_s/C_I \times A_o^{-1} + \Delta$. Δ is the capacitor ratio error.

Also, k is the gain error scale factor caused by incomplete opamp settling in the integrator. Eq. (4.36) can provide a practical model of SC integrators for system level simulation and analysis.

4.5 Summary

In this chapter, the design methodology for real implementation of each block in SC delta-sigma modulator was analyzed. The noise leakage caused by analog circuit imperfections in cascade delta-sigma modulators, such as finite opamp DC gain, capacitor ratio mismatch and incomplete opamp settling of switched-capacitor circuits, was investigated. The noise leakage caused by these imperfections limits the performance of the proposed delta-sigma modulator for certain fabrication process technology.

In the following chapters, the proposed 6th-order MASH delta-sigma modulator will be designed and implemented.

Chapter 5

Circuit Implementation

This chapter describes the transistor level circuit design and the implementation based on the architecture and principles depicted earlier. The proposed 6th-order MASH delta-sigma modulator was designed for fabrication in a 0.18 μ m CMOS process for wide band application. The objective is to achieve dynamic range of 50 to 80dB at oversampling ratio of 4, 6, 8, 12 and 16 at a 1.8-V power supply. This chapter begins with a depiction of the integrator circuits and the constituent operational amplifier. The programmable capacitor array, three-level quantizer, clock generator and voltage booster are described next. Finally, the entire system is discussed and a brief summary is given.

5.1 The Switched-Capacitor Integrators

Integrator is a fundamental building block of a low-pass delta-sigma modulator. It realizes the accumulation of the quantization noise in a way that the noise is significantly reduced near the signal frequency of interest. In the proposed 2-2-2 cascade delta-sigma modulator, six SC integrators were implemented to establish the three stages of the modulator. Each stage will be described next.

5.1.1 The First Stage Integrators

Figure 5.1 shows the schematic of the first stage of the proposed delta-sigma modulator.

Figure 5.1 The first stage modulator

The fully differential topology consists of two switched-capacitor integrators with two operational amplifiers. The differential topology adopted in the circuit ensures that common-mode disturbances such as noise from the power and ground, as well as signal-dependent switch charge injection will be cancelled to the first order [54]. The input signal is represented by the difference of two voltages V_{i+} and V_{i-} . The switches in Figure 5.1 are controlled by two non-overlapping clock phases, ϕ_1 and ϕ_2 , and their delayed versions, ϕ_{1d} and ϕ_{2d} . The circuit has symmetrical structure. The operation of the integrator can be explained as following.

During the sampling phase (ϕ_1 and ϕ_{1d} high), the integrator samples the input voltage V_{i+} and V_{i-} to the sampling capacitor C_s (which is C_{s11} as shown in Figure 5.1). The charge accumulated in each sampling capacitor will be $C_s \times (V_{i+} - V_{mid})$ and $C_s \times (V_{i-} - V_{mid})$. V_{mid} is chosen to be equal to half of the power supply voltage, which is 900mV. It can be shown that this common mode voltage does not affect the differential signal. During the integration phase (ϕ_2 and ϕ_{2d} high), the charge now is $C_s \times (V_f - V_{mid})$, where V_f is representing the feedback voltage level.

During this phase the charge difference (between the charge sampled during the sampling phase and the charge accumulated in the integration phase) will be transferred to the output. In the ideal case, the voltage change at the positive output of the integrator will be:

$$V_{o+}(n) = V_{o+}(n-1) + \frac{C_s}{C_f} [V_{i+}(n-1) - V_f(n)] \quad (5.1)$$

where $(n-1)$ indicates the output voltage at the previous clock cycle. Similarly, the voltage change at the negative output can be written as:

$$V_{o-}(n) = V_{o-}(n-1) + \frac{C_s}{C_f} [V_{i-}(n-1) - V_f(n)] \quad (5.2)$$

Taking the difference of the Eq. (5.1) and (5.2), it gives:

$$V_{o+}(n) - V_{o-}(n) = V_{o+}(n-1) - V_{o-}(n-1) + \frac{C_s}{C_f} [V_{i+}(n-1) - V_{i-}(n-1)] \quad (5.3)$$

The differential output is independent to the common mode voltage. The capacitor ratio is the integrator gain that can be changed based on application requirement. The z -domain transfer function of the differential signal can be written as:

$$V_o(z) = \frac{C_s}{C_f} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_i(z) \quad (5.4)$$

It realizes exactly the transfer function of an integrator as required.

At the same time, the reference voltage levels V_{p1} , V_{n1} and V_{z1} generated from the first stage three-level quantizer are also applied. ϕ_{z1} controls the switches connected to V_{mid} . This is the third level of the three-level quantizer output. As long as there is enough time for the bottom plate of the sampling capacitor to settle to V_{mid} when ϕ_{z1} is high, there will not be any DAC nonlinearity error. Taking the differential voltage at the output node, one can easily obtain a voltage level of close to zero. This is the reason that it is relatively easy to obtain a linear 3-level DAC. V_{vp1} and V_{vn1} are the input voltages to the three-level quantizer of the first stage. These voltages together with the three-level quantizer output of the first stage will be the input of the second stage.

By having the input and feedback signal sampled onto the same sampling capacitor, less kT/C noise is generated than when separate sampling capacitors are used for each signal [65]. Large capacitances are usually used at the first stage to suppress kT/C noise as described in the previous sections. To reduce input referred sampling noise and also save power consumption and silicon area it is desirable whenever possible to share the sampling capacitors. The coefficient a_{12} is implemented by re-using the sampling capacitors that is implementing the coefficient a_{b1} . The capacitor sizes used in the first and second integrator are summarized in Table 5.1.

Table 5.1 Capacitor sizes in the first and second integrator

Capacitors in the 1 st integrator		Capacitors in the 2 nd integrator	
C _{I1}	2.45 pF	C _{I2}	2.20 pF
C _{S11}	0.49 pF	C _{S21}	0.66 pF
		C _{S22}	0.44 pF

The implementations of the switches used in the first stage are tabulated in Table 5.2. An illustration of the clock phases to control the switches in the integrators is shown in Figure 5.2. The NMOS switches and transmission gate switches are demonstrated in Figure 5.3.

Table 5.2 Switches in the first and second integrator

Element	Clock	Switch type	Size (μ m)
S ₁₁	$\phi_{1d}, \overline{\phi_{1d}}$	Transmission gate	PMOS: 18.0/0.18 NMOS: 4.2/0.18
S ₁₂	$\phi_{2d}, \overline{\phi_{2d}}$	Transmission gate	PMOS: 18.0/0.18 NMOS: 4.2/0.18
S ₁₃	ϕ_1	NMOS	10/0.18
S ₁₄	ϕ_2	NMOS	16/0.18
S ₁₅	ϕ_{s1}	NMOS	10/0.18
S ₂₁	$\phi_{1d}, \overline{\phi_{1d}}$	Transmission gate	PMOS: 18.0/0.18 NMOS: 4.2/0.18
S ₂₂	$\phi_{2d}, \overline{\phi_{2d}}$	Transmission gate	PMOS: 18.0/0.18 NMOS: 4.2/0.18
S ₂₃	ϕ_{2d}	NMOS	6/0.18

S_{24}	ϕ_1	NMOS	6/0.18
S_{25}	ϕ_2	NMOS	10.8/0.18
S_{26}	ϕ_{z1}	NMOS	6/0.18

Figure 5.2 Illustration of the clock phases in the delta-sigma modulator

The requirements on the switches used is that the “ON” resistance should be such that the capacitors being switched settle to their final voltage, with the required accuracy, during the sampling phase of the integrator. To lower the on-resistance and ensure enough settling, all the switches should be sized big enough. While increasing the switch size involves a trade off of adding parasitic gate-to-source and gate-to-drain capacitances that contribute to charge injection into the signal path from the clock signal. This effect is mitigated by the use of clock boosting together with fully differential circuitry.

One crucial non-ideality in SC circuits is the charge injection effect. The detailed description of the charge injection effect in the MOS devices is available in appendix A2. In this project, the charge injection effect is especially important in the first integrator, as the noise shaping does not attenuate the error in this integrator. The use of fully differential circuit will then approximately cancel the injected charge. The common mode charge will be cancelled, leaving only differential charge. One technique that is popularly used to reduce the charge injection is the delayed clocking scheme. This is achieved through the delayed clock signals: ϕ_{1d} and ϕ_{2d} . When switches controlled by ϕ_1 are first turned off, the charge injection from those switches still remains independent of the input signal. Because one of the plates of the capacitor is now floating, turning off the switches controlled by ϕ_{1d} shortly after the ones controlled by ϕ_1 does not introduce charge-injection errors.

The switches at the signal side are transmission gates composed of complementary NMOS and PMOS transistors. It is also used in the second and third stage sampling. The signal-dependent impedance of the signal side switches causes input dependent charge injection due to second-order effects. By using transmission gate, the impedance of the switch is less dependent on the input signal. As a consequence, the impedance of a transmission gate is relatively constant with respect to input signal level (as can be seen from Figure 5.4). The transmission gate needs to be made large enough to tolerate the remaining signal dependency.

Figure 5.3 Switches (a) NMOS switch (b) CMOS transmission gate

Figure 5.4 Switch impedance

Consequently, b_1 as shown in Fig.3.2 can be expressed as a function of the capacitors ratios as:

$$b_1 = \frac{C_{S22}}{C_{I2}} \cdot \frac{C_{I1}}{C_{S11}} \cdot \frac{C_{I2}}{C_{S21} + C_{S22}} \quad (5.5)$$

It can be seen that the value of b_1 is obtained by the capacitor ratios instead of the absolute value of each capacitor. It can be proved that if the capacitors are modeled as Gaussian random variables whose mean is much greater than their standard deviation, then b_1 also can be modeled as a Gaussian random variable. The mismatch error can be restrained by controlling each of the integrator gain factors.

5.1.2 The Second Stage Integrators

The second stage of the proposed delta-sigma modulator is presented in Figure 5.5. It also contains two switched-capacitor integrators, Integrator 3 and Integrator 4, with two opamps. The Integrator 3 shown in Figure 5.5 has two parts of different feedback inputs, one part are V_{p2} , V_{n2} and V_{z2} from the second stage three-level quantizer, the other part are V_{vp2} and V_{vn2} from the output of Integrator 4. Y_{1n} , Y_{1p} and V_{vp1} , V_{vn1} represent the differential output signals of the first stage three-level quantizer and Integrator 2 respectively. There are two programmable capacitor arrays (PCA) in each integrator of the second stage delta-sigma modulator. They are used to realize the values of the feedback factors r_{21} and r_{22} for different M as listed in Table 3.2 for multi-standard functionalities. The PCA used in Integrator 3 and 4 will be shown in more detail in the following section.

The feedback sampling capacitor is shared using some unit capacitance of the overall input sampling capacitor. The remaining portion is connected to V_{mid} during the integration phase. V_{mid} is a dc voltage of 0.9-V. The capacitor sizes used in the third and fourth integrator are tabulated in Table 5.3. The capacitance values are less than the ones in the first stage due to noise shaping and also power consumption considerations. The switches used in the third and fourth integrator are tabulated in Table 5.4. The switches are also sized smaller than the ones in the first stage.

Figure 5.5 The second stage modulator

Table 5.3 Capacitor sizes in the third and fourth integrator

Capacitors in the 3 rd integrator		Capacitors in the 4 th integrator	
C_{I3}	1.50 pF	C_{I4}	600 fF
C_{S31}	0.30 pF	C_{S41}	180 fF
C_{S32}	0.30 pF	C_{S42}	120 fF
C_{S33}	0.90 pF		

Table 5.4 Switches in the third and fourth integrator

Element	Clock	Switch type	Size ($\mu\text{m}/\mu\text{m}$)
S_{31}	$\phi_{1d}, \overline{\phi_{1d}}$	Transmission gate	PMOS: 16.0/0.18 NMOS: 3.6/0.18
S_{32}	$\phi_{2d}, \overline{\phi_{2d}}$	Transmission gate	PMOS: 16.0/0.18 NMOS: 3.6/0.18
S_{33}	ϕ_1	NMOS	3.6/0.18
S_{34}	ϕ_2	NMOS	7.2/0.18
S_{35}	ϕ_{z1}	NMOS	3.6/0.18
S_{36}	ϕ_{2d}	NMOS	3.6/0.18
S_{41}	$\phi_{1d}, \overline{\phi_{1d}}$	Transmission gate	PMOS: 16.0/0.18 NMOS: 3.6/0.18
S_{42}	$\phi_{2d}, \overline{\phi_{2d}}$	Transmission gate	PMOS: 16.0/0.18 NMOS: 3.6/0.18
S_{43}	ϕ_1	NMOS	3.6/0.18
S_{44}	ϕ_2	NMOS	7.2/0.18
S_{45}	ϕ_{z1}	NMOS	3.6/0.18

S_{46}	ϕ_{2d}	NMOS	3.6/0.18
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Hence, g_1 , b_2 and l_1 can be expressed as a function of the capacitors ratio as:

$$g_1 = \frac{C_{S21} + C_{S22}}{C_{I2}} \cdot \frac{C_{S31} + C_{S32} + C_{S33}}{C_{I3}} \quad (5.6)$$

$$b_2 = \frac{C_{S41}}{C_{I4}} \cdot \frac{C_{I3}}{C_{S31}} \cdot \frac{C_{I4}}{C_{S41} + C_{S42}} \quad (5.7)$$

$$l_1 = \frac{C_{S32}}{C_{I3}} \cdot \frac{1}{g_1} \cdot \frac{C_{I3}}{C_{S31}} \quad (5.8)$$

The matching requirement of g_1 is one of the most stringent among the parameters and it relates to the sampling and integration capacitors in the Integrator 2 and 3. To get the desired noise shaping, besides the first integrator, the second and third integrators must also be designed carefully.

5.1.3 The Third Stage Integrators

Figure 5.6 The third stage modulator

The third stage integrators have the similar architecture and operation to the second stage integrators. The circuit diagram is as shown in Figure 5.6. The Integrator 5 has two parts of different feedback inputs also, one part includes V_{p3} , V_{n3} and V_{z3} from the third stage three-level quantizer, and the other part includes V_{vp3} and V_{vn3} from the output of Integrator 6. Y_{2n} , Y_{2p} and V_{vp2} , V_{vn2} represent the differential output signals of the second stage three-level quantizer and Integrator 4 respectively. There are another two programmable capacitor arrays (PCA) in each integrator of the third stage delta-sigma modulator. They are used to realize the values of the feedback factors r_{31} and r_{32} for different M as listed in Table 3.2. The PCA used in Integrator 5 and 6 will be shown in more detail in the following section.

The capacitors in the third stage are made smaller as Tabulated in Table 5.5. And also it has smaller size of switches in the third stage as Tabulated in Table 5.6.

Table 5.5 Capacitor sizes in the fifth and sixth integrator

Capacitors in the 3 rd integrator		Capacitors in the 4 th integrator	
C_{I5}	547.5 fF	C_{I6}	273.8 fF
C_{S51}	109.5 fF	C_{S61}	54.76 fF
C_{S52}	109.5 fF	C_{S62}	82.14 fF
C_{S53}	876.0 fF		

Table 5.6 Switches in the fifth and sixth integrator

Element	Clock	Switch type	Size (μ m)
S_{51}	$\phi_{1d}, \overline{\phi_{1d}}$	Transmission gate	PMOS: 14.0/0.18 NMOS: 3.0/0.18
S_{52}	$\phi_{2d}, \overline{\phi_{2d}}$	Transmission gate	PMOS: 14.0/0.18 NMOS: 3.0/0.18

S ₅₃	ϕ_1	NMOS	2.0/0.18
S ₅₄	ϕ_2	NMOS	3.6/0.18
S ₅₅	ϕ_{z1}	NMOS	2.0/0.18
S ₅₆	ϕ_{2d}	NMOS	2.0/0.18
S ₆₁	$\phi_{1d}, \overline{\phi_{1d}}$	Transmission gate	PMOS: 14.0/0.18 NMOS: 3.0/0.18
S ₆₂	$\phi_{2d}, \overline{\phi_{2d}}$	Transmission gate	PMOS: 14.0/0.18 NMOS: 3.0/0.18
S ₆₃	ϕ_1	NMOS	1.8/0.18
S ₆₄	ϕ_2	NMOS	3.6/0.18
S ₆₅	ϕ_{z1}	NMOS	2.0/0.18
S ₆₆	ϕ_{2d}	NMOS	1.8/0.18

The channel length used for all the switches is the minimum channel length: 0.18 μm to obtain lower on-resistance of the switches.

5.2 The OTA

The folded-cascode operational transconductance amplifier (OTA) shown in Figure 5.7 is used for the proposed delta-sigma modulator to achieve wide bandwidth [66] and modest dc gain.

Figure 5.7 The folded-cascode opamp

A general rule of thumb is that the clock frequency should be at least five times lower than the unity-gain bandwidth of the operational amplifier assuming little slewing behavior occurs and the phase margin is greater than 60 degrees.

The DC-gain A_o of the opamp shown in Figure 5.7 can be roughly estimated by doing a small signal analysis as given by:

$$\begin{aligned}
 A_o &= g_{m1} \cdot R_o \\
 &= g_{m1} \cdot [g_{m7} \cdot R_{o7} \cdot R_{o5} // R_{o9} \cdot g_{m9} \cdot (R_{o11} // R_{o13})]
 \end{aligned}
 \tag{5.9}$$

where g_{m1} , g_{m7} and g_{m9} are the transconductances of transistor M_1 , M_7 and M_9 respectively. R_o is the total output impedance to ground seen at the output node. R_{o5} , R_{o7} , R_{o9} , R_{o11} and R_{o13} are the output impedance of transistor M_5 , M_7 , M_9 , M_{11} and M_{13} respectively. The transistor output impedances normally increase as the channel

length is increased. Hence, the devices are sized larger than the minimum length to maximize the R_o in the DC gain expression.

The unity-gain frequency of the opamp is given by:

$$\omega_t = \frac{g_{m1}}{C_L} \tag{5.10}$$

where C_L is the load capacitance.

The output voltage swing of the folded-cascode opamp is determined by the cascode P-channel devices, M_6 and M_7 , at the upper end, and by the cascode N-channel devices, M_8 and M_9 , at the lower end. For proper operation, all the transistors should be operating in the saturation region.

The transistor sizes in the OTA are summarized in Table 5.7. P-channel transistors are used as each of the transistors in the input differential pair.

Table 5.7 Transistor sizes in the OTA

Transistor	Size (in μm)
M_1	$20 \times 400/0.18$
M_2	$20 \times 400/0.18$
M_3	$24 \times 90/1.8$
M_4, M_5	$12 \times 90/1.8$
M_6, M_7	$6 \times 60/0.6$
M_8, M_9	$3 \times 27.6/0.6$
M_{10}, M_{11}	$4 \times 42/1.2$
M_{12}, M_{13}	$2 \times 42/1.2$

The biasing circuit and common-mode feedback network will be described in the following section.

Both thermal noise and $1/f$ noise increase the total noise power of the folded-cascode amplifier. However, $1/f$ noise can be roughly neglected since this work is for wideband application. As such, considering only thermal noise, the input-referred noise power density σ_{OTA}^2 of the amplifier shown in Figure 5.7 is:

$$\sigma_{OTA}^2 = 2 \times \gamma \times \frac{4kT}{g_{m1}} \times \left(1 + \frac{g_{m4} + g_{m10} + g_{m12}}{g_{m1}} \right) \quad (5.11)$$

where the factor of 2 is considered for the differential topology. The value of γ is process dependent. Based on [67], a value of 4 is assumed for this amplifier. Because the noise currents generated in the transistor M_6 - M_9 will inject into output node, the noise contribution from these devices can be neglected compared with the devices M_1 , M_2 , M_4 , M_5 and M_{10} - M_{13} . The transistor M_3 is acting as the current-source and its noise will be rejected by the fully differential circuit.

Table 5.8 Simulated values of the transconductance of the transistors in the fully differential amplifier

Transistors	Transconductance g_m (mS)
M ₁ , M ₂	7.30
M ₄ , M ₅	4.46
M ₁₀ , M ₁₁	5.33
M ₁₂ , M ₁₃	2.67

Table 5.2 lists the simulated values of the transconductance of the main noise-contributing transistors in this fully differential amplifier. Substitute these values to Eq. (5.2), one can get the estimated value of the input-referred noise power density as:

$$\begin{aligned}\sigma_{OTA}^2 &= 2 \times \gamma \times \frac{4kT}{g_{m1}} \times \left(1 + \frac{g_{m4} + g_{m10} + g_{m12}}{g_{m1}} \right) \\ &= 2 \times 4 \times \frac{4 \times 1.38 \times 10^{-23} \text{ JK}^{-1} \times 300 \text{ K}}{7.3 \text{ mS}} \times \left(1 + \frac{4.46 \text{ mS} + 5.33 \text{ mS} + 2.67 \text{ mS}}{7.3 \text{ mS}} \right) \quad (5.12) \\ &= 2.46 \times 10^{-17} \text{ V}^2 / \text{Hz}\end{aligned}$$

The common mode feedback (CMFB) circuit for this fully differential operational amplifier is shown in Figure 5.8. Common-mode feedback is required in fully differential amplifier to define the voltage at the high impedance output nodes. In this design, both the input and output common-mode levels are set to 900mV. Capacitors labeled C₂ are used to sense the average of the output voltages. It also creates the control voltages for the opamp current sources. The dc voltage across C₂ is determined by capacitors C₁, which are switched between bias voltage V_{bias4} and DC voltage of V_{mid}. The capacitance values in the CMFB network are summarized

in Table 5.9. The switches are realized by the transistors having minimum channel length as listed in Table 5.10.

Figure 5.8 CMFB circuit of the opamp

Table 5.9 Capacitors in the CMFB circuit

C_1	109.5 fF
C_2	438.0 fF

Table 5.10 Switches in the CMFB circuit

Switch	Clock	Type	Size (μ m)
S_1	$\phi_{1d}, \overline{\phi_{1d}}$	Transmission gate	PMOS: 1.2/0.18 NMOS: 0.9/0.18
S_2	$\phi_{2d}, \overline{\phi_{2d}}$	Transmission gate	PMOS: 1.2/0.18 NMOS: 0.9/0.18

The circuit for the generation of the four biasing voltages for the amplifier is shown in Figure 5.9.

Figure 5.9 The biasing circuit

This circuitry is driven by an external current source I_{ref} which is equal to $126\mu A$ to lower the noise generated through power supply in a voltage-biasing structure. This current will be mirrored to the other branches of the circuit. The biasing voltages $V_{bias1} \sim V_{bias4}$ generated from this circuit will ensure the transistors in Figure 5.7 remain in the saturation region at all time. The gate voltages of the NMOS $M_1 \sim M_2$ and $M_3 \sim M_4$ are equal to $1.13V$ and $552mV$ respectively. The gate voltages of the PMOS $M_5 \sim M_6$ and $M_7 \sim M_8$ are equal to $1.285V$ and $714.4mV$ respectively. In this biasing circuit, all the transistors except M_9 , $M_{11} \sim M_{12}$, M_{13} and $M_{14} \sim M_{15}$ are operating in saturation mode. The transistors M_9 and M_{13} form the start-up circuit. While the transistors $M_{11} \sim M_{12}$ and $M_{14} \sim M_{15}$ are operating as resistors. These devices bias the voltage levels so as to ensure the transistors $M_1 \sim M_2$ and $M_7 \sim M_8$ are in saturation region while allowing for a relatively large swing at the output nodes of the amplifier. All the transistors except M_9 and M_{13} were designed to have non-minimum channel length in order to obtain the desired stable biasing voltages without the effect of channel length modulation.

Figure 5.10 Simulated CMFB voltage and differential output

Figure 5.10 shows the proper operation of the switched-capacitor CMFB circuit. It can be seen that the common-mode voltages at the outputs are settled at 900-mV in steady state. The common-mode feedback voltage settles at about 552-mV. The differential output is equal to zero for this transient simulation.

Table 5.11 Transistor size in the biasing circuit

Transistor	Size (μ m)
M ₁ , M ₂	27.6/0.6
M ₃ , M ₄	42.0/1.2
M ₅ , M ₆	360/1.8
M ₇ , M ₈	120.0/0.6
M ₉	0.72/0.18
M ₁₀	27.6/0.6
M ₁₁	5.6/0.8
M ₁₂	3.0/0.8
M ₁₃	0.72/0.18
M ₁₄	19.0/0.9
M ₁₅	17.0/0.9
M ₁₆	120.0/0.6
M ₁₇	27.6/0.6
M ₁₈	42.0/1.2

The fully differential folded-cascode operational amplifier is simulated with Spectre using a 0.18- μ m CMOS model. The simulated frequency response of the overall amplifier is shown in Figure 5.11. As shown in Figure 5.11, the simulated

unity-gain frequency of the OTA is approximately 347-MHz with a phase margin of 61-degree when driving a 2-pF capacitive load on each output. The final opamp parameters and simulation results are summarized in Table 5.12.

Table 5.12 Targets and simulation results of the differential OTA

Parameter	Target	Simulated
DC Gain	> 60 dB	68 dB
Unity-gain Frequency	320 MHz	347 MHz
Slew Rate	150 V/ μ s	>154.2V/ μ s
Output Load	2 pF	2 pF
Output Current	378 μ A	378 μ A
Phase Margin	60 ~ 70 degree	61 degree

Figure 5.11 Simulated frequency responses of the operational amplifier at the differential output

5.3 Programmable Capacitor Array (PCA)

To meet the multi-standard requirement, one straightforward way is to change sampling rate so as to get different signal bandwidth. However, practical consideration implies that different sampling rate will require different speed of the operational amplifier. When the sampling rate is increased too high, it is difficult to design a proper opamp to meet the fast operation speed due to the CMOS technology limitation.

The proposed delta-sigma modulator in this work can be programmed to achieve five different sets of signal bandwidth and resolution by adjusting the inherent coefficients in the *NTF* as provided in Chapter 3. It can be seen from Figure 5.1, 5.2 and 5.3 that the programmable capacitor array (PCA) is located in the second and third stage integrators of the modulator. In the proposed MASH delta-sigma modulator, the smallest “*r*” values are implemented by parallel-connecting or series-connecting the unit capacitance of C_0 .

The basic idea of PCA is to produce five different capacitor values, $4 \times C_{M0}$, $2 \times C_{M0}$, $1 \times C_{M0}$, $C_{M0}/2$, and $C_{M0}/4$ for each oversampling ratio by switching four identical unit capacitors C_{M0} using the minimum number of control signal. Since there are five possibilities, the minimum number of control signal is three with eight possibilities provided. Using more transistors instead of capacitors can reduce power consumption and silicon area.

Figure 5.12 Architecture of the PCA

Initially, there are nine switching signals (ϕ_{M1-9}) to control the output value of the capacitance that acquired between node A and B as shown in Figure 5.12. After simplifying the logic function using the expressions provided in Eq. (5.13) ~ Eq. (5.16), the final control signals required for the multi-standard functionality are: ϕ_{M1} , ϕ_{M2} and ϕ_{M3} . When ϕ_{M1} , ϕ_{M2} and ϕ_{M3} are all at the HIGH state, the capacitance between node A and B is equivalent to four C_{M0} in parallel, which is equal to $(4 \times C_{M0})$ Farad for the specification of $M=4$. When M is equal to 16, the control signals ϕ_{M1} , ϕ_{M2} and ϕ_{M3} are all at the LOW state. The capacitance between node A and B become four C_{M0} in series, which is equal to $(C_{M0} / 4)$. For different oversampling ratio M , the settings of the control signals in the PCA ϕ_{M1} , ϕ_{M2} and ϕ_{M3} are tabulated in Table 5.13.

$$\phi_{M4} = \overline{\phi_{M1}} \quad (\text{NOT}) \quad (5.13)$$

$$\phi_{M5} = \phi_{M6} = \overline{\phi_{M1} + \phi_{M2}} \quad (\text{NOR}) \quad (5.14)$$

$$\phi_{M7} = \phi_{M1} \cdot \phi_{M2} \quad (\text{AND}) \quad (5.15)$$

$$\phi_{M8} = \phi_{M9} = \phi_{M3} \quad (5.16)$$

Table 5.13 The control signals operating status in PCA

M	Capacitance	ϕ_{M1}	ϕ_{M2}	ϕ_{M3}
4	$4 \times C_{M0}$	HIGH	HIGH	HIGH
6	$2 \times C_{M0}$	HIGH	HIGH	LOW
8	$1 \times C_{M0}$	HIGH	LOW	LOW
12	$\frac{1}{2} \times C_{M0}$	LOW	HIGH	LOW
16	$\frac{1}{4} \times C_{M0}$	LOW	LOW	LOW

According to the coefficients stated in Table 3.2, the capacitance in the PCA of each integrator is different from one another. Table 5.14 lists the unit capacitor values in each integrator.

Table 5.14 Capacitor values in the PCA of each integrator

Location	C_{M0}
Integrator 3	187.5 fF
Integrator 4	37.50 fF
Integrator 5	136.875 fF
Integrator 6	34.225 fF

5.4 The Three-Level Quantizer

The block diagram of 3-level quantizer is shown in Fig 5.13. It is implemented using two comparators, two SR latches together with one DAC to produce the three level voltages which are V_p , V_n and V_z . V_p and V_n are feedback to the integrators through the switches controlled by the clock signal ϕ_{2d} which will produce the voltage level $-V_{dd}$ and $+V_{dd}$ of the 3-level quantizer. V_z will feedback as a switching control signal, which will produce the common dc voltage of $V_{dd}/2$ to the

positive and negative output nodes. As a result, the differential output will be zero, corresponding to the third voltage level of the 3-level quantizer. In order to minimize the switching errors due to V_z , the voltage-boosting circuitry was also adopted before V_z is feedback.

A simple regenerative latch without pre-amplifier is used as the comparator core to minimize the power consumption. Its schematic will be shown in the next section. The values of the reference voltages “ V_{ref+} ” and “ V_{ref-} ” are equal to 810mV and 990mV separately. To store full logic voltages levels and hold the data for the subsequent charge transfer period, some digital inverter buffers and the SR latches are adopted following each comparator.

Figure 5.13 The three-level Quantizer

The first comparator will compare the input voltage with -180mV ($=V_{\text{refp1}}-V_{\text{refn1}}$) while the second comparator will compare it with 180 mV . ($=V_{\text{refp2}}-V_{\text{refn2}}$). This voltage difference of 180mV corresponds to the threshold of the quantizer which is $0.25 \times 0.2 = 0.05$ in the SIMULINK. The two comparators used are identical and the two input voltages that are applied are also the same for both comparators except for the opposite reference voltages connections: $V_{\text{ref1}} = 810\text{mV}$, $V_{\text{ref2}} = 990\text{mV}$.

The result from the comparator will be latched in the static SR latch. The corresponding outputs from the latch will determine which of the switches in the DAC is on. There are three outputs V_p , V_n and V_z produced from the DAC corresponding to the desired output of the 3-level quantizer.

- i. V_p HIGH and V_n LOW and V_z LOW;
- ii. V_p LOW and V_n HIGH and V_z LOW;
- iii. V_z HIGH while V_p and V_n is in high impedance state.

These three voltages will feedback differently to the input of each stage modulators. Each sub circuit of the three-level quantizer will be described in more detail next.

5.4.1 The Comparator

A simple regenerative latch without pre-amplifier is used as the comparator core as shown in Figure 5.14 to minimize the power consumption [68]. It provides a logical zero when its input is below a preset reference value and a logical one when its input is above that value. The widths of the input transistors are four times of the reference transistors. By doing this, the threshold voltages are set from references at $+V_{\text{ref}}$ and $-V_{\text{ref}}$ without the need for sampling capacitors or switches at the input of the comparator. During the comparison phase, the input difference will be compared with the reference voltage difference. The “clk” signal in Figure 5.14 is

ϕ_2 . The comparison is performed when ϕ_2 is LOW. It is congruous with the Figure 5.14 in which the enabled signal of comparator is labeled as ϕ_1 .

Figure 5.14 The comparator

It has been examined in [69] that from the perspective of analog circuit design, special attention must be given to the design of the integrators in the modulator loop. The implementation of the comparator in the second-order delta-sigma modulator is less critical since large offset and hysteresis can be tolerated without significantly degrading the converter performance.

The sizes of the transistors adopted in the implementation of the comparator are listed in Table 5.15.

Table 5.15 Transistor sizes in the comparator

Transistor	Size (μ m)
M ₁ , M ₂	PMOS: 12/0.18
M ₃ , M ₄	PMOS: 48/0.18
M ₅ , M ₆	PMOS: 12/0.18
M ₇ , M ₈	PMOS: 12/0.18
M ₉ , M ₁₀	NMOS: 4.8/0.18
M ₁₁ , M ₁₂	NMOS: 4.8/0.18

5.4.2 The SR latch

Figure 5.15 The SR latch

To store full logic voltages levels and hold the data for the subsequent charge transfer period, some digital SR latches are adopted following each comparator. The SR latch in Figure 5.15 is basically formed by cross coupling NAND gates preceded

by the inverter buffers in each path. The inverter is used to set the threshold so that the comparator will not trigger wrong logic when it has not finished comparing. The inverter and the NAND gate used are shown in Figure 5.16 below.

Figure 5.16 The (a) Inverter and (b) NAND gate in the SR latch

5.4.3 The DAC

The D/A converter is crucial to the overall performance of the modulator since any errors introduced during the sampling of the reference voltage are transferred to the output without noise shaping. The DAC as shown in figure 5.17 basically consists of a controller, which will turn the switches on and off according to the comparison results from the comparators. The zero voltage of the three-level quantizer happens for input signal falling between -180 mV and 180 mV : the logic output voltage level is raised via the clock booster circuit to about 3.3 V . The operation of the DAC can be understood from the overall three-level quantizer operation as depicted in Table 5.5.

The buffers and NOR gates serve to reduce loading on SR latch and they are sized so that when Q_1 is low, the rise pulse of Q_2 will turn off the PMOS connecting to V_p first before turning on the NMOS. This will ensure no short circuit happen. The PMOS and NMOS connected to V_p and V_n are sized to ensure sufficient settling in the integrator during the comparison phase. Shown next are the Inverters and NOR gates used in the DAC. The $\overline{\phi_{2d}}$ is connected to one of the inputs of the 3-input-NOR gate. This is because $\overline{\phi_{2d}}$ is the latest signal to arrive at the input of the NOR gate. The delay of the NOR gate will be smaller if this critical signal is put nearer to the output path.

Figure 5.17 The DAC

Table 5.16 Three-level quantizer operation

Input difference to the comparator	S1	R1	S2	R2	Q ₂	Q ₁	out _A	out _B	out _C	out _D	V _p	V _n	V _z when $\overline{\phi_{2,d}}$ is low. (connecting output nodes to V _{mid} in each integrator)
V _{i+} -V _i >180 mV	0	1	0	1	0	0	0	0	1	1	V _{dd}	0	0
-180mV < V _{i+} -V _i <180 mV	0	1	1	0	0	1	1	0	1	0	Z (high impedance)	Z	3.3 V
V _{i+} -V _i <-180 mV	1	0	1	0	1	1	1	1	0	0	0	V _{dd}	0

5.5 The Clock Generator

In SC circuits, a set of two-phase non-overlapping clock is usually used. One ideal clock source is used as inputs to the clock generation circuitry. The clock generation circuitry is designed to generate the two non-overlapping-clocks and their delayed and complement version. The clock frequency used in this work is 64 MHz. The input clock signal has the pulse width of 6.625ns as shown in Figure 5.18. The rising-time and falling-time are all equal to 1ns.

Figure 5.18 The input clock signal

The clock generator scheme used to produce the clock signals ϕ_1 and ϕ_2 , their delayed versions ϕ_{1d} and ϕ_{2d} , their inversed versions $\overline{\phi_{1d}}$ and $\overline{\phi_{2d}}$ are as shown in Figure 5.19. The differential NOR and differential NOT circuitries are shown in Figure 5.20 and 5.21 respectively.

Figure 5.19 The clock generator scheme

Figure 5.20 Differential NOR Circuitry

Figure 5.21 Differential NOT Circuitry

5.6 The Clock Booster

For proper operation of the switches in low-voltage SC circuits, one solution is to use on-chip voltage boosters. The purpose of this approach is to drive the switches with clock signals higher than the supply voltage [70].

The clock booster block diagram is as shown in Figure 5.22. This circuit is used to produce an approximately 3.3 V output pulse from 1.8 V input pulse. This boosted voltage is adopted in the generation of the clock signals and ϕ_z .

Figure 5.22 The clock booster block diagram

The Voltage Doubler circuit is used to provide constant voltage of approximately twice of the supply voltage V_{dd} . This voltage is used as the N-well voltage in the output transistor in Clock Booster circuit to prevent latch up. The Voltage Doubler circuit is shown in Figure 5.23 while the Clock Booster circuit is as shown in the Figure 5.24.

If IN is “HIGH” in Voltage Doubler, the gate of NM₂ is raised to a voltage close to $2 \times V_{dd}$ (after a short transient). Since this gate voltage exceeds $V_{dd} - V_{th}$, the source of NM₂ can rise to V_{dd} . This still remains the device in strong inversion. When IN is at time t_2 , the top plate of C_1 sets to a voltage close to twice V_{dd} , NM₂ is turned OFF

now. This high voltage at the gate of NM₃ allows the top plate of C₂ to be charged to V_{dd}. The capacitor C₃ in Figure 5.23 serves to reduce ripple of the V_{well}. It was implemented by a transistor with its source, drain and bulk terminals all connected to ground. The transistor size used in generating the clocks is 38.4/1.6 (μm/μm).

Figure 5.23 Voltage doubler circuit

Figure 5.24 Clock Booster circuit

The total output of the Gate Booster needs to be reset periodically, and this is done by the inverter stage NM₅ and NM₆ in Clock Booster circuit. The bigger the C₂, the greater the output voltage is. This can be understood by realizing that C₂ and the load capacitance to ground form a voltage divider when the voltage at bottom plate of C₂ in Figure 5.24 rises from 0 V to 1.8 V.

The sizings of the inverters are large enough so as to give less than 1ns rise time and fall time for all the Clock Booster outputs.

5.7 Summary

In this chapter, the overall switched-capacitor implementation of the proposed delta-sigma modulator is presented. The constituent circuits are described one by one and simulation results are to be provided next.

Chapter 6

Experimental Results

The final prototype is implemented in a 0.18 μm , single poly, six-metal CMOS process. It can be shown in the following sections that the proposed modulator has achieved the desired multi-standard and wideband performances. With a single 1.8-V supply voltage and 64-MHz sampling rate, the measurement results prove that the implemented modulator can achieve a series of dynamic range of 69, 61, 57, 52 and 43dB for M equal to 4, 6, 8, 12 and 16 respectively.

In this chapter, the prototype layout of the delta-sigma modulator will be described first. Then the test setup to do the evaluation and the summary of the measurement results will also be provided.

6.1 Prototype Layout

As in any high-speed analog circuit design, careful attention must be paid to the layout of the circuit especially on the critical paths such as ground line to avoid excessive parasitic elements that could degrade the performance. To realize the benefits of the differential circuits used, all differential signal paths were routed close to each other to enable rejection of common mode pick-up. Separate power supplies and ground were provided for digital and analog sections. Some general precautions are listed in appendix A3. The transistors in the operational amplifier are fingered to share the diffusion area of the devices. This reduces the parasitic capacitances, and in turn improves the settling performance of the circuit components.

As discussed previously, the mismatch of the capacitor used in the integrator may affect the performance of the modulator. Common-centroid layout techniques were

used when doing the layout of the capacitors. Also, the dummy capacitors were placed around the capacitor arrays to achieve better accuracy and matching.

The complete layout of the delta-sigma modulator is shown in Figure 6.1. The chip size is $1683\mu\text{m} \times 1068\mu\text{m}$ with 36 I/O pins and the core area occupies $1600\mu\text{m} \times 600\mu\text{m}$.

Figure 6.1 The layout of the delta-sigma modulator

After the circuit layout is done, the chip is fabricated and ceramic samples are made. A 52-pin ceramic package was used to facilitate the troubleshooting process.

Figure 6.2 shows the Micro-photograph of the experimental IC. Multiple pins are supplied to the power and ground to strengthen the drivability and also reduce the parasitic effects.

Figure 6.2 Micro-photograph of the experimental IC

6.2 Test Setup and Measurement Results

6.2.1 Test Setup

In the absence of a decimator following the modulator, a typical delta-sigma ADC measurement uses a high-speed logic-analyzer to capture the output digital data stream. A fast Fourier transform (FFT) is employed on this captured data to obtain its spectrum. In our evaluation, we clocked the delta-sigma modulator at 64MHz. A signal generator plus filter and Balun were used to generate the pure sinusoidal input signal required for achieving the desired SNDR.

The chip was packaged in a 52-pin ceramic package and surfaced mounted on the device under test (DUT) board. A two-layer printed circuit board (PCB) was used. All the components required for testing are mounted on a single DUT board. Figure 6.3 shows the diagram of the experimental test set-up used to evaluate the circuit performance. The test circuit is powered by an Agilent E3630A DC power supply. The supply lines and ground to be used for the analog and digital parts are separated to prevent the noise coupling through the supply and ground lines. Amount of decoupling capacitors are added between each one of the supplies and ground. The

differential input of the modulator is generated by a sine wave generator (HP 8116A 0.001Hz-50MHz Synthesized Signal Generator). The outputs of the signal generator are connected to the test board through coaxial cables and terminated by a $50\,\Omega$ resistor in order to match the $50\,\Omega$ output impedance of the signal generator. The clock to the system is provided by a waveform generator (Wavetek 100MHz Synthesized Arbitrary Waveform generator). The modulator outputs are captured by a mixed signal oscilloscope with logic analyzer function (Agilent MSO6104A) and then transferred to a workstation for subsequent processing in Matlab.

Figure 6.3 Measurement test setup

Very large noise level was detected during preliminary tests on the prototype chip. Confirmed by doing laser opening and wire bonding, the current supply pin 'n1' was found to be the root-cause. One can see the figure 6.4 for the actual picture of the modulator pins. The original wire connects between the chip and pad was replaced by the wire bonding highlighted in Fig. 6.4.

Figure 6.4 Actual picture of the modulator pins with wire bonding

6.2.2 Data Collection Precautions

The digital outputs from all three stages are collected by a logic analyzer and transferred to a PC to do error cancellation, SNR and DR calculation. The digital postprocessing was performed using MATLAB.

Before we discuss the measurement results, it is worthwhile to look at the choice of input signal frequency and the postprocessing method. One precaution for the simulation is that for the windowing and FFT method as shown in appendix A4.1, the number of samples taken has to be an integer multiples of 2. Furthermore, the sampling frequency has to be an exact integer multiples of the input signal frequency as well. This is to avoid noise leakage due to frequency spread as shown in Figure 6.5. Both curves are from SIMULINK simulation using sampling frequency of $f_s=64$ MHz.

The solid line is for the case of using an input frequency of 250 kHz (f_s/f_{in} is an integer number) while the dotted line is for the case of using an input frequency of 250.1 kHz (f_s/f_{in} is not an integer number). Similarly, the results from the Spectre simulation also encounter this problem. This precaution needs to be taken as after the Spectre simulator, the output data are processed using FFT to obtain the SNDR. One should pick an input frequency that satisfies f_s/f_{in} is equal to an integer when doing the transient analysis using Spectre. It should be noted that this is due to the processing method we adopted. If using the method in appendix A4.2, the input frequency can be chosen as any values within $[0, f_B]$. One can refer to appendix A4.3 as comparison.

Figure 6.5 Noise leakage due to frequency spread

The simulation results will also be different when different numbers of samples were collected as shown in Figure 6.6. It is only sufficient to collect $N \geq 1024$ numbers of samples. Large value of N requires long simulation time and plenty of resources as well.

Figure 6.6 PSD for different numbers of samples taken

6.2.3 Measurement Results

When input level is increased, the distortion is worse in the evaluation than predicted in the simulation. The overload input level is at -5dBFS for the circuit level modulator instead of at -1dBFS as listed in Table 3.3. This is because the circuit noise and non-idealities such as thermal noise, parameter mismatch, amplifier settling and slew rate and etc. are not included in the system level modulator in Chapter 3. Multi-standard application is achieved by adjusting the control signals ϕ_{M1} , ϕ_{M2} and ϕ_{M3} in PCA as listed in Table 5.13, the measurement PSD at -5dBFS of the MASH delta-sigma modulator for different oversampling ratio M are shown in Figure 6.7.

Figure 6.7 Measurement PSD of the proposed MASH delta-sigma modulator for different oversampling ratio

The sinusoidal input signal frequency is 250 kHz and 2048 numbers of samples are taken. As can be seen from Figure 6.7, the resolution of the modulator is limited by thermal noise and flicker noise for high M while it is limited by quantization noise for

low M . After the circuit design, the modulator can achieve 66.68dB peak SNDR for oversampling ratio of 16. The output of the first stage modulator Y_1 achieves a SNDR of 44.18dB. The second stage and third stage reduce the noise still further, giving a SNDR of 60.09dB and 66.68dB, respectively. Each time for different oversampling ratio, Y_1 , Y_2 and Y_3 will be processed in PC using MATLAB simulation tools to calculate the SNDR. In this work, the SNDR at different input amplitude is obtained by FFT method (refer to the appendix A4). The input signal is a sinusoidal signal, which has the maximum amplitude of -5dBFS which is normalized to the full scale. The full-scale input level (0dBFS) is defined as a sine wave having an amplitude equal to the quantizer feedback level. Once the data of SNDR (dB) versus different input level (dBFS) is obtained, we can approximate the DR (dB) as illustrated in Figure 3.1.

Additional measurements were carried out with different amplitudes of the input signal. The plot of SNDR vs. input level for different M is Fig. 6.8. The dynamic range and effective resolution of the modulator for different M is plotted in Fig. 6.9.

Figure 6.8 SNDR vs. input level for different M

Figure 6.9 (a) *DR vs. M* (b) *Resolution vs. M*

Operating at low oversampling ratios of 4, 6, 8, 12 and 16, the performance of the proposed delta-sigma modulator has been presented in this chapter.

6.3 Discussion and State-of-the-Art Comparison

To compare with the other state-of-the-art implementations, the *FOM* is calculated as follows:

$$FOM_{(M=16)} = \frac{Power}{2^b \times (f_s/M)} = \frac{32 \times 10^{-3}}{2^{11} \times (4 \times 10^6)} = 3.91 pJ \quad (6.1)$$

$$FOM_{(M=12)} = \frac{Power}{2^b \times (f_s/M)} = \frac{32 \times 10^{-3}}{2^{10} \times (5.333 \times 10^6)} = 5.86 pJ \quad (6.2)$$

$$FOM_{(M=8)} = \frac{Power}{2^b \times (f_s/M)} = \frac{32 \times 10^{-3}}{2^9 \times (8 \times 10^6)} = 7.81 pJ \quad (6.3)$$

$$FOM_{(M=6)} = \frac{Power}{2^b \times \left(\frac{f_s}{M}\right)} = \frac{32 \times 10^{-3}}{2^{8.5} \times (10.667 \times 10^6)} = 8.29 pJ \quad (6.4)$$

$$FOM_{(M=4)} = \frac{Power}{2^b \times \left(\frac{f_s}{M}\right)} = \frac{32 \times 10^{-3}}{2^{6.5} \times (16 \times 10^6)} = 22.1 pJ \quad (6.5)$$

Table 6.1 collects several references on recent works related to wideband delta-sigma modulators, with indication of technology utilized, topology of the modulator, as well as parameters relevant to the calculation of *FOM*. Their Nyquist rate bandwidth is larger than 2MHz. The rightmost column shows the calculated *FOM* for each implementation. Noticeably, a low value of power dissipation does not necessarily result in a low *FOM*. The lower is the figure-of-merits, the higher the efficiency.

Table 6.1. Performance summary of the published delta-sigma modulators with greater than 2KHz Nyquist Rate output

Reference/ Year	DR (bits)	Nyquist Rate (MS/s)	Power (mW)	CMOS Process/ Supply	Architecture	f_s (MHz)	<i>FOM</i> (pJ)
[71]/07	12.9/ 10.9	3.84M/20M	7.4/20.5	0.13um/1.2V(3.3 V for bootstrap switch)	2(1.5b)-2(1.5b)	61.44/2 40	0.25/ 0.53
[72]/05	16	2.5	44	0.25um/1.2V	2(5b)-2(3b)	40	0.27
[73]/03	11.4	3.84M	4.3	0.13um/1.2V(±1 0%)	2-1	38.4	0.41
[74]/04	13	2.2	8	0.13um/1.5V	2(3b), DEM	105	0.44
[75]/04	14	25	200	0.18um/1.8V	5(4b), DWA	200	0.49
[76]/02	14	2.5	24	0.25um/2.5-1.3V	5(tri-level)	80	0.59
[77]/00	16	2.5	105	0.5um/5-3V	2(4b)-1(4b)- 1(4b),	20	0.64

					Bi-Directional DWA		
[78]/01	15.5	4	150	0.5um/2.5V	2(5b)-1(3b)-1(3b), Partitioned DWA	64	0.81
[79]/02	14	4.4	66	0.25um/2.5V	2-1-1(3b)	70.4	0.92
[80]/04	12.6	2	18.8	0.18um/1.8V	2-1-1	50	1.51
[81]/00	14	2	50	0.25um/2.5V	5(tri-level)	80	1.53
[82]/05	8.9	5M	4	0.18um/1.8V	3	40	1.67
[83]/00	15.8	2.5	295	0.65um/5V	3(4b), DWA	60	2.04
[84]/02	14.3	2.2	92	0.18um/3.3-1.8V	2-2-2(tri-level)	64	2.04
[85]/02	14	4	149	0.18um/1.8V	5(4b), DWA	32	2.27
[86]/03	13	3	59.4	0.18um/1.8V	3(5b), Pseudo-DWA	48	2.42
[87]/02	8.06	4M	2.9	0.13um/1.5V	2(5-level)	46	2.7
[88]/99	15	2.2	200	0.5um/3.3V	2-1-1	52.8	2.77
[89]/02	13	4	105	0.18um/1.8V	4(4b), Incremental DWA	48	3.2
[90]/99	12.9	2.2	55	0.7um/5V	2-1-1(3b)	35.2	3.27
[91]/98	14.8	2	230	1um/5V	2-1-1	48	3.98
[92]/01	13	2	77	0.35um/3.3V	2-1-1(program-level)	35.2/64(12b)	4.7
[93]/91	12	2.1	41	1um/5V	2-1(3b)	50	4.77
[94]/03	11.3	3.84	50	0.18um/2.7V	2(6b), DEM	46	4.81
[95]/00	12	12.5	491.6	0.6um/5-3V	3(4b), DWA	100	9.6

A figure of *FOM* vs. output rate of the lately reported DSM implemented by switched-capacitor circuit with bandwidth higher than 2MHz is shown in Fig. 6.11. Overall, [71] and [75] achieved the widest signal bandwidth with small *FOM*. Compared to the reported modulators, this work has relatively large *FOM*, while offers tunability over a wide frequency range.

The multi-standard modulators in [71] [73] [82] [87] and [94] all use more than one sampling rates to obtain different signal bandwidth. In contrast, the multi-standard modulator in this work achieves different bandwidth and resolution by controlling the PCA. Although they can achieve multiple bandwidth, only one or at most two [71] of the Nyquist rate bandwidth achieved is wider than 2MHz. The modulators with Nyquist rate bandwidth lower than 2MHz are not shown in Table 6.1 and Figure 6.10.

Figure 6.10 *FOM* vs. Nyquist Rate of some reported DSM

Although the above measurements show that the modulator is functional, the attained performances are far from what was expected from system simulation results. The noise floor is high and many of the harmonic components were not sufficiently attenuated which were further degrading the performance. The power spectral density is flattened and noise shaping function is not as expected. It is suspected that the input signal is not clean and contains noise, the first stage has leakage due to pole and gain errors of the first integrator, or there is noise coupling on the chip or PCB board. The testing results also showed that the last stage contributes little to the SNDR improvement. The reason behind the difference between simulation and evaluation could be the mismatch of the digital cancellation network, external noise, the thermal noise of the opamps or the nonlinearity of the opamps.

Another limitation of this system is that the life-test issue may be arising because the gate oxides of switches were bootstrapped by clock of about 3V in case of 1.8V process is used.

6.4 Summary

A multi-standard wideband 6th-order delta-sigma modulator operating at 64MHz sampling frequency has been implemented. The multi-standard operation is achieved by using proper circuit structure and optimized components. The dynamic range that can be achieved ranges from 69dB to 43dB with signal bandwidth ranging from 2MHz to 8MHz. The power consumption is 32mW when operating from a 1.8V supply voltage. The implementation technology is 0.18 μ m CMOS and the core size of the modulator is 1.6 $\times$ 0.6 mm².

The operation of this multi-standard wideband DSM is verified by test measurement and the results show a promising performance. The performance of the modulator in circuit level is summarized in Table 6.2.

Table 6.2. Performance summary of the implemented DSM

Parameter		Value
Clock frequency		64MHz
Supply voltage		1.8V
Power consumption		32mW
Technology		0.18μm CMOS
Core IC area		1.6 × 0.6 mm ²
Peak SNDR & DR	M = 16	66.68dB & 69dB
	M = 12	60.83dB & 61dB
	M = 8	56.59dB & 57dB
	M = 6	51.82dB & 52dB
	M = 4	41.75dB & 43dB

Chapter 7

Conclusion and Future Work

This chapter summarizes the research work done in this thesis, highlights the contributions, and provides suggestions for future work.

7.1 Contribution

In this work, the full design flow of a high-resolution SC sigma-delta modulator, 2-2-2 cascade architecture has been investigated, including system level, transistor level, circuit design techniques and IC implementation. All aspects of the delta-sigma modulator are investigated such as architectures, transfer functions, circuit non-idealities, switched-capacitor circuits, transistor level implementation, IC layout and testing etc.

Based on the measurement results, the performance of our proposed multi-standard and wideband delta-sigma modulator is quite promising. This is mainly due to several contributions as shown below.

First, our proposed $\Delta\Sigma$ modulator architecture supports wide band analog-to-digital conversion and allows operation at oversampling ratio as low as 4. So far, some of the previous wideband delta-sigma modulators also use low oversampling ratio (M). But this is the first $\Delta\Sigma$ modulator that uses M equals to 4 in the reported works without using multi-bit quantizer, such as M equals to 8 in [75] [77] [82] [85] [95], M equals to 12 in [71] [89] [94], 16 in [71] [72] [78] [79] [86] [90], 24 in [83] [88] [91] and 32 in [76].

Second, by inserting the proposed PCA (programmable capacitor array) blocks into the cascade architecture, the modulator can achieve the signal bandwidth from 2MHz to 8MHz. by operating at various oversampling ratios. Our proposed modulator can provide various signal bandwidth in a single modulator at a constant sampling frequency. It is implemented by adjusting the dc connection of three external PINs to fulfill the multi-standard requirement. The PCA is also optimized in terms of matching, chip area and power consumption consideration.

Third, all aspects of the delta-sigma modulator are investigated – transfer functions; structures; circuit nonlinearities; switched-capacitor architecture; transistor level circuit; IC layout – ultimately results in the realization. The methodology of designing a switched-capacitor delta-sigma modulator has been investigated. Non-idealities such as noise sources, integrator non-idealities, OTA characteristics and parameter mismatches which contribute to the system noise are also analyzed.

It has been demonstrated in the system level simulation that the proposed modulator has the potential to achieve high speed and high resolution in analog-to-digital conversion besides it achieves multi-standard and wide-band performances. However, the experimental results of the prototype showed lower resolutions than designed for. Several factors and issues limiting the achievable high performance are discussed. Further improvements are needed in the implementation. The multi-standard functionality with flexible bandwidth also makes the performance of the implemented delta-sigma modular worse than the one that is optimized for a certain application with fixed bandwidth and resolution.

7.2 Recommended Future Work

From the measurement results, it is obvious that 2nd and 3rd stage did not substantially increase the SNDR due to leakage of quantization noise in the 1st and

2nd stage. Digital calibration may be applied to help improve the matching of digital cancellation network to the analog circuits.

A fully integrated system combining the modulator, the digital logic and the decimation filter could be an interesting project.

The application of oversampling techniques to MegaHertz-range A/D conversion shows considerable promise. Double sampling [96] [97] [98] can be added to further increase the conversion rate.

Further increase in the signal bandwidth will also probably depend on the use of multi-bit quantization in the modulator. Analog or digital correction techniques might provide a means of compensating for DAC nonlinearity.

The work may be extended to low voltage below 1.0V for portable applications. It may be implemented in modern deep sub-micro technologies with even less gate length to achieve lower power consumption.

An alternative direction for future work is to explore new applications for delta-sigma modulation systems.

7.3 Related Publications

- Y.Y. Du, K.T. Tiew, "A low oversampling ratio delta-sigma modulator for standard and wideband applications," *IEEE MWSCAS*, Vol. 2, pp. II-173 - II-176, Jul. 2004.
- Y.Y. Du, K.T. Tiew, "A Low Oversampling Ratio 11-bit, 10.6-MHz Switched-Capacitor Delta-Sigma Modulator for Wideband Applications," *ISIC*, pp. 560 - 563, Sep. 2007.
- Y.Y. Du, K.T. Tiew, "A 1.8V 64MHz Switched Capacitor Delta-Sigma Modulator for Wideband and Multi-Standard Applications," *IEEE MWSCAS*, pp. 1368-1371, Aug. 2007.
- Y.Y. Du, K.T. Tiew and L. Siek, "A Programmable 1.8V 6th-order Delta Sigma Modulator for Multi-Standard and Wideband Applications," *Submitted for publication in Analog Integrated Circuits and Signal Processing*, Nov. 2009.

Appendix

A1. SIMULINK model of the delta-sigma ADC

Figure A.1 SIMULINK Model of the proposed delta-sigma ADC

A2. Charge injection of MOS switch transistors

One of the most serious limitations of monolithic switches is the charge injection (also called clock feedthrough, and charge feedthrough) effect. A SC at the sampling phase with a MOS transistor as a switch is shown in Figure A.3. When the switch is

ON, there is an amount of charge accumulated in the conducting channel of the transistor. The accumulated charge is given by:

$$Q_{ch} = W \cdot L \cdot C_{ox} \cdot (V_{gs} - V_{th})$$

Figure A.2 Charge injections in a MOS transistor

When the switch turns off, this charge is injected in either direction and part of the charge (ΔQ) is dumped into the capacitor C_S . The charge ΔQ results in an error voltage of $\Delta Q/C_S$ on C_S . In a fast switching-off condition when the falling time of the control clock is very fast, the transistor channel disappears quickly. In practice, the charge ΔQ is hardly predicted precisely.

The use of a fully differential circuit will then approximately cancel the injected charge. The common mode charge will be cancelled, leaving only differential charge.

One effective technique that is popularly used to reduce the charge injection is the delayed cutoff clocking scheme as depicted in Chapter 5.

A3. Layout precautions and testing prototype

In layout, all transistors should be placed in one direction to provide the same environment to all the transistors.

One should use the Metal 1 for horizontal routing and Metal 2 for the vertical routing as far as possible.

One should try to avoid running metal over poly gate as this cause to increase in parasitic capacitance. Avoid crossing of sensitive signals. Do not route the power signals in between the sensitive devices

One should put a guard ring around the differential pair. One should put as many as possible sub-contacts to eliminate latch-up.

To achieve good element matching, differential analog circuits have to be laid out as symmetrically as possible. The transistors are laid out as interleaved multiple-gate fingers. The common-centroid layout was used to match the transistors of a differential circuit. All matched devices should be as compact as possible.

In SC circuits, capacitor ratios should have a high accuracy. The approach in designing matched capacitors is to use unit capacitors (cells). In order to maintain the capacitor ratio we need to keep their area ratio constant as well.

In order to maintain a low impedance ground connection back to the system power supply it is usually necessary to use more than one connector pin for ground.

Do floor plan before layout.

A4. Methods to Calculate *SNDR*

A4.1 Fast Fourier Transform (FFT) Method

A MATLAB script used to calculate the *SNDR* (dB) of a delta-sigma modulator using Fast Fourier Transform (FFT) [99] method is presented below:

```
%-----

% SNDR calculation script

clear yw Y Pyy f nB Ps;

yw = y(1000:N+999).*hann(N);

Y = fft(yw,N);

Pyy = Y.* conj(Y) / N^2;

f = fs*(0:N/2)/N;

nB= ceil(N/(2*M));

[P,n]=max(Pyy(1:round(fin/fs*N)+10));

Ps=sum(Pyy(n-1:n+1));

SNDR=10*log10(Ps/(sum(Pyy(1:nB))-Ps));

%-----
```

y is the digital output of the modulator. yw is the Hanning window weighted signal of y . N is the number of the samples used in FFT calculation. The Hanning window is described by this MATLAB function:

```
%-----
```

```
function w=hann(n)
```

```
w = 0.5*(1-(cos(2*pi*(0:n-1)/n)));
```

```
%-----
```

The output spectrum at certain input amplitude can be plotted by this command:

```
%-----
```

```
semilogx(f,10*log10(Pyy(1:N/2+1)));
```

```
%-----
```

Note that throughout the clock frequency range $[-f_s/2, +f_s/2]$, there are N numbers of samples used. The interval between two samples is f_s/N . The value of N will be related to several factors such as input frequency f_{in} , oversampling ratio M , sampling frequency f_s and so on.

A4.2 Sinusoidal Minimum Error (SME) Method

An alternative method to calculate the SNR (dB) and/or $SNDR$ (dB) of a delta-sigma modulator using Sinusoidal Minimum Error (SME for short) proposed in [100] has been realized by programming and the code script is shown below:

```
%-----
```

```
clear Ycap INV_W_2 W_1 W_2 W_3 ycap;
```

```
%y2=y1(17:1040);
```

```
%y2=y1(1000:N1+999);
```

```
%y3=y(1000:N1+999);
```

```
% ys is the original sample
```

```
N1=1024;
```

```
%ys=yd(44:1067);
```

```
ys=yd(48:1071);
```

```
w=exp(j*2*pi*fin*M/fs);
```

```
%w=exp(j*2*pi*fin*1/fs);
```

```
K=2;
```

```

for iy=1:(2*K+1)

    for ix=1:N1

        W_1(iy,ix)=w^((ix-1)*(iy-K-1));

    end

end;

end;

% W_2=zeros

% Store 4K+1 W summation to form W_2 matrix

for iy=1:(4*K+1)

    W(iy)=0;

    for ii=0:(N1-1)

        W(iy)=W(iy)+w^((iy-2*K-1)*ii);

    end;

end;

end;

% To construct W_2

for iy=1:(2*K+1)

    for ix=1:(2*K+1)

        W_2(iy,ix)=W(iy+ix-1);
    
```



```
        end;

    end;

    Ycap=inv(W_2)*W_1*ys;    % Ycap

    for ii=1:2*K+1           % to calculate the ycap, estimated output

        for id=1:N1

            W_3(id,ii)=w^((ii-K-1)*(id-1));

        end

    end

    ycap=W_3*Ycap;    % estimated output

    %plot(1:length(y_result),real(y_result));

    a2=2*abs(Ycap(K-1));

    a1=2*abs(Ycap(K));

    a0=abs(Ycap(K+1));
```

```

Psigout=0.5*a1^2;

Psighh=0.5*a2^2;

Psigyy=sum(ys.^2)/N1;

ee=ys-real(ycap);           %modify the calculation

Psigee=sum(ee.^2)/N1;

%Psigee=Psigyy-Psigout-Psighh-a0^2;

SNR=10*log10(Psigout/Psigee);           % SNR (dB)

TSNR=10*log10(Psigout/(Psigee+Psighh));           % SNDR (dB)

% ----- end -----

```

A4.3 Comparison of FFT & SME method:

a. **FFT:**

Advantages:

It can provide the value of SNDR directly from the digital output without using filters. Consequently, it eliminates the complexity to find out a suitable filter even for the simulation purpose.

Disadvantages:

Because the windowing and FFT, it cannot get the correct SNDR when the numbers of samples taken is not an integer multiples of 2.

b. SME:

Advantages:

It can provide the value of SNR besides SNDR so that we can analyze the harmonics and noise distortion of the delta-sigma modulator separately.

It also can provide the corresponding results when f_{in} is equal to any values within signal band $[0, f_B]$.

Disadvantages:

It needs a good-performance filter before we use this method. To choose a suitable filter is an important and also complicated work because the modulators with different architecture will require different filters.

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