Analog class D amplifiers : non-linearities and power-efficiency

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**Analog Class D Amplifiers:
Non-Linearities and Power-Efficiency**

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University

in fulfillment of the requirement for the degree of

Doctor of Philosophy

2009

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Acknowledgements	i
Summary.....	v
List of Figures.....	vii
List of Tables	xi
List of Abbreviations	xii
Chapter 1 Introduction.....	1
1.1 Motivation.....	1
1.2 Objectives.....	7
1.3 Contributions.....	9
1.4 Organization of the Thesis	12
Chapter 2 A Review of Audio Amplifiers.....	15
2.1 An Overview of Audio Amplifiers.....	16
2.1.1 Classical Linear Audio Amplifiers	16
2.1.2 High Power-Efficiency Audio Amplifiers	20
2.1.3 A Comparison of the Power-Efficiency of Audio Amplifiers	23
2.2 A Review of Class D Amplifiers.....	24
2.2.1 Class D Modulation Techniques.....	28
2.2.2 Class D Output Stages.....	46
2.2.3 Filterless Class D Amplifiers	68
2.3 Conclusions.....	72
Chapter 3 PSRR and PS-IMD of PWM Class D Amplifiers	73
3.1 Introduction.....	73
3.2 PSRR and PS-IMD of PWM Class D Amplifiers	75

3.2.1	PSRR and PS-IMD of Open-Loop PWM Class D Amplifiers	75
3.2.2	PSRR and PS-IMD of Single- and Double-Feedback PWM Class D Amplifiers	79
3.3	Technique to Improve PSRR and PS-IMD	84
3.4	Results and Verification	89
3.5	Conclusions	97
Chapter 4	THD, PSRR and PS-IMD of Bang-Bang Control Class D Amplifiers	98
4.1	Introduction	98
4.2	A Comparison of Power-Efficiency of Bang-Bang Control and PWM Class D Amplifiers	100
4.3	THD of Bang-Bang Control Class D Amplifiers	103
4.3.1	THD of an 'ideal' Bang-Bang amplifier	103
4.3.2	The Effect of the Propagation Delay on THD	107
4.3.3	The Effect of the 'On' Output Impedance on THD	109
4.4	Power Supply Noise	111
4.4.1	PSRR	113
4.4.2	PS-IMD	115
4.5	Results and Verification	116
4.6	Conclusions	128
Chapter 5	Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation..	129
5.1	Introduction	129
5.2	Modeling of Loudspeakers	131
5.2.1	A Review of the Loudspeaker Model in the Audio Range	131
5.2.2	The Loudspeaker Model in the High Frequency Range (20kHz-1MHz) ..	132
5.3	Power Dissipation and Power-Efficiency of Conv and 3State Filterless Class D Amplifiers	136
5.3.1	Power Dissipation	136

5.3.2 Power-Efficiency 141

5.4 Results and Verification..... 143

5.5 Conclusions..... 148

Chapter 6 Conclusions and Recommendations..... 149

6.1 Conclusions..... 149

6.2 Recommendations for Future Work 153

Author’s Publications..... 155

Bibliography 157

Appendix A: Derivation of Eqns. (4.1) – (4.5)..... 172

Appendix B: Measurements on 10 Loudspeakers..... 175

Summary

This Ph.D research program pertains to investigations into the non-linearities and power-efficiency of a class of analog amplifiers – the high power-efficiency analog Class D (switching) amplifiers. The specific amplifiers include the prevalent Pulse-Width-Modulation (PWM) Class D amplifier, the somewhat esoteric Bang-Bang control Class D amplifier, and the more recent filterless Class D amplifier.

The mechanisms of power supply-related non-linearities, specifically the Power Supply Rejection Ratio (PSRR) and Power Supply induced Intermodulation Distortion (PS-IMD), of PWM Class D amplifiers are investigated. The associated expressions thereof are derived, thereby providing an analytical means to quantify the PSRR and PS-IMD, and they delineate the effects of the various parameters thereof. A simple method, with very low hardware overheads, is proposed to markedly improve ($\sim 26\text{dB}$) the PSRR and PS-IMD. Further, the associated expressions thereof are derived, thereby providing an analytical means to quantify the improved PSRR and PS-IMD arising from the proposed simple method, and they delineate the effects of the various parameters thereof.

The power-efficiency of Bang-Bang control Class D amplifiers is investigated, and these amplifiers are suggested as a viable alternative to the prevalent PWM Class D amplifiers for power-critical low-voltage applications, including hearing instruments (hearing aids). The input signal-related non-linearity, the Total Harmonic Distortion (THD), and the power supply-related non-linearities, the PSRR and PS-IMD, are investigated. The associated expressions thereof are derived, thereby providing an analytical means to quantify the THD, PSRR and PS-IMD, and they delineate the effects

of the various parameters thereof. When the Bang-Bang control Class D amplifier is benchmarked against the prevalent PWM Class D amplifier for power-critical low-voltage applications, the former is significantly advantageous in terms of power-efficiency (~50% at low modulation indexes), and in most cases, advantageous in terms of the aforesaid non-linearities (THD, PSRR and PS-IMD).

The power dissipation and power-efficiency of filterless Class D amplifiers based on the 3-state architecture and on the conventional 2-state architecture are investigated. The associated expressions thereof are derived, thereby providing an analytical means to quantify the power dissipation in the loudspeaker (due to the attenuation of high frequency components therein) and the ensuing power-efficiency of the filterless Class D amplifiers. These expressions further provide an analytical means to quantify the required power rating and intrinsic inductance of the loudspeaker. A high frequency (20kHz – 1MHz) loudspeaker model is proposed. If certain conditions are satisfied, the power-efficiency of the filterless Class D amplifier based on the conventional 2-state architecture can be comparable to that based on the 3-state architecture.

All aforesaid contributions are verified by computer simulations and on the basis of experimental measurements.

From an overall perspective, the contributions herein provide useful insight to Class D amplifier designers into the mechanisms of the pertinent non-linearities and of power-efficiency, and provide an analytical means to optimize (and/or trade-off) the various pertinent parameters of Class D amplifiers to meet a given set of specifications.

List of Figures

Figure 1-1	Block diagram of a Class D amplifier	3
Figure 2-1	(a) Schematic of a Class A amplifier, and (b) its waveform.....	17
Figure 2-2	(a) Schematic of a Class B amplifier, and (b) its waveform.....	18
Figure 2-3	(a) Schematic of a Class AB amplifier, and (b) its waveform.....	19
Figure 2-4	(a) Schematic of a Class G amplifier, and (b) its waveform.....	21
Figure 2-5	Block diagram of a Class AD amplifier	23
Figure 2-6	Power-efficiency of output stages of various audio amplifiers	24
Figure 2-7	Block diagram of a Class D amplifier	25
Figure 2-8	Schematic of a single-ended Class D output stage with load	27
Figure 2-9	Schematic of a BTL Class D output stage with load.....	27
Figure 2-10	Schematic of an open-loop PWM amplifier	29
Figure 2-11	Waveforms of a PWM Class D amplifier	30
Figure 2-12	Schematic of a single-feedback PWM Class D amplifier.....	33
Figure 2-13	(a) Schematic of a first-order synchronous Sigma-Delta Class D amplifier, and (b) its waveforms.....	37
Figure 2-14	Schematic of a first-order asynchronous Sigma-Delta Class D amplifier	39
Figure 2-15	(a) Block diagram of a Bang-Bang control Class D amplifier, and (b) its waveforms	42
Figure 2-16	Block diagram of a self-oscillating Class D amplifier	43

Figure 2-17 (a) Schematic of a Sliding Mode control Class D amplifier and (b) its block diagram.....44

Figure 2-18 Schematic of an improved Sliding Mode control Class D amplifier.....45

Figure 2-19 Schematic of a Class D output stage realized using a cascade of inverters.....47

Figure 2-20 Block diagram of a Class D output stage49

Figure 2-21 Schematic of drivers and power transistors: (a) *p*-channel-cum-*n*-channel inverter configuration, and (b) *n*-channel totem-pole configuration50

Figure 2-22 Layout of an NMOS transistor.....54

Figure 2-23 Output waveforms of a dead time circuit.....58

Figure 2-24 Schematic of a dead time circuit using the skewing method59

Figure 2-25 (a) Schematic of a dead time circuit using the offset voltage method, and (b) its waveforms60

Figure 2-26 Schematic of a dead time circuit using the non-overlapping logic method.....61

Figure 2-27 Safe Operating Area62

Figure 2-28 Schematic of an over-current protection circuit using series resistors.....64

Figure 2-29 Schematic of an over-current protection circuit using the parallel method.....65

Figure 2-30 Schematic of an improved over-current protection circuit using the parallel method66

Figure 2-31 Schematic of an over-temperature protection circuit67

Figure 2-32	Block Diagram of a filterless Class D amplifier.....	69
Figure 2-33	Waveforms of the filterless Class D amplifier at zero-input	70
Figure 2-34	Waveforms of the filterless Class D amplifier with a sinusoidal input.....	71
Figure 3-1	(a) Schematic of an open-loop PWM amplifier, and (b) its linear model.....	76
Figure 3-2	(a) Schematic of a single-feedback PWM amplifier, and (b) its linear model.....	80
Figure 3-3	Schematic of a double-feedback PWM amplifier.....	82
Figure 3-4	Schematic of the proposed carrier generator	85
Figure 3-5	Waveforms of the proposed carrier generator	86
Figure 3-6	Microphotograph of the single-feedback PWM amplifier.....	90
Figure 3-7	PSRR of the single-feedback, double-feedback and improved single- feedback PWM amplifiers	91
Figure 3-8	PS-IMD of the (a) single-feedback, (b) double-feedback, and the (c) improved single-feedback PWM amplifiers	94
Figure 4-1	Schematic of a Bang-Bang amplifier	102
Figure 4-2	Schematic of a PWM amplifier	102
Figure 4-3	Comparison of η_{PWM} and η_{Bang}	103
Figure 4-4	Waveforms of the Bang-Bang amplifier whose $t_D > 0$	108
Figure 4-5	Schematic of the Bang-Bang amplifier for $R_{on} > 0$	110
Figure 4-6	Microphotographs of the two Class D output stages: (a) Output 1: $R_{on} = 2.9\Omega$, and (b) Output 2: $R_{on} = 17\Omega$	117

Figure 4-7 THD of the Bang-Bang amplifier 119

Figure 4-8 THD @ $M=0.7$ of the Bang-Bang amplifier and the PWM amplifier 121

Figure 4-9 PSRR of the Bang-Bang amplifier and the PWM amplifier..... 123

Figure 4-10 PS-IMD of the Bang-Bang amplifier and the PWM amplifier (a)
versus input frequency, and (b) versus modulation index..... 125

Figure 5-1 Loudspeaker model for (a) audio frequency range, and (b)
simplified loudspeaker model for $f > 1\text{kHz}$ 132

Figure 5-2 R_L and X_L versus frequency 136

Figure 5-3 Schematic of a Conv amplifier 137

Figure 5-4 Schematic of a 3State amplifier 137

Figure 5-5 (a) P_{sw} , and (b) η of the Conv amplifier and the 3State amplifier 144

Figure 5-6 η of the Conv amplifier and the 3State amplifier 147

List of Tables

Table 2-I	Symbols used in eqns. (2.9)-(2.18).....	53
Table 3-I	Parameters of the single-feedback, double-feedback and improved single-feedback PWM amplifiers	90
Table 4-I	Parameters of the Bang-Bang amplifier and the PWM amplifier.....	102
Table 4-II	Circuit parameters of the Bang-Bang amplifier and the PWM amplifier	103
Table 4-III	Circuit Parameters of the Bang-Bang amplifier	118
Table 5-I	Parameters of the Conv amplifier and the 3State amplifier	143

List of Abbreviations

BJT	<u>B</u> ipolar <u>J</u> unction <u>T</u> ransistor
BTL	<u>B</u> ridge- <u>T</u> ied <u>L</u> oad
CMOS	<u>C</u> omplementary <u>M</u> etal <u>O</u> xide <u>S</u> emiconductor
DMOS	<u>D</u> ouble diffused <u>M</u> etal <u>O</u> xide <u>S</u> emiconductor
IMD	<u>I</u> nter <u>M</u> odulation <u>D</u> istortion
MOSFET	<u>M</u> etal <u>O</u> xide <u>S</u> emiconductor <u>F</u> ield <u>E</u> ffect <u>T</u> ransistor
NMOS	<i>n</i> -type <u>M</u> OSFET
PMOS	<i>p</i> -type <u>M</u> OSFET
PS-IMD	<u>P</u> ower <u>S</u> upply induced <u>I</u> nter <u>M</u> odulation <u>D</u> istortion
PSRR	<u>P</u> ower <u>S</u> upply <u>R</u> ejection <u>R</u> atio
PTAT	<u>P</u> roportional <u>T</u> o <u>A</u> bsolute <u>T</u> emperature
PWM	<u>P</u> ulse <u>W</u> idth <u>M</u> odulation
SNR	<u>S</u> ignal to <u>N</u> oise <u>R</u> atio
SOA	<u>S</u> ave <u>O</u> perating <u>A</u> rea of a power transistor
THD	<u>T</u> otal <u>H</u> armonic <u>D</u> istortion
$\Sigma\Delta$	Sigma Delta

Chapter 1 Introduction

1.1 Motivation

Audio amplifiers are some of the earliest electronic circuits and the first electronics audio amplifier (based on triode valves) can probably be attributed to Lee deForest in 1906 [1]. Audio amplifiers largely serve to amplify a low amplitude (electronic) input signal to a higher amplitude signal and provide sufficient power to drive an acoustic transducer, the loudspeaker.

The art of audio amplifier design is mature and well established, particularly for linear amplifiers (for example, Class A, Class AB and Class B). The signals therein are continuous-time and the transistors that output the signal operate in the active region (for bipolar transistors (BJTs), or equivalently the saturation region for Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)). The figures-of-merit that determine the quality of an audio amplifier typically include high power-efficiency, low non-linearities and in some applications, small form-factor; several other parameters defined by International Electrotechnical Commission [2] include frequency response, noise, cross-talk (for multi-channel amplifiers), etc. Power-efficiency is defined as the ratio of the output power over the supply power. In general, high power-efficiency is highly desirable. This is because in the case of portable devices, the lifespan of the remote power supply (typically batteries) is extended, and in the case of high-power

devices, the need for a heatsink is either eliminated or the size reduced. The non-linearities typically include Total Harmonic Distortion (THD) [3, 4], Intermodulation Distortion (IMD) [3, 4], Power Supply Rejection Ratio (PSRR) [3, 4], and Power Supply induced Intermodulation Distortion (PS-IMD) [5]. In general, it is desirable that THD, IMD and PS-IMD are low and PSRR, high.

The aforesaid figures-of-merit and their mechanisms for linear audio amplifiers are well established [6-12] and in general, very high quality (high-fidelity) linear audio amplifiers are routinely designed. However, the power-efficiency of linear amplifiers are low, for example 5% at low signal swings (in view of the large crest factor [13] of audio signals). The low power-efficiency is attributed to the active operating region of their output transistors. In Chapter 2, a comprehensive literature review of the various classes of linear amplifiers, including their power-efficiency attributes, will be provided. The low power-efficiency of linear audio amplifiers can be a major shortcoming in many applications.

To circumvent the low power-efficiency drawback of linear amplifiers, Class D (switching) amplifiers have more recently been reported in the literature [14] and are increasingly prevalent; a comprehensive literature review of Class D amplifiers will also be provided in Chapter 2. Although the first Class D amplifier was proposed in the early 1960s [14], practical monolithic Class D amplifiers appeared only in the 1990s when MOSFET devices matured to the juncture where they are practical. The primary mechanism for the increased power-efficiency of Class D amplifiers is the operating regions of their output transistors, specifically in the triode and cut-off regions (as in digital circuits) vis-à-vis the active region (of linear amplifiers).

Although Class D amplifiers have the high power-efficiency advantage over linear amplifiers, they are often deemed inferior to linear amplifiers in terms of the other aforesaid non-linearities. Interestingly, the mechanisms for most of these non-linearities are largely unknown (unlike that for linear audio amplifiers) – although in many cases, empirical rules-of-thumb are known within the esoteric Class D amplifier community, and this is probably a consequence of design and/or trial-and-error experience. For example, a higher switching frequency usually results in lower non-linearities but at the cost of reduced power-efficiency; also see below and the further examples and details delineated in Chapters 2 – 5 later.

Figure 1-1 depicts the block diagram of a ‘traditional’ (see later in Chapters 2 and 5 for the ‘non-traditional’ amplifier) Class D amplifier, comprising a modulator, an output stage and a load (including a lowpass filter and a loudspeaker). The modulator modulates the input analog signal into a digital-like modulated signal. The modulated signal serves as a control signal to control the switching in the output stage. The output stage provides sufficient current to drive the load.

Figure 1-1 Block diagram of a Class D amplifier

There are a number of modulation techniques, each with various characteristics and figures-of-merit, and a review will be provided in Chapter 2. Of these modulation techniques, the Pulse-Width-Modulation (PWM) is arguably most prevalent, largely due to its high power-efficiency arising from the low switching frequency. Interestingly, despite the increasing acceptance of PWM Class D amplifiers, the mechanisms of their non-linearities are (also) largely unknown, including the PSRR and PS-IMD; see Chapter 3 later.

In applications where power-efficiency (and hardware-efficiency) is critical, for example in hearing instruments (hearing aids), it is imperative to select the appropriate modulation technique largely because of its associated hardware requirements. Interestingly, although various modulation techniques are relatively well established in the literature, the modulation technique that potentially offers the simplest hardware and simultaneously the highest power-efficiency is largely unestablished. Specifically, although the Class D amplifier employed in hearing instruments typically embody the PWM modulation, it is not known if other modulation techniques can yield higher power-efficiency; the application of the simplest PWM modulation [15] that used an open-loop architecture (vis-à-vis the more accepted closed-loop architecture, for example Figure 1-1) and employed exponentially rising/falling carrier waveform is limited because the ensuing harmonic distortion is unacceptable (a high $\sim 3\%$ at high modulation indexes). Further, the effects of the design parameters (for example, the switching frequency) of the various possible modulation techniques to power-efficiency and to non-linearities are also largely unreported. As a case in point, there may be advantages in employing the Bang-Bang control modulation [16], a modulation technique that has hitherto been used for mid- and

high-power applications, for a micropower (hearing instruments) Class D amplifier design; see Chapter 4 later.

In traditional Class D amplifiers (Figure 1-1), a bulky output lowpass filter is typically required. From a practical/economic perspective, this filter accounts for ~30% of the cost and ~75% of the PCB area [17] in a Class D amplifier realization. It serves to attenuate the high frequency components arising from the switching and to reconstruct the desired output from the digital-like modulated signal to a continuous-time signal. From a realization perspective, the need for the output lowpass filter somewhat defeats the smaller form-factor advantage of the Class D amplifier arising from the reduced (or absence of) heat-sink. To circumvent these drawbacks, a design methodology that has recently received some acceptance is the ‘untraditional’ (more specifically termed, ‘filterless’) [18-22] approach where the abovementioned output filter is not required. Further, there have been claims [17], perhaps somewhat contentious, that the filterless approach has lower non-linearities, specifically the IMD.

Although filterless Class D amplifiers have the advantage of not requiring the lowpass filter, the loudspeakers are required to have some (intrinsic) inductance to attenuate the high frequency (beyond the audio range) components due to switching. There is a further need for the loudspeakers to be (slightly) higher rated to accommodate the additional power dissipation due to the attenuation of the high frequency components. Although it is known that the additional power dissipation results in reduced power-efficiency and may possibly damage the loudspeaker (if the total power exceeds the power rating of the loudspeaker), it is not known how the power-efficiency may be improved – specifically, if there are design parameters available to the designer to improve the power-

efficiency. Further, at this juncture, there is no established rigorous methodology to determine the added loudspeaker power rating and the required inductance – these are largely determined empirically. In the case of the power rating, some manufacturers simply advise an added 5% power rating. In the case of the inductance, it is empirically known that a loudspeaker with higher intrinsic inductance results in reduced power dissipation in the loudspeaker hence higher power-efficiency. In some cases, manufacturers simply advise a loudspeaker with an $\sim 10\mu\text{H}$ intrinsic inductance [23]. From a cost perspective, a loudspeaker with higher internal inductance is usually more expensive and consequently, a simple rule-of-thumb is often insufficient. Put simply, there is a need to develop an analytical procedure to quantify the power dissipation in loudspeakers and the power-efficiency of filterless Class D amplifiers, and the parameters thereof.

Further, to determine the power dissipation in a loudspeaker for filterless Class D amplifiers, the loudspeaker model in the high frequency range (beyond the audio frequency range, $>20\text{kHz}$) is necessary. To the best of the author's knowledge, although the audio frequency ($<20\text{kHz}$) loudspeaker model is well established [24-26], a high frequency model is unreported. This is because the high frequency loudspeaker model is unnecessary in linear amplifiers and in traditional Class D amplifiers (Class D amplifiers with output lowpass filters) as the high frequency components are either non-existent or largely attenuated by the output lowpass filter.

In most reported designs, the 3-state and conventional 2-state architectures are respectively routinely employed in filterless and traditional Class D amplifiers. This is because in typical designs, the filterless Class D amplifier based on the 3-state

architecture features higher power-efficiency compared to that based on the conventional (2-state) architecture. It is unknown that if certain circuit conditions are satisfied, the conventional architecture can perhaps be employed as filterless Class D amplifiers and their power-efficiency can be comparable to that of filterless Class D amplifiers based on the 3-state architecture.

In summary, there are strong motivations to investigate various aspects of analog Class D amplifier designs, in part to exploit their higher power-efficiency advantage (over classical linear amplifiers) and mitigate their inferior non-linearity figures-of-merit. These aspects include an investigation into the non-linearities of and their mechanisms in various analog Class D amplifier modulation techniques, and into power dissipation (and power-efficiency) and modeling of the loudspeaker for filterless analog Class D amplifiers. There are also motivations to propose novel methodologies to reduce these non-linearities. The technical results/outcomes of these motivations should provide useful and profound insight into the design of these analog Class D amplifiers (vis-à-vis an empirical approach), thereby providing designers with an analytical and deterministic means to optimize various figures-of-merit (and/or a trade-off of various parameters) of their Class D amplifier designs.

1.2 Objectives

In view of abovementioned motivations, the overall objectives of the Ph.D research program pertain to improving the fidelity and the power-efficiency of analog Class D amplifiers, including investigations into the mechanisms of some of the non-

linearities of various Class D amplifiers, proposals of novel design methodologies to mitigate these non-linearities, investigations into power dissipation and power-efficiency of filterless Class D amplifiers, and modeling of loudspeakers. The specific objectives are:

- (i) An investigation into the mechanisms of power supply-related non-linearities (the PSRR and PS-IMD) of PWM Class D amplifiers, and proposals of circuit design methodologies with low hardware overheads to mitigate these non-linearities;
- (ii) An investigation into the power-efficiency of Bang-Bang control Class D amplifiers designed for power-critical low-voltage applications (e.g. hearing instruments), and a comparison of the power-efficiency of Bang-Bang control Class D amplifiers and PWM Class D amplifiers;
- (iii) Further to (ii), an investigation into the mechanisms of the input signal-related non-linearity (the THD) and of power supply-related non-linearities (the PSRR and PS-IMD) of Bang-Bang control Class D amplifiers;
- (iv) An investigation into the power dissipation and power-efficiency of filterless PWM Class D amplifiers; and
- (v) Further to (iv), an investigation into the modeling of loudspeakers (beyond the audio frequency range).

1.3 Contributions

A number of contributions are made in this Ph.D research program, and they are largely reported in 4 journal [5, 27-29] and 5 conferences [30-34] publications. To the best of the author's knowledge, all contributions herein are novel and unreported in the literature.

The contributions pertaining to the aforesaid objective (i) include:

- (a) An investigation into the mechanisms of power supply-related non-linearities, specifically the PSRR and PS-IMD, of various PWM Class D amplifiers. The various PWM Class D amplifiers include the simple open-loop PWM Class D amplifiers, the prevalent single-feedback PWM Class D amplifiers and the higher fidelity double-feedback PWM Class D amplifiers. The contributions herein include the derivation of expressions to provide an analytical means to quantify the PSRR and PS-IMD of the three aforesaid PWM Class D amplifiers, and they delineate the effects of various parameters thereof.
- (b) The proposal of a simple method, with very low hardware overheads, to improve the PSRR and PS-IMD of PWM Class D amplifiers. The improvement is a worthy ~26dB.
- (c) Further to (b), the derivation of expressions to provide an analytical means to quantify the PSRR and PS-IMD of PWM Class D amplifiers for the abovementioned proposed simple method. These expressions delineate the effects of the key parameters thereof arising from the proposed simple method.

The contributions pertaining to the aforesaid objectives (ii) and (iii) include:

- (a) The proposal for the application of the Bang-Bang control Class D amplifier as a viable alternative to the prevalent PWM Class D amplifier for power-critical low-voltage applications, including hearing instruments; Bang-Bang control Class D amplifiers have hitherto been applied only to mid- and high-power amplifier applications.
- (b) In addition to (a) above, a comparison of the power-efficiency of Bang-Bang control Class D amplifiers and PWM Class D amplifiers. The comparison shows that the former indeed has a significant power-efficiency advantage over the latter for power-critical low-voltage applications.
- (c) An investigation into the input signal-related non-linearity (the THD) and the power supply-related non-linearities (the PSRR and PS-IMD) of Bang-Bang control Class D amplifiers. The contributions herein are twofold. First, expressions to provide an analytical means to quantify the THD, PSRR and PS-IMD of an ideal (i.e. all building blocks of the Bang-Bang Class D amplifier are ideal) Bang-Bang control Class D amplifier are derived. These expressions also delineate the effects of various parameters thereof.

Second, expressions embodying the two major practical non-idealities – the propagation delay of the Bang-Bang controller and the output impedance of the Class D output stage – for THD, PSRR and PS-IMD of practical Bang-Bang control Class D amplifiers are derived to provide an analytical means to determine

these non-linearities. These expressions also delineate the effects of the various parameters thereof.

- (d) A comparison of the non-linearities of Bang-Bang control Class D amplifiers and PWM Class D amplifiers. The comparison shows that in most cases, the former features lower non-linearities (than the latter) for power-critical low-voltage applications (including hearing instruments).

The contributions pertaining to the aforesaid objectives (iv) and (v) include:

- (a) An investigation into the power-efficiency and power dissipation of two filterless Class D amplifier architectures – the 3-state architecture and the conventional architecture. The contributions herein include the derivation of expressions to provide an analytical means to quantify the power dissipation in the loudspeaker due to the attenuation of high frequency (beyond the audio frequency range) components and the power-efficiency of the two filterless Class D amplifier architectures. These expressions further provide an analytical means to quantify the actual (vis-à-vis empirical) rating and the required intrinsic inductance of the loudspeaker.
- (b) The proposal for a high frequency (20kHz – 1MHz) loudspeaker model; reported loudspeaker models hitherto are only for the audio frequency range. The proposed model is used for the investigation in (a) above.
- (c) The proposal for using the conventional Class D architecture as a filterless Class D amplifier. This proposal shows that if certain conditions are satisfied, the

conventional architecture can indeed be employed as filterless Class D amplifiers and yet their power-efficiency can be comparable to that of 3-state filterless Class D amplifiers.

All abovementioned contributions, including proposals and derived expressions, are verified on the basis of computer simulations and on measurements on physical circuits either realized discretely or monolithically (prototype IC circuits). From an overall perspective, the contributions made in this research program are significant – they provide useful insight to Class D amplifier designers on the mechanisms of the pertinent non-linearities and of power-efficiency, and an analytical means to quantify the various figures-of-merit and on how various circuit parameters of Class D amplifiers may be varied to meet a given set of design specifications.

1.4 Organization of the Thesis

The subsequent chapters of this thesis are organized in the following manner.

In Chapter 2, a comprehensive literature review on audio amplifiers is provided. The classical linear audio amplifiers, including Class A, Class B and Class AB, are first reviewed, followed by more power-efficient audio amplifiers, including Class G, Class H, Class D and Class AD amplifiers, and finally power-efficiency of the abovementioned audio amplifiers are compared. A more detailed review on Class D amplifiers, including commonly used modulation techniques, design of Class D output stages and design of filterless Class D amplifiers, are also provided.

In Chapter 3, the PSRR and PS-IMD of PWM Class D amplifiers are investigated. This chapter commences with a brief introduction on PSRR and PS-IMD of PWM Class D amplifiers. The three types of PWM Class D amplifiers (open-loop, single-feedback and double-feedback PWM Class D amplifiers) are then modeled and the expressions for the associated PSRR and PS-IMD are derived. Subsequently, a simple design technique to improve PSRR and PS-IMD of PWM Class D amplifiers is proposed and the PSRR and PS-IMD of different amplifiers compared. The derived expressions are verified against HSPICE simulations and hardware measurements. Finally, conclusions are drawn.

In Chapter 4, the THD, PSRR and PS-IMD of Bang-Bang control Class D amplifiers are investigated. This chapter commences with a brief introduction on Bang-Bang control class D amplifier. The power-efficiency of the Bang-Bang control Class D amplifier and the PWM Class D amplifier are then compared. The expression for THD of the Bang-Bang control Class D amplifier is derived, and the pertinent parameters that affect the THD investigated. Subsequently, the PSRR and PS-IMD of the Bang-Bang control Class D amplifier are investigated. The derived expressions are verified against HSPICE simulation and hardware measurements. Finally, conclusions are drawn.

In Chapter 5, the power-efficiency and power dissipation of filterless PWM Class D amplifiers are investigated. This chapter commences with a brief introduction on filterless Class D amplifier and its power dissipation. The model for the loudspeaker in high frequency range is then derived, followed by the expressions for the power dissipation in loudspeaker and the power-efficiency for filterless PWM Class D amplifiers. The analytical work is verified by comparing the results obtained from analytical expressions against hardware measurements. Finally, conclusions are drawn.

In Chapter 6, conclusions of the research program are drawn and recommendations for further work presented.

Chapter 2 A Review of Audio Amplifiers

This chapter provides a comprehensive literature review of audio amplifiers and serves as a preamble to the contributions delineated in Chapters 3, 4 and 5.

In Section 2.1, various audio analog amplifiers are reviewed, including the well established classical (and relatively low power-efficient) linear Class A, Class B and Class AB amplifiers, and the relatively higher power-efficient Class G, Class H, Class D and Class AD amplifiers. In this section, the review includes a comparison of the power-efficiency of these audio amplifiers.

Class D amplifiers can be broadly classified into analog Class D amplifiers and digital Class D amplifiers [35-38]. The analog Class D amplifier (and the abovementioned classical analog amplifiers) typically amplifies an analog input signal from a preceding circuit (such as a pre-amplifier or a digital-to-analog converter). The digital Class D amplifier, on the other hand, processes a digital input signal (e.g. a pulse-code modulation signal) and converts the digital input signal to the desired output signal (e.g. PWM signal). The preceding circuit to a digital Class D amplifier is usually a digital signal processor. A comprehensive literature review on digital Class D amplifier may be found in [36]. Analog Class D amplifiers and digital Class D amplifiers have their own merits and drawbacks. The merits of digital Class D amplifiers include the elimination of the digital-to-analog converter, hence reducing the overall IC area and power dissipation of the audio system. Its drawback includes susceptibility to supply noise, largely because

digital Class D amplifiers are mostly open-loop designs. At this juncture, analog Class D amplifiers are more prevalent than digital Class D amplifiers probably because the design of the analog Class D amplifier is more mature, and the architecture typically embodies negative feedback. In view of this, the analog Class D amplifier is the Class D amplifier of interest in this research program.

Section 2.2 comprehensively reviews analog Class D amplifiers, including a review of various modulation techniques employed in Class D amplifiers, the design of reported Class D output stages, and the design of reported filterless Class D amplifiers. The review herein includes a critical review of the merits and drawbacks of these reported techniques. A conclusion is drawn in section 2.3.

2.1 An Overview of Audio Amplifiers

2.1.1 Classical Linear Audio Amplifiers

Audio amplifiers are traditionally linear amplifiers and are typically classified by the biasing condition of their output transistors [39]. Even with identical input and gain stages, audio amplifiers with different output stages exhibit different levels of performance and power-efficiency. The most common classes of linear audio amplifiers are Class A, Class B and Class AB.

In a Class A amplifier (Figure 2-1(a)), the output transistors are biased at a current I_{bias} greater than the maximum output current. Both transistors are 'on' for the entire cycle of the output signal (Figure 2-1(b)), and are always operating in their active region

regardless of the level of their input and output signals. As a result, Class A amplifiers often exhibit lower non-linearities compared to other classes of audio amplifiers; see later. Due to the large bias current, the power-efficiency of a Class A amplifier is typically very low – the maximum power-efficiency is 25% for a single-ended stage [39] and 50% for a push-pull stage [40]. It is worthwhile to note that this maximum power-efficiency is attained only when the output signal is at its maximum amplitude (i.e. when the modulation index $M=1$). At the typical operating condition where the output signal level is about 15dB to 20dB below the maximum (e.g. $M = 0.15$, and due to the crest factor of audio signals), the power-efficiency is poor – only a few percent (see Figure 2-6 later).

Figure 2-1 (a) Schematic of a Class A amplifier, and (b) its waveform

In a Class B amplifier (Figure 2-2(a)), the output transistors are biased at zero DC current and each output transistor only conducts for half of the output signal cycle (Figure 2-2(b)). Compared to the Class A amplifier, the power-efficiency of the Class B amplifier is higher – its maximum power-efficiency amplifier is 78.5% [39, 40]. As mentioned previously, at the typical operating condition when the signal swing is usually considerably lower than the maximum swing, its power-efficiency is substantially lower (see Figure 2-6 later), but higher than the Class A amplifier. However, the major drawback of the Class B amplifier is the large crossover distortion due to the time it takes to turn one transistor off and the other transistor on.

Figure 2-2 (a) Schematic of a Class B amplifier, and (b) its waveform

In a Class AB amplifier (Figure 2-3(a)), the output transistors are biased at a nonzero DC current that is much smaller than the bias current in a Class A amplifier.

Each transistor conducts for more than a half of the output signal cycle (Figure 2-3(b)). Consequently, the power-efficiency and the non-linearities of the Class AB amplifier are in between that of the Class A amplifier and the Class B amplifier (see Figure 2-6 later).

Figure 2-3 (a) Schematic of a Class AB amplifier, and (b) its waveform

In summary, amongst the abovementioned classical linear amplifiers, the Class A amplifier exhibits the lowest non-linearities but the lowest power-efficiency. The Class B amplifier, on the other hand, exhibits the highest power-efficiency but the highest non-linearities. The power-efficiency and the non-linearities of the Class AB amplifier are in between the Class A amplifier and the Class B amplifier. In general, the power-efficiency of all the three classes of audio amplifiers are low at the typical audio amplifier operating condition (see Figure 2-6 later).

2.1.2 High Power-Efficiency Audio Amplifiers

There are several high power-efficiency amplifiers reported in the literature, including the Class G [41, 42], Class H [14, 43], Class D [44] and Class AD [45-52] amplifiers. These amplifiers will now be reviewed.

The Class G amplifier proposed by Hitachi in 1977 is essentially a linear amplifier with two or more power supply voltages (that is two or more positive rails and two or more negative rails, vis-à-vis one positive rail and one negative rail in other amplifiers). The amplifier is powered by a high voltage when the input (or output signal) is high, and is otherwise powered by a low supply voltage. There are several ways to realize this, and a common used design is depicted in Figure 2-4.

(a)

Figure 2-4 (a) Schematic of a Class G amplifier, and (b) its waveform

In Figure 2-4(a), the output stage of the Class G amplifier comprises 4 transistors whose collector are connected to one of four voltage supplies, V_H , $-V_H$, V_L , $-V_L$. When the output current of the amplifier is less than a predefined current kI_{max} , transistors NPN_1 and PNP_1 conduct and are powered by V_L and $-V_L$ while NPN_2 and PNP_2 are turned off. When the current exceeds kI_{max} , all the four transistors conduct and are powered by V_H and $-V_H$; the power supplies V_L and $-V_L$ are disconnected because the diodes are reverse-biased. This results in relatively high power-efficiency at low modulation index compared to the Class A, Class B and Class AB amplifiers; see Figure 2-6 later.

The Class H amplifier [14, 43], also a linear amplifier, takes the Class G design one step further by modulating the power supply voltage according to the input signal. The impetus for this design approach is to further improve the power-efficiency. This improved power-efficiency is obtained by allowing the power supply to track the input signal.

Unlike the preceding linear amplifiers, the Class D amplifier [44] is essentially a switching amplifier, and features high power-efficiency. This high power-efficiency is obtained because the transistors in its output stage operate either in the ohmic region or in the cut-off region instead of the active region in the aforesaid linear amplifiers. Specifically, when the transistors are turned on and conduct large current (in the ohmic operation region), only a small voltage drops across the source and drain of the transistor. On the other hand, when they are turned off, no current conducts, resulting in virtually zero static bias current (except for a very small leakage current). The power-efficiency of a properly designed Class D amplifier can be very high, for example >90% over a large modulation index range – substantially higher than the other classes of audio amplifiers; see Figure 2-6 later. Nevertheless, one drawback of the Class D amplifier is the relatively high non-linearities compared to its linear counterparts. A comprehensive literature review on Class D amplifiers will be provided in the next section.

Another class of power-efficient amplifiers is the Class AD amplifier [45-52], sometimes called the switch-mode assisted linear amplifier [45] or Class K amplifier [48]. As its name implies, the Class AD amplifier is a combination of a switching (Class D) amplifier and a linear (Class A, Class B or Class AB) amplifier. Figure 2-5 depicts the block diagram of a Class AD amplifier, comprising a linear amplifier, a Class D amplifier, a current sensing block and a feedback loop. The high power-efficiency Class D amplifier provides most of the current needed in the load. The linear amplifier injects a small amount of current to the load to cancel the ripple current generated by the Class D stage due to switching. The switching of the Class D stage is controlled by the current sensing and the feedback of the Class AD amplifier. Due to the combination of the low distortion

linear amplifier and the high power-efficiency Class D amplifier, the Class AD amplifier features higher power-efficiency (see later in Figure 2-6) than the linear amplifier but lower than the Class D amplifier. Some researchers claim that the Class AD amplifier features lower distortion than the Class D amplifier, but this claim is somewhat contentious in the author's experience.

Figure 2-5 Block diagram of a Class AD amplifier

2.1.3 A Comparison of the Power-Efficiency of Audio Amplifiers

Figure 2-6 compares the power-efficiency of the abovementioned linear and high power-efficiency audio amplifiers (output stage). It is apparent from Figure 2-6 that amongst these amplifiers, the Class D amplifier features the highest power-efficiency, particularly when the modulation index, M , is low. For instance, at the typical operating condition of $M = 0.15$ (due to the large crest factor of audio signals), the power-efficiency of the Class D amplifier is $\sim 50\%$, much higher than other amplifiers. In view of its high power-efficiency, the Class D amplifier is the audio amplifier of interest in this research program.

Figure 2-6 Power-efficiency of output stages of various audio amplifiers

2.2 A Review of Class D Amplifiers

The Class D amplifier was probably first proposed in the 1950s by A. H. Reeves [14], the ‘father’ of Pulse Code Modulation, and the first commercial Class D amplifier [14] was probably reported by Gordon Edge and Jim Westwood in 1964. However, the Class D amplifier did not receive much acceptance until the 1980s due to the poor performance of the power transistors (such as low switching speed). Between 1979 and 1985, there was rapid development of power MOSFETs, and the power MOSFET was

able to switch up to 500kHz with acceptable losses. Finally, in 1983, a relatively high-fidelity Class D with $\text{THD} < 0.3\%$ was reported by Brian Attwood [44], and the Class D amplifiers thereafter became increasingly accepted. At this present day, Class D amplifiers are ubiquitous and can be found in many devices, ranging from low-power devices such as hearing instruments [15, 53-56] (and mobile phones [57-60]) to mid-power devices such as TVs [61, 62] to high-power devices such as public address systems.

As mentioned in Chapter 1, a typical Class D amplifier comprises a modulator, an output stage and a load (including a lowpass filter and a loudspeaker). For ease of description of each block, Figure 1-1 is redrawn below in Figure 2-7.

Figure 2-7 Block diagram of a Class D amplifier

Modulator

The modulator modulates the input analog signal into a digital-like modulated signal. The modulated signal serves as a control signal to control the switching in the output stage. The common modulation techniques employed in analog Class D amplifiers include (i) PWM [44], (ii) Sigma-Delta [63], (iii) Bang-Bang control [64], (iv) Self-

Oscillating [65], and (v) Sliding Mode control [66]. The selection of the modulation technique is particularly pertinent at the system level design of Class D amplifiers as the modulation technique directly affects the non-linearities, hardware complexity, IC area (hence cost), and switching frequency (hence power dissipation and power-efficiency) of the Class D amplifier. Each modulation technique has its advantages and drawbacks. A review on these modulation techniques, including their advantages and drawbacks, will be provided in the next section.

Output Stage

The function of the Class D output stage is to provide sufficient power to drive the low impedance loudspeaker load (4Ω to 32Ω in general audio applications, and typically 200Ω to 600Ω in hearing instruments). The output stage can be configured as single-ended shown in Figure 2-8 or as bridge-tied load (BTL) shown in Figure 2-9. In the single-ended Class D amplifier, a decoupling capacitor is usually needed to prevent the DC current from flowing in the loudspeaker. The BTL output stage comprises two single-ended output stages and generates a differential output signal at load. The two configurations are prevalent in practical designs, and each has its own advantages and drawbacks. For example, the BTL output stage features 6dB higher output power (for the same power supply and same load), and less susceptible to common-mode noise compared to the single-ended output stage. Its drawbacks, on the other hand, include larger IC area (~ 2 times of the area of the single-ended output stage), and lower power-efficiency for the same output impedance [67] (due to the doubling of the on output impedance of the Class D output stage; see section 2.2.2 later). Practically, the BTL

output stage is more common in the applications where high output power is required and in low-voltage applications where the supply voltage is limited. The single-ended output stage, on the other hand, is more common in the applications where small IC area and/or high power-efficiency are desired.

Figure 2-8 Schematic of a single-ended Class D output stage with load

Figure 2-9 Schematic of a BTL Class D output stage with load

In general audio applications whose loudspeaker impedance is 4Ω to 32Ω , the Class D output stage typically occupies $>50\%$ of the total IC area and dissipates $\sim 90\%$ of the total power. A detailed review on the design of Class D output stage, including the

optimization of the power-efficiency and design of the protection circuits, will be provided in section 2.2.2 later.

Lowpass filter and loudspeaker

In traditional Class D amplifiers, an output lowpass filter is required to attenuate the high frequency components in the output signal due to switching, and to recover the desired low frequency audio signal. As previously mentioned in Chapter 1, the need of the bulky lowpass filter sometimes defeats the smaller form-factor advantage of Class D amplifiers. An ‘untraditional’ (termed ‘filterless’) approach, where the abovementioned output filter is not required, has recently received some acceptance. In filterless Class D amplifiers, an inductive loudspeaker is required in place of the output lowpass filter to attenuate the high frequency carrier current (and related components). The filterless Class D amplifiers will be reviewed in section 2.2.3 later.

2.2.1 Class D Modulation Techniques

2.2.1.1 PWM Class D amplifiers

Amongst the abovementioned modulation techniques, the PWM Class D amplifier (henceforth abbreviated PWM amplifier) is most prevalent due to its hardware simplicity and low switching frequency (hence low power dissipation and high power-efficiency). A PWM amplifier can be implemented as a simple open-loop PWM amplifier, prevalent single-feedback PWM amplifier, or as the high-fidelity double-feedback PWM amplifier;

higher-order feedback designs are possible but the stability can be difficult and the hardware requirements high – they are hence unpopular.

The schematic of an open-loop PWM amplifier is depicted in Figure 2-10, comprising a PWM modulator (including a carrier generator and a comparator), an output stage and a load (including a lowpass filter and a loudspeaker). The comparator compares the input (modulating) signal with the internally generated carrier signal (by the carrier generator). The carrier frequency is usually much higher (typically > 6 times) than the input modulating frequency. The carrier frequency of V_M is the same as the carrier frequency. V_M serves as an input signal to the Class D output stage and controls the switching of the output stage. The output stage amplifies (in terms of power and/or voltage) V_M and provides drive to the load. The output signal, V_{out} , of the output stage is also a PWM signal. The waveforms at the pertinent nodes of the open-loop PWM amplifier are depicted in Figure 2-11.

Figure 2-10 Schematic of an open-loop PWM amplifier

Figure 2-11 Waveforms of a PWM Class D amplifier

PWM signals are well established. For example, the double-Fourier expression [68] for the PWM signal generated from an ideal (i.e. the carrier generator, comparator, output stage and the output lowpass filter are ideal) PWM amplifier is expressed in eqn. (2.1). The first term in eqn. (2.1) is the replica of the input signal, the desired output. The second term is the high frequency distortion components arising from the intermodulation between the carrier and input signals, and is inconsequential as it can be largely attenuated by the output lowpass filter.

$$\begin{aligned} \frac{V_{out}}{V_{DD}} &= M \cos(2\pi f_{in} t) \\ &+ 4 \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(4m\pi f_{sw} t + 4n\pi f_{in} t) \sin\left(\frac{m+n}{2}\pi\right) \end{aligned} \quad (2.1)$$

where V_{DD} is the supply voltage,

M is the modulation index,

f_{in} is the input frequency,

f_{sw} is the switching (carrier) frequency, and

$J_n()$ is the Bessel function of the first kind with order n .

It is apparent from eqn. (2.1) that the harmonic distortion components of the desired output signal are non-existent. In other words, there is zero THD in the output of an ideal open-loop PWM amplifier. The definition for THD is well established [4] and is:

$$\text{THD} = \frac{1}{V_{out}(f_{in})} \sqrt{\sum_{n=2}^{\infty} V_{out}(nf_{in})^2} \times 100\% \quad (2.2)$$

Although there is zero THD in the output of an ideal open-loop PWM amplifier, the THD in the output of a practical open-loop PWM amplifier is usually unacceptably high, 2% - 5% [69, 70]. The high THD arises primarily from the non-linearities in the carrier [69], and the dead time in the Class D output stage [70]. In addition to the high THD, other drawbacks of the open-loop PWM amplifier include a low PSRR (an unacceptable 6dB) [71] and a high PS-IMD (-9dB in the worst case condition where the modulation index, $M = 1$); these will be shown later in Chapter 3. It is worthwhile to remark that the high THD, low PSRR and high PS-IMD are only tolerated in power-

critical and hardware-critical applications, such as hearing instruments, but not tolerated in general audio applications.

As the non-linearities of open-loop PWM amplifiers are largely unacceptable, the PWM amplifiers that are typically used in practice are PWM amplifiers with feedback [72-75], also known as closed-loop PWM amplifiers. Examples of closed-loop PWM amplifiers include single-feedback, double-feedback, etc.

Figure 2-12 depicts a single-feedback PWM amplifier, comprising a 2nd-order integrator, an open-loop PWM amplifier, an input and feedback resistor, R_1 and R_{fb1} , and a load (including a lowpass filter and a loudspeaker). The THD in the single-feedback PWM amplifier is mainly due to (i) the harmonic distortions in the open-loop PWM amplifier, (ii) the phase error [76], and (iii) the duty cycle error [76]. The THD due to (i) arises mainly from the non-linearities in the carrier and the dead time in the Class D output stage. It is well established [74-76] that due to the negative feedback, the THD due to (i) is considerably reduced by a factor of $LG+1$ (where LG is the loop-gain of the closed-loop PWM amplifier) compared to the open-loop PWM amplifier. The THD due to (ii) and (iii) are recently established [76, 77], and arise from the feedback due to switching of the PWM signal. The analytical expressions for these THDs have been recently reported including deterministic methods to mitigate them.

Figure 2-12 Schematic of a single-feedback PWM Class D amplifier

Specifically, the THD due to (i), (ii) and (iii) are denoted as $\text{THD}_{1\text{FB_OL}}$, $\text{THD}_{1\text{FB}_\varphi}$ and $\text{THD}_{1\text{FB_D}}$ respectively, and they are expressed in eqns. (2.3) – (2.5) [76] below.

$$\text{THD}_{1\text{FB_OL}} = \frac{1}{V_{out}(f_{in})} \sqrt{\sum_{n=2}^{\infty} \left(\frac{\text{Dist}_n}{1 + LG_{1\text{FB}}(nf_{in})} \right)^2} \times 100\% \quad (2.3)$$

$$\text{THD}_{1\text{FB}_\varphi} = \frac{1}{2} J_1 \left(\frac{\pi f_{in} M^2}{16 f_{sw}^2 R_{fb1} C} \right) \times 100\% \quad (2.4)$$

$$\text{THD}_{1\text{FB_D}} = \sum_{m=1}^{\infty} \frac{\frac{4(-1)^m}{m\pi} J_m \left(\frac{m A \pi}{2} \right) \cos m\theta J_3 \left(\frac{m M \pi}{2} \right)}{M(1 + LG_{1\text{FB}}(3f_{in}))} \times 100\% \quad (2.5)$$

where Dist_n is the amplitude of the n^{th} -order harmonic distortion (i.e. the harmonic

distortion at frequency nf_{in}) of the open-loop PWM amplifier,

$LG_{1\text{FB}}(f)$ is the loop-gain of the single-feedback PWM amplifier at frequency f ,

$J_m()$ is Bessel function of the first kind with order m , and

A is the amplitude of the attenuated carrier, that is

$$A \approx \frac{2J_0\left(\frac{\pi M}{2}\right)}{\pi} LG_{1FB}(f_{sw})$$

It has been shown [76, 78-80] that amongst the abovementioned THDs, THD_{1FB_D} and THD_{1FB_p} are usually dominant. In other words, to reduce THD, it is imperative that the THD_{1FB_D} and THD_{1FB_p} be low, specifically, f_{sw} be high, $LG_{1FB}(3f_{in})$ be high and that $LG_{1FB}(f_{sw})$ be low. Furthermore, to reduce THD_{1FB_p} , several methods have been reported [77-80], and some of these proposed methods can reduce the THD to a very low level, for example, $THD < 0.01\%$ (at 7kHz input frequency).

Similar to the single-ended PWM amplifier, the THDs in the double-feedback PWM amplifier (see later in Figure 3-3 for an example) are also due to the (i) harmonic distortions in the open-loop PWM amplifier, (ii) phase error, and the (iii) duty cycle error. The expressions for these THDs can be similarly expressed. It has been shown [76] that the overall THD of the double-feedback PWM amplifier is usually comparable to the single-feedback PWM amplifier. This is because the dominant THDs, the THDs due to (ii) and (iii), in the double-feedback PWM amplifier are comparable to that in the single-feedback PWM amplifier. This is interesting because this is in spite of the fact that the THD due to (i) in double-feedback PWM amplifier is significantly lower than that in the single-feedback PWM amplifier. A more detailed analysis on the THD in double-feedback PWM amplifiers can be found in [76].

2.2.1.2 Sigma-Delta Class D amplifiers

Another modulation method commonly used to realize a Class D amplifier is the Sigma-Delta ($\Sigma\Delta$) Modulation [63, 81-84]. The primary advantage of $\Sigma\Delta$ modulation techniques is its lower non-linearities and lower noise (higher SNR) compared to other modulation techniques, such as PWM and Bang-Bang control. For example, a 3rd-order $\Sigma\Delta$ amplifier can feature a THD plus noise (THD+N) of 0.1% at 500kHz clock frequency [31], and a 7th-order $\Sigma\Delta$ -Class D amplifier can feature a THD+N of 0.001% at 450kHz clock frequency [85-87].

This approach is somewhat akin to the $\Sigma\Delta$ modulation approach in data converters where a high-order (>3rd-order) modulation is employed to shape the noise to a region that is out-of-band (a frequency range that is not within the frequency band of interest). The drawbacks of the $\Sigma\Delta$ modulation technique include increased circuit complexity (particularly when a high-order $\Sigma\Delta$ modulator is used), and high switching frequency (hence higher power dissipation and low power-efficiency).

On the basis of various quantizer designs depicted in Figure 2-13 and Figure 2-14 (see later), $\Sigma\Delta$ Class D amplifiers (abbreviated $\Sigma\Delta$ amplifiers) can be categorized into: (i) synchronous $\Sigma\Delta$ amplifier, and (ii) asynchronous $\Sigma\Delta$ amplifier. The quantizer in the former is realized using a comparator followed by a D-flip flop, whilst the quantizer in the latter is realized using a hysteresis comparator. The difference in their quantizer realizations consequently results in different non-linearities, and this will be delineated in the following review of these two $\Sigma\Delta$ amplifier types.

Synchronous $\Sigma\Delta$ Class D amplifiers

The schematic of a first-order synchronous $\Sigma\Delta$ amplifier is depicted in Figure 2-13(a), comprising an integrator, a quantizer (realized using a comparator and a D-flip flop), a feedback network, an output stage and a load. The integrator integrates the difference between the input and output signals, and shapes the quantization noise (generated during sampling due to finite sampling rate) to a frequency range that is out of the signal band of interest. The integrator output signal is fed to a comparator. The comparator generates a digital-like signal by comparing the integrator output against a pre-defined reference (usually the signal ground of the amplifier). The D-flip flop samples the comparator output at a high sampling frequency, f_s . The output of the D-flip flop (and the output of the output stage) is a Pulse Density Modulated (PDM) signal. Finally, the desired analog signal is recovered at the lowpass filter output. The signals of the synchronous $\Sigma\Delta$ amplifier are depicted in Figure 2-13(b). Note that the switching frequency of the $\Sigma\Delta$ amplifier varies with the magnitude of the input signal – this is different from the PWM amplifier whose switching frequency is independent of the input signal.

Figure 2-13 (a) Schematic of a first-order synchronous Sigma-Delta Class D amplifier, and (b) its waveforms

It is well established [63] that the in-band quantization noise, $N_{\Sigma\Delta 1}$, in the first order $\Sigma\Delta$ modulator is:

$$N_{\Sigma\Delta 1} = \int_{-BW}^{BW} \frac{N_s}{f_s} \left| 1 - \exp\left(-\frac{j2\pi f}{f_s}\right) \right|^2 df \approx \frac{\pi^2}{3} \frac{N_s}{[f_s/(2BW)]^3} \quad (2.6)$$

where N_s is the quantization noise of a Nyquist-rate system whose sampling frequency is twice of the bandwidth, BW.

It is apparent from eqn. (2.6) that a higher sampling frequency results in lower quantization noise, but at the cost of higher switching frequency in the Class D output stage. This higher switching frequency implies undesirable higher power dissipation and lower power-efficiency.

One of the most direct ways to reduce the in-band quantization noise is to use a high-order $\Sigma\Delta$ modulator. The in-band quantization noise, $N_{\Sigma\Delta,n}$, of an n^{th} -order $\Sigma\Delta$ modulator is expressed [63] in eqn. (2.7).

$$N_{\Sigma\Delta,n} = \int_{-BW}^{BW} \frac{N_s}{f_s} \left| 1 - \exp\left(-\frac{j2\pi f}{f_s}\right) \right|^{2n} df \quad (2.7)$$

$$\approx \frac{\pi^{2n}}{2n+1} \frac{N_s}{[f_s/(2BW)]^{2n+1}}$$

It is apparent from eqn. (2.7) that the higher the order of the modulator and the higher the sampling frequency, the lower is in-band quantization noise. Note that increasing the modulator order undesirably incurs increased hardware and hence cost.

Interestingly, although the noise mechanisms of synchronous $\Sigma\Delta$ amplifier are well established [63], the mechanisms of their non-linearities (including the THD, IMD, PSRR and PS-IMD) remain unreported. This may be due to the general appreciation that the non-linearities of synchronous $\Sigma\Delta$ amplifiers are very low.

Asynchronous $\Sigma\Delta$ Class D amplifiers

Unlike the synchronous $\Sigma\Delta$ amplifier whose quantizer is implemented using a comparator and a D-flip flop, the quantizer of an asynchronous $\Sigma\Delta$ amplifier is implemented using a hysteresis comparator. The block diagram of an asynchronous $\Sigma\Delta$ amplifier is depicted in Figure 2-14. Due to the continuous control of the hysteresis comparator, the quantization noise of an ideal asynchronous $\Sigma\Delta$ amplifier is theoretically zero [88] – this is unlike the ideal synchronous $\Sigma\Delta$ amplifier whose quantization noise is expressed in eqn. (2.7).

Figure 2-14 Schematic of a first-order asynchronous Sigma-Delta Class D amplifier

It has been shown [89] that the output of an ideal first-order asynchronous $\Sigma\Delta$ amplifier, V_{ASD} , is:

$$V_{ASD} = V_{DD}M \sin(2\pi f_{in}t) + \sum_{i=1}^{\infty} \sum_{n=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} \left[\frac{2V_{DD}(1 - (-1)^{i+2n+k})}{i\pi} J_n\left(\frac{iM^2 f_{sw}}{4f_{in}}\right) J_k\left(\frac{i\pi M}{2}\right) \cdot \sin\left(2\pi i f_{sw} \left(1 - \frac{M^2}{2}\right)t + 2\pi(2n+k)f_{in}t + \frac{i\pi}{2}\right) \right] \quad (2.8)$$

where f_{sw} is the idle switching frequency of the asynchronous $\Sigma\Delta$ amplifier.

Eqn. (2.8) can be interpreted as follows. The first term in eqn. (2.8) is the amplified replica of the input signal, the desired output signal. The second term is the high frequency intermodulation components between the input and switching components, and is usually inconsequential as these components can be largely attenuated by the output lowpass filter. It is apparent from eqn. (2.8) that the THD of an ideal asynchronous $\Sigma\Delta$ amplifier is zero.

Despite the appreciation that the THD of an ideal asynchronous $\Sigma\Delta$ amplifier is zero, other nonlinearities (including IMD, PSRR and PS-IMD) of the ideal asynchronous $\Sigma\Delta$ amplifier remain unreported. Likewise, the non-linearities of a practical asynchronous $\Sigma\Delta$ amplifier are also unreported.

2.2.1.3 Bang-Bang Control Class D amplifiers

Compared to PWM and $\Sigma\Delta$ modulations, the Bang-Bang Control modulation is less popular due to the advantages already offered by the PWM and the $\Sigma\Delta$ modulation approaches. Nevertheless, there is some recent interest [30-32, 48, 64] in this approach because of its simpler hardware compared to the PWM and the $\Sigma\Delta$ amplifiers. It will be

shown later in Chapter 4 that its simpler hardware consequently results in higher power-efficiency for power-critical low-voltage applications, including hearing instruments.

Figure 2-15(a) depicts the block diagram of a Bang-Bang control Class D amplifier (abbreviated as the Bang-Bang amplifier), comprising a Bang-Bang Controller, an output stage, a load and a feedback network. The feedback network, usually implemented using a 1st-order lowpass filter, feeds the noise-shaped output signal back to the input stage. The resultant signal, V_{error} , is the error between the desired output and actual output. The Bang-Bang controller, implemented using a hysteresis comparator, instantaneously compares the error signal against its hysteresis. Once the error signal exceeds the hysteresis band, the controller output state changes. The output of the controller, as a result, is a rectangular waveform that transitions between binary '0' and binary '1'. The Bang-Bang modulated signal is PDM-like – similar to the modulated signal in the asynchronous $\Sigma\Delta$ amplifier. Finally, the desired analog signal is obtained at the filter output. The waveforms of the Bang-Bang amplifier are shown in Figure 2-15(b).

Figure 2-15 (a) Block diagram of a Bang-Bang control Class D amplifier, and (b) its waveforms

It can be seen from a comparison of Figure 2-15(a) and Figure 2-12 that the Bang-Bang amplifier features simpler hardware (compared to the PWM amplifier). Specifically, the integrator and the carrier generator needed in the PWM amplifier are not required in the Bang-Bang amplifier. It will be shown later in Chapter 4 that its simpler hardware consequently results in higher power-efficiency in power-critical low-voltage applications, including hearing instruments.

The non-linearities of the Bang-Bang amplifiers are unestablished in the literature and some of these non-linearities, including THD, PSRR and PS-IMD, will be investigated in Chapter 4.

2.2.1.4 Self-Oscillating Class D amplifiers

In addition to abovementioned modulation techniques, self-oscillating [65, 90-95] is another modulation technique employed in Class D amplifiers. The block diagram of a self-oscillating Class D amplifier is depicted in Figure 2-16, and it comprises a modulator

(usually realized using a comparator), an output stage, a feedback network and a load (comprising a lowpass filter and a loudspeaker). The feedback can be taken at either the output of the output stage or at the output of the lowpass filter. It has been shown [95] that the self-oscillating Class D amplifiers whose feedback is taken at the output of the lowpass filter features lower non-linearities. This is because the non-linearities introduced by the lowpass filter can be suppressed by the feedback network.

Figure 2-16 Block diagram of a self-oscillating Class D amplifier

The operation principle of the self-oscillating Class D amplifier is similar to that of a normal oscillator. Oscillation occurs at the frequency where the total phase shift in the feedback network and the modulator is 180° . As the self-oscillating Class D amplifier is innately unstable (oscillation), there is no stability problem.

Some self-oscillating Class D amplifiers feature comparable THD as $\Sigma\Delta$ amplifiers. For example, a 250W self-oscillating Class D amplifier with lead/lag compensation circuit in feedback loop features an excellent THD+N of 0.005% [96]. Another self-oscillating Class D amplifier with the feedback taking after lowpass filter features 0.02% THD+N [93].

2.2.1.5 Sliding Mode control Class D amplifiers

Sliding Mode control Class D amplifiers [66, 97] are recently reported. The schematic of a sliding mode design and its block diagram are depicted in Figure 2-17(a) and Figure 2-17 (b).

Figure 2-17 (a) Schematic of a Sliding Mode control Class D amplifier and (b) its block diagram

In the Sliding Mode control Class D amplifier, the Sliding Mode controller (shown in the dotted box) and the comparator control the switching of the Class D amplifier. Op-amps A and C serve to increase the overall loop gain of the Class D amplifier, and the non-linearities of the Class D amplifier are consequently reduced. This design features a somewhat high THD of 0.8% at modulation index = 0.1.

One drawback of this design is its hardware complexity and high power dissipation. In view of this, an improved design is reported [97], and the schematic of the improved design is depicted in Figure 2-18 below. Compared to the design depicted in Figure 2-17 earlier, the improved design features significantly simplified hardware but comparable somewhat high THD.

Figure 2-18 Schematic of an improved Sliding Mode control Class D amplifier

2.2.2 Class D Output Stages

As previously mentioned, the Class D output stage is an integral block in a Class D amplifier because it not only usually occupies the largest area of the total IC area, it typically dissipates the largest power (of the total power). For instance, in general audio applications whose loudspeaker impedance is 4Ω to 32Ω , the Class D output stage usually occupies $>50\%$ of the total IC area and dissipates $\sim 90\%$ of the total power.

The simplest method [98] to realize an output stage, as shown in Figure 2-19, is to use a cascade of inverters whose aspect ratios (of the transistors therein) are increased from the input to the output. Each inverter functions as a driver to drive the next (higher aspect ratio) inverter. The final inverter functions as the (two) power transistors that serve as the low impedance driver stage to drive the loudspeaker load. This simplistic design is typically only applicable in low-voltage applications where the supply voltage is approximately equal to the sum of threshold voltages of the PMOS and NMOS transistors of the inverters. For example, in the hearing instrument application whose supply voltage is $\sim 1.3\text{V}$, the sum of the threshold voltages of the PMOS and NMOS transistors is $\sim 1.2\text{V}$.

Figure 2-19 Schematic of a Class D output stage realized using a cascade of inverters

In applications where the supply voltage is higher than the sum of the threshold voltages of the PMOS and NMOS transistors (e.g. where the supply voltage is 5V, and the sum of the threshold voltages is ~1.2V), there may be a short period when both the PMOS and NMOS transistors are simultaneously turned ‘on’ during the switching transitions. This may consequently result in a large short circuit current, i.e. the current flowing from one supply rail to the other (or ground for a single rail design). This short circuit current increases the power dissipation of the output stage, thereby reducing the power-efficiency. It may also damage the output stage if the short circuit current is higher than the maximum allowable current, if the heat generated is not sufficiently dissipated, or if the temperature is higher than the maximum allowable temperature (see details in Section 2.2.2.3 later). In view of these issues, this simple design is seldom used in the applications where the supply voltage is higher than the sum of the threshold voltages of the PMOS and NMOS transistors.

The block diagram of a more general (applicable to all applications ranging from low-voltage to high-voltage) Class D output stage is depicted in Figure 2-20. It comprises two power transistors, a dead time block, high-side and low-side drivers, over-current and over-temperature protection circuits, and a control logic. The power transistors provide a low impedance output and sufficient drive to the load. The dead time block generates a small dead time (typically $\sim 50\text{ns}$) to prevent the power transistors from turning on simultaneously, thereby preventing short circuit current during transitions; in practice, there is usually some residual short-circuit current. The high-side and low-side drivers provide sufficient current to drive the output transistors. The over-current protection block protects the Class D output stage from damage due to over-current and/or short circuit. It senses the currents in the power transistors and compares the currents against a reference current. If the currents in the power transistors are larger than the reference current, 'turn off' signals ($V_{\text{OverI_H}}$ and $V_{\text{OverI_L}}$) are input to the control logic, and the control logic turns off one or both power transistor(s) by means of $V_{\text{OverI_H}}$ and/or $V_{\text{OverI_L}}$. The over-temperature protection block protects the Class D output stage from damage due to excessive temperature. It senses the temperature of the IC and compares this temperature (obtained by means of an equivalent voltage or current) against a reference temperature (obtained by a reference voltage or current). If the temperature of the IC is higher than the reference temperature, a 'turn off' signal (V_{OverT}) is input to the control logic to turn off both power transistors. The design of each block will now be discussed in turn.

Figure 2-20 Block diagram of a Class D output stage

2.2.2.1 Power transistors and drivers

The power transistors and drivers of the Class D output stages can be configured either as *p*-channel-cum-*n*-channel inverter configuration [57, 60, 98] depicted in Figure 2-21(a) or as an *n*-channel totem-pole [61, 99, 100] configuration depicted in Figure 2-21(b). Both configurations are equally prevalent and each has its own advantages and drawbacks. For example, the *p*-channel-cum-*n*-channel inverter configuration features a simpler driver design, less number of external components (the bootstrap capacitor and diode are not required) and less number of IC pins (hence smaller footprint), but suffers from a larger IC area (due to lower mobility of the PMOS transistor) compared to the NMOS transistor. In commercial designs, the *p*-channel-cum-*n*-channel inverter configuration is commonly used in low-voltage (<5V) applications [57, 60] whilst the *n*-

channel totem-pole configuration is commonly used in high-voltage ($>10\text{V}$) applications [61, 99].

Figure 2-21 Schematic of drivers and power transistors: (a) *p*-channel-cum-*n*-channel inverter configuration, and (b) *n*-channel totem-pole configuration

The mechanisms of power dissipation and power-efficiency of the Class D output stage using the abovementioned two configurations are well established [67, 98, 101]. Systematic approaches to design the aspect ratio of the power transistor (so that the maximum power-efficiency can be achieved) for both design configurations have also been reported. The power dissipation, power-efficiency and optimization of the two design configurations will now be reviewed.

Power dissipation, power-efficiency and optimization of the p -channel-cum- n -channel output stage

As mentioned earlier, this configuration is usually used in low-voltage (<5V) designs, and in these designs, the CMOS process is preferred (as opposed to DMOS (Double diffused Metal Oxide Semiconductor)) process used in high-voltage Class D output stages) due to its low cost. In view of this, the following review is based on a Class D output stage [98] designed using CMOS.

The power dissipation of the Class D output stage is primarily due to the (i) parasitic capacitance, (ii) short circuit current during transitions and the (iii) 'on' output impedance. It has been shown [98] that the power dissipation due to (i), (ii) and (iii) (denoted as P_{C_pn} , P_{S_pn} , and P_{on_pn} respectively) are:

$$P_{C_pn} = \frac{1}{2} V_{DD}^2 f_C \left[2C_{pad} + (K_1 + K_2) W_p \sum_{i=0}^{N-1} R_{tap}^{-1} \right] \quad (2.9)$$

$$P_{S_pn} = K_3 (V_{DD} - 2V_{th})^3 f_C \tau W_p \sum_{i=0}^{N-1} R_{tap}^{-1} \quad (2.10)$$

$$P_{on_pn} = \frac{1}{2} M^2 I_o R_{on} \quad (2.11)$$

where

$$K_1 = 2 \left(1 + \frac{1}{\alpha} \right) [C_{ox} L + (C_{GSO} + C_{GDO})] \quad (2.12)$$

$$K_2 = 2 \left[\left(C_{JP} + \frac{C_{JN}}{\alpha} \right) L_{DS} + \left(1 + \frac{1}{\alpha} \right) (C_{GDO} + 2C_{JSW}) \right] \quad (2.13)$$

$$K_3 = \frac{1}{6} \frac{\varepsilon_{ox} \mu_p}{t_{ox} L} \quad (2.14)$$

$$R_{on} = \frac{K_4 + \alpha K_5}{W_P} + \frac{2K_6}{(V_{DD} - V_{th})W_P} \quad (2.15)$$

$$K_4 = (l_1 + 2l_3)R_P + 2(l_1 + l_2)R_{ctP} \quad (2.16)$$

$$K_5 = (l_1 + 2l_3)R_N + 2(l_1 + l_2)R_{ctN} \quad (2.17)$$

$$K_6 = \frac{L}{\mu_p C_{ox}} \quad (2.18)$$

The symbols used in eqns. (2.9)-(2.18) are tabulated in Table 2-I.

Table 2-I Symbols used in eqns. (2.9)-(2.18)

α	W_p/W_n
C_{GSO}	Gate-to-source capacitance per unit gate width
C_{GDO}	Gate-to-drain capacitance per unit gate width
C_J	Zero-biased p - n junction area capacitance
C_{JSW}	Zero-biased p - n junction periphery capacitance
C_{ox}	Oxide capacitance per unit gate area
C_{pad}	Bond pad capacitance
M	Modulation index
ϵ_{OX}	Permittivity of gate oxide
L_{DS}	Length of the source or drain area
R_L	Load resistance
R_{cn}	n -type contact resistance per contact
R_{cp}	p -type contact resistance per contact
R_n	Source and drain area resistance per square of an NMOS transistor
R_p	Source and drain area resistance per square of a PMOS transistor
R_{tap}	Tapering factor of a string of inverters
τ	Rise or fall time of a PWM signal
t_{ox}	Gate oxide thickness
μ_p	Hole mobility
V_{th}	Threshold voltage
W_n	Channel width of the NMOS transistor
W_p	Channel width of the PMOS transistor

The definitions of the dimensions l_1 , l_2 , l_3 , L_{DS} and W_n are illustrated in Figure 2-22 below.

Figure 2-22 Layout of an NMOS transistor

Based on eqns. (2.9)-(2.18), the power-efficiency of the output stage, η_{out} , can be easily derived:

$$\eta_{out} = \frac{P_{out}}{P_{out} + P_{C_{pn}} + P_{S_{pn}} + P_{on_{pn}}} \quad (2.19)$$

where P_{out} is the output power.

To obtain the maximum power-efficiency, the following condition should be satisfied [98]:

$$\frac{d\eta_{out}}{dW} = 0$$

The optimum channel width (hence the maximum power-efficiency) can be obtained by solving the above equation:

$$W_{opt_pn} = M \sqrt{\frac{B_1}{B_2 + B_3}} \quad (2.20)$$

where

$$B_1 = \frac{(K_4 + K_5 + \frac{2K_6}{V_{DD} - V_{th}})}{R_L} \quad (2.21)$$

$$B_2 = M^{-2} R_L f_c (K_1 + K_2) \sum_{i=0}^{N-1} R_{tap}^{-i} \quad (2.22)$$

$$B_3 = \frac{2M^{-2} R_L K_3 (V_{DD} - 2V_{th})^3}{V_{DD}^2} \sum_{i=0}^{N-1} R_{tap}^{-i} \quad (2.23)$$

It has been shown [98] that optimizing the channel width at the low modulation index (e.g. $M=0.15$) is more advantageous compared to optimizing at high modulation index (e.g. $M=0.9$). This is because in the lower modulation index range, the power-efficiency optimized at $M=0.15$ is significantly higher than that optimized at $M=0.9$, whilst in the high modulation index range, the two power-efficiencies are comparable. Further, compared to optimizing at $M=0.9$, optimizing the power-efficiency at $M=0.15$ results in 75% reduction in the IC area of the output stage, and this translates to a 50% reduction of the total IC area of the Class D amplifier. In view of this, it is recommended that the power-efficiency should be optimized at $M=0.15$. Note that this is also applicable to the n -channel totem-pole output stage (see later).

Power dissipation and Power-efficiency of n -channel totem-pole output stage

The n -channel totem-pole output stage is usually used in mid- to high-voltage (>5V) applications due to its smaller IC area. In mid- to high-voltage applications, Class D output stages are usually designed using DMOS (or high-voltage CMOS). This is because compared to CMOS, DMOS features a higher breakdown voltage [102-104] and the output impedance is significantly smaller for the same aspect ratio. In this section, the power dissipation and power-efficiency of an n -channel totem-pole output stage designed using DMOS process will be reviewed.

It has been shown [67] that the power dissipation due to the parasitic capacitance and due to the 'on' output impedance are:

$$P_{C_{nn}} = \frac{1}{2} f_c [V_{DD}^2 (2C'_d + 2k_3) + 4V_G^2 C'_g] W + \frac{1}{2} f_c V_{DD}^2 (2C_{pad} + k_4) \quad (2.24)$$

$$P_{r_{nn}} = \frac{1}{2} M^2 I_O^2 \frac{2R'_{on}}{W} \quad (2.25)$$

where

$$C'_d = C_{gdo} + \frac{C_{V1} \times C_{V2}}{C_{V1} + C_{V2}} \times \frac{1}{W_{unit}} \quad (2.26)$$

$$C'_g = C_{OX}L + C_{gso} + C_{gdo} + \frac{C_{V1} \times C_{V2}}{C_{V1} + C_{V2}} \times \frac{1}{W_{unit}} \quad (2.27)$$

$$R_{on} = R_{dsw} \times \frac{1 + P_{rwg}(V_{DD} - V_{th})}{10^6} + \frac{L}{\mu_n C_{ox}(V_{GS} - V_{th})} \quad (2.28)$$

$$+ 2 \left[\left(\frac{l_1}{2} + l_3 \right) R_s + (l_1 + l_2) R_{ct} \right] + R_{pkg}$$

For simplicity, in eqns. (2.24) - (2.29), the same symbols for the NMOS in eqns. (2.9)-(2.18) are used.

On the basis of eqns. (2.24) - (2.29) and the method delineated for the optimization of the p -channel-cum- n -channel output stage, the optimized W for the n -channel totem-pole output stage was reported to be:

$$W_{opt_nn} = \sqrt{\frac{M^2 I_o^2 R'_{on}}{f_c [V_{DD}^2 (C'_d + k_3) + 2V_G^2 C'_g]}} \quad (2.29)$$

Similar to the case of p -channel-cum- n -channel output stage, a comparison of n -channel totem-pole output stages optimized at $M=0.15$ and optimized at $M=0.9$ shows that the output stage optimized $M=0.15$ features higher power-efficiency in the lower modulation index range and ~75% smaller IC area. In view of this, it is recommended that the n -channel totem-pole output stage should be optimized at a low modulation index, e.g. $M=0.15$.

2.2.2.2 Dead time circuit

The purpose of the dead time circuit is to add a small dead time into the Class D output stage to ensure that both power transistors (one connected to the positive rail and

the other connected to the negative rail) do not turn on simultaneously. Figure 2-23 illustrates the output waveforms of the dead time block, where the dead time is the shaded area in the figure.

Figure 2-23 Output waveforms of a dead time circuit

There are several reported methods to realize the dead time circuit. One method [101] involves skewing the turn-on and turn-off times for each power transistor to realize a dead time. This is achieved by skewing the aspect ratio of the transistors in the driver stage with skew factor, s . Figure 2-24 depicts the schematic of the dead time circuit using this method where the width of each transistor is given, where t is the tapering ratio and a is the ratio of electron/hole mobility. It has been shown [101] that for a $0.5\mu\text{m}$ process with $s = 3$ and $t = 13$, a dead time of 40 ns can be achieved.

Figure 2-24 Schematic of a dead time circuit using the skewing method

Another reported method [105] to realize the dead time circuit involves creating an offset voltage in the input signal of the PWM modulator. The schematic of the dead time circuit using this method is shown in Figure 2-25(a) and the associated waveforms are shown in Figure 2-25(b). It is apparent from Figure 2-25(a) that due to the effects of the 4 resistors, small DC offsets are introduced at the two inputs, V_{in_H} and V_{in_L} , of the PWM modulator, and the DC offsets consequently result in a dead time in the Class D output stage. The dead time, t_{DT} , is:

$$t_{DT} = \frac{R_{DT_1}}{R_{DT_1} + R_{DT_2}} \frac{V_{DD}}{V_C} \frac{1}{2f_{sw}} \quad (2.30)$$

where V_C is the amplitude of the carrier.

Figure 2-25 (a) Schematic of a dead time circuit using the offset voltage method, and
(b) its waveforms

One drawback of the skewing method and the offset voltage method is that the short-circuit current may not be sufficiently reduced by the dead time. This is because there may be a delay in turning off the power transistor due to long charging (or discharging) time of the gate capacitance – if the delay is longer than the dead time, short circuit occurs. To circumvent this problem, a non-overlapping logic method was reported [106]. The simplified schematic of the dead time circuit using this method is depicted in Figure 2-26. It is apparent from Figure 2-26 that due to the feedback paths, the power transistors will not be simultaneously ‘on’. In other words, the short circuit current can be more completely reduced.

Figure 2-26 Schematic of a dead time circuit using the non-overlapping logic method

2.2.2.3 Over-current protection circuit

Figure 2-27 depicts the safe operating area [107-111] of a power transistor. This operating region is abbreviated as SOA, and is the region a power transistor has to operate within to avoid damage. Specifically, to avoid damage, the power transistor should operate within three limits. The first limit is the maximum drain-source voltage V_{MAX} , and is defined as the largest voltage before avalanche breakdown of the backgate diode. The second limit is the maximum current I_{MAX} , and is in general determined by electromigration in the metallization and bonding wires. The third limit is the maximum power dissipation P_{MAX} , and the value of P_{MAX} depends on the operating time of the power transistors – a shorter operating time results in higher P_{MAX} . As shown in Figure 2-27, the P_{MAX} for a short duration of 1ms is higher than the P_{MAX} for a relatively long duration of 10ms.

Amongst these limits, the most critical limit of the power transistor in a Class D output stage is often the I_{MAX} [108] – this is different from the power transistor in a linear amplifier whose critical limit is often P_{MAX} [112]. This is because the ‘on’ output impedance of the power transistor in the Class D output stage is very low and the power transistor usually reaches I_{MAX} before P_{MAX} . In view of this, a fairly precise Over-current protection circuit is required.

Figure 2-27 Safe Operating Area

An over-current protection circuit includes (i) two Over-current detection circuits, which sense the current in the high-side and low-side power transistors, and (ii) two comparators, which compare the currents in the power transistors against a reference current. The reference current should be just below I_{MAX} so that the power transistors can

be sized economically without compromising reliability. The design of the current detection circuit will now be reviewed.

Figure 2-28 shows an Over-current detection circuit that is commonly used in many discrete Class D (and Class AB) amplifiers. In this circuit, the current in the power transistors is measured by two series resistors, R_H and R_L . Once the current in the power transistor exceeds the predefined reference current, I_{Ref} (in this design, $I_{Ref} = (V_{Ref}/R_H) = (V_{Ref}/R_L)$), a turn-off signal $V_{overI_H} = '1'$ ($V_{overI_L} = '1'$) will be sent to the control logic to turn the power transistor off.

This design has two drawbacks. First, the presence of the two series resistors, R_H and R_L , results in reduced power-efficiency of the Class D amplifier. To minimize the reduction in the power-efficiency, the values of R_H and R_L should be substantially smaller than the on output impedance of the power transistors. In general audio applications with a 4Ω loudspeaker load, the on output impedance of the power transistor is $\sim 0.2\Omega$, and the values of R_H and R_L are recommended to be $< 50\text{m}\Omega$. Second, R_H and R_L are highly inaccurate due to process and temperature variations, as they are usually realized using the metal layer. In view of these drawbacks, this method is not recommended as an over-current detection circuit for Class D amplifiers realized monolithically.

Figure 2-28 Schematic of an over-current protection circuit using series resistors

Figure 2-29 shows another reported over-current protection circuit [108, 111] using a parallel detection method for monolithic Class D amplifiers. In this configuration, the current in the power transistors is measured by comparing their drain-to-source voltages to that of two (N -times) smaller replica transistors biased at reference current I_{Ref} . Note that this comparison is only valid if the corresponding power transistor is switched on. In other words, the high-side and low-side comparators should be active only when the corresponding power transistor is on, otherwise the outputs of the Over-current protection circuit, V_{overI_H} and V_{overI_L} , would be incorrect. In this design, the choice of N is a tradeoff between accuracy, device area and power consumption. Smaller N results in better accuracy (due to better matching between the current detection transistors and power transistors), but at the cost of larger device area and higher power consumption.

Figure 2-29 Schematic of an over-current protection circuit using the parallel method

Figure 2-30 shows a reported improved over-current protection circuit using the parallel method [108, 111]. There are two advantages in this design over that depicted in Figure 2-29. The first advantage is that the comparison of the current in the power transistors against the reference current is always valid. Conversely, note that for the design shown in Figure 2-29, the comparison is only valid when the corresponding power transistor is on. The second advantage is that a relatively small N can be used (such that the detection accuracy is high) without increasing the power consumption of the Class D amplifier.

Figure 2-30 Schematic of an improved over-current protection circuit using the parallel method

2.2.2.4 Over-temperature protection circuit

The design of over-temperature protection circuits [113-120] is well established and is commonly used in many applications, including linear audio amplifiers. Figure 2-31 depicts an over-temperature protection circuit comprising a reference circuit, a sensor circuit and a feedback circuit. The reference circuit generates a PTAT (proportional to absolute temperature) current, I_{PTAT} . M_{overT3} and M_{overT4} mirror the PTAT current flowing in M_{overT1} and M_{overT2} and provide a PTAT current to R_{overT1} and R_{overT2} . A PTAT voltage is hence generated at the base of Q_{overT1} .

Figure 2-31 Schematic of an over-temperature protection circuit

When the temperature is lower than the predetermined temperature, $V_{PTAT} = I_{PTAT} \cdot R_{OverT1}$ (note that M_{OverT6} is 'on') is lower than the threshold voltage of Q_{OverT1} , and Q_{OverT1} is hence 'off'. As a result, V_{be} is pulled to V_{DD} , and V_{OverT} is pulled to V_{DD} by means of inverters Inv 1 and Inv 2. Consequently, the logic control does not disturb or interface with the usual operation of the power transistors.

When the temperature just exceeds the predetermined temperature, both Q_{OverT1} and M_{OverT5} are in the active operating region, and V_{be} is just below the inherent threshold voltage of Inv 1 in the feedback circuit. The two inverters in the feedback circuit function as amplifiers. The output, V_{OverT} , of Inv 2 is $-V_{DD}$, and M_{OverT6} is turned 'off'.

V_{PTAT} subsequently increases from $I_{PTAT} \cdot R_{overT1}$ to $I_{PTAT} \cdot (R_{overT1} + R_{overT2})$, and the operating region of Q_{overT1} changes from the active region to the ohmic region. As a result, V_{overT} is pulled towards $-V_{DD}$. Consequently, the control logic turns off the power transistors to prevent the output stage from damage due to over-temperature.

2.2.3 Filterless Class D Amplifiers

As briefly discussed in Chapter 1, filterless Class D amplifiers [17-22] have recently received some acceptance due to the elimination of the bulky output filters. As mentioned earlier in Chapter 1, the primary reason for this acceptance is because the bulky output filter typically accounts for ~30% of the cost and ~75% of the PCB area in a Class D amplifier realization. Further, there have been claims [17], perhaps somewhat contentious, that the filterless approach has lower non-linearities, specifically the IMD.

Similar to traditional Class D amplifiers, the commonly used modulation techniques to realize a filterless Class D amplifier include (i) PWM [18-21], (ii) $\Sigma\Delta$ [22, 121], and (iii) self-oscillating [122]. The Filterless Class D amplifier based on Bang-Bang Control modulation technique remains unreported in the literature.

Regardless the modulation techniques, the architecture typically employed in filterless Class D amplifiers is the 3-state architecture¹ [123].

¹ Although it is not well known, the conventional (2-state) architecture may in fact be employed as a filterless Class D amplifier. At this juncture, it is unknown that if certain conditions are satisfied, the power-efficiency of the conventional architecture can be comparable to the 3-state architecture – this will be discussed in Chapter 5 later.

Figure 2-32 depicts the block diagram of a typical filterless Class D amplifier (whose supply rails are V_{DD} and $-V_{DD}$), where V_{out1} and V_{out2} are the two outputs (and are in phase) of the BTL output stage and I_{out} is the current in the loudspeaker.

Figure 2-32 Block Diagram of a filterless Class D amplifier

Figure 2-33 depicts the output waveforms V_{out1} and V_{out2} of the filterless Class D amplifier for the zero-input condition. It is apparent that the filterless Class D amplifier is attractive at this zero-input condition because the differential output voltage and current are both zero, hence highly power-efficient.

Figure 2-33 Waveforms of the filterless Class D amplifier at zero-input

Figure 2-34 depicts the output waveforms for a non-zero sinusoidal input. Notice that the output here is 3-state (vis-à-vis 2 state in the conventional Class D amplifier that requires an output lowpass filter), and this explains the reason for the term ‘3-state’ given to this Class D amplifier architecture. It is of interest to note that although the switching frequency at the output stages (V_{out1} and V_{out2}) here is the same as the conventional Class D amplifier, and the switching at the load here is two times faster. Nonetheless, this increased switching frequency has no effect on the power-efficiency as the switching frequency at the output stage is not increased.

Figure 2-34 Waveforms of the filterless Class D amplifier with a sinusoidal input

In filterless Class D amplifiers, an inductive loudspeaker is required in place of the output lowpass filter to attenuate the high frequency carrier current (and related components), hence the need for a higher power rated loudspeaker to accommodate the additional power dissipation. The additional power dissipation due to the attenuation of high frequency signals may cause two undesirable effects: (i) reduced power-efficiency, and (ii) damage to the loudspeaker if the total power dissipation exceeds the power rating of the loudspeaker.

Despite the maturity of filterless Class D amplifiers, much of the design considerations remain unreported in the literature, but empirical guidelines do exist. For example, the abovementioned additional power dissipation in the loudspeaker and the required value of the inductance (reactance) of the loudspeaker are empirically suggested by several manufactures. Further, the mechanisms of power dissipation in the

loudspeaker and the parameters available to vary/compromise to meet given design specifications are unreported. In Chapter 5, some of the ambiguities pertaining to filterless Class D amplifiers will be addressed, including the power dissipation, power-efficiency, the required value of the inductance in the loudspeaker, etc.

2.3 Conclusions

In this chapter, audio amplifiers, including both classical linear amplifiers and high power-efficient audio amplifiers, have been reviewed, and their power-efficiencies compared. It has been shown that Class D amplifiers feature the highest power-efficiency. In view of this, the emphasis of the literature review has been on Class D amplifiers, including commonly used modulation techniques, the output stage design and filterless Class D amplifiers. It has been shown that despite the wealth of knowledge and know-how on analog Class D amplifiers, there are a number of ambiguities/unknowns. Some of these will be addressed in Chapters 3-5 in this thesis.

Chapter 3 PSRR and PS-IMD of PWM Class D Amplifiers

3.1 Introduction

A large portion of this chapter has been published in the IEEE Transactions on Circuits and Systems II [28], and has been presented at the IEEE International Symposium on Circuits and Systems 2006 [33].

Although the PSRR of Class D amplifiers is largely unknown in the literature, several researchers within the Class D amplifier community have remarked that PSRR can be one of the major drawbacks of Class D amplifiers [71]. The mechanisms thereof are also not well understood with little, if any, reported literature. In practice, PSRR is an important consideration because the Class D amplifier typically operates within a large system and power rails may be noisy. Interestingly, it is also not well recognized that the power supply noise can intermodulate with the input signal, manifesting into PS-IMD, and that the PS-IMD can be significantly larger than the output distortion component at supply noise frequency. Further, current design techniques to improve PSRR and PS-IMD are largely empirical. For instance, a Class D amplifier with an increased number of feedback loops usually yields a design with improved PSRR but at the cost of increased hardware. However, the designer is generally unable to analytically determine/predict the improvement.

As mentioned in Chapter 1 and Chapter 2, of the various modulation techniques, PWM is arguably most prevalent largely because of its hardware simplicity and low quiescent current (due to its low switching frequency). In view of this, the analog PWM amplifier is the Class D amplifier of interest in this chapter.

In this chapter, analytical expressions for PSRR and PS-IMD of three PWM amplifiers are derived – the simple open-loop PWM amplifier, the prevalent single-feedback PWM amplifier and the higher fidelity double-feedback PWM amplifier. These expressions are particularly significant as they depict the primary parameters that affect PSRR and PS-IMD, and provide insight to a PWM amplifier designer on how various parameters may be varied and/or compromised to meet a given set of specifications. A simple design technique, at very low hardware cost, to improve PSRR and PS-IMD is proposed, and its efficacy by its application to the single-feedback PWM amplifier is demonstrated. The single-feedback PWM amplifier using the proposed technique is denoted as ‘improved single-feedback PWM amplifier’. The analytical expressions for PSRR and PS-IMD of the improved single-feedback PWM amplifier are derived. A comparison of the single-feedback PWM amplifier, the double-feedback PWM amplifier and the improved single-feedback PWM amplifier shows that the improved single-feedback PWM amplifier exhibits an ~26dB PSRR and PS-IMD improvement over the single-feedback PWM amplifier. The double-feedback PWM amplifier, however, does exhibit ~20dB better PSRR and PS-IMD in the low frequencies compared to the improved single-feedback PWM amplifier, but at the expense of more complex hardware and more I/O pins. The analytical expressions are verified by HSPICE simulations and by

measurements on a prototype PWM IC and on other PWM amplifiers realized using discrete components.

This chapter is organized in the following manner. In Section 3.2, the PSRR and PS-IMD of the open-loop, single-feedback and double-feedback PWM amplifiers are analyzed. In Section 3.3, the proposed design technique to improve PSRR and PS-IMD of PWM is presented, and the different Class D amplifiers are compared. In Section 3.4, the derived theoretical equations are verified against HSPICE simulations and hardware measurements on a prototype IC and on other Class D amplifiers constructed using discrete components. Finally, conclusions are drawn in Section 3.5.

3.2 PSRR and PS-IMD of PWM Class D Amplifiers

3.2.1 PSRR and PS-IMD of Open-Loop PWM Class D Amplifiers

In this section, the open-loop PWM amplifier with supply noise is modeled and its PSRR and PS-IMD are derived. These analyses also serve as a preamble for the analysis of the single-feedback, double-feedback and the improved single-feedback PWM amplifiers in Sections 3.2.2 and 3.3.

Figure 3-1(a) and Figure 3-1(b) respectively depict an open-loop PWM amplifier and its linear model, where v_n is the supply noise, G_{PWM} the gain of the PWM modulator and N_D the supply noise at the output.

$$G_{PWM} = \frac{V_{DD}}{V_C} \tag{3.1}$$

$$v_n = V_{DD} V_N \cos(\omega_n t) \tag{3.2}$$

where V_C is the magnitude of the triangular-wave carrier,
 V_N is the normalized magnitude of the supply noise, and
 ω_n is the supply noise frequency in rad/s.

Figure 3-1 (a) Schematic of an open-loop PWM amplifier, and (b) its linear model

On the basis of double-Fourier expression [68] of an ideal (with no supply noise) PWM signal, the PWM signal, V_{out_OL} , with supply noise can be easily derived:

$$\begin{aligned} \frac{V_{out_OL}}{V_{DD}} &= M \cos(\omega_{in}t) + N_D \\ &+ 4 \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(2m\omega_{sw}t + 2n\omega_{in}t) \sin\left(\frac{m+n}{2}\pi\right) \\ &+ 4 \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(2m\omega_{sw}t + 2n\omega_{in}t \pm \omega_n t) \sin\left(\frac{m+n}{2}\pi\right) \end{aligned} \quad (3.3)$$

where

$$N_D = \frac{V_N}{2} \cos(\omega_n t) + \frac{MV_N}{4} \cos(\omega_{in}t \pm \omega_n t) \quad (3.4)$$

where J_n is the Bessel function of the first kind with order n ,

ω_{sw} is the switching (carrier) frequency in rad/s, and

ω_{in} is the input frequency in rad/s.

Eqn. (3.3) can be interpreted as follows. The first term is the amplified replica of the input signal, the desired output signal. The second term is the supply noise components at output and is expressed in eqn. (3.4). The last two terms are harmonics of the carrier, and intermodulation products between the fundamental and harmonic components of the input signal, the carrier and the supply noise and can be either negligible or effectively removed by the lowpass filter of the load.

Based on eqn. (3.4), the PSRR and PS-IMD of an open-loop PWM Class D amplifier can be derived:

$$\text{PSRR}_{\text{OL}} = 20 \log \left(\frac{V_N}{V_N/2} \right) = 6\text{dB} \quad (3.5)$$

$$\begin{aligned} \text{PS-IMD}_{\text{OL}} &= 20 \log \left(\frac{1}{V_N} \sqrt{\left(\frac{MV_N}{4} \right)^2 + \left(\frac{MV_N}{4} \right)^2} \right) \text{dB} \\ &= (-9 + 20 \log M) \text{dB} \end{aligned} \quad (3.6)$$

Eqns. (3.5) and (3.6) are interpreted as follows. The PSRR of an open-loop PWM amplifier is undesirably low, typically 6dB, and is independent of the input signal. The PS-IMD, on the other hand, is dependent on the magnitude of the input signal and in the worst-case where $M=1$, the PS-IMD is undesirably high, PS-IMD=-9dB. Note that both the PSRR and the PS-IMD of an open-loop PWM amplifier are independent of the switching frequency – it will be later shown that this is not the case for single- and double-feedback PWM amplifiers where a high switching frequency is required for high PSRR and low PS-IMD. This simple analysis is insightful for Class D amplifier designers to appreciate the limitations of open-loop PWM amplifiers for high fidelity applications and that there is virtually no parameter available, save the magnitude of the input signal for PS-IMD, to improve PSRR and PS-IMD.

3.2.2 PSRR and PS-IMD of Single- and Double-Feedback PWM Class D Amplifiers

The PSRR and PS-IMD of the single- and double-feedback PWM Class D amplifiers will now be investigated. Note that in this investigation, only the PSRR and PS-IMD contributed by the output stage are considered. This is primarily because, the power supply to the op-amp and comparator are obtained from a regulated lower supply voltage (e.g. 5V), and that their PSRR is typically very high.

3.2.2.1 PSRR and PS-IMD of the single-feedback PWM amplifiers

Figure 3-2(a) depicts a common single-feedback PWM amplifier, comprising an open-loop PWM amplifier, an input and feedback resistor, R_1 and R_{fb1} , respectively, a 2nd-order integrator and the load.

Figure 3-2 (a) Schematic of a single-feedback PWM amplifier, and (b) its linear model

By straightforward linear control theory, the single-feedback PWM amplifier is modeled in Figure 3-2(b) where G_1 is the transfer function from the single-feedback PWM amplifier input to the integrator inverting input, G_{int1} is the gain of the integrator, and H_1 is the feedback factor. By inspection, the noise transfer function is:

$$\frac{V_{out_1FB}}{N_D} = \frac{1}{1 + |G_{int1}|G_{PWM}H_1} \quad (3.7)$$

where

$$G_{int1}(\omega) = \frac{-A_{op}(1 + 2R_2C\omega j)}{1 + (2R_2 + R_1 \parallel R_{fb1})C\omega j - (A_{op1} + 1)(R_1 \parallel R_{fb1})R_2C^2\omega^2} \quad (3.8)$$

$$H_1 = \frac{R_1}{R_1 + R_{fb1}} \quad (3.9)$$

where A_{op1} is the open-loop gain of the op-amp used in the integrator.

From eqns. (3.7) – (3.9), the expressions for PSRR and PS-IMD for the single-feedback PWM amplifier are:

$$\text{PSRR}_{1\text{FB}} = 20 \log \left(\frac{1 + LG_{1\text{FB}}(\omega_n)}{0.5} \right) \text{dB} \quad (3.10)$$

$$\text{PS-IMD}_{1\text{FB}} = 20 \log \sqrt{\left(\frac{M/4}{1 + LG_{1\text{FB}}(\omega_{in} + \omega_n)} \right)^2 + \left(\frac{M/4}{1 + LG_{1\text{FB}}(\omega_{in} - \omega_n)} \right)^2} \text{dB} \quad (3.11)$$

where

$$LG_{1\text{FB}}(\omega) = |G_{int1}(\omega)|G_{PWM}H_1 \quad (3.12)$$

The $\text{PSRR}_{1\text{FB}}$ and $\text{PS-IMD}_{1\text{FB}}$ are interpreted as follows:

- (i) $\text{PSRR}_{1\text{FB}}$ is independent of the input signal, whilst $\text{PS-IMD}_{1\text{FB}}$ increases as the magnitude of the input signal increases. Both the PSRR and PS-IMD are, as expected, largely determined by the loop-gain, $LG_{1\text{FB}}$. Specifically, the higher the $LG_{1\text{FB}}$, the higher is the PSRR and the lower the PS-IMD. It is apparent from eqn. (3.12) that to obtain a high $LG_{1\text{FB}}$, it is imperative that G_{PWM} , H_1 and G_{int1} are high, and the associated primary parameters for high G_{int1} are (high) A_{op1} and (high) f_{sw} (hence a high G_{int1} can be used).
- (ii) The PS-IMD components in the single-feedback PWM amplifier may be larger than the distortion component at f_n due to the fact that $LG_{1\text{FB}}$ at $f_{in} \pm f_n$ can be significantly smaller than $LG_{1\text{FB}}$ at f_n . For example, for $f_n = 100\text{Hz}$, $f_{in} = 15\text{kHz}$ and $M = 0.2$, the PSRR is rather unexpecting better than the PS-IMD, specifically, $\text{PSRR} = 47\text{dB}$ while $\text{PS-IMD} = -20\text{dB}$. In other words, the PS-IMD is about 27dB

larger than the distortion components at f_n . This example will be verified in Section 3.4 later.

3.2.2.2 PSRR and PS-IMD of the double-feedback PWM amplifiers

Figure 3-3 depicts a double-feedback PWM amplifier, comprising a single-feedback PWM amplifier (Figure 3-2(a)), an input and feedback resistor R_3 and R_{fb2} respectively, a 2^{nd} -order integrator, a unity-gain inverting amplifier and the load. The inverting amplifier ensures an overall negative feedback, and can be eliminated if the inner-loop (the single-feedback PWM amplifier) is non-inverting.

Figure 3-3 Schematic of a double-feedback PWM amplifier

As before, the PSRR and PS-IMD of the double-feedback PWM amplifier can be similarly derived as:

$$\text{PSRR}_{2\text{FB}} = 20 \log \left(\frac{1 + LG_{2\text{FB}}(\omega_n)}{0.5} \right) \text{dB} \quad (3.13)$$

$$\text{PS-IMD}_{2\text{FB}} = 20 \log \sqrt{\left(\frac{M/4}{1 + LG_{2\text{FB}}(\omega_{\text{in}} + \omega_n)}\right)^2 + \left(\frac{M/4}{1 + LG_{2\text{FB}}(\omega_{\text{in}} - \omega_n)}\right)^2} \text{ dB} \quad (3.14)$$

where $LG_{2\text{FB}}$ is the loop gain of the double-feedback PWM amplifier, that is:

$$LG_{2\text{FB}}(\omega) = |G_{\text{int}2}(\omega)| |G_{\text{int}1}(\omega)| G_{\text{PWM}} H_2 G_1 + LG_{1\text{FB}}(\omega) \quad (3.15)$$

$$G_{\text{int}2}(\omega) = \frac{-A_{\text{op}}(1 + 2R_4 C \omega j)}{1 + (2R_4 + R_3 \parallel R_{fb2}) C \omega j - (A_{\text{op}2} + 1)(R_3 \parallel R_{fb2}) R_3 C^2 \omega^2} \quad (3.16)$$

$$H_2 = \frac{R_3}{R_3 + R_{fb2}} \quad (3.17)$$

where $G_{\text{int}2}$ is the gain of the outer-loop integrator,

H_2 is the outer-loop feedback factor, and

$A_{\text{op}2}$ is the open-loop gain of the op-amp used in the integrator in the outer feedback loop.

$\text{PSRR}_{2\text{FB}}$ and $\text{PS-IMD}_{2\text{FB}}$ can be interpreted as follows:

- (i) Similar to the single-feedback PWM amplifier, $\text{PSRR}_{2\text{FB}}$ and $\text{PS-IMD}_{2\text{FB}}$ are largely determined by the loop-gain $LG_{2\text{FB}}$ – the higher the $LG_{2\text{FB}}$, the better is the $\text{PSRR}_{2\text{FB}}$ and the $\text{PS-IMD}_{2\text{FB}}$. Hence, it is desirable that $G_{\text{int}2}$, G_{PWM} and H_2 be high. As before, a high f_{sw} and high op-amp open-loop gain are recommended for high $G_{\text{int}2}$.

- (ii) A comparison between LG_{1FB} (eqn. (3.12)) and LG_{2FB} (eqn. (3.15)) shows that LG_{2FB} is significantly improved compared to LG_{1FB} . This significant improvement in loop-gain will consequently result in significant improvements in both PSRR and PS-IMD.
- (iii) In addition to (ii), since both G_{int1} and G_{int2} reduce as frequency increases, the loop-gain improvement also reduces as frequency increases. This reduction in the loop-gain improvement will consequently reduce the improvement in both PSRR and PS-IMD. For example, the PSRR and PS-IMD improvements is respectively reduced from ~35dB at 2kHz to ~17dB at 15kHz (see Section 3.4 later).

In summary, the double-feedback PWM amplifier design has worthy advantages over the single-feedback PWM amplifier design in both PSRR and PS-IMD but at the cost of increased hardware (larger IC area and larger form factor due to additional I/O pins and external passive components).

3.3 Technique to Improve PSRR and PS-IMD

In this section, a simple low hardware overhead technique to improve PSRR and PS-IMD is proposed. This technique involves replacing the conventional carrier generator with a modified generator depicted in Figure 3-4. In a conventional generator, the non-inverting input terminal of the comparator is tied to signal ground and its hysteresis is highly independent of the supply noise [124]. The hysteresis of the comparator used in the improved carrier generator, on the other hand, depends on the supply voltage and the ratio of R_{C1} and R_{C2} .

Figure 3-4 Schematic of the proposed carrier generator

The improved carrier generator introduces supply noise into the carrier such that the distortion components introduced by the supply noise are largely cancelled by the distortion components in the carrier. Figure 3-5 depicts the waveforms of the ideal modified carrier generator, where $V_{h1} = (V_{DD} + v_n)R_{C2}/(R_{C1} + R_{C2})$ and $V_{h2} = -V_{DD}R_{C2}/(R_{C1} + R_{C2})$ are the respective defined ideal upper and lower limits of the hysteresis, and V_{h3} and V_{h4} are the actual upper and lower practical limits of the hysteresis range. Note that the difference between the ideal and actual hysteresis is mainly due to the propagation delay, t_D , of the comparator. At time t_1 , when the carrier V_C is just above V_{h1} , the comparator output V_P ideally changes from $V_{DD} + v_n$ to $-V_{DD}$. However, in a practical case due to t_D , V_P instead changes at $t_1 + t_D$. Between t_1 and $t_1 + t_D$, the output V_C continues to rise, and the upper limit of the hysteresis is hence increased. Similarly, due to t_D , the lower hysteresis limit is lowered.

Figure 3-5 Waveforms of the proposed carrier generator

3.3.1.1 Open-loop PWM amplifier embodying the improved carrier generator

The output of an open-loop PWM amplifier (depicted in Figure 3-1(a)), V_{OLi} embodying the improved carrier generator will now be derived. Based on Figure 3-4 and Figure 3-5, the expressions for V_{h3} and V_{h4} are:

$$V_{h3} = \frac{V_{DD}}{G_{PWM}} + \frac{4V_{DD}t_D}{G_{PWM}T} + \frac{v_n}{G_{PWM}} \quad (3.18)$$

$$V_{h4} = -\left(\frac{V_{DD}}{G_{PWM}} + \frac{4V_{DD}t_D}{G_{PWM}T}\right) \quad (3.19)$$

where T is one switching period when $V_n=0$ and $t_D=0$, T and G_{PWM} can be expressed as:

$$G_{PWM} = \frac{V_{DD}}{G_{PWM}} + \frac{4V_{DD}t_D}{G_{PWM}T} + \frac{v_n}{G_{PWM}} \quad (3.20)$$

$$T = \frac{4C_C V_{DD}}{IG_{PWM}} \quad (3.21)$$

Based on Figure 3-4, Figure 3-5, eqns. (3.18) and (3.19), the ‘on’ and ‘off’ periods, t_{on} and t_{off} , of an open-loop PWM amplifier can be derived.

$$t_{on} = \frac{T}{2} + 2t_D + \frac{V_{in}G_{PWM}T}{2V_{DD}} \quad (3.22)$$

$$t_{off} = \frac{T}{2} + 2t_D + \frac{v_n T}{2V_{DD}} - \frac{V_{in}G_{PWM}T}{2V_{DD}} \quad (3.23)$$

where t_{on} is the period when $V_{out} = V_{DD} + v_n$ and t_{off} is the period when $V_{out} = -V_{DD}$. The output signal, V_{OLi} , can be derived by taking the average value over one carrier period.

$$\begin{aligned} V_{OLi} &= \frac{t_{on}(V_{DD} + v_n) - t_{off}V_{DD}}{t_{on} + t_{off}} \\ &= MV_{DD} \cos(\omega_{in}t) + \frac{4t_D}{T} \frac{V_N}{2} \cos(\omega_n t) + \frac{4t_D}{T} \frac{MV_N}{4} \cos(\omega_{in}t \pm \omega_n t) \end{aligned} \quad (3.24)$$

Note that the first term in eqn. (3.24) is the replica of the input signal, and the last two terms are the output distortion due to the supply noise in an open-loop. A comparison of the last two terms in eqn. (3.24) and eqn. (3.4) shows that by means of the improved carrier generator, the major distortion components in the open-loop PWM amplifier are significantly reduced from N_D to $(4t_D/T)N_D$ and that the smaller the t_D , the lower is the distortion. Note that in an ideal case where $t_D = 0$, the distortion components are completely eliminated.

3.3.1.2 Single-feedback PWM amplifier embodying the improved carrier generator

Consider now the embodiment of the improved carrier generator in the single-feedback PWM amplifier. Based on eqn. (3.24) and the linear model, the PSRR and PS-

IMD of the improved single-feedback PWM amplifier, denoted as $\text{PSRR}_{\text{1FBi}}$ and $\text{PS-IMD}_{\text{1FBi}}$, are:

$$\text{PSRR}_{\text{1FBi}} = \left(20 \log \frac{T}{4t_D} + 20 \log \left(\frac{1 + LG_{\text{1FB}}(\omega_n)}{0.5} \right) \right) \text{dB} \quad (3.25)$$

$$\text{PS-IMD}_{\text{1FBi}} = \left(20 \log \frac{4t_D}{T} + 20 \log \sqrt{\left(\frac{M/4}{1 + LG_{\text{1FB}}(\omega_{in} + \omega_n)} \right)^2 + \left(\frac{M/4}{1 + LG_{\text{1FB}}(\omega_{in} - \omega_n)} \right)^2} \right) \text{dB} \quad (3.26)$$

$\text{PSRR}_{\text{1FBi}}$ and $\text{PS-IMD}_{\text{1FBi}}$ can be interpreted as follows:

- (i) Similar to the usual single-feedback PWM amplifier and double-feedback PWM amplifier, $\text{PSRR}_{\text{1FBi}}$ and $\text{PS-IMD}_{\text{1FBi}}$ are largely affected by the loop-gain LG_{1FB} – the higher the LG_{1FB} , the higher is the $\text{PSRR}_{\text{1FBi}}$ and the lower is the $\text{PS-IMD}_{\text{1FBi}}$.
- (ii) Further to (i), compared to the single-feedback PWM amplifier, $\text{PSRR}_{\text{1FBi}}$ and $\text{PS-IMD}_{\text{1FBi}}$ are improved by $20 \log(T/4t_D) \text{dB}$. This improvement is usually significant as t_D (typically ranging from 10ns to 100ns) is much smaller than T (typically ranging from 1μs to 10μs). For example, if $t_D = 80 \text{ns}$ and $T = 6.6 \mu\text{s}$ ($f_{\text{sw}} = 150 \text{kHz}$), the PSRR and PS-IMD improvement is 26dB regardless of the supply noise frequency, and this will be verified in Section 3.4.

Obviously, a shorter t_D and/or lower f_{sw} (hence longer T) results in higher PSRR and PS-IMD.

- (iii) Furthermore, a comparison of improved single-feedback PWM amplifier and double-feedback PWM amplifier shows that improved single-feedback PWM

amplifier is likely to feature better PSRR and PS-IMD in the higher frequency range ($>2\text{kHz}$) but worse PSRR and PS-IMD in the lower frequency range (e.g. 100Hz). This is because, compared to the single-feedback PWM amplifier, the improvement of the improved single-feedback PWM amplifier is independent of frequency. In contrast, the PSRR and PS-IMD improvement of the double-feedback PWM amplifier reduces as frequency increases (see Section 3.4 later).

3.4 Results and Verification

In this section, the analytical expressions for PSRR and PS-IMD (eqns. (3.10), (3.11), (3.13), (3.14), (3.25) and (3.26)) are verified by HSPICE simulations and measurements on a prototype PWM amplifier IC and on other PWM amplifiers constructed using discrete components. The microphotograph of the prototype IC embodying a single-feedback PWM amplifier is shown in Figure 3-6. The double-feedback PWM amplifier is constructed by adding an external loop to the single-feedback PWM amplifier IC using discrete components and the improved single-feedback PWM amplifier is similarly constructed using discrete components. The circuit parameters of these PWM amplifiers are tabulated in Table 3-I.

Figure 3-6 Microphotograph of the single-feedback PWM amplifier

Table 3-I Parameters of the single-feedback, double-feedback and improved single-feedback PWM amplifiers

Parameter	Value
Supply Voltage (V_{DD})	10 V
Switching Frequency (f_{sw})	150 kHz
Speaker Impedance	4 Ω
$G_{PWM}, A_{op1}, A_{op2}$	5, 56dB, 86dB
$C, R_1, R_2, R_3, R_4, R_{fb1}, R_{fb2}$ (all external)	1nF, 3k Ω , 20k Ω , 3k Ω , 68k Ω , 90k Ω , 90k Ω
t_D	80ns

Figure 3-7 depicts the PSRR against f_n obtained analytically (eqns. (3.10), (3.13), and (3.25)), by HSPICE simulations and by practical measurements for the three PWM amplifiers.

(a)

(b)

Figure 3-7 PSRR of the single-feedback, double-feedback and improved single-feedback PWM amplifiers

The following observations are made based on Figure 3-7.

- (i) The derived analytical expressions agree well with the HSPICE simulations and practical measurements for all the three designs, hence verifying eqns. (3.10), (3.13), and (3.25).
- (ii) The PSRR of all the PWM amplifiers reduces as frequency increases. This is as expected as the loop-gain reduces with frequency.
- (iii) The PSRR of the double-feedback PWM amplifier is significantly better than the single-feedback PWM amplifier due to the additional feedback loop. The degree of improvement decreases as the supply noise frequency increases, e.g. the PSRR improvement reduces from ~45dB @ 100Hz to ~17dB @ 15kHz. This is predicted analytically and is because the improvement of the loop-gain reduces as the frequency increases.
- (iv) The PSRR of the improved single-feedback PWM amplifier is significantly better than the single-feedback PWM amplifier. Unlike the double-feedback PWM amplifier whose PSRR improvement reduces as frequency increases, the PSRR improvement of the improved single-feedback PWM amplifier over the single-feedback PWM amplifier is nearly frequency independent. For example, the PSRR improvement is ~26dB through out the audio frequency range.
- (v) Further to (iii) and (iv), a comparison between the double-feedback PWM amplifier and improved single-feedback PWM amplifier shows that the double-feedback PWM amplifier has worthy advantages in the low frequency range

(<2kHz) as the $PSRR_{2FB}$ is substantially better than the $PSRR_{1FBi}$. However, in the higher frequency range (2kHz to 20kHz), the $PSRR_{1FBi}$ becomes better than $PSRR_{2FB}$. In view of this, if PSRR in the lower frequency range is major parameter of concern, the double-feedback PWM amplifier should be a better choice. Otherwise, the improved single-feedback PWM amplifier is the better choice as it features a better PSRR in the high frequency range and much simpler design compared to the double-feedback PWM amplifier. Furthermore, if necessary, an additional feedback-loop can be added to the improved single-feedback PWM amplifier to further improve PSRR but at the cost of the increased hardware.

(b)

(c)

Figure 3-8 PS-IMD of the (a) single-feedback, (b) double-feedback, and the (c) improved single-feedback PWM amplifiers

Figure 3-8(a) – Figure 3-8 (c) respectively summarize the PS-IMD of the single-feedback, double-feedback and improved single-feedback PWM amplifiers obtained analytically (eqns. (3.11), (3.14) and (3.26)), by HSPICE simulations and by measurements. The noise frequency is $f_n=100\text{Hz}$, and the input frequency is $f_{in}=2\text{kHz}$ in one case and $f_{in}=15\text{kHz}$ in the second case. Note that the maximum $M=0.6$ is due to the parameters given in Table 3-I. The following observations are made based on Figure 3-8.

- (i) The derived analytical expression agrees well with the HSPICE simulations and practical measurements for all three designs, hence verifying eqns. (3.11), (3.14) and (3.26).
- (ii) The PS-IMD, as expected, degrades for higher modulation index. The PS-IMD also degrades for higher input frequencies, and this is due to the higher intermodulation frequencies where the loop-gain is lower.
- (iii) A comparison between Figure 3-8(a) and Figure 3-8(b) shows that, due to the additional feedback, the improvement of the PS-IMD of the double-feedback PWM amplifier over the single-feedback PWM amplifier is a significant $\sim 35\text{dB}$ and $\sim 17\text{dB}$ for $f_{in}=2\text{kHz}$ and $f_{in}=15\text{kHz}$ respectively. As expected, the improvement reduces as frequency increases.
- (iv) A comparison between Figure 3-8(a) and Figure 3-8(c) shows that, compared to the single-feedback PWM amplifier, the PS-IMD of the improved single-feedback PWM amplifier is significantly improved by $\sim 26\text{dB}$ for $f_{in}=2\text{kHz}$ and $f_{in}=15\text{kHz}$. Note that unlike the case of double-feedback PWM amplifier, the

improvement of the improved single-feedback PWM amplifier is independent of the frequency.

- (v) A comparison between Figure 3-8(b) and Figure 3-8(c) shows that, for $f_{in}=2\text{kHz}$, $\text{PS-IMD}_{2\text{FB}}$ is $\sim 10\text{dB}$ better than the $\text{PS-IMD}_{1\text{FBi}}$. However, for $f_{in}=2\text{kHz}$, $\text{PS-IMD}_{2\text{FB}}$ is $\sim 10\text{dB}$ worse than $\text{PS-IMD}_{1\text{FBi}}$. This is because the improvement of $LG_{2\text{FB}}$ over $LG_{1\text{FB}}$ reduces with frequency while the improvement of $\text{PS-IMD}_{1\text{FBi}}$ over $\text{PS-IMD}_{1\text{FB}}$ is frequency independent as t_D is nearly frequency independent (in the audio frequency range). Similar to the case of PSRR, if the low frequency PS-IMD is of primary interest, the double-feedback PWM amplifier would be the better choice; otherwise the improved single-feedback PWM amplifier would be preferred.
- (vi) From Figure 3-7(a) and Figure 3-8(a), for the single-feedback PWM amplifier when $f_n=100\text{Hz}$ $f_{in}=15\text{kHz}$ and $M=0.2$, note that the PS-IMD is substantially larger than the distortion component at f_n , specifically the $\text{PS-IMD}=-20\text{dB}$ while $\text{PSRR}=47\text{dB}$. As delineated earlier, this observation is not well known but can be easily explained from eqns. (3.10) and (3.11) as delineated earlier. Specifically, this is because $LG_{1\text{FB}}$ at f_n is much larger than $LG_{1\text{FB}}$ at $f_{in} \pm f_n$. For the same reason, a similar observation can be made for the double-feedback PWM amplifier and the improved single-feedback PWM amplifier.

3.5 Conclusions

By means of the linear model, the PSRR and PS-IMD of the single-feedback, double-feedback and improved single-feedback PWM amplifiers have been analyzed and analytical expressions derived. The proposed improved single-feedback PWM amplifier embodied an improved carrier generator that incorporated a simple design technique with very low hardware overheads. It has been shown that the proposed design technique has worthy advantages to improve PSRR and PS-IMD. The derived analytical expressions and the efficacy of the proposed technique have been verified by means of HSPICE simulations and on the basis of measurements on a prototype PWM amplifier IC and other PWM amplifiers realized using discrete components. The performance of the three PWM amplifiers has also been compared.

Chapter 4 THD, PSRR and PS-IMD of Bang-Bang Control Class D Amplifiers

4.1 Introduction

A large portion of this chapter has been published in the IEEE Transactions on Circuits and Systems I [27] and in the IEEE Transactions on Circuits and Systems II [5], and has been presented at the IEEE International Symposium on Circuits and Systems 2007 [32].

In power-critical applications, such as hearing instruments, high power-efficiency is imperative because of the limited energy capacity of the remote power supply, usually small cell-batteries. In view of the need for micropower operating conditions, Class D amplifiers employed in hearing instruments typically embody simple hardware, for example the single-feedback PWM amplifier [72] as opposed to multiple-feedback [75] or Sigma-Delta amplifiers; For completeness, it is interesting to note that in early designs, open-loop PWM Class D amplifiers [69] were employed; but as this simple architecture suffers from severe distortions (for example $\text{THD} \approx 5\%$), it is largely abandoned today.

In this chapter, the adoption of established Bang-Bang amplifiers [16, 64, 125] (as opposed to the prevalent single-feedback PWM amplifier) for power-critical hearing instruments is proposed; interestingly, Bang-Bang amplifiers have hitherto been applied

only to mid- to high-power audio applications [64]. The adoption of Bang-Bang amplifiers is due to the advantage of their simpler hardware and resultant lower power dissipation, and hence the highly desirable higher power-efficiency, η (see Figure 4-3 later). In this chapter, the power-efficiency of a Bang-Bang amplifier is compared against that of the single-feedback PWM amplifier.

In this chapter, the THD, PSRR and PS-IMD of a common Bang-Bang amplifier (see Figure 4-1 later) are investigated. For sake of brevity, the other common Bang-Bang amplifier (see Figure 4 in [5]) is not investigated here but can be similarly analyzed. In this investigation, analytical expressions for THD, PSRR and PS-IMD of the Bang-Bang amplifier are derived, and the effects of the important circuit parameters on the THD, PSRR and PS-IMD of the Bang-Bang amplifier are clearly depicted and delineated. It is shown that the THD is nearly independent of the input frequency, that the PSRR reduces as the magnitude of the input signal increases, and that the PS-IMD is independent of the supply noise and the input frequencies. These relationships are somewhat unexpected because in the competing PWM amplifier, the THD increases with the input frequency, the PSRR is independent of the magnitude of the input signal, and the PS-IMD increases with the supply noise and the input frequencies.

The investigations and analyses herein are significant because they provide insight to a Bang-Bang amplifier designer and how various parameters may be varied and/or compromised to meet a given set of specifications. The expressions are verified by comparing them against HSPICE simulations and on the basis of experimental measurements on prototype Class D amplifiers embodying Class D output stage ICs. For completeness, note that the analyses herein are applicable to Bang-Bang amplifiers

designed for power-critical low-voltage hearing instrument applications (whose bandwidth, BW, is typically 4kHz to 8kHz and load resistance, R_L , is $>200\Omega$ for subminiature Completely-In-Canal hearing instruments) and for general audio applications (whose BW=20kHz and $R_L=4\Omega$ to 32Ω) as they embody the same design architecture.

This chapter is organized in the following manner. In Section 4.2, the power-efficiency of the Bang-Bang amplifier and the PWM amplifier are compared. In Section 4.3, the analytical expression for the THD of the Bang-Bang amplifier is derived and the pertinent parameters that affect the THD investigated. In Section 4.4, the analytical expression for the PSRR and PS-IMD of the Bang-Bang amplifier are derived and the pertinent parameters that affect the PSRR and PS-IMD investigated. In Section 4.5, the derived expressions are verified against HSPICE simulations and measurements on prototype Bang-Bang amplifiers embodying Class D output Stage ICs. Finally, conclusions are drawn in Section 4.6.

4.2 A Comparison of Power-Efficiency of Bang-Bang Control and PWM Class D Amplifiers

In this section, the power dissipation and power-efficiency of the Bang-Bang amplifier and PWM amplifier are compared to depict the power dissipation advantage of the former for power-critical low-voltage applications, including hearing instruments.

The mechanisms of power dissipation in Class D amplifiers are well known and are (i) P_O , the power dissipated by the load, R_L , (ii) P_D , the power dissipated by the output

stage [98], and (iii) P_Q , the operating power of the remaining functional blocks within the Class D amplifier. As power-efficiency $\eta = P_O / (P_O + P_D + P_Q)$, it is apparent that P_D and P_Q should be minimized in order to obtain high power-efficiency. In power-critical hearing instruments where the load impedance, R_L , is usually relatively high (200Ω to 600Ω), P_Q is dominant when the modulation index, M , is low (e.g. $M < 0.5$). Note that a high power-efficiency for $M < 0.5$ is particularly important for hearing instruments because the operating M is typically 15dB to 20dB lower ($M \leq 0.15$) than the maximum M largely due to the crest factor of audio signals and to accommodate for signal swing headroom.

Table 4-I summarizes the parameters of a Bang-Bang amplifier (Figure 4-1) and of a PWM amplifier (Figure 4-2) for a hearing instrument. The circuit parameters for these amplifiers are tabulated in Table 4-I and Table 4-II. On the basis of Table 4-I and Table 4-II, it can be seen that despite the higher switching frequency, f_{sw} , of the Bang-Bang amplifier, it features a significantly lower P_Q – largely because the power-consuming op-amp and the carrier generator are not required. To delineate its power-efficiency advantage, Figure 4-3 depicts the power-efficiency of the two different amplifiers over the full modulation index range. Of specific interest, it can be seen that at $M = 0.15$, the η_{PWM} is a low 35% compared to $\eta_{Bang} = 53\%$, and this advantage remains significant until about $M = 0.4$ where $\eta_{PWM} = 76\%$ compared to $\eta_{Bang} = 87\%$. Put simply, the Bang-Bang amplifier is potentially a very good alternative to the incumbent PWM amplifier in power-critical audio applications.

Figure 4-1 Schematic of a Bang-Bang amplifier

Figure 4-2 Schematic of a PWM amplifier

Table 4-I Parameters of the Bang-Bang amplifier and the PWM amplifier

Parameter	Bang-Bang	PWM
Supply Voltage ($V_{DD}-V_{SS}$)	1.1V	1.1V
P_Q	10 μ W	30 μ W
$P_D@M=0$	4.5 μ W ($f_{sw}=125$ kHz)	1.5 μ W ($f_{sw}=40$ kHz)
R_L	200 Ω	200 Ω

Table 4-II Circuit parameters of the Bang-Bang amplifier and the PWM amplifier

Parameter	Value
Signal Bandwidth, BW	4kHz
R_1, R_{PWM}, C, C_{PWM}	120k Ω , 90k Ω , 0.68nF, 1nF
$f_{sw(Bang)}$	125kHz ($h=0.025$)
$f_{sw(PWM)}$	40kHz
Gain of PWM Modulator, G_{PWM}	5

Figure 4-3 Comparison of η_{PWM} and η_{Bang}

4.3 THD of Bang-Bang Control Class D Amplifiers

4.3.1 THD of an ‘ideal’ Bang-Bang amplifier

In this section, as a preamble, the THD of the ‘ideal’ Bang-Bang amplifier is first investigated; ‘ideal’ being defined as $t_D=0$ and $R_{on}=0$ (where t_D is the Bang-Bang controller propagation delay and R_{on} is the ‘on’ output impedance of the Class D output

stage). This investigation is thereafter extended to the practical Bang-Bang amplifier whose $t_D > 0$ and $R_{on} > 0$.

As depicted in Figure 4-1, the Bang-Bang amplifier comprises a Bang-Bang controller (realized by a hysteresis comparator), an output stage, an RC feedback network (including R_{in} , R_{fb} and C) and a load (including a lowpass filter, L_L and C_L , and a loudspeaker, R_L). An ‘error’ signal, V_e , with exponentially rising and falling edges is generated by charging and discharging the RC network with the input signal, V_{in} , and the modulated signal, V_{out} . The Bang-Bang controller generates a Pulse-Density-Modulated-like signal, V_M , at its output by comparing the error signal against its hysteresis band $\pm V_h$. V_M serves as a control signal to trigger the switching of the output stage. The output stage provides sufficient current drive to the load.

The normalized output signal of the ‘ideal’ Bang-Bang amplifier can be derived (see Appendix A) as:

$$\frac{V_{output_ideal}}{V_{DD}} = M \sin(\omega_{in} t) + V_{THD_ideal} \quad (4.1)$$

where

$$V_{THD_ideal} = \frac{2[(1+G)h]^2}{3} \sum_{p=2}^{\infty} k_p H_p H_{LPF_p} M \sin((2p-1)\omega_{in} t) \quad (4.2)$$

$$k_p = \left| 1 + j \frac{(2p-1)\omega_{in}}{\omega_p} \right| \quad (4.3)$$

$$H_p = \sum_{n=p}^{\infty} \left[M^{2n-2} \frac{(-1)^{p-1}}{2^{2n-2}} \binom{2n}{n-p} \right] \quad (4.4)$$

$$H_{LPF,p} = \frac{1}{1 + \frac{L_L}{R_L} (2p-1)\omega_{inj} - L_L C_L [(2p-1)\omega_{inj}]^2} \quad (4.5)$$

where $h=V_h/V_{DD}$ is the normalized hysteresis of the Bang-Bang controller,

$G=R_{fb}/R_{in}$ is the closed-loop gain of the Bang-Bang amplifier,

$H_{LPF,p}$ is the magnitude response of the lowpass filter, and

$\omega_p=[(R_{in}/R_{fb})C]^{-1}$ is the corner frequency of the RC feedback network.

Eqn. (4.1) can be interpreted as follows. The first term is the amplified replica of the input signal, the desired output signal. The second term is the undesired odd harmonics of the output signal and constitutes the THD of the ‘ideal’ Bang-Bang amplifier. Based on eqns. (4.1) – (4.5), the THD is derived as:

$$\text{THD}_{\text{ideal}} = \frac{2((1+G)h)^2}{3} \sqrt{\sum_{p=2}^{\infty} (k_p H_p H_{LPF,p})^2} \quad (4.6)$$

Eqns. (4.1) – (4.5) can be interpreted as follows.

- (i) As expected, THD increases as M increases, and this is similarly observed in PWM amplifiers [76] and in linear amplifiers.
- (ii) A smaller h results in lower THD. It will be shown later in Figure 4-7 that by reducing h from 0.05 to 0.025, THD is reduced by ~75% but at the cost of increased power dissipation [98] in the output stage due to the increased switching

frequency (see eqn. (4.10) later). Nevertheless, as shown in Figure 4-3, for power-critical low-voltage applications, the higher power-efficiency advantage of the Bang-Bang amplifiers over PWM amplifiers remains.

- (iii) Similar to h , a smaller G also results in lower THD. It will be shown later that by reducing G from 2 to 1, THD is reduced by ~55%. However, reducing G further is not recommended because it undesirably reduces the maximum output power (hence dynamic range) of the Bang-Bang amplifier. In view of a desirable low THD, $G=1$ is recommended for a given h . If a higher G is required, a pre-amplifier can be used but at the cost of increased hardware and reduced power-efficiency. On the other hand, if the value of h is externally adjustable, a higher G can be used by reducing h . It can be seen from eqns. (4.6) and (4.10) later that both the THD and the switching frequency remain unchanged if the product of h and $(1+G)$ is unchanged.
- (iv) In addition to M , h and G , the THD is also affected by ω_p . In the low frequency range where $3\omega_{in} < \omega_p$ (where $3\omega_{in}$ is the frequency of the dominant 3rd-order harmonic distortion component of the output signal), such that $1 < k_p < 1.41$ (eqn. (4.3)), the THD is nearly independent of the input frequency. It can be seen from Figure 4-8 (see later) that the THD at $f_{in}=1\text{kHz}$ is only 20% higher than the THD at $f_{in}=100\text{Hz}$. Note that this is different from the PWM amplifier where its THD at $f_{in}=1\text{kHz}$ is 5 times higher than the THD at $f_{in}=100\text{Hz}$. In the high frequency range where $3\omega_{in} > \omega_p$, such that $k_p > 1$, the THD increases as input frequency increases. A high ω_p results in a relatively low THD in the high frequency range, but it undesirably increases the switching frequency (see eqn. (4.10) later) of the Bang-

Bang amplifier. In view of this analysis and (v) below, and on the basis of the author's experience, $BW \leq \omega_p \leq 1.5BW$ is recommended as it is a good compromise between low THD and low switching frequency.

- (v) The THD is also affected by f_{in} . Specifically, for $f_{in} < BW/3$, the THD is nearly independent of f_{in} whilst for $f_{in} > BW/3$, the THD reduces with f_{in} because the harmonic components of the output signal are attenuated by the output lowpass filter.

In summary, to obtain low THD_{ideal} , it is desirable that h be low, $G=1$, and that $BW \leq \omega_p \leq 1.5BW$. It will be shown later that these analyses are also applicable to the practical Bang-Bang amplifier whose $t_D > 0$ and $R_{on} > 0$.

The above analyses will be now extended to practical Bang-Bang amplifiers where the effects of t_D and R_{on} on THD will be investigated.

4.3.2 The Effect of the Propagation Delay on THD

First, consider the case when $t_D > 0$ and $R_{on} = 0$. Figure 4-4 depicts the pertinent waveforms of the Bang-Bang amplifier whose $t_D > 0$. It can be seen that due to t_D , the upper and lower limits of the hysteresis band are increased from $\pm V_h$ to V_1 and $-V_2$. V_1 and $-V_2$ can be derived as:

$$V_1 = \frac{V_{DD}(1 - M \sin(\omega_{in}t))(1 - \exp(-t_D\omega_p))}{1 + G} + V_h \exp(-t_D\omega_p) \quad (4.7)$$

$$V_2 = \frac{V_{DD}(1 + M \sin(\omega_{in}t))(1 - \exp(-t_D \omega_p))}{1 + G} + V_h \exp(-t_D \omega_p) \quad (4.8)$$

Figure 4-4 Waveforms of the Bang-Bang amplifier whose $t_D > 0$

Based on eqns. (4.7) and (4.8), and the method delineated before, the harmonic components of the Bang-Bang amplifier, V_{THD_delay} , whose $t_D > 0$ can be derived as:

$$V_{THD_delay} = \frac{2((1 + G)h)^2}{3} (1 + 8t_D f_{sw}) \cdot \sum_{p=2}^{\infty} k_p H_p H_{LPF_p} M \sin((2p - 1)\omega_{in}t) \quad (4.9)$$

where f_{sw} is the idle (zero input) switching frequency of the Bang-Bang amplifier, i.e.:

$$f_{sw} = \frac{\omega_p}{4(1 + G)h} \quad (4.10)$$

Hence, the THD when $t_D \neq 0$ (denoted as THD_{delay}) can be expressed as:

$$\text{THD}_{\text{delay}} = (1 + 8t_D f_{sw}) \text{THD}_{\text{ideal}} \quad (4.11)$$

A comparison of eqn. (4.6) and eqn. (4.11) shows that the THD arising from the propagation delay of the Bang-Bang controller increases the THD by $8t_D f_{sw}$ times. Consider the case of a typical Bang-Bang controller for a power-critical hearing instrument where the propagation delay is relaxed, $10\text{ns} < t_D < 100\text{ns}$, and the switching frequency is low, $f_{sw} = 125\text{kHz}$ (due to the low BW of the instrument). It can be shown that the effect of this relatively large t_D has negligible effect to the THD because its effect is mitigated by the low f_{sw} . This observation is of particular pertinence for the power-critical instruments because a Bang-Bang controller with a relaxed (higher) t_D usually requires lower power dissipation (because of the associated lower bias and driving current). Furthermore, a higher t_D results in better PSRR (see later in Section 4.4), a desirable attribute.

4.3.3 The Effect of the ‘On’ Output Impedance on THD

Consider now the case when $t_D > 0$ and $R_{on} > 0$. In this case, the practical output stage [98] can be effectively modeled by an output stage with zero ‘on’ output impedance and a series resistor R_{on} as depicted in Figure 4-5.

Figure 4-5 Schematic of the Bang-Bang amplifier for $R_{on} > 0$

It can be seen from Figure 4-5 that for $R_{on} > 0$, the voltage at V'_{out} is $(1 + R_{on}/R_L) \cdot V_{out}$. Hence, the harmonic components of the output signal can be derived as eqn. (4.12) by substituting the modulation index M for $(1 + R_{on}/R_L)M$ in eqns.(4.1)-(4.6) and using the method delineated in Appendix A:

$$V_{THD} = \frac{2((1+G)h)^2}{3} (1 + 8t_D f_{sw}) \cdot \sum_{p=2}^{\infty} k_p H'_p H_{LPF,p} M \sin((2p-1)\omega_{in}t) \quad (4.12)$$

where

$$H'_p = \sum_{n=p}^{\infty} \left[\left(1 + \frac{R_{on}}{R_L}\right)^{2n-1} \frac{M^{2n-2} (-1)^{p+1}}{2^{2n-2}} \binom{2n}{n-p} \right] \quad (4.13)$$

On the basis of eqn. (4.12), the THD of the practical Bang-Bang amplifier can be expressed as:

$$\text{THD} = \frac{2((1+G)h)^2}{3} (1 + 8t_D f_0) \sqrt{\sum_{p=2}^{\infty} (k_p H'_p H_{LPF-p})^2} \quad (4.14)$$

A comparison of eqn. (4.11) against eqn. (4.14) shows that R_{on} results in increased THD, and for a given R_L , the higher the R_{on} , the higher is the THD increment. For example, a low $R_{on}=2.9\Omega$ results in a small THD increment (compared to the case when $R_{on}=0$) of 10% at $M=0.8$. On the other hand, a relatively high $R_{on}=17\Omega$ results in a significant THD increment of ~120%. The effect on R_{on} is more pronounced in the high ($M>0.5$) modulation index range than in the low ($M<0.5$) modulation index range; refer to Figure 4-7 later for an example. Practically, this means that if a low THD at high modulation index range is required, it is imperative to use an output stage with low R_{on} . However, if only the THD at lower modulation index range is important, an output stage with relatively high R_{on} can be used. From an economic and operational perspectives, note that a lower R_{on} requires expensive larger IC area (see later in Figure 4-6) but results in lower power dissipation and higher power-efficiency.

In summary, to obtain low THD, it is desirable that h be low, $G=1$, $BW \leq \omega_p \leq 1.5BW$, t_D be high and R_{on} be low.

4.4 Power Supply Noise

In this section, the expressions for the PSRR and PS-IMD are derived and pertinent circuit parameters that affect PSRR and PS-IMD are investigated.

Adopting the analysis method delineated in Section 4.3 and Appendix A, the output signal $V_{output,N}$ of the Bang-Bang amplifier with supply noise can be derived as:

$$\begin{aligned} \frac{V_{output,N}}{V_{DD}} = & M \sin(\omega_{in} t) + V_{THD} + V_{PSRR} \sin(\omega_n t) \\ & + V_{PS-IMD1} \sin((\omega_{in} + \omega_n)t) + V_{PS-IMD2} \sin((\omega_{in} - \omega_n)t) \end{aligned} \quad (4.15)$$

where

$$V_{PSRR} = V_N \left[\frac{((1+G)h)^2}{3} \left(1 + \sum_{p=1}^{\infty} \frac{M^{2p}(2p+1)!}{2^{2p}p!p!} \right) - \frac{t_D \omega_p}{2} \right] \left| 1 + j \frac{\omega_n}{\omega_p} \right| \quad (4.16)$$

$$V_{PS-IMD1} = V_N \frac{((1+G)h)^2}{3} \sum_{p=1}^{\infty} \frac{M^{2p-1}p}{2^{2p-2}} \binom{2p-1}{p-1} \left| 1 + j \frac{\omega_{in} + \omega_n}{\omega_p} \right| \quad (4.17)$$

$$V_{PS-IMD2} = V_N \frac{((1+G)h)^2}{3} \sum_{p=1}^{\infty} \frac{M^{2p-1}p}{2^{2p-2}} \binom{2p-1}{p-1} \left| 1 + j \frac{\omega_{in} - \omega_n}{\omega_p} \right| \quad (4.18)$$

In eqn. (4.15), the first term is the desired output signal, the second term is the harmonic components (eqn. (4.12)), the third term (eqn. (4.16)) is the supply noise component at the output and the last two terms (eqns. (4.17) and (4.18)) are the two PS-IMD components at $\omega_{in} + \omega_n$ and $\omega_{in} - \omega_n$ respectively.

From eqns. (4.16)-(4.18), the PSRR, PS-IMD of the Bang-Bang amplifier can be derived as eqns. (4.19) and (4.20):

$$\begin{aligned}
 \text{PSRR} &= 20 \log \left(\frac{V_N}{V_{\text{PSRR}}} \right) \\
 &= 20 \log \frac{1}{\left[\frac{((1+G)h)^2}{3} \left(1 + \sum_{p=1}^{\infty} \frac{M^{2p}(2p+1)!}{2^{2p}p!p!} \right) - \frac{t_D \omega_p}{2} \right] \left(1 + j \frac{\omega_n}{\omega_p} \right)} \text{dB} \quad (4.19)
 \end{aligned}$$

$$\begin{aligned}
 \text{PS-IMD} &= 20 \log \left(\frac{\sqrt{V_{\text{PS-IMD1}}^2 + V_{\text{PS-IMD2}}^2}}{V_N} \right) \\
 &= 20 \log \left[\frac{\frac{((1+G)h)^2}{3} \sum_{p=1}^{\infty} \frac{M^{2p-1}p(2p-1)}{2^{2p-2}(p-1)}}{\sqrt{\left| 1 + j \frac{\omega_{in} + \omega_n}{\omega_p} \right|^2 + \left| 1 + j \frac{\omega_{in} - \omega_n}{\omega_p} \right|^2}} \right] \text{dB} \quad (4.20)
 \end{aligned}$$

PSRR and PS-IMD will now be interpreted in turn and in the context of a practical design.

4.4.1 PSRR

The following can be observed from eqn. (4.19):

- (i) A lower h results in improved (higher) PSRR but at the cost of higher switching frequency. It will be shown later that reducing h from 0.05 to 0.025 results in 12dB PSRR improvement.
- (ii) Further, a lower G results in higher PSRR. Specifically, reducing G from 2 to 1 results in 7dB PSRR improvement. In view of this, $G=1$ is recommended. As delineated in interpretation (iii) of eqns. (4.1) – (4.5) earlier, if higher G is required,

a pre-amplifier and/or a lower h can be used. Note that compared to the PWM amplifier, G has greater influence on the PSRR of the Bang-Bang amplifier. For example, reducing G from 2 to 1 results in 7dB and 3.5dB improvement in PSRR of the Bang-Bang amplifier and the PWM amplifier respectively.

- (iii) The PSRR of the Bang-Bang amplifier reduces as M increases – this is unlike the PWM amplifier [28, 126] and linear amplifiers whose PSRR is largely independent of M . It will be shown later that the PSRR at $M=0.8$ is ~15dB lower than the PSRR at $M=0$. This drawback of the Bang-Bang amplifier is usually not serious because when properly designed, the PSRR remains relatively high throughout the range of input signal swing (see Figure 4-9 later) and, in part, because in most cases of the low nominal signal swing (<15dB from the peak signal swing) for signal headroom.
- (iv) A higher t_D results in higher PSRR. This is largely because the supply noise component at the output due to t_D and due to h cancel each other (see eqn. (4.16)). Specifically, because the contribution by h is larger, as t_D increases, total supply noise at the output decreases. It will be shown in Section 4.5 later that $\text{PSRR}@t_D=50\text{ns}$ is approximately 10dB higher than $\text{PSRR}@t_D=10\text{ns}$. Practically, this means that a lower power dissipative Bang-Bang controller arising from a more relaxed t_D can yield an amplifier with higher PSRR – the quiescent current for the $t_D=50\text{ns}$ Bang-Bang controller and $t_D=10\text{ns}$ Bang-Bang controller are $8\mu\text{A}$ and $40\mu\text{A}$ respectively.

- (v) For $\omega_n < \omega_p$, the PSRR is almost frequency independent because $1 < |1 + j\omega_n/\omega_p| < 1.41$. Compared to PSRR at $\omega_n \ll \omega_p$, PSRR at $\omega_n = \omega_p$ is only 3dB lower. However, for $\omega_n \geq \omega_p$, the PSRR reduces as the frequency increases. Although a higher ω_p results in higher PSRR in the high frequency range, it undesirably increases the switching frequency. In view of the general desire for high PSRR (tolerance to supply noise) and low switching frequency (low power dissipation, hence high power-efficiency), it is recommended that $BW \leq \omega_p \leq 1.5BW$. Note that the same ω_p range is recommended for a low THD.

4.4.2 PS-IMD

The following can be observed from eqn. (4.20):

- (i) Similar to PSRR, a lower h and lower G result in improved (lower) PS-IMD but at the cost of higher switching frequency. For instance, reducing h from 0.05 to 0.025 results in 12dB PS-IMD improvement (see Figure 4-10(a) later), and reducing G from 2 to 1 results in 7dB PS-IMD improvement. As delineated before, if higher G is required, a pre-amplifier and/or a lower h can be used.
- (ii) As expected, the PS-IMD increases with M , and as delineated in Chapter 3 the same can be observed in PWM amplifiers.
- (iii) Unlike the case of PSRR, t_D has little effect on PS-IMD. For instance, for a given h and G , the PS-IMD difference for $t_D=10\text{ns}$ and $t_D=50\text{ns}$ is $< 2\text{dB}$.

- (iv) PS-IMD is almost input frequency independent in the lower frequency range ($\omega_{in} \pm \omega_n < \omega_p$), but increases marginally with frequency in the higher frequency range ($\omega_{in} \pm \omega_n > \omega_p$); see Figure 4-10(a) later. As before, in view of the general desire for low PS-IMD and low switching frequency, $BW \leq \omega_p \leq 1.5BW$ is recommended.

4.5 Results and Verification

In this section, the derived analytical expressions for the THD (eqn. (4.14)), PSRR (eqn. (4.19)) and PS-IMD (eqn. (4.20)) are verified by comparing them against HSPICE simulations and against measurements on prototype Class D amplifiers embodying two Class D output stage ICs with different output impedances. The microphotographs of the two Class D output stage ICs are shown in Figure 4-6.

Figure 4-6 Microphotographs of the two Class D output stages: (a) Output 1: $R_{on}=2.9\Omega$, and (b) Output 2: $R_{on}=17\Omega$

To illustrate the effects of the important circuit parameters on THD, PSRR, and PS-IMD, and to compare against the competing PWM amplifier (Figure 4-2), the THD, PSRR, and PS-IMD of the Bang-Bang amplifier are obtained for 5 different practical cases. The circuit parameters of the Bang-Bang amplifier for these cases are tabulated in Table 4-III.

Table 4-III Circuit Parameters of the Bang-Bang amplifier

Parameter	Value				
	Case 1	Case 2	Case 3	Case 4	Case 5
h	0.025	0.05	0.025	0.05	0.025
f_{sw}	125kHz	62.5kHz	83.8kHz	62.5kHz	125kHz
t_D	10ns	10ns	10ns	10ns	50ns
G	1	1	2	1	1
R_{in}	120k Ω ,	120k Ω	90k Ω	120k Ω	120k Ω
R_{fb}	120k Ω	120k Ω	180k Ω	120k Ω	120k Ω
R_{on}	2.9 Ω	2.9 Ω	2.9 Ω	17 Ω	2.9 Ω
R_L, C	200 Ω , 0.68nF (for all cases)				
BW, ω_p	2 π ×4kHz, 2 π ×4kHz (for all cases)				

Figure 4-7 summarizes the THD versus modulation index of the Bang-Bang amplifier for the parameters given in Table 4-III obtained analytically using eqn. (4.14), by HSPICE simulations and by measurements on the prototype Bang-Bang amplifiers. To illustrate the effects of h and R_{on} on the THD, the THD for Case 1, Case 2 and Case 4 are plotted.

Figure 4-7 THD of the Bang-Bang amplifier

On the basis of Figure 4-7, the following observations are made:

- (i) The derived analytical expression agrees well with the HSPICE simulations and measurements, thereby verifying eqn. (4.14).
- (ii) A comparison of Case 1 and Case 2 shows that, as expected, a lower h results in lower THD. Specifically, reducing h from 0.05 to 0.025 results in ~75% THD reduction over the entire modulation index range (0.1 to 0.8), but at the cost of lower power-efficiency due to increased switching frequency (eqn. (4.10)). Nonetheless, the power-efficiency advantage of the Bang-Bang amplifier over other Class D amplifiers, such as PWM amplifiers, remains. Where necessary, the

THD can be further improved by further reducing h but at the cost of further increased switching frequency.

- (iii) A comparison of Case 2 and Case 4 shows that it is very worthwhile to use an output stage with lower 'on' output impedance, but at the cost of larger IC area. Specifically, reducing R_{on} from 17Ω to 2.9Ω results in 50% THD reduction at $M=0.8$. From a low THD perspective, reducing R_{on} further is of diminishing return as the THD difference between $R_{on}=2.9\Omega$ and $R_{on}=0\Omega$ ('ideal' output stage) is less than 10%. Also, as reviewed in Chapter 2, note that there is an optimal size of the output transistors (and output impedances) for maximum output stage power-efficiency.
- (iv) The THD increases as M increases. For example, the THD $< 0.02\%$ for both Case 1 and Case 2 at $M = 0.15$ (a typical Class D amplifier output power setting given the large crest factor of audio signals), and increases to $\sim 0.15\%$ and $\sim 0.55\%$ for Case 1 and Case 2 respectively at $M=0.8$. These values are generally acceptable because from a practical hearing instrument perspective, THD $<0.5\%$ is acceptable.

Figure 4-8 summarizes the THD versus input frequency at a fixed $M=0.7$ for the Bang-Bang amplifier, also obtained analytically using eqn. (4.14), by HSPICE simulations and by measurements. To illustrate the effect of G , the THD for Case 1 and Case 3 are plotted. For comparison, the THD of the PWM amplifier, obtained from simulations, is also plotted.

Figure 4-8 THD @ $M=0.7$ of the Bang-Bang amplifier and the PWM amplifier

On the basis of Figure 4-8, the following observations are made:

- (i) As before, the derived analytical expression agrees well with the HSPICE simulations and measurements, thereby verifying eqn. (4.14).
- (ii) A comparison of Case 1 and Case 3 shows that, as expected, a lower G results in lower THD. Specifically, reducing G from 2 to 1 results in 55% THD reduction. As delineated before, if h can be externally adjusted, a smaller value of h can be used to mitigate the effect of G on THD. It can be seen from eqns. (4.14) and (4.10) that if the product of $(1+G) \cdot h$ remains unchanged, both the THD and the switching frequency (hence power dissipation in the output stage) remains unchanged.

- (iii) In the low frequency range where $f_{in} < 1.4\text{kHz}$, the THD of the Bang-Bang amplifier is nearly independent of the input frequency, whilst the THD of the PWM increases with the input frequency. In the high frequency range where $1.4\text{kHz} < f_{in} < 4\text{kHz}$, the THD of both the Bang-Bang amplifier and the PWM amplifier reduces as frequency increases.
- (iv) A comparison of the Bang-Bang amplifier and the PWM amplifier shows that the Bang-Bang amplifier (Case 1) exhibits higher THD for $f_{in} < 800\text{Hz}$ but features lower THD for $800\text{Hz} < f_{in} < 4\text{kHz}$. In general, the THD levels of these amplifiers are appropriate for general applications and exceed that required for hearing instruments – the overall lower THD attribute of the Bang-Bang is nonetheless particularly attractive for power-critical applications.

Figure 4-9 summarizes the PSRR @ $f_n = 120\text{Hz}$ against M of the Bang-Bang amplifier obtained analytically using eqn. (4.19), by HSPICE simulations and by measurements. To illustrate the effect of h and t_D on PSRR, the PSRR for Case 1, Case 2 and Case 5 are plotted. For comparison, the PSRR of the PWM amplifier is also plotted.

Figure 4-9 PSRR of the Bang-Bang amplifier and the PWM amplifier

On the basis of Figure 4-9, the following observations are made:

- (i) As before, the derived analytical expression agrees well with the HSPICE simulations and measurements, thereby verifying eqn. (4.19).
- (ii) A comparison of Case 1 and Case 2 shows that a lower h results in higher PSRR, and this is expected because a lower h results in lower supply noise at the output as expressed in eqn. (4.16). Specifically, reducing h from 0.05 to 0.025 results in ~12dB PSRR improvement, but at the cost of increased switching frequency.
- (iii) A comparison of Case 1 and Case 5 shows that it is very worthwhile to use a Bang-Bang controller with relatively relaxed (high) propagation delay, t_D . Specifically, a Bang-Bang controller with a 50ns propagation delay not only results in ~10dB PSRR improvement compared to one with a 10ns propagation

delay, it yields a design with lower power dissipation. For example, the quiescent current for the $t_D=50\text{ns}$ Bang-Bang controller and $t_D=10\text{ns}$ Bang-Bang controller are $8\mu\text{A}$ and $40\mu\text{A}$ respectively.

- (iv) The PSRR reduces as M increases, and this contrasts with the PWM amplifier whose PSRR is usually independent of M . For example, in Case 1 and Case 2, PSRR at $M=0.8$ is $\sim 15\text{dB}$ lower than at $M=0$. The reduction of PSRR at high modulation index is not usually a serious drawback as discussed previously.
- (v) Compared to the PWM amplifier, the Bang-Bang amplifier usually features higher PSRR even for the poorer case (Case 2) where a relatively high $h=0.05$ is used. It can be seen that for Case 2, the PSRR of the Bang-Bang amplifier is higher for $M<0.6$, whilst for Case 1 and Case 5, the PSRR of the Bang-Bang amplifier is higher throughout the entire modulation index range. Note that this comparison is based on the supply noise frequency, $f_n = 120\text{Hz}$ – if f_n is higher, the PSRR of the Bang-Bang amplifier becomes even more advantageous. This is because the PSRR of the Bang-Bang amplifier is nearly independent of f_n whilst the PSRR of the PWM amplifier reduces with f_n at the rate of 20dB/dec .

Figure 4-10(a) and (b) summarize the PS-IMD of the Bang-Bang amplifier against the input frequency and against M respectively. To illustrate the effect of h on PS-IMD, the PS-IMD for Case 1 and Case 2 are plotted in Figure 4-10(a). As before and for comparison, the PS-IMD of the PWM is also plotted. In Figure 4-10(a), $f_n=120\text{Hz}$ and $M=0.7$, and in Figure 4-10(b), $f_n=120\text{Hz}$ and $f_{in}=1\text{kHz}$.

(a)

(b)

Figure 4-10 PS-IMD of the Bang-Bang amplifier and the PWM amplifier (a) versus input frequency, and (b) versus modulation index

On the basis of Figure 4-10(a) and Figure 4-10(b), the following observations are made:

- (i) As before, the derived analytical expression agrees well with the HSPICE simulations and measurements, thereby verifying eqn. (4.20).
- (ii) It can be seen from Figure 4-10(a) that the PS-IMD is nearly independent of frequency except for a slight increment for $f_{in} > 2\text{kHz}$. For example, PS-IMD at $f_n = 4\text{kHz}$ is merely 3dB higher than PS-IMD at $f_n = 100\text{Hz}$. Although the slightly higher PS-IMD in the higher frequency range is not usually considered a drawback, it can be easily circumvented by increasing ω_p but at the cost of increased power dissipation in the output stage due to the increased switching frequency. For example, if ω_p is selected to be 1.5 times the 4kHz signal bandwidth, $\omega_p = 2\pi \cdot 6\text{kHz}$, PS-IMD at $f_{in} = 4\text{kHz}$ is only 1.5dB higher than the PS-IMD at $f_{in} = 100\text{Hz}$, but at the cost of increasing the switching frequency from 125kHz to 188kHz.
- (iii) It can be seen from Figure 4-10(a) that in general, the PS-IMD of the Bang-Bang amplifier is significantly lower (better) than that of the PWM amplifier. Specifically, for Case 1, the PS-IMD of the Bang-Bang amplifier is lower than that of the PWM amplifier for all the frequencies, and for Case 2, the PS-IMD of the Bang-Bang amplifier is lower than that of the PWM amplifier for $f_{in} > 300\text{Hz}$. Further, the PS-IMD advantage of the Bang-Bang amplifier over the PWM amplifier increases markedly as the input frequency increases.

- (iv) From Figure 4-10(b) and as expected, the PS-IMD increases as M increases. Specifically, the PS-IMD increases (degrades) from -80dB to -45dB for $M=0.1$ to 0.8.
- (v) Further to (iii) and (iv), it can be seen from Figure 4-10(b) that for the given input frequency of $f_{in}=1\text{kHz}$, the PS-IMD of the Bang-Bang amplifier is highly advantageous over the PWM amplifier, especially in the lower modulation index range. Specifically, at $M=0.15$ and $M=0.8$, the PS-IMD of the Bang-Bang amplifier is $\sim 30\text{dB}$ and $\sim 15\text{dB}$ lower than the PWM amplifier respectively.
- (vi) A comparison of Figure 4-10(b) and Case 1 in Figure 4-9 shows that the PS-IMD is usually smaller than the supply noise component (at f_n) at the output (eqn. (4.16)). Conversely, as delineated in Chapter 3, in the case of the PWM amplifier, the PS-IMD can be significantly larger than the supply noise component at the output. The difference between the Bang-Bang amplifier and the PWM amplifier is largely because the PSRR and PS-IMD of the PWM amplifier degrade with f_{in} , whilst the PSRR and PS-IMD of the Bang-Bang amplifier are nearly independent of f_{in} .

In summary, in addition to the higher power-efficiency and lower hardware advantages of the Bang-Bang amplifier, its PSRR and PS-IMD attributes are advantageous over the PWM amplifier.

4.6 Conclusions

The adoption of a Bang-Bang amplifier over the incumbent PWM amplifier for power-critical low-voltage applications has been suggested, and it has been shown that compared to the PWM amplifier, Bang-Bang amplifiers are advantageous in power-efficiency. Analytical expressions for the THD, PSRR and PS-IMD of the Bang-Bang amplifier have been derived and verified against HSPICE simulations and on the basis of measurements on a prototype Class D amplifiers embodying two Class D output stage ICs. On the basis of these analytical expressions, the primary parameters affecting the THD, PSRR and PS-IMD of the Bang-Bang amplifiers have been investigated. The analyses have provided an analytical means to quantify the THD, PSRR and PS-IMD, and provide valuable insight to the mechanisms and pertinent parameters therein. The Bang-Bang amplifier and the prevalent PWM have also been compared, and in most cases, the former has been shown to have superior parameters over the latter.

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

5.1 Introduction

A large portion of this chapter has been published in the *IET Circuits, Devices and Systems* [29].

As discussed in Chapter 1, in a traditional Class D amplifier [28, 66, 76, 126, 127], an output *LC* lowpass filter is commonly used to attenuate the high frequency carrier signal (and related components), and the amplified replica of the input is thereby obtained. A design methodology that has recently received some acceptance is the filterless approach where the abovementioned bulky output filter that typically accounts for ~30% of the cost and ~75% of the PCB area in a Class D amplifier realization is not required.

Filterless Class D amplifiers are usually based on the 3-state modulation architecture depicted in Figure 5-4 (see later) whilst the conventional (2-state) architecture in a filterless configuration is depicted in Figure 5-3 (see later); the conventional architecture in a 'filterless' configuration that will be proposed here is a somewhat unorthodox approach. In typical designs, the former has a higher power-efficiency attribute. In this chapter, it is shown, for the first time, that it is possible to employ the conventional 2-state architecture as a filterless amplifier if certain circuit conditions are

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

satisfied – specifically a sufficiently high carrier frequency and a loudspeaker with sufficient inductance. For brevity, the filterless Class D amplifiers based on the 3-state architecture and based on the conventional architecture are abbreviated as the 3State amplifier and Conv amplifier respectively. In both the Conv amplifier and 3State amplifier, an inductive loudspeaker is required in place of the output lowpass filter to attenuate the high frequency carrier current (and related components), hence the need for a higher power rated loudspeaker to accommodate both the usual audio power and the additional power dissipation due to the attenuation of the high frequency components. This additional power dissipation is denoted P_{sw} .

In this chapter, the established model [24-26] for loudspeakers in the audio frequency range is extended to the high frequency range (20kHz – 1MHz); this range will henceforth be referred to as the ‘high frequency’ range. This is the first loudspeaker model for the high frequency range reported in the literature – the high frequency model was unnecessary in linear audio amplifiers and traditional filtered Class D amplifiers because the high frequency components are respectively either largely non-existent or eliminated by the output lowpass filter, but it is pertinent to filterless Class D amplifiers due to the existence of the high frequency components. On the basis of the model for loudspeakers in the high frequency range, analytical expressions for P_{sw} and power-efficiency, η , for both the Conv amplifier and 3State amplifier are thereafter derived. These derived analytical expressions are significant as they provide insight to Class D amplifier designers on the mechanisms and details of the high frequency output components, how the (additional) power rating and inductance of the loudspeaker should be selected for Conv amplifiers and for 3State amplifiers, and what parameters are

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

available and may be varied and/or compromised to meet a given set of specifications, including η . The practical implications for the variations of several parameters are also delineated. For completeness, note that the analyses herein are applicable to both analog and digital [36] Class D amplifiers as they employ the same output stage topology. On the basis of the derived analytical work herein, it is shown, somewhat serendipitously, that the Conv and the 3State amplifiers can feature nearly comparable η if certain circuit conditions are satisfied.

This chapter is organized in the following manner. In Section 5.2, the model for the loudspeaker in high frequency range is derived. In Section 5.3, the analytical expressions for P_{sw} and η for both the Conv amplifier and 3State amplifier are derived. In Section 5.4, the analytical work herein is verified by comparing the results obtained from the derived analytical expressions against practical measurements on Class D amplifiers. Finally, conclusions are drawn in Section 5.5.

5.2 Modeling of Loudspeakers

5.2.1 A Review of the Loudspeaker Model in the Audio Range

Figure 5-1(a) depicts the well established loudspeaker model [24-26] for the audio frequency range ($<20\text{kHz}$), comprising the voice coil inductance (L_C), DC voice coil resistance (R_C), and the electrical equivalents of the major mechanical components, including the suspension compliance (L_{CES}), cone mass (C_{MEC}) and suspension losses (R_{EC}).

Figure 5-1 Loudspeaker model for (a) audio frequency range, and (b) simplified loudspeaker model for $f > 1\text{ kHz}$

In the lower frequency range of the audio band, the effects of L_{CES} , C_{MEC} and R_{EC} dominate. As the frequency increases, the loudspeaker impedance is dominated by R_C and L_C , and the model can be simplified [24-26] as a series $L_C R_C$ in Figure 5-1(b). Due to the effect of eddy currents in the magnet structure in the loudspeaker, L_C is usually modeled [26] as a lossy inductor whose impedance in the audio band is:

$$Z_{L(AF)}(\omega) = R_A \omega^{r_A} + jX_A \omega^{x_A} \quad (5.1)$$

where R_A , X_A , r_A and x_A are loudspeaker dependent parameters.

5.2.2 The Loudspeaker Model in the High Frequency Range (20kHz-1MHz)

In the high frequency range, the simplified model in Figure 5-1(b) applies where R_C , as expected, remains invariant and L_C can be similarly modeled. On the basis of eqn.

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

(5.1), the impedance of L_C in the high frequency range are re-expressed in a slightly different way to facilitate a simple measurement means to obtain the pertinent parameters of the loudspeaker.

$$Z_{L(HF)}(\omega) = R_L(\omega) + jX_L(\omega) \quad (5.2)$$

where

$$X_L(\omega) = X_{ref} \cdot \left(\frac{\omega}{\omega_{ref}} \right)^{x_H} \quad (5.3)$$

$$R_L(\omega) = R_{ref} \cdot \left(\frac{\omega}{\omega_{ref}} \right)^{r_H} \quad (5.4)$$

where X_{ref} and R_{ref} are the measured reactance and resistance of the lossy inductor at the reference frequency ω_{ref} (carrier frequency), and x_H and r_H are loudspeaker dependent parameters that would need to be determined. It can be seen by comparing eqns. (5.2) – (5.4) against eqn. (5.1) that $X_{ref}/(\omega_{ref}^{x_H})$, $R_{ref}/(\omega_{ref}^{r_H})$, x_H and r_H in eqns. (5.2) – (5.4) are effectively X_A , R_A , x_A and r_A respectively in eqn. (5.1).

The parameters in eqns. (5.2) – (5.4) may be obtained in a number of ways, and the following simple procedure is suggested:

Step 1: Determine the carrier frequency, f_{sw} , of the Class D amplifier and $\omega_{ref} = 2\pi f_{sw}$.

Step 2: Measure $X_{ref} = X_L(\omega_{ref})$, $X_L(2\omega_{ref})$ and $X_L(4\omega_{ref})$.

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

Step 3: (a) Substitute $X_L(2\omega_{ref})$, X_{ref} , ω_{ref} and $\omega = 2\omega_{ref}$ into eqn. (5.3), and the first instance of x_H value, denoted as x_{H1} , is obtained.

(b) Substitute $X_L(4\omega_{ref})$, X_{ref} , ω_{ref} and $\omega=4\omega_{ref}$ into eqn. (5.3), and the second instance of x_H value, denoted as x_{H2} , is obtained.

(c) To obtain the value of x_H in eqn. (5.3), $x_H = 0.5(x_{H1} + x_{H2})$.

All parameters in eqn. (5.3) are now obtained.

Step 4: Repeat Steps 1 to 3 to obtain the parameters in eqn. (5.4). Note that, unlike $X_L(\omega_{ref})$, $X_L(2\omega_{ref})$ and $X_L(4\omega_{ref})$ whose values are directly obtained from measurements using an *RLC* meter, $R_L(\omega_{ref})$, $R_L(2\omega_{ref})$ and $R_L(4\omega_{ref})$ are obtained from measuring the loudspeaker resistance (across its input terminals) at ω_{ref} , $2\omega_{ref}$ and $4\omega_{ref}$ minus R_C .

As an example using the suggested procedure, Z_L of the popular Visaton SC5.9 loudspeaker is determined:

$$Z_{L(HF)}(\omega) = 26.2 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.66} + j38.9 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.57} \quad (5.5)$$

In the author's experience and measurements on 10 different loudspeakers (see Appendix B), the values of x_H and r_H of most loudspeakers are approximately equal and may be approximated as $x_H = r_H = 0.6$. In the high frequency range where $\omega \geq \omega_{sw}$ and $R_C \ll R_L(\omega)$, the phase angle of the loudspeaker, $\varphi(\omega)$, can hence be estimated by:

$$\varphi(\omega) = \cos^{-1} \left(\frac{R_{ref} + R_C}{\sqrt{X_{ref}^2 + (R_{ref} + R_C)^2}} \right) \quad (5.6)$$

This implies that although both $X_L(\omega)$ and $R_L(\omega)$ are frequency dependent, the phase angle of the loudspeaker $\varphi(\omega)$ is almost frequency independent (but loudspeaker dependent) and typically ranges between 50° to 60° . The physical implication of this observation to power dissipation will be delineated in Section 5.3 later.

To show the validity of the extended model for loudspeaker in the high frequency range and the suggested procedure, the resistance $R_L(\omega)$ and reactance $X_L(\omega)$ predicted by the high frequency model (eqn. (5.5)) are compared against measured data in Figure 5-2. It can be seen that the characteristics of the loudspeaker modeled from eqn. (5.5) and the measurements agree well, thereby verifying the extended model of the loudspeaker in the high frequency range and the suggested procedure. Note that for the sake of brevity, only one loudspeaker example is illustrated – the extended model and the suggested procedure are valid for 10 different loudspeakers given in Appendix B.

Figure 5-2 R_L and X_L versus frequency

5.3 Power Dissipation and Power-Efficiency of Conv and 3State Filterless Class D Amplifiers

In this section, on the basis of the high frequency loudspeaker model, the additional power dissipation, P_{sw} , and the power-efficiency, η , of the Conv and 3State amplifiers will be derived.

5.3.1 Power Dissipation

Figure 5-3 and Figure 5-4 respectively depict the schematic of a Conv and 3State amplifiers. For the Conv amplifier in Figure 5-3, the two output modulated PWM signals, V_{out1} and V_{out2} , are 180° out of phase with respect to each other, whilst for the 3State amplifier in Figure 5-4, the two output modulated PWM signals, V_{out3} and V_{out4} , are in

phase. It will be shown later that the in-phase and out-of-phase difference in their output signals consequently results in a difference in their P_{sw} .

Figure 5-3 Schematic of a Conv amplifier

Figure 5-4 Schematic of a 3State amplifier

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

On the basis of the double-Fourier series expression [68] for a single-ended PWM signal, the differential output voltage of the Conv amplifier (denoted as $V_{\text{Conv}}=V_{\text{out1}}-V_{\text{out2}}$) and of the 3State amplifier (denoted as $V_{\text{3State}}=V_{\text{out3}}-V_{\text{out4}}$) can be derived:

$$\begin{aligned}
 V_{\text{Conv}} = & V_{DD} M \cos(\omega_{in} t) \\
 & + 4V_{DD} \sum_{m=1}^{\text{even}} \sum_{n=1}^{\pm \text{odd}} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(m\omega_{sw} t + n\omega_{in} t) \sin\left(\frac{m+n}{2}\pi\right) \\
 & + 4V_{DD} \sum_{m=1}^{\text{odd}} \sum_{n=0}^{\pm \text{even}} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(m\omega_{sw} t + n\omega_{in} t) \sin\left(\frac{m+n}{2}\pi\right)
 \end{aligned} \tag{5.7}$$

$$\begin{aligned}
 V_{\text{3State}} = & V_{DD} M \cos(\omega_{in} t) \\
 & + 4V_{DD} \sum_{m=1}^{\text{even}} \sum_{n=1}^{\pm \text{odd}} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(m\omega_{sw} t + n\omega_{in} t) \sin\left(\frac{m+n}{2}\pi\right)
 \end{aligned} \tag{5.8}$$

Eqns. (5.7) and (5.8) are interpreted as follows. The first term in eqns. (5.7) and (5.8) is the amplified replica of the input signal, the desired output signal. The second term in eqns. (5.7) and (5.8) is the intermodulation distortion between the even harmonics of the carrier and odd harmonics of the input signal. The third term in eqn. (5.7), which is absent in eqn. (5.8), is the odd harmonics of the carrier and the intermodulation distortion between the odd harmonics of the carrier and the even harmonics of the input signal. Note that the second and third terms in eqn. (5.7) and the last term in eqn. (5.8) are the high frequency components and respectively constitute the components of P_{sw} of the Conv

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

amplifier (denoted as $P_{sw(Con v)}$) and the 3State amplifier (denoted as $P_{sw(3State)}$) that are dissipated in the loudspeaker. The absence of the harmonics of the carrier and the intermodulation products between the odd harmonics of the carrier and the even harmonics of the input signal consequently results in lower P_{sw} of the 3State amplifier in the loudspeaker (hence higher η) than the Conv amplifier, and this will be verified in Section 5.4 later.

On the basis of the extended model for the loudspeaker in the high frequency range and eqns. (5.7) and (5.8), $P_{sw(Con v)}$ and $P_{sw(3State)}$ can now be derived. Note that $P_{sw(Con v)}$ and $P_{sw(3State)}$ can be expressed in two forms, and each form depicts a different interpretation for Class D amplifier designers. In the first form, $P_{sw(Con v)}$ and $P_{sw(3State)}$ are:

$$P_{sw(Con v)} = \sum_{m=1}^{even} \sum_{n=1}^{\pm odd} \frac{\left(4V_{DD}J_n\left(\frac{m\pi M}{2}\right) \cdot \frac{1}{m\pi}\right)^2 (R_L(m\omega_{sw} + n\omega_{in}) + R_C)}{2(Z_L(m\omega_{sw} + n\omega_{in}) + R_C)^2} \quad (5.9)$$

$$+ \sum_{m=1}^{odd} \sum_{n=0}^{\pm even} \frac{\left(4V_{DD}J_n\left(\frac{m\pi M}{2}\right) \cdot \frac{1}{m\pi}\right)^2 (R_L(m\omega_{sw} + n\omega_{in}) + R_C)}{2(Z_L(m\omega_{sw} + n\omega_{in}) + R_C)^2}$$

$$P_{sw(3State)} = \sum_{m=1}^{even} \sum_{n=1}^{\pm odd} \frac{\left(4V_{DD}J_n\left(\frac{m\pi M}{2}\right) \cdot \frac{1}{m\pi}\right)^2 (R_L(m\omega_{sw} + n\omega_{in}) + R_C)}{2(Z_L(m\omega_{sw} + n\omega_{in}) + R_C)^2} \quad (5.10)$$

The interpretation of eqns. (5.9) and (5.10) is similar to that given for eqns. (5.7) and (5.8) respectively. For practical computation of eqns. (5.9) and (5.10), m and n can be truncated to $m=5$ and $n=5$ as the power dissipation components beyond these are negligible. It can be observed from eqns. (5.9) and (5.10) that if $R_L(\omega)$ is invariant (R_C is

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

always invariant), $P_{sw(Con v)}$ and $P_{sw(3State)}$ are inversely proportional to $(Z_L(\omega)+R_C)^2$. Physically, this means that if the reactance $X_L(\omega)$ is increased (for example, by adding an external inductor) and $R_L(\omega)+R_C$ is left unchanged, both $P_{sw(Con v)}$ and $P_{sw(3State)}$ are reduced. For example, by inserting a $47\mu\text{H}$ inductor between one of the Class D amplifier outputs and one of the loudspeaker terminals, the total reactance at $f_{sw}=150\text{kHz}$ increases from 38.9Ω to 83.2Ω and the total impedance (eqn. (5.5)) increases from 50.8Ω to 89.4Ω . From eqns. (5.9) and (5.10), $P_{sw(Con v)}$ and $P_{sw(3State)}$ are reduced by $\sim 70\%$ and $\sim 80\%$ respectively. This example will be further delineated in detail in Section 5.4 later.

In the second form, $P_{sw(Con v)}$ and $P_{sw(3State)}$ can be expressed as follows:

$$P_{sw(Con v)} = \sum_{m=1}^{even} \sum_{n=1}^{\pm odd} \frac{\left(4V_{DD}J_n\left(\frac{m\pi M}{2}\right) \cdot \frac{1}{m\pi}\right)^2 \cos \varphi(m\omega_{sw} + n\omega_{in})}{2(Z_L(m\omega_{sw} + n\omega_{in}) + R_C)} \\ + \sum_{m=1}^{odd} \sum_{n=0}^{\pm even} \frac{\left(4V_{DD}J_n\left(\frac{m\pi M}{2}\right) \cdot \frac{1}{m\pi}\right)^2 \cos \varphi(m\omega_{sw} + n\omega_{in})}{2(Z_L(m\omega_{sw} + n\omega_{in}) + R_C)} \quad (5.11)$$

$$P_{sw(3State)} = \sum_{m=1}^{even} \sum_{n=1}^{\pm odd} \frac{\left(4V_{DD}J_n\left(\frac{m\pi M}{2}\right) \cdot \frac{1}{m\pi}\right)^2 \cos \varphi(m\omega_{sw} + n\omega_{in})}{2(Z_L(m\omega_{sw} + n\omega_{in}) + R_C)} \quad (5.12)$$

The interpretations for eqns. (5.11) and (5.12) are similar to that given for eqns. (5.7) and (5.8) respectively, and m and n can be similarly truncated to $m=5$ and $n=5$. It can however be observed here that if $\varphi(\omega)$ is a constant, $P_{sw(Con v)}$ and $P_{sw(3State)}$ are inversely proportional to $Z_L(\omega)+R_C$. As delineated in Section II earlier, in the high frequency range, $\varphi(\omega)$ is usually frequency independent (but loudspeaker dependent) and

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

typically ranges from 50° to 60° . This observation leads to two practical design possibilities.

First, $P_{sw(\text{Conv})}$ and $P_{sw(3\text{State})}$ are reduced if a higher carrier frequency is used. This is largely because $Z_L(\omega) + R_C \approx Z_L(\omega)$ and is approximately proportional to ω^{x_H} . For example, as doubling the carrier frequency increases $Z_L(\omega)$ by $\sim 50\%$ (for the case of $x_H = 0.6$), P_{sw} is consequently reduced by $\sim 35\%$. Other than this power dissipation consideration, there are other practical considerations when selecting f_{sw} . Specifically, increasing f_{sw} results in improved dynamic range and THD [76]. However, it also results in added switching losses [98] in the output stage, somewhat defeating the power advantage in the reduction of P_{sw} . In some cases, this switching loss (heat) would need to be dissipated safely by a heatsink, defeating the small form factor and cost advantages of the filterless Class D amplifiers.

Second, $P_{sw(\text{Conv})}$ and $P_{sw(3\text{State})}$ can be reduced by selecting a loudspeaker with an $X_L(\omega)$ and $R_L(\omega)$ that are large in the high frequency range. For example, doubling the $X_L(\omega)$ and $R_L(\omega)$ in the high frequency range reduces P_{sw} by $\sim 50\%$.

5.3.2 Power-Efficiency

From the analytical expressions for $P_{sw(\text{Conv})}$ and $P_{sw(3\text{State})}$, the power-efficiency of the Conv and 3State amplifiers (denoted as $\eta_{(\text{Conv})}$ and $\eta_{(3\text{State})}$ respectively) can now be obtained.

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

$$\eta_{(Conv)} = \frac{P_{sig}}{P_{sig} + P_{on} + P_{sw(Conv)} + P_{CDA}} \quad (5.13)$$

$$\eta_{(3State)} = \frac{P_{sig}}{P_{sig} + P_{on} + P_{sw(3State)} + P_{CDA}} \quad (5.14)$$

where P_{sig} (eqn. (5.15) below) is the desired audio signal power,

P_{on} [98] is the power dissipation (eqn. (5.16) below) due to the output impedance,

R_{on} , of the output stage, and

P_{CDA} is the power dissipation due to the remaining functional blocks of the Class D amplifier plus the switching losses of the output stage.

$$P_{sig} = \frac{V_{DD}^2 M^2 (R_L(\omega_{in}) + R_C)}{2(Z_L(\omega_{in}) + R_C)^2} \quad (5.15)$$

$$P_{on} = P_{sig} \cdot \frac{2R_{on}}{R_L(\omega_{in}) + R_C} \quad (5.16)$$

It will be shown later in Section 5.4 that the dominant parameters of $\eta_{(Conv)}$ and $\eta_{(3State)}$ are usually P_{sw} and P_{CDA} respectively.

In summary, with the extended model for loudspeakers in the high frequency range in Section 5.2, expressions for P_{sw} and η for the Conv and 3State amplifiers have been derived.

5.4 Results and Verification

In this section, the analytical expressions for P_{sw} and η (eqns. (5.9) – (5.14)) for the Conv and 3State amplifiers are verified by measurements on prototype amplifiers constructed using discrete components. The effects of various parameters on the performance of the two amplifiers are discussed, and their power-efficiency compared. Table 5-I tabulates the parameters for the two amplifiers where for fair comparison, their parameters are identical.

Table 5-I Parameters of the Conv amplifier and the 3State amplifier

Parameter	Value
f_{sw}, f_{in}	150kHz, 1kHz
Supply Voltage, V_{DD}	10V
Maximum output power, $P_{O,Max}$	6W
P_{CDA} (assumed)	200mW
R_{on} , Loudspeaker (Visaton SC 5.9)	0.3 Ω , 8 Ω
Maximum modulation index, M_{Max}	0.7

Figure 5-5(a) and Figure 5-5(b) respectively plots P_{sw} and η of the Conv and the 3State amplifiers against modulation index, M , obtained analytically via eqns. (5.9) – (5.14) and by practical measurements. For the Conv amplifier, two cases are measured – in Conv Case 1, the Visaton SC5.9 loudspeaker is connected directly to the outputs of the Conv amp; in Conv Case 2, a 47 μ H inductor is connected between the output of the Conv amplifier and the Visaton SC5.9 loudspeaker. To elucidate η from a practical perspective, the ‘ideal’ η is also plotted in Figure 5-5(b) – this ‘ideal’ η is the maximum achievable η for a filterless amplifier whose $P_{sw}=0$ but accounting for the power dissipation due to R_{on} (P_{on} in eqn. (5.16)) and assuming that $P_{CDA}=200$ mW.

(a)

(b)

Figure 5-5 (a) P_{sw} , and (b) η of the Conv amplifier and the 3State amplifier

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

On the basis of Figure 5-5(a) and Figure 5-5(b), the following observations are made:

- (i) The derived analytical expressions, eqns. (5.9) – (5.14), agree well with the practical measurements, thereby verifying eqns. (5.9) – (5.14).
- (ii) A Comparison of the Conv Case 1 and 3State amplifiers shows that the 3State amplifier features a lower P_{sw} , hence a higher η , for a given loudspeaker. The differences between the P_{sw} of the two topologies are attributed to the absence of the harmonics of the carrier, and the intermodulation products between the fundamental and the odd harmonics of the carrier and the even harmonics of the input signal in the 3State amplifier as delineated earlier in eqns. (5.7) and (5.8) respectively.
- (iii) A Comparison of Conv Case 1 and Conv Case 2 shows that it is very worthwhile to add an inductor in series with the loudspeaker; refer to eqn. (5.9); also see comment (v) below. The inclusion of the inductor yields a significant reduction of P_{sw} by ~70%, thereby increasing the power-efficiency from ~55% to ~70% at $M=0.5$. The drawback here is the added cost of the 47 μ H inductor and the increased form-factor of the overall Class D amplifier.
- (iv) Following on (iii) and in the overall perspective of power dissipation, P_{sw} is the dominant parameter of the ‘wasted’ power (comprising P_{on} , P_{sw} and P_{CDA}) in the Conv amplifier. In contrast, in the case of the 3State amplifier, P_{CDA} is the dominant parameter of the total ‘wasted’ power. Put simply, if a high power-efficient amplifier is required, P_{CDA} is the major parameter to consider in the

Chapter 5 Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation

3State amplifier whilst P_{sw} is the major parameter to consider in the Conv amplifier.

- (v) Following on (iii) and eqns. (5.9) - (5.14), it appears that a higher η may be attained if an inductor with a higher inductance (reactance) is used to further reduce P_{sw} . However, there is a practical limit to the inductance as the inductor may attenuate the upper end of the audio band spectrum (10kHz to 20kHz). For example, if a 100 μ H inductor is used instead of 47 μ H, P_{sw} is further reduced by ~75% in Conv Case 2 and η is increased to ~35% (very close to the 'ideal' efficiency). This, however, undesirably reduces the signal power at 10kHz by ~50% and at 20kHz by ~70%, causing the Class D amplifier frequency response to undesirably droop at the upper end of the audio frequency range.
- (vi) Instead of an additional inductor in comment (iii) above, a loudspeaker with higher internal inductance (whose low frequency impedance remains relatively constant (dominated by the DC resistance)) may be used. As interpreted in eqn. (5.11), a lower P_{sw} , hence a higher η , can be achieved. For instance, if Eurotec International: 59-P12.00-01F loudspeaker (whose inductance is ~ 2.4 times of the inductance of Visaton SC 5.9 loudspeaker, see eqn. (B.6) in Appendix B) is used, P_{sw} is reduced by ~60% throughout the entire modulation index range.

Figure 5-6 compares the η of the 3State amplifier and the Conv amplifier when the carrier frequency and the internal inductance of the loudspeaker are relatively high. Specifically, the carrier frequency of the 3State amplifier and the Conv amplifier is

500kHz and the loudspeaker is Eurotec International: 59-P12.00-01F (see eqn. (B.6) and Figure A(vi) in Appendix B).

Figure 5-6 η of the Conv amplifier and the 3State amplifier

It is apparent from Figure 5-6 that if the internal inductance of the loudspeaker and the carrier frequency of the amplifier are high, the power-efficiency of the Conv amplifier is nearly comparable to that of the 3State amplifier. Note that high carrier frequency results in low THD and higher PSRR, but at the cost of higher power dissipation in the output stage. For completeness, design parameters pertaining to power dissipation in the output stage of Class D amplifiers had been previously discussed.

5.5 Conclusions

A model for loudspeakers in the audio frequency range has been extended to a loudspeaker model in the high frequency range (20kHz – 1MHz), and a procedure to obtain the parameters of the latter has been suggested and verified to be precise. Based on the extended loudspeaker model and by means of double-Fourier series analysis, expressions for the additional power dissipation (P_{sw}) due to the attenuation of the high frequency components in the loudspeaker and for power-efficiency (η) of the Conv and 3State amplifiers have been derived. The P_{sw} and η expressions provide insight into the mechanisms of P_{sw} and provide several practical means of improving η , and the implications thereof have been delineated. It has been shown that if the carrier frequency is high and the loudspeaker inductance is high, the power-efficiency of the Conv amplifier can be nearly comparable to that of the 3State amplifier.

Chapter 6 Conclusions and Recommendations

6.1 Conclusions

In this Ph.D research program, various aspects of analog Class D amplifiers have been investigated. These aspects included investigations into the mechanisms of some non-linearities (specifically the THD, PSRR and PS-IMD) of various Class D amplifiers, proposals of novel design methodologies to mitigate some of these non-linearities, investigations into power dissipation and power-efficiency of filterless Class D amplifiers, and modeling of loudspeakers. These investigations and design proposals presented in this research program are useful as they provide analog Class D amplifier designers useful insight into mechanisms of the pertinent non-linearities and of the power-efficiency, and provide the designers an analytical means on how various design parameters can be varied to meet a given set of design specifications.

In Chapter 2, linear and switching audio amplifiers have been comprehensively reviewed. A comparison of the power-efficiency of various classes of audio amplifiers showed that Class D amplifiers feature significantly higher power-efficiency than classical linear amplifiers. A comprehensive review on Class D amplifiers has been provided, including various modulation techniques, Class D output stage design, and traditional (filtered) and filterless Class D amplifiers. Amongst the various modulation techniques reviewed, the PWM Class D amplifier is most prevalent largely due to its

simple hardware and high power-efficiency (due to the low switching frequency), and the Bang-Bang control Class D amplifier features the simplest hardware (hence possibly the highest power-efficiency in power-critical low-voltage applications such as hearing instruments).

In Chapter 3, the mechanisms of power supply-related non-linearities, PSRR and PS-IMD, of three PWM Class D amplifiers, open-loop, single-feedback and double-feedback PWM Class D amplifiers, have been investigated and the associated analytical expressions derived. It has been shown that to obtain good PSRR and PS-IMD (specifically, high PSRR and low PS-IMD), it is imperative that the loop-gain is high, and the associated parameters for high loop-gain (hence high PSRR and low PS-IMD) are high integrator gain, low feedback factor, and high switching frequency. The comparison of the double-feedback PWM amplifier and single-feedback PWM amplifier has shown that the double-feedback PWM amplifier features worthy PSRR and PS-IMD advantages over the single-feedback PWM amplifier but at the cost of increased hardware.

A simple design methodology to improve PSRR and PS-IMD has been proposed, wherein the proposed technique improves the PSRR and PS-IMD by $\sim 26\text{dB}$ with very low hardware overheads.

The analytical expressions for PSRR and PS-IMD of the Class D amplifiers using the aforesaid proposed methodology have been derived, and the effects of key parameters on PSRR and PS-IMD have been delineated. These expressions have provided an analytical means to quantify the PSRR and PS-IMD of PWM Class D amplifiers (designed on the basis of the proposed method).

In Chapter 4, the power-efficiency of the Bang-Bang control Class D amplifier has been investigated, and on the basis of this investigation, the Bang-Bang control Class D amplifier has been proposed as a viable alternative to the prevalent PWM Class D amplifier for power-critical low-voltage applications, including hearing instruments.

The power-efficiency of the Bang-Bang control Class D amplifier has been compared against its PWM Class D amplifier counterpart. It has been shown that the former features a significant power-efficiency advantage over the latter for power-critical low-voltage applications.

Several non-linearities of the Bang-Bang control Class D amplifier have been investigated and the associated analytical expressions derived. These non-linearities included the input signal-related non-linearity (the THD) and the power supply-related non-linearities (the PSRR and PS-IMD). The investigations herein included an investigation of the abovementioned non-linearities of an ideal (i.e. all building blocks are ideal) Bang-Bang control Class D amplifier, and an investigation of the effects of two major practical non-idealities (the propagation delay of the Bang-Bang controller and the output impedance of the Class D output stage of a practical Bang-Bang control Class D amplifier) on these non-linearities.

The non-linearities of the Bang-Bang control Class D amplifier have been compared against the PWM Class D amplifier. It has been shown that in most cases, the former features lower non-linearities for power-critical low-voltage applications (including hearing instruments).

In Chapter 5, the power-efficiency and power dissipation of filterless Class D amplifiers based on two architectures, the 3-state architecture and the conventional architecture, have been investigated. This investigation included the derivation of analytical expressions for the power dissipation in the loudspeaker due to the attenuation of high frequency components and for the power-efficiency of the two filterless Class D amplifier architectures. These expressions have provided an analytical means to quantify the actual (vis-à-vis empirical) rating and the required intrinsic inductance of the loudspeaker. A high frequency loudspeaker model (20kHz – 1MHz) has been proposed.

On the basis of the investigation of the power-efficiency and power dissipation of the filterless Class D amplifiers based on the two abovementioned architectures, it has been shown that if certain conditions are satisfied, the conventional architecture can indeed be employed as filterless Class D amplifiers and yet their power-efficiency can be comparable to that of 3-state filterless Class D amplifiers.

As an overall conclusion, the work delineated in this thesis is significant to the analog Class D amplifier literature. Specifically, the work herein provides useful insight to analog Class D amplifier designers on the mechanisms of the pertinent non-linearities and of power-efficiency, and analytical means on how various circuit parameters of Class D amplifiers may be varied to meet a given set of pertinent design specifications.

6.2 Recommendations for Future Work

On the basis of the literature review and investigations in this research program, the following further work is recommended:

- (i) Investigation into design of Bang-Bang control Class D amplifiers with low non-linearities without requiring a high switching frequency.

Although the THD of Bang-Bang control Class D amplifiers has been shown to be sufficient ($\sim 0.2\%$ at high modulation index) for general applications and exceed that required for hearing instruments, a lower THD attribute is always attractive, for example, $\text{THD} < 0.01\%$ at high modulation index. It has been shown in Chapter 4 that a higher switching frequency results in lower non-linearities. However, increasing the switching frequency results in increased power dissipation (hence lower power-efficiency) and this somewhat defeats the low power attribute of the Bang-Bang control Class D amplifier.

In view of this, a recommendation for further work is an investigation into the design of a novel Bang-Bang control Class D amplifier with low non-linearities without requiring a high switching frequency.

- (ii) Further to (i), it would be interesting to investigate the use of a variable hysteresis comparator (whose hysteresis varies according to the magnitude of the input signal) as the Bang-Bang controller. Intuitively, it may then be possible that the ensuing THD generated due to normal Bang-Bang controller can be compensated by the variations of the hysteresis of the variable hysteresis comparator.

- (iii) Investigation into the mechanisms of non-linearities of practical sigma-delta Class D amplifiers and self-oscillating Class D amplifiers.

The literature review in Chapter 2 showed that the mechanisms of the non-linearities (including THD, IMD, PSRR and PS-IMD) of practical sigma-delta Class D amplifiers and self-oscillating Class D amplifiers are unestablished – although sigma-delta Class D amplifiers feature relatively lower non-linearities (compared to PWM Class D amplifiers).

In view of this, it would be interesting to investigate the mechanisms of non-linearities of practical sigma-delta and self-oscillating Class D amplifiers.

- (iv) Investigation into optimization of power-efficiency of filterless Class D amplifiers.

The investigation in Chapter 5 showed that a high switching frequency results in reduced power dissipation (due to the attenuation of high frequency components) in the loudspeaker but at the cost of increased power dissipation in the output stage.

It would be interesting to investigate the optimization of the power-efficiency, taking into consideration both the power dissipation of Class D amplifier and the power dissipation in the loudspeaker due to the attenuation of high frequency components therein.

Author's Publications

Journal Publications

- [1] T. Ge and J. S. Chang, "Bang-Bang Control Class D Amplifiers: Total Harmonic Distortion and Supply Noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Accepted, 2008.
- [2] T. Ge and J. S. Chang, "Bang-Bang Control Class D Amplifiers: Power Supply Noise," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, Accepted, 2008.
- [3] T. Ge and J. S. Chang, "Modeling and Technique to Improve PSRR and PS-IMD in Analog PWM Class D Amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, pp. 512-516, Jun 2008.
- [4] T. Ge and J. S. Chang, "Filterless Class D Amplifiers: Power-Efficiency and Power Dissipation," *IET Circuits, Devices and Systems*, Accepted, 2009.

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Appendix A: Derivation of Eqns. (4.1) – (4.5)

Derivation of the output signal of the ‘ideal’ Bang-Bang amplifier

Based on Figure 4-1 and Taylor series, t_{on} (the period when $V_{out}=V_{DD}$) and t_{off} (the period when $V_{out}=-V_{DD}$) of the ‘ideal’ Bang-Bang amplifier are derived as eqns. (A.1) and (A.2), where V_{DD} and $-V_{DD}$ are the positive and negative power supplies of the Bang-Bang amplifier.

$$\begin{aligned}
 t_{on} &= \frac{1}{\omega_p} \ln \left[\frac{V_{DD}(1-m) + V_h(1+G)}{V_{DD}(1-m) - V_h(1+G)} \right] \\
 &\approx \frac{2}{\omega_p} \frac{(1+G)h}{1-m} + \frac{2}{\omega_p} \frac{[(1+G)h]^3}{3(1-m)^3}
 \end{aligned} \tag{A.1}$$

$$\begin{aligned}
 t_{off} &= \frac{1}{\omega_p} \ln \left[\frac{V_{DD}(1+m) + V_h(1+G)}{V_{DD}(1+m) - V_h(1+G)} \right] \\
 &\approx \frac{2}{\omega_p} \frac{(1+G)h}{1+m} + \frac{2}{\omega_p} \frac{[(1+G)h]^3}{3(1+m)^3}
 \end{aligned} \tag{A.2}$$

where m (eqn. (A.3)) is the desired output signal normalized with respect to the power supply V_{DD} ,

$\omega_p = [(R_{in}/R_{fb})C]^{-1}$ is the corner frequency of the RC feedback network,

$h = V_h/V_{DD}$ the normalized hysteresis of the Bang-Bang controller, and

$G = R_{fb}/R_{in}$ the closed-loop gain of the Bang-Bang amplifier.

Appendix A: Derivation of Eqns. (4.1)-(4.5)

$$m = -\frac{R_{fb} V_{in}}{R_{in} V_{DD}} = M \sin(\omega_{in} t) \quad (A.3)$$

where M is the modulation index, and

ω_{in} is the input frequency in rad/s.

Based on eqns. (A.1)-(A.3) and Figure 4-1, the normalized output signal can be derived as:

$$\frac{V_{output_ideal}}{V_{DD}} = \frac{t_{on} - t_{off}}{t_{on} + t_{off}} = m + V_{THD_ideal} \quad (A.4)$$

where

$$V_{THD_ideal} = \frac{2[(1+G)h]^2}{3} \frac{m}{1-m^2} k(\omega_{Dis}) \quad (A.5)$$

where $k(\omega_{Dis})$ is a frequency-related parameter and ω_{Dis} is the frequency of the harmonic distortion component.

$$k(\omega_{Dis}) = \left| 1 + j \frac{\omega_{Dist}}{\omega_p} \right| \quad (A.6)$$

$$H_{LPF}(\omega_{Dis}) = \frac{1}{1 + \frac{L_L}{R_L} \omega_{Dist} j - L_L C_L [\omega_{Dist}]^2} \quad (A.7)$$

Based on Trigonometric functions and eqns. (A.3) and (A.7),

$\frac{m}{1-m^2} k(\omega_{Dis}) H_{LPF}(\omega_{Dis})$ can be expressed as:

Appendix A: Derivation of Eqns. (4.1)-(4.5)

$$\begin{aligned}
& \frac{m}{1-m^2} k(\omega_{Dis}) H_{LPF}(\omega_{Dis}) \\
&= \sum_{n=1}^{\infty} m^{2n-1} k(\omega_{Dis}) H_{LPF}(\omega_{Dis}) \\
&= \sum_{n=1}^{\infty} (M \sin(\omega_{in} t))^{2n-1} k(\omega_{Dis}) H_{LPF}(\omega_{Dis}) \\
&= \sum_{n=1}^{\infty} \sum_{p=2}^n \left[\frac{M^{2n-2} \frac{(-1)^{p-1}}{2^{2n-2}} \binom{2n}{n-p} M \cdot \sin((2p-1)\omega_{in} t) k((2p-1)\omega_{in} t)}{1 + \frac{L_L}{R_L} (2p-1)\omega_{in} j - L_L C_L [(2p-1)\omega_{in}]^2} \right] \quad (A.8) \\
&= \sum_{p=2}^{\infty} \sum_{n=p}^{\infty} \left[\frac{M^{2n-2} \frac{(-1)^{p-1}}{2^{2n-2}} \binom{2n}{n-p} M \cdot \sin((2p-1)\omega_{in} t) k((2p-1)\omega_{in} t)}{1 + \frac{L_L}{R_L} (2p-1)\omega_{in} j - L_L C_L [(2p-1)\omega_{in}]^2} \right]
\end{aligned}$$

Substituting eqn. (A.8) into eqns. (A.4) and (A.5), eqns. (A.4) and (A.5) can be re-expressed as eqns. (4.1) – (4.5) in Chapter 4.

Appendix B: Measurements on 10 Loudspeakers

To show the validity of the extended model for loudspeaker in the high frequency range and the suggested procedure, the resistance $R_L(\omega)$ and reactance $X_L(\omega)$ of 10 loudspeakers obtained from the high frequency model are compared against measured data in Figures A(i) - (x). The 10 loudspeakers and their high frequency models are tabulated in Table A below.

TABLE A LOUDSPEAKERS AND THEIR HIGH FREQUENCY MODELS

Loudspeaker	High frequency model
Visaton SC 5.9	$Z_{L(HF)}(\omega) = 26.2 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.66} + j38.9 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.57}$ (B.1)
Visaton FR10	$Z_{L(HF)}(\omega) = 34.2 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.70} + j57.0 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.64}$ (B.2)
Visaton FRWS5	$Z_{L(HF)}(\omega) = 19.6 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.72} + j34.4 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.63}$ (B.3)
Visaton 2918	$Z_{L(HF)}(\omega) = 20.2 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.75} + j40.8 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.69}$ (B.4)
Audio design services YDT 813-6	$Z_{L(HF)}(\omega) = 36.3 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.78} + j61.5 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.66}$ (B.5)

Appendix B: Measurements on 10 loudspeakers

Eurotec

$$\text{International: } Z_{L(HF)}(\omega) = 63.1 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.70} + j94.0 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.65} \quad (\text{B.6})$$

59-P12.00-01F

Eurotec

$$\text{International: } Z_{L(HF)}(\omega) = 36.2 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.68} + j56.4 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.61} \quad (\text{B.7})$$

59-F20.00-01F

Eurotec

$$\text{International: } Z_{L(HF)}(\omega) = 9.10 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.75} + j15.4 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.58} \quad (\text{B.8})$$

59-F129.CX-

OOF

$$\text{Unbranded } Z_{L(HF)}(\omega) = 20.1 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.72} + j30.3 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.57} \quad (\text{B.9})$$

$$\text{Unbranded } Z_{L(HF)}(\omega) = 24.2 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.73} + j41.7 \left(\frac{\omega}{2\pi \cdot 150\text{kHz}} \right)^{0.64} \quad (\text{B.10})$$

Appendix B: Measurements on 10 loudspeakers

(i) Visaton SC 5.9

(ii) Visaton FR10

Appendix B: Measurements on 10 loudspeakers

(iii) Visaton FRWS5

(iv) Visaton 2918

Appendix B: Measurements on 10 loudspeakers

(v) Audio design services YDT 813-6

(vi) Eurotec International: 59-P12.00-01F

Appendix B: Measurements on 10 loudspeakers

(vii) Eurotec International: 59-F20.00-01F

(viii) Eurotec International: 59-F129.CX-OOF

Appendix B: Measurements on 10 loudspeakers

(ix) Unbranded

(x) Unbranded

Figure A (i) - (x) R_L and X_L of 10 loudspeakers