Heteroepitaxial growth and characterization of III-V compound semiconductor on silicon

Hendrix Tanoto

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HETEROEPITAXIAL GROWTH AND CHARACTERIZATION OF III-V COMPOUND SEMICONDUCTOR ON SILICON

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School of Electrical & Electronic Engineering

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Doctor of Philosophy

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Summary

With the number of transistors in a Si IC chip passing the 2 billion mark, there are tremendous ongoing efforts to connect all these devices and make them function. Nonetheless, the RC time delay and power loss in the current copper interconnects have become a major impediment to improving IC performance. On the other hand, optical interconnect offers much higher speed and much larger bandwidth over copper interconnects and could potentially revolutionize the IC performance if successfully implemented. However, realization of optical interconnect's key component, the light-emitter, on a Si substrate is difficult as Si is an indirect bandgap material that does not efficiently generate photons. On the other hand, high-performance InAs quantum dot (QD) light-emitters are routinely demonstrated on GaAs substrates. This thesis presents systematic studies on monolithic heteroepitaxial integration of III-V compound semiconductor QD-based light-emitters on a Si substrate employing a graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer.

Firstly, the benefits of the migration enhanced epitaxy (MEE) growth technique for GaAs/Ge growth were investigated. Atomic force microscope (AFM) root-mean square (RMS) surface roughness is four times lower on the GaAs surface with the MEE nucleation process due to two-dimensional growth mode. Consistent with the surface roughness data, a 40% reduction in the full-width at half-maximum (FWHM) of the X-ray diffraction (XRD) spectrum was seen in the MEE-nucleated GaAs sample, indicating significant improvement in the crystalline quality. Further studies revealed that low temperature (250°C) initial GaAs nucleation on a vicinal Ge surface by MEE ensures complete As dimer coverage on the double-atomic step Ge surface and a two-dimensional growth mode.

Anti phase boundaries (APB)-free GaAs layer was realized on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate by employing GaAs initiation by MEE at 250°C . To investigate the performance of InAs QD light-emitters on the integrated platform, several investigations were carried out. First, $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ capping layer was shown to reduce strain around the InAs QD structures leading to realization of large and defect-free QD structures grown on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The InAs QD structures capped with an $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ layer were found to have a slower thermal quenching rate as compared to the ones capped with a GaAs layer due to the absence of V-shaped defects. A dense ($7 \times 10^{10} \text{ cm}^{-2}$) InAs QD ensemble was achieved on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate using alternate beam MBE. When the InAs monolayer coverage was 2.9 ML, $1.3 \mu\text{m}$ room-temperature (RT) PL emission was achieved.

Finally, the characteristics of an InAs QD LED grown on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate were investigated. Cross-sectional TEM analysis revealed the InAs QDs take on a lens shaped structure with average base width and height of $29 \pm 3 \text{ nm}$ and $6.7 \pm 0.8 \text{ nm}$, respectively. The LED exhibits a turn-on voltage $\sim 0.8 \text{ V}$, with diode ideality factor n of 2.4 and emits at a peak wavelength of $1.29 \mu\text{m}$ at room temperature. The maximum optical output power from the device is $20 \mu\text{W}$, which translates to power per unit area of 7.6 mW.cm^{-2} . The external efficiency, η_{ext} , reduces from 0.1 % to 0.00 8% following increase in injection current.

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List of Abbreviations

AFM	-	Atomic Force Microscope
APB	-	Anti-phase Boundaries
DI water	-	De-ionized water
IC	-	Integrated Circuit
IPA	-	Isopropyl Alcohol
MBE	-	Molecular Beam Epitaxy
MEE	-	Migration Enhanced Epitaxy
PL	-	Photoluminescence
QD	-	Quantum Dot
RHEED	-	Reflection High Energy Electron Diffraction
SEM	-	Scanning Electron Microscope
TDD	-	Threading Dislocation Density
TEM	-	Transmission Electron Microscope
XRD	-	X-ray Diffraction

Chapter 1 Introduction

1.1 Background and motivations

Historically, germanium (Ge) was the original material of choice for the solid-state transistor, the key device in today's integrated circuits (IC). In the 1940s, the Ge crystal was the only available crystal with high enough purity for such an application. Hence, the first solid-state transistor developed in Bell Labs was made of Ge. Soon after the availability of pure Si crystals, Si transistors were demonstrated [1]. Thanks to its larger bandgap, Si transistors operated more reliably at elevated temperature compared to Ge ones. Nevertheless, when Jack Kilby of Texas Instrument (TI) first built an IC in the form of a phase-shift oscillator in 1958, he still used Ge rather than Si because he could not find suitable Si crystals. The first Si IC came from Robert Noyce of Fairchild Semiconductors in the following year [2], demonstrating a method of making an IC using a Si planar process. Following the invention by Noyce, silicon's other major advantage was unveiled, in the form of stable and high-quality native oxide on its surfaces which can be readily employed to form circuit isolation layers and dielectric gate barriers. This leads to reliable methods of producing good-quality SiO_2 on the complementary metal-oxide-semiconductor (CMOS) devices which in turn simplifies the planar IC manufacturing process tremendously.

Today, silicon's highly developed manufacturing process and design technologies allow production of inexpensive-large-area substrates and exponential-rate of miniaturization of the transistors. Since the transistors inside an IC chip function as binary switches, the smaller they are the faster they become. Intense efforts in making

the transistor as small as possible are prompted by the relationship of the transistor speed as function of its dimension, as depicted by the relationship [3]:

$$I_{drive} \sim \left(\frac{\mu \times C_{ox} \times (W / L)}{2} \right) \times (V_{gs} - V_t)^2 \quad (1-1)$$

where I_{drive} = MOS current in saturation, μ = carrier mobility, C_{ox} = gate capacitance, W = gate width, L = gate length, V_{gs} = voltage from gate to source, and V_t = threshold voltage. To increase the drive current, and consequently improve the device's speed, the common method is to reduce the gate length and increase the gate capacitance. This means shrinking the gate length and thinning down the gate oxide thickness, respectively. However, there are limits as to how small one could shrink the transistors size, namely lithography limitations and gate oxide current leakage limitations. An alternative method to improve the device speed is to increase the carrier mobility. However, silicon's low carrier mobility as compared to, for example Ge and InSb, acts as an upper bound for the transistor switching speed. This is the first fundamental limit of Si.

Another factor that limits the IC performance is the matter of interconnects [4]. It starts to limit the performance of Si ICs when physical gate length of the transistor enters sub-100nm. With the number of transistors-per-chip passing the 2 billion mark [5], there is no doubt that there are tremendous ongoing efforts in the copper interconnects technology to connect all these devices and make them function. Nevertheless, crosstalk between neighbouring circuits, coupled with increasing RC signal delays and thermal loss in the current copper interconnects have become a major impediment to improving the IC performances. Even employing the most optimistic estimates for conductor resistivity and dielectric permittivity, it is extremely challenging to reach the IC performances targeted in the International Technology Roadmap for

Semiconductors (ITRS) [6]. Therefore, a drastically different approach is required in the interconnect technology.

One promising approach is the incorporation of high-speed optical interconnects on future Si ICs, where copper lines are replaced by optical waveguides and photons are used to transfer data from chip-to-chip or from block-to-block inside a chip. As information is transferred by photons, optical interconnects promise crosstalk-free data paths with dramatic increase in the data transfer rate from copper interconnect. The improvements in the data transfer rate offered by optical interconnect on Si ICs are essentially the same as the improvements brought about by fiber optic technology that replaced much of the copper lines in the telecommunication networks. Fiber optics offer up to 40 Gb/s bandwidth and are capable of serving up to 32,000 discrete frequency channels [7]. In short, fiber optic cables offer over 1,000 times as much bandwidth as copper lines. Beside the speed and bandwidth advantages, other attractive benefits of optical interconnects would be an improved temperature resistance, better power-efficiency and immunity to electromagnetic noise. A successful integration of optical interconnects into the established Si ICs manufacturing infrastructure promises to deliver ICs with revolutionary performances. A cartoon drawing of what future ICs with optical interconnects might look like is shown in Fig. 1-1.

Figure 1-1 An artist's impression of a future IC incorporating optical interconnects.

Integration of the key active component in optical interconnects, light emitters, into the Si ICs manufacturing infrastructure is tricky. First and foremost, Si has an indirect-bandgap, which makes it unable to efficiently generate photons for light-emitting device applications. This is the second fundamental limit of Si. Although some progress has been made in realizing Si-based light emitters [8-10], they still require much advancement to reach the performance level required to realize highly-efficient and high-speed operation. On the other hand, many III-V compound semiconductor alloys have a direct-bandgap and efficiently generate photons following carrier relaxations. Alloys of III-V compound semiconductors, such as GaAs, InP, and GaN are used in various important light-emitting devices. High-brightness light-emitting diodes (LED) for high-efficiency and long-lasting lighting applications are made of GaN alloys. Meanwhile, high-speed semiconductor lasers which drive modern fiber optic telecommunications circuits are mostly made of GaAs alloys and InP alloys.

Cost-effective integration of suitable III-V compound semiconductor light-emitting devices into Si IC manufacturing lines would offer high-speed calculation, ultra-large scale integration, and the low cost of present Si IC technology together with

the fast data transfer rate of III-V compound semiconductor optoelectronics. Undoubtedly, the impact of such integration is remarkable and naturally has attracted intense efforts in the course of more than 20 years to realize practical and reliable methods for such integration [11]. Some degree of success in the integration efforts has been reported, which employed laser diode chiplets [12] and other hybrid integration techniques [13, 14]. However, these techniques do not demonstrate commercially viable III-V semiconductor optoelectronic on Si platform integration. Monolithic integration, involving heteroepitaxial growth of III-V compound semiconductors on Si substrate will remain the most promising technique for eventual realization of commercial wafer-scale integration; only this integration technique can be readily incorporated into the mature Si IC manufacturing infrastructure. Another major advantage of monolithic integration is the potential of realizing more affordable advanced devices, such as high-speed CMOS [3, 15] or high-performance heterojunction bipolar transistor (HBT), using device-quality III-V compound semiconductor heteroepitaxially grown on economical large-area Si wafer. Lastly, the monolithic heteroepitaxial integration adheres to the planar integration spirit, the same spirit leading to the IC invention itself.

For optical interconnect application, light-emitting devices operating at either one of the three minimal attenuation windows of an optical fiber (0.85 μm , 1.3 μm or 1.55 μm) is preferred. To obtain 1.3 μm or 1.55 μm emission, light-emitting devices made of GaAs and InP alloys can be employed. Currently, most commercially available light-emitting devices emitting at 1.3 μm or 1.55 μm are InP-based. However, for the purpose of integration into Si, GaAs has clear advantages compared to InP in terms of its economical value and its smaller lattice constant mismatch with Si as can be observed from Fig. 1-2. Nonetheless, direct GaAs heteroepitaxy on Si is still extremely challenging due to the substantial lattice and thermal expansion mismatch between

GaAs and Si. Moreover, the difference in the symmetry of their crystalline structure gives rise to the anti-phase boundary (APB) defects. The ~4% lattice mismatch creates misfit dislocations at the GaAs/Si interface and eventually results in threading dislocations (TD) at the GaAs surface. Through intense efforts, the TD density (TDD) on GaAs layers grown on Si can be reduced to $\sim 10^8 \text{ cm}^{-2}$ [16], but this TDD value is still too high for light-emitting devices that operate based on minority carrier injection. Furthermore, the ~110 % thermal expansion mismatch produces cracks in the GaAs layer grown on Si during substrate cooling. Cracks can act as scattering centers for light propagation, can act as resistance to horizontal electrical current flow, and can lead to electrical shorting in vertical current flow [17]. Hence, while direct growth of GaAs on Si is obviously preferred, the material incompatibilities described earlier make it very difficult to achieve this.

Figure 1-2 Plots of bandgap (wavelength) vs. lattice constant of selected semiconductor materials.

Given the above motivations and challenges, a solution for eventually integrating GaAs with Si is to have an intermediate step whereby the GaAs is first grown on an intermediary buffer layer on Si substrate. There have been constant efforts in realizing a

good quality intermediary buffer layers on Si for this purpose. The intermediary layer serves to accommodate both lattice mismatch and thermal expansion difference between GaAs and Si. Amongst the proposed buffer layers [18-20], Ge is the most promising one. Ge is an ideal intermediary material between GaAs and Si because of its closely matched lattice constant and thermal expansion coefficient with GaAs and its complete miscibility with Si. Using a compositionally graded buffer layer, $\text{Si}_{1-x}\text{Ge}_x$, with $x = 0$ to 1, the lattice mismatch strain from Si to Ge is effectively relaxed without increasing surface threading dislocation densities (TDD) on the final pure Ge top layer [21-23]. Surface TDD of $7.4 \times 10^5 \text{ cm}^{-2}$ on this platform has been measured *via* plan-view transmission electron microscopy (TEM) [24]. Furthermore, the use of slightly misoriented (100) Ge surface promises an APB-free GaAs layer [25]. On a side note, the invention of relaxed SiGe buffer layers also serves another purpose, which is the realization of strained Si or Ge high-mobility MOS field-effect-transistors (MOSFET) [3, 26-28].

GaAs-based light-emitting devices have been attempted either directly on Si [29-31] or through some intermediate buffer layers [32-35], but there is yet a successful demonstration of light-emitting devices operating at 1.3 μm on Si substrates. For a start, it is more challenging to realize light-emitting devices operating at 1.3 μm on GaAs than on InP. As shown in Fig. 1-2, the III-V compound semiconductors alloys with the required bandgap energy have much larger lattice constant than GaAs. Therefore, when these alloys are deposited on GaAs, two scenarios might occur. First, the film is strained when the deposited thickness is below a certain critical thickness, h_c . The h_c itself is largely dependent on the lattice mismatch value between the film and the GaAs substrate; larger mismatch means smaller h_c . When the deposited film thickness exceeds h_c , the film starts to relax usually through misfit dislocations formation [36]. These

dislocations typically act as non-radiative recombination centres, detrimental to the light-emitting devices performances and lifetime. Therefore, a strained film below h_c is preferred to a dislocated film above h_c . Indeed, a strained-layer structure such as a strained quantum well (QW) and strained nanostructures such as self-assembled quantum dots (QD) are widely used in light-emitter active regions. The effects of strain must be considered carefully as it alters the bandgap of the film, hence changing its emission wavelength. This brings about flexibility in tailoring the emission wavelength to suit a particular application but also another complication in the active layer design.

Figure 1-3 shows an example of the effects of strain on the band structure of $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer. For $\text{In}_x\text{Ga}_{1-x}\text{As}$ QW grown pseudomorphically on a GaAs substrate, it will be under compressive strain and will exhibit larger effective bandgap, E_g , as compared to an $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer under no strain. Therefore, to realize 1.3 μm emission, high In-content and highly-strained $\text{In}_x\text{Ga}_{1-x}\text{As}$ QW needs to be grown on a GaAs substrate. However, this is challenging as excessive strain might cause misfit dislocations to occur. Another factor needs to be taken into account when growing a strained-layer QW on heteroepitaxial GaAs layer grown on Si. Such heteroepitaxial GaAs layers understandably contain more defects and dislocations compared to a homoepitaxial GaAs layer. Therefore, it is desirable to employ a more defect-resistant active region compared to the strained-QW layer. This might be achieved using self-assembled QD structures [37].

Figure 1-3 The energy-band structure in the momentum space for $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer under (a) biaxial tension, (b) lattice-matched condition, and (c) biaxial compression.

Self-assembled QD structures have attracted intense research effort due to their unique physical properties arising from the three-dimensional quantum confinement of carriers and delta-like density of states [38, 39], as illustrated in Fig. 1-4. Self-assembled QD structures generate large strain fields around the surrounding materials, underneath and around the dots. These large strain fields could be used as dislocation bending and defect filtering mechanisms, similar to the use of strained-layer superlattices. Although such structures were initially demonstrated on III-V compound semiconductor systems, there are currently intense parallel research efforts in Ge and Si QD structures for 1.3 μm emission [40] on Si substrates. However, no one has yet to demonstrate room-temperature operation from devices utilizing such structures. On the

other hand, InAs/GaAs self-assembled QD structures are promising candidates for 1.3 μm emission and to act as the active region in the light-emitting devices grown on Si substrates. Integration of high-quality QD light emitting devices operating at 1.3 μm on Si substrates constitutes a critical step towards the realization of optical interconnects on Si [41].

Figure 1-4 Density of states (DOS) characteristics as confinement of carriers increases from bulk semiconductor to QD structures (left to right).

1.2 Objectives and major contributions of the Thesis

The paramount goal of this thesis is to demonstrate III-V compound semiconductor QD-based light emitting device on a Si substrate through the exploitation of a graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer. The graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer effectively controls the nucleation of dislocations producing low TDD on the final pure Ge layer which act as GaAs nucleation surface. The low TDD is critical for realization of high-performance and reliable light-emitting devices. Nevertheless, obtaining APB-free GaAs layer on the final pure Ge surface of the graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer is the crucial first step to realize vast arrays of high-performance III-V compound semiconductor devices on Si

substrates. In order to accomplish the main goal of the thesis, the following systematic studies were performed.

First, the effects of MEE on the quality of the GaAs layer grown on nominal (100) Ge surface were investigated. Two samples with and without a MEE-nucleated 10 ML-thick GaAs on nominal (100) Ge/Si substrate were compared. Scanning electron microscope (SEM) and atomic force microscope (AFM) measurements show that significant island-like formation occurred at the GaAs surface in the sample grown without the MEE-nucleated GaAs layer due to three-dimensional growth. On the other hand, the GaAs surface in the sample grown with the MEE nucleation process show four times lower AFM root-mean square (RMS) surface roughness, 9 nm vs. 37 nm, due to two-dimensional growth. Consistent with the surface roughness data, a 40% reduction in the full-width at half-maximum (FWHM) of the x-ray diffraction (XRD) spectrum, 160 arcsec vs. 280 arcsec, was seen in the MEE-nucleated GaAs sample, indicating significant improvement in the crystalline quality. As a result of the two-dimensional growth, the higher-strained layer in the sample grown with the MEE-nucleated GaAs layer exhibits early relaxation. Due to the larger strain along the [100] and [010] directions, the photoluminescence (PL) peak energy of the InGaAs quantum well in this sample exhibits a blue shift compared to the sample grown without the MEE-nucleated GaAs layer.

Secondly, study on the APB propagation mechanism on a nominal (100) Ge surface and misoriented (100) Ge surface was performed. In the GaAs layer grown on misoriented (100) Ge surface, the APB propagation directions were in a higher index plane, with a smaller angle with respect to the GaAs/Ge interface. On the other hand, in the GaAs layer grown on a nominal (100) surface, the APB propagates on the (110) plane perpendicular to the GaAs/Ge interface. Therefore, the APB on a nominal Ge

surface is less likely to self-annihilate compared to the ones on misoriented (100) Ge surface. However, in GaAs layers on a nominal (100) Ge surface, APB with lower energy might change their propagation direction, from the initial (110) plane to less energetic higher index planes, such as the (112) plane and self-annihilate one another.

Thirdly, the effects of low-temperature MEE to totally suppress APB formation in GaAs/Ge heteroepitaxy were investigated. It was found that employing an offcut Ge surface alone is not sufficient; instead, it has to be complemented by a properly chosen low temperature MEE growth initial nucleation. This is to ensure complete As dimers coverage on the double-atomic step Ge surface and to ensure that the growth mode lies within a two-dimensional growth mode by limiting Ga adatom migration onto the step-edges and kinks. Surface roughness as measured by AFM was reduced by 10 times in the sample grown with MEE at a substrate temperature of 250°C, the lowest in this experiment, while the InGaAs SQW PL integrated intensity improved by two orders of magnitude. Comparison of PL emission from InGaAs SQWs in samples with the MEE performed at 450°C and 250°C revealed a shift in the PL emission wavelength, and is attributed to the indium out-diffusion mechanism and dislocation-induced strain. Moreover, comparison with a sample with the same structures grown on a GaAs substrate demonstrated that the quality of the GaAs layer grown on Ge substrate is comparable to homoepitaxial GaAs, and further improvements of the heteroepitaxial GaAs can be expected.

Fourthly, the optimized growth conditions leading to APB-free GaAs on misoriented Ge substrate were employed to realize good quality GaAs layers on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates. There are several factors that need to be taken into account especially in terms of thermal conductivity difference between a Ge substrate and the Si-based one. Nevertheless, the transision from Ge substrate to graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$

substrate was found to be seamless; this indicates the success of the $\text{Si}_{1-x}\text{Ge}_x$ buffer technology in realizing a ‘virtual’ Ge substrate. To check the viability of this platform, a minority carrier device in the form of an AlGaAs/GaAs heterojunction bipolar transistor (HBT) with emitter area of $\sim 1.6 \times 10^{-5} \text{ cm}^2$ was realized on this platform. The AlGaAs/GaAs HBT on graded SiGe/Si exhibited a maximum current gain (β) of ~ 40 , which is large enough for microwave applications. The RF performance of the device was investigated and the cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) are 20 GHz and 13 GHz, respectively for a $2 \times 15 \text{ }\mu\text{m}^2$ emitter area device. The f_{max} value is compromised by the thin base layer (45 nm, 10^{19} cm^{-3} Be-doped) used in the HBT. This could be improved if the base doping level is increased by using carbon as the p-type dopant. Compared to a similar device grown on a GaAs substrate, the f_t value is lower due to higher emitter contact resistance, which can be improved by increasing the In composition in the emitter cap layer and optimizing the contact annealing condition.

Fifthly, upon successful demonstration of an AlGaAs/GaAs HBT, growth of self-assembled InAs QD structures was performed. The effectiveness of an $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ capping layer to reduce strain around the InAs QDs grown on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate was demonstrated. The InAs QD structures capped with an $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ layer were found to have slower thermal quenching rate as compared to the ones capped with GaAs layer due to the absence of V-shaped defects. A dense ($7 \times 10^{10} \text{ cm}^{-2}$) InAs QD ensemble was achieved on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate using alternate beam MBE. The InAs QDs are at least two times larger and have smaller aspect ratio compared to typical InAs QDs on GaAs substrates. When InAs θ_c was 2.9 ML, 1.3 μm RT PL emission was achieved with PL FWHM of 65 nm. However, at this θ_c , optically-inactive large InAs dots/islands ($>80 \text{ nm}$) occur alongside optically-active smaller InAs

QDs. Hence, although the size variation of optically-active QDs is smaller, as deduced from the narrowing of the PL FWHM compared to samples with different θ_c , the integrated PL intensity drops significantly due to the optically-inactive large islands observed in this sample.

Finally, the characteristics of InAs QD LEDs grown on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate were investigated. Cross-sectional TEM analysis revealed the InAs QDs take on a lens shaped structure with average base width and height of 29 ± 3 nm and 6.7 ± 0.8 nm, respectively. This translates to QD structures with aspect ratio of 0.23 ± 0.05 . The LED exhibits a turn-on voltage ~ 0.8 V, with diode ideality factor n of 2.4 and emits at a peak wavelength of 1.29 μm at room temperature. The maximum optical output power from the device is 20 μW , which translates to power per unit area of 7.6 mW.cm^{-2} . The external efficiency, η_{ext} , reduces from 0.1 % to 0.008 % following increase in injection current. Various carrier recombination processes which reduce the external efficiency, η_{ext} , were identified from analysis of the current-optical power relationship.

1.3 Organization of the Thesis

The background and motivation of the thesis are presented in this chapter, followed by the thesis' goals and major contributions. In chapter 2, theoretical background and literature survey of the topics covered by this thesis are presented. They are on the heteroepitaxial growth of GaAs on Si substrates, molecular beam epitaxy (MBE) and migration-enhanced epitaxy (MEE) growth technique, and self-assembled quantum dot (QD) structures. Chapter 2 ends with brief overview of some important characterization techniques employed in this thesis. Chapter 3 and chapter 4 discuss the experimental studies to achieve device-quality GaAs layer on Ge surface. The experiments started with studies on the effects of MEE to the quality of GaAs layer

grown on nominal (100) Ge surface. This is promptly followed by studies on the effects of Ge surface misorientation and the effects of low-temperature MEE to anti-phase boundary (APB) propagation mechanisms and suppression in chapter 4. In chapters 5 to 7, growth of GaAs on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate is studied. In chapter 5, the optimized GaAs/Ge growth conditions achieved in chapter 4 are employed to realize good quality GaAs layer on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate, followed by an investigation on the characteristics of AlGaAs/GaAs HBT grown on this platform. In chapter 6, the required conditions for high areal-density defect-free InAs QD structures on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate are presented. In chapter 7, characteristics of InAs QD-based LED on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate emitting at $1.29\mu\text{m}$ are discussed. Finally, conclusions and recommendations for future research are presented in chapter 8.

Chapter 2 Theoretical Background and Literature Reviews

2.1 Heteroepitaxial growth of GaAs on Si substrate

2.1.1 Challenges

As briefly mentioned in the previous chapter, direct monolithic integration of III-V compound semiconductors on Si faces numerous challenges. In the case of GaAs and Si, three major material incompatibilities, namely large lattice mismatch ($\sim 4\%$), large difference in thermal expansion coefficient ($\sim 110\%$), and anti-phase boundaries (APB) prevent realization of a device-quality GaAs layer on Si. Table 2-1 shows the Si and GaAs material properties to illustrate the incompatibilities described above. Heteroepitaxial growth of two dissimilar materials may proceed in mainly three ways, as illustrated in Fig. 2-1. For the case of two lattice-matched materials, the epitaxial growth proceeds according to the one illustrated in Fig. 2-1(a). An epitaxial film will grow almost perfectly as its lattice size matches the lattice size of the substrate. On the other hand, heteroepitaxial growth of lattice-mismatched materials might proceed as illustrated in Fig. 2-1(b) and Fig. 2-1(c). When the deposited film thickness is less than a particular critical thickness, h_c , a pseudomorphic strained layer occurs, as depicted in Fig. 2-1(c). Such a layer experiences elastic strain with its parallel lattice size following the substrate's lattice size and its perpendicular lattice size changes elastically. In this case, no misfit dislocations are formed in the grown film as the lattice mismatch is accommodated elastically by the crystal lattices. When the deposited film exceeds its critical thickness, misfit dislocations start to occur as a form of strain relaxation, as depicted in Fig. 2-1(b). In this case, a misfit dislocation in the form of a one-

dimensional line of broken atomic bonds at the film/substrate interface is formed and will extend linearly along the interface to terminate at a free surface of the crystal. In the nominal (100) surfaces, the $\{111\}\langle 110 \rangle$ slip system of the mismatched crystal will encourage misfit dislocations to propagate along the low-energy $[110]$ and $[1-10]$ directions.

Material	Group	Lattice Constant (Å)	Mismatch with GaAs (%)	Thermal expansion coeff (K ⁻¹)	Melting point (°C)	Thermal Conductivity (W/cm.K)
Si	IV	5.431	4.092	2.6×10 ⁻⁶	1412	1.3
GaAs	III-V	5.653	0	5.5×10 ⁻⁶	1240	0.6

Table 2-1 Compilation of Si and GaAs material properties.

Figure 2-1 Three scenarios of heteroepitaxial growth, (a) lattice matched, (b) lattice mismatch and above critical thickness, and (c) lattice mismatch and below critical thickness. The filled circles are atoms of deposited film while the empty circles are atoms of the substrate.

To predict the critical thickness of a heteroepitaxial layer, thermodynamic critical thickness models were proposed [36, 42-44]. Two basis for these models are mechanical equilibrium theory [36] and the energy balance theory [42, 43]. In the mechanical equilibrium theory, the critical thickness is reached when the force by the misfit stress balances the tension on the preexisting edge-type dislocation segments in the dislocation line. The critical thickness, h_c , predicted by this theory is given by the following expression.

$$h_c = \frac{b}{2\pi f} \frac{(1 - \nu \cos^2 \theta)}{(1 + \nu) \cos \lambda} \left(\ln \frac{h_c}{b} + 1 \right) \quad (2-1)$$

where f is the lattice mismatch, ν is the Poisson ratio, θ is the angle between the dislocation lines, b is the Burgers vector (~ 4 Å for GaAs substrate), and λ is the angle between the slip direction and the direction in the epilayer plane that is perpendicular to the line of intersection between the slip plane and the interface. This theory has demonstrated that edge-type dislocations provide a thermodynamically stable lower limit of experimental critical thickness.

In the energy balance theory [42, 43], the critical thickness h_c is reached when the areal energy density associated with a noninteracting screw-type dislocation overcomes the areal density of the strained heteroepitaxial layer. Then h_c is given by the following expression

$$h_c \cong \left(\frac{1 - \nu}{1 + \nu} \right) \left(\frac{1}{16\pi\sqrt{2}} \right) \left[\frac{b^2}{a} \right] \left[\left(\frac{1}{f^2} \right) \ln \left(\frac{h_c}{b} \right) \right] \quad (2-2)$$

where a is the heteroepitaxial film lattice constant. Employing this theory, it has been shown that the pure screw-type dislocation provides the thermodynamically metastable upper limit of experimental results. In the case of GaAs grown directly on Si, h_c was

found to be $\sim 20\text{-}40$ Å [45, 46]. This means misfit dislocations can form as soon as 10 monolayer (ML) of GaAs is deposited directly on the Si substrate.

As soon as dislocations are formed in the heteroepitaxial film, they might interact with one another. Threading dislocations are attracted or repelled by the strain fields of adjacent dislocations, and threading dislocations moving in a film during growth can group into large dislocation pileups [47]. In such a case, they are no longer effective in relieving misfit strain and more dislocations must be formed to relieve the remaining strain. Therefore, the total threading dislocation density (TDD) in a mismatched heteroepitaxial film could increase rapidly if dislocations interact and pin one another during growth. Such dislocation multiplication is the main culprit for the rapid rise in TDD with increasing lattice mismatch. Furthermore, threading dislocations might act as non-radiative recombination centers in optoelectronic devices as the localized mid-gap energy levels in their cores act as efficient trap states for injected minority carriers. These traps can significantly shorten the minority carrier lifetime in the material [48]. Reductions in minority carrier lifetime are especially detrimental for light-emitting devices, such as LEDs and lasers. In LEDs, the efficiency of the device will be reduced whenever minority carriers recombine non-radiatively. On the other hand, lasers will be affected more severely. If many of the injected minority carriers recombine non-radiatively before the local carrier densities necessary for population inversion are reached, no lasing operation would occur.

Apart from the lattice mismatch factor, there is also the large thermal expansion mismatch between GaAs and Si that could potentially induce cracks during growth thermal cycle. In the epitaxial growth of GaAs film on Si substrate, thermal mismatch strain as function of the temperature difference between the growth temperature and the ambient temperature (ΔT) can be expressed as

$$\varepsilon_t = (\alpha_s - \alpha_f) \Delta T \quad (2-3)$$

where α_s and α_f are temperature-dependent thermal expansion coefficients of Si and GaAs, respectively. During cooling down of GaAs/Si heteroepitaxial layers from an elevated growth temperature to ambient temperature, the GaAs layer will be under tensile strain. Since the system is cooling down, dislocation relaxation mechanisms are much less efficient at relieving the resulting tension. Therefore, the residual thermal expansion strain that remains in the GaAs layer when it reaches ambient temperature can be as high as 90 % of the total thermal mismatch [49]. Such a situation can lead to microcrack formation in the GaAs layer. Crack nucleation is also dependent on an effective critical cracking thickness, t_c , similar to the h_c for misfit dislocation formation. Plots of theoretical and experimental t_c for the GaAs/Si system as function of ΔT [50] are shown in Fig. 2-2. Cracks occur when the thickness of the GaAs layer on Si substrate exceeds t_c and the whole system is subjected to a temperature variation exceeding a particular ΔT as shown in Fig. 2-2. Moreover, the thermal mismatch strain can also reduce the critical thickness of strained layer structures such as QW and QD thus should be taken into account when growing such strained structures.

Figure 2-2 Plots of theoretical (solid line) and experimental (▲) critical cracking thickness, t_c , for GaAs/Si system as function of ΔT [50].

Another incompatibility between GaAs and Si is the difference in the crystalline symmetry between zincblende (GaAs) and diamond (Si) structures. This gives rise to a type of defect called anti-phase boundaries (APB). APB is basically a crystalline defect that is generated due to the lower sub-lattice bond symmetry of the III-V zincblende crystal structure compared to the higher symmetry of the diamond crystal structure [51]. APB affects the heteroepitaxy of any zincblende structure on diamond structure, which means it also occurs during GaAs/Ge or InGaP/Si heteroepitaxy. In the case of GaAs/Si, the atoms in the zincblende GaAs crystal take the same positions as those in the diamond Si crystal, but with the distinct Ga and As sites of GaAs, the symmetry of its unit cell is reduced. Exchanging the Ga anion positions with the As cation positions effectively rotates the unit cell by 90°; this effect is illustrated in Fig. 2-3. During GaAs deposition on Si, the reduction of symmetry forces the GaAs unit cell to assume one of

two distinct and perpendicular orientations at the GaAs/Si interface. The final orientation depends on the underlying orientation of the Si surface and the initial conditions of the GaAs layer.

Figure 2-3 Ball and stick drawings of two possible orientations of a GaAs unit cell.

On a real (100) Si substrate, single atomic-height steps exist on its surface due to the slight surface tilt occurring in a real wafer. These single atomic-height steps typically run along one of the two $\langle 011 \rangle$ directions on the (100) plane and thus there are two different kinds of terrace-and-edge combinations possible as shown in Fig. 2-4 [51, 52]. First, there are type-A-terraces on the surface with Si atom dangling bonds point parallel to the step edge. Second, there are type-B-terraces with Si atoms dangling bonds pointed perpendicularly to the step edge. This clearly indicates a 90° rotation of the Si-Si dimer orientations across the step. From the fact that As-Si bonds are stronger than the Ga-Si bonds, the first layer bonding to the Si substrate would naturally be an As layer [53]. Therefore, when a subsequent Ga layer is deposited, GaAs unit cells are formed, each with a matching rotation with the Si dimers underneath it. At the step edge, a GaAs unit cell will form a boundary between the adjacent 90° rotated GaAs unit cell. Within this boundary, a charged two-dimensional plane of As-As or Ga-Ga bonds is

formed instead of regular Ga-As bonds, as illustrated in Fig. 2-5. APB in GaAs leads to electrically charged defects, which may reduce the minority carrier lifetime and degrade the electronic properties of optoelectronic devices. Furthermore, APB can also generate threading dislocations in the GaAs layer, thus significantly degrade the quality of subsequent deposited layers.

Figure 2-4 Two different kinds of terrace-and-edge combinations on real (100) Si surface exhibiting single atomic-height steps.

Figure 2-5 Anti-phase boundary (APB) formation due to single atomic-height steps on real (100) Si or Ge surfaces.

2.1.2 Strategies to realize device-quality GaAs on Si substrate

To realize device-quality GaAs on Si substrate, one has to solve the problems discussed earlier. There are several methodologies proposed to overcome the lattice constant mismatch in the GaAs/Si heteroepitaxy. For monolithically integrated GaAs on Si, there are two major approaches to reduce TDD in the final GaAs layer. The first approach is selective-area epitaxy or nanoheteroepitaxy [54, 55], which basically confines the GaAs epitaxy onto a much smaller Si area defined by an oxide mask. The idea is to confine the threading dislocations into a smaller area and to limit their interactions and effectively prevent dislocation pileups. Nevertheless, such selective-area epitaxy incurs additional steps of mask lithography and cannot offer as much flexibility as wafer-level epitaxy. A more promising approach is to employ some intermediate buffer layer in between the GaAs and Si to accommodate the material incompatibilities. Amongst the proposed intermediate buffer layers [18-20], Ge is the most promising candidate. First and foremost, GaAs and Ge have negligible lattice

mismatch ($\sim 0.08\%$) and almost no thermal expansion mismatch as shown in Table 2-2. Since the GaAs/Ge system contains less than 0.1% lattice mismatch and no thermal mismatch, the threading dislocations or epilayer cracking are expected to be much less compared to the GaAs/Si system discussed previously. The next step now is to realize a device-quality Ge layer on a Si substrate ready for GaAs nucleation.

Material	Group	Lattice Constant (Å)	Mismatch with GaAs (%)	Thermal expansion coeff (K^{-1})	Melting point (°C)	Thermal Conductivity (W/cm.K)
Ge	IV	5.658	0.082	5.5×10^{-6}	937	0.8
GaAs	III-V	5.653	0	5.5×10^{-6}	1240	0.6

Table 2-2 Compilation of Ge and GaAs material properties.

Wafer bonding of a Ge substrate on a Si substrate has been suggested to realize a Ge/Si substrate [56, 57]. However, wafer bonding technology is hindered by difficulties with bonding yield, poor mechanical strength and poor thermal stability at the bonded interfaces. This technology is also limited by the differences in the Ge and Si wafer sizes available for bonding. Moreover, with increasing cost of Ge wafers, this is certainly not the economical way to move forward. Therefore, it is clear that monolithic heteroepitaxial integration is again needed to realize a Ge/Si substrate.

For Ge/Si integration, relaxed, compositionally-graded $Si_{1-x}Ge_x$ buffer layers have been shown to successfully grade the Ge content from $x=0$ to 1 while maintaining low 10^6 cm^{-2} TDD in the final pure Ge layer [23, 24, 58]. Compositionally graded layers have several advantages [59, 60]. First, by promoting strain relaxation at each incremental compositional step, threading dislocations in the layers can be recycled to prevent additional dislocation nucleation or multiplication. The individual

compositional layers in the $\text{Si}_{1-x}\text{Ge}_x$ buffer layer acts to suppress dislocation interactions, thus high amount of mismatch strain relaxation can be achieved with no increase in the overall TDD. A schematic diagram of compositionally graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer on Si substrate is shown in Fig. 2-6. A threading dislocation from the substrate extends its misfit length at each interface, increasing the strain relaxation without increasing the overall TDD. Second, there are no residual thermal strains or cracks observed at room temperature in the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. This is mainly because there is always a constant compositional gradient in the layer, so when a strain is applied, the distribution of dislocations through the relaxed graded region can be redistributed, eliminating the residual strain, except for the small strain due to thermal expansion from $\sim 500^\circ\text{C}$ to ambient temperature, when dislocations can no longer move.

Figure 2-6 Cross-sectional schematic of relaxed graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer grown on Si substrate. A threading dislocation from the substrate is shown moving into the graded $\text{Si}_{1-x}\text{Ge}_x$ buffer without creating additional dislocation [59].

With a low TDD pure Ge layer realized by a compositionally graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate, the problem of lattice and thermal expansion mismatch in the GaAs/Si

integration is partly solved. There is still, however, the problem of APB formation and interface auto-doping. To suppress APB formation, single-domain Ge-Ge dimer orientations across all surface step boundaries have to be realized. This is to prevent the occurrence of 90°-rotated adjacent GaAs unit cells at the step edge, as previously discussed. The single-domain Ge surfaces exhibiting uniformly oriented Ge-Ge dimers with respect to the $\langle 110 \rangle$ step edges can be achieved if the Ge surface steps height is of double atomic high. With all dimer pairs aligned the same way, GaAs deposited on these Ge surfaces will not experience domain rotation at the surface step edges, and APB will not form, as illustrated in Fig. 2-7.

Figure 2-7 Schematic diagram of APB suppression when GaAs is deposited on single-domain Si or Ge surfaces with double atomic-height steps.

Double atomic-height steps are more easily attainable by introducing a deliberate offcut to the (100) Ge substrate. When a (100) Ge substrate is offcut by several degrees towards one of the [110] directions (or {111} plane), the spacing of the steps w will be reduced since w is function of the offcut angle θ and step height d .

$$w = \frac{d}{\tan \theta} \quad (2-4)$$

Large area suppression of APB has been demonstrated by annealing a misoriented Ge surface at 640°C [25] or Si surface at high temperature of 1000°C [61]. Therefore, there should be a preference for one of the two Ge (or Si) sublattices over the other, either type-A or type-B, as shown earlier in Fig. 2-4. Indeed, at sufficiently high temperature, atoms from type-B edges would diffuse towards type-A edges until all the edges are of type-A. Furthermore, with the smaller step spacing on the misoriented surface, such diffusions are effectively enhanced. This results in perfect double-atomic height step Ge surface with all terraces belonging to type-A, leading to an APB-free GaAs layer [62-64]. Furthermore, a type-A atomic configuration can lower its energy by about 40 meV per edge atom through a drastic reconstruction forming π -bonded chains that are observed in the 2×2 Si or Ge (100) surface reconstructions. This model demonstrates that the energetic preference is not for either type-A single steps nor type-B single steps but only for double-height type-A steps, over all other kind of steps. This atomic reconstruction is illustrated in Fig 2-8.

Figure 2-8 Atomic surface reconstructions of Si surfaces with type-A double atomic-height steps proposed in [62, 63]. Top: unreconstructed step edges. Bottom: π -bonded chains are formed on step edges.

Although the double atomic-height steps on the Ge surfaces could potentially suppress APB formation, an optimized GaAs nucleation conditions needs to be achieved before truly APB-free GaAs layer can be realized. This will be discussed in detail in chapters 4 and 5. The other challenge of GaAs/Ge heteroepitaxy is the interface

auto-doping which occurs as Ga and As atoms act as substitutional p-type and n-type dopants, respectively in the Ge crystal lattice, while the Ge atoms act as amphoteric substitutional dopants (usually n-type) in the GaAs crystal lattice. The atomic inter-diffusion is encouraged by the typical elevated-temperature growth condition for the GaAs layer. This atomic inter-diffusion phenomenon is able to alter the doping concentration at the interface significantly and may lead to the formation of a parasitic pn junction near the interface region, degrading the electrical properties of the GaAs layer and/or devices built on top of it. Some promising solutions to this problem have been proposed, including the use of low-temperature GaAs initiation by migration enhanced epitaxy (MEE) [65], which is discussed in the following section.

2.2 Molecular beam epitaxy (MBE)

2.2.1 Overview

Molecular Beam Epitaxy (MBE) is an advanced crystalline growth technique mainly used to grow high-purity compound semiconductor epitaxial layers [66-69]. MBE is able to deposit high-quality crystalline layers with excellent control in thickness, doping and composition. With these abilities, MBE has established itself as one of the leading research and production tools in the development of high-performance electronics and optoelectronic devices. The highly precise film deposition control achieved in MBE is also crucial in the growth of nanostructures. The MBE system used to grow all the samples presented in this thesis was the RIBER 32P solid-source MBE (SSMBE). In this system, the constituent elements of the group III semiconductors (Ga, In, Al) and the dopants (Si and Be) in the form of molecular beams are deposited onto a heated crystalline substrate. The molecular beams originated from thermally evaporated extremely pure (typically 99.9999 %) elemental sources contained in a crucible made of

pyrolytic boron nitride (PBN). A valved arsenic (As) cracker cell was employed in this system for supply of As₄. This evaporation technique for solid As overcomes the conventional problems associated with the handling of hydrides and metalorganics employed in growth processes involving the use of gas sources. The use of a valve in the cracker cell enables precise delivery and control of the As flux required for the growth process without rapid depletion of the source materials.

The epitaxial deposition occurs within an ultra-high vacuum (UHV) deposition environment; UHV is achieved when the total gas pressure is lower than 10^{-9} Torr. Therefore, epitaxial layers with purity levels lower than 10 parts-per-billion (ppb) are routinely obtained. Another attractive feature of MBE is that the growth rates can be varied by simply changing the temperature at which the crucible is heated, directly changing the intensity of the molecular beams. The crystal growth rate in MBE depends on the group III adatoms flux; in this thesis growth rates of ~ 0.3 Å/sec up to ~ 3 Å/sec were employed. In SSMBE, the molecular beams can be blocked by means of mechanical shutters in a fraction of a second, allowing for nearly atomically abrupt transitions from one material to another. This feature also allowed advanced epitaxial growth techniques such as alternate-beam epitaxy and migration-enhanced epitaxy (MEE) possible [70].

MBE system normally comes in modular form, hence giving the user more flexibility in combining only the desired block into the final production system. A typical MBE system consists of three main vacuum chambers: a load lock or introduction chamber, a transfer chamber, and a growth chamber. The load lock is used to bring samples into and out of the vacuum environment while maintaining the vacuum integrity of the other chambers. The transfer chamber is used for sample preparation (normally thermal degassing) but can also be equipped for material characterization.

The growth chamber is the place where the epitaxial deposition takes place. A schematic of an MBE growth chamber is illustrated in Fig. 2-9. After thermal degassing in the transfer chamber, the sample is mounted onto the substrate holder by a mechanical arm. The sample surface is then rotated until it is in-line of sight with the molecular beams.

Figure 2-9 Schematic diagram of an MBE growth chamber [69].

During epitaxial deposition in an MBE system, a reflection high-energy-electron diffraction (RHEED) system is used to provide *in-situ* monitoring. RHEED has become an essential tool in MBE, providing real-time information of the epitaxial film being grown inside the growth chamber. The geometry of the RHEED system allows it to operate without interrupting the molecular beams path, allowing the growth to take place smoothly. The RHEED electron beam is at grazing incidence with the substrate surface, penetrating only a few outermost atomic layers, whereas the molecular beams impinge almost normally to the substrate surface. The RHEED diffraction pattern on the

fluorescent RHEED screen is routinely used to interpret important information. First, it is used to check the removal of substrate surface oxide. If the surface is still covered by oxide, a diffused diffraction pattern will appear on the fluorescent screen. A complete removal of surface oxide is achieved once the elongated streaky RHEED pattern, in the case of smooth and crystalline surface, is observed. Second, the RHEED pattern is frequently used to monitor the changes in the substrate surface geometry and crystal quality, with spotty or diffused patterns indicating a rough surface and an elongated streaky pattern indicating a smooth and crystalline surface. This is especially useful when three-dimensional growth indicating islanding on the surface occurs. The transition from two-dimensional to three-dimensional growth mode can be seen by the change in the RHEED pattern from streaky to spotty. Such islanding is the growth mode for self-assembled QD structures, which will be discussed in the following section.

The third application of RHEED is the interpretation of RHEED specular beam spot intensity as the real-time measurement of the film growth rate [66]. Figure 2-10 illustrates a correlation of surface coverage of 2D-clusters with idealized RHEED oscillations. During typical MBE growth, the film grows layer-by-layer, which means the growth of each atomic layer is largely completed before the next layer growth begins. The film surface would be atomically rough before an atomic layer is grown completely, hence creating a more diffuse RHEED beam spot, leading to lower diffracted beam intensity. Once a complete atomic layer is grown, an atomically smooth surface is established, leading to higher diffracted beam intensity. Thus a period of completion of growth of a single atomic layer corresponds to the period of RHEED intensity oscillation. For example, in GaAs growth, one GaAs ML is 2.83 Å-thick. Therefore, if an average period of RHEED intensity oscillation is found to be t seconds,

then the growth rate of the film can be determined as $\frac{3600}{t} \times 2.83 \text{ \AA/hour}$. This third interpretation of RHEED pattern is indeed of a paramount importance, especially in the growth of nanostructures and advanced epitaxial growth techniques, such as MEE in which the ability to accurately control the deposited monolayers is very crucial.

Figure 2-10 Schematic diagram of a RHEED intensity oscillation, corresponding to one complete ML deposition [66].

2.2.2 Migration enhanced epitaxy (MEE) growth technique

As mentioned earlier, a typical MBE growth of GaAs proceeds layer-by-layer, which means small 2D islands occur on the surface and progressively coalesced with one another as the growth progresses, as illustrated in Fig. 2-10. However, such a growth process is not ideal as there will be periods when some surface roughening

occurs due to non-ideal islands coalition. Neave *et al.* reported that GaAs grown on a misoriented surface at sufficiently high surface temperature resulted in the absence of RHEED intensity oscillation, indicating the elimination of surface roughening [71]. This phenomenon occurred mainly because of two reasons. First, the adatoms migration distance, λ , is enhanced as temperature increases up to the limit where desorptions take over. With larger migration distance, adatoms could travel to their appropriate sites and could also travel to the step edges where they are adsorbed. In the latter case, growth no longer occurs on the step terraces but rather on the step edges; such a growth mode is called the step-flow growth mode. This mode is naturally easier to occur on a misoriented or vicinal surface, since the steps width, l , is narrower and adatoms can migrate to the step edges more easily. A comparison between the layer-by-layer growth mode and the step-flow growth mode is shown in Fig. 2-11(a) and Fig. 2-11(b), respectively. In Fig. 2-11(a), two-dimensional islands occur on the step terraces and create atomically rough surfaces which give rise to the RHEED intensity oscillations. On the other hand, in the step-flow growth mode shown in Fig. 2-11(b), most of the adatoms are adsorbed by the step-edges while the step terraces are always atomically smooth so there is no RHEED intensity oscillations observed.

Figure 2-11 Schematic drawing of (a) layer-by-layer or two-dimensional growth mode and (b) step-flow growth mode. Note that the RHEED intensity oscillation ceases in (b).

The step-flow growth mode in typical MBE growth is achieved at higher temperature, meaning that the adatoms possess higher energy to migrate to the steps/kinks available on the vicinal growth surface, as described above. However, high growth temperature would worsen the auto-diffusion at the GaAs/Ge heterointerface as

previously discussed. Therefore, a low-temperature growth process that produces an atomically smooth surface is preferred; this could be achieved in MEE [72, 73]. High-quality GaAs could be achieved by MEE at surface temperature as low as 300°C compared to typical MBE GaAs epitaxial deposition performed under As-overpressure environment at surface temperature of 580°C - 600°C. With the As overpressure in typical MBE, Ga adatoms arriving on the growing surface would immediately form GaAs islands/molecules. These GaAs islands are less mobile on the surface because of the stable chemical bonds between GaAs molecules in the islands and As atoms in the underlying plane. On the other hand, the As and Ga are supplied onto the growth surface in an alternate fashion during MEE. In MBE, this is done by alternating the opening of the As and Ga mechanical shutters by certain periods of time. The amount of As and Ga flux is designed such that there is a complete monolayer coverage on the surface each time the adatoms are supplied. In between the supply of adatoms, a growth interruption is inserted. During the growth interruption, the surface adatoms migration distance is high as there is no immediate bonding between Ga and As and hence less formation of GaAs molecule. This ensures that the Ga adatoms remain mobile and surface smoothing process can occur even at low temperature of 300°C [70, 73-75]. In the case of GaAs/Ge heteroepitaxy, large migration distance is crucial as it ensures the adatoms reached the proper position before the next layer is deposited, and thus prevent APB formation. Furthermore, with low temperature deposition, the inter-diffusion of Ge and/or As at the GaAs/Ge heterointerface is minimized.

2.2.3 Substrate preparation procedure

In heteroepitaxy, pre-growth substrate preparation is one of the most critical factors in achieving good quality epitaxial layers. Many types of defects found in epitaxial layer are related to the cleanliness of the substrate surface. Hence, pre-growth

substrate preparation to remove surface impurities and to make well-defined substrate surface is critical. Amongst surface impurities, carbon and surface native oxide are the most common ones, with carbon demanding more severe cleaning techniques to ensure its removal. All samples presented in this thesis went through a similar cleaning process, with the exception of those of GaAs substrates. For epi-ready GaAs substrates, the cleaning was done thermally in the preparation chamber at 400°C. This initial thermal degassing process is to eliminate organic contaminations on the surface. After this process, the sample is transferred into the growth chamber where thermal oxide desorption is carried out prior to epitaxy growth.

All other remaining substrates employed in this thesis are terminated with a pure Ge surface. A variety of substrates was employed, namely: nominal (100) Ge on Si substrate, (100) Ge substrate misoriented 6° towards (111) plane and (100) graded Si_{1-x}Ge_x/Si misoriented 6° towards (111) plane. Each of them underwent similar substrate preparation procedures prior to GaAs heteroepitaxial growth. First, the sample was cleaned using IPA and Acetone to remove organic contaminants, followed by 1-minute DI water rinse to remove Ge native oxide, as the Ge oxide is soluble in water. The sample was then immediately blown dried using pure N₂ gas. Afterwards, it was subjected to a UV-ozone treatment at 100°C for 20 minutes [25, 65, 76]. This step is crucial as it has been shown to reduce the carbon level on the substrate surface. Carbon contaminants on the surface may create rough interface and defects, which will eventually degrade the optical and electrical quality of the grown layer. Upon completion of this step, the sample was immediately put onto a 3" molybdenum block and transferred into the load-lock chamber. Two-step thermal treatments similar to the ones employed for GaAs substrate were used. After the sample was mounted on the substrate holder in the growth chamber, oxide desorption was done thermally at a

surface temperature, T_s , of 640°C for 20 minutes under As overpressure. During this period, the sample concurrently underwent *in-situ* annealing to create double atomic-height steps. At the end of the thermal desorption process, a streaky 2×2 RHEED pattern was observed, indicating removal of native Ge oxide.

2.3 Self-assembled quantum dots

Ever since Arakawa and Sasaki [39] proposed the concept of three-dimensional (3-D) quantum confinement to achieve temperature-independent laser operation, research in this area has been accelerating rapidly. The ultimate quantum confinement can finally be realized in a structure called a quantum dot (QD). A QD is basically a crystalline structure with dimensions smaller than the de Broglie wavelength or the mean free path of the carriers inside the structure. In order to achieve the 3-D confinements of carriers, the QD is encapsulated within a material of wider bandgap that will then act as potential walls for the carriers inside QD structure. The QD small dimension induces discrete energy levels inside the QD structure, which mirrors the discrete energy levels in atoms. This unique QD characteristic produces a narrow optical transition spectrum, a very attractive characteristic especially for laser device application. Furthermore, the confinement also leads to delta-like Density of States (DOS), which leads to high temperature stability and high optical gain in laser devices [77].

In order to realize the potential advantages of QDs, their size should be optimized such that at least a localized state in the QD structure exists, and the spacing between discrete energy levels is maximal, bringing temperature stability to the structures. An estimated optimum size for InAs QDs in a GaAs matrix suggests that the QDs size should lie between 4 nm and 20 nm, assuming a perfect cubic QDs structure. The areal

density of the QD should be high ($10^{10} \text{ cm}^{-2} - 10^{11} \text{ cm}^{-2}$) in order to maintain a high modal gain for lasers. They should be uniform in shape and size; otherwise the optical transition will be broadened, preventing ideal QD laser performances. Finally, they should be free from defects that produce centres of non-radiative recombination [77].

Most of the early efforts to realize QD structure that can satisfy the above requirements revolved around the use of lithographic tool to define patterns into which QDs will be grown [78]. There are other techniques, however, which include the use of AFM/STM to induce formation of oxides on the surface, which, after being removed, will act as the QDs nucleation sites [79-81]. Substrate patterning employing block copolymer [82] and aluminum oxide nanohole array template masks [83] were also attempted. Nevertheless, these techniques generally have very low throughput and are not able to produce a large area of regular arrays of dots with sub-100nm periodicity. In the case of lithographically defined patterns, electron-beam lithography (EBL) has recently gained more popularity [84]. The popularity of EBL is predictable, as it is one of the most widely used sub-100nm patterning tools, mainly for patterning masks for photolithography process. However, EBL's low throughput and high cost prevent the widespread implementation of this technique for QD realization.

In search of a better technique to realize QD, several groups reported realization of defect-free QD employing the self-assembly-in-nature Stranski-Krastanow (SK) growth technique [77, 85, 86]. This technique employs a natural island formation phenomenon arising from the release of surface strain energy in large lattice-mismatched systems. Figure 2-12 illustrates three main heteroepitaxial growth modes; note that in the SK growth mode, 3D islands are formed after a period of 2D growth; this 2D layer is called the wetting-layer. However, due to the fact that humans do not have total control over the formation of these naturally occurring islands, non-

uniformity of the islands' size, shape and nucleation sites is expected. These non-uniformities increase the threshold current density and reduce the characteristic temperature, hence preventing realization of ideal-QD lasers. Nevertheless, proper growth parameters could lead to high areal density and high uniformity for self-assembled QD structures. Quantum dot structures as the active layer materials in LEDs devices are attractive, especially to achieve super-luminescent and broad-luminescence LED. For optical interconnect application, LEDs emitting at 1.3 μm and 1.55 μm , corresponding to the lowest dispersion and lowest loss of optical communication fibers, is preferred. The InAs/GaAs QD system is the most potential material system. This system benefits from the fact that it can be employed readily to realize emission at 1.3 μm without complicated device structure or complicated material composition [41].

Figure 2-12 Heteroepitaxial growth mode: (a) Volmer-Weber, (b) Frank-van der Merwe, and (c) Stranski-Krastanow.

However, it was found that In segregation and strain prevent the realization of defect-free InAs QD on GaAs for 1.3 μm emission. Several solutions to these problems were proposed, which include the growth of dots in a well (DWELL) structures, and strain-reducing and strain-compensating layer. However, employing a strain-

compensating layer, which normally employs a dilute nitride layer, is challenging as the quality of the layer tends to be compensated by ineffective nitrogen incorporation. Although nitrogen was found to induce a large bowing effect in the semiconductor material researchers are still trying hard to overcome the nitrogen-related defects. Furthermore, the temperature growth window for such dilute-nitride layer is normally narrower than in the other layers. Another more promising way to prevent defects due to strain and prevent In segregation is the employment of a strain-reducing (SR) layer, such as InGaAs layer [81, 87-89].

The growth of QDs relies heavily on the strain and surface energy. In the growth on an undulated surface, these parameters are less-ideal. Furthermore, employment of a vicinal surface required to suppress APB during the GaAs growth on Ge must be taken into account as it creates another complication for the QD growth. An advanced growth technique called alternate-beam (AB) MBE was found to help both in the improvement of QD uniformity as well as increasing the areal density during growth of QD on a vicinal surface [90]. This technique is similar to MEE, which allow more time for the group III adatoms to migrate on the surfaces hence creating more uniform QD ensemble. The difference between AB-MBE and MEE is the constant As supply in AB-MBE even during the growth interruption. In the growth of InAs QD this overexposure condition is important as it prevents the re-evaporation of indium from the growth surface.

2.4 Characterization techniques

In this section, some of the characterization techniques employed in this study are discussed. These tools were used to understand the structural and optical characteristics of GaAs layer grown on Si-based platform. Furthermore, they were also used to assess the structural and optical quality of QW and QD structures.

2.4.1 X-Ray Diffraction (XRD)

The X-Ray Diffraction (XRD) measurements in this thesis were performed using a Philips X'Pert High Resolution XRD system. The x-ray is generated by using the $K\alpha_1$ of Cu with photon energy of 8.05 keV corresponding to an x-ray wavelength of 1.54056 Å. XRD is a non-destructive and accurate way to characterize the crystallographic quality and residual strain in semiconductor epitaxial layers. The high-energy x-rays diffracted by the epilayers crystalline planes generate a diffraction pattern revealing information on the symmetry, lattice spacing, orientation, and crystalline quality of the epilayers and the substrate. Triple-axis XRD, in which the diffracted beam from the sample underwent an additional analyzer-collimator crystal before being detected, allows for reciprocal space maps that allow measurement of residual strain, alloy composition, and crystallographic tilt in heteroepitaxial layers [91].

2.4.2 Photoluminescence (PL)

Photoluminescence (PL) spectroscopy was the main optical characterization tool used in this study. In the measurements, the sample is excited by the 5145Å line of an Ar^+ laser. The PL signals were detected using a liquid nitrogen cooled germanium detector in conjunction with a standard lock-in technique. The photon energy of the excitation laser was able to generate electron-hole pairs in the material, as most of the materials studied in this thesis were narrow bandgap materials. The energy of the detected luminescence is related to the difference in energy levels between two electron states involved in the transition, typically the conduction and valence band edges. The intensity of the emitted light is directly dependent on the radiative process in the material, hence could give some estimate of the quality of the sample. PL measurements in this thesis were performed at ambient temperature and also at cryostat-cooled temperature as low as 5K.

2.4.3 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is a microscopy technique whereby a high-energy electron beam is transmitted through an ultra-thin sample (typically 5 μm -thick), interacting with the sample as it passes through it. A diffraction image is formed from the electrons transmitted through the specimen and a real image of the structure can be obtained from the fourier-transform of the diffraction image. For heteroepitaxial layers investigation, cross-sectional TEM is especially useful to observe the quality of the various heterointerfaces and dislocations mechanism at these interfaces. TEM can provide sub-nanometer resolution capable of accurately measuring thin QW structures, QD structures and different type of defects, including threading dislocations and APB. Proper preparation of useful TEM samples and proper alignment of the TEM electron beam optics to produce high-quality images require extensive hands-on experience. The high magnification of TEM results in very small sampling areas, and thus limits the use of cross-sectional TEM for accurate measurements of TDD at levels below 10^8 cm^{-2} [92].

2.4.4 Atomic force microscopy (AFM)

Atomic force microscopy (AFM) was used to investigate the surface quality of the GaAs heteroepitaxial layer and to study the size and density of QD structures in this thesis. In the AFM experiment, a sharp tip of nanometer-scale radius is mounted on the end of a flexible cantilever and brought into sufficiently close proximity with the sample surface that a detectable force is generated. Detection of the tip-sample force is through deflection of a laser beam reflected from the back of the cantilever to a photodiode. The tip is rastered above the surface and a control loop keep the distance between the tip and the sample at a constant value through the actuation of a piezoelectric translator that moves the sample (in the z direction perpendicular to the

sample). The detected signals were processed by built-in software and resulted in contour maps depicting the different feature heights on the sample surface.

Chapter 3 Growth of GaAs on nominal (100) Ge/Si Substrate

In this chapter, heteroepitaxial growth of GaAs on a nominal (100) Ge/Si substrate is investigated. The purpose is to understand the mechanisms of GaAs nucleation on this nominal surface and how the migration-enhanced epitaxy (MEE) growth technique affects the GaAs growth mechanisms and, eventually, the quality of the GaAs layer.

3.1 Experimental procedures

Two samples (M1 and M2) cleaved from an 8-inch diameter Ge on Si (100) substrate were employed in this study. The Ge layer was grown directly on the Si substrate using PECVD elsewhere. Figure 3-1 shows cross-section and plan-view transmission electron microscopy (TEM) images of the Ge/Si substrate. The Ge layer thickness is approximately 1 μm and was grown directly on (100) Si substrate. From the cross section TEM image, the threading dislocations due to the high lattice mismatch ($\sim 4\%$) between the Ge layer and Si substrate are clearly observed, especially near the interface region. The average threading dislocation density at the top of the Ge surface was estimated to be $4.3 \times 10^8 \text{ cm}^{-2}$. This value was estimated by calculating the number of dislocations observed at the surface of the Ge layer at several regions of the Ge surface.

The samples were cleaned by de-ionized water to remove the Ge native oxide, followed by a 20-minute UV-ozone treatment at 100°C to remove carbon contamination before the transfer to molecular beam epitaxy (MBE) growth chamber. Inside the MBE

chamber, oxide desorption was achieved at 640°C. This was then followed by in-situ thermal annealing for 20 minutes, after which the typical (2×2) RHEED pattern was observed [25, 65, 76]. For sample M1, the substrate temperature was lowered to 450°C for the MEE process after the *in situ* thermal annealing step. No arsenic flux was introduced into the chamber before and during this time. The MEE process was performed by alternating the As and Ga shutter opening/closing cycles, each with two-second opening time. A two-second growth interruption was inserted following each supply of Ga and As. The As/Ga beam equivalent pressure (BEP) ratio during this process was set at 25. The shutter opening time has been optimized to supply enough Ga and As adatoms to complete a monolayer (ML) (2.83 Å) growth during each cycle. The MEE process was repeated for 10 cycles, corresponding to the growth of 10 MLs of GaAs. After the 10th cycle, the As shutter was kept open to maintain an As overpressure inside the chamber. This was to prevent As re-evaporation from the freshly-grown GaAs layer surface. Subsequently, a standard GaAs molecular beam epitaxy (MBE) growth process was used to grow a structure comprising a 250nm-thick GaAs buffer layer, 6nm-thick In_{0.2}Ga_{0.8}As single quantum-well and 100nm-thick GaAs cap layer. Both GaAs layers were grown at 590°C with an As/Ga BEP ratio of 25 and growth rate of 1 µm/hr. The In_{0.2}Ga_{0.8}As single quantum well (SQW) was grown at 500°C at a growth rate of 1.2 µm/hr. The SQW serves as a built-in optical probe to assess the optical quality of the structures. On the other hand, the growth procedure of sample M2 was identical to that of sample M1 with the exception of the MEE process. Therefore the entire structure in sample M2 was grown by standard MBE without the 10 ML of MEE-nucleated GaAs.

Figure 3-1 (a) cross-sectional TEM image and (b) plan view TEM image of the Ge/Si substrate.

3.2 Calculations of Ge layer relaxation state

In order to ascertain the extent of Ge layer relaxation and to calculate the Ge layer parallel lattice constant $a_{\parallel}$, the Ge/Si substrate was characterized by high resolution x-ray diffraction (XRD). The first step of the characterization was to record a (004) XRD rocking curve, which provides information on the perpendicular Ge layer lattice constant $a_{\perp}$. The formulae [93-95] used were:

$$\lambda = 2d_{hkl} \sin \theta_B \quad (3-1)$$

$$d_{hkl} = \frac{a_{\perp}}{\sqrt{(h^2 + k^2 + l^2)}} \quad (3-2)$$

where λ is equal to 1.5406 Å, which is the x-ray wavelength, and θ_B is the Ge peak Bragg angle. Employing equations (3-1) and (3-2) and knowing from the (004) scan in Fig. 3-2(a) that θ_B is 33.28°, $a_{\perp}$ was calculated to be 5.615 Å.

Inclination between the asymmetric planes, (115) in this case, of the substrate and the epitaxial layer is usually observed if the film is subjected to tetragonal distortion. In the case of Ge/Si heteroepitaxy, this distortion is highly probable as the lattice mismatch is high. The symbol Ψ represents the angle between the (001) plane and (115) plane of the epitaxial layer. Meanwhile, $\Delta\Psi$ represents the tilt angle between the Si(115) plane and Ge(115) plane, which can be calculated using the following equation:

$$\Delta\Psi = \tan^{-1} \left(\frac{\sqrt{2}}{5} \right) - \tan^{-1} \left(\frac{\sqrt{2}a_{\perp}}{5a_{\parallel}} \right) \quad (3-3)$$

Alternatively, $\Delta\Psi$ can be found from the (115) x-ray space map, which is defined as the separation in the rocking angle, ω , between the Si and Ge peaks. Figure 3-2(b) shows the (115) x-ray space map constructed by repeated Ω -2 θ scans at different ω offsets. $\Delta\Psi$ is indicated in the figure as 0.048°. Diffused scattering close to the Ge layer reflection

can be observed from the (115) XRD space map. This might be due to the dislocations observed in the cross section TEM image in Fig. 3-1. Using equation (3-3), and knowing the value of $a_{\perp}$ and $\Delta\Psi$, $a_{\parallel}$ was calculated to be 5.632 Å. Meanwhile, using equation (3-4) below, the relaxation ratio was calculated to be 93.5 % (the cubic Ge lattice constant is 5.646 Å and cubic Si lattice constant is 5.431 Å) [96].

$$\text{Relaxation ratio, } R = \frac{a_{\parallel} - a_{Si}}{a_{Ge} - a_{Si}} \quad (3-4)$$

This result indicates that the Ge parallel lattice constant at the surface of the Ge/Si sample is less than the Ge cubic lattice constant. This should result in elongation of the perpendicular GaAs lattice when grown pseudomorphically on the Ge/Si substrate. Knowing that the cubic GaAs lattice constant is 5.653 Å, the mismatch between cubic GaAs and the Ge parallel lattice constant on the Ge/Si substrate was calculated to be 0.12 %, indicating a closely matched system.

Figure 3-2 Plot of (a) (004) XRD rocking curve of the Ge/Si substrate and (b) (115) XRD space map of the Ge/Si substrate.

3.3 Significant improvements observed due to MEE

Samples M1 and M2 were first characterized using scanning electron microscope (SEM) and atomic force microscope (AFM). SEM images of the topmost GaAs surface presented in Figure 3-3 clearly demonstrate a marked improvement in the surface topography of sample M1 over sample M2. At 1000x magnification, the surface of sample M1 appears featureless, while the surface of sample M2 shows many island-like formations. However, from the AFM image in Fig. 3-4(a), it can be seen that the surface of sample M1 exhibits undulation over a small scale, with average width of 20nm. Initial nucleation of the GaAs layer by MEE has evidently enhanced the surface quality of the GaAs layer. During the MEE, the substrate temperature was lowered to 450°C, which is 24 % lower than the typical MBE GaAs growth at 590°C. The lower growth temperature translated to less energetic adatoms and the lower possibility of adatoms escaping from dislocations present on the Ge substrate surface. However, with the growth interruption following the introduction of adatoms onto the growth surface, the adatoms had much higher probability to migrate to their proper equilibrium atomic configuration, hence minimizing the occurrence of defects related to adatoms misplacement/adatoms clustering [70, 74].

Figure 3-3 SEM images of GaAs surface of (a) sample M1 and (b) sample M2. GaAs surface of sample M2 shows island-like formations, while GaAs surface of sample M1 is almost featureless.

Figure 3-4 $10\ \mu\text{m} \times 10\ \mu\text{m}$ AFM images of GaAs surface of (a) sample M1 and (b) sample M2. The GaAs surface in sample M2 has large island-like formations with RMS surface roughness of 37 nm, while GaAs surface of sample M1 has RMS surface roughness of 9 nm.

Since the MEE process employed in this study was first initiated by flooding the substrate surface with As_4 , by the time the Ga adatoms arrived at the substrate surface, they would arrive on an As-rich surface. It has been shown that As forms symmetric dimers on a bulk terminated Ge substrate. All the dangling bonds are saturated in this configuration, and the surface is very stable. Arsenic has been found to lower the surface free energy of Ge surface and therefore, it is a good candidate to be used as a surfactant in GaAs/Ge heteroepitaxy to improve the Ga adatoms migration [97, 98]. On the other hand, the M2 sample surface exhibits large island-like formations of average width and height of $1\mu\text{m}$ and $\sim 200\text{ nm}$, respectively, as shown in Fig. 3-4(b). It is strongly suspected that these features originated from the three-dimensional nucleation during the initial GaAs growth on the Ge surface. The GaAs layer in sample M2 was nucleated by standard MBE growth (without the MEE process) at 590°C . The high deposition rate of $1\mu\text{m/hr}$ and high nucleation temperature is likely to cause significant islanding and defect formation. The RMS surface roughness across a $10\mu\text{m} \times 10\mu\text{m}$ AFM scan area has improved four times from 37 nm in sample M2 to 9 nm in sample M1.

Figure 3-5(a) shows the (004) XRD omega scan plots of sample M1 and M2. The full-width at half maximum (FWHM) of the GaAs peak in sample M1 and M2 is 160 arcsec and 280 arcsec , respectively. The 40 % improvement in FWHM of the GaAs layer peak in sample M1 with the MEE-nucleated GaAs layer strongly indicates better GaAs crystalline quality. The mismatch between the GaAs layer and Ge layer in sample M1 was found to be -1600 ppm , indicating a smaller GaAs perpendicular lattice constant, $a_{\perp}$, value as compared to the Ge layer $a_{\perp}$ value. In sample M2, the mismatch between the GaAs layer and Ge layer was found to be $+1600\text{ ppm}$, indicating a larger GaAs $a_{\perp}$ value compared to the Ge layer $a_{\perp}$ value. This indicates that the GaAs layer

nucleated by the MEE process exhibits early relaxation compared to the GaAs layer grown without the MEE process. As the MEE process promotes two-dimensional growth, the GaAs layer grown by this technique has a lesser degree of island-like formations. The pseudomorphic GaAs layer in sample M1 has higher energy due to compressive strain compared to the GaAs layer with more island-like formations [99] where most relaxation occurs on the free surfaces of the islands. The higher strain energy in the planar GaAs layer in sample M1 leads to earlier relaxation of the layer.

This early relaxation of the GaAs layer in sample M1 is further supported by the (115) XRD space map shown in Fig. 3-5(b). By calculating $a_{\perp}$ from the (004) rocking curve in Fig. 3-5(a) and knowing $\Delta\psi$ is 0.004° from the (115) XRD space map, it is found that the GaAs layer in sample M1 is fully relaxed with $a_{\parallel}$ of 5.658 Å. The $\Delta\psi$ value in the (115) XRD space map represents the tilt angle between the GaAs (115) plane and the Ge (115) plane. Meanwhile, the (115) XRD space map of sample M2 is shown in Fig. 3-5(c). It can be seen that the $\Delta\psi$ value is 0.02° . Employing the same calculation used in sample M1, it is found that the relaxation ratio of the GaAs layer in sample M2 is 26% with $a_{\parallel}$ of 5.637 Å.

Figure 3-5 Plots of (a) (004) XRD rocking curve of sample M1 and M2, in relative arcsec (main) and in degrees (inset), (115) XRD space maps of (b) sample M1 and (c) sample M2.

Figure 3-6 shows a comparison of the 5 K PL spectrum of the InGaAs single quantum well in sample M1 and M2. The full-width at half maximum (FWHM) of the InGaAs PL spectrum of sample M1 is 19 nm, which is slightly better than the 21 nm FWHM of the InGaAs quantum well in sample M2. From the PL plot, a blue shift in the InGaAs PL peak energy in sample M1 was observed. This can be explained by considering the InGaAs/GaAs quantum well emission as coming from electron transitions from conduction band edge to the heavy-hole valence band edge [100]. Hence the change in band gap due to strain is proportional to the biaxial strain parallel to the [100] and [010] directions, or $\Delta E_g \propto \varepsilon$ [101]. Recall that the GaAs $a_{\perp}$ value in sample M1 is smaller than the GaAs $a_{\perp}$ value in sample M2. This indicates that the GaAs $a_{\parallel}$ value in sample M1 is larger than the GaAs $a_{\parallel}$ value in sample M2. As $\varepsilon = \frac{a_{\text{GaAs}} - a_{\text{InGaAs}}}{a_{\text{InGaAs}}}$, the larger GaAs $a_{\parallel}$ value in sample M1 in turn induced a larger strain parallel to the [100] and [010] directions in the InGaAs quantum well. Therefore, the bandgap of the InGaAs quantum well in sample M1 increased due to the larger strain, resulting in the observed blue shift in the InGaAs PL peak energy.

Figure 3-6 Plot of 5 K PL spectra from the InGaAs single quantum well in sample M1 and M2. The blue-shift in the PL peak energy of sample M1 is due to the larger GaAs parallel lattice constant.

3.4 Summary

This section reports the characterization of the Ge/Si (100) substrate to determine the Ge layer tilt and relaxation ratio using (004) XRD rocking curve measurement and (115) XRD space mapping. The mismatch between the GaAs cubic lattice constant and Ge layer parallel lattice constant $a_{||}$ was found to be 0.12 %, indicating a closely lattice-matched system. A comparison was made between the GaAs layer grown with and without a MEE-nucleated 10 ML-thick GaAs on the Ge/Si (100) substrate. SEM and AFM measurements show that significant island-like formation occurred at the GaAs surface in the sample grown without the MEE-nucleated GaAs layer due to three-

dimensional growth. On the other hand, the GaAs surface in the sample grown with the MEE nucleation process show RMS surface roughness which is four times lower due to two-dimensional growth. Consistent with the surface roughness data, a 40% reduction in the FWHM of the XRD spectrum was seen in the MEE-nucleated GaAs sample, indicating significant improvement in the crystalline quality. As a result of the two-dimensional growth, the higher strain energy in the sample grown with the MEE-nucleated GaAs layer exhibits early relaxation. Due to the larger strain along the [100] and [010] directions, the PL peak energy of the $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ quantum well in this sample exhibits a blue shift compared to the sample grown without the MEE-nucleated GaAs layer.

From the experimental results presented in this chapter, the MEE process clearly shows potential to improve the GaAs layer quality grown on Ge surface. By maintaining layer-by-layer growth, the quality of the GaAs layer grown on nominal (100) Ge surface has improved significantly. Nevertheless, with surface roughness of ~ 9 nm, as measured by AFM, clearly there is a need to further improve the GaAs quality. It is suspected that the high roughness is caused by APB formation. The following chapter discusses the effects of Ge surface misorientation and MEE GaAs nucleation temperatures to the APB formations and suppressions.

Chapter 4 Realizing Anti-Phase Boundary (APB)-free GaAs on Ge Substrate

As discussed in section 2.1, the different symmetry of the zinc-blende crystal structure with diamond structure introduces a defect called an anti-phase boundary (APB) during growth of GaAs on Ge or Si. On a vicinal surface, especially the (100) surface offcut at more than 4° towards the (111) planes, double atomic-height steps necessary for APB suppression can be achieved through relatively short annealing at 640°C for 20 mins [51, 62, 102]. In this chapter, the effects of surface misorientation on the APB propagation and suppression mechanism on GaAs epilayer on Ge surface are discussed.

4.1 Effects of Ge surface misorientation on APB propagation mechanisms

Heteroepitaxial growth of GaAs on two types of Ge surface, the first type having a vicinal (100) surface offcut 6° towards (111) plane, while the second type has a nominal (100) surface was performed. Sample A is the (100) Ge offcut 6° towards the (111) plane and sample B is the nominal (100) Ge/Si. The experimental procedures are similar to the ones presented in the previous chapter. All samples were cleaned using acetone and IPA for 1 min, followed by 30 sec of de-ionized (DI) water rinse to remove the native Ge oxide. A 20 min UV-ozone exposure was done following the cleaning process to minimize carbon contamination. The samples were then loaded into the MBE system in the shortest possible time typically within 10 mins after UV-ozone exposure. Oxide desorption was carried out at 640°C , followed by in-situ thermal annealing for 20

mins in the MBE growth chamber. The annealing process is to ensure the formation of double-atomic surface steps on the Ge surface [25]. Nevertheless, given the same annealing process performed on both samples, it is expected that the offcut surface would exhibit much more uniform double-atomic steps arrangements compared to the nominal surface. The reasons for this were discussed in section 2.2. Upon observation of the (2×2) streaky RHEED pattern, the substrate temperature was reduced in preparation for the start of the MEE sequence.

The growth sequence was started by depositing 10 monolayers (MLs) of GaAs at $0.25 \mu\text{m/hr}$ using MEE at 450°C for both samples. The substrate surface temperatures were measured by an infrared pyrometer, calibrated to thermocouple readings. No As flux was introduced into the chamber before the start of the MEE sequence. The MEE sequence involved opening the As shutter for two seconds, followed by two seconds of growth interruption, two seconds of Ga shutter opening and another two seconds of growth interruption. The As/Ga beam equivalent pressure (BEP) ratio was kept at ~ 40 . The shutter opening and interruption times were calculated to supply enough Ga and As adatoms to the growth surface for a complete ML growth in every cycle.

The MEE sequence was repeated for 10 cycles; corresponding to growth of 10 MLs of GaAs. At the end of the 10th cycle, the As overpressure was maintained by keeping the As shutter open to prevent As re-evaporation from the GaAs layer surface. The growth conditions after the MEE sequence were kept constant across the samples. The remaining structures were grown by other typical MBE process. First, a 100 nm-thick low-temperature GaAs layer was grown at $1 \mu\text{m/hr}$ at 500°C . Following this, the substrate temperature was increased to 590°C for a 400 nm-thick GaAs layer at the same growth rate. After this layer, the substrate temperature was lowered to 520°C to grow a 6 nm-thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ single quantum well (SQW) at $1.2 \mu\text{m/hr}$. The SQW

again serves as an optical probe to assess the optical quality of the sample structure. The samples were finally capped with a 100 nm-thick GaAs layer grown at 590°C at 1 $\mu\text{m/hr}$. The As/Ga BEP ratio of 25 was maintained for all the GaAs layers. Cross-sectional TEM (XTEM) and 5 K photoluminescence (PL) characterizations were carried out on the samples. The 514.5 nm line of an Ar-ion laser was used as excitation source for the PL measurement. A cooled Ge detector was used in conjunction with a standard lock-in amplification technique to detect the PL emissions.

A bright-field (BF) XTEM image of sample A is presented in Fig. 4-1. It is clear that the GaAs layers in sample A contain a large concentration of defects. When the MEE sequence was carried out at substrate temperature of 450°C, evaporation of As dimers from the starting Ge surface could occur, creating As vacancies in the process. During the opening of the Ga shutter, the Ga adatoms arrived at the surface and occupied these As vacancies. If the Ga clusters reside just at the surface step edges, they could be creating APB as seen propagating on the (111) plane. Otherwise, they could be acting as nucleation sites for GaAs islands that may become the origins of stacking faults or other dislocations. The defects shown in Fig. 4-1 are mostly confined in the (111) plane, indicating that they are APB in nature. It is also observed that these defects can meet with each other after a certain GaAs thickness leading to their self-annihilation.

A BF XTEM image of sample B, presented in Fig. 4-2, shows APB that propagated more perpendicularly to the GaAs/Ge interface, making the self-annihilation mechanism less likely to happen. The difference in employing a vicinal (100) surface compared to a nominal (100) surface can be seen from the XTEM images of sample A and sample B from Figs. 4-1 and 4-2, respectively. In sample A, the APB propagation directions were in the higher index plane, with a smaller angle with respect to the GaAs/Ge interface. It is likely that an interplay between the initial nucleation

temperature of 450°C and single atomic-height steps occurring on the Ge surface of sample B induces APB with enough energy in its system to stay propagating on the (110) plane, perpendicular to the GaAs/Ge interface [103].

Figure 4-1 Bright-field (BF) XTEM image of sample A. APB can be observed propagating mainly on (111) planes.

Nonetheless, as observed from Figs. 4-1 and 4-2, there are also APB that self-annihilate each other. These APB supposedly have smaller energy in their system as compared to the ones propagating up to the surface. As their energy is lower, after a certain GaAs thickness, their propagation plane changed to lower energy planes, such as (111) or (112), to minimize the overall energy in their system. This effect is illustrated in Figs. 4-3 and 4-4. APB occasionally have “kinks” or “steps” which shift their position laterally by one lattice unit. Such kinks will either be Ga-rich or As-rich, depending on the direction of the kink. Alternate APB should naturally have different directions. If

particular kinks are energetically preferred, two alternate APB will gradually shift in opposite directions until they annihilate. In the model of APB self-annihilation [103], the thickness of the GaAs layer required for self-annihilation is at least several times the step spacing, which is much larger on a nominal (100) surface compared to vicinal surface. This again shows the advantages of employing a vicinal surface. Lastly, annihilation of APB at the strained QW layer can also be seen in the image. This effect is similar to the strained-layer superlattice (SLS) as a dislocation filter.

Figure 4-2 BF XTEM image of sample B. APB can be observed propagating on (110) plane.

Figure 4-3 Schematic diagram of APB self-annihilation mechanism.

Figure 4-4 Higher resolution BF XTEM image showing an APB switching its propagation planes (circled)

4.2 Effects of substrate temperature during MEE

In this study, the effects of substrate temperature during MEE are investigated. (100) orientated Ge substrates with 6° offcut towards the (111) planes were used in this study. The experimental procedures are similar to the ones presented earlier. Three samples having a 4 cm^2 area were soaked in acetone and IPA for 1min, followed by 30 sec of DI water rinse to remove the native Ge oxide. A 20 min UV-ozone exposure was done following the cleaning process to minimize carbon contamination. The samples were then loaded into the MBE system in the shortest possible time; typically within 10 mins after UV-ozone exposure. Oxide desorption was carried out at 640°C , followed by in-situ thermal annealing for 20 mins in the MBE growth chamber. The annealing process is to ensure the formation of double-atomic surface steps. Upon observation of the (2×2) streaky RHEED pattern, the substrate temperature was reduced in preparation for the start of the MEE sequence.

The growth sequence started by depositing 10 monolayers (MLs) of GaAs at $0.25\text{ }\mu\text{m/hr}$ using MEE at three different substrate temperatures; 450°C , 350°C and 250°C in three separate samples. The temperatures were measured by an infrared pyrometer, calibrated to thermocouple readings. No As flux was introduced into the chamber before the start of the MEE sequence. The MEE sequence involved opening the As shutter for two seconds, followed by two seconds of growth interruption, two seconds of Ga shutter opening and another two seconds of growth interruption. The As/Ga beam equivalent pressure (BEP) ratio was kept at ~ 40 . The shutter opening and interruption times were calculated to supply enough Ga and As adatoms to the growth surface for a complete ML growth every cycle.

The MEE sequence was repeated for 10 cycles; corresponding to growth of 10 MLs of GaAs. At the end of the 10th cycle, the As overpressure was maintained by

keeping the As shutter open to prevent As evaporation from the GaAs layer surface. Thereafter, the substrate temperature was increased to 500°C for low-temperature GaAs MBE growth. A 100 nm-thick GaAs layer was grown at 1 $\mu\text{m/hr}$. Following this, the substrate temperature was increased to 590°C for growing a 400 nm-thick GaAs layer at the same growth rate, and a 6 nm-thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ single quantum well (SQW) at 520°C at 1.2 $\mu\text{m/hr}$. The InGaAs SQW again serves as an optical probe to assess the optical quality of the sample structure. The samples were finally capped with a 100 nm-thick GaAs layer grown at 590°C at 1 $\mu\text{m/hr}$. The As/Ga BEP ratio of 25 was maintained for all the GaAs layers. AFM and 5 K PL characterizations were carried out on the samples. The 514.5 nm line of an Ar-ion laser was used as excitation source for the PL measurement. A cooled Ge detector was used in conjunction with a standard lock-in amplification technique to detect the PL emissions.

During growth of all the samples, the RHEED pattern exhibits split (2×2) surface reconstruction following an in-situ thermal anneal of the Ge substrate at 640°C. Such RHEED pattern surface reconstruction indicates the existence of a single sub-lattice domain on the Ge surface. The single domain indicates that the dangling bonds of the surface Ge atoms are oriented in the same direction. It also implies that the steps are of double-atomic height. This happened because prolonged thermal anneal at high temperature causes the Ge atoms to diffuse from energetically unfavorable edges (perpendicular to step-edge) into favorable ones (parallel to step-edge) [62]. Towards the end of the growth process, the samples where the MEE sequence was carried out at substrate temperature of 450°C and 350°C showed a dovetailed RHEED pattern. On the other hand, the sample where the MEE sequence was carried out at 250°C showed (2×4) RHEED pattern reconstruction, which is to be expected from a regular As-rich GaAs surface.

Figure 4-5 shows plots of integrated PL intensity of the InGaAs SQW and AFM root-mean square (RMS) surface roughness of the GaAs cap layer as function of the MEE substrate temperature. It can be clearly seen that as the MEE substrate temperature is lowered, the surface roughness decreased and the PL intensity of the InGaAs SQW significantly improved, indicating a condition of improved structural and optical quality. The surface roughness decreased by 10 times from the sample whose MEE temperature is 450°C to the sample whose MEE temperature is 250°C, while the PL integrated intensity increased by two orders of magnitude.

Figure 4-5 Plot of the 5 K InGaAs SQW PL integrated intensity and the GaAs cap AFM RMS surface roughness from all the samples in this experiment vs. their MEE substrate temperature. The AFM scan area was $5\ \mu\text{m} \times 5\ \mu\text{m}$ in all samples.

In order to further assess the level of improvement obtained, a comparison with a reference sample on a GaAs substrate was performed. The structures of this sample are

identical to the ones grown on the vicinal Ge substrate. The initial GaAs nucleation on this reference sample was also by MEE. Comparing the sample grown on the GaAs substrate with the one grown on offcut Ge with the MEE step carried out at substrate temperature of 250°C, it was found that the sample on the GaAs substrate has a two times smaller GaAs cap surface roughness, three times higher InGaAs SQW PL integrated intensity, and three times smaller InGaAs SQW PL spectra full-width at half maximum (FWHM). These results indicate that the quality of the GaAs layer grown on Ge have nearly reached the quality of homoepitaxial GaAs; further improvements are expected as the GaAs/Ge growth process is optimized further.

Figures 4-6 and 4-7 show the XTEM images of the samples whose MEE were carried out at substrate temperature of 450°C and 250°C, respectively. It is clearly evident that the sample with the MEE step carried out at 450°C contains a large concentration of APB. At such a temperature, evaporation of As dimers from the starting Ge surface could occur, creating As vacancies in the process. Upon opening the Ga shutter, the Ga adatoms arrive at the surface and occupy these As vacancies. If the Ga clusters resided just at the surface step edges, they could be creating APB as seen propagating on the (111) plane. Otherwise, they could be acting as nucleation sites for GaAs islands that may become the origins of stacking faults or other dislocations. From Fig. 4-6, the defects are mostly confined in the (111) plane, indicating they are APB in nature and self-annihilation mechanisms were again observed. However, some APBs do not self-annihilate, but rather get terminated or reflected when they reach the strained-SQW layer as indicated by the arrow in Fig. 4-6. This phenomenon is due to the influence of strain in InGaAs SQW layer, similar to the strained layer superlattice (SLS) layers filter dislocations.

Figure 4-6 XTEM image of the sample whose GaAs MEE nucleation was carried out at 450°C. It can be seen that APB still occurred in this sample. APB self-annihilation mechanisms can be observed from this image. Some APB also stop or change direction when they reached the InGaAs SQW layer.

On the other hand, from the XTEM image shown in Fig. 4-7, it is clear that the APB are well suppressed in the sample with the MEE step carried out at 250°C. The defects at the GaAs/Ge heterointerface are localized within a few nanometers. In this sample, it is likely that the As dimers have covered up the whole surface more uniformly, with few As vacancies. At such low substrate temperature, re-evaporation of As from the surface is expected to be negligible. Furthermore, the migration distance of

the Ga adatoms during the MEE process at low temperature is shorter; possibly even shorter than the average distance (27 Å) between two adjacent step edges of the vicinal surface oriented 6° towards (111). This means that the adatoms could have been absorbed more uniformly on the surface rather than only migrated and be adsorbed on the step-edges.

Figure 4-7 XTEM image of the sample whose GaAs MEE nucleation was carried out at 250°C. It is clear that APB are well-suppressed in this sample, which is mainly attributed to the low substrate temperature during the MEE.

The above XTEM results demonstrate that APB-free GaAs on Ge can be achieved even without prior deposition of epitaxial Ge [65], whose purpose is to bury surface contamination and ensure a clean Ge surface prior to GaAs nucleation. Here, a clean Ge surface was achieved by UV ozone exposure that removed carbon contamination.

Furthermore, the GaAs nucleation temperature in this experiment was very low and due to this, full monolayer surface coverage by As would be easier to achieve. Hence the MEE GaAs could be done possibly at even higher growth rate.

4.3 Blue-shift in the PL emission from embedded quantum well

5 K PL spectra of InGaAs SQW from the samples with the MEE step carried out at substrate temperature, T_s , of 450°C and 250°C are presented in Fig. 4-8. Observation of the InGaAs SQW emission spectra from both samples revealed a shift in the emission peak. Considering that emission in the InGaAs/GaAs quantum well system only comes from electron transitions from the conduction band edge to heavy-hole valence band edge [100], the change in band gap due to strain is given by [101]

$$\Delta E_g = \left[-2a \left(\frac{C_{11} - C_{12}}{C_{11}} \right) + b \left(\frac{C_{11} + 2C_{12}}{C_{11}} \right) \right] \varepsilon \quad (4-1)$$

where C_{11} and C_{12} are elastic constants, a and b are the hydrostatic and shear deformation potential constants, respectively. ε is the biaxial strain parallel to [100] and [010] directions and is given by [104]

$$\varepsilon = \frac{a_{GaAs} - a_{InGaAs}}{a_{InGaAs}} \quad (4-2)$$

Employing equations (4-1) and (4-2), and by linear interpolation of the binary data of GaAs and InAs presented in Table 4-1 [105], the emission wavelength of $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ SQW grown pseudomorphically on GaAs is calculated to be 1.3 eV.

Figure 4-8 Plots of the 5 K PL spectra of the InGaAs QW in the samples with GaAs MEE nucleation temperature, T_s , of 450°C and 250°C. The PL spectra of the sample with MEE T_s of 450°C is fitted with two Gaussian plots (dotted lines).

Parameter	GaAs	InAs
E_0 (eV)	1.425	0.36
C_{11} (dyne/cm ²)	11.88×10^{11}	8.329×10^{11}
C_{12} (dyne/cm ²)	5.38×10^{11}	4.526×10^{11}
a_0 (Å)	5.64191	6.0584
a (eV)	-9.8	-5
b (eV)	-1.76	-1.8

Table 4-1 GaAs and InAs binary data used in the strained InGaAs SQW calculations. The actual values used in the calculations are linearly interpolated for InGaAs SQW with 20 % indium composition.

However, as observed from Fig. 4-8, the emission wavelength of the InGaAs SQW in the sample with the MEE carried out at substrate temperature of 250°C is 1.32 eV, and the InGaAs SQW in the sample with the MEE at substrate temperature of 450°C has split emission wavelength of 1.294 eV and 1.333 eV. The differences in the emission wavelength could be due to indium out-diffusion and/or segregation. Assuming this to be the sole origin of the wavelength shift, the amount of indium out-diffusion causing the InGaAs SQW PL wavelength shift in the sample with the MEE at substrate temperature of 250°C is calculated to be 2 %. In the sample with the MEE at a substrate temperature of 450°C, the calculated indium out-diffusion is 3 %. However, from the XTEM image of this sample as presented in Fig. 4-6, it can be clearly observed that the InGaAs SQW in this sample is distorted due to dislocations. This distortion might have also disturbed the strain distribution, inducing more strain to the InGaAs SQW and caused the shift in the emission wavelength. Another possible cause of the wavelength shift might be due to some partial chemical ordering mechanisms due to the offcut orientation used in this experiment [106], but more investigations need to be done before the cause of the InGaAs SQW wavelength shift in these samples could be accurately determined.

4.4 Summary

APB occurrences in GaAs/Ge heteroepitaxy were effectively suppressed by combining both vicinal Ge surface and low temperature (250°C) initial nucleation by MEE. The observed APB self-annihilation mechanism on both nominal and vicinal surfaces contributed to the width of surface steps and the initial nucleation energy. APB with lower energy might change their propagation direction, from the initial (110) plane into a plane with higher index but less energetic, such as the (112) plane. In GaAs grown on a vicinal Ge surface, the APB propagate mainly on (111) planes. This makes

self-annihilation occur much earlier, preventing APB to propagate into the active region. This is shown by a 40 times improvement in the optical quality of the InGaAs SQW in the sample with no APB.

The low temperature (250°C) initial nucleation ensured complete As dimer coverage on the double-atomic step Ge surface and ensured that the growth mode lies within the two-dimensional growth mode. Surface roughness as measured by AFM was reduced by 10 times in the sample grown with MEE at 250°C, the lowest in this experiment, while the InGaAs SQW PL integrated intensity improved by two orders of magnitude. Moreover, comparison with a reference sample of the same structures grown on a GaAs substrate demonstrated that the quality of the GaAs layer grown on a Ge substrate is comparable to homoepitaxial GaAs, and further improvements of the heteroepitaxial GaAs can be expected. A shift in the InGaAs SQW PL emission wavelength was also observed, and it is attributed mainly to the indium out-diffusion mechanism and dislocation-induced strain.

Chapter 5 Heteroepitaxial Growth of GaAs on Graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ Substrate

In this chapter, heteroepitaxial growth of GaAs on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates is investigated. Having established the importance of the misoriented Ge surface and low-temperature MEE GaAs nucleation in the preceeding chapter, such growth conditions are used for GaAs growth on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. Furthermore, characteristics of AlGaAs/GaAs heterojunction-bipolar transistor (HBT) grown on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate is investigated to explore the viability of the integrated platform.

5.1 Graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate

Fitzgerald, *et al.* have worked on the graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer to realize a virtual vicinal Ge substrate on Si [23, 107]. Employing cleverly designed grading and chemical mechanical polishing (CMP) to eliminate surface roughness that may lead to dislocation pinning and pile up, a good quality Ge layer with dislocation density in the mid 10^5 cm^{-2} has been achieved [24]. To maintain low TDD, the kinetics for dislocation glide in the graded layers need to be maximized while the nucleation rate of new dislocations is minimized. High growth temperatures and relatively low strain grading rates during the growth of graded $\text{Si}_{1-x}\text{Ge}_x$ layers serve to increase the effective dislocation glide velocity at the graded buffer interfaces. This is to increase the total misfit segment lengths of the existing dislocations, and thus be able to efficiently relieve large amounts of misfit strain before reaching the surface. In addition, to minimize the nucleation of new dislocations during $\text{Si}_{1-x}\text{Ge}_x$ graded buffer growth, pre-existing dislocations should be allowed to move easily through the film to avoid dislocation pileups.

Surface roughness occurring naturally in graded buffer layers can induce dislocation pileups. This surface roughness is typically in the form of an orthogonal network of parallel ridges and troughs on the graded buffer surface and is commonly called “crosshatch” patterns. “Crosshatch” is caused by low residual amounts of strain which remain in the top layers of the $\text{Si}_{1-x}\text{Ge}_x$ graded buffer during growth. During growth at elevated temperature, this residual elastic strain tries to relax by introducing undulations in the film surface. The constant strain rate occurring in the $\text{Si}_{1-x}\text{Ge}_x$ graded buffer makes this undulation propagate to the top of the buffer layer. Fitzgerald *et al.* have found that by stopping the growth at 50% Ge and performing a CMP process to remove surface undulations [58], dislocation pileups can be reduced dramatically in the graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer. The $\text{Si}_{1-x}\text{Ge}_x$ graded buffer layer produced using this technique exhibits only a slight increase in TDD with increasing Ge content from 50 %–100 %. A XTEM image of the final $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate, with $x=0$ to 1 is shown in Fig. 5-1. A network of misfit dislocations can be observed within the graded buffer interfaces, without obvious threading dislocations reaching the surface of the pure Ge cap layer. The TDD level routinely achieved on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate is $\sim 1 \times 10^6 \text{ cm}^{-2}$.

Figure 5-1 XTEM image of the $\text{Si}_{1-x}\text{Ge}_x$ graded buffer with a $1\mu\text{m}$ Ge cap on misoriented Si substrate.

5.2 Realizing good quality GaAs on $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates

To realize good-quality GaAs on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate, several growth parameters need to be reconsidered as it is certainly different from growing GaAs on a Ge substrate. First and foremost, the substrate material and thickness is different. The $\text{Si}_{1-x}\text{Ge}_x$ graded buffer is grown on a Si substrate, which in this case is $\sim 1.5\times$ the thickness of the Ge substrate employed previously. Coupled with differing thermal expansion and thermal conductivity, this brings about issues on controlling substrate temperature during growth. The issue of strain development due to differing thermal expansions have been tackled in the design of the graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer. Nonetheless, at elevated growth temperature, the pure Ge layer will be under slight compressive thermal strain of $\sim 0.2\%$. Another factor is the thermal conductivity of the substrates. Since Si is twice as good a thermal conductor as Ge [108], the thermal

conduction from the heater to the substrate surface is actually better in the Si substrate. With these differences in mind, slower thermal cycle rates were employed to accommodate differing thermal conductivity and expansion in the Ge, $\text{Si}_{1-x}\text{Ge}_x$ graded buffer and Si substrate.

Optimized growth processes achieved in GaAs/Ge heteroepitaxy were employed to grow GaAs on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The sample underwent similar preparation procedures except for a higher thermal degassing temperature at 500°C prior to loading into growth chamber. It was found that the thermal oxide desorption was consistently achieved at 640°C . The *in-situ* thermal annealing of 20mins in the MBE growth chamber produced the split (2×2) streaky RHEED pattern, indicative of a double-atomic steps Ge surface. The growth started by depositing 10 ML of GaAs at $0.25\text{ }\mu\text{m/hr}$ using MEE at 250°C , followed by $\sim 1\text{ }\mu\text{m}$ GaAs deposition by MBE at 580°C . An XTEM image of the sample is shown in Fig. 5-2. The resulting GaAs layer is APB-free, which clearly demonstrates the effectiveness of the low-temperature MEE process on a vicinal Ge surface.

Figure 5-2 XTEM image of $\sim 1\mu\text{m}$ GaAs layer grown on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate.

Apart from the differences in thermal property, there is a difference in the TDD level between the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate and the Ge substrate. TDD in the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ is $\sim 1 \times 10^6 \text{ cm}^{-2}$, but TDD in a typical Ge substrate is at least 2 orders of magnitude lower. Therefore, it is crucial to understand the impact of higher TDD level on the device performance. In order to do this, Chen *et al.* [109] have compared p-n junctions at various distances from the GaAs/Ge heterointerface with a reference device grown on a GaAs substrate. Three separate samples (A, B, C) with identical GaAs p-n diodes were grown on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate with buffer thickness of 600nm, 300 nm, and 50 nm, respectively. Fig. 6-3 shows the reverse biased characteristics of these diodes. Sample D is the reference sample with identical device structure grown on

GaAs substrate. The results in Fig. 6-3 indicate that devices grown beyond 300 nm away from the GaAs/Ge heterointerface (samples A and B) perform favourably compared to the one on GaAs substrate. Degradation in epitaxy quality, and thus inferior breakdown and higher leakage current, occur as the buffer layer thickness is below ~ 300 nm.

Figure 5-3 Reverse biased characteristic of GaAs p-n diodes grown on the Ge/SiGe/Si substrate with different GaAs buffer thickness. The control sample (sample D) was an identical GaAs diode grown on a GaAs substrate [109].

Although a thicker buffer layer of ~ 600 nm shows excellent epitaxy quality, the total GaAs thickness is limited by a cracking threshold due to the thermal expansion difference between the GaAs material and the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate [50]. In the case of MBE grown GaAs, the difference between growth temperature and ambient, ΔT , is 550°C - 580°C . Therefore, according to the theoretical and experimental results shown

in Fig. 5-4 [50], the critical thickness prior to cracking, t_c , of the III-V compound semiconductor layer on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate is $\sim 3\ \mu\text{m}$. This should be used as firm upper limit when designing device layer structures on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate.

Figure 5-4 Plots of theoretical (dashed line) and experimental (■) critical cracking thickness, t_c , for GaAs grown on $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate as function of ΔT [50].

5.3 Characteristics of AlGaAs/GaAs Heterojunction Bipolar Transistor (HBT) on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate

As a minority carrier device, a HBT is sensitive to defects or deep-level centers and thus is ideally suited to demonstrate the viability of the integrated platform. The low TDD of $\sim 10^6\ \text{cm}^{-2}$ in the integrated GaAs/ $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ platform should improve the carrier lifetimes and result in a high device current gain, compared to previously reported HBTs on Si substrates [110]. In addition, low TDD would also lead to a smaller reverse-biased base-collector junction leakage current. A large value of leakage

current is undesirable, especially for power HBT application, since it reduces both breakdown voltage and output power and causes reliability problem. This section presents the first experimental radio-frequency (RF) performance of an AlGaAs/GaAs HBT grown on a graded Si_{1-x}Ge_x/Si substrate. The devices were fabricated and characterized by Dr. Lew Kim Luong. The HBT device structure is shown in Table 5-1. The sample underwent similar preparation procedures as discussed in the preceeding section. The initial GaAs nucleation on the Ge surface was done using MEE at 250°C prior to the growth of 300 nm buffer GaAs layer by standard MBE at 590°C. Such a thin buffer was employed so as avoid cracking when the full device structure undergone thermal cycles [111]. The HBT devices were fabricated using standard mesa etching techniques. A Ti/Au p-metal contact and Ni/Ge/Au/Ni/Au n-metal contact were deposited using a standard electron beam deposition technique.

Emitter cap	In _{0.2} Ga _{0.8} As:Si	20 nm	1x10 ¹⁹ cm ⁻³
Emitter cap	GaAs:Si	200 nm	5x10 ¹⁸ cm ⁻³
Emitter	Al _{0.25} Ga _{0.75} As:Si	100 nm	5x10 ¹⁷ cm ⁻³
Spacer layer	GaAs	5 nm	intrinsic
Base	GaAs:Be	45 nm	1x10 ¹⁹ cm ⁻³
Collector	GaAs:Si	300 nm	5x10 ¹⁶ cm ⁻³
Sub-collector	GaAs:Si	200 nm	5x10 ¹⁸ cm ⁻³
Buffer	GaAs	300 nm	intrinsic
MEE	GaAs	10 ML	intrinsic
Graded Si _{1-x} Ge _x /Si substrate			

Table 5-1 Layer structure of the HBT grown on graded Si_{1-x}Ge_x/Si substrate.

Figure 5-5 shows the common-emitter current-voltage (I-V) characteristic of the HBT with emitter area of $\sim 1.6 \times 10^{-5} \text{ cm}^2$. At room temperature, the device exhibited current gain of ~ 15 at collector current of 15 mA. The collector-emitter offset voltage ($V_{\text{CE}(\text{offset})}$) and knee voltage (V_k) are $\sim 250 \text{ mV}$ and $\sim 1 \text{ V}$, respectively. These results are comparable to the performance observed in the reference AlGaAs/GaAs HBT on GaAs substrate as shown in Fig. 5-6, with $V_{\text{CE}(\text{offset})}$ and V_k of $\sim 200 \text{ mV}$ and $\sim 0.8 \text{ V}$, respectively. Figure 5-7 shows the current gain (β) vs. collector current (I_C) of the HBT on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. A maximum current gain (β) of ~ 40 is achieved, which is large enough for microwave applications. Figure 5-8 shows the RF performance of the HBT. As shown in the figure, the cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) are 20 GHz and 13 GHz, respectively for a $2 \times 15 \text{ } \mu\text{m}^2$ emitter area device. The f_{max} value is compromised by the thin base layer (45 nm, 10^{19} cm^{-3} Be-doped) used in the HBT. This could be improved if the base doping level is increased by using carbon as the p-type dopant. Compared to a similar device grown on a GaAs substrate, the f_t value is lower due to the higher emitter contact resistance, which can be further improved by increasing the indium composition in the emitter cap layer and optimizing the contact annealing condition.

Figure 5-5 Common-emitter characteristics of the AlGaAs/GaAs HBT on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The base current is stepped from 0 to 1 mA in 50 μA increments.

Figure 5-6 Common-emitter characteristics of an AlGaAs/GaAs HBT on GaAs substrate. The base current is stepped from 0 to 0.5 mA in 50 μA increments.

Figure 5-7 Plot of current gain vs. collector current at room temperature of the AlGaAs/GaAs HBT on graded Si_{1-x}Ge_x/Si substrate.

Figure 5-8 Common emitter current gain (H_{21}) and unilateral gain (U) of the AlGaAs/GaAs HBT on graded Si_{1-x}Ge_x/Si substrate.

5.4 Summary

In this chapter, details of graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates were discussed along with the differences in the GaAs growth parameters on this platform compared to GaAs growth on Ge substrates. After optimization, an APB-free GaAs layer can be realized employing similar growth conditions for APB-free GaAs on Ge substrate. An AlGaAs/GaAs HBT was grown on the integrated platform and it was found to exhibit a maximum current gain of ~ 40 , which is an acceptable value for microwave application. Furthermore, the cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) of the HBT were found to be 20 GHz and 13 GHz, respectively. The f_{max} value is compromised by the thin base layer and could be improved if the base doping level is increased by using carbon as a p-type dopant. Compared to a similar device grown on a GaAs substrate, the f_t value is lower due to higher emitter contact resistance, which can be further improved by increasing the indium composition in the emitter cap layer and optimizing the contact annealing condition.

Chapter 6 Growth of InAs QD Structures for 1.3 μ m Emission on Graded Si_{1-x}Ge_x/Si Substrate

High-performance HBTs on graded Si_{1-x}Ge_x/Si substrates demonstrate the viability of the platform for minority carrier devices. The next step is to investigate the growth of self-assembled quantum dot (QD) structures on this platform. InAs/GaAs QD structures were selected due to their potential in emitting at 1.3 μ m without requiring complex active layer structures. Nevertheless, it is crucial to obtain large-enough InAs QD to emit at such a wavelength and this is challenging as large QD tends to induce defects during capping. Furthermore, the areal density of the QD structures has to be high in order to achieve high gain or efficiency in light-emitting devices.

6.1 Defects suppressions employing InGaAs strain-reducing layer

Ideal quantum dot (QD) based devices promise to deliver improved performance due to the three-dimensional carrier confinement and delta-like density of states in these structures [39]. QD-based high-speed optoelectronic devices grown on Si substrates will play a crucial role in future optical interconnects in Si integrated circuits. Although QD structures grown on Si substrates have been reported [112-115], a study of defect mechanisms and defect suppression during capping of the QDs on Si substrate is still lacking. In order to achieve high-performance QD-based devices, one of the most important requirements is to achieve defect-free QD structures. The defect-free regions have to be realized both inside the QD structures as well as the layer surrounding the QDs. Occurrence of defects in either region will have detrimental effects on the QD

optical efficiency and QD-based device lifetime [116]. Defects during capping of self-assembled QD structures are likely to occur due to excess strain which causes plastic deformation of the capping layer. In typical InAs QD structures grown on GaAs and capped with a GaAs layer, defects in the capping layer are commonly observed, especially around large InAs QDs [117]. On the other hand, one needs to extend the size of the InAs QDs on GaAs in order to achieve 1.3 μ m emission wavelength, which is important for high-speed optical communication [118]. This section discusses the effects of capping the InAs QDs by an In_{0.1}Ga_{0.9}As layer to suppress defects and to realize 1.3 μ m emission on a graded Si_{1-x}Ge_x/Si substrate.

Four samples, labelled A to D, were prepared for this study. The experimental parameters related to the four samples are listed in Table 6-1. Sample D was grown on GaAs substrate and serves as a reference in this study. In samples A to C, the compositionally graded Si_{1-x}Ge_x layers, with $x=0$ to 1, were grown using chemical vapor deposition (CVD) on a (100) oriented Si substrate with 6° off-cut towards the {111} plane [24]. The GaAs layer grown in samples A to C were initiated by low-temperature MEE nucleation which effectively suppressed anti-phase boundary defects and yield device-quality GaAs layer [119]. A GaAs buffer layer of at least 300 nm thick was grown in all four samples prior to the InAs QD layer. The InAs QD layer was grown at 450°C using alternate-beam molecular beam epitaxy (MBE) [120] at 0.1 monolayer (ML)/sec. The InAs monolayer coverage (θ_c) used lies within the range where the QD formation process has stabilized [118]. The InAs QD structures in samples A and D were immediately capped with a 50 nm-thick GaAs layer. On the other hand, the InAs QD structures in samples B and C were immediately capped with a 5 nm-thick In_{0.1}Ga_{0.9}As layer followed by a 40 nm-thick GaAs layer. The samples were characterized by TEM and PL using the 5145 Å line of an Ar⁺ laser. The PL signals

were detected using a liquid nitrogen cooled germanium detector in conjunction with a standard lock-in technique.

Sample ID	Substrate type	InAs monolayer coverage (θc)	Capping layer
A	Si _{1-x} Ge _x /Si	2.6 ML	GaAs
B	Si _{1-x} Ge _x /Si	2.6 ML	In _{0.1} Ga _{0.9} As
C	Si _{1-x} Ge _x /Si	2.9 ML	In _{0.1} Ga _{0.9} As
D	GaAs	2.6 ML	GaAs

Table 6-1 Details of the QD samples used in this study. Samples A to C were grown on graded Si_{1-x}Ge_x/Si substrate while sample D was grown on GaAs substrate and used as a reference.

Bright-field (BF) cross-sectional TEM images of samples A to D are presented in Figs. 6-1(a) to 6-1(d), respectively. The average aspect ratio, defined as QD height over base width, of the QDs in samples A to D are 0.15 ± 0.04 , 0.20 ± 0.06 , 0.27 ± 0.1 , and 0.12 ± 0.01 , respectively. The QDs capped with GaAs have smaller aspect ratio compared to the ones capped with an In_{0.1}Ga_{0.9}As layer. It was found that the QDs in samples A and D take on a truncated pyramid shape, whereas the QDs in samples B and C take on a lens-shape. The InAs QDs capped with GaAs take on a truncated pyramid shape because of collapse in the QD height as deposited material migrated from the top of the QDs towards the surrounding capping layer [121]. On the other hand, the In_{0.1}Ga_{0.9}As capping layer leads to the formation of QDs with a more isotropic shape [122]. This has been attributed to several reasons, namely, segregation of In atoms from the In_{0.1}Ga_{0.9}As capping layer at the top of the QDs [123], reduction in In migration from the QDs to the capping layer due to smaller surface chemical potential gradient, and reduction in strain due to smaller lattice mismatch between the QDs and the capping layer [121].

Figure 6-1 Bright-field (BF) cross-sectional TEM images of the InAs QDs in (a) sample A, (b) sample B, (c) sample C, and (d) sample D. V-shaped defects are seen in the samples with GaAs capping layer. InAs QDs capped with GaAs layer have a truncated pyramid shape, whereas the ones capped with In_{0.1}Ga_{0.9}As layer have a lens shape.

It was discovered that V-shaped defects were the dominant defect type in samples A and D. On the contrary, V-shaped defects were not found in samples B and C within the limit of observation. V-shaped defects are seen to be located symmetrically at both

top edges of the truncated pyramid QDs. This type of defect typically consists of two pairs of dislocations propagating in different $\{111\}$ planes from the QDs through the capping layer towards the surface [117]. Unlike previously reported observations [117, 124], the V-shaped defects observed in samples A and D do not originate from the edges at the QD base region. The V-shaped defects observed in samples A and D originated from the region around the top edges of the truncated pyramid QDs. The strain in self-assembled QDs reaches a maximum value at the base edges and it increases as each new atom is incorporated into the QD [124]. When the QD size reaches a critical value [118], it may become energetically unfavourable for more atoms to be incorporated into the QD base edges. It is therefore necessary for the atoms to find a lower energy position. In the case of a truncated pyramid QD, this position lies at the top edges where the apex is removed, as shown by the arrows in Fig. 6-2(a). Atoms migrating from the QD apex into the GaAs capping layer might be incorporated into these edges and form partial dislocations or stacking faults which extend to the capping layer [117, 125]. It is noteworthy that the symmetrical arrangement of the V-shaped defects might indicate a symmetrical rate of atoms migration from the QD apex to the GaAs capping layer. On the other hand, in the case of the In_{0.1}Ga_{0.9}As capping layer, the interplay between the reduced strain and the reduced chemical potential between the InAs QDs and the capping layer might be responsible for the absence of the V-shaped defects in samples B and C; with the reduced strain playing a more important role. Clear evidence of this is seen from the absence of dislocations around a large coalesced InAs island as shown in Fig. 6-2(b), with base width of ~ 50 nm and height reaching 20 nm. The arrow in Fig. 6-2(b) indicates the intersection of two coalesced QDs.

Figure 6-2 (a) BF cross-sectional TEM images of an InAs QD from sample D with a V-shaped defect. The arrows point to the origin of the defect at the top-edges of the truncated pyramid QD. (b) BF cross-sectional TEM images depicting large coalesced InAs QDs capped with In_{0.1}Ga_{0.9}As layer from sample C. No defect is observed around the QD. The arrow points to the intersection of two coalesced InAs QDs.

Temperature-dependent PL measurements were carried out to provide greater insight into the PL characteristics of the samples. Samples A and D show strong thermal quenching that basically rendered the PL emission beyond 60 K undetectable. Since the V-shaped defects are found to have an activation energy of 0.52 eV [126], this forms a deep level state in the GaAs capping layer. The carriers from the QDs can easily escape to this deep level, giving rise to the strong thermal quenching effect observed in these samples. On the other hand, samples B and C exhibit much slower thermal quenching

and, as shown in the inset of Fig. 6-3, emit strong PL signals at room-temperature (RT) with emission wavelength of 1.22 μ m and 1.3 μ m, respectively. The Arrhenius plots of the temperature-dependent integrated PL intensity for samples B and C are shown in Fig. 6-3. At temperatures beyond 77 K, the curves display an exponential thermal quenching characteristic which is proportional to $\exp(E_a/kT)$ due to thermal escape of carriers from the dots and non-radiative capture of carriers by extrinsic defects with thermally activated capture cross-section. Two activation energies E_{a1} and E_{a2} for each sample were deduced by measuring the slopes of the curves at these strong thermal quenching regimes [127]. The activation energy deduced by this method is the total binding energy, which includes the confinement energy and exciton binding energy [128]. The softer decay region between 77 to 150 K corresponds to activation energies E_{a2} of (4 ± 0.5) meV and (19 ± 1) meV for samples B and C, respectively. The sharp decay region beyond 200 K corresponds to activation energies E_{a1} of (103 ± 12) meV and (136 ± 10) meV. From the inset in Fig. 6-3, the QD ground-state RT energy levels for samples B and C are 1.014 eV and 0.954 eV, respectively. Given the same capping layer composition and thickness, the barrier height difference between samples B and C is ~ 60 meV. Therefore, the E_a of sample C should have been 130 meV instead of 110 meV as deduced earlier. The smaller E_a might be due to the presence of large coalesced InAs islands in this sample. These large islands act as non-radiative recombination centres with barrier height smaller than that of the QD-to-capping layer. The effects of these non-radiative recombination centres can also be seen from Fig. 6-3 as the integrated RT PL intensity of sample C reduces significantly by five times as compared to sample B.

Figure 6-3 Arrhenius plots of the temperature-dependent integrated PL intensity for samples B and C. (Inset) Room-temperature PL spectra of samples B and C.

6.2 Effects of InAs monolayer coverage on QD areal density

In this section, the effects of InAs monolayer coverage on the QD areal density are investigated. InAs deposition in this study was performed at 450°C because at this low temperature, the adatom migration length is reduced and impinging adatoms are more likely to form new sites on the surface instead of combining with existing dots [129]. Such conditions are desirable to realize a high-areal density QD ensemble. The sample structure used in this study is shown in Fig. 6-4. A (100)-oriented Si substrate misoriented 6° towards the (111) plane was employed. The GaAs growth was initiated by low-temperature MEE [119]. All the QD layers were grown at a rate of 0.1 monolayer/sec (ML/sec) by alternate-beam molecular beam epitaxy [120]. This technique prolongs the dislocation-free growth mode to form larger QDs, for longer

emission wavelength. This technique has been shown to increase the QD areal density [90] when employed to grow InAs QDs on vicinal surface. Capping the InAs QDs with a thin In_{0.1}Ga_{0.9}As strain-reducing (SR) layer reduces the strain component along the growth direction, resulting in smaller strain-induced bandgap [130]. The inclusion of the In_{0.1}Ga_{0.9}As SR layer has been shown to reduce localized strain by nearly 20 % [131] and to suppress V-shaped defects as shown in section 6.1. The 33 nm-thick GaAs spacer layer was employed to decouple the electronic and strain effects of the stacked QD layers [132].

Figure 6-4 Schematic diagram of the sample structure. Three samples with InAs deposition thickness, θ_c , of 1.9 ML, 2.6 ML, and 2.9 ML, respectively were studied.

This study involves three samples with an InAs θ_c of 1.9 ML, 2.6 ML and 2.9 ML, respectively. From the 1 $\times$ 1 μ m² AFM scans presented in Fig. 6-5(a), the areal density of the exposed QD layer reached a maximum of 7 $\times$ 10¹⁰ cm⁻² when θ_c = 2.6 ML. This areal density is comparable to the highest reported InAs QD density on GaAs substrates

grown by alternate-beam MBE [133]. Such a high QD areal density is important for potentially obtaining high modal gain or high efficiency and ground-state emission in QD-based emitters on Si-based platforms. There have been reports on preferential nucleation of Ge QDs along cross-hatched lines, more specifically on the hills of the undulated surface of the graded Si_{1-x}Ge_x/Si substrate [134, 135]. This undulation also appears on the GaAs surface grown on the graded Si_{1-x}Ge_x/Si substrate. However, as seen from the $5 \times 5 \mu\text{m}^2$ AFM scan of the InAs QDs ensemble with $\theta_c = 2.6$ ML presented in Fig. 6-5(b), such preferential QD nucleation was not observed. Further magnification of the $1 \times 1 \mu\text{m}^2$ area inside the square clearly shows the presence of InAs QDs on the hills as well as in the valleys, without any sign of preferential nucleation. This observation suggests that the dislocation strain field is more uniformly distributed on the GaAs surface, or the smaller elastic constants of the GaAs layer compared to Si and Ge prohibit large structural modification by dislocation slips [134].

From Fig. 6-5(a), the average QD base-width (W_{QD}) of the InAs QDs is found to be at least two times larger than the value reported for typical InAs QDs grown on GaAs substrate [129, 133]. The average W_{QD} increases following an increase in θ_c from 1.9 ML to 2.9 ML, with islands as wide as 90 nm observed at $\theta_c = 2.9$ ML. The aspect ratio (QD height/QD base-width) of 0.08 ± 0.005 was found to be unchanged regardless of θ_c variation. The large yet flat InAs QDs might be the consequence of having a pure compressive Ge layer on the graded Si_{1-x}Ge_x/Si surface. The compressive Ge cap layer is to suppress microcracks due to the large tensile strain created as the Si substrate expands/contracts at a rate double that of Ge or GaAs during the growth temperature cycle [58]. However, at elevated growth temperature, GaAs grown on the compressive Ge layer will incorporate this compression, and this leads to a negative intrinsic surface stress tensor, favoring lateral expansion of the QDs.

Figure 6-5 (a) $1 \times 1 \mu\text{m}^2$ AFM scans of the exposed InAs QDs layer with 1.9 ML, 2.6 ML, and 2.9 ML InAs deposition thickness, respectively. Below the AFM scans is a plot of the effects of θ_c variation on the QDs areal density and QDs average base-width. The lines are guide to the eyes. (b) $5 \times 5 \mu\text{m}^2$ AFM scan of the InAs QDs ensemble with 2.6 ML InAs deposition thickness. The area inside the square is $1 \times 1 \mu\text{m}^2$.

The RT PL emission wavelength red-shifted from 1.05 μm to 1.3 μm when θ_c was varied from 1.9 ML to 2.9 ML, with a near-linear relationship, as seen in the inset of Fig. 6-6(a). The energy states in the QDs decrease monotonically following the increase in QD size; or $E \sim \text{size}^{-\gamma}$, where γ refers to the dependency factor [136]. As the aspect ratio of the QDs was found to be nearly constant across the θ_c variation, the effective volume of the QDs increases following increase in θ_c . This results in decrease in the energy states due to reduction in the carrier confinement effect.

To correlate the QD's base-width to the RT PL emission wavelength, we employed a simplified model of a quantum box with infinite barrier height [136]. By considering only the electron ground state energy E_{e1} and heavy hole ground state energy E_{hh} , the InAs QD ground state energy at RT can be expressed as:

$$E_g(300\text{K}) = E_{\text{InAs}}(300\text{K}) + E_{e1} + E_{hh} \quad (6-1)$$

where

$$E_{e1(hh)} = \frac{\hbar^2 \pi^2}{2m_{e1(hh)}^*} \left[\left(\frac{1}{L_x^2} \right)^2 + \left(\frac{1}{L_y^2} \right)^2 + \left(\frac{1}{L_z^2} \right)^2 \right] \quad (6-2)$$

with $E_{\text{InAs}}(300\text{K}) = 0.55 \text{ eV}$, $m_{e1}(\text{InAs}) = 0.04m_0$ and $m_{hh}(\text{InAs}) = 0.59m_0$. Here L_z represents the height of the QDs and $L_x = L_y$ as we assume a lens-shaped QD. Taking the aspect ratio as 0.08 ± 0.005 , RT PL emission wavelength of 1.3 μm corresponds to QDs with base-width of $\sim 63 \text{ nm}$, consistent with the QD base-width observed from the sample with $\theta_c = 2.9 \text{ ML}$.

Figure 6-6(b) shows the effects of θ_c on the PL integrated intensity and full width at half-maximum (FWHM). As expected, the PL integrated intensity is the highest from the sample with the highest QD areal density. The drastic drop in PL intensity at $\theta_c = 2.9 \text{ ML}$ might be attributed to non-radiative recombination centers around defects

created by large InAs islands. In this sample, smaller InAs QDs (~60 nm) are optically active while larger InAs dots/islands (>80 nm) are optically inactive [117]. Therefore, they behave as non-radiative recombination centers detrimental to the PL efficiency. On the other hand, the PL FWHM improves by 40 % from 110 nm at $\theta_c = 1.9$ ML to 65 nm at $\theta_c = 2.9$ ML. This FWHM value is about two times higher than the value reported for InAs QDs grown on GaAs substrates [130]. The PL FWHM narrows as the QDs size variation is smaller in the sample with $\theta_c = 2.9$ ML compared to the QDs size variation in the sample with $\theta_c = 1.9$ ML. The QD base-width standard deviation, σ , was found to be 6.6 nm in the sample with $\theta_c = 1.9$ ML. Excluding QDs larger than 80 nm from calculation, σ was calculated to be 4.5 nm in the sample with $\theta_c = 2.9$ ML.

Figure 6-6 (a) Plot of RT PL spectra of the InAs QDs as function of InAs θ_c . (Inset) Plot of the PL peak wavelength as function of θ_c variation. (b) Plot of the PL line-width and PL integrated intensity as function of θ_c variation. The lines are guide to the eyes.

Figure 6-7 shows the temperature dependence of the InAs QDs optical property. The PL intensity quenches by two-orders of magnitude in all samples when the

temperature was varied from 5 K to RT. The high rate of quenching indicates the high density of carriers escaping to the wetting/barrier layer and non-radiative recombination centers. The weaker carrier confinement of the In_{0.1}Ga_{0.9}As barrier layer compared to the GaAs barrier enhances the carrier escape rates. From Fig. 6-7, evidence of carrier hopping among QDs was observed as the PL FWHM reaches a minimum at 100 K in all three samples. The carrier hopping, typically observed at 100 -150 K, occurs from QDs with a high energy state to QDs with a low state, resulting in a narrowing of the PL FWHM followed by a red-shift in the PL peak wavelength [137].

Figure 6-7 Plot of the PL integrated intensity and PL line-width as function of temperature. The PL intensity quenches by two-orders of magnitude in all three samples from T = 5 K to RT. Evidence of carrier hopping is observed at T = 100 K, where the FWHM reaches a minimum value.

6.3 Summary

The effectiveness of In_{0.1}Ga_{0.9}As capping layer for strain reduction around the InAs QDs leading to realization of large and defect-free QDs grown on graded Si_{1-x}Ge_x/Si substrates which exhibit RT PL at 1.3 μ m were demonstrated in this section. The InAs QD structures capped with an In_{0.1}Ga_{0.9}As layer were found to have a slower thermal quenching rate as compared to the ones capped with a GaAs layer due to the absence of V-shaped defects. A dense ($7 \times 10^{10} \text{ cm}^{-2}$) InAs QDs ensemble was grown on graded Si_{1-x}Ge_x/Si substrate using alternate beam MBE. The InAs QDs are at least two times larger and have smaller aspect ratio compared to typical InAs QDs on GaAs substrates. At an InAs θ_c of 2.9 ML, 1.3 μ m RT PL emission was achieved with a FWHM of 65 nm. At this θ_c , optically-inactive large InAs dots/islands (>80nm) occur alongside optically-active smaller InAs QDs. Hence, although the size variation of optically-active QDs is smaller, as deduced from the narrowing of the PL FWHM, the integrated PL intensity drops significantly due to the optically-inactive large islands observed in this sample.

Chapter 7 Characteristics of InAs/In_{0.1}Ga_{0.9}As QD LEDs Grown on Graded Si_{1-x}Ge_x/Si Substrate

Employing the growth conditions achieved in previous section, an InAs/InGaAs QD LED emitting at 1.29 μm was fabricated. The characteristics of the LED are discussed in this chapter.

7.1 InAs/In_{0.1}Ga_{0.9}As QD LED structure

Realization of a LED on a Si substrate has been attempted by employing rare-earth ion implanted Si in the active region [138] and Si QD structures [139]. However, the LEDs only operate at the low temperature of 80 K. On the other hand, on InGaAs/GaAs QD-based laser on a Si substrate was recently demonstrated [140] but the emission wavelength is below the technologically important 1.3 μm . Furthermore, a study on various recombination processes in the QD-based LED grown on Si substrate is still lacking. In this section, 1.29 μm emission from InAs QD-based LED grown on graded Si_{1-x}Ge_x/Si substrates is demonstrated. The LED external efficiency as function of injected current is investigated and the dominant carrier recombination processes are identified.

Figure 7-1 shows the dark-field (DF) cross-sectional transmission electron microscope (TEM) image of the LED structure accompanied by a schematic diagram of the structure. The LED structure was monolithically grown on a graded Si_{1-x}Ge_x/Si substrate. The compositionally graded Si_{1-x}Ge_x layers, with $x=0$ to 1, were grown using chemical vapor deposition (CVD) on a (100) oriented Si substrate with 6° off-cut towards the {111} plane [24]. The initial GaAs nucleation on the Ge surface was

performed by low temperature migration enhanced epitaxy (MEE) [119]. The n-type GaAs layer and n-type Al_{0.3}Ga_{0.7}As cladding layer were doped with Si at $3 \times 10^{18} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, respectively. The active region consists of a 5-layer stacked self-assembled InAs QD structure grown at 450°C by alternate-beam molecular beam epitaxy (MBE) [120] and capped with In_{0.1}Ga_{0.9}As strain-reducing (SR) layer. Details of the QD growth conditions are presented earlier. The InAs monolayer coverage was set to 2.6 ML at deposition rate of 0.1 monolayer/sec (ML/s). The previous chapter has shown that this condition results in an InAs QD ensemble with areal density of $\sim 7 \times 10^{10} \text{ cm}^{-2}$. Finally, the p-type Al_{0.3}Ga_{0.7}As cladding layer and p-type GaAs layer were doped with Be at $5 \times 10^{17} \text{ cm}^{-3}$ and $2 \times 10^{19} \text{ cm}^{-3}$, respectively. The interfaces between the GaAs and AlGaAs were abrupt, and no compositional grading was done. Both top and bottom Al_{0.3}Ga_{0.7}As cladding layers were doped to ensure that there is less heating due to high-resistivity of undoped cladding layers. Lastly, the thin top Al_{0.3}Ga_{0.7}As cladding layer was designed to avoid carrier reabsorption by the cladding layer.

Figure 7-1 Dark-field (DF) cross-sectional TEM image of the LED structure, accompanied by a schematic diagram of the sample.

7.2 LED characteristics

A bright-field (BF) cross sectional TEM image of the InAs/In_{0.1}Ga_{0.9}As QD layers is shown in Fig. 7-2. No vertical coupling between the QD layers is observed, suggesting negligible strain-induced coupling between the QD layers [141]. This is attributed to the 30 nm-thick GaAs spacer layer and the use of the In_{0.1}Ga_{0.9}As SR layer [131]. The InAs QDs were found to take on a lens shape, which is consistent with previous report on InAs QDs capped with an In_{0.1}Ga_{0.9}As SR layer [122]. Furthermore, no defects or dislocations were observed within the field of observation in the cross-sectional TEM images. The average InAs QD base width and height were 29±3 nm and

6.7±0.8 nm, respectively. This translates to an aspect ratio (defined as QD height over QD width) of 0.23±0.05.

Figure 7-2 Bright-field (BF) cross-sectional TEM image of the InAs/In_{0.1}Ga_{0.9}As QD layers. No vertical coupling between the QD layers was observed.

The fabricated device is a 600 μm-diameter mesa surface emitting LED with ring contacts. Ti/Au p-metal contact was deposited on the GaAs:Be layer and a Ni/Ge/Au/Ni/Au n-metal contact was deposited on the GaAs:Si layer. Mesas to a depth of ~600 nm were defined by standard optical lithography and wet chemical etching. A schematic diagram of the LED is shown in the inset of Fig. 7-3(a). The current was collected laterally across the GaAs:Si layer from the active region. The forward biased current-voltage (I-V) characteristic and optical power vs. injection current (L-I)

characteristic of the LED were obtained by employing a Newport 8000 system with an integrating sphere. Room temperature (RT) electroluminescence (EL) was stimulated by injecting current continuously into the device. The EL signals were detected using a liquid nitrogen cooled germanium detector in conjunction with a standard lock-in technique.

The forward biased I-V characteristic of the device is shown in Fig. 7-3(a). The turn-on voltage of the LED is ~ 0.8 V and the diode ideality factor, n , is 2.4. This indicates that the current is limited by recombination in the active region. The L-I plot of the LED is shown in Fig. 7-3(b). The maximum optical output power from the device is 20 μ W, which translates to power per unit area of 7.6 mW.cm⁻². The external efficiency, η_{ext} , reduces from 0.1 % to 0.008 % following increase in injection current, as shown in Fig. 7-3(b). This could be partly attributed to the increased contribution from excited state emission [142], which is to be expected, considering the high aspect ratio of the dots. Carriers in the excited states are more likely to escape into the wetting-layer (WL) or the In_{0.1}Ga_{0.9}As barrier layer.

Figure 7-3 (a) Plot of forward biased I-V characteristic of the LED. Turn-on voltage is ~ 0.8 V and diode ideality factor n is 2.4. Inset: schematic diagram of the LED. (b) Plots of LED optical output power L , and external efficiency η_{ext} , as function of injection current.

To obtain greater insight into various carrier recombination processes in the InAs/In_{0.1}Ga_{0.9}As QD layers that give rise to the observed trend of η_{ext} , Boltzmann statistics and an absence of leakage currents were assumed, and thus the injected current can be described as

$$I_f = eV(An + Bn^2 + Cn^3) \quad (7-1)$$

where e is the electronic charge, V is the active volume, n is the carrier density, An is the nonradiative monomolecular recombination rate, Bn^2 is the bimolecular radiative recombination rate, and Cn^3 is the Auger recombination rate. As the optical output power is naturally related to Bn^2 , and assuming only one recombination process dominates within certain level of injection current, a general relationship between injected current and LED optical output power [143, 144] can be written

$$\ln(I_f) = Z \ln(L^{1/2}) + C \quad (7-2)$$

where I_f is the injection current, L the optical output power, Z the gradient of the $\ln(I_f)$ vs. $\ln(L^{1/2})$ plot and C a constant. Assuming that only one recombination process dominates under certain conditions, one can identify the principal process by examining the value of Z . When $Z = 1$, the recombination process is dominated by non-radiative monomolecular recombination, where carriers are trapped and recombine in deep level states due to defects or impurities. When $Z = 2$, the bimolecular radiative recombination process dominates and produces spontaneous photon emission. When $Z = 3$, the non-radiative Auger recombination process dominates. For non-integer values of Z , two or more carrier recombination processes might occur simultaneously.

From the η_{ext} values, three distinct regions in the plot of $\ln(I_f)$ vs. $\ln(L^{1/2})$ could be identified as shown in Fig. 7-4. The Z value in the low current injection region

(just after turn-on until ~30 mA) was found to be 2.1, which indicates the strong dominance of the bimolecular radiative recombination process. This corresponds to the high η_{ext} within this region. The second region lies between ~40-70 mA with $Z = 1.3$, which might indicate the dominance of monomolecular recombination. However, the monomolecular recombination process should decrease following an increase in injection current as these levels are saturated with carriers [145]. The fact that the possible dominance of this recombination mechanism was observed indicates that there are abundant non-radiative recombination centres that are not saturated at mid-level injection current. It is suspected that the cross-hatched patterns on the GaAs surface grown on graded Si_{1-x}Ge_x/Si act as non-radiative recombination centres. The cross-hatched lines were formed during growth of the graded Si_{1-x}Ge_x buffer layer [146, 147] and appear as dark lines in cathodoluminescence measurements, which are characteristics of non-radiative centres. The third region lies above 80 mA injection current with $Z = 2.8$. The Auger recombination process dominates [148] as the carrier density is high and the energy levels in the QDs are filled. The filling of QD energy levels gives rise to excited states emission. This can be observed from the EL emission at injection current within this region as shown by the arrow in the RT EL plot in the inset of Fig. 7-4. Furthermore, as the injection current increases, the junction temperature will follow suit. This leads to acceleration of the non-radiative recombination processes which further reduces the η_{ext} of the device.

Figure 7-4 Plot of $\ln(I_f)$ vs. $\ln(L^{1/2})$. The various carrier recombination processes are identified from the values of the gradient Z . The lines are guides to the eye. Inset: Plot of room-temperature EL spectrum of the LED at 105 mA injection current. The arrow points to emission from the excited states.

7.3 Summary

In summary, we have investigated the characteristics of InAs QD LED grown on graded Si_{1-x}Ge_x/Si substrate. Cross-sectional TEM analysis revealed that the InAs QDs take on a lens shaped structure with average base width and height of 29±3 nm and 6.7±0.8 nm, respectively. This translates to QD structures with aspect ratio of 0.23±0.05.

The LED exhibits a turn-on voltage ~ 0.8 V, with diode ideality factor n of 2.4 and emits at peak wavelength of $1.29 \mu\text{m}$ at room temperature. The maximum optical output power from the device is $20 \mu\text{W}$, which translates to power per unit area 7.6 mW.cm^{-2} . The external efficiency, η_{ext} , reduces from 0.1 % to 0.008 % following increase in injection current. Various carrier recombination processes which reduce the external efficiency, η_{ext} , were identified from analysis of the current-optical power relationship.

Chapter 8 Conclusions and Recommendations

8.1 Conclusions

This thesis presents a systematic study on the monolithic heteroepitaxial integration of III-V compound semiconductor QD-based light emitters on Si substrates through the use of a graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer. The investigations presented in chapters 3 and 4 aimed to establish the growth conditions to achieve good-quality GaAs on the Ge surface. In chapter 3, the effects of the MEE growth technique to the quality of the GaAs on Ge were investigated. SEM and AFM measurements show significant island-like formation occurred due to three-dimensional growth on the surface of the sample grown without the MEE-nucleated GaAs layer. On the other hand, the GaAs surface in the sample grown with the MEE nucleation process was free from islanding, as observed from SEM. Furthermore, samples made using the MEE nucleation process shows four times lower AFM root-mean square (RMS) surface roughness compared to the sample without the MEE due to two-dimensional growth. Consistent with the surface improvements, a 40 % reduction in the FWHM of the XRD spectrum was seen in the MEE-nucleated GaAs sample, indicating significant improvement in the crystalline quality. As a result of the two-dimensional growth, the higher strained layers in the sample grown with the MEE-nucleated GaAs layer experienced early relaxation. Due to the larger strain along the [100] and [010] directions, the photoluminescence (PL) peak energy of the InGaAs single quantum well (SQW) in this sample exhibits a blue shift compared to the sample grown without the MEE-nucleated GaAs layer.

The growth of GaAs on Ge was further optimized by ensuring a complete suppression of APB. In chapter 4, APB occurrence in the GaAs/Ge heterointerface was

shown to be effectively suppressed by employing a vicinal Ge surface and low temperature (250°C) initial GaAs nucleation by MEE. The Ge surface employed was a nominal (100) surface offcut 6° towards the nearest (111) plane. The observed APB self-annihilation mechanism was contributed to both the width of surface steps and the initial nucleation energy. APB with opposite orientation coalesced and annihilated each other. The low surface temperature during MEE is to ensure complete As dimer coverage on the double-atomic step Ge surface and to ensure that the growth mode lies within the two-dimensional growth mode by limiting Ga adatom migration onto the step-edges and kinks. Surface roughness as measured by AFM was reduced by one order in the sample grown with MEE at a substrate temperature of 250°C as compared to the sample grown with MEE at 450°C. On the other hand, the InGaAs SQW PL integrated intensity improved by two orders of magnitude. Meanwhile, comparison with a sample with the same structures grown on a GaAs substrate demonstrated that the quality of the GaAs layer grown on a Ge substrate is comparable to homoepitaxial GaAs, and further improvements of the heteroepitaxial GaAs can be expected. A shift in the InGaAs SQW PL emission wavelength was also observed, and it is attributed mainly to the indium out-diffusion mechanism and dislocations-induced strain.

The optimized GaAs/Ge heteroepitaxial growth condition was employed to realize good quality GaAs on graded SiGe/Si substrates in chapter 5. As a result of the optimization, an AlGaAs/GaAs HBT with maximum current gain (β) of ~40 was achieved, which is large enough for microwave applications. The RF performance of the HBT was investigated and the cut-off frequency (f_t) and maximum oscillation frequency ($f_{\max}$) were 20 GHz and 13 GHz, respectively for a $2 \times 15 \mu\text{m}^2$ emitter area device. The $f_{\max}$ value was compromised by the thin base layer (45 nm, 10^{19} cm^{-3} Be-doped) used in the HBT. This could be improved if the base doping level is increased by

using carbon as p-type dopant. Compared to a similar device grown on a GaAs substrate, the f_t value is lower due to higher emitter contact resistance, which can be further improved by increasing the indium composition in the emitter cap layer and optimizing the contact annealing condition

In chapter 6, a dense ($7 \times 10^{10} \text{ cm}^{-2}$) InAs QD ensemble grown on a graded SiGe/Si substrate using alternate beam MBE was demonstrated. The structure, which comprises a 5-layer InAs QD stack shows room-temperature (RT) PL emission at $1.3 \mu\text{m}$. Through AFM measurements, the InAs QDs were found to be at least two times larger compared to typical InAs QDs grown on GaAs substrate. Moreover, the InAs QDs grown on this Si-based platform were found to have a smaller aspect ratio compared to similarly grown InAs QDs on a GaAs substrate. At an InAs deposition thickness, θ_c , of 2.9 monolayer (ML), $1.3 \mu\text{m}$ room temperature PL emission was achieved with a FWHM of 65 nm. At this θ_c , optically-inactive large InAs dots/islands ($>80 \text{ nm}$) occur alongside optically-active smaller InAs QDs. Hence, although the size variation of optically-active QDs is smaller, as deduced from the narrowing of the PL FWHM, the integrated PL intensity drops significantly due to the optically-inactive large islands observed in this sample. To gain greater insight into the defect suppression mechanisms during capping of QDs, the effects of the $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ capping layer in self-assembled InAs QDs grown on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate were investigated. It was found that the $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ capping layer reduces material migration from the QDs into the capping layer and reduces strain around the QDs, which lead to realization of large-sized and defect-free QDs. InAs QDs capped with GaAs have smaller aspect ratio compared to the ones capped with $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ layer. The InAs QDs capped with GaAs take on a truncated pyramid shape because of collapse in the QD height as deposited material migrated from the top of the QDs towards the surrounding capping layer. On the other hand, the

$\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ capping layer leads to the formation of QDs with a more isotropic shape (lens or pyramid). A particular type of defect, the V-shaped defect was found dominant in the GaAs capping layer. V-shaped defects are seen to be located symmetrically at both top edges of the truncated pyramid QDs. This type of defect typically consists of two pairs of dislocations propagating in different $\{111\}$ planes from the QDs through the capping layer towards the surface. Subsequently, the InAs QDs capped with $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ layer show a much slower thermal quenching rate as compared to the ones capped with GaAs layer due to the absence of V-shaped defects.

The characteristics of InAs QD-based LED grown on the graded SiGe/Si substrate were presented in chapter 7. A 5-layer stacked self-assembled InAs/ $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ quantum dot (QD) structure serves as the active region. The QD structures were found to take on a lens shape with aspect ratio of 0.23 ± 0.05 . The LED exhibits a turn-on voltage of ~ 0.8 V with ideality factor, η , of 2.4. Room-temperature electroluminescence shows emission at $1.29 \mu\text{m}$. The maximum optical output power obtained from the device is $20 \mu\text{W}$, which translates to power per-area of 7.6 mW.cm^{-2} . The external efficiency, η_{ext} , reduces significantly from 0.1 % to 0.008 % with increasing current injection. This is partly attributed to the increasing contribution from excited state emission, which should be quite prominent considering the high aspect ratio of the dots. Carriers in the excited states are more likely to escape into the wetting-layer (WL) or the $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ barrier layer. The dominant carrier recombination processes in the QD layers were identified for the various injection current regions.

8.2 Recommendations for future research

It is a logical step to continue with further optimization in the QD quality and device design to realize a QD-based laser on this platform. There are, however, several

difficulties to realize a laser on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. A laser needs an optimized cladding layer design to ensure good optical and carrier confinement within the active region. When integrating such a device on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate, the bottom cladding layer would be directly on top of the GaAs buffer layer. Therefore, it is crucial to prevent light-leakage out of the cladding layers into this less-perfect GaAs buffer layer grown on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$. For an InAs QD laser structure, typically the cladding layers are in excess of $1\ \mu\text{m}$ [149-151]. This is needed especially for low Al content cladding layers. However, as discussed earlier, there is a critical thickness for III-V compound semiconductor layers grown on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates, which is $\sim 3\ \mu\text{m}$. III-V compound semiconductor layers exceeding that thickness are likely to exhibit crack formation, as reported by Lew *et al.* in HBT structure grown by similar growth conditions as presented in this thesis [111]. Therefore, carefully designed cladding layers that could accommodate both the critical thickness requirements and the optical confinement requirements are desired.

Furthermore, as discussed in section 7.2, the cross-hatch patterns behave as non-radiative recombination centers which would reduce the optical efficiencies of the laser active region. The cross-hatch patterns also create atomically rough surfaces which could contribute significantly to waveguide interfacial scattering losses in a laser device [59]. Finally, there is loss of photons escaping through the laser mirrors. In an edge-emitting laser device grown on GaAs substrate, cleaved $\{110\}$ planes are typically used as mirrors with near-perfect reflectivity. However, similar laser mirrors on graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate would have difficulties in achieving the near-perfect reflectivity. This is due to the preference along the $\{111\}$ cleavage planes for Si [108]. Hence, attempts to cleave on different planes could produce a rough cleavage surface that is not suitable for laser mirrors.

To realize a laser on this integrated platform, AlGaAs cladding layers with larger Al contents could be considered as possible way of reducing the required cladding layer thickness. Furthermore, the issues of mirrors cleavage for edge-emitting lasers grown on Si-based substrate could be solved possibly through employment of a two-step dry and wet chemical etching to create smooth and defect-free planes suitable for laser mirrors. Extension of the InAs QD emission wavelength to 1.55 μm is another area of interest. These could be achieved by incorporating a larger indium content capping layer to further reduce the strain in the InAs QD or by using nitrogen-containing Sb-assisted InAs QDs. However, nitrogen-related defects may affect the quality of such QDs and could prevent high-optical efficiencies.

Another interesting issue to investigate is the exact GaAs growth mechanisms on the double-atomic step Ge surface during low-temperature MEE. A real-time *in situ* investigation employing scanning tunneling microscope (STM) during the GaAs MEE nucleation onto the double-atomic step Ge surface would provide rich information. Revelations on the nature of GaAs nucleation on this surface such as whether it can indeed proceed *via* step-propagation growth would be very interesting. Furthermore, such study could potentially provide more precise explanations on the APB suppression mechanisms.

Author's Publications

Publications in refereed journals

- 1) H. Tanoto, S. F. Yoon, K. L. Lew, W. K. Loke, C. Dohrman, E. A. Fitzgerald, and L. J. Tang, **“Electroluminescence and structural characteristics of InAs/In_{0.1}Ga_{0.9}As quantum dots grown on graded Si_{1-x}Ge_x/Si substrate”**, submitted to the Applied Physics Letters (under review).
- 2) H. Tanoto, S. F. Yoon, T. K. Ng, C. Y. Ngo, C. Dohrman, E. A. Fitzgerald, L. H. Tan, and C. H. Tung, **“Origin and suppression of V-shaped defects in the capping of self-assembled InAs quantum dots on graded Si_{1-x}Ge_x/Si substrate”**, submitted to the Applied Physics Letters (under review).
- 3) K. P. Chen, S. F. Yoon, T. K. Ng, H. Tanoto, K. L. Lew, C. L. Dohrman, and E. A. Fitzgerald, **“Study of surface microstructure origin and evolution for GaAs grown on Ge/Si_{1-x}Ge_x/Si substrate”**, Journal of Physics D – Applied Physics **42**, 035303 (2009).
- 4) K. P. Chen, S. F. Yoon, T. K. Ng, H. Tanoto, K. L. Lew, C. L. Dohrman, and E. A. Fitzgerald, **“Characterization of GaAs grown on SiGe/Si graded substrates using P-N junction diodes”**, Journal of Applied Physics **104**, 073710 (2008).
- 5) H. Tanoto, S. F. Yoon, C. Y. Ngo, W. K. Loke, C. Dohrman, E. A. Fitzgerald, and B. Narayanan, **“Structural and optical properties of stacked self-assembled InAs/InGaAs quantum dots on graded Si_{1-x}Ge_x/Si substrate”**, Applied Physics Letters **92**, 213115 (2008). Selected for the June 9, 2008 issue of Virtual Journal of Nanoscale Science & Technology

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- 6) H. Tanoto, S. F. Yoon, W. K. Loke, K. P. Chen, E. A. Fitzgerald, C. Dohrman, and B. Narayanan, **"Heteroepitaxial growth of GaAs on (100) Ge/Si using migration enhanced epitaxy"**, Journal of Applied Physics **103**, 104901 (2008).
 - 7) K. L. Lew, S. F. Yoon, H. Tanoto, K. P. Chen, C. L. Dohrman, D. M. Isaacson, and E. A. Fitzgerald, **"InGaP/GaAs heterojunction bipolar transistor grown on Si substrate with SiGe graded buffer layer"**, Electronics Letters **44**, 243 (2008).
 - 8) K. L. Lew, S. F. Yoon, W. K. Loke, H. Tanoto, C. L. Dohrman, D. M. Isaacson, and E. A. Fitzgerald, **"High gain AlGaAs/GaAs heterojunction bipolar transistor fabricated on SiGe/Si substrate"**, Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures **25**, 902 (2007).
 - 9) H. Tanoto, S. F. Yoon, W. K. Loke, E. A. Fitzgerald, C. Dohrman, B. Narayanan, M. T. Doan, and C. H. Tung, **"Growth of GaAs on vicinal Ge surface using low temperature migration-enhanced epitaxy"**, Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures **24**, 152 (2006).

Conference/symposiums presentations

- 1) H. Tanoto, S. F. Yoon, W. K. Loke, E. A. Fitzgerald, C. Dohrman, and B. Narayanan, **"InAs quantum dots growth on vicinal SiGe/Si substrate"**, presented at the European Material Research Society Spring Meeting, Strasbourg, France, 28 May – 1 June 2007.
 - 2) H. Tanoto, S. F. Yoon, W. K. Loke, E. A. Fitzgerald, C. Dohrman, B. Narayanan, M. T. Doan, and C. H. Tung, **"Growth of GaAs on (100) Ge and vicinal Ge surface by migration enhanced epitaxy"**, Material Research Society Symposium Proceeding, Fall Meeting 2005, Vol. 891, EE03 p 17.1-17.6, December 2005.
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- 3) H. Tanoto, S. F. Yoon, and B. Narayanan, "**Improvement in surface and optical quality of GaAs/Ge heteroepitaxy by migration enhanced epitaxy**", Symposium of Microelectronics, Singapore, 5 August 2005.

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