Design of a power efficient output stage for dc-to-dc converters

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2010

Lao, J. (2010). Design of a power efficient output stage for dc-to-dc converters. Master's thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/47033>

<https://doi.org/10.32657/10356/47033>

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**DESIGN OF A POWER EFFICIENT OUTPUT STAGE
FOR
DC-TO-DC CONVERTERS**

LAO JIAHONG

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

**A DISSERTATION SUBMITTED IN FULFILMENT OF
THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF ENGINEERING IN CIRCUITS AND SYSTEMS**

2010

ACKNOWLEDGEMENTS

ACKNOWLEDGEMENTS

I would like to express my sincerest gratitude to my advisor, Assistant Professor Tan Meng Tong, for his invaluable guidance and continuous encouragement throughout my graduate study. Without his valuable suggestions and support, the journey of study would not have been so smooth and wonderful.

I would also like to thank Mr Ling Chia How and Mr Yu Guolei, the staff in Panasonic Singapore for their support and encouragements during the course of my graduate study. Without their generously sharing experiences with me, my study could be full of frustration.

Many thanks to the laboratory executives from the Centre for Integrated Circuits and Systems: Mr Sia Liang Poo, Mr. William Seow Yong Hing, and Mr Jimmy Goh Mia Yong. All of them have offered great help in our work.

Last but not least, I would like to take this opportunity to thank my parents, siblings, and my girlfriend for their understanding and great support. Without their support, I will not be able to complete my master course successfully.

Lao Jiahong
July 2009

SUMMARY

SUMMARY

This thesis describes the analysis and design of a power-efficient output stage for DC-to-DC buck converters based on low swing voltage and DCM mode. The theoretical aspect of this thesis pertains to the mathematical analysis of the power dissipation mechanism of a DC-to-DC converter output stage. The practical aspect pertains to the design and implementation of a DC-to-DC buck converter to achieve better power efficiency performance over the entire load current range, in particular at light load and extreme light load conditions.

The market for battery-operated portable applications such as cellular phones, portable DVD players, CD players, and etc has grown dramatically in the last decade. Hence, it is imperative to have high power efficiency DC-DC converter for the entire load range to extend the life time of the battery, especially at light load condition. This is because most of the portable devices usually operate in standby mode with low standby current.

For theoretical research, the analysis includes a complete theoretical analysis of the power dissipation mechanism of the output stage. The analysis also includes the power dissipation of the output stage operating in different control modes.

For practical research, a novel technique to improve the light load power efficiency of the output stage of a synchronous buck converter is proposed. This is achieved by reducing the gate drive voltage of the output power transistors and by recycling the charge store in a charge recycling capacitor. In addition, a new control technique based on PWM DCM with pulse skipping is applied to the proposed output stage to further improve the power efficiency at extreme light load. The improvement in power efficiency is verified by schematic simulations, post-layout simulations and measurements on hardware prototype. The results from simulations and measurements show that the proposed output stage has a better power efficiency performance than the conventional design and a segment output stage design reported in literature.

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CHAPTER 1 INTRODUCTION

CHAPTER 1

INTRODUCTION

1.1 Background

The market of battery-operated portable applications such as cellular phone, portable DVD, CD player, and etc has grown dramatically in the last decade. In all of these applications which are remotely power by batteries, a DC-to-DC converter is required to convert the time varying input voltage from the battery into a regulated output voltage. In general, the energy capacity of the battery is very limited. Hence, the power efficiency of DC-to-DC converter is critical to extend the life time of the battery. Ideally, the power efficiency of a DC-to-DC converter is 100%, but this is unachievable practically due to the power losses in the output stage.

There are two main types of DC-to-DC converter, namely the linear regulator and the switching regulator. A linear regulator can only step down the input voltage to a lower level and is usually chosen for its simplicity and cost. However, it suffers from poor power efficiency. On the other hand, a switching regulator can step up or down the input voltage from the battery. The power efficiency of the switching regulator is usually much

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higher than that of the linear regulator. However, this is achieved at the expense of more complex feedback topology. The basic differences between linear and switching regulators are tabulated in Table 1.

Table 1 Comparison between Linear and Switching Regulators [1]

	Linear	Switching
Function	Only steps down; input voltage must be greater than output.	Steps up, steps down, or inverts
Efficiency	Low to medium, but actual battery life depends on load current and battery voltage over time; high if $V_{IN}-V_{OUT}$ difference is small.	High, except at very low load currents (μA), where switch-mode quiescent current is usually higher.
Waste Heat	High, if average load and/or input/output voltage difference are high	Low, as components usually run cool for power levels below 10W
Complexity	Low, which usually requires only the regulator and low-value bypass capacitors	Medium to high, which usually requires inductor, diode, and filter caps in addition to the IC; for high-power circuits, external FETs are needed
Size	Small to medium in portable designs, but may be larger if heat sinking is needed	Larger than linear at low power, but smaller at power levels for which linear requires a heat sink
Total Cost	Low	Medium to high, largely due to external components
Ripple/Noise	Low; no ripple, low noise, better noise rejection.	Medium to high, due to ripple at switching rate

A basic block diagram of a linear regulator is depicted in Figure 1.1. It consists of a reference voltage, an operational amplifier and a variable resistor. The output voltage of the linear regulator is forced to be equal to the reference voltage by the large open-loop gain of the amplifier in the feedback loop.

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Figure 1.1 Linear regulator

The biggest disadvantage of a linear regulator is that the load current passes through the variable resistor all the time while the circuit is “ON”. In other words, the power efficiency of a linear regulator is low, and it decreases as the input to output voltage ratio increases.

Due to the low power efficiency of linear regulators, switching regulators are dominant for high efficiency applications especially for portable devices. Switching regulators are commonly used for both step-up and step-down applications. In this project, only step-down converter or so called buck converter is considered. Buck or step-down voltage converters produce an average output voltage lower than the input source voltage. There are two types of switching buck converter, namely the synchronous and asynchronous converters, as depicted in Figure 1.2(a) and (b). The primary difference between a synchronous buck converter and an asynchronous buck converter is that a FET switch is used to replace the diode in the asynchronous converter. The high side FET switch of the synchronous buck converter operates in the same way as that of the asynchronous buck

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converter. When the high side FET switch of the synchronous converter is turned off, the low side FET switch turns on to provide a current path for the inductor when it is discharging. Although the synchronous buck converter requires more components and additional switch logic sequencing, this topology improves the efficiency with faster switch turn-on time and lower on resistance, R_{on} , when the output is low. Hence, the synchronous buck converter is selected in this project for its higher efficiency.

Figure 1.2 (a) Synchronous buck converter and (b) Asynchronous buck converter

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The block diagram of a voltage mode control synchronous buck converter is depicted in Figure 1.3. It consists of a feedback loop, a comparator, a ramp generator, two power switches and an output lowpass filter (inductor and capacitor). In a voltage buck converter, the error signal V_{ctl} is derived from the output voltage only. The error signal V_{ctl} is compared with a sawtooth signal and generates a control signal to drive the output stage. Hence, synchronous buck converter does not operate in the linear region. It switches between two different voltage levels: supply voltage V_{IN} and ground voltage by turning ON and OFF the two power switches $SW1$ and $SW2$ alternately to achieve regulation. Synchronous buck converter has much higher efficiency than linear regulator because power can be stored in the inductor and the “ON” resistance of the switches is always very low.

Figure 1.3 Voltage mode control synchronous buck converter

One of the major power losses of a synchronous buck converter output stage is the switching loss. It is because all MOSFET has input and output capacitance and switching loss is induced when they are being charged and discharged. In addition, the capacitance

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of the synchronous buck converter output stage is mainly contributed by the two power switches, $SW1$ and $SW2$ in Figure 1.3. When the gate drive voltage of power switch, $SW1$, is high, the input capacitance of $SW1$ will be charged to the supply voltage, V_{IN} . On the other hand, when its gate drive voltage goes low, the input capacitance of $SW1$ will be discharged to ground. The same charging and discharging process occurs at the input capacitance of the power switch, $SW2$. Therefore, the charge is transferred from supply voltage, V_{IN} , to ground as both power switches are turning “ON” and “OFF” alternately. In other words, the major switching loss of the output stage is mainly caused by the losses in these two power switches.

As the power switches act as the dominant resistors and capacitance in the synchronous buck converter output stage, the major power loss of the output stage is induced by them. To improve the power efficiency of a synchronous buck converter output stage, the losses of the power switches must be reduced.

1.2 Motivation

According to the BCC research reports on energy & resources [2, 3], the global market for premium portable power will rise at an average annual growth rate of 7.2%, from \$4.4 billions in year 2004 to \$6.3 billion in the year of 2009 [2] as depicted in Figure 1.4. Figure 1.5 shows the U.S. wholesale market for battery control technology. The wholesale market was in excess of \$2.2 billions in year 2003 and should rise at the average annual growth rate of 11.3% to more than \$4.2 billions by year 2009 [3]. In addition, battery chargers and power converters currently represent the largest of the

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three battery control technology market sectors, with about \$1.4 billions total sales in year 2003. The high market growth for portable power indicates that the demands for portable devices are rising year by year. Moreover, more and more functions will be implemented in portable devices. Hence, it is imperative to have a high performance power supply.

Figure 1.4 Global market for premium portable power [2].

Figure 1.5 U.S. wholesale market for battery control technology [3].

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In all portable applications, DC-to-DC converters are required to regulate the battery voltage and provide DC supply voltage for the electronic circuits. Hence, the demand for the DC-to-DC converters, especially high power efficiency DC-to-DC converters are rising annually. This is because the primary design considerations for portable devices are the life time of the battery and low power and low voltage operations. Figure 1.6 depicts the cellular phone talk and standby times for three popular phone brands. As shown in Figure 1.6, the talk time is about 5 to 6 hours. However, the standby time can be extended up to more than 12 days and is continuing to increase annually. In typical applications, the cellular phones operate in standby mode most of the time. Hence the battery can last for about 3 days without charging. As the power efficiency of the DC-to-DC converter at light load condition is lower than that at heavy load, power efficiency improvement for DC-to-DC converters at light load condition has become more and more important to extend the life time of the battery.

Figure 1.6 Cellular phone talk and standby times [4].

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In a DC-to-DC converter, the power loss is usually dominated by the output stage. For instance, the finite on resistance and internal parasitic capacitance of the large MOS power transistors in a synchronous buck converter will induce power losses. Generally speaking, the two major power losses in the output stage are the switching loss and the conduction loss. Switching loss is primarily caused by the charging and discharging of the internal parasitic capacitance of the power transistors when they switch on and off. On the other hand, conduction loss is usually caused by current flowing through the resistive components. In typical applications, switching loss is the dominant power loss at light load condition (i.e. when the output current is low) whereas conduction loss is dominant at heavy load.

In order to improve the light load efficiency of buck converter, the switching loss at light load has to be reduced. The switching loss of CMOS power switches can be expressed as

$$P_{SW} = CV_{IN}^2 f_s \quad (1.1)$$

where C is the internal parasitic capacitance of output stage, V_{IN} is the input voltage and f_s is the switching frequency.

Based on equation (1.1), it is noted that the parameter that has the most significant influence on the switching loss is the switching voltage level of the parasitic capacitance. Based on this observation, we proposed a low voltage swing output stage design with capacitor charge recycling scheme to improve the light load efficiency. The proposed design improve the efficiency by reducing the switching voltage level of the internal parasitic capacitance and recycle the charge stored in the parasitic capacitor to turn on the

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NMOS power transistor. The proposed technique is simple and elegant and can be implemented easily in an integrated DC-to-DC converter.

1.3 Objective

The demand of high efficiency DC-to-DC converters is growing dramatically in this decade due to the increasing popularity of portable devices. Generally speaking, most of the portable devices operate in the standby mode with low output load current, e.g. cellular phone applications. Therefore, the primary objective of this project is to design a DC-to-DC converter with improved light load power efficiency.

To obtain the primary objective, the two specific objectives of the project are as follows.

(i) To design a buck converter output stage with a low swing gate drive voltage control and charge recycling scheme to improve the power efficiency at light load. The proposed technique reduces the switching loss significantly while the increase in conduction loss is insignificant. (ii) To design a DC-to-DC buck converter that operates in different control modes to maintain relatively high power efficiency throughout the entire load condition. The proposed design can be simply implemented and produces less switching activities.

1.4 Organization of the Report

The report is organized as follows. Chapter 2 presents a brief review of the operation modes of buck switching converter, namely the Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) and control methodologies, Pulse Width

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Modulation (PWM) and Pulse Frequency Modulation (PFM). Next, the reported power efficiency improvement techniques namely the PFM and PWM dual mode technique, the segmented output stage technique and the low voltage swing technique will be discussed. The power dissipations analysis of the switching buck converter output stage is detailed in Chapter 3. Chapter 4 discusses the proposed low voltage swing output stage design. In Chapter 5, the power efficiency of the proposed output stage based on theoretical calculations, computer simulations and hardware measurements are presented and discussed. Finally, the conclusions and the future work are presented in Chapter 6.

CHAPTER 2 LITERATURE REVIEW

CHAPTER 2

LITERATURE REVIEW

2.1 Overview of Buck Converter Operation**2.1.1 Basics of Buck Converter**

A buck converter is a step-down converter which converts a higher DC input voltage V_{IN} into a lower average output voltage, V_{OUT} . Figure 2.1(a) depicts the schematic of a synchronous buck converter. It consists of a PWM controller, an output lowpass filter and an output stage, in which the high side and the low side switches are implemented with MOS transistors. In a synchronous buck converter, the input voltage from the battery is stepped down by turning the high side and low side switches ON or OFF alternately to produce a Pulse Width Modulated (PWM) signal as depicted in Figure 2.1(b). The switching duty ratio D of the buck converter is defined as the ratio of the high side FET on time to the switching time period as shown in equation (2.1).

$$D = \frac{T_{on}}{T_s} \quad (2.1)$$

where T_{on} is the high side FET turn on time and T_s is the switching time period.

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The duty ratio of the PWM signal is also proportional to the ratio of the output voltage versus the input voltage (i.e. V_{OUT}/V_{IN}). To obtain the average output voltage, a second-order LC lowpass filter is used to attenuate the AC components of the high frequency carrier of the pulse modulated signal so that the voltage ripple at the output is reduced to an acceptable level. Neglecting the power losses in the converter, the output DC voltage V_{OUT} is given by [6]

$$V_{OUT} = V_{IN} \times D \quad (2.2)$$

Based on the above equation, the output voltage V_{OUT} can be controlled by varying the duty ratio D of the PWM control signal. In order to have small voltage ripple at output, the corner frequency f_c of the second-order LC filter is chosen to be much lower than the switching frequency f_s of the output stage.

Figure 2.1 (a) Buck converter schematic and (b) Switching node voltage, V_x , waveform at steady-state (*to be continued*)

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Figure 2.1 (a) Buck converter schematic and (b) Switching node voltage, V_x , waveform at steady-state (*continued*)

2.1.2 Continuous Conduction Mode

Figure 2.2 depicts the schematic, the switching node voltage waveform and the inductor current waveform of a synchronous buck converter operating in continuous conduction mode (CCM). A DC-to-DC converter is said to be operating in continuous conduction mode if the inductor current remains positive or is allowed to reverse by the high-side or the low-side switch. The “ON” time of the high side control switch is defined as $T_{on} = DT_s$, and the inductor current ripple is given by

$$\Delta I_L = \frac{V_{OUT}(1-D)}{L_O} T_s \quad (2.3)$$

where T_s is the switching time period and L_O is the inductance of the output lowpass filter.

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Figure 2.2 (a) Buck converter schematic, (b) Switching node voltage waveform at steady-state, (c) Inductor current waveform in CCM mode ($I_{OUT} > \Delta I_L/2$) and (d) Inductor current waveform in CCM mode ($I_{OUT} < \Delta I_L/2$) (to be continued).

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Figure 2.2 (a) Buck converter schematic, (b) Switching node voltage waveform at steady-state, (c) Inductor current waveform in CCM mode ($I_{OUT} > \Delta I_L/2$) and (d) Inductor current waveform in CCM mode ($I_{OUT} < \Delta I_L/2$) (*continued*).

In steady-state, the average output voltage is given by equation (2.2), and the output current I_{OUT} is equal to the DC component of the inductor current I_L . If the output current, I_{OUT} , is greater than half of the inductor ripple current, $\Delta I_L/2$, the inductor current remains positive in the entire switching cycle as shown in Figure 2.2(c). Otherwise, the inductor current becomes negative momentarily in the switching cycle as depicted in Figure 2.2(d). Negative inductor current implies that the output capacitor is being discharged through the inductor and the low side switch to ground, thereby resulting in an extra power loss. Hence, in order to maintain high power efficiency for the buck converter output stage, negative inductor current must be prevented.

In CCM operation, the current flowing through the switches and the inductor is the output load current and the inductor ripple current [7]. So the RMS value of the current in CCM operation is given by

$$I_{rms,CCM}^2 = I_{OUT}^2 + \frac{1}{12} \Delta I_L^2 \quad (2.4)$$

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2.1.3 Discontinuous Conduction Mode

A buck converter is said to be operating in discontinuous conduction mode (DCM) if the output current of the buck converter, I_{OUT} , is less than half of the inductor current ripple, $\Delta I_L/2$, at light load condition and the inductor current goes to zero momentarily in every switching cycle. As mentioned earlier, negative inductor current implies that the output capacitor is being discharged through the inductor and the low side power switch to ground and results in additional power loss. Negative inductor current can be prevented in DCM operation by turning off the low side switch when the inductor current reaches zero and goes negative. Figure 2.3 presents the equivalent circuit schematic of a synchronous buck converter operating in discontinuous conduction mode (DCM), the corresponding switching node voltage waveform and the inductor current waveform. Note that the output inductor discharges its stored energy to the output capacitor when the low side power switch is turned on. When inductor current reaches zero, the low side power switch is forced to switch off and the reversed inductor current flowing from the output capacitor to ground is blocked by the body diode of the low side power switch. Because both high side and low side power switches are off, the inductor current remains zero until the high side power switch turns on in the next switching cycle. This operation mode is called discontinuous conduction mode as the inductor current is ideally zero for finite intervals of the switching cycle.

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Figure 2.3 (a) Schematic of a buck converter in DCM, (b) Switching node voltage and (c) inductor current waveforms in DCM.

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In DCM operation, the average output voltage of the converter does not satisfy equation (2.2). Instead, the new expression for the duty ratio is given by [6]

$$D = \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{I_{OUT} / I_{LB,max}}{1 - V_{OUT} / V_{IN}}} \quad (2.5)$$

where $I_{LB,max}$ is the maximum value of average inductor current at the edge of the continuous conduction mode I_{LB} if V_{OUT} is constant:

$$I_{LB,max} = \frac{T_s V_{OUT}}{2L_O} \quad (2.6)$$

So the RMS value of the current in DCM is given by [8].

$$I_{rms,DCM}^2 = \frac{1}{3} (2I_{OUT})^{3/2} \Delta I_{L,CCM}^{1/2} \quad (2.7)$$

From equation (2.7), it can be observed that the RMS current of the DC-to-DC buck converter operating in DCM at light load is lower than that of the converter in CCM mode. In other words, the conduction loss of the converter can be reduced in DCM operation at light load.

2.2 Buck Converter Modulation Techniques

Synchronous buck converter is controlled by a modulator which produces a control signal to turn ON/OFF the two output power switches alternately and generates a regulated output voltage. The two most popular modulation techniques for buck converters are Pulse Width Modulation (PWM) technique and Pulse Frequency Modulation (PFM) technique. In general, the PWM technique is the best choice for buck converters operating at heavy load. On the other hand, PFM technique is widely applied for light

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load operation because the circuit complexity of the PFM technique is simpler and the switching frequency is lower.

2.2.1 PWM Modulation

Pulse width modulation controller can be implemented using both analog and digital control schemes [11-13]. It produces a logic signal $P(t)$, which is periodic with frequency f_s and a duty ratio D . The periodic signal $P(t)$ controls the duration over which the power transistor in the converter output stage is switched on. The input of the analog pulse width modulator is an error voltage generated by a compensation circuit in the PWM. The inputs of the compensation circuits are the output voltage and the reference voltage. On the other hand, the input of a digital pulse width modulator is an N-bit digital command word obtained from a DSP/microprocessor unit. The N-bit digital command word is subsequently manipulated by the modulator to produce a PWM signal with duty cycle proportional to the command word. In this project, analog PWM control technique is applied for its simple implementation. A compensation network is required for analog PWM control to adjust to load perturbations or changes in the input voltage which may adversely affect the output voltage and the system stability [14-15].

Figure 2.4 illustrates a ramp based analog PWM circuit and its PWM control signal waveforms. The switching control signal $P(t)$ of the converter is generated by comparing a saw-toothed waveform $V_{saw}(t)$ with the analog control voltage $V_c(t)$. The logic level of the $P(t)$ signal goes high whenever $V_c(t)$ is greater than $V_{saw}(t)$. Otherwise, the logic level is low. Hence, the switching frequency f_s of the PWM control signal is the same as the frequency of the saw-toothed signal. While the pulse width of the PWM signal $P(t)$ is

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dependent on the voltage level of the analog input $V_C(t)$, which is the error voltage between the output voltage and the reference. In other words, when the output voltage is lower than the reference voltage, the voltage level of the analog input $V_C(t)$ increases and generate a PWM signal with a longer pulse width. By means of negative feedback, this cycle will repeat until the output voltage is approximately equal to the reference voltage. Ignoring the power loss at the output stage, the duty cycle of the PWM signal is proportional to the ratio of the output voltage versus the input voltage in steady state.

Figure 2.4 (a) Ramp based pulse width modulator circuit and (b) Typical waveforms obtained by ramp based pulse width modulator.

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2.2.2 PFM Modulation

Pulse Frequency Modulation (PFM) is a nonlinear operation [8, 16]. In PFM operation, a series of inductor current pulses are applied to the load and the output capacitor maintains the output voltage within the preset boundaries. PFM control reduces the switching frequency effectively, thereby lowering the switching loss for the buck converter output stage. This operation is preferred at light load condition for its low switching activities. There are several types of PFM operation technique such as the single-pulse PFM, the multi-pulse PFM and the burst-mode PFM [8, 16]. Burst-mode PFM is discussed in this report for its easy analysis and calculation.

Figure 2.5 depicts the typical inductor current and output voltage waveforms of buck converter operating in burst-mode PFM mode. In the burst-mode PFM control scheme, there are four boundary conditions: peak inductor current, zero-crossing detection of the inductor current, upper and lower threshold of the output voltage

Figure 2.5 Output voltage and inductor current waveforms in burst-mode PFM control [8]

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Under the burst-mode PFM operation, when the buck converter output voltage is lower than the output voltage lower threshold, the high side FET (PMOS) will turn on and the inductor current will ramp up during time interval $dt1$ until it reaches the current limit, which is set specifically for the PFM mode. The time interval $dt1$ is given by

$$dt1 = \frac{I_{peak,PFM} \times L_O}{V_{IN} - V_{OUT}} \quad (2.8)$$

where $I_{peak,PFM}$ is the peak inductor current in PFM mode.

After the high-side FET turns off, the low-side FET (NMOS) will turn on and the inductor current will reduce during time interval $dt2$ until it reaches zero. This action is described by the following equation:

$$dt2 = \frac{I_{peak,PFM} \times L_O}{V_{OUT}} \quad (2.9)$$

So the pulse frequency f_1 can be defined as:

$$f_1 = \frac{1}{dt1 + dt2} = \frac{1}{T_1} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak,PFM} \times L_O \times V_{IN}} \quad (2.10)$$

At the instance when the inductor current reaches zero, if the output voltage is still lower than the output voltage upper threshold, another pulse with frequency f_1 will be generated. Otherwise, no pulse will be generated until the output voltage is lower than the lower threshold.

Because the charge provided by the inductor current pulses and the charge supplied by the output capacitor C_{OUT} to the load should be equal within a single burst period to maintain a stable dc output voltage. The burst frequency f_2 is determined by:

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$$f_2 = \frac{1}{T} = \frac{1}{NT_1 + T_2} = \frac{2 \times I_{OUT} \times \left(\frac{I_{peak,PFM}}{2} - I_{OUT} \right)}{V_R \times C_{OUT} \times I_{peak,PFM}} \quad (2.11)$$

where C_{OUT} is the capacitance of the output capacitor, T_2 is the dead time, V_R is the ideal ripple voltage of the output as defined by the upper and lower control threshold and N is the number of pulses generated in a period T .

2.3 Transistors Model in Buck Converter Output Stage

In a synchronous buck converter output stage, both power switches operate in the triode region and the finite on resistance of the power transistor will induce conduction loss. Ignoring channel length modulation and assuming that the source-to-gate voltage, V_{SG} , is much larger than the source-to-drain voltage (i.e. $V_{SG} \gg V_{SD}$) for a PMOS transistor, the drain current of PMOS can be expressed as:

$$I_D = \mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{SG} - |V_{tp}|) V_{SD} \quad (2.12)$$

where μ_p is hole mobility, C_{ox} is oxide capacitance per unit gate area, W_p is the channel width of PMOS, L is the channel length, V_{SG} is the source-to-gate voltage, V_{tp} is the threshold voltage and V_{SD} is the source-to-drain voltage.

Hence, the turn on resistance, R_p , of the PMOS can be expressed as

$$R_p = \frac{V_{SD}}{I_D} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{SG} - |V_{tp}|)} \quad (2.13)$$

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Equation (2.13) shows that R_p is inversely proportional to both the channel width W_p and the voltage difference between the source-to-gate voltage and the threshold voltage (i.e. $V_{SG} - V_{tp}$) as μ_p , C_{ox} , L and V_{tp} are constants. On the other hand, the turn on resistance, R_N , of the NMOS is inversely proportional to both the channel width, W_N , and the voltage difference between the gate-to-source voltage and the threshold voltage (i.e. $V_{GS} - V_{tn}$).

Figure 2.6 depicts the turn on resistance of the PMOS and NMOS transistors operating in different gate-to-source voltage levels. From the figure, note that the variations of the turn on resistance of the PMOS and NMOS transistors are small when the gate-to-source voltage, V_{GS} , is three times higher than the threshold voltage, V_t . In other words, the increase in turn on resistance of the power switches is relatively small if they are operating with a lower gate drive voltage swing, which is at least three times higher than the threshold voltage, V_t .

Figure 2.6 MOS turn on resistance versus gate-to-source voltage, V_{GS} .

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Next, the switching loss of the buck converter shall be analysed. Most of losses in switching are caused by the internal parasitic capacitance of the large output stage MOS transistors. The dominant parasitic capacitance is the input capacitance of the PMOS and NMOS transistors [7], which can be expressed as

Input capacitance of the PMOS:

$$C_{G-P} = C_{ox}W_P L + (C_{GSO} + 2C_{GDO})W_P \quad (2.14)$$

Input capacitance of the NMOS:

$$C_{G-N} = C_{ox}W_N L + (C_{GSO} + 2C_{GDO})W_N \quad (2.15)$$

where C_{GSO} and C_{GDO} are the gate-to-source and the gate-to-drain capacitance per unit gate width.

From equations (1.1), (2.14) and (2.15), it is noted that the switching loss of the buck converter output stage is proportional to the size of the PMOS and NMOS transistors.

2.4 Reported Techniques for Power Efficiency Improvement

The power efficiency of a buck converter is ideally 100%. However, this efficiency cannot be achieved practically due to the various power losses of the non-ideal components in the output stage. As mentioned earlier, the two major power losses of buck converter output stage are conduction loss and switching loss. At light load condition, the conduction loss is small because the output load current is small. On the other hand, the switching loss is independent of the output load current and is

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proportional to the switching frequency. Hence, the switching loss must be reduced to improve the power efficiency of the buck converter output stage at light load condition.

Based on equation (1.1), the switching loss, P_{SW} , is proportional to three parameters, namely the internal parasitic capacitance, C , the square of switching voltage range V_{IN}^2 and the switching frequency f_s . Hence, the switching loss can be reduced by reducing either one or combinations of these three parameters. Three techniques have been reported to improve power efficiency by reducing the switching loss at light load: (i) PFM and PWM dual mode control technique [17], (ii) segmented output stage technique [5] and (iii) low voltage swing technique [18]. In these three techniques, different methodologies are applied to lower the switching loss by reducing the switching loss parameters C , V_{IN}^2 and f_s . The details of these three techniques will be described in the following sub-sections.

2.4.1 PFM and PWM Dual Mode Technique

As discussed in the previous chapter, PWM control provides good regulation quality and high power efficiency at heavy load. However, the power efficiency of DC-to-DC converter with PWM control drops rapidly at light load because the power loss is dominated by the switching loss of the power transistors. According to equation (1.1), the switching loss is proportional to the switching frequency of the buck converter output stage. Hence, the switching loss can be reduced by reducing the switching frequency through PFM control at light load as given in equation (2.11). This will result in a significant reduction in switching loss. However, as the output load current increases, the

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switching frequency of the PFM controller will also increase. This will increase the power dissipation and cause the PFM controller to have a low efficiency than the PWM controller at heavy load. Hence, the dual-mode control technique has been used widely for power efficiency improvement of buck converters [17, 19-22, 28] (i.e. PFM control for light load and PWM control for heavy load).

Figure 2.7 depicts the details of a dual-mode buck converter IC with power train and gate drivers [17]. The design supports PWM mode at heavy load and PFM mode at light load. The switching between these two modes is controlled by a signal pin MODE according to the output load current. The PFM control mode will be selected when the output load current is low and the PWM control mode will be selected when the output load current is high.

Figure 2.8 illustrates the power efficiency of the buck converter operating in both PFM and PWM mode. At light load condition, the power efficiency of the output stage operating in PFM mode is higher than that of the output stage controlled by PWM. In contrast, the output stage with PWM control has higher power efficiency if the output current is greater than about 40mA. The cross-section point of the two efficiency curves indicates the output current value at which the transaction of the two control mode occurs. The PFM/PWM dual mode design improves the light load power efficiency of a buck converter by reducing the switching loss. However, PFM control reduces only one parameter of the switching loss (i.e. switching frequency f_s .) and operates with a variable switching frequency, which is proportional to the output load current. This will induce unpredictable and wide frequency range noise, which may affect the applications of the

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portable devices, i.e. RF application. The switching control between PFM and PWM modulation also increases the switching complexity and the IC area cost of the design.

Figure 2.7 Block diagram of a digitally controlled buck converter IC for cellular phone applications [18]

Figure 2.8 Measured PWM and PFM buck converter efficiency vs output current [17]

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2.4.2 Segmented Output Stage Technique

In the PFM and PWM dual mode technique, the switching frequency of the buck converter output stage is reduced to reduce the switching loss at light load condition. The segmented output stage technique improves the light load efficiency of the buck converter by the optimizing of the channel width of CMOS transistors [5], [23] and [24]. As the capacitance of the power switches is proportional to their channel width [12], the segmented output stage technique reduces the switching loss by reducing the channel width of the power switches to reduce the internal parasitic capacitance, C .

In the buck converter output stage, the MOS transistors operate in the triode region as switching resistors. From equation (2.13), note that the on resistance of the MOS transistors is inversely proportional to their channel widths W whereas the input capacitance is linearly proportional to their channel width [23]. Hence, the two major power losses of buck converter output stage are affected by the channel width of the MOS transistors and there should be an optimized value for the channel width, W to achieve the lowest power losses. Since the switching loss is dominant at light load, the channel width should be reduced to reduce the switching loss.

Figure 2.9 depicts the architecture of a digitally controlled DC-to-DC converter with segmented output stage. The PMOS and NMOS output stage transistors are partitioned into three independently controlled segments. These transistor segments are created by using identical unit cells connected in parallel to achieve binary weighting and monotonic resistance. The DPWM output is controlled by two 3-bit segment enable buses, en_P and en_N .

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Figure 2.9 Architecture of a digitally controlled DC-DC converter with a segmented output stage [5]

The measured power efficiency of the segmented output stage design with different channel widths (different enable codes) is shown in Figure 2.10. At extreme light load ($I_{OUT} < 10mA$), the segmented output stage design also adopts the PFM mode to improve the efficiency. The power efficiency at different load conditions is optimized by varying the channel width of the segmented output stage. However, it is very costly to implement all the combinations of the segments. For easy implementation, only 4 combinations (001,010,100,111) are chosen for the segment enable code.

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Figure 2.10 Measured efficiency versus output current for different channel width [5]

Figure 2.11 presents the power efficiency comparisons between the conventional design and the segmented output stage design with only 4 segment combinations of the output stage. The maximum power efficiency improvement is about 6.9% with both designs applying the PFM mode in the extreme light load.

Figure 2.11 Measured power efficiency comparison with and without segmented output stage [5]

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From Figure 2.11, note that the segmented output stage design has a great improvement in power efficiency for buck converter operating at high switching frequency. However, this design increases the circuit complexity and switching activities due to the dynamic adjustments of the channel widths according to different load conditions.

2.4.3 Low Voltage Swing Technique

Based on equation (1.1), the previous two techniques reduce the switching loss of the buck converter output stage by reducing the switching frequency f_s or both the switching frequency f_s and the internal parasitic capacitance, C . However, the switching loss is proportional to the square of the switching voltage range, V_{IN} . Hence, the gate drive voltage of the power switches is the most significant parameter for reducing the switching loss of the buck converter output stage. Figure 2.12 depicts the low voltage swing output stage of a buck converter [18]. This technique reduces the gate drive voltage of the MOS transistors by providing two voltage levels, V_{gp} and V_{gn} , for the upper and lower power switches, N1 and P1 respectively and their respective gate drive circuits. With these two voltages, the upper MOS transistors operate in a lower voltage swing between supply voltage V_{DDI} and voltage V_{gp} instead of between supply voltage and ground. On the other hand, the lower MOS transistors will operate between voltage V_{gn} and ground instead of between supply voltage and ground. The gate drive voltage waveforms for both the upper and lower power switches (P1 and N1) operating in full swing and low swing operations are depicted in Figure 2.13. As shown in the figure, the low voltage swing design reduces the switching voltage range of the internal parasitic capacitance of the MOS transistors, thereby resulting in less charge being required to

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charge and discharge the internal parasitic capacitance. In other words, the switching loss of buck converter output stage is reduced.

Figure 2.12 Low voltage swing output stage [18]

Figure 2.13 (a) Full swing gate drive voltage waveforms and (b) Low swing gate drive voltage waveforms. *(to be continued)*

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Figure 2.13 (a) Full swing gate drive voltage waveforms and (b) Low swing gate drive voltage waveforms. (*continued*)

The low voltage swing output stage design reduces the switching loss of buck converter output stage by reducing the most significant parameter in the switching loss equation - the switching voltage range of internal parasitic capacitance of the MOS transistors. However, two voltage levels, V_{gp} and V_{gn} , are required and both high side and low side power switches, P1 and N1, consume switching loss.

In this project, the proposed output stage design is based on the low swing technique because it is the most effective way to reduce the switching loss at light load condition.

2.5 Summary

In this chapter, two conduction mode operations for buck converter were introduced, namely the continuous conduction mode, CCM, and discontinuous conduction mode, DCM. In addition, two popular control techniques were discussed namely the PWM

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control with fixed switching frequency for medium or heavy load conditions and the PFM control with variable switching frequency for extreme light load condition.

Due to the limited energy capacity of battery, it is imperative to have high efficiency DC-to-DC converter over the entire load condition to extend the battery life time of portable devices. Three DC-to-DC converter output stage designs have been introduced in this chapter to improve the power efficiency of the converter over the entire load condition. First, the PWM and PFM dual mode technique improve the efficiency at light load by reducing the switching frequency of the converter. Second, the segmented output stage technique improves the efficiency at light load by reducing both the switching frequency and the internal parasitic capacitance to reduce the switching loss. Third, the low voltage swing technique improves light load efficiency by reducing the switching voltage range of the internal parasitic capacitance. However, the implementations of these techniques are complex and costly.

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As mentioned in Chapter 1, a DC-to-DC converter is unable to achieve 100% power efficiency due to power losses in the output stage. In general buck converter applications, the two major power losses of the output stage are the conduction loss and the switching loss. As mentioned in Chapter 2, switching loss is the dominant power loss at light load condition, while conduction loss is the dominant loss at heavy load. In this chapter, the power dissipation mechanisms of the DC-to-DC converter such as the conduction loss, switching loss, dead time loss, ESR (Equivalent Series Resistance) loss and controller quiescent power loss, etc shall be analysed in detail. The power dissipation mechanism analysis will also be carried out for buck converter output stage operating in different modes [8-10].

3.1 Conduction Loss

As mentioned earlier, conduction loss is caused by heat dissipated in the resistive components of the DC-to-DC converter. In a synchronous buck converter output stage, the dominant resistive components are (i) the finite on resistance of the high side (PMOS)

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and the low side (NMOS) switches, denoted by R_P and R_N respectively and (ii) the non-ideal DC resistance of the output inductor, R_{L-DC} . When the synchronous buck converter operates in different modes (PWM CCM mode, PWM DCM mode and PFM DCM mode), their conduction loss is different. This is because the rms current flowing through the resistive components in the output stage (R_P , R_N , and R_{L-DC}) is different. The conduction loss calculations for these three operation modes will be presented in the following subsections.

3.1.1 Conduction Loss in PWM CCM mode

As discussed in section 2.1.2, the RMS current value of the output stage working in PWM CCM mode is given in equation (2.3). The conduction loss includes 3 components: the PMOS conduction loss P_{P-Cond} , the NMOS conduction loss P_{N-Cond} and the inductor DC resistance conduction loss $P_{LDC-Cond}$ and can be expressed as follows.

The PMOS conduction loss (power loss when PMOS is conducting) can be expressed as:

$$\begin{aligned} P_{P_Cond} &= DR_P I_{rms,CCM}^2 \\ &= DR_P \left[I_{OUT}^2 + \frac{(\Delta I_L)^2}{12} \right] \end{aligned} \quad (3.1)$$

The NMOS conduction loss (power loss when NMOS is conducting) can be expressed as:

$$\begin{aligned} P_{N_Cond} &= (1-D)R_N I_{rms,CCM}^2 \\ &= (1-D)R_N \left[I_{OUT}^2 + \frac{(\Delta I_L)^2}{12} \right] \end{aligned} \quad (3.2)$$

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The inductor DC resistance conduction loss is:

$$\begin{aligned} P_{LDC_Cond} &= R_{L_DC} I_{rms,CCM}^2 \\ &= R_{L_DC} \left[I_{OUT}^2 + \frac{(\Delta I_L)^2}{12} \right] \end{aligned} \quad (3.3)$$

Hence, the total conduction loss of buck converter in PWM CCM mode is:

$$\begin{aligned} P_{Cond} &= P_{P_Cond} + P_{N_Cond} + P_{LDC_Cond} \\ &= [R_P D + R_N (1 - D) + R_{L_DC}] \times \left[I_{OUT}^2 + \frac{(\Delta I_L)^2}{12} \right] \end{aligned} \quad (3.4)$$

3.1.2 Conduction Loss in PWM DCM mode

As discussed in Section 2.1.3, the PWM DCM mode can achieve lower current RMS value by preventing negative inductor current from flowing across the low side switch, thereby resulting in a reduction in the conduction loss. The current RMS value of the output stage working in PWM DCM mode is given in equation (2.7). The PMOS conduction loss P_{P_Cond} , the NMOS conduction loss P_{N_Cond} and the inductor DC resistance conduction loss P_{LDC_Cond} in PWM DCM mode can be expressed as follows.

The PMOS conduction loss (power loss when PMOS is on) can be expressed as:

$$\begin{aligned} P_{P_Cond} &= DR_P I_{rms,DCM}^2 \\ &= DR_P \frac{1}{3} (2I_{OUT})^{3/2} \Delta I_{L,CCM}^{1/2} \end{aligned} \quad (3.5)$$

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The NMOS conduction loss (power loss when NMOS is on) is:

$$\begin{aligned} P_{N_Cond} &= (1-D)R_N I_{rms,DCM}^2 \\ &= (1-D)R_N \frac{1}{3}(2I_{OUT})^{3/2} \Delta I_{L,CCM}^{1/2} \end{aligned} \quad (3.6)$$

The inductor DC resistance conduction loss is:

$$\begin{aligned} P_{LDC_Cond} &= R_{L_DC} I_{rms,DCM}^2 \\ &= R_{L_DC} \frac{1}{3}(2I_{OUT})^{3/2} \Delta I_{L,CCM}^{1/2} \end{aligned} \quad (3.7)$$

Hence, the total conduction loss of buck converter in PWM DCM mode is:

$$\begin{aligned} P_{Cond} &= P_{P_Cond} + P_{N_Cond} + P_{LDC_Cond} \\ &= [R_P D + R_N (1-D) + R_{L_DC}] \times \frac{1}{3}(2I_{OUT})^{3/2} \Delta I_{L,CCM}^{1/2} \end{aligned} \quad (3.8)$$

3.1.3 Conduction Loss in PFM DCM mode

Pulse frequency modulation is applied at light load condition to further reduce the switching loss by reducing the switching frequency. The operation of the Burst frequency PFM has been discussed in section 2.2.1 where the number of pulse N and the burst frequency f_2 depends on the load condition. The RMS current is given by

$$\begin{aligned} I_{rms,PFM}^2 &= \left(\frac{I_{Peak,PFM}}{2} \sqrt{\left(1 + \frac{1}{3}\right) \frac{NT_1}{T}} \right)^2 \\ &= \frac{2}{3} I_{OUT} I_{Peak,PFM} \end{aligned} \quad (3.9)$$

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Hence, the conduction loss of the buck converter output stage operating in PFM DCM mode is given as follows.

The PMOS conduction loss (power loss when PMOS is on) can be expressed as:

$$\begin{aligned} P_{P_Cond} &= DR_P I_{rms,PFM}^2 \\ &= R_P \frac{2}{3} I_{OUT} I_{Peak,PFM} \frac{V_{OUT}}{V_{IN}} \end{aligned} \quad (3.10)$$

The NMOS conduction loss (power loss when NMOS is on) is:

$$\begin{aligned} P_{N_Cond} &= (1-D)R_N I_{rms,PFM}^2 \\ &= R_N \frac{2}{3} I_{OUT} I_{Peak,PFM} \frac{V_{IN} - V_{OUT}}{V_{IN}} \end{aligned} \quad (3.11)$$

The inductor DC resistance conduction loss is:

$$\begin{aligned} P_{LDC_Cond} &= R_{L_DC} I_{rms,PFM}^2 \\ &= R_{L_DC} \frac{2}{3} I_{OUT} I_{Peak,PFM} \end{aligned} \quad (3.12)$$

Hence, the total conduction loss of buck converter in PFM DCM mode is:

$$\begin{aligned} P_{Cond} &= P_{P_Cond} + P_{N_Cond} + P_{LDC_Cond} \\ &= \left[R_P \frac{V_{OUT}}{V_{IN}} + R_N \frac{V_{IN} - V_{OUT}}{V_{IN}} + R_{L_DC} \right] \times \left(\frac{2}{3} I_{OUT} I_{Peak,PFM} \right) \end{aligned} \quad (3.13)$$

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3.1.4 Comparison of Conduction Loss

The conduction loss of a synchronous buck converter output stage operating in three different control modes have been discussed in the previous sections. In this section, the conduction loss of the three different control modes will be compared and discussed.

Figure 3.1 depicts the conduction loss comparison between these three control modes. Note that the conduction loss in PWM DCM control is the smallest among the three operations when the output load current is less than 40mA. When output load current is higher than 40mA, the conduction loss is the same for both PWM DCM operation mode and PWM CCM operation mode. This is because when the output load current is greater than 40mA which is about half of the inductor current ripple, the conduction mode of the output stage switches from DCM to CCM. According to equation (3.13), the conduction loss in PFM DCM mode is linearly proportional to the output load current as shown in Figure 3.1. In addition, the conduction loss in PFM DCM mode is higher than that in the other two modes when output current is larger than about 5mA. Hence, the PWM DCM operation mode offers the lowest conduction loss at light load condition. This is because the PWM DCM control mode reduces the conduction time for both high side and low side power switches.

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Figure 3.1 Conduction loss comparisons

3.2 Switching Loss

At mentioned earlier, switching loss is one of the major power losses in a buck converter output stage. It is caused by the charging and discharging of the internal parasitic capacitances (switch node capacitance and gate capacitance of power switches) and can be categorized into two losses: hard switching loss and gate drive loss.

3.2.1 Hard Switching Loss

Hard switching loss is associated with the switching loss due to the lumped parasitic capacitance, C_x , at the switching node as depicted in Figure 3.2(a). The lump parasitic

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capacitance, C_x , is composed of the junction capacitance of the PMOS and the NMOS. The idealized transient waveforms of the drain current, I_d , and the drain source voltage, V_{DS} , of the high side PMOS is depicted in Figure 3.2(b). To simplify the analysis, the inductor current ripple is assumed to be negligible and the finite turn on resistance of power switches are ignored. Thus, the inductor current is equal to the output current (i.e. $I_L = I_{OUT}$) in steady state.

During the dead time before the PMOS is turned on, the drain-to-source voltage, V_{DSp} , of the PMOS is approximately equal to the supply voltage, V_{IN} . When the gate voltage, V_{G-P} , of the PMOS is reduced to approximately one threshold below the input voltage, the PMOS starts to turn on and the inductor current starts to shift from the low side switch to the high side switch. The drain-to-source voltage, V_{DSp} , of the PMOS remains equal to V_{IN} until I_D is close to I_{OUT} . The drain current I_D continues to increase until it reaches the peak value, I_{Peak} . The current charging up C_x is the difference in current between I_{Peak} and I_{OUT} (i.e. $I_{Peak} - I_{OUT}$) and the V_{DSp} of the PMOS will decrease until $V_{DSp} = 0V$.

Figure 3.2 (a) Schematic of buck converter with parasitic capacitor C_x at the switching node and (b) hard switching transient waveforms in PMOS (*to be continued*)

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Figure 3.2 (a) Schematic of buck converter with parasitic capacitor C_x at the switching node and (b) hard switching transient waveforms in PMOS (*continued*)

The total charge accumulated on C_x during the turn-on transient can be calculated by integrating the I_D waveform in the shaded area in Figure 3.2(b). Since the PMOS is operating in the saturation region during most of the transient, capacitance C_x is the dominant internal parasitic capacitance at the switching node of the output stage. If the charge stored in C_x at the end of the turn-on transient is Q_x . The current exceeding I_{OUT} , I_{Cx} , to charge the switching node can be expressed as

$$I_{Cx} = I_{Peak} - I_{OUT} = \frac{Q_x}{t_{vf}} = \frac{C_x V_{IN}}{t_{vf}} \quad (3.14)$$

where t_{vf} is the V_{DS} falling time.

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As shown in Figure 3.2(b), the total energy dissipated in the PMOS during the turn on transient can be calculated as

$$\begin{aligned} E_{P,on} &= \frac{1}{2}(I_{OUT} + I_{C_s})V_{IN}t_{cr} + \frac{1}{2}V_{IN}(I_{OUT} + I_{C_s})V_{IN}t_{vf} \\ &= \frac{1}{2}V_{IN}(I_{OUT} + I_{C_s})(t_{cr} + t_{vf}) \end{aligned} \quad (3.15)$$

Thus, the switching loss at the turn on transient of the PMOS is

$$P_{P,on} = \frac{E_{P,on}}{T_s} = \frac{V_{IN}(I_{OUT} + I_{C_s})(t_{cr} + t_{vf})}{2T_s} \quad (3.16)$$

Similarly, the loss at the turn off transient of the PMOS, $P_{P,off}$, can be calculated as

$$P_{P,off} = \frac{V_{IN}(I_{OUT} - I_{C_s})(t_{cr} + t_{vf})}{2T_s} \quad (3.17)$$

The switching loss of the PMOS during the turn on and turn off transients can be calculated by summing (3.16) and (3.17) as shown below. The turn on time is assumed to be equal to the turn off time.

$$P_{P,SW} = \frac{V_{IN}I_{OUT}(t_{cr} + t_{vf})}{T_s} \quad (3.18)$$

3.2.2 Gate Drive Loss

Gate drive loss is predominantly caused by the dynamic power used to charge and discharge the input parasitic capacitance of the power switches and their driving circuits.

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The input parasitic capacitance includes the gate-to-source capacitance, C_{GS} , and the gate-to-drain capacitance, C_{GD} . The equivalent input capacitance, C_G , is given by

$$\begin{aligned} C_G &= C_{GS} + 2C_{GD} \\ &= C_{ox} LW + (C_{GSO} + 2C_{GDO})W \end{aligned} \quad (3.19)$$

Note that the gate-to-drain capacitance has to be multiplied by two because the voltage change across C_{GD} is two times the switching voltage at the input [7].

Therefore, the gate drive power loss of the PMOS and the NMOS power switches can be expressed as follows.

$$P_{G,P} = f_s (C_{GS,P} + 2C_{GD,P}) V_{GS,P}^2 \quad (3.20)$$

$$P_{G,N} = f_s (C_{GS,N} + 2C_{GD,N}) V_{GS,N}^2 \quad (3.21)$$

Besides the gate drive loss of the PMOS and NMOS power switches, the gate drive loss also includes the loss in the gate drive circuits which is linearly proportional to their internal capacitance. The gate drive circuit consists of two strings of inverters to drive the power transistors – one for the PMOS and one for the NMOS. The string of inverters with M number of stages are designed with a tapering factor ap so that the driving circuit has sufficient current driving capability to drive the large input parasitic capacitance of the PMOS and NMOS power transistors. Therefore, the power consumption of the gate drivers for the PMOS and the NMOS power switches can be expressed as follows.

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$$P_{G,P} = f_s (C_{GS,P} + 2C_{GD,P}) V_{GS,P}^2 \left(\frac{ap^N - 1}{ap^N (ap - 1)} \right) \quad (3.22)$$

$$P_{G,N} = f_s (C_{GS,N} + 2C_{GD,N}) V_{GS,N}^2 \left(\frac{ap^N - 1}{ap^N (ap - 1)} \right) \quad (3.23)$$

The gate drive loss is independent of the load current whereas the hard switch loss is dependent on the load current. Hence, the gate drive loss is the dominant switching loss at light load whereas the hard switching loss is the dominant switching loss at heavy load.

3.2.3 Comparison of Switching Loss

In the previous chapter, two modulation control techniques namely the pulse width modulation control (PWM) and pulse frequency modulation control (PFM), have been introduced. In this section, the switching loss of the output stage operating in PWM and PFM modulation control at light load as depicted in Figure 3.3 will be compared. Note that the switching loss for both PWM and PFM controlled output stages are proportional to the output load current. This is because the hard switching loss in PWM mode is linearly proportional to the output load current. It can also be observed from the graph that the switching loss of the output voltage operating in PWM control mode is much higher than that in PFM control mode. This is because the PWM control operates at a much higher switching frequency than PFM control and the switching loss of the output stage is linearly proportional to its switching frequency. Hence, it is beneficial to operate at a lower switching frequency using PFM control at light load condition to reduce switching loss. Although PWM control achieves good regulation quality and high power

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efficiency at heavy load with high fixed switching frequency, the power efficiency drops rapidly at light load condition due to high switching loss.

Figure 3.3 Switching loss comparison

3.3 Dead Time Loss

Dead time is introduced in the PWM control signals to ensure that the two power switches are not turned on simultaneously. Thus, shoot through current between the high side and the low side power switches can be prevented. During the dead time when both of the power switches are off, the inductor current relies on the body diodes of the NMOS to flow continuously. Assuming that the dead time required for the PMOS to turn off before the NMOS turns on is the same as that required for the NMOS to turn off before the PMOS turns on, the dead time loss can be calculated as

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$$P_{Deadtime} = 2 \times V_{Diode} \times I_{OUT} \times T_{Deadtime} \times f_s \quad (3.24)$$

where V_{Diode} is the forward voltage drop of the diode.

3.4 ESR Loss

A non-ideal capacitor in the output filter has an equivalent series resistance, ESR [13] which consumes power when the capacitor is being charged and discharged. The current flowing through the ESR in the PWM mode and the PFM mode is different and the ESR loss can be calculated as follows.

ESR loss in PWM mode:

$$P_{ESR,PWM} = R_{ESR} \times \frac{(\Delta I_L)^2}{12} \quad (3.25)$$

ESR loss in PFM mode:

$$\begin{aligned} P_{ESR,PFM} &= R_{ESR} \times \left(\frac{I_{Peak,PFM}}{2} \sqrt{\frac{1}{3} \times \frac{N \times T_1}{T}} \right) \\ &= R_{ESR} \times \frac{1}{6} \times I_{OUT} \times I_{Peak,PFM} \end{aligned} \quad (3.26)$$

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3.5 Quiescent Power of the Controller

The equivalent power consumed by the controller of the DC-to-DC converter is known as the controller quiescent power. Typically, the quiescent power of the PWM controller is much lower than the sum of the switching and the conduction losses of the converter in continuous conduction mode. The controller quiescent power loss can be calculated as

$$P_Q = I_Q \times V_{IN} \quad (3.27)$$

where I_Q is the quiescent current.

3.6 Power Consumption at Light Load Condition

As discussed in Chapter 2, switching loss is the dominant power loss of the buck converter output stage at light load condition. Hence, the switching loss, in particular the gate drive loss, has to be reduced in order to improve the power efficiency at light load. According to equation (1.1), switching loss is proportional to three parameters, namely the switching frequency, the internal parasitic capacitance and the switching voltage range. In order to reduce the switching loss at light load, one or a combination of these three parameters has to be reduced. However, the reduction of these three parameters will have the same side effect of increasing the conduction loss of the output stage. Figure 3.4 depicts the total power losses of a buck converter output stage operating in PWM CCM mode with one of the three parameters reduced at light load. From Figure 3.4, note that the buck converter with reduced switching frequency has the highest power losses at light

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load, because according to equations (2.3) and (3.4), the conduction loss is linearly proportional to the square of the inductor current ripple at light load condition and the inductor current ripple is inversely proportional to the switching frequency. Put differently, the conduction loss is inversely proportional to the square of the switching frequency at light load. Hence, the conduction loss will be increased significantly when the switching frequency of the output stage is increased. On the other hand, a buck converter with reduced switching voltage has the lowest power losses. This is because according to equations (1.1), (2.13) and Figure 2.6, the switching loss is linearly proportional to the square of the switching voltage swing. The increase in turn on resistance of the power transistors is small if the gate drive voltage is three times higher than the threshold voltage of the power transistors.

Based on equations (1.1), (2.13) and (3.19), the switching loss is linearly proportional to the internal capacitance of the output stage and the method to reduce the internal capacitance of the output stage is to reduce the channel width of the power transistors, but the channel width of the power transistor has a inverse proportion relationship with its turn on resistance.

In summary, the reduction of the switching voltage of the buck converter output stage produces the greatest reduction in switching loss and result in only a small increase in the conduction loss. Hence, this is the best method to improve the light load power efficiency.

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Figure 3.4 Total Power Losses at Light Load

3.7 Summary

This chapter presents the power dissipation analysis of buck converters output stage operating in three different modes namely PWM with CCM mode, PWM with DCM mode and PFM with DCM mode. Next, power loss comparison is presented and discussed for the output stage operating in different operation modes. The two major power losses in the buck converter output stage are conduction loss and switching loss. Switching loss is the dominant power loss at light load condition and conduction loss is the dominant loss at heavy load condition. Therefore, in order to improve the light load power efficiency of the buck converter output stage, the switching loss needs to be reduced. Through the analysis, it is noted that the most efficient method to improve the

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light load power efficiency is to reduce the switching voltage swing of the power transistors of the output stage.

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In Chapter 2 and 3, we have shown that the conduction and switching losses of the power output stage are dependent on MOS parameters such as the channel width W and the gate-to-source voltage, V_{GS} . Based on equation (1.1) and Figure 2.6, we note that a more effective way to reduce the power dissipation of the buck converter output stage at light load condition is to reduce the switching loss by means of reducing the V_{GS} of the PMOS and NMOS transistors. However, the V_{GS} has to be at least three times higher than the threshold voltage so that the on resistance of the power transistors is not increased significantly. Therefore, instead of reducing the switching frequency at light load in dual-mode PFM/PWM technique or adjusting the channel width of the transistors according to the load current in the segmented output stage technique, the proposed design reduces the gate drive voltage of the power switches and recycles the gate drive charge stored in the internal capacitance to improve the light load power efficiency. The proposed design operating in different load conditions and different control modes will be introduced in the following subsections.

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4.1 Proposed Design at Light Load

In Chapter 3, the two types of switching loss for the buck converter output stage namely the hard switching loss and the gate drive loss have already been discussed. Since the hard switching loss is proportional to the output load current, while gate drive loss is independent of the load current, gate drive loss is the dominant loss at light load condition. Hence, the main focus in this chapter is to reduce the gate drive loss at light load in order to improve the light load power efficiency of the buck converter output stage.

Figure 4.1 depicts the schematic of the proposed output stage for the buck converter at light load. In the proposed design, a charge recycling capacitor $C1$ is connected to the source of the NMOS, $N2$, and the source of the PMOS, $P3$. The basic concept of this design is to reduce the switching voltage swing of the input parasitic capacitance of the upper and lower power switches, $P1$ and $N1$. In addition, the proposed design also recycles the charge stored in the input parasitic capacitance of the PMOS power transistor, $P1$, to charge up the input parasitic capacitance of the NMOS power transistor, $N1$.

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Figure 4.1 Proposed design schematic at light load

The operation of the proposed design at light can be divided into two operations: startup operation and steady stage operation. The operating principles are as follows.

4.1.1 Startup Operation

At the beginning of the startup period, the voltage across the charge recycling capacitor $C1$ is zero. Hence, it is unable to provide any power to drive the lower power switch $N1$ through transistor, $P3$. During the startup period, capacitor $C1$ will accumulate the charge discharged by the input capacitance of power switch $P1$ when $P1$ is turning on. The voltage across $C1$, V_{C1} , is compared with a predetermined voltage level, V_{refc} . When V_{C1} is lower than V_{refc} , transistor $P4$ will be enabled to drive the lower power switch $N1$. Note that transistor $P3$ is off. The total charge stored in the capacitor $C1$ is given by

$$Q = CV \quad (4.1)$$

where Q is the total charge in the capacitor, C is the capacitance and V is the voltage across the capacitor.

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According to equation (4.1), the total charge stored in capacitor $C1$ is linearly proportional to the voltage across it as capacitance C is a constant. Therefore, the voltage across capacitor $C1$ increases as the total charge stored in $C1$ increases. Figure 4.2 depicts the control waveforms across the various nodes when $C1$ is charging. The waveforms include the PWM signal, the gate control voltage, V_{G-P1} and V_{G-N1} , of the two power switches, P1 and N1, respectively, the voltage across the charge recycling capacitor $C1$, V_{C1} , and the output voltage of the comparator, V_{CMP} , in the startup state. As shown in Figure 4.2, the gate control voltage of power switch P1 increases as the voltage across the charge recycling capacitor $C1$ increases, while the gate control voltage of N1 remains constant at supply voltage level, V_{IN} . In addition, the output voltage of the comparator is low as the voltage across $C1$ is lower than the predetermined voltage level, V_{refc} .

Figure 4.2 Gate control waveforms in the startup state

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4.1.2 Steady Stage Operation

The steady state operation commences when the capacitor voltage, V_{C1} , is greater than the predetermined voltage level V_{refc} and the comparator output goes from low to high. As a result, transistor P4 is switched off while transistor P3 is activated to drive the power switch N1. Put differently, the charge in capacitor C1 will flow through transistor P3 to charge up the input capacitance of power switch N1 when N1 is turning on. In this state, the charge discharged from the input capacitance of power switch P1 and the charge required to charge up the input capacitance of power switch N1 can be expressed as follows.

The charge discharged from the input capacitance of P1 is

$$Q_{CP} = C_{G-P}(V_{IN} - V_{C1}) \quad (4.2)$$

The charge required to charge up the input capacitance of N1 is

$$Q_{CN} = C_{G-N}V_{C1} \quad (4.3)$$

where C_{G-P} and C_{G-N} are the input capacitance of power switch P1 and N1 respectively.

Based on charge conservation theory in the steady state, the charge discharged from the input capacitance of power switch P1 is equal to the charge required to charge up the input capacitance of power switch N1 at a certain capacitor voltage level. Therefore, the capacitor voltage V_{C1} in steady state is given by

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$$V_{C1} = \frac{C_{G-P} V_{IN}}{C_{G-P} + C_{G-N}} \quad (4.4)$$

Figure 4.3 depicts the PWM signal, the gate control voltage, V_{G-P1} and V_{G-N1} , of the two power switches, P1 and N1, respectively, the voltage across the charge recycling capacitor C1, V_{C1} , and the output voltage of the comparator, V_{CMP} , in steady state. In Figure 4.3, note that the gate control voltage of power switches, P1 and N1, is equal to the voltage of the charge recycling capacitor C1, V_{C1} . In other words, at voltage V_{C1} , the charge discharged from the input capacitance of the upper power switch P1 is fully transferred to the charge recycling capacitor C1 to charge up the input capacitance of the lower power switch N1. Hence, the input capacitance of the lower power switch does not consume any charge from the power supply.

Figure 4.3 Gate control waveforms in the steady state

At light load condition, the gate-to-source voltage for both power switches P1 and N1 is reduced from the supply voltage V_{IN} to $V_{IN} - V_{C1}$ and V_{C1} respectively, in steady state. This will reduce the switching loss of power switches P1 and N1 tremendously. In

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addition, the charge of the input capacitance can be recycled. However, as we have shown in equation (2.13) earlier, the reduction of gate-to-source voltage will increase the turn on resistance of the power switches.

4.2 Proposed Design for the Entire Load Condition

As discussed in the previous chapters, the conduction loss and the hard switching loss are proportional to the output load current. Hence, these losses will be increased when the load current increases. Figure 4.4 depicts the conduction loss and the switching loss of the output stage at different load conditions. Note that the switching loss is higher than the conduction loss when the output load current is less than 120mA. However, the conduction loss increases at a much faster rate than the switching loss when the load current is higher than 120mA. Therefore, the conduction loss is the dominant power loss of the buck converter output stage at medium and heavy load conditions.

Figure 4.4 Output stage power losses versus load current

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As the switching loss is dominant at light load, the proposed design reduces the gate drive voltage for both the upper and the lower power switches to reduce the switching loss. However, the reduction of the gate drive voltage induces an incremental increase in the turn on resistance of the power switches. In other words, the conduction loss is increased as a result.

At medium and heavy load conditions, the conduction loss will become the dominant power loss of the output stage. In other words, the power loss induced by the incremental increase in turn on resistance of the power transistors is more than the reduction in power loss due to the switching loss. Therefore, the proposed design will have lower power efficiency than the conventional design when the load current is higher than a certain value. In order to have relatively high power efficiency in the entire output load current range for the buck converter output stage, the gate-to-source voltage for both power switches P1 and N1 should be switched to full swing at medium and heavy load conditions.

The proposed design of the DC-to-DC converter output stage for the entire output load condition is depicted in Figure 4.5. It contains an upper switch control circuit and a lower switch control circuit, which control the gate drive voltage levels for both the upper and the lower power switches, P1 and N1, respectively, according to the output signal of the current sensing circuit.

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Figure 4.5 Proposed design for the entire load condition

Figure 4.6 presents the waveforms of the proposed design at different output operation periods: startup period and operating period (light load and heavy load conditions). The waveforms include the PWM drive signals of both the upper and the lower power switches, V_{drive_P} and V_{drive_N} , the output signal of the current sensing circuit V_S , the output signal of the comparator V_{CMP} , the output signals of the both upper and the lower switch control circuits, V_{P2} , V_{N2} , V_{N4} , V_{P4} , V_{P3} and V_{N3} , and the gate drive voltages for P1 and N1, V_{G_P1} and V_{G_N1} respectively.

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Figure 4.6 (a) Signal waveforms in startup period and (b) Operating period (light load and heavy load conditions) *(to be continued)*

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Figure 4.6 (a) Signal waveforms in startup period and (b) Operating period (light load and heavy load conditions) (*continued*)

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During the startup period, the voltage across the charge recycling capacitor $C1$, V_{C1} , is lower than the predetermined voltage level V_{refc} . Hence, the output voltage of the comparator, V_{CMP} , is low. Transistor N2 is enabled to turn on the power switch P1 when the upper gate drive voltage V_{drive_P} goes low and P4 is activated to drive the lower power switch N1. Hence, the charge recycling capacitor $C1$ accumulates the charge discharged from the input capacitance of power switch P1 and the voltage across the capacitor $C1$ will increase. During this period, the gate drive voltage of P1 is between the supply voltage, V_{IN} , and the capacitor $C1$ voltage, V_{C1} , while the gate drive voltage of N1 is between the supply voltage, V_{IN} , and ground. The output signal of the current sensing circuit has no effects on the low swing or full swing voltage control selection.

During the operating period, the voltage across the charge recycling capacitor $C1$, V_{C1} , is high than the predetermined voltage level V_{refc} , and the output voltage of the comparator, V_{CMP} , goes from low to high. Hence, the output signal of the current sensing circuit becomes the control signal for the full swing and low swing gate control selection. Note that the signals, V_{P2} and V_{N3} , always follow the gate drive signals, V_{drive_P} and V_{drive_N} , while the activations of transistors, N2, N4, P2 and P4, are controlled by the output signal of the current sensing circuit, V_S . When V_S is low, indicating that the load current is light, transistors, N2 and P3, are enabled to drive the upper and lower power switches, P1 and N1, while transistors, N4 and P4, are always off. Therefore, the upper gate drive voltage, V_{G_P1} , switches between the supply voltage, V_{IN} , and the capacitor voltage, V_{C1} , while the lower gate drive voltage, V_{G_N1} , switches between the capacitor voltage, V_{C1} , and ground. In other words, the switching voltage swing for both the upper and lower power switches, P1 and N1, is reduced. The lower power switch, N1, only consumes the recycled charge

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for charging up its input capacitance when it is turned on, instead of drawing current from the power supply in conventional design. When output load current increases, the output signal of the current sensing circuit, V_S , goes from low to high. This will cause transistors, N2 and P3, to turn off and the charge recycling capacitor $C1$ will be idling, while transistors, N4 and P4, will be enabled to drive the upper and the lower power transistors. Hence, the gate drive voltage for both the upper and the lower power switches is between the supply voltage, V_{IN} and ground. In other words, full swing gate drive control is applied just like the conventional design at medium and heavy load conditions.

4.3 Proposed Design with DCM Control and Pulse Skipping in Extreme Light Load

As discussed in Chapter 2, if the output load current is less than half of the inductor current ripple and the output stage is operating in continuous conduction mode, the inductor current will go negative momentarily. This will result in a discharge of the output capacitor, C_{OUT} , through the inductor, L_O , and the lower power switch, N1, thereby resulting in power loss. Hence, negative inductor current has to be prevented to improve the efficiency at the extreme light load condition. An effective way to prevent the negative inductor current is to turn off the lower switch N1 when the inductor current reaches zero and is about to go negative. When the transistor N1 is off, the body diode of N1 will block the current from flowing to ground.

To improve the extreme light load efficiency, PWM DCM mode is adopted for the proposed design. The PWM DCM mode operates with a fix switching frequency and the

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inductor current is discontinuous at extreme light load. Figure 4.7 depicts the inductor current waveforms and directions for the PWM CCM and DCM modes at the extreme light load condition.

Figure 4.7 (a) Inductor current waveforms in PWM CCM and DCM modes and (b) Direction of inductor current following.

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Figure 4.8 depicts the proposed low swing design with PWM DCM control and pulse skipping ability at extreme light load condition. PWM DCM control and pulse skipping ability are utilized by a comparator CMP1, a DCM controller and a pulse skipper. The basic idea of the proposed design at extreme light load is to turn off the lower power switch, N1, to prevent negative inductor current from flowing, when the inductor current, I_L , reaches zero and goes negative. The PWM DCM also skips one pulse for every two pulses to reduce the switching frequency by half. With this control technique, the turn on time of both the upper and the lower power switches will be reduced, thereby reducing the conduction loss. In addition, the switching frequency is reduced by half and makes the switching loss even lower.

Figure 4.8 Proposed low swing design with PWM DCM control and pulse skipping ability at extreme light load

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4.3.1 DCM Controller

In order to detect the direction of the induction current when the power transistor N1 is conducting, a comparator CMP1 is used to compare the switching node voltage, V_X , with ground. This is because when the current flow of the inductor, I_L , changes from positive to negative, the switching node voltage, V_X , will also change from negative to positive. The output voltage of comparator CMP1, V_{CMP1} , is used as an input of the DCM controller to generate the DCM control signal to prevent the negative inductor current from following.

Figure 4.9 depicts the block diagram of the DCM controller. There are four inputs, V_{drive_P} , V_{CMP} , V_{CMP1} and V_{drive_N} , and one output, V_{DCM} . As mentioned in Chapter 3 and Figure 3.2(a), the parasitic capacitances at the switching node are lumped together and denoted as C_x . When the inductor current reaches zero and goes negative while the lower power switch, N1 is turned off, the inductor and the lumped parasitic capacitance, C_x , will become a resonant circuit and generate high frequency components, V_X , at switching node. This will also creates high frequency switching at the output of comparator CMP1. To circumvent this problem, a SR latch as shown in Figure 4.9 is used to remove the high frequency components at the output of the comparator.

Figure 4.9 Block diagram of DCM controller

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Figure 4.10 depicts the input and output waveforms of the DCM controller. Note that when the output voltage of the comparator CMP, V_{CMP} , remains low, the output of the DCM controller will follow the input signal, V_{drive_N} , and the buck converter output stage will operate in CCM mode. On the other hand, when the output voltage of the comparator CMP, V_{CMP} , goes high, the buck converter will operate in DCM. In DCM mode, the on time of the lower power switch, N1, will be reduced. This is because the lower power switch, N1, will turn off when the inductor current reaches zero and goes negative. Hence, negative inductor current is prevented in DCM mode.

Figure 4.10 Input and output waveforms of DCM controller

When the output load current, I_{OUT} , is higher than half of the inductor current ripple, I_{ripple} , the inductor current is always positive. Hence, the switching node voltage, V_X , is always negative when the lower power switch, N1, conducts. In other words, the output voltage

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of comparator CMP1 will remain low during the period when N1 conducts. Thus, the output signal of the DCM controller, V_{DCM} , will follow the input signal, V_{drive_N} and the buck converter output stage will operate in CCM mode.

4.3.2 Upper and Lower Switch Control

As discussed earlier, the upper and the lower switch control circuits are used to select whether the output power transistors are in the low swing or full swing gate voltage control for the entire load condition. While operating in the extreme light load condition, the lower switch control circuit has another function - to turn off the lower power switch, N1, if the inductor current reaches zero and goes negative. This will prevent the output capacitor C_{OUT} from discharging through the inductor.

Figure 4.11 depicts the schematic of the lower switch control for DCM operation. Note that the upper switch control is the same as that in Figure 4.5. The main difference in the lower switch control for DCM in Figure 4.11 and the lower switch control in Figure 4.5 is the addition of one OR gate to implement the DCM operation in extreme light load condition.

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Figure 4.11 Lower switch control for DCM operation

There are four inputs, V_{CMP} , V_S , V_{drive_N} and V_{DCM} , and three outputs, V_{P4} , V_{P3} , V_{N4} in the lower switch control block. Figure 4.12 depicts the input and output waveforms of the lower switch control in DCM operation. Note that the output signal, V_{P4} , remains high and transistor, P4, is always off while the output signals, V_{P3} and V_{N4} , follow the output signal of DCM controller, V_{CMP} . Therefore, the lower power switch, N1, is turned off when the inductor current reaches zero, thereby preventing the output capacitor C_{OUT} from discharging. It can also be observed that the turn on time of the lower power switch, N1, is shorter than that in CCM operation.

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Figure 4.12 Input and output waveforms of lower switch control

4.3.3 Pulse Skipper

At extreme light load condition, the output power is low since the output current is small and the power loss is dominated by the switching loss. Although the proposed low swing design reduces the switching loss significantly by reducing the gate drive voltage of the upper and lower power switches and by recycling the gate drive charge, the switching loss still contributes a relatively large portion of power consumption in the output stage. In order to reduce the switching loss further at extreme light load condition, a pulse

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skipper circuit is introduced. The basic concept of the pulse skipper circuit is to skip one PWM pulse for every two pulses. Hence, the switching frequency of the buck converter output stage will become half of the switching frequency at medium or heavy load conditions.

Figure 4.13 illustrates the block diagram of the pulse skipper circuit. The circuit consists of two D latches and some logic gates such as inverter, OR and AND gates. There are four inputs, V_{PWM} , V_{CMP} , V_{drive_N} and V_{DCM} , and one output, V_{DCMS} .

Figure 4.13 Block diagram of the pulse skipper

Figure 4.14 depicts the inputs and output waveforms of the pulse skipper circuit in DCM and CCM operations. As shown in Figure 4.14(a), when the output voltage of the comparator CMP, V_{CMP} , is low, the pulse skipper circuit is deactivated. Hence, the output signal, V_{PWMS} , follows the input PWM signal, V_{PWM} . On the other hand, when the comparator output voltage, V_{CMP} , goes from low to high, the pulse skipper will detect the output load current condition by detecting the voltage level of the input signal, V_{drive_N} , at the rising edge of the input signal, V_{DCM} . If the voltage level of the input signal, V_{drive_N} , is detected low, the buck converter is operating in DCM condition then the pulse skipping is

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enabled. Hence, one pulse is skipped at the output for every two input PWM pulses, thereby reducing the switching frequency by half at extreme light load condition.

Figure 4.14 Input and output waveforms of pulse skipper (a) DCM operation and (b) CCM operation

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On the other hand, if the voltage level of the input signal, V_{drive_N} , is detected high at the rising edge of the input signal, V_{DCM} , this indicates the buck converter operates in CCM mode. Then the output signal of the pulse skipper, V_{PWMs} , follows the input PWM signal, V_{PWM} . Hence, no pulse will be skipped.

4.4 Layout of Proposed Design

The proposed low swing output stage design had been implemented in layout level using AMS 0.35 μ m CMOS process. Figure 4.15 presents the layout of the design. The size of the IC without bond pads is approximately 1.3mm $\times$ 1.3mm.

Figure 4.15 Layout of the proposed design

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The layout of the proposed design has been converted to the extracted view and the post-layout simulation has been performed to verify the power efficiency improvement of the proposed design. The power efficiency comparisons between the schematic simulation and the post-layout simulation will be discussed in detail in the next chapter.

4.5 Summary

In this chapter, the proposed low voltage swing output stage design with charge recycling scheme is discussed in detail. In order to have a relatively high power efficiency in the entire output load current range, different control operations are applied in different output load range. First, the pulse skipping PWM DCM control operation with low voltage swing output stage configuration is enabled at extreme light load condition when the output load current is lower than half of the inductor current ripple. Second, the PWM CCM control operation with low voltage swing output stage configuration is applied at light load condition, when output load current is higher than half of the inductor current ripple but is less than a predetermined current value (i.e. 100mA). Finally, the PWM CCM control operation with full voltage swing output stage configuration is applied when the output load current is higher than a predetermined current value (i.e. 100mA). The proposed design has been realized in IC layout level and post-layout simulation has been performed to verify the proposed design.

CHAPTER 5 POWER EFFICIENCY COMPARISON

CHAPTER 5

POWER EFFICIENCY COMPARISON

In portable electronic devices, the energy is usually drawn from a battery through a DC-to-DC converter or a linear voltage regulator. As the energy capacity of a battery is very limited, it is imperative to have a DC-to-DC converter with high power efficiency in the entire output load range, in particular at light load condition, to extend the life time of the battery. This is because most of the portable applications are usually operating in the standby mode with low output current. Hence, the proposed low voltage swing design is adopted to improve the light load power efficiency of a synchronous buck converter. As a result, the power efficiency comparisons at light load condition are mainly focused in this chapter.

For power efficiency comparison, the power dissipation analysis and power efficiency calculation as discussed in Chapter 3 will be applied for the three buck converter output stage designs: the conventional design, the segmented design and the proposed design. Meanwhile, these three output stage designs are implemented and simulated with AMS

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0.35 μ m CMOS process in Cadence. To provide a fair comparison, the total channel width of the power switches, P1 and N1, of the three output stages are designed to be the same. The other design parameters are presented in Table 2 below.

Table 2 Design parameters for buck converter output stage

Design parameter	Value
Input voltage	3.6V
Output voltage	1.2V
Switching frequency	2MHz
Output inductor	4.7 μ H
Output capacitor	4.7 μ F

5.1 Power Efficiency in PWM CCM Mode

As mentioned in Chapter 2, the output stage is controlled by the PWM and operates with a fixed frequency and a variable duty ratio depending on the output and input voltage ratio. It may also be worthwhile to note that the inductor current flows continuously when output stage is operating in continuous conduction mode.

5.1.1 Power Consumption Comparison

Before the power consumption comparison of the three output stages is made, it may be worthwhile to have a summary of the important point which has been discussed in the previous chapters.

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In Figure 4.4, it is noted that switching loss is the dominant power loss at light load condition when the output load current is less than 120mA. It may also be worthwhile to reiterate that switching loss depends mainly on the switching frequency instead of the output load current. In order to reduce the switching loss at light load condition, the segmented output stage design [5] reduces the input capacitance of the power switches by reducing their channel widths at light load, while the proposed low voltage swing design reduces the gate drive voltage of the power switches and recycles the gate drive charge to achieve low switching loss. Although the approach adopted by the two designs increases the turn on resistance of the power switches at light load condition, thereby increasing the conduction loss, the overall power losses of the output stage are still reduced. This is because the switching loss of the output stage is much higher than the conduction loss at light load condition.

Figures 5.1(a) and 5.1(b) depict the power consumption distribution of the output stage operating in PWM CCM mode for the three designs at different load conditions, $I_{OUT} = 1\text{mA}$ and 50mA . To compare the performance of these three designs, the total power consumption of the conventional output stage design is being used as a reference. As shown in the power distribution charts in Figure 5.1, the switching loss, conduction loss, dead-time loss and ESR loss are considered. Note that the conduction loss increases as output load current increases from 1mA to 50mA for all the three output stage designs, which is in line with the dominant power loss graph in Figure 4.4.

From Figure 5.1, note that the proposed design has the lowest power loss followed by the segmented output stage design and the conventional design. The major differences of the

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power loss distribution in the three designs are the switching loss and the conduction loss. The switching loss of both segmented output stage design and the proposed low voltage swing design is much lower than that in the conventional design, especially at 1mA load current condition. On the other hand, the conduction loss of these two designs is slightly greater than that in the conventional design. Therefore, the total power losses for the segmented and the proposed design are smaller than the conventional design. Hence, the power efficiency of the segmented and the proposed output stage design at light load condition is higher than that of the conventional design.

From Figure 5.1(a), it can be observe that the switching loss of the segmented design and the proposed design is comparable. However, the proposed design has a smaller conduction loss. This is because the segmented output stage reduces the channel width of the power switches to reduce the switching loss. Since the channel width of the power switches is linearly proportional to the turn on resistance according to equation (2.13), the conduction loss will also be increased proportionally. On the other hand, the proposed design reduces the gate-to-source voltage of the power transistor to reduce the switching loss. This approached will have a lower effect on the turn on resistance of power switches as discussed in Chapter 2 (see Figure 2.6). Therefore, the power efficiency of the proposed design is better than the segmented design and the conventional design in light load condition.

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(a)

(b)

Figure 5.1 Power consumption distribution (a) $I_{OUT} = 1\text{mA}$ and (b) $I_{OUT} = 50\text{mA}$

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When the load current is increased from 1mA to 50mA, the power loss saving for both the segmented output stage design and the proposed design is much lesser. This is because the contribution of the hard switching loss and the conduction loss is increased when the output load current increases. In addition, the switching loss reduction of the two designs is about the same as their increment in conduction loss. Hence, the conventional output stage configuration is preferred at medium and heavy load condition.

5.1.2 Power Efficiency Comparison

The three output stage designs are implemented and simulated using AMS 0.35 μ m CMOS process model in Cadence. Figure 5.2 depicts the power efficiency of the three designs operating in PWM mode (DCM mode is applied when output load current is less than 45mA; otherwise, CCM mode is applied). The dotted lines depict the power efficiency based on theoretical calculation and the solid lines depict the power efficiency obtained by Hspice simulation.

From Figure 5.2, note that the proposed design has the best performance in terms of power efficiency across the entire load current range, followed by the segmented output stage design. The power efficiency of both segmented output stage and proposed design based on simulation is lower than that based on theoretical calculation at light load condition. This is because the additional control circuits required in the proposed design and the segmented output stage design consume additional power. However, the power efficiency of the proposed design and the segmented output stage design is still higher than the conventional design when output load current is less than 50mA.

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At light load condition, the power efficiency of the proposed design is much higher than the other two designs, 8% higher than the segmented output stage design and 15% higher than the conventional design. At medium and heavy load condition, the proposed design switches from low swing configuration to full swing configuration, which has the same configuration as the conventional design. Therefore, the power efficiency of the proposed design is almost the same as that of the conventional design.

Although the power efficiency of the proposed design is the highest at light load condition, it is still very low compared to that at medium and heavy load condition. Hence, further power efficiency improvement at light load condition is necessary.

Figure 5.2 Power efficiency in PWM mode

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5.2 Power Efficiency in PWM DCM Mode with Pulse Skipping

As discussed in the previous chapter, the PWM DCM operation mode with pulse skipping control is introduced to the proposed output stage at the extreme light load condition to reduce the switching frequency to improve the power efficiency. By operating in DCM mode, negative inductor current is prevented. Hence, the output capacitor is not discharged through the inductor and the low side switch to ground. Due to the skipping of one pulse for every two pulses, the switching frequency of the output stage is reduced by half at heavy load condition. Hence, the power efficiency of the proposed design operating in DCM mode with pulse skipping control will be higher than that of the output stage operating in the PWM DCM mode since the switching loss is effectively reduced.

Figure 5.3 depicts the power efficiency of the proposed output stage operating in PWM DCM with skipping mode and PWM DCM mode at light load condition. As shown in the figure, the power efficiency of the proposed design operating in PWM DCM mode with pulse skipping control is higher than that operating in PWM DCM mode when the output load current is lower than 45 mA. The load current is about half of the inductor current ripple value. As the output load current is higher than half of the inductor current ripple value, the DC-to-DC converter in PWM DCM mode with pulse skipping control will be switched to PWM CCM control automatically. Hence, the power efficiency of the DC-to-DC converter can be optimized over the entire load range by switching the converter between PWM DCM mode and PWM CCM mode.

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Figure 5.3 Power efficiency of proposed design operating in PWM mode and PWM mode with pulse skipping

5.3 Power Efficiency in PFM Mode

As technology becomes more advanced, more RF functions will be available in portable devices. The RF functional blocks are usually very sensitive to noise. Hence, the power supply for the portable applications cannot be taken simply as a black box with guaranteed maximum output noise level in the specifications [26]. Noise analysis of the power supply for portable devices must be taken into consideration.

In some of the DC-to-DC converter designs, pulse frequency modulation (PFM) control technique is preferable at light load condition [17], [20-22]. This is because PFM control can reduce the switching frequency substantially at extreme light load condition, i.e. 1/50 times of the switching frequency at full load condition, or even 1/100 times. According to

CHAPTER 5 POWER EFFICIENCY COMPARISON

equation (2.11), the switching frequency of PFM control technique is proportional to the output load current (i.e. the output load current increases when the switching frequency increases). Hence, PFM control has variable switching frequency, which produces unpredictable noise performance that spreads over a wider range of frequencies [26], [27]. On the other hand, fixed frequency PWM does not encounter such problem. PWM control will provide the most stable and predictable noise performance and generates noise peak at the switching frequency and its harmonics.

In order to have predictable noise of the power supply and comparable power efficiency, a lower fixed switching frequency PWM control (i.e. 1/10 times of full load switching frequency) is applied to the proposed design at light load condition. Unlike PFM control where the switching frequency is proportional to the output load current, the duty ratio of the PWM signal (at fixed switching frequency) is proportional to the output load current.

Figure 5.3 depicts the power efficiency of the proposed design operating in lower PWM control, the segmented output stage design and the conventional design operating in PFM mode. As shown in the figure, the proposed design with lower fixed switching frequency has comparable power efficiency to the other two designs operating in PFM mode. As the proposed design operates at a fixed higher frequency, it provides the most stable and predictable noise performance and generates noise peak at the switching frequency and its harmonics.

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Figure 5.4 Power Efficiency in PFM mode

5.4 Post-layout Simulation Result

As mentioned in Chapter 4, the proposed output stage design has been implemented in layout level and post-layout simulation has been performed by using the extracted view of the layout to verify the power efficiency improvement of the proposed design. The power efficiency in DCM mode obtained from schematic simulation and post-layout simulation is depicted in Figure 5.5. From Figure 5.5, note that the power efficiency obtained from post-layout simulation is much closed to the power efficiency obtained from schematic simulation, thereby showing that the power efficiency of the proposed design is achievable.

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Figure 5.5 Efficiency comparisons between schematic and post-layout simulation

5.5 Measurement Results

In order to verify that the proposed output stage design can achieve better power efficiency for DC-to-DC converters at light load condition in practical implementation, the proposed output stage design for light load and the conventional output stage have been implemented using discrete components. The part numbers of the discrete components are listed in Table 3 below.

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Table 3 Part numbers of discrete components

Schematic Label	Part Number
P1	NTR1P02LT1
N1	NTA4153N
P2	BSS84LT1
N2	BSS123LT1
P3	BSS84LT1
N3	BSS123LT1
OR	SN74LVC2G32
INV	NC7SZ14
L _O	10uH
C _{OUT}	22uF

The schematics of the proposed output stage and conventional output stage implemented with discrete components are depicted in Figure 5.6. As shown in Figure 5.6, the charge recycling capacitor C1 in the proposed output stage is used to reduce the switching voltage swing of the internal parasitic capacitance of the power transistors, N1 and P1. Additional power is also being saved by using capacitor C1 to collect the charge discharge by the PMOS power transistor P1. The charge stored in C1 is subsequently recycled by using it to drive the NMOS power transistor N1. As a result, the proposed output stage can achieve higher power efficiency than the conventional output stage design.

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The specifications of the DC-to-DC converter are: 5V supply voltage, 1.2V output voltage and the switching frequency is 1MHz. For easy implementation, a function generator is used to generate the PWM signal.

(a)

(b)

Figure 5.6 Schematics of (a) proposed output stage and (b) conventional output stage

Figure 5.7 presents the operation waveforms at light load condition for both conventional output stage design and proposed output stage design. The waveforms are the output voltage, the gate drive voltage for the upper and the lower side power switches and the input current.

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(a)

(b)

Figure 5.7 Operation waveforms of (a) conventional design and (b) proposed design

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From Figure 5.7, note that the gate drive voltage of the output power switches in the proposed design are reduced compared to that of the conventional design. Hence, the proposed design will have lower switching loss and total power loss at light load condition. Figure 5.8 depicts the power efficiency of the proposed design and the conventional obtained through measurement at light load condition. From Figure 5.8, it can be easily observe that the proposed low voltage swing output stage design has a better power efficiency than that of the conventional output stage. Hence, the results obtained through post-layout simulation and measurement show that the proposed output stage design technique can achieve higher power efficiency.

Figure 5.8 Light load power efficiency measurement

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However, as you can observe from the efficiency measurement result of the hardware implementation, the power efficiency of the hardware design cannot achieve above 70%, which is much lower than that of the schematic simulation and post-layout simulation results presented previously in this chapter. The reason is that the external components in the discrete-component implementation have excessive parasitic components compared to those on chip components, i.e. the parasitic capacitances of the two power switches and their driving circuits are much larger than those of the on chip components. In other words, the power losses in the hardware implementation are much higher than those in the on chip implementation.

5.6 Summary

In this chapter, the power efficiency of three output stage designs namely the proposed design, the segmented design and the conventional design operating in different control modes (i.e. PWM CCM mode, PWM DCM mode and PFM mode) are presented. Note that the proposed design has comparable power efficiency when output load current is less than 10mA and has higher power efficiency as output load current is between 10mA to 50mA. In addition, the proposed design generates a stable and predictable noise when output load current is less than 10mA as opposed to the other two designs which operates in PFM mode. The proposed design has been simulated in Cadence and implemented in discrete components. The results obtained from post-layout simulations and measurements shows that the proposed output stage design can achieve a better power efficiency performance than the other two designs over the entire load current range.

CHAPTER 6 CONCLUSIONS AND FUTURE WORKS

CHAPTER 6

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6.1 Conclusions

An analysis and design of a DC-to-DC buck converter based on low swing voltage and DCM mode has been proposed and presented in the thesis. The theoretical aspect of this thesis pertains to the mathematical analysis of the power dissipation mechanism of the output stage of the buck converter. The practical aspect pertains to the design and implementation of the DC-to-DC converter to achieve a better power efficiency performance over the entire load current range, in particular at light load and extreme light load conditions.

In Chapter 1, the basic operation, power dissipation analysis and design approach of a synchronous buck converter output stage for portable applications (e.g. cellular phone) has been presented. The emphasis of this project is to improve the light load power efficiency of the synchronous buck converter. This is because most of the portable

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devices usually operate in standby mode with very low output load current. By improving the light load efficiency, the life time of the battery, which is critical for most of the portable devices, can effectively be extended.

In Chapter 2, the basic operations of a synchronous buck converter were described. The operations include conduction modes, control techniques and power transistor model. Next, the prior-art designs to improve the light load efficiency were presented. Chapter 3 provided the theoretical power dissipation analysis of the output stage in detail. The analysis also includes the power dissipation of the output stage in different control modes.

In Chapter 4, the proposed low voltage swing output stage design with charge recycling scheme was presented. The basic idea of the proposed design is to reduce the gate drive voltage of the output power switches to lower the switching loss at light load. This is because switching loss is the dominant power loss at light load and the loss is mainly dependent on the switching voltage across the parasitic input capacitance of the power transistors. To reduce the switching voltage, a capacitor is added to the power stage. The capacitor also act as a charge recycling capacitor to store the charge discharged from the input capacitance of the upper power switch and use this charge to drive the lower power switch. In other words, the lower power switch does not consume any switching loss from the power supply in the proposed low voltage swing design. As a result, the switching loss of the proposed output stage at light load can be reduced significantly. The primary drawback of reducing the gate drive voltage of the power switches is the resultant increase in the turn on resistance of the power switches. However, the increase in the turn on resistance is insignificant if the gate drive voltage is at least three times

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higher than the threshold voltage of the power transistors. Moreover, conduction loss is not the dominant power loss at light load condition. Hence, the proposed low voltage swing output stage design with charge recycling scheme can achieve a lower total power loss at light load, thereby improving the power efficiency.

In Chapter 4, the different configurations and control modes that have been adopted in the proposed design to improve the power efficiency of the buck converter at different load conditions were also discussed. First, at extreme light load condition, the PWM DCM mode with skip pulse control and low voltage swing configuration is applied for further reduction of the switching frequency and the power switches' turn on time. Second, the PWM CCM control mode with low voltage swing output stage is adopted for condition between light load and medium load (i.e. 50mA). This is because the conduction loss is increased when output current increases. Finally, when the output current is above medium load level, the PWM CCM control mode with full swing output stage configuration (i.e. conventional design) is applied. This is because at medium load current, the conduction loss has become the dominant power loss at the output stage.

In Chapter 5, the power efficiency performance of the proposed design is compared against that of the segmented output stage design and the conventional design. From the comparison, it is noted that the performance of the proposed low voltage swing output stage design operating in PWM CCM mode is much better than that of the segmented output stage design and the conventional design. The power efficiency improvement has been verified by theoretical calculation, Hspice simulation, post-layout simulation and hardware implementation. A power efficiency comparison has also been done for the

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proposed design operating in lower PWM control mode against the segmented output stage design and the convention design operating in PFM control mode. The comparison shows that the proposed design has a slightly lower efficiency than the segment output stage design at extreme light load condition and has the highest efficiency at light load to medium load condition. By operating in PWM mode, the proposed design has the advantage of having a stable and predictable noise.

In summary, the proposed design is simple and elegant and can be implemented easily in an integrated DC-to-DC converter. By operating in CCM and DCM with pulse skipping mode, the buck converter can provide relatively high efficiency over the entire output load range for portable devices.

6.2 Future Works

When the buck converter output stage operates in DCM mode at the extreme light load condition, high frequency components are generated at the switching node because the internal parasitic capacitance of the power switches and the output inductor form a LC circuit. A more detail study should be carried out to determine the mechanism of the high frequency components generation and the effects of these high frequency components on the buck converter output stage operation. Effective methodologies to suppress the high frequency components should also be developed. This is because in some applications that are very sensitive to noise and these high frequency components may induce unwanted oscillation in the sensitive part of the circuits.

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As mentioned in this thesis, the proposed low voltage swing output stage with charge recycling scheme reduces the gate drive loss and recycles the input capacitance charge of the power switches. However, there are two power losses which also contribute significant loss in the output stage. These two losses are the switching loss of the gate drive circuits of the power switches and the hard switching loss at the switching node of the output stage. Therefore, in order to improve the power efficiency of the output stage further, the future work for output stage should be focused on reducing the gate driver loss and the hard switching loss for both light load and heavy load conditions. This is because the hard switching loss is proportional to the output load current.

At light load condition, the low voltage swing output stage configuration is applied with lower gate drive voltage of the upper and the lower power switches. As a result, the rise and the fall times of the power switches are different from that in the full voltage swing output stage configuration. In other words, the dead time control circuit design will be different for the low voltage swing and full voltage swing output stage configurations. Further study should be carried out to design an adaptive dead time control circuit for low voltage swing output stage configuration to maximize the light load power efficiency.

LIST OF PUBLICATION

LIST OF PUBLICATION

One paper on this project had been published in TENCON 2009 - 2009 IEEE Region 10 Conference in year 2009.

The name of the paper is:

Design of a low swing power-efficient output stage for DC-DC converters

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