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INVESTIGATION OF GOLD NANOPARTICLE BASED ORGANIC MEMORY DEVICES

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School of Materials Science and Engineering

A thesis submitted to the Nanyang Technological University
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Abstract

The implementation of plastic electronic solutions to large area displays, flexible sensors, and memory tags necessitate the development of organic memories that are solution-processable and readily integrated with printed electronics. Organic transistor based memories are amenable to direct integration into existing technologies. In this thesis, we explore organic memories based on gold nanoparticles (AuNPs) which serve as a floating gate allowing the modulation of flat-band voltages in capacitors and threshold voltages in transistors.

The first part of this dissertation proposes an organic memory system, using pentacene as active semiconductor layer and citrate-stabilized AuNPs (citrate-AuNPs) as charge storage elements, in a metal-pentacene-insulator-silicon (MPIS) configuration. The citrate-AuNPs were immobilized onto amine-terminated modified silicon substrate surfaces through electrostatic attraction. Capacitance measurements showed a significant hysteresis of 1.25V to 2.05V achievable under 5V to 10V programming range. The origin of trapping in the citrate-AuNPs was confirmed through frequency-dependent conductance measurements. Fowler-Nordheim tunneling has been found to be the principle conduction mechanism and temperature-dependent studies revealed charge storage activation energy of 13.3 meV. A charge retention ability of 85% over more than 10,000 seconds was also exhibited.

The second part of this dissertation focuses on a polymeric memory that comprises an *in-situ* synthesis strategy of AuNPs in polystyrene-*b*-poly-4-vinylpyridine (PS-*b*-P4VP) copolymer. The memory ability was first demonstrated in a capacitor device where charge carriers can be trapped in the AuNPs upon applied voltage. The ability to tune memory behavior was also illustrated by varying the loading of AuNPs. Hole trapping is observed to be more efficient than electron trapping which is attributed to presence of Schottky barrier between the gold electrode and P4VP. At higher electric fields (>0.4 MV/cm), quasi-two-dimensional tunneling through the arrays of AuNPs is

observed. The contribution of electrode work function was demonstrated with improved electron charging by the replacement of gold electrode with aluminum.

We have also developed organic field-effect transistors (OFETs) incorporating the active memory layer of AuNPs in PS-*b*-P4VP as a floating gate. We have demonstrated both *p*-type (pentacene) and *n*-type (hexadecafluorophthalocyaninatocopper) OFET based memories, which have stable large charge capacity and programmable-erasable properties. To improve minority carrier injection for erasing operations, we have utilized photogenerated carriers for trapping in AuNPs. The memory devices can hence be written and read electrically and erased optically, resulting in large memory windows, high on/off ratio between memory states and long retention times. These devices clearly exhibit the characteristics needed to satisfy the new demands for memory application and indicate the usefulness of utilization of nanoparticle-polymer composite for organic memory device fabrication

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Chapter 1

Introduction

1.1 Overview of Organic Electronics

Organic materials, especially polymers have traditionally been considered as insulating materials and have been long deployed in the field of electrical engineering, for example as an insulating wrapping of cables. It was only in the 1970s that electrically conducting organic materials and semiconducting polymers were investigated. For their efforts in this research area, the Nobel Prize in 2000 for Chemistry was awarded to Alan J. Heeger, Alan G. MacDiarmid and Hideki Shirakawa.^[1] With the deployment of such materials for electronic applications, the word "organic electronics" has entered the vocabulary.

Organic electronics (also called polymer electronics) has experienced wide spread interest over the past decade and research groups in academia and industry have been racing to fabricate optical, electronic, memory, bio-sensing and display devices, which are based not on silicon but on semiconducting polymers. The enormous progress in this field has been driven by the expectation to realize new applications, such as large area, flexible light sources and displays, low-cost printed integrated circuits or plastic solar cells from these materials. Numerous organizations and companies such as Philips, Infineon, Siemens, STMicroelectronics and Thomson are actively pursuing polymer electronics.^[2] Such major collaborations hint at a groundswell of interest in polymer electronics.

1.2 Organic Memories

During the evolution of organic electronics, most of the attention has shown either on organic transistors,^[3, 4] organic light emitting diodes,^[5, 6] or on organic photovoltaic cells.^[7, 8] However, it stands to reason that organic electronics will need memory as much as regular electronics. This memory could be supplied with conventional silicon memory interconnected to organic devices. Alternatively, electronic memory could simply be realised using organic materials. New applications such as flexible sensors, radio-frequency identification tags (RFIDs), large area active-matrix displays, and various smart packaging devices are under development and require high performance organic transistors and memories.^[9-11] The value of products using organic thin-film transistors (OTFTs) and/or organic memories is predicted to exceed \$700 million by 2010 and approach \$5.8 billion by 2012.^[12]

Furthermore, exploration of advanced materials for data storage is critical for future technology especially since silicon technology is running out of steam in terms of scalability. Many novel methods have been reported in inorganic non-volatile memory, such as electrical switching in oxide semiconductors,^[13] phase change memory,^[14] programmable metallization

cell,^[15] quantized atomic switch,^[16] and nanocrystal memory.^[17, 18] Only recently have organic memories been considered as potential candidates due to their simple structure, lower cost, and the prospect of stacking them for packing bits at high densities.

Among the three main streams of semiconductor memory technologies – Static Random Access Memory (SRAM),^[19] Dynamic Random Access Memory (DRAM)^[20] and Flash Memory,^[21] only the Flash memory shows non-volatile characteristics. DRAM shows high density capabilities while SRAM has fast read/write performance. The driving force for novel memories is to be able to combine the benefits of these three types of inorganic memories – non-volatility, fast switching speeds ($\sim 1\mu\text{s}$), low operating voltage ($\sim 5\text{V}$), long retention times (ranging from few seconds for volatile

DRAM alternatives to many years for Flash-like standard), thermally stable up to at least 100 °C and high densities. Organic memories offer the potential to exhibit such desired characteristics. Several different categories of emerging organic memories and major progresses are briefly described in Table 1.1. A more detailed description of each of these memory devices can be found in recent comprehensive review articles.^[22-24]

A popular memory architectural approach has been the cross point arrays^[25-27] where the memory state is determined by switching between low and high conductance. The key to create the memory effect is through charge trap engineering. The trap sites can be created either on nanoparticles,^[24, 28, 29] on redox molecules,^[30, 31] or between interfaces created by donor/acceptor conjugated molecules^[32, 33] or nanoparticle/organic molecules.^[34-36] The trap site either undergoes a charge transfer process, for example, from molecule to nanoparticles or molecule to molecule, or has the ability to store the injected charges. Another alternative memory architecture that can be adopted relies upon a capacitance type response towards organic field effect transistor (OFET) based memory devices.^[37-41] Information is held by charge storage or polarization inside a dielectric layer or in the region between the channel and dielectric, allowing the modulation of the threshold voltage, V_T , of the transistor. The presence or absence of current flow defines a Boolean '1' or '0'. The memory element can be in the form of space charge electrets,^[37-39] ferroelectric polymers,^[42-44] or nanoparticles.^[45, 46] OFET based memory devices are amenable to direct integration into existing technologies since an external driver (transistor) is no longer necessary.

Nanoparticle based memory transistors (akin to present day Flash memories) are especially attractive due to reduced charge loss from defects in the underlying dielectric and capability of multiple bit storage. In general, these nanoparticles can be deposited at room temperature using simple chemical self-assembly,^[47] Langmuir-Blodgett^[48] or spin-coating methods.^[49] The concept of room temperature formation of nanoparticles could find application in future 3-D organic memory architectures,

compatible with the low temperature processable materials like polymers. In addition, its solution processable approach is especially suitable for low-cost large-area processing on flexible substrates, which may be considered to be the cornerstone of organic electronics applications.

Table 1.1: Different categories of emerging organic memories

		Typical Device ^a	Who/When	Mechanism	Advantages	Challenges
Organic Resistive Memory	Small Molecule	Al-tetracene-Al ^[50]	Drexel Institute of Tech (1968)	Charge trapping	Simple device	Volatile
		Al-pentacene-Al ^[51]	CNRS (2004)	Electrode inclusion	Simple device	Reliability issue
	Polymer	Au-PEDOT:PSS-ITO ^[52]	Princeton (2003)	Redox reaction	Solution processable	Not rewritable, Hard to shrink
		Al-MEH-PPV-ITO ^[53]	University of Arizona (2006)	Not disclosed	High ON/OFF ratio in conductance	Response time not disclosed
	Nanoparticle / Nanocomposite	Al-AIDCN/Al/AIDCN-Al ^[28]	UCLA (2002)	Charge trapping	High ON/OFF ratio in conductance	High vacuum process
		Al-PANI :Au nanoparticle-Al ^[36]	UCLA (2005)	Charge transfer	Fast switching time (25ns)	Reproducible only for fresh solutions
Organic Transistor Memory	Donor-acceptor complexes	Al-PVP:C ₆₀ -Al ^[35]	Rutgers University (2006)	Charge transfer	Fast switching time (10ns)	1000s of retention
		Cu-CuTCNQ-Al ^[32]	John Hopkins (1979)	Charge transfer	Easy fabrication	Thermal instability
		Al-TTF:PCBM:PS/Al ^[33]	UCLA (2005)	Charge transfer	Solution processable	Material stability not disclosed
	Ferroelectric polymer	OFET with PVDF-TrFE as gate dielectric ^[44]	Philips (2005)	Polarization	Cheap, Non-volatile	High operating voltage (80V)
	Charged electrets	OFET with PαMS as gate dielectric ^[38]	Cambridge (2006)	Charge storage	Programming speed of 1μs	High operating voltage (100V)
	Floating gate	OFET with self-assembled Au nanoparticles integrated in gate dielectric ^[45]	Louisiana Tech (2006)	Charge storage	Large memory window (~30V)	200s of retention

^a Abbreviations of chemical name: PEDOT, polyethylenedioxythiophene; PSS, polystyrene sulphonic acid; MEH-PPV, poly[2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene]; AIDCN, 2-amino-4,5-imidazoledicarbonitrile; PANI, polyaniline; PVP, poly-vinyl-phenol; C₆₀, fullerene; CuTCNQ, Copper-7,7,8,8-tetracyanoquinodimethane; TTF, tetrathiafulvalene; PCBM, C61-butyric acid methyl ester; PS, polystyrene; PVDF-TrFE, poly(vinylidene fluoride/trifluoroethylene); PαMS, poly(α-methylstyrene).

1.2.1 Challenges in Organic Memories

From Table 1.1, we can see limitations associated with the reported organic memories. For the organic resistive memory, the issues lie in the scalability, reliability and cost. Some recent reports also begin to address the issues of reproducibility in the resistive memory performance. For example, asperities in the bottom electrode such as formation of native oxide at the electrode,^[54] impurities,^[55] residual ions,^[56] and irregularities in the deposition of the top electrode^[57] can all contribute to the observed ‘switching’ events and/or obfuscate the intrinsic properties of the memory system. Another challenge here is to figure out how to wire these crossbars into complex integrated circuitry for large scale logic and memory applications. Also, crossbars are usually prone to cell write/erase disturbs and may require integration of access diode or transistor at each intersection. For transistor memory, the major drawback is the high operational voltage and complexity in fabrication. Their physical limitations could also hinder scalability: difficulty in reducing the thickness of the active dielectric layer without compromising the gate leakage current.^[58]

A critical gap also exists in the establishment of the charge transport and charge storage mechanisms in an organic memory device. The basic picture of charge transfer or trapping has been given but there is very little experimental evidence that proves the proposed switching mechanism or examines the effect of materials’ properties, device structure, and electrode material on the device performance in terms of retention time, switching speed and size of memory window.

1.3 Thesis Objective

The main objective of this research work was to develop novel organic memories and study the properties of the memory element. The approach that our research has taken is suitable for devices which rely upon a capacitance type response or towards organic thin film transistor (OTFT) based memory devices. The active memory layer serves as

a dielectric for capacitors/OTFTs. The memory effect would then be reflected as a shift of flat-band voltages in capacitors and threshold voltages in transistors (akin to present day flash memories). In particular, this study focused on investigating the feasibility of tailoring gold (Au) nanoparticles as charge storage components. The following initiatives were undertaken to that extent:

1. Design and characterization of memory storage elements. Two approaches for memory storage elements are explored. They are through the use of (i) citrate-stabilized Au nanoparticles deposited on 3-aminopropyl-triethoxysilane (APTES) modified substrate surface through electrostatic attraction and (ii) *in-situ* synthesized Au nanoparticles self-assembled within a polystyrene-*b*-poly-4-vinylpyridine (PS-*b*-P4VP) diblock copolymer template.

2. Study and establish the operation mechanism by describing and clarifying the charge transport and charge storage mechanisms in these organic memory devices. Physical models for the above memories are developed.

3. Realize organic thin film transistors (OTFT) based memory device by incorporating the above memory elements in the gate dielectric layer with the intent of studying the interaction of the organic semiconductor channel with the trapped charge carriers.

1.4 Thesis Outline

This thesis is focused on the design, fabrication and characterization of organic non-volatile memory devices. Chapter 2 introduces the reader to the underlying theories of conduction in organic semiconductor, dielectrics and charge trapping effects in them. Special emphasis is placed on mechanisms of charge injection from metallic contacts into organic semiconductors and dielectrics. A summary of memory effects based on charge storage model is theoretically discussed for floating-gate type memory device

and various concepts relating to memory characterization techniques such as capacitance and conductance spectroscopy are also given in this chapter.

The rest of this thesis is divided into two main parts: Part I, consisting of Chapter 3, reports an organic memory device using pentacene as the active semiconductor layer and citrate-stabilized gold (Au) nanoparticles as charge storage elements. The Au nanoparticles are immobilized onto amine-terminated modified silicon substrate surfaces through electrostatic attraction. The fabrication processes and various characterization techniques to investigate the optical or structural properties of the active charge storage layer are presented. The charging effect in this novel memory system (capacitor and transistor-based) is also demonstrated in Chapter 3. The influence of organic ligands surrounding the Au nanoparticles on charging ability is also examined and discussed.

Part II of the thesis describes a block copolymer approach for memory applications. Chapter 4 reports the *in-situ* synthesis of Au nanoparticles in self-assembled block copolymer of polystyrene-*b*-poly-4-vinylpyridine (PS-*b*-P4VP) and the characteristic results. The memory effect of these discrete nanoparticles arrays self-assembled within PS-*b*-P4VP diblock copolymer template is also evinced in Chapter 4. The charge transport mechanism is proposed to explain the current-voltage characteristics and memory behavior. The influence of electrode material on memory performance is examined and discussed. This chapter also documents analysis of the memory structure using impedance spectroscopy to elucidate the dynamics of injected and stored charge.

Chapter 5 extends the memory element of block copolymer approach into the gate dielectric layer of an organic transistor. Both *p*-type (pentacene) and *n*-type (hexadecafluorophthalocyaninatocopper) transistor based memories have been demonstrated. Relevant trapping effects are described and discussed. Through the studies of light illumination on the organic memory transistor, the role of organic semiconductor layer on charging/discharging process in Au nanoparticles is clarified. Finally, Chapter 6 summarizes and concludes the dissertation and presents recommendation for future work.

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Chapter 2

Introduction to non-volatile organic memory devices

This review chapter focuses on the principles and materials for organic thin-film memory devices. First, device structures and performance in state-of-the-art organic memories are introduced. Then, discussion is directed to organic field-effect transistor based memories which employs nanoparticles as charge storage components. Basic aspects of charge conduction mechanisms in organic semiconductor and dielectrics are also described. Special emphasis is placed on mechanisms of charge injection from metallic contacts into organic films. Finally, various concepts relating to memory characterization techniques such as admittance spectroscopy and transient capacitance spectroscopy are outlined.

2.1 Current memory technology

Memory devices can program (write), store, retain and recall information. Depending on the storage capability, memory devices are divided into two categories: volatile and nonvolatile. Volatile memory loses information while nonvolatile memory retains its information, when the external power is turned off.

Nonvolatile memory can be roughly classified by the methods of erasing: EPROM (Electrically Programmable Read Only Memory) and EEPROM (Electrically Erasable Programmable ROM). Both the EPROM and EEPROM have to erase the previous information before writing in new data, and the later can be erased electrically providing the convenience of in-circuit alterability while the former can only be erased using UV light.^[1] In either case, a stacked-gate Metal-Oxide-Semiconductor (MOS)

structure, having a floating gate^[2] between the gate (called a control gate in this case) and the substrate, is most commonly used as a memory cell (Figure 2.1). Writing information is done by making electrons injected from the silicon across the gate-dielectric film and stored in the floating gate by applying a bias to the drain and the control gate [Figure 2.2(a)]. The stored electrons in the floating gate will increase the threshold voltage, V_T , of the transistor. These electrons can be released by applying a voltage to the source while keeping the control gate grounded [Figure 2.2(b)]. The V_T of the device is lowered when the charge is released. The state of the device can be read by detecting the source-drain current while applying a voltage between the high and low V_T to the control gate. Once programmed, a cell can retain its charge since the floating gate is surrounded completely by insulating films (usually SiO_2) whose interfacial energy barrier is too high (>3 eV) for the stored electrons to surmount.

Figure 2.1: Device structure of a flash memory cell.

Figure 2.2: Operation mechanism of a flash memory. (a) Hot electron injection from channel into the floating gate and (b) erasure process: stored electrons are released through a tunneling process from floating gate into source.

2.2 Introduction to organic memory devices

As described in *Chapter 1*, each emerging memory device provides its unique advantages and challenges. For the “next” memory device to be considered as a silver bullet solution, it would need to possess the following attributes: 1) fast access time, 2) non-volatility, 3) infinite read/write cycles, 4) low power, and 5) wide operating temperature range. From a manufacturing perspective, additional attributes are also required such as 6) scalability, 7) low cost, 8) manufacturability and 9) integration ability with the silicon platform.

This section provides a taste of the current state-of-the-art organic memories and presents the ever-increasing material options, processes and mechanisms. The primary focus is on organic bistable devices (based on conductance switching) and on OFETs with controlled threshold voltage shifts. The device structure, memory characteristics and operations in these memory devices have also been summarized in Appendix B.

2.2.1 Conductance switching approach in organic bistable devices

2.2.1.1 Working principle

Figure 2.3: Cross point memory architecture.

The most common approach in organic memory devices has been the bistable conductance switch device. The device generally has a metal/organic film/metal structure (see Figure 2.3).

The memory device utilizes electrical bistability of the organic thin film. Electrical bistability means that the device is stable in two electrical states. Figure 2.4 illustrates an example of the current-voltage characteristic of this kind of devices. The original device first exhibits a low conductance (or high resistance) state; therefore very little current flows through it. It then transits to a state of high conductivity (low resistance) when the external electric voltage is higher than the threshold voltage. The device at the high conductivity state can return to the low conductivity state by applying a voltage of negative polarity. The device in these states could be different in conductivity by several orders of magnitude. The different conductance states define the written (ON state, “1”) and erase (OFF state, “0”) state of the memory device.

Figure 2.4: Current-voltage characteristics of an organic bistable device with the structure Al/AIDCN/Al/AIDCN/Al.^[3]

The electrical bistability is attributed to the effect of an external electric field on the interaction between the materials in the active layer. Under a high electric field, an electric field-induced charge transfer can occur between molecule to molecule or molecule to nanoparticles. Conjugated organic materials can be oxidized by losing an electron or reduced by gaining an electron. These conjugated organic materials exhibit higher conductivity after oxidation or reduction.^[4, 5] With addition of metal nanoparticles, interesting property of storage of charge has been observed. When a

metal nanoparticle is near a conjugated organic compound, charge transfer may take place between them when the external electric field is high enough. After the charge transfer, the charge is stored in the metal nanoparticle and remained stable due to the insulator coating layer surrounding the nanoparticle. The conductivity of the organic compound increases as it loses its charge to the metal nanoparticle. In this way, the device switches from a low conductivity state to a high conductivity state. The following section highlights the various combination of materials reported.

2.2.1.2 Categories of organic bistable devices

There are four main approaches in the material systems based on these devices:

1. Small molecule

The first organic material exhibiting a bistable memory effect can be traced back to 1969 by Szymanski *et al.*^[6] who used tetracene molecules sandwiched between gold and aluminum electrodes. The bistable phenomenon was explained in terms of charge trapping in the amorphous tetracene film. After that, several acene derivatives including naphthalene^[7] and anthracene^[8] have been reported. Redox molecules such as catenane,^[9] rotaxane^[10, 11] and ferrocene derivatives^[12, 13] have showed unique conformational changes accompanied by redox reactions controlled by external biases. However, control experiments have suggested that the memory effect is more likely due to nanofilamentary^[14] metal switching mechanisms rather than molecular electronic behavior.

2. Polymer

In 2003, Forrest *et al.* discovered a write-once-read-many-times memory using a commercially available polymer PEDOT:PSS (Baytron P).^[15] Sandwich between ITO and gold electrodes, the thin polymer film can be permanently switched off – going from conducting to insulating when enough current is put through it. Conductance switching in poly[2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene] (MEH-

PPV)^[16] with good retention times of several weeks was demonstrated but the nature of the switching was not well understood.

3. Nanoparticle/ nanocomposite

Hybrid organic-inorganic systems have been extensively investigated, especially metallic nanoparticles embedded in an organic host. Such nanoparticle based system was pioneered by University of California, Los Angeles (UCLA)^[3, 17] and IBM's Almaden Research Center,^[18] where the device has an architecture of a triple layer configuration (organic/metal nanocluster/organic) sandwiched between two metal electrodes. This is based on two semiconducting or insulating organic layers and a middle discontinuous metal layer. The organic layers that have been reported are molecules such as 2-amino-4,5-imidazoledicarbonitrile (AIDCN), Tetrathiafulvalene (TTF), [6,6]-phenyl C₆₁-butyric acid methyl ester (PCBM), N⁴,N^{4'}-Dinaphthalene-1-yl-N⁴,N^{4'}-diphenylbiphenyl-4,4'-diamine (NPB) and Aluminum tris (8-hydroxyquinoline) (Alq₃). The operating mechanism is believed to be due to the charge storage at the middle metal nanocluster (usually Al or Au) layer, which subsequently induces charge at the organic layers. The major drawback of these triple-layer devices is that the need for fabrication through thermal evaporation in high vacuum and/or stringent morphology control of the middle, discontinuous metal layer.

Figure 2.5: Schematic charge transfer between Au nanoparticle and (a) 8-HQ,^[19] (b) conducting polymer of PANI^[20] induced by an electric field.

The UCLA group accelerates the research in organic memories further by blending synthesized nanoparticles and/or conjugated molecules in a polymeric matrix. They observed electronic bistability in a polymer film containing both gold (Au)

nanoparticles capped with alkanethiol and a small organic conjugated compound called 8-hydroxyquinoline (8HQ).^[19] The operating mechanism is attributed to an electric-field-induced charge transfer between the Au nanoparticles and the surrounding conjugated compounds [Figure 2.5(a)]. A write-once-read-many-times memory was also reported where the active layer is a polystyrene film containing 2-naphthalenethiol capped gold nanoparticles.^[21] Another memory system which has aroused much interest is polyaniline (PANI) decorated with Au nanoparticles [Figure 2.5(b)].^[20] After the charge transfer, the trapped charges are stable due to the barrier or bridge molecule. The simple synthesis process, fast switching response (< 25 ns) and good retention time of 10,000 seconds marks a decisive step towards making organic memory technology fit for technological purposes. There have also been many groups utilizing conjugated polymers as hosts, namely, poly(3-hexylthiophene) containing Au-dedecanethiol^[22] and poly(N-vinylcarbazole) embedded with Au nanoparticles.^[23] Nanomaterials incorporating carbon nanotubes,^[24, 25] and nonmetallic particles have also been blended into organics, including wide-bandgap inorganic oxides (ZnO) in polystyrene,^[26] copper phthalocyanine in Alq₃,^[27] CdS in MEH-PPV^[28] and C₆₀ inside poly-vinyl-phenol.^[29]

4. Donor-acceptor complexes

Combinations of electron donors and acceptors, motivated by the conductive properties of organic charge-transfer complexes, have also been explored as potential storage media. In particular, TCNQ (7,7,8,8-tetracyanoquinodimethane) and various metals to form charge-transfer complex.^[30, 31] The metals act as electron-rich donors and can be Li, Na, K, Ag, Cu or Fe. Other donor-acceptor complexes, where both components are organic, are also numerous in the literature. For example, the acceptor and donor molecules are simply mixed,^[32-34] while in some cases, the molecules are blended in a common host polymer.^[35] In other cases, the donor-acceptor species are coupled into one molecule^[36] or onto the backbone of a copolymer.^[37] In all of these systems, the assumption is frequently that charge transfer to conductive state is driven by an electric field. But there is very little experimental evidence that has prove the proposed switching mechanism.

2.2.2 Threshold voltage shift approach in an organic field-effect transistor

Besides the widely used two-terminal bistable organic memory devices, another alternative memory architecture that can be adopted relies upon a capacitance type response towards organic field effect transistor (OFET) based memory devices. This section introduces the concept of OFET, the memory operation and the current state of art.

2.2.2.1 Working principle of an organic field-effect transistor

The organic transistor inherits its design features from its inorganic counterpart, Metal Insulator Semiconductor Field Effect Transistor (MISFET). It is composed of: (i) source (S), drain (D) and gate (G) electrodes, (ii) a dielectric layer, and (iii) an active semiconductor layer, as illustrated in Figure 2.6(a). The basic idea of a field effect transistor is to modulate the current that flows between two ohmic contacts (source and drain electrodes) by applying a voltage to a third contact (the gate electrode). The semiconductor film and the gate electrode are capacitively coupled such that the application of a bias on the gate induces charge in the semiconductor film. The inorganic MISFETs normally operate in the inversion mode where the electric field applied at the gate electrode is enough to induce minority carriers at the semiconductor-dielectric interface. In the case of organic materials with the low density of charge carriers, the preferred regime of operation is in the accumulation mode.

For a transistor based on a *p*-type semiconductor, the accumulation regime is induced on the application of a sufficiently high negative gate voltage. The application of a negative bias causes the conduction band and valence band levels to shift up such that the valence becomes resonant with the Fermi energy level of the contact. This allows the injection of holes from the contacts. The injected holes can then move under the application of an applied drain electric field. In the case of an *n*-type transistor, the application of a positive gate voltage results in the valence and conduction levels

shifting down so that the conduction levels align with the Fermi level of the electrode, allowing injection of electrons into the semiconductor.

The current flowing through the organic channel from source to the drain, I_D , is described by the same equations that apply to conventional silicon FETs^[38]:

$$I_D = \frac{W}{L} \mu C_i (V_G - V_T) V_D \quad (\text{in the linear region}) \quad (2.1)$$

and

$$I_{D,Sat} = \frac{W}{2L} \mu C_i (V_G - V_T)^2 \quad (\text{in saturation region}) \quad (2.2)$$

Here W and L are the width and length of the accumulation channel respectively and C_i the capacitance per unit area of the gate insulation. The threshold voltage, V_T , corresponds to the onset of strong accumulation and will include contributions from differences in work function between the gate electrode and the semiconductor as well as charges trapped in the bulk insulator and at the interface with the semiconductor.

Figure 2.6: OFET configurations: (a) top contact and (b) bottom contact, with different dielectric layers (c) floating gate or nanoparticle OFET, (d) charge trapping or charge electrets OFET and (e) ferroelectric OFET, for exhibiting memory effects. The separation between the source and drain electrodes defines the channel length (L) and the width of the electrodes defines the channel width (W).^[39]

2.2.2.2 Basic operation in OFET memory

As described in above section, an OFET is volatile, which means that once the gate voltage is removed, the accumulated charges are depleted and the transistor returns to the OFF state. In an OFET floating-gate memory device, an additional voltage, via charge storage or polarization is introduced between the gate and the semiconductor channel to alter the charge distribution in the transistor (see Figure 2.6). This phenomenon results in a shift of threshold voltage, V_T , or hysteresis in the transfer curve (I_D - V_G). Figure 2.7 shows an example of the memory operations.

In particular, the working principle of an OFET nanoparticle based memory device is very similar to that of the traditional flash memory described in Section 1.1, or nanocrystal memory,^[40] with a threshold voltage that is given by:

$$V_T = K - Q_{FG}/C_{CG} \quad (2.3)$$

where K is a constant that depends on the gate and substrate material, as well as the gate dielectric thickness, Q_{FG} is the charge in the Floating Gate and C_{CG} is the capacitance between Control Gate and Floating Gate.

Figure 2.7: An example of the shift in transfer characteristics for an OFET memory device.^[41]

The threshold voltage can be altered by changing the amount of charge present in the floating gate. Thus, by storing/removing charge in/from the floating gate, the threshold

voltage can be changed repetitively from a high to low state (“programmed” and “erased” states, respectively). The “read” operation is performed by applying a gate voltage that is between the values of the erased and programmed threshold voltages and sensing the current flowing through the device. The main difference of an OFET based memories with conventional nanocrystal memories lies in the low mobility of organic semiconductor materials. Assuming an average mobility (μ) of $0.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, the velocity (v) of carriers in an OFET should be four orders of magnitude smaller than that in a silicon-based transistor (from $v=\mu E$). As a result, there are few hot electrons or holes in the channel to be injected into the floating gate of an OFET. Hence, the read/write mechanisms of an OFET memory should be basically tunneling.

2.2.2.3 Types of OFET memory

On the basis of charge storage and polarization methods in the dielectric layer or interfaces, OFET memories can be divided into three categories: (1) Ferroelectric, (2) charge electrets and (3) nanoparticle based OFET memories.

1. Ferroelectric polymer

Most of the organic field effect transistor (OFET) memory reported so far is based on ferroelectric behavior of the gate dielectric.^[42-44] Notably poly(vinylidene difluoride) (PVDF)

and its copolymer trifluoroethylene (TrFE). The ferroelectric polarization is inherently bistable, directed towards either electrode, and may be reversed by application of a sufficiently high voltage of the appropriate polarity.

2. Charge electrets

This is similar to floating gate but the charges are trapped locally on a thin layer of chargeable polymer inserted between the dielectric and organic semiconductor layer, rather than on an isolated floating gate. Memory based on charge electrets has been investigated before,^[45, 46] but Baeg *et al.*^[41] are the first to report a million times improvement in the programming speeds (around 1 microsecond). But the operating

voltage of the device is 100V which is not practical; further optimization of the device performance is thus needed.

3. Nanoparticle

Another type of memory element is the utilization of nanoparticles as charge storage components. Such devices are analogous to inorganic memory devices where charge storing nanoparticles (such as Si or Ge) are incorporated into an insulating matrix (such as SiO₂). In 2004, a hybrid non-volatile gold nanoparticle floating-gate memory metal insulator semiconductor field effect transistor (MISFET) device combining silicon technology and organic thin film deposition, has been fabricated.^[47] The gold nanoparticles are deposited by chemical processes at room temperature, where charge injection/rejection into the nanoparticles takes place by applying different voltage pulses (less than 6 V) to the gate electrode, resulting in significant threshold-voltage shift (Figure 2.8). From these pioneering works, Liu *et al.*^[48] produced an organic transistor memory with gold nanoparticles in the gate dielectric. The gold nanoparticles were deposited on the substrate using electrostatic layer- by-layer self-assembly method. The device fabrication process is shown schematically in Figure 2.9. The gold nanoparticles were charged or discharged with different gate bias so that the channel conductance is modulated. The memory transistor has a retention ability of 200 seconds. The short retention time has been attributed to the poor insulating property of the poly (4-vinyl phenol) (PVP) barrier layer surrounding the gold nanoparticles.

Figure 2.8: Schematic of the hybrid memory device. S and D are the source and drain contacts, C the channel area. The memory stack is made of a 5 nm SiO₂ (bottom, numbered by 1), gold nanoparticle layer in the middle (2) and organic insulator on top (3).^[47]

Figure 2.9: Schematic illustration of the fabrication process of a nano floating gate OFET for non-volatile memory applications.^[48]

2.3 Basic aspects of charge injection and transport in organic memory devices

There are two basic processes that control the charge transport in an organic film (insulating or semiconducting): (1) injection of charge carriers from electrodes into the organic layer; and (2) transport of charge carriers in the bulk of the film. The occurrence of injection limitation is due to a mismatch of energy levels between the electrode work function and the corresponding transport levels of the organic material. Bulk transport limitation, by contrast, depends on intrinsic mobility of the bulk or presence of charge trapping sites. Hence controlling the conditions and surface states in metal/organic contacts is one of the key issues required to understand conduction mechanism and device characteristics. In this section, we will briefly give an overview on some basic concepts for the description of these processes.

2.3.1 Band structure

Organic materials for use in electronic and optoelectronic devices are often called organic semiconductors, which play the role of charge carrier transport as well as

charge carrier generation or injection. They are basically aggregates of carbon-based small molecules or polymers with typical energy gaps ranging from about 1.5 eV to 3.5 eV. The electronic states of organic molecules are derived from p -orbitals of carbon atoms through sp^2 - p hybridization. In a sp^2 hybridized orbital, there are three σ -bond with high bonding energies. The electrons in the σ -bond are called σ -electrons, which are localized. The remaining p -orbitals form relatively weak π -bonds with much lower bonding energies. The electrons in the π -bonds, namely, π -electrons, are loosely bound and delocalize inside the molecule. The

highest π -bonding orbital that is occupied by electrons is called highest occupied molecular orbital (HOMO), while the lowest π -antibonding orbital that is unoccupied by electrons is called the lowest unoccupied molecular orbital (LUMO).^[49] The HOMO and LUMO are, in some sense, analogous to the valence band and conduction band of an inorganic semiconductor. For organic semiconductors with high purity, the amount of free charge carriers present in the materials is usually negligible and the materials typically show relatively low conductivities. Thus, organic semiconductors can be considered to be insulators and theories of carrier conduction or injections across metal/inorganic dielectric interfaces have been applied to metal/organic semiconductor interfaces.

The energy band diagrams presented in this chapter with forbidden gap separating the conductance and valence band has been shown with well-defined boundaries. Strictly speaking, a well-defined energy gap is a property of a crystalline solid [Figure 2.10(a)] and in general, we are not dealing with such materials; rather we are concerned with polycrystalline or amorphous insulators. However, Mott 1967^[50] has shown that the essential features of the band structure of a solid are determined by the short-range order within the solid; thus the general properties of the band structure of the crystalline state are carried over to the polycrystalline state. The lack of the long-range order in a non-crystalline solid is to cause smearing of the conduction and valence band edges. Because the band edges are diffused, there is a gradual transition from quasi-continuous states (conduction and valence bands), in which carriers can move

freely, to strictly localized states (density-of-states-tail) or traps in which the carriers are immobilized [Figure 2.10(b)].

Figure 2.10: Energy levels in a (a) nearly perfect molecular crystal, with well-defined conduction band (E_C) and valence band (E_V), containing a small amount of guest molecules forming electron (E_{te}) and hole (E_{th}) traps, (b) disordered solid built of the same molecules. The energy of a quasi-discrete electron transport level is E_C , the energy of the hole transport level is E_V . In the disordered solid, the quasi-discrete levels are split into Gaussian distribution of local states. The local states due to the chemical impurity may either form traps (hole traps) or broaden the distribution of the local states (electron states).

2.3.2 Potential barriers at metal–organic interfaces

From conventional semiconductor electronics, it is known that creating a low resistance ohmic contact requires alignment of the metal Fermi level (E_F) with the energy levels (bands) of the semiconductor. Figure 2.11 shows a simple diagram depicting energy level alignments at a metal-organic semiconductor junction. This diagram assumes that the Mott-Schottky^[38, 51, 52] rule holds: namely, that the vacuum levels of the metal and organic semiconductor are in registry. The outcome of this assumption is that one can easily estimate the conduction band (LUMO) and valence band (HOMO) offsets from the Fermi level. For example, the valence band offset, $E_F - E_V$, is the difference between the work function of the metal (ϕ_m) and ionization potential (IP) of the organic semiconductor, or $E_F - E_V = \phi_m - \text{IP}$. This offset is in turn a good estimate of the potential barrier to hole injection from the metal to the semiconductor.

There are four distinctly different mechanisms for injection of carriers across a metal-organics junction. They are ohmic injection, thermionic emission, Fowler-Nordheim tunneling injection and defect-assisted tunneling injection. In a given junction, a combination of all four mechanisms could exist. However, typically one finds that only one current mechanism dominates.

Figure 2.11: Simple band line-up diagram for a metal-organic semiconductor interface assuming that the Mott-Schottky rule holds and that the vacuum levels for the metal and semiconductor are aligned.

2.3.2.1 Ohmic injection

An ohmic contact is defined as having a negligible contact resistance relative to the bulk or spreading resistance of the semiconductor. In order to achieve an ohmic contact at a metal-semiconductor interface, the electrode work function must be smaller than the semiconductor work function. Under this conduction, in order to satisfy the thermal equilibrium requirements, electrons are injected from the electrode into the conduction band of the semiconductor. This type of contact acts as a reservoir of charge which is capable of supplying electrons to the semiconductor as required by bias conditions. Thus, with contacts of this type, the conduction process is limited by the rate at which the electrons can flow through the bulk of semiconductor, rather than the rate at which they are supplied by the electrode.

2.3.2.2 Thermionic emission

In the thermionic injection model, only energetic carriers which have energy equal to or large than the conduction/valence band energy at the metal-semiconductor interface, contribute to the current flow. For example in Figure 2.12(a), applying a negative bias to the metal relative to the semiconductor can result in electron injection into the conduction band if the electrons can surmount the barrier $E_C - E_F$.

An image force potential can be formed due to Coulomb attraction between the electrons injected and the holes left behind in the metal after electron injection.^[53] This so called image force will effectively accelerate negative charge injection and lead to the modification of the resulting potential profile near the interface. Hence, the thermally excited carriers from the electrodes have to overcome the potential maximum resulting from the superposition of the image charge potential and external field. Figure 2.12(b) depicts the energy diagram of the injection barrier lowering due to the image force. The potential barrier height ϕ is reduced with an amount V_m and moves the maximum away from the interface:

$$V_m = \frac{1}{2} \cdot q \cdot \sqrt{(qE / \pi \epsilon \epsilon_0)} \quad (2.4)$$

where ϵ is the relative dielectric permittivity, ϵ_0 is permittivity of free space, E is the external electric field and q is the elementary charge. Such field-assisted lowering of the barrier height results in a field dependent thermionic injection current which follows the Richardson-Schottky equation.^[38, 54]

$$J_{th} = A^* \cdot T^2 \cdot \exp\left(-\frac{\Phi_B - V_m(E)}{k_B T}\right) \quad (2.5)$$

$$J_{th} = A^* \cdot T^2 \cdot \exp \left[-\frac{q(\Phi_B - \sqrt{qE/4\pi\epsilon\epsilon_0})}{k_B T} \right] \quad (2.6)$$

with the Richardson constant $A^* = 4\pi q m^* k_B^2 / h^3$, T is absolute temperature, and the zero-field injection barrier height Φ_B . (k_B : Boltzmann's constant, h : Planck's constant, m^* is the effective mass of charge carrier).

Figure 2.12: Energy diagram of Schottky barrier (a) without and (b) with the presence of electrostatic image potential at a metal-organic interface.

2.3.2.3 Tunneling injection

When the applied electric field is high, quantum tunneling of carriers can occur through a triangular potential barrier into continuum states (Figure 2.13). This process is called Fowler-Nordheim (FN) tunneling injection model.^[55] Ignoring the contribution of the image force, the calculation of the current is based on the Wentzel-Kramers-Brillouin (WKB) approximation yielding the following relation, between the current density, J_{FN} , and the electric field in the insulator, E :

$$J_{FN} = \frac{q^3}{8\pi\hbar\phi_B} \cdot E^2 \cdot \exp\left(-\frac{4\sqrt{2m^*\phi_B^3}}{3q\hbar E}\right) \quad (2.7)$$

where ϕ_B is the barrier height at the metal/organic interface, m^* is the effective mass of carriers, q is the elementary charge, $\hbar$: reduced Planck's constant ($= h/2\pi$), and E is the external electric field. To check for this current mechanism, experimental I - V characteristics are typically plotted as $\ln(J_{FN}/E^2)$ versus $1/E$, a so-called Fowler-Nordheim plot. Provided the effective mass of electrons is known, one can then fit the experimental data to a straight line yielding a value for the barrier height under the valid E field.

Figure 2.13: Energy band diagram of field emission (tunneling) injection at a metal-organic contact.

2.3.2.4 Defect-assisted tunneling injection

If the organic layer contains a high concentration of impurities that is able to create new transport sites between the LUMO and HOMO levels of the organic material, the tunneling may occur from the metal to empty localized states in the organic layer by a hopping-type process.^[56, 57]

Figure 2.14: Energy band diagram of defect-assisted injection at a metal-organic contact.

2.3.3 Charge transport processes in organic films

Table 2.1 summarizes the basic conduction processes in organic semiconductor and insulator films which are namely, Schottky emission, Tunnel emission, Poole-Frenkel emission, space charge effects, ohmic conduction as well as ionic conduction. For a given insulator, each conduction process may dominate in certain temperature and voltage ranges. The processes are also not exactly independent of one another and should be carefully examined.

2.3.3.1 Schottky emission

The Schottky emission process is similar to the process discussed in previous section, where thermionic emissions across the metal/insulator or insulator/semiconductor interfaces are responsible for carrier transport. A plot of $\ln(J/T^2)$ versus $1/T$ in which J is current density and T is temperature, yields a straight line with a slope determined by the permittivity ϵ_i of the insulator.

2.3.3.2 Tunnel emission

The tunnel emission is caused by field ionization of trapped electrons into the conduction band or by electrons tunneling from the metal Fermi energy into the

insulator conductance band. The tunneling emission has the strongest dependence on the applied voltage but is essentially independent of the temperature. Thus, the tunneling emission is usually separated into two processes: (1) direct tunneling (tunneling through a square barrier) at relatively low voltage region^[38] and (2) Fowler-Nordheim tunneling (tunneling through a triangular barrier) at relatively high voltage region.^[55]

Table 2.1: List of voltage and temperature dependence of the typical conduction models commonly applied to insulators.

Conduction Mechanism	Characteristics Behavior^a	Voltage Dependence	Temperature Dependence
Ohmic conduction	$J_{ohm} \propto \frac{V}{d}$	$J \propto V$	None
Direct Tunneling (low bias)	$J_{DT} \propto V \cdot \exp\left[\frac{-2d\sqrt{2m^*\phi_B}}{\hbar}\right]$	$J \propto V$	None
Fowler-Nordheim tunneling	$J_{FN} \propto V^2 \cdot \exp\left(-\frac{4d\sqrt{2m^*\phi_B^3}}{3q\hbar V}\right)$	$\ln\left(\frac{J}{V^2}\right) \propto \frac{-1}{V}$	None
Schottky emission (SE)	$J_{SE} \propto T^2 \cdot \exp\left[-\frac{q(\Phi_B - \sqrt{qV/4\pi\epsilon\epsilon_0})}{k_B T}\right]$	$\ln(J) \propto V^{1/2}$	$\ln\left(\frac{J}{T^2}\right) \propto \frac{-1}{T}$
Poole-Frenkel (PF) emission	$J_{PF} \propto V \exp\left[-\frac{q}{kT}\left(\phi_{PF} - \sqrt{\frac{qV}{\pi\epsilon\epsilon_0}}\right)\right]$	$\ln\left(\frac{J}{V}\right) \propto V^{1/2}$	$\ln\left(\frac{J}{V}\right) \propto \frac{-1}{T}$
Hopping conduction	$J_H \propto V \cdot \exp\left(-\frac{\phi}{k_B T}\right)$	$J \propto V$	$\ln\left(\frac{J}{V}\right) \propto \frac{-1}{T}$
Space-charge limited	$J_{SCL} \propto \left(\frac{\epsilon\epsilon_0\mu V^2}{L^3}\right)$	$J \propto V^2$	None
Ionic conduction	$J_{ion} = \frac{V}{dT} \exp\left(\frac{-\Delta E_{ai}}{k_B T}\right)$	$J \propto V$	$\ln(JT) \sim \frac{1}{T}$

^a ϕ_B = barrier height, ϵ_i = insulator dynamic permittivity, k_B = Boltzmann's constant, $\hbar$ = reduced Plank's ($= \hbar/2\pi$), m^* = effective mass, d = insulator thickness, μ = charge carrier mobility, ΔE_{ae} = activation energy of electron, ΔE_{ai} = activation energy of ions.

2.3.3.3 Hopping conduction

The process by which an electron may move from one site to the other can be by thermal excitation over a potential barrier, by tunneling through it, or a combination of the two. Hopping conduction corresponds to the intermediate situation whereby a trapped electron is brought by thermal activation to a level which has the same energy as that of an empty site, which it then moves to by tunneling.^[58] The conductivity is obtained as:

$$J = A \exp\left(-\frac{B}{T^n}\right) \quad (2.8)$$

where A, B are constants and $0.25 < n < 0.5$.

2.3.3.4 Poole-Frenkel emission

The expression for Fowler-Nordheim tunneling implies that carriers are injected into the conduction band of the insulator and free to move through the insulator. However, in deposited insulators, which contain a high density of structural defects, this is not the case. The structural defects cause additional energy states close to the band edges and restrict the current flow by capture and emission processes, thereby becoming the dominant Poole-Frenkel (PF) emission mechanism. The Poole-Frenkel effect is the lowering of a Coulombic potential barrier when it interacts with an electric field, and is usually associated with the lowering of a trap barrier in the bulk of an insulator,^[59] as shown in Figure 2.15. This process is the bulk analogue of the Schottky effect at an interfacial barrier. The barrier height, however, is the depth of the trap potential wall, and the quantity $\sqrt{q/\pi\epsilon\epsilon_0}$ is larger than in the case of Schottky emission by a factor of 2, since the barrier lowering is twice as large due to the immobility of the positive charge. The current is described by:

$$J_{PF} = BE \exp \left[-\frac{q}{kT} \left(\phi_{PF} - \sqrt{\frac{qE}{\pi \epsilon \epsilon_0}} \right) \right] \quad (2.9)$$

where B is a constant and ϕ_{PF} is the depth of a trapped level.

Figure 2.15: Mechanism of Pool-Frenkel effect. The solid line represents the potential energy as a function of distance (r) without an electric field. The dash line shows the effect of the electric field on the potential energy, which results in lowering the Coulombic barrier. The slope of the dash-dot line is proportional to the applied field.

2.3.3.5 Space-charge effects

Both Fowler-Nordheim tunneling and Poole-Frenkel emission mechanisms yield low current densities with correspondingly low carrier densities. For structures where carriers can readily enter the insulator and freely flow through the insulator one finds that the resulting current and carrier densities are much higher. The high density of free carriers can lead to charge accumulations in the film and causes a field gradient, which limits the current density. This charge build-up partially screens out the applied electric field, leading to its redistribution. When the external field is high, the injected current density is higher than intrinsic charge density near the electrode/organic interface. Thus, the internal electric field is enhanced by the space charges and the current is governed by the Space-Charge-Limited current (SCLC).

The theory of SCLC was first given by Mott and Gurney^[60] and has been extended by several authors including Lampert.^[61] For a trap-free insulator, the J - V characteristic is given by the Mott-Gurney Law:

$$J_{SCL} = \frac{9}{8} \left(\frac{\varepsilon \varepsilon_0 \mu V^2}{L^3} \right) \quad (2.10)$$

where μ is the free carrier mobility, ε is the relative dielectric constant, ε_0 is permittivity of free space and L is the thickness of the organic film. The current is assumed to be due to carriers of one sign only, the effect of diffusion is neglected and the mobility is assumed to be independent of the field.

In the presence of a single shallow trapping level, the above equation is replaced by:

$$J_{SCL} = \frac{9}{8} \left(\frac{\theta \varepsilon \varepsilon_0 \mu V^2}{L^3} \right) \quad (2.11)$$

where θ is the ratio of the free electron density and the density of the filled trapping sites.

Lampert and Mark^[62] has pointed out that if sufficient charge is injected into the insulator, the traps will become filled (trap-filled limit). Further injected charge then exists as free charge in the conduction band and contributed the current. Beyond, the trap-filled limit, the J - V characteristics is given by equation (2.10) rather than (2.11).

2.4 Characterization of traps

While relatively steady-state measurements such as J - V analysis are extremely useful, a device's response to ac signals can also be of great use in investigating the electrical properties of thin insulating films and the semiconductor surfaces. Studies of the

capacitance (C) and the conductance (G) associated with the depletion region can provide additional information about the concentration and characteristics of electrical active centers. For that reason, the ac properties of the active memory layer are monitored using capacitance and conductance spectroscopy.

2.4.1 Admittance spectroscopy[†]

A common method of profiling the ac response falls under the blanket name of admittance spectroscopy, where the spectrum referred to is the range of ac driving frequencies. Admittance spectroscopy is a powerful tool for studying relaxation processes, charge carrier injection, transport mechanisms, electrically active defects in semiconductor devices, the behavior of metal/organic interfaces and interfacial layers in organic semiconductor devices.

This section provides a background in the theory of admittance spectroscopy applied to metal-insulator-semiconductor (MIS) capacitors. The discussion begins with the introduction of the concepts in the measurement technique, followed by examination of the simple case of a single majority-carrier trap in an organic based MIS capacitor. The theory is developed to determine the influence of interface traps – the trap energy, density and capture cross section from frequency and temperature dependent impedance measurements. An equivalent circuit diagram is also derived to depict the essential physics of the theory.

2.4.1.1 Basic technique

The basic experimental technique for admittance spectroscopy is shown in Figure 2.16. A driving voltage of the form $V(\omega, t) = V_{dc} + V_{ac}e^{i\omega t}$ is supplied by the voltage source across the device-under-test (DUT) and a low-resistance load resistor, R_L , where this

[†] A great body of literature is available on this topic; therefore the following discussion is directed at a working understanding of the specific methods used in this dissertation. In particular, the reader is referred to Ref. [63].

resistance must be much less than the resistance of the DUT. A lock in amplifier phase-synchronized to the voltage source then measures the ac voltage drop, $V_{L,ac}$, across R_L and its phase shift, θ , relative to the source. A multimeter measures the dc signal, $V_{L,dc}$, across R_L concurrently.

Figure 2.16: Basic circuit for admittance spectroscopy measurements.

Determination of $V_{L,ac}$ and θ allows for the ac component of the complex current through the circuit to be written as

$$I = \frac{1}{R_L} (V_{L,ac} e^{i(\omega t + \theta)}) \quad (2.12)$$

Invoking a complex form of Ohm's law, the complex impedance can then be written as,

$$Z = \frac{V}{I} = \frac{V_{ac} e^{i\omega t} R_L}{V_{L,ac} e^{i(\omega t + \theta)}} = Z' - iZ'' \quad (2.13)$$

where Z' and Z'' , the real and (negative) imaginary parts of Z respectively.

The admittance, Y can be simplified to be^[63]

$$Y = \frac{1}{Z} = G(\omega) + i\omega C(\omega) \quad (2.14)$$

where the real part, $G(\omega)$, is the frequency dependent conductance (inverse of resistance), and the imaginary part, $\omega C(\omega)$, gives the frequency dependent capacitance of the device. Due to the parallel nature of the admittance, $G(\omega)$ and $C(\omega)$ correspond to a parallel resistance-capacitor ("RC") circuit (Figure 2.17).

Figure 2.17: Equivalent RC circuit for admittance analysis.

A Metal-Insulator-Semiconductor (MIS) capacitor is used frequently in admittance spectroscopy as it has the advantages of simplicity of fabrication and analysis. The structure shown in Figure 2.18 is the basic configuration of MIS capacitor: a dielectric layer is deposited on a semiconductor surface, followed by top gate metal electrode (eg. Au, Al). There are four main types of charges that can exist inside the dielectric and contribute to the capacitance: (i) fixed charges, primarily due to the structural defects in the dielectric; (ii) trapped charges in the bulk of the dielectric; (iii) mobile ionic charges (presence of ionic impurities); and (iv) interface charge, formed due to structural defects, imperfect processing or by dangling bonds at the interface.^[38] When organic semiconductor is employed instead of conventional silicon, it has been suggested that interface traps,^[64] trap recharging^[65] or mobile ions and impurities,^[66] structural defects,^[67] or formation/dissociation of bipolarons^[68, 69] in the accumulation layer can also cause charging effect. These charges can be determined through measurements of capacitance as a function of voltage across the MIS structures.

Figure 2.18: (a) Schematic illustration of a Metal-Insulator-Semiconductor (MIS) structure and its equivalent model circuit. (b) High-frequency and low-frequency capacitance-voltage (C-V) characteristics of MIS structure for dielectric/insulator film with and without (ideal) traps.

In a MIS structure (taking *p*-type semiconductor as an example), the application of negative voltages at the metal electrode (gate) induce an accumulation of majority holes at the dielectric-semiconductor interface. Hence, the measured capacitance is equal to that of the gate dielectric. When the positive gate voltages are applied, majority holes are repelled, causing depletion, which is similar to a parallel plate capacitor in series with the dielectric capacitance [Figure 2.18(a)]. In Figure 2.18(b),

the C - V characteristics of a MIS structure (p -type semiconductor) are illustrated using 2 scenarios: (i) ideal dielectric (without traps) and (ii) dielectric with traps. In an ideal MIS system, the flat-band voltage, V_{FB} , is zero. When trap states are present, the occupation of these states can be monitored by noting the resulting shift in the flat-band voltage, ΔV_{FB} , with reference to an ideal C - V curve. The sign of the shift depends on whether electron or hole trapping is dominant. Negative charge trapping in film translates to $\Delta V_{FB} > 0$, whereas for positive charge trapping, it is $\Delta V_{FB} < 0$. As shown in Figure 2.18(b), the presence of electron traps (negatively charged) in the MIS device cause

the C - V characteristics to shift to the right of the ideal curve. These electron traps can be in the bulk dielectric and/or interface traps. The shift in flat-band voltage, $\Delta V_{FB} = V_{FB}' - V_{FB}$ is used in equation 2.15 to calculate the total trapped charge in the dielectric, Q_{tot} .

$$Q_{tot} = C_{dielectric} \Delta V_{FB} \text{ (coulombs)} \quad (2.15)$$

2.4.1.2 Trap level occupancy

The measurement of surface conductance enables computation of trap density, in particular, interface trap density. While both capacitance and conductance measurements are able to probe interface traps, greater inaccuracies arises in capacitance measurements. This is because the interface-trap capacitance is extracted from the measured capacitance which also includes capacitances of dielectric and depletion layer. In the conductance method, this difficulty does not apply as the measured conductance is directly related to the trap states.^[64]

Figure 2.19 clarifies this idea for interface trap states. In (a) is shown the band diagram of a p -type semiconductor biased into depletion with band-bending such that the equilibrium, Fermi level of the semiconductor interrogates an interface state of energy, E_{Ti} . The small-signal equivalent circuit is shown in Figure 2.19(b). The depletion region of width, X_D , and bulk semiconductor are represented by the series parallel R - C

elements. Capacitor C_I is added to represent the gate insulator while the series elements $C_{Ti}R_{Ti}$ represent the interaction of carriers in the majority band-holes in this case-with the interface state, E_{Ti} . For completeness, a small series resistance, R_S , is included which is associated with the electrodes.

Note that the model is only accurate under depletion conditions where the majority carriers dominate the conductance process. In other situations, the interaction of the minority carriers with interface traps and their recombination with the majority carriers cannot be ignored, and as a consequence, no simple analytical model, which can explain the measured conductance behavior, exists.

Figure 2.19: (a) Band diagram for an MIS capacitor based on a p -type semiconductor when driven into depletion. The applied bias is such that the semiconductor Fermi level is probing the interface state at E_{Ti} . (b) The corresponding equivalent circuit. C_{Ti} and R_{Ti} represent the effect of the interface state at E_{Ti} . A distribution of interface states is represented by additional CR elements one for each energy state in the quasi-continuum.^[64]

The contribution, $Y(\omega)$, made to the device admittance by the depletion region and the discrete interface state can be described using the equivalent parallel capacitance (C_p) and conductance (G_p) (equation 2.14):

$$Y(\omega) = G_p(\omega) + j\omega C_p(\omega)$$

The capacitance term is then given by

$$C_p(\omega) = C_D + \frac{C_{Ti}}{1 + \omega^2 \tau^2} \quad (2.16)$$

and the loss by

$$\frac{G_p(\omega)}{\omega} = \omega \tau \frac{C_{Ti}}{1 + \omega^2 \tau^2} = \omega \tau \frac{qD_{Ti}}{1 + \omega^2 \tau^2} \quad (2.17)$$

where τ is the interface trap time constant defined as the ratio of C_{Ti} to G_p (i.e. $\tau = C_{it}/G_p$).

Although this is the simplest model, it captures the physical essence of the measured conductance as a result of the interaction of carriers with interface traps. The equation tells us that G_p/ω has its maximum value of $qD_{Ti}/2$ when $\omega\tau = 1$, and goes to zero at a very low frequency (i.e. $\omega\tau \rightarrow 0$) or at a very high frequency (i.e. $\omega\tau \rightarrow \infty$). The physical explanation for this behavior is as follows: At a very low frequency, the interface traps change occupancy in phase with the ac gate voltage, maintaining equilibrium, thereby no energy loss (no conductance) occurs. On the other hand, at a very high frequency, interface traps hardly respond and do not change occupancy with the ac gate voltage, thereby energy loss occurs but G_p/ω is very small (high frequency). At a frequency between very high and very low, the interface traps lag behind the ac gate voltage and energy loss occurs, which maximizes at the condition of $\omega\tau = 1$.

2.4.2 Deep Level Transient Spectroscopy (DLTS)

In contrast to the steady-state capacitance-voltage (C - V) methods described so far, transient capacitance spectroscopy gives information by measuring how the non-steady state capacitance changes with time t . The emission rate per trapped electron is the probability per unit time that a particular electron is emitted and is characteristic of a trap. The rate which electrons are captured at any instant is time dependent. Emission rate is dependent on capture cross section and the trap activation energy level. This requires measurement techniques which are sensitive to low concentrations of such centers in the presence of much greater concentrations of shallow impurities. By using a depletion region and by appropriate choices of external stimuli such as biases and temperature, it is possible to control the filling processes which contribute to the transient response. Transient time constant provides information about the emission rates and the transient amplitude provides information about the concentration of deep states.

Deep level transient spectroscopy (DLTS) invented by Lang^[70] is a very sensitive technique to detect deep trap levels down to a concentration of around 10^{10} - 10^{11} cm⁻³, and is normally used to characterize Schottky diodes, thin films and p - n depletion regions. It is a form of capacitance measurement which measures charge responding to applied time-varying voltage and temperature. In principle, the DLTS signal is the difference of capacitances at two different times after a filling pulse:

$$DLTS = a(C(t_2) - C(t_1)) \quad (2.18)$$

It shows peaks for different trap levels in the sample at the respective temperatures T . If traps are filled by a filling pulse and the reverse bias is switched on again, the sample is in thermal non-equilibrium and relaxes into equilibrium by detrapping the charges back. This relaxation is related with a capacitance transient. Its time constant is governed by the thermal emission rate e_n , which depends on the trap energy E_t and the temperature T :

$$e_n = \frac{1}{\tau_e} = \frac{N_n \sigma_n v_n}{g} \exp\left(\frac{-E_t}{kT}\right) \quad (2.19)$$

Here N_n is the effective density of states in the conduction band or valence band, σ_n is the capture cross section of the trap, v_n is the carrier velocity, g is the degeneracy factor. We can see here, the emission rate is exponential dependent on $1/T$, so that thermal energy (or activation energy E_t) determining its slope and the capture cross section σ determining its intercept, are the main features of the curve.

Generally, a DLTS measurement starts at a low temperature. The signal is recorded and the temperature is ramped up for measurement. During the raising of T , according to $\exp(-E_t/kT)$ dependence of the thermal emission rate, as long as T is too low for significant thermal emission until t_2 , the difference in equation 2.18 is zero. If T is so high that the thermal emission is already over at t_1 , the difference in equation 2.18 is also zero. Only if the emission time constant (or its inverse, the emission rate) of one level falls into the so-called “rate window” given by the definition of t_1 and t_2 , a DLTS peak appears. Figure 2.20 shows one example of hole traps identified by DLTS measurements in a single Si/Ge/Si structure.

Figure 2.20: DLTS spectra carried out on self-assembled SiGe quantum nanostructure using hole-filling measurements. The filling pulse duration in DLTS scans range from 1 μ s to 1 ms.^[71]

In conclusion, this chapter has presented the reader with an introduction on the principles of organic memory devices, including the basic theory of charge transport and mechanisms of charge injection from metallic contacts into organic films. The current state-of-the-art in organic memories has been reviewed. The various concepts relating to admittance and deep-level transient spectroscopy are also outlined which are useful for characterization of charge trapping effect.

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Chapter 3

Memory phenomena in chemically assembled gold nanoparticle arrays

3.1 Introduction

As highlighted in *Chapter 1*, among the many types of nonvolatile memory technology, flash memory devices with discrete charge trapping layers, such as silicon-oxide-nitride-oxide-silicon (SONOS) devices^[1] or nanocrystal-based devices,^[2] are of great interest to the electronics industry, because of their better endurance, smaller chip size and lower power consumption. However, it is very difficult to control the trap density and distribution in SONOS devices. Nanocrystal-based devices have an advantage over this since the density and location of the nanocrystals can be controlled by adjusting the process parameters. Most of the research effort has focused on nanostructure/nanoparticle formation using high temperature CMOS compatible processes.^[3] Organic memory devices which use organically passivated nanoparticles as charge storage elements can be deposited at room temperature using simple chemical self-assembly,^[4] Langmuir-Blodgett,^[5] layer-by-layer adsorption techniques,^[6] or spin-coating methods.^[7]

Much attention has been paid to chemical self-assembly, especially in the covalent or noncovalent immobilization of nanoparticles onto functionalized solid surface to obtain ultrathin nanoparticulate films. This is due to the degree of control that can be exercised over the size, shape and functions of the nanoparticle blocks and by their integration with bulk solid surfaces. Work along this line was pioneered by Colvin *et*

al.,^[8] who reported the chemisorption of CdS nanocrystals onto a metal surface by using bifunctional self-assembled monolayers (SAMs) as adhesion layers. Gold nanoparticles have also been chemically assembled to the surfaces of silanized glass, quartz and indium-tin oxide for various electrical, optical, and catalytic purposes.^[9-11] The common feature of the above works is the use of chemisorbed self-assembled monolayers (SAMs) modified solid surfaces. SAMs are molecular assemblies that are formed spontaneously by the immersion of an appropriate substrate into a solution of an active surfactant.^[12] The assembly strategy of the nanoparticles is based on the use of non-covalent electrostatic interactions as the driving force. Hence, it can be envisioned that various self-assembled monolayers and nanostructures with physical and / or chemical affinity to the self-assembled monolayers can be combined onto any substrates for various applications.

3.1.1 Objective

The present chapter seeks to define the basic process steps for fabrication and manufacturing of an organic memory device, employing gold nanoparticles (AuNPs) as charge storage components which are held by self-assembled monolayers (SAMs). The possibility to form a new organic transistor based memory system was demonstrated using pentacene as the active organic semiconductor layer and citrate-stabilized AuNPs as the charge storage elements in a metal-pentacene-insulator-silicon (MPIS) configuration (see Figure 3.1). Silicon substrate with thermally grown oxide was used as the initial platform. The SiO₂/Si substrate surface is first derivatized with 3-aminopropyl-triethoxysilane (APTES) self-assembled monolayers. Citrate-stabilized AuNPs with affinity to APTES are then deposited through electrostatic interactions and self-organized into two-dimensional arrays. The purpose of surface functionalization is to produce a uniform surface with the maximum positive charge possible to enable the efficient adsorption of negatively charged AuNPs.

Since homogeneous and highly dense assemblies of nanoparticles are desired for enhance memory performance, it is essential to begin the chapter with a brief review on the development of assembly methods, with particular attention to immobilization of metal nanoparticles on surfaces.

Figure 3.1: Schematic illustration of metal-pentacene-insulator-silicon (MPIS) organic memory device with citrate-stabilized Au nanoparticles.

3.2 Functionalized metal nanoparticle arrays on surfaces

Various functionalized solid supports such as glass, silicon wafers and metallic electrodes have been used for the adsorption of nanoparticles. The most common route for chemical derivatization of glass and silicon substrates is silanization.^[13-15] The silanized surface bears chemical groups that are capable of binding a colloid particle covalently (e.g. thiol to bind Au nanoparticles, Figure 3.2(a)) or through electrostatic interactions (e.g. amine to bind anionic nanoparticles, Figure 3.2(b)). The formation of a colloid monolayer is achieved by placing the surface-functionalized glass substrate in a solution of nanoparticles, which binds to the surface, assembling into a saturated monolayer over a period of time. The monolayer density is dependent on factors such as the particle size and charge as well as the attachment method and the substrate.^[16] The assembly of nanoparticles on gold surfaces often follows a similar procedure to that for glass substrate, i.e. surface modification of the substrate followed by the adsorption of colloid particles. The modification of the gold surface is achieved by use of a thiol,^[17] which forms a covalent link to the Au-surface. This thiol also bears a

group capable of binding a nanoparticle, for instance another thiol for Au or Pt nanoparticles,^[18] or an amine for Au nanoparticles.^[4, 19]

Figure 3.2: The construction of Au-nanoparticle monolayers on silanized substrates.

Significant results have been accomplished using layer-by-layer assembly of functionalized metal nanoparticles to create multilayers of nanoparticulate films.^[20] The assembly of electrostatically-linked nanoparticle arrays is a general method (Figure 3.3) which has been shown to be effective up to the micron-scale using charged polymers or small molecules as linkers.^[21] Metal nanoparticles stabilized with weakly bound ionic species (e.g. citrate ions) as well as charged thiolate-functionalized nanoparticles have been used in this kind of layered assemblies. For example, negatively charged 11-mercaptoundecanoic acid functionalized gold nanoparticles were self-assembled in a multilayer configuration using positively charged poly (allylamine hydrochloride) as a linker.^[22] The charge on anionic Au nanoparticles allows them to be adsorbed onto the cationic polymer and vice versa, allowing a three-dimensional structure to be built up in a stepwise fashion. Surfaces have also been prepared for nanoparticle organization by the formation of Langmuir-Blodgett films.^[23]

This methodology gives access to very thin, dense sub-layers but is not suitable for large-scale production.

Figure 3.3: Electrostatic assembly of negatively charged nanoparticles on positively charged polymer using the layer-by-layer assembly approach.^[20]

A more promising approach was undertaken in the assembly of citrate-stabilized gold nanoparticles on amine- and thiol- functionalized ITO substrates. By carefully varying the particle size, it was found that 80 nm particles formed layers over 20 times less dense than 15 nm particles (ca. 2×10^9 particles/cm² as opposed to ca. 4.5×10^{10} particles/cm²).^[13] Amine-functionalized substrates are also found to bind the particles at a slightly higher density than thiol-functionalized substrates. It should be noted that electrostatic adsorption of negatively charged gold nanoparticles on amino-functionalized solid supports is pH-dependent.^[24] The electrostatic attraction of the oppositely charged nanoparticles and the amino-functionalized surface is effective only when the amino groups are protonated at pH smaller than the pKa-value of the surface bound amino groups. The possibility of creating high density and closed-packed arrays of citrate-stabilized gold nanoparticles on amine-functionalized substrates (Figure 3.2(b)) makes this approach a very attractive one in leading the way towards the construction of addressable arrays of nanoparticle memory devices.

The following sections will describe in detail, our efforts in the fabrication of an organic memory device utilizing citrate-stabilized Au nanoparticles (as charge storage elements) on amine-functionalized substrate, in a metal-pentacene-insulator-silicon (MPIS) configuration. The citrate-shell of the nanoparticles has also been replaced with dodecanethiol ligands to study the effect of the organic capping layer on the memory performance.

3.3 Materials synthesis, preparation and characterization

This section describes the various experimental procedures, starting from synthesis of citrate-stabilized Au nanoparticles (citrate-AuNPs), surface functionalization of substrate, assembly of the nanoparticles onto substrate and fabrication of the memory device as well as the characteristic results.

3.3.1 Synthesis of gold nanoparticles

Among the conventional methods of synthesis of gold nanoparticles (AuNPs) by reduction of gold (III) derivatives, the most popular one is the classical Turkevich method,^[25] which is the citrate reduction of hydrogen tetrachloroaurate (III) (HAuCl_4) in water. Figure 3.4 illustrates the schematic representation for the synthesis. This method leads to gold nanoparticles of an average size of 20 nm in diameter. Trisodium citrate ($\text{Na}_3\text{C}_6\text{H}_5\text{O}_7 \cdot 2\text{H}_2\text{O}$) functioned as a reducing agent as well as stabilizer. As the reducing agent was added to HAuCl_4 , gold ions were immediately reduced to gold atoms until the solution became supersaturated with gold atoms. Nucleation started whereby atoms continued to bind to the nucleation sites, forming gold nanoparticles. The colloidal gold particles are surrounded by an electrical double layer formed by adsorbed citrate and chloride ions and cations which are attracted to them. This results in a Coulombic repulsion between particles, giving an overall negative charge to each gold nanoparticle.

Figure 3.4: Schematic representation for the synthesis of citrate-stabilised gold nanoparticles.

In this work, the synthesis of AuNPs was carried out via a modified Turkevich method which used trisodium citrate as the stabilising agent and sodium borohydride (NaBH_4) as the reducing agent. The main difference in the modified and classical method is the use of a stronger reducing agent, sodium borohydride. Briefly, 0.5 ml of 0.01M Hydrogen Tetrachloroaurate (III) ($\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$, 99.9%) was mixed with 0.5 ml of 0.01M trisodium citrate. The mole ratio of $\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$ to $\text{Na}_3\text{C}_6\text{H}_5\text{O}_7 \cdot 2\text{H}_2\text{O}$ was 1:1. The solution was diluted with 18 ml of deionised water and vigorously stirred. 0.5 ml of 0.1M NaBH_4 aqueous solution was added dropwise and the red solution was stirred for 30 seconds. The solution was left undisturbed for two hours.

The size of the citrate-AuNPs can be determined from the Transmission Electron Microscopy (TEM) images. TEM was performed on a JEOL 2010 operating at a magnification of 30000x. The microscope is fitted with a LaB_6 filament, and an acceleration voltage of 200 kV was used. Droplets of the gold colloids were dropped onto a copper grid with holey carbon film and dried in vacuum. Figure 3.5 shows monodisperse AuNPs of approximately $5 \pm 2\text{nm}$ in size; the agglomeration of Au nanoparticles is minimized due to the citrate induced surface energy stabilization.^[26] As compared to the classical method, the synthesized AuNPs are much smaller due to the use of a stronger reducing agent. The AuNPs synthesized using the classical method is of approximately 20-23 nm in diameter (Figure 3.6).

Figure 3.5: TEM images of 3-5nm AuNPs synthesized using modified Turkevich method.

Figure 3.6: TEM images of 20-23 nm AuNPs synthesized using classical Turkevich method.

The size of the gold nanoparticles can also be evaluated by studying their surface plasmons. UV-Vis spectra reflects the surface plasmon band (SPB) which is related to the dipole oscillations of the free electrons in the conduction band occupying the energy states immediately above the Fermi energy level. Hence, as the particle size decreases into the nanosized regime of $<5\text{ nm}$, the electron density in the conduction band becomes very small, thus accounting for the decrease in intensity of the SPB and a broadening of the plasmon bandwidth. In general, a colloidal solution of gold nanoparticles with diameters of 5–20 nm exhibits a red color, because such nanoparticles have an optical absorption peak around 520 nm, caused by surface plasmon resonance.^[26] The AuNPs using both the classical and modified Turkevich method has been characterized using UV-Vis spectroscopy. The UV-Vis spectrometer used is Shimadzu UV-2501 PC. The absorption spectra as depicted in Figure 3.7 showed a peak at approximately 523 nm for the classical Turkevich method. The absorption spectrum of modified Turkevich method shows a broadening of the absorption peak and a slight blue shift in the wavelength (509.4 nm). This is because of the use of stronger reducing agent of sodium borohydride, which resulted in much smaller AuNPs.

Figure 3.7: UV-Vis spectra of Au nanoparticles synthesized using classical and modified Turkevich method.

3.3.2 Gold nanoparticle Assemblies

In this section, the method of preparing a colloidal gold monolayer on thermally grown SiO_2 film on Si substrate is described, which is achieved by the specific electrostatic interaction of the negatively charged citrate-stabilized AuNPs with the positively charged amine functions of an amino-terminated silane (APTES) monolayer.^[27] The deposition process is delineated in Figure 3.8.

Figure 3.8: Schematic illustration of nanoparticle assemblies.

3.3.2.1 Formation of Self-assembled Monolayers on substrate

The silicon wafers were first cleaned in piranha solution (2:1 concentrated H_2SO_4 : 30% H_2O_2), followed by RCA clean,^[28] to remove possible organic contaminants. After the RCA clean, the silicon substrate surface is rich in hydroxyl groups, which were used to link the 3-aminopropyl-triethoxysilane (APTES) molecules. The amino-terminating APTES self-assembled monolayer was formed on the silicon surface by immersing the silicon substrate in 5% volume of APTES in absolute ethanol for 1 hour. The modified substrate was then rinsed successively in ethanol and deionized water to remove any loosely bound molecules and blow dried with nitrogen gas. Finally, the substrates were baked in vacuum oven at 120°C for 30 minutes to complete the Si-O bond formation.^[29]

The main observation indicating the formation of a self-assembled monolayer on the substrate is a drastic reduction of the surface wettability as revealed by contact angle measurement. Wettability studies were carried out on a FTA100 series contact angle measuring instrument, equipped with a charge coupled device (CCD) camera. A total of 3 droplets of deionised water on different spots were tested for each samples. Figure 3.9(a) and (b) shows the sessile water drop on unmodified SiO_2/Si substrate, cleaned by Piranha and RCA treatment and with APTES modified substrate respectively. The water contact angle increased from 27.36° to 60.99° . The measured contact angle of APTES modified substrate is in agreement with previous published work,^[30] which gives a contact angle of 67° .

Figure 3.9: Sessile water on (a) Piranha plus RCA solution treated SiO_2/Si substrate (b) with APTES modification.

Another characterization technique used to confirm the chemisorption of APTES on silicon substrate is by X-ray Photoelectron Spectroscopy (XPS) measurements. The XPS measurement was done by Kratos AXIS spectrometer (UK) with the monochromatic Al $K\alpha$ radiation source (1486.6 eV photons, 150 W). The base vacuum in XPS analysis chamber was about 1×10^{-9} torr. All spectra were calibrated using C1s at 284.6 eV as a reference.

Figure 3.10: XPS spectra of (a) APTES on SiO_2/Si substrate surface, (b) High-resolution scan of the N_{1s} region in APTES-coated silicon substrate.

Figure 3.10(a) shows the XPS spectra acquired from APTES-coated silicon substrate which indicates the surface composition from the substrate and the SAM layer: silicon ($\text{Si } 2s, 2p$), carbon ($\text{C } 1s$), oxygen ($\text{O } 1s$) and nitrogen ($\text{N } 1s$). The Si_{2p} core level peak at 102.8 eV proves the existence of Si-O bonds on the surface. The N_{1s} signal in the spectrum can qualitatively account for the existence of APTES on silicon surface. The high-resolution XPS spectra of N_{1s} are also shown in Figure 3.10(b), where the N_{1s} peak is centered at 398.6 eV. All the XPS spectra obtained are in agreement with the observations of Wei *et al.*^[31]

The presence of APTES was also determined using FTIR in the attenuated total reflection (ATR) mode. Infrared spectroscopy gives information on molecular vibrations or more precisely on transitions between vibrational and rotational energy levels in molecules. These transitions can be directly related to the molecular structure or chemical bonding. A Perkin Elmer System 2000 Fourier transform infrared spectrometer was used to characterize the APTES film on $\text{SiO}_2\text{-Si}$ substrate. The vibrational energies of around 3454, 1230, 1095 cm^{-1} corresponds to the NH_2 absorption, $\text{Si-CH}_2\text{-CH}_2\text{CH}_3$ and $\text{Si-O-CH}_2\text{CH}_3$ respectively (Figure 3.11).^[32-34]

Figure 3.11: FTIR spectra of APTES film on SiO₂-Si substrate. R represents CH₂CH₃. The inset shows the FTIR spectra from same APTES film but in the range 3480 – 3420 cm⁻¹, to show the NH₂ absorption clearly.

Figure 3.12(a) and (b) show the AFM surface plot of APTES modified substrate and bare substrate respectively. AFM images were obtained in tapping mode with a Digital Instruments DimensionTM 3000 scanning force microscope. The atomic force microscope was operated with an optical readout using Si cantilevers. The roughness of the APTES-modified substrate is only 0.304 nm, which did not differ much from that of the unmodified substrate of 0.205 nm. This shows that the APTES layer is molecularly flat and free of pinholes.

Figure 3.12: Height-contrast images of (a) APTES-modified substrate and (b) bare SiO₂/Si substrate.

Finally, the thickness of the amino-terminated silane on the silicon substrate was measured by ellipsometry. The ellipsometer used is Variable Angle Spectroscopic Ellipsometer (VASE), Model VB250. The refractive index used is 1.50. The thickness of the silicon substrate was fixed at 1mm so that the substrate can be assumed to be infinitely thick and no significant amount of light can reach the back side of the substrate. The thickness of the SiO₂ layer was measured separately on an unmodified substrate first and subtracted from the total layer thickness determined for the APTES monolayer-covered SiO₂/Si substrate. The difference in thickness yields the thickness of the APTES layer. A monolayer of APTES on the silicon was confirmed by ellipsometry, which revealed a film thickness of 0.9 nm, consistent with previous reports.^[35, 36]

3.3.2.2 Gold nanoparticle immobilization

The AuNPs were assembled on the amino-terminated silicon substrate surface by immersing the substrates into the solution of AuNPs for 12 hours. The pH of the gold colloids was adjusted to 6. Since the solution of the AuNPs was slightly acidic, adding this solution to the amino-silylated substrates led to the protonation of the amino groups on the surface. Such positively charged substrate surfaces enabled electrostatic attraction of negatively charged citrate stabilized AuNPs. The substrates were removed from the solution, rinsed with deionised water and blow dried with nitrogen.

To observe the distribution of the AuNPs and have a more close inspection on the packing features of these nanoparticles when the pH environment differs, AFM images are given in Figure 3.13 for a clear comparison. The AFM images showed a more densely-packed layer of gold nanoparticles when the pH of the gold colloids is decreased to 6, as compared to the original pH value of 8. The average particle density (at pH 6) is around $7 \times 10^{10} / \text{cm}^2$, which is comparable to previous work.^[13] It should be noted that the particle widths in both AFM images are in the range of 20–30 nm, considerably larger than the value determined from TEM measurements (5 ± 4 nm). However, if a section analysis is performed on the AFM image, it is found that the particle height is nearly identical with the TEM size. Such a deviation is attributed to

the convolution effect of true particles with the AFM tip, which is often observed in AFM imaging.^[37]

Figure 3.13: AFM image of deposited AuNPs on APTES-modified substrate at (a) pH 8 and (b) pH 6.

The surface plasmon band of the gold nanoparticulate film was also characterized. Glass slide coated with the AuNPs was placed perpendicular to the light beam. As a result of the dipole-dipole electromagnetic interaction between the particles,^[38, 39] the surface plasmon resonance of the Au nanoparticles shifted from 509 nm, for the particles in the colloid (Figure 3.14, curve a) to 526 nm for the particles immobilized on the surface of APTES-modified glass slide (Figure 3.14, curve b).

Figure 3.14: Absorption spectra of (a) gold colloid, (b) gold nanoparticle assembled on APTES-modified substrate.

3.3.3 Memory device fabrication

The final memory device structure has been depicted in Figure 3.1. It comprises of a metal-pentacene-insulator-silicon (MPIS) structure, where pentacene is the active semiconductor layer. Pentacene is used as *p*-channel material in this work since the performance of pentacene-based OFETs now reaches the level of amorphous Si devices.^[40, 41] It is an organic molecule composed of five fused benzene rings, with energy gap of about 1.9 eV (HOMO level of ~5 eV and LUMO level of ~3.1 eV).

The degenerately doped *n*-type silicon substrate is used as the bottom gate electrode, with 4.5-nm thermally grown silicon dioxide on top. The AuNP layer was deposited on the SiO₂ substrates at room temperature and pressure by chemical self-assembly. The pentacene is thermally evaporated, at a deposition rate of 0.1 nm/s and a pressure of 10⁻⁷ torr, to form a 45-nm-thick film. The top metal electrode of gold was subsequently deposited by thermal evaporation through a shadow mask forming capacitor and transistor electrodes.

All electrical measurements were carried out at room temperature and in vacuum environment (~10⁻⁴ torr). The Capacitance-Voltage (*C-V*) and Conductance-Voltage (*G-V*) measurements were done with an HP 4284A Precision LCR Meter at the frequency of 100 kHz and amplitude of 15mV was superimposed on the DC bias. Current-Voltage (*I-V*) measurements were done with Keithley 4200 semiconductor characterization system. The low temperature measurements are done in a cryogenic probe station (Lakeshore TTP6), where the sample temperature was monitored using a Lakeshore-model 332S auto tuning temperature controller with sensitivity better than ±0.1K.

3.4 Organic Memory Capacitor

3.4.1 Memory characteristics and charge trapping

Figure 3.15(a) first shows the C - V and G - V characteristics of control device (metal/pentacene/APTES-modified substrate), where the gold nanoparticles deposition step was omitted. In each measurement, the scan was started from depletion region and swept towards accumulation. It can also be clearly seen in the C - V curve that pentacene is p -type, where the accumulation region occurred when the negative gate bias is applied and the low capacitance of the depletion regime occurred at positive gate biasing. Similarly, from the G - V characteristics, the pentacene layer exhibits high conductivity in the negative bias region and low conductivity in the positive bias region due to accumulation and depletion of charge carriers respectively. The measured flatband voltage is approximately -2.3V . Such negative flatband voltage implies the presence of positive charges within the fabricated structure. This could be associated with the self-assembled APTES layer. It was found that organosilane molecules have different functional groups that possess a permanent electric dipole field.^[42] This dipole field has the same effect as applying a gate bias. The reaction of APTES with hydroxyl terminated SiO_2 surfaces forces the direction of the dipole moment to be outward (i.e. outward from the SiO_2 surface towards pentacene).^[34] Therefore, the potential across this dipole layer changes the surface potential at the pentacene/APTES interface, which is equivalent to applying a positive electric potential on the pentacene. This explains why the accumulation region occurs only after the application of a more negative voltage. Another significant observation is negligible C - V or G - V hysteresis (i.e. flat band voltage shift), indicating absence of trapped charges in the fabricated control structure.

Figure 3.15: Double sweeping $C-V$ and $G-V$ characteristics at 100 kHz obtained by sweeping gate voltage between +5V and -5V on (a) control sample (pentacene on APTES-modified substrates without Au nanoparticles) and (b) with Au nanoparticles respectively.

Figure 3.15(b) shows the $C-V$ and $G-V$ characteristics of the MPIS structure with deposited AuNPs, where a clockwise hysteresis window of 1.25V is observed upon double sweeping within the range of ± 5 V. This indicates a net hole trapping effect. The lack of significant hysteresis in the reference devices indicates that the charge trapping effect came from the AuNPs. Under the influence of a negative bottom gate voltage, there are two competing processes: (1) electrons can be injected into the AuNPs from the n -type substrate where electrons are the majority carriers, (2) holes are injected into the pentacene layer from the top Au electrode (due to the highest

occupied molecular orbital level of pentacene which is close to the work-function of Au^[43], creating an abundance of holes in the pentacene layer. This promotes the injection of holes from the pentacene layer to the citrated AuNPs and leads to a net hole trapping effect. Upon applying a positive gate voltage, the stored charges in the AuNPs are flushed out, resulting in a flat-band voltage shift. The clockwise nature of the hysteresis indicates that process 2 is the dominant mechanism. For process 1, where charge injection occurs via the 4.5nm-SiO₂ layer (leading to counter-clockwise hysteresis), the carrier transport distance is greater than 10 nm when the additional thickness of the capping layer (the center to center distance of citrate shell is 6.8-7.2 nm^[44]), and the self-assembled APTES layer (~1 nm) are taken into consideration. This is too large for effective tunneling through substrate and hence carrier transport through pentacene layer dominates.

There is also the appearance of a conductance peak in both forward and reverse directions [Figure 3.15(b)]. This means that single-hole trapping and de-trapping events are occurring. In other words, the peak in conductance around flat band condition indicates a trap event occurring when a hole is stored per AuNP. In *G-V* measurements, the trap levels are detected through the energy or ac loss resulting from changes in their occupancy produced by small variations of gate voltage.^[45] For a given ac frequency in the experiment, the dc gate voltage was varied from depletion to accumulation state. The capture rate of the carriers in the depletion state is low since almost no carriers are exchanged between the AuNP and the pentacene layer. In the accumulation state, majority carrier density is very large near the pentacene/AuNP interface, so that the AuNP capture rates are very high compared to the ac frequency. The AuNP levels respond immediately to the ac voltage, and no loss is observed. Energy loss, which is due to capture/emission of carriers (represented by an equivalent conductance, G_p , of the MPIS structure) is minimal in both the cases. This could be the reason for the appearance of a single conductance peak around flat-band voltage. It should be noted that the occurrence of the single conductance peak observed is not associated with the pentacene/APTES interface states, a conclusion that can be drawn by comparison with the observation of the control sample without AuNPs.

With the increment of the maximum operation bias from 5V to 10V, the hysteresis window of the C - V curve increases from 1.25 V to 2.05V (Figure 3.16). This indicates that more and more holes are being trapped in the AuNPs and/or at the interface of the AuNPs upon increasing the gate voltage. There is also little or negligible shift in the initial flat-band voltage upon increasing the operation bias, indicating minimal influence of interface traps. The trapped hole density (Q) calculated using the equation $Q = C \Delta V_{FB}$ (where C is the capacitance per unit area of dielectric stack and ΔV_{FB} is the memory window), can be determined to be $\sim 3.59 - 5.89 \times 10^{11}$ charges/cm².

Figure 3.16: C - V curves of MPIS device with Au nanoparticles at 100 kHz for different gate bias sweeps.

There are two important features observed in the C - V characteristics between the MPIS structures with and without the AuNPs (Figure 3.17). First, the maximum and minimum capacitance per unit area in the control sample (i.e. metal-pentacene-APTES-SiO₂-gate) is higher than the sample with gold nanoparticles. Second, the flat-band voltage of the control sample is more negative than the sample with AuNPs.

During the C - V measurements, only the charges from relatively shallow states responded to the variation of voltages at high test frequencies, since the capture-and-

release of charges in these states had small time constants.^[46] Charge carriers that are deeply trapped do not contribute to the determined capacitance. The fact that the control sample is able to achieve higher capacitance than the sample with AuNPs under the same frequency suggested that there were fewer states which localize charges in the pentacene layer of the control sample; there is presence of more mobile holes that can accumulate in the forward bias. Comparing the AFM images (Figure 3.18) of the pentacene layer in the control sample and in the sample with AuNPs, the grain size in the control sample is much larger and lesser grain boundaries resulted. Since the roughness of the surface of the deposited AuNPs is higher than the control sample, the pentacene growth will be more disordered, resulting in deeper charge trapping sites in the grains or grain boundaries.

Figure 3.17: Single C - V characteristics of Control Sample and With AuNPs, sweeping from +5V to -5V. Frequency used is 100 KHz.

The more positive shift in the initial flat-band voltage for the sample with AuNPs as compared to control sample might be due to 1) difference in total charge in the MPIS structure, where charge trapping in the gold nanoparticles occurred during the C - V measurements, 2) incorporated negatively charge citrate ions associated with the

nanoparticles, and 3) difference in the work function between the gold nanoparticles and APTES.

Figure 3.18: AFM topology images of pentacene on (a) APTES-modified substrate (b) immobilized gold nanoparticles –APTES modified substrate. The average pentacene grain size in (a) is around 570 nm while in (b) is 160 nm.

3.4.2 Frequency response

In order to relate the origin of the conductance peaks and hysteresis with the AuNPs, as opposed to the interface traps, frequency dependent measurements were performed. As is evident in Figure 3.19, we found similar clockwise C - V hysteresis and an almost constant (standard deviation of 0.04) full width at half maximum (FWHM) of the conductance peaks in G - V characteristics in the frequency range of 50 kHz – 1MHz at room temperature. This indicates that the hysteresis and conductance peak are of the same origin,^[47, 48] and since interface traps are minimal in the high frequency ranges, we can conclude that the charge trapping effect originates from the AuNPs.

Figure 3.19: Frequency dependent (a) C - V and (b) G - V characteristics of the organic memory device. The inset shows the FWHM as a function of frequency.

3.4.3 Nanoparticle density dependence

We have varied the Au nanoparticle density deposited on the substrate by changing the immersion times of the substrate in the gold colloids, ranging from 4 to 12 hours. The C - V hysteresis window widens as the particle density increases (see Table 3.1). This is

because a higher nanoparticle density will lead to more charge trapping events and hence comparatively more stored charges.

Table 3.1: Relationship of Nanoparticle Density with Memory Window

Immersion time (hour)	Nanoparticle Density (particles/cm ²)	Memory Window (C-V hysteresis over an operating voltage of $\pm 5V$)
4	6×10^9	0.74 V
6	8×10^9	0.88 V
12	7×10^{10}	1.2 V

3.4.4 Temperature dependence

The capacitance and conductance characteristics at various temperatures, ranging from 100K to 300K, were investigated (Figure 3.20). The MPIS organic memory device at various temperatures showed the typical clockwise *C-V* hysteresis and single conductance peaks in both forward and reverse sweeps. It is observed that the *C-V* hysteresis window widens as the temperature decreases to 100K. The inset of Figure 3.20(a) shows the dependence of flat-band voltage shift (ΔV_{FB}) with respect to temperature. The ΔV_{FB} increased from 0.82V to 2.28V when the temperature decreased from 300K and 100K. The increase in ΔV_{FB} at lower temperature might be due to the decrease in lateral diffusion of holes through the Au nanoparticles and/or freeze-out of holes at low temperatures. The decrease in conductance peak at lower temperatures [Figure 3.20(b)] further suggests the freeze-out of holes and hence lower tunneling (discharging) paths existed. An activation energy (E_a) of 13.3 meV can be derived from the plot of conductance peak value as a function of reciprocal temperature [Figure 3.20(c)]. This value is considered low when compared to the thermal activation energy of pentacene which ranges from 50-300 meV^[49, 50] and to the deep trap levels in nanocrystals based memory devices which ranges from 500-1500 meV.^[51] Such weak temperature dependence of conductance indicates that deep defects have negligible contribution in the charging and discharging processes in AuNPs.

Figure 3.20: (a) C - V and (b) G - V characteristics measured at 100 kHz for various temperatures. The inset shows the dependence of flat-band voltage shift (ΔV_{FB}) with respect to temperature. (c)

Conductance peak value (G_p) vs reciprocal temperature measurement at 100 kHz. The estimated activation energy is 13.3 meV.

A number of studies of nanoparticle arrays have reported the scaling of activation energies with nanoparticle size, with the smallest nanoparticle having the largest activation energy.^[52-54] The dependence of activation energies on nanoparticle size suggests that they arise from charging of nanoparticles. The charging energy of a nanoparticle takes into account the capacitance of the nanoparticle ensemble and cross-capacitances since charges on one nanoparticle can polarize the neighboring nanoparticles. A simple approach is to employ an electrostatic model, where we approximate the neighboring nanoparticles as a conducting continuum separated from the central nanoparticle by an insulating shell as described by Abeles *et al.*^[55] We attempt to use this electrostatic model to determine the charging energy from particle size and spacing, and compare with the experimentally determined activation energy.

In this electrostatic model, the capacitance of the nanoparticle, C_{NP} , is

$$C_{NP} = 4\pi\epsilon_0\epsilon_r \left(\frac{1}{R} - \frac{1}{R+s} \right)^{-1} = 4\pi\epsilon_0\epsilon_r \frac{R(R+s)}{s} \quad (3.1)$$

and the charging energy, E_C , can be expressed as

$$E_C = \frac{e^2}{8\pi\epsilon_0\epsilon_r} \frac{s}{R(R+s)} \quad (3.2)$$

where each nanoparticle has a radius R and separated from neighboring nanoparticles by an average distance s . ϵ_r is the dielectric constant of the material surrounding the nanoparticles (Figure 3.21).

Figure 3.21: (a) Conducting nanoparticle of radius R separated from neighboring nanoparticles by an average distance s . The nanoparticles are embedded in an insulating medium with dielectric constant ϵ_r . (b) Nanoparticle in (a) is modeled as a sphere separated from a conducting surrounding by an insulating shell with thickness s and dielectric constant ϵ_r .

In this work, the radius of the nanoparticles is around 5 nm, with separating distance of around 5–7 nm (determined from the AFM images in section 3.3.2.2). We took into account two types of material surrounding the nanoparticles – the pentacene matrix and the citrate shell. The dielectric constant of pentacene ($\epsilon_{\text{pentacene}}$) is around 6^[56] while of citrate shell ($\epsilon_{\text{citrate}}$) is around 0.25–0.6.^[57] Due to the much higher polarizability of the pentacene matrix, it will determine the effective capacitance. Hence, the effective dielectric constant, $\epsilon_{\text{effective}} \sim 6$. Thus, the charging energy of our system is calculated to be about 14 meV. This charging energy is in close agreement to the experimentally determined E_a of 13.3 meV, further implying it is easy to charge or discharge the charge carriers in the AuNPs.

3.4.5 Charge transport mechanism

Figure 3.22(a) displays the current density through the whole device stack with and without Au nanoparticles in both forward and reverse bias. Lower current through the whole device is observed for the sample with Au nanoparticles; the current obtained from the control sample (pentacene/APTES/SiO₂) was at least two orders of magnitude higher. This might be due to charges being stored inside the Au nanoparticles and “screens” the effective electric gate field, resulting in lower effective voltage applied and hence lower current. During voltage sweeping from 0 to -4.5V, the applied electric

field can cause charging and discharging of some Au nanoparticles, leading to the breaking or formation of some conductive paths and thus decrease or increase of current respectively. Hence, the current oscillates with the charging and discharging of the Au nanoparticles for low electric fields, i.e. below 8.24 MV/cm. For higher electric fields, an enhanced conductivity is observed and the current rises rapidly. Given the relatively thick citrate shell (center to center distance 6.8-7.2 nm^[44]), we predict that the main transport mechanism might be Fowler-Nordheim (F-N) tunneling rather than direct tunneling. F-N tunneling effect between nanoparticle and polymer has also been observed by Laurent *et al.*^[58] We fitted our experimental data using the F-N plot [inset of Figure 3.22(b)]; using the slope constant of the F-N plot and the effective hole mass in pentacene to be $1.5m_0$ (where m_0 is the free electron mass),^[59] the barrier height is calculated to be 0.84 eV.

We have also calculated the highest occupied molecular orbital (HOMO)-lowest unoccupied molecular orbital (LUMO) energies of citrate shell using the (DFT B3LYP) density function theory with the 6-31+G (d, p) basis set. The modeling was performed by Dr Zhang Xiang at Nanyang Technological University, Singapore. The HOMO and LUMO of the citrate shell is determined to be 1.3 eV and 6.7 eV respectively. This leads to a barrier height of 1.7 eV between the citrate shell and pentacene layer, which the holes have to overcome to reach the AuNP. The experimental determined barrier height is lower than the theoretical barrier height. One possible explanation is due to the assumption of an ideal platform in DFT modeling, where the calculation of the molecules are done in gaseous phase and not taking into account any interactions with other molecules or environmental influences. Another possibility is due to electrostatic charging of the AuNPs,^[60] where the AuNPs are charged with positive charges, capturing holes from the pentacene layer and thus changing the potential in the vicinity of the barrier.

Figure 3.22: (a) Current density–voltage (J - V) characteristics of the MPIS device with (blue, solid line) and without (red, dotted line) gold nanoparticles. (b) The schematic diagram of charge transport (tunneling) in pentacene-nanoparticle system including two nanoparticles, with quantized energy bands. The open circles represent holes. (c) Fowler-Nordheim (F-N) plot of MPIS structure with gold nanoparticles, where the voltage range from -4.5V to -10V. A linear fitting of the F-N plot for a limited range of $1/E$ values (voltage range is from -5.7V to -10V) is also presented. (d) Energy-level representation of Pentacene, citrate shell and core of Au nanoparticle. The highest occupied molecular orbital (HOMO)-lowest unoccupied molecular orbital (LUMO) energies of citrate shell were calculated using the (DFT B3LYP) density function theory with the 6-31+G (d, p) basis set, with LUMO to be ~1.3eV and HOMO to be ~6.7eV.

3.4.6 Data retention characteristics

The charge storage effects were examined further by monitoring the C - V and G - V characteristics after a “write” voltage of -3V is applied for different charging times, Figure 3.23(a). There is a continuous positive shift in the ΔV_{FB} after the “write” voltage of -3V is applied for 1-120 seconds. When a single sweep from $+2\text{V}$ to -2V of the bottom gate voltage is first applied, injection of holes from the pentacene layer to the citrated Au nanoparticles occurred. It is believed that the stored positive charges in the Au nanoparticles will cause a polarization effect around the pentacene molecules^[61, 62] and results in decrease in ionization energy (i.e. lowering of LUMO levels). Verlaak *et al.*^[62] has shown that shrinking of LUMO-HOMO levels resulted when positive polarization occurs around a hole trap-rich pentacene molecule. The positive shift in the ΔV_{FB} for the C - V characteristics is most likely due to this decrease in the energy level. This prevents the direct observation of hole tunneling (which implies negative ΔV_{FB}). A positive ΔV_{FB} can also imply electron injection from the silicon substrate but the possibility of electrons is eliminated since the I - V characteristic (see Figure 3.22) has shown low tunneling paths for low E fields ($< -4.5\text{ V}$).

The retention properties are studied by first charging the capacitor 60 seconds at a write voltage of -3V as shown in Figure 3.23(b). The initial flat-band voltage of a typical MPIS device with Au nanoparticles is measured to be -0.75 V . The decayed capacitance measurement was carried out under a -0.75 V bias voltage. A retention ability of over $\sim 85\%$ is observed for 10,000 seconds. It should be noted that the capacitance measured is sometimes more than the initial capacitance. This means that the reading voltage of -0.75V is also able to charge up the gold nanoparticles. Hence, some random charging occurs when the reading voltage is applied. We attribute the good retention ability to two main factors: (1) As mentioned earlier, the barrier height seen by the holes inside the nanoparticle is increased due to the shrinking of HOMO-LUMO level of pentacene molecule. (2) The double citrate buffer layer between Au nanoparticles (barrier height between the HOMO level of citrate shell and Au

nanoparticle is ~ 1.6 eV) may also contribute to the retention ability by reducing tunneling probabilities between the nanoparticles.

Figure 3.23: (a) C - V and G - V sweeps measured on MPIS structures incorporating Au nanoparticles before and after applying a “write” voltage of -3V for various stressing times (t); $t = 0$ (blue), 1s (red), 60s (green), 100s (pink) and 120s (black). The inset shows the dependence of ΔV_{FB} on the stressing times. The bottom gate voltage is swept from $+2\text{V}$ to -2V in steps of 0.05V . (b) Time dependences of the stored charge from the flat-band state. The memory device is first charged at -3V for 60seconds and the decayed capacitance measurement is carried out under a -0.75V bias voltage.

For the application of positive gate voltages, there is no shift in the C - V characteristics observed. Figure 3.24 shows an example where a positive 8V was applied for 5 seconds. At positive gate voltages, the pentacene layer is depleted and it is difficult to induce minority carriers in pentacene which is unipolar nature (holes only). The low current density at the positive electric field as shown in Figure 3.22 further illustrates this explanation and hence there is absence of any charging or trapping events occurring in the Au nanoparticles. We will explain in subsequent chapters on this issue of single-carrier mode (holes or electrons only) in organic semiconductors and its impact on programming-erasing operations.

Figure 3.24: C - V sweeps measured on MPIS structures incorporating Au nanoparticles before and after applying a positive gate voltage of 8V for 5s; $t = 0$ (black), 5s (red).

3.4.7 Dependence of organic capping layer of nanoparticle

Citrate is known to be a relatively weak stabilizer ionically bound to the surface of inorganic colloids. On the other hand, thiols are known to have a strong affinity for metal chalcogenides and to form covalent bonds on their surface. In this section, we attempt to study the effect of organic capping layer surrounding the AuNPs on the charging effect by replacing the citrate ions with alkanethiol molecules. Since

alkanethiols have been reported to have a higher tunnel resistance,^[63, 64] the retention time maybe improved upon (trapped charge carriers are prevented from tunneling out easily).

After the process of gold nanoparticle assembly (as described in section 3.3.2.2), the substrates are immersed in 5mM ethanolic solution of dodecane-1-thiol (DDT) for 24 hour, and rinsed with an ethanol bath and dried with nitrogen gun. Because of the strong affinity of sulfur to gold, this treatment replaces the citrate adsorbates with the alkanethiol molecules. In addition to the adsorbate removal, the bonding between the sulfur and gold can even displace the bonding between the amino group and gold (Figure 3.25). This results in the complete ligandation of the gold particle with DDT molecules (DDT-AuNPs). The electrostatic interaction between the negatively charged surface of AuNPs and the positively charged amino groups on the substrate surface was removed and replaced by Van der Waals attraction. As a consequence, the once immobilised particles are now released from the substrate and acquire some mobility on the substrate surface. As the interaction between the nanoparticles and the substrate becomes lower, the amplitude of the localizing Brownian motion or lateral diffusion of DDT-AuNPs will become larger. These DDT-AuNPs can move and collide with each other on the surface and aggregate due to the Brownian motion and Van der Waals attraction.

Figure 3.25: Schematic illustration of replacing citrate with DDT.

Figure 3.26: AFM image of deposited DDT-AuNPs on APTES-modified substrate.

Figure 3.26 presents the AFM image of the deposited DDT-AuNPs, with an average size of 8 ± 1 nm. It can be seen that the coverage of the deposited DDT-AuNPs is lesser as compared to citrate-AuNPs., with an average particle density of $2 \times 10^8 / \text{cm}^2$. Following similar fabrication procedures as described in section 3.3.3, pentacene thin film and top gold electrode are deposited to complete the MPIS structure (see Figure 3.27).

Figure 3.27: Schematic illustration of metal-pentacene-insulator-silicon (MPIS) organic memory device with dodecane-1-thiol (DDT)-stabilized Au nanoparticles.

Figure 3.28(a) first compares the ΔV_{FB} ($C-V$ hysteresis) of the devices based on citrate-AuNPs and DDT-AuNPs at various operating voltages. In general, a much larger memory window is observed for the DDT-AuNPs system. Although a larger memory window is exhibited, the non-parallel shift of the $C-V$ characteristics [Figure 3.28(b)]

suggests presence of interface traps.^[47] The magnitude of the V_{FB} shift is also dependent on the sweep speed of voltage (10-100mV/s). This reflects that the stored charges tunnel out with a certain charge-loss rate.^[65] This greatly contrasts to the initial prediction of improved retention ability. This is also in contrast to the citrate system [inset of Figure 3.28(b)] where its hysteresis or conductance peak shift is independent of the scan direction and speed.

To investigate further, the response of the $C-V$ and $G-V$ characteristics with frequency is measured to check for influence of interface traps, Figure 3.28(c). The moderate frequency dependence of G_p/ω peak is indicative of the combined effects from both interface traps and nanoparticles. The appearance of sharp conductance peak in the forward sweep and broad conductance peak in the reverse sweep also indicates the presence of interfacial defects. Both peaks follow similar response to frequency, typical of interfacial defects with an energy distribution close to valence band edge.^[47]

Next, we also compare the current density through the devices [Figure 3.28(d)]. Overall, the current level in DDT-AuNPs system is also lower as compared to citrate-AuNPs system. This might be due to lesser density of AuNPs and/or increase in tunneling resistance due to DDT ligands. Similar to the citrate-AuNPs system, the current conduction in the DDT system has showed F-N tunneling characteristics [inset of Figure 3.28(d)]. The barrier height is calculated to be 1.77 eV, which is higher than that of the citrate system. The increase in barrier height and tunneling resistance further indicates that the observed increased in memory window is not due to direct trapping of holes from pentacene to the DDT-AuNPs. Instead holes are most likely to be initially trapped in DDT/pentacene and/or DDT/AuNP interfaces and then transferred to the AuNPs.

But it should be noted that we cannot make a concrete comparison between the citrate and DDT-system since there are many variables that can affect each individual system. For example, we need to take into account the difference in nanoparticle density on substrate ($7 \times 10^{10}/\text{cm}^2$ for citrate system versus $2 \times 10^8/\text{cm}^2$ for DDT system), the

packing density, the nanoparticle size deviation ($5 \pm 2\text{ nm}$ for citrate system versus $8 \pm 1\text{ nm}$ for DDT system) and particle spacing (citrate to citrate shell distance of $\sim 7\text{ nm}$ versus DDT to DDT ligand spacing of $\sim 3\text{ nm}$ ^[66]). We have also not considered the non-ideal situations where the nanoparticles are not in close pack distribution. Nevertheless, these results provide insights on the importance of interfaces. Most reports focuses on physical tailoring of distances between nanoparticles and chemical manipulation of the linker molecules between the nanoparticles and their effects on the mode of transport (tunneling or hopping).^[67, 68] The influence of local charge environment (since nanoparticles have large surface area) and/or its interfaces can be another important contributing factor in charge transfer.

Figure 3.28: (a) Dependence of flat-band voltage shift (ΔV_{FB}) with respect to increasing operation voltages (from $\pm 3\text{ V}$ to $\pm 10\text{ V}$) for the MPIS devices employing citrate-AuNPs and DDT-AuNPs. The ΔV_{FB} is measured by double sweeping C - V characteristics at 100 kHz (sweeping gate voltage

between +2V and -2V. (b) Dependence of voltage step (ranging from 0.1V to 0.01V steps) of the $C-V$ hysteresis. (c) Frequency dependent $C-V$ characteristics of the organic memory device using DDT-AuNPs. The inset shows its corresponding $G-V$ characteristics (from 50 kHz to 1MHz). (d) Current density–voltage ($J-V$) characteristics of MPIS device with citrate-AuNPs and DDT-AuNPs respectively. The inset shows the F-N plot of the DDT-AuNPs system, where the linear fitting is done for a limited range of $1/E$ values (voltage range is from -7V to -10V).

3.5 Organic memory transistor

In this section, we integrate the MPIS memory structure into a transistor configuration (see Figure 3.29). Source and drain electrodes were evaporated through a shadow mask with channel length of 175 μm and width of 1000 μm . A reference transistor is also fabricated for comparison (pentacene on APTES-modified substrate, without nanoparticle deposition).

Figure 3.29: Schematic illustration of organic field-effect memory transistor comprising citrated-stabilized Au nanoparticles.

The typical output and transfer characteristics of the OFET memory device are shown in Figure 3.30. The measured values of the typical hole mobility (μ_{hole}) and on/off ratio ($I_{on/off}$) were $0.03 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and 10^5 – 10^6 respectively. The threshold voltage, V_T , was obtained to be around -1.85V determined from the x -intercept of the linear portion of the plot of $I_D^{0.5}$ versus V_G .

Figure 3.30: (a) Output characteristics (I_D versus V_D) of a pentacene based organic field-effect transistor (OFET) memory utilizing citrate-stabilized Au nanoparticles. The gate voltage varies between 0V to -40V in steps of 10V. (b) Double sweeping semilog plots of I_D - V_G transfer characteristics of pentacene OFET utilizing citrate-stabilized Au nanoparticles. The inset shows the I_D - V_G characteristics of reference device (pentacene OFET with only APTES treated substrate). The channel length and width of the transistors are 175 μm and 1000 μm respectively. The drain voltage (V_D) is -10V. The gate leakage currents are plotted in dotted lines.

For the reference APTES transistor, a poorer device performance is yielded: $\mu_{\text{hole}} = 0.00007\text{--}0.0005 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, $I_{\text{on/off}} = 10^2\text{--}10^4$ and $V_T = -11.5\text{V}$ [see inset of Figure

3.30(b)]. The reference device has a more negative threshold voltage which may be related to the surface functionalization by positively charge amino-terminated silane. It should be noted that control pentacene transistor with thermal oxide alone gave a standard OFET performance with mobility of around $0.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and on/off ratio of 10^6 .

To investigate the memory properties, double sweeping of the transfer characteristics was measured. As shown in Figure 3.30(b), an anticlockwise hysteresis loop was observed, with a threshold voltage shift of 4V. This large negative threshold voltage shift can be ascribed to positive charge trapping in the Au nanoparticles. It should be noted that such hysteresis effect is not observed in the reference transistor [inset of Figure 3.30(b)]. The number of stored charges (Δn) can be determined from the shift in V_T according to $\Delta n = (\Delta V_T * C_i / e) = 8.62 \times 10^{11} \text{ cm}^{-2}$, where C_i is the oxide capacitance of $3.45 \times 10^{-8} \text{ Fcm}^{-2}$ and e is the elementary charge.

The memory performance during programming and erasing operations was also investigated, through the application of voltage pulses of fixed durations. The transfer characteristics were measured before and after each programming or erasing pulses. Figure 3.31 presents typical results for the memory transistor. The programming operation consisted in applying a negative gate pulse which causes a negative threshold shift in the transfer curve, due to the trapping of holes from the pentacene channel into the Au nanoparticles. Increasing V_T shifts could be brought about by increasing the magnitude of the programmed pulse or pulsing time, further demonstrating the increasing hole trapping events. A large reduction in the drain current is observed after a programming gate pulse of -30V for 30s. The occurrence of strong charge carrier trapping is also observed when the application a positive gate pulse of 30V for 30s could not bring the programmed curve back to the pristine curve (“erasing” mode); no recovering of the curve. The ‘difficulty’ in erasing is probably due to the (1) unipolar nature of transport across pentacene and hence prevents efficient electron injection and transport at positive gate voltages, and/or (2) the channel is depleted for $V_G > 0$; the lifted channel potential reduces the effective electric field and thus lowering the

potential seen by the Au nanoparticles. This effect has already been observed in the MPIS capacitor where no shift in the C - V characteristics was observed during positive voltages pulsing (see section 3.4.6).

Figure 3.31: Transfer characteristics obtained after different gate pulse conditions for pentacene based OFETs using citrate-stabilized Au nanoparticles with channel length of 175 μm and channel width of 1000 μm . The gate voltage varies between +20V to -20V while the drain voltage, V_D , is -10V. The transfer characteristic of pristine device is in blue curve. The programming and erasing operations are according (1) $V_G = -20$ V was applied for 5s; red curve, (2) $V_G = -30$ V was applied for 5s; black curve, (3) $V_G = 30$ V was applied for 30s; green curve, (4) $V_G = -30$ V was applied for 30s; pink curve. $V_D = 0$ V during all programming and erasing operations.

3.6 Summary

In conclusion, we have fabricated, at relatively low temperature by chemical self-assembly, an organic memory structure containing pentacene as the organic semiconductor and self-organized Au nanoparticles. A pronounced clockwise capacitance-voltage (C - V) hysteresis is observed with a memory window of 1.25V to 2.05V achievable under 5V to 10V programming range. Temperature-dependent measurements revealed activation energy of 13.3 meV. The increase in flat-band

voltage at lower temperature might be due to the freeze-out of electrons at interface states and decrease in lateral diffusion of holes through the Au nanoparticles. Current voltage characteristics were used to study the charge transport of the carriers in the gold nanoparticles and it is shown that Fowler-Nordheim hole tunneling is the main tunneling mechanism that has occurred. A charge retention ability of 85% over more than 10,000 seconds has been demonstrated. The study of the influence of insulating barrier surrounding the gold nanoparticles on the charging effect has also been done. Finally, we have extended the two-terminal memory device to a pentacene organic field-effect memory transistor, where the occurrence of strong hole trapping from the channel to the gold nanoparticles is observed.

Although the assembly strategy of the nanoparticles showed stable, memory potential, the fabrication process is rather time-consuming, making it not suitable for large-area processing. In extending to all-organic transistor based memories, degradation of device properties may also be observed due to multiple process steps – nanoparticle deposition, tunnel and/or control dielectrics formation and/or post metal annealing making it more prone to defects or interface trap generation. Therefore, it is desirable to find a simple and low-temperature method able to produce a homogeneous high density nanoparticles array as charge storage elements that can be reliably incorporated into organic transistors. Hence, in the next few chapters, we will dedicate our efforts on self-assembling amphiphilic diblock copolymers, where a one-step fabrication process is used to generate ordered arrays of gold nanoparticles.

3.7 Reference

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Chapter 4

Non-volatile memories enabled by in-situ synthesis of gold nanoparticles within a self-assembled block copolymer

4.1 Introduction

The possibilities of realizing nanoscale electronic, optoelectronic, magnetic and biological devices have fueled a groundswell of interest in technologies that enable facile nanostructure formation. As traditional top-down patterning methods like photolithography has been shown to be time-consuming and expensive, self-assembly techniques are currently the focus of intense research. Self-organized nanoparticles represent an elegant approach to create huge ensembles of electronic traps that enable the memory functionality. Much efforts have been carried out to assemble nanoparticles on substrates^[1, 2] since a homogeneous and high density array of charge storage dots is desired. In *Chapter 3*, we have paid attention to one specific method which is the covalent or noncovalent immobilization of nanoparticles onto functionalized solid surface to obtain ultrathin nanoparticulate films. Another variant of the bottom-up approach, which is the focus of the present chapter, exploits self-assembling amphiphilic diblock copolymers, whose ability to micro-phase separate offers an effortless approach to ordered organization on the nanometer scale^[3, 4] and hence providing a template for creation arrays of nanoparticles.

Another major advantage of employing block copolymer is the one-step preparation of nanoparticles/polymer composite by binding the precursor component of the nanoparticle to specific (hydrophilic) domains of the block copolymer and *in-situ*

synthesis of the nanoparticles by chemical reduction. The size of the nanoparticles can be controlled by varying the volume fraction of each block or the loading ratio of the precursor to binding block. Such a preparation method also solves the problem of particle size control and stabilization as compared to the classical stabilization systems by surfactants or in microemulsions.^[5] A narrow size distribution of the particles is necessary to maintain the memory performance and a polymeric dielectric medium will prevent electronic interactions between the nanoparticles and other conductive materials.

Due to the variability of the block copolymer chemistry, it is possible to modify the binding block for stabilization of different types of nanoparticles. The choice of monomer can also be tailor-made where the volume fraction of each block and/or total molecular weight can be varied to create different types of tunneling barrier, and hence utilized in different memory architectures and applications. In other words, a wide range of block copolymers and metal or semiconducting nanoparticles can be combined to realize low-cost, solution processable design and process schemes in memory applications.

4.1.1 Objective

This chapter seeks to develop organic memories based on *in-situ* synthesized gold (Au) nanoparticles in self assembled block copolymer of polystyrene-*block*-poly-4-vinylpyridine (PS-*b*-P4VP).

In the first part, a brief literature review of current activities related to the application of block copolymers as stabilizers for nanoparticles and its related electrical properties are discussed. In the second part, micellar characteristics are studied and a solvent extraction method was implemented to “clean” the copolymer where residual impurities were removed which would otherwise interfere with the memory and electrical properties. We also summarize data on the synthesis procedures of Au nanoparticles in self-assembled block copolymer micelles and characterization

techniques of polymer and its solution and film properties. Next, the electrical properties of Au nanoparticles in PS-*b*-P4VP are examined: A metal-insulator-semiconductor (MIS) structure was used to study the charging/discharging phenomena of the Au nanoparticles. The conduction mechanism of the nanoparticles in block copolymer nanodomains has also been studied in details. The electrical studies indicate the potential use of nanoparticles in block copolymers for nano-Flash memory applications.

4.2 Nanoparticles in amphiphilic block copolymers: material and electrical properties

4.2.1 Microdomain formation and nanoparticle synthesis

Block Copolymers are linear macromolecules that consist of different blocks (often incompatible) of different types of monomers. The tendency of block copolymers to self-assemble in bulk and solution through microphase separation (driven by the chemical incompatibilities between the different blocks) into nanometer-scale structures is a well-known phenomenon.^[6-9] The microphase separation in block copolymers gives rise to formation of different types (lamellar, cylindrical or spherical) of microdomains in the solid state (Figure 4.1). The polymer morphology and domain size are determined by the volume fraction of each block and the total molecular weight of the block copolymer. Typical periodicities are in the range of 10-200 nm. The unique architecture of block copolymers allows them to be widely used in soft lithography^[10] or self-assembled templates as a substrate for inorganic nanoparticles.^[11, 12] Kinetic control over block copolymer film morphology proved as an effective means of arranging the nanoparticles in an ordered array (Figure 4.2).

Figure 4.1: Common morphologies of microphase separated block copolymers: body centered cubic (bcc) packed spheres (BCC), hexagonally ordered cylinders (HEX), gyroid ($Ia\bar{3}d$), hexagonally perforated layers (HPL), modulated lamellae (MLAM), lamellae (LAM), cylindrical micelles (CYL), and spherical micelles (MIC).^[9]

Figure 4.2: TEM cross-section images of (a) Au-salt-loaded micelles deposited onto a carbon coated copper grid, (b) final array of Au nanodots prepared on top of a sapphire substrate, and on (c) silicon, demonstrating the nearly spherical shape of the resulting particles.^[13] (d) TEM of

poly(styrene-*b*-4-vinylpyridine) block copolymer micelles containing small Au colloids per micelle after fast reduction with LiAlH_4 .^[9] (e) Cross-sectional TEM images of thin PS-*b*-P4VP films containing Au nanoparticles. The Au nanoparticles are enriched in the P4VP microphase after direct formation within the matrix via reduction from a $\text{HAuCl}_4/\text{NaBH}_4$ solution.^[14] (f) Scheme of illustration for formation of extended monomicellar films and subsequent plasma treatment.^[15]

Block copolymer domains can also be used as ‘nanoreactors’ for the synthesis of inorganic nanoparticles. Reviews of the subject are available.^[3, 9, 16] Two basic approaches have been developed. The first involves the binding of inorganic species to the monomer prior to polymerization or to one of the blocks of a copolymer prior to micellization (which may be induced by the ion binding^[9]). The most important approach, however, involves the loading of preformed micelles, whether in solution or in bulk. In either case, there are basically four steps, i.e., preparation of the block copolymers, loading of the precursor, micellization, chemical reaction followed by nucleation and growth process (Figure 4.3). The succession of steps is variable. The critical factor is that the block copolymer must be selected in such a way that one block has affinity with the precursor and the other block with the liquid medium. The block copolymer micelles turned out to be an excellent model system, which is simple and provides nanoparticles that do not aggregate together. In addition, the corrosion of metal particles can be avoided by binding the metal particles to the polymeric micro-environment.

Figure 4.3: Schematic illustration of preparing inorganic colloids in block copolymer microdomains.

Cohen *et al.* have methodically examined the preparation of diblock copolymer nanoreactors, which are loaded with metal salt and subsequently reduced to form nanoparticles in the nanodomains. They have demonstrated the patterning of complexes of silver,^[17, 18] gold^[17] and zinc.^[19] In 1992, Saito *et al.*^[20] prepared silver nanoparticles in a poly-2-vinylpyridine block of polystyrene-*b*-poly-2-vinylpyridine

(PS-*b*-P2VP) by soaking partly cross linked film with Ag compounds and consequent reduction of silver from AgI. PS-*b*-P2VP and polystyrene-polyethylene oxides (PS-*b*-PEO) have been employed as media for preparation of gold colloids by Möller *et al.*^[21-23] Particularly relevant to quantum dot applications of semiconductor nanoparticles, A. Eisenberg and coworkers described the preparation of CdS and PbS nanoparticles within the cores of PS-*b*-poly(cadmium acrylate) diblocks from organic solvents.^[24, 25] The size of the particles were controlled by changing the length of the ionic poly(cadmium acrylate) block. An alternative approach to the preparation of CdS nanoparticles exploits complexation with the P2VP core of PS-*b*-P2VP micelles.^[26] Here, the nanoparticles are aggregated into ‘raspberry’ morphology clusters.

Among many well known block copolymers as micellar nanoreactors for metallic nanoparticles, polystyrene-*block*-poly-2-vinylpyridine (PS-*b*-P2VP) or polystyrene-*block*-poly-4-vinylpyridine (PS-*b*-P4VP) block copolymers are of particular interest. This is due to the ability of poly(vinylpyridine), P2VP or P4VP, to form complexes with metal salts in the presence of an N atom.^[13, 14, 27-30] For example, Pd clusters have been produced by reduction of Pd(CH₃COO)₂ that coordinates to the P4VP micellar core formed by PS-*b*-P4VP diblocks in toluene.^[27, 30] Other metal nanoclusters including cobalt,^[31] gold,^[13, 14, 28, 30] rhodium^[27] and platinum^[27] have been prepared in a similar way. Antonietti *et al.* has also observed the effect of reducing agent used for gold particles in PS-*b*-P2VP copolymer – strong reducing agent like superhydride or sodium borohydride leads to formation of many particles in each micelle core, while in the case of hydrazine reduction, slow nucleation forms one particle per micelle.^[30]

4.2.2 Charge transport in block copolymer nanocomposites

The carrier transport between semiconductor/metal nanoparticles embedded in block copolymer remains unexplored until recently. In 1999, Simon *et al.*^[32] commented that the interparticle spacing for Au nanoparticles in polystyrene-*block*-polyethyleneoxide

micelles in the range of more than 10 nm is expected to be large enough to exclude charge transport. But recently, Li and coworkers observed tunneling behavior in CdSe quantum dots self-assembled in P4VP domains of a PS-*b*-P4VP diblock copolymer thin film at room temperature,^[33] Figure 4.4(a). The electron tunneling rate constant of CdSe quantum dots confined in P4VP nanodomain is found to be much larger than that in a random distribution in PS-*b*-P4VP using conductive atomic force microscopy (C-AFM) and Fowler-Nordheim (FN) tunneling of electrons has been modeled to be the conduction process from the C-AFM tip through P4VP and into the conduction band of CdSe dots. The conductivity of the CdSe/P4VP nanodomain was also found to increase in accordance with a percolation model with increasing amount of CdSe. In 2007, the same research group replaced CdSe with Au nanoparticles^[34] and proposed the model of collective charge transport in the nanodomain-confined Au nanoparticles [Figure 4.4(b)]. The Au nanoparticles are treated as capacitively coupled conductors where charges are allowed to tunnel between neighboring particles. The current is assumed to flow through the Au nanoparticles-P4VP nanodomains, owing to a much high resistance of PS phase. The accessible current-conducting pathways are described by Equation 4.1:

$$I \sim (V/V_T - 1)^\zeta \quad \text{for } V > V_T$$

(4.1)

where I is the current, V is the voltage, ζ is a scaling exponent, and V_T is the threshold voltage (onset of conduction). The scaling exponent ζ can be regarded as the dimensionality for collective electron transport for arrays of dots as modeled by Middleton *et. al.*^[35]

Figure 4.4: (a) Current-voltage (I - V) curves of a single CdSe/P4VP nanodomain in (CdSe/P4VP)- b -PS thin films, as measured by C-AFM. The dotted lines are best fits of the FN equation. Inset: The energy bands of the C-AFM tip, CdSe/P4VP monolayer, and substrate, E_f is the electron Fermi energy inside Pt, and ϕ_e is the barrier height between Pt and CdSe/P4VP. eV_a is the applied potential energy difference between the tip and the substrate.^[33] (b) Scaling behavior of I - V curves of 48% (Au nanoparticles /P4VP)- b -PS and Au nanoparticles/homo-P4VP at 78K.^[34]

4.3 Materials synthesis, preparation and characterization

This section focuses on the experimental procedures; the controlled synthesis of stabilized Au nanoparticles in the micelles of amphiphilic block copolymers. The binding processes as well as the colloidal structure parameters were characterized by electron microscopy, IR- and UV spectroscopy, dynamic light scattering, x-ray photoelectron spectroscopy and small-angle x-ray scattering.

4.3.1 Block copolymer micelles: preparation technique and characteristics

PS-*b*-P4VP diblock copolymers ($M_n^{\text{PS}} = 11\,800$ kg/mol, $M_n^{\text{P4VP}} = 15\,000$ kg/mol, $M_w/M_n = 1.04$) were obtained from Polymer Source, Inc. The molecular structure of the copolymer is shown in Figure 4.5.

Figure 4.5: Molecular Structure and micellation process of PS-*b*-P4VP

Due to the widely different solution behaviors of PS and P4VP, the corresponding block copolymer is able to form micelles in a wide range of organic solvents. In this work, the copolymer was dissolved in toluene to form a concentration of 5 mg/mL. The micellation process is also illustrated in Figure 4.5. Toluene preferentially dissolves the PS block, whereas the P4VP is almost insoluble. As a consequence, the diblock copolymers associate to form micelles at a rather low concentration. The

micellar solution was under ultrasonic agitation for 10 minutes, followed by placing in hot plate at 120 °C for 5 minutes. The micellar solution was then left undisturbed for 2 hours.

The formation of micelles, packing and their assembly within thin films was studied by transmission electron microscopy (Jeol JEM 2010 operating at 80 kV) and atomic force microscopy (Digital Instruments DimensionTM 3000 scanning force microscope in the tapping mode). Thin films were deposited from the micellar solution either on a carbon-coated copper grid (for TEM) or on a silicon substrate (for AFM). The PS-*b*-P4VP films were either spun coat on silicon surfaces at 1000 rpm for 60 sec or a drop was left on the carbon-coated copper grid and then immediately freed from the wetting liquid by bringing it into contact with a soaking tissue.

The TEM images allow us to obtain a projection image through the film where the contrast was caused by the difference in electron density between the P4VP core and the PS corona of micelles. As shown in Figure 4.6(a), the co-polymer film showed a continuous bright PS matrix and dark spherical P4VP cores. The diameter of the P4VP cores is 33 nm. The spacing between the adjacent P4VP cores is approximately 29 nm.

Figure 4.6: (a) Transmission electron micrograph and (b) Topography image of PS-*b*-P4VP monofilm. (c) cross section line profile using the topography image in (b) with the average diameter of the micelle determined to be ~29nm, and (d) schematic illustration of self-assembled PS-*b*-P4VP micellar film on substrate.

As a complementary method, atomic force microscopy gave information on the topological structure of the block copolymer films. Figure 4.6(b) depicts a layer of rather uniformly and densely packed spherical micelles. The micelles have sufficient kinetic stability to keep their original shape after rapid evaporation of the toluene solvent and can be arranged on the substrates to form ordered nanostructures. They appear to be forming hexagons by the interaction with the adjacent micelles which is typical for densely packed soft balls.^[36] The thickness of the copolymer film and diameter of the micelles were also measured by utilizing the AFM. Using the cross-section line scan profile, the diameter of the micelle is around 29-31 nm. The 30 nm measured thickness of the layer is consistent with the diameter of the micelle, indicating the formation of a monofilm. Hence, Figure 4.6(d) illustrates the schematic diagram of the self-assembled PS-*b*-P4VP micellar film on substrate.

4.3.1.1 Cleaning of block copolymer (Solvent Extraction Method)

Similar to other nanocrystal-based memory devices, charge trapping can also occur due to defects of the host dielectric matrix itself. They are four main types of charge trapping elements in a host matrix: 1) mobile ionic charges, 2) fixed charges, 3) trapped charges and 4) interface trapped charges.^[37] These undesirable charges are present as a result of impurities and process imperfections, which can interfere with the memory properties. Therefore, further treatment or process to the block copolymer film may be needed to increase its integrity as a dielectric layer.

To check the integrity of the copolymer film, capacitance-voltage (*C-V*) measurements were done in a capacitor device utilizing “as-purchased” PS-*b*-P4VP layer (see inset of Figure 4.7 for device structure). As shown in Figure 4.7, a hysteresis loop is observed in the *C-V* characteristics for the “as-purchased” copolymer, where the hysteresis is defined to be the flat band voltage shift (ΔV_{FB}), indicating charging effect in the copolymer film. This is most likely attributed to the ionic impurities such as LiOCH₃ (catalyst end product) due to the synthesis process. To further confirm, absorbance spectrum of the solution was measured. One must see a shoulder, valley or excessive

tailing in the absorption spectrum to suspect the presence of an impurity.^[38] As shown in Figure 4.8, the UV-vis spectrum of the PS-*b*-P4VP copolymer solution shows a strong absorption peak at 281 nm which corresponds to the $n \rightarrow \pi^*$ transition.^[39, 40] However, a shoulder peak was observed, implying the existence of impurities. Hence, a cleaning method was implemented to remove these residual impurities.

Figure 4.7: Capacitance-voltage (C - V) characteristics of “as-purchased” PS-*b*-P4VP at 100 kHz. The inset shows the schematic illustration of the metal-insulator-semiconductor (MIS) structure utilizing the dielectric stack of PS-*b*-P4VP and SiO₂ (4.5nm).

Figure 4.8: Absorption spectrum of “as-purchased” PS-*b*-P4VP solution. The polymer concentration was 0.1M in toluene.

The detailed purification process of the copolymer is described in Appendix C. Generally, the purification was done by dissolving the “as-purchased” PS-*b*-P4VP in toluene and washing the copolymer solution with de-ionized water. The ionic impurities will be transferred to the water phase. The water phase containing the impurities is then removed and the toluene phase containing the PS-*b*-P4VP was precipitated from hexane. The final precipitate was dried at 50 °C under vacuum for 48 h.

As noted in Figure 4.9, the absorption intensity of the “cleaned” copolymer solution is substantially increased and the shoulder peak has disappeared. In addition, Figure 4.10 reveals that, after the purification of the PS-*b*-P4VP, hysteresis-free *C-V* curve is observed. The hysteresis-free *C-V* curve is independent of the scan direction and speed (10-100 mV/s) as shown in the inset of Figure 4.10. The “cleaned” PS-*b*-P4VP also exhibits better dielectric properties where the leakage current density and dielectric constant is around 10^{-9} A/cm² and 3.08 respectively as compared to the “as-purchased” polymer with 10^{-6} A/cm² and 2.24. The decreased in leakage current for the “cleaned” copolymer reflects a reduction in ionic conductivity, further proving the success of solvent extraction process.

Figure 4.9: Absorption spectra of “cleaned” and “as-purchased” PS-*b*-P4VP solutions. The polymer concentration was 0.1M in toluene.

Figure 4.10: Capacitance-voltage (C - V) characteristics of “cleaned” PS- b -P4VP at 100 kHz. The inset shows the C - V characteristics of “cleaned” PS- b -P4VP at different voltage steps.

4.3.2 In-situ synthesis of gold nanoparticles in block copolymer micelles

When a micellar solution of PS- b -P4VP (“cleaned” form) is treated with tetrachloroauric acid ($\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$) with the required amounts given in molar relation to the P4VP units, AuCl_4^- ions were bound as counterions in the polar core of the micelles by protonating the pyridine units, resulting in the formation of polyionic block. The P4VP block is a strong metal-chelating agent, where a large number of metal ions can be fixed in the micelle core. The molar ratios of HAuCl_4 /pyridine units in the final solutions for this work are 0.1, 0.2 and 0.3 respectively. The solutions were subsequently stirred for 24 h and then treated with hydrazine monohydrate (ratio of $\text{N}_2\text{H}_4 \cdot \text{H}_2\text{O}$: $\text{Au}^{3+} = 1:1$). Because of its polar character, hydrazine is taken up preferentially in the core of the micelles where Au^{3+} ions were reduced and nucleated to form elemental gold particles in micelle cores (Figure 4.11). The originally pale yellow solution turns deep purple within a few seconds.

Figure 4.11: Scheme of synthesis of Au nanoparticles in PS-*b*-P4VP

In the following sections, we provide characteristics of the synthesized gold nanoparticles (AuNPs) in PS-*b*-P4VP copolymer; PS-*b*-(P4VP/AuNPs).

4.3.2.1 Particle size, spacing and distribution

The aspects of particle spacing, size and homogeneity are characterized by electron microscopy, atomic force microscopy, dynamic light scattering and small-angle X-ray scattering. Figure 4.12 shows a series of TEM images of micellar films, where the P4VP core had been loaded with different amounts of tetrachloraurate ions and after chemical reduction to form Au nanoparticles. It can be seen clearly that the Au nanoparticles that are generated in the P4VP core are 10 ± 3 nm in diameter.

Figure 4.12: TEM of poly(styrene-*b*-4-vinylpyridine) block copolymer micelles containing gold nanoparticles. For (a) and (b), the molar ratio of H[AuCl₄]: P4VP is 0.1. For (c), the molar ratio of H[AuCl₄]:P4VP is 0.3.

Figure 4.13 presents the scanning force micrographs of the assembling micelles on substrate. The micelles retained their integrity, demonstrating that the ion pair

interaction within the core is sufficiently strong and permanent to prevent formation of a lamellar equilibrium organization.^[36] Using the cross-section line scan profile [Figure 4.13(b)], the diameter of the micelle is around 50 nm. The size of the micelle has increased due to the loading of the gold compound. The measured thickness of the layer is consistent with the diameter of the micelle, indicating the formation of a monolayer.

Figure 4.13: (a) Topography image of spin-coated PS-*b*-P4VP containing gold nanoparticles thin film, (b) cross section line profile using the topography image in (a) with the average diameter of the micelle determined to be ~52nm, and (c) schematic illustration of self-assembled PS-*b*-P4VP containing gold nanoparticles on substrate.

To reflect the arrangement of the nanoparticles on substrate, field emission scanning electron microscopy (Jeol JSM 6340F) and topography (from atomic force microscopy) images are presented (Figure 4.14), where oxygen plasma treatment were performed on the PS-*b*-(P4VP/AuNPs) micellar film. After the oxygen plasma process, the block copolymer had been completely removed and revealed reasonably good order of the nanoparticles.

Figure 4.14: Scanning electron microscopy and topography image of Au nanoparticles arrays after removal of the PS-*b*-P4VP micelles by oxygen plasma treatment on the SiO₂-Si substrates.

Dynamic light scattering (DLS) experiments have also been done to determine the size of the micelle core upon loading of Au nanoparticles. Dynamic light scattering, known as photon correlation spectroscopy, determines Brownian motion of the particles and relates size to it by measuring the temporal fluctuations of the intensity of scattered light.^[6] Zetasizer Nano-ZS system was used to perform these experiments and the scattering intensity was measured at an angle of 173°. The solutions were diluted to concentrations of 0.01 mg/mL in toluene.

Table 4.1 summarizes the hydrodynamic radius (R_h) of the parental micelles in toluene as well as of the Au-salt and nanoparticles-containing micelles. As seen by the hydrodynamic radius as well as the polydispersity of the aggregates, the micellar characteristics remain essentially unchanged after the synthesis of the Au nanoparticles. The pure PS-*b*-P4VP copolymer has R_h value of 24.4 nm and increased to 39.0 nm after the loading of precursor salt (HAuCl₄). Upon reduction, the micelles are still well defined and narrowly distributed with R_h measured to be 29.5 nm.

Table 4.1: Micelle Parameters determined by Dynamic Light Scattering

Sample	Polydispersity index (PDI)	R _h (nm)
Pure PS- <i>b</i> -P4VP	0.017	24.4
PS- <i>b</i> -(P4VP/HAuCl ₄)	0.093	39.0
PS- <i>b</i> -(P4VP/AuNPs)	0.313	29.5

Although the microscopy images give a good indication for the shape and size of the Au nanoparticles, it is more precise to add X-ray analysis for the quantitative description of the sample where the properties of some 10^{12} particles are averaged without selection.^[41] Hence, we have conducted small angle x-ray scattering measurements (SAXS). SAXS measurements can be conducted on dispersions and thin films to obtain information about the shape of the core, size distribution and inter-particle interactions. The SAXS experiments were performed using a SAXSess camera (Anton Paar) with a standalone X-Ray generator (PANalytical, PW3830) operating at 40 kV and 50 mV with a sealed-tube Cu anode. A Göbel mirror was used to convert the divergent polychromatic X-ray beam into a collimated line-shaped beam of CuK α radiation ($\lambda = 0.154$ nm). The two-dimensional scattering pattern was collected on an imaging plate and then integrated into a one-dimensional scattering function $I(q)$ using SAXSQuant software from Anton-Paar. The measurements are performed on thin films of PS-*b*-(P4VP/AuNPs) which were obtained by simple spin-coating onto thin mica substrates. The scan was carried out at 25 °C. In addition, dilute solutions sealed in a quartz capillary holder were also performed, resulting in essentially the same results.

As slit collimation of the primary beam was used in the experimental setup, desmearing of the scattering curve was required and this was done using the indirect Fourier transformation (IFT) algorithm^[42] using the general inverse Fourier transform (GIFT) routine. The experimentally measured SAXS curve is used to calculate the pair distance distribution (PDDF) using IFT which is the probability (statistical average) of finding a second particle as a function of distance from an initial particle. The pair

distance distribution (PDDF), $p(r)$, can be used to determine the overall shape and size of the scattering particles. The separating distance (r) equals the diameter of a particle. Figure 4.15 shows the PDDF of the scattering, which is symmetrical. This indicates that the particles are monodispersed and spherical. The average diameter (r) is determined to be 14 nm which is in agreement with the average size observed using the TEM.

Figure 4.15: Pair distance distribution function for poly(styrene-*b*-4-vinylpyridine) block copolymer micelles containing gold nanoparticles thin film on mica substrate. The molar ratio of HAuCl_4 : P4VP is 0.1. The size (r) of the gold nanoparticle is 14 nm.

4.3.2.2 Particle density

The particle densities in PS-*b*-P4VP micelles are estimated by considering the size of the Au nanoparticles, loading of the Au precursors (Au^{3+} :P4VP = 0.1, 0.2, 0.3) and total number of micelles in the system. The detailed calculations are provided in Appendix D.

The micelle density, ρ_{micelle} is assumed to be 1 g/cm^3 , which is constant in the micelle volume and equal to the bulk density of PS and P4VP.^[36] The weight of one micelle (M_{micelle}) is defined as:

$$M_{micelle} = \rho_{micelle} \frac{4}{3} \pi R^3$$

where R is the radius of micelle.

The total number of micelles ($N_{micelle}$) is then determined to be:

$$N_{micelle} = M_{copolymer} / M_{micelle}$$

where $M_{copolymer}$ is the weight of copolymer solution used.

The total number of gold nanoparticles ($N_{particle}$) can be defined to be

$$N_{particle} = \frac{N_{T,gold_atoms}}{N_{gold_atoms}} = \frac{\eta_{HAuCl_4} \cdot N_A}{V_{particle} \cdot d_{Au} \cdot N_A / MW}$$

where $N_{T,gold_atoms}$ is defined as the total number of gold atoms, N_{gold_atoms} is the number of gold atoms in one particle, η_{HAuCl_4} is the number of moles of $HAuCl_4$, N_A is the Avogadro's number, $V_{particle}$ ($= 4/3\pi r^3$) is the volume of a Au nanoparticle with diameter ($2r$), d_{Au} is the density of gold, MW is the molecular weight of gold.

Therefore, for an area A (cm^2), the number of particle density ($D_{particle}$) is defined as

$$D_{particle} = N_{particle} / M_{micelle} * A / \pi R^2$$

Table 4.2 summaries the particle density with various loading of Au precursors and the sizes of each particle as determined from TEM and SAXS respectively.

Table 4.2: Particle Density with different concentration of Au precursors

Loading of Au precursors (Au ³⁺ : P4VP)	Particle Density (cm ⁻²) (R=10 nm as determined from TEM)	Particle Density (cm ⁻²) (R=14 nm as determined from SAXS)
0.1	2.61 x 10 ¹⁰	9.50 x 10 ⁹
0.2	4.01 x 10 ¹⁰	1.46 x 10 ¹⁰
0.3	6.67 x 10 ¹⁰	2.43 x 10 ¹⁰

4.3.2.3 Chemical state of Particle

To study various physical properties of the nanoparticles, more detailed information on all preparation steps is necessary. Hence, this section emphasizes the study of the interfacial interaction of gold precursor in PS-*b*-P4VP and their final chemical state after the synthesis through absorption, fourier transform infrared spectroscopy and x-ray photoelectron spectroscopy.

Figure 4.16 shows the UV-vis absorption spectra of various Au nanoparticle solutions. The absorbance bands were located around the same position (ca. 545 nm) irrespective of the incorporation ratio of HAuCl₄, and their intensity increased linearly with increasing incorporation ratio. The absorption band with a maximum at ca. 545 nm can be ascribed to the surface plasma (SP) band of Au nanoparticles, further confirming the formation of Au nanoparticles. As well known, unprotected Au nanoparticles display an absorption band with a maximum at ca. 520 nm. Here, the red shift of SP band can be attributed to an interaction between the Au nanoparticles and the pyridine units of P4VP.^[43]

Figure 4.17 shows the absorption spectra of PS-*b*-P4VP thin films. The position of the absorption maximum in the block copolymer thin film at 256 nm is almost unchanged upon *in-situ* synthesis of the Au nanoparticles. This finding suggests non-covalent interactions between the Au nanoparticles and PS-*b*-P4VP copolymer.^[44] These spectra are simply the sum of the absorption spectra of the constituent parts of the composite films, with no evidence of additional absorption peaks in the spectra range measured

(200-900 nm). These results indicate that there is negligible ground-state charge-transfer between the copolymer and the nanoparticles.^[45]

Figure 4.16: UV-vis absorption spectra of Au nanoparticles in PS-*b*-P4VP with various loading ratios (Molar ratios of Au³⁺:P4VP = 0.1, 0.2 and 0.3).

Figure 4.17: UV-vis absorption spectra of PS-*b*-P4VP (with or without Au nanoparticles) thin films. The molar ratio of Au³⁺: P4VP is 0.3.

Fourier Transform Infrared (FTIR) spectroscopy is a powerful tool for the study of specific interactions in polymer/molecule blends^[46] and in polymer-surfactant systems.^[47] FTIR features of interest have been considered recently in relation to polymer blends of P4VP and P2VP with other polymers containing hydroxyl groups that form hydrogen bonds with the basic nitrogen.^[48, 49] FTIR spectroscopy was performed to study the complex formation between P4VP and gold precursor (HAuCl_4) during the synthesis. As reported previously, the incorporation of HAuCl_4 results in local protonation of the pyridine units followed by electrostatic interaction of the quaternary ammonium species with AuCl_4^- anions (*i.e.* complexation of HAuCl_4 and the pyridine units).^[30] Figure 4.18 presents a schematic illustration of the complexation process between Au^{3+} and nitrogen lone electron pair in the pyridine ring.

Figure 4.18: Complexation of pyridine unit and HAuCl_4

A Perkin Elmer System 2000 Fourier transform infrared spectrometer was again used to characterize the polymers. First a background scan was run with ground potassium bromide (KBr) die-pressed into flat circular pellet. Then drops of the copolymer sample were dropped onto the surface of the KBr pellet. The spectrum of the mixed pellet was then collected against the spectrum of the background. A total of 100 scans at a resolution of 2 cm^{-1} (in the mid IR region of 4000 to 400 cm^{-1}) were obtained.

Figure 4.19: Comparison of the IR-spectra of the pure block copolymer PS-*b*-P4VP and a metallated micelle filled with stoichiometric amounts of HAuCl₄ (Au³⁺:P4VP = 0.2).

The FTIR study of the PS-*b*-[P4VP/(HAuCl₄)] composite, with equimolar ratio of 1:5 is shown in Figure 4.19. The spectrum of pure PS-*b*-P4VP is given in the same figure, emphasizing the most affected bands after the complexation (1380 – 1650 cm⁻¹ region). A characteristic carbon-nitrogen stretching band due to the pyridine ring in P4VP is observed at 1601, 1493, 1453, and 1419 cm⁻¹. The disappearance of the bands characteristics for the pyridine units (1557 and 1419 cm⁻¹) and the appearance of new bands (1637, 1610, and 1502 cm⁻¹) is direct signature of occurrence of protonation in pyridine units; formation of pyridine- Au³⁺ complex, in agreement with previous studies.^[30] It is worth noting that the 1601 cm⁻¹ band of pure PS-*b*-P4VP is slightly shifted towards higher energy (1604 cm⁻¹), confirming that coordination bonds have

formed after the complexation process. Metal particles have been reported to interact with P4VP to give a peak at the $400 - 500 \text{ cm}^{-1}$ region.^[50] The absorbance at $\sim 439 \text{ cm}^{-1}$ (see Figure 4.20) can be considered to be due to the interaction between the Au nanoparticles and P4VP.

Figure 4.20: Comparison of the IR-spectra of the block copolymer PS-*b*-P4VP filled with stoichiometric amounts of HAuCl_4 and after reduction to Au nanoparticles. The molar ratio of Au^{3+} :P4VP is 0.2.

The oxidation state of the Au nanoparticles was confirmed through X-ray photoelectron spectroscopy (XPS). The XPS measurement was done by Kratos AXIS spectrometer (UK) with the monochromatic Al K α radiation source (1486.6 eV photons, 150 W). The base vacuum in XPS analysis chamber was about 1×10^{-9} torr. All spectra were calibrated using C1s at 284.6 eV as a reference.

Figure 4.21: (a) XPS spectra of PS-*b*-(P4VP/AuNPs) showing the high resolution scan of Au 4f_{7/2} and 4f_{5/2} doublet with binding energies of 83.7 eV and 87.4 eV respectively. (b) N 1s XPS spectra of the pure PS-*b*-P4VP and PS-*b*-(P4VP/AuNPs) composites (Au³⁺: P4VP = 0.2).

The binding energies of the doublet for Au 4f_{7/2} (83.7 eV) and 4f_{5/2} (87.4 eV) are characteristics of Au⁰, indicating the presence of elemental Au only [Figure 4.21(a)].

There is no peaks observed at 90.1 eV and 86.4 eV corresponding to Au^{3+} , hence one can conclude that the Au salts become metallic Au after the reduction process. Figure 4.21(b) displays the N 1s high resolution XPS spectra of the pure PS-*b*-P4VP and the PS-*b*-(P4VP/AuNPs) composite. The N1s signal of the pure PS-*b*-P4VP presented a peak at 399.1 eV which corresponds to the aromatic N ring of the pyridine unit. The PS-*b*-(P4VP/AuNPs) composite exhibited an additional peak at 400.6 eV, indicative of the interaction between the pyridine groups and the metallic Au nanoparticle surfaces. This new peak at higher energy means that lower electron density of the nitrogen atom in the reaction product. The lowliness should come from the interaction between the pyridine groups and the metallic Au nanoparticle surfaces.^[51]

4.3.2.4 Electrochemical studies

Cyclic voltammetry has been recognized as an important technique for measuring bandgaps, electron affinities and work functions of various conjugated polymers. The oxidation process corresponds to removal of charge from the HOMO energy level whereas the reduction cycle corresponds to electron addition to the LUMO. These values give valuable information on the energy barrier or charge injection efficiency in the fabrication of memory devices. The solid state ionization potential (*IP*) and electron affinity (*EA*) of the polymers were estimated by using the following relations:^[52]

$$[E_{\text{onset}}]^{\text{OX}} = IP - 4.4 \quad (4.2)$$

$$[E_{\text{onset}}]^{\text{red}} = EA - 4.4 \quad (4.3)$$

where $[E_{\text{onset}}]^{\text{OX}}$ and $[E_{\text{onset}}]^{\text{red}}$ are the onset potentials for the oxidation and reduction of polymers versus the reference electrode. The onset potentials were determined from the intersection of the two tangents drawn at the rising current and background charging current of the cyclic voltammograms.

The cyclic voltammograms of PS-*b*-P4VP copolymer, P4VP homopolymer and PS-*b*-(P4VP/AuNPs) copolymer have been measured by coating the thin films on Au/Cr substrates, using the standard three electrode cell. This consisted of the thin film on Au/Cr substrate, a platinum counter electrode and an Ag/AgCl reference electrode. 0.1 M *n*-tetrabutylammonium tetrafluoroborate [(*n*-Bu)₄NBF₄] in anhydrous acetonitrile was used as the electrolyte and the scanning rate was set to 50 mV/sec. All measurements were controlled using Autolab PGSTAT 302 module interfaced to a personal computer.

Figure 4.22: Cyclic voltammograms of P4VP homopolymer and PS-*b*-P4VP block copolymer coated on Au/Cr substrates and using Ag/AgCl as the reference electrode and 0.1 M (*n*-Bu)₄NBF₄/acetonitrile as the electrolyte; the scanning rate was set to 50 mV/sec.

Figure 4.22 depicts the cyclic voltammetry spectra of P4VP homopolymer and PS-*b*-P4VP block copolymer. The electrochemical reduction and oxidation of the thin films of the polymers are stable during repeated scanning and no obvious change of the feature of the cyclic voltammograms is observed. The onset potentials are measured from the spectra and their HOMO and LUMO levels are summarized in Table 4.3. From Table 4.3, it appears that the HOMO and LUMO levels of P4VP homopolymer and PS-*b*-P4VP copolymer to be similar, confirming that the anodic and cathodic peaks in the block copolymer are attributed mainly to the P4VP block.

Table 4.3: HOMO and LUMO levels of P4VP homopolymer and PS-*b*-P4VP copolymer using cyclic voltammetry measurements

Sample	HOMO level	LUMO level
P4VP homopolymer	5.2 ± 0.5 eV	3.5 ± 0.07 eV
PS- <i>b</i> -P4VP copolymer	5.4 ± 0.1 eV	3.6 ± 0.05 eV

Figure 4.23 presents the cyclic voltammograms of PS-*b*-(P4VP/AuNPs) film, which has more positive cathodic potential and more negative anodic potential than that of PS-*b*-P4VP, indicating that the PS-*b*-(P4VP/AuNPs) film has better electrocatalytic activity.^[53] There is the effect of decreasing the onset oxidation potential and increasing the onset reduction potential ($[E_{onset}]^{OX} = 0.48$ V and $[E_{onset}]^{red} = -0.85$ V vs Ag/AgCl). This can be ascribed to the transfer of electrons from the P4VP unit to the Au nanoparticles (*i.e.* removal of electrons from P4VP has the effect of lowering the oxidation potential and increasing the reduction potential). It was noted that the oxidation and reduction peak currents from PS-*b*-(P4VP/AuNPs) were both about 0.5 mA, which dropped significantly in comparison with that of PS-*b*-P4VP film.

Figure 4.23: Cyclic voltammograms of PS-*b*-(P4VP/AuNPs) copolymer coated on Au/Cr substrates and using Ag/AgCl as the reference electrode and 0.1 M (n-Bu)₄NBF₄/acetonitrile as the electrolyte; the scanning rate was set to 50 mV/sec. The molar ratio of Au³⁺:P4VP is 0.1.

4.4 Electrical properties and memory characteristics of capacitors based on PS-*b*-(P4VP/AuNPs)

4.4.1 Device fabrication

The memory device used in this study has a MIS structure (see Figure 4.24) which has a metal (Au) gate electrode and a *n*-type silicon substrate, with either a 4.5 nm or 100 nm thermally grown silicon dioxide (SiO₂) on top. A 30 nm thick micellar film of self-assembled PS-*b*-P4VP or 50 nm thick micellar film of self-assembled PS-*b*-P4VP with Au nanoparticles was spun coat on top of the SiO₂-silicon substrates. After spin-coating, the copolymer film was annealed at 110 °C in vacuum for 72 hours. A top metal electrode of gold was subsequently deposited by thermal evaporation means through a shadow mask of 0.3 mm diameter size. The substrate backside was coated with a layer of gold after removing the backside oxide to form an ohmic contact.

Figure 4.24: Device Structure of metal-insulator-semiconductor (MIS) structure.

4.4.2 Dielectric properties

The development of polymer-based composites utilizing quasispherical particles was reported to have a high dielectric constant.^[54-56] Murugaraj *et al.*^[55] achieved high dielectric constants in a polymer composite employing conductive particles by increasing the particle volume fraction close to but not exceeding the percolation threshold within the polymer medium. Such a heterostructure of conductive particles separated by thin insulating polymer films can be considered as a cascade of capacitors connected in series and parallel operating through space-charge polarization. Each nanoparticle dipole is recognized as behaving like a basic harmonic oscillator or dipole with a relaxation frequency.^[57] In this section, we discuss and compare the permittivity of the pure copolymer and copolymer containing Au nanoparticles, and their frequency dependencies.

The frequency dependencies of dielectric constants are plotted in Figure 4.25. The control sample of pure PS-*b*-P4VP exhibits relatively little frequency dependence on silicon substrate. The slightly higher values of dielectric constant at low frequencies can be attributed to molecular polarization of the asymmetric pyridine group in the copolymer. At high frequencies, since these groups cannot maintain the alignment in the alternating field, only electronic polarization exists: It was reported by Meunier and coworkers^[58] that chemical defects such as conjugated carbon double bonds (C=C)) or nitro group (C=N) in a polymer film can create a trap site that captures an electric charge carrier. These chemical defects have inherent (permanent) dipole moments that form an electric potential well to capture surface charges /charge carriers. But the

trapping depth of chemical defects contained in the polymer is not sufficiently deep to capture the charge carriers permanently.^[59]

Figure 4.25: Dielectric constants of the two samples with and without Au nanoparticles.

The sample with Au nanoparticles exhibits a frequency enhancement of dielectric constant ϵ . Relative to the control sample, the PS-*b*-(P4VP/AuNPs) sample shows approximately 1.5 times higher in the dielectric constant. The dielectric constant also increases as the concentration of the Au nanoparticles increase. One possible explanation for the frequency dependent nature of this permittivity increase is due to space charge polarization at the nanoparticle:dielectric interfaces. At the influence of electric field, the trap levels in the Au nanoparticles are deep enough to trap the charge carriers, resulting in space charge formation in the nanocomposite.^[60] The charge accumulation at the nanoparticle and/or its interfaces will produce an increase in capacitance which is most prominent at lower frequencies. Hence, as the concentration of Au nanoparticles increase, higher capacitance (and hence dielectric constant) occurs.

Another contributing factor is the effect of induced dipoles, created by the Au nanoparticles. Electrical potential well is produced by an induced electric dipole of

nanoparticles subjected to a dc electric field. Because Au has a relatively higher dielectric constant than P4VP, and the size of the Au nanoparticles is on the order of 10 nm, the depth and extent of the effect of potential wells formed by these particles are expected to be very large. As such, the induced dipole polarization will affect the overall permittivity. Hence, the observed decrease in dielectric constant at higher frequencies is most likely to be due to relaxation in dipole polarization.

In summary, space charge polarization can be used to account for the i) increase in dielectric constant at lower frequencies and ii) increase in dielectric constant as the concentration of Au nanoparticles increase, while the decrease in dielectric constant at higher frequencies is mostly likely due to the dipole polarization.

4.4.3 Memory characteristics and charge trapping

Figure 4.26 depicts the shift in V_{FB} for the MIS structure with PS-*b*-(P4VP/AuNPs) film (ΔV_{FB} of -0.19 V) for 0.1 molar ratio of HAuCl₄ per P4VP unit. This hysteresis window indicates a charge trapping effect while the negative shift in V_{FB} implies that holes are predominantly trapped while double sweeping the device within the ± 3 V range. The magnitude of ΔV_{FB} was dependent on the voltage sweeping range; with the memory window increasing from -0.19 to -0.68 V when sweeping range amplitude was increased from ± 3 to ± 5 V, indicating an increased charge injection. Since the MIS control sample displayed an absence of charge trapping effect (see Figure 4.10), the origin of charge trapping in the PS-*b*-(P4VP/AuNPs) MIS structures is attributed to the Au nanoparticles and/or interface states between the nanoparticles and P4VP units. The charge transport between Au nanoparticles via the block copolymer nanodomains has been observed to be a tunneling process (section 4.2.2). Tunneling phenomena between nanoparticles and polymer has also been observed by many others.^[61-63] These experimental results suggest that, under the influence of a positive voltage applied to the top gold electrode, holes can be injected and stored in the Au nanoparticles and/or their interface states by a tunneling process through the PS and P4VP layer. When the

voltage is swept to a negative value, from +3 to -3 V, electron trapping will occur in the Au nanoparticles, resulting in the shift in capacitance characteristics.

Figure 4.26: Double sweeping C - V characteristics at 100 kHz on MIS structure with PS- b -(P4VP/AuNPs) film. The C - V hysteresis window increases from -0.19 V to -0.34 V and to -0.68 V upon increasing the operation bias from ± 3 V to ± 4 V and to ± 5 V respectively. The molar ratio of Au^{3+} : P4VP is 0.1.

We have also measured the current-voltage (J - V) characteristics of a diode device; Au electrode/PS- b -P4VP/(AuNPs)/Al electrode (presented in Appendix E) with the reverse scan included. The J - V characteristics displays a shift in threshold voltages, V_t , measured by scanning the potential from +10V to -10V and reverse, indicating the occurrence of charge injection. This is because when electrons or holes are injected and stored into the Au nanoparticles, the stored charge will “screen” the applied electric field and cause the shift of V_t . Such phenomenon has already been reported in silicon based memory devices.^[64] This also shows that our memory mechanism is different from the bistable memory approach where high / low conductive states are employed.

The charge density Q accumulated in the Au nanoparticles can be estimated^[37] from $Q \approx C_i \Delta V_{FB}$, where C_i is the capacitance value of the dielectric stack layer. For instance, the voltage shift of -0.19 V at a ± 3 V sweep corresponds to a hole charge density of

$9.07 \times 10^{10} \text{ cm}^{-2}$. Using $2.61 \times 10^{10} \text{ cm}^{-2}$ as the density of the gold nanoparticles, one can estimate the average charge per Au nanoparticle for the given system to be around 3 holes per Au nanoparticle. This is comparable to existing few-electron memory devices which use Au nanocrystals embedded in a silicon dioxide matrix.^[65, 66]

Next, the charging kinetics in PS-*b*-(P4VP/AuNPs) thin film were evaluated by applying a voltage pulse at the top Au electrode (defined as “gate”, V_{gate}) and subsequently monitoring the resultant shift of the C - V characteristics or change in the flatband voltage (V_{FB}). Both positive and negative charge trapping in the Au nanoparticles may be realized, determined by the polarity of pulse voltage. Figure 4.27(a) presents the resulting shift of the C - V curves after the application of a +5 V pulse voltage for various charging time (ranging from 1 ms to 1 s) for the highest Au nanoparticle concentration experimented (0.3 molar ratio of HAuCl₄ per P4VP unit). The observed negative shift in V_{FB} reflects a net positive charge in the system which is attributed to hole injection into the confined states of the Au nanoparticles and/or its interface states. A short charging time of 1 ms is sufficient to observe an appreciable shift in the ΔV_{FB} (-0.2 V). On the other hand, under a -5 V pulse, electron injection from the Au gate electrode into the Au nanoparticles effects a positive V_{FB} shift [Figure 4.27(b)].

The relationship between the change in V_{FB} , the magnitude/polarity of pulse voltage and charging times (t) are summarized in Figures 4.27(c) and (d). In general, both hole and electron trapping events increased with increasing pulse voltage and/or t , indicating increasing charge injection. Two distinct features are noticeable: 1) For same magnitude of pulse voltage, the ΔV_{FB} due to electron trapping is lesser as compared to the ΔV_{FB} due to hole trapping. 2) Hole trapping in Au nanoparticles can occur in a much shorter time (in the range of milliseconds) as compared to electron trapping (in the range of seconds). Such differences may be related to chemical or physical properties of the nanoparticles, and/or due to the variations in energy barrier between the metal electrode and highest occupied molecular orbital (HOMO)/ lowest unoccupied molecular orbital (LUMO) levels of P4VP.

Figure 4.27: Dependence of C - V characteristics on cumulative charging time (t), for voltage sweeping range of $\pm 2\text{V}$, under (a) Pulse voltage = +5V, $t = 0, 1, 10, 100, 500$ ms and 1s, and (b) Pulse voltage = -5V, $t = 0, 1, 2, 3, 5, 8$ and 10s. C - V curve shifts from right to left with increasing t for (a) while C - V curve shifts from left to right with increasing t for (b). ΔV_{FB} as a function of charging time for (c) positive and (d) negative pulse voltages.

We first postulated the reason for smaller ΔV_{FB} due to electron trapping to be due to the higher electron injection barrier (i.e. LUMO level of P4VP is around 3.6 eV using cyclic voltammetry; section 4.3.2.4, while the work function of top gold electrode is around 5.1 eV) which in turn leads to a reduced electron tunneling probability.^[67] The effect of the higher electron tunneling barrier was also observed in the retention studies (Figure 4.28) where the loss rate of electrons is lower than that of holes (i.e. HOMO

level of P4VP is around 5.2 eV). This is because a higher electron tunneling barrier will also means the energy barrier height seen by the trapped electrons inside the Au nanoparticle to be higher. In order to better understand the kinetics for the trapping phenomena, the carrier transport mechanism was investigated in the following section.

Figure 4.28: ΔV_{FB} as a function of time for MIS memory device after hole trapping (Pulse voltage = +5V, $t = 1$ s and after electron trapping (Pulse voltage = -7V, $t = 10$ s).

4.4.4 Charge transport mechanism

In analyzing the negative voltage range, two regions of electronic transport through Au nanoparticles in PS-*b*-P4VP copolymer: electrode-limited followed by bulk limited transport are observed. Figure 4.29(a) depicts a comparison of J - V characteristics between a pure PS-*b*-P4VP thin film and PS-*b*-P4VP thin film containing Au nanoparticles in the applied negative gate voltage (V_g) up to the range of 6V (1.09 MV/cm). At low applied voltage ($V_g < -0.5$ V), the current is oxide limited and band bending in the block copolymer is rather small. When the applied voltage increases, the current increment corresponds mainly to charge transport in the PS-*b*-P4VP film or through the Au nanoparticles. In the voltage range, -1.2 V $< V_g < -2$ V (electric field range of 0.2-0.4 MV/cm), $\ln(J/T^2)$ versus $E^{1/2}$ yields a linear dependence at

temperatures of 300 K – 343 K. This fits well with the Schottky emission theory^[68] and a barrier height of 0.72 eV is determined [inset of Figure 4.29(a)]. This value is half that of the theoretical barrier height of 1.5 eV between the Au electrode and P4VP (P4VP LUMO is determined to be ≈ 3.6 eV; work function of Au ≈ 5.1 eV). This could possibly be attributed to the reduction in effective Schottky barrier height due to electrostatic charging of the Au nanoparticles.^[69] With a further increase in the applied voltage ($-2 \text{ V} < V_g < -6 \text{ V}$), the J - V relation of the Au nanoparticles in PS-*b*-P4VP film changes and can be described by a power-law relationship similar to the model of collective charge transport in arrays of metallic quantum dots separated by tunnel barriers.^[34, 70] The Au nanoparticles may be treated as capacitively coupled conductors and charges are able to tunnel between the neighboring nanoparticles, with $I \sim (V - V_T)^\zeta$, where V_T is the threshold voltage (onset of conduction), and ζ is a scaling exponent. Note that V_T is approximately zero for the room temperature measurement. The scaling exponent ζ can be regarded as the dimensionality for collective electron transport in an array of nanoparticles. The scaling exponent ζ , determined to be 1.43, indicates that the current conduction is a quasi-two-dimensional transport; in agreement with a previous report in the literature.^[34] On the other hand, the control PS-*b*-P4VP device yields a scaling exponent ζ of ~ 1.08 which is close to one-dimensional transport. The scenario for the memory device is likely to be that there are both one- and two-dimensional tunneling paths – charge carriers can tunnel through the intrinsic P4VP nanodomains as well as the Au nanoparticles which provide additional tunneling paths, and as a result, the current conduction in the thin film is greatly enhanced.

Figure 4.29: J - V characteristics of PS-*b*-(P4VP/AuNPs) memory and control PS-*b*-P4VP capacitor for (a) $V_g < 0V$; inset shows the Schottky emission plot of $\ln(J/T^2)$ vs. $E^{1/2}$ for 300-343 K for memory capacitor. The curve fitting is performed in the field of 0.2 – 0.35 MV/cm. (b) $V_g > 0V$; inset shows $T = 300 - 343$ K range. The corresponding band diagrams under applied bias are also illustrated. Electrons and holes are represented by solid and open circles respectively.

For a positive voltage range ($V_g = 0$ to +6 V applied to top Au gate), a much higher current density is observed [Figure 4.29(b)], indicating that charge carriers readily enter the block copolymer. At low electric field, there is weak temperature dependence from 300 K to 343 K [inset of Figure 4.29(b)] and hence direct tunneling of holes through the PS and P4VP layer into the Au nanoparticles is likely to occur.^[71] At

higher electric fields ($1 < V_g < 6$ V), collective charge transport in PS-*b*-P4VP and PS-*b*-(P4VP/AuNPs) thin films with similar dimensionality of 0.86 and 1.46 respectively were again observed, indicating an intrinsic quasi-two-dimensional transport of the system.

From the C - V and J - V characteristics, we can conclude that the reduced electron injection and trapping (in Au nanoparticles) effect as compared to hole trapping is attributed to the high work function of the Au gate electrode and high electron affinity of P4VP. Hence, a higher electron injection barrier (Schottky barrier) exists and a higher applied voltage will be needed for the generation of a large amount of electrons for injection and trapping events. This factor will be discussed later when a lower work function metal of aluminum (Al) is used as the top gate electrode (see section 4.4.6).

The time required for hole versus electron trapping is discussed next: The flatband shifts as a function of charging time can be seen in Figures 4.27 (c) and (d). A longer charging time is required for electrons trapping as compared to holes trapping. Although the barrier height for electrons is higher, a “writing” time similar to that of holes would be anticipated since the applied gate voltage is well above the threshold voltage (for example, the current conduction through the whole dielectric stack has been measured to be $\sim 10^{-7}$ A/cm² for an electric field of 0.9 MV/cm, corresponding to an applied bias of -5 V). A possible explanation is related to the electron-accepting nature (i.e. high tendency to conduct electrons away) of P4VP,^[72] and hence a sufficiently long charging time is needed to observe appreciable electron trapping in the Au nanoparticles.

4.4.5 Influence of Au loading

The effect of the Au nanoparticle loading on the memory effect has also been studied. For an operating voltage of ± 5 V, it was observed that the C - V hysteresis window widens with an increase in the Au nanoparticle concentration (corresponding to 0.05,

0.1, 0.2, and 0.3 molar ratio of HAuCl_4 per P4VP unit) thus indicating the occurrence of strong carrier trapping with increasing Au concentration (Figure 4.30).

Figure 4.30: Relationship of C - V hysteresis window (ΔV_{FB}) with increasing Au loadings at the operation bias of ± 5 V.

Figure 4.31 summarizes the ΔV_{FB} after the pulsing experiment for various Au nanoparticles loading in the system (0.1, 0.2 and 0.3 molar ratios of HAuCl_4 :P4VP). In general, the hole trapping events increased with increasing pulse voltage and/or Au loadings, indicating increasing charge injection. Electron trapping is more significant for the device using lower concentration of Au nanoparticles. This might be due to the fact that for lower Au nanoparticle concentrations, there is a lesser chance of electron conduction between neighboring Au particles (see inset of Figure 4.31). This was also observed in current-voltage measurements, where enhanced conductivity occurred for higher concentration of Au nanoparticles (Figure 4.32). Li *et al.*^[34] has also recently reported an increase in electron tunneling constant and conductivity with increasing Au nanoparticle concentrations in PS-*b*-P4VP which is due to a decrease in interparticle distances.

Figure 4.31: Flat band voltage shift as a function of different (a) positive pulse voltages at a charging time of 500 ms, and (b) negative pulse voltages at a charging time of 2 s for various Au concentrations (0.1, 0.2 and 0.3 molar ratios of HAuCl_4 :P4VP). The voltage bias is applied from the top Au electrode. The inset shows a schematic illustration of electron conduction through the Au nanoparticles as the Au loading inside a P4VP core increases.

Figure 4.32: Current density–voltage (J - V) characteristics of the MIS device using various concentrations of Au nanoparticles in PS-*b*-P4VP (HAuCl₄/P4VP molar ratios of 0.1, 0.2 and 0.3). An increase in conductivity is observed as the concentration of Au nanoparticles in PS-*b*-P4VP increases.

4.4.6 AC conductance characteristics

Besides using C - V characteristics to evaluate the charge trapping characteristics, information can also be obtained from conductance-voltage (G - V) characteristics. As shown in Figure 4.33(a), a decrease in the conductance peak (G_{max}) is observed after a positive pulse voltage is applied. This suggests the occurrence of hole trapping events in the nanoparticles under the influence of positive gate voltage. The increase in trapped holes leads to an increase in the number of charged nanoparticles. These charged nanoparticles will block the conduction of the tunneling paths, and hence the conduction peak is reduced. We can hence evaluate the charge trapping effect using the change in conductance peak (ΔG_{max}). The increase in Au nanoparticles concentration also leads to an increase in ΔG_{max} [Figure 4.33(b)] This is consistent with the change in flatband voltage shown in Figure 4.31(a).

In contrast, as shown in Figure 4.33(c), for the negative voltage stress, there are no significant changes in the ΔG_{max} . This means no significant charging/discharging of the

gold nanoparticles occurring during the application of a negative gate voltage, which is consistent with the insignificant change in the flatband voltage shown Figure 4.31(b).

Figure 4.33: Dependence of G - V characteristics for voltage sweeping range of $\pm 2V$, under (a) Pulse voltage = +5V for a charging time of 500 ms, (b) ΔG_{max} as a function of positive pulse voltages for a charging time of 500 ms for various Au concentrations. Dependence of G - V characteristics for voltage sweeping range of $\pm 2V$, under (c) Pulse voltage = -5V for a charging time of 2 s. (d) ΔG_{max} as a function of negative pulse voltages for a charging time of 2 s for various Au concentrations. The molar ratio of $HAuCl_4$: P4VP is in (a) and (c) is 0.1. For (b) and (d), the various Au nanoparticle concentrations are 0.1, 0.2 and 0.3 molar ratios of $HAuCl_4$:P4VP.

4.4.7 Influence of electrode work function

High electron affinity polymers and low work function metals have been used to achieve efficient electron injection in devices such as light-emitting diodes.^[73] Thus to validate the Schottky barrier effects, discussed in a previous section 4.4.4, devices with Al as the top gate electrode (work function ≈ 4.3 eV) were fabricated. The ΔV_{FB} corresponding to electron trapping significantly increased with the use of Al gate [Figure 4.34(a)], however the timescale for charging time did not show any appreciable differences. The unchanged charging time lends further support to the theory that the electron-accepting nature of P4VP contributes to the longer electron writing time. The higher ΔV_{FB} of 0.34V for Al compared with a value of 0.04 V for Au (pulse voltage = -6 V, $t = 5$ s,) also leads credence to the Schottky barrier observations detailed in previous sections. The current level of Al gate capacitor is higher than the Au gate capacitor, further implying that the barrier between Al and P4VP is smaller than that between Au and P4VP under the same electric field [inset of Figure 4.34(a)]. The role of metal gate is also readily observed for hole trapping effect, with Al yielding a much reduced V_{FB} compared with that of Au [(Figure 4.34(b)]. This highlights the need for work function engineering in understanding the charging dynamics and hence the memory behavior in the nanoparticle based organic memories. It should be noted that both Au and Al gate capacitors utilizing pure PS-*b*-P4VP (without Au nanoparticles) exhibit hysteresis-free C - V characteristics, thus suggesting that electro-forming or nano-filamentary^[74] effects due to the metal gate electrodes are not a contributing factor in this study.

Figure 4.34: ΔV_{FB} for both Au and Al gated devices for (a) negative pulse voltages, $t = 5$ s and (b) positive pulse voltages, $t = 500$ ms. Insets show the $J-V$ characteristics in negative and positive voltage ranges respectively.

4.4.8 Frequency response

We have also fabricated MIS-based memory devices with 100 nm thermal oxide layer and similar charging response is observed. Next, we show the $G-V$ characteristics and evaluate the effects of the interface traps where frequency-dependent $G-V$ measurements with frequency ranging from 1 kHz to 1 MHz were carried out. We found similar clockwise $C-V$ hysteresis and negligible variation in the conductance peak with frequency [Figure 4.35(a)]. This suggests that the influence of interface traps is minimal or the effect of the nanoparticles is more dominant than that of interface traps. An equivalent circuit as shown in Figure 4.35(c) represents the MIS structure with PS-*b*-(P4VP/AuNPs) and presence of interface traps. It consists of the effective dielectric stack capacitance C_{eff} , the depletion layer capacitance C_D , the capacitance due to charge stored in interface traps C_{it} and gold nanoparticles C_{nc} . Here G_{it} and G_{nc} represent the lossy process of capture-emission of carriers by interface traps and Au nanoparticles.

Since the Au nanoparticles in PS-*b*-P4VP play the major role of charge storage, the equivalent circuit can be simplified further to Figure 4.35(d). Figure 4.35(e) contains

the parallel combination of equivalent conductance, G_p , and capacitance, C_p , derived from the parallel network of Figure 4.35(d). The measured parallel conductance, G_m , and capacitance, C_m , across the two-terminal MIS structure are also indicated in Figure 4.35(f).

Figure 4.35: (a) Frequency-dependent conductance (G_m/ω) characteristics of MIS memory capacitor. The inset shows the corresponding C - V characteristics. (b) Parallel conductance (G_p/ω) versus ω characteristics of the MIS memory capacitor in the depletion region; the curves correspond to different gate bias of 0V, 0.2V, 0.4V and 0.5V. Equivalent circuit diagram of an Au/PS-*b*-(P4VP/AuNPs)/100nm SiO₂/Si MIS capacitor for conductance measurements: (c) MIS capacitor with nanoparticle and interface trap capacitance (C) and conductance (G) components which are represented by the subscripts "nc" and "it" respectively. C_{eff} and R_s are the effective dielectric capacitance and series resistance of the structure, respectively, (d) simplified equivalent circuit of (c) when the effect of nanoparticles is more dominant than that of interface traps, (e) simplified equivalent circuit of (d), (f) the measured circuit.

Using the conductance method^[37] where C - f and G - f measurements were performed as a function of the applied voltage in the depletion region, and the simplified equivalent

circuit model of Figure 4.35(f), the corrected capacitance (C_c) and conductance (G_c) for series resistance (R_s) were evaluated from the relations:

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{\alpha^2 + \omega^2 C_m^2} \quad (4.4)$$

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2) \alpha}{\alpha^2 + \omega^2 C_m^2} \quad (4.5)$$

$$\alpha = G_m - (G_m^2 + \omega^2 C_m^2) R_s \quad (4.6)$$

$$R_s = \frac{G_{acc}}{G_{acc}^2 + \omega C_{acc}^2} \quad (4.7)$$

$$C_{eff} = C_{acc} \left[1 + \left(\frac{G_{acc}}{\omega C_{acc}} \right)^2 \right] \quad (4.8)$$

where C_m and G_m are the measured capacitance and conductance, C_{acc} and G_{acc} are the measured capacitance and conductance in strong accumulation. $\omega=2\pi f$ is the radian frequency. The series resistance is calculated to be in the range of 500 Ω -16 k Ω . These R_s values are used to correct the measured C - V and G - V curves.

The trap conductance, G_p and trap density D_T , were then evaluated from the relations:

$$\frac{G_p}{\omega} = \frac{\omega C_{eff} G_c}{G_c^2 + \omega^2 (C_{eff} - C_c)^2} \quad (4.9)$$

$$D_T = \frac{2.5}{qA} \left(\frac{G_p}{\omega} \right)_{\max} \quad (4.10)$$

where A is the area of the capacitor, q the electron charge, $(G_p/\omega)_{\max}$ is the extracted conductance peak (after correcting for series resistance).

To extract $(G_p/\omega)_{\max}$, we have plotted the parallel conductance (G_p/ω) versus ω characteristics of the MIS memory capacitor in the depletion region [Figure 4.35(b)].

It can then be shown that the density of gold nanoparticles is given by:

$$D_{NP} = \frac{2.5 \left(\frac{G_p}{\omega} \right)_{\max}}{A(4\pi\epsilon_0\epsilon_{Au}r_{NP})} \quad (4.11)$$

where ϵ_0 is the permittivity of free space, ϵ_{Au} is the relative permittivity of Au (can range from 1.3 to 5.6^[75]), and r_{NP} is the radius of a nanoparticle. The term $1/4\pi\epsilon_0\epsilon_{Au}r_{NP}$ in equation 4.11 multiplied by the electronic charge q (i.e. $q/4\pi\epsilon_0\epsilon_{Au}r_{NP}$) represents the surface potential of a nanoparticle, assuming the nanoparticles act like point charges.^[76] The density of Au nanoparticles is hence estimated to be $1.50\text{-}6.46 \times 10^{10} \text{ cm}^{-2}$, which is in good agreement with the value $2.61\text{-}6.67 \times 10^{10} \text{ cm}^{-2}$ obtained in section 4.3.2.2.

4.5 Summary

In summary, this chapter has described a new memory system which is enabled by *in-situ* synthesized Au nanoparticles in self-assembled block copolymer of polystyrene-*b*-poly-4-vinylpyridine (PS-*b*-P4VP). The obvious memory effect of the memory capacitor was demonstrated by the presence of hysteresis in the C - V curves with a stored charge density of up to 10^{10} cm^{-2} . Hole trapping is observed to be more efficient than electron trapping and is attributed to a lower electron injection current (due to presence of Schottky barrier between the Au electrode and P4VP layer). At higher electric fields ($>0.4 \text{ MV/cm}$), quasi-two-dimensional charge transport through the arrays of gold nanoparticles in P4VP nanodomains is observed. The contribution of electrode work function was demonstrated with improved electron charging by the replacement of gold electrode with aluminum. The effects of density of Au nanoparticles to the charge storage and thus the memory characteristics have also been

investigated. Frequency-dependent G - V measurements have enabled the study of trap density, where an equivalent circuit model is proposed and correlates well to the nanoparticle density in the memory system.

4.6 References

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Chapter 5

Organic memory transistors based on discrete self-assembled nanoparticles

5.1 Introduction

In *Chapter 4*, we have demonstrated the charging ability of gold nanoparticles (AuNPs) in a block copolymer system of polystyrene-*block*-poly-4-vinylpyridine (PS-*b*-P4VP). In this approach, high density, uniform and discrete charge storage node arrays of Au nanoparticles in PS-*b*-P4VP nanodomains with an aerial density of more than $6 \times 10^{10} \text{ cm}^{-2}$ and average particle size of $10 \pm 3 \text{ nm}$ are achieved. The block copolymer micelles are an excellent model system and their functionalities provide optimum control over nanoparticle size formation, isolation, and self-assembly which may be leveraged to form a template for the fabrication of a nanocomposite architecture.

5.1.1 Objective

This chapter takes the next step, demonstrating how the process of incorporation of Au nanoparticles in block copolymer gate dielectric can be exploited in designing nano-floating gate organic memory transistors. Figure 5.1 summarizes the block copolymer approach to realizing an organic field-effect transistor (OFET) based memory. Both *p*-type (pentacene) and *n*-type (perfluorinated copper phthalocyanine) OFET based memories are reported, which have stable large charge capacity and programmable-erasable properties due to charge confinement in the embedded Au nanoparticles.

A. *In-situ* synthesis of Gold Nanoparticles in PS-*b*-P4VP block copolymer B. Self-assembling of PS-*b*-(P4VP/AuNPs) on substrate

C. Organic Transistor Floating Gate Memory

Figure 5.1: Schematic illustration of a) micellation process with *in-situ* synthesis of Au nanoparticles in PS-*b*-P4VP block copolymer; PS-*b*-(P4VP/AuNPs), b) the self-assembling of PS-*b*-(P4VP/AuNPs) micellar film on substrate and c) cross-section of an organic field-effect transistor (OFET) using PS-*b*-(P4VP/AuNPs) as floating gate elements.

5.2 Organic MPIS memory

In order to explore the capability of PS-*b*-(P4VP/AuNPs) layer for organic transistor-based memory applications, a capacitor structure comprising a metal-pentacene-insulator-silicon (MPIS) structure, with pentacene as the active semiconductor layer, was first studied. The schematic illustration of the MPIS device is shown in Figure 5.2. Such architecture is an integral part of a typical organic field-effect transistor (OFET) structure, which can therefore be extended to a floating-gate organic memory transistor. Similar to *Chapter 3*, pentacene is used as *p*-channel material in this work since the performance of pentacene-based OFETs now reaches the level of amorphous Si devices,^[1, 2] with energy gap to be about 1.9 eV (HOMO level of ~5 eV and LUMO level of ~3.1 eV).

Figure 5.2: Schematic illustration of metal-pentacene-insulator-silicon (MPIS) memory device employing (PS-*b*-P4VP/AuNPs) as charge storage components. The thickness of control thermal oxide layer is 100 nm.

The MPIS devices were fabricated on *n*-type silicon wafer with 100 nm thermally grown silicon dioxide (SiO₂) on top. A 30 nm thick micellar film of self-assembled PS-*b*-P4VP or 50 nm thick micellar film of self-assembled PS-*b*-P4VP with AuNPs was spun coat on top of the SiO₂-silicon substrate. After spin-coating, the copolymer film was annealed at 110 °C in vacuum for 72 hours. The pentacene was thermally evaporated, at a deposition rate of 0.1 nm/s and a pressure of 10⁻⁷ torr, to form a 45-nm-thick film. Finally, a top metal electrode of gold was subsequently deposited by thermal evaporation means through a shadow mask of 0.3mm diameter size. In this

MPIS device, the gate electrode refers to the heavily doped silicon substrate at the bottom.

5.2.1 Memory characteristics and charge trapping

Figure 5.3(a) presents the C - V characteristics of the MPIS device containing PS-*b*-(P4VP/AuNPs). It can be clearly seen in the C - V curve that the high capacitance of the accumulation region of *p*-type pentacene occurs when negative gate bias is applied and the low capacitance of the depletion regime occurs at positive gate biasing. It is evident that a significant clockwise C - V hysteresis (i.e. net hole trapping) occurs for all operating bias ranges, indicative of clear memory effects. From the relation $Q = C_i \cdot \Delta V_{FB} / A$, where C_i is the capacitance of dielectric stack, ΔV_{FB} is the shift in flatband voltage and A the device area, the shift corresponds to $\sim 1.57 \times 10^{11} \text{ cm}^{-2}$ of holes trapped in the Au nanoparticles with an operating voltage of $\pm 10\text{V}$. Increasing the operating voltages to ± 20 and $\pm 30\text{V}$ cause further shifts in ΔV_{FB} to more negative voltages and hence increase in stored charge density to $\sim 4.61 \times 10^{11}$, and $1.02 \times 10^{12} \text{ cm}^{-2}$ respectively.

Figure 5.3(b) shows the C - V characteristics at various measuring frequencies (50 kHz - 1 MHz) and it is observed that the C - V hysteresis window is independent of the applied frequency. The frequency dependence of interface traps is due to their inability to respond completely at higher frequencies, and the frequency-independent behavior observed here indicates that the interface traps that may exist at the interfaces between the pentacene layer, PS-*b*-P4VP, and the thermal oxide, do not make any contribution to the charging process.^[3] Conductance-voltage (G - V) characteristics are also presented in the inset of Figure 5.3(b) where a single conductance peak is observed in two directions and at all the measured frequency ranges, indicating trapping and de-trapping events of the charge carriers.^[4] In accumulation (negative voltage applied to the bottom silicon substrate), holes may be injected from the pentacene to the AuNPs and/or interface states around the AuNPs via tunneling through the PS block layer.

Figure 5.3: (a) Double sweeping $C-V$ characteristics at 100 kHz on organic memory MPIS device. The hysteresis window increases from 1.0V to 2.6V and to 6.8V upon sweeping the gate voltage from ± 10 , $\pm 20\text{V}$ and $\pm 30\text{V}$ respectively. The inset shows the schematic structure of metal-pentacene-insulator-silicon (MPIS) using PS-*b*-P4VP with Au nanoparticles as floating gate memory elements. The gate voltage is applied to the heavily doped bottom silicon substrate. (b) Frequency-dependent $C-V$ characteristics of the organic memory device. The inset shows the corresponding conductance-voltage ($G-V$) characteristics from 50 kHz to 1 MHz. Molar ratio of HAuCl_4 : P4VP is 0.2.

Control device of pentacene with PS-*b*-P4VP (without AuNPs), did not display any charge trapping behavior, as shown in the inset of Figure 5.3, further confirming that the AuNPs play the major role for charge storage of the holes from pentacene, acting as deep trapping sites. Upon applying a positive bottom gate voltage, the stored

charges in the AuNPs are flushed out, resulting in a flat-band voltage shift. The proposed potential charge transfer mechanism is schematically shown in Figure 5.4.

Figure 5.4: Energy level representation for charge transfer and trapping between pentacene and Au nanoparticle in PS-*b*-P4VP.

Figure 5.5(a) demonstrates the typical high frequency C - V curves of the MPIS memory device under programming and erasing modes. The initial memory device displayed a V_{FB} of -0.5V. When the memory device is pulsed at negative gate voltage ($V_G = -15V$) for 500 ms, defined as a program operation, holes from the pentacene layer tunnel through the PS layer and are trapped in the AuNPs. The resulting C - V curve demonstrates a negative V_{FB} of 2V. Subsequently, the programmed C - V curve is pulsed at $V_G = +30V$ for 500 ms, illustrating an erase operation. The C - V curve revealed a ΔV_{FB} of +0.1V away from the initial one. Note that, there is no shift in the C - V curve when a pulse of positive gate voltage (when depletion of holes in pentacene layer occurs) is first applied on the initial memory device. This indicates the source of holes is the pentacene accumulation layer and there is little influence from interface states and/or mobile ions (if any). The change in flat band voltages under various programming and erasing operations can be defined as logic operation of '1' or '0' for a memory device. For the aforementioned program and erase operations, the memory window attains 2.1V, which is suitable for practical memory applications.

Figure 5.5: C - V curves of the MPIS memory device at 100 kHz after various programming and erasing modes: (a) programming operation is $V_G = -15V$ for 500 ms and erasing operation is $V_G = +30V$ for 500 ms. (b) programming operation is $V_G = -20V$ for 500 ms and erasing operation is $V_G = +40V$ for 500 ms. The gate voltage sweeping range is $\pm 10V$. The molar ratio of Au^{3+} :P4VP is 0.2.

For the erasing operations, it should be noted that we also observed little V_{FB} shift after the erasing operation in some devices within similar voltage pulses. Figure 5.5(b) shows the situation of one sample that did not exhibit significant shifts in V_{FB} after a positive voltage of +40V is applied for 500ms. The same observations have also been made in *Chapter 3* for the citrate-AuNPs system. In erasing operation, the extent of V_{FB}

shift depends on (1) the presence of inducing minority carriers in pentacene and/or (2) the emission of holes from floating gate and from the gate electrode through the control thermal oxide. The first proposed mechanism is difficult to occur since the unipolar (hole-only) nature of the transport across the pentacene and the use of high work function metals prevent efficient electron injection. Moreover, most of the potential drop also occurred in the 100 nm thick control thermal oxide layer. Hence, the emission of holes from the floating gate and from the gate electrode is likely to be the main mechanism. This implies that the “effectiveness” of the applied erasing voltage applied depends on the integrity or “leakiness” of the control thermal oxide and hence, lead to the two different V_{FB} shifts observed in Figure 5.5(a) and (b). For (b), the applied pulse voltage of +40V is the voltage limit of our instrument (HP 4284A LCR analyzer), suggesting that a much higher gate voltage is required to flush out the trapped holes completely.

Figure 5.6: Charge retention characteristics (normalized charge density) after the memory device is programmed at -30V for 500ms. The molar ratio of Au^{3+} :P4VP is 0.2.

In addition to the ability of AuNPs to store charges from the pentacene layer, data retention is of utmost importance for non-volatile memory applications. Possible charge loss mechanisms during retention include vertical charge loss through the

dielectric stack or lateral charge diffusion among the AuNPs. The memory data retention characteristics at room temperature for this nanoparticle floating gate organic memory capacitor are displayed in Figure 5.6. The memory capacitor was first charged for 500ms at a ‘write’ voltage of -30V and the time dependence of the ΔV_{FB} is evaluated by sweeping the gate voltage from +10V to -10V. The measured ΔV_{FB} was then expressed in terms of hole charge density correspondingly. A retention ability of ~92% was observed after 60,000 seconds, confirming that this device has the potential to be considered for non-volatile memory applications. It is believed that the retention ability can be further enhanced by increasing the volume fraction of PS and/or P4VP block to increase the potential energy barrier seen by the trapped charges.

5.2.2 Charge transport

We have also investigated the charge transport through the MPIS memory device. Figure 5.7 shows the current density in both forward and reverse bias. The relatively lower current density in the positive voltage range further proves the low efficiency in erasing operations as seen in section 5.2.1. For the negative gate voltage range, at higher electric fields, an enhanced conductivity is observed and the current rises rapidly. The main transport mechanism has been postulated to be Fowler-Nordheim (F-N) tunneling. The experimental data has been fitted using the F-N plot [inset of Figure 5.7]; using the slope constant of the F-N plot and the effective hole mass in pentacene to be $1.5m_0$ (where m_0 is the free electron mass),^[5] the barrier height is calculated to be 0.085 eV. This is lower than the theoretical barrier height of 0.2 eV (HOMO of pentacene is ≈ 5.0 eV while HOMO of P4VP ≈ 5.2 eV).

Figure 5.7: Current density–voltage (J - V) characteristics of the MPIS device with PS-*b*-(P4VP/AuNPs). The molar ratio of Au^{3+} :P4VP is 0.2. A linear fitting of Fowler-Nordheim (F-N) plot of the MPIS memory structure, where the voltage range from -7.5V to -40V is also presented.

5.2.3 Trap center studied using Deep Level Transient Spectroscopy (DLTS)

As described previously in *Chapter 2*, deep level transient spectroscopy (DLTS) invented by Lang^[6] is a very sensitive technique to detect deep trap levels down to a concentration of around 10^{10} - 10^{11}cm^{-3} , and is normally used to characterize Schottky diodes, thin films and p - n depletion regions. This technique has been very rarely applied to trap characterization in organic materials, except for one report on polycrystalline pentacene film, which shows presence of deep gap states.^[7] Hence, this trap characterization technique remains open for exploration in organic memories. In particular, for nanoparticle based MPIS organic memory device, if the charge emission from the states of nanoparticle is detectable, it is worthwhile to use DLTS for characterization in order to understand the trapping process and the spatial distribution of the memory traps available in the MPIS structure.

In this DLTS experiment, the temperature scans are performed at different rate windows, i.e. period width (T_w) and pulse width (t_p), for survey of trap spectrum. T_w is the period width which is also the observation window. If T_w is reduced, there may not be enough time for traps to emit and there will not be any transient recording and analysis. Organic materials need longer time to react; hence it is necessary to set a longer period width to observe the full spectrum of traps. If the period width is too small, the analysis measured will not paint a full picture of the defect spectrum. The second parameter is t_p , which is the pulse width; the time of application of the chosen forward pulse bias to fill up all the traps. As t_p is increased, the number of traps filled will increase. This will lead to increased emission and a stronger signal detected. A suitable pulse width must be chosen so as to ensure all the traps have been fully occupied. If the value applied is too small, the trap spectrum will not be representative of the original traps present in the device. Each set of chosen T_w and t_p constitute a set of parameters, denoted by T1T, T2T, and T3T in this DLTS experiment.

DLTS scans were run for samples consisting of just the PS-*b*-P4VP copolymer alone and for PS-*b*-(P4VP/AuNPs) in the MPIS structure as depicted in Figure 5.2, using BioRad-DI-8000 digital DLTS system and performed in the 77 – 330K temperature range with variable pulse bias and rate windows. The heating rate was 0.05K/s and the frequency used is 1MHz. Three sets of T_w and t_p parameters have been experimented – T1T(T_{w1} , t_{p1} : 10s, 1 μ s), T2T(T_{w2} , t_{p2} : 3.07s, 1ms) and T3T(T_{w3} , t_{p3} : 6.85s, 100ms). The forward and reverse pulse bias applied to the samples was -2V and 2V respectively.

Figure 5.8(a) presents the DLTS scan for the PS-*b*-(P4VP/AuNPs) based MPIS memory device. Regardless of the rate window used, there is no detrapping of charge carriers observed below temperature of 250K. This indicates the Au nanoparticles are stable charge storage centers, with negligible charge emission from the interfaces states and/or bulk states from pentacene layer. Beyond 250K, the DLTS signal starts to increase. Unfortunately, 330K is the temperature limit in our testing apparatus, the temperature hence could not be raised further to observed the dominant signal and explores the detrapping process. It should be noted that such distinct behavior of DLTS

spectra has been repeated for at least three scans. On the other hand, for the control PS-*b*-P4VP MPIS device [see Figure 5.8(b)], we do not observed such phenomenon and no dominant peaks appear. Instead, a dip in the DLTS signal between 100K and 200K is observed, of which the origin is unclear.

Figure 5.8: Temperature scans of hole trapping in (a) PS-*b*-(P4VP/AuNPs) and (b) control PS-*b*-P4VP in a metal-pentacene-insulator-silicon (MPIS) structure, with pentacene as the active semiconductor layer. The molar ratio of Au^{3+} :P4VP is 0.2. The forward and reverse pulse bias is -2V and 2V respectively. T1T represents T_W of 10s and t_p of 1 μ s, T2T represents T_W of 3.07s and t_p of 1ms and T3T represents T_W of 6.85s, and t_p of 100ms.

Figure 5.9: Temperature scans of hole trapping in a metal-pentacene-SiO₂-silicon structure. The inset shows the corresponding Arrhenius plot. The forward and reverse pulse bias is -2V and 2V respectively. T1T represents T_W of 204.8ms and t_p of 500 μ s, T2T represents T_W of 10.48s and t_p of 1ms and T3T represents T_W of 300.03ms, and t_p of 1ms. τ represents the emission time constant, v_{th} is the thermal velocity while N_v is the effective valence band densities.

We have also conducted DLTS measurements on control device of pentacene on thermal oxide only. As shown in Figure 5.9, the hole trap energy levels of all 3 parameter windows correspond to a mean value of 0.365 eV. This is similar to values cited in literature,^[7, 8] which is around 0.38 eV. This hole trap can be attributed to hydrogen- and oxygen-induced defects.^[9]

In summary, through DLTS, the results provide a clue that the trapping mechanism in the MPIS memory device is related mainly to the Au nanoparticles and the detrapping process occurred above 330K. Besides C - V measurements, DLTS can be a supplementary electrical characterization method to supply information on the trap centers in organic memories.

5.2.4 Stability over time

We have also investigated the stability of the MPIS memory device. Degradation of the memory device can occur due to moisture and oxygen absorption in the pentacene layer, leading to pentacenequinone and anthraquinone. Water can also diffuse into the hydrophilic P4VP cores through the hydrophobic PS-rich coronae because of the hydrogen bonding between P4VP and water, which led to swelling of the P4VP cores.^[10] Figure 5.10 presents the double sweeping C - V characteristics of a fresh device and after 20 months (stored in ambient). There are still memory characteristics in the aged device, with the memory window changing by less than 20% (see inset of Figure 5.9).

Figure 5.10: Comparison of double sweep C - V characteristics at 100 kHz on organic memory MPIS device using PS-b-P4VP with Au nanoparticles between a fresh device and after 20 months. The gate voltage range is ± 30 V. The gate voltage is applied to the heavily doped bottom silicon substrate. The molar ratio of Au^{3+} :P4VP is 0.2.

5.3 Pentacene based p-type memory transistor

Figure 5.11 illustrates the schematic cross-sectional view of the fabricated pentacene based floating-gate memory transistor. This is an extended architecture of the MPIS device studied in earlier sections. The floating-gate memory transistor consists of a block copolymer of PS-*b*-P4VP with Au nanoparticles; PS-*b*-(P4VP/AuNPs), sandwiched between pentacene and a control thermal oxide layer. The channel is hence under the electric field influence of two serial sections; the floating-gate comprising PS-*b*-(P4VP/AuNPs) and the control gate.

Figure 5.11: Schematic cross-section of an organic field-effect transistor (OFET) with *p*-type pentacene and using PS-*b*-P4VP with Au nanoparticles as floating gate memory elements.

5.3.1 Output and transfer characteristics

Typical output and transfer characteristics of the OFET memory device (channel length of 100 μm and width of 1000 μm , Figures 5.12(b) and (c)) indicate reproducible, stable device performance, suggesting that the additional floating gate layer does not interfere with standard OFET performance. The polycrystalline pentacene thin film consists of grain sizes of approximately 0.25 μm [Figure 5.12(a)]. The measured values of the typical hole mobility (μ_{hole}) and on/off ratio ($I_{\text{on/off}}$) were 0.2 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ (maximum of 0.5 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$) and 10^4 – 10^6 respectively. The threshold voltage, V_T , was obtained to be ranging from -3.8V to -4.4V from the x-intercept of the linear portion of the plot of I -

$I_D^{0.5}$ versus V_G . The control transistor utilizing pure PS-*b*-P4VP (without Au nanoparticles) yielded comparable device performance: $\mu_{hole} = 0.1\text{--}0.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, $I_{on/off} = 10^5\text{--}10^6$, and $V_T = -2.7\text{V}$ to -3.3V .

An informative measure of the memory effect is the hysteresis window of the transfer curve upon double sweeping [Figure 5.12(c)]. The anticlockwise I_D - V_G hysteresis loop ($\Delta V_T \approx 7\text{V}$) further indicates that there is a net hole trapping effect. A physical mechanism for the memory effect has been suggested previously in section 5.2.1. Briefly, holding a negative voltage across the gate dielectric (“writing”) during the forward sweep causes the injection of holes from the pentacene to gold nanoparticles. This phenomenon results in a shift in the electrical potential between the gate and semiconductor, and alters the charge distribution in the transistor. The positive charge stored in the Au nanoparticles “screens” the applied electric field and hence the threshold voltage shifts to a higher negative gate voltage during the reverse sweep. These results are consistent with the C - V characteristics observed in MPIS capacitor [inset of Figure 5.12(c)]. The number of stored charges (Δn) can be determined from the shift in V_T according to $\Delta n = (\Delta V_T * C_i / e) = 1.09 \times 10^{12} \text{ cm}^{-2}$, where C_i is the capacitance of the dielectric stack and e is the elementary charge.

Figure 5.12: (a) Pentacene morphology on PS-*b*-(P4VP/AuNPs)/SiO₂ substrate. (b) Output characteristics (I_D versus V_D) of a pentacene based organic field-effect transistor (OFET) memory utilizing PS-*b*-(P4VP/AuNPs). The gate voltage varies between 0V to -40V in steps of 5V. (c) Double sweeping semilog plots of I_D - V_G transfer characteristics of pentacene OFET utilizing PS-*b*-(P4VP/AuNPs) and pure PS-*b*-P4VP (black and blue line respectively). The drain voltage (V_D) is -10V. The channel length and width of transistor are 100 μm and 1000 μm respectively. The inset shows the corresponding double sweeping C - V characteristics of the Au electrode-pentacene-PS-*b*-(P4VP/AuNPs)-100nm SiO₂-silicon structure, measured at frequency of 100 kHz. The molar ratio of Au³⁺:P4VP is 0.1.

One interesting observation is the appearance of staircase response of the drain current at gate voltages higher than $V_G = \sim -22\text{V}$ (Figure 5.13) in the transfer characteristic. The corresponding transconductance is also plotted and appears to oscillate with gate voltage, further highlighting this step-wise behavior (see inset of Figure 5.13). The distance between successive conductance peaks, or the periodicity of the staircase response of drain current, ΔV_g , is on average 2-3V. It should be noted that the transconductance of the reference transistor (employing pure PS-*b*-P4VP without Au nanoparticles) does not exhibit such periodic oscillation behavior (see inset of Figure 5.12 for comparison); the slight variation in the transconductance may be attributed to the influence of increased gate leakage at higher gate electric fields. The oscillating or staircase component is possibly related to direct hole trapping from pentacene channel into the Au nanoparticles. Similar modulation of drain current has been observed in devices with quantum dots.^[11, 12] The relatively large gate voltage of -22V for the first observed hole transfer is most likely due to the low charge carrier density (the initial threshold voltage is around -4V, below which no hole transfer is possible), the relatively large tunneling distance of 5-8nm from pentacene channel through PS and P4VP into the Au nanoparticles and/or the ‘competition’ of hole carriers in the channel which can either flow towards the drain electrode or towards the Au nanoparticles.

Figure 5.13: Transfer characteristics (I_D versus V_G) of the memory device in linear scale. The drain voltage (V_D) is -10V. The inset shows the oscillating transconductance versus gate voltage. The transconductance of the control transistor utilizing pure PS-*b*-P4VP is also plotted for comparison. The channel length and width of the transistor are 100 μm and 1000 μm respectively. The molar ratio of Au^{3+} :P4VP is 0.1.

5.3.2 Programming and erasing characteristics

The performances of the devices as electrically programmable and erasable memory cells were then evaluated. In general, the programming and erasing procedures of such devices consist of the application of voltage pulses of fixed durations. Depending on the polarity of the voltage pulses, holes or electrons can be injected into the floating gate. Such a modulation of the charge in the floating gate modifies the V_T of the memory transistor. During programming or erasing, the source and drain electrodes were grounded. After pulsing, the threshold voltage was determined by monitoring the I_D - V_G transfer characteristics in a specified gate voltage range (+20V to -20V) while the drain potential (V_D) was fixed at -10V. The cell can be defined to be in the programmed state when enough holes are stored on the floating gate to give a ‘high’ V_T level. The erase state exists when trapped holes are flushed out or electrons are stored on the floating gate, resulting in the ‘low’ V_T level. It should be noted that when a

pentacene OFET device was fabricated with pure PS-*b*-P4VP (without Au nanoparticles), no significant shifts in V_T were observed under the same gate bias conditions that were used in the experiments. This device merely exhibited a degradation in OFET properties such as $I_{on/off}$, showing negligible shift in V_T (less than 1V) which may be attributable to bias-stress effects.^[13]

Upon application of a programming voltage ($V_{G,program} = -30V$, 1s), a V_T shift of -6.7V was observed, with a negative shift in the entire transfer curve [Figure 5.14(a)]. The negative gate voltage pulses ($V_{G,program}$) cause negative shifts in V_T indicating holes are injected from pentacene channel into the Au nanoparticles. This V_T shift was retained in subsequent voltage sweeps and increasing V_T shifts could be brought about by increasing $V_{G,program}$ [inset of Figure 5.14(a)], further demonstrating the increasing *programming (writing)* or hole trapping events.

On the other hand, the *erasing* operation could not be brought about even upon the application of a higher positive gate voltage [$V_{G,erase} = +40V$, 30s, Figure 5.14(a)]. Repetitive erasing cycles ($V_{G,erase} = +40V$ to $\sim +80V$, 30 – 300s) also displayed little effect on the programmed state. This may be comprehended on the consideration that the erasing efficiency is largely dependent on the presence of induced minority carriers in the organic semiconductor. The unipolar (hole-only) nature of transport across the pentacene, and the large work function difference between the Au electrode (~ 5.1 eV) and lowest unoccupied molecular orbital (LUMO) level of pentacene (~ 3 eV) prevents efficient electron injection and transport at positive gate voltages. Pentacene also has a large bandgap of ~ 2 eV which makes it hard to generate the electrons in the inversion regime.^[14] Additionally, for $V_G > 0V$, the channel is depleted and the lifted channel potential reduces the effective electric field. Most of the potential drop also occurs in the 100 nm thick control thermal oxide layer.

Application of erasing voltages in excess of ~ 80 V (fields of $> 5MV/cm$) brought about a positive shift in V_T [Figure 5.14(b)]. The positive shift in V_T was accompanied with high gate leakage current implying that the high erasing voltage brought about a

possible breakdown in the dielectric and hence, the erasing operation occurred mainly through high field emission of holes from floating gate and from the gate electrode through the control thermal oxide. Subsequently, the uncharged Au nanoparticles now do not screen (or impede) the tunneling conduction paths (from control gate $\rightarrow$ through PS-*b*-P4VP and/or uncharged Au nanoparticles $\rightarrow$ to Pentacene, as described in Figure 5.15), contributing to the increase in gate current. The effectiveness of this transistor memory is however compromised by the increased leakage currents.

Figure 5.14: Transfer characteristics obtained after different gate pulse conditions for pentacene based OFETs using PS-*b*-(P4VP/AuNPs) as gate dielectric with channel length of 100 μm and channel width of 1000 μm . The gate voltage varies between +20V to -20V while the drain voltage,

V_D is -10V. The transfer characteristic of pristine device, after programming and erasing operations is in black, red and blue curve respectively. a) Programming: $V_G = -30$ V was applied for 1s and erasing: $V_G = +40$ V was applied for 30s. b) Programming: $V_G = -30$ V was applied for 1s and erasing: $V_G = +100$ V was applied for 30s. $V_D = 0$ V during all programming and erasing operations. The gate leakage currents are plotted in dotted lines. The inset shows the shifts in V_T as a function of programming voltage, $V_{G,program}$ at a charging time of 5s. The molar ratio of Au^{3+} :P4VP is 0.1.

Data presented in the prior sections illustrate efficient programming of holes enabled by direct tunneling from the channel to the floating gate. The magnitude of the electric field is limited by the thickness of the control thermal oxide layer (100 nm in this study) and significant interlevel conduction only occurs via high field emission (> 5 MV/cm), making electrical erase impractical at low voltages. Figure 5.15 summarizes the various programming/erasing mechanisms under low and high electric fields. The high erase voltage is likely to degrade cell reliability and may interfere with subsequent read or programming operations. Although thinner control oxides may be utilized to lower the erasing voltages and improve the programming/erasing times, leakage and charge retention is likely to be compromised; necessitating the use of high- k dielectric layers.^[15, 16] In the next section, the approach proposed herein to lower the erasing voltages is by utilization of a photoinduced charge transfer mechanism,^[17-20] i.e. enabling electron injection with the use of light.

Figure 5.15: Energy band diagrams of the pentacene OFET using PS-*b*-(P4VP/AuNPs) at (a) flatband condition, (b,c) low and high electric field programming modes, (d,e) low and high erasing modes. Holes and electrons are represented by open and solid circles respectively. The solid arrows represent the flow of charge carriers.

5.3.3 Optical erasing

Transfer of nonequilibrium photoinduced charges from the organic semiconductor to polymeric dielectric layer and localization of these charges by deep traps in the dielectric^[21] and/or semiconductor-dielectric interface^[17] have been reported. Such devices were shown to be usable as light-controlled memories and as optical switches. But recombination of the charge carriers upon termination of illumination results in poor data retention. Carbon nanotube networks have also been coated with polymers to form optoelectronic memory devices but the memory capability is lost when the nanotubes are separated from the substrate.^[18] To improve charge retention and operating voltage, it has been envisioned that the combination of nanoparticles (charge centers) based organic memories with optically induced charges is a promising strategy^[17, 20] but this approach is still exploratory.

In the present study, the memory devices were illuminated under vacuum (1×10^{-4} torr) using a Xenon lamp. The optical power density of all illumination was fixed to ~ 74.4 mW/cm² using neutral density filters. The light was illuminated from the top side of the device, i.e. opposite side of the bottom gate electrode. The temperature of the device was monitored using a temperature controller to avoid measurement error, which might be induced by the heating of the device during the illumination. Heating during illumination is minimized by positioning the light source far from the sample (~ 18 cm).

Illumination of the memory transistor under a positive gate electric field thus provides a source of electrons for efficient erasing operations, as illustrated in Figure 5.16 which displays transfer characteristics after programming ($V_G = -25$ V for 1 s) and illumination assisted erasing ($V_G = +20$ V, 30 s) resulting in a shift of the dark transconductance characteristics toward lower V_G . It should be noted that all the transfer characteristic measurements were done in the dark in order to exclude the effect of accumulation of photoelectrons under the source electrode.^[22]

Figure 5.16: Semilog plots of transconductance characteristics of a pentacene OFET memory device, measured at a fixed $V_D = -20V$ in the dark, after programming operation (red line, $V_G = -25V$ for 1s) and after illumination of the device with white light (intensity = 75 mW/cm^2) for 30 seconds. During illumination, a positive gate voltage of $+20V$ (blue dash line) and $+40V$ (blue solid line) is applied. The channel width and length are $4000 \mu\text{m}$ and $75 \mu\text{m}$ respectively. The molar ratio of $\text{Au}^{3+}:\text{P4VP}$ is 0.1.

The explanations on the observed optical memory behavior that involves the charge exchange between the Au nanoparticles and pentacene or gate electrode are described hereafter. First, upon illumination, photoexcitation results in the generation of photoinduced charge carriers (electrons and holes). With the application of a positive electric field at the semiconductor-dielectric interface during illumination, the electron-hole pairs are separated; electrons are transferred and trapped into the Au nanoparticles and/or interfaces between pentacene-PS-*b*-P4VP. Upon switching off the photoexcitation, the OFET memory displays a characteristic governed by the stored charges in the Au nanoparticles. These stored electrons in the Au nanoparticles effectively provide a built-in potential across the channel, leading to an effective shift in V_T . It is also observed that higher positive gate voltages under illumination produced greater threshold voltage shifts since more electrons are transferred to pentacene and trapped into the Au nanoparticles and/or its interfaces. This effect is consistent with a model proposed in the literature wherein the gate electric field assists in the transfer of

charge.^[21] Figure 5.16 also illustrates the increase in threshold shift and drain current after a higher positive gate voltage of +40V is used while the OFET is illuminated. It should be noted that the significant difference in the current output at electrical programming and optical erasing modes for $V_G = 0V$ (~ 4 orders of magnitude) allow us to reliably probe the state of the memory system. This is because a reading voltage of $V_G < 0V$ will otherwise modify the system during the retention studies; a long retention ability will have to be compromised since de-trapping events can occur under the influence of a negative gate electric field.

The high conductance state induced by the optical erasing can be switched back to the 'programmed' or low conductance state using a single pulse of negative gate voltage [Figure 5.17(a)]. When a negative pulse gate voltage is applied, the channel is in accumulation mode and provides the necessary holes to recombine with the trapped electrons. The negative gate field can also assist in the detrapping process of electrons. The transistor thus can be switched between high and low conductance states repeatedly. Figure 5.17(b) presents a series of program/erase cycles where a writing gate voltage of -40V was applied for 5s, or an erasing voltage of +40V under illumination is applied for 30s, keeping the drain voltage grounded. The drain current is then observed at a gate bias of -10V and drain voltage of -20V. After the writing state, holes are trapped in the Au nanoparticles, giving a low drain current, indicating the "OFF" state of the transistor. Whereas after the erasing state, a considerably high drain current is observed and gives the "ON" state. Hence, the responsivity of this OFET memory device can be controlled using a combination of the gate voltage and the incident light source to perform the write, store and erase operations.

Figure 5.17: (a) Time responses of the drain current at $V_G = -5V$ and $V_D = -20V$, after programming ($V_G = -40V$ for 5s) or optical erasing operation (under illumination and $V_G = +40V$ for 30s). (b) Dynamic responses of the electrical programming and optical erasing of the pentacene OFET memory device at $V_G = -10V$, $V_D = -20V$. Light was turned on for 30s and a positive gate voltage of +40V was applied during the illumination. A negative gate voltage pulse (-40V for 5s) was applied to switch the transistor to OFF state. The channel width and length are 4000 μm and 75 μm respectively. The molar ratio of Au^{3+} :P4VP is 0.1.

To sort out the photoinduced charging effects on the Au nanoparticles and the relationship with pentacene-dielectric interaction, we studied the transient response. Figure 5.18 compares the transient response of the drain current after the illumination for the memory transistor and the reference devices. For the memory transistor, a more gradual reduction of the I_D over a period of 100 seconds is observed. This behavior is consistent with our previous explanations. The photogenerated electrons have remained trapped in the Au nanoparticles, providing a built-in potential and hence defining the channel conductance even in the absence of a gate bias. A similar effect in rubrene single-crystal transistors conclusively demonstrated the link between the reduced rate of recombination of carriers and presence of electron traps.^[23] Unlike the memory transistor, the I_D decayed rapidly for the reference devices after switching off the light source, as any trapped electrons at the interfaces will escape and recombine. This fast decay of I_D we observed in reference devices is consistent with results previously observed in both pentacene and regioregular poly(3-hexylthiophene) thin film transistors.^[20, 24]

Figure 5.18: Time response of the normalized drain current at $V_G = 0\text{V}$, $V_D = -20\text{V}$ for memory and reference devices; pentacene OFET using PS-b-(P4VP/Au nanoparticles), pentacene OFET using pure PS-b-P4VP (without Au nanoparticles) and pentacene OFET using control thermal oxide (100nm) only. The normalization is done with respect to highest drain current observed in each device. The molar ratio of Au^{3+} :P4VP is 0.1.

5.3.4 Retention characteristics

Figure 5.19 shows a longer timescale observation of individual ON and OFF devices. Both the on and off current states were measured at time intervals of 10s in the dark after applying a programming and erasing bias of $V_G = -25\text{V}$ for 5s and $V_G = 40\text{V}$ for 30s (under illumination) respectively. In the initial OFF state, the current decreases slightly, suggesting that the reading gate voltage of -10V is sufficient to ‘write’ the memory device. After which the drain current starts to increase gradually. This shows that the trapped holes are slowly discharged from the gold nanoparticles. In the ON state, a gradual discharge of the trapped electrons over 1000 seconds is also observed. The time required for the ratio between ON-current and OFF-current state to decrease to one-order magnitude difference was estimated to be more than 50,000 seconds by extrapolation of the ON-current and OFF-current state curves.

Figure 5.19: Time responses of the drain current at $V_G = -10\text{V}$ and $V_D = -20\text{V}$, after programming ($V_G = -25\text{V}$ for 5s) or erasing (under light illumination and $V_G = +40\text{V}$ for 30s) operation for a pentacene OFET using PS-*b*-(P4VP/AuNPs). The channel width and length are $4000\text{ }\mu\text{m}$ and $125\text{ }\mu\text{m}$ respectively. The molar ratio of Au^{3+} :P4VP is 0.1.

In summary, we have demonstrated an OFET memory device where *in-situ* synthesized Au nanoparticles in block copolymer nanodomains successfully functioned as charge storage elements. The unipolar nature of transport across the pentacene and the use of high work function Au electrode prevent efficient electron injection. To improve electron injection, we have utilized optical excitation to induce photogenerated electrons for the erasing operation. Information can hence be introduced and read electrically, and erased optically. Figure 5.20 summarizes the various mechanisms that occurred with programming and erasing operations.

Figure 5.20: Schematic of memory transistor under various operations

5.4 F₁₆CuPc based n-type memory transistor

Till now, we have extensively proved the memory capability of PS-*b*-(P4VP/AuNPs) in *p*-type pentacene transistors, where charge carriers of holes are being trapped in the AuNPs. In this section, we report *n*-channel based organic memory transistor. *n*-type materials typically have LUMO levels between -3 and -4 eV and usually have better contact with low work function metals such as calcium and lithium, but these metals are highly reactive in air.^[25] In this work, we employed hexadecafluorophthalocyaninatocopper (F₁₆CuPc) which is a promising *n*-type semiconducting material proposed by Bao *et al.*^[26] This *n*-type molecule exhibits high thermal and chemical stability and excellent crystalline quality. Moreover, the LUMO of F₁₆CuPc is -4.8 eV, which is well aligned with the work function of the gold electrode (-5.1 eV) for efficient electron injection.

Figure 5.21: Schematic cross-section of an organic field-effect transistor (OFET) with *n*-type hexadecafluorophthalocyaninatocopper (F₁₆CuPc) and using PS-*b*-P4VP with Au nanoparticles as floating gate memory elements. The simplified energy band diagram of Au electrode/F₁₆CuPc/floating gate is also presented.

Figure 5.21 shows the schematic cross-section of the fabricated *n*-channel memory transistor. F₁₆CuPc was purchased from Sigma Aldrich Company and used without purification. A heavily doped *n*-type Si wafer with 50nm thick SiO₂ layer was used as the gate electrode. Similar device fabrication procedures as described in section 5.2 have been used. Under a base pressure of 5×10^{-7} torr, thin film of F₁₆CuPc (~40nm thick) was deposited. As illustrated in the energy band diagram in Figure 5.20, one would expect that the injection of electrons from gold electrode into LUMO level of F₁₆CuPc and into the floating gate to be possible.

5.4.1 Output and transfer characteristics

Figure 5.22(a) shows the output characteristics in electron accumulation, clearly showing the linear and saturation region. The drain current (I_D) characteristics curves as a function of gate voltage (V_G) are shown in Figure 5.22(b). The I_{DS} increased as V_G increased, indicating typical *n*-type operative characteristics. The surface image of F₁₆CuPc thin film is shown in the inset of Figure 5.22(b), which has an average grain size of 186 nm and surface roughness of 4.68 nm. The electron mobility and on/off ratio are determined to be $0.005 - 0.007 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $10^3 - 10^4$ respectively. These performance parameters are on par with literature reports.^[26, 27]

Figure 5.22: (a) Output characteristics (I_D versus V_D) with channel length of 150 μm and channel width of 500 μm . The gate voltage varies between 0V to 20V in steps of 5V. (b) Double sweeping semilog plots of I_D - V_G transfer characteristics of $F_{16}CuPc$ OFET transistor utilizing PS-*b*-(P4VP/AuNPs). The drain voltage is at +5V. The gate voltage sweeping range increases from +20V (blue line) to +30V (red line) and to +40V (black line). The molar ratio of Au^{3+} :P4VP is 0.25. The inset shows the surface image of $F_{16}CuPc$ thin film which has an average grain size of 186 nm.

The $I_{DS}-V_G$ characteristics of the memory transistor measured with a narrow gate bias sweep (between -5V to 20V) showed no hysteresis. The observed non-hysteresis curve indicates that the charges are not programmed to the Au nanoparticles under a narrow V_G range. An increase in gate voltage to 40V induced a lateral shift of I_D-V_G curve with clockwise hysteresis. This is a typical memory behavior of a floating gate memory and the observed clockwise hysteresis loop indicates that the memory characteristics originate from the tunneling of the charge carriers from $F_{16}CuPc$ channel into the Au nanoparticles and that charge confinement in the Au nanoparticles occurred. During the forward positive gate voltage sweeping, injection of electrons from the $F_{16}CuPc$ to Au nanoparticles occurred. The energy levels, as depicted in Figure 5.23, correlates well with this electron injection process. The negative charge stored in the Au nanoparticles effectively “screens” the applied electric field and hence the threshold voltage shifts to a higher positive voltage during the reverse sweep. The amount of electrons stored in these Au nanoparticles can be estimated by the relation $\Delta V_T = Q/C_i$, where Q is the total charge stored, C_i is the capacitance of the dielectric stack. At the operating voltage of +40V, the amount of stored charges is estimated to be $5.65 \times 10^{11} \text{ cm}^{-2}$ (with ΔV_T to be $\sim 3\text{V}$).

Figure 5.23: Energy level representation for charge transfer and trapping between $F_{16}CuPc$ and Au nanoparticle in PS-*b*-P4VP.

The transistor characteristic of a reference transistor with PS-*b*-P4VP without Au nanoparticles is presented in Figure 5.24. The electron mobility and on/off ratio are determined to be $0.003\text{--}0.0085 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $10^3\text{--}10^4$ respectively. A stable I_D-V_G characteristic is exhibited but no memory effects.

Figure 5.24: (a) Output characteristics (I_D versus V_D) of F₁₆CuPc OFET transistor utilizing pure PS-*b*-PVP. The gate voltage varies between 0V to 20V in steps of 5V. (b) Double sweeping semilog plots of I_D - V_G transfer characteristics of F₁₆CuPc OFET transistor utilizing pure PS-*b*-PVP. The drain voltage is at +5V. The channel length and width is 75 μm and 4000 μm respectively.

In comparing the memory performance in *p*-type pentacene and *n*-type F₁₆CuPc transistor, it can be seen that there is higher hole trapping effect in the Au nanoparticles from pentacene channel as compared to electron trapping from F₁₆CuPc channel. This may be attributed to difference in 1) charge carrier density in the channel which affects the tunneling probability, 2) mobility of charge carriers and/or 3) hole injection barrier ($\sim 0.5\text{eV}$ between HOMOs of pentacene and P4VP) and electron injection barrier ($\sim 1.3\text{eV}$ between LUMOs of F₁₆CuPC and P4VP). In particular, organic semiconductors with higher charge carrier densities may induce higher electric field coupling between the nanoparticle and the channel and hence higher probability of tunneling. Hence, further work needs to be done in order to have a better understanding and address the physical origins.

5.4.2 Programming and erasing characteristics

The performances of the devices as electrically programmable and erasable memory cells were evaluated next. During programming or erasing, the source and drain electrodes were grounded. After pulsing, the threshold voltage was determined by

monitoring the I_D - V_G transfer characteristics in a specified gate voltage range (-5V to +20V) while the drain potential (V_D) was fixed at 5V. Charge programming was performed by sweeping the gate voltage at 40V ($V_{G,program}$) for 5 seconds. The I_D - V_G shifts to the negative voltage direction (V_T shift of -7.5V) can be explained as being due to the electrons injection from $F_{16}CuPc$ channel into the Au nanoparticles, Figure 5.25. Increasing V_T shifts could be brought about by increasing $V_{G,program}$ (inset of Figure 5.25), further demonstrating the increasing electron trapping events.

As highlighted in earlier sections, most of organic semiconductors exhibit only single carrier (electron or hole) operation mode. Therefore, the efficiency of erasing is rather low. This effect can again be seen in Figure 5.25, where we observed little V_T shift on the programmed curve after the erasing operation ($V_{G,erase} = -40V$ for 5s).

Figure 5.25: Transfer characteristics obtained after different gate pulse conditions for $F_{16}CuPc$ OFETs using PS-*b*-(P4VP/AuNPs) as gate dielectric with channel length of 150 μm and channel width of 500 μm . The transfer characteristic of pristine device, after programming and erasing operations is in black, red and blue curve respectively. Programming: $V_G = +40$ V and $V_D = 0$ V was applied for 5s and erasing: $V_G = -40V$ and $V_D = 0V$ was applied for 5s. The gate voltage varies between -5V to 20V. The drain, V_D , is 5V. The inset shows the shifts in V_T as a function of programming voltage, $V_{G,program}$, at a charging time of 5s. The molar ratio of Au^{3+} :P4VP is 0.25.

5.4.3 Optical erasing

Likewise in pentacene based memory transistor, optical erasing is implemented on F₁₆CuPc based memories to enable minority carriers (hole in this case) injection with the use of light. As shown in Figure 5.26(a), the increase of I_D is caused by the creation of large number of charge carriers due to photoinduced charge transfer between F₁₆CuPc channel and the Au nanoparticles. The same explanations in section 5.3.3 can be used: With the generation of photoinduced charge carriers and the application of a negative electric field during illumination, the electron-hole pairs are separated and holes are transferred and trapped into the AuNPs and/or its interfaces. Upon switching the photoexcitation off, the trapped holes in the AuNPs will lower the potential barrier between the source and F₁₆CuPc channel, leading to a negative V_T shift.

Again, the OFF and ON states of the memory device can be switched repeatedly [see Figure 5.26(b)], where a writing voltage of +40V for 5s or an erasing voltage of -25V for 10s (under illumination) is applied respectively.

Figure 5.26: (a) Semilog plots of transconductance characteristics of a $F_{16}CuPc$ OFET memory device, measured at a fixed $V_D = 10V$ in the dark, after programming operation (red line, $V_G = +40V$ for 5s) and after illumination of the device with white light (intensity = 75 mW/cm^2) for 30 seconds. During illumination, a positive gate voltage of $-25V$ (blue line) is applied. The channel width and length are $1000 \mu\text{m}$ and $100 \mu\text{m}$ respectively. (b) Dynamic responses of the electrical programming and optical erasing of the $F_{16}CuPc$ OFET memory device at $V_G = +3V$, $V_D = 10V$. Light was turned on for 10s and a negative gate voltage of $-25V$ was applied during the illumination. A positive gate voltage pulse ($+40V$ for 5s) was applied to switch the transistor to OFF state. The molar ratio of Au^{3+} :P4VP is 0.25.

5.4.4 Retention characteristics

To study the retention of the shifted characteristics after programming and erasing operations, we measured the on and off current states at time intervals of 10s in the dark (at $V_G = 3\text{V}$ and $V_D = 10\text{V}$), after applying programming and erasing bias of $V_G = 40\text{V}$ for 5s and $V_G = -25\text{V}$ for 30s (under illumination) respectively. After the writing state, the transistor goes into OFF state, giving a low drain current at reading gate bias of 3V. The transistor is kept in the OFF state for 700 s, as shown in Figure 5.27, where the drain current increased slightly during this time interval. To erase the state, a gate voltage of -25V and illumination was applied for 30s and the high drain current indicates the ON state of the transistor. A small amount of decay in the ON-state drain current is observed.

Figure 5.27: Time responses of the drain current at $V_G = 3\text{V}$ and $V_D = 10\text{V}$, after programming ($V_G = 40\text{V}$ for 5s) or erasing (under light illumination and $V_G = -25\text{V}$ for 30s) operation. The channel width and length are $1000\text{ }\mu\text{m}$ and $100\text{ }\mu\text{m}$ respectively. The molar ratio of $\text{Au}^{3+}:\text{P4VP}$ is 0.25.

5.5 Summary

This chapter detailed the design of nano-floating gate organic memory transistors by utilizing the incorporation of Au nanoparticles in block copolymer gate dielectric. We first studied an organic memory capacitor device, with pentacene as the organic semiconductor and Au nanoparticles in PS-*b*-P4VP block copolymer nanodomains which successfully functioned as charge storage elements. A clockwise *C-V* hysteresis indicated a net hole trapping effect. This novel structure displays a large memory window of 2.1V after writing and erasing modes and a long charge retention ability of ~92% over 60,000 seconds.

Next, we have demonstrated both *p*-type (pentacene) and *n*-type (hexadecafluorophthalocyaninatocopper) OFET based memories, which have large charge capacity, stable and programmable-erasable properties. The unipolar nature of transport across the organic semiconductors prevents efficient minority carrier injection. To improve minority carrier injection, we have utilized optical excitation to induce photogenerated carriers for the erasing operation. Information can hence be introduced and read electrically, and erased optically, resulting in a large memory window, displays a high on/off ratio between memory states and a long retention time. These results clearly indicate the usefulness of the utilization of nanoparticle-polymer composite for organic device fabrication. Since both *p*-channel and *n*-channel memory transistors have been demonstrated separately, it is hence proposed that the fabrication of organic memory using bi-channel^[28] (both *n*-type and *p*-type semiconductors) device structure, or blend of *n* and *p* materials offers an effective programming-erasing approach. The utilization of asymmetric source-drain electrodes (for example, gold and aluminum or calcium electrodes) for efficient hole and electron injections offers another alternative approach; in *Chapter 4*, we have improved electron trapping in PS-*b*-(P4VP/AuNPs) through the use of aluminum electrode.

5.6 References

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Chapter 6

Conclusions and Perspectives

Non-volatile memory devices based on conventional silicon electronics have experienced explosive growth over the past decade in applications ranging from high end computing to low-cost mobile pen-sized flash drives. Applications such as large area electronics, low-cost dispensable sensor arrays, and memory tags on the other hand necessitate the design and development of alternate cost-effective memory solutions. Organic electronics has been considered as candidates for such non-volatile memory applications due to their simple structure, lower-cost, and the prospect of stacking them for packing bits at high densities. In order to explore the fundamental mechanisms at play in an organic memory device as well as to explore the feasibility of such devices, we have focused on floating gate devices based on gold nanoparticles as charge storage components. Our work involved rational development of functional nanoparticles/nanocomposites, demonstration of working memory devices and understanding the basic processes of device operation and charge conduction in these unique systems. In this chapter, we draw conclusions based on our observations and analysis (a table of summary depicting the main contributions of work done is also presented in Appendix F), and provide recommendations for future directions on nanoparticle based nonvolatile memory devices.

6.1 Conclusions

In the first part of our work, we developed a new organic memory system, using pentacene as the active semiconductor layer and citrate-stabilized gold nanoparticles (citrate-AuNPs) as charge storage elements, in a metal-pentacene-insulator-silicon

(MPIS) configuration. The citrate-stabilized Au nanoparticles were immobilized onto amine-terminated silicon surfaces through electrostatic attraction. A pronounced clockwise capacitance-voltage (C - V) hysteresis is observed with a memory window of 1.25V to 2.05V achievable under 5V to 10V programming range. Similar clockwise C - V hysteresis window and an almost constant full width at half maximum (FWHM) of the conductance peaks in conductance-voltage (G - V) characteristics, obtained in the frequency range of 50 kHz – 1 MHz, indicated that positive charge trapping/de-trapping originated mainly from the Au nanoparticles. Current-voltage characteristics are analyzed to determine the charge transport mechanism, which indicates the occurrence of Fowler-Nordheim hole tunneling. At a writing voltage of -3V, the charge retention ability of 85% over more than 10,000 seconds has been demonstrated. An experimental analysis for the charge storage activation energy of 13.3 meV in the citrate-AuNPs system is established. The citrate-AuNPs memory element has also been integrated into a pentacene organic field-effect transistor, where the occurrence of strong hole trapping from the channel to the gold nanoparticles is observed. The system introduced here is versatile- the choice of the appropriate head and tail groups of the SAM layer allows immobilization of different nanoparticles on a variety of surfaces. The separation of the nanoparticle synthesis from its integration into the memory device allows room temperature fabrication.

Despite the perceived advantages of the chemical self assembly approach, the fabrication of the device is time consuming and affords less control over the arrangement and density of charge storage centers. The second part of the thesis deals with a more efficient methodology for creation of arrays of nanoparticles which involves the utilization of self-assembling amphiphilic diblock copolymer of polystyrene-*b*-poly-4-vinylpyridine (PS-*b*-P4VP). The block copolymer micelles prove to be an excellent model system, which is simple, forms a self-assembled ordered nanostructure and provides optimum control over nanoparticle size formation and isolation. We demonstrate herein, a polymeric memory that comprises an *in-situ* synthesis strategy of gold nanoparticles in PS-*b*-P4VP; PS-*b*-(P4VP/AuNPs). The response of the memory device is controlled by the applied voltage where a spatial distribution of charge carriers can be retained (trapped) in the nanoparticles, and

thereby offers a non-volatile function to the memory device. The ability to tune the memory behavior was also illustrated by changing the loading of Au nanoparticles. It was found that purity of the copolymer matrix had a large effect on the electrical properties; copolymer purified by solvent extraction method maintained their core size and improved the memory properties.

The kinetics of charging and discharging of charge carriers in PS-*b*-(P4VP/AuNPs) layer has also been studied. Hole trapping is observed to be more efficient than electron trapping and is attributed to a lower electron injection current (due to presence of Schottky barrier between the gold electrode and P4VP layer). At higher electric fields (>0.4 MV/cm), quasi-two-dimensional charge transport through the arrays of gold nanoparticles in P4VP nanodomains is observed. The contribution of electrode work function was demonstrated with improved electron charging by the replacement of gold electrode with aluminum. Based on impedance measurement, the equivalent circuit of the memory device was identified as a parallel combination of the depletion layer capacitance C_D and the capacitance C_{nc} and resistance R_{nc} due to charge stored in gold nanoparticles, in series with effective dielectric stack capacitance C_{eff} and series resistance of the device, where the influence of interface traps has been shown to play a minimal role in the charge storage.

Chapter 5 describes our efforts to develop organic field-effect transistors incorporating the active memory layer of PS-*b*-(P4VP/AuNPs). We have demonstrated both *p*-type (pentacene) and *n*-type (hexadecafluorophthalocyaninatocopper) OFET based memories, which have large charge capacity and programmable-erasable properties. A large charge capacity (i.e. I_D - V_G hysteresis window) of ~ 7 V and 3V is observed in pentacene and F₁₆CuPc based OFET memory respectively. To improve minority carrier injection for erasing operations, we have utilized optical excitation to induce photogenerated minority carrier trapping in PS-*b*-(P4VP/AuNPs). The memory device can hence be written and read electrically and erased optically, resulting in a large memory windows, high on/off ratio between memory states ($>10^2$) and long retention times.

Generally, the overall device performance based on PS-*b*-(P4VP/AuNPs) block copolymer surpasses the one with citrate-AuNPs. One main reason is the utilization of a copolymer matrix which provides optimum control over nanoparticle size formation and isolation. The block copolymer approach is also more advantageous due to the ability to control the size, density and/or distribution of nanoparticles more precisely through modification of the molecular weight of each polymer block or the ratios between the blocks allowing improvements in the memory characteristics to be made more easily. The limitation of the citrate-AuNPs system also includes the time-consuming fabrication process, which involves pre-synthesizing the nanoparticles followed by 12 hours of deposition time. The negatively charged AuNPs will also limit the density of the nanoparticles since these charges will repel from each other. However, the citrate-AuNPs system produces a larger memory window due to lower tunneling resistance of citrate shell.

It is noted that the overall performance in both memory systems are still in early development stage. We have summarized some of the crucial parameters of both memory devices and compared with existing assembly methods (see Appendix G). Both systems serve as a prototype for a generic memory device using nanoparticles as floating gate charge storage centers and in particular, for integration into OFET based circuits. The demonstration of these architectures in both p-type and n-type transistors illustrate that the difficulties in erasing arise from the unipolar nature of the organic semiconductor and is not an indication of the intrinsic nature of the systems. We believe that our work suitably illustrates the potential of two novel memory systems, where a wide range of organic semiconductors, self-assembled monolayers or block copolymers and metal or semiconducting nanoparticles, can be combined to realize low-cost, solution processable design and process schemes in memory applications such as large area integrated electronics, RFIDs, and smart tags amongst others. In particular, the choice of block copolymer can be tailor-made where the volume fraction of each block and/or total molecular weight can be varied to create different types of tunneling barrier, and hence utilized in different memory architectures and applications.

The experimental techniques explored in this thesis as well as the results allow the extension of understanding and applicability of charge trapping using either arrays of self-assembled Au nanoparticles or Au nanoparticles in block copolymer nanodomains. Fundamental understanding of charge transport, evaluation on the role of interface traps, influence of barrier height or electrode work function and the role of organic semiconductors on charge trapping effect investigated in this thesis allow the future optimization of device performance for practical memory applications. These results also shed light on the design parameters to achieve a high performance organic memory element (see Appendix H):

- (i) Isolated nanoparticles can serve as trap centers and control of the trapped charges can be made possible by design of their size and density;
- (ii) Tuning of work function of the electrode and/or energy levels of the materials system is necessary to allow facile carrier injection from the electrodes, and to trap/confine the charges for increased retention ability;
- (iii) High- k dielectrics can be used to lower the magnitude of programming/erasing voltages and improve the switching times;
- (iv) High mobility organic semiconductor with favorable band alignment for the transport of charge carriers to the floating gate is desired;
- (v) Both n -type and p -type semiconductors can be combined (either as blends or bilayers) for efficient programming and erasing operations.

6.2 Future outlook

Although the devices covered in this thesis show promising performance, development of such organic memory technology warrants continuous study and optimization of the devices. Several important questions remained unanswered at this moment. The effects of nanoparticle sizes on the performance of these memory devices as well as the parameters that determine the programming and erase speeds are still to be studied in detail. In order to qualify these two systems as effective organic memory solutions,

data concerning the device reliability and cycling stability need to be collected alongside a study of the device failure mechanisms and causes of degradation.

Some recommendations for future work that may shed light on these concerns are proposed below:

6.2.1 All-organic based memory transistor

To fully utilize the unique advantages provided by organic materials and devices, which include low fabrication cost, compatibility with flexible substrates, solution processibility is an important criterion. A printable flexible memory element for OTFT makes it suitable for display driver logic, radio frequency identification (RFID) tags and electronic paper (e-Paper) applications. Hence, soluble organic semiconductors and polymer dielectrics (to replace the current thermal oxide layer) are suggested to be tried and tested in the memory device. Figure 6.1 presents the design of an all-organic memory transistor using top-gate configuration. Top-gate device architectures are especially advantageous for technological applications due to the presence of gate dielectric layer on top of the active layers (organic semiconductor and memory layers) hence providing a sealing or encapsulation effect against environmental exposure.^[1] Device lifetime can thus be improved upon.

The main challenge in making an all-organic based memory device is the solvent compatibility problem between each organic layer. Hence, cross-linking of the block copolymer may be needed when any solution processable dielectrics or semiconductor are to be spin-coated on top.

Figure 6.1: Schematic of top-gate organic memory transistor with using a standard OFET device structure.

6.2.2 Device modeling and simulations

Technology Computer-Aided Design (TCAD) based simulations have been carried to describe the behaviors of OFETs numerically. For example, the effects of traps,^[2, 3] field-dependent mobility models,^[4] device structures,^[5] etc on the device characteristics have all been pursued. Hence it is desired to report the two-dimensional modeling and simulation of OFET memory device with the influence of both floating gate traps and/or interface traps. Correlation of charge trapping and carrier transport with process parameters can also be validated based on experimentation and simulation. TCAD tool Taurus-Medici can be used to qualitatively explain or verify the proposed charge storage model with 2D simulation of transfer and output characteristics and memory behavior. Besides TCAD simulation, theoretical analysis or modeling can be performed to study the energy distribution of traps or the effect of tunneling barrier property on the programming/erasing speeds of the memory cell.

6.2.3 Charge storage mechanism study using Electrostatic Force Microscopy (EFM)

For memory device applications, it is necessary to understand the charging and discharging behaviors of the charge storage elements, since the data retention in the

memory is determined by the discharging properties. The usage of atomic force microscopy to inject, detect and quantify the amount of charges trapped in dielectric films was demonstrated by Boer *et al.*^[6] and the charging effect of Cobalt nanoclusters in dielectric films^[7] has already been mapped out using electrostatic force microscopy (EFM). These advanced techniques can give information of localized charging properties. In contrast, device characterization such as capacitance-voltage (*C-V*) measurements can only give macroscopic device information which represents the averaged property over an area but not the variation in nanometer scale. With the EFM technique, information of electrical properties can be obtained with nanometer resolution and the distribution of charges trapped in the nanocrystals embedded in the thin film can be mapped based on the total electrostatic potential of the cantilever tip.

6.2.4 New chemistry / materials

New types of block copolymer and nanoparticles can be utilized to improve the charge retention ability. For example, 1) the PS block can be replaced with a lower chain length so that the tunneling barrier is reduced, 2) the P4VP block can be replaced with another type that has a higher HOMO level to increase the retention (reduced hole-loss) or 3) the Au nanoparticles can be replaced with a higher work-function metal nanoparticles (eg. Pt) to reduce charge loss. The memory characteristics can be tuned by using a mixture of metal nanoparticles with different electron affinities, hence creating multi-state levels. The size of the particles can also be simply regulated so that they exhibit Coulomb blockade at room temperature within a useful bias range.

In addition, the *in-situ* synthesis process of Au nanoparticles in PS-*b*-P4VP is proposed to be modified. In the current procedure, the use of chemical reducing agent may introduce ionic impurities. Photoreduction of Au precursor to nanoparticles offers the option of a “cleaner” process.^[8] The reactions for the formation of Au nanoparticles in PS-*b*-P4VP by UV irradiation are listed as below:^[9]

The preliminary results of the absorption spectra for the synthesized Au nanoparticles in PS-*b*-P4VP using UV-irradiation method are shown in Figure 6.2. The UV irradiation was carried out using the UV Curing System F300s. The whole synthesis process requires ~1 hour 30 minutes for the complete reduction of the Au precursor to nanoparticles.

Figure 6.2: Absorption spectrum of the PS-*b*-P4VP nanocomposites in toluene (a) 6 minutes, (b) 51 minutes, and (c) 85 minutes after UV irradiation.

6.3 References

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- [3] S. Scheinert, G. Paasch, T. Doll, *Synthetic Metals* **2003**, *139*, 233.
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Appendix A List of Abbreviations

AFM	atomic force microscope (microscopy)
APTES	3-aminopropyl-triethoxysilane
AuNPs	gold nanoparticles
C-V	capacitance-voltage
DDT	dodecane-1-thiol
DLTS	deep level transient spectroscopy
DLS	dynamic light scattering
DSC	differential scanning calorimetry
EA	electron affinity
FET	field-effect transistors
FTIR	Fourier transform infrared spectroscopy
FWHM	full-width-at-half-maximum
F ₁₆ CuPc	hexadecafluorophthalocyaninatocopper
G-V	conductance-voltage
HOMO	highest occupied molecular orbital
I-V	current-voltage
IP	ionization potential
J-V	current density-voltage
LUMO	lowest unoccupied molecular orbital
MOS	metal-oxide-semiconductor
MIS	metal-insulator-semiconductor
MPIS	metal-pentacene-insulator-silicon
MOSFET	MOS field-effect transistor
nm	nanometer
OFET	organic field-effect transistor
PL	photoluminescence
P4VP	poly-4-vinylpyridine
PS	polystyrene

PS- <i>b</i> -P4VP	polystyrene- <i>b</i> -poly-4-vinylpyridine
SAM	self-assembled monolayer
SAXS	small-angle x-ray scattering
Si	silicon
TEM	transmission electron microscope (microscopy)
UV-vis	ultraviolet to visible light range
XPS	X-ray photoelectron spectroscopy

Appendix B

Table B.1: Summary of device structure, behavior and mechanism in resistor- and transistor-type organic memories

Types of memory	Resistor-type	Transistor-type (or capacitive-type)
Physical Description	Data storage is based on the high and low conductivity states of resistor in response to the applied electric field.	Charge storage and/or polarization in the dielectric layer or interfaces of an organic field effect transistor.
Device Structure	<p>(a) Metal-insulator-metal</p>	<p>(a) Floating gate OFET (b) Charge trapping OFET (c) Ferroelectric OFET</p>
Material systems	<p>(a) Small molecule (b) Insulating polymers (c) Isolated chromophores, donors and acceptors (d) Semiconducting polymers (e) Composite materials</p>	<p>(a) Semiconductor materials (b) Gate insulator: inorganic insulators, discrete metal nanoparticles, polymer dielectrics (electrets), ferroelectric polymers</p>
Device Behavior	<p>- Six types of current versus voltage curves reported for organic bistable devices.^[1]</p>	<p>- Shift in threshold voltage in the transfer characteristics</p>
Mechanism	Electrical bistability can be induced by: (a) a change in carrier concentration, (b) a change in charge mobility and (c) a change in both.	Charge storage or polarization in OFET gives rise to an additional voltage between the gate and the semiconductor channel, and hence a shift of threshold voltage (V_{th}) or hysteresis.

Reference:

[1] J. C. Scott, L. D. Bozano, *Advanced Materials* **2007**, *19*, 1452.

Appendix C Solvent extraction procedures

Purification of the as-purchase PS-*b*-P4VP was carried out rigorously as follows to ensure the removal of the catalyst side product:

- 1) Dissolve the block copolymer in toluene and wash with de-ionized distilled water to remove any soluble organic side product.
- 2) The copolymer is extracted from water with toluene.
- 3) The copolymer solution in toluene is dried over anhydrous sodium sulfate.
- 4) The solution is filtered and passed through a column packed with basic Al₂O₃.
- 5) The solution is concentrated on rota-evaporator.
- 6) The solution is precipitated in cold hexane and redissolved in benzene and freeze dried.
- 7) The precipitates are dried under vacuum for 48hr at 50°C.

Appendix D Determination of nanoparticle density in block copolymer micelles

Given:

Mean micellar diameter (2R) of micelle: 28.9 nm (as calculated from DLS)

Radius (R) of a micelle: 14.45 nm

Approximate block copolymer density (D): 1 g/cm³

$$1 \text{ cm}^3 = 1 \times 10^{21} \text{ nm}^3$$

Calculate the volume of a micelle (assuming a spherical shape)

Volume (V_{micelle}) of a sphere = $\frac{4}{3} \times \pi \times \text{radius (R) of a micelle}^3$

$$V_{\text{micelle}} = \frac{4}{3} \times \pi \times R^3$$

$$V_{\text{micelle}} = \frac{4}{3} \times \pi \times (14.45 \text{ nm})^3$$

$$V_{\text{micelle}} = 12.638 \times 10^3 \text{ nm}^3$$

Calculate the weight of 1 micelle (M_{micelle})

Density (D) = grams (g)/ volume (v)

$$D = g/v$$

$$g = D \times v$$

$$g = 1 \text{ g/cm}^3 \times (12.638 \times 10^3 \text{ nm}^3 / 1 \times 10^{21} \text{ nm}^3)$$

$$M_{\text{micelle}} = 1.2638 \times 10^{-17} \text{ grams}$$

Calculate the weight of the block copolymer solution (W_{BC})

Given:

Concentration of copolymer solution: 5 mg/mL

Volume of solution: 5 mL

Weight of block copolymer solution (W_{BC})

$$= 5 \text{ mg/mL} \times 5 \text{ mL} = 0.025 \text{ g} = 25 \text{ mg}$$

Calculate the total number of micelles (N_{micelle})

$$N_{\text{micelle}} = \text{Weight of copolymer solution} / \text{Weight of micelle}$$

$$= W_{\text{BC}} / M_{\text{micelle}} = 0.025 \text{ g} / 1.2638 \times 10^{-17} \text{ g} = 1.9781 \times 10^{15} \text{ micelles}$$

Calculation of total number of gold atoms ($N_{\text{T, gold atoms}}$)

Given:

Molecular weight (MW) of $\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$: 393.79 g/molWeight of $\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$: W_{HAuCl_4} (g)Avogadro's number (N_A): 6.023×10^{23} atoms/ molecule)Moles of $\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$

$$= W_{\text{HAuCl}_4} / \text{MW}$$

$$= \eta_{\text{HAuCl}_4}$$

$$N_{\text{T, gold atoms}} = \eta_{\text{HAuCl}_4} \times N_A$$

Calculation of number of gold atoms in one particle ($N_{\text{gold atoms}}$)

Given:

Density of gold: 19.2 g/cm³

Molecular weight of gold: 196.97 g/mol

$$1 \text{ cm}^3 = 1 \times 10^{21} \text{ nm}^3$$

Assume that all of gold atoms combine to form the diameter of a gold particle.

Volume of a gold particle = $V_{\text{particle}} = \frac{4}{3} \pi r^3$ (r = size of particle as determined from TEM image or SAXS)

$$V_{\text{particle}} = 1 / \text{Density of gold} \times \text{MW} \times 1 / N_A \times N_{\text{gold atoms}}$$

$$N_{\text{gold atoms}} \text{ (in one particle)} = V_{\text{particle}} * \text{Density of gold} * N_A / \text{MW} / 10^{21}$$

Calculation of Total number of particles (N_{particle})

$$N_{\text{particle}} = N_{\text{T, gold atoms}} / N_{\text{gold atoms (in one particle)}}$$

Calculation of Number of nanoparticle per micelle ($N_{\text{particle/micelle}}$)

$$N_{\text{particle/micelle}} = N_{\text{particle}} / N_{\text{micelle}}$$

$$\text{For an area of } A \text{ cm}^2, \text{ no. of micelles} = A / \pi R^2 = A / [\pi (14.45 \text{ nm} \times 1 \times 10^{-7})^2]$$

$$\text{For an area of } A \text{ cm}^2, \text{ no. of nanoparticles} = N_{\text{particle/micelle}} * A / [\pi (14.45 \text{ nm} \times 1 \times 10^{-7})^2]$$

Appendix E Current-voltage characteristics of a diode device using block copolymer containing gold nanoparticles; PS-*b*-(P4VP/AuNPs)

Figure E.1: Current density-voltage (J-V) characteristics of a Au electrode/PS-*b*-(P4VP/AuNPs)/Al electrode device (0.3 molar ratio of H_{AuCl₄}/P4VP). The potential is scanned from +10 to -10V and back, showing shift in threshold voltage, V_t .

Appendix F Main contributions of work done

Table F.1: Summary of main contributions of work done

Chemically assembled gold nanoparticle arrays		Gold nanoparticles within a self-assembled block copolymer		
Device Structure		Device Structure		
MPIS*	OFET [#]	MIS [@]	MPIS*	OFET [#]
<p>1. Proof of memory effect where holes from pentacene layer are trapped in the Au nanoparticles (double sweeping $C-V$ measurements, see page 75-79).</p> <p>2. Frequency-dependent studies to determine the origin of trap states ($C-V$ measurements at various frequencies, see page 81-82).</p> <p>3. Temperature-dependent studies to determine the charge storage activation energy ($C-V$ measurements at various temperatures, see page 83-86).</p> <p>4. Charge transport mechanism ($I-V$ measurements, see page 86-88).</p> <p>5. Programming and Retention studies ($C-V$ measurements, see page 89-91).</p> <p>6. Dependence of organic capping layer surrounding the gold nanoparticles ($C-V$ and $I-V$ measurements, see page 92-97).</p>	<p>1. Proof of memory concept (double sweeping I_D-V_G measurements, see page 97-99).</p> <p>2. Programming studies (voltage pulsing on I_D-V_G measurements, see page 100).</p>	<p>1. Proof of memory effect (double sweeping $C-V$ measurements, see page 143-144).</p> <p>2. Frequency-dependent studies to determine the origin of trap states ($C-V$ measurements at various frequencies, see page 157-160).</p> <p>3. Charge transport mechanism ($I-V$ measurements, see page 148-150).</p> <p>4. Programming, erasing and retention studies ($C-V$ measurements, see page 145-48).</p> <p>5. Study of dependence of work function of injecting electrode on charging effect ($C-V$ and $I-V$ measurements, see page 156).</p>	<p>1. Proof of memory effect where holes from pentacene layer are trapped in the Au nanoparticles (double sweeping $C-V$ measurements, see page 170).</p> <p>2. Frequency-dependent studies to determine the origin of trap states (using $C-V$ measurements at various frequencies, see page 171-172).</p> <p>3. Programming, Erasing and retention studies (using $C-V$ measurements, see page 173-176).</p>	<p>1. Realize floating gate transistor based organic memories using p-type and n-type organic molecules (double sweeping I_D-V_G measurements, see page 183-186, 203-204).</p> <p>2. Programming, Erasing and retention studies (voltage pulsing on I_D-V_G measurements, see page 187-190, 205-206).</p> <p>3. Optical studies to induce photoexcited charge carrier trapping in the Au nanoparticles (under illumination and I_D-V_G measurements, see page 192-198, 206-209).</p>

*MPIS: Metal-Pentacene-Insulator-Silicon capacitor structure, [@]MIS: Metal-Insulator-Semiconductor capacitor structure, [#]OFET: Organic Field-Effect Transistor

Appendix G Summary of memory devices prepared from
different assembly methods

Table G.1: Summary of memory devices prepared from different assembly methods

	Memories based on nanoparticle assemblies			
	Block copolymer assembly (PS-b- P4VP/AuNPs) (our work)	Chemical self- assembly (APTES-AuNPs) (our work)	Hybrid self- assembly ^[1]	Layer-by-layer assembly ^[2]

Device Type, Material Used	Floating gate (pentacene OFET), block copolymer of PS- b-P4VP and gold nanoparticles	Floating gate (pentacene OFET), self-assembly monolayer of APTES and citrate- gold nanoparticles	Floating gate (Si-based MISFET), APTES and citrate-gold nanoparticles	Floating gate (P3HT OFET), polyions of PEI and PSS and citrate-gold nanoparticles
Nanoparticle Density (cm ⁻²)	2.61 – 6.67 x 10 ¹⁰	7 x 10 ¹⁰	7 x 10 ¹²	-
Stored Charge Density (cm ⁻²)	1.09 x 10 ¹²	8.62 x 10 ¹¹	1.87 x 10 ⁻¹²	-
Write time (seconds)	~1 s	~5 s	~1 s	~15 s
ON/OFF ratio	10 ⁵ -10 ⁶	10 ² -10 ⁴	10 ⁷	10 ⁴
Retention time (seconds)	> 10,000	>10,000	>10,000	~ 200

Reference:

[1] S. Kolliopoulou, P. Dimitrakis, P. Normand, N. C. H.-L. Zhang, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, D. Tsoukalas, *Microelectronic Engineering* **2004**, 73, 725.

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Appendix H List of materials implemented in the memory systems

Table H.1: Summary of list of materials implemented in the memory systems

	Functions	Requirements/Parameters for Material selection	Insights
Gold nanoparticles	Charge storage centers	<ul style="list-style-type: none"> - Work function: Au has high work function (~5eV), in comparison with silicon and other metals such as Ag. With a larger work function, the barrier height seen by the electrons inside the nanoparticles is increased. The increase of barrier height translates into reduced tunneling probabilities and enhanced charge retention. - Ease of synthesis - Tunable size 	Discrete nanoparticles can serve as trap centers and control of charge density can be made possible by design of their size and density.
Self-assembled monolayer of APTES	To graft the nanoparticles	<ul style="list-style-type: none"> - Functional group: suited for self assembly - Insulating nature: prevent leakage of charges from the nanoparticles to the electrode. 	-
Block copolymer of PS- <i>b</i> -P4VP	Both PS and P4VP acts as tunneling barrier	<ul style="list-style-type: none"> - The block copolymer acts as a template for nanoparticle array. - The P4VP core acts as a reactor for nanoparticle synthesis. The metal-chelating nature of the pyridine unit allows easy binding of the gold precursors. High density of nanoparticles can hence be synthesized for increased charge density. - The thin PS (2-3nm) layer allows easy tunneling of charge carriers into the nanoparticles. 	Tuning of tunneling barrier can be done by varying the volume fraction of each block and/or total molecular weight.
Citrate ions or DDT for chemically assembly nanoparticles array	Tunneling barrier	The citrate ions are negatively charged, resulting in nanoparticles repelling from one another. Shorting or crossing talking between the particles is prevented.	-
Organic semiconductor (pentacene and fluorinated copper phthalocyanine)	Semiconductor in transistor acting as source of charge carriers	- High mobilities: These p- and n-type semiconductors have been well-researched upon, with high charge mobilities ($10^{-2} - 1 \text{ cm}^2/\text{Vs}$).	High mobility organic semiconductor with favorable band alignment for the transport of charge carriers to the floating gate is desired.
Control SiO ₂ layer	Prevent leakage of charges through the device	<ul style="list-style-type: none"> - Good dielectric breakdown, dielectric constant of 3.9. - Minimum interfacial traps 	High-K dielectrics can be used to lower the magnitude of programming/erasing voltages and improve the switching times.
Gold electrode	Injecting charges	Work function of Au matches well with HOMO of pentacene and LUMO of F ₁₆ CuPc. There is little energy barrier for injection of holes or electrons from Au electrode to the organic semiconductor.	Tuning of electrode work function is necessary to allow facile carrier injection from electrodes.

Appendix I Author's Publication List

JOURNAL ARTICLES

- (1) Micellar poly(styrene-*b*-4-vinylpyridine)-nanoparticle hybrid system for non-volatile organic transistor memory

W. L. Leong, N. Mathews, S. G. Mhaisalkar, Y. M. Lam, T. P. Chen, and P. S. Lee

Journal of Materials Chemistry, 19, 7354 (2009)

- (2) Charging Dynamics of discrete gold nanoparticles arrays self-assembled within a poly(styrene-*b*-4-vinylpyridine) diblock copolymer template

W. L. Leong, N. Mathews, S. G. Mhaisalkar, T. P. Chen, and P. S. Lee

Applied Physics Letters 93, 222908 (2008)

(Selected V18, N25, 2008 issue of Virtual Journal of Nanoscale Science & Technology)

- (3) Non-volatile Organic Memory Applications Enable by In-situ Synthesis of Gold Nanoparticles in a Self-Assembled Block Copolymer

W. L. Leong, P. S. Lee, A. Lohani, Y. M. Lam, T. P. Chen, S. Zhang, A. Dodabalapur, and S. G. Mhaisalkar

Advanced Materials 20, 2325 (2008)

- (4) Charging phenomena in pentacene-gold nanoparticle memory device

W. L. Leong, P. S. Lee, S. G. Mhaisalkar, T. P. Chen, and A. Dodabalapur

Applied Physics Letters 90, 042906 (2007)

(Selected V15 N5, 2007 issue of Virtual Journal of Nanoscale Science & Technology)

CONFERENCE PRESENTATIONS

- (1) Floating Charge Storage Centers for Non-volatile Organic Memory Applications enabled by in-situ synthesis of Gold Nanoparticles in a Self-assembled Block Copolymer

W. L. Leong, P. S. Lee, T. P. Chen, and S. G. Mhaisalkar

3rd International Conference on Smart Materials, Structures and Systems (CIMTEC 2008), Acireale, Sicily (Italy), 8-12 June 2008 (oral presentation)

- (2) Gold Nanoparticles in Self-assembled Copolymer Thin Films for Organic Memory Applications

W. L. Leong, G. K. Lim, P. S. Lee, T. P. Chen, Y. M. Lam, and S. G. Mhaisalkar

4th International Conference on Materials for Advanced Technologies (ICMAT 2007), Singapore, 1-6 July 2007 (oral presentation)

- (3) Fabrication of Gold Nanoparticle-Pentacene memory device and investigation on its charge storage phenomena

W. L. Leong, P. S. Lee, T. P. Chen, and S. G. Mhaisalkar

4th International Conference on Materials for Advanced Technologies (ICMAT 2007), Singapore, 1-6 July 2007 (oral presentation)

- (4) Nanoparticles in Self assembled Block copolymer thin films for organic memory applications

W. L. Leong, P. S. Lee, T. P. Chen, Y. M. Lam, and S. G. Mhaisalkar

E-MRS 2007 Spring Meeting, Strasbourg, France, 28 May – 1 June 2007 (oral presentation)

- (5) Self assembled gold nanoparticles for organic memory applications

W. L. Leong, P. S. Lee, T. P. Chen, and S. G. Mhaisalkar

E-MRS 2006 Spring Meeting, Nice, France, 29 May – 2 June 2006 (oral presentation)

PATENT

Synthesis, Design, and Method of forming nanostructure-based organic floating gate memory devices

W. L. Leong, P. S. Lee, Y. M. Lam, L. Song, E. B. Namdas, and S. G. Mhaisalkar

US Patent filed on 22 May 2007 (PCT Patent Application No. PCT/SG2007/000141)