Analysis and design of CMOS mixers for direct conversion receivers

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Analysis and Design of CMOS Mixers for Direct Conversion Receivers

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Master of Engineering

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

Date

Liu Jingjing

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Abstract

The direct conversion receiver (DCR) architecture eliminates the requirement of high quality factor image-reject band-pass filters and realizes the full receiver integration on chip. However, The DCR also has its own problems, which do not exist or have any serious effect in other receiver architectures. The most critical drawback of the DCR architecture is the DC offset due to the LO-RF leakage, which arises from capacitive and substrate coupling. In this case the down-converted signal spectrum includes the zero frequency. If the DC offset is large, it will corrupt the signals. Many techniques have been proposed in the literature to reduce and minimize the offset. But no quantitative analysis of the LO-RF leakage has been made.

In this project, the analysis and design of CMOS mixers for direct conversion receivers have been explored. A CMOS double-balanced Gilbert mixer operating at the centre frequency of 2.45GHz for direct conversion applications is designed using Cadence SpectreRF for the Chartered 0.18um CMOS Digital/Analog/RF process. The LO-RF leakage caused by the LO mismatch in the Gilbert mixer is examined and analyzed for three scenarios of an ideal mixer, a non-ideal mixer with parasitic effects, and an ideal mixer with LO mismatch. The LO mismatch includes phase mismatch only, amplitude mismatch only and the combination of the two mismatches. It is found that if there is no LO mismatch, an ideal mixer will not have an LO leakage and DC offset. If a phase mismatch or amplitude mismatch exists, the LO leakage is proportional to the mismatch

Abstract

value. If both types of mismatches occur at the same time, the amplitude square of the LO leakage is equal to the sum of amplitude squares of each contribution. The relation between the mismatch and the LO leakage is derived. The analysis agrees with simulation results.

The DC offset and the high flicker noise are the main problems in the design of direct conversion CMOS mixers. A novel even harmonic switching mixer implemented in a standard 0.18 μm CMOS process for applications in 2.45GHz direct conversion receivers is proposed. The mixer circuit overcomes the problems of DC offset and high flicker noise. It has an 8.24dB conversion loss, 5.21dB DSB noise figure at 100kHz, 17.25dBm IIP3 and zero DC power consumption. The DC offset problem is solved by the even harmonic technique. The low noise figure is obtained by the zero bias current in the transistors. The conversion gain is less than unity, but it is not critical and can be compensated by using a low noise amplifier (LNA) with a high gain in the direct conversion receivers.

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List of Abbreviations

ADC – Analog-Digital Converter

AM – Amplitude Modulation

BB - Baseband

BBA – Baseband Amplifier

BBF – Baseband Filter

CDMA – Code Division Multiple Access

CMFB – Common Mode Feedback

CSM – Chartered Semiconductor Manufacturing

DAC – Digital-Analog Converter

DCOC – DC Offset Corrector

DCR – Direct Conversion Receiver

DCS – Digital Communications System

DMD – Demodulator Block

DSP – Digital Signal Processing

EDGE – Enhanced Data Rates for GSM Evolution

EGSM – Extended Global System for Mobile Communications

FSK – Frequency Shift Keying

GPRS – General Packet Radio Service

GSM – Global System for Mobile Communications

HB – High-Band

HM – Harmonic Mixer

List of Abbreviations

IF – Intermediate Frequency

IIP2 – Input Second-order Intermodulation Product

IIP3 – Input Third-order Intermodulation Product

LB – Low-Band

LNA – Low Noise Amplifier

LPA – Low-Pass Filter

MiM – Metal-insulator-Metal

NADC – North American Digital Cellular

NF – Noise Figure

PCS – Personal Communications System

Pdisto – Periodic Distortion

PGA – Programmable Gain Amplifier

PHS – Personal Handy-phone System

PIS – Poly-Insulator-Substrate

PLL – Phase-Locked Loop

Pnoise – Periodic Noise

PPF – Poly Phase Filter

PSS – Periodic Steady State

PTAT – Proportional to Absolute Temperature

PXF – Periodic Transfer Function

QPSK – Quadrature Phase Shift Keying

RF – Radio Frequency

SAW – Surface Acoustic Wave

List of Abbreviations

SFDR – Spurious-Free Dynamic Ranges

SNR – Signal to Noise Ratio

TDMA – Time Division Multiple Access

VCO – Voltage-Controlled Oscillator

VCTCXO – Voltage Controlled Temperature-Compensated Crystal Oscillator

VGA – Variable Gain Amplifier

WLAN – Wireless Local Area Network

Chapter 1

Introduction

1.1 Motivation

The tremendous growth in the wireless consumer services has made a significant impact on today's semiconductor industry and its relationship to *RF* and microwave products. With the increasing number of cellular phone users and the introduction of new wireless applications such as Bluetooth and Wireless Local Area Network (*WLAN*) systems, sale of *RF* and microwave products has turned into a very profitable business. The demand for high performance *RF* and microwave products is growing rapidly.

Since its introduction, the heterodyne/superheterodyne architecture has been adopted in almost every receiver. The idea of down-converting the interested spectrum to one or more intermediate frequencies (*IFs*) makes it possible to process the signal under well-controlled conditions. High selectivity is achieved by inserting high quality filters. With the need to suppress the image, an image-rejection filter is required at the *RF* front-end. In addition to the image-rejection filter, high quality band-pass filters must be used for an acceptable selectivity. As these filters are difficult to integrate on the silicon base, discrete passive devices become the most common choice. Although the performance of the heterodyne system is guaranteed, the drawback is high cost, low integration level, high power consumption and so on.

In the midst of such trends to cut cost, increase manufacturability and portability, the direct conversion transceiver topology can make a tremendous difference. The direct conversion architecture can reduce the cost and the size of a receiver by decreasing the number of individual ICs, off-chip components, and expensive and bulky surface-acoustic-wave (*SAW*) filters [1][2].

However, a number of issues which do not exist or are not serious in the heterodyne architecture become important in the direct conversion architecture, such as DC offset, I/Q mismatch, even order distortion and so on. Among these the DC offset generated by the self-mixing in the mixer is the most critical. Approaches to remove the offset have so far mostly been focused on three methods. The first approach involves the selection of modulation formats that have no or little spectral power at DC, so that AC coupling at the mixer output, or at some downstream stage, can be used to remove the offset [3][4]. The second common approach is the use of baseband analog and/or digital signal processing (DSP) techniques for offset estimation and cancellation [5]-[7]. It is a widely used method, which increases the complexity and cost of receivers. Another approach is to use a DC-offset-free mixing topology, such as harmonic mixers [8]-[10]. This technique gives a simple solution to the DC offset problem, but it has not gain much attention. The DC offset is caused by the LO-RF leakage that is induced by the substrate coupling and the asymmetry of the mixer. Much research has been done on DC offset cancellation techniques. Nevertheless, no detailed analysis of the LO-RF leakage has been reported in the literature.

1.2 Objectives and Scope

The DC offset is an inherent problem of the direct down conversion Gilbert mixer and it is caused by the LO-RF leakage due to the substrate coupling and the asymmetry of the mixer. There are two objectives in this project. Firstly, The LO-RF leakage and feedthrough in double-balanced CMOS Gilbert mixers will be analyzed for scenarios of an ideal mixer, an ideal mixer with LO mismatch and a non-ideal mixer with parasitic effects. Secondly, a CMOS mixer with DC offset free and low noise figure will be designed for direct conversion receivers.

1.3 Major Contributions of the Thesis

A CMOS double-balanced Gilbert mixer operating at the centre frequency of 2.45GHz for direct conversion applications has been designed using the Chartered Semiconductor Manufacturing (CSM) 0.18 μ m CMOS process, and simulated using Cadence SpectreRF. The LO-RF leakage caused by the LO mismatch in the Gilbert mixer is examined and analyzed for three scenarios of an ideal mixer, a non-ideal mixer with parasitic effects, and an ideal mixer with LO mismatches. The LO mismatch includes the phase mismatch only, the amplitude mismatch only and the combination of the two mismatches. It is found that if there is no LO mismatch, an ideal mixer will not have an LO leakage and DC offset. If a phase mismatch or amplitude mismatch exists, the LO leakage is proportional to the mismatch value. If both types of mismatches occur at the same time, the amplitude square of the LO leakage is equal to the sum of amplitude squares of each contribution. The relation between the mismatch and the LO leakage is derived. The analysis agrees with simulation results.

A novel even harmonic switching mixer implemented in a standard 0.18 μ m CMOS process for applications in 2.45GHz direct conversion receivers is also proposed. The mixer circuit overcomes the problems of DC offset and high flicker noise. The mixer gain is -8.24dB. The double sideband noise figure is 5.21dB at 100kHz. The IIP3 is 17.25dBm and the bias current is zero. The even harmonic technique eliminates the DC offset problem. Because the transistor bias current is zero and it works in the deep triode region, the flicker noise is very small. The conversion gain is less than unity, but it is not critical and can be compensated by using a low noise amplifier (LNA) with a high gain in the direct conversion receiver.

1.4 Organization of the Thesis

This thesis is organized into seven chapters. Chapter 1 provides an introduction to the problem faced in the design and objectives of the thesis.

Chapter 2 provides some background on the receiver architectures and fundamental parameters in receiver design. The advantages and disadvantages of the direct conversion architecture comparing to the heterodyne architecture are described.

Chapter 3 discusses the problem of DC offset of the mixer in the direct conversion architecture. Some typical DC offset cancellation techniques of the literature are illustrated in details.

Chapter 1

Chapter 4 shows the design of a CMOS double-balanced Gilbert mixer operating at the centre frequency of 2.45GHz for direct conversion applications. The analysis of LO-RF leakage of the mixer is performed by simulation and formulation.

Chapter 5 proposes a novel even harmonic switching mixer with DC offset free and low noise figure especially for direct conversion application.

Chapter 6 discusses some layout design issues and shows the layouts of the Gilbert mixer in Chapter 4 and the even harmonic switching mixer in Chapter 5. Finally the post-layout simulation results are compared with the schematic simulation results.

Chapter 7 concludes the thesis with a summary of results and some recommendations for further research in this area.

Chapter 2

Direct Conversion Receivers (DCR)

2.1 Direct Conversion Architecture

The direct conversion, also known as the homodyne or zero-IF conversion, is a natural approach to downconverting an RF signal directly to the baseband. This architecture, shown in Fig. 2.1, employs low-pass filtering in the baseband to suppress nearby interferers and select the desired channel. The quadrature down conversion (I and Q channels) is necessary in frequency modulated signals because in general the two sidebands of the RF spectrum are different. Mixing of the received RF signal with a real sinusoid would result in irreversible corruption of the information.

Figure 2.1 (a) Homodyne receiver for double-sideband AM modulation, (b) for frequency modulation.

The direct conversion architecture has some *advantages* comparing to the heterodyne architecture.

■ Image Rejection

In the homodyne architecture, the wanted channel is directly down-converted to base-band. To distinguish between positive and negative IF frequencies, which correspond to the upper and lower sideband of the RF signal, two mixers are used to generate a complex signal. The IF is supposed to be zero. Therefore, the image frequency of a channel consist of this channel itself. In this way, the problem of image rejection is circumvented.

■ Channel Selectivity Filters

The need of high quality factor bandpass filters in the heterodyne architecture is alleviated since the channel selectivity filter becomes a low-pass filter. Consequently, the channel selectivity filter can be fully integrated since there is no more need in accurate and high quality passive components. Power consumption of the filter is reduced since filter poles are located at the minimum possible frequency.

■ Reduction of Complexity

Several advantages can be achieved from the reduction of the complexity of the receiver architecture. As external components are avoided, higher impedance circuits can be used between cascaded blocks. The power consumption will be reduced accordingly. Full integration of the receiver also reduces the possible crosstalk between stages. In the zero-

IF architecture, only one oscillator is required in the receiver (with in-phase and quadrature component). The receiver may have the same frequency as the transmitter in Time Division Duplex Systems. However, the full compatibility will depend on the switching time accorded between reception and transmission.

The direct conversion architecture has some serious *drawbacks*. They are illustrated below.

■ DC Offsets

The most serious problem is the DC offset in the baseband section of the homodyne receiver. These extraneous offset voltages can corrupt the desired signals and/or saturate the following stages. They arise due to the self-mixing phenomenon of the local oscillator or of the in-band interferer caused by the element mismatches in the signal path circuitry.

To better understand the origin of these offsets, consider the received signal path shown in Fig. 2.2. First, the isolation between the LO port and the inputs of the mixer and the LNA is not perfect, and a finite amount of feedthrough exists from the LO port to the other mixer input and to the input of the LNA. Known as the *LO leakage*, this effect arises from capacitive and substrate coupling and, if the LO signal is provided externally, through bond-wire coupling. The leakage signal appearing at the inputs of the LNA and the mixer is now mixed with the original LO signal, thus producing a DC component at the output of the mixer. This LO self-mixing can be quite severe, and a time varying DC-offset occurs when the LO signal leaks out through the antenna, and is radiated and

reflected from nearby objects back to the receiver. A similar effect occurs if a large inband interferer (in the passband of the RF pre-selection filter) leaks from the LNA output to the mixer LO port and mixes with itself [11]. It should be noted that these DC-offsets exist in heterodyne receivers as well, but are mostly eliminated naturally by the IF band-pass filters.

Figure 2.2 Self-mixing problem caused by LO leakage

Thus, direct-conversion receivers require appropriate methods to remove undesired DC offsets. A simple approach is to use AC-coupling in the downconverted signal path. However, since the spectra of most spectrally efficient modulation schemes commonly used exhibit significant energy at DC, such signals are corrupted by AC-coupling filters. A better method is the use of baseband analog and/or digital signal processing (DSP) techniques for offset estimation and cancellation. However, these techniques add complexity and do not solve the problems associated with $1/f$ noise at low frequencies in CMOS implementations. A natural system solution to the DC offset problem in direct-conversion receivers is to minimize the baseband signal energy near DC by choosing a

“DC-free” modulation scheme and use AC-coupling for offset elimination. This approach has been successfully used in pager systems with the frequency shift keying (FSK) modulation, despite the spectral inefficiency of the FSK [1]. In the Chapter 3, some DC offset cancellation techniques will be discussed in detail.

■ LO Leakage

In addition to introducing DC offsets, leakage of the LO signal to the antenna and radiation from there creates in-band interference for other receivers using the same standard. This problem becomes less severe as more sections of RF receivers are fabricated on the same chip. With differential LOs, the net coupling to the antenna can approach acceptably low levels [2].

■ I/Q Mismatch

As mentioned earlier, for most currently used modulation schemes, a homodyne receiver must incorporate the quadrature downconversion. This requires shifting either the RF signal or the LO output by 90° . Since phase-shifting the RF signal generally entails a severe noise-power-gain tradeoff [2] and is especially difficult for the wideband signals used in high-data-rate systems, it is often desirable to shift the LO signal phase. In either case, the errors in the nominal 90° phase shift and mismatches between the amplitudes of the I and Q signal paths corrupt the downconverted signal constellation, thereby increasing the bit error rate. Note that all sections of the circuit in the I and Q paths contribute to gain and phase mismatches.

To gain an insight into the effect of I/Q mismatch, and show the versatility and convenience of using complex formulation, consider the practical case where the quadrature LO generates the complex signal $x_{LO}(t) = \cos(\omega_{LO}t) - j(1 + \varepsilon)\sin(\omega_{LO}t + \theta)$. Here, ε and θ represent LO gain and phase errors. One can rewrite the quadrature LO output as

$$x_{LO}(t) = \frac{1}{2} \left[1 - (1 + \varepsilon)e^{j\theta} \right] e^{j\omega_{LO}t} + \frac{1}{2} \left[1 + (1 + \varepsilon)e^{-j\theta} \right] e^{-j\omega_{LO}t} \quad (2.6)$$

Ideally, the complex LO output should contain only the negative frequency. However, from the above expression it is apparent that, due to gain and phase errors, there is a positive frequency component with a magnitude of $|1 - (1 + \varepsilon)e^{j\theta}|/2$. This component causes interfering images and, if not compensated for, can deteriorate the receiver performance. One can consider the effects of gain and phase mismatches separately. The magnitude of the undesired positive frequency component for the gain mismatch is $|\varepsilon|/2$, and for the phase mismatch $|\sin(\theta/2)|$, which can be approximated by $|\theta|/2$ when the phase mismatch is small.

Aside from the problems mentioned above, direct-conversion receivers are sensitive to even order distortions [12][13]. Also, since the downconverted spectrum is located around the zero frequency, the flicker ($1/f$) noise of the devices has a profound effect on the SNR, a severe problem in CMOS implementations [14]. Furthermore, integrating the high-frequency low-phase-noise channel-select frequency synthesizer is difficult to achieve with low-Q VCOs [5].

Despite all these problems, direct-conversion transceivers for digital mobile phones using the silicon bipolar technology have been in full production at Alcatel since 1991 [15]. The same company recently introduced a direct-conversion transceiver in a silicon germanium BiCMOS process [16] for the Global System for Mobile Communications (GSM) standards. In these transceivers, in order to handle the problems associated with static and dynamic DC offsets, DSP algorithms are used. These algorithms rely on the constant-envelope property of the modulation scheme used in GSM. To the best of the authors' knowledge, direct-conversion transceivers have not been used commercially in systems with nonconstant envelope modulation schemes, which are required in high-data-rate communication systems.

2.2 Recent Development of DCR

As discussed in the previous section, there are many challenging issues in the design of direct conversion receivers. Much research is being focused in the design and the improved the performance. In this section, some latest developments of direct conversion receivers are introduced. Due to the complexity of receivers, not all the components could be covered here. The emphases are focused on the structure of the DCR, the mixer circuits, and the LNA circuits and so on in the DCR.

2.2.1 Direct Conversion Receiver for GSM/GPRS/EDGE [17]

This work [17] describes a highly digitized direct conversion receiver of a single-chip quadruple-band RF transceiver that meets GSM/GPRS and EDGE requirements. The chip uses an advanced 0.25 μ m BiCMOS technology. The I and Q on-chip fifth-order

single-bit continuous-time sigma-delta ADC has 84-dB dynamic range over a total bandwidth of $\pm 135\text{kHz}$ for an active area of 0.4mm^2 . Most of the channel filtering is realized in a CMOS IC where digital processing is achieved at a lower cost. The systematic analysis of DC offset at each stage of the design enables to perform the DC offset cancellation loop in the digital domain as well. The receiver operates at 2.7V with a current consumption of 75mA.

The quad-band DCR is shown in Fig. 2.3. The low-band (LB) term is used for the GSM900 and GSM850 systems (880–960 MHz) and the high-band (HB) is for the DCS1800 and PCS1900 systems (1805–1990 MHz).

Figure 2.3 Block diagram of the implemented quad-band DCR.

The low-noise amplifiers (LNAs) consist of four differential transconductors recombined through a cascode stage into one common resistive load for each band. The RF outputs of

the LNAs are AC coupled to the in-phase (I) and quadrature-phase (Q) mixers so that the low-frequency distortion generated by the second-order nonlinearities in the LNA is blocked to prevent leakage through the mixer. The multiplier cells of the mixers use 1/2 or 1/4 sub-harmonic LO signal when high-band or low-band is selected, respectively [18][19]. This LO configuration ensures sufficient frequency separation between the VCO frequency and the largest received blockers and their harmonics. It avoids VCO pulling and the associated LO phase noise degradation that would degrade the sensitivity performance in presence of interferers. The baseband chain includes a third-order low-pass filter that prevents the interferers from saturating the high dynamic range 1-bit continuous-time fifth-order $\Sigma\Delta$ ADC. The bit-stream coming from the ADC drives a low-voltage slew rate controlled digital output buffer.

Fig. 2.4 shows the direct conversion double-balanced Gilbert mixer. This topology provides inherently high IIP2 [1], [12], [18], [19], [20]. The resistive 100Ω degeneration (R_{EE}) and the 7.8mA current consumption has been chosen to trade off NF, IIP3, and input impedance. Since the $1/f$ noise spectrum of the mixers falls on top of the desired signal at baseband, only small NPN bipolar transistor with 40 GHz f_T were used in the mixers design to avoid the effect of flicker noise at the mixer output [20]. Transistor Q1 (Q2) drives Q5–Q6 (Q3–Q4) and Q9–Q10 (Q7–Q8) switch core transistors of BBI and BBQ, respectively. When properly scaled, the I_1 , I_2 , I_3 , and I_4 current matching rely on the R_D resistors area while the switch core Q3–Q10 transistors can remain small. As a result, the parasitic capacitors are small. Thus, the LO transitions are sharp and the

random modulation of the switching time instants are small. Consequently, the flicker noise at the mixer output is minimized.

Figure 2.4 Circuit diagram of the mixer.

There is a 5mV DC offset at the mixer output. However, the total baseband filter (*BBF*) amplification of the baseband chain is 25dB. Therefore, the 5mV DC offset will result in 89mV DC offset at the *BBF* output. This amount of DC offset does not overload the ADC and can be fully cancelled by the digital baseband processor.

2.2.2 GSM/EGSM/DCS/PCS Direct Conversion Receiver [21]

This work [21] presents a direct conversion receiver implemented with a 0.35 μ m BiCMOS technology operating in GSM/EGSM/DCS/PCS band. The receiver has a

66dBm IIP2, a 90kHz bandwidth and draws 57/63mA from a 2.7V supply. Fig. 2.5 shows the receiver block diagram.

Figure 2.5 Receiver block diagram: LNA, PPF, HM, 3-stage PGA, 8-pole LPF, 3-stage DCOC, and fractional-N synthesizer with integrated loop filter.

In Fig. 2.6, the LNA schematic is shown. It is designed by a differential cascaded common source with degeneration inductors, which are realized by bonding wire. For reducing chip area, the four LNAs for four modes are merged into GSM and EGSM LNAs, and DCS and PCS LNAs. For covering both modes for each LNA, the quality factor of the inter-stage matching between the LNA and the following block should be decreased. In this design, the following block is the 400Ω -poly-phase filter (PPF), which generates the quadrature signals at the signal paths. Thus, the quality factor of inter-stage matching circuit is decreased by the resistive load, and wide-band matching can be achieved naturally.

Figure 2.6 Differential LNA schematic with gain control for the GSM/EGSM and DCS/PCS mode ($N=9$)

To improve the DC offset characteristic, the harmonic mixer (HM) circuit in Fig. 2.7 is adopted [21]. In this HM, the LO frequency is different from the RF frequency. Only the second harmonic component of the LO signal contributes to the self-mixing by the radiated power, and this contribution is negligible. To remove the down converted strong interferer, the 327pF internal capacitor, which is implemented with stacked capacitors, between differential nodes at the output of mixer is connected. To increase the IP3 of the mixer, the passive resistance is used as degeneration impedance in order to reduce the chip area.

Figure 2.7 Harmonic mixer schematic and LO conduction diagram.

The baseband chain consists of filters and programmable gain amplifiers (PGAs) to provide required selectivity and gain. The performance of filtering, amplifying, and canceling the DC offset at the mixer output makes an effect on the linearity and noise characteristics of the receiver full path. In this design, the low-noise baseband amplifier with low-pass filtering and DC offset canceling is located at the mixer output to overcome noise contribution from the next stages and to remove large blocker signals efficiently at the same time. As shown in Fig. 2.8, the PGA circuit has been partitioned into three sub-blocks according to their functions, which are: 1) the differential gain amplifier; 2) the common-mode feedback (CMFB); and 3) the DC offset corrector (DCOC) blocks [22]. The R - $2R$ ladder network is used as degeneration impedance and decibel-linear gain control.

Figure 2.8 Block diagram of the PGA

2.2.3 Front-End of DCR for CDMA-2000 [23]

This work [23] describes the front-end of a highly integrated dual-band direct-conversion receiver IC for CDMA-2000 mobile handset applications. The RF front-end included a CELL-band low-noise amplifier (LNA), dual-band direct-conversion quadrature I/Q down-converters, and a local-oscillator (LO) signal generation circuit. The LNA had a noise figure of 1.2 dB and input third-order intermodulation product (IIP3) of 9 dBm. I/Q down-converters had a noise figure of 4–5 dB and IIP3 of 4–5 dBm and IIP2 of 55 dBm. An on-chip phase-locked loop and external voltage-controlled oscillator generates the LO signal. The receiver RFIC implemented in a 0.35 μ m SiGe BiCMOS process meets or exceeds all CDMA-2000 requirements when tested individually or on a handset.

The block diagram of the receiver is shown in Fig. 2.9. The receiver block diagram consists of the RF portion, which includes the low-noise amplifier (LNA) and the direct-conversion quadrature down-conversion mixers. These also demodulate the received

Chapter 2

signal into in-phase (I) and quadrature (Q) components, thus referred to as the demodulator block (DMD). The RF portion of the chip supports two frequency bands of CELL and PCS, which cover 869–894 and 1930–1990 MHz, respectively. The chip can also support the Korean band (1840–1870 MHz) and the IMT2000 band (2110–2170 MHz) without any on-chip modifications. The RF portion also includes the circuitry required to generate and amplify the local LO signal for the quadrature down-conversion. The baseband I and Q components of the received signal with a bandwidth of 615 kHz are combined for the CELL and PCS receiver paths using a shared resistive load and feed the I and Q channels of the analog baseband portion of the chip.

Figure 2.9 Simplified block diagram of a direct conversion receiver

The baseband portion of the RFIC consists of a variable-gain baseband amplifier (BBA) and a two-stage variable gain amplifier with DC offset compensation circuitry. The three variable gain blocks provide about 90dB of gain range in 3-dB steps. DC offset compensation is performed at multiple stages of the baseband circuit to prevent build up at the ADC input. The DC offset is removed from the baseband path using a combination of high-pass filtering and dynamic and static offset compensation.

The baseband filter is a seventh-order active *RC* architecture with an elliptical frequency response. It provides over 70 dB of rejection at a 900-kHz offset from the center of the desired channel. The cascaded bi-quads of the filter are individually optimized for noise figure, linearity, power consumption, and die size. The corner frequency of the filter is tuned externally at around 615 kHz.

An Integer-*N* synthesizer is used to lock the external voltage-controlled oscillator (VCO) frequency using an externally referenced voltage-controlled temperature-compensated crystal oscillator (VCTCXO) signal. The required VCO frequency is twice that of the LO frequency for the PCS band and four times the LO frequency for the CELL band. The VCO signal is buffered to feed the PLL prescaler and the divider circuits for the quadrature LO generation. The PLL consists of a BiCMOS prescaler with dual-modulus control, CMOS programmable dividers and reference divider, CMOS phase/frequency detector, and a CMOS charge pump.

A 3-b serial interface is provided for programming internal data resistors that control the functionality of the chip. The 16-b data registers are loaded serially and are used to program the PLL, power up individual blocks, set gain levels, adjust dc currents, and perform other digital controls such as performance tuning. Separate central biasing blocks are provided for the RF and BB portions of the IC. The bias included reference currents which are fixed over temperature or varied proportional to absolute temperature (PTAT). External resistors are used to set accurate reference currents.

Figure 2.10 Simplified schematic diagram of the quadrature mixer

A highly optimized Gilbert-cell mixer with common-emitter bipolar RF stage and inductor degeneration is selected for this design (Fig. 2.10). To minimize die area, differential inductors are used for the emitter degeneration. Sharing the degeneration inductors in the RF stage results in improvement in the IIP3 since twice as much current will flow through the inductors. The most compact inductor configuration is chosen because the Q-factor of these inductors does not affect the noise figure performance. The bias circuits of the RF stage and the LO stage are optimized for the tight headroom in the Gilbert mixer arrangement that has to tolerate process and temperature variations with a supply voltage of 2.7 V. The tight headroom is particularly profound when combined with the large LO signal swing applied to the quad-switching transistors (Q3–Q6). The DC bias for the base voltage of these transistors is critical for good IIP3 performance. Optimization of this type of mixer has been presented extensively [24], [25].

The mixer load resistor is made variable to control the gain and the common-mode voltage of the baseband signal and to guarantee adequate headroom for the mixers under process variations. The gain is selectable using a 3-b digital code and is controlled by the digital signal processing (DSP) software. The common-mode voltage level at the input to the baseband blocks is critical for proper operation of these blocks. This common-mode voltage, which propagates through the baseband circuits, can be tuned externally. A common-mode detector circuit senses the common-mode voltage, which is then used by the DSP to tune the mixer load resistors. The resistor tuning is done by switching a number of parallel resistors in and out using MOS switches controlled by the 3-b digital signal. The mixer load also consists of large capacitors that form an RC pole in

combination with the mixer load resistor. External 270-pF capacitors are used for setting appropriate corner frequency of this first-order low-pass filter. This RC filter is used to attenuate the single-tone interferer which has been amplified by both the LNA and the mixer. Any attenuation of the single-tone at this point lowers the dynamic range requirement of the active low-pass filter in the baseband block.

2.2.4 Discussion on the mixers used in the DCRs

From the description of DCRs in the previous sections, it is found that the direct conversion mixers are mostly implemented using the BiCMOS process at present, which is more expensive than the standard CMOS process. This is due to some problems in the CMOS direct conversion mixers. The CMOS mixers have a higher average noise figure caused by flicker noise. The LO-RF leakage, which causes the DC offset in direct conversion receivers, is also larger in the CMOS mixers due to the required larger CMOS switching pair in the mixer.

Let us now summarize how the DC offset problem is solved in the DCRs of the previous sections. In [17], the DC offset is cancelled by DSP techniques in the baseband. In this technique, it must ensure that the DC offset does not saturate the ADC after amplified by the baseband filters. In [21], the harmonic mixing technique is used to prevent the DC offset in the mixer caused by the LO-RF leakage. In [23], the DC offset is cancelled by high pass filtering. DC blocking capacitors are placed before ADCs shown in Fig. 2.9. The detailed DC offset cancellation techniques in the direct conversion receivers will be presented in Chapter 3.

Chapter 3

DC Offset Cancellation Techniques in DCR

There are three main causes of LO leakage, which result in DC offset voltages at the mixer output, (i) the poor isolation between the LO port and RF port of the mixer, (ii) the coupling between the mixer LO port and the LNA, and (iii) in general, any amount of coupling such as capacitive coupling, substrate coupling and bond-wire coupling from the LO port to the signal path. The leaked LO signal is then mixed with itself and produces a DC offset at the output of the mixer. Apart from self-mixing, circuit imperfections due to process-mismatch can introduce serious amounts of DC at the output of the mixer. While the self-mixing related DC offset can exhibit a rapid changing nature, process-mismatch related DC offset changes only with temperature variations and aging [2].

There are several investigations done on the DC offset cancellation. Most approaches to remove the offset have so far been focused on three methods. For modulation formats that have no or little spectral power at DC, the AC coupling at the mixer output, or at some downstream stage, can be used to remove the offset. To avoid unacceptable distortion due to tracking the lower frequency spectrum of the signal, the AC coupling requires large capacitances that are not realizable on-chip [26][27]. Furthermore, the AC coupling using a large capacitor often results in a failure to track fast variations in the offset voltage [7]. If the capacitor value is large, the charging and discharging time of the

AC coupled high pass filters are long. Therefore, the filters are slow and cannot track fast variations of offset voltage.

The second common approach to remove offsets is to apply a digital cancellation algorithm to the sampled signal before the decision device [5]-[7][28][29]. In this approach the offset is detected and removed digitally by time averaging or by using more complex methods such as differentiating the received signal [28]. However, the digital cancellation technique requires analog baseband stages with large spurious-free dynamic ranges (*SFDR*) to tolerate the DC offset. It also requires more bits (as many as 5 or 6 more bits) in the ADC to achieve the same sensitivity and bit error rate as when the offset is not present.

The third approach involves the modification to the Gilbert cell [30] or replaces it with other mixing circuits instead, such as harmonic mixers [8]-[10], because the DC offset is an inherent problem of Gilbert cell. In the following sections, some DC-offset cancellation techniques are illustrated.

3.1 Feed-Forward or Feed-back DC-Offset Compensation

The system level description of the feed-forward approach is presented in Fig. 3.1 [31]. The signal at the output of the mixer is fed to an A/D converter and the DC value of the signal is measured. When the received signal strength is high enough, signal variations are partially represented at the output of the A/D block. Using this method, the mean of the signal is traced in the DSP domain. Different approaches for effectively extracting the

mean of the noisy signal will be discussed later in this section. The estimated DC offset, which is the error signal, is fed through a control algorithm which can be as simple as a look-up table. The output of the control unit is fed to a latch and is updated periodically. Choosing the update period as large as the DC offset variations, the noise contribution due to the DC level shifter becomes limited. The aim of this approach is not to completely remove the DC offset, but reducing its magnitude to a level where it does not saturate the following stages. Although the DC offset is not completely removed in this method, its effect is suppressed to avoid the saturation of the baseband circuits. The authors do not state the details of A/D. This work is focus on illustration of the method of DC offset cancellation.

Figure 3.1 Feed-forward DC-offset compensation

The process mismatch induces a quadratic LO component at the output of the mixer. Hence, if a proper DC offset on the LO signal is induced, this quadratic dependence can be exploited for compensation. The system level diagram of the feed-back DC offset compensation is shown in Fig. 3.2. As in the feed-forward compensation approach, the DC offset is sensed through an A/D converter and its mean is computed. The control block produces the corresponding control signal which can have high frequency noise contributions due to errors in the estimate of the signal mean. Thus a latch with a periodical update of the signal is necessary and the update period should be chosen as large as the DC offset variations permit. This technique is too complex and may not be applicable to practical mixer circuits. It has not been seen in the industry.

Figure 3.2 Feed-back DC-offset compensation

3.2 DC-Offset Canceller

A canceller constructed from analog and digital signal processing circuits is suitable for the reception of burst mode QPSK signals such as those employed in the *NADC* (North American Digital Cellular) and *PHS* (Personal Handy-phone System) systems [32]. The time-invariant DC components are removed in the analog stage, and the time-variant components in the digital stage. Fig. 3.3 shows the DC offset canceller. It consists of analog subtractors at the input port of the LPFs, digital subtractors subsequent to the ADCs, digital-analog converters (DACs) to supply DC data to be cancelled into the analog subtractors, averaging circuits to detect the DC offset in the output of the ADCs, and memories to store the detected DC data. The analog-stage canceller functions as follows. First, the time-invariant DC offset value is estimated by disconnecting the LNA from the antenna and terminating the input port in the stand-by period, and is stored in the memories. Since a different DC offset is produced at each gain mode, the DC offset in the respective gain mode is estimated and stored in the memories table. In the operation mode, the stored DC offset value is read out in accordance with a corresponding gain mode and is fed back to the analog subtractor through the DAC to compensate the inherent DC offset.

Figure 3.3 DC-offset canceller

The digital-stage canceller is activated in the burst mode of TDMA systems to which every channel consists of repetitions of frames, which includes multiple slots. The digital-stage canceller is composed of the averaging circuit and digital subtractor in Fig. 3.3. Averaging circuit consists of an accumulator, a divider, and a latch circuit (Fig. 3.4). Fig.3.5 shows the procedure. Digitized signals including DC offset are accumulated for a predetermined time period. The accumulated result is then divided by the time period to obtain the mean value, which is considered to be the DC offset because the original QPSK mean value approaches zero with sufficiently long time averaging. The DC value held in the latch circuit is subtracted from the input signal during the following receiving slot, while the averaging circuit is activated again to obtain the DC value in the slot. Applying this procedure repeatedly, the DC offset can be removed completely and dynamically in the time-varying environment, and a remarkable receiving characteristic is obtained.

Figure 3.4 Detail of the averaging circuit

Figure 3.5 Cancellation procedure

The DC offset can be completely removed by the digital-stage canceller only if the sum of the time-invariant and time-variant DC values is sufficiently small not to saturate the ADC in receiving a large signal. However, if a larger DC offset is fed to the ADC, the ADC is saturated in the receiving the large input signal. In the proposed canceller, which utilizes the analog-stage canceller together with the digital-stage canceller, the time-invariant DC offset is removed to prevent the saturation of the ADCs.

3.3 Self-Mixing-Free Harmonic Mixer

The DC offset arises because the RF carrier and the LO signal operate at exactly the same frequency as shown in Fig. 3.6(a). For the harmonic mixing shown in Fig. 3.6(b), it is the second harmonic of the LO signal that takes part in the mixing process. As a result, the LO leakage does not generate a DC component but an output which is still situated at the LO frequency and can be easily filtered out [33].

Figure 3.6 Working principles of (a) the conventional mixer and (b) the harmonic mixer

A CMOS balanced harmonic mixer is shown in Fig. 3.7(a). The second harmonic is easily obtained because of the inherent square-law operation of the CMOS transistor. The LO stage is actually a squaring cell which converts the differential LO voltage to the time-varying current which contains the second harmonic. In principle, the fundamental and all odd harmonics of the LO will be cancelled out at the connected drain terminals and the DC offset problem will be mitigated. The self-mixing-induced DC offset is about 44dB lower than that of the conventional mixer.

Figure 3.7 CMOS harmonic mixers

However, its noise performance is still largely degraded by the severe flicker noise. To eliminate the effect of flicker noise, lateral bipolar devices were used to replace MOS transistors at the RF stage of the mixer as shown in Fig. 3.7 (b) [10]. The LO stage has no flicker noise contribution at the mixer output due to the noise up-conversion and the common-mode operation while the RF stage has a very low flicker noise corner due to the bipolar mode. A double balanced harmonic mixer can also be used to improve the linearity [34]. An alternative topology of harmonic mixer is constructed by cascading 90° (LO_{90}) and 270° LO (LO_{270}) switches with 0° (LO_0) and 180° LO (LO_{180}) switches, respectively. The input RF signal behaves as if it is mixed with an LO signals with a non-50% duty cycle. Hence, this topology generates the LO even harmonics [9]. (Fig. 3.7 (c))

This mixer can achieve 87dB DC offset cancellation. We can see it uses more transistors comparing to Fig. 3.7 (a) and (b), but it achieves a better performance.

3.4 Offset Current Cancellation Technique

The basic circuit structure considered is the Gilbert cell mixer. Offsets are cancelled by dynamically varying the bias on the loads [30]. Fig. 3.8 shows how the operation of a Gilbert cell is affected by the offset current. A fraction of the LO signal gets coupled to the RF input (added to the desired signal) and the transconductors M1-M2 convert it into a current signal. The combined RF current signal (leaked LO signal plus the desired) is downconverted to the baseband by the switches M5-M8. The LO portion self-mixes causing an offset current to appear in the legs above the switches. This undesired offset current is then converted to an undesired offset voltage in the loads. However, if we can control the biases of M3-M4 to produce a cancellation current equal to the offset current, no voltage offset will appear at the differential output.

Figure 3.8 Differential current offsets in the Gilbert cell are cancelled by M3 and M4

This method can detect the dynamic offsets, while maintaining a good steady state performance, by employing an adaptive digital "gear shifting" approach. The basic idea is to utilize two IIR filters (one slow, one fast). When the offset is stationary, the slow filter detects and tracks the offset. However, when there is a sudden change in value of the offset, the slow loop can no longer provide a good estimator for the offset. This situation is detected when the outputs of the fast and slow filters differ by more than a pre-designated threshold. When this occurs, two things happen. First, the fast mode IIR filter's output is used. Second, its data history replaces the data history in the slow mode

IIR filter. This method has been simulated and been shown to perform well in tracking dynamic offsets [35].

The complete mixer design, including the Gilbert cell, the differential offset cancellation circuitry and the common-mode feedback (*CMFB*), is shown in Fig. 3.9. The differential cancellation circuitry is controlled by a 6-bit DAC to cancel the differential offset voltages. The *CMFB* fixes the output voltage and reduces even order distortions caused by the offset cancellation.

As shown, this method needs mixed signal circuits to detect the offset current. The circuit is much more complicated than the harmonic mixer. Therefore our direct conversion mixer design is focused on the topology of harmonic mixing. Chapter 5 will propose a novel CMOS even harmonic switching mixer.

Figure 3.9 Circuit diagram of the adaptive cancellation mixer

3.5 Offset Cancellation loop through VGA

In the conventional Gilbert cell mixer, second-order intermodulation currents, generated by the input transconductor, are directly transmitted at the mixer output, due to switching devices and load resistors mismatch. Fig. 3.10 shows the schematic of the mixer [36]. The input transconductor is formed by a PMOS fully differential input stage shunting an *LC* degenerated NMOS stage. In this way, the switching stage current is the difference between the NMOS and the PMOS currents. Although fully differential transconductors produce lower second-order distortion, an *LC* degenerated NMOS stage has been chosen.

Figure 3.10 Mixer schematic

To reduce the third-order nonlinearity due to the switching stage, an LC filter resonating at twice the LO frequency has been introduced between common source and ground. The filter gives a low common-mode impedance at twice the local oscillator frequency, i.e., reducing the common-mode oscillation at the switching pair common source, increasing IIP3 [37]. The impact of the filter on gain and noise performances is limited because, for differential signals, it is equivalent to a small capacitance [37].

The first baseband block, the VGA, allows adjusting receiver gain to limit the output signal level. A simplified schematic is shown in Fig. 3.11(a). The input stage is a degenerated differential pair of MOS devices, biased in the linear region, shunting fixed value resistors. The input stage transconductance and therefore the amplifier gain are varied by varying the MOS resistance. Large input devices are used to lower flicker noise. Moreover, the large aspect ratio ($3000\ \mu\text{m}/1\ \mu\text{m}$) forces the transistors in the weak inversion region for maximum transconductance. To maximize the voltage gain the resistive load ($1.2\ \text{k}\Omega$) is differential while two PMOS devices provide current to the input stage. This configuration requires a common-mode feedback but has the advantage of a lower DC voltage drop. The flicker noise of the PMOS current sources has a negligible impact on the noise figure. The VGA output capacitors implement, together with the resistors, an 8-MHz pole, further lowering in-band and out-of-band blockers.

Figure 3.11 (a) VGA schematic, (b) offset cancellation loop block diagram.

An offset cancellation loop is built around the VGA, as shown in Fig. 3.11(b). The DC output voltage difference is sensed by a Miller integrator which varies the mixer output differential voltage (DC connected to the VGA input) by means of a transconductor driving stage.

While the VGA has no impact on the receiver out-of-band IIP3, due to the filtering action of the mixer, it determines the in-band IIP3. Simulations in this work provide an in-band IIP3 equal to 3 dBm, referred to $50\ \Omega$, and $4\text{ nV}/\sqrt{\text{Hz}}$ equivalent input-referred noise voltage spectral density, in maximum gain condition. The voltage gain can be varied between 0 and 16 dB. The 1-dB compression point in minimum gain condition is 5 dBm. The VGA together with the offset cancellation loop consumes 1 mA.

Chapter 4

Gilbert Mixer Design and LO Leakage Analysis

In this chapter, the analysis and design of CMOS mixers for direct conversion receivers have been explored. A CMOS double-balanced Gilbert mixer operating at the centre frequency of 2.45GHz for direct conversion applications is designed using Cadence SpectreRF for the Chartered 0.18 μ m CMOS Digital/Analog/RF process. Many SpectreRF analyses are used in the simulations. They are Periodic Transfer Function (PXF) analysis for conversion gain, Periodic Steady State (PSS) analysis for 1dB compression point and conversion gain, Periodic Distortion (Pdisto) analysis for IIP3, and Periodic Noise (Pnoise) analysis for noise figure. The LO-RF leakage caused by the LO mismatch in the Gilbert mixer is examined and analyzed for two scenarios of an ideal mixer and a mixer with LO mismatches. The LO mismatches include phase mismatch only, amplitude mismatch only and the combination of the two mismatches.

4.1 CMOS Gilbert Mixer Design

A CMOS double-balanced Gilbert cell mixer operating at the center frequency of 2.45GHz (Fig. 4.1) is designed by Cadence SpectreRF using the Chartered 0.18 μ m CMOS Digital/Analog/RF Technology file.

Figure 4.1 Double-balanced Gilbert cell mixer

The switching transistors are biased at the edge of saturation. Two transistors out of four are made to conduct in the saturation region by the LO signal. The conversion gain given by this mixer can be calculated using equation (4.1), where $(W/L)_{rf}$ and I_{rf} denote the aspect ratio and the DC drain current of transistor M0 and M1, while R_L denotes the load resistors, $R0$ and $R1$.

$$\frac{V_{BB}}{V_{rf}} = \frac{2}{\pi} \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{rf} I_{rf} R_L} \quad (4.1)$$

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Assuming that only two out of four switching transistors are conducting in saturation region at anytime, the input referred noise spectral density and the noise figure of the mixer are given by equation (4.2) and (4.3) respectively [38].

$$\overline{V_{ni}^2} = 8kT \frac{1}{g_{mRF}^2 R_L} + \frac{16}{3} kT \frac{1}{g_{mRF}} + 4kTR_{Bias} + \frac{8}{3} kT \frac{g_{mlo}}{g_{mRF}^2} + \frac{4K_N}{g_{mRF}^2 W_{lo} L_{lo} C_{ox} f} \quad (4.2)$$

$$NF = 10 \log(1 + \frac{\overline{V_{ni}^2}}{4kTR_s}) \quad (4.3)$$

where the *RF*, *lo*, *Bias*, *s* and *L* subscripts denote that the parameters belong to the transconductance transistors (M0-M1), the switching pair transistors (M2-M5), bias resistors, the source and load respectively. K_N is the $1/f$ noise coefficient of NMOS transistor. The gain and the noise equations are derived based on long channel MOS model, hence the non-ideality caused by short channel devices are ignored. As you noticed, there is no flicker noise of transconductance MOS (M0, M1) in the equation (4.2). That is because the noise in the two MOS transistors accompanies the RF input signal, and is translated in frequency just like the signal is. Therefore, flicker noise in these MOS is upconverted to ω_{LO} and to its odd harmonics, while white noise at ω_{LO} (and its odd harmonics) is translated to DC. If the output of interest lies at zero IF, then the transconductance MOS only contribute white noise after frequency translation [20].

As the output signal of the direct conversion mixer is at the baseband, the flicker noise is dominant. In choosing the transistor size, the aspect ratio of the switching pair transistors should be increased to reduce noise and to increase the conversion gain. Increasing the bias current also helps in reducing noise. The LO bias voltage is carefully chosen so that

v_{lo} can exactly turn on/off the M2-M5. In this way, the conversion gain is maximized. The RF bias voltage is used to obtain the drain currents of M0 and M1. The circuit parameters and biasing conditions are tabulated in Table 4.1. All of the transistors are implemented using the RF MOS transistors.

Table 4.1 Mixer circuit parameters and biasing conditions

Parameters	Values
W/L (M0-M1)	60 μ m/0.18 μ m
W/L (M2-M5)	100 μ m/0.18 μ m
R0-R1	300.09 Ω
R2-R5	5 k Ω
Voltage source	2.5 V
DC bias at LO input	1.35 V
DC bias at RF input	650.2 mV
M0 drain current	2.23 mA

In the following subsections, the simulated performance parameters of the ideal symmetrical mixer are illustrated, including conversion gain, bandwidth, input referred 1dB compression point, input referred IP3, noise figure and power consumption.

4.1.1 Conversion Gain and Bandwidth

In the direct conversion, the RF frequency is set to be same as LO frequency, 2.45GHz. So the output IF frequency is 0Hz, which is a DC value. In order to distinguish the DC

output from the DC biasing voltage, a differential output is chosen so that the DC biasing voltages are cancelled out. Therefore the conversion gain here is referred to the differential conversion gain. It is shown in equation 4.4. Normally differential conversion gain is 6dB higher than the single-ended gain.

$$Gain = 20 \log\left(\frac{V_{BB+} - V_{BB-}}{V_{rf}}\right) \tag{4.4}$$

Figure 4.2(a) shows the conversion gain of the mixer when the LO is held constant at 2.45GHz and while varying the RF frequency from 2.4GHz to 2.5GHz. It shows that the mixer has flat gain across the simulated frequency range. The gain value is 15.3dB. Figure 4.2(b) shows the gain when RF is swept from 1.45GHz to 3.45GHz, we can see that at point A and point B, the gain is 3dB lower than the peak value.

(a)

(b)

Figure 4.2 (a) Differential conversion gain, (b) bandwidth at $f_{LO}= 2.45\text{GHz}$

In order to investigate the mixer bandwidth, the RF frequency is set at the same value as the LO frequency and both are swept together. In this case, IF frequency is always 0Hz. In Fig. 4.3, when the frequency increases to 9GHz, the gain decreases to 12.35dB, which is about 3dB lower than the gain at 2.45GHz.

Figure 4.3 Mixer bandwidth with respect to f_{LO} variation

4.1.2 Input Referred 1dB Compression Point and IIP3

The small signal gain of a circuit is usually obtained with the assumption that the gain is constant and the harmonics are negligible. However, as the input signal reaches a certain level, the gain of the circuit begins to drop. This effect is quantified by the “ 1dB compression point, ” which is defined as the input signal level that causes the small signal gain to drop by 1dB. The 1dB compression point of the designed mixer is shown in Fig. 4.4, which is -11.71dBm.

Figure 4.4 Input referred 1dB compression point

The corruption of signals due to the third-order intermodulation of two nearby interferers is so common and so critical that a performance parameter has been defined to characterize this behavior. It is called the “ third intercept point” (IP3). Plotted on a logarithmic scale, the magnitude of the IM products grows at three times the rate at which the fundamental components increase. The third-order intercept point is defined by the intersection of the two lines. The horizontal coordinate of this point is called the input IP3 (IIP3). The IIP3 point of the designed mixer is shown in Fig. 4.5, which is 0.43dBm.

Figure 4.5 Input referred IP3

4.1.3 Noise Figure and Summary of Performance Parameters

The presence of flicker noise at the signal band immediately at the output of the downconversion mixers is a significant drawback of the direct conversion architecture. The linearity requirements limit the acceptable gain of the LNA typically to less than 25dB in the front-end, and hence the effect of flicker noise cannot be eliminated by increasing the gain. Fig. 4.6 shows that the double sideband noise figure is 32dB at 100kHz. It is so high that the mixer is better to use in the modulation formats that have no or little spectral power at DC.

Figure 4.6 Double sideband noise figure

All the performance parameters discussed in the previous subsections are shown in Table 4.2 below.

Table 4.2 Summary of performance parameters

Gain (dB)	BW (GHz)	1dB (dBm)	IIP3 (dBm)	NF (dB)	Power (mW)
15.26	9	-11.71	0.43	32.00	11.15

4.2 Theoretical Analysis of LO-RF Leakage due to LO Mismatch

In this section, the theoretical analysis of LO-RF leakage caused by the LO mismatch in double-balanced CMOS Gilbert mixers is analyzed in four cases, no LO mismatch, LO phase mismatch only, LO amplitude mismatch only and the combination of the two mismatches.

Figure 4.7 (a) Double-balanced mixer, (b) single-balanced mixer

4.2.1 Assumptions

Before starting the analysis of the common mode LO leakage, some reasonable assumptions should be made to simplify the problem. Without loss of generality, consider the single-balanced mixer in Fig. 4.7. Firstly, it is assumed that the circuit switches sharply, that is, a small LO voltage change causes the current of V-I converter (M0) to completely switch from one side of the differential pair to the other, see Fig. 4.8. Secondly, the small signal current caused by the RF input is considered as negligible comparing to the M0 biasing current. Therefore only this biasing current is switched by the LO signals. Thirdly, C_{gb} and C_{sb} in the small signal equivalent circuit of M0 are ignored to further simplify the results. C_{gb} is normally ignored when the transistor works

in the saturation region [39]. C_{sb} is neglectable because the source and body of M0 are tied together.

Figure 4.8 Current switching by LO signals

4.2.2 No LO Mismatch

First consider the M0 biasing current. In order to reflect the behavior of sub-micrometer transistors, short channel modulation effects should be taken into account. An acceptable MOSFET model in the saturation region is

$$I_{bias\sin g} = K(V_{GS0} - V_{th})^2 [1 + \lambda(V_{DS0} - V_{eff0})] \quad (4.5)$$

where V_{GS0} and V_{eff0} are the gate-source voltage and saturation voltage of M0 in Fig. 4.7(b), V_{th} is the threshold voltage, K is the current factor. λ is the channel length modulation coefficient. Assume M1 is turned ON when V_{LO-} is positive. V_{DS0} is the drain-source voltage of M0, that is, the common source voltage of the switching pair. So it can be written as

$$V_{DS0} = V_{LObias\sin g} + V_{LO-} - V_{eff1} - V_{th} \quad (4.6)$$

where $V_{LObiasing}$ is the biasing voltage of the switching pair, $V_{LO-} = A \sin \omega_{LO} t$ is the LO signal injected to M1. V_{eff1} is the saturation voltage of M1. Substitute equation (4.6) into equation (4.5), and rearrange it. We get

$$I_{biasing} = I_0 [1 + \lambda(V_{LO-} + V_{dc})] = (1 + \lambda V_{dc}) I_0 + \lambda I_0 V_{LO-} \quad (4.7)$$

in which

$$\begin{aligned} I_0 &= K(V_{GS0} - V_{th})^2 \\ V_{dc} &= V_{LObiasing} - V_{eff0} - V_{eff1} - V_{th} \end{aligned}$$

Note the M0 biasing current is not a constant current now, but a function of V_{LO-} .

Now let us get each drain current of the switching pair. When $V_{LO+} > 0$, M2 switches ON and M1 switches OFF, and a current equal to $I_{biasing}$ appears in the right branch. In the next half period, the current switches to the left branch. Then, each drain current of the switching pair should be equal to $I_{biasing}$ times a square-wave at the frequency of f_{LO} ,

$$S(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin n\omega_{LO} t, \quad (4.8)$$

where n is an odd integer.

Drain current of switching pair I_{D1} and I_{D2} are as the following,

$$\begin{aligned}
I_{D1} &= I_{bias\ sin\ g} \times S(t) \\
&= (1 + \lambda V_{dc}) I_0 \times \left(\frac{1}{2} + \frac{2}{\pi} \sin \omega_{LO} t + \frac{2}{3\pi} \sin 3\omega_{LO} t \right. \\
&\quad \left. + \frac{2}{5\pi} \sin 5\omega_{LO} t + \dots \right) + \frac{\lambda I_0 A}{\pi} + \frac{\lambda I_0 A}{2} \sin \omega_{LO} t \\
&\quad - \frac{2\lambda I_0 A}{\pi} \left(\frac{1}{1 \times 3} \cos 2\omega_{LO} t + \frac{1}{3 \times 5} \cos 4\omega_{LO} t + \dots \right)
\end{aligned} \tag{4.9}$$

$$\begin{aligned}
I_{D2} &= I_{bias\ sin\ g} \times S\left(t - \frac{T_{LO}}{2}\right) \\
&= (1 + \lambda V_{dc}) I_0 \times \left(\frac{1}{2} - \frac{2}{\pi} \sin \omega_{LO} t - \frac{2}{3\pi} \sin 3\omega_{LO} t \right. \\
&\quad \left. - \frac{2}{5\pi} \sin 5\omega_{LO} t - \dots \right) + \frac{\lambda I_0 A}{\pi} - \frac{\lambda I_0 A}{2} \sin \omega_{LO} t \\
&\quad - \frac{2\lambda I_0 A}{\pi} \left(\frac{1}{1 \times 3} \cos 2\omega_{LO} t + \frac{1}{3 \times 5} \cos 4\omega_{LO} t + \dots \right)
\end{aligned} \tag{4.10}$$

We are interested in the common source current of the switching pair, so the sum of the I_{D1} and I_{D2} is

$$\begin{aligned}
I_{common_source} &= I_{D1} + I_{D2} \\
&= (1 + \lambda V_{dc}) I_0 + \frac{2\lambda I_0 A}{\pi} \\
&\quad - \frac{4\lambda I_0 A}{\pi} \left(\frac{1}{1 \times 3} \cos 2\omega_{LO} t + \frac{1}{3 \times 5} \cos 4\omega_{LO} t + \dots \right)
\end{aligned} \tag{4.11}$$

From above, we can see all the odd harmonics have been cancelled out including the fundamental frequency ω_{LO} . Therefore there are no fundamental frequency signals that can feedthrough to the RF port. So an ideal mixer has no LO leakage and DC offset. This is consistent with the simulation results.

4.2.3 LO Phase Mismatch Only

Let us consider only the fundamental frequency term of I_{common_source} . Assume there is a mismatch of θ degrees between LO+ and LO-, then

$$\begin{aligned}
 I_{common_source} &= I_{D1} + I_{D2} \\
 &= D \sin(\omega_{LO}t + \frac{\theta}{2}) + D \sin(\omega_{LO}t + \pi - \frac{\theta}{2}) \quad (4.12) \\
 &= 2D \cos \omega_{LO}t \sin \frac{\theta}{2} \approx D\theta \cos \omega_{LO}t
 \end{aligned}$$

where

$$D = \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda A}{2} \right] I_0$$

and if $\theta/2$ is quite small. Hence if there is a small phase mismatch between LO+ and LO-, it will generate a small current of fundamental frequency which is proportional to the phase mismatch at the common source of the switching pair. This small current is injected into M0 from its drain and induces a voltage of fundamental frequency at the gate, which is considered to be the LO leakage. Now let us use the small signal equivalent circuit of NMOS in Fig. 4.9 to obtain the relation between that small current and the LO leakage. Fig. 4.10 shows the small signal equivalent circuit of M0 in Fig. 4.7(b).

Figure 4.9 Small signal equivalent circuit of NMOS [39]

Figure 4.10 Small signal equivalent circuit of M0

In the Fig. 4.10, the small signal current i represents the one at the drain of M0 caused by the LO mismatch. We want to get v_g induced by i . v_g is the voltage at the gate of M0 (node G). So we set up equations and use i to represent v_g .

$$i_1 = (v_d - v_b) s C_{db} \quad (4.13)$$

$$i_2 = v_b s C_{sb} \quad (4.14)$$

$$i_3 = i_2 - i_1 \quad (4.15)$$

$$v_b = v_g - \frac{i_3}{s C_{gb}} \quad (4.16)$$

$$v_d = v_g + \frac{i_3 + v_g s C_{gs}}{s C_{gd}} \quad (4.17)$$

$$i = g_{mb} v_b + g_{ds} v_d + g_m v_g + v_b s C_{sb} + v_g s C_{gs} \quad (4.18)$$

There are 6 equations and 7 variables, $i, i_1, i_2, i_3, v_b, v_g, v_d$. So I can use i to represent v_g , which is the LO leakage. After solving equations, we get

$$v_b = \frac{v_g (C_{gs} + C_{gd} + C_{gb} + C_{gb} C_{gd} / C_{db})}{C_{gb} + C_{gd} + C_{gd} C_{gb} / C_{db} + C_{gd} C_{sb} / C_{db}} \approx v_g \left(1 + \frac{C_{gs}}{C_{gb} + C_{gd}}\right) \approx v_g \left(1 + \frac{C_{gs}}{C_{gd}}\right) \quad (4.19)$$

$$v_d = \frac{v_b (C_{db} + C_{gb} + C_{sb}) - v_g C_{gb}}{C_{db}} \approx v_b \approx v_g \left(1 + \frac{C_{gs}}{C_{gd}}\right) \quad (4.20)$$

$$\begin{aligned} v_g &= \frac{i}{g_m + (g_{mb} + g_{ds})(1 + C_{gs} / C_{gd}) + s C_{gs}} \\ &\approx \frac{i}{g_m + (g_{mb} + g_{ds})(1 + C_{gs} / C_{gd})} \approx \frac{i}{g_m} \end{aligned} \quad (4.21)$$

In the section 4.3.1, it has been said that C_{gb} and C_{sb} in the small signal equivalent circuit of M0 are ignored to simplify the results. Moreover, below 10GHz sC_{gs} is quite small comparing to the real part of the denominator, so it is ignored. Because we got $g_m = 0.0185$, $C_{gs} = 5.313 \times 10^{-14}$ F from the simulations. So at 2.45 GHz, sC_{gs} will be $j8.174 \times 10^{-4}$, which is still much smaller than g_m . Therefore sC_{gs} is ignored. From above, I have shown that, the LO phase mismatch is proportional to a small current i , see equation (4.12). Then such a small current i is also proportional to the LO leakage, see equation (4.21). As a result, the LO leakage is proportional to the LO phase mismatch and its magnitude is approximately $D\theta/g_m$.

4.2.4 LO Amplitude Mismatch Only

If there exists an amplitude mismatch ε between LO+ and LO–, the fundamental frequency term of common source current is

$$\begin{aligned}
 I_{common_source} &= I_{D1} + I_{D2} \\
 &= \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda(A + \varepsilon/2)}{2} \right] I_0 \sin \omega_{LO} t \\
 &\quad + \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda(A - \varepsilon/2)}{2} \right] I_0 \sin(\omega_{LO} t + \pi) \\
 &= \frac{\lambda I_0}{2} \varepsilon \sin \omega_{LO} t
 \end{aligned} \tag{4.22}$$

Hence if there is a small amplitude mismatch between LO+ and LO–, it will generate a small current of fundamental frequency which is proportional to the mismatch amplitude at the common source of the switching pair. Combining with equation (4.21), we can see

that the LO leakage is proportional to the LO amplitude mismatch and its magnitude is approximately $\lambda I_0 \varepsilon / (2g_m)$.

4.2.5 Both of LO Phase and Amplitude Mismatch

In general, the differential LO signals have both phase mismatch θ and amplitude mismatch ε . Therefore the fundamental frequency term of common source current is

$$\begin{aligned}
 I_{\text{common_source}} &= I_{D1} + I_{D2} \\
 &= \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda(A + \varepsilon/2)}{2} \right] I_0 \sin(\omega_{LO}t + \theta/2) \\
 &\quad + \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda(A - \varepsilon/2)}{2} \right] I_0 \sin(\omega_{LO}t + \pi - \theta/2) \\
 &\approx \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda A}{2} \right] I_0 \theta \cos \omega_{LO}t + \frac{\lambda \varepsilon I_0}{2} \sin \omega_{LO}t \\
 &= I_{\text{phase_mismatch}} + I_{\text{amplitude_mismatch}}
 \end{aligned} \tag{4.23}$$

It is found that when the phase mismatch and amplitude mismatch both occur, the common source current of fundamental frequency is just equal to the sum of the currents caused by each of them. Please compare equation (4.23) with equations (4.12) and (4.22). So the superposition principle applies here. Therefore,

$$|I_{\text{common_source}}|^2 = |I_{\text{phase_mismatch}}|^2 + |I_{\text{amplitude_mismatch}}|^2 \tag{4.24}$$

From sections 4.3.3 and 4.3.4, we know that if a phase mismatch or amplitude mismatch exists, the LO leakage is proportional to the fundamental frequency term of common source current. Combining equations (4.21) and (4.23), we have

$$|V_{LO\text{leakage_total}}|^2 = \left(\frac{D\theta}{g_m} \right)^2 + \left(\frac{\lambda I_0 \varepsilon}{2g_m} \right)^2 \tag{4.25}$$

where

$$D = \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda A}{2} \right] I_0$$

As a result, when both of phase and amplitude mismatch exist, the amplitude square of LO leakage is equal to the sum of amplitude square of each contribution.

$$|V_{LOleakage_total}|^2 = |V_{phase_mismatch}|^2 + |V_{amplitude_mismatch}|^2 \quad (4.26)$$

4.3 Analysis of LO-RF Leakage by Simulations

To better understand the origin of the DC offset, consider the received signal path shown in Fig. 4.11 (a). As the isolation between the LO port and the inputs of the mixer is not perfect, and a finite amount of feedthrough, which is known as LO leakage, couples from the LO port to the other mixer inputs. The leakage signal is reflected back at the outputs of the LNA (ignoring the feedthrough from the LNA outputs to its inputs) and now mixed with the original LO signal, thus producing a DC component at the output of the mixer. So the DC offset can be expressed by equation (4.27).

$$DC\ Offset = LO\ Leakage \times \beta \times G \quad (4.27)$$

where β is the reflection factor and G is the mixer gain.

Fig. 4.11 (b) shows how the circuit is constructed to measure the LO-RF leakage. The RF signals are disconnected and only LO signals are injected to the mixer. Then the signal of LO frequency appear at the RF port is the LO leakage. That amount of leakage divided by the LO signals at the LO switching transistor gates is the LO feedthrough. . In the following subsections, LO leakage and LO feedthrough are discussed in two cases, an ideal mixer and a mixer with LO mismatches.

4.3.1 Ideal Mixer

An ideal mixer circuit is perfectly symmetrical without any parasitic effects. See Fig. 4.12, all the odd harmonics at the RF ports are cancelled due to the symmetry of the circuit. When a signal -17.72dBv was injected to the LO ports, the voltage at the RF ports was -135.7dBv , which is consider as LO leakage.

$$\begin{aligned} \text{LO feedthrough} &= \text{LO leakage} - \text{LO Signal} \\ &= (-135.7\text{dB}) - (-17.72\text{dB}) = -117.98\text{dB} \end{aligned} \tag{4.28}$$

Figure 4.12 LO Feedthrough for the ideal case

In this case LO leakage is in the noise level, so it is concluded that there is no LO feedthrough for an ideal double-balanced mixer, which is consistent with theory.

4.3.2 Mixer with LO Phase Mismatch Only

In the real application, the LO does not supply perfectly balanced signals. The phase mismatch at the LO port could be due to the source, i.e. the LO, or due to the load, i.e. mixer LO input port. So it is necessary to do some simulations to see how the LO mismatch affects the LO feedthrough. For the analysis of phase mismatch only, LO+ and LO- had the same amplitude, which is 130mV (-17.72dBv). However, the phase angle of LO+ was changed from 0° to 5° to represent the mismatch phase while LO- kept the constant of 180°. Table 4.3 shows the simulation results.

Table 4.3 LO leakage for the case of LO phase mismatch only

LO+ phase (degree)	LO leakage (dB)	LO feedthrough (dB)
0.0	-135.7	-117.98
0.01	-111.4	-93.68
0.04	-99.10	-81.38
0.1	-91.08	-73.36
0.2	-85.04	-67.32
0.5	-77.08	-59.36
1.0	-71.00	-53.28
1.5	-67.47	-49.75
2.0	-64.97	-47.25
2.5	-63.04	-45.32
3.0	-61.45	-43.73
3.5	-60.12	-42.40
4.0	-59.03	-41.31
4.5	-57.93	-40.21
5.0	-57.02	-39.30

Figure 4.13 LO feedthrough caused by LO phase mismatch

According to the data in Table 4.3, the relation of LO feedthrough versus LO phase mismatch is plotted in Fig. 4.13. It is found that the LO feedthrough (dB) is exponentially proportional to the phase mismatch in the linear scale when the mismatch is small, less than 5°. It is concluded that the LO leakage in volts is directly proportional to the LO phase mismatch with the value less than 5°.

4.3.3 Mixer with LO Amplitude Mismatch Only

Similarly, the amplitude mismatch at the LO port could be due to the source, i.e. the LO, or the load, i.e. the input impedance of the LO port. For the analysis of amplitude mismatch only, different powers of LO+ and LO- were injected while keeping 180° phase difference. The two differential LO signals were large enough to completely turn on/off the switching pairs so that the mixer had a constant gain while they were changing

in a small range. The amplitude of LO- was fixed and LO+ was increased to make the amplitude mismatch change from 0mV to 50mV. Table 4.4 shows the simulation results.

Table 4.4 LO leakage for the case of LO amplitude mismatch only

LO+ input (mV)/ (dB)	LO- input (mV)/ (dB)	LO leakage (dB)	Feedthrough (dB)
270/-11.37	270/-11.37	-123.1	-111.73
270.1/-11.37	270/-11.37	-98.72	-87.35
270.4/-11.36	270/-11.38	-86.91	-75.55
271/-11.34	270/-11.38	-79.01	-67.67
272/-11.30	270/-11.38	-73.01	-61.71
275/-11.20	270/-11.38	-65.07	-53.87
280/-11.03	270/-11.39	-59.06	-48.03
285/-10.87	270/-11.40	-55.54	-44.67
290/-10.70	270/-11.41	-53.05	-42.35
295/-10.55	270/-11.42	-51.12	-40.57
300/-10.39	270/-11.43	-49.55	-39.16
305/-10.23	270/-11.44	-48.22	-37.99
310/-10.08	270/-11.45	-47.07	-36.99
315/-9.935	270/-11.46	-46.05	-36.11
320/-9.790	270/-11.47	-45.14	-35.35

Figure 4.14 LO feedthrough caused by LO amplitude mismatch

Fig. 4.14 shows the relation of LO feedthrough versus LO amplitude mismatch. It can be seen that the LO feedthrough (dB) is also exponentially proportional to the amplitude mismatch in the linear scale. When the mismatch amplitude is larger than 10mV, the curve starts to slightly bend down. It is concluded that the LO leakage in volts is directly proportional to the LO amplitude mismatch with the value less than 10mV.

4.3.4 Mixer with Both of LO Phase and Amplitude Mismatch

In general, the differential LO signals have both phase mismatch and amplitude mismatch at the same time. Table 4.5 shows the simulation results of the total LO leakage. The data is plotted in Fig. 4.15 to show the relation of the total LO leakage to the amplitude mismatch for several fixed phase mismatches. It is found that when the phase mismatch is small, the total LO leakage is simply proportional to the amplitude mismatch. When the phase mismatch is large enough, the shape of curve representing the relation between the total leakage and amplitude mismatch is hyperbolic.

Table 4.5 LO leakage in mV, θ is phase mismatch and ε is amplitude mismatch

	$\theta = 0^\circ$	$\theta = 1^\circ$	$\theta = 3^\circ$	$\theta = 4^\circ$	$\theta = 5^\circ$
$\varepsilon = 0 \text{ mV}$	0.0007	0.552077	1.657677	2.200392	2.748
$\varepsilon = 5 \text{ mV}$	0.557828	0.795243	1.770109	2.320064	2.864178
$\varepsilon = 10 \text{ mV}$	1.114295	1.25603	2.034698	2.561533	3.040885
$\varepsilon = 15 \text{ mV}$	1.671091	1.772148	2.401596	2.89068	3.353513
$\varepsilon = 20 \text{ mV}$	2.225871	2.306747	2.828134	3.288516	3.647539
$\varepsilon = 25 \text{ mV}$	2.779713	2.847738	3.296097	3.719632	4.097321
$\varepsilon = 30 \text{ mV}$	3.330428	3.388442	3.784426	4.087898	4.523765
$\varepsilon = 35 \text{ mV}$	3.881504	3.935501	4.285485	4.565623	4.977371
$\varepsilon = 40 \text{ mV}$	4.430982	4.48229	4.797334	5.176068	5.47016

$\varepsilon = 45 \text{ mV}$	4.983105	5.029213	5.31496	5.688529	5.841172
$\varepsilon = 50 \text{ mV}$	5.533501	5.604024	5.841172	6.060382	6.324119

Figure 4.15 Total LO leakage vs. amplitude mismatch

In order to verify that the shape of the curves in Fig. 4.15 is hyperbolic, for example, let consider the curve of $\theta = 1^\circ$. It is related to the values of column $\theta = 1^\circ$ in the Table 4.5. These values of the column, denoted by $V_{(\theta = 1^\circ, \varepsilon = x)}$ where $x = 5, 10 \dots 50$, show the total LO leakage induced by the phase mismatch of $\theta = 1^\circ$ and the amplitude mismatch of $\varepsilon = x$. It is found that $V_{(\theta = 1^\circ, \varepsilon = x)}$ is approximately equal to

$$V_{(\theta = 1^\circ, \varepsilon = x)}^2 \cong V_{(\theta = 1^\circ, \varepsilon = 0)}^2 + V_{(\theta = 0^\circ, \varepsilon = x)}^2. \tag{4.29}$$

Similarly, the same relation exists for other columns in the Table 4.5. The total LO leakage $V_{(\theta = y^\circ, \varepsilon = x)}$, where $x = 5, 10, \dots, 50$ and $y = 1, 3, 4, 5$, is approximately equal to

$$V_{(\theta=y^{\circ},\varepsilon=x)}^2 \cong V_{(\theta=y^{\circ},\varepsilon=0)}^2 + V_{(\theta=0^{\circ},\varepsilon=x)}^2 \tag{4.30}$$

Table 4.6 (a) Mismatch of equation (4.30) when $\theta = 1^{\circ}$, (b) mismatch of equation (4.30) when $\theta = 5^{\circ}$, $Mismatch = 1 - \text{Column3/Column2}$

	$V_{(\theta=1^{\circ},\varepsilon=x)}^2$	$V_{(\theta=1^{\circ},\varepsilon=0)}^2 + V_{(\theta=0^{\circ},\varepsilon=x)}^2$	<i>Mismatch</i>
$\varepsilon = 0 \text{ mV}$	0.30478	0.30478	0
$\varepsilon = 5 \text{ mV}$	0.63241	0.61595	2.60%
$\varepsilon = 10 \text{ mV}$	1.57761	1.54643	1.97%
$\varepsilon = 15 \text{ mV}$	3.14051	3.09733	1.37%
$\varepsilon = 20 \text{ mV}$	5.32108	5.25928	1.16%
$\varepsilon = 25 \text{ mV}$	8.10961	8.03158	0.96%
$\varepsilon = 30 \text{ mV}$	11.48154	11.39653	0.74%
$\varepsilon = 35 \text{ mV}$	15.48817	15.37085	0.76%
$\varepsilon = 40 \text{ mV}$	20.09092	19.93790	0.76%
$\varepsilon = 45 \text{ mV}$	25.29298	25.13612	0.62%
$\varepsilon = 50 \text{ mV}$	31.40508	30.92441	1.53%

(a)

	$V_{(\theta=5^{\circ},\varepsilon=x)}^2$	$V_{(\theta=5^{\circ},\varepsilon=0)}^2 + V_{(\theta=0^{\circ},\varepsilon=x)}^2$	<i>Mismatch</i>
$\varepsilon = 0 \text{ mV}$	7.55150	7.55150	0
$\varepsilon = 5 \text{ mV}$	8.20351	7.86267	4.15%
$\varepsilon = 10 \text{ mV}$	9.24698	8.79315	4.90%
$\varepsilon = 15 \text{ mV}$	11.24605	10.34405	8.02%
$\varepsilon = 20 \text{ mV}$	13.30454	12.50600	6.00%
$\varepsilon = 25 \text{ mV}$	16.78804	15.27830	8.99%
$\varepsilon = 30 \text{ mV}$	20.46445	18.64325	8.90%
$\varepsilon = 35 \text{ mV}$	24.77422	22.61757	8.70%
$\varepsilon = 40 \text{ mV}$	29.92265	27.18510	9.15%
$\varepsilon = 45 \text{ mV}$	34.11929	32.38284	5.09%

$\varepsilon = 50 \text{ mV}$	39.99448	38.17113	4.56%
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(b)

Table 4.6 shows the quantification of equation (4.30) and is obtained by using the data in Table 4.5. When the phase mismatch θ is small, the mismatch of equation (4.30) is small and gives accurate estimations. When the phase mismatch increases to 5° , the mismatch of equation (4.30) is around 8%. In Fig. 4.15, ε is a variable and θ is fixed. So the set of curves can be represented by

$$V_{(\theta=y^\circ, \varepsilon=x)}^2 - V_{(\theta=0^\circ, \varepsilon=x)}^2 \cong V_{(\theta=y^\circ, \varepsilon=0)}^2. \quad (4.31)$$

Equation (4.31) is a hyperbola function, which is in the form of $y^2 - x^2 = a$, where a is a constant. Note that $V_{(\theta=0^\circ, \varepsilon=x)}$ is proportional to ε .

Table 4.7 shows the total LO leakage for some fixed amplitude mismatches while the phase mismatch is changing. The data is plotted in Fig. 4.16. It is found that when the amplitude mismatch is small, the total LO leakage is simply proportional to the phase mismatch. When the amplitude mismatch is large enough, the shape of curve representing the relation between the total leakage and phase mismatch is hyperbolic. Similarly, the set of curves can be represented by equation (4.32).

$$V_{(\theta=y^\circ, \varepsilon=x)}^2 - V_{(\theta=y^\circ, \varepsilon=0)}^2 \cong V_{(\theta=0^\circ, \varepsilon=x)}^2 \quad (4.32)$$

where $x = 1, 10, 30, 50$, and $y = 0.5, 1, 1.5, \dots, 5$.

Table 4.7 LO leakage in mV, θ is phase mismatch and ε is amplitude mismatch

	$\varepsilon = 0 \text{ mV}$	$\varepsilon = 1 \text{ mV}$	$\varepsilon = 10 \text{ mV}$	$\varepsilon = 30 \text{ mV}$	$\varepsilon = 50 \text{ mV}$
$\theta = 0^\circ$	0.000631	0.112073	1.114295	3.330428	5.533501
$\theta = 0.5^\circ$	0.276058	0.300262	1.156112	3.353513	5.552646
$\theta = 1^\circ$	0.552077	0.566892	1.25603	3.388442	5.571857
$\theta = 1.5^\circ$	0.828896	0.83946	1.407667	3.455413	5.616943
$\theta = 2^\circ$	1.101539	1.114295	1.614359	3.544051	5.675446
$\theta = 2.5^\circ$	1.377209	1.386756	1.807174	3.655948	5.754399
$\theta = 3^\circ$	1.657677	1.665329	2.034698	3.784426	5.841172
$\theta = 3.5^\circ$	1.934194	1.940886	2.275097	3.926449	5.942922
$\theta = 4^\circ$	2.200392	2.213095	2.523481	4.183117	6.060382
$\theta = 4.5^\circ$	2.471724	2.485994	2.779713	4.265795	6.187283
$\theta = 5^\circ$	2.779713	2.763758	3.037386	4.523765	6.324119

Figure 4.16 Total LO leakage vs. phase mismatch

Table 4.8 shows the quantification of equation (4.30) and is obtained by using the data in Table 4.7. When the amplitude mismatch ε is small, the mismatch of equation (4.30) is small and gives accurate estimations. When the amplitude mismatch increases to 50mV, the mismatch of equation (4.30) is around 3%. From Table 4.6 and 4.8, it is concluded that the equation (4.30) is correct with acceptable mismatch.

Table 4.8 (a) Mismatch of equation (4.30) when $\varepsilon = 1$ mV, (b) mismatch of equation (4.30) when $\varepsilon = 50$ mV, *Mismatch* = 1- Column3/Column2.

	$V_{(\theta=y^\circ,\varepsilon=1)}^2$	$V_{(\theta=y^\circ,\varepsilon=0)}^2 + V_{(\theta=0^\circ,\varepsilon=1)}^2$	<i>Mismatch</i>
$\theta = 0^\circ$	0.01256	0.01256	0
$\theta = 0.5^\circ$	0.09016	0.08877	1.54%
$\theta = 1^\circ$	0.32137	0.31735	1.25%
$\theta = 1.5^\circ$	0.70469	0.69963	0.72%
$\theta = 2^\circ$	1.24165	1.22595	1.26%
$\theta = 2.5^\circ$	1.92309	1.90926	0.72%
$\theta = 3^\circ$	2.77332	2.76045	0.46%
$\theta = 3.5^\circ$	3.76704	3.75367	0.35%
$\theta = 4^\circ$	4.89779	4.85428	0.89%
$\theta = 4.5^\circ$	6.18017	6.12198	0.94%
$\theta = 5^\circ$	7.63836	7.73936	-1.32%

(a)

	$V_{(\theta=y^\circ,\varepsilon=50)}^2$	$V_{(\theta=y^\circ,\varepsilon=0)}^2 + V_{(\theta=0^\circ,\varepsilon=50)}^2$	<i>Mismatch</i>
$\theta = 0^\circ$	30.61963	30.61963	0
$\theta = 0.5^\circ$	30.83188	30.69584	0.44%
$\theta = 1^\circ$	31.04559	30.92442	0.39%
$\theta = 1.5^\circ$	31.55005	31.3067	0.77%

$\theta = 2^\circ$	32.21069	31.83302	1.17%
$\theta = 2.5^\circ$	33.11311	32.51633	1.80%
$\theta = 3^\circ$	34.11929	33.36752	2.20%
$\theta = 3.5^\circ$	35.31832	34.36074	2.71%
$\theta = 4^\circ$	36.72823	35.46135	3.45%
$\theta = 4.5^\circ$	38.28247	36.72905	4.06%
$\theta = 5^\circ$	39.99448	38.34643	4.12%

(b)

4.4 Comparison of LO Leakage due to LO Mismatch between Theory and Simulations

From Section 4.2.5, the theoretical analysis shows that, when both LO phase and amplitude mismatches occur at the same time, the amplitude square of the LO leakage is equal to the sum of amplitude squares of each contribution. The total LO leakage is represented by

$$|V_{LOleakage_total}|^2 = \left(\frac{D\theta}{g_m} \right)^2 + \left(\frac{\lambda I_0 \varepsilon}{2g_m} \right)^2 \quad (4.33)$$

where,

$$D = \left[\frac{2(1 + \lambda V_{dc})}{\pi} + \frac{\lambda A}{2} \right] I_0$$

$$I_0 = K(V_{GS0} - V_{th})^2$$

$$V_{dc} = V_{LObias} \sin g - V_{eff0} - V_{GS1}$$

$$K = \frac{1}{2} \mu_n C_{ox} \frac{W_0}{L_0}$$

$$C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}}$$

In Section 4.3.4, simulation results also show that there is such a relation and it is represented by

$$V_{(\theta=y^\circ, \varepsilon=x)}^2 \cong V_{(\theta=y^\circ, \varepsilon=0)}^2 + V_{(\theta=0^\circ, \varepsilon=x)}^2. \quad (4.34)$$

In this section, the simulation results of LO leakage due to LO mismatch are compared with the results of theoretical analysis. From the model files, simulations and calculation, some necessary parameters are obtained as shown in the Table 4.9.

Table 4.9 Parameter values for equation (4.33)

$g_m = 0.0185 \text{ 1}/\Omega$	$A = 270 \text{ mV}$	$V_{Lobiasing} = 1.35 \text{ V}$
$V_{GSI} = 0.598 \text{ V}$	$V_{GSO} = 0.647 \text{ V}$	$V_{eff0} = 0.157 \text{ V}$
$V_{th} = 0.472 \text{ V}$	$\lambda = 0.543$	$t_{ox} = 4.1 \times 10^{-9} \text{ m}$
$\mu_n = 0.05 \text{ m}^2/\text{V}\cdot\text{s}$	$\varepsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$	$\varepsilon_r = 3.9$
$W_0 = 60 \text{ }\mu\text{m}$	$L_0 = 0.18 \text{ }\mu\text{m}$	$I_0 = 1.724 \text{ mA}$

After calculation, equation (4.33) is simplified as below

$$|V_{LOleakage_total}|^2 = (0.0853\theta)^2 + (0.0253\varepsilon)^2 \quad (4.35)$$

where θ is in radians and ε is in Volts.

Table 4.10 shows the comparison of LO leakage between the simulation results and theoretical results. The simulation results are taken from Table 4.7. As shown in Table 4.10, the results do not match very well. It should be noted that the model of RF MOS devices in the simulations is BSIM3 V3.2, so the transistors are well defined by many parameters. However, in the theoretical analysis we only use the most fundamental equations of MOS. It is difficult to perform the theoretical analysis manually if we

include many parameters characterizing those complicated effects, such as the variation of threshold along the channel, the degradation of the mobility with the vertical field in the channel, and so on. Thus, circuit simulation tools are required for more accurate results. However, the key point of the theoretical analysis is the demonstration of the LO leakage due to LO mismatch. That is verified by the simulations.

Table 4.10 Comparison of simulation results and theoretical results

	LO leakage, mV (Simulation)	LO leakage, mV (Theoretical)
$\theta = 0^\circ, \varepsilon = 0 \text{ mV}$	0.000631	0
$\theta = 0^\circ, \varepsilon = 1 \text{ mV}$	0.112	0.0253
$\theta = 0^\circ, \varepsilon = 10 \text{ mV}$	1.114	0.253
$\theta = 0^\circ, \varepsilon = 30 \text{ mV}$	3.330	0.759
$\theta = 0.5^\circ, \varepsilon = 0 \text{ mV}$	0.276	0.744
$\theta = 0.5^\circ, \varepsilon = 1 \text{ mV}$	0.300	0.744
$\theta = 0.5^\circ, \varepsilon = 10 \text{ mV}$	1.156	0.786
$\theta = 0.5^\circ, \varepsilon = 30 \text{ mV}$	3.353	1.063
$\theta = 1^\circ, \varepsilon = 0 \text{ mV}$	0.552	1.488
$\theta = 1^\circ, \varepsilon = 1 \text{ mV}$	0.567	1.488
$\theta = 1^\circ, \varepsilon = 10 \text{ mV}$	1.256	1.509
$\theta = 1^\circ, \varepsilon = 30 \text{ mV}$	3.388	1.670
$\theta = 1.5^\circ, \varepsilon = 0 \text{ mV}$	0.829	2.232
$\theta = 1.5^\circ, \varepsilon = 1 \text{ mV}$	0.839	2.232
$\theta = 1.5^\circ, \varepsilon = 10 \text{ mV}$	1.408	2.246
$\theta = 1.5^\circ, \varepsilon = 30 \text{ mV}$	3.455	2.358

4.5 Rules for MOS Transistor Matching

The Gilbert cell mixer is a symmetrical differential circuit. There are three differential pairs in the mixer, and the matching of the transistors is important. In the following, some critical rules for MOS transistor matching [40] will be described.

1. Orient transistors in the same direction.

Transistors that do not lie parallel to one another become vulnerable to stress- and tilt-induced mobility variations that can cause several percent variations of their transconductance.

2. Place transistors in close proximity.

MOS transistors are vulnerable to gradient in temperature, stress, and oxide thickness. Moderately or precisely matched transistors should be kept next to one another to facilitate common-centroid layout.

3. Keep the layout of the matched transistors as compact as possible.

MOS transistors naturally lend themselves to long, spindly layouts that are extremely vulnerable to gradients. Common-centroid layout cannot entirely eliminate this vulnerability, so the designer should strive to create as compact an arrangement of matched devices as possible. This usually requires that each device be divided into a number of fingers.

4. Place dummy segments on the ends of arrayed transistors.

Arrayed transistors should include dummy gates at either end. These dummies need not have the same length as the actual gates, but the spacing between the dummy gates and the actual gates must be equal to the spacing between actual gates. The dummy gates should be connected to the substrate potential.

5. Place transistors in areas of low stress gradients.

The stress gradients reach a broad minimum in the center of the die. Any location ranging from the center of the die out halfway to the edges will fall within this broad minimum. Whenever possible, precisely matched transistors should reside within this low-stress area.

6. Place transistors well away from power devices.

For purposes of discussion, any device dissipating more than 50mW should be considered a power device, and any device dissipating more than 250mW should be considered a major power device. Precisely matched transistors should reside on an axis of symmetry of the major power devices using an optimal symmetry arrangement. Moderately and precisely matched transistors should reside no less than 250 to 500 μ m away from the closest power device.

7. Place precisely matched transistors on axes of symmetry of the die.

Arrays of precisely matched transistors should be placed so that the axis of symmetry of the array aligns with one of the two axes of symmetry of the die.

8. Consider using NMOS transistors rather than PMOS transistors.

NMOS transistors generally match better than PMOS transistors. Whenever circuit considerations allow, consider using NMOS transistors rather PMOS transistors.

According to the above rules for drawing the layout, the mismatch could be minimized. For the Gilbert cell mixer designed in this thesis, BSIM3 RF transistors of the Chartered Semiconductor 0.18 μm RFMOS process design kit (library) are used. The sizes of these transistors are not scalable. The gate width of each finger is 5 μm . Silicon-verified models are provided for five transistors with different number of fingers, such as 6, 12, 20, 24, and 30. The accuracy of gate length is 1.5e-08m and the accuracy of gate width is 8.719e-08m. So there will be a little mismatch in the fabrication.

4.6 Conclusion

In this chapter, I first show the design a Gilbert CMOS mixer operating at the centre frequency of 2.45GHz. After that this mixer is used to do the analysis of LO-RF leakage. It is found that if there is no LO mismatch, an ideal mixer will not have an LO leakage and DC offset. If a phase mismatch or amplitude mismatch exists, the LO leakage is proportional to the mismatch value. If both types of mismatches occur at the same time, the amplitude square of the LO leakage is equal to the sum of amplitude squares of each contribution. The relation between the mismatch and the LO leakage is derived. The analysis agrees with simulation results. Finally some important device mismatch issues are addressed. The LO-RF leakage of a non-ideal mixer with parasitic effects will be discussed in Chapter 6.

Chapter 4

The LO leakage is a very important issue in the conventional mixers for direct conversion applications, because the LO leakage can generate DC offset due to LO self-mixing, as explained in Section 4.3. The conventional mixers, such as Gilbert cell mixer, cannot eliminate the DC offset caused by LO leakage. As LO frequency is near to RF frequency, the LO leakage at the RF port, as an input signal, mixes with the original LO signal at the LO port and generate the DC output.

Recently, a new mixing topology, called harmonic mixer, has been proposed [8]-[10]. This topology enables the second harmonic of LO signals to mix with the RF signals. For example, LO signal is at 1.2GHz and RF signal is at 2.4GHz. The harmonic mixer enables the second harmonic of the LO signal at 2.4GHz to mixer with 2.4GHz RF signal to realize the direct down-conversion. In this type of mixer, there is still LO leakage. But the leakage is at 1.2GHz, which is far away from the 2.4GHz RF frequency. In the harmonic mixer, only 2.4GHz components generate the baseband output. So the 1.2GHz LO leakage does not produce the DC offset. As a result, harmonic mixers successfully eliminate the DC offset caused by LO self-mixing. In the next chapter, a novel harmonic mixer will be proposed.

Chapter 5

CMOS Even Harmonic Switching Mixer for DCR

The direct conversion techniques have increasingly gained more attention as a possible solution for the single-chip radio due to its low power, low complexity and easy integrating properties in recent years. However, a number of issues which do not exist or are not serious in the heterodyne architecture become important in the homodyne architecture, such as DC offset, flicker noise, I/Q mismatch, even order distortion and so on. Among these the DC offset generated by LO self-mixing is the most critical. Chapter 4 has shown that the LO-RF leakage and DC offset are the inherent problems of the Gilbert mixers and Chapter 3 has discussed several DC offset cancellation techniques. One of the approaches is to use a DC-offset-free mixing topology, such as harmonic mixers. This technique could give a simple solution to the DC offset, but less research has been done on this approach.

In the direct conversion architecture, the down-converted spectrum is located around the zero frequency, so the flicker ($1/f$) noise of the devices has a profound effect on the SNR, a severe problem in CMOS implementations [14]. However, it is found that the high flicker noise problem can be solved by the switching mixer topology [41]-[43] using a zero bias current. Unfortunately, not much attention has been paid to this solution.

In this chapter, a novel CMOS even harmonic switching mixer with DC offset free and low noise figure is introduced. In section 5.1 and 5.2, the topologies of an even harmonic mixer and a simple switching mixer are discussed respectively. After that the design of a simple switching mixer is shown in section 5.3. Section 5.4 describes the design of the novel even harmonic switching mixer. Finally section 5.5 gives the conclusions.

5.1 Even Harmonic Mixer

Fig. 5.1 shows the schematic of a bipolar or BiCMOS even harmonic mixer [8]. The quadrature LO signals are applied to the mixer at half the RF frequency.

Figure 5.1 Even harmonic mixer

When operating with LO signals with large amplitude, the switching core (Q3-Q10) acts as a mixer. The resulting performance is that the circuit is mixing the RF signals with the one of twice the LO input frequency. For example, in the switching core (Q3-Q6), each transistor only conducts when the sinusoidal LO signal is close to the positive peak value. That makes the RF signal to be switched on every quarter cycle of the LO drive waveform, creating an effective $2f_{LO}$ signal.

Figure 5.2 LO waveforms

Fig. 5.2 shows the waveforms within the mixer driven by the quadrature LO inputs without the RF drive, to assist the reader in visualizing the generation of the doubled LO frequency internal to the mixer. The mixer design exploits the short off period of the devices in the switching core of the design. If the LO drive signals are ideal square waves, the switching core would have multiple transistors turn on simultaneously, resulting in no IF signal [8]. Because The 4-phase LO signal is at the frequency $F_{RF}/2$. However, we want a F_{RF} LO signal to mix with RF signal to generate baseband output. So if the LO transistors only turn on at the around peak of each phase LO signals, we can get the collector currents of I (Q3-Q6) shown in Fig. 5.2. In this case, the sum of these 4 collector currents will have the frequency of F_{RF} , which is the I(Q1). Therefore, it creates an effect that the RF signal of F_{RF} is mixed by a virtual LO signal of the same frequency. But if the 4 phases of LO signal are square wave, Q3 and Q5 will turn on at the same time, same as Q4 and Q6. In this case, the sum of I (Q3-Q6) will not be a current with frequency of F_{RF} , but still $F_{RF}/2$. The harmonic mixing will fail. Therefore the performance is better when the LO signals become more triangular. But the simulation result is almost identical when the mixer is driven by either a sinusoidal, or triangular sources. Fig. 5.3 shows the effect of rise time as a function of LO pulse width on the conversion gain. Note that the conversion gain does not degrade by 3dB until the rise time drops below one quarter of the pulse width. As the wave shape approaches a square wave, the conversion loss rises rapidly.

Figure 5.3 Conversion Gain vs. LO wave shapes, rise time/pulse width ratio [8]

Characteristics of this even harmonic mixer

1. The larger the LO power, the less the gain is. Because the LO power is larger, the wave shape is more like a square wave.
2. There is no DC offset caused by self-mixing of LO signals. It is suitable for direct conversion receiver.
3. It uses a bipolar or BiCMOS process. The fabrication cost is higher than that of the standard CMOS.

5.2 Simple Switching Mixer

The switching mixer performs a multiplication between the RF signals and LO signals ideally represented by square waves switching between +1 and -1 (Fig. 5.4). It has two bias voltages, V_{LO_DC} and V_{IF_DC} for LO input and IF output respectively. The difference

between V_{LO_DC} and V_{IF_DC} defines the gate-source bias voltage for the four transistors. If the gate-source bias voltage is exactly equal to the transistor threshold voltage V_{th} , the switching takes places precisely when the local oscillator output reaches the bias voltage. In this case, the mixer conversion gain is maximized.

Figure 5.4 Simple switching mixer

The four identical transistors working in the triode region operate as switches. When the transistors turn on, they are equivalent to resistors. The value is given by:

$$R_{on} = \frac{L}{\mu_n C_{ox} W [(V_{gs} - V_{th}) - V_{ds}]} \quad (5.1)$$

where L is the gate length, μ_n is the average electron mobility in the channel, C_{ox} is the gate oxide capacitor per unit area, and W is the gate width. The theoretical optimum conversion gain for the simple switching mixer is equal to $2/\pi$ (-3.9dB) assuming that the LO signal at the gate is a square waveform and the turn-on resistance R_{on} is zero. When the LO power and gate width W are increased, the performance of the switching mixer is better, see Fig. 5.5. Because the larger sinusoidal LO signal is closer to a square wave and the transistors behave more like ideal switches. Moreover, we can see from equation (5.1)

that a large W gives a small turn-on resistance. Fig. 5.5 shows that little effect on the conversion gain (Loss) and noise figure is seen when the LO power and gate width are increased beyond certain values.

Figure 5.5 Gain, noise and LO power versus transistor width [41]

The distinct advantages of CMOS switching mixers are the zero power consumption and low noise figure. That is because MOS transistors can turn on without a bias current as long as $V_{gs} > V_{th}$. The bias current in the transistors is zero, leading to a low flicker noise. Another advantage is the inherent linearity of the switching mixer due to the good linearity of MOS devices operated in the triode region. But this simple switching mixer will have DC offset problem due to LO self-mixing if it is used in the direct conversion receivers.

Characteristics of the switching mixer

1. The larger LO power will give better performance parameters, such as higher conversion gain, lower NF, higher 1dB compression point.
2. The larger device width W will give better performance parameters. However, these performance parameters cannot be improved further when W exceeds a certain value.
3. A lower NF and higher linearity than that of active CMOS mixers are obtained due to no bias current.

5.3 Design of Simple Switching Mixers

A simple switching mixer according to Fig. 5.4 was designed. The schematic without the bias circuit is shown in Fig. 5.6.

Figure 5.6 Simple switching mixer.

Simulations Setup

1. The baseband bias voltage BB is chosen at 0.6V by considering the voltage level of subsequent stages. It can be changed without affecting the circuit performance.
2. The LO bias voltage is set at 1.2V, so the gate-source bias voltage for the four transistors is $V_{GS} = V_{LO_bias} - V_{BB_bias} = 1.2 - 0.6 = 0.6 > V_{th} = 0.596V$.
3. The LO signal is set at -5dBm and 2.45GHz. The power can be increased for a better performance.
4. The RF signal is set at -40dBm and 2.445GHz for direct conversion application, so the baseband output signal is at 5MHz.
5. RFMOS devices are used in this design. The size of the transistors are $L = 0.18\mu m$, $W = 150\mu m$.

Simulation Results

1. Single end conversion gain = -3.54dB

Fig. 5.7 shows the single end conversion gain. The crosshair marker A shows the RF input signal is -7.07dBV at 2.445GHz and the crosshair marker B shows the baseband output is -10.61dBV at 5MHz. As a result, the gain (conversion loss) is -3.54dB. So the differential conversion gain is 2.46dB.

Figure 5.7 Single end conversion gain

2. 1dB compression point = -7.67dBm

Figure 5.8 1dB compression point

3. $IIP3 = 1.35\text{dBm}$

Figure 5.9 IIP3

4. Noise figure = 7.96dB at 100KHz

Figure 5.10 Noise figure

Comments

The overall performance of the switching mixer can be summarized as: Gain = -3.54dB, 1dB compression point = -7.67dBm, $IIP3 = 1.35\text{dBm}$, $NF = 7.96\text{dB}$. This simple switching mixer has a low NF at quite low frequencies comparing to that of the active mixers (Note that NF of the Gilbert mixer designed in Chapter 4 is 32dB). The 1dB compression point and $IIP3$ are also higher than the ones of the Gilbert mixer. The linearity is improved. The only drawback is the conversion gain. Because the switching mixer is passive, the conversion gain is less than 1. So it is often called “conversion loss”. However, there still exists the DC offset due to the self-mixing of LO in the simple switching mixer, because LO frequency is close to RF frequency. This switching mixer has the same problem as the conventional Gilbert mixer.

5.4 Design of an Even Harmonic Switching Mixer

As explained in the previous sections, the switching mixer has a low NF due to no bias current. The even harmonic mixer has no DC offset due to the difference of the LO frequency and the RF frequency. If these two circuits are combine together, the characteristics of low NF and DC offset free could be obtained.

Fig. 5.11 is the schematic of the proposed even harmonic switching mixer without the biasing circuit for simplicity. The transistors M1-M8 working in the triode region operate as switches connecting either the input or the inverse of the input to the output terminal. The novel even harmonic switching mixer utilizes the method in the section 5.1 to create the effective twice LO switching frequency.

Figure 5.11 Even harmonic switching mixer

5.4.1 Design Parameters and Gain Optimization

The design parameters for the even harmonic switching mixer are the transistor channel width W and channel length L , the local oscillator amplitude V_{LO} , and the DC bias voltages V_{LO_bias} and V_{BB_bias} for the LO input and baseband output, respectively. The difference between V_{LO_bias} and V_{BB_bias} defines the gate-source voltage V_{GS} for all the eight identical transistors. The baseband bias voltage V_{BB_bias} should be chosen to ensure compatibility with subsequent stages. It has no influence on the performance of the mixer. The V_{GS} should be equal to the transistor threshold voltage V_{th} , and the switching takes place precisely when the local oscillator output reaches the bias voltage. Therefore the performance is optimized when $V_{LO_bias} = V_{BB_bias} + V_{th}$.

Figure 5.12 Single end conversion gain versus transistor width

Transistor dimensions and LO power are selected as the variables for the analysis and simulation of the mixer gain. Because the conversion gain is generally small for the switching type mixer, the optimization of the mixer gain becomes an important issue. The gate length is chosen to be $0.18\mu\text{m}$. Simulation results show that the conversion gain first increases and then decreases while the transistor width is increasing, see Fig. 5.12. The peak is at $W = 70\mu\text{m}$. When $W < 70\mu\text{m}$, the conversion gain increases with the transistor width. As discussed in Section 5.2, one characteristic of the switching type mixers is that the larger device width W gives better performance, because large size transistors behave more like ideal switches [41]. The Fig. 5.5 is shown below for better understanding. The “conversion gain” mentioned above is actually a conversion loss because the switching mixer is passive and there is no voltage gain.

Figure 5.13 Gain, noise and LO power versus transistor width

When $W > 70\mu\text{m}$, the conversion gain decreases with the transistor width. As discussed in Section 5.1, one characteristic of the even harmonic mixing topology is that as the LO wave shape approaches a square wave, the conversion loss rises rapidly [8] (Fig. 5.14). Thus, large size transistors behave more like ideal switches and as a result, the conversion gain drops.

Figure 5.14 Conversion Gain vs. LO wave shapes, rise time/pulse width ratio

The conversion gain is also dependent on the LO power. Fig. 5.15 shows the graph of the conversion gain versus LO amplitude (peak to peak) obtained from simulations. Initially, the conversion gain increases with the LO amplitude. As discussed in Section 5.2, one characteristic of the switching type mixers is that the larger LO power will give better performance parameters, such as higher conversion gain, because large LO power makes transistor switch sharp and behave more like ideal switches [41]. After that, the conversion gain decreases with the LO amplitude increasing. As discussed in Section 5.1, one characteristic of the even harmonic mixing topology is that the larger the LO power, the less the gain is [8]. Because the LO power is larger, the wave shape is more like a square wave. Therefore the gain drops. Please refer to Fig. 5.14 for better understanding. When the LO amplitude is 1.5V, the slope of the curve in Fig. 5.15 is almost zero and the gain approaches to the maximum.

Figure 5.15 Single end conversion gain versus LO amplitude (peak to peak)

Simulations Setup

1. The baseband bias voltage is chosen 0.6V by considering the voltage level of subsequent stages. It can be changed to any value without affecting the performance.
2. The LO bias voltage is 1.19V, then the gate-source bias voltage for the four transistors is $V_{GS} = V_{LO_bias} - V_{BB_bias} = 1.19 - 0.6 = 0.59 \geq V_{th} = 0.590V$.
3. The LO signal is set at 1.5V and 1.225GHz.
4. The RF signal is -40dBm at 2.445GHz for direct conversion application. After mixing with twice the LO frequency, the baseband output is at 5MHz.
5. The NMOS_TN is used. $L = 0.18\mu m$, $W = 70\mu m$.

5.4.2 Simulation Results and Comparison

In this section, the simulation results of the designed even harmonic mixer are given. After that, a comparison of the performance is carried out between the designed circuit and the existing designs in the literature.

1. Single end conversion gain = -8.24dB

Fig. 5.16 shows the single end conversion gain. The crosshair marker A shows the RF input signal is -58.78dBV at 2.445GHz and the crosshair marker B shows the baseband output is -67.03dBV at 5MHz. As a result, the gain (conversion loss) is -8.24dB.

Figure 5.16 Single end conversion gain

2. 1dB compression point = 7.10dBm

Figure 5.17 1dB compression point

3. $IIP3 = 17.25\text{dBm}$

Figure 5.18 IIP3

4. Noise figure = 5.21dB at 100KHz

Figure 5.19 Noise Figure

The Figure of Merit (FOM) of mixers is defined below.

$$FOM\ (dB) = 20\log(f_{RF}) + Gain - NF + IIP3 - 10\log(Power) \tag{5.2}$$

For my even harmonic switching mixer, it is difficult to get the power consumption by simulations. But one thing is sure that the power consumption could be very small, because there is no DC bias current for the circuit. It is passive.

A comparison of the performance is carried out between the four circuits. They are the proposed even harmonic switching mixer, the even harmonic mixers in [8] and [9], and the switching mixer in [41]. The proposed circuit was constructed and simulated using Cadence SpectreRF. The performance parameters of the selected mixer circuits are shown in Table 5.1.

Table 5.1 Performance comparisons

	This work	[8]	[9]	[41]
Technology	0.18μm CMOS	0.35μm BiCMOS	0.25μm CMOS	0.25μm CMOS
Mixer type	Harmonic switching	Harmonic Gilbert	Harmonic Gilbert	Switching
DC offset	No	No	No	Yes
Number of transistors	8	10	20	4
RF/LO freq. (GHz)	2.445/1.225	2.144/1.07	2.0122/1.006	2.105/2.1
Output freq. (MHz)	5	4	0.2	5
Supply current (mA)	0	4.6	1.71	0
LO Vpp (V)	1.5	0.5	-	1.0

Gain (dB)	-8.24	18.2	11.61	-6.1
DSB NF (dB)	5.2 at 100kHz	8.0	12	5.6
IIP3 (dBm)	17.25	-6.6	-13.5	21

The proposed mixer has two transistors less, lower noise figure and higher IIP3 comparing to [8]. Moreover, the DC power consumption is zero due to zero bias current. Another disadvantage of [8] is the higher cost of the BiCMOS technology. The even harmonic mixer in [9] is implemented in a 0.25 μ m standard CMOS process. So the noise figure is high due to the high flicker noise. Furthermore, there are 20 transistors in this double-balanced mixer. That increases the cost and complexity of the circuit. The switching mixer in [41] has the DC offset due to the LO self-mixing in direct conversion receivers. As shown, the proposed mixer has both the characteristics of even harmonic mixers and switching mixers. The DC offset problem is solved due to the even harmonic technique used. The low noise figure is caused by the zero bias current in the transistors. The conversion gain is less than unity, but it is not critical and can be compensated by using a low noise amplifier (LNA) with a high gain in the direct conversion receivers.

5.4.3 LO Self-mixing in the Even Harmonic Switching Mixer

The conventional mixers, such as Gilbert mixer, have the problem of DC offset in the direct conversion applications. The main contribution of the DC offset is due to LO self-mixing. To better understand the origin of the DC offset, consider the received signal path shown in Fig. 5.20. As the isolation between the LO port and the inputs of the mixer

is not perfect, and a finite amount of feedthrough, which is known as LO leakage, couples from the LO port to the other mixer inputs. The leakage signal is reflected back at the outputs of the LNA (ignoring the feedthrough from the LNA outputs to its inputs) and now mixed with the original LO signal, thus producing a DC component at the output of the mixer. So the DC offset can be expressed by equation (5.2).

$$DC\ Offset = LO\ Leakage \times \beta \times G \quad (5.3)$$

where β is the reflection factor and G is the mixer gain. So the analysis of LO leakage in the conventional Gilbert mixer is meaningful. In Chapter 4, LO leakage caused by LO mismatch is especially analyzed. That is one of the contributions of this project.

Figure 5.20 Self-mixing problem caused by LO leakage

The even harmonic switching mixer proposed in this chapter can eliminate the DC offset caused by LO self-mixing. Actually in this circuit, LO signals can still leak to the RF ports and become LO leakage. The LO leakage is caused by the same ways as the ones in the Gilbert mixer, such as LO mismatch, circuit mismatch, substrate coupling, and so on.

However, this LO leakage at the RF port does not generate the DC output after mixing with the original LO signals. The example below will clarify this concept.

In the normal situation, RF signal is at 2.445GHz and LO signal is at 1.225GHz. The mixer gain is -8.24dB and the output is at 5MHz. In this case, the LO leakage at the RF port would be at 1.225GHz. The even harmonic mixer, however, mainly mix the signal at the RF input port with the second harmonic of the LO signal at 2.45GHz. Thus, the leakage at 1.225GHz cannot be down-converted to a DC signal.

Simulations Setup

1. The baseband bias voltage is chosen 0.6V by considering the voltage level of subsequent stages. It can be changed to any value without affecting the performance.
2. The LO bias voltage is 1.19V, then the gate-source bias voltage for the four transistors is $V_{GS} = V_{LO_bias} - V_{BB_bias} = 1.19 - 0.6 = 0.59 \geq V_{th} = 0.590V$.
3. The LO signal is set at 1.5V and 1.225GHz.
4. The RF signal is -40dBm at 1.22GHz. If the circuit can directly down-convert the RF signal, the output we are interested in is at 5MHz.
5. The NMOS_TN is used. $L = 0.18\mu m$, $W = 70\mu m$.

Fig. 5.21 shows the single end conversion gain. The crosshair marker A shows the RF input signal is -58.76dBV at 1.22GHz and the crosshair marker B shows the baseband output is -169.07dBV at 5MHz. So the gain (conversion loss) is -110.31dB. This low

gain means that the even harmonic switching mixer cannot directly down-convert a RF signal of the same frequency as LO signal. Therefore the LO leakage at the RF port does not generate the DC offset by LO self-mixing. This is the key principle of the even harmonic mixer. Hence, the effect of LO leakage due to mismatches in the even harmonic switching mixer is not important.

Figure 5.21 Single end conversion gain

5.5 Conclusion

In this chapter, an even harmonic mixer and a simple switching mixer are discussed first. Due to the special mixing topology of the even harmonic mixer, there is no DC offset caused by self-mixing of LO signals. Moreover, higher LO power will cause a lower mixer gain. The performance of the simple switching mixer is better when transistor

width is increasing and LO power is higher. However, it has DC offset if used in direct conversion receivers.

A novel even harmonic switching mixer with DC offset free and low noise figure, especially for the direct conversion application, is proposed. The characteristic of the even harmonic mixer gives a zero DC offset. The low noise figure and high linearity are due to the switching type of the mixer. Switching type mixers need the transistors to switch sharply to obtain good performance. However, to create the effective twice LO frequency here requires the transistors to turn on slowly. Therefore, appropriate design parameters are chosen to optimize the circuit. The proposed mixer is actually a combination of the even harmonic mixer and the switching mixer. It attains a better performance than that of the above mixers. Moreover, this even harmonic switching mixer is simple and easy to design.

Chapter 6

Layout Design and Post-layout Simulations

A layout is basically a drawing of the mask from which the design of the integrated circuit will be fabricated. The performance of an RFIC design is heavily influenced by its layout. Creating the layout is as important as specifying the parameters of the device. It will determine the behavior of the realized design.

This chapter will discuss some considerations on the layout of both passive components and active devices, including resistors, capacitors and transistor. The information is based on the CMOS 6-Metal, 1-Poly, 0.18 μ m process of Chartered Semiconductor Manufacturing Ltd. (CSM). After that, the post-layout simulation results of the designed circuits will be shown.

6.1 Layout of Resistors

The considerations for matching resistors are similar to those of matching transistors. It is recommended that the matched resistors are constructed from a single material and should be of the same width. Identical geometries should be used for all the resistors in one circuit whenever possible.

For the Chartered CMOS 0.18 μ m process, N-well, N⁺, P⁺ and Poly are available layers for implementing resistors. N⁺ diffusion and P⁺ diffusion resistors have a low sheet

resistance ($6\Omega/\text{square}$ for both) and a low accuracy (10% and 25% tolerance for N+ and P+, respectively). On the other hand, N-well layer has a high sheet resistance, $660\Omega/\text{square}$, with high tolerance at about 19%. N-Poly Resistor ($85\Omega/\text{square}$) and P-Poly resistor ($330\Omega/\text{square}$) have the highest accuracy among all.

Fig. 6.1 and 6.2 show the structures of the N-Poly resistor and the P-Poly resistor, respectively. Both are used for implementing the resistor in the Gilbert mixer. The earlier is used for implementing smaller resistances ($<1.5\text{k}\Omega$) while the later is used for implementing larger resistances.

Figure 6.1 The N-Poly resistor [44]

Figure 6.2 The P-Poly resistor [44]

6.2 Layout of Capacitors

Currently, there are four types of capacitors used in RFIC design. They are gate capacitors, junction capacitors, metal-to-metal/poly-to-metal capacitors, and thin insulated capacitors. The gate capacitors have a high capacitance per unit area, however they are not linear, requiring the dc bias and have a low breakdown voltage when implemented in thin gate oxide. Junction capacitors are unpopular as in addition to the problem faced by the gate capacitors, they are very sensitive to the process variation, having a poor quality factor (Q) and a large temperature coefficient.

Metal-to-metal and metal-to-poly capacitors are linear and have high Q with low temperature variations. However, the density (capacitance per unit area) of this type of capacitor is quite low due to relatively thick inter-level oxide layers.

The Chartered 0.18 μ m CMOS technology offers MiM (Metal-insulator-Metal) capacitors and PIS (Poly-Insulator-Substrate) capacitors. Compared to the conventional metal-to-metal capacitors, these capacitors have a relatively high density, which is 1.27fF/ μ m² and 4fF/ μ m² for the MiM and PIS capacitors, respectively. Only MiM capacitors are used in this design. Fig. 6.3 shows the structure of the MiM capacitor.

Figure 6.3 Structure of the MiM capacitor [44]

The Fuse-Top layer in the MiM capacitor acts as the top plate of the capacitor and the 2nd last metal layer act as the bottom layer. Thus, the MiM capacitor uses a thin oxide layer to achieve a much higher density than the conventional metal-to-metal capacitor. As it is implemented on the last two top metals, which are far from the substrate, it has a much lower parasitic capacitance compared to other structures.

6.3 Layout of Transistors

In a layout, a transistor with a large W/L aspect ratio is drawn either as multiple transistors or as a multifinger transistor. Multiple transistors are identical devices wired in parallel while a multifinger transistor is a single transistor which is splitted into a number of parallel equal parts arranged in a stack of polysilicon gates within the same active region. The rule of thumb is to choose the width of each finger such that the resistance of the finger is less than the inverse transconductance associated with the finger, i.e., $R_{gi} < 1/g_{mi}$ [39].

Transistor pairs in RFIC should be drawing in matching structures to provide good matching performance despite of the process variation. There are five types of matching structures: Strip, Common Centroid, ABBA-1, ABBA-2 and ABBA-2 gate-separated. The illustration of the configurations of these matching structures is shown in Fig. 6.4.

(iii) ABBA-1

(iv) ABBA-2

(v) ABBA-2 Gate-separated

Figure 6.4 Transistor matching structures

Several guidelines should be considered for achieving a good layout for transistors matching. Firstly, we should keep the transistors to be matched close to each other. Secondly, we should place groups of devices around a common geometric center. Thirdly, we should employ identical devices layouts and place them in identical surroundings. Finally, we should orient devices in the same direction.

6.4 Layout Design and Post-layout simulations

The layout of the conversion circuits is done using the Cadence Virtuoso Layout Editor. The placement of the devices and the interconnections are done according to the design rules provided by the CMS's PDK (Process Design Kit) for the 0.18 μm CMOS Analog/RF technology. The parasitic effect is very important at high frequencies, so it must be taken into account in the design of RFICs. Conductors and interconnections must be considered as distributed networks of resistors and capacitors. The general principle is to keep them small and short while meeting the current density requirement proposed by the design rules. In order to get the accurate results, we extract the parasitic capacitors and resistors from the layout, and add them back to the schematic to run the post-layout simulation. In this section, the layout design and post-layout simulation results of the Gilbert mixer in Chapter 4 and the even harmonic switching mixer in Chapter 5 are shown.

6.4.1 Gilbert Mixer

Fig. 6.5 (a) shows the layout of the Gilbert mixer shown in Fig. 4.1.

Figure 6.5 (a) Layout of the Gilbert mixer

Figure 6.5 (b) Mixer with parasitic effects

Fig. 6.5 (b) shows the mixer schematic with parasitic effects. Each node has a parasitic capacitance, which is extracted from the layout. There is also a parasitic resistor in series with each pin. The layout extraction process only enables to extract the parasitic capacitance and parasitic resistance. The parasitic inductance is not obtainable from the current design tools. The schematic in Fig. 6.5 (b) is used to do the post-layout simulations. The performance parameters of the mixer for post-layout simulations are shown in Table 6.1.

Table 6.1 Performance parameters for post-layout simulation

Gain (dB)	BW (GHz)	1dB (dBm)	IIP3 (dBm)	NF (dB)	Power (mW)
14.37	7.45	-11.28	-0.105	33.32	11.15

Comparing Table 6.1 with Table 4.2, most of the performance parameters do not vary so much, except bandwidth. Due to parasitic capacitances, bandwidth drops from 9GHz to 7.45GHz.

The LO leakage of the non-ideal mixer with the parasitic effects is also analyzed. In this case, odd harmonics at the RF ports were induced by parasitic effects as shown in Fig. 6.6. We focus on the first harmonic, which is the LO leakage caused by substrate coupling. The LO leakage of the ideal mixer shown in Fig. 4.12 is shown in Fig. 6.7 for comparison.

Figure 6.6 LO leakage for the non-ideal mixer

Figure 6.7 LO leakage for the ideal case

$$\begin{aligned} LO \text{ feedthrough} &= LO \text{ leakage} - LO \text{ Signal} \\ &= (-78.94\text{dBv}) - (-17.67\text{dBv}) = -61.27\text{dB} \end{aligned} \tag{6.1}$$

So for the CMOS Gilbert mixer, the LO feedthrough is around -60dB . Fig. 6.7 shows that there is no LO leakage in the ideal mixer. Therefore the parasitic effects of the circuit can induce the LO leakage and the DC offset.

6.4.2 Even Harmonic Switching Mixer

Fig. 6.8 shows the layout of the even harmonic switching mixer shown in Fig. 5.11.

Figure 6.8 The layout of the even harmonic switching mixer

The performance parameters of the mixer for post-layout simulations are shown in Table 6.2. Comparing with the ideal even harmonic switching mixer, the performance parameters of the non-ideal mixer do not change so much.

Table 6.2 Performance parameters for post-layout simulation

Gain (dB)	NF (dB)	1dB (dBm)	IIP3 (dBm)	Power (mW)
-8.37	5.32 at 100KHz	6.37	16.43	0

6.5 Conclusions

In this chapter, some layout issues of resistors, capacitors and transistors are illustrated first. The layout and post-layout simulation results for the Gilbert mixer and even harmonic switching mixer are shown. The simulation results of ideal case and non-ideal case for these two mixers are summarized in Table 6.3 and Table 6.4 respectively.

Table 6.3 Summary of the performance parameters for the Gilbert mixer

	Gain (dB)	BW (GHz)	1dB (dBm)	IIP3 (dBm)	NF (dB)	Power (mW)	LO Feed-through(dB)
Schematic	15.26	9	-11.71	0.43	32.00	11.15	-117.98
Post-layout	14.37	7.45	-11.28	-0.105	33.32	11.15	-61.27

We can see parasitic capacitors mainly influence the bandwidth and LO feedthrough. Other parameters do not change so much. For the ideal Gilbert mixer, the LO leakage is almost zero and there is no DC offset at the output. When adding parasitic effects to the ideal mixer, the feedthrough is -61.27dB.

Table 6.4 Summary of the performance parameters for the even harmonic mixer

	Gain (dB)	1dB (dBm)	IIP3 (dBm)	NF (dB)	Power (mW)
Schematic	-8.24	7.10	17.25	5.21	0
Post-layout	-8.37	6.37	16.43	5.32	0

From Table 6.4, we can see that the parasitic effects do not degrade the performance so much. That is because the parasitic effects extracted from the layout is quite small. Moreover, the even harmonic switching mixer is a passive circuit. The transistors work in the linear region. They are just switches. Electrically, they are equivalent to resistors. This even harmonic switching mixer could be used in the direct conversion receivers.

Chapter 7

Conclusions and Recommendations

This chapter summarizes the major contributions of this project entitled “Analysis and Design of CMOS Mixers for Direct Conversion Receivers”. Chapter 2 provides some background on the receiver architectures and fundamental parameters in receiver design. Some DC offset cancellation techniques are shown in chapter 3. Chapter 4 discusses the design of a CMOS double-balanced Gilbert mixer and the analysis of the LO-RF leakage in the mixer. Chapter 5 proposes a novel even harmonic switching mixer with DC offset free and low noise figure especially for direct conversion application. Finally Chapter 6 describes some layout design issues and post-layout simulation results. This chapter will be closed with the recommendation for the future work.

7.1 Conclusions

In this project, heterodyne, image-reject, direct conversion and low-IF receiver architectures have been reviewed. Most of today’s commercially available RF receivers utilize the conventional heterodyne architecture. The drawbacks of high cost, low integration level and high power consumption of the heterodyne architecture leads to the development of new receiver architectures. The direct conversion architecture is an alternative solution and believed to be the most simple and straightforward way to build a receiver. However, a number of issues which do not exist or are not serious in the heterodyne architecture become important in the direct conversion architecture, such as

DC offset, I/Q mismatch, even order distortion and so on. The DC offset is the most critical problem and some typical DC offset cancellation techniques have been discussed.

The analysis and design of CMOS mixers for direct conversion receivers have been explored. A CMOS double-balanced Gilbert mixer operating at the centre frequency of 2.45GHz for direct conversion applications has been designed using the Chartered Semiconductor Manufacturing (CSM) 0.18 μ m CMOS process, and simulated using Cadence SpectreRF. The LO-RF leakage caused by the LO mismatch in the Gilbert mixer is examined and analyzed for three scenarios of an ideal mixer, a non-ideal mixer with parasitic effects, and an ideal mixer with LO mismatch. The LO mismatch includes phase mismatch only, amplitude mismatch only and the combination of the two mismatches. It is found that if there is no LO mismatch, an ideal mixer will not have an LO leakage and DC offset. If a phase mismatch or amplitude mismatch exists, the LO leakage is proportional to the mismatch value. If both types of mismatches occur at the same time, the amplitude square of the LO leakage is equal to the sum of amplitude squares of each contribution as given by equation (7.1).

$$|V_{LOleakage_total}|^2 = |V_{phase_mismatch}|^2 + |V_{amplitude_mismatch}|^2 \quad (7.1)$$

The relation between the mismatch and the LO leakage is derived. The analysis agrees with simulation results. Moreover, the post-layout simulations show that the parasitic effects could induce an LO feedthrough of around -60dB.

A novel even harmonic switching mixer with DC offset free and low noise figure, especially for the direct conversion application, has been proposed. It has a -8.24dB gain,

a 5.21dB DSB noise figure at 100kHz, a 17.25dBm IIP3 and zero DC power consumption. The characteristic of the even harmonic mixer gives a zero DC offset. The low noise figure and high linearity are due to the switching type of the mixer. Switching type mixers need the transistors to switch sharply to obtain a good performance. However, to create an effective mixing at twice the LO frequency, the transistors are required to turn on slowly. Therefore, appropriate design parameters are chosen to optimize the circuit. The proposed mixer is actually a combination of the even harmonic mixer and the switching mixer. It attains a better performance than that of the above mixers. Moreover, this even harmonic switching mixer is simple and easy to design.

Table 7.1 summarizes the simulation results of the Gilbert mixer (GM), the simple switching mixer (SM) and the even harmonic switching mixer (EHSM). As shown below, the EHSM has the much better linearity than the active GM and the passive SM. Moreover, it has no DC offset and a low noise figure. So it could be used in the direct conversion receivers.

Table 7.1 Summary of the work

Work	Gain (dB)	1dB (dBm)	IIP3 (dBm)	NF (dB)	Power (mW)	DC offset
GM	15.26	-11.71	0.43	32.00	11.15	Yes
SM	-3.54	-7.67	1.35	7.96	0	Yes
EHSM	-8.24	7.10	17.25	5.21	0	No

7.2 Recommendations

This project only analyzed the LO-RF leakage of the CMOS Gilbert mixer. In the future research, the DC offset could be analyzed and it will be a much more challenging work. In Fig. 7.1, the LO signal which feedthroughs to the RF port is the LO leakage. A small part of this LO leakage further feedthroughs to the LNA input, then it is reflected back by the antenna, and amplified at the output of the LNA.

Figure 7.1 LO signal self-mixing

Ignoring the effect of LNA feedthrough and antenna reflection, we can use equation (7.2) to represent the DC offset.

$$DC\ Offset = LO\ Leakage \times \beta \times G \quad (7.2)$$

where the LO leakage and the mixer gain G are known. However, the reflection factor β is difficult to determine. Further research could be focus on the analysis of β . If taking consideration of the LNA feedthrough and antenna reflection, the problem becomes more complicated.

In the direct conversion receiver, the second-order input intercept point (IIP2) becomes sensitive. In a manner similar to the definition of the IIP3, two equal-amplitude interferers are applied at the input of mixer and their low-frequency beat signal is observed at the output. Plotting the beat signal power versus the input power and extrapolating the results yield the IIP2. However, it is difficult to find the correct IIP2 level through simulations. So the circuit should be fabricated and taken the measurement to obtain the IIP2.

Author's Publications

[1] J. J. Liu, M. A. Do, X. P. Yu, J. G. Ma, K. S. Yeo, and S. Jiang, "CMOS Even Harmonic Switching Mixer for Direct Conversion Receivers", accepted for publication by *Journal of Circuits, Systems, and Computers (JCSC)*.

[2] M. A. Do, J. J. Liu, K. S. Yeo and J. G. Ma, "Analysis of LO Leakage in CMOS Gilbert Mixer by Cadence SpectreRF for Direct Conversion Application", Proceeding of 2004 IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS 2004), Taiwan, December, 2004, pp. 309 – 312.

[3] J. J. Liu, M. A. Do, K. S. Yeo and J. G. Ma, "Analysis of LO Leakage due to LO Mismatch in CMOS Gilbert Mixer for Direct Conversion Application", Proceeding of 2004 IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS 2004), Taiwan, December, 2004, pp. 297 – 300.

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