Investigation of hybrid multilevel DC/AC inverters

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**NANYANG
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**INVESTIGATION OF HYBRID MULTILEVEL
DC/AC INVERTERS**

**LIU YU
SCHOOL OF ELECTRICAL & ELECTRONIC
ENGINEERING
2007**

Investigation of Hybrid Multilevel DC/AC Inverters

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University

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Summary

In modern technology, power electronics is very important and is now used in a great variety of products, including heat controls, light controls, motor controls, power supplies, vehicle propulsion systems, flexible ac transmission system (FACTS) and high-voltage dc (HVDC) system. A dc-ac converter is also known as an inverter. The function of an inverter is to produce an ac voltage /current, with regulable magnitude, frequency and phase angle. In recent years, multilevel inverters whose output voltages have many levels have attracted lots of research interest. The family of multilevel inverters has emerged as the solution for high power application, since it is hard to be implemented via single power semiconductor switch directly in medium-voltage network. As a cost effective solution, the application of multilevel inverters is also extended to medium and low power applications. Various kinds of multilevel inverters have been proposed, tested and installed. Hybrid multilevel inverters can synthesize more voltage levels than other kinds of multilevel inverters. A hybrid multilevel inverter is based on the connection of H-bridge (HBs) and dc capacitor voltage sources whose voltages are asymmetrical. Existing topologies of hybrid multilevel inverters include binary hybrid multilevel inverter (BHMI), quasi-linear hybrid multilevel inverter and trinary hybrid multilevel inverter (THMI).

Among the existing topologies of hybrid multilevel inverters, the THMI has the greatest number of output voltage levels using the same number of HBs for a given number of switching components among all sorts of multilevel inverters. I have investigated the aspects of the THMI. The circuit topology and operation of the THMI are described. Various modulation strategies for THMI are investigated. Low-frequency modulation strategies such as step modulation strategy and virtual stage modulation strategy are applicable in THMI. The simple modulation strategy can also be used in the THMI that includes more HBs. The problem of regenerative power in THMI is analyzed and a new solution to avoid regenerative power is presented. Based on the research results above, the possible application of the THMI is described. The first one is the application of reactive power compensation in which the problem of regenerative power is avoided.

The second one is the application in which the inverter always works at higher modulation indexes.

I have investigated the application of a three-phase nine-level THMI in static synchronous compensator (STATCOM) with unbalanced voltages. The issues about the counts of gate-turn-off thyristors (GTOs), series connection of GTOs, devices power losses, cooling systems and cost of dc capacitors are investigated. The application of the THMI in STATCOM is proved cost-effective because of reduced cost of switching components, cooling systems and dc capacitors. The control system of the STATCOM with unbalanced voltages is designed. Vector control based on synchronous frame transform lead to high dynamic performance of STATCOM. Moreover, the bus voltages are rebalanced during the unbalanced conditions and the compensation currents is limited within normal values. The new method by which the switching signals are generated from the reference inverter voltages is based on the comparison of amplitudes instead of angles. By this method, the output voltage of inverter does not contain lower-order harmonics under stable balanced conditions and the inverter can keep high dynamic performance under unbalanced conditions or transient processes. Simulation results and experimental results to verify the performance of the THMI are given.

I have also investigated a three-phase 81-level THMI for an induction motor drive. The dc links of H-bridges are supplied by bidirectional dc-dc converters, which can absorb power from some dc links in cases with lower modulation index and alleviate the ripples of dc link voltages. The space vector modulation used in the motor drive, which selects the voltage vectors that generate zero common-mode voltage in the load, working at low switching frequency. With up to 81-level voltage levels per phase, the THD is small, and the relationship between the fundamental load voltage and the modulation index is precisely linear. Vector controller is used to control induction motor, which results in high dynamic response for speeds or toques. The performance of the proposed inverter is confirmed by simulation and experiment.

A new topology of hybrid multilevel inverter is proposed in the thesis. It can work in three operation modes: single-direction-balance mode, bi-direction-balance mode and non-balance mode. Voltages of dc capacitors can be balanced in the single-direction-balance mode with a non-regenerative load. If a regenerative load is fed by the inverter,

the bi-direction-balance mode can be used to balance the dc capacitor voltages. When the inverter works in above modes, the switches in HBs except HB₁, switch at zero-voltage conditions. Less required components, only a dc source needed, the ability of self voltage balancing, the ability of voltage boosting and zero-voltage switching make the new inverter promising in low power application, especially with high frequency. Moreover, the non-balance mode with which the charging or discharging currents can be avoided is presented for the new inverter working in high power application. Another solution for high power application is that the inverter works in the single-direction-balance mode but with modified dc voltages. Simulation results and experimental results to verify the performances of the new inverter are given.

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List of Abbreviations

AEP	American Electric Power
AFE	Active Front End
ARCP	Auxiliary Resonant Commutated Pole
BHMI	Binary Hybrid Multilevel Inverter
CCMI	Capacitor-Clamped Multilevel Inverter
CMI	Cascade Multilevel Inverter
DCMI	Diode-Clamped Multilevel Inverter
FACTS	Flexible Ac Transmission System
GMI	Generalized Multilevel Inverter
GTO	Gate-Turn-Off Thyristor
HB	H-Bridge
HEV	High-power electric vehicle
HVDC	High-Voltage DC
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NPC	Neutral-Point Clamped
P2	Two-Level Phase Leg
PLL	Phase Lock Loop
PWM	Pulse-Width Modulation
STATCOM	STATic synchronous COMpensator
SVC	Static Var Compensator
THD	Total Harmonic Distortion
THMI	Trinary Hybrid Multilevel Inverter
UPFC	Unified Power Flow Controller
ZVT	Zero-Voltage Transition

List of Principal Symbols

J	phase angle in vector transformation
j	Angle of power factor
$ x _1$	amplitude of fundamental component of x (a periodical variable)
$ x _n$	amplitude of n th order harmonic of x (a periodical variable)
ABS	function of absolute value
B_b	bi-polar binary function
B_u	uni-polar binary function
C	capacitor
C	capacitance of capacitor
CC	cost of cooling system
D	diode
E	unit voltage
E_L	energy losses
E_T	transferred energy
F	switching function
FSS	function of switching angles
FT	target function
h	number of H-bridges in a single-phase inverter
i_A	currents flowing through an arm of a H-bridge
i_{an}	output phase current of the inverter
i_{dc}	current flowing through the dc bus
$\mathbf{I}_G$	current generated by STATCOM
$i_{G,a}$	A-phase current generated by STATCOM
$\mathbf{i}_{G,abc}$	three-phase inverter output currents
$\mathbf{i}_{G,dq+}$	inverter output currents in $dq+$ phase frame
$\mathbf{i}_{G,\alpha\beta}$	inverter output currents in $\alpha\beta$ phase frame
$\mathbf{I}_L$	load current
$\mathbf{I}_S$	source current

k	number of steps in the voltage between two phases of the load
l	ordinal of expected voltage level that the inverter outputs
L_I	inductance of interface impedance
m	number of steps of the phase voltage with respect to the negative terminal of the inverter,
M	modulation index
M_a	modulation index of A-phase
MAX	function of selecting one with the maximum value
MR	relative modulation index
n	neutral point
N_{null}	number of null voltage levels
p	penalty factor
P	power
$P_{D,ON}$	on-state power losses of an antiparallel diode
$P_{O,ON}$	on-state power losses of a GTO
$P_{O,SW}$	switching losses of a GTO
R_I	resistance of interface impedance
R_M	on-state resistance of the switch
S	switch
SS	switching signal
TSA	table of theoretical switching angles
v_{a0}	voltage across point a and point 0
v_{an}	voltage across point a and neutral point n
v_{an}	phase voltage of the multilevel inverter with respect to neutral point
$\mathbf{V}_B$	bus voltage
$v_{B,a}$	A-phase bus voltage
$\mathbf{v}_{B,abc}$	three-phase bus voltages
$\mathbf{v}_{B,dq+}$	bus voltages in $dq+$ phase frame
$\mathbf{v}_{B,\alpha\beta}$	bus voltages in $\alpha\beta$ phase frame
v_C	capacitor voltage
$v_{C,av}$	average unit voltage of dc capacitors

V_D	forward voltage of a diode
V_{dc}	voltage of dc source or dc capacitor
$\mathbf{V}_G$	generated voltage of STATCOM
$v_{G,a}$	A-phase voltage of the inverter in STATCOM
$\mathbf{v}_{G,abc}$	three-phase output voltage waveform of the inverter
$\mathbf{v}_{G,abc}^*$	three-phase reference output voltage of inverter
v_H	output voltage of a H-bridge
v_{in}	input voltage of a H-bridge
V_O	voltage drops of a GTO
v_{out}	output voltage of a H-bridge
$\mathbf{v}_{P,abc}^*$	three-phase output of power control module
v_{ref}	reference voltage
$\mathbf{V}_S$	source voltage
$\mathbf{v}_{U,abc}^*$	three-phase output of unbalanced voltage control module
WB	width of dead zone
$\mathbf{Z}_I$	interface impedance
$\mathbf{Z}_L$	equivalent impedance of the load
$\mathbf{Z}_S$	equivalent impedance of the source
β	number of virtual stages
Γ	an instantaneous variable
δ	final switching angle
$\Delta\delta$	shifted value of switching angle
ε	deviation of the capacitor voltage
η	list of [1,5,7,11,13...]
θ	theoretical switching angle
ς	number of switching angles in quarter wave of v_{an}
σ	number of positive/negative levels of v_{an}
$\sigma_{\max}$	maximum number of positive/negative of v_{an}

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1.1 Inverters in power electronics

Power electronics is very important in modern technology and is now used in a great variety of products [1, 2], including heat controls, light controls, motor controls, power supplies, vehicle propulsion systems, flexible ac transmission systems (FACTS) and high-voltage dc (HVDC) systems. The power electronics circuits can be classified into six categories: (i) diode rectifiers; (ii) ac-dc converters (controlled rectifiers); (iii) ac-ac converters (ac voltage controllers); (iv) dc-dc converters (dc choppers); (v) dc-ac converters (inverters) and (vi) static converters [2].

A dc-ac converter is also known as an inverter. The function of an inverter is to produce an ac voltage /current, with controlled magnitude and frequency. Fig. 1-1 is a conceptual block diagram of a dc/ac inverter. The dc voltage source of the inverter can be either a controlled/uncontrolled rectifier or batteries. A typical three-phase inverter is shown in Fig. 1-2.

Fig. 1-1. Block diagram of a dc/ac inverter

Fig. 1-2. Three-phase inverter

1.2 Introduction to multilevel inverters

Multilevel inverters contain several power semiconductors and capacitor voltage sources. Output voltages of multilevel inverters are the additions of the capacitor voltages due to the commutation of the switches. Fig. 1-3 shows a schematic diagram of one phase leg of inverters with several numbers of levels. The action of power semiconductors is represented by an ideal switch with several actions. A two-level inverter, as shown in Fig. 1-3 (a), generates an output voltage with two levels with respect to the negative terminal of the capacitor, while the three-level inverter of Fig. 1-3 (b) generates three voltages, and so on. Thus, the output voltages of multilevel inverters have several levels. Moreover, they can reach high voltage, while the power semiconductors must withstand only reduced voltages.

Multilevel inverters have been receiving increasing attention in recent years [3], since multilevel inverters have many attractive features. Firstly, the output voltage distortion is very low due to multiple levels in the output voltages. Secondly, the dv/dt of switches is low since the switches endure reduced voltage. Thirdly, the switches can operate at a lower switching frequency. Finally, in the applications of motor drives, the input currents have low distortions and the common-mode voltages are reduced. Additionally, the common-mode voltages can be eliminated using sophisticated modulation methods [4, 5].

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Fig. 1-3. One phase leg of an inverter

(a) Two levels, (b) Three levels, and (c) n levels

Various kinds of multilevel inverters have been proposed, tested and installed. They are diode-clamped (neutral-clamped) multilevel inverters [6]; capacitors-clamped (flying capacitors) multilevel inverters [3, 7], cascade multilevel inverters with separate dc sources [3, 8, 9], hybrid multilevel inverters [10-15], generalized multilevel inverters [16], mixed-level multilevel inverters [17], , multilevel inverters by the connection of three-phase two-level inverters [9], and soft-switched multilevel inverters [18-25]. The family tree of multilevel level inverters is shown as Fig. 1-4.

Fig. 1-4. Family tree of multilevel inverters

The family of multilevel inverters has emerged as the solution for high power application, since it is hard to be implemented via single power semiconductor switch

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directly in medium-voltage network [3, 26, 27]. Multilevel inverters have been applied to different high power applications, such as large motor drives [13, 17, 27-34], railway traction applications [28-31, 35], high voltage dc transmissions (HVDC) [36], unified power flow controllers (UPFC) [37-40], static var compensators (SVC) and static synchronous compensators (STATCOM) [36, 41-51]. The output voltage of the multilevel inverter has many levels synthesized from several dc voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the effort of output filters can be decreased. The transformers can be eliminated due to reduced voltage that the switch endures. Moreover, as cost effective solutions, the applications of multilevel inverters are also extended to medium and low power applications, such as electrical vehicle propulsion systems [27, 34], active power filters (APF) [52-55], voltage sag compensations [56], photovoltaic systems [57-59] and distributed power systems [26].

Multilevel inverter circuits have been around for about 30 years. The cascade multilevel inverter was first proposed in 1975 [60]. Separate dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. The diode-clamped inverter, also called the neutral-point clamped (NPC) inverter, was presented in 1980 [61]. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in 1980s. The capacitor-clamped multilevel inverter came in the 1990s [62, 63]. Although the cascade multilevel inverter was invented earlier, its application did not prevail until the mid 1990s. The advantages of cascade multilevel inverters were prominent for motor drives and utility applications. The cascade inverter has drawn great interest due to the great demand of medium-voltage high-power inverters. The cascade inverter is also used in regenerative-type motor drive application [64, 65]. Recently, some new topologies of multilevel inverters emerge, such as generalized multilevel inverters [16], mixed multilevel inverters [17], hybrid multilevel inverters [10, 14] and soft-switched multilevel inverters [18-22]. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels, such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. Moreover, as a cost-effective solution, the applications of multilevel inverters are also extended to low power application, such as photovoltaic systems [58], hybrid electrical vehicles [34] and voltage sag compensation [56], in which the effort of output filter

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components can be decreased much due to low harmonics distortions of output voltages of the multilevel inverters.

1.3 Multilevel inverter using diode/capacitor clamped topologies

In this category, the switching devices are connected in series to make up the desired voltage rating and output levels. The inner voltage points are clamped by either two extra diodes or one high frequency capacitor. The switching devices of an m -levels inverter are required to block a voltage level of $V_{dc}/(m-1)$. The clamping diode or clamping capacitor needs to have different voltage rating for different inner voltage levels.

1.3.1 Diode-clamped inverter

A three-level diode-clamped inverter is shown in Fig. 1-5 (a). In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2 . The middle point of the two capacitors, n , can be defined as the neutral point. The output voltage v_{an} has three states: E , 0 and $-E$. For voltage level E , switches S_1 and S_2 need to be turned on; for $-E$, switches $S_{1'}$ and $S_{2'}$ need to be turned on; and for the 0 level, S_2 and $S_{2'}$ need to be turned on.

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Fig. 1-5. Diode-clamped multilevel inverter circuit topologies
(a) Three-level (b) Five-level

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and $D_{1'}$. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S_1 and S_2 turn on, the voltage across a and 0 is $2E$, i.e., $v_{a0} = 2E$. In this case, $D_{1'}$ balances out the voltage sharing between $S_{1'}$ and $S_{2'}$ with $S_{1'}$ blocking the voltage across C_1 and $S_{2'}$ blocking the voltage across C_2 . Notice that output voltage v_{an} is ac, and v_{a0} is dc. The difference between v_{an} and v_{a0} is voltage across C_2 , which is E . If the output is removed between a and 0 , then the circuit becomes a dc/dc converter, which has three output voltage levels: E , 0 and $-E$.

Fig. 1-5 (b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C_1 , C_2 , C_3 and C_4 . For dc bus voltage $4E$, the voltage across each capacitor is E , and each device voltage stress will be limited to one capacitor voltage level E through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are five switch combination to synthesize five level voltage across a and n .

- For voltage level $v_{an} = 2E$, turn on all upper switches $S_1 \sim S_4$.

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- For voltage level $v_{an} = E$, turn on three upper switches $S_2 \sim S_4$ and one lower switch $S_{1'}$.
- For voltage level $v_{an} = 0$, turn on two upper switches S_3 and S_4 and two lower switches $S_{1'}$ and $S_{2'}$.
- For voltage level $v_{an} = -E$, turn on one upper switch S_4 and three lower switches $S_{1'} \sim S_{3'}$.
- For voltage level $v_{an} = -2E$, turn on all lower switches $S_{1'} \sim S_{4'}$.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turn on. In this example, the four complementary pairs are $(S_1, S_{1'})$, $(S_2, S_{2'})$, $(S_3, S_{3'})$, and $(S_4, S_{4'})$.

Although each active switching device is only required to block a voltage level of E , the clamping diodes must have different voltage ratings for reverse voltage blocking. Using $D_{1'}$ of Fig. 1-5 (b) as an example, when lower devices $S_{2'} \sim S_{4'}$ are turned on, $D_{1'}$ needs to block three capacitor voltages, or $3E$. Similarly, D_2 and $D_{2'}$ need to block $2E$, and D_1 needs to block $3E$.

1.3.2 Capacitor-clamped inverter

Fig. 1-6 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter with dependent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig. 1-6 (a) provides a three-level output across a and n , i.e. $v_{an} = E, 0$, or $-E$. For the voltage level E , switches S_1 and S_2 need to be turned on; for $-E$, switches $S_{1'}$ and $S_{2'}$ need to be turned on; and for the 0 level, either pair $(S_1, S_{1'})$ or $(S_2, S_{2'})$ needs to be turned on. Clamping capacitor C_1 is charged when S_1 and $S_{1'}$ are turned on, and is discharged when S_2 and $S_{2'}$ are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination.

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 1-6 (b) as the example, the voltage of the

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five-level phase-leg a output with respect to the neutral point n , v_{an} , can be synthesized by the following switching combinations.

Fig. 1-6. Capacitor-clamped multilevel inverter circuit topologies

(a) Three-level (b) Five-level

- For voltage level $v_{an} = 2E$, turn on all upper switches $S_1 \sim S_4$.
- For voltage level $v_{an} = E$, there are three combinations:
 - $S_1, S_2, S_3, S_{1'}: v_{an} = 2E$ (upper C_4) - E (C_1);
 - $S_2, S_3, S_4, S_{4'}: v_{an} = 3E$ (C_3) - $2E$ (lower C_4); and
 - $S_1, S_3, S_4, S_{3'}: v_{an} = 2E$ (upper C_4) - $3E$ (C_3) + $2E$ (C_2).
- For voltage level $v_{an} = 0$, there are six combinations:
 - $S_1, S_2, S_{1'}, S_{4'}: v_{an} = 2E$ (upper C_4) - $2E$ (C_2);
 - $S_3, S_4, S_{3'}, S_{4'}: v_{an} = 2E$ (C_2) - $2E$ (lower C_4);
 - $S_1, S_3, S_{1'}, S_{3'}: v_{an} = 2E$ (upper C_4) - $3E$ (C_3) + $2E$ (C_2) - E (C_1);
 - $S_1, S_4, S_{2'}, S_{3'}: v_{an} = 2E$ (upper C_4) - $3E$ (C_3) + E (C_1);
 - $S_2, S_4, S_{2'}, S_{4'}: v_{an} = 3E$ (C_3) - $2E$ (C_2) + E (C_1) - $2E$ (lower C_4); and
 - $S_2, S_3, S_{1'}, S_{4'}: v_{an} = 3E$ (C_3) - E (C_1) - $2E$ (lower C_4).
- For voltage level $V_{an} = -E$, there are three combinations:
 - $S_1, S_{1'}, S_{2'}, S_{3'}: v_{an} = 2E$ (upper C_4) - $3E$ (C_3);
 - $S_4, S_{2'}, S_{3'}, S_{4'}: v_{an} = E$ (C_1) - $2E$ (lower C_4); and

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- $S_3, S_{1'}, S_{3'}, S_{4'}$: $v_{an} = 2E (C_2) - E (C_1) - 2E (\text{lower } C_4)$.
- For voltage level $v_{an} = -2E$, turn on all lower switches, $S_{1'} \sim S_{4'}$.

In the preceding description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode. By proper selection of capacitor combinations, it is possible to balance the capacitor charge.

1.4 Multilevel inverters using HBs connected

The basic structure is based on the connection of HBs. Fig. 1-7 shows the power circuit for one phase leg of a multilevel inverter with three HBs (HB₁, HB₂ and HB₃) in each phase. Each HB is supplied by a separate dc source. The resulting phase voltage is synthesized by the addition of the voltages generated by the different HBs. If the dc link voltages of HBs are identical, the multilevel inverter is called the cascade multilevel inverter. However, it is possible to have different values among the dc link voltages of HBs, and the circuit can be called as the hybrid multilevel inverter.

Fig. 1-7. Multilevel inverter based on the connection of HBs

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1.4.1 Cascade multilevel inverter (CMI)

In cascade multilevel inverter, the dc link voltages of HBs are identical, etc. in Fig. 1-7,

$$V_{dc1} = V_{dc2} = V_{dc3} = E \quad (1.1)$$

where E is unit voltage. Each HB generates three voltages at the output: $+E$, 0 , and $-E$. This is made possible by connecting the capacitors sequentially to the ac side via the three power switches. The resulting output ac voltage swings from $-3E$ to $3E$ with seven levels as shown in Fig. 1-8.

Fig. 1-8. Waveforms of cascade multilevel inverter

1.4.2 Binary hybrid multilevel inverter (BHMI)

In binary hybrid multilevel inverter, the dc link voltages of HB_i (the i th HB), V_{dci} , is $2^{i-1}E$. In a 3-HB one phase leg,

$$V_{dc1} = E \quad V_{dc2} = 2E \quad V_{dc3} = 4E \quad (1.2)$$

As shown in Fig. 1-9, the output waveform, v_{an} , has 15 levels. One of the advantages is the HB with higher dc link voltage has lower number of commutation and thereby reducing the associated switching losses. Manjrekar, et. al [14] illustrates a seven-level inverter using this hybrid topology. The HB with higher dc link voltage consists of lower switching frequency component, e.g. IGCT. The higher switching frequency components, e.g. IGBT, are used to construct the HB with lower dc link voltage.

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Fig. 1-9. Waveforms of binary hybrid multilevel inverter

1.4.3 Quasi-linear multilevel inverter (QLMI)

In quasi-linear multilevel inverter, the dc link voltages of HB_i , V_{dci} can be expressed as

$$V_{dci} = \begin{cases} E & i = 1 \\ 2 \times 3^{i-2} E & i \geq 2 \end{cases} \quad (1.3)$$

In a 3-HB one phase leg,

$$V_{dc1} = E \quad V_{dc2} = 2E \quad V_{dc3} = 6E \quad (1.4)$$

As shown in Fig. 1-10, the output waveform, v_{an} , has 19 levels.

Fig. 1-10. Waveforms of quasi-linear multilevel inverter

1.4.4 Trinary hybrid multilevel inverter (THMI)

In trinary hybrid multilevel inverter, the dc link voltages of HB_i , V_{dc_i} , is $3^{i-1}E$. In a three-HB one phase leg,

$$V_{dc1} = E \quad V_{dc2} = 3E \quad V_{dc3} = 9E \quad (1.5)$$

As shown in Fig. 1-11, the output waveform, v_{an} , has 27 levels. To the best of author's knowledge, this circuit has the greatest level number for a given number of HBs among existing multilevel inverters.

Fig. 1-11. Waveforms of trinary hybrid multilevel inverter

1.5 Other kinds of multilevel inverters

1.5.1 Generalized multilevel inverters (GMI)

A generalized multilevel inverter topology has previously been presented in [16]. The existing multilevel inverters, such as diode-clamped and capacitor-clamped multilevel inverters, can be derived from this generalized inverter topology. Moreover, the generalized multilevel inverter topology can balance each voltage level by itself

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regardless of load characteristics. Therefore, the generalized multilevel inverter topology provides a true multilevel structure that can balance each dc voltage level automatically at any number of levels, regardless of active or reactive power conversion, and without any assistance from other circuits. Thus, in principle, it provides a complete multilevel topology that embraces the existing multilevel inverters.

As shown in Fig. 1-12, the basic cell is a two-level phase leg, so this generalized multilevel inverter is called P2 multilevel inverter. Each switching device, diode, or capacitor's voltage is E , i.e., $1/(m-1)$ of the dc-link voltage. Any inverter with any number of levels, including the conventional two-level inverter can be obtained using this generalized topology.

Fig. 1-12. Generalized P2 multilevel inverter structure

As an application example, a four-level bidirectional dc/dc converter, shown in Fig. 1-13, is suitable for the dual-voltage system to be adopted in future automobiles. The four-level dc/dc converter has a unique feature, which is that no magnetic components are

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needed. From this generalized multilevel inverter topology, several new multilevel inverter structures can be derived.

Fig. 1-13. Application example: a four-level P2 converter for the dual-voltage system in automobiles

1.5.2 Mixed-level multilevel inverter topologies

For high-voltage high-power applications, it is possible to adopt multilevel diode-clamped or capacitor-clamped inverters to replace the full-bridge cell in a cascade multilevel inverter [17]. The reason for doing so is to reduce the amount of separate dc sources. The nine-level cascade inverter requires four separate dc sources for one phase leg and twelve for a three-phase inverter. If a three-level inverter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate dc sources are needed for one phase leg and six for a three-phase inverter. The configuration can be considered as having mixed-level multilevel cells because it embeds multilevel cells as the building block of the cascade multilevel inverter.

1.5.3 Multilevel inverters by the connection of three-phase two-level inverters

Standard three-phase two-level inverters are connected by transformers as shown in Fig. 1-14 [9]. In order for the inverter output voltages to be added up, the inverter outputs of the three modules need to be synchronized with a separation of 120° between each

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phase. For example, obtaining a three-level voltage between outputs a and b , the voltage is synthesized by $V_{ab} = V_{a1-b1} + V_{a1-b1} + V_{a1-b1}$. The phase between b_1 and a_2 is provided by a_3 and b_3 through an isolated transformer. With three inverters synchronized, the voltages V_{a1-b1} , V_{a1-b1} , V_{a1-b1} are all in phase; thus, the output level is simply tripled.

Fig. 1-14. Cascade inverter with three-phase cells

1.5.4 Soft-switched multilevel inverters

There are numerous ways of implementing soft-switching methods, such as zero voltage switching (ZVS) and zero current switching (ZCS), to reduce the switching losses and to increase efficiency for different multilevel inverters. For the cascade multilevel inverter, because each inverter cell is a two-level circuit, the implementation of soft switching is not at all different from that of conventional two-level inverters. For capacitor- or diode-clamped inverters, however, the choices of soft-switching circuit can be found with different circuit combinations [18, 21, 23-25]. Although zero-current switching is possible [66], most literatures proposed zero-voltage-switching types including auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations.

1.6 Multilevel inverters in high power applications

In medium-voltage network, it is hard to connect a single power semiconductor switch directly to medium-voltage grids (2.3, 3.3, 4.16, or 6.9 kV). Multilevel inverters are presented as the solutions for working with higher voltage levels.

1.6.1 Large motor drives with non-regenerative front ends.

Diode-clamped three-level multilevel inverters are now widely applied in medium-voltage (2.3, 3.3, 4.16, and even 6 kV) application, using an IGBT with forced-air cooling. There applications cover a wide range of high-power loads including fans, pumps, blowers, compressors, and conveyors. A three-level capacitor-clamped multilevel inverter is also used as a motor drive [67]. A seven -level cascade multilevel inverter is used in non-regenerative drives in 2.3 kV network [8]. The input part of each HB has a three-phase diode rectifier, which does not allow the regeneration of power. Tolbert, et. al [68] presents a transformerless multilevel inverter as an application for high-power electric vehicle (HEV) motor drives. Multilevel inverters have almost no electromagnetic interference or common-mode voltage; and make an HEV more accessible/safer and open wiring possible for most of an HEV's power system. A hybrid seven-level inverter is applied in 4.16 kV system, in which the top HB uses IGBT and the low one uses GTO [14].

1.6.2 Large motor drives with regenerative front ends

The use of a three-level active front end (AFE) at the input side of a three-level diode-clamped inverter has become a very popular solution for high-power regenerative loads [69, 70]. Especially in [70], two three-level AFEs are used in a so-called tandem configuration. Rodriguez, et. al [71] presents a multilevel converter with regeneration capacity. Each cell in the converter contains a single-phase inverter at the output side and a PWM rectifier at the input side. The output side inverters of the cells are connected in series, while the input side rectifiers are connected in parallel through the input transformer. A single-phase AFE, instead of a three-phase one, has been considered at the

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input side of each cell for the following reasons: less power semiconductors and simpler control.

1.6.3 Applications in power systems

The first unified power flow controller (UPFC) in the world was based on a diode-clamped three-level inverter [38]. The UPFC is comprised of the back-to-back connection of two identical GTO thyristor-based three-level converters, each rated at 160 MVA. It was commissioned in mid 1998 at the Inez Station of American Electric Power (AEP) in Kentucky for voltage support and power-flow control. On the other hand, the cascade multilevel inverter is best suited for harmonic/reactive compensation and other utility applications [48, 72, 73], since each HB inverter unit can balance its dc voltage without requiring additional isolated power sources. GEC Alsthom T&D has commercialized the cascade multilevel inverter for reactive power compensation/generation (STATCOM).

1.7 Multilevel inverters in medium and low power application

The ac output terminal voltage that multilevel inverters synthesize have low harmonic distortion, thus the filter requirement is reduced. Moreover, with the topologies of multilevel inverters, the transformers can be eliminated. In recent years, the volume and price of active components (semiconductor switches) decreased much, while the passive components, such as inductors, capacitors or transformers are kept the almost same. Therefore, in the medium and low application, the systems with the configuration of multilevel inverters can be compacter and cheaper.

1.7.1 Photovoltaic systems

Various topologies of multilevel inverters are investigated for the application of photovoltaic system in [57]. Amongst the topologies for transformerless systems, the diode clamped multilevel inverters and the cascade multilevel inverters have been identified as the most promising topologies. The design and control issues associated with

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the development of a 1.8 kW prototype single-phase grid-connected photovoltaic system incorporating a cascade multilevel inverter are discussed in [59].

1.7.2 Voltage sag compensation

A cascade multilevel inverter was studied as a cost-effective way of series sag compensation, because it eliminates the bulky injection transformers and other large filter components used in series active filters [74]. Batteries and high-current automotive MOSFETs proved to be interesting options in terms of energy storage and switching components for this design.

1.7.3 Distributed energy application

Distributed energy system, mostly those using alternative energies such as fuel cells or photovoltaic panels, can be easily configured with a separate source connected through the power conversion circuits used as an energy module or building block to provide individual output. A cascade multilevel inverter can then be configured with multiple modules. Such a system does not need a transformer to provide isolation, and the system can be constructed in a cost effective manner [26].

1.8 Objective

Among different sorts of multilevel inverters mentioned above, one of most popular topologies is the cascade multilevel inverter that is based on the series connection of H-bridges (HBs) with separate dc sources whose voltages are equal. The cascade multilevel inverter requires less number of components than the diode-clamped multilevel inverter and the capacitor-clamped multilevel inverter [3]. Moreover, the problem of voltage balancing is avoided because of separate dc sources. The flexibility of circuit layout is another advantage of the cascade multilevel inverter. Modularized circuit layout and packaging is possible because each HB has the same structure, and there are no extra clamping diodes or voltage balancing circuits. The number of output voltage levels can be easily adjusted by adding or removing the HBs.

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The hybrid multilevel inverter is based on the connection of HBs and dc capacitor voltage sources whose voltages are asymmetrical. Existing topologies of hybrid multilevel inverters include BHMI, quasi-linear hybrid multilevel inverter and THMI. The hybrid multilevel inverter inherits the advantages of the cascade multilevel inverter. Moreover, the asymmetry of dc voltages allows more levels to be created in the output voltage, and thus reduces the harmonic contents with fewer HBs required. Recent trends in the power semiconductor technology indicate a tradeoff in the selection of power devices in terms of switching frequency and voltage-sustaining capability [75]. Normally, the voltage-blocking capability of faster devices such as insulated gate bipolar transistors (IGBTs) and the switching speed of high-voltage thyristor-based devices like integrated gate commutated thyristors (IGCTs) are found to be limited. In the hybrid multilevel inverter, the switches in higher/lower voltage HBs switch at lower/higher frequency, so the higher/lower-voltage lower/higher-speed switches can be used in higher/lower voltage HBs.

The topology of THMI was proposed in [10]. In [13, 76], the topology of the THMI is studied and the problem of regenerative power in the THMI was found. Among the existing topologies of hybrid multilevel inverters, the THMI has the greatest number of output voltage levels using the same number of HBs. To the best of the author's knowledge, actually, the THMI has the greatest level number for a given number of switching components among all multilevel inverters.

The THMI is promising because of the above prominent advantage. However, the existing investigation of the THMI is still not enough. Therefore, the first objective is to study the modulation and control strategies for the THMI. The problem of regenerative power will be analyzed and a solution for the problem will be presented.

There are many kinds of multilevel inverters and many sorts of applications for different multilevel inverters. Based on the investigation of the THMI, the reactive power shunt compensator in power system is regarded as one of the applications for which the THMI are most suitable. A STATCOM operates as a shunt-connected static var compensator whose capacitive or inductive output current can be controlled independent of the ac system voltage. The STATCOM is one of key FACTS controller. The FACTS technology has been widely used in power system to increase the capacity of existing

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lines and stability of power system. The definition of FACTS is that alternating current transmission systems incorporating power electronic-based and other static controllers to enhance controllability and increase power transfer capability [42]. It has been long been recognized that the steady-state transmittable power can be increased and the voltage profile along the line can be controlled by appropriate reactive power shunt compensation. The purpose of this reactive compensation is to change the natural electrical characteristics of the transmission line to make it more compatible with the prevailing load demand. The ultimate objective of applying reactive shunt compensation in a transmission system is to increase the transmittable power. The STATCOM is based on a voltage-sourced inverter or a current-sourced inverter. From an overall cost point of view, the voltage-source inverters are preferred. For the voltage-source inverter, its ac output voltage is controlled such that it is just right for the required reactive current. The dc capacitor voltage is automatically adjusted as required to serve as a voltage source for the inverter. The earlier implementation of the STATCOM are based on eight two-level voltage-sources switching at line frequency [44, 45]. To meet the high voltage requirement in transmission system, the multilevel inverters are used in the STATCOM. Studies of a three-level and five-level diode-clamped multilevel inverter for the STATCOM is introduced in [77] and [78], respectively. Ooi, et. al [41] offers a topology for the implementation of a shunt STATCOM based on a grouping of four three-level diode-clamped multilevel inverter, switching at line frequency and coupled to the ac system through wye/wye and wye/delta phase-shifting transformers. For over two decades, the cascade multilevel inverter has demonstrated numerous advantages over its counterparts both in university laboratories and in industrial products for the STATCOM [46, 48, 79-83] due to scalable power rating, modularity, and cost effective. A ± 75 MVar STATCOM based on the cascade multilevel inverter was developed by GEC Alstom T&D Ltd. [84, 85]. As variations of the cascade multilevel inverter, hybrid multilevel inverters are also promising for the STATCOM. The application of the BHMI in the STATCOM has also been investigated because the BHMI can generate more voltage levels than the cascade multilevel inverter with the same number of switches [35, 50, 51].

Therefore, the application of the THMI in STATCOM is investigated thoroughly. For a STATCOM system, due to the topology of THMI, the THMI will use fewer switching components than the cascade multilevel inverter and the BHMI. Moreover, cost of

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cooling systems and dc capacitors will be expected to be less in the THMI for a STATCOM.

The motor drive is the most important application for the inverters. Recently, multilevel inverters have been widely applied in motor drives. Diode-clamped three-level multilevel inverters are now widely applied in medium-voltage (2.3 kV, 3.3 kV, 4.16 kV, and even 6 kV) application [1]. A seven-level cascade multilevel inverter is used in non-regenerative drives in 2.3 kV network [2]. Lai, et. al [3] presents a transformerless multilevel inverter as an application for high-power electric vehicle (HEV) motor drives. A hybrid seven-level inverter is applied in 4.16 kV system, in which the top HB uses IGBT and the low one uses GTO [4]. With multiple voltage levels, the THD of voltage is decreased. At the same time, it is possible to reduce, and even eliminate the common mode voltage with the topology of multilevel inverter.

Therefore, a three-phase THMI for an induction motor drive is proposed. 81-level output voltages per phase result in a very low THD. To overcome the problem of regenerative power of some HBs and stabilize the dc link voltages of HBs, bidirectional dc-dc converters are used as dc sources of HBs. The space vector modulation used here, which selects voltage vectors that generate zero common-mode voltage in the load, works at lower switching frequency. Vector controller is used to control induction motor, which results in high dynamic response for speeds or torques.

In final part, new topologies of hybrid multilevel inverters are proposed. The definition of a hybrid multilevel inverter is that the topology of the hybrid multilevel inverter is based on the connection of HBs and capacitor voltage sources whose voltages are asymmetrical in the thesis. Existing topologies of hybrid multilevel inverters are based on series connection of HBs. The difference ratios of dc source voltages of HBs, such as 1:2:4 [14, 15, 35], 1:2:6 [10] and 1:3:9 [10-13], have been presented. Rech, et. al [76] proposed a generalized design methodology for hybrid multilevel inverters based on series connection of HBs. It has been difficult to find new valuable topologies of hybrid multilevel inverters only by changing the ratio of dc source voltages. The chance of new topologies lies in the different ways that HBs and capacitor voltage sources are connected. In the thesis, a new hybrid multilevel inverter based on a special connection of HBs and capacitor voltage sources is proposed.

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In short, the objectives of this research work are as follows:

- To investigate the aspects about the THMI, including the modulation strategies applicable to the THMI, the solutions to avoid regenerative power in the THMI and possible applications of the THMI;
- To study the application of THMI in the STATCOM with unbalance voltages and design the control system of the STATCOM;
- To investigate an 81-level THMI for motor drive with zero common-mode voltage;
- To propose new topologies of hybrid multilevel inverters.

1.9 Major contributions

The major contributions are:

- Investigate the modulation strategies applicable to the THMI based on the investigation of the topology and the switching pattern of the THMI. The low-frequency modulation strategies such as the step modulation strategy and the virtual stage modulation strategy are suitable in THMI. Additionally, the simple modulation strategy can be used in the THMI with many voltage levels.
- Propose a cost-effective solution to avoid regenerative power in the THMI without using extra equipment, such as bi-directional dc-dc converters, controlled bridge ac-dc converters or output transformers. The dc capacitor voltages of lower voltage HBs are kept stable by the proposed method. The tradeoff is that power quality will decrease a little with lower modulation indexes.
- Investigate the application of THMI in the STATCOM, which is cost-effective because of reduced cost of switching components, cooling systems and dc capacitors.
- Design the control scheme for the above the STATCOM with unbalanced voltages. Vector control based on synchronous frame transforms lead to high dynamic performance of the STATCOM. Moreover, the bus voltages are rebalanced during the unbalanced conditions and the compensation currents are limited within

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normal values. The new method by which the switching signals are generated from the reference inverter voltages is based on the comparison of amplitudes instead of angles. By this method, the output voltage of inverter does not contain lower-order harmonics under stable balanced conditions and the inverter can keep high dynamic performance under unbalanced conditions or transient processes.

- Investigate the application of the 81-level THMI for motor drive with zero common mode voltage. A space vector modulation is designed to eliminate common mode voltage and keep the linearity between modulation index and fundamental load voltage. Bidirectional dc-dc converters are implemented as dc sources of HBs. Vector controller is designed to control the induction motor to achieve high dynamic response for speeds and torques.
- Propose a new topology of hybrid multilevel. It can work in three operation modes: single-direction-balance mode, bi-direction-balance mode and non-balance mode. Voltages of dc capacitors can be balanced in the single-direction-balance mode with a non-regenerative load. If the regenerative load is fed by the inverter, the bi-direction-balance mode can be used to balance the dc capacitor voltages. When the inverter works in above modes, the switches in HBs (except HB_1) switch at zero-voltage conditions. Less required components, only a dc source needed, the ability of self voltage balancing, the ability of voltage boosting and zero-voltage switching make the new inverter promising in low power application, especially with high frequency. Moreover, the non-balance mode with which the charging or discharging currents can be avoided is presented for the new inverter working in high power application. Another solution for high power application is that the inverter works in the single-direction-balance mode but with modified dc voltages.

1.10 Organization of the thesis

In the first chapter, the background of power electronics, inverters and multilevel inverters are introduced. The objective, main contributions of the research work are also given in the first chapter.

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The content of the second chapter focuses on the investigation the THMI. The topology and operation principle of the THMI are introduced. The theoretical prove and comparison results are given to show that the THMI have the greatest number of voltage levels using same number of components among multilevel inverters. Modulation strategies suitable for the THMI are the subject matters for an in depth study. The problem of regenerative power in THMI is analyzed and a new solution to avoid regenerative power is presented. Based on the research results above, the possible application of the THMI is described. Experimental results to verify the performance of modulation strategies and the new solution to avoid regenerative power in the THMI are given.

In the third chapter, the application of a three-phase nine-level THMI in a STATCOM with unbalanced voltages is specified. The issues about the counts of GTOs, series connection of GTOs, devices power losses, cooling systems and cost of dc capacitors are investigated. The control system of the STATCOM with unbalanced voltages is studied thoroughly. At first, vector representation and transformation of instantaneous three-phase quantities are given. The control system contains three modules: power control module, unbalanced voltage control module and inverter control modules, which are specified one by one. Finally, simulation experimental results are given to verify the performance of the THMI.

In the fourth chapter, the application of an 81-level THMI for a motor drive with zero common mode voltage is described. A space vector modulation is introduced to achieve zero common mode voltage, and to obtain a good linearity between the fundamental load voltage and modulation index. The bidirectional dc-dc converters are used as dc sources of HBs. The design and operation of the converters are described. A vector controller for induction motor is introduced. The performance of the proposed THMI inverter for the motor drive is confirmed by simulation and experiment.

In the fifth chapter, a new topology of hybrid multilevel inverter is proposed. The general topology of the new inverter is presented. The new inverter can operate in three modes: single-direction-balance mode, bi-direction-balance mode and non-balance mode. Principles of operation in three operation modes are described. Possible applications of the new inverter are pointed out. Simulation results and experimental results to verify the

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performances of the new inverter are given. Finally, comparison with other topologies of multilevel inverters, comparison of switching losses among three operating modes, and energy losses during voltage balancing is discussed.

Finally, a summary of the research work and some suggestions for further developments are given in the sixth chapter.

Chapter 2 Investigation of THMI

2.1 Topology and operation

A single-phase THMI with h HBs connected in series is shown in Fig. 2-1. The key feature of the THMI is that the ratio of dc link voltage is $1:3:\dots:3^{h-1}$, where h is the number of HBs. The maximum number of synthesized voltage levels is 3^h .

Fig. 2-1. Configuration of THMI

As shown in Fig. 2-1, v_{Hi} represents the output voltage of the i th HB. V_{dci} represents the dc link voltage of the i th HB. A switching function, F_i , is used to relate V_{Hi} and V_{dci} as shown in

$$v_{Hi} = F_i \cdot V_{dci} \quad (2.1)$$

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The value of F_i can be either 1 or -1 or 0. For the value 1, switches S_{i1} and S_{i4} need to be turned on. For the value -1, switches S_{i2} and S_{i3} need to be turned on. For the value 0, switches S_{i1} and S_{i3} need to be turned on or S_{i2} and S_{i4} need to be turned on. Table 2-1 shows the relationship between the switching function, the output voltage of a HB and states of switches.

Table 2-1. Relationship between the switching function, output voltage of a HB and states of switches

F_i	v_{Hi}	S_{i1}	S_{i2}	S_{i3}	S_{i4}
1	V_{dci}	conduct	block	block	conduct
-1	$-V_{dci}$	block	conduct	conduct	block
0	0	conduct	conduct	block	block
0	0	block	block	conduct	conduct

The output voltage of the THMI, v_{an} , is the summation of the output voltages of HBs.

$$v_{an} = \sum_{i=1}^h v_{Hi} \quad (2.2)$$

From (2.1) and (2.2), we can get

$$v_{an} = \sum_{i=1}^h F_i \cdot V_{dci} \quad (2.3)$$

In a single-phase h -HB THMI, the ratio of dc link voltage is $1:3:\dots:3^{h-1}$. Suppose E is unit voltage, the dc link voltage can be expressed as:

$$V_{dci} = 3^{i-1} E \quad (2.4)$$

From (2.3) and (2.4), we can get

$$v_{an} = \sum_{i=1}^h F_i \cdot 3^{i-1} E \quad (2.5)$$

Suppose l is ordinal of expected voltage level that the inverter outputs. If l is positive or zero, the inverter outputs the positive l th voltage level. If l is negative, the inverter outputs the negative $(-l)$ th voltage level. The value of F_{ak} can be determined by

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$$\begin{aligned}
F_{a4} &= B_u(ABS(l) - 13) \cdot ABS(l) / l & l_3 &= l - F_{a4} \cdot 27 \\
F_{a3} &= B_u(ABS(l_3) - 4) \cdot ABS(l_3) / l_3 & l_2 &= l_3 - F_{a3} \cdot 9 \\
F_{a2} &= B_u(ABS(l_2) - 1) \cdot ABS(l_2) / l_2 & l_1 &= l_2 - F_{a2} \cdot 3 \\
F_{a1} &= B_u(ABS(l_1)) \cdot ABS(l_1) / l_1
\end{aligned} \tag{2.6}$$

where ABS is the function of absolute value and B_u is defined as

$$B_u(t) = \begin{cases} 1 & t > 0 \\ 0 & t \leq 0 \end{cases} \tag{2.7}$$

From (2.6), we can get the relationship between the output voltage of the inverter, v_{an} , and the values of switching functions in the THMI with different number of HBs. In the case of a two-HB THMI, Table 2-2 shows the relationship between the output voltage of the inverter and the values of switching functions. The waveforms of a single-phase two-HB THMI is shown in Fig. 2-2.

Table 2-2. Relationship between the output voltage of the inverter and the values of switching functions in a single-phase two-HB THMI

v_{an}	$-4E$	$-3E$	$-2E$	$-E$	0
F_1	-1	0	1	-1	0
F_2	-1	-1	-1	0	0
v_{an}	$4E$	$3E$	$2E$	E	
F_1	1	0	-1	1	
F_2	1	1	1	0

Fig. 2-2. Waveforms of a single-phase two-HB THMI

Chapter 2. Investigation of THMI

The output voltage of a single-phase three-HB is shown in Fig. 1-11. It is evident that v_{H1} and v_{H2} can be negative when v_{an} is positive. Table 2-3 shows relationship between the output voltage of the inverter and the values of switching functions in a single-phase three-HB THMI. From (2.6), we can get

$$v_{an} = -v'_{an} \Leftrightarrow F_i = F'_i \quad i = 1 \dots h \quad (2.8)$$

The cases about the negative value of v_{an} can be deduced from Table 2-3 and (2.8), so they are not listed in Table 2-3.

Table 2-3. Relationship between the output voltage of the inverter and the values of switching functions in a single-phase three-HB THMI

v_{an}	$13E$	$12E$	$11E$	$10E$	$9E$	$8E$	$7E$
F_1	1	0	-1	1	0	-1	1
F_2	1	1	1	0	0	0	-1
F_2	1	1	1	1	1	1	1
v_{an}	$6E$	$5E$	$4E$	$3E$	$2E$	E	0
F_1	0	-1	1	0	-1	1	0
F_2	-1	-1	1	1	1	0	0
F_2	1	1	0	0	0	0	0

2.2 Proof for the greatest number of output voltage levels of the THMI

In [10], it is said that, among existing multilevel levels THMI has the greatest levels of output voltage using the same number of components. In the section, firstly, the theoretical prove for this conclusion is specified, then the comparison between various kinds of multilevel inverters is given.

2.2.1 Theoretical proof

This section proves that the THMI has greatest levels of output voltage using the same number of HBs among the multilevel inverters using HBs connected. A phase voltage waveform is obtained by summing the output voltages of h HBs as shown in (2.2). If the

Chapter 2. Investigation of THMI

dc link sources of all HB cells are equal, the multilevel inverter is called the cascade multilevel inverter and the maximum number of levels of phase voltage is given by

$$m = 1 + 2h \quad (2.9)$$

On the other hand, if at least one of the dc link sources is different from the other ones, the multilevel inverter is called the hybrid multilevel inverter [86-88]. In section 1.4, the BHMI, the quasi-linear multilevel inverter and the THMI are introduced. Thus, considering that the lowest dc link source E is chosen as base value for the p.u. notation, the normalized values of all dc link voltages must be natural numbers to obtain a uniform step multilevel inverter, i.e.:

$$V_{dci^*} \in \mathbb{N}, \quad i = 1, 2, \dots, h \quad (2.10)$$

Moreover, to obtain a uniform step multilevel inverter, the dc link voltage of the HB cells must also respect the following relation [87]:

$$V_{dci^*} \leq 1 + 2 \sum_{k=1}^{i-1} V_{dk^*}, \quad i = 2, 3, \dots, h \quad (2.11)$$

where it is also considered that the dc link voltages are arranged in an increasing way, that is:

$$V_{dc1^*} \leq V_{dc2^*} \leq V_{dc3^*} \leq \dots \leq V_{dch^*} \quad (2.12)$$

Therefore, the maximum number of levels of output phase voltage waveform can be given by [87]:

$$m = 1 + 2s_{\max} \quad (2.13)$$

where $s_{\max}$ is the maximum number of positive/negative voltage levels and can be expressed:

$$s_{\max} = \sum_{i=1}^h V_{dci^*} \quad (2.14)$$

From (2.9), (2.13) and (2.14), it can be verified that hybrid multilevel inverters can generate a large number of levels with the same number of cells. Moreover, in the THMI, the dc link voltages satisfy the following equation:

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$$V_{dci*} = 1 + 2 \sum_{k=1}^{i-1} V_{dck*}, \quad i = 2, 3, \dots, h \quad (2.15)$$

Therefore, the THMI has greatest levels of output voltages using the same number of HBs among multilevel inverters with HBs connected.

2.2.2 Comparison between various kinds of multilevel inverters

Two kinds of comparisons are presented in this section. In the first comparison, the components are considered to have same voltage rating, E . This comparison is for high power and high voltage applications, in which the devices connected in series, are used to satisfy the requirement of high voltage ratings. Table 2-4 shows the comparison between multilevel inverters: diode-clamped multilevel inverter (DCMI), capacitor-clamped multilevel inverter (CCMI), cascade multilevel inverter (CMI), generalized multilevel inverter (GMI), BHMI [14, 15], and THMI [10, 11]. The letter m is the number of steps of phase voltage. From Table 2-4, we can find that CMI, BHMI and THMI use fewer components. The CMI, BHMI and THMI use the same number of components. However, in practical systems, the redundancy requirement must be satisfied. THMI uses fewer components than BHMI and CMI in practical systems since THMI use less redundant components. Moreover, the THMI uses fewer dc sources than the CMI and the BHMI.

The second comparison is for medium and low power application, in which the voltage rating of main switching components, diodes and capacitors can be obtained easily. Therefore, the numbers of main switching components, diodes and capacitors are minimal required values. Table 2-5 shows the comparison results among DCMI, CCMI, CMI, GMI, BHMI and THMI. From Table 2-5, we can find that the THMI uses the fewest components among these multilevel inverters.

Table 2-4. The first comparison between multilevel inverters

Converter type	DCMI	CCMI	GMI	CMI	BHMI	THMI
Main switching devices	$2m-2$	$2m-2$	2^m-2	$2m-2$	$2m-2$	$2m-2$
Diodes	$m(m-1)$	$m-1$	2^m-2	$2m-2$	$2m-2$	$2m-2$
Capacitors	$m-1$	$0.5m(m-1)$	$m-1$	$(m-1)/2$	$(m-1)/2$	$(m-1)/2$
Total components	$(m-1)(m+1)$	$(m-1)(0.5m+3)$	$2^{m+1}+m-5$	$4.5(m-1)$	$4.5(m-1)$	$4.5(m-1)$

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Table 2-5. The second comparison between multilevel inverters

Converter type	DCMI	CCMI	CMI	GMI	BHMI	THMI
Main switching devices	$2m-2$	$2m-2$	$2m-2$	2^m-2	$4 \times \log_2[(m+1)/2]$	$4 \times \log_3 m$
Diodes	$4m-6$	$2m-2$	$2m-2$	2^m-2	$4 \times \log_2[(m+1)/2]$	$4 \times \log_3 m$
Capacitors	$m-1$	$2m-3$	$0.5m-0.5$	$m-1$	$\log_2[(m+1)/2]$	$\log_3 m$
Total components	$7m-9$	$6m-7$	$4.5m-4.5$	$2^{m+1}+m-5$	$9 \times \log_2[(m+1)/2]$	$9 \times \log_3 m$

2.3 Modulation strategies for THMI

Four modulation strategies for the THMI are investigated. They are the step modulation strategy, the virtual stage modulation strategy, the hybrid modulation strategy, the sub-harmonics pulse width modulation (PWM) strategy and the simple modulation strategy. Since multilevel inverters are used in three-phase systems typically, only modulation strategies for the three-phase systems will be investigated here. In the three-phase systems, triple-order harmonic components of voltages need not be eliminated by the modulation strategies since they can be eliminated by proper connection of three-phase voltage sources and loads. In other words, only 5th, 7th, 11th, 13th, 17th, 19th ... harmonic components should be eliminated by the modulation strategies. In addition, the amplitude of the fundamental component should be controlled. The list [1, 5, 7, 11, 13, 17, 19...] can be expressed by

$$h_i = \begin{cases} 3i-2 & \forall i = \text{odd} \\ 3i-1 & \forall i = \text{even} \end{cases} \quad i > 0 \quad (2.16)$$

The step modulation strategy, the virtual stage modulation strategy and the simple modulation strategy belong to low-frequency modulation strategies. The high-frequency modulation strategies used in the hybrid multilevel inverters include the hybrid modulation strategy and the sub-harmonic PWM strategy [89].

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2.3.1 Step modulation strategy

Fig. 2-3 shows a general quarter-wave symmetric stepped voltage waveform synthesized by a THMI where E indicates unit voltage of dc source. Consider that ς is the number of switching angles in quarter wave of v_{an} and σ is the number of positive/negative levels of v_{an} . In step modulation strategy,

$$V = S \quad (2.17)$$

By applying Fourier series analysis, the amplitude of any odd j th harmonic of v_{an} can be expressed as

$$|v_{an}|_j = \frac{4}{jp} \sum_{i=1}^{\varsigma} [E \cos(jq_i)] \quad (2.18)$$

where j is an odd harmonic order and θ_i is the i th switching angle. The amplitudes of all even harmonics are zero. According to Fig. 2-3, θ_1 to θ_{ς} must satisfy

$$0 < q_1 < q_2 < \dots < q_{\varsigma} < p/2 \quad (2.19)$$

The switching angles controlled by step modulation technique are derived from (2.20). Up to $(\varsigma-1)$ harmonic contents can be removed from the voltage waveform and the amplitude of fundamental component can be controlled.

$$\left\{ \begin{array}{l} \sum_{i=1}^{\varsigma} \cos(h_1 q_i) = S \cdot MR \\ \sum_{i=1}^{\varsigma} \cos(h_2 q_i) = 0 \\ \mathbf{M} \\ \sum_{i=1}^{\varsigma} \cos(h_{\varsigma} q_i) = 0 \end{array} \right. \quad (2.20)$$

where MR is the relative modulation index and is expressed as

$$MR = \frac{p |v_{an}|_1}{4S E} \quad (2.21)$$

where $|v_{an}|_1$ is the amplitude of fundamental component of the output voltage of the inverter.

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Fig. 2-3. Step modulation strategy of THMI

The equation sets (2.20) from which the switching angles can be derived are nonlinear and transcendental. For example, in a two-HB THMI, with the step modulation technique, the equations set are expressed as (2.22) when the relative modulation index is 0.83. The correct solution must satisfy the inequational condition as shown in (2.19).

$$\begin{aligned}
 \cos(q_1) + \cos(q_2) + \cos(q_3) + \cos(q_4) &= 0.83 \times 4 \\
 \cos(5q_1) + \cos(5q_2) + \cos(5q_3) + \cos(5q_4) &= 0 \\
 \cos(7q_1) + \cos(7q_2) + \cos(7q_3) + \cos(7q_4) &= 0 \\
 \cos(11q_1) + \cos(11q_2) + \cos(11q_3) + \cos(11q_4) &= 0
 \end{aligned} \tag{2.22}$$

The constrained optimization approach can be used to solve the nonlinear and transcendental equations sets. Each equation is regarded as an equational constraint. However, the computational problems of constrained optimization do not converge easily. Since in the actual electric system there are always mismatches and parameter tolerances, lower order harmonics will be small but not exactly zero. This gives a rise to an idea of transforming the constraint optimization model to a non-constraint one. The non-constraint optimization is expected to have better convergence property. The target function of the new scheme of optimization without equational constraints can be written as:

$$FT = p_1 \left[\sum_{i=1}^V \cos(h_1 q_i) - s \cdot M \right]^2 + p_2 \left[\sum_{i=1}^V \cos(h_2 q_i) \right]^2 + \mathbf{L} + p_v \left[\sum_{i=1}^V \cos(h_v q_i) \right]^2 \tag{2.23}$$

The $p_1 \sim p_\varsigma$ are penalty factors. The penalty factors were selected as

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$$p_i = \frac{4}{2i-1} \quad (2.24)$$

Fig. 2-4. Synthesized phase leg voltage waveform and frequency spectrum of a two-HB THMI with step modulation technique

Thus, the penalty factors put more weight on elimination of lower order harmonics. Function *fmincon* in the Matlab optimization toolbox was used to solve this minimization problem.

The two-HB THMI can synthesize nine-level output voltage. Fig. 2-4 and Fig. 2-5 show the typical synthesized waveform of the phase leg voltage, line-to-line voltage waveform and their frequency spectrums, as *MR* is equal to 0.83. The switching angles are 0.1478, 0.3232, 0.5738 and 0.9970. According to (2.20), the fifth, seventh and eleventh harmonics of phase leg voltage can be eliminated in the two-HB THMI as shown in Fig. 2-4. The THD of phase leg voltage is 9.66%. The triple-order harmonic components do not exist in the line-to-line voltage as shown in Fig. 2-5. The THD of line-to-line voltage is 5.91%.

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Fig. 2-5. Synthesized line-to-line voltage waveform and frequency spectrum of a two-HB THMI with step modulation technique

According to (2.20), all switching angles must satisfy the constraint (2.19). If switching angles do not satisfy the constraint, this scheme no longer exists. The theoretical maximum amplitude of fundamental component is $4\zeta E/p$, which occurs as $q_1 \sim q_h$ equal to zero. Because of the internal restriction of switching angles, the relative modulation index has upper and lower limitation. The limitation of the relative modulation index can be explained using Fig. 2-6 and Fig. 2-7. As shown in Fig. 2-6, as the relative modulation index is less than a certain value, denoted by MR (min), q_ζ approaches to $p/2$ and the limitation of minimum modulation index occurs. Similarly, when the relative modulation index is greater than MR (max), q_1 approaches to zero and the limitation of maximum modulation index occurs as shown in Fig. 2-7.

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Fig. 2-6. Limitation to the minimum MR in the step modulation

Fig. 2-7. Limitation to the maximum MR in the step modulation

For a THMI with h HBs, the maximum number of levels of the phase leg voltage is m , which equals to 3^h . The maximum number of the positive/negative phase leg voltage levels is $\sigma_{\max}$, which equals to $(m-1)/2$. As mentioned above, the relative modulation index MR has limitations. To extend the smaller ranges of modulation index, the inverter will output fewer voltage levels. Consequently, the number of positive/negative voltage levels that the inverter outputs, σ is smaller than the maximum number of the positive/negative levels, $\sigma_{\max}$. In the step modulation strategy, the number of switching angles in the quarter wave of v_{an} , ς equals to σ . The definition of relative modulation index MR is based on σ as shown in (2.21). This definition is easily included in (2.20) to express the nonlinear transcendental equation sets that are used to calculate the switching

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angles. In practice, the modulation index, M , is used. M is based on the $\sigma_{\max}$ and can be expressed as:

$$M = \frac{P |v_{an}|_1}{4s_{\max} E} \quad (2.25)$$

The relationship between MR and M can be expressed as

$$\frac{M}{MR} = \frac{s}{s_{\max}} \quad (2.26)$$

In the two-HB THMI, according to (2.20), the maximum MR is calculated as 0.86 and the minimum MR is 0.55 as the levels of output voltage are nine. The range of M is also from 0.55 to 0.86 with the nine-level output voltage. To extend lower modulation index, fewer output voltage levels are synthesized. The range of MR is 0.46~0.83 when the output voltage levels are seven. According to (2.26), the range of M is 0.34~0.62 when output voltage levels are seven. Thus, the modulation range is extended to 0.34 by decreasing levels of output voltage.

Table 2-6 shows the relative modulation index and the modulation index with different output voltage levels in the two-HB THMI. Firstly, the minimum and maximum MR is calculated by the optimization method. Secondly, the minimum and maximum M is calculated by (2.26). It is preferable to use more output voltage levels. The last column of Table 2-6 shows the arrangement of M with different output voltage levels. In addition, the maximum limitation of M can reach 0.94 without regard to the elimination of the 11th harmonic as shown in last row of Table 2-6.

Table 2-6. Range of modulation index under different output voltage levels with the step modulation in a two-HB THMI

σ	MR (min)	MR (max)	M (min)	M (max)	Range of M
1	0	1	0	0.25	0-0.15
2	0.3	0.9	0.15	0.45	0.15-0.34
3	0.46	0.83	0.34	0.63	0.34-0.55
4	0.55	0.86	0.55	0.86	0.55-0.86
4*	0.3	0.94	0.3	0.94	0.86-0.94

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Scheme of switching angles of the two-HB THMI is shown in Fig. 2-8. When the modulation index reaches the lower limitation, such as 0.34, the third switching angle is close to $\pi/2$, which verifies Fig. 2-6. When the modulation index reaches the maximum value 0.86 or 0.94, the first angle is close to zero, which is verified in Fig. 2-7.

Fig. 2-8. Scheme of switching angles with the step modulation as a function of modulation index in a two-HB THMI

2.3.2 Virtual stage modulation strategy

In the step modulation strategy, the output voltage levels of the multilevel inverter limit the amount of eliminated lower order harmonics. Only three lower order harmonics can be eliminated by the step modulation in a two-HB THMI. It is not very satisfied in the applications that required a high-quality sinusoid voltage output. The virtual stage modulation strategy is a new modulation strategy that increases the amount of eliminated lower order harmonics without increasing the number of output voltage levels. The switching angles can be derived as:

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$$\left\{ \begin{array}{l} \sum_{i=1}^a \cos(h_1 q_{pi}) - \sum_{i=1}^b \cos(h_1 q_{ni}) = s \cdot MR \\ \sum_{i=1}^a \cos(h_2 q_{pi}) - \sum_{i=1}^b \cos(h_2 q_{ni}) = 0 \\ \mathbf{M} \\ \sum_{i=1}^a \cos(h_v q_{pi}) - \sum_{i=1}^b \cos(h_v q_{ni}) = 0 \end{array} \right. \quad (2.27)$$

where σ is the number of positive/negative levels of v_{an} and can be expressed as

$$s = a - b \quad (2.28)$$

ς is the number of switching angles in quarter waveform of v_{an} and can be expressed as

$$V = a + b \quad (2.29)$$

MR is shown in (2.21). The equation (2.27) is subject to

$$\left\{ \begin{array}{l} 0 < q_{p1} < q_{p2} < \dots < q_{pa} < p/2 \\ 0 < q_{n1} < q_{n2} < \dots < q_{nb} < p/2 \\ q_{nj} < q_{p(j+s)} \quad j = 1, 2, \dots, b \end{array} \right. \quad (2.30)$$

In the two-HB THMI, when the output voltage changes between E and $2E$ or $-E$ and $-2E$, the switching components of the higher voltage HB will switch on/off as shown in Fig. 2-2. To keep high-voltage switching components switch at lower frequency in the THMI, the limitation (2.31) is added into (2.27) to assure that higher voltage switching components switch at the fundamental frequency.

$$q_{p2} < q_{n1} \quad (2.31)$$

Fig. 2-9 illustrates the waveform using the virtual stage modulation for the two-HB THMI whose output voltage levels are nine. The number of virtual stages, β , is two.

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Fig. 2-9. Waveform using the virtual stage modulation
Two-HB, nine-level, $a=6$, $b=2$

Fig. 2-10 and Fig. 2-11 show the typical synthesized waveform of phase leg voltage, line-to-line voltage waveform and their frequency spectrum in the virtual stage modulation strategy. The MR is 0.83 and the number of virtual stages is two. q_{p1} to q_{p6} is 0.1321, 0.3320, 0.5307, 0.6226, 0.9133 and 1.0419. q_{n1} is 0.5750 and q_{n2} is 0.9652. Because of two additional virtual stages, four more degrees of freedom of switching angles are created such that 13th, 17th, 19th and 23rd harmonics can be eliminated from the phase leg voltage as shown in Fig. 2-10. The THD of phase leg voltage is 10.67%. The triple-order harmonic components of line-to-line voltage do not exist and the harmonics are pushed to 1250Hz as shown in Fig. 2-11. The THD of the line-to-line voltage is 7.3%.

In virtual stage modulation strategy, the relative modulation index also has upper and lower limitation. Compared with the step modulation strategy, the optimal computation of the virtual stage modulation strategy endures more unequal restriction as shown in (2.30) and (2.31). When the switching angles do not satisfy these restrictions, the themes of switching angles no longer exist.

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Fig. 2-10. Synthesized phase leg voltage waveform and frequency spectrum of a two-HB THMI with the virtual stage modulation

Fig. 2-11. Synthesized line-to-line voltage waveform and frequency spectrum of a two-HB THMI with the virtual stage modulation

The concept of the relative modulation index can be used in the step modulation strategy by the similar method. Table 2-7 shows two cases. One is the nine-level output voltage with two virtual stages and the other is the seven-level output voltage with one virtual stage. With the nine-level output voltage and two virtual stages, the 5th, 7th, 11th, 13th, 17th, 19th and 23rd harmonics can be eliminated. With the seven-level output

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voltage and one virtual stage, the 5th, 7th, 11th and 13th can be eliminated. When output voltage levels are five or three, the virtual stage modulation strategy is not applicable in the two-HB THMI since the restriction (2.31) must be violated. Therefore, when M is less than 0.38 in this case, the step modulation strategy will be used. With the virtual stage modulation strategy, the scheme of switching angles is shown in Fig. 2-12.

Table 2-7 Range of modulation index with the virtual stage modulation in a two-HB THMI

σ	β	MR (min)	MR (max)	M (min)	M (max)	Range of M
3	1	0.51	0.92	0.38	0.69	0.38-0.459
4	2	0.459	0.92	0.459	0.92	0.459-0.92

Fig. 2-12. Scheme of switching angles for the virtual stage modulation as a function of modulation index in a two-HB THMI

p1 to p6 mean q_{p1} to q_{p6} , n1 to n2 mean q_{n1} to q_{n2}

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2.3.3 Hybrid modulation strategy

The hybrid modulation strategy for the hybrid multilevel inverters has been presented in [14], which incorporates stepped voltage waveform synthesis in higher power HB cells in conjunction with high frequency variable PWM in the lowest power HB cell. Fig. 2-13 presents a block diagram of the command circuit utilized to determine the command signals of the power devices of all HB. As shown in Fig. 2-13, the reference signal of the hybrid multilevel inverter, v_{ref} is the command signal of the HB with the highest dc voltage source ($V_{dc,h}$). This signal is compared with a voltage level corresponding to the sum of all smaller dc voltage sources of the hybrid multilevel inverter, $\sigma_{\max,h-1}$. If the command signal is greater than this level, the output of the inverter with the highest dc voltage source must be equal to $V_{dc,h}$. In addition, if the command signal is less than the negative value of $\sigma_{\max,h-1}$, the output of this cell must be equal to $-V_{dc,h}$, else the output of this cell must be zero. The command signal of i th HB cell is the difference between the command signal of the HB_{i+1} and the output voltage of the HB_{i+1} . In this way, the command signal of the i th cell contains information about the harmonic content of the output voltage of all higher voltage cells. This command signal is compared with a voltage level corresponding to the sum of all voltage sources until the HB_{i-1} ($\sigma_{\max,i-1}$). In the same way that presented for the HB_h , the output voltage of this cell is synthesized from the comparison of these two signals. Finally, the command signal of HB_1 (lowest power inverter) is compared with a high frequency triangle carrier signal, resulting in a high frequency output voltage. Therefore, the output voltage harmonics will be concentrated around the frequencies multiples of the switching frequency of the inverter with the lowest dc voltage source. Consequently, the spectral response of the output voltage depends on the switching frequency of the lowest power inverter, while the power processing depends on the inverter with the highest dc voltage source.

However, with the hybrid modulation strategy, a voltage waveform must be synthesized to modulate at high frequency among all adjacent voltage steps. Only the lower voltage HB can switch at high frequency, so the dc voltages must satisfy the following equation:

$$V_{dci*} \leq 2 \sum_{k=1}^{i-1} V_{dck*}, \quad j = 2, 3, \mathbf{K}, h \quad (2.32)$$

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where symbol * mean the normalized value. Therefore, the hybrid modulation strategy can be applied in binary hybrid multilevel inverters and quasi-linear multilevel inverters. The relationship of dc voltages of the THMI is shown in (2.15), so the THMI can not use the hybrid modulation strategy.

Fig. 2-13. Hybrid modulation for hybrid multilevel inverters

2.3.4 Sub-harmonic PWM strategies

Sub-harmonic PWM strategies for multilevel inverters employ extensions of carrier-based techniques used for conventional inverters. It has been reported that the spectral performance of a five-level waveform can be significantly improved by employing alternative dispositions and phase shifts in the carrier signals [32, 90, 91]. This concept can be extended to a nine-level case with the available options for polarity and phase variation. A representative sub-harmonic PWM waveform with the nine-level phase leg voltage is shown in Fig. 2-14.

If a two-HB THMI is used to synthesize the nine-level phase leg voltage as shown in Fig. 2-14 (b), the higher voltage HBs will switch at high frequencies, since the output voltage varies between E and $2E$ or $-E$ and $-2E$ continually in certain interval. In THMI, it is not appropriate that the higher voltage HBs switch at high frequency. Therefore, the sub-harmonic PWM is not applicable in THMI.

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Fig. 2-14. Representative waveforms for sub-harmonic PWM waveform with carrier polarity variation

2.3.5 Simple modulation strategy

The simple modulation strategy is the simplest modulation strategy with which the switching pattern is determined by comparing a reference signal with stages and then choosing the stages most close to the reference signal. Fig. 2-15 shows the illustration of the simple modulation strategy with the nine-level output voltage.

The advantage of this strategy is simple control algorithm, high flexibility and dynamic response. The disadvantage is that the amplitudes of lower order harmonic components are relatively higher. The THMI can generate the greatest voltage levels among all multilevel inverters using the same number of components. If the number of voltage levels is high enough, the lower-order harmonic components of output voltages will be very small with the simple modulation strategy. For example, in the case of a four-HB THMI that can generate 81-level voltage, with the simple modulation strategy, the amplitude of each lower-order harmonic components of the output voltage is less than 0.9% of the amplitude of the fundamental component and THD of output voltage is less than 2%.

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Fig. 2-15. Illustration of the simple modulation strategy

2.3.6 Summary of modulation strategies for THMI

Several modulation strategies have been investigated. With the hybrid modulation strategy and modulation strategies working with high switching frequencies, such as sub-harmonic PWM strategy, a voltage waveform must be synthesized to modulate at high frequency among all adjacent voltage steps. However, in THMI, it cannot be achieved when only the lowest voltage HB switch at high frequency, which can be derived from (2.15) and (2.32). In other words, if a voltage can be synthesized to modulate at high frequency in THMI, the higher voltage HBs must switch at high frequency. One of most important advantage of THMI is that higher voltage HBs can switch at lower frequency. Therefore, higher-frequency switching of higher voltage HBs not only is unacceptable in high power application but also violate the main advantage of THMI. Therefore, the hybrid modulation strategy and other modulation strategies working with high switching frequencies are not applicable in THMI. The low-frequency modulation strategies such as step modulation strategy and virtual stage modulation strategy are suitable in THMI. In

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the virtual stage modulation, additional constraint, such as (2.31) for two-HB THMI, must be added to ensure the higher HB switch at lower frequency. Additionally, the simple modulation strategy can be used in the THMIs that can generate many voltage levels. At the same time, for the THMIs that can generate many voltage levels, the space vector modulation [4] can achieve a very good linearity between the modulation index and the fundamental component of load voltage and eliminate common-mode voltages.

2.4 Regenerative power

The dc sources of the THMI can be batteries or bridge rectifies. Batteries cannot endure large reverse current for a long time, which will damage batteries. Diode bridge rectifies cannot permit reverse power. Controlled bridge rectifies can transmit energy to supplies. However, compared to simple diode bridge rectifies, the controlled bridge rectifies are much more complex and costly because of complex control circuits and higher price of controlled semiconductors.

2.4.1 Analysis of dc bus power injection

The switching function is involved in the analysis of dc bus power injection. The switching function, F , is shown in Table 2-1. The relationship between output voltage of a HB, v_H , and dc link voltage of the HB, V_{dc} , can be written as (2.33). The relationship between i_{dc} (current flowing through the dc bus) and i_{an} (output current of the THMI) can be also derived as (2.34).

$$v_H = F \cdot V_{dc} \quad (2.33)$$

$$i_{dc} = F \cdot i_{an} \quad (2.34)$$

Only fundamental component of output current of the THMI is considered since high frequency harmonic components do not generate average power [92]. So i_{an} can be expressed as

$$i_{an} = I_{an} \cdot \sin(\omega t + j) \quad (2.35)$$

where I_{an} is the amplitude of i_{an} and j is the angle of power factor.

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General waveforms of v_H and i_{an} are shown in Fig. 2-16. The average dc power that supplies the HB over a period can be calculated as (2.36)

$$P_{dc} = \frac{1}{T} \int_0^T V_{dc} \cdot i_{dc} dt \quad (2.36)$$

where T is the period of i_{an} . From (2.34) and (2.36), we can get

$$P_{dc} = \frac{1}{T} \int_0^T V_{dc} \cdot F \cdot i_{an} dt = \frac{1}{T} \int_0^T v_H \cdot i_{an} dt \quad (2.37)$$

Fig. 2-16. General waveform of dc bus voltage and THMI output current

The relationship between switching angles in Fig. 2-16 can be expressed as (2.38).

$$q_i = \begin{cases} p + q_{i-2V} & i = (2V+1)L \ 4V \\ p - q_{2V+1-i} & i = (V+1)L \ 2V \end{cases} \quad (2.38)$$

Derived from (2.38), v_H has following characteristic

$$v_H(p - wt) = v_H(wt) \quad (2.39)$$

$$v_H(wt + p) = -v_H(wt) \quad (2.40)$$

From (2.35), we can get

$$i_{an}(wt + p) = -i_{an}(wt) \quad (2.41)$$

Derived from (2.40) and (2.41), the average dc power can be calculated over half period as:

$$P_{dc} = \frac{2}{T} \int_0^{\frac{T}{2}} v_H \cdot i_{an} dt \quad (2.42)$$

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Suppose P_i mean the power is generated by the voltage pulse from q_i/w to q_{i+1}/w and corresponding voltage pulse from $q_{2\zeta-i}/w$ to $q_{2\zeta+1-i}/w$. P_i can be expressed as:

$$P_i = \frac{(-1)^n w}{p} \left(\int_{q_i/w}^{q_{i+1}/w} V_{dc} \cdot I_{an} \cdot \sin(\omega t + j) dt + \int_{q_{2\zeta-i}/w}^{q_{2\zeta+1-i}/w} V_{dc} \cdot I_{an} \cdot \sin(\omega t + j) dt \right) \quad (2.43)$$

where $i = 2n - 1$ and n is natural number. Derived from (2.38) and (2.43), P_i is expressed as

$$P_i = \frac{(-1)^n}{p} V_{dc} \cdot I_{an} \cdot 2 \cdot \cos(j) \cdot (\cos(q_i) - \cos(q_{i+1})) \quad (2.44)$$

Thus, the average dc power of the HB can be expressed as:

$$P_{dc} = \frac{2}{p} V_{dc} \cdot I_{an} \cdot \cos(j) \cdot \sum (\cos(q_{4n-3}) - \cos(q_{4n-2}) - \cos(q_{4n-1}) + \cos(q_{4n})) \quad (2.45)$$

In (2.45), if q_j is greater than $p/2$, q_j will be set as $p/2$.

In general, power factor angle j is from $-p/2$ to $p/2$, so $\cos(\varphi)$ is greater than zero. V_{dc} and I_{an} are positive. Thus, we can conclude from (2.45) that the power of dc bus is negative if:

$$\sum (\cos(q_{4n+1}) - \cos(q_{4n+2}) - \cos(q_{4n+3}) + \cos(q_{4n+4})) < 0 \quad (2.46)$$

Negative power of dc bus means regenerative power.

2.4.2 Regenerative power in THMI

Regenerative power may occur in lower-voltage HBs of THMI. Take the example of a two-HB THMI. If the step modulation strategy is applied, the restrictions that are added to (2.20) to ensure power of dc buses is always positive are shown in Table 2-8. With these restrictions, ranges of relative modulation index are calculated as shown in Table 2-9. The range of relative modulation index decreases much when σ is two or three compared with Table 2-6. The range of modulation index is not continuous as shown in the last column of Table 2-9. The regenerative power will occur in the lower voltage HB when M is from 0.51 to 0.55 or from 0.33 to 0.44.

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Table 2-8 Additional restriction to avoid regenerative power of dc buses in the step modulation

σ	Restriction
1	$\cos(\theta_1) > 0$
2	$\cos(\theta_1) - 2\cos(\theta_2) > 0$
3	$\cos(\theta_1) - 2\cos(\theta_2) + \cos(\theta_3) > 0$
4	$\cos(\theta_1) - 2\cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) > 0$

Table 2-9 Range of modulation index with the step modulation in a two-HB THMI (avoid regenerative power of dc buses)

σ	MR (min)	MR (max)	M (min)	M (max)	Range of MA
1	0	1	0	0.25	0-0.15
2	0.3	0.66	0.15	0.33	0.15-0.33
3	0.59	0.68	0.44	0.51	0.44-0.51
4	0.55	0.86	0.55	0.86	0.55-0.86
4*	0.56	0.94	0.56	0.94	0.86-0.94

The virtual stage modulation strategy is used in a two-HB THMI. In Table 2-7, two cases are analyzed. One is four-level positive/negative output voltage with two virtual stages and the other is five-level positive/negative output voltage with one virtual stage. Only dc bus of the lower voltage HB is possible to have regenerative power. For the first case, the restriction that ensures positive power can be written as:

$$\cos(q_{p1}) - 2\cos(q_{p2}) + \cos(q_{p3}) + \cos(q_{p4}) + \cos(q_{p5}) + \cos(q_{p6}) - \cos(q_{n1}) - \cos(q_{n2}) > 0 \quad (2.47)$$

To the second case, the restriction can be expressed as:

$$\cos(q_{p1}) - 2\cos(q_{p2}) + \cos(q_{p3}) + \cos(q_{p4}) + \cos(q_{p5}) - \cos(q_{n1}) > 0 \quad (2.48)$$

With these restrictions, the range of relative modulation index decreases as shown in Table 2-10. The regenerative power will occur in the lower voltage HB when M is from 0.53 to 0.62.

Table 2-10 Range of modulation index range with the virtual stage modulation strategy in a two-HB THMI (avoid regenerative power of dc bus)

σ	β	MR (min)	MR (max)	M (min)	M (max)	Range of M
3	1	0.62	0.71	0.46	0.53	0.46-0.53
4	2	0.62	0.92	0.62	0.92	0.62-0.92

2.4.3 Method to avoid regenerative power

As discussed in last section, the power of lower voltage HBs is likely to be regenerative. In this section, the solutions will be introduced. In [13], a method is proposed that the dc links of lower voltage HBs are supplied by the low-power and isolated power sources fed from a common power supply from the highest voltage HB. These power sources are bidirectional and a bidirectional dc-dc power supply is used for this purpose [93]. It is also possible to use independent output transformers with a common dc supply, as show in Fig. 2-17. A variation of this configuration was used by ABB in his 16 2/3 Hz substation for railroads in Bremen. In the system described here, the transforms are smaller for lower voltage HBs because the voltages are scaled in power of three. Besides, the switching frequency of transformers connected with lower voltage HBs are lower. Then the transforms connected with lower voltage HBs become smaller for two reasons: voltage and switching frequency.

Fig. 2-17. THMI with output transformers

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The above two methods to solve the problem of the regenerative power use additional equipments, such as bi-directional dc-dc converter or output transformers, which increase the cost of the inverter system and power losses. A new method is presented to avoid regenerative power. This method does not use additional devices. The regenerative power is eliminated by avoiding outputting several null voltage levels, which is explained by an example of a four-HB THMI below.

The average power of the dc bus of a HB can be expressed by (2.45). In general, power factor angle j is from $-p/2$ to $p/2$, so that $\cos(\varphi)$ is greater than zero. V_{dc} and I_{an} are positive. Therefore, from (2.45) and Fig. 2-16, we can conclude that the reason of the regenerative power is the negative segments of v_H when the fundamental component of v_{an} is positive or the positive segments of v_H when the fundamental component of v_{an} is negative. The segments of v_H resulting in the regenerative power of the HB are called regenerative segments. The basic idea of eliminating regenerative power is to avoid output several levels of v_{an} which will cause regenerative segments in HBs. Table 2-11 shows the voltage levels of v_{an} which cause regenerative segments of HBs in the case of a four-HB THMI. The voltage levels of v_{an} which are not selected to output are called null voltage levels. Table 2-11 also shows the priority of null voltage levels. For example, if the regenerative power occurs in the dc link of the HB₁, the voltage level (14) and (-14) are selected as null voltage levels firstly. If the regenerative power still occurs, the voltage levels (17) and (-17) are also selected as null voltage levels. With the priority shown in the Table 2-11, the null voltage levels distribute as evenly as possible, which results in better power quality.

Table 2-11 Voltage levels of v_{an} which cause regenerative segments of HBs

HB ₁	$\pm 14, \pm 17, \pm 32, \pm 23, \pm 5, \pm 20, \pm 38, \pm 29, \pm 26, \pm 11, \pm 2, \pm 8, \pm 35$
HB ₂	$\pm 14, \pm 32, \pm 23, \pm 5, \pm 15, \pm 34, \pm 25, \pm 7, \pm 16, \pm 6, \pm 24, \pm 33$
HB ₃	$\pm 14, \pm 17, \pm 15, \pm 20, \pm 19, \pm 16, \pm 21, \pm 18, \pm 22$

Fig. 2-18 shows the flow chart of the algorithm that stabilizes the dc link voltage of a HB. V_{dc} is the dc link voltage of a HB. $V_{dc,normal}$ is the normal dc link voltage. $V_{dc,last}$ is the dc link voltage in the previous sampling. N_{null} is the number of null voltage levels. In the switch table, the voltage levels are set as null or not based on N_{null} and Table 2-11.

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Fig. 2-18. Flow chart of the algorithm to stabilize dc link voltages

With lower modulation index, the power quality that the THMI outputs is a little bit poorer with the proposed control scheme because more null voltage levels do not devote themselves to the output voltage of the THMI. In the case of the four-HB THMI, with up to 81-level output voltage of the THMI, the simple modulation strategy as shown in section 2.3.5 is suitable for the THMI. If the simple modulation strategy is used and the new method is applied to eliminate the effect of regenerative power, the relationship between the modulation index and the THD is shown in Fig. 1-3.

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Fig. 2-19. Relationship between the modulation index and THD

2.4.4 Summary of regenerative power in THMI

The topology of THMI has distinct advantage of least components used compared with other topologies of multilevel inverters, but the THMI also has notable disadvantage that power of the lower voltage HBs is possible to be regenerative with lower modulation index. If the THMI feeds a RL or RC load and simple diode bridge rectifies are used as dc sources, the regenerative power will cause the increase of the dc capacitor voltages, which will damage devices.

Therefore, basically, the THMI is suitable for two applications. The first one is the application of reactive power compensation. The average power of dc link of a HB is zero when power factor is zero as shown in (2.45), so the problem of regenerative power is avoided. The second one is the application in which the inverter always runs with higher modulation index. From Table 2-9, we can find that the two-HB THMI runs with step modulation without problem of regenerative power when M is from 0.55 to 0.94. From Table 2-10, we can find that the two-HB THMI runs with virtual stage modulation without problem of regenerative power when M is from 0.62 to 0.92.

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However, the inverter is required to work at any modulation index for active load in most cases. Two methods have been presented to solve regenerative power problem. The first one uses bidirectional dc/dc converters and the second one uses additional output transformers. A new method to solve the regenerative power is presented as a cost-effective solution, because it does not use additional equipments. The dc capacitor voltages of lower voltage HBs are kept stable by the new method. The tradeoff is that power quality will decrease with lower modulation index.

2.5 Experimental results

2.5.1 Experiment to verify the step modulation and virtual stage modulation

The performance of step modulation strategy and virtual stage modulation strategy has been verified by the experimental of a single two-HB THMI. In the control circuit, a TMS320F240 DSP is used as the main processor, which provides the gate logic signals. In a HB, four MOSFETs, IRF540, are used as the main switches, which are connected in a full-bridge configuration. The load is a 23.2Ω resistor. The total ratio of voltage measure is 1:2. The frequency spectrums are analyzed by the FFT (Fast Fourier Transform) function of oscilloscope. The scale of Y-axis of frequency spectrum is 5dbV/div and reference level is 5dbV.

The switching pattern of step modulation technique is programmed and is loaded to the DSP. In step modulation strategy, when output voltage levels are nine and M is 0.83, the switching angles are 0.14778, 0.32325, 0.57376 and 0.99696. The output voltage of the THMI is shown in Fig. 2-20. The frequency is 50Hz and the step voltage is about 5V. The frequency spectrum is shown in Fig. 2-21. The 5th, 7th and 11th harmonics are less than 0.028V ($-37\text{db}\times 2\text{V}$), which means they are nearly eliminated. It verifies the simulation result as shown in Fig. 2-4.

When output voltage levels are seven and M is 0.49, the switching angles are 0.44717, 0.9097 and 1.1215. The output voltage of the THMI is shown in Fig. 2-22 and the

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frequency spectrum is shown in Fig. 2-23. The 5th and 7th harmonics are less than 0.02V ($-40\text{db} \times 2\text{V}$), which means they are nearly eliminated.

When output voltage levels are five and M is 0.32, the switching angles are 0.51847 and 1.1468. The output voltage of the THMI is shown in Fig. 2-24 and the frequency spectrum is shown in Fig. 2-25. The fifth harmonics are less than 0.02V ($-40\text{db} \times 2\text{V}$), which means they are nearly eliminated.

Fig. 2-20. Output voltage of the THMI with the step modulation $M = 0.83$ (10V/div)

Fig. 2-21. Frequency spectrum with the step modulation $M = 0.83$

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Fig. 2-22. Output voltage of the THMI with the step modulation $M = 0.49$ (10V/div)

Fig. 2-23. Frequency spectrum with the step modulation $M = 0.49$

Fig. 2-24. Output voltage of the THMI with the step modulation $M = 0.32$ (10V/div)

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Fig. 2-25. Frequency spectrum with the step modulation $M = 0.32$

The switching pattern of modified virtual stage modulation technique is programmed and is loaded to the DSP. In virtual stage modulation, when output voltage levels are nine and M is 0.83, the switching angles are 0.13177, 0.33186, 0.52855, 0.6202, 0.91294, 1.0423, 0.57124 and 0.96573. The output voltage of the THMI is shown in Fig. 2-26 and the frequency spectrum is shown in Fig. 2-27. The 5th, 7th, 11th, 13th, 17th, 19th and 23rd harmonics are less than 0.035V ($-35\text{db} \times 2\text{V}$), which means they are nearly eliminated. It verifies the simulation result as shown in Fig. 2-10.

When output voltage levels are seven and M is 0.49, the switching angles are 0.40549, 0.88038, 1.1497, 1.5318 and 1.5082. The output voltage of the THMI is shown in Fig. 2-28 and the frequency spectrum is shown in Fig. 2-29. The 5th, 7th, 11th and 13th harmonics are less than 0.02V ($-40\text{db} \times 2\text{V}$), which means they are nearly eliminated

Fig. 2-26. Output voltage of the THMI with the virtual stage modulation $M = 0.83$ (10V/div)

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Fig. 2-27. Frequency spectrum with the virtual stage modulation $M = 0.83$

Fig. 2-28. Output voltage of the THMI with the virtual stage modulation $M = 0.49$ (10V/div)

Fig. 2-29. Frequency spectrum with the virtual stage modulation $M = 0.49$

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2.5.2 Experiment to verify the new method to eliminate the regenerative power

The performance of the methods to eliminate the effect of regenerative power by avoiding output the null voltage levels is verified by the experiment of a 4-HB THMI, in which diode bridge rectifies are used as the dc sources of HBs. The step voltage is 5.9V. The frequency of output voltage is set at 50 Hz and the sampling frequency is set at 10 kHz. The output voltage levels of the inverter has up to 81 levels, so the simple modulation strategy as show in section 2.3.5. The control algorithm to stabilize the dc link voltages is shown in Fig. 2-18. A TMS320F240 DSP EVM board is used to control the inverter. The configuration of experimental system is shown in Fig. 2-30.

Fig. 2-30. General representation of experimental test system

Fig. 2-31 shows the waveform of output voltage of the 4-HB THMI with simple modulation strategy when modulation index is 0.79. The power quality is good.

Fig. 2-32 shows the output voltage waveform with some null voltage levels when modulation index is 0.7. From the enlarged figure, we can observe that some voltage levels are not generated. Moreover, the step voltages are kept nearly same, which means that the voltages of dc capacitors are kept stable. Fig. 2-33 shows the worst case when the

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modulation index is 0.53. In this case, null voltage levels include ± 5 , ± 14 , ± 15 , ± 16 , ± 17 , ± 19 , ± 20 , ± 21 , ± 23 , ± 32 and ± 34 .

Fig. 2-31. Waveform of output voltage of the inverter with the simple modulation strategy $M = 0.79$ (100V/div)

Fundamental frequency = 50 Hz, THD = 1.94%

Fig. 2-32. Waveform of output voltage of the inverter $M = 0.7$ (100V/div)

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Fig. 2-33. Waveform of output voltage of the inverter $M = 0.42$ (100V/div)

2.6 Summary

This chapter investigates various aspects of the THMI. The most important advantage of the THMI is that the THMI can synthesize the greatest number of output voltage levels using the same components compared with other topologies of multilevel inverters. The more output voltage levels the multilevel inverters have, the more similar sinusoid waveform can be synthesized. Thereby, lower order harmonics and total harmonics distortion can be reduced greatly.

Various modulation strategies for THMI are investigated. The modulation strategies working with high switching frequencies, such as hybrid modulation strategy and sub-harmonic PWM strategy, are not suitable for the THMI. Low-frequency modulation strategies such as step modulation strategy and virtual stage modulation strategy are applicable in THMI. The virtual stage modulation strategy can eliminate more lower-order harmonic components than step modulation strategy, but additional constraints must be added into the virtual modulation strategy to ensure the higher voltage HBs switch at lower frequency. The simple modulation strategy can be used in the THMI that includes many HBs.

THMI also has a disadvantage. Power of the lower voltage HBs is possible to be regenerative with lower modulation index. If the THMI feeds a RL or RC load and simple diode bridge rectifies are used as dc sources, the regenerative power will cause the increase of the dc capacitor voltages, which will damage devices. Two methods have been presented to solve regenerative power problem: using bidirectional dc/dc converters or using additional output transformers. The third method presented can stabilize the dc

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capacitor voltages by avoiding outputting so-called several null voltage levels. The first two methods are expensive since they need additional bidirectional dc-dc converter or output transformers. The third method is cost-effective, but the tradeoff is that power quality will decrease a little with lower modulation index.

Thus, the THMI is suitable for the applications in which no HB generates regenerative power. The first one is the application of reactive power compensation in which the problem of regenerative power is avoided. The second one is the application in which the inverter always runs with higher modulation index.

In next chapter, the application of the THMI in reactive power compensation will be investigated. In this application, the problem of regenerative power is avoided. The step modulation strategy is used in this application.

Chapter 3 THMI Used in STATCOM with Unbalanced Voltages

3.1 Introduction

Based on the investigation of the last chapter, the THMI is very suitable for the application of reactive power compensation. Synchronous Static Compensation (STATCOM) is a flexible ac transmission system (FACTS) device, which is connected as a shunt to the network, for generating or absorbing reactive power. STATCOM can be utilized to regulate voltage, control power factor and stabilize power flow [94]. Many inherent benefits of multilevel inverter have led to their increased interest in STATCOM. In [46, 48], cascade multilevel inverters have been used in STATCOM. Furthermore, the application of binary hybrid multilevel inverters in STATCOM has also been investigated because the binary hybrid multilevel inverter can generate more voltage levels than the cascade multilevel inverter with the same number of switches [35, 50, 51]. However, the application of the THMI in STATCOM is still not studied.

This chapter investigates the application of THMI in STATCOM. In this topology, not only fewer switches are required, but also the cost of cooling systems and dc capacitors is decreased. Moreover, the problem of regenerative power in the THMI mentioned in [76] and the previous chapter is avoided because the STATCOM mainly generates or absorbs reactive power.

Voltage imbalance is a problem that STATCOM must deal with in the distribution system. Steady-state voltage imbalance can arise from unequal loading on each phase or from unbalanced faults on the power system, which cause single-phase voltage sags. These sags are detrimental since they cause heating in motors and affect sensitive single-phase loads. The proposed STATCOM can balance bus voltages under unbalanced conditions.

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The step modulation strategy is widely used in STATCOM [34, 49] since GTOs with lower switching frequency are employed as switches in such applications of high power and high voltage [95-97]. The vector control based on synchronous frame transform has been used successfully in STATCOM to regulate reactive power [47, 48] and reduce negative sequence component of the bus voltage [98]. Here the vector control and the step modulation strategy are combined to reach the control aims. The challenge here is that the conventional method based on the comparison of switching angles and phase angles [34, 48, 49] to generate the switching signals can not work well in such control system. A new method based on the comparison of reference amplitudes and reference signals is proposed. Furthermore, dead-zone control is used to improve performance of the inverter. The performance of the proposed control system is confirmed by simulation and experiment.

3.2 System configuration

3.2.1 Configuration of STATCOM system

Fig. 3-1 shows one line diagram of a distribution system with STATCOM and Fig. 3-2 shows a simplified model of Fig. 3-1.

Fig. 3-1. Distribution system with the STATCOM

The STATCOM that is based on a three-phase 9-level THMI is connected to the bus B through the interface impedance Z_I . Z_S is the equivalent impedance of the source and Z_L

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is the equivalent impedance of the load. In steady states and balanced conditions, voltages and currents can be expressed as phasors. In Fig. 3-2, V_S is the source voltage, V_B is the bus voltage, V_G is the generated voltage of the STATCOM, I_G is the current generated by the STATCOM, I_S is the source current and I_L is the load current.

Fig. 3-2. Simplified model of the distribution system with the STATCOM

Parameters of the compensator and the distribution system are shown in Table 3-1. The STATCOM in steady states will generate a leading reactive current when the amplitude of V_G is larger than that of V_B , and vice versa, it will draw a lagging current from the source.

Table 3-1 Parameters of the compensator and the distribution system for simulations and experiments

	Simulations	Experiments
Operating frequency	50 Hz	50 Hz
Rating of source voltage (line-to-line rms value)	13.5 kV	196 V
Rating of reactive power	10 MVar	2000 VAr
Rating of STATCOM current (phase rms value)	428 A	6 A
Interface impedance per phase	$\omega L_I = 3.64 \Omega$; $R_I = 0.3 \Omega$	$\omega L_I = 3.64 \Omega$; $R_I = 0.3 \Omega$
Source impedance per phase	$\omega L_S = 2.2 \Omega$; $R_S = 0.3 \Omega$	$\omega L_S = 2.2 \Omega$; $R_S = 0.3 \Omega$
Unit voltage of dc capacitors, E	3.3 kV	48 V
dc capacitor in the HB with dc voltage U_D	2933 μF	3300 μF
dc capacitor in the HB with dc voltage $3U_D$	1114 μF	1100 μF

3.2.2 Three-phase nine-level THMI

Fig. 3-3 shows a three-phase Y-configured nine-level THMI used in the STATCOM. The inverter has separate dc capacitors for each HB unit of each phase. To get maximum output voltage levels of the inverter, the ratio of dc capacitor voltages is arranged as 1:3, so the inverter can output nine voltage levels each phase. $v_{H,ak}$ and $v_{C,ak}$ represent the output voltage and the dc capacitor voltage of the HB_{ak} , respectively. A switching function, F_{ak} , is used to relate $v_{H,ak}$ and $v_{C,ak}$ as

$$v_{H,ak} = F_{ak} \cdot v_{C,ak} \quad (k = I, II) \quad (3.1)$$

Fig. 3-3. Three-phase nine-level THMI

The switching function is shown in Table 2-1. The A-phase voltage of the inverter, $v_{G,a}$, is represented as:

$$v_{G,a} = \sum_{k=I}^{II} (F_{ak} \cdot v_{C,ak}) \quad (3.2)$$

The unit voltage of dc capacitors is E , i.e., $v_{C,aI}$ and $v_{C,aII}$ are E and $3E$, respectively. So $v_{G,a}$ has 9 levels totally. The relationship between the output voltage of the phase leg and the values of switching functions is shown in Table 2-2.

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In this distribution system, the proposed STATCOM works under high voltage, so GTOs are selected as switching components that cannot switch at high frequency. To ensure that GTOs switch at low frequency and eliminate lower-order harmonic components, the step modulation strategy is used in the proposed STATCOM system.

Fig. 3-4 shows the A-phase waveforms of the inverter (only waveforms with solid lines are considered). The switching angles, θ_1 , θ_2 , θ_3 and θ_4 , are chosen to cancel predominant lower frequency harmonics. For the nine-level case in Fig. 3-4, the 5th, 7th and 11th harmonics can be eliminated with the appropriate choice of the switching angles. One degree of freedom is used so that the magnitude of the output waveform corresponds to the modulation index of A-phase, M_a , which is expressed as:

$$M_a = \frac{P \cdot |v_{G,a}|_1}{16E} \quad (3.3)$$

where $|v_{G,a}|_1$ is the amplitude of the fundamental component of $v_{G,a}$.

Table 3-2 shows the off-line calculated switching angles, which are stored in a look-up table.

Table 3-2 Table of theoretical switching angles for different modulation index

M_a	θ_1 (rad)	θ_2 (rad)	θ_3 (rad)	θ_4 (rad)
0.56	0.59438	0.85477	1.0383	1.3207
N	N	N	N	N
0.78	0.17641	0.39873	0.726	1.086
0.79	0.17371	0.37637	0.6986	1.0709
0.8	0.17175	0.35575	0.6703	1.0545
N	N	N	N	N
0.85	0.078667	0.35911	0.48161	0.95097

Fig. 3-4. Waveforms of the output voltage of A-phase inverter, the A-phase current and the output voltages of HBs of A-phase inverter

3.2.3 Counts of GTOs

GTOs are selected as switching components in the STATCOM. A readily available GTO (MITSUBISHI GTO FG1000BV-90DA) has a typical repetitive peak off state voltage of 4.5 kV and repetitive controlled on-state current of 1 kA [99]. Normally, the GTO repetitive peak off state voltage and repetitive controlled on-state current are chosen to be 2~3 times of the system nominal ratings. In each HB module, GTOs are connected in series to make up rated dc source voltage to satisfy the redundancy requirement. The redundancy requirement is that if any single GTO fails (such as short circuit) in one inverter arm, the remaining functional GTOs can sustain continuous operation until the

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next planned maintenance outage. The number of GTOs required in the nine-level THMI and common nine-level cascade inverter are given in Table 3-3, where unit voltage of dc capacitors, E is 3.3 kV. The comparison shows the THMI uses fewer GTOs since the fewer redundant switches are needed in trinary hybrid topology.

Table 3-3 Comparison of GTO counts

	Nine-level THMI	Nine-level cascade multilevel inverter
GTOs in series per valve in the HB with dc voltage E	3 (1 redundant)	3 (1 redundant)
GTOs in series per valve in the HB with dc voltage $3E$	6 (1 redundant)	
Total number of GTOs	108	144

3.2.4 Series connection of GTOs

One of the advantages of a multilevel inverter is to achieve high voltage without having to connect switching devices in series directly. However, with the increase of power and voltage of the applications, the series connection of switching devices is inevitable. The total dc link voltages each phase is 13.2 kV here and [100], 16 kV in [101], and 38.4 kV in [102]. If the cascade multilevel inverters are used in these systems and each valve contains only one GTO specified here, each phase of inverter will contain 8 HBs here and [100], 10 HB in [101] and 23 HBs in [102]. Too many HBs result in very complicated power circuits, too many control signals and bulky system. Therefore, in very high power and voltage application, the series connection of power semiconductors is necessary.

Early, a large snubber is used to limit the dv/dt of the switching component during the turn-off period [103], and a variable inductor is to be placed between each gate drive circuit and the corresponding switching component in order to control the rising/falling time and to adjust the transient voltage [44, 104]. These modifications will increase the losses and reduce the dynamic performance, so a system with fewer GTOs connected in series provides better voltage sharing, and improves efficiency and dynamic performance [51]. Recently, however, the technology that allows the robust, reliable and cost-efficient series connection of GTOs is industrially mature [100]. Especially, in [102], with a

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digital control circuit for extremely accurate adjustment of gate turn-off timing in units of $0.1 \mu\text{s}$, the up to 16 GTOs connected in series shared the voltage uniformly in the turn-off period. This technology of adjustment can be available even the number of GTOs is further increased for a higher-voltage converter in the future. Moreover, with such technology, a system with more GTOs connected in series has almost the same voltage sharing, dynamic performance and efficiency as a system with fewer GTOs connected in series. Thanks to the precise gate turn-off timing adjustment presented in [102], the nine-level THMI in which up to 6 GTOs connected in series is not only feasible, but also has almost the same performances as the cascade multilevel inverter in which 3 GTOs connected in series.

3.2.5 Device power losses and the cost of cooling systems

Fig. 3-5 and Fig. 3-6 show waveforms of the currents flowing through arms of the HB_{aI} and the HB_{aII} , respectively. $i_{A,aij}$ ($i = \text{I, II}$ $j = 1 \dots 4$) is the current flowing through the j th arm of the HB_{ai} . The positive value of the $i_{A,aij}$ means that the current flows through GTOs, while the negative value of the $i_{A,aij}$ implies that the current flows through antiparallel diodes. As mentioned previously, if the output voltage of an HB is zero, the switches S_1 and S_3 will be turned on or the switches S_2 and S_4 will be turned on. For balancing the current stresses and power losses of switches, both of these two switching states for the zero output voltage of an HB are used and each switching state is used in an alternative cycle. In Fig. 3-5, if $v_{H,aII}$ is 0, the S_1 and S_3 of the HB_{aII} are turned on when ωt is from θ_2 to $\theta_2 + 2\pi$, but the S_2 and S_4 of the HB_{aII} are turned on when ωt is from 0 to θ_2 or from $\theta_2 + 2\pi$ to 2π . In Fig. 3-6, if $v_{H,aI}$ is 0, the S_1 and S_3 of the HB_{aI} are turned on when ωt is from θ_1 to $\theta_1 + 2\pi$, but the S_2 and S_4 of the HB_{aI} are turned on when ωt is from 0 to θ_1 or from $\theta_1 + 2\pi$ to 2π .

From Fig. 3-5 and Fig. 3-6, we note that the combination of waveforms of the non-zero current that flows through an arm during two periods is just the waveform of i_{Ga} in a complete period. So the on-state power losses of a GTO, $P_{O,ON}$, and the on-state power losses of an antiparallel diode, $P_{D,ON}$, can be expressed as

$$P_{O,ON} = \frac{V_o}{2T} \int_{p/2}^{3p/2} i_{G,a} d(\omega t) \quad (3.4)$$

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$$P_{D,ON} = \frac{V_D}{2T} \int_{p/2}^{3p/2} i_{G,a} d(\omega t) \quad (3.5)$$

where V_O and V_D are the voltage drops of a GTO and a diode respectively if they are in on-state. T is the period of $i_{G,a}$. V_O is 2.8 V approximately according to the data sheet of the GTO and V_D is 1.3 V approximately. So, from equations (3.4), (3.5) and Table 3-1, we can get $P_{O,ON}$ is 269 W and $P_{D,ON}$ is 125 W for the worst case.

Fig. 3-5. Waveforms of the currents flowing through arms of the HB_{aII} of the inverter

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Fig. 3-6. Waveforms of the currents flowing through arms of the HB_{aI} of the inverter

As shown in Fig. 3-5, the current that flows through a GTO in the HB_{aII} is $|i_{G,aI}|\sin\theta_2$ before the GTO is turned off, where $|i_{G,aI}|$ is the amplitude of the A-phase STATCOM current. For the worst case, the current is 454 A. Fig. 3-7 shows the data sheet of turn on and turn off switching energy of the GTO (MITSUBISHI GTO FG1000BV-90DA) when the dc off-state voltage is 2250 V. Based on Fig. 3-7, the turn off switching energy is 1.6 J when dc off-state voltage is 2250 V. As shown in Table 3-3, there are five GTOs (not including redundant one) connected in series in a arm of the HB_{aII} , so the GTOs endure the Off-state voltage, $3E/5$ (1980 V), after they are turned off. The turn off switching energy of the GTO in the HB_{aII} can be calculated as $1.6 \times 1980 / 2250 = 1.4$ J. From Fig. 3-5, one can find out the switching losses of the GTO in the HB_{aII} are due to a switching-off

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process of the GTO in a period. So, this switching losses can be calculated as $P_{O,SW,aII}=1.4 \times 50=70\text{W}$ for the worst case. The switching losses of the GTO in the HB_{aI} are due to three switching-off processes and two switching-on processes in a period. By the same method, the switching losses of the GTO in the HB^{aI} are calculated as $P_{O,SW,aI}=194\text{W}$ for the worst case.

Fig. 3-7. Turn on and turn off switching energy of the GTO (MITSUBISHI GTO FG1000BV-90DA)

If a nine-level cascade multilevel inverter is used in such a STATCOM system, the on-state losses and switching losses of the GTOs for the worst cases can be calculated by the same method above and the calculating results are shown in Table 3-4.

Table 3-4 Comparison of device power losses and cost of cooling systems

	HB (dc voltage)	Worst cases considered, redundant GTOs excluded			Cost of cooling system for a GTO and an antiparallel diode (\$)	Total cost of cooling systems in three-phase inverter (\$)
		GTO on-state power losses (W)	GTO switching losses (W)	Antiparallel diode on-state power losses (W)		
THMI	HB (E)	269	194	125	$588 k_{cl}$	$54576 k_{cl}$
	HB ($3E$)	269	70	125	$464 k_{cl}$	
Cascade multilevel inverter	HB (E)	269	51	125	$445 k_{cl}$	$65644 k_{cl}$
	HB (E)	269	62	125	$456 k_{cl}$	
	HB (E)	269	66	125	$460 k_{cl}$	
	HB (E)	269	69	125	$463 k_{cl}$	

Suppose the cost of cooling system is proportional to the power losses, that is

$$CC = k_{cl} P_{loss} \quad (3.6)$$

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where CC is the cost of cooling system, P_{loss} is power losses, and k_{cl} is the coefficient whose unit is \$/W. As shown in Table 3-4, the cost of the cooling system for a GTO and an antiparallel diode in the HB with $3E$ dc voltage in the THMI is almost the same as that in the cascade multilevel inverter. Comparatively, the cost of the cooling system for a GTO and an antiparallel diode in the HB with E dc voltage in the THMI are a little higher since the GTO switches at higher frequency. However, the total cost of cooling systems for the THMI are lower than that for the cascade multilevel inverter as shown in Table 3-4 since fewer GTOs are used in the THMI.

3.2.6 Cost of dc capacitors

The THMI not only needs fewer GTOs than the cascade multilevel inverter, but also has less cost of dc capacitors. Firstly, the required capacitance values of dc capacitors of the THMI are analyzed. Fig. 3-4 shows A-phase waveforms of the inverter (only waveforms with solid lines are considered). The STATCOM supplies reactive power, so the output voltage and output current of the inverter is orthogonal. Suppose the current generated by the STACOM is sinusoidal and $|i_{G,a}|_1$ is the amplitude of A-phase current. The A-phase current of the STATCOM in Fig. 3-4 can be expressed as:

$$i_{G,a} = |i_{G,a}|_1 \sin(\omega t - p/2) \quad (3.7)$$

where ω is radian frequency. Assuming initial voltages of A-phase dc capacitors are E and $3E$, respectively. Table 3-5 shows capacitor voltages during first half cycle in Fig. 3-4, where

$$m_1 = \frac{|i_{G,a}|_1}{\omega C_{a1}} \quad m_2 = \frac{|i_{G,a}|_1}{\omega C_{aII}} \quad (3.8)$$

The ε , dc voltage regulation factor, is selected as 5%, which means the dc capacitor voltages fluctuate within 0.95-1.05 times of the normal value. To keep the dc capacitor voltages within this range, the expression of capacitances for dc capacitors are expressed as:

$$C_{aI} = \frac{|i_{G,a}|_1 \cdot \text{MAX}[\text{ABS}(\sin q_1 - \sin q_2), \text{ABS}(\sin q_1 - 2 \sin q_2 + \sin q_3), \text{ABS}(\sin q_1 - 2 \sin q_2 + \sin q_3 + \sin q_4 - 1)]}{2\omega \varepsilon E} \quad (3.9)$$

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$$C_{aII} = \frac{|i_{G,a}|_I \cdot (1 - \sin q_2)}{6\omega E} \quad (3.10)$$

where ABS is the function of absolute value, MAX is the function of selecting one with the maximum value. Based on the consideration of the worst case from the Table 3-2, the required capacitances C_{aI} and C_{aII} are 2580 μF and 1050 μF .

Table 3-5 A-phase dc capacitor voltages during half cycle

Instant	$V_{C,aI}$	$V_{C,aII}$
0	E	$3E$
$\theta_1/(\omega t)$	E	$3E$
$\theta_2/(\omega t)$	$E - m_1(\sin\theta_1 - \sin\theta_2)$	$3E$
$\theta_3/(\omega t)$	$E - m_1(\sin\theta_1 - 2\sin\theta_2 + \sin\theta_3)$	$3E - m_2(\sin\theta_2 - \sin\theta_3)$
$\theta_4/(\omega t)$	$E - m_1(\sin\theta_1 - 2\sin\theta_2 + \sin\theta_3)$	$3E - m_2(\sin\theta_2 - \sin\theta_4)$
$\pi/(2\omega t)$	$E - m_1(\sin\theta_1 - 2\sin\theta_2 + \sin\theta_3 + \sin\theta_4 - 1)$	$3E - m_2(\sin\theta_2 - 1)$
$(\pi - \theta_4)/(\omega t)$	$E - m_1(\sin\theta_1 - 2\sin\theta_2 + \sin\theta_3)$	$3E - m_2(\sin\theta_2 - \sin\theta_4)$
$(\pi - \theta_3)/(\omega t)$	$E - m_1(\sin\theta_1 - 2\sin\theta_2 + \sin\theta_3)$	$3E - m_2(\sin\theta_2 - \sin\theta_3)$
$(\pi - \theta_2)/(\omega t)$	$E - m_1(\sin\theta_1 - \sin\theta_2)$	$3E$
$(\pi - \theta_1)/(\omega t)$	E	$3E$
$\pi/(\omega t)$	E	$3E$

If a nine-level cascade multilevel inverter is used in such STATCOM system, the required capacitances are calculated by (3.11) for the comparison. From (3.11) and Table 3-2, for the worst cases, the required capacitances are 5380 μF , 3960 μF , 3130 μF and 1060 μF .

$$C_{ak} = \frac{|i_{G,a}|_I (1 - \sin q_k)}{2\omega E} \quad (3.11)$$

Table 3-6 shows the prices of high-voltage high-capacitance capacitors [105] and Table 3-7 shows the counts and cost of capacitors. Capacitors are connected to form an array of capacitors to satisfy required capacitance and rating voltage. The array has n rows in parallel and each row includes m capacitors connected in series. Moreover, an additional row is used to satisfy the redundancy requirement. Normally, the peak voltage and current rating of the capacitor array are chosen to be 2-3 times of the system nominal voltage. The comparison results show the cost of dc capacitors in the THMI is less than that in cascade multilevel inverters in which the current and voltage stresses of switches

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are balanced [34] or not balanced [48]. There are two reasons why the cost of dc capacitors in THMI is less. Firstly, it needs less redundancy capacitors. Secondly, the capacitor C_{al} was both charged and discharged in quarter cycles ($0-\pi/2$, $\pi/2-\pi$, $\pi-3\pi/2$ or $3\pi/2-2\pi$) as shown in Fig. 3-4, so the required C_{al} is smaller.

Table 3-6 Prices of capacitors with high-voltage and high-capacitance

Capacitors	Series	Prices (Europe \$)
A	GMKPg 3.6kV/1114 μ F	1873
B	GMKPg 2.6kV/4400 μ F	2565
C	GMKPg 1.9kV/4000 μ F	1248
D	GMKPg 1kV/9000 μ F	943
E	GMKPg 0.9kV/12000 μ F	1598

Table 3-7 Comparison of Counts and costs of capacitors

	HB (dc voltage) per phase	Capacitance / rating voltage of dc capacitor	Capacitor	m series	$n+1$ parallel	Total price (Europe \$)
THMI	HB (E)	2.58 mF / 3.3 kV	B	3	2+1	305,253
	HB ($3E$)	1.05 mF / 9.9 kV	A	6	6+1	
Cascade multilevel inverter (without balancing stresses)	HB (E)	5.38 mF / 3.3 kV	B	3	4+1	333,816
	HB (E)	3.96 mF / 3.3 kV	B	3	3+1	
	HB (E)	3.13 mF / 3.3 kV	B	3	3+1	
	HB (E)	1.06 mF / 3.3 kV	A	2	2+1	
Cascade multilevel inverter (with balancing stresses)	Four HBs (E)	5.38 mF / 3.3 kV	B	3	4+1	461,700

3.3 Control system of the STATCOM

Fig. 3-8 shows the control system of STATCOM. The power control module controls not only the reactive power but also the active power that compensates the power losses of the inverter and interface impedance. The input signals of the power control module are positive sequence components of bus voltages and inverter output currents. The function of unbalanced voltage control module is to eliminate the negative sequence components of the bus voltages, so that the bus voltages can be balanced. The reference output voltage of inverter $\mathbf{v}_{G,abc}^*$ is the addition of the output of power control module $\mathbf{v}_{P,abc}^*$ and the output of unbalanced voltage control module $\mathbf{v}_{U,abc}^*$. Each phase of the inverter is controlled separately by the inverter control module A, B or C. Inverter control modules not only control the output voltage waveform of the inverter, $\mathbf{v}_{G,abc}$, but also are

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responsible for the balancing of each dc capacitor voltage. At first, introduce vector representation and transformation of instantaneous three-phase quantities, and then specify these modules one by one.

Fig. 3-8. Control system of the STATCOM

3.3.1 Vector representation and transformation of instantaneous three-phase quantities

A set of three instantaneous phase variables γ_a , γ_b and γ_c that sum to be zero can be uniquely represented in the $\alpha\beta$ -phase frame through the $abc \rightarrow \alpha\beta$ transformation matrix $[\mathbf{T}_{abc \rightarrow \alpha\beta}]$.

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$$[\mathbf{T}_{abc \rightarrow ab}] = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (3.12)$$

The $\alpha\beta \rightarrow abc$ transformation matrix $[\mathbf{T}_{\alpha\beta \rightarrow abc}]$ is the inverse of $[\mathbf{T}_{abc \rightarrow \alpha\beta}]$.

$$[\mathbf{T}_{ab \rightarrow abc}] = [\mathbf{T}_{abc \rightarrow ab}]^{-1} = \frac{3}{2} [\mathbf{T}_{abc \rightarrow ab}]^T \quad (3.13)$$

Thus,

$$\begin{bmatrix} \mathbf{g}_a \\ \mathbf{g}_b \\ 0 \end{bmatrix} = [\mathbf{T}_{ab \rightarrow abc}] \boldsymbol{\gamma}_{abc}, \quad \boldsymbol{\gamma}_{abc} = [\mathbf{T}_{abc \rightarrow ab}] \begin{bmatrix} \mathbf{g}_a \\ \mathbf{g}_b \\ 0 \end{bmatrix} \quad (3.14)$$

where

$$\boldsymbol{\gamma}_{abc} = \begin{bmatrix} \mathbf{g}_a \\ \mathbf{g}_b \\ \mathbf{g}_c \end{bmatrix} \quad (3.15)$$

Furthermore, one can get $dq+$ or $dq-$ coordinate expressions by using the positive or negative sequence synchronous reference frame transformations $[\mathbf{T}_{\alpha\beta \rightarrow dq+}]$ or $[\mathbf{T}_{\alpha\beta \rightarrow dq-}]$, respectively.

$$\boldsymbol{\gamma}_{dq+} = [\mathbf{T}_{ab \rightarrow dq+}] \boldsymbol{\gamma}_{ab} \quad \boldsymbol{\gamma}_{ab} = [\mathbf{T}_{dq+ \rightarrow ab}] \boldsymbol{\gamma}_{dq+} \quad (3.16)$$

$$\boldsymbol{\gamma}_{dq-} = [\mathbf{T}_{ab \rightarrow dq-}] \boldsymbol{\gamma}_{ab} \quad \boldsymbol{\gamma}_{ab} = [\mathbf{T}_{dq- \rightarrow ab}] \boldsymbol{\gamma}_{dq-} \quad (3.17)$$

where

$$\boldsymbol{\gamma}_{ab} = \begin{bmatrix} \mathbf{g}_a \\ \mathbf{g}_b \end{bmatrix}, \quad \boldsymbol{\gamma}_{dq+} = \begin{bmatrix} \mathbf{g}_{d+} \\ \mathbf{g}_{q+} \end{bmatrix}, \quad \boldsymbol{\gamma}_{dq-} = \begin{bmatrix} \mathbf{g}_{d-} \\ \mathbf{g}_{q-} \end{bmatrix} \quad (3.18)$$

$$[\mathbf{T}_{ab \rightarrow dq+}] = \begin{bmatrix} \cos J & \sin J \\ -\sin J & \cos J \end{bmatrix}, \quad [\mathbf{T}_{dq+ \rightarrow ab}] = [\mathbf{T}_{ab \rightarrow dq+}]^T \quad (3.19)$$

$$[\mathbf{T}_{ab \rightarrow dq-}] = \begin{bmatrix} \cos J & -\sin J \\ -\sin J & -\cos J \end{bmatrix}, \quad [\mathbf{T}_{dq- \rightarrow ab}] = [\mathbf{T}_{ab \rightarrow dq-}]^T \quad (3.20)$$

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$$J = \int \omega t + J_0 \quad (3.21)$$

where J_0 is determined by the definition of the $dq+$ co-ordinate frame.

3.3.2 Power control module

The power control module regulates the positive sequence reactive power and active power injected into the bus. Three-phase bus voltages $\mathbf{v}_{B,abc}$ and three-phase inverter output currents $\mathbf{i}_{G,abc}$ can be transformed into $\mathbf{v}_{B,\alpha\beta}$ and $\mathbf{i}_{G,\alpha\beta}$ in $\alpha\beta$ phase frame by (3.14). The active power and reactive power can be shown as:

$$P = \frac{3}{2}(v_{B,a}i_{G,a} + v_{B,b}i_{G,b}), \quad Q = \frac{3}{2}(v_{B,a}i_{G,b} - v_{B,b}i_{G,a}) \quad (3.22)$$

The $\mathbf{v}_{B,\alpha\beta}$ and $\mathbf{i}_{G,\alpha\beta}$ can be transformed into $\mathbf{v}_{B,dq+}$ and $\mathbf{i}_{G,dq+}$ in $dq+$ frame by (3.16). The $dq+$ co-ordinate frame is defined where $d+$ axis is always coincident with the instantaneous voltage vector and the $q+$ axis is in quadrature with it, i.e.

$$J = \arctan\left(\frac{v_{B,b}}{v_{B,a}}\right) \quad (3.23)$$

Under balanced steady-state conditions,

$$\mathbf{v}_{B,dq+} = \begin{bmatrix} |\mathbf{v}_{B,abc}| \\ 0 \end{bmatrix} \quad (3.24)$$

where $|\mathbf{v}_{B,abc}|$ is the amplitude of phase voltage of the bus. Therefore, the active power and reactive power can be expressed as:

$$P = \frac{3}{2} \cdot |\mathbf{v}_{B,abc}| \cdot i_{G,d+}, \quad Q = \frac{3}{2} \cdot |\mathbf{v}_{B,abc}| \cdot i_{G,q+} \quad (3.25)$$

In Fig. 3-2, the resistance and inductance of interface impedance are expressed as R_I and L_I . From the Fig. 3-2

$$L_I \frac{d\mathbf{i}_{G,abc}}{dt} + R_I \mathbf{i}_{G,abc} = \mathbf{v}_{G,abc} - \mathbf{v}_{B,abc} \quad (3.26)$$

From (3.14) and (3.26)

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$$L_l \frac{d\mathbf{i}_{G,ab}}{dt} + R_l \mathbf{i}_{G,ab} = \mathbf{v}_{G,ab} - \mathbf{v}_{B,ab} \quad (3.27)$$

From (3.16), (3.23) and (3.27)

$$L_l \frac{d}{dt} \begin{bmatrix} i_{G,d+} \\ i_{G,q+} \end{bmatrix} + \omega L_l \begin{bmatrix} -i_{G,q+} \\ i_{G,d+} \end{bmatrix} + R_l \begin{bmatrix} i_{G,d+} \\ i_{G,q+} \end{bmatrix} = \begin{bmatrix} v_{G,d+} - v_{B,d+} \\ v_{G,q+} - v_{B,q+} \end{bmatrix} \quad (3.28)$$

Thus, under balanced conditions, the plant of the STATCOM system can be expressed as (3.29) in s domain, as shown in Fig. 3-9.

$$\begin{bmatrix} v_{G,d+} - v_{B,d+} + \omega L_l i_{G,q+} - R_l i_{G,d+} \\ v_{G,q+} - v_{B,q+} - \omega L_l i_{G,d+} - R_l i_{G,q+} \end{bmatrix} = \begin{bmatrix} sL_l i_{G,d+} \\ sL_l i_{G,q+} \end{bmatrix} \quad (3.29)$$

Fig. 3-9. Plant of the STATCOM system in s domain

A PI controller is used for both active and reactive current control loop as shown in Fig. 3-10. Under balanced conditions, the inverter can be regarded as a unit function. $v_{G,d+}$ and $v_{G,q+}$ in Fig. 3-9 are equal to $v_{G,d+}^*$ and $v_{G,q+}^*$ in Fig. 3-10, i.e.,

$$v_{G,d+} = v_{G,d+}^* \quad v_{G,q+} = v_{G,q+}^* \quad (3.30)$$

The Fig. 3-11 shows the equivalent control diagrams for $i_{G,d+}$ and $i_{G,q+}$, which is derived from Fig. 3-9, Fig. 3-10 and (3.30). The controlled system is reduced to a first order transfer function [49].

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Fig. 3-10. Power control module

Fig. 3-11. Equivalent control diagram for $i_{C,d+}$ and $i_{C,q+}$.

Active power flowing into STATCOM will regulate dc capacitor voltages of the inverter. E is the reference value of unit voltage of dc capacitors. $v_{C,av}$ is the average unit voltage of dc capacitors and can be calculated by

$$v_{C,av} = \frac{1}{12}(v_{C,aI} + v_{C,aII} + v_{C,bI} + v_{C,bII} + v_{C,cI} + v_{C,cII}) \quad (3.31)$$

The active current reference, $i_{G,d+*}$, is generated from a PI controller, which controls $v_{C,av}$. The reactive current reference, $i_{G,q+*}$, is given according to different compensation aims. For example, for an STATCOM to compensate the reactive power of a load, it will be the load reactive current. Under balanced conditions, the $dq+$ component of the bus voltages is shown in (3.24). The output of this module, $\mathbf{v}_{P,abc*}$, is obtained from $i_{G,d+*}$ and $i_{G,q+*}$ through $\mathbf{T}_{dq+ \rightarrow \alpha\beta}$ and $\mathbf{T}_{\alpha\beta \rightarrow abc}$ as previously mentioned.

3.3.3 Unbalanced voltage control module

Assuming sequence components are not coupled, Fig. 3-2 can be thought as separately representing either the positive or the negative sequence. Considering the case of the negative sequence components and using the phasors. V_{G-} represents the negative sequence component of compensator voltage generated by the STATCOM and V_{B-} means the negative sequence component of bus voltage. Setting V_{G-} equals to k times V_{B-} , V_{B-} can be expressed as

$$V_{B-} = V_{S-} \cdot \frac{Z_I \cdot Z_L}{Z_S \cdot Z_I + Z_I \cdot Z_L + (1-k) \cdot Z_S \cdot Z_L} \quad (3.32)$$

A Proportional controller in the synchronous reference dq - frame is used to produce the amplitude of v_{G-} from the amplitude of v_{B-} as shown in Fig. 3-12. A large Proportional can reduce the negative sequence component of the bus voltage greatly, which is derived from (3.32). The output of transform $T_{\alpha\beta \rightarrow dq-}$ contains second harmonic components with frequency 100 Hz in addition to dc components. A mean function that generates the average value of input during last 0.01 second is used to eliminate the second harmonic components. Thus, in the dq - frame, the regulated quantities appear as dc. When the STATCOM is used to balance the bus voltages, there is a problem that the inverter current may be over rating. Under unbalanced conditions, the output of the Proportional control in Fig. 3-12 is a signal corresponding to the voltage drop across the STATCOM interface impedance. By limiting the value of this voltage drop, the inverter current is limited.

Fig. 3-12. Unbalanced voltage control module

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When the STATCOM balances the bus voltages, the negative sequence power that the inverter sends can be expressed as:

$$P_- = \frac{V_{G-}(V_{G-} - V_{B-})R_I}{R_I^2 + (wL_I)^2} \quad (3.33)$$

Since $R_I = wL_I$, the P_- is quite small. This small deviation of dc capacitor voltages that caused by the P_- can be balanced by ejecting or absorbing additional positive sequence power.

3.3.4 Inverter control modules

Fig. 3-13 shows the inverter control module A. The operation and principle of the inverter control module B and C are the same as that of the inverter control module A. The inverter control module A can be divided as part A and part B as shown in Fig. 3-13

Fig. 3-13. Inverter control module A

The part A of Fig. 3-13 addresses the issue of balancing individual capacitor voltages $v_{C,aI}$ and $v_{C,aII}$. Without additional control for balancing the individual capacitor voltages, the capacitor voltages will become unequal under unbalanced conditions or during transient process. Additionally, each dc capacitor voltage may not exactly be balanced even under steady balanced conditions since inverter devices are not ideal and have different

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tolerance errors. Fig. 3-4 shows the waveforms when the STATCOM supplied reactive power to the system.

Firstly, the second HB of A-phase, HB_{aII}, is analyzed. When the output voltage of HB_{aII}, $v_{H,aII}$, has the same direction as $i_{G,a}$, the capacitor C_{aII} is discharged and vice versa. If the $v_{H,aII}$ is shown as real line in the Fig. 3-4, the average charge into the capacitor C_{aII} over each half cycle is zero. However, if $v_{H,aII}$ is shifted by $\Delta\delta_2$ by the dark dished line, the charge over each half cycle can be expressed as

$$Q_{aII} = \int_{q_2 + \mathbf{V}d_2}^{p - q_2 + \mathbf{V}d_2} 3E |i_{G,a}|_1 \cos J dJ = -6E |i_{G,a}|_1 \cos q_2 \sin \mathbf{V}d_2 \quad (3.34)$$

where $i_{G,a}$ is sinusoidal and $|i_{G,a}|_1$ is amplitude of $i_{G,a}$. Q_{aII} is proportional to $\Delta\delta_2$ when $\Delta\delta_2$ is small. So approximately Q_{aII} can be written as:

$$Q_{aII} = -6E |i_{G,a}|_1 \cos q_2 \sin \mathbf{V}d_2 \quad (3.35)$$

Therefore, the capacitor voltage $v_{C,aII}$ can be controlled by slightly shifting the switching pattern. For high-power high-voltage applications, the total power loss of the inverter is less than 1%, thus $\mathbf{V}d_2 = 0.1$ rad [48]. The shifted switching angles about HB_{aII} during 0 to 2π are $\theta_2 + \Delta\delta_2$, $\pi - (\theta_2 - \Delta\delta_2)$, $\pi + (\theta_2 + \Delta\delta_2)$ and $2\pi - (\theta_2 - \Delta\delta_2)$. Suppose

$$d_2 = q_2 - B_b(v_{G,a} i_{G,a}) \cdot \mathbf{V}d_2 \quad (3.36)$$

where $B_b(\cdot)$ is bi-polar binary function and can be expressed as

$$B_b(t) = \begin{cases} 1 & t > 0 \\ 0 & t = 0 \\ -1 & t < 0 \end{cases} \quad (3.37)$$

Therefore, the shifted switching angles about HB_{aII} during 0 to 2π are δ_2 , $\pi - \delta_2$, $\pi + \delta_2$ and $2\pi - \delta_2$.

The average charge current for C_{aII} can be expressed as:

$$i_{C,aII} = 100Q_{aII} \quad (3.38)$$

And the relationship between the current of C_{aII} , $i_{C,aII}$ and the voltage of C_{aII} , $v_{C,aII}$, can be expressed as:

$$i_{C,aII} = C_{aII} \frac{dv_{C,aII}}{dt} \quad (3.39)$$

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From (3.35), (3.38) and (3.39), the transfer function from $\Delta\delta_2$ to $v_{C,aII}$ in s domain can be written as:

$$\frac{v_{C,aII}}{\mathbf{V}d_2} = \frac{k_1}{s} \quad (k_1 = \frac{-600E|i_{G,a}| \cos q_2}{C_{aII}}) \quad (3.40)$$

Once the switching angles of HB_{aII} is decided, the switching angles of HB_{aI} will be regulated for controlling the dc capacitor voltage of HB_{aI} , $v_{C,aI}$. As shown in Fig. 3-4, the switching angles of HB_{aII} over the first quarter cycle is $\theta_2 + \Delta\delta_2$, so the second switching angles of HB_{aI} over the first quarter cycle must be $\theta_2 + \Delta\delta_2$, otherwise the inverter will generate voltage spikes. If the switching angles of HB_{aI} over the first half cycle are θ_1 , $\theta_2 + \Delta\delta_2$, θ_3 , θ_4 , $\pi - \theta_4$, $\pi - \theta_3 + \Delta\delta_2$, $\pi - \theta_2$ and $\pi - \theta_1$, the charge to C_{aI} during the first half cycle can be expressed as

$$Q'_{aI} = 4E|i_{G,a}| \cos q_2 \sin \mathbf{V}d_2 \quad (3.41)$$

For balancing the C_{aI} , other switching angles will shift slightly as shown in Fig. 3-4. Then the charge to the C_{aI} during half cycle can be expressed as

$$Q_{aI} = -2E|i_{G,a}| (-2 \cos q_2 \sin \mathbf{V}d_2 + \cos q_1 \sin \mathbf{V}d_1 + \cos q_3 \sin \mathbf{V}d_3 + \cos q_4 \sin \mathbf{V}d_4) \quad (3.42)$$

To shift switching angles averagely, $\Delta\delta_1$, $\Delta\delta_3$ and $\Delta\delta_4$ are set equal as $\Delta\delta$. So (3.42) can be rewritten as

$$Q_{aI} = -2E|i_{G,a}| [-2 \cos q_2 \sin \mathbf{V}d_2 + (\cos q_1 + \cos q_3 + \cos q_4) \sin \mathbf{V}d] \quad (3.43)$$

In s domain, the $v_{C,aI}$ can be expressed as

$$v_{C,aI} = \frac{k_2}{s} \mathbf{V}d_2 + \frac{k_3}{s} \mathbf{V}d \quad (3.44)$$

where

$$k_2 = \frac{200E|i_{G,a}| \cos q_2}{C_{aI}} \quad k_3 = \frac{-200E|i_{G,a}| (\cos q_1 + \cos q_3 + \cos q_4)}{C_{aI}} \quad (3.45)$$

PI controllers are used to regulate the dc capacitor voltages as shown in Fig. 3-14. In the control loop, additional feed forward path (bold part) can enhance dynamic response. The relationship between $-k_2/k_3$ and modulation index is shown in Fig. 3-15. In general,

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the inverter runs at the modulation index higher than 0.7. So $-k_2/k_3$ is selected as 0.81 approximately.

Fig. 3-14. Control scheme for individual dc capacitor voltages

Fig. 3-15. Relationship between $-k_2/k_3$ and the modulation index M

The part B of Fig. 3-13 shows the main control scheme to generate desired switching signals from the reference voltages of the inverter. In the thesis and [48, 49], the step modulation strategy is used. In [48, 49], only the balanced condition is considered and the control aim is just to regulate the reactive power, so the amplitude of inverter voltage can be controlled by control loop for reactive power and the phase angle of inverter voltage can be controlled by the control loop for active power, respectively. The above method

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cannot be applied in the STATCOM control system presented in the thesis since, in addition to regulation of reactive power, balance of bus voltages during unbalanced conditions is involved in the control aims. To achieve these aims, the reference voltages of the inverters, $\mathbf{v}_{G,abc}^*$, are the addition of the resulting signals of the power control module, $\mathbf{v}_{P,abc}^*$, and the resulting signals of the power control module, $\mathbf{v}_{U,abc}^*$, as shown in Fig. 3-8. Based on the reference voltages of the inverter, the switching signals are produced to control the inverter.

Under balanced conditions, the reference voltages of the inverter are quite close to pure sinusoidal waveforms since they only contain higher-order harmonic components whose amplitudes are very low. The 5th, 7th and 11th order harmonics of the output voltage of the A-phase (B-phase or C-phase) inverter are nearly eliminated by the step modulation strategy, so these harmonic components of the STATCOM currents and bus voltages are very small. The output voltage of the A-phase (B-phase or C-phase) inverter contains triple-order harmonic components. Under balanced conditions, the amplitudes of triple-order harmonic components of the output voltage of the A-phase inverter are the same as those of the B-phase inverter and the C-phase inverter, so triple-order harmonic components of the STATCOM currents and bus voltages don't exist with the proper connection of the STATCOM system. Amplitudes of other higher-order harmonic components of the STATCOM currents and bus voltages are very low. As stated above, the reference voltages of the inverter are the addition of resulting signals of the power control module and the unbalanced voltage control module that are fed by the STATCOM currents and the bus voltages as show in Fig. 3-8. As shown in Fig. 3-12, the unbalanced voltage control module contains the mean functions that eliminate the effect of harmonic components of the STATCOM currents and the bus voltages. However, the power control module does not contain them to keep high dynamic performance. Therefore, the reference voltages of the inverter contain higher-order harmonic components whose amplitudes are very low.

Under unbalanced conditions, the reference voltages of the inverters are far from pure sinusoidal waveforms since they contain lower-order harmonic components whose amplitudes are high. Under unbalanced conditions, the amplitudes of output voltages of A-phase inverter, B-phase inverter and C-phase inverter are not identical, so the

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amplitudes of triple-harmonic components of these output voltages are not identical. It causes that the STATCOM currents and the bus voltages contain high triple-order harmonic components, especially the third-order harmonic components. The reference voltages of the inverter also contain high triple-order harmonic components that passed from the STATCOM currents and the bus voltages through the power control module. Therefore, the reference voltages of the inverter are far from pure sinusoidal waveforms. Without good sinusoidal reference voltages of the inverter, the 5th, 7th and 11th order harmonic components of the output voltages of the A-phase, B-phase and C-phase inverters cannot be eliminated effectively by the step modulation strategy. Thus, the STATCOM currents and the bus voltages under unbalanced conditions contain higher 5th, 7th and 11th order harmonic components than those under balanced conditions. Therefore, the reference voltages of the inverter are far from pure sinusoidal waveforms because of not only high tripe-order harmonic components but also 5th, 7th and 11th order harmonic components. If mean functions or filters are added into the power control module to eliminate the lower-order harmonic components of the reference voltages of the inverter, the dynamic performance of the reactive and active power control will be worse. It is undesirable since the main purpose of STATCOM is to regulate reactive power quickly and the STATCOM works under balanced conditions at most of time.

Therefore, a robust control method is needed in this STATCOM system, which must satisfy the following two items. Firstly, under balanced conditions, reactive power can be regulated rapidly and $v_{G,a}$ does not contain 5th, 7th and 11th harmonics. Secondly, under unbalanced conditions, the STATCOM can work steadily and the bus voltages can be balanced. To achieve above aims, a new control method is proposed. By this method, $v_{G,a}$ is synthesized and satisfies the following two items. Firstly, under balanced conditions, the amplitude and phase angle of fundamental component of $v_{G,a}$ are the same as those of $v_{G,a}^*$. Moreover, $v_{G,a}$ does not contain 5th, 7th and 11th harmonics. Secondly, under unbalanced conditions, $v_{G,a}$ can follow the track of $v_{G,a}^*$.

The method by which the $v_{G,a}$ is synthesized is shown in the part B of Fig. 3-13. $\text{ABS}(v_{G,a}^*)$ is the absolute value of $v_{G,a}^*$. The reference signal S_a equals to $\text{ABS}(v_{G,a}^*)/(4E)$. $|S_a|_1$ is the amplitude of fundamental component of S_a . From (3.3), one can get modulation index M_a that is just $|S_a|_1\pi/4$. From the table of switching angles (TSA) shown in Table

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3-2, the theoretical switching angles, $\theta_1 - \theta_4$, can be gained. The theoretical switching angles are shifted slightly to balance individual capacitor voltages by the control loop shown in the part A of Fig. 3-13. Thus, the final switching angles are δ_1 to δ_4 .

The following is the key part of the new method. The conventional method used in [34, 48, 49] is to compare the phase angle ωt with switching angles to determine the switching states. The new method is to compare the reference signal ($S_a/|S_{a1}|$) with a series of reference amplitudes ($\sin\delta_1$ to $\sin\delta_4$) as shown in Fig. 3-16.

Fig. 3-16. Demonstration of comparing reference amplitudes with the reference signal in the inverter control model A

Firstly, the case in which v_{G,a^*} is a perfect sinusoidal waveform is considered. In the first quarter cycle, S_a is a perfect sinusoidal waveform and can be expressed as

$$S_a = |S_{a1}| \sin(\omega t) \quad (3.46)$$

In the first quarter cycle,

$$\frac{S_a}{|S_{a1}|} > \sin d_i \Leftrightarrow \omega t > d_i \quad (i=1,2,3,4) \quad (3.47)$$

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The (3.47) shows, as v_{G,a^*} is perfect sinusoidal, the new method has the same function as the conventional method by which the lower-order harmonics can be eliminated. In practice, under balanced conditions, the v_{G,a^*} is quite close to a sinusoidal waveform. Therefore, under balanced conditions, the new method can also eliminate lower-order harmonics just like the conventional method.

Secondly, under unbalanced conditions, the v_{G,a^*} is far from a sinusoidal waveform because of lower-order harmonics. With the new method as shown in Fig. 3-16, one can get the $v_{G,a}$ whose waveform is quite similar to that of v_{G,a^*} . Moreover, the new method is more robust than the method in which the switching angles are compared with ωt gotten by Phase Locked Loop (PLL). Under unbalanced condition and during transient process, the increasing rate of the value of ωt is not very stable, so a small deviation of this rate will result in a large deviation of comparison result. Therefore, the new method based on the comparison of amplitudes is more robust than the conventional method based on the comparison of angles under unbalanced conditions and during transient processes.

Thus, with the new method, the two aims mentioned previously are achieved. Moreover, the dead zone control is used to avoid high frequency switching of switches in a short interval. In the Fig. 3-16, WB is the width of dead zone. The control system of dead zone is shown in Fig. 3-13. The values of $(S_a/|S_a|_1 + WB)$ and $(S_a/|S_a|_1 - WB)$ are compared with $\sin\delta_1$ to $\sin\delta_4$, respectively. The comparison results are the inputs of $B_u(\cdot)$ that is uni-polar binary function shown as

$$B_u(t) = \begin{cases} 1 & t \geq 0 \\ 0 & t < 0 \end{cases} \quad (3.48)$$

The addition results of $B_u(\cdot)$ are compared in the function of comparing and keeping, FC, as shown in Fig. 7. Suppose l is the expected level number of $v_{G,a}$ and $ABS(l)$ is the absolute value of l . If the two addition results are different, the FC outputs the $ABS(l_{last})$ (the last values of $ABS(l)$). If the two addition results are identical, the FC outputs this addition result. The l is gotten from $ABS(l)$ and the polar of v_{G,a^*} . Finally, based on Table 2-2 and definition of the switching function, the switching signals for the A-phase inverter can be gotten from l . From Fig. 3-16, one can see that the waveform of $ABS(l)$ will slightly shift right because of dead zone, which will result in additional charge or

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discharge of dc capacitors. However, with the control loop shown in the part A of Fig. 3-13, the dc capacitor voltages can be balanced.

3.4 Simulation results

The performance of the STATCOM system presented above has been verified under balanced and unbalance conditions by simulation. The simulation investigations were performed with MATLAB Simulink. The parameters of the distribution system and STATCOM are shown in Table 3-1. In Table 3-1, the capacitance of dc capacitors used in simulation is calculated based on Table 3-6 and Table 3-7 (redundancy capacitors are not considered). The parameters of the GTOs are shown in Table 3-8.

Table 3-8 Parameter of the GTO (MITSUBISHI GTO FG1000BV-90DA)

Forward voltage	2.3 V
Turn-on resistance	0.002 Ω
Turn-on inductance	10 μ H
Current falling time	10 μ s
Current tail time	20 μ s
Diode forward voltage	1.2 V
Diode turn-on resistance	0.0005 Ω
Snubber resistance	10 Ω
Snubber capacitor	0.7 μ F

Fig. 3-17 shows simulated waveforms under balanced conditions. The step changes of the reference signal of the reactive power, Q^* , is from 0 to 7 MVar at 0.12 seconds and from 7 MVar to -7 MVar at 0.18 seconds. It is seen that the reactive power Q rapidly tracks the step-changing reference while the active power maintains zero. Complete decoupled control is achieved. Because maximum rms value of output voltage of one phase of the inverter is bounded at $2\sqrt{2}p(4E)$, the respond speed of this system is only constrained by a practical dc voltage.

Fig. 3-18 shows simulated frequency spectrums of the A-phase STATCOM current, the A-phase line-neutral voltage of the bus and the reference voltage of the A-phase inverter when Q^* is -7 MVar. In them, the triple-order harmonic components are nearly zero and the 5th, 7th and 11th order harmonic components are low. The reference

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voltages of the inverter still contains still contain 13th and higher order harmonics which may result in additional switching of the switches. Two methods are used to avoid the additional switching. Firstly, Smaller P in PI controller as shown in Fig. 3-10 will reduce the amplitude of harmonics of $v_{G,abc}^*$. P and I are adjusted to 9 and 500 respectively so that the inverter has enough dynamic response and the amplitude of harmonics of $v_{G,abc}^*$ is limited in appropriate range. Furthermore, the dead zone control as shown in the part B of Fig. 3-13 eliminates the effect of the harmonics. The width of dead zone, WB , is selected as 0.008. From the Fig. 3-17, one can see that voltage levels of the inverter is identical, which means the dc capacitor voltages are balanced by the control loops shown in the part A of Fig. 3-13 in which P and I is selected as 0.001 and 0.01 respectively.

Fig. 3-17. Simulation waveforms of the STATCOM under balanced conditions.

- a P, Q and Q*: active power, reactive power and reference value of reactive power
- b $v_{G,a}^*$, $v_{G,b}^*$ and $v_{G,c}^*$: reference voltages of the inverter
- c $v_{G,a}$, $v_{G,b}$ and $v_{G,c}$: the output voltage of A-phase, B-phase and C-phase inverter
- d phase currents of the STATCOM
- e line-neutral voltages of the bus

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Fig. 3-18. Simulated frequency spectrums under balanced conditions

a Simulated frequency spectrum of the A-phase current of the STATCOM

b Simulated frequency spectrum of the A-phase line-neutral voltage of the bus

c Simulated frequency spectrum of the reference voltage of the A-phase inverter

Fig. 3-19 shows simulated waveforms of the STATCOM during unbalanced conditions. Before 0.2 seconds and after 0.4 seconds, the source voltage is balanced. From 0.2 seconds to 0.3 seconds, the source voltages are unbalanced with 0.25 p.u. negative sequence voltage components added. Fig. 3-19 (a) and (b) show the bus voltages without compensation and with compensation. With compensation, the bus voltage is balanced. By limiting the value of P controller in Fig. 6, the current sent by the STATCOM is limited within the rating values as shown Fig. 3-19 (d). When compensator is active, the negative sequence component of the bus voltage is reduced. The amount of compensation is subjected to the limitation of the inverter current. In the unbalanced voltage control module as shown in Fig. 6, the P is selected as 10 and limitation of P controller is from -7000 to 7000.

Fig. 3-20 shows simulated frequency spectrums of the STATCOM currents, the bus voltages and the reference voltages of the inverter during the unbalanced conditions with compensation. The inverter is controlled well to compensate the bus voltages in spite of high lower-order harmonic components in the reference voltages of the inverter, which proves that the new method as shown in the part B of Fig. 3-13 is effective. The dominate lower-order harmonic components in the STATCOM currents are the third-order harmonics, whose amplitudes are lower than 15% of the rating value of the STATCOM

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currents. In the worst case, the voltage ripple of a dc capacitor caused by the third-order harmonic component of the STATCOM current is less than 0.5% of the normal voltage of a dc capacitor. The effect of other harmonic components on the voltage ripple of a dc capacitor is much lower than that of the third-order harmonic. And the durations of unbalanced conditions are short generally. So the effect of harmonic components of the STATCOM currents on the voltage ripples of dc capacitors is small and transitory. The determination of dc capacitance can still be based on the assumption of a sinusoidal current from the STATCOM.

Fig. 3-19. Simulated waveform of the STATCOM under unbalanced conditions

- a* line-neutral voltages of the bus without compensation
- b* line-neutral voltages of the bus with compensation
- c* negative component of bus voltages with compensation and without compensation
- d* phase currents of the STATCOM with compensation

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Fig. 3-20. Simulated frequency spectra under unbalanced conditions

- a* Simulated frequency spectrum of the A-phase current of the STATCOM
- b* Simulated frequency spectrum of the A-phase line-neutral voltage of the bus
- c* Simulated frequency spectrum of the reference voltage of the A-phase inverter
- d* Simulated frequency spectrum of the B-phase current of the STATCOM
- e* Simulated frequency spectrum of the B-phase line-neutral voltage of the bus
- f* Simulated frequency spectrum of the reference voltage of the B-phase inverter
- g* Simulated frequency spectrum of the C-phase current of the STATCOM
- h* Simulated frequency spectrum of the C-phase line-neutral voltage of the bus
- i* Simulated frequency spectrum of the reference voltage of the C-phase inverter

3.5 Experimental results

To verify the performance of the proposed compensator experimentally, a hardware prototype has been built in the laboratory using the scaled system parameters as shown in Table 3-1. For the experimental system, a programmed ac source is used to represent the voltage source of the system. The STATCOM consists of a three-phase nine-level MOSFET inverter which is controlled using a TMS320F240 controlled card, and three inductances.

TMS320F240 has 16 multiplexed analog input channels and 26 digital I/O. Four analog input channels share pins with four digital I/O. Twelve analog input A/D are used to sample three-phase currents, three phase AC side voltages and six DC cap voltages. Twelve digital outputs trigger the power semiconductors in six H-bridges. One digital signal controls two power semiconductors in a leg through a simple dead-time circuit. Photo couplers, like TLP 250, drive the power MOSFETs and protect the control circuit in low power side. DSP interrupt service routine runs at 10K Hz to satisfy the accuracy of Phase Lock Loop and support higher bandwidth of STATCOM controller. There are several program blocks in the interrupt service routine: Phase Lock Loop Block, Park Transformation Block, Inverse Park Transformation Block, PI Update Block, Low Pass Filter Block, COS Function Block, Step Modulation Block and Protection Block.

Fig. 3-21 shows the output voltages of A-phase, B-phase and C-phase inverters and the phase currents. From 0 to 20 ms, the reference value of reactive power that the STATCOM sends is set as zero. At 20 ms, there is a step-change of the reference value of reactive power from 0 to 850 VAr and it is called the inductive mode. For output voltage of the inverter, the high voltage pulses are narrow and the low voltage pulses are wide, which results in smaller value of fundamental component. At 60 ms, there is a step change of the reference value from 850 VAr to -850 VAr, which means that the STATCOM enter the capacitive mode. For output voltage of the inverter, the low voltage pulses are narrow and the high voltage pulses are wide, which means that the fundamental component of the output voltage of the inverter is larger. The results show excellent dynamic response to the step changes.

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Fig. 3-21. Experimental waveforms of the STATCOM under balanced conditions

From 0 to 20 ms, the reference value of reactive power that the STATCOM sends is zero; from 20 ms to 60 ms, the reference value is 850 Var; from 60 ms to 100 ms, the reference value is -850 Var.

a CH1: Output voltage of the A-phase inverter (200V/div); CH2: A-phase current of the STATCOM (1A/div)

b CH1: Output voltage of the B-phase inverter (200V/div); CH2: B-phase current of the STATCOM (1A/div)

c CH1: Output voltage of the C-phase inverter (200V/div); CH2: C-phase current of the STATCOM (1A/div)

Fig. 3-22 shows the line-to-line bus voltages without compensating unbalanced voltages.

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Fig. 3-22. Experimental waveforms of the STATCOM under unbalanced conditions without compensation

From 0 to 40 ms and from 120 ms to 200 ms, the source voltages are balanced; from 40 ms to 120 ms, the source voltages are unbalanced.

a CH1: AB line-to-line voltage of the bus (200V/div); CH2: BC line-to-line voltage of the bus (200V/div)

b CH1: CA line-to-line voltage of the bus (200V/div)

Fig. 3-23 shows the line-to-line bus voltages and phase currents of the STATCOM with compensation of unbalanced voltages. From 0 to 40 ms and from 120 ms to 200 ms, the source voltages are balanced. From 40 ms to 120 ms, the source voltages are unbalanced with 0.25 p.u. negative sequence voltage components added. As shown in Fig. 3-23, with the help of STATCOM, the bus voltages are partially balanced. The extent of compensation is constrained by the current rating of the STATCOM. The A phase current is distorted by the negative sequence component. The B and C phase currents increase a lot because of negative sequence component added.

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Fig. 3-23. Experimental waveforms of the STATCOM under unbalanced conditions with compensation

From 0 to 40 ms and from 120 ms to 200 ms, the source voltages are balanced; from 40 ms to 120 ms, the source voltages are unbalanced.

a CH1: AB line-to-line voltage of the bus (200V/div); CH2: A-phase current of the STATCOM (1A/div)

b CH1: BC line-to-line voltage of the bus (200V/div); CH2: B-phase current of the STATCOM (1A/div)

c CH1: CA line-to-line voltage of the bus (200V/div); CH2: C-phase current of the STATCOM (1A/div)

3.6 Summary

The application of the THMI in STATCOM with unbalanced voltages is investigated, which is cost-effective because of reduced cost of switching components, cooling systems and dc capacitors. The step modulation strategy permits the inverter run at lower frequency. Vector control based on synchronous frame transform lead to high dynamic performance of STATCOM. Moreover, the bus voltages are rebalanced during the unbalanced conditions and the compensation current is limited within normal values. The new method by which the switching signals are generated from the reference inverter voltages is based on the comparison of amplitudes instead of angles. By this method, the output voltage of inverter does not contain lower-order harmonics under stable balanced conditions and the inverter can keep high dynamic performance under unbalanced conditions or transient processes.

Chapter 4 81-Level THMI for Motor Drive with Zero Common-Mode Voltage

4.1 Introduction

Multilevel inverters have been widely applied in motor drives. Diode-clamped three-level multilevel inverters are now widely applied in medium-voltage (2.3 kV, 3.3 kV, 4.16 kV, and even 6 kV) application [67]. A seven-level cascade multilevel inverter is used in non-regenerative drives in 2.3 kV network [8]. Tolbert, et. al [68] presents a transformerless multilevel inverter as an application for high-power electric vehicle (HPEV) motor drives. A hybrid seven-level inverter is applied in 4.16 kV system, in which the top HB uses IGBT and the low one uses GTO [14].

The asymmetric hybrid multilevel inverter is a very attractive topology for motor drive, since it can synthesize more output voltage levels with the same number of components. Among the topologies of hybrid multilevel inverters, the THMIs can synthesize the most output voltage levels [10, 11]. However, the THMI has a problem for the application of motor drive, as mentioned in section 2.4. Controlled rectifiers can be used to transmit the regenerative power. However, with rectifiers, the dc voltages still have larger fluctuation, which will result in the severe decrease of power quality of the inverter. It is also possible to use independent output transformers with a common dc supply. However, this method also leads to larger fluctuation. Another disadvantage is that the low-frequency transformers are bulky.

Conventional two-level pulse width modulated (PWM) inverters and multilevel PWM inverters generate common-mode voltage within the motor windings which may result in motor and drive application problems [106]. The common-mode voltage causes excessive bearing currents that may cause premature motor bearing failures and causes a much larger common-mode leakage current to flow into the ground. It will also cause significant common-mode electromagnetic interference (EMI) emission.

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In this chapter, a THMI for motor drive is proposed. The bi-directional dc-dc converters used as dc sources of the HBs result in stable voltages and permit bi-directional transmission of power. A low-frequency space vector modulation method (SVM) is used to control the inverter and eliminate the common mode voltages. The vector control technique is applied to control motor.

4.2 Power circuit topology

Fig. 4-1 shows the power circuit topology of the THMI for motor drive.

Fig. 4-1. Power circuit topology of the THMI for motor drive

To get maximum output voltage levels of the inverter, the ratio of dc source voltages is arranged as 1:3:9:27, so the inverter can output 81 voltage levels each phase. The operation of THMI is specified in section 2.1. Bi-directional DC-DC converters supply DC links of H-bridges. All DC-DC converters are fed by a rectifier based on assumption that the power of motor is not reversible. If the motor need operate in regenerative mode, the rectifier needs to be replaced by a controlled bridge rectifier.

4.3 Space vector modulation method

$v_{G,a}$, $v_{G,b}$ and $v_{G,c}$ are the voltages of terminals a , b and c of the inverter with respect to the neutral n . Three-phase inverter output voltages can be represented by a space vector in an x - y plane using the following transformation:

$$v = v_x + j \cdot v_y = \frac{2}{3} \cdot (v_{G,a} + a \cdot v_{G,b} + a^2 \cdot v_{G,c}) \quad (4.1)$$

where

$$a = \frac{-1}{2} + j \frac{\sqrt{3}}{2} \quad (4.2)$$

Equation (4.1) can be expressed as a function of their real and imaginary components:

$$v_x = \frac{1}{3} \cdot (2 \cdot v_{G,a} - v_{G,b} - v_{G,c}) \quad (4.3)$$

$$v_y = \frac{1}{\sqrt{3}} (v_{G,b} - v_{G,c}) \quad (4.4)$$

Each phase can generate 81 different voltages. Therefore, the three-phase has a total $81 \times 81 \times 81 = 531441$ different combination of output voltages. Totally

$2 \times 81 - 1 + \sum_{i=81}^{160} 2i = 19441$ different voltage vectors can be generated as shown Fig. 4-2.

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Fig. 4-2. Voltage vectors of a three-phase 81-level inverter

The common-mode voltage is defined as

$$v_{cm} = \frac{1}{3}(v_{G,a} + v_{G,b} + v_{G,c}) \quad (4.5)$$

Considering this definition, we can find vectors generated by three phase voltages, which produce zero common-mode voltage as shown in Fig. 4-3. The use of only vectors that generate zero common-mode voltages to the load reduces the density of vectors available to be applied, but there are still $(80 + 41) \times 40 + 81 = 4921$ different voltage vectors available.

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Fig. 4-3. Voltage vectors of a three-phase 81-level inverter with zero common-mode voltage

The nearest voltage vector in Fig. 4-3 with respect to the reference vector v_{ref} is delivered. The following algorithm is used to select the appropriate vector based on the information of the reference vector.

Step 1. Normalize the reference vector $v_{ref} = v_{xref} + jv_{yref}$

$$v'_{ref} = \frac{v_{xref}}{E} + j \frac{\sqrt{3}v_{yref}}{E} = x + jy \quad (4.6)$$

Step 2. Normalize the candidate space vector with the transformation (4.6), converting them into integer values. After conversion, the space vectors with zero common-mode voltage are shown in Fig. 4-4.

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Fig. 4-4. Normalized voltage vectors of a three-phase 81-level inverter with zero common-mode voltage

Step 3. v'_{ref} will lie in one of rectangles defined by two normalized candidate space vectors. The rectangle is identified by the values of left-bottom point of the rectangle. $v'_{ref}(x, y)$ lies in the rectangle $(\text{floor}(x), \text{floor}(y))$, where $\text{floor}(\alpha)$ is the function that rounds the elements of α to the nearest integer that is less than or equal to α . In the rectangle $(\text{floor}(x), \text{floor}(y))$, there are two normalized voltage vectors, $(\text{floor}(x), \text{floor}(y))$ and $(\text{floor}(x)+1, \text{floor}(y)+1)$, if the addition of $\text{floor}(x)$ and $\text{floor}(y)$ is even. Two vectors are $(\text{floor}(x)+1, y)$ and $(x, \text{floor}(y)+1)$, if the addition of $\text{floor}(x)$ and $\text{floor}(y)$ is odd. Suppose the reference vector, $v'_{ref}(x, y)$, and lies in the rectangle with two normalized voltage vectors, v_1 and v_2 . The nearest vector is selected by comparing the distances of each candidate vector, v_1 and v_2 , with respect to v'_{ref} , using the following equations:

$$d_1 = \sqrt{(3 \cdot (x - \text{Re}(v_1)))^2 + (y - \text{Im}(v_1))^2} \quad (4.7)$$

$$d_2 = \sqrt{(3 \cdot (x - \text{Re}(v_2)))^2 + (y - \text{Im}(v_2))^2} \quad (4.8)$$

The selection is done by

$$\begin{aligned} \text{if } d_1 < d_2 \text{ then } v_{sel} &= v_1 \\ \text{else } v_{sel} &= v_2 \end{aligned} \quad (4.9)$$

Step 4. Three-phase output voltages with zero common-mode voltage are generated by an inverse transformation for v_{sel} as:

$$\begin{aligned}
v_{G,a} &= \text{round}(\text{Re}(v_{rel})) \\
v_{G,b} &= v_{G,a} + \frac{\text{Im}(v_{sel}) - 3 \times \text{Re}(v_{rel})}{2} \\
v_{G,c} &= v_{G,a} + \frac{-\text{Im}(v_{sel}) - 3 \times \text{Re}(v_{rel})}{2}
\end{aligned} \tag{4.10}$$

4.4 DC sources of H-bridges

There are three reasons why dc sources of HBs are bidirectional dc-dc converters in the proposed topology.

The first reason is the bidirectional dc-dc converter can transfer the regenerative power from the HB to the rectifier. The phenomenon of regenerative power in THMI is described in section 2.4.

The second reason is that variation of dc link voltage of a HB is required to be very small. For example, the variation of dc link voltage of the HB with dc link voltage of $27E$ must be less than $0.5/27 = 0.019$. Otherwise, the contribution of the HB with dc link voltage of E for the power quality will be almost nothing. The dc-dc converters with high band-width close loop control can stabilize the dc link voltages of HBs.

The third reason is that transformers used in bidirectional converters are small, cost-effective and high efficient. In other topologies of hybrid multilevel inverters for motor drives, the output ports of HBs are connected together by transformers. However, these low-frequency transformers are bulky and low efficient. Compared with the configurations with low-frequency transformers, the efficiency of the dc-dc converter is higher. The efficiency of the dc-dc converter measured in the low power experiments is around 90%. In practical high power application, that can reach 97%, which is much higher than that of the traditional configuration of low-frequency transformers and rectifiers.

The topology of bidirectional dc-dc converter is shown in Fig. 4-5. The transformer provides galvanic isolation between the input and the output. The primary side of the converter is a half bridge and is connected to the dc link of rectifier. The secondary side,

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connected to the dc link of the HB, forms a current-fed push-pull. The converter has two modes of operation. In the forward mode, the dc link of an HB is powered by the dc link of the rectifier. In the backward mode, the dc link of an HB provides the energy to the dc link of rectifier.

Fig. 4-5. bidirectional dc-dc converter

Left part of Fig. 4-6 shows the idealized waveforms in the forward mode. *Interval $t_0 - t_1$* : Switch S_2 is off and S_1 is on at time t_0 . A voltage across the primary winding is $v_{Cr}/2$. The body diode of switch S_4 , D_{S4} , is forward biased. The current flow through S_1 , i_{S1} , contributes to the linearly increasing inductor current and the transformer primary magnetizing current. *Interval $t_1 - t_2$* : Switch S_1 is turned off at time t_1 and S_2 remains on. No power is transferred to the secondary side during this dead time interval since there is zero voltage across the primary. The energy stored in L_o results in the freewheeling of the current i_{Lo} , equally through the body diodes D_{S3} and D_{S4} . *Interval $t_2 - t_3$* : Switch S_2 is turned on at time t_2 and S_1 remains off. The operation is similar to that during interval $t_0 - t_1$, but now D_{S3} conducts and provides secondary side rectification. Inductor current rises linearly again. *Interval $t_3 - t_4$* : Switch S_2 is turned off at time t_2 and S_1 remains off. The operation is similar to that in the interval $t_1 - t_2$. Fig. 4-5 shows a balancing winding N_{p1} and two diodes D_1 and D_2 on the primary side of the half bridge. They maintain the center point voltage at the junction of C_1 and C_2 to one-half of the input voltage and prevent a runaway condition of staircase situation of the transformer core. N_{p1} has the same number of turns as the winding N_p and is phrased in series with it through the on time of S_1 and S_2 .

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Fig. 4-6 Waveforms of bidirectional dc-dc converter during the forward/backward mode

In the backward mode, the switch S_3 and S_4 of the current-fed push-pull topology are driven at duty ratios greater than 0.5. The converter operation during this mode is shown in the right part of Fig. 4-6. *Internal $t_0 - t_1$:* Switch S_3 is turned on and S_4 remain on at time t_0 . N_s is subject to a short circuit, which causes the inductor L_o to store energy as the dc link voltage of the HB appears across it. i_{Lo} ramps up linearly and is shared equally by both S_3 and S_4 . During this interval, C_1 and C_2 provide the output power. *Internal $t_1 - t_2$:* Switch S_4 is turned off and S_3 remains on at time t_1 . The energy stored in the inductor during the previous interval is now transferred to the load through D_{S2} and D_1 . Voltages across N_{p1} and N_p are identical due to their series phasing and equal number of turns. This allows simultaneous and equal charging of both C_1 and C_2 through D_1 and D_{S2} , respectively. *Internal $t_2 - t_3$:* Switch S_4 is turned on and S_3 remains on at time t_2 . This interval is similar to the internal $t_0 - t_1$. The duty ratio for S_3 is therefore greater than 0.5. *Internal $t_3 - t_4$:* Switch S_3 is turned off and S_4 remain on at time t_3 . The stored energy of L_o is transferred to the primary side of the converter through S_4 , D_{S1} and D_2 . The conduction of D_{S1} and D_2 results in equal charging of C_1 and C_2 , respectively.

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Current mode control is used for both modes of converter operations. Small signal analysis for both modes under mode control is performed to generate the transfer functions to design and evaluate the control loop. In the forward mode, the control-to-output transfer function is shown as

$$\frac{\hat{v}_{C_H}}{\hat{v}_{cf}} = G_{cf} \cdot \frac{1 + \frac{s}{w_z}}{1 + \frac{s}{w_L / p_1} + \frac{s^2}{w_L w_c / p_1}} \quad (4.11)$$

where

$$G_{cf} = \frac{\frac{4L_o}{R_s T_s}}{(1 + \frac{2M_c}{M_1})(1 - D_f) - D_f + \frac{4L_o}{RT_s}}$$

$$p_1 = \frac{[(1 + \frac{2M_c}{M_1})(1 - D_f) - D_f] \cdot r + \frac{4L_o}{T_s}}{[(1 + \frac{2M_c}{M_1})(1 - D_f) - D_f] \cdot R + \frac{4L_o}{T_s}}$$

$$w_L = \frac{1}{(R + r) \cdot C_o} \quad w_z = \frac{w_L R}{r}$$

$$w_c = \frac{r \cdot (1 - \frac{D_f}{1 - D_f} \cdot \frac{M_1}{M_1 + 2M_c})}{L_o} + \frac{4f_s}{1 - D_f} \cdot \frac{M_1}{M_1 + 2M_c}$$

r is equivalent series resistor of C_o ; R is output operating point; R_s is the ratio of voltage for comparing to switch current; M_1 is inductor current slope during switch on time and M_c is slope of compensating ramp.

In the backward mode, the control-to-output transfer function is shown as

$$\frac{\hat{v}_{C_r}}{\hat{v}_{cb}} = G_{cb} \cdot \frac{1 - \frac{s}{w_{z2}}}{1 + \frac{s}{w_L / p_a} + \frac{s^2}{w_L w_c / p_b}} \quad (4.12)$$

where

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$$G_{cb} = \frac{16L_o[NR(1-D_{ov})-2r_e]}{RR_sT_s[\frac{64L_o}{RT_s} + (1+\frac{2M_c}{M_1})N^2(1-D_{ov})^3]}$$

$$C_a = \frac{\frac{32L_o}{T_s} + (1+\frac{2M_c}{M_1})r_eN^2(1-D_{ov})^2}{R[\frac{64L_o}{RT_s} + (1+\frac{2M_c}{M_1})N^2(1-D_{ov})^3]}$$

$$C_b = \frac{\frac{16L_o}{T_s} + (1+\frac{2M_c}{M_1})r_eN^2(1-D_{ov})^2}{2R[\frac{32L_o}{RT_s} + (1+\frac{2M_c}{M_1})N^2(1-D_{ov})^3]}$$

$$w_L = \frac{1}{(R+r_e) \cdot C_e}$$

$$w_{z1} = \frac{4L_o + r_eRC_eN(1-D_{ov})}{N(1-D_{ov})[2r_e - RN(1-D_{ov})]}$$

$$w_c = \frac{r_e \cdot N^2(1-D_{ov})}{4L_o} + \frac{2f_s}{1-D_{ov}} \cdot \frac{M_1}{M_1+2M_c}$$

D_{ov} is the overlap interval in each half switching period for S_3 and S_4 . r_e is *esr* of equivalent capacitance of C_1 and C_2 .

The compensators of output voltage controllers for both modes are shown as (4.13) and (4.14)

$$A_f = \frac{R_{f,f}}{R_{in,f}(1+sR_{f,f}C_{f,f})} \quad (4.13)$$

$$A_b = \frac{R_{f,b}}{R_{in,b}(1+sR_{f,b}C_{f,b})} \quad (4.14)$$

where R_f and R_{in} are feedback resistor and input resistor, and C_f is feedback path capacitor.

4.5 Motor controller

The proposed multilevel inverter is used to feed an induction motor. Vector control technique is applied in the motor controller. Vector control implies independent control of

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flux-current and torque/current components of stator current through a coordinated change in the supply voltage amplitude, phase and frequency. As the flux variation tends to be slow, constancy of flux should produce a fast torque/current response and finally fast speed (position) response.

The controller is shown in Fig. 4-7 and the current decoupling network in the controller is shown in Fig. 4-8. To simplify the current decoupling network, the rotor flux orientation is used in the current decoupling network. Once the reference d-q current i_{da}^* , i_{qa}^* and flux orientation angle $\theta_{er} + \gamma_a^*$ are known, the dc current controllers are used to translate these commands to v_{da}^* and v_{qa}^* , and use Park transformation to translate v_{da}^* and v_{qa}^* to v_α^* and v_β^* . The output signal of the motor controller, v_α^* and v_β^* , will be sent to the inverter controller to control the multilevel inverter to provide the appropriate voltages to feed the motor.

Fig. 4-7. Motor controller

Fig. 4-8. Current decoupling network

4.6 Simulation and experimental results

The performance of the 81-level THMI for motor drive presented above has been verified by simulation. The simulation investigations were performed with MATLAB Simulink.

The unit voltage of the multilevel inverter, E , is set as 8V. The modulation index is define as

$$M = \frac{P |v_{an}|_1}{4 \times 40E} \quad (4.15)$$

where $|v_{an}|_1$ is the fundamental amplitude of output phase voltage. Based on the simulation results, the relationship between $|v_{an}|_1$ and modulation index is shown in Fig. 4-9. In the range of very low modulation index, it does not have a very good linear relationship. However, due to a great number of voltage steps, the relationship becomes satisfied linear with higher modulation index.

Fig. 4-9. Amplitude of phase voltage versus modulation index

At 1 ms, there is a command of step change of reference speed from 1430 to 715 rpm when the inverter drives an induction motor. Fig. 4-10 shows simulation results of speed, output phase voltage of the inverter, output phase current of the inverter, dc link voltages of HBs in the A-phase and the common-mode voltages. The speed has a rapid response. During the transient process from 1s to 1.05s, DC-link voltages has ripples due to large values of higher frequency components of the currents. The common mode voltage is very small except during the short transition time. Total harmonic distortion (THD) of output voltage is as low as 1%. Fig. 4-11 shows the detailed waveforms of output voltage

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of inverters. Fig. 4-12 shows the simulation results of torque, output voltages and output currents of the inverter, when the reference torque has step change from 1.29 Nm to 7.74 Nm. The motor drive system also has a good dynamic response for the step change of torque.

Fig. 4-10. Simulation waveforms for a step change of speed

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Fig. 4-11. Simulation waveforms of output voltages of the inverter

Fig. 4-12. Simulation waveforms for a step change of torque (T from 1.29 Nm to 7.74 Nm)

To verify the performance of the proposed inverter experimentally, a hardware prototype has been built in the laboratory. The experimental setup of the proposed control

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system consists of a 3-phase, 380 V, 50 Hz, 4 pole, 3-kW induction motor and power circuit using THMI. The inverter and motor are controlled using TMS320F240 controller cards. One DSP is used to control motor and the other DSP is applied to control the inverter. The DSP for motor drive control sample the three-phase currents and voltages, and generates the three-phase reference voltages for the multilevel inverter. The DSP for the inverter will sample the reference voltages for the multilevel inverter and generate switching sigils for each power MOSFETs through dead-time circuits and gate drive circuits. Current mode controllers of the dc-dc converters are implemented by UC 3846 and UCC 3804, for the forward mode and backward mode, respectively.

Fig. 4-13 and Fig. 4-14 show the waveforms of speed, phase current, phase voltage and line-to-line voltage when the reference speed of motor has a step change. They verify the simulation results as shown Fig. 4-10. Fig. 4-15 and Fig. 4-16 shows the experimental waveforms of dc-link voltages for A phase. They have small ripples during the transiting process. Fig. 4-17 shows the detailed waveforms of phase voltage and common mode voltage. As shown in Fig. 4-17, the phase voltage is synthesized by lots of stable step voltages and the common mode voltage is almost zero.

Fig. 4-13. Experiment waveforms for a step change of reference speed. CH1: phase current (2A/div); CH2: speed (750 rad/s /div)

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Fig. 4-14. Experiment waveforms for a step change of speed. CH1: phase voltage (200V/div); CH2: line-to-line voltage (400V/div)

Fig. 4-15. Experiment waveforms for a step change of speed. CH1: dc link voltage of the first H-bridge in A-phase (2V/div); CH2: dc link voltage of the second H-bridge in A-phase (5V/div)

Fig. 4-16. Experiment waveforms for a step change of speed. CH1: dc link voltage of the third H-bridge in A-phase (20V/div); CH2: dc link voltage of the fourth H-bridge in A-phase (50V/div)

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Fig. 4-17. Experiment detailed waveforms. CH1: phase voltage (100V/div); CH2: common-mode voltage (20V/div)

Fig. 4-18 shows the experimental waveforms off phase current and phase voltages when torque has a step change, which verify the simulation results as shown in Fig. 4-12.

Fig. 4-18. Experiment waveforms for a step change of torque. CH1: phase voltage (200V/div); CH2: phase current (2A/div)

4.7 Summary

A trinary hybrid 81-level multilevel inverter is proposed for motor drive in the paper. The inverter can output 81-level voltages per phase with the fewest components. THD of output voltage is as low as 1%. Bi-directional dc-dc converters are used as the dc links of HBs, which results in stable dc link voltages, whatever the power that flows through the HB is regenerative or not. The space vector modulation can reduce common-mode voltages and leads to precise linearity between the fundamental component and the

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modulation index. Vector controller is used to control induction motor, which results in high dynamic response for speeds or torques.

Chapter 5 A New Hybrid Multilevel Inverter

5.1 Introduction

Previous research described in the thesis covers the existing topologies of hybrid multilevel inverter. Further research focuses on proposal of new topologies of hybrid multilevel inverters whose definition is that the topology of the hybrid multilevel inverter is based on the connection of HBs and capacitor voltage sources whose voltages are asymmetrical in the thesis. Existing topologies of hybrid multilevel inverters are based on series connection of HBs. The difference ratios of dc source voltages of HBs, such as 1:2:4 [14, 15, 35], 1:2:6 [10] and 1:3:9 [10-13], have been presented. Rech, et. al [76] proposed a generalized design methodology for hybrid multilevel inverters based on series connection of HBs. It has been difficult to find new valuable topologies of hybrid multilevel inverters only by changing the ratio of dc source voltages. The chance of new topologies lies in the different ways that HBs and capacitor voltage sources are connected.

In this chapter, a new hybrid multilevel inverter based on a special connection of HBs and capacitor voltage sources is proposed. It can work in three operation modes: single-direction-balance mode, bi-direction-balance mode and non-balance mode. Only a dc source is required when the inverter works in single-direction-balance mode or bi-direction-balance mode. Compared with other topologies that require only a dc source, the new inverter requires fewer components and the number of output voltage levels of the new inverter can be great. Moreover, the new inverter has the ability of self voltage balancing without any assistance from other circuits regardless of active or reactive power conversion, just like the generalized multilevel inverter. At the same time, the new inverter has ability of voltage boosting, which means that low dc input voltage can result in high ac output voltage. This characteristic implies that the new inverter be a good choice in the application of fuel cells. The last important merit of the new inverter is that most of switches switch at zero-voltage conditions, which make the new inverter suitable in high-frequency application. The new inverter that works in single-direction-balance

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mode or bi-direction-balance mode is expected to work in low power application. If the application of the new inverter is extended to high power application, the multiple dc sources are required and non-balance mode is applied. Another solution for high power application is that the inverter works in single-direction-balance mode but with modified dc source voltages. The comparison among the new multilevel inverter and other multilevel inverters, the switching losses in the new inverter and energy losses during self voltage balancing are also discussed. The performance of the proposed inverter is confirmed by simulation and experiment.

5.2 New multilevel inverter

5.2.1 General Topology

Fig. 5-1 shows the general topology of the new multilevel inverter. This single-phase multilevel inverter consists of several HBs (HBs). Dashed line circled dc sources are optional according to operation modes of the inverter, which will be specified in following sections. $v_{in,i}$ and $v_{out,i}$ represent the input voltage and output voltage of the i th HB, HB_{*i*}, respectively. A switching function, F_i , is used to relate the input quantity to the output quantity as

$$v_{out,i} = F_i \cdot v_{in,i} \quad (5.1)$$

The Relationship between the switching function, output voltage of a HB and states of switches are shown in Table 2-1.

Fig. 5-1. General topology of the new multilevel inverter

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Suppose E is unit voltage. The voltage of dc capacitor of HB_{*i*}, v_{Ci} , is expressed as

$$v_{Ci} = \begin{cases} E & i = 1 \\ 2^{i-2} E & i = 2 \mathbf{L} m \end{cases} \quad (5.2)$$

The output voltage of the inverter, v_{an} , is represented as

$$v_{an} = E \times \prod_{k=1}^m F_k + E \times \prod_{k=2}^m F_k + 2E \times \prod_{k=3}^m F_k + \mathbf{L} + 2^{m-2} E \times \prod_{k=m}^m F_k \quad (5.3)$$

v_{an} reaches the maximum value $2^{m-1}E$ when the values of all switching functions are 1 and v_{an} reaches the minimum value $-2^{m-1}E$ if they are -1. The output voltage of the inverter has $(2^m + 1)$ levels. To explain the operating principle and analyze the circuits, a three-HB single-phase inverter that can output nine voltage levels is used in the following sections. There are three sorts of operation modes of the new multilevel inverter: single-direction-balance mode, bi-direction-balance mode and non-balance mode. The inverter has a little difference in configuration of dc sources corresponding to each operation mode.

5.2.2 Single-direction-balance Mode

In single-direction-balance mode, only the capacitor of HB₁, C_1 , is supplied by a dc source whose voltage is E as shown in Fig. 5-2. The voltages of other dc capacitors are maintained by self voltage balancing. The load that the inverter feeds is a non-regenerative load.

Fig. 5-2. Topology of a three-HB new inverter for the single-direction-balance mode or the bi-direction-balance mode

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The voltage of C_2 , v_{C2} , is balanced when S_{12} and S_{13} are turned on. Suppose that the initial voltages of v_{C1} and v_{C2} are E . After the inverter supplies energy to a non-regenerative load, v_{C2} will be less than E , but v_{C1} is maintained as E by the dc source. When S_{12} and S_{13} are turned on, because v_{C1} is larger than v_{C2} , the current flows from the positive pole of the dc source and the C_1 , then through S_{13} and C_2 , then through D_{22} and D_{21} or D_{24} and D_{23} , then through S_{12} , then back to the negative pole of the dc source and the C_1 . The equivalent circuit is shown in Fig. 5-3. In this way, the dc source and the C_1 supplies energy to the C_2 , and the v_{C2} is kept stable.

Fig. 5-3. Equivalent circuit during balancing C_1 and C_2 in the single-direction-balance mode

The v_{C2} decreases when the C_2 supplies energy to the load or increases when the C_2 is supplied energy by the C_1 and the dc source. Suppose the v_{C2} fluctuates between $V_{C2,L}$ and $V_{C2,H}$ as shown in Fig. 5-4. If the C_2 is charged for a infinite time with no load, v_{C2} will reach the maximum value, $V_{C2,max}$. The voltage of the dc source is E , so $V_{C2,max}$ can be expressed as

$$V_{C2,max} = E - 2V_D \quad (5.4)$$

where V_D is forward voltage of diodes. As mentioned, the load is non-regenerative and the C_2 supplies energy to the load. For simplicity, the load current that flows through the C_2 is averaged and expressed as $i_{C2,av}$. Suppose the v_{C2} is $V_{C2,L}$ before the C_2 is charged. After the C_2 is charged, the v_{C2} is $V_{C2,H}$ and can be expressed as

$$V_{C2,H} = V_{C2,max} (1 - e^{-t_c/T_2}) + V_{C2,L} e^{-t_c/T_2} - \frac{i_{C2,av} t_c}{C_2} \quad (5.5)$$

where t_c is charging time and T_2 is time constant of the circuit as shown in Fig. 5-3. The T_2 can be expresses as

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$$T_2 = 2R_M C_2 \quad (5.6)$$

where R_M is the on-state resistance of the switch. After the procession of charging of the C_2 is finished, the v_{C2} begins to decrease. Suppose t_p is the cycle of fluctuation of the v_{C2} . After $(t_p - t_c)$, the v_{C2} reaches minimum value, $V_{C2,L}$, which can be expressed as

$$V_{C2,L} = V_{C2,H} - \frac{i_{C2,av}(t_p - t_c)}{C_2} \quad (5.7)$$

From (5.4), (5.5) and (5.7),

$$V_{C2,H} = E - 2V_D - \frac{i_{C2,av}t_c}{C_2} - \frac{i_{C2,av}t_p e^{-t_c/T_2}}{C_2(1 - e^{-t_c/T_2})} \quad (5.8)$$

$$V_{C2,L} = E - 2V_D - \frac{i_{C2,av}t_p}{C_2(1 - e^{-t_c/T_2})} \quad (5.9)$$

The difference between $V_{C2,H}$ and $V_{C2,L}$, ΔV_{C2} , can be derived from (5.8) and (5.9).

$$\Delta V_{C2} = \frac{i_{C2,av}(t_p - t_c)}{C_2} \quad (5.10)$$

The difference between $V_{C2,max}$ and $V_{C2,L}$, $\Delta V_{C2,max}$, can be derived from (5.4) and (5.9).

$$\Delta V_{C2,max} = \frac{i_{C2,av}t_p}{C_2(1 - e^{-t_c/T_2})} \quad (5.11)$$

ΔV_{C2} must be small for stable output voltage level, and $\Delta V_{C2,max}$ must be small for small difference between output voltage levels. The value of t_p and t_c is determined by the frequency and the modulation strategies and the value of $i_{C2,av}$ is determined by the load. Large value of the C_2 can lead to small ΔV_{C2} . But large value of the C_2 also suggests that large value of the T_2 , which result in large value of $\Delta V_{C2,max}$. So, the values of the C_2 must be selected carefully to achieve the required quality of output voltage of the inverter.

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Fig. 5-4. Waveform of the V_{C2}

The voltage of C_3 , v_{C3} , is balanced when S_{11} , S_{14} , S_{22} and S_{23} are turned on. Suppose initial voltages of v_{C1} , v_{C2} and v_{C3} are E , E and $2E$, respectively. After the inverter supplies energy to a non-regenerative load, the addition of v_{C1} and v_{C2} will be larger than v_{C3} , since v_{C1} is maintained as E by the dc source and v_{C2} is maintained by the method as shown in Fig. 5-3. When S_{11} , S_{14} , S_{22} and S_{23} are turned on, the current flows from the positive pole of the dc source and the C_1 , then through S_{11} , S_{23} and C_3 , then through D_{32} and D_{31} or D_{34} and D_{33} , then through S_{22} , C_2 and S_{14} , then back to the negative pole of the dc source and the C_1 . The equivalent circuit is shown in Fig. 5-5. In this way, v_{C3} is kept stable. The v_{C3} has similar fluctuation as the v_{C2} . Likewise, the quality of output voltage is regulated by selecting the value of the C_3 carefully.

Fig. 5-5. Equivalent circuit during balancing C_1 , C_2 and C_3 in the single-direction-balance mode

The v_{C2} is balanced if S_{12} and S_{13} are turned on, i.e., the value of the switching function, F_1 , is -1. The v_{C3} is balanced if S_{11} , S_{14} , S_{22} and S_{23} are turned on, i.e., F_1 is 1 and F_2 is -1. To balance the v_{C2} and v_{C3} , the state in which F_1 is -1 and the state in which F_1 is 1 and F_2 is -1 must last a certain time periodically. Fig. 5-6 shows the diagram of state transition

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and Table 5-1 shows the values of switching functions for difference states. With state l_x , the inverter outputs the positive l th level of voltage if l is not negative, and the inverter outputs the negative $(-l)$ th level of voltage if l is negative. In states $2_h, 2_s, 2_l, -2_h, -2_s$ and -2_l , the v_{C2} is balanced. In states $0_h, 0_s$ and 0_l , the v_{C3} is balanced. In other words, the v_{C2} is balanced when the inverter outputs the second level or the negative second level of voltage, and the v_{C3} is balanced when the inverter outputs zero voltage.

Another important merit is that the switches of HB₂ and HB₃ switch at zero voltage conditions. Firstly, the switching of the switches of HB₃ is analyzed. From Table 5-1, one can find out that the switches of HB₃ switch at the transitions among states ($0_h \leftrightarrow 0_s \leftrightarrow 0_l$). In these three states, F_1 is 1 and F_2 is -1, so the input voltage of HB₃, $v_{in,3}$, can be expressed as

$$v_{in,3} = E + v_{C2} - v_{C3} \quad (5.12)$$

Fig. 5-6. State diagram of a three-HB inverter in single-direction-balance mode

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Table 5-1 Values of switching functions for different states

Single-direction-balance mode				Bi-direction-balance mode				Non-balance mode			
State	F ₁	F ₂	F ₃	State	F ₁	F ₂	F ₃	State	F ₁	F ₂	F ₃
4	1	1	1	4	1	1	1	4	1	1	1
3	0	1	1	3	0	1	1	3	0	1	1
2 _h	-1	1	1	2 _h	-1	1	1	2 _N	0	0	1
2 _S	-1	0	1	2 _B	-1	0*	1				
2 _l	-1	-1	1	2 _l	-1	-1	1				
1	0	-1	1	1	0	-1	1	1	0	-1	1
0 _h	1	-1	1	0 _h	1	-1	1	0 _N	0	-1	0
0 _S	1	-1	0	0 _B	1	-1	0*				
0 _l	1	-1	-1	0 _l	1	-1	-1				
-1	0	-1	-1	-1	0	-1	-1	-1	0	-1	-1
-2 _h	-1	-1	-1	-2 _h	-1	-1	-1	-2 _N	0	0	-1
-2 _S	-1	0	-1	-2 _B	-1	0*	-1				
-2 _l	-1	1	-1	-2 _l	-1	1	-1				
-3	0	1	-1	-3	0	1	-1	-3	0	1	-1
-4	1	1	-1	-4	1	1	-1	-4	1	1	-1

The $v_{in,3}$ is very small since the v_{C2} is a little lower than E and the v_{C3} is a little lower than $2E$. Therefore, the switches of HB₃ switch at zero-voltage conditions. Secondly, the switching of switches of HB₂ is analyzed. The switches of HB₂ switch at the transition among states ($2_h \leftrightarrow 2_S \leftrightarrow 2_l$, $-2_h \leftrightarrow -2_S \leftrightarrow -2_l$). In these states, F_1 is -1, so the input voltage of HB₂, $v_{in,2}$, can be expressed as

$$v_{in,2} = v_{C2} - E \quad (5.13)$$

The $v_{in,2}$ is very small since the v_{C2} is a little lower than E . Therefore, the switches of HB₂ switch at zero-voltage conditions.

The following is the explanation of the operation principle of the inverter in single-direction-balance mode. To explain it clearly, we use step modulation strategy with which the waveform of output voltage of the inverter is shown in Fig. 5-7. As shown in Fig. 5-7, the transitions after which the output voltage will reach the second level, the negative second level or the 0 level are different from other transitions. Take the example of the transition from the first level output voltage to the second level output voltage. Initial state of the inverter state is 1. When the command that the inverter should output the second level voltage arrives, the state of the inverter transmits from state 1 to state 2_l. As shown in Table 5-1, only the switches in HB₁ switch in this transition. The duration of state 2_l is very short. In fact, shortly after the transition from state 1 to state 2_l is finished

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and the $v_{in,2}$ becomes very small as mentioned above, the transition from state 2_l to state 2 starts. In this transition, the switches of the HB₂ switch at zero-voltage conditions due to tiny value of the $v_{in,2}$. After this transition ends, the transition from state 2 to state 2_h starts immediately. The state 2_h is kept until the next command that the inverter should output the third level voltage arrives. Noticeably, in this complete transition from the first level output voltage to the second level output voltage, a short time slot of the state 2_l ensures that the $v_{in,2}$ drops to a tiny value before switches of HB₂ switch. In similar manner, in the transition from the third level output voltage to the second level voltage, a short time slot of state 2_h ensures that the $v_{in,2}$ decreases to a tiny value before switches of HB₂ switch. Thus, the zero-voltage-switching of switches of HB₂ is achieved. The operation principle of the transitions after which the output voltage will reach 0-level is similar and the switches of HB₃ switch at zero-voltage conditions.

Fig. 5-7. Waveform of output voltage of the inverter with the step modulation strategy in the single-direction-balance mode

5.2.3 Bi-direction-balance Mode

In single-direction-balance mode, the power that flows from the dc source to the C₂ and the C₃ maintains voltages of the C₂ and the C₃. It is effective for a non-generative load. However, if the load is regenerative, the voltage of the C₂ and the C₃ might be much higher than E and $2E$ due to regenerative power, which will decrease the quality of the output voltage, and even damage dc capacitors. The bi-direction-balance mode is presented to solve this problem. The topology of a 3-HB inverter in bi-direction-mode is almost the same as that in single-direction-mode as shown in Fig. 5-2. The only difference is that the C₁ is supplied by a regenerative dc source. The voltages of other

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capacitors are also maintained by self voltage balancing. The voltage balancing in bi-direction-mode is more complex than that with in single-direction-mode presented above. As mentioned, with regenerative load, the v_{C2} might be higher than the v_{C1} and the v_{C3} might be higher than the addition of v_{C1} and v_{C2} . So the inverter must provide the mechanism by which power can flow from the C_2 to the dc source during the voltage balancing of the C_2 , and from the C_3 to the dc source and the C_2 during the voltage balancing of the C_3 . With regenerative load, it is still possible that the v_{C1} is higher than the v_{C2} and the addition of v_{C1} and v_{C2} is higher than v_{C3} . So the inverter still keep the mechanism by which power can flow from the dc source to the C_2 during the voltage balancing of the C_2 , and from the dc source and the C_2 to the C_3 during the voltage balancing of the C_3 . In other word, when the inverter works in bi-direction-balance mode, the transfer of energy between the dc sources and the C_2 and the transfer of energy between the dc sources, the C_2 and the C_3 must be bi-directional.

Firstly, the special state of an HB, 0^* , is introduced. For this state, the switches S_1 and S_2 need to be turned on or S_3 and S_4 need to be turned. If the former switching states are used, Fig. 5-8 shows the HBs with 0^* state, in which the switches with dashed circles are turned on. Before the 0^* state arrives, the input voltage of the HB, v_{in} , must be kept zero, otherwise a huge short-circuit current will occur. If the load current flows into point A, the current flows through S_2 or D_1 , then flows through D_4 to point B. If the load current flows into B point, the current flows through D_3 , then flows through S_1 or D_2 to point A. So output voltage of the HB, v_{out} , is zero. The switching function can be regarded as 0^* due to zero-output-voltage of the HB.

Fig. 5-8. The 0^* state of an HB

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During the voltage balancing of the C_2 , not only the S_{12} and S_{13} need to be turned on, but also after that, the state of HB_2 is set as 0^* . Before the 0^* state of HB_2 , S_{12} and S_{13} are on and the $v_{in,2}$ is very small, so there are no huge short-circuit currents. Suppose the 0^* state of HB_2 is achieved by turning on S_{21} and S_{22} . If the v_{C1} is greater than the v_{C2} , the current flows from the positive pole of the dc source and the C_1 , then through S_{13} and C_2 , then through D_{22} and D_{21} or D_{24} and D_{23} , then through S_{12} , then back to the negative pole of the dc source and the C_1 . It is the same as the voltage balancing of the v_{C2} in single-direction-balance mode. However, if the v_{C1} is lower than the v_{C2} , the current flows from the positive pole of the C_2 , then through D_{13} , then through the C_1 and the regenerative dc source, then through D_{12} , S_{21} and S_{22} , then back to the negative pole of the C_2 . Fig. 5-9 shows the equivalent circuit during the energy transition from the C_2 to the C_1 and the dc source. In this way, the extra energy of the C_2 flows to the C_1 and the regenerative dc source, so the v_{C2} can be limited below the maximum permitted value.

Fig. 5-9. Equivalent circuit during the energy transition from C_2 to C_1 and the dc source in the bi-direction-balance mode

During the voltage balancing of the C_3 , not only the S_{11} , S_{14} , S_{22} and S_{23} need to be turned on, but also after that, the state of HB_3 is set as 0^* . Before the 0^* state of HB_3 , the $v_{in,3}$ is very small, so there are no huge short-circuit currents. Suppose the 0^* state of HB_3 is achieved by turning on S_{31} and S_{32} . If the addition of the v_{C1} and the v_{C2} is greater than the v_{C3} , the current flows from the positive pole of the dc source and the C_1 , then through S_{11} , S_{23} and C_3 , then through D_{32} and D_{31} or D_{34} and D_{33} , then through S_{22} , C_2 and S_{14} , then back to the negative pole of the dc source and the C_1 . It is the same as the voltage balancing of the v_{C3} in single-direction-balance mode. However, if the addition of v_{C1} and the v_{C2} is lower than the v_{C3} , the current flows from the positive pole of the C_3 , then through D_{23} and D_{11} , then through the C_1 and the dc source, then through D_{14} , C_2 , D_{22} , S_{31}

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and S_{32} , then back to the negative pole of the C_3 . Fig. 5-10 shows the equivalent circuit during the energy transition from the C_3 to the C_2 , the C_1 and the dc source.

Fig. 5-10. Equivalent circuit during the energy transition from C_3 to C_2 , the C_1 and the dc source in the bi-direction-balance mode

In fact, in most applications with regenerative load, the inverter supplies energy to the load at most of time. In these times, the inverter can work in single-direction-balance mode. But when the load feeds energy back to the inverter, it is possible that the v_{C1} is lower than the v_{C2} and the addition of v_{C1} and v_{C2} is lower than v_{C3} . In these cases, the inverter should work in bi-direction-balance mode. Fig. 5-11 shows the diagram of state transition in bi-direction-balance mode and Table 3-1 shows the values of switching functions for different states. The only difference between the state diagram in bi-direction-balance mode and that in single-direction-balance load is that the states 2_B , 0_B , and -2_B substitute the states, 2_S , 0_S , and -2_S , respectively. In states 2_B , 0_B , and -2_B , the extra energy of the C_2 and C_3 can feed back to the regenerative dc source. In bi-direction-balance mode, the switches of HB_2 and HB_3 also switch at zero-voltage conditions. The analysis is the same as that in single-direction-balance mode mentioned in the previous section.

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Fig. 5-11. State diagram of a three-HB inverter in the bi-direction-balance mode

When the inverter works in bi-direction-balance mode, if with step modulation strategy, the output voltage of the inverter is shown in Fig. 5-12. As shown in Fig. 5-12, the transitions related with the second level, the negative second level and the 0 level output voltage are different from others. Take the example of the transitions from the first level output voltage to the second level output voltage and the transition from the second level output voltage to the third level output voltage. Initial state of the inverter is 1. When the command that the inverter should output the second level arrives, the state of the inverter transmits from state 1 to state 2_l by the switching of switches of HB₁. Shortly after the transition from state 1 to state 2_l is finished and the $v_{in,2}$ becomes very small, the transition from state 2_l to state 2 starts. The 0^* state of HB₂ would not result in large short-circuit currents due to tiny value of the $v_{in,2}$, which also contribute to zero-voltage switching of switches of HB₂. The inverter remains in the state 2 to balance the v_{C2} until the next command that the inverter should output the third level voltage arrives. Then the state of the inverter transmits from state 2 to state 2_h , in which the switches of HB₂ switch at zero-voltage conditions. After this transition ends, the state of the inverter transmits from state 2_h to state 3 immediately. The short time slots of the states 2_l and 2_h ensure that switches of HB₂ switch at zero-voltage conditions. There are two differences between the operation principle in bi-direction-balance mode and that in single-direction-balance mode. Firstly, during the transitions presented above, the state 2 lasts as long as possible to balance the v_{C2} in bi-direction-balance mode. Secondly, due to the state 2_h , there are a little delay between the instant that the command of the third level output voltage arrives and the instant that the inverter outputs the third level voltage. But the effect of the delay to the performance of the inverter can be ignored due to very short duration of the state 2_h .

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Fig. 5-12. Waveform of output voltage of the inverter with the step modulation strategy in the bi-direction-balance mode

When the inverter feeds a reactive load, the inverter also works in bi-direction-balance mode. No dc source is needed as shown in Fig. 5-13. The summation of the capacitor voltages is regulated by the control of active power. The active power flowing into the inverter will compensate the power losses of devices of the inverter. The voltage of individual capacitor is regulated by the mechanism of self voltage balancing in bi-direction-balance mode presented above. Due to this mechanism, the ratio of the v_{C1} , v_{C2} and v_{C3} can be kept about 1:1:2. Thus, only with the outer active power control, every voltage of dc capacitors can be stabilized at the normal value.

Fig. 5-13. Topology of the three-HB inverter for a reactive load

5.2.4 Non-balance Mode

In single-direction-balance mode and bi-direction-balance mode, only a dc source is needed in a single-phase inverter and the voltages of other capacitors are maintained by mechanism of self voltage balancing mentioned above. The charging or discharging currents of the capacitors for self voltage balancing is much larger than the load current,

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which is not acceptable in some applications, especially in high power applications. So the non-balance mode is presented here to avoid the charging or discharging currents. The topology of the inverter that works in non-balance mode is shown in Fig. 5-14, in which each dc capacitor is supplied by a separate dc source.

Fig. 5-14. Topology of the three-HB inverter in the non-balance mode

Conditions of self voltage balancing are shown in Table 5-2. From Table 5-2, we can derive that an effective way for avoiding the charging or discharging currents for self voltage balancing is to avoid the state in which $F_1=-1$ and the state in which $F_1=1$ and $F_2=-1$. Fig. 5-15 shows the state diagram of a three-HB inverter in non-balance mode and Table 5-1 shows the values of switching functions in the states used in Fig. 5-15. The waveform of the output voltage of the inverter with step modulation strategy in this case is shown in Fig. 5-16.

Table 5-2 Conditions of self voltage balancing

Charging current	Conditions
From C_1 to C_2	$F_1=-1$ and $v_{C1}>v_{C2}$
From C_1 and C_2 to C_3	$F_1=1, F_2=-1$ and $v_{C1}+v_{C2}>v_{C3}$
From C_2 to C_1	$F_1=-1, F_2=0^*$ and $v_{C1}<v_{C2}$
From C_3 to C_1 and C_2	$F_1=1, F_2=-1, F_3=0^*$ and $v_{C1}+v_{C2}<v_{C3}$

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Fig. 5-15. State diagram of the three-HB inverter in the non-balance mode

Fig. 5-16 Waveform of output voltage of the inverter with the step modulation strategy in the non-balance mode

Suppose E is unit voltage, in other words, the v_{C1} is E , the v_{C2} is about E and the v_{C3} is about $2E$. If the inverter works based on the state diagram as shown in Fig. 5-15, the voltages across all switches are about E when they switch. From Table 5-1, we can find out that the switches of HB₃ switch at the transition among the states $(-1 \leftrightarrow 0_N \leftrightarrow 1)$. In these three states, the F_1 is 0 and the F_1 is -1, so the input voltage of HB₃, $v_{in,3}$, can be expressed as

$$v_{in,3} = v_{C3} - v_{C2} \approx E \quad (5.14)$$

The switches of HB₂ switch at the transition among the states $(-3 \leftrightarrow -2_N \leftrightarrow -1, 1 \leftrightarrow 2_N \leftrightarrow 3)$. In these states, the F_1 is 0, so the input voltage of the HB₂, $v_{in,2}$, can be expressed as

$$v_{in,2} = v_{C2} \approx E \quad (5.15)$$

Obviously, the input voltage of HB₁, $v_{in,1}$, is always E . So the input voltage of a HB is about E when the switches of this HB switch in non-balance mode.

5.3 Application of the new multilevel inverter

The application of the new multilevel inverter is shown in Table 5-3. The inverter that works in single-direction-balance mode is suitable in the application with non-regenerative load, especially for higher frequency application. In single-direction-balance mode, the switches of all HBs except HB₁ switch at zero-voltage conditions as mentioned above, so the switching losses of these switches are very small. Moreover, the switching losses of switches in HB₁ can be decreased much by selecting lower-voltage higher-frequency switching components since the voltages that the switches of HB₁ endure are small. Thus, due to fewer switching losses, the inverter in single-direction-balance mode is especially suitable for the high frequency application. In the inverter in single-direction-balance mode, the voltage of the only dc sources is low (E), but the amplitude of the output ac voltage of the inverter is high (about $2^{m-1}E$ where m is the number of HBs). So the new inverter can be used in the application of fuel cells, in which the dc voltage of fuel cells is very low but the required amplitude of output ac voltage might be high. The single-direction-balance mode also can be used in high power application. But to avoid the charging or discharging currents, the following conditions must be satisfied according to Table 5-2.

$$v_{C1} < v_{C2} \quad v_{C1} + v_{C2} < v_{C3} \quad (5.16)$$

In high power application, 5% fluctuation of dc voltages is acceptable. So the ratio of dc source voltages must be $1:\alpha:(1+\alpha)\alpha$ in a three-HB inverter, where α is greater than 105%. Compared with the inverter that works in non-balance mode for high power application, the advantage of this method is that the nearly zero voltage switching of the switches in HB₂ and HB₃ can still be achieved. The disadvantage of this method is that the output voltage levels are not identical.

The inverter that works in bi-direction-balance mode is suitable in low power application with regenerative load, especially for high-frequency application or the application that require higher ac output voltage but with lower dc source voltage, just as discussed above. The inverter that works in bi-direction-balance mode is also suitable in low power application with reactive load, in which no dc source is needed and every voltage of dc capacitor can be stabilized at the normal value only with the outer active

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power control. The inverter that works in non-balance mode can be used in high power application with non-regenerative or regenerative load.

Table 5-3 Application of the new multilevel inverter

Operation mode	Application	Comment
Single-direction-balance mode	Low power application with non-regenerative load	Especially for high-frequency application. Especially for the demand of the higher ac output voltage, but with lower dc source voltage
	High power application with non-regenerative load	Each dc capacitor is supplied by a dc source. And the ratio of voltages of dc sources is $1:\alpha:(1+\alpha)\alpha$, where α is greater than 105%.
Bi-direction-balance mode	Low power application with regenerative load	Especially for high-frequency application. Especially for the demand of the higher ac output voltage, but with lower dc source voltage
	Low power application with reactive load	
Non-balance mode	High-power application with non-regenerative load or regenerative load	

5.4 Simulation results

The performance of the new inverter in different operation modes presented above has been verified by simulation. The simulation investigations were performed with MATLAB Simulink.

The first simulation was implemented to verify the ability of self voltage balancing in single-direction-balance mode and bi-direction-balance mode. The topology is shown in Fig. 5-2 and the switches are MOSFETs. The on-state resistance of the MOSFETs in HB₁, R_{M1} , is 0.077Ω . The on-state resistance of the MOSFETs in HB₂, R_{M2} , is 0.18Ω . The on-state resistance of the MOSFETs in HB₃, R_{M3} , is 0.55Ω . The C_2 is 4.7mF and C_3 is 2.2mF. No load. The voltage of the dc source of HB₁, $v_{in,1}$, increases linearly from 48V to 58V during the time interval from 0.2S to 0.4S and decreases linearly from 58V to 48V during

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the time interval from 0.4S to 0.6S. Fig. 5-17 and Fig. 5-18 show the capacitor voltages when the inverter works in single-direction-balance mode and bi-direction-balance mode, respectively. The capacitor C_1 is supplied by the dc source, so the waveform of v_{C1} is the same as that of the dc source voltage. With single-direction-balance mode and bi-direction-balance mode, the v_{C2} and the half of the v_{C3} follow the v_{C1} when the v_{C1} increases, which means that the v_{C2} and v_{C3} can be balanced if the v_{C1} is a little larger than the v_{C2} and the addition of v_{C1} and v_{C2} is a little larger than the v_{C3} with these two modes. However, only with bi-direction-balance mode, the v_{C2} and the half of the v_{C3} follow the v_{C1} when the v_{C1} decrease, which means that only with bi-direction-balance mode, the v_{C2} and v_{C3} can be balanced if the v_{C1} is a little smaller than the v_{C2} and the addition of v_{C1} and v_{C2} is a little smaller than the v_{C3} . The differences between the v_{C1} , v_{C2} and half of v_{C3} are due to voltage drops of anti-parallel diodes and incomplete charging.

Fig. 5-17. Simulated waveforms of capacitor voltages in the single-direction-balance mode

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Fig. 5-18. Simulated waveforms of capacitor voltages in the bi-direction-balance mode

The second simulation verifies the performance of the inverter working in single-direction-balance mode. The topology is shown in Fig. 5-2 and the switches are MOSFETs. The on-state resistances of MOSFETs and the capacitances of the capacitors are the same as that in the first simulation. The dc voltage of HB₁ is 48V. The RL load is 100Ω and 0.19H. Fig. 5-19 shows the waveforms of capacitor voltages (v_{C2} and v_{C3}), load voltage (v_{an}), load current (i_{an}) and the current flowing through the dc link of HB₁ (i_{C1}). The v_{C2} and v_{C3} are stabilized at 46V and 87V by the self voltage balancing as shown in Fig. 5-19. The maximum absolute value of v_{an} is 181V, which is addition of v_{C1} , v_{C2} and v_{C3} . The maximum absolute value of i_{C1} is 12.5A for balancing the v_{C3} and 9.6A for balancing the v_{C2} , which is about eight times and six times maximum absolute value of the load current, respectively. The efficiency of the inverter in this simulation is about 91%. Fig. 5-20 shows waveforms of switching signals of the switch S₂₁ (SS_{21}), the voltage across the S₂₁ (v_{21}), switching signals of the switch S₃₁ (SS_{31}) and the voltage across the S₃₁ (v_{31}). When the S₂₁ and S₃₁ are turned on or off, the voltages across them, v_{21} and v_{31} are zero as shown in Fig. 5-20, which verifies that the switches of HB₂ and HB₃ switch at zero-voltage conditions.

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Fig. 5-19. Simulated waveforms of capacitor voltages, load voltage, load current and the current flowing through the dc link of HB₁ in the single-direction-balance mode

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Fig. 5-20. Simulated waveforms of signals and voltage of S_{21} and S_{31} in the single-direction-balance mode

The third simulation verifies the performance of the inverter in bi-direction-balance mode. The topology and simulation parameters are the same as those in the second simulation except that an ac source is connected with the load in series. The peak value, phase and frequency of the ac source are 300V, 0° and 50Hz. Thus, the inverter is in regenerative mode. The power is transferred from the ac source to the regenerative dc source of HB₁ through the inverter. Fig. 5-21 shows the waveforms of capacitor voltages (v_{C2} and v_{C3}), load voltage (v_{an}), load current (i_{an}) and the current flowing through the dc link of HB₁ (i_{C1}). The v_{C2} and v_{C3} are stabilized at 51V and 106V by the voltage balancing as shown in Fig. 5-21. The maximum absolute value of v_{an} is 207V, which is addition of v_{C1} , v_{C2} and v_{C3} . The maximum absolute value of i_{C1} is 5.6A for balancing the v_{C3} and 5A for balancing the v_{C2} , which is about seven times and six times maximum absolute value of the load current, respectively. The efficiency of the inverter in this simulation is about 92%. Fig. 5-22 shows waveforms of switching signals of the switch S_{21} (SS_{21}), the voltage across the S_{21} (v_{21}), switching signals of the switch S_{31} (SS_{31}) and the voltage across the S_{31} (v_{31}). When the S_{21} and S_{31} are turned on or off, the voltages across them, v_{21} and v_{31}

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are zero as shown in Fig. 5-22, which verifies that the switches of the HB₂ and the HB₃ switch at zero-voltage conditions.

Fig. 5-21. Simulated waveforms of capacitor voltages, load voltage, load current and the current flowing through the dc link of HB₁ in the bi-direction-balance mode

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Fig. 5-22. Simulated waveforms of signals and voltage of S_{21} and S_{31} in the bi-direction-balance mode

The fourth simulation shows the huge charging current of the inverter in high power application with single-direction-balance mode. The topology is shown in Fig. 5-14, in which v_{C1} , v_{C2} and v_{C3} are 3000V, 3000V and 6000V, respectively. Switches used in the simulation are GTOs, whose forward voltage, on-state resistance, current falling time and current tail time are 2.3V, 0.002 Ω , 10 μ S and 20 μ S, respectively. The forward voltage of anti-parallel diode is 1.2V. An arm in HB_1 includes a GTO, an arm in HB_2 includes two GTOs connected in series, and an arm in HB_3 includes four GTOs connected in series. The load is 30 Ω and 0.057H. The operation mode used in the simulation is single-direction balance mode. Fig. 5-23 shows the waveforms of load voltage (v_{an}), load current (i_{an}) and the current flowing through the dc link of HB_1 (i_{C1}). As shown in Fig. 5-23, the i_{C1} is very big, which is not acceptable in high power application.

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Fig. 5-23. Simulated waveforms of load voltage, load current and the current flowing through the dc link of HB₁ in the single-direction-balance mode for high power application

The fifth simulation verifies the performance of inverter in high power application with non-balance mode. The topology and simulation parameters are the same as those in the fourth simulation. The operation mode is non-balance mode. Fig. 5-24 shows the waveforms of load voltage (v_{an}), load current (i_{an}) and the current flowing through the dc link of HB₁ (i_{c1}). i_{c1} only includes the component of load current as shown in Fig. 5-24, so no charging or discharging current exist in the circuit. The efficiency of the inverter in this simulation is about 94%. Fig. 5-25 shows waveforms of switching signals of the switch S_{21} (SS_{21}), the input voltage of HB₂ ($v_{in,2}$), switching signals of the switch S_{31} (SS_{31}) and the input voltage of HB₃ ($v_{in,3}$). When the S_{21} and S_{31} are turned on or off, the input voltages of HB₂ and HB₃ are unit voltage (3000V) as shown in Fig. 5-25, so the switches in the HB₂ and HB₃ don't switch at zero-voltage conditions.

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Fig. 5-24. Simulated waveforms of load voltage, load current and the current flowing through the dc link of HB_1 in the non-balance mode for high power application

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Fig. 5-25. Simulated waveforms of signals of S_{21} and S_{31} , $V_{in,2}$ and $V_{in,3}$ in the non-balance mode for high power application

The sixth simulation shows the alternative method to avoid charging or discharging current in high power application with single-direction-balance mode. The topology and simulation parameters are the same as those in the fourth simulation, except that v_{C2} and v_{C3} are 3200V and 6400V, respectively. Fig. 5-26 shows the waveforms of load voltage (v_{an}), load current (i_{an}) and the current flowing through the dc link of HB₁ (i_{C1}). As show in Fig. 5-26, no big charging or discharging currents exist, but the tradeoff is that the output voltage levels of the inverter are not exactly even.

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Fig. 5-26. Simulated waveforms of load voltage, load current and the current flowing through the dc link of HB₁ in the single-direction-balance mode with modified dc source voltages for high voltage application

5.5 Experimental results

To verify the performance of the proposed inverter experimentally, a hardware prototype of a single-phase three-HB new inverter has been built in the laboratory. The type of the switches in HB₁ is IRF540 whose on-resistance is about 0.077Ω . The type of the switches in HB₂ is IRF640 whose on-resistance is about 0.18Ω . The type of the switches in HB₃ is IRF540 whose on-resistance is about 0.55Ω . The C_2 is 4.7mF and C_3 is 2.2mF. Thus, the experimental system parameters are the same as the simulation parameters. The inverter is controlled using a TMS320F240 controller card.

In the first experiment, the dc link of the HB₁ is supplied by a programmed voltage source whose voltage increases from 18V to 58V linearly, and then decreases from 58V to 18V linearly. No load. Fig. 5-27 shows the experimental waveforms of v_{C1} and v_{C2} in single-direction-balance mode. Fig. 5-28 shows the experimental waveforms of v_{C1} and

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v_{C3} in single-direction-balance mode. Fig. 5-29 shows the experimental waveforms of v_{C1} and v_{C3} in bi-direction-balance mode. Fig. 5-30 shows the experimental waveforms of v_{C1} and v_{C3} in bi-direction-balance mode. The results of the first experiment verify the results of the first simulation.

Fig. 5-27. Experimental waveforms of v_{C1} and v_{C2} in the single-direction-balance mode.

CH1: v_{C1} (20V/div); CH2: v_{C2} (20V/div)

Fig. 5-28. Experimental waveforms of v_{C1} and v_{C3} in the single-direction-balance mode

CH1: v_{C1} (20V/div); CH2: v_{C3} (40V/div)

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Fig. 5-29. Experimental waveforms of v_{C1} and v_{C2} in the bi-direction-balance mode
CH1: v_{C1} (20V/div); CH2: v_{C2} (20V/div)

Fig. 5-30. Experimental waveforms of v_{C1} and v_{C3} in the bi-direction-balance mode
CH1: v_{C1} (20V/div); CH2: v_{C3} (40V/div)

In the second experiment, the dc link of the HB₁ is supplied by series-connected batteries whose total voltage is 48V. The load is 100Ω and 0.19H. A resistance is added into dc link of HB₁ to decrease the charging current in the process of pre-charge of dc capacitors as shown in Fig. 5-31. A delay connected in parallel with this resistance will be turned on after the completion of pre-charging process. Fig. 5-32 shows the experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{C1}) in single-direction-balance mode, which verifies the results of the second simulation.

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Fig. 5-31. Current-limited resistance and delay used in the process of pre-charging dc capacitors

Fig. 5-32. Experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{C1}) in the single-direction-balance mode

CH1: v_{an} (100V/div); CH2: i_{C1} (10A/div)

In the third experiment, the dc capacitors of the HB₁ is also supplied by series-connected batteries whose total voltage is 48V, and a small resistance connected in parallel with the batteries to absorb the regenerative energy in regenerative mode. A program ac source is connected with the load in series. The peak value, phase and frequency of the ac source are 300V, 0° and 50Hz. Thus, the system is in regenerative mode and the inverter works in bi-direction-balance mode. Fig. 5-33 shows the experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{C1}) in bi-direction-balance mode, which verify the results of the third simulation.

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Fig. 5-33. Experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{C1}) in the bi-direction-balance mode

CH1: v_{an} (100V/div); CH2: i_{C1} (5A/div)

In the fourth experiment, all dc capacitors of HBs are supplied by series-connected batteries. The v_{C1} , v_{C2} and v_{C3} are 48V, 48V and 96V, respectively. The inverter runs in non-balance mode. Fig. 5-34 shows the experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{C1}) in non-balance mode, which verify the results of the fourth simulation.

Fig. 5-34. Experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{C1}) in the non-balance mode

CH1: v_{an} (100V/div); CH2: i_{C1} (1A/div)

In the fifth experiment, the dc capacitors of HBs are supplied by series-connected batteries too, but the v_{C1} , v_{C2} and v_{C3} are 48V, 60V and 120V, respectively. The inverter works in single-direction-balance mode. Fig. 5-35 shows the experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{C1}) in single-direction-balance mode with modified dc source voltages.

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Fig. 5-35. Experimental waveforms of load voltage (v_{an}) and the current flowing through the dc link of HB₁ (i_{c1}) in the single-direction-balance mode with modified dc source voltages

CH1: v_{an} (100V/div); CH2: i_{c1} (2A/div)

5.6 Discussions

5.6.1 Comparison with other topologies of multilevel Inverters

Popular topologies of multilevel inverters include diode-clamped multilevel inverters, capacitor-clamped inverters, cascade multilevel inverters and generalized multilevel inverters [3, 16, 26]. In a diode-clamped multilevel inverter or a capacitor-clamped inverter, only a dc source is needed. However, when the number of output voltage levels is high, the number of components required in these two topologies will make the systems impractical to implement [26]. Cascade multilevel inverters can provide a great deal of output voltage levels with fewer components, but separate dc sources are needed in this topology. The generalized multilevel inverter topology provides a true multilevel structure that can balance each dc voltage level automatically regardless of active or reactive power conversion without any assistance from other circuits [16]. With the generalized multilevel inverter topology, low dc voltage can result in high dc/ac output voltage. Similar to the diode-clamped inverter and the capacitor-clamped inverter, the number of the generalized multilevel inverter is fewer since the number of required components increase exponentially with an increase in the number of output voltage levels. Emerging topologies of multilevel inverters include hybrid multilevel inverters [26] and soft-switched multilevel inverters [23-25, 107-109]. Hybrid multilevel inverters have similar structure as cascade multilevel inverters, but the voltage levels of cells are different. This feature allows more levels to be created in the output voltage, and thus

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reduces the harmonic contents with fewer components required. Moreover, higher-voltage lower-speed switching devices can be used in the cells with higher voltage, while lower-voltage higher-speed switching devices can be used in the cells with lower voltage. Similar to the cascade multilevel inverter, the hybrid multilevel inverter still needs multiple separated dc sources. Several topologies of soft switching multilevel inverters have been presented. In general, the decrease of switching losses and dv/dt is at the cost of auxiliary circuits, such as auxiliary switches and snubber circuits.

When the new inverter works in single-direction-balance mode or bi-direction-balance mode, only a dc source is needed in the inverter as shown in Fig. 5-2. Here the topology of the new inverter in single-direction-balance mode and bi-direction-balance mode is compared with other topologies of multilevel inverters that are diode-clamped multilevel inverters (DCMI), capacitor-clamped multilevel inverters (CCMI), cascade multilevel inverter (CMI), generalized multilevel inverter (GMI), binary hybrid multilevel inverters (BHMI) [14, 15], and trinary hybrid multilevel inverter (THMI) [10, 11]. Table 5-4 shows the comparison results, where m is the number of output voltage levels. Since the new inverter in single-direction-balance mode or bi-direction-balance mode is mainly applied in low power application, the voltage ratings of the main switching components, diodes and capacitors can be reached easily. So the numbers of main switching components, diodes and capacitors shown in Table 5-4 are minimal required values. From Table 5-4, one can get that the multilevel inverters in which only a dc source is required are DCMI, CCMI, GMI and the new multilevel inverter. Among them, it is the new multilevel inverter that uses the fewest main switching components, diodes and capacitors. The BHMI and THMI use fewer components than the new multilevel inverter, but the BHMI and THMI need separate dc sources, just as the CMI. Moreover, only the new multilevel inverter and the GMI have the ability of self voltage balancing and the ability of voltage boosting (lower dc input voltage result in higher ac output voltage), but the latter requires much more components than the former.

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Table 5-4: Comparison between multilevel inverters

Converter type	DCMI	CCMI	CMI	BHMI	THMI	GMI	New multilevel inverter
Main switching devices	$2m-2$	$2m-2$	$2m-2$	$4 \times \log_2[(m+1)/2]$	$4 \times \log_3 m$	2^m-2	$4+4 \times \log_2[(m-1)/2]$
Diodes	$4m-6$	$2m-2$	$2m-2$	$4 \times \log_2[(m+1)/2]$	$4 \times \log_3 m$	2^m-2	$4+4 \times \log_2[(m-1)/2]$
Capacitors	$m-1$	$2m-3$	$0.5m-0.5$	$\log_2[(m+1)/2]$	$\log_3 m$	$m-1$	$1+\log_2[(m-1)/2]$
Total components	$7m-9$	$6m-7$	$4.5m-4.5$	$9 \times \log_2[(m+1)/2]$	$9 \times \log_3 m$	$2^{m+1}+m-5$	$9+9 \times \log_2[(m-1)/2]$
dc sources	1	1	$0.5m-0.5$	$\log_2[(m+1)/2]$	$\log_3 m$	1	1
Self voltage balancing	No	No	No	No	No	Yes	Yes
Voltage boosting	No	No	No	No	No	Yes	Yes

5.6.2 Comparison of switching losses in three operation modes

Suppose the step modulation strategy is used. From Table 5-1, Fig. 5-6, Fig. 5-7, Fig. 5-11, Fig. 5-12, Fig. 5-15 and Fig. 5-16, we can get the switching frequencies of switching devices of HB_i and the input voltage of HB_i during the switching of the switching devices in HB_i , as show in Table 5-5. In single-direction-balance mode and bi-direction-balance mode, the switching power losses of a switching device in HB_1 can be expressed as

$$P_{s1} = 200k_1 E \quad (5.17)$$

where k_1 is a coefficient. The switching losses of a switching device in HB_2 and HB_3 are zero in single-direction-balance mode and bi-direction-balance mode. In non-balance mode, the switching losses of a switching device in HB_1 , HB_2 and HB_3 can be expressed as

$$P_{N1} = 25k_1 E \quad (5.18)$$

$$P_{N2} = 100k_2 E \quad (5.19)$$

$$P_{N3} = 50k_3 E \quad (5.20)$$

where k_2 and k_3 are coefficients. The switching devices used in different HBs are different due to different voltages they endure. Suppose k_i is proportional to the voltage that switching devices in HB_i endure. So

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$$k_2 = 2k_1 \quad k_3 = 4k_1 \quad (5.21)$$

From (5.17), (5.18), (5.19), (5.20) and (5.21), we can get the total switching losses in single-direction-balance mode and bi-direction-balance mode shown as

$$P_s = 800k_1 E \quad (5.22)$$

and the total switching losses in non-balance mode shown as

$$P_N = 1700k_1 E \quad (5.23)$$

The equations, (5.22) and (5.23), show that the total switching losses in single-direction-balance mode and bi-directional-balance mode are less than those in non-balance mode. Moreover, in single-direction-balance mode and bi-directional-balance mode, the switching losses only exist in the switching devices in HB₁, which results in fewer cooling devices.

Table 5-5: Comparison of switching frequencies and input voltage during the switching of a HB in three sorts of operation modes (with step modulation strategy)

Operation mode	Switching frequencies of switching devices in HB _i			Input voltage of HB _i while switching devices of HB _i switch		
	HB ₁	HB ₂	HB ₃	HB ₁	HB ₂	HB ₃
Single-direction-balance	200Hz	100Hz	50Hz	E	0	0
Bi-direction-balance	200Hz	100Hz	50Hz	E	0	0
Non-balance	25Hz	100Hz	50Hz	E	E	E

5.6.3 Energy losses during voltage balancing

When the inverter works in single-direction-balance mode or bi-direction-balance mode, the v_{C2} is balanced by the connection of the dc source of HB₁ and the C₂ through switches and diodes, and the v_{C3} is balanced by the connection of the dc source of HB₁, the C₂ and the C₃. Here take the example of the balance of the v_{C2} to analyze the energy losses during the self voltage balancing. The equivalent circuit is shown in Fig. 5-3. Suppose the initial voltage difference between v_{C1} and v_{C2} is ΔV_{C12} , the charging time is infinite, R_M is on-state resistance of the switch and V_D is forward voltage of diodes. At each transition energy losses, E_L , is expressed as

$$E_L = C_2 (\Delta V_{12} - 2V_D)^2 \quad (5.24)$$

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The energy losses are proportional to the voltage difference and the capacitor but independent of the on-state resistance of the switch. The resistance only affects the initial charging/discharging current and duration, but has no effect on the energy losses. As mentioned previously, higher frequency can result in smaller C_2 and smaller ΔV_{12} . Thus, the energy losses will be decreased in higher frequency application. At each transition, the energy transferred from the dc source of HB₁ to the C_2 is expressed as

$$E_T = \frac{1}{2} C_2 (\Delta V_{12} - 2V_D)(2v_{C1} - 2V_D - \Delta V_{12}) \quad (5.25)$$

where the v_{C1} is the voltage of dc source of HB₁. Suppose the deviation of the capacitor voltage is ϵ , that is

$$\Delta V_{12} = \epsilon v_{C1} \quad (5.26)$$

From (5.24), (5.25) and (5.26), we can get that the ratio between E_L and E_T is expressed as

$$\frac{E_L}{E_T} = \frac{2(\Delta V_{12} - 2V_D)}{2v_{C1} - 2V_D - \Delta V_{12}} \approx \frac{\Delta V_{12}}{v_{C1}} = \epsilon \quad (5.27)$$

which means the ratio between E_L and E_T is about the deviation of the capacitor voltage.

5.7 Summary

A new topology of multilevel inverter is proposed in this chapter. Aspects of the new multilevel inverter are studied, including structures, operation modes and applications. Voltages of dc capacitors can be balanced in single-direction-balance mode with non-regenerative load. If the regenerative load is fed by the inverter, bi-direction-balance mode can be used to balance the dc capacitor voltages. When the inverter works in above modes, the switches in HBs (except HB₁) switch at zero-voltage conditions. Less required components, only a dc source needed, the ability of self voltage balancing, the ability of voltage boosting and zero-voltage switching make the new inverter promising in low power application, especially with high frequency. Moreover, the non-balance mode with which the charging or discharging currents can be avoided is presented for the new inverter working in high power application. Another solution for high power application is that the inverter works in single-direction-balance mode but with modified dc voltages.

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The simulation and experimental results describe and verify the performance of the new inverter.

Chapter 6 Conclusion and Recommendations

6.1 Conclusion

The thesis describes an investigation into the circuit topology, control and applications of hybrid multilevel inverters. The basic structure of the hybrid multilevel inverter is based on the connection of HBs and dc capacitor sources whose voltages are not identical. Several topologies of the hybrid multilevel inverters, BHMI, quasi-linear multilevel inverter and THMI are introduced. As a kind of emerging topologies of multilevel inverters, the hybrid multilevel inverters are promising since it can synthesize more voltage levels using the same number of components. Moreover, in the hybrid multilevel inverters, the lower-voltage switching components switch at higher frequency, while the higher-voltage switching components switch at lower frequency. The power semiconductors of the hybrid multilevel inverters can be selected based on this characteristic. For example, the faster devices with lower-voltage blocking capability, such as IGBT, is used in lower-voltage HBs, while the slower devices with higher-voltage blocking capability, such as GTO, is used in higher-voltage HBs. Other topologies of multilevel inverters are also introduced. They are diode-clamped multilevel inverters, capacitor-clamped multilevel inverters, cascade multilevel inverters, generalized multilevel inverters, mixed-level multilevel inverters, multilevel inverters by the connection of three-phase two-level inverters, and soft-switched multilevel inverters. The family of multilevel inverters is now widely applied in medium voltage applications, such as large motor drives and power systems. As a cost-effective solution, multilevel inverters are also used in medium and low power applications, such as distributed energy system due to elimination of filters and transformer.

According to applications, two kinds of comparisons among the hybrid multilevel inverters and other multilevel inverters are given. The comparison results show that the THMI has the greatest level number for a given number of components among the existing multilevel inverters. The theoretical prove that the THMI has the greatest level

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number among the hybrid multilevel inverters is also given. Aspects of the THMI are investigated. With more voltage levels, the output voltage waveform synthesized by the multilevel inverter is more similar to sinusoid waveform. Thereby, lower order harmonics and total harmonics distortion can be reduced greatly.

The circuit topology and operation of the THMI are described. Various modulation strategies for THMI are investigated. The modulation strategies working with high switching frequencies, such as hybrid modulation strategy and sub-harmonic PWM strategy, are not suitable for the THMI. Low-frequency modulation strategies such as step modulation strategy and virtual stage modulation strategy are applicable in THMI. The virtual stage modulation strategy can eliminate more lower-order harmonic components than step modulation strategy, but additional constraints must be added into the virtual modulation strategy to ensure the higher voltage HBs switch at lower frequency. The simple modulation strategy can be used in the THMIs with many HBs. THMI also has a disadvantage. Power of the lower voltage HBs is possible to be regenerative with lower modulation index. If the THMI feeds a RL or RC load and simple diode bridge rectifiers are used as dc sources, the regenerative power will cause the increase of the dc capacitor voltages, which will damage devices. Two methods have been presented to solve regenerative power problem: using bidirectional dc/dc converters or using additional output transformers. The third method proposed in the thesis can stabilize the dc capacitor voltages by avoiding outputting so-called several null voltage levels. The first two methods are expensive since they need additional bidirectional dc-dc converters or output transformers. The third method is cost-effective, but the tradeoff is that power quality will decrease a little with lower modulation index. Therefore, basically, the THMI is suitable for the applications without regenerative power. The first one is the application of reactive power compensation in which the problem of regenerative power is avoided. The second one is the application in which the inverter always runs with higher modulation index.

The application of THMI in STATCOM with unbalanced voltages is investigated. In the proposed 10 MVar STATCOM, a three-phase nine-level THMI is used, in which GTOs connected in series are used as switching components. The solution of THMI is cost-effective because of reduced cost of GTOs, cooling systems and dc capacitors. The

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reduced cost of GTO is due to fewer redundant switches required in THMI. The total cost of cooling systems for THMI is lower since fewer GTOs are used. There are two reasons why THMI has less cost of dc capacitors. Firstly, it needs less redundancy capacitors. Secondly, the capacitors in lower voltage HBs are both charged and discharged in quarter cycles.

The step modulation strategy permits the inverter work at lower frequency. The switching angles obtained from the off-line calculation are stored in a look-up table. Vector control based on synchronous frame transform lead to high dynamic performance of STATCOM. The control loops of active power and reactive power are decoupled and the controlled system is reduced to a first order transfer function. Moreover, the bus voltages are rebalanced during the unbalanced conditions and the compensation current is limited within normal values. The new method by which the switching signals are generated from the reference inverter voltages is based on the comparison of amplitudes instead of angles. By this method, the output voltage of inverter does not contain lower-order harmonics under stable balanced conditions and the inverter can keep high dynamic performance under unbalanced conditions or transient processes. Each capacitor voltage is also controlled to be stable. The performance of the proposed STATCOM and control system is confirmed by simulations. Furthermore, a 2 kVAr laboratory prototype system is built and the performance is verified by experiments.

A trinary hybrid 81-level multilevel inverter is proposed for motor drive in the paper. The inverter can output 81-level voltages per phase with the fewest components. THD of output voltage is as low as 1%. Bi-directional dc-dc converters are used as the dc links of HBs, which results in stable dc link voltages, whatever the power that flows through the HB is regenerative or not. The space vector modulation working in lower frequency can reduce common-mode voltages and leads to precise linearity between the fundamental component and the modulation index. Vector controller is used to control induction motor, which results in high dynamic response for speeds or toques.

A new topology of hybrid multilevel inverter is proposed in the thesis. It is also based on the connection of HBs and dc capacitor source, but the method of connection is different from other hybrid multilevel inverters. Aspects of the new multilevel inverter are studies, including structures, operation modes and applications. Voltages of dc

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capacitors can be balanced in single-direction-balance mode with non-regenerative load. If the regenerative load is fed by the inverter, bi-direction-balance mode can be used to balance the dc capacitor voltages. When the inverter works in above modes, the switches in HBs (except HB₁) switch at zero-voltage conditions. The new inverter is promising in low power application, especially with high switching frequency, due to less required components, only a dc source needed, the ability of self voltage balancing, the ability of voltage boosting and zero-voltage switching. Moreover, the non-balance mode with which the charging or discharging currents can be avoided is presented for the new inverter working in high power application. Another solution for high power application is that the inverter works in single-direction-balance mode but with modified dc voltages. The simulation and experimental results verify the performance of the new inverter.

6.2 Recommendations

In the proposed STATCOM, the voltages and currents of the STATCOM contain lower-order harmonic components under unbalanced conditions since the step modulation strategy does not eliminate triple order harmonic components. Further work should be considered to eliminate lower-order harmonic components under unbalanced conditions. The STATCOM system used in this thesis, is only prototype. Although it could explain some fundamental laws of the topology and the principle of control system, the experiment results with higher voltage STATCOM seems more close to the practical applications. Protection and reliability are other factors that should be considered for practical applications.

The topology circuit and operation principle of the new hybrid inverter with the ability of self voltage balancing are described in this thesis. The specific application of the new inverter should be further studied.

Author's Publications

Journal papers

- Y. Liu and F. L. Luo, "Trinary hybrid 81-level multilevel inverter for motor drive with zero common-mode voltage," *IEEE Trans. Ind. Electron.*, accepted.
- Y. Liu and F. L. Luo, "Multilevel inverter with the ability of self-voltage balancing," *IEE Proc. Electr. Power Applicat.*, vol. 153, pp. 105-115, Jan 2006.
- Y. Liu and F. L. Luo, "Trinary hybrid multilevel inverter used in STATCOM with unbalanced voltages," *IEE Proc. Electr. Power Applicat.*, vol. 152, pp. 1203-1222, Sep 2005.
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- K. Y. Wang, W. H. Huang, Y. Liu and Y. P. Qian, "Application of design pattern in software framework of power system supervisory and control," *Automation of Electric Power Systems*, vol. 27, pp. 50-53, 2003.

Conference papers

- F. L. Luo and Y. Liu, "A new asymmetric hybrid multilevel inverter," *International Power Engineering Conference*, 2003, pp. 311-316.
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