Development of power conditioners and controllers for microgrids

Li, Yun Wei

2006

Li, Y. W. (2006). Development of power conditioners and controllers for microgrids. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/4784>

<https://doi.org/10.32657/10356/4784>

Nanyang Technological University

Downloaded on 26 Apr 2023 19:16:59 SGT

Development of Power Conditioners and
Controllers for Microgrids

Li Yun Wei

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2006

TJ
163-2
L693
2006

Acknowledgements

First, I am grateful to Nanyang Technological University, Singapore, for providing me an opportunity to pursue my Ph.D. study with a research scholarship.

I would like to express sincere gratitude and appreciation to my supervisor, Associate Professor Dr. Mahinda Vilathgamuwa, for his invaluable guidance, enthusiastic help, and consistent encouragement throughout all phases of the research program. I am also thankful to Assistant Professor Dr. Poh Chiang Loh for many fruitful discussions and nice collaborations. Without them, my work would have been much more difficult, or even impossible, to accomplish.

Thanks go to laboratory staff of Electric Power Research Lab (EPRL), Tiow Koon Yeoh, Annie Chew-Sim and Ting Yeng Lee, for the effective technical support and help provided. My gratitude is extended to all colleagues in EPRL, for their help and providing a good working environment.

Some experimental work involved in this thesis was carried out at the Institute of Energy Technology, Aalborg University, Denmark. I would like to thank Professor Frede Blaabjerg for supervision and providing the fund and all the facilities. Also thanks to Assistant Professor Hilmy Awad (from Chalmers University of Technology, Sweden), Associate Professor Hans Nielsen and the laboratory staff Martin Gunge and Walter Neumayr for their help during the experiment.

I would also like to express my deepest gratitude and love to my parents for their unconditional support and encouragement throughout my entire education.

Last, but surely not least, I would like to thank Lihua, for her love, encouragement and understanding.

Table of Contents

Acknowledgements	i
Table of Contents	ii
Summary	vii
List of Figures.....	ix
List of Tables	xx
List of Abbreviations	xxi

Chapter 1

Introduction.....	1
1.1 Motivation.....	2
1.2 Objectives	3
1.2.1 Realization of the basic functions of microgrid operation.....	3
1.2.2 Further power quality improvement with consideration of utility voltage quality problems impacts	4
1.2.3 Robust performance under microgrid load disturbances	4
1.3 Major Contribution of the Thesis.....	6
1.3.1 A unified controller for realization of all the basic functions of a microgrid	6
1.3.2 Three-phase three-wire grid-interfacing compensator for utility voltage unbalance	6
1.3.3 Three-phase four-wire grid-interfacing compensator for utility voltage unbalance	7
1.3.4 Fault current limiting algorithms for use in utility voltage sag.....	7
1.3.5 Robust control of microgrid with capacitive loads	8
1.3.6 Investigation and improvement of transient response.....	9
1.3.7 Verification of the developed control algorithms	9
1.4 Organization of the Thesis	10

Chapter 2

The Microgrid Concept	13
2.1 Introduction.....	13

2.1.1 Distributed generation.....	13
2.1.2 Microgrid concept.....	16
2.2 Background Technologies	17
2.2.1 Generation technologies.....	18
2.2.2 Energy storage technologies	19
2.3 Application of Microgrids.....	21
2.4 Example Microgrid Structure	23
2.5 Control Issues for the Microgrid.....	26
2.5.1 Basic operation requirements.....	27
2.5.2 Impacts from utility voltage quality problems.....	27
2.5.3 Load impacts in the microgrid	30
2.6 Discussion.....	31
 Chapter 3	
A Multi-Functional Unified Controller for Microgrid	33
3.1 Introduction.....	33
3.2 System Configuration	34
3.3 Controller Design.....	35
3.3.1 Inner current and voltage control loops	35
3.3.2 External real and reactive power control loops.....	41
3.3.3 Synchronization of the microgrid and utility	44
3.4 Off-Line Simulation of the Microgrid System.....	47
3.4.1 Transition from grid-connected to islanding mode of operation	48
3.4.2 Transition from islanding to grid-connected mode of operation	50
3.5 Real-Time Digital Simulation Implementation	52
3.5.1 System configuration of the real-time implementation platform.....	53
3.5.2 Transition from grid-connected to islanding mode of operation	55
3.5.3 Transition from islanding to grid-connected mode of operation	56
3.6 Hardware Implementation of the Microgrid System	59
3.6.1 Description of the proposed microgrid hardware prototype	59
3.6.2 Implementation of the controller	60
3.6.3 Experimental results.....	61
3.7 Discussion.....	65

Chapter 4

Dual-Inverter Grid-Interfacing Power Quality Compensators for Microgrid	66
4.1 Introduction.....	66
4.2 Power Quality Compensator for Three-Phase Three-Wire Microgrids.....	68
4.2.1 Control of shunt three-leg inverter A.....	69
4.2.2 Control of series three-leg inverter B.....	77
4.3 Simulation Results on the Three-Wire Microgrid System.....	82
4.4 Experimental Verification of the Three-Wire Compensator.....	84
4.5 Power Quality Compensator for Three-Phase Four-Wire Microgrid Implementation	87
4.5.1 Control of shunt four-leg inverter A	88
4.5.2 Control of series four-leg inverter B.....	93
4.6 Simulation Results on the Four-Wire Microgrid System.....	98
4.7 Experimental Verification of the Four-Wire Compensator	101
4.8 Discussion	105

Chapter 5

Protection of Microgrid during Utility Voltage Sags.....	107
5.1 Introduction.....	107
5.2 General Operating Principles of the Proposed Current-Limiting Algorithms	108
5.3 RL Feedforward Current-Limiting Algorithms	110
5.3.1 Description of control algorithm and implementation issues	110
5.3.2 Optimal R/L ratio.....	112
5.3.3 Analysis of worst case condition	114
5.4 Flux-Charge-Model Feedback Current-Limiting Algorithm.....	115
5.4.1 Analysis of flux-model control	115
5.4.2 Development and analysis of flux-charge-model control.....	117
5.4.3 Analysis of worst case condition	122
5.5 Simulation Results	123
5.5.1 RL feedforward algorithm	124
5.5.2 Flux-charge-model algorithm	126
5.6 Experimental Verification.....	127
5.6.1 RL feedforward algorithm	128

5.6.2 Flux-charge-model algorithm	129
5.7 Discussion	132
 Chapter 6	
Robust Control Scheme for a Microgrid with PFC Capacitor Connected.....	133
6.1 Introduction.....	133
6.2 Modeling and Analysis of a Microgrid System with PFC Capacitor Connected ...	135
6.2.1 Grid-connected mode.....	136
6.2.2 Islanding mode.....	137
6.3 Analysis and Design of the VSI Control.....	138
6.3.1 H_∞ controller for the voltage loop.....	139
6.3.2 Inner current loop.....	144
6.4 Further Resonance Attenuation Using Dual-Inverter Microgrid Conditioner.....	148
6.4.1 Retrieval of harmonic line current components.....	150
6.4.2 Development and analysis of voltage control.....	151
6.5 Simulation Results	154
6.6 Experimental Results	157
6.7 Discussion	161
 Chapter 7	
Medium Voltage Experimental Verifications.....	162
7.1 Introduction.....	162
7.2 Medium Voltage Experimental System Setup.....	163
7.3 Comparison and Implementation of H_∞ and P+resonant Controllers	167
7.3.1 Overall DVR control scheme.....	168
7.3.2 Review of P+resonant controller	169
7.3.3 Design description of H_∞ controller.....	171
7.3.4 Performance and robustness comparison.....	177
7.3.5 Experimental comparison under balanced voltage sag and linear load	181
7.3.6 Experimental comparison under balanced voltage sag and nonlinear load ...	183
7.3.7 Experimental comparison under unbalanced voltage sag.....	185
7.3.8 Experimental verification of H_∞ controller with motor load	186
7.4 Implementation of Fault Current Limiting Algorithm.....	187
7.4.1 Downstream fault at a DVR connected system	188

7.4.2 Using DVR to limit fault currents.....	189
7.4.3 Detection and recovery from a downstream fault.....	191
7.4.4 Flux-charge-model control algorithm implementation for DVR.....	191
7.4.5 Experimental verification under three-phase short circuit.....	194
7.4.6 Experimental verification under single-phase short circuit	196
7.5 Investigation and Improvement of Transient Response.....	197
7.5.1 Resonance damping effects by different control schemes	198
7.5.2 Proposed control strategy for transient improvement.....	201
7.5.3 Experimental verification of single-loop with/without posicast controller under linear load	208
7.5.4 Experimental verification of double-loop with/without posicast controller under linear load	209
7.5.5 Experimental verification of single-loop with/without posicast controller under nonlinear load	210
7.5.6 Experimental verification of double-loop with/without posicast controller under nonlinear load	212
7.6 Discussion	214
 Chapter 8	
Conclusions and Recommendations	215
8.1 Conclusions.....	215
8.2 Recommendations.....	219
 Author's Publications	221
Bibliography	223
Appendix.....	A1

Summary

Microgrid is a cluster of loads and distributed generation (DG) systems operating together within a certain local area. Being a systematic organization of DG systems, the microgrid has larger power capacity and more control flexibilities to fulfill system reliability and power quality requirements, in addition to all the inherited advantages of a single DG. Furthermore, as a system approach to realize the emerging potential of DG system, the microgrid can combat problems caused by the unconventional behaviors of DG.

Proper operation of a microgrid requires robust local voltage regulation as well as dispatched power generation. During a power system interruption, the microgrid must disconnect itself from the utility and protect the loads in it. After the utility voltage is restored, the microgrid should synchronize with the utility and reconnect to it smoothly. A unified controller is first designed to achieve those functions with fast responses and smooth transients. The proposed controller contains an inner voltage and current control block for voltage regulation, external real and reactive power control blocks based on the "plug and play" concept, and a synchronization block for smooth and safe connection of the microgrid and utility.

The grid-interfacing nature of a microgrid implies that the microgrid is subjected to utility power quality problems. Other than the voltage interruptions, two common problems that would cause microgrid voltage unbalance, line current unbalance or even large fault current are utility voltage unbalances and voltage sags. To address those issues, dual-inverter grid-interfacing power quality compensators (a three-phase three-wire compensator and a three-phase four-wire one) are proposed. Each compensator comprises of two inverters, a three/four-leg shunt and a three/four-leg series inverter. In each inverter, both positive- and negative-sequence (and zero-sequence for the four-wire compensator) components are controlled to compensate for the effects caused by the unbalanced utility grid voltages.

Considering the utility voltage sag, two current-limiting algorithms, termed as RL feedforward and flux-charge-model feedback algorithms are proposed and integrated

within the dual-inverter microgrid compensators' control schemes. The algorithms are developed based on different control principles, but respond similarly by controlling the series inverter to act like a large virtual RL or L impedance to limit the line current flow during an utility voltage sag.

Being a larger system also means that the microgrid can easily be disturbed by the numerous power apparatuses connected within its vicinity. In particular, the switching of power factor correction (PFC) capacitors can cause system parameter variations, and hence performance degradation of the designed microgrid controller. The presence of PFC capacitors can also result in high resonant voltages and currents. A detailed study of the scenario of a microgrid with PFaC capacitor installed is thus conducted. A H_∞ control scheme is designed for control of microgrid voltage under system parameter variations. For the resonance situation, a thorough analysis is carried out to show that inner filter inductor current feedback method is more effective for the resonance damping than filter capacitor current feedback. A further damping method is also proposed by employing the dual-inverter compensator, where the series inverter is controlled as a virtual harmonic resistor to dampen the resonance without affecting the fundamental power flow.

A transient improvement method for the inverter output voltage regulation is also developed in this work. For typical inverter and filter topology, the filter circuit designed to eliminate the high frequency inverter switching noises, would introduce a lightly damped plant model and initiate LC resonance under a sudden change of reference. An effective and simple resonance damping method is proposed by employing closed loop (single-loop or multi-loop) control and an embedded two-step posicast controller. As a general control algorithm, the proposed method is applicable to both the shunt and series inverters used for microgrid voltage conditioning.

All the proposed controllers, compensators and every single control algorithm in this work are extensively tested and verified through experiment (on a low voltage laboratory microgrid prototype or on a 10 kV medium voltage level grid-interfacing series inverter), after initially simulated in off-line simulations or on a designed real-time implementation platform.

List of Figures

Figure 2.1. Single line diagram of: (a) traditional radial power system and (b) power system with the inclusion of DG.....	15
Figure 2.2. Typical diagram of micro-source generation system.	18
Figure 2.3. CHP versus separate heat and power energy flows (adapted from [30]).	22
Figure 2.4 Basic microgrid structure.	24
Figure 3.1. Microgrid configuration.	34
Figure 3.2. Power circuit and control schematic for the three-phase grid-interfacing inverter with LC filters.....	36
Figure 3.3. Block diagram of inner current loop.	38
Figure 3.4. Bode plots of I_C / I_C^* and I_C / I_{load}	38
Figure 3.5. Bode plot of the closed-loop voltage transfer function.	39
Figure 3.6. Block diagram of the voltage and current loops with feedforward control.....	40
Figure 3.7. Bode plots of V_C / V_C^* and V_C / I_{load}	41
Figure 3.8. Real and reactive power flows between two nodes with voltages $V_1 \angle \delta$ and $V_2 \angle 0$ separated by an inductor L.	41
Figure 3.9. P – ω droop characteristics.	42
Figure 3.10. Real power compensator.	44
Figure 3.11. Reactive power compensator.....	44
Figure 3.12. Real power compensator with synchronization function.	45
Figure 3.13. Reactive power compensator with synchronization function.....	46
Figure 3.14. Overview of proposed microgrid unified controller.....	47
Figure 3.15. Real power flow of DG systems.....	48
Figure 3.16. Reactive power flow of DG systems.	48
Figure 3.17. Frequency of the DG system 1.	49
Figure 3.18. Magnitude of the capacitor voltages of the DG system 1	49
Figure 3.19. Three-phase capacitor voltages at $t = 1.5$ s.....	49
Figure 3.20. Synchronization of the microgrid and the utility system (phase A).....	50
Figure 3.21. Switch current (phase A) during reconnection.	50

Figure 3.22. Frequency of the DG system 1 during synchronization and reconnection....	51
Figure 3.23. Magnitude of the capacitor voltage of the DG system 1 during synchronization and reconnection.....	51
Figure 3.24. Real power of DG systems.	52
Figure 3.25. Reactive power of DG systems.	52
Figure 3.26. Real-time implementation platform.....	53
Figure 3.27. Laboratory setup for real-time digital simulation.....	55
Figure 3.28. Real power flow of the DG systems (RTDS).	56
Figure 3.29. Reactive power flow of DG systems (RTDS).	56
Figure 3.30. Phase A capacitor voltage of the DG system 1 (RTDS).....	56
Figure 3.31. Switch current (phase A, RTDS).....	56
Figure 3.32. Synchronization of the microgrid and the utility system (phase A, RTDS).	57
Figure 3.33. Real power flow of DG systems during synchronization (RTDS).....	57
Figure 3.34. Reactive power flow of DG systems during synchronization (RTDS).	57
Figure 3.35. Switch current during reconnection (phase A, RTDS).....	58
Figure 3.36. Real power flow of DG systems during reconnection (RTDS).....	58
Figure 3.37. Reactive power flow of DG systems during reconnection (RTDS).	58
Figure 3.38. Hardware setup (part a).	59
Figure 3.39. Hardware setup (part b).	59
Figure 3.40. Real and reactive power outputs of DG system 1 when the microgrid islands (experimental).	61
Figure 3.41. Real and reactive power outputs of DG system 2 when the microgrid islands (experimental).	61
Figure 3.42. Output line voltage of DG system 1 when the microgrid islands (experimental).	62
Figure 3.43. Switch current when the microgrid islands (experimental).....	62
Figure 3.44. Synchronization of microgrid and utility (voltages V_{ab} ; experimental).	62
Figure 3.45. Real and reactive power outputs of DG system 1 during synchronization (experimental).	63
Figure 3.46. Real and reactive power outputs of DG system 2 during synchronization (experimental).	63
Figure 3.47. Real and reactive power outputs of DG system 1 during reconnection (experimental).	63

Figure 3.48. Real and reactive power outputs of DG system 2 during reconnection (experimental).	63
Figure 3.49. Switch current during reconnection (phase A; experimental).	63
Figure 4.1 Proposed three-phase three-wire microgrid configuration.	68
Figure 4.2. Overall control structure of shunt inverter A for three-wire compensator.	69
Figure 4.3. Voltage control scheme of shunt inverter A of three-wire compensator.	71
Figure 4.4. Bode plot of closed-voltage-loop of shunt inverter A for three-wire compensator.	76
Figure 4.5. Control scheme of series three-leg inverter B.	77
Figure 4.6. Block diagram of closed-voltage-loop of series inverter B ($K_{inv} = 2/V_{dc}$).	78
Figure 4.7. Control of series three-leg inverter B in negative synchronous frame: (a) filtering of positive-sequence currents and (b) closed-current-loop.	80
Figure 4.8. Bode plots of G_{kl} and $G_{kl} \cdot G_{lp}$	81
Figure 4.9. Simulated three-wire system: (a) utility grid voltages and (b) sensitive load voltages in the microgrid.	83
Figure 4.10. Simulated three-wire system: (a) line currents, (b) negative-sequence line currents in the negative synchronous frame and (c) filtered voltages generated by series inverter B.	83
Figure 4.11. Simulated three-wire system: (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B.	84
Figure 4.12. Experimental three-wire system: (a) utility grid voltages and (b) sensitive load voltages in the microgrid.	85
Figure 4.13. Experimental three-wire system: (a) line currents, (b) negative-sequence line currents in the negative synchronous frame and (c) filtered voltages generated by series inverter B.	86
Figure 4.14. Experimental three-wire system: (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B.	86
Figure 4.15. Proposed four-wire microgrid compensator (a) overall system structure and (b) inverter topology.	87

Figure 4.16. Control scheme for shunt four-leg inverter A (a) overall control structure and (b) voltage control algorithm.....	88
Figure 4.17. Bode plots of P+resonant compensators using (a) (4.21) and (b) (4.39) with $k_p=1$, $k_i=20$, $\omega=314\text{rad/s}$ and $\omega_{\text{cut}}=10\text{ rad/s}$	91
Figure 4.18. Bode plot of closed-voltage-loop of inverter A in four-wire compensator...	93
Figure 4.19. Control scheme for series four-leg inverter B (a) general representation (b) outer current loop in the negative synchronous frame.	94
Figure 4.20. Open-loop bode plot of zero-sequence control path.....	97
Figure 4.21. Simulated four-wire system waveforms of (a) mains grid voltages, (b) a-b-c frame sensitive load voltages in the microgrid and (c) α - β -0 frame sensitive load voltages in the microgrid.....	99
Figure 4.22. Simulated four-wire system line currents without series inverter B: (a) a-b-c frame and (b) negative d-q-0 frame.	99
Figure 4.23. Simulated four-wire system filtered voltages generated by series inverter B: (a) a-b-c frame and (b) α - β -0 frame (zoomed-IN view in the steady-state).....	100
Figure 4.24. Simulated four-wire system line currents with series inverter B: (a) a-b-c frame and (b) negative d-q-0 frame.	100
Figure 4.25. Simulated four-wire system waveforms of (a) real power supplied by shunt inverter A, (b) reactive power supplied by shunt inverter A, (c) real power supplied by series inverter B and (d) reactive power supplied by series inverter B.	101
Figure 4.26. Experimental four-wire system waveforms of (a) mains grid voltages, (b) a-b-c frame sensitive load voltages in the microgrid and (c) α - β -0 frame sensitive load voltages in the microgrid.....	103
Figure 4.27. Experimental four-wire system filtered voltages generated by series inverter B: (a) a-b-c frame and (b) α - β -0 frame (zoomed-IN view in the steady-state).	103
Figure 4.28. Experimental four-wire system line currents with series inverter B: (a) a-b-c frame and (b) negative d-q-0 frame.	104
Figure 4.29. Experimental four-wire system waveforms of (a) real power supplied by shunt inverter A, (b) reactive power supplied by shunt inverter A, (c) real	

power supplied by series inverter B and (d) reactive power supplied by series inverter B.	104
Figure 5.1. Single-phase representation of microgrid system under study with specific voltage phasors indicated.....	108
Figure 5.2. RL feedforward current-limiting algorithm (a) control block diagram representation and (b) implementation representation.....	111
Figure 5.3. Phasor diagrams for analyzing (a) optimal R/L ratio and (b) worst-case condition.....	113
Figure 5.4. Per-phase control block representation of flux-model control.....	116
Figure 5.5. Simplified per-phase control block representation of flux-model control. ...	117
Figure 5.6. Root locus and open-loop bode plots of flux-model control.....	117
Figure 5.7. Control block representation of flux-charge-model algorithm.....	118
Figure 5.8. Modification of (a) multi-loop voltage-current control to give (b) flux-charge-model control.	119
Figure 5.9. Closed-loop bode plot of inner charge-model.....	120
Figure 5.10. Open-loop bode plot of flux-charge-model.....	121
Figure 5.11. Closed-loop bode plot of flux-charge-model.	122
Figure 5.12. Simulated (a) sag voltages at PCC, (b) sensitive load voltages in the microgrid and (c) line currents when no current-limiting algorithm is incorporated.	124
Figure 5.13. Simulated (a) voltages injected by the series inverter and (b) line currents using the RL feedforward algorithm.....	125
Figure 5.14. Simulated power supplied by the series inverter: (a) active power and (b) reactive power using the RL feedforward algorithm.	125
Figure 5.15. Simulated (a) voltages injected by the series inverter and (b) line currents using the flux-charge-model algorithm.....	126
Figure 5.16. Simulated power supplied by the series inverter: (a) active power and (b) reactive power using the flux-charge-model algorithm.	127
Figure 5.17. Experimental (a) voltages injected by the series inverter and (b) line currents using the RL feedforward algorithm.....	128
Figure 5.18. Experimental power supplied by the series inverter: (a) active power and (b) reactive power using the RL feedforward algorithm.....	129

Figure 5.19. Experimental (a) voltages injected by the series inverter and (b) line currents using the flux-charge-model algorithm.	130
Figure 5. 20. Experimental power supplied by the series inverter: (a) active power and (b) reactive power using the flux-charge-model algorithm.....	130
Figure 6.1. Microgrid system with a single DG.....	135
Figure 6.2. Equivalent circuit of the resonant microgrid system: (a) grid-connected mode (b) islanding mode.....	136
Figure 6.3. Standard H_{∞} configuration.....	138
Figure 6.4. Singular values of $\Delta(s)$ and W_3	140
Figure 6.5. Singular values of weighting functions of : (a) W_1 and (b) $S(s)$	142
Figure 6.6. Bode plot of designed H_{∞} controller.....	143
Figure 6.7. Singular values of $1/W_1$, $1/W_3$, $S(s)$ and $T(s)$	144
Figure 6.8. PFC capacitor connected system and the double-loop control of the shunt inverter.	145
Figure 6.9. Equivalent simplified schematic of Figure 6.8.....	145
Figure 6.10. Root locus plot of V_{pf}/V_{ref}	147
Figure 6.11. Bode magnitude plot of V_{pf}/V_{ref}	147
Figure 6.12. Dual-inverter compensator for the microgrid.....	148
Figure 6.13. Control scheme of the series inverter.	150
Figure 6.14. Retrieval of line currents harmonic components.....	150
Figure 6.15. Bode plots of $G_{lp} = i_{dqf}/i_{dq}$ and $G_{hp} = i_{dqh}/i_{dq}$	151
Figure 6.16. Bode plot of G_{v1} and R'_i	153
Figure 6.17. Simulated Load1 voltages with capacitor change.	154
Figure 6.18. Simulated Load2 voltages with filter capacitor currents feedback.....	156
Figure 6.19. Simulated line currents with filter capacitor currents feedback.	156
Figure 6.20. Simulated Load2 voltages with filter inductor currents feedback.....	156
Figure 6.21. Simulated line currents with filter inductor currents feedback.....	156
Figure 6.22. Simulated Load2 voltages with filter inductor currents feedback and series compensation.	156
Figure 6.23. Simulated line currents with filter inductor currents feedback and series compensation.	156
Figure 6.24. Simulated series voltages generated by the series inverter.....	157

Figure 6.25. Experimental Load 1 voltages with capacitor change.	158
Figure 6.26. Experimental Load2 voltages with filter capacitor currents feedback.	159
Figure 6.27. Experimental line currents with filter capacitor currents feedback.	159
Figure 6.28. Experimental Load2 voltages with filter inductor currents feedback.	159
Figure 6.29. Experimental line currents with filter inductor currents feedback.	159
Figure 6.30. Experimental Load2 voltages with filter inductor currents feedback and series compensation.	159
Figure 6.31. Experimental line currents with filter inductor currents feedback and series compensation.	159
Figure 6.32. Experimental series voltages generated by the series inverter.	160
Figure 7.1 Typical series DVR circuit topology at medium voltage level	163
Figure 7.2. 10 kV experimental system setup.	164
Figure 7.3 Photos of: (a) 20-feet DVR container and step-up, step-down transformers, (b) DC supply and control system (inside the container), (c) IGBT inverter, DC link capacitor, filter circuit and bypass circuit (inside the container), (d) injection transformers (inside the container) and (e) programmable AC supply (in HV lab).	165
Figure 7.4. Overall DVR control scheme.	168
Figure 7.5. Bode diagram of an ideal P+resonant controller.	170
Figure 7.6. Singular values of $\Delta(s)$ and W_3	172
Figure 7.7. Bode plot of designed H_∞ controller.	174
Figure 7.8. Plants with closed current loop.	175
Figure 7.9. Effects of difference current regulator gains on (a) synthesized H_∞ controller and (b) final open loop system.	176
Figure 7.10. Disturbance rejection from load current to inverter output.	176
Figure 7.11. Disturbance rejection from filter inductor feedback current to inverter output.	177
Figure 7.12. Bode plot of designed P+resonant and H_∞ controller.	179
Figure 7.13. Bode plot of open loop system with P+resonant and H_∞ controller.	179
Figure 7.14. Robustness checking for H_∞ controller: (a) (b) injected and load voltages with 2/3 of system parameter values and (c) (d) injected and load voltages with nominal system parameters.	181

Figure 7.15. Robustness checking for P+resonant controller: (a) (b) injected and load voltages with 2/3 of system parameter values and (c) (d) injected and load voltages with nominal system parameters.....	181
Figure 7.16. PCC voltages: (a) with P+resonant controller and (b) with H_∞ controller.	182
Figure 7.17 Injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.	182
Figure 7.18. Load voltages: (a) with P+resonant controller and (b) with H_∞ controller.	182
Figure 7.19. Load voltages Zoom-In view: (a) with P+resonant controller and (b) with H_∞ controller.	182
Figure 7.20. Frequency spectra of injected voltage: (a) with P+resonant controller and (b) with H_∞ controller.....	182
Figure 7.21. Frequency spectra of load voltage: (a) with P+resonant controller and (b) with H_∞ controller.	182
Figure 7.22. Nonlinear load current (phase C).....	183
Figure 7.23. PCC voltages: (a) with P+resonant controller and (b) with H_∞ controller.	184
Figure 7.24 Injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.	184
Figure 7.25. Load voltages: (a) with P+resonant controller and (b) with H_∞ controller.	184
Figure 7.26. Zoom-In view of injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.	184
Figure 7.27. Frequency spectra of injected voltage: (a) with P+resonant controller and (b) with H_∞ controller.....	184
Figure 7.28. Frequency spectra of load voltage: (a) with P+resonant controller and (b) with H_∞ controller.	184
Figure 7.29. PCC voltages: (a) with P+resonant controller and (b) with H_∞ controller.	185
Figure 7.30. Injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.	185
Figure 7.31. Load voltages: (a) with P+resonant controller and (b) with H_∞ controller.	186
Figure 7.32. Negative-sequence components of the PCC and load voltages: (a) with P+resonant controller and (b) with H_∞ controller.	186
Figure 7.33. PCC voltages	187

Figure 7.34. Injected voltages.....	187
Figure 7.35. (a) Induction motor load voltages and (b) motor speed.	187
Figure 7.36. Zoom-In views of load voltage transient during (a) sag occurrence (b) recovery from a sag.....	187
Figure 7. 37. DVR connected system with downstream fault.	188
Figure 7. 38. Proposed DVR control scheme for fault current limiting.	192
Figure 7.39. Flux-charge model based control for DVR implementation.	192
Figure 7.40. Bode plot of flux open loop.....	193
Figure 7.41. Load voltages during three-phase short circuit.	195
Figure 7.42. DVR injected voltages during three-phase short circuit.....	195
Figure 7.43. Line currents (DVR side) during three-phase short circuit.	195
Figure 7.44. PCC voltages during three-phase short circuit.	195
Figure 7.45. Real and reactive power injected by DVR during three-phase short circuit.	195
Figure 7.46. Load voltages during single-phase short circuit.....	196
Figure 7.47. DVR injected voltages during single-phase short circuit.....	196
Figure 7.48. Line currents (DVR side) during single-phase short circuit.....	196
Figure 7.49. PCC voltages during single-phase short circuit.....	196
Figure 7.50. Real and reactive power injected by DVR during single-phase short circuit.	197
Figure 7.51. Control schemes of (a) single-loop feedback or feedforward+feedback, (b) double-loop control.	198
Figure 7.52. Bode plot of single voltage loop control with and without reference feedforward ($k_p=0.0125$, $2k_i=30$, $\omega_{cut}=5$. feedforward gain $k_f=1$).....	200
Figure 7.53. Bode plot of double-loop control with different inner current feedback variables (voltage controller $k_p=0.5$, $2k_i=400$, $\omega_{cut}=5$. current controller $k_C=1.2$).	201
Figure 7.54. Two-step posicast controller embedded in (a) single-loop feedback and reference feedforward control, (b) double-loop control.....	202
Figure 7.55. Two-step posicast controller.....	203
Figure 7.56. Two-step posicast response, from top to bottom: first, second, and summation steps.....	204
Figure 7.57. Bode diagram of two-step posicast controller ($T_d=0.000785s$, $\delta=98.1\%$)..	204
Figure 7.58. Three-step method.	206

Figure 7.59. Bode plot of single voltage loop feedback plus reference feedforward with posicast controller ($T_d = 0.000785s$, $T_{dI}=0.0008s$, $\delta=98.1\%$).....	207
Figure 7.60. Bode plot of double-loop feedback with posicast controller ($T_d=0.000785s$, $T_{dI}=0.0008s$, $\delta=98.1\%$).....	207
Figure 7.61. DVR injected voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.	208
Figure 7.62 Load voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.....	208
Figure 7.63. Startup transient zoom-in view of DVR injected voltages with single- loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.	209
Figure 7.64. Recovery transient zoom-in view of DVR injected voltages with single- loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.	209
Figure 7.65. Startup transient zoom-in view of load voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.....	209
Figure 7.66. Recovery transient zoom-in view of load voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.....	209
Figure 7.67. DVR injected voltages with double-loop control (linear load): (a) without posicast control and (b) with posicast control.....	210
Figure 7.68 Load voltages with double-loop control (linear load): (a) without posicast control and (b) with posicast control.....	210
Figure 7.69. Startup transient zoom-in view of DVR injected voltages with double- loop control (linear load): (a) without posicast control and (b) with posicast control.	210
Figure 7.70. Startup transient zoom-in view of load voltages with double-loop control (linear load): (a) without posicast control and (b) with posicast control.	210
Figure 7.71. DVR injected voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.	211
Figure 7.72. Load voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.	211

Figure 7.73. Startup zoom-in view of DVR injected voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.....	212
Figure 7.74. Recovery zoom-in view of DVR injected voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.....	212
Figure 7.75. Recovery zoom-in view of load voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast control.	212
Figure 7.76. Frequency spectra of DVR injected voltage with single-loop feedback and feedforward (nonlinear load): (a) without posicast control and (b) with posicast control.	212
Figure 7.77. DVR injected voltages with double-loop control (nonlinear load): (a) without posicast control and (b) with posicast control.	213
Figure 7.78. Load voltages with double-loop control (nonlinear load): (a) without posicast control and (b) with posicast control.....	213
Figure 7.79. Startup zoom-in view of DVR injected voltages with double-loop control (nonlinear load): (a) without posicast l and (b) with posicast.....	213
Figure 7.80. Frequency spectra of DVR injected voltage with double-loop control (nonlinear load): (a) without posicast and (b) with posicast.	213
Figure a.1. Configuration of SKM 50G 123D IGBT module.....	A2
Figure a. 2. Block diagram of DS1103 controller board.....	A4

List of Tables

Table 3.1. System parameters for MATLAB/SIMULINK simulation, RTDS simulation and experiment.	64
Table 3.2. Parameters of motor load used in MATLAB/SIMULINK and RTDS simulation.	65
Table 4.1. System parameters for simulation and experiment.	105
Table 5.1. System parameters for simulation and experiment.	131
Table 5.2. Summarized performance features of proposed current-limiting algorithms.	131
Table 6.1 System parameters for simulation and experiment.	160
Table 7.1 System parameters for 10 kV DVR setup.	166
Table 7.2. Parameters of induction motor load used in DVR system.	167

List of Abbreviations

ADC	Analog to Digital Converter
ASD	Adjustable Speed Drive
CHP	Combined Heat and Power
DAC	Digital to Analog Converter
DG	Distributed Generation
DITS	Digital Input Time Stamp
DPRAM	Dual Port RAM
DSP	Digital Signal Processor
DVR	Dynamic Voltage Restorer
ESS	Energy Storage System
HV	High Voltage
IGBT	Insulated Gate Bipolar Transistor
LV	Low Voltage
MV	Medium Voltage
PCC	Point of Common Coupling
PFC	Power Factor Correction
PI	Proportional Integral
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RTDS	Real-Time Digital Simulator
SMES	Superconducting Magnetic Energy Storage
SPWM	Sinusoidal Pulse Width Modulation
STS	Static Transfer Switch
THD	Total Harmonic Distortion
TPC	Tandem Processor Card
UPQC	Unified Power Quality Conditioner
UPS	Uninterruptible Power Supply
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

Chapter 1

Introduction

In last few years, small Distributed Generation (DG) systems based on micro-sources have been gaining popularity due to their higher efficiencies and lower emissions, and the technologies have already been used to [1]:

- A) Share peak generation during peak load hours when the cost of electricity is high and
- B) Provide standby generation during system outages.

The micro-sources, such as fuel cells, photovoltaic cells, small wind turbines, and microturbines etc., are low voltage, highly reliable and have electronic interfaces and reduced emission.

Despite the mentioned benefits that DG can provide, there are technical limits in reality on the degree to which DG can be connected. The distribution system was intended to cope with the conventional loads supplied by central generation, where power flows radially from the transmission network down. Changing the power flow causes problems since DG does not behave the same way as a conventional load. Therefore, nowadays, there are two main parts of technical study on DG system [2]: traditional approach is to deal with influence induced by individually connected DG system without large modification of the conventional distribution system control scheme such as in [3-6, 22]. Those issues include instantaneous disconnection of the DG in even of a system outage, prevention of islanding operating of DG, avoiding inverse power flow caused by DG etc. By contrast the other more recent topic is how to create a brand-new concept for more efficient use of the DG systems such as in [2, 7-12, 18, 21, 23-31], which leads to the new paradigm called microgrid.

The concept of microgrid is proposed in [7], where it is defined as a cluster of loads and micro-sources operating under a unified controller within a certain local area. The microgrid can then be understood as a cluster of loads and paralleled DG systems operating together. Being a systematic organization of DG systems, a microgrid has larger power capacity and more control flexibilities to fulfill system reliability and power quality requirements, in addition to all the inherited advantages of a single DG system. It also offers many opportunities for optimizing DG systems, such as Combined Heat and Power (CHP), premium power and peaking sharing, to name a few.

1.1 Motivation

As a system approach to realize the emerging potential of DG system, the microgrid would combat problems caused by the unconventional behaviors of DG system. A microgrid would present itself to the utility as an ideal conventional load or even a small generation source [8]. As a result, the microgrid can be expected to be connected to the mains utility or operated autonomously, unlike a single DG system. During a utility disturbance, the microgrid could disconnect from the system while continue serving the loads in it. Therefore microgrid benefits both the utility side and the customer side.

This new scenario of operation of a microgrid requires the development of applied research at several areas, such as proper control of the microgrid, micro-source electrical modeling, power quality and network reliability, protection coordination and personnel safety, communications, economical and electrical market driven procedures and the definition of new interconnection standards, and so on.

To exploit the potential benefits that a microgrid can provide to the customer's as well as the utility's side, a very important area of study is the development of control algorithms for the microgrid. A critical feature of the microgrid is the power electronic interface of each DG system in the microgrid. The control of microgrid mainly refers to control of each DG system in it, and this is realized by the control algorithms implemented on the interfacing inverter for each DG system. The control issues can be roughly categorized as:

- A) Basic operation function realization,
- B) Further power quality enhancement with consideration of impacts from utility grid voltage quality problems and
- C) Microgrid loads disturbances.

1.2 Objectives

The focus of this thesis is development of controllers and conditioners for microgrids and to exploit the potential benefits that a microgrid would provide to the customer's as well as the utility's side. The main objectives of this research project are given below.

1.2.1 Realization of the basic functions of microgrid operation

The basic functions of a microgrid operation include:

- A) Each DG system should be able to regulate local voltage and generate the dispatched real and reactive power when the microgrid is connected with the utility grid.
- B) When there is an interruption in the utility, the microgrid should be disconnected from the utility as fast as possible and the parallel operating DG systems should share the changed power demand automatically in a predetermined manner without communication between them.
- C) After the fault in the utility is cleared, a synchronization algorithm should be used to synchronize the microgrid with the utility and reconnect them smoothly and safely.

1.2.2 Further power quality improvement with consideration of utility voltage quality problems impacts

Due to the interfacing nature of microgrid and utility system, the microgrid is subjected to numerous utility system power quality problems, among them are voltage unbalance and voltage sags. Proper operation of the microgrid however requires careful considerations of such impacts from the utility.

- A) Utility voltage unbalance would cause microgrid voltage unbalance, which leads to motor overheating, abnormal operation of the sensitive equipment, unnecessary tripping of the loads etc. Therefore, the microgrid voltage must be controlled to be balanced even under unbalance utility voltage. The voltage difference between the well controlled balanced microgrid and unbalanced utility leads to another concern: extremely unbalance currents will flow on the line, which is harmful to the microgrid components such as transmission lines and cables. This requires that the line currents should also be controlled to be balanced to improve the interfacing current quality.

- B) Utility voltage sag is another important problem that needs to be looked into. First, voltages in the microgrid should be well-regulated to prevent tripping of sensitive loads. In this case, large fault current will flow along the interconnecting distribution feeder between the microgrid and utility system. Therefore, both voltage control scheme and fault current limiting algorithms should be developed to enable the microgrid to ride through the utility voltage sag before it is cleared (by opening of a circuit breaker).

1.2.3 Robust performance under microgrid load disturbances

Being a larger system also means that the microgrid would easily be disturbed by the numerous power apparatuses connected within its vicinity. Satisfactory operating

performance of a microgrid requires that the voltage in the microgrid should be robustly controlled under any kinds of loads in it.

- A) The microgrids are possibly at low voltage distribution level with four-wire configuration to accommodate single-phase loads [8]. To meet the requirements of three-phase four-wire systems, a proper interfacing converter topology should be employed for each DG. The load voltage may be unbalanced due to the uneven distribution of single-phase loads or asymmetries in the wiring. Therefore a suitable control strategy should be designed to guarantee voltage quality even with an unbalanced system.
- B) Capacitive loads such as power factor correction (PFC) capacitors are widely used for improving system efficiency. When a capacitive load is connected in the microgrid, it may change the system parameters and hence performance degradation of the designed DG controller or even cause resonance in the system. Therefore the control algorithms with consideration of the system parameter variation and resonant attenuation should be developed.
- C) At the distribution side, a large number of nonlinear loads such as electronic devices with nonlinear characteristics could be installed. The nonlinear currents drawn by these loads will cause line heating, voltage distortions etc. When the harmonic currents have a frequency near the inverter output filter cutoff frequency, the nonlinear loads could continuously excite the filter LC resonance. Therefore the impacts of nonlinear loads should also be investigated.

Note that the development of microgrid control algorithms are challenging, since most of these control issues have not been actively addressed in DG literature so far.

1.3 Major Contribution of the Thesis

The main contributions of this research work can be summarized as follows:

1.3.1 A unified controller for realization of all the basic functions of a microgrid

A multi-functional unified controller for use with each DG system in the microgrid is proposed. The proposed controller contains inner current and voltage loops for regulating the grid-interfacing inverter, and outer real and reactive power loops for controlling the flow of power within the microgrid with particular attention focused on the proper sharing of changed power demand between the DG systems when a utility fault occurs and the microgrid islands. The proposed controller also incorporates algorithms for synchronizing the microgrid with the utility system once the fault is cleared and the microgrid is on the verge of transiting from islanding to grid-connected mode.

1.3.2 Three-phase three-wire grid-interfacing compensator for utility voltage unbalance

To control both the sensitive load voltages in the microgrid and the line currents flowing between the microgrid and utility system during a utility voltage unbalance, a dual-inverter three-phase three-wire grid-interfacing power quality compensator (with a shunt connected inverter and a series connected inverter) are proposed for each DG system. In each inverter, both positive- and negative-sequence components are controlled to compensate for the effects caused by the unbalanced utility grid voltages. Specifically, the shunt inverter is controlled to ensure balanced voltages within the microgrid under unbalanced utility voltage or unbalanced loads, to regulate power dispatches among parallel-connected DG systems and to incorporate synchronization algorithms for ensuring smooth and safe reconnection of the microgrid and utility. On the other hand, the

series inverter balances the line currents by injecting only negative-sequence voltage components with zero real and reactive power injection.

1.3.3 Three-phase four-wire grid-interfacing compensator for utility voltage unbalance

To accommodate the possible four-wire microgrid system configuration, a three-phase four-wire grid-interfacing power quality compensator for microgrid applications is proposed. This topology is similar to the three-wire dual-inverter compensator except that two four-leg inverters (a shunt and a series) are employed instead of three-leg inverters. Using four-leg inverters, the compensator would compensate for all the unwanted positive-, negative- and zero-sequence voltage/current components exist due to an unbalanced utility grid or unbalanced loads. Similarly the shunt four-leg inverter is controlled to ensure balanced voltages within the microgrid as well as other basic functions of microgrid operation. The series inverter is controlled complementarily to inject negative- and zero-sequence voltages in series to balance the line currents, while generating zero real and reactive power.

1.3.4 Fault current limiting algorithms for use in utility voltage sag

To prevent the flow of large line currents and hence protect the microgrid during an utility voltage sag, two current-limiting algorithms, termed as RL feedforward and flux-charge-model feedback algorithms, are proposed and integrated within the dual-inverter grid-interfacing compensator control schemes. The algorithms are developed based on different control principles, but respond similarly by controlling the series inverter to act like a large virtual RL or L impedance to limit the line current flow during a sag.

The RL algorithm functions by controlling the series inverter, connected between the microgrid and the utility, to insert a large virtual RL impedance along the distribution feeder to limit the line currents and damp transient oscillations with a non-zero active

power circulating through the series and shunt inverter. In contrast, the alternative flux-charge algorithm inserts only a virtual inductive impedance with zero active power absorption and relies on its closed-loop control tuning to damp transient oscillations. Detailed descriptions of the algorithm theoretical principles, controller designs and parameter selection criteria are discussed. Phasor analyses of both methods are presented to show how the inserted RL or L values can be optimally tuned to improve the inverter damping performance, and minimize its injected voltages and circulating power under all operation conditions.

1.3.5 Robust control of microgrid with capacitive loads

Being a larger system also means that the microgrid can easily be disturbed by the numerous power apparatuses connected within its vicinity. In particular, the switching of PFC capacitors can cause system parameter variations, and hence performance degradation of the designed DG controller. The presence of PFC capacitors would also result in high resonant voltages and currents.

To address these complications, an integrated control algorithm, comprising of a H_∞ voltage controller, an inner filter inductor current feedback controller and a virtual-resistance compensator is proposed for operating the microgrid with reduced parameter sensitivity and improved damping performance. By properly selecting the weighting functions, the synthesized H_∞ controller would have high gains at the vicinity of the line frequency, and can thus have nearly zero steady-state error with its degree of robustness explicitly specified. An evaluation of filter inductor and filter capacitor inner current control options is also carried out. It is shown that filter inductor current control is more effective in resonant damping caused by the PFC capacitors connected in the microgrid. For DG systems with dual-inverter compensator, a virtual-resistance compensator for controlling the series inverter to further dampen the system resonance is also proposed. The series inverter is controlled to resist only harmonic components without affecting the fundamental power flow.

1.3.6 Investigation and improvement of transient response

Methods to improve inverter voltage transient are also investigated and an effective technique is developed. For typical inverter and filter topology, the filter circuit (LC filter or LCL filter) designed to eliminate the high frequency inverter switching noises, will introduce a lightly damped plant model and initiate LC resonance under a sudden change of reference. The widely used nonlinear loads, with high frequency harmonic currents which have frequencies around the LC filter cutoff frequency, will continuously excite the LC resonance. For conditioning the supplied power and damping high frequency oscillations simultaneously, an investigation on the transient response is carried out. Different classical control schemes and their effect on the oscillation attenuation are studied. An effective and simple resonance damping method is proposed by employing closed loop (single-loop or multi-loop) control and an embedded two-step posicast controller. It is commented that the proposed method is equally applicable to both the shunt and series inverters used for microgrid voltage conditioning, although it is only designed and implemented on a series inverter in this work.

1.3.7 Verification of the developed control algorithms

All the proposed control algorithms and compensators are tested experimentally in a low voltage laboratory microgrid prototype (except the transient improvement method, which is tested on a medium voltage series inverter system), after simulated using off-line computer simulations and on a designed real-time implementation platform (comprising a real time digital simulator (RTDS) and an external DSP control board). Part of the work (P+resonant controller, robust control method, fault current limiting algorithm and transient improvement method) is further successfully implemented on a grid-interfacing series inverter at 10kV medium voltage level in a high voltage test laboratory.

1.4 Organization of the Thesis

This thesis is composed of eight chapters including this introductory chapter. They are arranged as follows:

Chapter 2 presents the microgrid concept. After a brief introduction of DG system and background technologies such as generating technologies and energy storage technologies, an example structure of microgrid is presented. The operation modes, control issues, and possible application areas of the microgrid are discussed.

Chapter 3 proposes a unified controller for realization of all the basic functions of microgrid. It is designed to implement on each DG system in the microgrid. By regulating the DG output voltage, the proposed controller controls power flow in the grid-connected mode of operation, enables real and reactive power sharing between the parallel-operating DG systems when the microgrid islands, and re-synchronizes the microgrid with the utility before reconnecting them. The proposed controller would respond fast, allowing the controlled microgrid to transit smoothly between the grid-connected and islanding modes without disrupting critical loads connected to it. The performance of the proposed controller has been tested extensively in simulation using MATLAB/SIMULINK software and a real-time digital simulator (RTDS) and experimentally using a scaled hardware prototype.

In Chapter 4, two new grid-interfacing dual-inverter power quality compensators (a three-phase three-wire compensator and a three-phase four-wire compensator) for microgrid applications are proposed. Controlled properly, the proposed dual-inverter compensators, using a shunt and a series inverter, would enhance both the quality of power within the microgrid and the quality of currents flowing between the microgrid and utility system under utility voltage unbalance or microgrid load unbalance. Functionally, the shunt inverter is controlled to maintain a set of balanced, distortion-free voltages within the microgrid as well as realizing all the basic functions of a microgrid. To complement, the series inverter is controlled to inject negative-sequence (and zero-sequence for the four-leg compensator) voltages in series to balance the line currents, generating zero real and

reactive power during compensation. The proposed compensators have been tested in simulations and experimentally using a laboratory hardware prototype.

Chapter 5 presents RL feedforward and flux-charge-model feedback algorithms for protecting utility-interfaced microgrids from large line currents during utility voltage sags. To assist in choosing the appropriate algorithm for different applications, this chapter presents detailed descriptions of the algorithm theoretical principles, controller designs and parameter selection criteria. Phasor analyses of both methods are presented to show how the inserted RL or L values can be optimally tuned to improve the inverter damping performance, and minimize its injected voltages and circulating power under all operation conditions. A comparison table summarizing performance features of both algorithms is also presented. Both methods have been tested in simulation and experimentally using an emulated laboratory microgrid system.

In Chapter 6, an in-depth study is carried out for a microgrid with PFC capacitor installed. The study reveals that the effective inverter filter capacitance would be changed when a PFC capacitor is connected to a local load of a DG system. Also, resonance can occur in islanding mode of the microgrid operation due to the connected PFC capacitor. An H_∞ controller is designed to have high gains at the vicinity of line frequency, while providing explicit robustness in face of the filter capacitance variation. For the resonance situation, a thorough analysis is carried out to show that inner filter inductor current feedback method is more effective for the resonance damping than filter capacitor current feedback. Further damping is achieved by employing the dual-inverter microgrid conditioner proposed in Chapter 4. The series inverter, acting as a virtual harmonic resistor, is effectively controlled. This method has been tested in simulation and experimentally using an emulated laboratory microgrid system.

In Chapter 7, part of the proposed work is implemented on a 10kV medium voltage level system. The experiments are conducted during an overseas research attachment at the Institute of Energy Technology at Aalborg University, Denmark. The proposed P+resonant controller (in Chapter 4) and H_∞ robust controller (in Chapter 6) (with a comparative approach), and flux-charge-model fault current limiting algorithm (in

Chapter 5) are successfully tested on a series connected voltage source inverter in a high voltage test laboratory, with satisfactory results obtained. This further verifies the performance of the proposed control algorithms. In addition, a transient improvement method for inverter voltage regulation is also developed during the stay at Aalborg University and verified on the series inverter at medium voltage level. The investigation of LC oscillatory transient response caused by the inverter filter circuit and transient improvement methods using medium voltage experimental setup are therefore explained in Chapter 7.

Finally, Chapter 8 concludes the research work and proposes future research topics based on the achievements of this work.

Chapter 2

The Microgrid Concept

In the last few decades, the traditional power system witnessed an evolutionary change in the conventional centralized operation due to the emergence of smaller generating systems, such as microturbines, connected to the medium voltage and low voltage distribution levels. This change has opened new opportunities for on-site power generation by electricity users. In this context, distributed generation (DG) at the customer's side is developed as a promising option to meet the growing customer needs for electric power with an emphasis on reliability and power quality [8]. More recently, due to the economical, technological and environmental reasons, the concept of microgrid has gained popularity, which is a cluster of loads and micro-sources operating under a unified controller within a certain local area [7]. This chapter introduces the concept of microgrid as well as the background technologies which are needed to form a microgrid. Some potential impacts on the microgrid control caused by the utility power quality problems and microgrid loads are also addressed and the control issues for the microgrid are discussed at the end.

2.1 Introduction

2.1.1 Distributed generation

Distributed generation (DG) is an electric power generation source that is connected directly to the distribution network or on the customer side of the meter [13]. Today distributed generation encompasses a wide variety of new and emerging technologies that utilize an equally wide array of micro-sources (or distributed energy sources), including fuel cells, photovoltaic cells, wind turbines, and microturbines, etc. Those micro-sources offer competitive generation options and promise better economics with high reliability, high efficiency and reduced emissions. Another contributing factor is their power

electronic interface, which provide flexible interface to the utility grid. A background introduction of the micro-sources is given in Section 2.2.

Actual benefits of DG applications can be broken up into a few categories such as: customer benefits, supplier benefits, and general benefits [10].

From the customer point of view, DG application benefits can be described as:

- Ensures reliability of energy supply, especially when interruption of service is unacceptable.
- Provides the power quality needed in many industrial applications.
- Offers efficiency for on-site applications by avoiding line losses.
- Used for combined heat and power (CHP) or cogeneration applications and significantly increase the overall efficiencies.
- Enables savings on electricity rates by self generation during high-cost peak power periods.
- Allows power to be delivered in environmentally sensitive areas by having characteristically high efficiency and near zero pollution emissions.

DG system would also benefit the supplier; those benefits can be listed as:

- Limits capital risk because of the size, siting flexibility and rapid installation time.
- Avoids major investments in transmission and distribution system upgrades by providing generation at the customer side.
- Offers relatively low cost entry point into a competitive market.

For the general benefits, DG system would:

- Respond to increasing power demands and pollution emission concerns while providing low cost, reliable energy.
- Reduce emissions through efficiency gains and potential renewable resource use.

- Enhance productivity through improved reliability and quality of power delivered.

Figure 2.1. Single line diagram of: (a) traditional radial power system and (b) power system with the inclusion of DG.

Despite the above mentioned benefits provided by DG, there are technical limits in reality on the degree to which DG can be connected. Indiscriminate application of individual DG systems can cause as many problems as it may solve [12]. This is because the distribution system was intended to cope with the conventional loads supplied by central generation, where power flows radially from the transmission network down as shown in Figure 2.1(a). Changing the power flow causes problems since DG does not behave the same way as a conventional load (Figure 2.1(b)). The problems of connecting DG can be summarized as [3, 5, 14, 19]:

- Steady-state or transient over/under voltages at the point of connection due to sudden connecting or disconnecting DG.
- Protection malfunctions such as breaker reclosing problem, over-current protection relaying interference etc.
- Increase short current levels.
- Possible power quality problems, such as voltage flickers and harmonics.
- Impact on power system dynamics.
- Damage (to customers or DG itself) or safety (public or utility personnel) concern of islanding operation of a single DG.

2.1.2 Microgrid concept

To find a better way to realize the emerging potentials of DG, more recently, a new paradigm called microgrid is presented. This brand new concept is becoming more attractive, since it can optimally group DG systems for higher efficiency, reliability and flexibilities, and at the same time, minimize the potential problems caused by an individual DG system.

The concept of microgrid is proposed in [7], where it is defined as a cluster of loads and micro-sources operating under a unified controller within a certain local area. The microgrid can thereby be understood as a cluster of loads and paralleled DG systems operating together. Being a systematic organization of DG systems, a microgrid has larger power capacity and more control flexibilities to fulfill system reliability and power quality requirements, in addition to all the inherited advantages of a single DG system. It also offers many opportunities for optimizing DG systems, such as CHP, premium power and peaking sharing to name a few.

As a system approach to realize the emerging potential of DG system, the microgrid can combat problems caused by the unconventional behaviors of a single DG system. A

microgrid can present itself to the utility as an ideal conventional load or even a small generation source [8]. The microgrid can be expected connected to the mains utility or be operated autonomously, unlike a single DG system. During a utility disturbance, the microgrid can disconnect from the system while continue serving the loads in it. As a result, microgrid benefits both the utility side and the customer side. More discussions of the microgrid structure and operation are given in Section 2.4.

This new scenario of operation of a microgrid requires the development of applied research in several areas, such as proper control of the microgrid, micro-source electrical modeling, power quality and network reliability, protection coordination and personnel safety, communications, economical and electrical market driven procedures and the definition of new interconnection standards, etc. This thesis aims to exploit the potential offered by the microgrid with a focus on the development of control schemes for the microgrid.

2.2 Background Technologies

The background technologies for proper operation of a microgrid include generating technologies, storage technologies, interfacing and control technology. A typical DG system based on micro-source depicted in Figure 2.2 illustrates that the micro-source generation involves all the generation, storage, interfacing and control technologies. A most distinguishing feature of the microgrid is its power electronics interfaces as shown in Figure 2.2. All the power, DC or non-power frequency AC, generated by each DG in the microgrid must use an electronic inverter to interface with the electrical power system. This power electronic interface provides significant flexibilities and permits the microgrid to function as a semi-autonomous power system. Control of the microgrid mainly refers to the control of the interfacing power electronic inverters, which is presented in detail through Chapter 3 to Chapter 6. In this section the generating and storage technologies are briefly described.

Note that the DG systems in this work mainly refer to those based on micro-sources. DG systems based on conventional generators (instead of micro-sources) and interfaced to the utility system through synchronous motors and induction motors are usually not considered for microgrid.

Figure 2.2. Typical diagram of micro-source generation system.

2.2.1 Generation technologies

The generating technologies of microgrid would include the following [8, 14]:

Microturbines

Microturbine is a new combustion turbine technology. The major advantages of this technology are its compact packaging and low emissions. Microturbines are mechanically simple, single shaft, permanent magnet devices, using high-speed (10000 to 100000 rpm) typically with airfoil bearings. They are normally in sizes of 30 to 75 kW, which are most commonly matched to small commercial loads. Its generation efficiency is 25 to 30 percent. However, when coped with an appropriate thermal load, net energy efficiencies exceeding 60 percent can be achieved [14]. This technology is best suited for CHP applications. The microturbine output is rectified to DC voltage and fed into an inverter that interfaces with the AC power system.

Fuel cells

Fuel cells are well suited for DG and microgrid. A fuel cell is basically a battery powered by an electrochemical process based on the conversion of hydrogen. This technology also occupies a relatively small space, is very quiet, and has virtually no harmful emissions during operation, but is currently expensive. Fuel cells are efficient generators and maybe employed in CHP applications to achieve among the very best possible energy-conversion efficiencies. Output of a fuel cell is DC voltage, and an inverter is required for interfacing to the power system.

Renewable generation

Renewable generation could also appear in microgrids, especially those interconnected through power electronics interfaces, such as photovoltaic systems, wind turbines etc.

2.2.2 Energy storage technologies

Unlike conventional generators such as synchronous and induction generators, DG units (based on micro-sources) have low inertia, and they do not have sufficient energy storage capacity to meet immediate demand of loads in the transient. Therefore storage technologies are important components of microgrids. Storage on the micro-source's DC bus provides ride-through capabilities during system changes.

The energy storage systems (ESS) have become more versatile recently. Storage technologies suitable for microgrid can be roughly described as:

DC capacitor banks

Large capacitor banks made up of individual capacitors connected to form a number of separate units are one solution to provide energy storage requirement. The capacitors for the energy storage are charged from the micro-source generation. Storage on the DC bus provides the power required by microgrid operation. But due to the storage capacity, capacitor banks are rarely used solely to store energy for a DG. Usually they are

connected to the DC bus as part of the regulated DC bus energy storage system (Figure 2.2).

Batteries

Batteries are the traditional method of storing electrical energy. The cost of the battery energy per kJ is much cheaper than that of capacitors. The internal impedance of the battery is much higher than that of a capacitor. Therefore it has a larger discharging time which results in longer time to provide required amount of power. The lead-acid batteries, available in almost any size, are used in many applications that require back-up power. But the lead-acid batteries contain materials which have adverse effects on the environment and require regular maintenance to guarantee high reliability [15]. These factors may lead to increase the cost of battery energy storage.

Supercapacitors

A supercapacitor can be considered as a complementing device that improves the power density of a battery or energy density of a traditional capacitor [16]. The internal impedance of this device is greater than that of capacitor and less than that of a battery. Therefore the discharging time of a supercapacitor is faster than a battery and could handle fast load changes in a microgrid. The main disadvantage of these devices is that they are only available for voltages of few volts (1 V, 2.5 V). Therefore a large number of supercapacitors need to be connected in series to get a higher voltage.

Flywheels

Another energy storage is the fast-spinning flywheel energy. Flywheels systems now incorporate composite rotors, magnetic bearings and advanced power electronics. Flywheel store energy in high-speed (up to 100000-rpm) rotating wheel-like rotors or disks connected to motors. Energy stored in flywheel is in kinetic form. High-speed rotation is important, since the flywheel energy is proportional to the square of the rotational speed. Flywheel systems come in a wide range of sizes with differing discharge rates for different amounts of time. A flywheel can be discharged at high power (kW) for a short time or at a slower rate for a longer period. Flywheels contain no hazardous

materials and are not affected by temperature extremes as batteries are, but flywheels are costly and cannot store energy indefinitely.

Superconducting magnetic energy storage system (SMES)

Superconducting magnetic energy storage system (SMES) converts the AC electrical current to DC current flowing in a superconducting coil and store the energy in the form of magnetic field [36]. As there is no conversion of energy to other forms involved, the overall efficiency of the energy storage system of SMES is very high. The major energy loss in this system results from the need to cool the coil to very low temperatures. Power electronic interfaces charge and discharge the superconducting coil. Most commercial systems are larger than 250kW in capacity and could be adapted to relatively larger microgrid applications.

2.3 Application of Microgrids

Depending on the locations and capacities of DG units in the power system (see Figure 2.1(b)), a microgrid could be operated at medium voltage [24] or at low voltage distribution level [18, 27]. Operating at medium voltage level needs larger capacity and wind turbine is a suitable energy source. Whilst a more possible location for microgrid is at low voltage level, since most of the micro-sources is of relatively low power with capacity around several hundred kW.

The microgrid may take the form of an industrial site (comprising factories, warehouses and offices) [18], shopping center, or college campus [31]. Incorporating combined heat and power (CHP) in to the application of microgrid is a recent and significant effort [30].

The main components of the CHP system include: an engine which drives an electricity generator, a generator, which produces the electricity, a heat recovery system, to recover the waste heat from the engine, a control system, and an exhaust system and an acoustic enclosure. CHP applications are generally sized by reference to their electrical output.

The capacity of CHP ranges from small commercial or domestic premises (under 0.03 MW) to medium sized industrial sites or large building heating systems (around 20 MW) and can extend to power station size plants with electricity fed into the grid and heat supplied as steam to large industrial sites or large communal heating systems (with a capacity > 100 MW).

Because typically half to three-quarter of the primary energy consumed in power generation is ultimately released unutilized to the environment, the potential benefits using CHP applications are significant, which can be described as:

- Significantly increase the overall energy generation efficiency.
- Reduce overall energy costs.
- Benefit the environment by reducing or eliminating the power plant waste heat disposing.

Figure 2.3. CHP versus separate heat and power energy flows (adapted from [30]).

Figure 2.3 shows the typical fuel input needed to produce 35 units of electricity and 50 units of heat using conventional separate heat and power. For typical electrical and thermal efficiencies, CHP is nearly twice as efficient.

Unlike electricity, heat, usually in the form of steam or water, cannot be easily or economically transported long distance. As a result, CHP systems typically provide heat for local use. When a microgrid is implemented in form of CHP applications, more benefits can be generated [8, 12]:

- The production of heat can move closer to the point of use. Because electricity is more readily transported than heat, generation of heat close to the location of the heat load will usually make more sense than generation of heat close to the electrical load, and the microgrid permits generators to be placed optimally in relation to heat loads.
- The scale of heat production for individual units is small and therefore offers greater flexibility in matching to heat requirements. A microgrid could be constructed from the most economic combination of waste-heat-producing generators and non-waste-heat producing generators so that the combined generation of electricity and heat is optimized.

2.4 Example Microgrid Structure

The microgrid structure assumes a cluster of DG systems and loads operating as a single system providing power and heat. As stated, a critical feature for DG systems in the microgrid is the power electronic interfaces, which can provide powerful control flexibilities to realize the optimal operation of a microgrid as a single system.

An example structure of microgrid is shown in Figure 2.4. The microgrid is connected to the utility system through a separation device, usually a static transfer switch (STS), at the Point of Common Coupling (PCC). The STS would ensure that the grid can be disconnected from the microgrid within half a line frequency cycle in event of a utility interruption (in addition to the time required for detect the fault).

Figure 2. 4 Basic microgrid structure.

As shown in Figure 2.4, three DG systems and a collection of loads are employed. Each DG system comprised of micro-source energy (microturbines, fuel cells, photovoltaic systems etc.), energy storage devices for DC voltage supply, and an interfacing inverter. DG system 1 is connected near a heat load for CHP application. DG system 3 is connected near a critical load for both voltage regulation and power flow control. DG system 2 is connected to the feeder directly for voltage and power support. Each bus in the microgrid has one or more circuit breakers (S) for protection of faults in the microgrid. This microgrid structure allows the line losses reduction, local voltage and power support and waste heat usage. Comparing with all the DG connected to the PCC, this kind of structure (micro-sources on a radial feeder) increases the problem of power flow control and voltage support along the feeder. Therefore the “plug and play” concept [8] is key to this arrangement which is discussed in Section 2.5.

The microgrid has two modes of operation, namely **grid-connected mode** and **islanding mode**. In grid-connected mode operation, the microgrid is connected to the utility, and the DG systems in the microgrid provide heat and local voltage support for the nearby loads and, if the capacity of the microgrid permits, the non critical loads at the PCC. As a

consequence of this, the burden of power generation and delivery of the utility system can be shared; the power losses on the feeder can be reduced. When there is an interruption in the utility system, microgrid is disconnected from the utility as fast as possible and pick up the loads and operate in islanding mode. Thus an uninterruptible power supply (UPS) function is achieved. Also, the noncritical loads can be shed if the capacity of the microgrid is limited.

The flexibility of advanced power electronics that control the DG systems enables the microgrid benefit both the utility and the customers. Besides reducing the burden of generation and transmission in the grid, the microgrid is a single controlled entity from the grid perspective [8]. It can be regarded as a load, or most possible, a dispatched load. Even it might be a small generation source. Microgrid would also help the customers in terms of increase in reliability, power quality and efficiency, to name a few.

There are three parts critical to the microgrid structure:

DG controller

The systematic organization and operation of DG systems are realized by proper control for each DG unit. Controller for each DG system should be able to regulate the voltage, generate the dispatched power in grid-connected mode of microgrid operation, and share the changed power demand automatically in islanding operation. Also those controllers should ensure smooth connection of the microgrid and the utility system as well as enable the microgrid to withstand the impacts from utility power quality problems and load disturbances.

Energy manager or microgrid central controller

The energy manager provides for system operation of microgrid through dispatching real and reactive power to each DG system controller during grid-connected mode of operation. Some possible criteria of the dispatched power are: ensure that necessary heat and electrical loads are met by the DG, ensure that the microgrid satisfies operational contract with the bulk power provider, minimize emission and system losses and

maximize operational efficiency of the DG, etc. The energy manager is also in function during synchronization process by providing the utility voltage information to each DG controller. In islanding operation, proper controlled DG systems in the microgrid should be able to share the changed power demand without the energy manager by using a predefined manner according to each DG capacity and the dispatched power in grid-connected mode.

Protection

Protection system of the microgrid must respond to both mains and microgrid faults. When the fault is in the utility system, the desired reaction of microgrid is to disconnect from the utility as fast as possible and protect the load in it. When a fault occurs in the microgrid, the minimum part of the feeder should be cut from the microgrid.

2.5 Control Issues for the Microgrid

As mentioned above, with correctly designed power electronics and controllers, microgrid should be able to fulfill customers' and utilities' requirements. Furthermore, realistically, it would not be appropriate to assume that when the microgrid is connected with the grid, the utility voltage to be ideal; and similarly when in islanding operation, the DG systems in the microgrid act as ideal voltage sources. Relevant control schemes are required for the microgrid to withstand the power quality problem impacts from the mains as well as load impacts from the microgrid. Therefore special attention must be paid to the development of controllers for the microgrid.

The control issue is divided here into three parts: basic operation requirements, utility voltage quality problems compensation and proper control under load disturbances.

2.5.1 Basic operation requirements

The basic operation of a microgrid requires the controllers of DG systems have the following functions:

- A) When the microgrid is connected to the power system grid and operates in grid-connected mode, the DG systems in the microgrid should be able to regulate the local voltages and accurately control the dispatched real and reactive power flows on the feeders.
- B) The DG systems must be able to share the changed power demands automatically when an interruption occurs in the utility and the microgrid operates in islanding mode.
- C) When the fault in the utility is cleared and the microgrid is ready to be reconnected to the utility, the control scheme should be able to synchronize the microgrid with the power system and reconnect them smoothly.

An important aspect is that controllers should use the information available locally and obtain the above function in a predetermined manner without communication between the paralleled operating DG systems. This is important as the DG system thus can have a “plug-and-play” characteristic [8], which means that a new DG unit can be added to the microgrid without changing the control or protection scheme of the ones already in it.

2.5.2 Impacts from utility voltage quality problems

Due to nature of interfacing of microgrid and utility system, the microgrid is subjected to numerous power quality problems which could occur in the utility system such as PCC voltage unbalance and voltage sags. On the other hand, as the number of DG units connected to the mains grid tends to increase tremendously, the simultaneous disconnection of DG units under fault conditions may lead to a reduction in power dispatch and an increase in system instability. Therefore it is essential that the DG

systems are kept connected during disturbances to support the mains grid [55]. To facilitate this additional requirement, the power converter units must be equipped with embedded fault tolerance capabilities and appropriate control algorithms for the microgrid should be developed to enable the microgrid to ride through the PCC voltage disturbances.

Interruptions

Interruptions can be categorized as sustained interruptions and short interruptions. When the supply voltage has been zero for a period of time in excess of 1 minute, this long-duration voltage interruption is considered as sustained interruption. Sustained interruptions are often permanent and require human intervention for system restoration. Short interruptions are complete loss of voltage (<0.1 pu) on one or more phase conductors for a time period less than 1 minute. The causes of short interruptions are fault clearing by the protection, incorrect protection intervention etc. During a PCC voltage interruption the microgrid must be disconnected from the utility as quickly as possible and operate in islanding mode to protect critical loads in it.

Voltage unbalance

Voltage unbalance (also called voltage imbalance) is usually expressed in percent. But it is defined differently in different standards. For example, sometimes voltage unbalance is defined as the maximum deviation from the average of the three-phase voltages or currents, divided by the average of the three-phase voltages or currents. In this thesis, the definition as the ratio of negative-sequence components to the positive-sequence components is adopted. The primary source of voltage unbalance of less than 2 percent is caused by single-phase loads on a three-phase circuit. Blown fuses in one phase of a three-phase capacitor bank would also result in voltage unbalance. Severe voltage unbalance (greater than 5 percent) would result from single-phasing condition [14].

If the unbalance is serious the switch will open and the microgrid is forced to operate in islanding mode. But when the voltage unbalance is not so serious, the separation device keeps closed and that results in a sustained unbalanced voltage at the PCC. Such imbalance causes motor overheating, abnormal operation of the sensitive equipment,

unnecessary tripping of the loads, to list a few. During the PCC voltage unbalance, the DG system output voltages must be maintained to be balance for local voltage support. This will then result in extremely unbalanced line currents due to the low line impedance, which will harm the system components in the microgrid such as transmission lines and cables. Therefore, the quality of current flowing between the microgrid and the utility system should also be considered. The compensation of such an unbalanced utility voltage using a proposed dual-inverter microgrid compensator is discussed in Chapter 4, where the unbalance of PCC voltage is considered as serious as 10%.

Voltage sags

Voltage sag (or voltage dip) is a decrease in rms voltage or current (0.1 pu to 0.9 pu) at the power frequency typically for a duration of 0.5 cycles to 1 minute. The causes of the voltage sags are local and remote faults in the power system, switching of large induction motor loads etc. Usually, the utility voltage can dip to 80% of its nominal value when a motor is started within its vicinity. A deeper dip could be caused by the occurrence of a single-line-to-ground fault (as deep as 20% of the nominal value [14]). In [15], it is assumed that the typical worst-case voltage sag scenario is a utility voltage dip of 50% and phase angle jump of $\theta = -60^\circ$.

The voltage sag, even for a short period, if not considered seriously will have a damaging impact on semiconductor devices in the inverters and the system components in the microgrid such as overhead lines and cables etc. This is because the large voltage difference between the microgrid and the utility (assuming that voltages in the microgrid are well-regulated to prevent tripping of sensitive loads) will cause extremely high current flowing on the lines due to the low line impedance. To prevent the flow of large line currents and hence protect the microgrid, proper control method should be implemented. The voltage sag effects and the compensation method are discussed in Chapter 5, where the worst case voltage sag scenario reported in [15] is considered.

Voltage swells

Voltage swell is an increase (1.1 pu to 1.8 pu) in rms voltage or current at the power frequency for duration from 0.5 cycle to 1 min. When a single-line-to-ground fault occurs in the power system, voltage of the healthy phases can rise (swell) above the nominal voltage. Swells can also be caused by switching off a large load or energizing capacitor bank. Similar to voltage sag, a PCC voltage swell will also cause large current flow between the microgrid and the utility system. Similar compensation method as used for voltage sag compensation might be able to take effect in a voltage swell too. This is worth for further research.

Harmonic distortions

Harmonics distortion is defined as a distortion where the waveform is non-sinusoidal but periodic with a period equal to the period of the power system frequency (50 or 60 Hz) [17]. Harmonic distortions originate in the nonlinear characteristics of devices and loads on the power system. Harmonic voltage at PCC could cause harmonic line current to be generated, which would cause line heating or even will excite system resonance when the harmonic frequency becomes close to the system natural frequency. So this is another interesting research area.

2.5.3 Load impacts in the microgrid

As mentioned, the DG system output voltage should not be assumed as ideal and the load impact in the microgrid should be considered. Good voltage control performance should be achieved under any possible loads in the microgrid.

Unbalanced loads

The microgrids, which are located at the distribution side, are possibly fed with a low voltage with four-wire configuration to accommodate single-phase loads [8]. To meet the requirements of three-phase four-wire system, proper electronics converter topology should be employed. The load voltage may be unbalanced due to the uneven distribution

of single-phase loads or asymmetries in the wiring, and suitable control strategy should be designed to deal with unbalanced loading effects.

Capacitive loads

Capacitors are widely used for power factor corrections (PFC) in power system. When a PFC capacitor is connected in parallel with a load in the microgrid, it may cause system parameter variations. The presence of PFC capacitors can also result in high resonant voltages and currents, which can damage semiconductor devices and other power equipment. Therefore the control issues such as system parameter variation and resonant attenuation should be considered.

Nonlinear loads

At the distribution side, a large number of nonlinear loads such as electronic devices with nonlinear characteristics could be installed. The nonlinear currents drawn by these loads will cause line heating, voltage distortions, resonant etc. Therefore the influence of nonlinear loads on the microgrid is also an important issue.

2.6 Discussion

This chapter introduces the microgrid concept. As a systematic organization of DG systems, the microgrid has more capacity and control flexibilities to fulfill system reliability and power quality requirements, in addition to all the inherited advantages of a single DG system. As a system approach, the microgrid would also be able to combat problems caused by the unconventional behaviors of single DG systems. Background technologies which enable to form a microgrid are briefly introduced. An example microgrid structure is presented. Furthermore, potential impacts from both utility and microgrid loads are discussed and the control issues of microgrid are addressed. The development of the control algorithms are challenging, since most of these control issues do not exist in currently available DG control literature. In this thesis, the control issues of basic microgrid operation, utility power quality impact (such as voltage unbalance,

voltage sag) compensation, and microgrid loads disturbance (such as unbalance and capacitive loading impacts) rejection are addressed for the microgrid control scheme design. The development and implementation of the microgrid control schemes are presented in the following chapters.

Chapter 3

A Multi-Functional Unified Controller for Microgrid

3.1 Introduction

As discussed, proper operation of the microgrid in both the grid-connected and islanding modes requires the implementation of high performance power flow control and voltage regulation algorithms. The implemented control algorithms should preferably have no communication links between the paralleled DG systems, which would be located far apart. Thus, the control algorithms of each individual DG system should be designed to use only feedback variables that can be measured locally and to exhibit “plug and play” characteristics. Other desired performance features include the appropriate sharing of changed power demand in a predetermined manner between the paralleled DG systems when a utility fault occurs and the microgrid islands, and the proper re-synchronization of the microgrid and utility grid for smooth reconnection when the fault is cleared.

To realize the aforementioned performance features, a new unified controller for use with each DG system in the microgrid is proposed in this chapter. By regulating the output voltage, the proposed controller controls power flow in the grid-connected mode of operation, enables real and reactive power sharing between the parallel-operating DG systems when the microgrid islands, and re-synchronizes the microgrid with the utility before reconnecting them. The presented controller would respond fast, allowing the controlled microgrid to transit smoothly between the grid-connected and islanding modes without disrupting critical loads connected to it. The performance of the proposed controller has been tested extensively in simulation using MATLAB/SIMULINK software and a real-time digital simulator (RTDS) based platform, and experimentally using a scaled hardware prototype.

3.2 System Configuration

Figure 3.1 shows the multi-bus microgrid configuration considered in this chapter, where two paralleled DG systems 1 and 2 are employed. Each DG system is comprised of a DC source, a PWM voltage source inverter (VSI) and LC filters. Under normal mode of operation, the microgrid is connected to the utility system at the Point of Common Coupling (PCC) usually through a static transfer switch (STS). In this mode, the two DG systems are controlled to provide local power and voltage support for critical loads 1, 2 and 3. This configuration reduces the burden of generation and delivery of power directly from the utility grid and enhances the immunity of critical loads to system disturbances in the utility grid.

Figure 3.1. Microgrid configuration.

When a utility fault occurs, the STS opens to isolate the microgrid and utility system. The two DG systems are now the sole power sources left to regulate the load voltages and to supply uninterrupted power in a certain predetermined DG power sharing scheme to all critical loads within the microgrid. Subsequently when the fault is cleared, the microgrid has to be re-synchronized with the utility grid before the STS can be re-closed to return the system smoothly back to the grid-connected mode of operation.

3.3 Controller Design

This section presents the design of a unified controller for use with each DG system to allow the microgrid in Figure 3.1 to function as described in Section 3.2. The proposed controller consists of inner voltage and current control block and external real and reactive power control block. Also a synchronization algorithm is embedded to the power block for smooth connection of the microgrid with the utility system. Detailed design of the controller is given in the following subsections. (The proposed controller can also be used for more complex microgrids where more DG systems operate in parallel, even though a microgrid with only two DG systems is considered in this chapter for illustration).

3.3.1 Inner current and voltage control loops

The inner current-regulated voltage-controlled strategy used for controlling the three-phase grid-interfacing VSI is shown in Figure 3.2 [39], [40]. As shown, an outer capacitor voltage feedback compensator K_v is used to force the capacitor voltages $\{V_a, V_b, V_c\}$ to track their sinusoidal reference waveforms $\{V_a^*, V_b^*, V_c^*\}$ stiffly with an acceptable low output total harmonic distortion (THD). The outputs of this voltage compensator $\{I_{Ca}^*, I_{Cb}^*, I_{Cc}^*\}$ are then fed to an inner capacitor current compensator K_i , acting as the capacitor current reference signals for this inner compensator. The inner capacitor current compensator is included here mainly to stabilize the system and to improve the system dynamic response by rapidly compensating for near-future variations in the load voltages whose rate of change is indirectly sensed by measuring the capacitor currents. The output modulating signals $\{\tilde{m}_a, \tilde{m}_b, \tilde{m}_c\}$ from the inner current compensator are finally fed to the sinusoidal pulse-width modulator (SPWM) to generate the high frequency gating signals for driving the three-phase VSI.

To allow for transfer function analysis of the control scheme shown in Figure 3.2, the single-phase equivalent model of the grid-interfacing inverter is first derived, as follows:

$$L \frac{di_{fa}}{dt} = S_1^* V_{dc} - (v_{an} + V_{ng}) \quad (3.1)$$

$$L \frac{di_{fb}}{dt} = S_2^* V_{dc} - (v_{bn} + V_{ng}) \quad (3.2)$$

$$L \frac{di_{fc}}{dt} = S_3^* V_{dc} - (v_{cn} + V_{ng}) \quad (3.3)$$

where S_j^* represents the state of each semiconductor switch ($S_j^* = 1$ when switch S_j is ON and $S_j^* = 0$ when switch S_j is OFF, $j = 1, 2$ or 3), V_{dc} is the DC link voltage, V_{xn} is the phase to neutral voltage, V_{gn} is the voltage between filter capacitor neutral and DC link negative rail, and i_{fx} is the current through filter inductor L ($x = a, b$ or c).

Figure 3.2. Power circuit and control schematic for the three-phase grid-interfacing inverter with LC filters.

Assuming that the three-phase loads and grid voltages are balanced, then:

$$v_{an} + v_{bn} + v_{cn} = 0 \quad (3.4)$$

$$i_{fa} + i_{fb} + i_{fc} = 0 \quad (3.5)$$

Substituting (3.4) and (3.5) into the sum of (3.1), (3.2) and (3.3), V_{ng} can be expressed in terms of the switch states as:

$$V_{ng} = \frac{V_{dc}}{3}(S_1^* + S_2^* + S_3^*) \quad (3.6)$$

For a high “switching to modulating frequency” ratio, the discrete variable S_j^* can be replaced by its duty cycle expressed as:

$$d_x = \frac{\tilde{m}_x}{2} + \frac{1}{2} \quad (3.7)$$

Where $\tilde{m}_x$ is the modulation index for phase a , b or c . Replacing S_j^* by d_x , (3.6) can be simplified as $V_{ng} = \frac{V_{dc}}{2} + S_0$, where $S_0 = \frac{V_{dc}}{6}(\sum \tilde{m}_x)$. Equations (3.1) to (3.3) can then be re-expressed as:

$$L \frac{di_{fa}}{dt} = \frac{1}{2} m_a V_{dc} - v_{an} - S_0; \quad (3.8)$$

$$L \frac{di_{fb}}{dt} = \frac{1}{2} m_b V_{dc} - v_{bn} - S_0; \quad (3.9)$$

$$L \frac{di_{fc}}{dt} = \frac{1}{2} m_c V_{dc} - v_{cn} - S_0 \quad (3.10)$$

Note that (3.8)-(3.10) consist of only two independent equations, as the sum of the three is nil. Assuming the sum of the modulation signals is nil (i.e. $\sum \tilde{m}_j = 0$ and thus S_0 is nil), the final governing differential equations for each phase can be written as:

$$L \frac{dI_f}{dt} = \frac{1}{2} \tilde{m} V_{dc} - V_C \quad (3.11)$$

$$C \frac{dV_C}{dt} = I_f - I_{load} \quad (3.12)$$

where $\tilde{m}$ is the modulating signal, C is the filter capacitor, V_C is the capacitor voltage (same as phase to neutral voltage), and I_f , I_C and I_{load} are the currents flowing through the filter inductor, capacitor and load respectively. The representation of (3.11) and (3.12) with the added inner capacitor current control loop, is shown in Figure 3.3, where the load

current is represented as a disturbance input. The following closed-loop transfer function is obtained:

$$I_C = \frac{\frac{k_i V_{dc}}{2} Cs}{LCs^2 + \frac{k_i V_{dc}}{2} Cs + 1} I_C^* - \frac{LCs^2}{LCs^2 + \frac{k_i V_{dc}}{2} Cs + 1} I_{load} \quad (3.13)$$

Frequency domain analysis can now be performed using (3.13) to plot the Bode diagrams of I_C / I_C^* and I_C / I_{load} in Figure 3.4 for the case of gain $k_i = 0.1$ (The system parameters used are given in Table 3.1)

Figure 3.3. Block diagram of inner current loop.

Figure 3.4. Bode plots of I_C / I_C^* and I_C / I_{load} .

Ideally, the bandwidth of I_C / I_C^* in Figure 3.4 should be maximized (tend towards ∞) by using a higher k_i , to achieve perfect reference tracking at all input frequencies, a faster dynamic response and the complete blocking of disturbance input from feeding forward to the output ($I_C / I_{load} = 0$). A high gain would however degrade the control loop stability

when physically implemented, since the capacitor current has a significant amount of switching ripples. A large k_i will amplify this current noise unless a filter is implemented at the detection of I_C to filter out the switching ripples, which will definitely affect the performance and design of the whole current and voltage control loops. A satisfactory compromise therefore is to use a smaller k_i that will give a near-unity closed-loop current gain at the fundamental frequency. Based on this gain selection criterion, k_i is set as 0.1, which will give a closed-loop current gain of $I_C / I_C^* = 0.971$ and a negligibly small I_C / I_{load} gain at the fundamental frequency (50 Hz).

Once the inner current loop design is finished, the next step is to fine-tune the gain of the outer voltage feedback loop, whose open-loop transfer function without considering the influence of load disturbance is given by:

$$G_v(s) = \frac{V_C}{I_C^*} = \frac{1}{Cs} \frac{I_C}{I_C^*} \quad (3.14)$$

Figure 3.5. Bode plot of the closed-loop voltage transfer function.

Similar to the inner capacitor current loop, only a simple proportional compensator is used in the capacitor voltage loop to avoid phase errors commonly introduced by a PI compensator. The gain k_v of this proportional compensator should again be selected to give a satisfactory compromise between the attainable control bandwidth and control loop

stability. In this work, the voltage loop tuning criteria is to obtain a steady-state voltage error of less than 2% at the fundamental frequency. Specifically, $k_v = 1.15$ results in the closed-loop voltage frequency response curves in Figure 3.5, which have a steady-state error of 1.9% at the fundamental frequency.

It is commented that although $k_v = 1.15$ gives the desired performance on the ideal system model, stability problem would still arise during physical implementation in Sections 3.5 and 3.6 due to the sampling delay and measurement offset or noises etc. The stability as well as steady-state performance of the capacitor voltage control can be improved by including an additional feedforward path for inverter voltage [65, 76], as shown in Figure 3.6. The proportional gain $2/V_{dc}$ on this feedforward path is to compensate the gain of inverter model. With this feedforward path, the closed-loop transfer function of the outer voltage loop can be written as:

$$V_C = \frac{\frac{V_{dc}k_i k_v}{2} + 1}{LCs^2 + \frac{V_{dc}k_i}{2}Cs + \frac{V_{dc}k_i k_v}{2} + 1} V_C^* - \frac{Ls}{LCs^2 + \frac{V_{dc}k_i}{2}Cs + \frac{V_{dc}k_i k_v}{2} + 1} I_{load} \quad (3.15)$$

Figure 3.6. Block diagram of the voltage and current loops with feedforward control.

Using (3.15), the bode plots of V_C / V_C^* and V_C / I_{load} with $k_i = 0.1$ and $k_v = 0.35$ can be plotted as in Figure 3.7. Observing this figure, it is clear that the additional feedforward path gives rise to a similar steady-state performance (steady-state error of 2.0%), while with much smaller k_v (reduced from 1.25 to 0.35) and hence better stability. Also shown in Figure 3.7 is that the load current again has no appreciable influence on the voltage loop performance.

Figure 3.7. Bode plots of V_c/V_c^* and V_c/I_{load} .

3.3.2 External real and reactive power control loops

Conceptually illustrated in Figure 3.8, the flow of real power P between two nodes can be controlled by varying the supply frequency and hence the power angle δ , whilst the flow of reactive power Q can be controlled by changing the voltage magnitude. Using these concepts, external real and reactive power control loops are proposed in this section for use with each DG system operating in either the grid-connected or islanding mode.

Figure 3.8. Real and reactive power flows between two nodes with voltages $V_1 \angle \delta$ and $V_2 \angle 0$ separated by an inductor L .

When the STS separation device opens to isolate a utility fault, the DG systems in Figure 3.1 must immediately share the increased power demand in a predetermined manner

among themselves so as to continue supply power to all critical loads within the microgrid adequately. This sharing of power can be achieved with no physical communication link between the DG systems by introducing artificial “real power versus supply frequency ($P - \omega$)” and “reactive power versus voltage ($Q - E$)” droop characteristics into the DG controllers (a method commonly used in power systems with multiple generators [9], [38], [41]).

For illustration, consider the $P - \omega$ droop characteristics in Figure 3.9 for the two DG systems in Figure 3.1. Preferably, these droop characteristics should be coordinated to make each DG system supplying real and reactive power in proportion to its power ratings, and can mathematically be expressed as:

$$\omega_j(t) = \omega^* - \beta_j (P_j^* - P_j(t)) \quad (3.16)$$

$$\beta_j = \frac{\omega^* - \omega_{\min}}{P_j^* - P_{j,\max}} \quad (3.17)$$

where $P_j(t)$ is the actual real power output of DG system j ($j = 1$ or 2), $\{P_{j,\max}, \omega_{\min}\}$ are the maximum real power output of DG system j and the minimum allowable operating frequency, $\{P_j^*, \omega^*\}$ are the dispatched real power and operating frequency of DG system j when in grid-connected mode and β_j (< 0) is the slope of the droop characteristics. The physical block diagram realization of (3.16) and (3.17) is shown in Figure 3.10.

Figure 3.9. $P - \omega$ droop characteristics.

As shown in Figure 3.9, each DG system is initially designed to dispatch real power output of P_j^* at the common base frequency of ω^* when operating in the grid-connected mode (ω^* is fixed solely by the stiff utility grid). Once islanded, the power outputs of both DG systems must immediately be raised in accordance with their individual droop characteristics, to supply power to all critical loads within the microgrid adequately at a reduced steady-state frequency of ω_{ss} . This arrangement obviously allows both DG systems to share the total load demand in a predetermined manner according to their individual power ratings. It is commented here that operating at a reduced frequency in the islanding mode also can be beneficial for the re-synchronization and reconnection of the microgrid and utility grid, and can serve as an indicator for the system operator to differentiate whether the microgrid is in the grid-connected or islanding mode.

In a similar manner, the magnitude set point of each DG output voltage can be tuned according to a specified $Q - E$ droop characteristics, to control the flow of reactive power within the microgrid. Mathematically, the $Q - E$ characteristics can be expressed as:

$$E_j(t) = E^* + \zeta_j (Q_j^* - Q_j(t)) \quad (3.18)$$

$$\zeta_j = \frac{E^* - E_{\min}}{Q_{j,\max} - Q_j^*} \quad (3.19)$$

where $Q_j(t)$ is the actual reactive power output of DG system j ($j = 1$ or 2), $\{Q_{j,\max}, E_{\min}\}$ are the maximum reactive power output and minimum voltage magnitude of DG system j , $\{Q_j^*, E^*\}$ are the dispatched reactive power of DG system j and PCC voltage magnitude when in grid-connected mode and ζ_j is the slope of the droop characteristics. The physical block diagram realization of (3.18) and (3.19) is shown in Figure 3.11.

Figure 3.10. Real power compensator.

Figure 3.11. Reactive power compensator.

The only complication with droop $Q - E$ control is that the DG output voltages have to be different from that of the utility grid to allow for proper reactive power control in the grid-connected mode. Therefore, the $Q - E$ droop characteristics specified in (18) and (19) cannot be applied directly for the control of reactive power in the grid-connected mode. This is unlike $P - \omega$ control where the DG systems and utility grid have the same steady-state frequency in the grid-connected mode, allowing the same $P - \omega$ control algorithm to be used for both the grid-connected and islanding modes.

A possible solution to resolve this complication is to add an additional PI reactive power compensator for use in the grid-connected mode, as shown in Figure 3.11. When connected to the utility grid, only the PI compensator is selected for reactive power control, forcing the DG reactive power output to track its desired value with zero steady-state error. For this PI compensator, low gains of $k_p = 0.0003$ (proportional), $k_i = 0.0055$ (integral) are used to give a sufficiently long response time, which in turn allows the dynamics of the inner voltage/current loops and external power loops to be decoupled. When a utility fault occurs and the microgrid islands, the control selector in Figure 3.11 switches over to select the $Q - E$ droop characteristics for reactive power sharing between the DG systems, ensuring a smooth transition from grid-connected to islanding mode.

3.3.3 Synchronization of the microgrid and utility

When the utility grid returns back to normal operating conditions, the microgrid has to get re-synchronized with the utility grid for reconnection. Synchronization can be achieved by aligning the voltage phasors at the microgrid and utility ends of the STS separation device shown in Figure 3.1, and can conveniently be implemented by adding two separate

synchronization compensators to the external real and reactive power control loops, as shown in Figures 3.12 and 3.13. Inputs to these synchronization compensators are the magnitude ΔE and phase $\Delta\delta$ errors of the two voltage phasors at both ends of the STS, and their outputs are fed to the real and reactive power loops to make the voltage phasor at the microgrid end track the phasor at the utility end closely (both in magnitude and frequency). Once synchronized and upon closing the STS separation device, the synchronization compensators must be deactivated by setting their outputs to zero so as not to interfere with the proper operation of the real and reactive power control loops in the grid-connected mode. (Note that although there are no communications between the DG systems during synchronization, a communication between STS and individual DG is required for the acquisition of ΔE and $\Delta\delta$. This communication is provided by the Energy Manager or Microgrid Central Controller. See Section 2.4 for the functions of Energy Manager or Microgrid Central Controller.)

In this work, the response times of both synchronization compensators are chosen to be around 0.5 s to ensure that the voltage magnitude and frequency of each DG system ramp up/down gradually within the tolerance limits of the critical loads. Based on this selection criterion, a PI compensator with gains tuned at $k_p = 0.5$ (proportional), $k_i = 7$ (integral) and saturation limits of ± 10 rad/s is used for phase/frequency synchronization, whilst an integrator with gain of $k_i = 8$ and saturation limits of ± 30 V is used for magnitude synchronization.

Figure 3.12. Real power compensator with synchronization function.

Figure 3.13. Reactive power compensator with synchronization function.

A complication anticipated when using the aforementioned synchronization algorithms is the possible occurrence of jitter when $\Delta\delta$ approaches 0. Since the phases of voltages at both ends of the STS device range from -180° to $+180^\circ$, their phase difference $\Delta\delta$ can range from -360° to $+360^\circ$, allowing jitter to occur when $\Delta\delta$ oscillates between 0 and $+360^\circ$ or 0 and -360° . This complication can be resolved by using the algorithm

$$\Delta\delta = \begin{cases} \Delta\delta - 360^\circ & \text{for } \Delta\delta > 180^\circ \\ \Delta\delta + 360^\circ & \text{for } \Delta\delta \leq -180^\circ \end{cases} \text{ to limit } \Delta\delta \text{ within the range of } \pm 180^\circ.$$

A second complication would occur when multiple DG systems are operated in parallel. Under paralleled operation, each DG system must have the same rate of change of voltage (both in magnitude and phase) to prevent real and reactive power oscillations between the DG systems. Since the synchronization compensators for each DG system use the same inputs ($\Delta\delta$ and ΔE), this second complication can easily be resolved by using the same controller parameters for all the DG systems.

Note that when synchronizing the microgrid with the utility system, the magnitude controller increases the DG system's voltage magnitude smoothly to match it with the utility grid. While the phase controller has different operation steps in the following two conditions:

- A) If the phase of the microgrid is leading that of the utility system when synchronization begins ($-180^\circ < \Delta\delta < 0$), the phase controller tends to reduce the frequency of the microgrid to lessen the phase difference between the microgrid and the utility system. After the phase difference comes to 0, the frequency in the

microgrid is then increased to match the grid frequency. Finally, a sustained 0 phase difference is obtained.

- B) If the phase of the microgrid is lagging that of the utility grid at the beginning of synchronization ($0 < \Delta\delta \leq 180^\circ$), the frequency of the islanding microgrid is increased directly to reduce the phase difference. Once the frequencies in the microgrid and the utility system equals, the phase controller maintains the 0 phase difference.

To summarize, the final block diagram representation of the proposed unified controller is shown in Figure 3.14.

Figure 3.14. Overview of proposed microgrid unified controller.

3.4 Off-Line Simulation of the Microgrid System

Off-line simulations have been carried out to verify the effectiveness of the proposed control structure for the microgrid shown in Figure 3.1. There are many software packages capable of simulating power electronics circuits, such as: MATLAB/SIMULINK, SABER, PSpice, PSCAD etc. Each simulation package has certain advantages and disadvantages especially in terms of modeling, mathematical richness and computational time. MATLAB provides a separate toolbox for power system modeling which includes most of the power electronics devices as models. Moreover

MATLAB is more efficient in control system design and evaluation and it is easy to generate customized modules depending on the requirement. Therefore MATLAB/SIMULINK (version 6.5.0) has been chosen for this work for modeling, control system simulation and evaluation. Simulation parameters are given in Tables 3.1 and 3.2.

3.4.1 Transition from grid-connected to islanding mode of operation

The microgrid starts up at $t = 0$ in grid-connected mode. At $t = 1.5$ s, the separation device opens and the microgrid is disconnected from the utility system and operates in islanding mode. Figures 3.15 and 3.16 show the real and reactive power flows and sharing of DG systems 1 and 2.

Figure 3.15. Real power flow of DG systems. Figure 3.16. Reactive power flow of DG systems.

It can be seen from Figure 3.15 that when STS at the PCC opens, the two DG systems share the increased real power demands proportionately. Also it is interesting to note that the reactive power sharing between the DG systems may not be perfectly proportional compared to the real power sharing. This is due to the line impedance between the DG systems, which will affect the accuracy of the reactive power sharing [42].

Figure 3.17. Frequency of the DG system 1.

Figure 3.18. Magnitude of the capacitor voltages of the DG system 1

The frequency and magnitude of capacitor voltage of the DG system 1 are shown in Figures 3.17 and 3.18. The frequency droop is less than 0.2 Hz, and the voltage magnitude droop is less than 15 V, which is quite acceptable.

The three-phase capacitor voltage of the DG system 1 at $t = 1.5$ s (When separation switch opens) is shown in Figure 3.19, which demonstrates that the critical loads experience very smooth transition when the microgrid transfers its operation from grid-connected mode to islanding mode.

Figure 3.19. Three-phase capacitor voltages at $t = 1.5$ s.

3.4.2 Transition from islanding to grid-connected mode of operation

The waveforms showing the synchronization of microgrid with the utility grid and transition of the microgrid from islanding mode to grid-connected mode are illustrated in Figures 3.20 to 3.25. The microgrid starts up in islanding mode at $t = 0$ s. At $t = 2$ s, the synchronization controller begins to work. The switch is closed at $t = 3$ s, and the microgrid operates in grid-connected mode from that point onwards.

Figure 3.20 shows the process of synchronization where phase A voltages at both ends of the separation switch are illustrated. At the beginning of synchronization, the two voltages have a phase difference: $\Delta\delta = 86^\circ$ and a magnitude difference: $\Delta E = 23$ V. The synchronization process is complete smoothly within 0.5 s.

Figure 3. 20. Synchronization of the microgrid and the utility system (phase A).

Figure 3. 21. Switch current (phase A) during reconnection.

Figure 3.21 shows the switch current (phase A) during reconnection of the microgrid with the utility grid. The transition is very smooth during reconnection and this verifies the effectiveness of the synchronization controller.

Figures 3.22 and 3.23 show the frequency and voltage magnitude of the DG system 1 during synchronization and reconnection. After reconnecting the microgrid with the grid the voltage magnitude decreases. This is due to the effect of line impedance. While operating in islanding mode, power demands for the DG systems are larger and thus large currents flow in lines 1 and 2 (refer to the microgrid configuration in Figure 3.1). As a consequence of this, the voltage drop on the lines is higher and the DG systems must provide little higher voltage to compensate for the voltage drop during synchronization. When the switch is closed, the power provided by the microgrid decreases and the voltage drop on the lines reduces. Thus the output voltages of DG systems decrease.

Figure 3.22. Frequency of the DG system 1 during synchronization and reconnection.

Figure 3.23. Magnitude of the capacit voltage of the DG system 1 during synchronization and reconnection.

Figure 3.24. Real power of DG systems.

Figure 3.25. Reactive power of DG systems.

From Figures 3.24 and 3.25, it can be seen that when the microgrid transits from islanding mode to grid-connected mode, the DG systems take up the dispatched real and reactive power automatically. During synchronization, there should be no power oscillations between the paralleled operating DG systems as the rate of change of voltage phase and magnitude of each DG system is held the same. But slight power oscillations appear in Figures 3.24 and 3.25 during synchronization, which are caused by the dynamics of the motor loads.

3.5 Real-Time Digital Simulation Implementation

The performance of the proposed unified controller was further tested in real-time digital simulation using the laboratory setup and shown in Figures 3.26 and 3.27 with system parameters listed in Tables 3.1 and 3.2. The setup is comprised of a Real Time Digital Simulator (RTDS) [43] [44], two digital input time stamp (DITS) interface cards, a workstation for facilitating modeling and communication with the RTDS, and an external dSPACE DS1103 controller card [45] for physical implementation of the proposed controller. This arrangement is commonly referred to as “hardware-in-the-loop-simulation” where a hardware controller is physically integrated within a plant (consisting of the utility grid, microgrid and interfacing inverters) simulated using the RTDS simulator, to test the controller performance in real time. It gives more accurate results than offline simulation, and is preferably performed after offline simulation but before

experimental investigation, as a sequential procedure for testing controller performance in complex plants like power systems.

Figure 3. 26. Real-time implementation platform.

3.5.1 System configuration of the real-time implementation platform

The real-time implementation platform is illustrated in Figures 3.26 and 3.27. It comprises the following main functional blocks:

- A) The RTDS: the RTDS simulator is designed for performing real-time digital electromagnetic transient power system simulation based on Dommel Algorithm. The computational power of the simulator is provided by multiple parallel-running digital signal processors (DSPs) housed in two racks. The processors are mounted either on one of the 35 Tandem Processor Cards (TPCs) or the single 3-PC card, with each TPC card having two on-board NEC processors and the more advanced 3-PC card having three SHARC processors. Both processor cards also have accessible digital and analogue I/O ports for measurement output and control action input;

- B) The WorkStation: The SUN WorkStation actually plays as a communication tool between the RTDS and human operators. Simulation cases are drafted and compiled by the RTDS software resided in the workstation. DSPs are automatically assigned to compute various components. Executable codes are also generated and transferred to the RTDS hardware. Simulation results can readily be transferred back to the WorkStation accessible for human operators. On-line adjustment of some system parameters and randomly applying event sequences can also be achieved;
- C) The external control system: Control algorithms are realized in the external control system. In this proposed system, a DS1103 DSP card inserted in a PC ISA slot calculates the control algorithm in effect. The external control system receives the necessary input information from the RTDS and sends back the required control signals such as gating signals to the RTDS through an interface circuit; (More detailed description of the DS1103 DSP controller card is given in the Appendix).
- D) Interface circuits: Besides the analog-to-digital (A/D), digital-to-analog (D/A) modules and necessary protection circuits in the proposed system, there are two irreplaceable cards named Digital Input Time Stamp (DITS) cards, which function as the intermediate between external gate signals and the Voltage Source Converters (VSC) modeled in the RTDS. The DITS cards enable the RTDS to model the switching of power electronics devices digitally with almost the same accuracy as an analog system. The real-time implementation system can handle simulation cases with two VSC models with the two DITS cards available;

As shown in Figure 3.27, the power system grid and microgrid components are modeled in TPCs and 3PC on the RTDS, where the inverters are modeled on the 3PC. Upon simulated, the RTDS simulated plant sends system voltages and currents to the DS1103 controller. On the DS1103 card, the received analog signals are digitized by on-board analog-to-digital converters (ADCs) before being processed by the Slave DSP to generate the required SPWM gating signals. These gating signals are then sent back to the

simulated inverter modules in the RTDS simulator through DITS cards and optical isolation, completing the real-time simulation of a control cycle.

Figure 3.27. Laboratory setup for real-time digital simulation.

3.5.2 Transition from grid-connected to islanding mode of operation

The microgrid operates in grid-connected mode at the beginning. At $t = 6$ s, the switch at PCC opens and the microgrid transits to islanding mode. Figures 3.28 and 3.29 show the real and reactive power flow and sharing of the DG systems when the microgrid islands.

Figure 3.28. Real power flow of the DG systems (RTDS).

Figure 3.29. Reactive power flow of DG systems (RTDS).

The capacitor voltage of the DG system 1 (phase A) is shown in Figure 3.30. The transition of the microgrid from grid-connected mode to islanding mode is very smooth.

Figure 3.31 is the switch current (phase A) when microgrid islands. The switch is opened when the current crosses zero for the first time after a turn off command is applied

Figure 3.30. Phase A capacitor voltage of the DG system 1 (RTDS).

Figure 3.31. Switch current (phase A, RTDS).

3.5.3 Transition from islanding to grid-connected mode of operation

The microgrid operates in islanding mode at first. The synchronization begins at $t = 6$ s. The separation device closes at $t = 13$ s. The microgrid operates in grid-connected mode

from then on. The synchronization of voltages (phase A) at both ends of the switch is shown in Figure 3.32.

Figure 3.32. Synchronization of the microgrid and the utility system (phase A, RTDS).

Figures 3.33 and 3.34 show the real and reactive power flow of the DG systems during synchronization. Both the real and reactive power injection of DG systems increase because the magnitudes of the DG system output voltages are increased for the purpose of synchronization.

Figure 3.33. Real power flow of DG systems during synchronization (RTDS).

Figure 3.34. Reactive power flow of DG systems during synchronization (RTDS).

Figure 3.35 shows the switch current (phase A) during reconnection of the microgrid and the utility system. The smooth transition results from the good performance of the synchronization controller.

Figure 3.35. Switch current during reconnection (phase A, RTDS).

Figure 3.36. Real power flow of DG systems during reconnection (RTDS).

Figure 3.37. Reactive power flow of DG systems during reconnection (RTDS).

Figures 3.36 and 3.37 show the real and reactive power flow of DG systems during reconnection of the microgrid and utility. The DG systems feed the dispatched real and reactive power once microgrid enters into grid-connected mode.

These real-time test results match closely with off-line simulation results and that shows the effectiveness and correctness of the proposed control algorithm.

3.6 Hardware Implementation of the Microgrid System

Real-time digital control of power devices using cost effective digital signal processor (DSP) based hardware system has become popular. The DSP hardware architecture enables most of its instructions to be executed in a single instruction cycle and complex control algorithm can be implemented in a fast rate compared to the single-chip microprocessors. Thus, with this implementation of digital control, the performance of the proposed control scheme for the microgrid system could be implemented by setting up a prototype of the proposed microgrid system in a DSP hardware architecture environment.

3.6.1 Description of the proposed microgrid hardware prototype

The hardware microgrid prototype made up of several parts such as three-phase half bridge inverters using IGBT switches, IGBT gate drive board, three-phase back-to-back SCR switch, inductors and capacitors for the inverters filter circuits, load resistors and inductors, line resistors and inductors, current transducers, voltage transducers, interface circuits, DC sources for the inverters, AC source representing the utility system, and DSP controller board (DS1103). Figures 3.38 and 3.39 depict the schematic diagram of the proposed laboratory prototype of the microgrid system highlighting the major components. A detailed description on hardware microgrid system components is given in the Appendix.

Figure 3.38. Hardware setup (part a).

Figure 3.39. Hardware setup (part b).

3.6.2 Implementation of the controller

The feedback voltages and currents are measured using the voltage and current transducers and fed to the ADC of the DSP controller board. ADC outputs are then multiplied by appropriate scale factors determined by a preliminary test in order to obtain the actual values of the measured quantities. Certain biases are used for the current transducers to adjust the zero level. This is required due to high current rating of the current-transducers (50A for LTA 50-P/SP1 and 200A for HA 200-SB), which has a significant zero error at low current level for the experiment. Three-phase solid switch control signal is fed to the DSP controller board through digital I/O port for proper function of the reactive compensator (see Figure 3.11) during different microgrid operation modes.

Implementation of the control algorithm is accomplished by dSPACE DS1103 PPC/333MHz controller board connected to Pentium II host computer. The real-time interface (RTI) adds a hardware-specific block library to the MATLAB/SIMULINK software environment, which allows the SIMULINK to be linked with the real-time hardware of the DSP. Once the controller is build in the SIMULINK environment, it is then downloaded to the dSPACE Control Desk Software in order to implement the controller in real-time. Some algorithms used in the synchronization and the duty calculation for PWM are implemented using hand-coded C programs used as s-functions of the SIMULINK.

At the start of the program, all necessary parameters in the program are initialized. The sampling frequency is set to 5 kHz. In every sampling interrupt, the utility voltages, DG system output voltages (or filter capacitor voltages) and filter capacitor currents are acquired. The duty cycles are then calculated using the feedback variables and the proposed control algorithms. The calculated duty cycles are fed to the PWM generation unit of the DS1103 slave DSP and six-gate signals for each voltage source inverter are then tapped from I/O pins. This TTL signal (5V) is voltage shifted to CMOS compatible level of 15V by the interface circuit. Finally output of the interface circuit is fed to each IGBT driver board to drive the inverters.

3.6.3 Experimental results

A scaled hardware prototype of Figure 3.1 was implemented for experimental verification. For the experimental system, the utility grid, represented by a stiff AC source, was connected through a three-phase back-to-back SCR switch to the microgrid consisting of two three-phase IGBT inverters and critical loads 1, 2 and 3. The proposed unified controller was implemented using the DS1103 controller card with its output signals driving the hardware IGBT inverters. Other system details for this experimental investigation are given in Table 3.1.

3.6.3.1 Transition from grid-connected to islanding mode of operation

Figures 3.40 and 3.41 show the real and reactive power outputs of DG systems 1 and 2 respectively, while Figures 3.42 and 3.43 show the corresponding output voltages of DG system 1 and current through the SCR switch when the SCR switch opens at $t = 23$ s to disconnect the microgrid from the utility grid. As anticipated, these figures show the DG systems operating with the desired power sharing ratios and the smooth transition from grid-connected to islanding mode.

Figure 3.40. Real and reactive power outputs of DG system 1 when the microgrid islands. (Experimental).

Figure 3.41. Real and reactive power output of DG system 2 when the microgrid islands (Experimental).

Figure 3.42. Output line voltage of DG system 1 when the microgrid islands.
(Experimental).

Figure 3.43. Switch current when the microgrid islands.
(Phase A; experimental).

3.6.3.2 Transition from islanding to grid-connected mode of operation

Figure 3.44 shows the process of synchronizing the voltages at both ends of the SCR switch, while Figures 3.45 and 3.46 show the slight changes in power outputs of the DG systems when the synchronization algorithms start functioning at $t = 43$ s in the islanding mode. Noted experimentally, the voltage at the microgrid end of the SCR switch moves to track that of the utility end with nearly zero tracking error and without transient power oscillation between the DG systems. Figures 3.47 and 3.48 show the real and reactive power outputs of the DG systems during reconnection process, while Figure 3.49 shows the current through the SCR switch when it closes at $t = 50$ s to reconnect the microgrid and utility grid. These figures show the DG systems injecting their predetermined dispatched powers automatically upon returning back to the grid-connected mode and again confirm the smooth reconnection process that can be achieved using the proposed synchronization algorithms.

Figure 3. 44. Synchronization of microgrid and utility (voltages Vab; experimental).

Figure 3.45. Real and reactive power outputs of DG system 1 during synchronization.

(Experimental).

Figure 3.46. Real and reactive power output of DG system 2 during synchronization.

(Experimental).

Figure 3.47. Real and reactive power outputs of DG system 1 during reconnection.

(Experimental).

Figure 3.48. Real and reactive power output of DG system 2 during reconnection.

(Experimental).

Figure 3. 49. Switch current during reconnection (phase A; experimental).

It is commented here that although pulsations in both real and reactive power at steady state are noticeable in Figures 3.40-3.41 and 3.45-3.48, the viability and effectiveness of the proposed unified controller are verified by the experiments.

Table 3. 1. System parameters for MATLAB/SIMULINK simulation, RTDS simulation and experiment.

Parameters		MATLAB/SIMULINK and RTDS Simulation	Experiment
DG system 1	Inverter switching frequency	1 kHz	10 kHz
	Inverter filter inductance	0.9 mH (0.19 pu)	5 mH (0.11 pu)
	Inverter filter capacitance	250 μ F (0.11 pu)	30 μ F (0.14 pu)
	DC link voltage	1000 V	250 V
DG system 2	Inverter switching frequency	1 kHz	10 kHz
	Inverter filter inductance	0.9 mH (0.19 pu)	10 mH (0.21 pu)
	Inverter filter capacitance	250 μ F (0.11 pu)	30 μ F (0.14 pu)
	DC link voltage	1000 V	250 V
Rating of each DG system		70 kVA	420 VA
Controller parameters	ω^*	50 Hz	50 Hz
	ω_{min}	48.5 Hz	49 Hz
	E^*	310 V	98 V
	E_{min}	290 V	90 V
	P_1^*	35 kW	180 W
	P_2^*	30 kW	150 W
	Q_1^*	15 kVar	100 Var
	Q_2^*	10 kVar	70 Var
	β_1	-3/70000	-1/240
	β_2	-3/80000	-1/270
	ζ_1	4/11000	1/40
	ζ_2	1/3000	4/175
Nominal power		100 kVA	1 kVA
RMS line voltage of utility grid		380 V	120 V
Common parameters of Lines 1 and 2		0.05 Ω (0.03 pu), 1.6 mH (0.34 pu)	1 Ω (0.06 pu), 6.3 mH (0.13 pu)
Rating of Load 1	RL load (30 kW, 10 kVar)	RL load (120 W, 90 Var)	
Rating of Load 2	RL load (20 kW, 6 kVar)	RL load (110 W, 65 Var)	

Rating of Load 3	RL load (13 kW, 10 kVar) + Induction motor (see Table 3.2)	RL load (200 W, 145 Var)
------------------	---	--------------------------

Table 3. 2. Parameters of motor load used in MATLAB/SIMULINK and RTDS simulation.

Type		Induction Motor
No. of poles		2
Nominal values	Rated RMS phase voltage	220 V
	Rated RMS phase current	41.7 A
	Frequency	50 Hz
Stator	Stator resistance	0.087 Ω
	Leakage inductance	0.8 mH
Rotor (referred to the stator)	Rotor resistance	0.228 Ω
	Leakage inductance	0.8 mH
Magnetizing inductance		34.7 mH
Inertia		0.089 $\text{kg} \cdot \text{m}^2$
Applied mechanical torque		84.2 Nm

3.7 Discussion

This chapter presents a multi-functional unified controller for use with each DG system in a multi-bus microgrid. The proposed controller contains inner current and voltage loops for regulating the grid-interfacing inverter, and outer real and reactive power loops for controlling the flow of power within the microgrid with particular attention focused on the proper sharing of power between the DG systems when a utility fault occurs and the microgrid islands. The proposed controller also incorporates algorithms for synchronizing the microgrid and utility system once the fault is cleared and the microgrid is on the verge of transiting from islanding to grid-connected mode. Off-line and real-time simulated results and experimental results have confirmed the viability and effectiveness of the proposed unified controller in the grid-connected and islanding modes, and during operational mode transitions.

Chapter 4

Dual-Inverter Grid-Interfacing Power Quality Compensators for Microgrid

4.1 Introduction

As stated in previous chapters, microgrids are systems with clusters of micro-generators, which are installed for distributed power generation. These micro-generators are usually connected to the utility grid using Voltage Source Inverter (VSI) based interfaces, where a case of concern related to this interfacing is the impact of unbalanced grid voltages (usually caused by unbalanced system faults or connected loads) on the overall system performance. If the unbalance in voltages is serious, a solid-state circuit breaker, connected between the microgrid and utility grid as in Figure 4.1 or Figure 4.15(a), will open to isolate the microgrid. But when the voltage unbalance is not so serious, the circuit breaker may remain closed, resulting in sustained unbalanced voltages at the Point of Common Coupling (PCC). Such a voltage unbalance can cause an increase in losses in motor loads (and hence motor overheating) [46]. Special consideration should also be paid to the sensitive loads in the microgrid because some electronic equipment, such as computers, may experience problems if the voltage unbalance is more than 2% [46]. Usually, the primary source of voltage unbalances of less than 2% is caused by load unbalance (e.g. blowing of fuse in one phase of a three-phase capacitor bank). Severe voltage unbalances of greater than 5% are due to single-phasing conditions [14]. In this chapter, 10% voltage unbalance is considered for the case study in simulation as well as in experiment which is more than sufficient for describing worst case scenario.

An obvious solution to the above-mentioned unbalance voltage problem is to balance the sensitive load voltages in the microgrid using certain voltage regulation technique. However large unbalanced currents can flow between the unbalanced utility grid and microgrid due to very low line impedance interfacing both grids, if only the microgrid

voltages are regulated [47]. This flow of large unbalanced currents can over-stress semiconductor devices within the interfacing inverters and system components such as overhead lines and feeder cables. For low voltage distribution where microgrids are usually constructed with a four-wire configuration to supply both single-phase and three-phase loads, the problem is further complicated by the flow of zero-sequence currents through the line and neutral conductors.

Therefore, to control both the sensitive load voltages in the microgrid and the line currents flowing between the microgrid and utility system, grid-interfacing power quality compensators using two inverters (inverters A and B) are proposed for DG systems, as illustrated in Figure 4.1 (for three-phase three-wire microgrid implementation) and Figure 4.15 (for three-phase four-wire microgrid implementation). In each inverter, both positive- and negative-sequence components are controlled to compensate for the effects caused by the unbalanced utility grid voltages (for the four-wire microgrid power quality compensator, zero-sequence components are also controlled). Specifically, the shunt inverter is controlled to ensure balanced voltages within the microgrid and to regulate power dispatches among parallel-connected DG systems, while the series inverter balances the line currents by injecting appropriate voltage components. Current-limiting algorithms are also proposed and integrated within the inverter control schemes to protect the microgrid from large fault currents during utility voltage sags and are presented in Chapter 5. The proposed compensator has been tested in simulations and experimentally using a laboratory hardware prototype.

Note that these control objectives of the proposed compensators are different from those of other reported power conditioners, e.g. unified power quality conditioners (UPQCs), whose series inverter is controlled to balance the load terminal voltages by appropriate series voltage injection, and shunt inverter is controlled to inject harmonic compensating currents to shape the utility currents drawn as balanced sinusoids. In addition, the UPQC is usually designed to function with zero real power flow through it during steady-state to minimize the size of the DC link energy storage capacitor [48]. These control objectives of a UPQC are obviously different from those of the proposed three (four)-leg dual-inverter compensator, where inverter A is used for voltage regulation and power control, and inverter B is used for line current balancing and fault current limiting. Therefore, for

the proposed compensator, the development of an appropriate control algorithm is challenging since existing control algorithms are not directly applicable. This control development for the three-wire and four-wire microgrid compensators is presented in the following sections of the chapter.

4.2 Power Quality Compensator for Three-Phase Three-Wire Microgrids

Figure 4.1 Proposed three-phase three-wire microgrid configuration.

This section proposes a dual-inverter power quality compensator for three-phase three-wire microgrid applications with consideration of both the power quality of the microgrid and the quality of currents flowing between the microgrid and utility system. It is proposed that two inverters connected in shunt and series are used for each DG system in the microgrid as illustrated in Figure 4.1. The main functions of shunt inverter A, which is similar to those proposed in Chapter 3, are to maintain a balanced set of sensitive load voltages in the microgrid under all grid and load operating conditions, generate and dispatch power, share the power demand with other parallel-connected DG systems when the microgrid operates in islanding mode, and to synchronize the microgrid with the utility system at the instant of connection. Also, being connected directly to the micro-source, inverter A must have sufficiently high power capacity with rated voltage and headroom for current higher than the rated value (in fault conditions) in order to continuously condition the routine energy supplied by the micro-source (similar to most shunt inverter applications on power systems). On the contrary the main functions of

series inverter B are to inject appropriate voltage components along the distribution feeder to balance the line currents flowing between the microgrid and unbalanced utility grid, and to limit the flow of large fault currents during utility voltage sags. This second control task would require inverter B to carry relatively large current with a high compensating voltage appearing across it, implying that inverter B must have high power rating too. (Detailed discussion of the fault current limiting algorithms is provided in Chapter 5). The control development for each inverter is presented next in subsections (4.2.1 and 4.2.2).

4.2.1 Control of shunt three-leg inverter A

As shown in Figure 4.2, the control scheme of shunt inverter A contains internal voltage/current regulation loops and external power control loops. The detailed design of the power control loops has already been presented in Chapter 3 and therefore is not duplicated in this chapter. Here attention is focused on the design of shunt inverter's internal voltage/current control loops, after an introductory description of the power control loops to give an overview of the functionalities of shunt inverter A.

Figure 4. 2. Overall control structure of shunt inverter A for three-wire compensator.

In brief, the power loops are designed to control real and reactive power flow, and facilitate power sharing between the paralleled DG systems when a utility fault occurs and the microgrid operates in islanding mode. The power loops achieve this appropriate sharing of power by producing the desired command frequency ω , phase δ and positive-

sequence voltage magnitude E , which are subsequently transformed into the stationary-frame references of $\{V_\alpha^*, V_\beta^*\}$ to be used in the internal voltage/current regulation loops. Ideally, the power loops should perform these reference calculations independently with no physical communication link between the DG systems, and can conveniently be implemented by introducing artificial “real power versus supply frequency” and “reactive power versus voltage magnitude” droop characteristics to the power loops. Furthermore, since the outputs of the power loops contain only positive-sequence components, the calculation of these outputs is independent of the series inverter outputs, which consist of only negative-sequence components when the power loops are functioning. The detailed control and functions of the series inverter are presented in the next subsection 4.2.2.

Besides power control, the external power loops also govern the synchronization of microgrid and utility to ensure smooth and safe reconnection of the two grids when the fault is cleared and the system returns to grid-connected mode of operation. Synchronization can be achieved by aligning the voltage phasors at the microgrid and utility ends of the circuit breaker shown in Figure 4.1, and can conveniently be implemented by adding two separate synchronization PI regulators to the external real and reactive power control loops. As shown in Figure 4.2, inputs to these synchronization regulators are the magnitude and phase errors (ΔE and $\Delta \delta$) of the two voltage phasors at both ends of the circuit breaker. Their outputs are then fed to the real and reactive power loops to make the voltage phasor at the microgrid end track the phasor at the utility end closely both in magnitude and frequency (PI regulators forcing $\Delta E \rightarrow 0$ and $\Delta \delta \rightarrow 0$).

Figure 4.3 shows the voltage control scheme of shunt inverter A, which contains an inner filter inductor current control loop and an outer load voltage control loop. For the outer voltage loop, alternative second-order stationary-frame controllers with zero tracking errors and a higher computational efficiency (details presented later in the subsection) are chosen. Theoretically, these second-order controllers can be derived by transforming PI controllers from the synchronous to the stationary frame. A systematic method for presenting the voltage control loop is therefore to first present the theoretical analysis in the positive- and negative-sequence reference frames rotating in the opposite directions

(see control block diagram enclosed within dotted box in Figure 4.3), and subsequently converts the developed synchronous voltage controllers to the stationary frame.

Figure 4. 3. Voltage control scheme of shunt inverter A of three-wire compensator.

As illustrated in Figure 4.3, the three-phase load voltages are first transformed from the stationary a-b-c frame to the stationary α - β frame $\{V_\alpha, V_\beta\}$ by using matrix A in (4.1) before subtracted from their reference values $\{V_\alpha^*, V_\beta^*\}$ to give the voltage errors $\{e_\alpha, e_\beta\}$. An obvious way for ensuring zero tracking errors is to first convert the stationary α - β voltage errors to their positive- and negative-sequence components $\{e_d^+, e_q^+, e_d^-, e_q^-\}$ by using the d-q synchronous transformation matrices T_1 and T_2 in (4.2) and (4.3) respectively. These synchronous frames errors are then passed through two PI controllers placed along the control paths for eliminating the tracking errors and are finally transform back to stationary α - β frame using T_1^T and T_2^T (transpose of T_1 and T_2) to generate the reference current for the inner loop.

$$A = \begin{bmatrix} \sqrt{\frac{1}{6}} & 0 & -\sqrt{\frac{1}{6}} \\ \frac{\sqrt{2}}{6} & \frac{\sqrt{2}}{3} & -\frac{\sqrt{2}}{6} \end{bmatrix} \quad (4.1)$$

$$T_1 = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \quad (4.2)$$

$$T_2 = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ -\sin(\omega t) & -\cos(\omega t) \end{bmatrix} \quad (4.3)$$

While for easier physical implementation, a more practical form of the positive- and negative-sequence PI controllers can be derived by transforming the PI controllers to the stationary α - β frame [49]. The derivation of α - β frame controllers can be obtained as follows by checking the relationship of the variables in Figure 4.3.

For the positive-sequence:

$$\begin{bmatrix} e_d^+ \\ e_q^+ \end{bmatrix} = T_1 \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \quad (4.4)$$

$$\frac{d}{dt} \begin{bmatrix} X_d^+ \\ X_q^+ \end{bmatrix} = k_i^+ \begin{bmatrix} e_d^+ \\ e_q^+ \end{bmatrix} \quad (4.5)$$

$$\begin{bmatrix} I_d^+ \\ I_q^+ \end{bmatrix} = \begin{bmatrix} X_d^+ \\ X_q^+ \end{bmatrix} + k_p^+ \begin{bmatrix} e_d^+ \\ e_q^+ \end{bmatrix} \quad (4.6)$$

And for the negative-sequence:

$$\begin{bmatrix} e_d^- \\ e_q^- \end{bmatrix} = T_2 \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \quad (4.7)$$

$$\frac{d}{dt} \begin{bmatrix} X_d^- \\ X_q^- \end{bmatrix} = k_i^- \begin{bmatrix} e_d^- \\ e_q^- \end{bmatrix} \quad (4.8)$$

$$\begin{bmatrix} I_d^- \\ I_q^- \end{bmatrix} = \begin{bmatrix} X_d^- \\ X_q^- \end{bmatrix} + k_p^- \begin{bmatrix} e_d^- \\ e_q^- \end{bmatrix} \quad (4.9)$$

Finally, the reference currents in the α - β frame are:

$$\begin{bmatrix} I_\alpha^* \\ I_\beta^* \end{bmatrix} = T_1^T \begin{bmatrix} I_d^+ \\ I_q^+ \end{bmatrix} + T_2^T \begin{bmatrix} I_d^- \\ I_q^- \end{bmatrix} \quad (4.10)$$

Where $\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \begin{bmatrix} V_\alpha^* \\ V_\beta^* \end{bmatrix} - \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}$ are the stationary frame voltage errors; $\begin{bmatrix} e_d^+ \\ e_q^+ \end{bmatrix}$ and $\begin{bmatrix} e_d^- \\ e_q^- \end{bmatrix}$ are the errors transformed into the $d^+ - q^+$ frame and $d^- - q^-$ frame respectively; $\begin{bmatrix} I_d^+ \\ I_q^+ \end{bmatrix}$, $\begin{bmatrix} I_d^- \\ I_q^- \end{bmatrix}$ are the reference currents in the positive- and negative-sequences. While $\begin{bmatrix} X_d^+ \\ X_q^+ \end{bmatrix}$ and $\begin{bmatrix} X_d^- \\ X_q^- \end{bmatrix}$ are the state variables related to the positive- and negative-sequence integrator in the PI controllers. k_p^+, k_i^+ and k_p^-, k_i^- are the parameters of the controllers in the $d^+ - q^+$ frame and $d^- - q^-$ frame respectively.

To simplify the control algorithm, $k_p^+ = k_p^- = k_p$ and $k_i^+ = k_i^- = k_i$ are chosen. Also by employing the controllers in the two-phase stationary α - β frame as suggested by [49-52], the frame transformations can be avoided without deteriorating the function of the controllers. Take $\begin{bmatrix} X_\alpha^+ \\ X_\beta^+ \end{bmatrix} = T_1^T \begin{bmatrix} X_d^+ \\ X_q^+ \end{bmatrix}$ and $\begin{bmatrix} X_\alpha^- \\ X_\beta^- \end{bmatrix} = T_2^T \begin{bmatrix} X_d^- \\ X_q^- \end{bmatrix}$, the following control equations can be obtained:

$$\frac{d}{dt} \begin{bmatrix} X_\alpha^+ \\ X_\beta^+ \end{bmatrix} = k_i \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} + \omega \begin{bmatrix} -X_\beta^+ \\ X_\alpha^+ \end{bmatrix} \quad (4.11)$$

$$\frac{d}{dt} \begin{bmatrix} X_\alpha^- \\ X_\beta^- \end{bmatrix} = k_i \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} + \omega \begin{bmatrix} X_\beta^- \\ -X_\alpha^- \end{bmatrix} \quad (4.12)$$

$$\begin{bmatrix} I_\alpha^* \\ I_\beta^* \end{bmatrix} = \begin{bmatrix} X_\alpha^+ \\ X_\beta^+ \end{bmatrix} + \begin{bmatrix} X_\alpha^- \\ X_\beta^- \end{bmatrix} + 2k_p \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \quad (4.13)$$

The controller can be further simplified by introducing:

$$\begin{bmatrix} Y_\alpha \\ Y_\beta \end{bmatrix} = \begin{bmatrix} X_\alpha^+ \\ X_\beta^+ \end{bmatrix} + \begin{bmatrix} X_\alpha^- \\ X_\beta^- \end{bmatrix} \quad (4.14)$$

$$\begin{bmatrix} Z_\alpha \\ Z_\beta \end{bmatrix} = \omega \left(\begin{bmatrix} -X_\beta^+ \\ X_\alpha^+ \end{bmatrix} + \begin{bmatrix} X_\beta^- \\ -X_\alpha^- \end{bmatrix} \right) \quad (4.15)$$

Finally (4.16)-(4.18) can be obtained as:

$$\frac{d}{dt} \begin{bmatrix} Y_\alpha \\ Y_\beta \end{bmatrix} = 2k_i \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} + \begin{bmatrix} Z_\alpha \\ Z_\beta \end{bmatrix} \quad (4.16)$$

$$\frac{d}{dt} \begin{bmatrix} Z_\alpha \\ Z_\beta \end{bmatrix} = -\omega^2 \begin{bmatrix} Y_\alpha \\ Y_\beta \end{bmatrix} \quad (4.17)$$

$$\begin{bmatrix} I_\alpha^* \\ I_\beta^* \end{bmatrix} = \begin{bmatrix} Y_\alpha \\ Y_\beta \end{bmatrix} + 2k_p \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \quad (4.18)$$

Where $\begin{bmatrix} Y_\alpha \\ Y_\beta \end{bmatrix}$ and $\begin{bmatrix} Z_\alpha \\ Z_\beta \end{bmatrix}$ are the state variables related to the PI controller in the stationary

α - β frame; the input of the controllers are the stationary frame voltage errors $\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix}$, and

the outputs are the reference signal, $\begin{bmatrix} I_\alpha^* \\ I_\beta^* \end{bmatrix}$, for the inner current loop.

Analyzing (4.16)-(4.18), it is obvious that there is no cross coupling term in the α - β frame, and the equations can be expressed in state-space form by representing (4.16)-(4.18) as (ω is the grid fundamental angular frequency):

$$\begin{bmatrix} \dot{Y}_\alpha \\ \dot{Y}_\beta \\ \dot{Z}_\alpha \\ \dot{Z}_\beta \end{bmatrix} = U \cdot \begin{bmatrix} Y_\alpha \\ Y_\beta \\ Z_\alpha \\ Z_\beta \end{bmatrix} + W \cdot \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \quad (4.19)$$

$$\begin{bmatrix} I_\alpha^* \\ I_\beta^* \end{bmatrix} = C \cdot \begin{bmatrix} Y_\alpha \\ Y_\beta \\ Z_\alpha \\ Z_\beta \end{bmatrix} + D \cdot \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \quad (4.20)$$

$$\text{where } U = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ -\omega^2 & 0 & 0 & 0 \\ 0 & -\omega^2 & 0 & 0 \end{bmatrix}, W = \begin{bmatrix} 2k_i & 0 \\ 0 & 2k_i \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}, D = \begin{bmatrix} 2k_p & 0 \\ 0 & 2k_p \end{bmatrix}.$$

By using the state-space techniques the second-order stationary-frame controllers can be derived as in (4.21):

$$C \cdot (sI - U)^{-1} \cdot W + D = \begin{bmatrix} 2k_p + \frac{2k_i s}{s^2 + \omega^2} & 0 \\ 0 & 2k_p + \frac{2k_i s}{s^2 + \omega^2} \end{bmatrix} \quad (4.21)$$

Another method using frequency domain techniques can also derive these stationary controllers as in [51], and the second-order stationary-frame controller is called P+resonant controller. In this work, (4.21) is used for implementing the voltage controllers as it allows processing of the α - β variables directly without any intermediate α - $\beta \leftrightarrow d$ - q variable transformations. This method is not only computationally more efficient, but the steady-state voltage errors are also forced (both positive- and negative-sequence components) to zero by having infinite gains at frequencies $\pm\omega$.

The outputs of the voltage controllers are the sums of the positive- and negative-sequence reference inductor currents, expressed in the stationary frame as $\{ I_\alpha^*, I_\beta^* \}$. These demanded reference current signals are transformed to the stationary a-b-c frame using matrix B in (4.22), and fed into the inner current control loop with peak current limiting capability. This inner current loop is implemented using only proportional controllers K_c with the three-phase inductor currents chosen as feedback variables, since it does not

influence the tracking accuracy of the outer voltage loop. With the chosen voltage and current controllers, and representing the inner current loop as a unity gain block (due to its dynamically fast response), the closed-loop “output voltage to reference” transfer function of shunt inverter A is derived as (4.23). Its corresponding bode plot is shown in Figure 4.4 with k_p and k_i chosen as 0.05 and 100 respectively (other system parameters are listed in Table 4.1). This figure shows the controller good performance at the fundamental frequency and its immunity to high frequency distortion.

$$B = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\sqrt{\frac{1}{6}} & \frac{\sqrt{2}}{2} \\ -\sqrt{\frac{1}{6}} & -\frac{\sqrt{2}}{2} \end{bmatrix} \quad (4.22)$$

$$V_D = \frac{2k_p s^2 + 2k_i s + 2\omega^2 k_p}{Cs^3 + 2k_p s^2 + (\omega^2 C + 2k_i)s + 2\omega^2 k_p} V^* \quad (4.23)$$

Figure 4.4. Bode plot of closed-voltage-loop of shunt inverter A for three-wire compensator.

4.2.2 Control of series three-leg inverter B

The circuit connection of series inverter B is shown in Figure 4.1. For the proposed microgrid application, this series inverter is controlled to maintain a balanced set of line currents (I_{Linea} , I_{Lineb} and I_{Linec}) along the distribution feeder by suppressing negative-sequence current flow through the injection of appropriate negative-sequence voltages (V_{Ca} , V_{Cb} and V_{Cc}). Controlled in this way, series inverter B is expected to supply zero real and reactive power to the grid system as it injects only negative-sequence voltages along the feeder, which now conducts only positive-sequence currents. Obviously, this method of control is different from that used in a series Dynamic Voltage Restorer (DVR) whose main functionality is to improve the downstream load voltage quality by generating suitable series voltages to compensate for the upstream utility voltage sags. It is also commented here that the series inverter is not designed for controlling the positive-sequence currents in this mode of operation, since these are already (directly) regulated by shunt inverter A.

Figure 4.5. Control scheme of series three-leg inverter B.

Figure 4.5 shows the control scheme for series inverter B, where an inner voltage loop is shown embedded within an outer current loop. The outer current loop (also referred to as the reference voltage generator) functions to generate reference voltages for the inner voltage loop using the negative-sequence line currents as inputs. As seen, the measured

line currents are first transformed to the negative synchronous reference frame and then controlled to follow zero reference values. The outputs of this outer reference voltage generator, consisting only of negative-sequence components, are then transformed back to the α - β frame and fed into the inner voltage control loop. As this method of control to balance the line currents using a series inverter has not been recorded in the literature, its design will be covered in detail, as follows.

Figure 4.6. Block diagram of closed-voltage-loop of series inverter B ($K_{inv} = 2/V_{dc}$).

As a common practice, the design of the proposed control algorithm for the series inverter begins with the voltage loop in the α - β frame. If open-loop voltage control is to be applied with pure negative-sequence reference voltages, the voltages generated at the series transformers will have both positive- and negative-sequence components. This is because although inverter B (unfiltered) output contains pure negative-sequence voltages, the positive-sequence line currents induce positive-sequence voltages across the filter inductors, which also appear across the series transformers. Therefore, to produce the desired pure negative-sequence voltages across the series injection transformers to balance the line currents, a closed-loop voltage control scheme is used, as shown in Figure 4.6, where the P+resonant controllers as in (4.21) are used for voltage control. Initial comparison between the controls of shunt inverter A and series inverter B might suggest that a filter inductor current loop can be embedded within the inner voltage loop of inverter B to improve its dynamic response. Further observation however reveals that the dynamics of inverter B is limited solely by the relatively slower outer reference voltage generation loop. Therefore, filter inductor current feedback is considered not necessary and only a single voltage loop is used for this application. (It should be noted that with an inner current loop, more damping of the LC filter resonance could be achieved).

For analysis, the closed-loop transfer function of Figure 4.6 is derived and given in (4.24). Also shown are the Routh stability criteria of (4.25) and (4.26), which must be met for the inner voltage loop, to ensure stability. To confirm the robustness of inverter B control scheme, a typical distribution system where the line reactance is either the same or smaller than the line resistance [53], is considered. Here the series transformer leakage impedance is lumped together with the line impedance for simplicity. Even with an onerous condition of $X_{Line} = (2\pi f)L_{Line} = 2R_{Line}$ for this distribution system, the stability condition (4.25) becomes $L_f - \frac{2k_i R_{Line}}{\pi^2 f^2} > 0$, which can easily be met. Consequently, (4.26) can also be met since the α term in (4.26) is now minimized by having a relatively larger denominator than numerator (the numerator is usually small due to the presence of a μF capacitive term C_f).

$$G_{vcl} = \frac{k_p L_{Line} s^3 + (2k_p R_{Line} + 2k_i L_{Line}) s^2 + (2k_p \omega^2 L_{Line} + 2k_i R_{Line}) s + 2k_p \omega^2 R_{Line}}{L_f C_f L_{Line} s^5 + L_f C_f R_{Line} s^4 + (L_f + L_{Line} + 2k_p L_{Line} + L_f C_f L_{Line} \omega^2) s^3 + (2k_p R_{Line} + 2k_i L_{Line} + R_{Line} + L_f C_f R_{Line} \omega^2) s^2 + [(2k_p + 1) \omega^2 L_{Line} + \omega^2 L_f + 2k_i R_{Line}] s + (2k_p + 1) \omega^2 R_{Line}} \quad (4.24)$$

$$L_f - \frac{2k_i L_{Line}^2}{R_{Line}} > 0 \quad (4.25)$$

$$2k_p R_{Line} + 2k_i L_{Line} + R_{Line} + L_f C_f R_{Line} \omega^2 - \frac{\overbrace{2k_i L_f C_f R_{Line}^2 + L_f^2 C_f R_{Line} \omega^2}^{\alpha}}{L_f - \frac{2k_i L_{Line}^2}{R_{Line}}} > 0 \quad (4.26)$$

Figure 4. 7. Control of series three-leg inverter B in negative synchronous frame: (a) filtering of positive-sequence currents and (b) closed-current-loop.

Once the design of the inner voltage loop is completed, the next step is to design the reference voltage generator in the negative synchronous frame (negative synchronous frame is used because the series inverter regulates only the negative-sequence line current, and a zero reference can be easily set in this frame compared to the stationary frame with a P+resonant controller requiring a reference for positive-sequence current, which is directly controlled by the shunt inverter). In the negative synchronous frame, negative-sequence line currents are transformed to DC signals, whereas positive-sequence currents are transformed to AC signals at twice the fundamental frequency. These AC signals should be filtered out to avoid the interference with positive-sequence current control in the shunt inverter. In this work, filtering is performed by averaging the currents over half a fundamental cycle in the negative synchronous frame, as shown in Figure 4.7(a). Using MATLAB control system toolbox to compute the second order Pade approximation of the transport delay block with $f_0 = 50$ Hz, the transfer function of the mean value calculation block can be expressed as in (4.27):

$$G_{lp} = \frac{1 - e^{-s/2f_0}}{s} 2f_0 = \frac{120000}{s^2 + 600s + 30000} \quad (4.27)$$

By representing the inner voltage loop as a unity gain (this is reasonable since the outer reference voltage generation loop is relatively slow), the series inverter connected system can be represented in the negative synchronous frame as in Figure 4.7(b), where the coupling effects of the system are taken into account and measures have been taken to achieve decoupling (indicated by dotted lines in the figure). Analyzing this figure, the closed-current-loop transfer function for the d- and q-axes is derived as:

$$G_{kl} = \frac{k_p s + k_i}{L_{Line} s^2 + (R_{Line} + k_p) s + k_i} \quad (4.28)$$

Using (4.28) and choosing k_p as 1.5 and k_i as 80, the gain margin, phase margin and settling time of the outer voltage generation loop are set to infinity, 114° and 0.2s respectively. With further consideration of the dynamics of the mean value calculation filter, bode plots of G_{kl} and $G_{kl} \cdot G_{lp}$ are drawn in Figure 4.8, where the bandwidths of G_{kl} and $G_{kl} \cdot G_{lp}$ remain close to each other due to the large difference of bandwidths between G_{kl} (3.4 Hz) and G_{lp} (43 Hz). This in turn ensures a stable and robust controller performance.

Figure 4. 8. Bode plots of G_{kl} and $G_{kl} \cdot G_{lp}$

Another concern for the negative synchronous frame control is the requirement of angular frequency ω for the frame transformation. Normally, ω is obtained by a phase locked loop (PLL) algorithm, which accurately tracks the system frequency. While for the microgrid, the tracking of frequency does not require a PLL. This is because for the shunt inverter, the power loop outputs are voltage amplitude (E) and frequency (ω), and therefore the microgrid system frequency information can be obtained from the shunt inverter control loop. Subsequently, phase angle ωt or $\int \omega dt$ used for the series inverter can be calculated using the system frequency obtained from the shunt inverter. Similarly, the fundamental frequency f_0 required for mean value calculation, as shown in Figure 4.7(a), and ω for the controller in (4.21) can again be obtained from the shunt inverter control loop.

4.3 Simulation Results on the Three-Wire Microgrid System

Simulations using MATLAB/SIMULINK have been carried out to test the effectiveness of the proposed three-wire compensator, as shown in Figure 4.1. The system parameters used have been selected to represent those of typical distribution systems in [53], and are given in Table 4.1 (the transformer leakage resistance and inductance are lumped with R_{Line} and L_{Line} , as mentioned in Section 4.2.2). In addition, to emulate the digitally controlled experimental system implemented in Section 4.4, simulations have been performed with zero-order-hold blocks added to all feedback variables.

Figure 4.9(a) and (b) show the utility and microgrid load voltages respectively. Initially, the utility voltages are maintained balanced. At $t = 1.5s$, they are intentionally made unbalanced by introducing 0.1 p.u. negative-sequence and 0.1 p.u. zero-sequence voltage components to the utility grid. With shunt inverter A in action, the load voltages in the microgrid are shown to be balanced throughout the simulated period, confirming the effect of inverter A in enhancing the quality of power in the microgrid. Similarly, with series inverter B added, the line currents are brought back to balanced condition with the

negative-sequence current components gradually suppressed, as shown in Figure 4.10(a) and (b). This balancing effect is achieved through proper injection of negative-sequence voltages (V_{Ca} , V_{Cb} and V_{Cc} in Figure 4.1) by the series inverter from $t = 1.5$ s onwards, as shown in Figure 4.10(c). To further confirm the proper functioning of the proposed compensator, Figure 4.11(a) and (b) show shunt inverter A dispatching the specified real power of 300W and reactive power of 160Var, while Figure 4.11(c) and (d) show zero real and reactive power injection of series inverter B, as analyzed in Section 4.2.2.

Figure 4. 9. Simulated three-wire system: (a) utility grid voltages and (b) sensitive load voltages in the microgrid.

Figure 4. 10. Simulated three-wire system: (a) line currents, (b) negative-sequence line currents in the negative synchronous frame and (c) filtered voltages generated by series inverter B.

Figure 4. 11. Simulated three-wire system: (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B

4.4 Experimental Verification of the Three-Wire Compensator

The performance of the proposed three-wire compensator is verified experimentally using the hardware prototype described in Section 3.6, Chapter 3. The system parameters are chosen same as in simulation (Table 4.1). For the experimental system, a programmable AC source is used to represent the utility grid and is connected to an emulated microgrid through a three-phase back-to-back SCR isolation switch. The microgrid consists of the proposed three-wire compensator (a shunt IGBT inverter and a series IGBT inverter with an injection transformer), which is controlled using a dSPACE DS1103 controller card, and a connected RL load. To ensure proper starting of the experimental system, the utility and microgrid are powered up separately. After synchronizing the voltages at both ends of the SCR switch, the switch is closed to connect the microgrid and utility, allowing the system to transit smoothly into the grid-connected mode of operation.

Figure 4.12(a) and (b) show the utility voltages and microgrid load voltages respectively. At $t = 3.8$ s, the utility voltages become unbalanced with 0.1 p.u. negative-sequence and 0.1 p.u. zero-sequence voltage components added. Despite this unbalance in utility voltages, the load voltages in the microgrid are kept balanced by controlling shunt inverter A. Similarly, by controlling series inverter B, the currents flowing between the microgrid and utility grid can be balanced, as shown in Figure 4.13(a). Other performance features such as the suppression of negative-sequence line currents and injection of negative-sequence voltages by series inverter B are shown in Figure 4.13(b) and (c) respectively. Figure 4.14(a) to (d) show the real and reactive power supplied by the shunt and series inverters. These figures clearly show the shunt inverter supplying its specified dispatched power of 300W and 160Var, and the series inverter injecting zero real and reactive power, as anticipated.

Figure 4. 12. Experimental three-wire system: (a) utility grid voltages and (b) sensitive load voltages in the microgrid.

Figure 4. 13. Experimental three-wire system: (a) line currents, (b) negative-sequence line currents in the negative synchronous frame and (c) filtered voltages generated by series inverter B.

Figure 4. 14. Experimental three-wire system: (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B.

4.5 Power Quality Compensator for Three-Phase Four-Wire Microgrid Implementation

(a)

(b)

Figure 4. 15. Proposed four-wire microgrid compensator (a) overall system structure and (b) inverter topology.

With consideration of a possible four-wire microgrid configuration, this section presents a three-phase four-wire grid-interfacing power quality compensator for four-wire microgrid application. The dual-inverter compensator, proposed for use with each individual DG system in the microgrid, consists of two four-leg inverters (a shunt and a series), optimally controlled to compensate for all the unwanted positive-, negative- and zero-sequence voltage/current components found within an unbalanced utility grid. Figure 4.15 shows the general layout of the proposed dual-inverter power quality compensator. Similar to the three-wire compensator proposed in Section 4.2, the shunt four-leg inverter is controlled to ensure balanced voltages within the microgrid, to regulate power sharing among the parallel-connected DG systems, and to incorporate synchronization algorithms for ensuring smooth and safe reconnection of the microgrid and utility system. The series

inverter is controlled complementarily to inject negative- and zero-sequence voltages in series to balance the line currents, while generating zero real and reactive power. The four-leg compensator system is useful especially where there are zero sequence components in the system as a result of unbalance load or supply conditions.

4.5.1 Control of shunt four-leg inverter A

4.5.1.1 Description of control algorithm

Figure 4. 16. Control scheme for shunt four-leg inverter A (a) overall control structure and (b) voltage control algorithm.

As shown in Figure 4.16(a), the control system of shunt inverter A contains a voltage/current regulation block, and external real and reactive power control blocks similar to the control scheme of shunt inverter of the three-wire compensator. For the three-phase-leg and four-phase-leg compensators, the power control blocks are almost same with the only difference being that outputs of the power controllers, which are the reference frequency ω , phase δ and the positive-sequence voltage magnitude E , are transformed to stationary α - β -0 frame quantities $\{V_\alpha^*, V_\beta^*, V_0^*\}$, used as reference voltages for the voltage/current regulation block for the four-phase-leg compensator. Since the outputs of power loops are only of positive-sequence components, the zero-sequence reference voltage V_0^* is zero. While for the three-leg compensator, the reference voltages are $\{V_\alpha^*, V_\beta^*\}$, without V_0^* due to the lacking of neutral lines.

Figure 4.16(b) shows the voltage/current regulation scheme for inverter A, which contains an inner filter inductor current control loop and an outer load voltage control loop. For the outer voltage loop, the theoretical analysis is again first presented in the synchronous d-q-0 reference frames to assist in understanding the control principles. The developed voltage controllers are subsequently converted back to the stationary frame to allow for easier physical implementation. This approach is similar to that used in Section 4.2, but here an effort is put on the frame transformations for four-leg inverter.

As illustrated in Figure 4.16(b), the three-phase load voltages are first transformed from the stationary a-b-c frame to the stationary α - β -0 frame using the following quad transformation matrices [54]:

$$U_{\alpha\beta 0} = \sqrt{\frac{2}{3}} T_{\alpha\beta 0} U_{abcn} \quad (4.29)$$

$$U_{\alpha\beta 0} = \begin{bmatrix} U_\alpha & U_\beta & U_0 \end{bmatrix}^T \quad (4.30)$$

$$U_{abcn} = \begin{bmatrix} U_{an} & U_{bn} & U_{cn} & U_n \end{bmatrix}^T \quad (4.31)$$

$$T_{\alpha\beta 0} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \end{bmatrix} \quad (4.32)$$

where U_n is a placeholder quantity, usually chosen to be 0 [54]. The α - β -0 voltages are subsequently transformed to the forward rotating positive-sequence synchronous frame (indicated with superscript “+”) and reverse-rotating negative-sequence frame (indicated with superscript “-”) using the following transformation matrices:

$$U_{dq0}^+ = \begin{bmatrix} U_d^+ & U_q^+ & U_0^+ \end{bmatrix}^T = T_{dq0}^+ U_{\alpha\beta 0} \quad (4.33)$$

$$T_{dq0}^+ = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (4.34)$$

$$U_{dq0}^- = \begin{bmatrix} U_d^- & U_q^- & U_0^- \end{bmatrix}^T = T_{dq0}^- U_{\alpha\beta 0} \quad (4.35)$$

$$T_{dq0}^- = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & 0 \\ -\sin(\omega t) & -\cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (4.36)$$

Note that the first two rows of $T_{\alpha\beta 0}$, T_{dq0}^+ and T_{dq0}^- resemble the commonly used three-phase “a-b-c to α - β to d-q” transformation. Equations (4.29) to (4.36) can therefore be viewed as simply an extension from the three-phase “a-b-c to α - β to d-q” transformation with only an independent zero-sequence row added. It would therefore be convenient to control the d-q voltages independently from the zero-sequence voltages, as indicated in Figure 4.16(b) with the zero-sequence control path drawn external to the dotted box enclosing the d-q control paths.

To achieve zero steady-state errors when controlling the positive- and negative-sequence d-q voltages, two PI controllers are used along the positive- and negative-sequence d-q

control paths. Similarly, the implementation of these d-q controllers can be transformed to the stationary α - β frame using either the state-space technique as in Section 4.2.1 or frequency-domain technique in [51]. Performing this inverse transformation with $k_p^+ = k_p^- = k_p$ and $k_i^+ = k_i^- = k_i$, the α - β frame voltage controllers can be derived same as the P+resonant controllers for shunt inverter of the three-wire compensator as expressed in (4.21).

Figure 4. 17. Bode plots of P+resonant compensators using (a) (4.21) and (b) (4.39) with $k_p=1$, $k_i=20$, $\omega=314\text{rad/s}$ and $\omega_{cut}=10\text{ rad/s}$.

As analyzed in Section 4.2, these voltage controllers (P+resonant) introduce an infinite gain at the positive (50Hz) and negative (-50Hz) fundamental frequencies to force the positive- and negative-sequence voltage errors to zero (see Figure 4.17(a) for an example bode plot of (4.21) using a positive resonant frequency of 50Hz), and can conveniently be implemented in the stationary α - β frame with minimum computational requirements. The same P+resonant compensator with the resonant frequency set at 50Hz can also be used for controlling the zero-sequence voltage, again with zero steady-state error, as shown in Figure 4.16(b).

The outputs of the individual voltage controllers when added together, give the demanded reference currents I_α^* , I_β^* and I_0^* for the inner filter inductor current loop. This inner loop is implemented using only proportional controllers with peak current limiting in the stationary α - β -0 frame as any steady-state error in this loop would not affect the outer voltage loop accuracy substantially. The outputs of the current controllers are then transformed back to the a-b-c frame and sent to a four-phase-leg PWM modulator for switching shunt inverter A.

4.5.1.2 Closed-loop transfer functions

As for the dynamics of the outer voltage loop is concerned, the inner current loop is considered to be having fast dynamic response. The inner loop can therefore be represented as a constant gain and the closed-loop transfer functions of inverter A control scheme can be derived in the α - β frame as:

$$V = \frac{2k_p s^2 + 2k_i s + 2\omega^2 k_p}{Cs^3 + 2k_p s^2 + (\omega^2 C + 2k_i)s + 2\omega^2 k_p} V^* \quad (4.37)$$

and along the zero-sequence axis as:

$$V = \frac{k_p^0 s^2 + 2k_i^0 s + \omega^2 k_p^0}{Cs^3 + k_p^0 s^2 + (\omega^2 C + 2k_i^0)s + \omega^2 k_p^0} V_0^* \quad (4.38)$$

Both (4.37) and (4.38) are third order transfer functions, and by choosing $2k_p = k_p^0 = 0.1$ and $k_i = k_i^0 = 100$, they share the same bode plot, as shown in Figure 4.18. This figure clearly indicates good fundamental compensation and rapid high frequency attenuation of the controller.

Figure 4. 18. Bode plot of closed-voltage-loop of inverter A in four-wire compensator.

4.5.2 Control of series four-leg inverter B

4.5.2.1 Description of control algorithm

The circuit connection of series inverter B is shown in Figure 4.15(a), where a four-leg inverter is again adopted for the control of zero-sequence component. The main function of the series inverter is to maintain a set of balanced line currents; i.e. to force the negative- and zero-sequence currents to zero in the three-phase four-wire system. Similar to the three-wire compensator, this series four-leg inverter is not designed to control the positive-sequence currents under unbalanced PCC voltage.

Figure 4.19. Control scheme for series four-leg inverter B (a) general representation (b) outer current loop in the negative synchronous frame.

Figure 4.19(a) shows the control scheme for series inverter B, where an inner voltage loop is shown embedded within an outer current loop. The outer current loop functions to generate reference voltages for the inner voltage loop using the negative- and zero-sequence line currents as inputs. As seen, the measured line currents are first transformed to the negative synchronous d-q-0 reference frame using (4.29) and (4.35), and regulated with zero reference values, using PI controllers for the negative-sequence d-q currents and a P+resonant controller for the zero-sequence component (see Figure 4.19(b)). (Note the

use of a non-ideal P+resonant controller along the zero-sequence control path, which is explained in the next subsection 4.5.2.2). Also shown in Figure 4.19(b) are measures taken to decouple the d- and q-control paths (indicated by dotted lines in the figure) to arrive at three decoupled d-, q- and 0-axis control paths, which can be tuned independently. The outputs of this outer reference voltage generator, consisting only of negative- and zero-sequence components, are then transformed back to the α - β -0 frame and fed into the inner voltage control loop.

The block representation of the inner voltage loop is same as Figure 4.16 (and is not shown again here), where P+resonant controllers are used along the α - β -0 control paths. The use of P+resonant controllers in the inner control loop will force the filtered capacitor voltages V_c of the series inverter to track the demanded negative- and zero-sequence reference voltages V_c^* with zero steady-state errors, and eliminate any positive-sequence component since its reference value is kept at zero for the series inverter. The series inverter therefore injects only negative- and zero-sequence voltages into the system to maintain a set of balanced line currents with no real and reactive power generation (or absorption) in the steady state.

Similarly, an inner filter inductor current loop can be added to the voltage control loop to give a better dynamic response; and due to the slow response of the outer reference voltage generation loop, a single inner voltage loop is considered sufficient and this loop can reasonably be represented by a unity gain when designing the control scheme.

4.5.2.2 Closed-loop transfer functions

The design of the proposed control algorithm for the series inverter begins with the inner voltage loop in the α - β -0 frame. Analyzing inner voltage loop (see Figure 4.16) with $K_{inv} = 2/V_{dc}$, the closed-loop transfer function of it can be derived same as (4.24) in Section 4.2.2, where R_{Line} and L_{Line} which normally represent line resistance and inductance, are lumped together with the series transformer winding parameters for convenience. When performing zero-sequence analysis neutral line parameters are also lumped into R_{Line} and

L_{Line} . From the analysis in Section 4.2.1, it is clear that closed inner voltage loop is stable for a typical microgrid at the distribution side. And the Routh's stability criteria of (4.25) and (4.26) can be easily met for the inner voltage loop.

Once the design of the inner voltage loop is completed, the next step is to design the outer reference voltage generator in the negative synchronous reference frame. Again, the AC signals in the negative synchronous d-q frame is filtered out first by averaging the d-q currents over half a fundamental cycle as discussed in Section 4.2.2.

Another consideration when designing the reference generator is to identify an alternative non-ideal resonant controller (see Figure 4.17(b)) for use along the zero-sequence control path, whose transfer function is expressed as [51]:

$$k_p^0 + \frac{2k_i^0 \omega_{cut} s}{s^2 + 2\omega_{cut} s + \omega^2} \quad (4.39)$$

where ω_{cut} represents the low-frequency cutoff. An example bode plot of (4.39) is given in Figure 4.17(b), which obviously shows a wider resonant peak with a large finite gain, as compared to Figure 4.17(a). Equation (4.39) is therefore less sensitive to frequency fluctuation and the steady-state error would be still kept relatively small. This non-ideal controller should generally be used in cases with resonant frequency variations, and is particularly applicable to the experimental series inverter implemented in Section 4.7. Through experimental observation, the sampling of the measured line currents causes the frequency of the calculated zero-sequence component I_{Line0} to fluctuate slightly, which is suspected to be related to asynchronous switching of the inverter neutral leg. (In the prototype, the inverter neutral leg is asynchronously switched by an external analog comparator and triangular signal generator due to the shortage of synchronized PWM channels on the dSPACE DS1103 controller card.) Therefore the non-ideal P+resonant compensator with a wider resonant bandwidth is needed for reducing the system sensitivity level.

Incorporating these fine-tuning schemes, the final closed-loop transfer functions of the proposed control algorithm can be written as (4.40) in the negative d-q frame and (4.41) along the 0-axis.

$$G_{Icl} = \frac{k_p s + k_i}{L_{Line} s^2 + (R_{Line} + k_p) s + k_i} \quad (4.40)$$

$$G_{Icl} = \frac{k_p^0 s^2 + 2\omega_{cut}(k_p^0 + k_i^0)s + \omega^2 k_p^0}{L_{Line} s^3 + (2\omega_{cut} L_{Line} + R_{Line} + k_p^0) s^2 + (\omega^2 L_{Line} + 2\omega_{cut} R_{Line} + 2\omega_{cut} k_p^0 + 2\omega_{cut} k_i^0) s + \omega^2 (R_{Line} + k_p^0)} \quad (4.41)$$

Using (4.40) and setting $k_p = 1.5$ and $k_i = 80$, the gain margin, phase margin and settling time of the outer voltage generation loop in the negative d-q frame are set to infinity, 114° and 0.2s respectively. For the 0-axis, setting $k_p^0 = 16$, $k_i^0 = 200$ and $\omega_{cut} = 10$ rad/s, and using the open-loop bode plot in Figure 4.20 for the zero-sequence control path with the neutral line impedance included (see Table 4.1 for the neutral impedance parameters), the gain and phase margins are set to infinity and 89.7° respectively. Together, these selected control parameters ensure the stability of series inverter B.

Figure 4. 20. Open-loop bode plot of zero-sequence control path.

4.6 Simulation Results on the Four-Wire Microgrid System

Simulation results using MATLAB/SIMULINK are provided to verify the effectiveness of the proposed system. The system parameters used for simulation are given in Table 4.1. Figure 4.21(a) shows the voltage profile used for simulation where the grid voltages are initially balanced. From $t = 1.2\text{s}$ onwards, negative sequence voltages of 0.1 p.u. and zero-sequence voltages of 0.1 p.u. are added to the original balanced voltages.

With the proposed dual-inverter compensator added, Figure 4.21(b) and (c) show that the sensitive load voltages in the microgrid are kept well balanced even under unbalanced utility voltage conditions. This clearly verifies the performance of shunt inverter A in maintaining good power quality within the microgrid. Figure 4.22(a) and (b) show the extremely unbalanced line currents under grid voltage unbalance and without the functioning of series inverter B, which can cause system complications, as described in Section 4.5. By operating series inverter B, these unbalanced line currents can be mitigated, as illustrated in Figures 4.23 and 4.24. Figure 4.23(a) shows the filtered voltages (V_{Can} , V_{Cbn} and V_{Ccn} , see Figure 4.15(a)) generated by series inverter B during the transient period of inverter B activation (from 1.15s to 1.5s), while Figure 4.23(b) shows the zoomed-IN view of the voltages in the steady-state (from 1.9s onwards), which clearly show the presence of only negative- and zero-sequence components. The performance of series inverter B is further verified by observing the line currents shown in Figure 4.24(a) and (b). In these figures, the initial unbalanced line currents quickly become balanced again due to the proper control action of inverter B.

Figure 4.25(a) to (d) show the power generated by the two inverters. As illustrated in these figures, shunt inverter A dispatches a constant real power of 300W and a reactive power of 160Var in the steady-state, while series inverter B constantly maintains zero real and reactive power output. The zero power output of series inverter B is expected since it injects only negative- and zero-sequence voltages into a system where only positive-sequence line currents flow.

Figure 4. 21. Simulated four-wire system waveforms of (a) mains grid voltages, (b) a-b-c frame sensitive load voltages in the microgrid and (c) α - β -0 frame sensitive load voltages in the microgrid.

Figure 4. 22. Simulated four-wire system line currents without series inverter B: (a) a-b-c frame and (b) negative d-q-0 frame.

Figure 4. 23. Simulated four-wire system filtered voltages generated by series inverter B: (a) a-b-c frame and (b) α - β -0 frame (zoomed-IN view in the steady-state).

Figure 4. 24. Simulated four-wire system line currents with series inverter B: (a) a-b-c frame and (b) negative d-q-0 frame.

Figure 4. 25. Simulated four-wire system waveforms of (a) real power supplied by shunt inverter A, (b) reactive power supplied by shunt inverter A, (c) real power supplied by series inverter B and (d) reactive power supplied by series inverter B.

4.7 Experimental Verification of the Four-Wire Compensator

A hardware prototype of the three-phase four-wire microgrid system has been built in the laboratory, which has the same system parameters as in simulation (Table 4.1). The proposed four-leg compensator is made of a shunt four-leg IGBT inverter and a series four-leg IGBT inverter with an injection transformer. The control algorithms are implemented on a dSPACE DS1103 controller card. The dSPACE DS1103 control board can provide maximum 7 PWM channels, while an additional PWM channel is required for the switching of the proposed four-leg compensator. This additional channel is provide by using a D/A converter of the DS1103 controller card for outputting the sinusoidal modulating signal, which is compared with the triangle carrier generated by an external signal generator. Outputs of the comparison unit (LM311), which is 0-5 V is then up rated to 0-15 V and fed to the IGBT driver to switch the neutral leg of series inverter.

As discussed in Section 4.5.2.2, this asynchronously PWM switching of series inverter fourth leg caused slight frequency variation in the neutral line current waveform.

Figure 4.26(a) to (c) show the utility voltages and microgrid load voltages, which are initially balanced. At $t = 3.775\text{s}$, the utility voltages become unbalanced with 0.1 p.u. negative-sequence and 0.1 p.u. zero-sequence voltage components added. Despite this unbalance in utility voltages, the load voltages in the microgrid are kept balanced by controlling shunt inverter A. Similarly, to balance the currents flowing between the microgrid and utility, series inverter B is operated with its injected negative- and zero-sequence voltages shown in Figure 4.27(a) and (b).

As compared to their simulated counterparts in Figure 4.23, the experimental α - β waveforms in Figure 4.27(b) are observed to be oscillatory, whereas the 0-axis waveform is (nearly) undistorted. This is due to the relatively low experimental sampling frequency (5 kHz) used, which can cause oscillatory response in the system. Along the α - β control path for series inverter B (see Section 4.5.2), this oscillatory distortion is averaged out by the “half fundamental cycle” filter, and therefore not eliminated by the PI controllers. On the other hand, along the 0-axis control path where no filtering is performed, this distortion is directly compensated, and therefore has lesser effect on the system.

The effectiveness of series inverter B in balancing the line currents by suppressing negative- and zero-sequence current components is shown in Figure 4.28(a) and (b). Figure 4.29(a) to (d) show the real and reactive power supplied by the shunt and series inverters. These figures clearly show the shunt inverter supplying its specified dispatched power of 300W and 160Var, and the series inverter injecting zero real and reactive power, as anticipated.

Figure 4. 26. Experimental four-wire system waveforms of (a) mains grid voltages, (b) a-b-c frame sensitive load voltages in the microgrid and (c) α - β -0 frame sensitive load voltages in the microgrid.

Figure 4. 27. Experimental four-wire system filtered voltages generated by series inverter B: (a) a-b-c frame and (b) α - β -0 frame (zoomed-IN view in the steady-state).

Figure 4. 28. Experimental four-wire system line currents with series inverter B: (a) a-b-c frame and (b) negative d-q-0 frame.

Figure 4. 29. Experimental four-wire system waveforms of (a) real power supplied by shunt inverter A, (b) reactive power supplied by shunt inverter A, (c) real power supplied by series inverter B and (d) reactive power supplied by series inverter B.

Table 4.1. System parameters for simulation and experiment.

Parameter	Value
Nominal line-to-line grid voltage	120V
Nominal power	1kVA
Frequency	50Hz
DC supply voltage	250V
Switching frequency for both inverters	10kHz
Series inverter filter capacitance	10 μ F (0.05 pu)
Series inverter filter inductance	3.9mH (0.08 pu)
Series transformer turns ratio	1:1
Shunt inverter filter capacitance	30 μ F (0.14 pu)
Shunt inverter filter inductance	5mH (0.11 pu)
Line resistance R_{Line}	3 Ω (0.2 pu)
Line inductance L_{Line}	10mH (0.21 pu)
Neutral line resistance (four-wire microgrid)	1 Ω (0.06 pu)
Neutral line inductance (four-wire microgrid)	5mH (0.11 pu)
Grid dispatch power	300W, 160Var
Sensitive load in the microgrid	120W, 90Var

4.8 Discussion

This chapter presents dual-inverter grid-interfacing power quality compensators (three-phase three-wire or three-phase four-wire) for microgrid applications. Controlled properly, each proposed compensator, using a shunt and a series inverter, could enhance both the quality of power within the microgrid and the quality of currents flowing between the microgrid and utility system. Functionally, the shunt inverter is controlled to maintain a set of balanced, distortion-free voltages within the microgrid and to regulate power sharing among the parallel-connected DG systems. To complement, the series inverter is controlled to inject negative-sequence (and zero-sequence for the four-leg compensator)

voltages in series to balance the line currents, generating zero real and reactive power during compensation. These control objectives of the proposed compensators are different from those of other reported power conditioners (e.g. unified power quality conditioners (UPQCs)). The proposed system has been tested in simulation and experimentally using a laboratory prototype with satisfactory results obtained for confirming the effectiveness of the compensators.

The control schemes for the compensators proposed in this chapter however need further fine-tuning to ensure satisfactory performance in the event of utility voltage sag and the flow of large fault currents must be limited. In the next chapter, the current-limiting algorithms are proposed and integrated within the compensator control schemes to protect the microgrid from large fault currents during utility voltage sags.

Chapter 5

Protection of Microgrid during Utility Voltage Sags

5.1 Introduction

As discussed in previous chapters, microgrids are systems with clusters of micro-generators, which are installed for distributed power generation. The formed microgrid is usually connected to the utility system and is therefore exposed to common utility power quality disturbances. These power disturbances can seriously influence the microgrid operation. In Chapter 4 an investigation of the impact of utility voltage unbalance on the microgrid is presented. The three-phase three- (or four-) wire dual-inverter power quality compensator is proposed for the microgrid implementation to enhance both the voltage quality in the microgrid and the quality of current flowing between the microgrid and the utility system under such utility voltage unbalances. While another particular area of concern is the large fault current flow along the interconnecting distribution feeder between the microgrid and utility system during utility voltage sags (assuming that voltages in the microgrid are well-regulated to prevent tripping of sensitive loads). As the number of DGs connected to the mains grid tends to increase tremendously, the simultaneous disconnection of DGs under fault conditions may lead to a reduction in power dispatch and an increase in system instability. Therefore it is essential that the DGs are kept connected during disturbances to support the mains grid [55]. To facilitate this additional requirement, the power converter units must be equipped with embedded fault tolerance capabilities.

To prevent the flow of large line currents and hence protect the microgrid, this chapter proposes two alternative current-limiting algorithms, termed as RL feedforward and flux-charge-model feedback algorithms, for use with a VSI connected in series between the microgrid and utility system. The algorithms are developed based on different control principles, but they respond similarly by effectively controlling the series VSI to mimic a large virtual RL or L impedance for limiting the line current flow during a sag. To assist

in choosing the appropriate algorithm for different applications, this chapter presents detailed descriptions of the algorithm theoretical principles, controller designs and parameter selection criteria. Phasor analyses of both methods are presented to show how the inserted RL or L values can be optimally tuned to improve the inverter damping performance, and minimize its injected voltages and circulating power under all operation conditions. A comparison table summarizing performance features of both algorithms is also presented. Lastly, both methods have been tested in simulation and experimentally using an emulated laboratory microgrid system.

5.2 General Operating Principles of the Proposed Current-Limiting Algorithms

Figure 5.1. Single-phase representation of microgrid system under study with specific voltage phasors indicated

The microgrid system studied in this work is shown in Figure 5.1. As shown, the DG source in the microgrid is interfaced to the utility grid using a shunt VSI (either of a three-leg or a four-leg configuration) whose functionalities, as stated in Chapter 4, are to regulate load voltages and power dispatches in the microgrid, maintain proper power sharing when the microgrid islands, and synchronize the microgrid and utility system for smooth reconnection when the system returns to the grid-connected mode of operation. An additional degree of control freedom can be added by using a second VSI (either of a three- leg or a four- leg configuration) series-connected along the distribution feeder to balance the current flow along the line even under continuous unbalanced utility grid conditions, as proposed in Chapter 4. Together, the two inverters enhance the quality of

power in the microgrid, and quality of current flowing between the microgrid and utility system.

The presented microgrid system in Figure 5.1 functions well under normal utility operating conditions. However, during utility voltage sags, large line currents can flow through the line impedance interconnecting the microgrid and utility system, which can be illustrated using Figure 5.1. During the sag period, the voltage phasor at the PCC $\vec{V}_{Sag}$ drops below its nominal value, while the load voltage phasor $\vec{V}_D$ is regulated to remain relatively constant at its nominal value to prevent tripping of sensitive loads. A large voltage difference ($\Delta \vec{V} = \vec{V}_D - \vec{V}_{sag}$) therefore appears across the series inverter and distribution feeder. If no current-limiting algorithm is implemented for the series VSI, large line currents can flow through the small line impedance $\{R_{Line}, L_{Line}\}$ until the clearance of sag, thus risking semiconductor devices in the inverters and system components in the microgrid from potential damages.

A technique to protect the microgrid from the above-mentioned damaging situations and to ride-through voltage sags is to control the series inverter as a large virtual current-limiting (RL or L) impedance in series with the distribution feeder immediately after the sensing of a voltage sag. As the PCC can be located far away from the series inverter, detection of voltage sags can only be done locally by measuring the three-phase line currents. Upon the instantaneous current value of a phase exceeding a specified threshold I_T , the series inverter responds by introducing a large impedance with a series-injected voltage of $\vec{V}_{Inj}$ to lift the voltage phasor $\vec{V}_E$ at the microgrid end of the feeder to a value close to $\vec{V}_{Sag}$ ($\vec{V}_E \approx \vec{V}_{Sag}$). The voltage drop ($\vec{V}_E - \vec{V}_{sag}$) across the line impedance $\{R_{Line}, L_{Line}\}$ and hence the line current through it are then significantly reduced. Maintaining $\vec{V}_E \approx \vec{V}_{Sag}$ also allows smooth recovery from a voltage sag by simply sensing $\vec{V}_E$, which will rise with $\vec{V}_{Sag}$ back to its nominal value, and after which, inhibiting the current-limiting action of the series inverter to return the microgrid back to normal operating conditions. In passing, it is commented that the current-limiting technique

presented in the chapter is equally applicable to other power quality conditioners using a series VSI such as unified power quality conditioner (UPQC), dynamic voltage restorer (DVR) etc., and would be able to limit fault currents effectively. The implementation of proposed flux-charge-model fault current limiting algorithm to a series grid interfacing VSI at medium voltage level is presented in Chapter 7.

For controlling the series inverter as a fault limiting impedance, two control implementations based on feedforward and feedback control theories are proposed. These control algorithms are presented in the following two sections.

5.3 RL Feedforward Current-Limiting Algorithms

This section presents the RL feedforward current-limiting algorithms for controlling the series inverter as a large virtual RL impedance during utility voltage sags.

5.3.1 Description of control algorithm and implementation issues

The block diagram representation of the RL feedforward algorithm is shown in Figure 5.2(a). To insert a virtual RL impedance upon sensing of a voltage sag by the “sag detection” block ($I_{Line} > I_T$), the algorithm simply measures and multiplies the line currents by an impedance of $(R_{inj} + sL_{inj})$, where ‘s’ is the Laplace operator, to give the desired series injection voltages. The calculated voltages are then fed forward as references to the voltage regulator or PWM modulator for controlling the series inverter.

Upon clearance of the sag, again detected by the “sag detection” block ($\vec{V}_E \approx \vec{V}_{Sag}$ rising back to its nominal value), the feeding forward of the RL impedance is inhibited and the microgrid returns to normal grid-connected mode of operation. Note that by using the feedforwarding approach, this current-limiting algorithm can be easily added in parallel with the series inverter’s negative (zero)-sequence current control scheme discussed in Chapter 4, and therefore can compensate an unbalanced voltage sag.

Figure 5. 2. RL feedforward current-limiting algorithm (a) control block diagram representation and (b) implementation representation.

Although theoretically feasible, this method has a few practical considerations, which must be analyzed before it can be used for controlling a physical inverter. Firstly, being a feedforward method, the RL algorithm has poor damping performance, which can only be improved by increasing the resistive value R_{Inj} of the inserted impedance. Increasing R_{Inj} however means that the series inverter absorbs more active power, which must be re-channelled through the shunt inverter back to the microgrid to prevent a surge in voltage across the DC link capacitor. A tradeoff in the selection of an appropriate value for R_{Inj} is therefore required, and the selected R_{Inj} and L_{Inj} values should preferably satisfy the optimal R/L ratio and worst-case criteria derived in the next two subsections. The second concern of the RL algorithm is the presence of a derivative term ('s' operator in the Laplace domain) needed for calculating the inductive injected voltage. Differentiation would cause high frequency noise amplification, which in turn would destabilize the microgrid at the instant of voltage sag. A common approach to avoid noise amplification is to add a first-order pole to the derivative term to flatten the high frequency gain of the resulting transfer function ($s/(s+p)$, where p is the added pole). This approach would however introduce phase errors into the control algorithms, which would in turn affect the optimal R/L ratio control presented in Section 5.3.2.

A more robust approach is therefore proposed here, which avoids differentiation by approximating $(R_{Inj} + sL_{Inj})$ as $(R_{Inj} + j\omega L_{Inj})$, where ω is the system angular frequency. This approximation is indicated in Figure 5.2(a), and can be implemented conveniently in the stationary $\alpha\beta$ or synchronous dq frame, as shown in Figure 5.2(b). In Figure 5.2(b), the measured three-phase currents are first transformed to the $\alpha\beta$ or dq frame to give I_{xy} ($= I_x + jI_y$), where xy represents $\alpha\beta$ or dq . I_{xy} is then converted to the polar form of $|I_{xy}| \angle \arg(I_{xy})$, where $|I_{xy}| = \sqrt{I_x^2 + I_y^2}$ and $\arg(I_{xy}) = \tan^{-1}(I_y/I_x)$. (In the dq frame with I_{dq} aligned to the d-axis (q-axis), $|I_{dq}|$ and $\arg(I_{dq})$ are simply given by I_d (I_q) and 0° (90°) respectively). Multiplying I_{xy} with the inserted impedance of $|Z_{Inj}| \angle \arg(Z_{Inj})$, where $|Z_{Inj}| = \sqrt{R_{Inj}^2 + (\omega L_{Inj})^2}$ and $\arg(Z_{Inj}) = \tan^{-1}(\omega L_{Inj}/R_{Inj})$, then gives the desired series injection voltages as $V_{Cxy}^* = |V_{Cxy}^*| \angle \arg(V_{Cxy}^*) = |I_{xy}| |Z_{Inj}| \angle (\arg(I_{xy}) + \arg(Z_{Inj}))$.

5.3.2 Optimal R/L ratio

Having two impedance control parameters, the RL algorithm can be optimized such that the voltage injected by the series inverter, and hence the voltage rating of the DC link capacitor, are minimized. To determine the optimal RL parameters, the following phasor equation for the circuit in Figure 5.1 is considered:

$$\Delta \vec{V} = \vec{V}_D - \vec{V}_{Sag} = \vec{V}_{Inj} + \vec{V}_{Line} = \vec{V}_{Inj} + R_{Line} \vec{I}_{Line} + L_{Line} \frac{d\vec{I}_{Line}}{dt} \quad (5.1)$$

where $\vec{I}_{Line}$ is the line current phasor. Equation (5.1) can also be represented graphically as in Figure 5.3(a) for a given voltage difference of $\Delta \vec{V}$. With a preset current limit of I_T , the feeder voltage drop $\vec{V}_{Line}$ should be controlled to lie anywhere within the dashed

circle with a fixed radius of $I_T \sqrt{R_{Line}^2 + (\omega L_{Line})^2}$, as indicated in Figure 5.3(a). For illustration, Figure 5.3(a) shows two possible orientations of $\vec{V}_{Line}$ on the dashed circle. These orientations give rise to two possible injected voltage phasors ($\vec{V}_{Inj}$ and $\vec{V}'_{Inj}$) for the series inverter. Comparing these voltage phasors, it is obvious that the injected voltage phasor of the series inverter is minimized by orientating $\vec{V}_{Inj}$ to be in phase with $\vec{V}_{Line}$. Mathematically, this condition is expressed as (where k_f is a constant):

$$\vec{V}_{Inj} = R_{Inj} \vec{I}_{Line} + L_{Inj} \frac{d \vec{I}_{Line}}{dt} = k_f \left(R_{Line} \vec{I}_{Line} + L_{Line} \frac{d \vec{I}_{Line}}{dt} \right) = k_f \vec{V}_{Line} \quad (5.2)$$

which simply implies that for minimal voltage injection, the series inverter must act like a virtual impedance $\{R_{Inj}, L_{Inj}\}$ whose ratio is proportional to that of the feeder impedance $\{R_{Line}, L_{Line}\}$.

Figure 5. 3. Phasor diagrams for analyzing (a) optimal R/L ratio and (b) worst-case condition.

5.3.3 Analysis of worst case condition

A further criterion to note when selecting values for R_{Inj} and L_{Inj} is that the worst voltage sag condition (largest $\Delta \vec{V}$) must be considered to make sure that $\vec{V}_{Line}$ lies within the dashed circle in Figure 5.3(a) under all operating conditions. The worst case condition can be analyzed by considering the phasor diagram in Figure 5.3(b), which shows the voltage phasors before and after an utility sag. Upon the occurrence of a sag, the PCC voltage phasor changes from $\vec{V}_{Grid}$ (pre-sag) to $\vec{V}_{Sag}$ with a certain magnitude drop and a phase-angle jump θ . Instantly, the shunt inverter controlled voltage phasor changes, for an example, from $\vec{V}_{D0}$ (pre-sag) to $\vec{V}_D$ with $\vec{V}_D = 0.9\vec{V}_{D0}$. $\Delta \vec{V}$ is then expressed as $\Delta \vec{V} = \vec{V}_D - \vec{V}_{Sag}$.

It is assumed that the worst-case sag condition for this study occurs when the utility voltage magnitude drops by 50% and $\theta = -60^\circ$, which is believed to be a typical worst-case scenario [15]. In addition, assuming that θ is the angle between $\vec{V}_D$ and $\vec{V}_{Sag}$ (since δ is usually small), and the magnitude of $\vec{V}_{D0}$ is nearly equal to that of $\vec{V}_{Grid}$ (rated utility voltage E), the largest magnitude of $\Delta \vec{V}$ can be calculated as $|\Delta \vec{V}| = 0.78E$. The required R_{Inj} and L_{Inj} can then be calculated using this limit, the given current limit I_T , line parameters $\{R_{Line}, L_{Line}\}$, the optimal condition of $\frac{R_{Inj}}{L_{Inj}} = \frac{R_{Line}}{L_{Line}}$ derived in Section 5.3.2 and the following expression:

$$(R_{Inj} + R_{Line})^2 + \omega^2 (L_{Inj} + L_{Line})^2 = \left| \Delta \vec{V} \right|^2 / I_T^2 \quad (5.3)$$

5.4 Flux-Charge-Model Feedback Current-Limiting Algorithm

The RL feedforward algorithm functions well, but results in active power circulating through the series and shunt inverters, as described in Section 5.3.1. In addition, practical implementation of the optimal R/L ratio in (5.2) is difficult, since this requires accurate knowledge of the line impedance. To overcome the aforementioned problems, an alternative closed-loop flux-charge-model current-limiting algorithm is proposed for controlling the series inverter to insert only a virtual inductance L_0 along the distribution feeder. Without a resistive component, satisfactory transient damping of the flux-charge algorithm is achieved solely through the appropriate tuning of the feedback controller gains.

Conceptually, the flux-charge algorithm is an extension of the existing flux-model control reported in [56], [57]. Therefore, to assist in conceptual understanding, this section first presents an analysis of flux-model control to highlight its performance merits and shortcomings, before proceeding to present the development and analysis of the flux-charge control to show how it achieves improved performance and stability, as compared to its precedent. (Note that a “sag detection block”, as indicated in Figure 5.2 for the RL algorithm, is also needed for the flux-charge control but is not explicitly shown in figures used in this section for classical control analysis).

5.4.1 Analysis of flux-model control

For flux-model control (see Figure 5.4), the feedback variable used is the inverter terminal flux, defined as $\Phi = \int V_C dt$, and its reference is calculated as $\Phi_{ref} = -L_0 i_{Line}$, where V_C and i_{Line} represent the filter capacitor voltage and inverter output current (equal to the line current if a 1:1 series transformer is used) of the series inverter. (Note from the reference flux expression that a negative sign is intentionally added to account for the representation of i_{Line} as flowing out of the series inverter). Subtracting the flux variable

from its reference then gives the flux error, which is subsequently fed to the flux regulator and PWM modulator represented as $k_{inv} = \frac{2}{V_{dc}}$ in Figure 5.4.

For a second-order LC filtered inverter, the flux-model control cannot damp out the resonant peak of the LC filter, as can be shown by analyzing Figure 5.4 using the MATLAB single-input-single-output (SISO) control system design tool. To match the custom control structure needed by the design tool, Figure 5.4 is simplified to the equivalent form in Figure 5.5, whose root locus and open-loop frequency response (bode) plots without considering the transfer function of the flux regulator are drawn in Figure 5.6 using the system parameters listed in Table 5.1. On the root locus plot, two poles, introduced by the passive LC filter, are observed to be close to the imaginary axis (or directly on the imaginary axis if the resistance of the filter inductor is ignored), which can cause the system to resonate when excited at the natural frequency of the two poles. This resonant condition is also reflected on the frequency response plot, where a resonant peak in magnitude and a sharp crossover of phase are observed at the natural frequency of the poles. The scenario is worsened when the controller gain is increased, which according to Figure 5.6, causes the two poles to move into the right half-plane, making the system unstable. This instability of the flux-model control cannot be readily solved by designing a simple lead-lag flux regulator to enhance the model stability margin and bandwidth. The existing flux-model control is therefore not suitable for controlling a LC filtered inverter.

Figure 5.4. Per-phase control block representation of flux-model control.

Figure 5.5. Simplified per-phase control block representation of flux-model control.

Figure 5.6. Root locus and open-loop bode plots of flux-model control.

5.4.2 Development and analysis of flux-charge-model control

The instability problem of the flux-model control has previously been addressed in [57], where a predictive flux-model control is presented. That predictive algorithm is highly sensitive to system parameter variations, which is a common feature for most predictive schemes, and therefore an alternative robust flux-charge-model control, with an outer flux-model and an inner charge-model as shown in Figure 5.7, is proposed here for controlling the series inverter as a virtual inductance. The outer flux-model functions as described in Section 5.4.1 and outputs a reference charge signal Q_{ref} . By duality, the charge control variable is defined as $Q = \int i_c dt = C_f V_C$, where i_c and C_f are the current

and capacitance of the filter capacitor of the series inverter. Clearly, this expression reveals that the Q variable can be calculated by simply multiplying C_f and V_c (V_c is readily accessible since it is usually measured for voltage regulation purposes) without requiring additional current sensor for measuring i_c and mathematical integration. After subtracting the calculated charge variable from its reference Q_{ref} , the obtained charge error is fed to the inner charge regulator, whose output is finally passed to a PWM modulator (represented by $k_{inv} = 2/V_{dc}$) for driving the physical inverter.

Figure 5. 7. Control block representation of flux-charge-model algorithm.

Conceptually, the proposed flux-charge-model can be derived from the multi-loop voltage-current control commonly used for the voltage regulation of AC power supplies and power quality conditioners. This development is illustrated in Figure 5.8, where Figure 5.8(a) shows an outer filter capacitor voltage and an inner filter capacitor current control loop. For improved tracking performance, the outer voltage loop uses a

P+resonant compensator [51], expressed mathematically as $G_{Flux}(s) = 2k_p + \frac{2k_i s}{s^2 + \omega_0^2}$,

where k_p and k_i are gain constants, and ω_0 is the compensator resonant frequency set at 50Hz for this work. As analyzed in Chapter 4, the P+resonant compensator introduces infinite gains at the positive and negative resonant frequency ω_0 to force the positive- and negative-sequence input errors to zero, and can conveniently be implemented in the stationary α - β frame with minimum computational requirements [51], [52]. The inner current loop uses only proportional controller kT_d since it does not influence the tracking accuracy of the outer voltage loop. It also uses the filter capacitor current as the feedback control variable, rather than the filter inductor current, because of its implementation benefits mentioned above when calculating Q_{ref} .

Without modifying the voltage regulation performance, intermediate derivative ‘ s ’ and integral ‘ $1/s$ ’ terms can be added to the forward control path of the multi-loop voltage-current control, as demonstrated in Figure 5.8(a). The integral “ $1/s$ ” term can be shifted backwards along the control path to give the control structure in Figure 5.8(b), where the control blocks in the shaded region give details of the flux-charge-model in Figure 5.7. As seen, the outer flux regulator is implemented using a P+resonant compensator $G_{Flux}(s)$, while the inner charge regulator is implemented using a derivative compensator. In practice, the inner derivative charge regulator is approximated as $kT_d s \approx \frac{kT_d s}{1 + (T_d s/N)}$, where the added pole is used for limiting the regulator gain to Nk at high frequencies to prevent noise amplification.

Figure 5. 8. Modification of (a) multi-loop voltage-current control to give (b) flux-charge-model control.

To verify the stability of the derived flux-charge-model, a detailed control design example is presented next, beginning with an analysis of the inner charge loop, whose open-loop transfer function is given as:

$$G_{Qol} = \frac{kT_d C_f s}{(C_f L_f s^2 + C_f R_f s + 1)(1 + (T_d s/N))} \quad (5.4)$$

The closed-loop bode plot of (5.4), with $kT_d = 1000$, $T_d/N = 0.00002$ and using system parameters listed in Table 5.1, is shown in Figure 5.9, which shows a band-pass response and a near unity gain at the fundamental frequency. As anticipated, these characteristics are similar to those of the inner capacitor current loop of the multi-loop voltage-current control (example bode plot for the inner capacitor current loop can be found in Figure 3.4, Chapter 3) since the flux-charge control algorithm is derived directly from the multi-loop voltage-current control by simply rearranging intermediate 's' and '1/s' terms without affecting the control performance (see Figure 5.8).

Figure 5.9. Closed-loop bode plot of inner charge-model.

Once the inner charge-model is designed, the response of the outer flux-model is analyzed. With the flux regulator implemented using the P+resonant compensator, the open-loop transfer function of the flux-charge-model is given as:

$$G_{\Phi_{ol}} = \frac{2k_p kT_d s^2 + 2k_i kT_d s + 2k_p kT_d \omega_0^2}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}$$

$$a_5 = \frac{T_d}{N} C_f L_f; \quad a_4 = \frac{T_d}{N} C_f R_f + C_f L_f; \quad a_3 = \frac{T_d}{N} + C_f R_f + kT_d C_f + \frac{T_d}{N} C_f L_f \omega_0^2$$

$$a_2 = \frac{T_d}{N} C_f R_f \omega_0^2 + C_f L_f \omega_0^2 + 1; \quad a_1 = \omega_0^2 \left(\frac{T_d}{N} + C_f R_f + kT_d C_f \right); \quad a_0 = \omega_0^2$$
(5.5)

The open- and closed-loop bode plots of (5.5) are plotted in Figures 5.10 and 5.11 respectively with $2k_p = 0.08$, $2k_i = 160$, and $\omega_0 = 314 \text{ rad/sec}$. The open-loop response shows an infinite gain at the fundamental frequency, which ensures zero steady-state error, while the closed-loop response shows the system exhibiting good performance at the fundamental frequency with effective high frequency noise attenuation. These performance features are again similar to those exhibited by the multi-loop voltage-current control, as anticipated.

Figure 5. 10. Open-loop bode plot of flux-charge-model.

Figure 5. 11. Closed-loop bode plot of flux-charge-model.

5.4.3 Analysis of worst case condition

The same worst case analysis (largest $\vec{\Delta V}$ in Figure 5.3(b)) presented in Section 5.3.3 for the RL feedforward algorithm can equally be applied to the flux-charge-model control for selecting an appropriate value for L_0 . Referring to the phasor diagram in Figure 5.5(b) and using the same assumptions as in Section 5.3.3, the largest magnitude of $\vec{\Delta V}$ is again calculated as $|\vec{\Delta V}| = 0.78E$ and the required inductance L_0 can be calculated using:

$$L_o = \frac{1}{\omega} \sqrt{\frac{|\vec{\Delta V}|^2}{I_T^2} - R_{line}^2} - L_{line} \quad (5.6)$$

where the current threshold I_T , system angular frequency ω and line parameters $\{R_{Line}, L_{Line}\}$ are known parameters. The only difference here is that the optimal R/L impedance ratio formulated in Section 5.3.2 is not used for the flux-charge control algorithm since it is designed to insert only a finite virtual inductance and zero resistance.

5.5 Simulation Results

Simulations using MATLAB/SIMULINK have been conducted to test the effectiveness of the two proposed current-limiting algorithms when controlling a series inverter during utility voltage sags. The simulated microgrid closely models the implemented laboratory prototype shown in Figure 5.1 and Figure 4.1 with zero-order-hold blocks added to all feedback variables to emulate the digitally controlled shunt and series interfacing inverters. The system parameters are given in Table 5.1 (similar to Chapter 4, the transformer leakage resistance and inductance are lumped with R_{Line} and L_{Line}). The calculated virtual impedance values using (5.3) and (5.6) for the two algorithms are also listed in Table 5.1.

As an example case for the study of the two current-limiting algorithms, a utility voltage sag profile is programmed, as shown in Figure 5.12(a), where the utility voltages are initially balanced and at $t = 1s$, a sag of $\{ V_{Ga} = 32\angle -44.7^\circ, V_{Gb} = 66.4\angle -170^\circ, V_{Gc} = 54.5\angle 38.6^\circ \}$ is introduced. As described in Section 5.3.3, during the sag, the microgrid voltages are regulated at 90% of their nominal value (see Figure 5.12(b)) to prevent tripping of sensitive loads in the microgrid. With no current-limiting algorithm incorporated, this regulation of microgrid voltages gives rise to large line currents along the distribution feeder connecting the microgrid to the utility (see Figure 5.12(c)). This flow of large currents can be limited below a set threshold of $I_T = 5A$ by using either of the proposed algorithms, as illustrated in the following subsections.

Figure 5. 12. Simulated (a) sag voltages at PCC, (b) sensitive load voltages in the microgrid and (c) line currents when no current-limiting algorithm is incorporated.

5.5.1 RL feedforward algorithm

Using the RL algorithm, the series inverter functions by inserting a virtual RL impedance $\{R_{inj}, L_{inj}\}$ in series with the distribution feeder to immediately limit the line currents. Simulated voltages across and line currents through the series inverter controlled using the RL feedforward algorithm are shown in Figure 5.13(a) and (b) respectively, where the line currents are obviously limited below $I_T = 5A$ by the rapid injection of large compensating voltages by the series inverter. In addition, negligible transient oscillations are observed on these waveforms, which are expected due to the use of resistive damping impedance R_{inj} . R_{inj} however causes the series inverter to absorb active power, which must be re-channeled through the shunt inverter back to the microgrid to prevent a surge in DC link capacitor voltage.

The detailed active and reactive power flows are better illustrated in Figure 5.14(a) and (b) respectively. In the figures, the series inverter is shown to consume zero pre-sag real and reactive power since its designed functionality is to force only positive sequence balanced line currents to flow by injecting only negative sequence series voltages during normal

operating conditions (Chapter 4). Upon sensing the occurrence of a sag at $t = 1$ s, the series inverter would begin to absorb both active and reactive power since it now functions as a RL impedance. This absorption of power by the series inverter is clearly reflected in Figure 5.14 with the active and reactive power values intentionally indicated as negative to account for the representation of i_{Line} as flowing out of the series inverter.

Figure 5. 13. Simulated (a) voltages injected by the series inverter and (b) line currents using the RL feedforward algorithm.

Figure 5. 14. Simulated power supplied by the series inverter: (a) active power and (b) reactive power using the RL feedforward algorithm.

5.5.2 Flux-charge-model algorithm

The flux-charge-model algorithm controls the series inverter to insert only a large virtual inductance L_0 and zero resistance in series with the distribution feeder. Using this algorithm, the voltages across the series inverter and the limiting of line currents below $I_T = 5A$ are shown in Figure 5.15(a) and (b) respectively. These figures also demonstrate the excellent closed-loop damping nature of the flux-charge algorithm even with no virtual resistive component inserted. Without a resistive component, the series inverter now absorbs only reactive power and zero active power, as shown in Figure 5.16(a) and (b) (see Figure 5.14(a) and (b) for comparison with the RL feedforward algorithm).

Figure 5. 15. Simulated (a) voltages injected by the series inverter and (b) line currents using the flux-charge-model algorithm.

Figure 5. 16. Simulated power supplied by the series inverter: (a) active power and (b) reactive power using the flux-charge-model algorithm.

5.6 Experimental Verification

The proposed methods are also tested experimentally using the hardware microgrid prototype (see Figure 5.1 and Figure 4.1). System parameters are given in Table 5.1. For the experimental system, a programmable AC source with a parallel-connected RL load is used to represent the utility grid, which is connected to an emulated microgrid through a three-phase back-to-back SCR isolation switch. The microgrid consists of a shunt IGBT inverter, a series IGBT inverter with an injection transformer and a RL load. Both inverters are digitally controlled using a dSPACE DS1103 controller card.

For the experimental studies, the sag voltages are programmed to start at $t = 1.2s$ with $\{ V_{Ga} = 32\angle -44.7^\circ, V_{Gb} = 66.4\angle -170^\circ, V_{Gc} = 54.5\angle 38.6^\circ \}$, similar to those used in simulation. Under this programmed sag condition, the performances of the proposed current-limiting algorithms are described as follows.

5.6.1 RL feedforward algorithm

The experimental results obtained using the RL feedforward algorithm, are depicted in Figures 5.17 and 5.18. These figures show the limiting of line currents below 5A in Figure 5.17(b), the absorption of finite active power in Figure 5.18(a) and the effective damping of transient oscillations in all figures. These performances clearly demonstrate the effectiveness of the RL algorithm. A note here is that the less oscillatory experimental power waveforms in Figure 5.18, as compared to their counterparts in Figure 5.14, are obtained due to the lesser experimental sample points captured to maintain a tradeoff between file size and accuracy.

Figure 5. 17. Experimental (a) voltages injected by the series inverter and (b) line currents using the RL feedforward algorithm.

Figure 5. 18. Experimental power supplied by the series inverter: (a) active power and (b) reactive power using the RL feedforward algorithm.

5.6.2 Flux-charge-model algorithm

Figures 5.19 and 5.20 show the corresponding experimental results obtained using the flux-charge-model control. These figures again show the effective and well-damped limiting of line currents with the only performance difference (as compared with the RL feedforward method) being the absorption of (nearly) zero active power by the series inverter. Other observations noted when comparing Figure 5.16 (simulated) and Figure 5.20 (experimental) are the slight active power absorption by the experimental series inverter due to the presence of a small voltage across the filter capacitor before the sag. (In this experiment, the series inverter is in passive mode with modulation signal kept at zero when no sag is detected, which allows the line current flow into inverter filter circuit and thus results in a small voltage drop on filter capacitor as seen in Figure 5.19(a). This is in contrast with the RL feedforward experiment, where the series inverter is actively controlled all the time for compensating possible unbalance utility voltage, resulting in zero power generation when there is no sag.). The slight active power generation after the sag can be attributed to the small steady state phase error between the reference flux and flux feedback (integration of the filter capacitor voltage) which results in a slight deviation from the ideal inductor behavior. Finally, the presence of less oscillatory experimental power waveforms, which again are due to the lesser experimental sample

points captured to maintain a tradeoff between file size and accuracy, can be noticed in Figure 5.20.

Figure 5. 19. Experimental (a) voltages injected by the series inverter and (b) line currents using the flux-charge-model algorithm.

Figure 5. 20. Experimental power supplied by the series inverter: (a) active power and (b) reactive power using the flux-charge-model algorithm.

Table 5.1. System parameters for simulation and experiment.

Parameter	Value
Nominal line-to-line grid voltage	120V
Nominal power	1kVA
Frequency	50Hz
DC supply voltage	250V
Switching frequency for both inverters	10kHz
Series inverter filter capacitance	10 μ F (0.05 pu)
Series inverter filter inductance	3.9mH (0.08 pu)
Series transformer turns ratio	1:1
RL feedforward impedance $\{ R_{inj}, L_{inj} \}$	7.8 Ω (0.52 pu), 26mH (0.55 pu)
Flux-charge-model inductance $\{ L_o \}$	38mH (0.8 pu)
Shunt inverter filter capacitance	30 μ F (0.14 pu)
Shunt inverter filter inductance	5mH (0.11 pu)
Line resistance R_{Line}	3 Ω (0.2 pu)
Line inductance L_{Line}	10mH (0.21 pu)
Sensitive load in the microgrid	120W, 90Var

Table 5.2. Summarized performance features of proposed current-limiting algorithms.

	RL Algorithm	Flux-Charge Algorithm
Inserted impedance type	RL	L
Operating frame	Stationary α - β or synchronous d - q	Stationary a - b - c and α - β
Control principle	Feedforward	Multi-loop feedback
Damping principle	Insertion of virtual R	Closed-loop gain tuning
Sensed control variable(s)	i_{Line}	V_C & i_{Line}
Active power absorption	Non-zero	Zero
Optimal R/L ratio	$R_{inj} / L_{inj} = R_{Line} / L_{Line}$	—
Worst-case impedance	Equation (5.3)	Equation (5.6)

5.7 Discussion

This chapter presents the RL feedforward and flux-charge-model feedback algorithms for protecting utility-interfaced microgrids from large line currents during utility voltage sags. The RL algorithm functions by controlling a series inverter, connected between the microgrid and utility, to insert a large virtual RL impedance along the distribution feeder to limit the line currents and damp transient oscillations with a non-zero active power circulating through the series (and shunt) inverter. In contrast, the alternative flux-charge algorithm inserts only a virtual inductive impedance with zero active power absorption and relies on its closed-loop control tuning to damp transient oscillations. Other performance features of the two algorithms are summarized in Table 5.2. Furthermore, both algorithms have been tested to function well in simulation and experimentally using an emulated laboratory microgrid system. Lastly, it is worth to comment that with the fault current limiting function, the proposed dual-inverter grid-interfacing compensator has a weakness in that the compensator requires increased inverter ratings as mentioned in Section 4.2 of Chapter 4, which leads to higher cost.

Chapter 6

Robust Control Scheme for a Microgrid with PFC Capacitor Connected

6.1 Introduction

A microgrid, being a larger entity, possesses a larger power capacity and more control flexibilities to fulfill system reliability and power quality requirements, in addition to all inherited advantages of a single DG system. While being a larger system also means that the microgrid can easily be disturbed by numerous power devices connected within its vicinity. In particular, the switching of power factor correction (PFC) capacitors, widely used for improving system efficiency, would create problems and affect proper microgrid operations. This chapter investigates the performance of a microgrid with PFC capacitors connected. The impacts of switching of a PFC capacitor to microgrid are studied and robust control schemes are proposed for microgrid.

Most loads used in industry are inductive. The inductive loads absorb reactive power, causing the power factor to be less than unity. The poor power factor will result in inefficiency of distribution power system, poor regulation of voltage etc. For the improvement of power factor, PFC capacitors are widely used to provide reactive power and correct the power factor, due to their low installation cost and larger capacity. Typically, capacitor banks are connected in parallel with the inductive loads. The size of capacitors in operation depends on the compensation demand of the load.

One drawback of using the PFC capacitors is that they introduce oscillatory transients when switched. Some capacitors are energized all the time as a fixed bank, while others are switched according to load level. Common power quality problems of the transient resonance caused by switching a PFC capacitor are adjustable speed drive (ASD) trippings and malfunctioning of other electrically controlled load equipment [14].

There are plenty of reasons for PFC applications in the customer side, such as reduced electric utility bill, reduced losses and therefore, heating in lines and transformers, increased voltage at the load and more importantly, elimination of utility power factor penalties [14]. It is therefore necessary to consider the scenario of PFC capacitor application in a microgrid, where the switching of capacitor can cause more complex phenomena than the traditional drawbacks. For example, switching of PFC capacitor within a microgrid can cause system parameter variations, and hence performance degradation of the designed DG controller. The presence of PFC capacitors would also result in high resonant voltages and currents, which could damage semiconductor devices and other power equipment or jeopardize the control scheme leading to malfunctioning of the microgrid.

To address aforementioned complications, this chapter first conducts an in-depth investigation of the scenario of a microgrid with PFC capacitor connected. It reveals that effective shunt filter capacitance can be changed by the switching of PFC capacitors connected to a local load in the microgrid (Load1 in Figure 6.1). While when the PFC capacitor is connected to the remote load (Load2 at Point of Common Coupling (PCC) in Figure 6.1) which is connected to the DG through a transmission line, resonance can occur between the line inductor and the PFC capacitor when the microgrid operates in islanding mode. An integrated control algorithm is then proposed, comprising of a H_∞ voltage controller, an inner filter inductor current feedback controller and a virtual-resistance compensator, for operating the microgrid with reduced parameter sensitivity and improved damping performance. For the control scheme development, the chapter begins by designing a H_∞ voltage controller for stable control of the DG interfacing voltage-source inverter (VSI) even when its effective filter capacitance is changed by the switching of a PFC capacitor. By properly selecting the weighting functions, the synthesized H_∞ controller would have high gains at the vicinity of the line frequency, similar to the P+resonant controller (discussed in Chapters 4 and 5), and thus possess nearly zero steady-state error with its degree of robustness explicitly specified. The chapter then evaluates filter inductor and filter capacitor inner current control possibilities to show that filter inductor current control is more effective in damping the resonant caused by the switching of PFC capacitor in microgrid islanding operation mode.

Figure 6.1. Microgrid system with a single DG.

For DG system using dual-inverter microgrid conditioner with an additional series inverter as discussed in Chapters 4 and 5, a virtual-resistance compensator for controlling the series inverter to further dampen the system resonance is presented in this chapter. Similar to [58] and [59], the series inverter is controlled to resist only harmonic components, by acting as a virtual harmonic resistance, without affecting the fundamental power flow. Lastly, the integrated controller developed in this chapter has been tested in MATLAB/SIMULINK simulation and experimentally using an emulated laboratory microgrid system.

6.2 Modeling and Analysis of a Microgrid System with PFC Capacitor Connected

The microgrid system with a single DG is shown in Figure 6.1. As shown, the DG source is interfaced to the utility grid using a VSI, whose functionalities, as discussed in Chapter 3, are to regulate load voltages and dispatch power in the microgrid, share the power demand changes with other paralleled DG systems in the microgrid when the microgrid islands, and to synchronize the microgrid with the utility for smooth connection of them. There can be two possible locations for the loads to be connected in the microgrid as shown in Figure 6.1. Load1 is the local load of a DG system, and the DG system provides local power and voltage support for it. Load2 at the PCC is separated from the DG system by a distribution line. Usually Load2 is supplied by both the microgrid and the utility in grid-connected mode of the microgrid operation and solely by the microgrid when the microgrid islands.

The PFC capacitor can be connected in parallel with Load1 or Load2 in the microgrid. First consider it is connected in parallel with Load1. In this case, the PFC capacitor is also in parallel with the filter capacitor of the interfacing VSI, causing an increase of effective capacitance of VSI filter capacitor. Note that the increase of the filter capacitance will reduce the LC cutoff frequency and subsequently affect the performance of VSI controller, which is tuned based on original parameters. Therefore attention must be paid in the inverter controller design with regard to filter capacitance variations.

A second possible location for the PFC capacitor to be installed is in parallel with Load2 at the PCC. In this condition, a resonant circuit can be formed by the PFC capacitor and the line inductance. But this potential resonance condition in the microgrid needs to be studied in the two modes of the microgrid operation, namely, grid-connected mode and islanding mode, where the resonant circuit behaves differently.

Figure 6.2. Equivalent circuit of the resonant microgrid system: (a) grid-connected mode (b) islanding mode.

6.2.1 Grid-connected mode

The equivalent circuits of the microgrid system with a PFC capacitor connected with Load2 are illustrated in Figure 6.2, where Load1 and Load2 are represented as current sources, and the DG system output voltage (filtered inverter output voltage) is treated as a voltage source. Figure 6.2(a) shows the grid-connected mode, where the utility voltage at PCC would be represented as a voltage source too, since it is stiff enough compared to the voltage in the microgrid. As a result, the line current is completely determined by the difference of the DG system output voltage and the PCC voltage. Therefore in the grid-

connected mode of operation, the resonance between the PFC capacitor and the line impedance is highly suppressed.

6.2.2 Islanding mode

Figure 6.2(b) illustrates the equivalent circuit for the microgrid system in islanding mode. In this equivalent circuit, observed from Load2 side the PFC capacitor and the line inductance form a parallel resonant circuit. Thus harmonic line currents in the vicinity of resonant frequency drawn by Load2 can be amplified excessively. Looking from the DG system side, the PFC capacitor and the line inductance represent a series resonant circuit, and harmonic voltages injected by the DG system in the range of resonant frequency can cause amplified resonant voltages on Load2 and the PFC capacitor, which could in turn result in inadmissible high resonant line currents.

According to the equivalent circuit in Figure 6.2(b), the transfer functions between load current i_{load2} and the line current i_{line} , and between DG system voltage and the Load2 voltage can be derived. It turns out that these two transfer functions have the same form G_{res} as in (6.1):

$$G_{res} = \frac{i_{line}}{i_{load2}} = \frac{V_{pf}}{V_d} = \frac{1}{L_{line} C_{pf} s^2 + R_{line} C_{pf} s + 1} \quad (6.1)$$

For G_{res} , the peak response at resonant frequency mainly depends on the ratio of $R_{line} \cdot \omega_0 L_{line}$ in the line impedance. A larger line resistance would damp out the resonance caused by the line inductance and the PFC capacitor more quickly. In a microgrid system at the distribution side, the ratio of $R_{line} \cdot \omega_0 L_{line}$ would be nearly 1:1. Even so, the resonance can be serious as will be discussed in Section 6.3 (also refer to Figure 6.11).

Once a disturbance with frequency near resonance value occurs, the resonance would be excited. The harmonic frequency disturbance can be initiated by a disturbance in Load2 or DG system output voltage such as when the microgrid islands or the dispatched power

for the DG system changes resulting in a sudden change of reference voltage for the DG system. These different sources of resonance have equally damaging effect on the microgrid as seen from (6.1). Note that although the islanding operation for a microgrid might last for an only short period, the resonance can cause inadmissible high line currents or load voltages and could further disrupt the control and proper operation of each DG system.

6.3 Analysis and Design of the VSI Control

As mentioned, when the PFC capacitor connected to Load1, the effective filter capacitance for the VSI is changed to the sum of the original filter capacitance and the capacitance of PFC capacitor. To mitigate the effects of effective filter capacitance variation, a H_∞ controller is proposed for the VSI voltage regulation. By proper selection of the weighting functions, the H_∞ controller would have similar characteristic as the P+resonant controller (discussed in Chapter 4) with significant gain at the line frequency and would thus have almost zero steady state error for the fundamental components regulation, while with its robustness explicitly specified. An inner current feedback loop is also employed to improve transient performance. But a special attention should be paid to the feedback current variables, since different feedback variables (filter capacitor currents or filter inductor currents) for the current loop behaves quite differently during resonance situation caused by the switching of PFC capacitor connected to Load2. Detailed analysis will be given in the following subsections.

Figure 6.3. Standard H_∞ configuration.

6.3.1 H_∞ controller for the voltage loop

The form of a standard configuration for H_∞ control synthesis is shown in Figure 6.3, where z , y , w and u are the controlled output, the measured output, the exogenous input and the control input respectively; G_N is the nominal plant and $K(s)$ is the controller. W_1 , W_3 and W_2 are the weighting functions for tracking error performance, robust performance and the weight on the controller transfer function respectively. The H_∞ controller synthesis is conducted by the singular value loop-shaping using mixed sensitivity approach, such that the H_∞ norm of the transfer function from w to z is less than one. This can be expressed as:

$$\left\| \begin{array}{c} W_1 S \\ W_3 T \end{array} \right\|_\infty < 1 \quad (6.2)$$

or equivalently

$$\|T_{wz}\|_\infty < 1 \quad (6.3)$$

where $T(s) = \frac{G_N(s)K(s)}{1 + G_N(s)K(s)}$ is the complementary sensitivity transfer function,

$S(s) = \frac{1}{1 + G_N(s)K(s)}$ is the sensitivity transfer function. It can be seen from (6.2) or (6.3)

that the mixed sensitivity approach is simply the shaping of $T(s)$ (transfer function from reference to output, or closed loop transfer function) and $S(s)$ (transfer function from reference to error), by properly selecting their respective weighting functions W_1 and W_3 . A small value 0.1 is assigned to W_2 , to ensure the D_{12} matrix of the augmented plant is full rank as required by the MATLAB *augtf* and *hinf* function [60]. To ensure the existence of a H_∞ controller, the weighting functions cannot be chosen arbitrarily. A basic criterion is the 0 dB crossover frequency of W_1 must be sufficiently below the 0 dB crossover frequency of $1/W_3$.

6.3.1.1 Weighting function for robust performance

The nominal plant (with current loop closed) can be described as:

$$G_N = \frac{\frac{V_{dc}}{2} k_C}{C_f L_f s^2 + C_f (R_f + \frac{V_{dc}}{2} k_C) s + 1} \quad (6.4)$$

where k_C is the proportional controller for the current loop. For the filter capacitance uncertainty, a tolerance of parameter variation from 100% to 500% of the filter capacitance is applied for the H_∞ controller design. This parameter uncertainty can be transformed to multiplicative output uncertainty [61], and the resulting relative plant uncertainty with respect to the nominal plant is expressed as in (6.5):

$$\Delta(s) = \sigma\left(\frac{G_P - G_N}{G_N}\right) \quad (6.5)$$

where $\Delta(s)$ is the plant uncertainty, G_P is the disturbed plant and $\sigma(H)$ stands for the singular values of transfer function H .

For the robustness measure, the requirement of $\|W_3 T\|_\infty < 1$, must be satisfied. By using filter capacitor as 500% of its nominal value, the worst case $\Delta(s)$ can be obtained. Finally the weighting function W_3 is determined from the worst case $\Delta(s)$ and is selected to lie just above the worst case uncertainty spectrum. Figure 6.4 shows the worst case plant uncertainty and the weighting function W_3 , where $W_3 = 0.000133s + 0.8$.

Figure 6.4. Singular values of $\Delta(s)$ and W_3 .

6.3.1.2 Weighting function for tracking error performance

The tracking error performance can be expressed in terms of H_∞ constrain as $\|W_1 S\|_\infty < 1$. For proper shaping of $S(s)$ (which is from the reference to error) and therefore achieving satisfactory sinusoidal reference tracking performance, the weighting function W_1 should be carefully determined. Authors in [62] proposed a guideline for the tracking of sinusoidal command by using phasors and straight line approximation of magnitude response. Unfortunately, the controller derived by this method will have relatively high gains to achieve small steady state error over the full bandwidth, and might be sensitive to system resonance caused by the switching of PFC capacitor.

Since the reference command of the inverter is a sinusoid at line frequency, a better choice would be to use a controller that exhibits high gains at only line frequency while providing smaller gains at the other frequencies similar to the P+resonant controller discussed in Chapter 4. Small tracking error at the line frequency can be obtained by properly shaping $S(s)$ to have very small gain at the line frequency. This can be achieved by using a standard second order weighting function $S(s)$ similar to [63]. This weighting function is shown in (6.6):

$$W_1 = \frac{k_A \omega_0^2}{s^2 + 2\zeta \omega_0 s + \omega_0^2} \quad (6.6)$$

where natural frequency ω_0 is selected as the line frequency. The term k_A in the numerator gives a freedom for adjusting the tracking error over the whole frequency range and the damping ratio ζ provide another freedom for special regulation of the tracking error at the line frequency ω_0 .

Since the resulting sensitivity function $S(s)$ is shaped in frequency according to the profile specified by $1/W_1$, as shown in Figure 6.5(a) and (b), a smaller ζ will give a larger peak response of W_1 at the natural frequency and thus guarantee smaller steady state error at

the line frequency. When $\zeta \rightarrow 0$, the resulting H_∞ controller would look like an ideal P+resonant controller, which has theoretically infinite gain and zero steady state error at fundamental frequency. Also seen from Figure 6.5 is the width of notches of W_I and resulting $S(s)$ is not related to ζ , therefore ζ can be made as small as possible for better error tracking although a too small ζ is almost not possible due to finite precision for digital system implementation or component tolerances in analog system. The tracking error at ω_0 as well as the other frequencies can also be regulated by tuning k_A in (6.6). Note that by increasing k_A the overall gain of W_I on the frequency frame can be increased, which has similar effect as broadening the notch band of W_I around the line frequency and hence making the system less sensitive to operating frequency variations. In this work $k_A=1$ and $\zeta=0.01$ are used.

Figure 6. 5. Singular values of weighting functions of : (a) W_I and (b) $S(s)$.

6.3.1.3 Mixed sensitivity H_∞ controller synthesis

Having defined necessary weighting functions, the next step is to conduct mixed sensitivity optimization control design to synthesize $K(s)$ such that the H_∞ norm of the transfer functions from w to z is less than one, as expressed in (6.2) and (6.3). By using MATLAB *hinf* function, the resulting controller $K(s)$ would have the same order as the plant model including the augmentation with the weights. The H_∞ controller is then reduced to a third-order controller as shown in (6.7), with bode plot drawn in Figure 6.6.

$$K(s) = \frac{0.02398s^3 + 1.222 \cdot 10^4 s^2 + 1.024 \cdot 10^7 s + 5.629 \cdot 10^8}{s^3 + 1.145 \cdot 10^5 s^2 + 8.228 \cdot 10^5 s + 1.13 \cdot 10^{10}} \quad (6.7)$$

As expected, the designed H_∞ controller has high gains at the vicinity of the line frequency. Therefore, robust performance with nearly zero steady state error can be achieved. (Plotting the bode plot at negative frequency reveals that the designed H_∞ controller has significant gains at both ± 50 Hz to ensure nearly zero steady state errors for any unbalanced voltage regulation, similar to the P+resonant controller, which will be further discussed in Chapter 7.) Compared to the P+resonant controller, the proposed H_∞ controller can explicitly specify the degree of robustness in face of filter capacitance variations due to the switching of PFC capacitor, and therefore is found to be more suitable for this work.

Finally the singular values of weighting functions $1/W_1$, $1/W_3$ and the resulting sensitivity function $S(s)$ and the complementary sensitivity function $T(s)$ are shown in Figure 6.7. It can be seen that the weighting functions W_1 and W_3 properly shape the systems steady state error and reference-output transfer functions to guarantee its good performance of both error tracking and robustness.

Figure 6.6. Bode plot of designed H_∞ controller.

Figure 6.7. Singular values of $1/W_1$, $1/W_3$, $S(s)$ and $T(s)$.

6.3.2 Inner current loop

To achieve better transient and robustness, an inner current feedback loop is also adopted. Filter capacitor current feedback is usually used for better rejection of load current disturbance when an inverter (with filter) is directly connected to a load [64] [65]. In addition, capacitor current can be easily estimated using the capacitor voltage (inverter output voltage), and thus it would save extra sensors. While for the purpose of damping the LC resonance caused by the switching of PFC capacitor connected to Load2 in this chapter, filter inductor current feedback is found to be more effective, as discussed later.

Figure 6.8 shows the schematic of PFC capacitor connected system together with the controllers for the inverter. To simplify the analysis, two proportional controllers are used for the current and voltage control loops. Also Load1 is not considered here due to its limited effect on the resonance phenomena. The block diagram in Figure 6.8 can be equivalently simplified as in Figure 6.9, where:

$$G_1 = \frac{\frac{V_{dc}}{2} k_C k_V}{C_f L_f s^2 + C_f (R_f + \frac{V_{dc}}{2} k_C) s + (1 + \frac{V_{dc}}{2} k_C k_V)}; \quad G_2 = \frac{L_f s + R_f + \frac{V_{dc}}{2} k_C}{\frac{V_{dc}}{2} k_C k_V};$$

$$G_2' = \frac{L_f s + R_f}{\frac{V_{dc}}{2} k_C k_V}; \quad G_3 = \frac{1}{L_{line} s + R_{line}}; \quad G_4 = \frac{L_{load} s + R_{load}}{C_{pf} L_{load} s^2 + C_{pf} R_{load} s + 1}.$$

Note that G_2 and G_2' represent function blocks for cases of filter inductor and capacitor current feedback respectively.

Figure 6.8. PFC capacitor connected system and the double-loop control of the shunt inverter.

Figure 6.9. Equivalent simplified schematic of Figure 6.8.

It can be observed that the only difference between filter inductor and capacitor current feedbacks is the presence of an additional term of $\frac{V_{dc}}{2} k_C$ in the numerator of G_2 . As shown in Figure 6.9, the line current has a negative feedback loop $-G_1 G_2 G_3$ or $-G_1 G_2' G_3$, which would in turn compensate the resonance that would occur between the line (G_3) and the PFC capacitor connected load (G_4). Therefore with a larger feedback gain, the filter inductor current feedback would compensate the line current resonance more effectively ensuring rapid attenuation of the system resonance.

The block diagram of Figure 6.9 would also explain why capacitor current feedback is more robust to the load disturbance: in this case, the load current (treated as disturbance) will pass through $G_1 G_2$ or $G_1 G_2'$ and affect the load voltage. It is clear that smaller gain of $G_1 G_2'$ with capacitor current feedback ensures more stable load voltage under the load current disturbance.

With consideration of the dynamics of the VSI control model, the resonance transfer function in (6.1) can be re-written as $\frac{V_{pf}}{V_{ref}}$ in (6.8), whose root locus plot and bode magnitude plot are shown in Figures 6.10 and 6.11 respectively.

$$\frac{V_{pf}}{V_{ref}} = \frac{k_C k_V (L_{load} s + R_{load}) V_{dc} / 2}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (6.8)$$

where:

$$a_5 = C_{pf} C_f L_f L_{line} L_{load}$$

$$a_4 = C_{pf} C_f L_f L_{line} R_{load} + C_{pf} C_f L_f L_{load} R_{line} + C_{pf} C_f L_{line} L_{load} (R_f + \frac{V_{dc}}{2} k_C)$$

$$a_3 = C_f L_f L_{line} + C_f L_f L_{load} + C_{pf} L_f L_{load} + C_{pf} L_{line} L_{load} (1 + \frac{V_{dc}}{2} k_C k_V) + C_{pf} C_f L_f R_{line} R_{load} \\ + C_{pf} C_f L_{line} R_{load} (R_f + \frac{V_{dc}}{2} k_C) + C_{pf} C_f L_{load} R_{line} (R_f + \frac{V_{dc}}{2} k_C)$$

$$a_2 = C_{pf} C_f R_{line} R_{load} (R_f + \frac{V_{dc}}{2} k_C) + C_f L_f R_{line} + C_f L_f R_{load} + C_f L_{line} (R_f + \frac{V_{dc}}{2} k_C) \\ + C_f L_{load} (R_f + \frac{V_{dc}}{2} k_C) + C_{pf} L_f R_{load} + C_{pf} L_{line} R_{load} (1 + \frac{V_{dc}}{2} k_C k_V) + C_{pf} L_{load} R_{line} (1 + \frac{V_{dc}}{2} k_C k_V) \\ + C_{pf} L_{load} (R_f + \frac{V_{dc}}{2} k_C)$$

$$a_1 = L_f + L_{line} (1 + \frac{V_{dc}}{2} k_C k_V) + L_{load} (1 + \frac{V_{dc}}{2} k_C k_V) + C_f R_{line} (R_f + \frac{V_{dc}}{2} k_C) \\ + C_f R_{load} (R_f + \frac{V_{dc}}{2} k_C) + C_{pf} R_{line} R_{load} (1 + \frac{V_{dc}}{2} k_C k_V) + C_{pf} R_{load} (R_f + \frac{V_{dc}}{2} k_C)$$

$$a_0 = R_{line} (1 + \frac{V_{dc}}{2} k_C k_V) + R_{load} (1 + \frac{V_{dc}}{2} k_C k_V) + R_f + \frac{V_{dc}}{2} k_C$$

It is clear from Figure 6.10 that the transfer functions with inner filter inductor or capacitor current feedback share the same zero location. While for the five poles, two of them are located at positions which are nearly ten times away from the imaginary axis compared to the others, one is on the real axis and is cancelled by the nearby zero. So the dynamics of the transfer function mainly depend on the two conjugate poles near the imaginary axis. For capacitor current feedback, these two poles have damping ratio of 0.0703. The corresponding damping ratio is increased to 0.163 with inductor current feedback. Same effect can also be observed from bode magnitude plot in Figure 6.11, where the resonance is well damped by filter inductor current feedback.

Figure 6.10. Root locus plot of V_{pf}/V_{ref} .

Figure 6.11. Bode magnitude plot of V_{pf}/V_{ref} .

Further analysis also reveals that by using a smaller gain k_V for the voltage loop the resonance damping for both current feedback methods is improved. However a smaller k_V means larger steady state error, therefore the voltage controller should have larger gain at the line frequency with small tracking error while smaller gains at the other frequencies (especially at the resonant frequency) for the better damping of the resonance. Obviously, proposed H_∞ controller would be more suitable for this purpose.

6.4 Further Resonance Attenuation Using Dual-Inverter Microgrid Conditioner

The resonance between the line and the PFC capacitor connected to Load2 can be further damped if the dual-inverter microgrid compensator proposed in Chapter 4 is adopted. As shown in Figure 6.12, two inverters (a shunt and a series) are employed for each DG system in the microgrid and therefore an additional degree of control freedom can be obtained by using a second series-connected VSI along the distribution feeder to balance the line current flow or limit the fault currents as discussed in Chapters 4 and 5. The series VSI can be employed here for further improving the resonance damping.

Figure 6.12. Dual-inverter compensator for the microgrid.

Different topologies and control methods have been proposed in the literature for applying an additional VSI to damp the resonance effect. In [58] a hybrid filter is proposed for active damping of the resonance in power system with PFC equipment, and providing harmonic current compensation at the same time. In [59], the power converter connected in series with the PFC capacitor is controlled to act as a virtual harmonic resistor to damp the resonance and protect the power capacitor. The inverter in [59] can

regenerate the real power consumed by the virtual resistor back to the utility system at the fundamental frequency and guarantee zero real power consumption ideally.

An obvious way to attenuate the microgrid resonance is to insert a resistor in series with the line impedance, which would further increase the $R_{line}:\omega_0 L_{line}$ ratio and damp out the resonance effectively. This series resistance can be obtained by properly controlling the series inverter as a virtual resistor. A consideration here is, although the fundamental component dominates in the microgrid system, under resonant conditions the virtual resistor makes its contribution only at the resonant frequency. Furthermore, by acting as a virtual resistor at all the frequencies, the series inverter will absorb active power corresponds to all the frequencies from the system, which is re-channeled through the shunt inverter back to the microgrid to prevent a surge in voltage across the DC link capacitor. This power circulation will introduce additional power losses on the inverters and filter circuits.

An alternative method is to control the series inverter in such a way that it presents zero resistance at the fundamental frequency but a finite resistance R_i at the harmonic frequencies similar to [58] [59]. Therefore the series inverter does not play any role at the fundamental frequency, while at harmonic frequencies it acts as a resistor or a harmonic isolator between the DG source and the load to suppress the resonance.

For control the series inverter to act like a virtual resistor only at the harmonic frequencies, the line current fundamental components must be filtered out first. As shown in Figure 6.13, the extracted harmonic line currents are used to generate the reference voltage for the series inverter. For the voltage control, multiple feedback loops with inner (estimated) filter capacitor current loop and outer filter capacitor voltage loop and an additional reference feedforward loop are used for better dynamic performance. Control structure of the series inverter including the fundamental component filtering, voltage control scheme development and virtual harmonic resistor model analysis will be discussed in the following text.

Figure 6.13. Control scheme of the series inverter.

6.4.1 Retrieval of harmonic line current components

The fundamental component of the line currents is filtered out in the synchronous reference frame. As shown in Figure 6.14, the line currents are first transformed from stationary a-b-c frame to synchronous d-q frame. The synchronous frame currents i_{dq} then contain DC components representing the fundamental line current i_{dqf} and AC components representing the harmonic i_{dqh} . By calculating the mean value of i_{dq} over one fundamental frequency period, all the harmonic components (multiple of 100Hz) as well as any possible measurement DC offset (50Hz) become zero with only fundamental components (DC value) remaining as shown in Figure 6.14, where f_0 represents the fundamental frequency. Subsequently the harmonic line currents are generated by subtracting fundamental components from the line currents ($i_{dqh} = i_{dq} - i_{dqf}$). These synchronous d-q frame harmonic line currents are finally transformed back to stationary a-b-c frame.

Figure 6.14. Retrieval of line currents harmonic components.

MATLAB Control System Toolbox is used to analyze the harmonic current retrieval block with the second order Pade approximation of the transport delay block at $f_0=50$ Hz. The bode plots of the mean value calculation block in synchronous frame i_{dqf}/i_{dq} , and the whole harmonic currents retrieval filter i_{dqf}/i_{dq} can be drawn in Figure 6.15, with the transfer functions given in (6.9) and (6.10) respectively:

$$\frac{i_{dqf}}{i_{dq}} = G_{lp} = \frac{1 - e^{-s/f_0}}{s} f_0 = \frac{30000}{s^2 + 300s + 30000} \quad (6.9)$$

$$\frac{i_{abch}}{i_{abc}} = G_{hp} = 1 - \frac{1 - e^{-s/f_0}}{s} f_0 = \frac{s^2 + 300s}{s^2 + 300s + 30000} \quad (6.10)$$

It can be observed from Figure 6.15 and (6.9) (6.10) that the synchronous frame mean value calculation block is actually a low pass filter (G_{lp}) which allows the fundamental (DC) components to pass through. The harmonic currents retrieval block is a high pass filter (G_{hp}) that filters out the fundamental components of the line currents. The cutoff frequency of i_{dqf}/i_{dq} plot is 12.1 Hz.

Figure 6.15. Bode plots of $G_{lp} = i_{dqf}/i_{dq}$ and $G_{hp} = i_{dqf}/i_{dq}$.

6.4.2 Development and analysis of voltage control

Figure 6.13 shows the control diagram for the series inverter. As shown, the line currents first pass through a high pass filter (Figure 6.14) to generate the harmonic line current components i_h . Multiplying the harmonic line currents with a proportional gain R_i , which

represents the virtual resistance at the harmonic frequency, gives the reference voltages V_{Cref} for the series inverter (the negative sign for i_h is due to the identical terminal locations at each side of the transformer in Figure 6.12).

To improve the voltage control performance, an inner current loop by estimating the capacitor current using the capacitor voltage is added and it can be expressed as $I_C = C_f V_C s$. In practice, the current derivative estimator is approximated as

$C_f s \approx \frac{C_f s}{1 + s/N}$, where the added pole is used for limiting the regulator gain to $C_f N$ at high frequencies to prevent noise amplification.

Two proportional controllers k_{IV} and k_{IC} are employed along the outer voltage and inner current control paths. These proportional controllers can guarantee series inverter's fast response to the reference. Since the reference voltage for the series inverter consists only of harmonic components, proportional controllers are found to be very suitable for this implementation as they can provide equally good control at all the harmonic frequencies. (Note that using multiple P+resonant controllers at selected harmonic frequencies as did in [52, 66, 67 and 82] is also an option which can guarantee very small steady state error for harmonic regulation but with more control effort.)

System damping and stability margin can be improved by properly tuning the gains k_{IV} and k_{IC} . These gains are determined for a given design specification by deriving the transfer function between series inverter filter capacitor voltage V_C and the reference voltage V_{Cref} , which is shown in (6.11):

$$\frac{V_C}{V_{Cref}} = G_{vi} = \frac{\frac{k_{IV}k_{IC} + k_F}{N}s + k_{IV}k_{IC} + k_F}{\frac{C_f L_f}{N}s^3 + C_f(L_f + \frac{R_f}{N})s^2 + (C_f R_f + C_f k_{IC} + \frac{k_{IV}k_{IC} + 1}{N})s + k_{IV}k_{IC} + 1} \quad (6.11)$$

Specifically, the increase of current controller gain k_{IC} tends to increase the damping level, while the increase of voltage gain k_{IV} tends to decrease it. As the feedforward gain k_F is present only in the numerator of the transfer function, it does not contribute to the improvement of system damping and stability margin. However, it can be independently

adjusted to decrease steady state error [65] and increase the response of the voltage control. With consideration of all the above-mentioned factors, the proportional gains for the series inverter voltage control are chosen as $k_{IC}=50$, $k_{IV}=0.18$, $k_F=1$ and $k_{inv}=2/V_{dc}$ (for other system parameters, refer to Table 6.1). Finally bode plot of the voltage control transfer function G_{vl} in (6.11) is shown in Figure 6.16. It is clear from this bode plot that the voltage control scheme has good performance up to the bandwidth of 3.74 kHz and the gain gets rapidly attenuated at high switching frequencies. Also shown in Figure 6.16 is the bode plot of the actual virtual harmonic resistor model with transfer function (6.12), which is a product of series connected high pass filter, the ideal virtual harmonic resistor and the series inverter voltage control model in (6.11).

$$R'_i = \frac{V_C}{-i_{line}} = G_{hp} \cdot R_i \cdot G_{vl} \quad (6.12)$$

As shown in Figure 6.16, the fundamental component is filtered out (in synchronous reference frame), and the actual virtual harmonic resistance is equal to the ideal value ($R_i=10 \Omega$) with the bode magnitude of 20 dB at harmonic frequencies (a very small error might remains due to the finite value of proportional gains of k_{IV} and k_{IC}).

Adding this harmonic resistor model R'_i to the line impedance, bode magnitude plot of the resonance transfer function (6.8) can again be drawn in Figure 6.11, where it can be seen that the high frequency disturbance is attenuated obviously proving the effectiveness of the series virtual harmonic resistor model for the resonance damping.

Figure 6.16. Bode plot of G_{vl} and R'_i .

6.5 Simulation Results

Simulations using MATLAB/SIMULINK have been carried out to test the designed H_∞ controller and the effectiveness of the proposed methods for the resonance attenuation. To emulate the digitally controlled shunt and series interfacing inverters implemented as laboratory prototype, the simulated microgrid uses zero-order-hold blocks of $100\mu\text{s}$ sampling along all feedback variables. The system parameters used are listed in Table 6.1 (the transformer leakage resistance and inductance are lumped together with line impedance R_{line} and L_{line}).

The first simulation run is for testing the performance of the H_∞ controller when PFC capacitor of $70\mu\text{F}$ is connected to Load1. The effective capacitance of the filter capacitor increases from the original $30\mu\text{F}$ to $100\mu\text{F}$. As can be seen from Figure 6.17, the designed H_∞ controller is robust enough for the filter capacitance changes caused by the switching of PFC capacitor. A performance comparison of the P+resonant controller and the designed H_∞ controller is presented in Chapter 7 (with simulated results shown in Figures 7.14 and 7.15). Basically, the change in capacitance modifies the open-loop gain of the voltage controller. Although it has no effect on the P+resonant controller at the fundamental frequency (where controller gain remains as infinity), the controller gains around the LC cutoff frequency would affect the overall performance and may even lead to an unstable closed-loop system due to the lacking of robustness margins for the P+resonant controller. A detailed discussion is provided in Section 7.3 of Chapter 7.

Figure 6.17. Simulated Load1 voltages with capacitor change.

The resonance effect of connecting a PFC capacitor and the proposed damping method is tested in the second simulation. The harmonic disturbance source is chosen to be the DG system output voltages, which have a phase shift (60 degrees), a magnitude drop (phase voltage drops from 98V to 96V) and a frequency drop (from 50 Hz to 48 Hz) simultaneously at $t = 0.1$ s. The control scheme with filter capacitor current feedback is checked first. Figures 6.18 and 6.19 are the Load2 voltages and line currents respectively, where voltages and line currents have oscillations at the resonant frequency around 350 Hz (7th harmonic). These oscillations are finally damped out by the line resistance R_{line} . Even though the resonance shown here is only for a short period, it may cause damaging effects to the system components or affect the control algorithm of the microgrid if the control scheme is not robust enough.

Figures 6.20 and 6.21 show the Load2 voltages and line currents with filter inductor currents feedback. It can be seen that both the peak value and sustenance time for the resonance is reduced obviously, proving that the filter inductor current feedback method is more effective for the resonance damping.

Further attenuation of the resonance by employing the dual-inverter conditioner is shown in Figures 6.22 to 6.24. By using an additional series inverter controlled as a virtual resistor at the harmonic frequencies, the resonance is almost unnoticeable, with both the voltages and currents settle down almost immediately as seen from Figures 6.22 and 6.23. The voltages generated by the series inverter are shown in Figure 6.24. As seen, the series inverter generates harmonic voltages during the transient under the disturbance, while it provides zero voltage at steady state. A relatively long transient shown in Figure 6.24 is caused by the dynamics of high pass filter.

Figure 6.18. Simulated Load2 voltages with filter capacitor currents feedback.

Figure 6.19. Simulated line currents with filter capacitor currents feedback.

Figure 6.20. Simulated Load2 voltages with filter inductor currents feedback.

Figure 6.21. Simulated line currents with filter inductor currents feedback.

Figure 6.22. Simulated Load2 voltages with filter inductor currents feedback and series compensation.

Figure 6.23. Simulated line currents with filter inductor currents feedback and series compensation.

Figure 6. 24. Simulated series voltages generated by the series inverter.

6.6 Experimental Results

To verify the effectiveness of the analysis, the designed controller and proposed damping methods experimentally, a laboratory hardware prototype has been built with the system parameters listed in Table 6.1 (same as those used in simulation). The emulated microgrid consists of a DC source, an IGBT interfacing inverter (or a shunt and a series IGBT inverters with an injection transformer as a dual-inverter microgrid conditioner) and two RL loads (Load1 and Load2 as in Figure 6.1). The inverters are digitally controlled using a dSPACE DS1103 controller card.

Similarly, the first experiment is for testing the proposed H_∞ controller robustness. The capacitance is changed from $30\mu\text{F}$ to $100\mu\text{F}$ by switching on the PFC capacitor using a three-phase back-to-back SCR switch at $t = 1.377$. As seen from Figure 6.25, the H_∞ controller works well under the capacitance variations. The little distortion of the voltages after switching on the PFC capacitor is caused by the SCR switch. (The switch is turned on each time the phase current crosses zero. Since the current is leading the voltage by 90 degrees, the voltage has some switching noises at the top.)

Figure 6.25. Experimental Load 1 voltages with capacitor change.

The resonance effect of switching on a PFC capacitor and the proposed damping method is tested in the second experiment. Similar to simulation in Section 6.5, the harmonic disturbance source is chosen to be the DG system output voltages, which is programmed to have a phase shift (60 degrees), a magnitude drop (phase voltage drops from 98V to 96V) and a frequency drop (from 50Hz to 48Hz) simultaneously. Under this disturbance, the performance of the microgrid with inner capacitor current feedback method, inductor current feedback method is shown in Figures 6.26-6.27 and Figures 6.28-6.29 respectively. The fast settling time of the resonance voltages (Figure 6.28) and currents (Figure. 6.29) with filter inductor current feedback method proves it is more effective for the resonance damping.

Further attenuation of the resonance by employing the dual-inverter conditioner is shown in Figures 6.30 to 6.32. By controlling the series inverter as a virtual harmonic resistor, the resonance becomes almost unnoticeable, with both the voltages and currents settle down rapidly as seen from Figures 6.30 and 6.31. The voltages generated by the series inverter are shown in Figure 6.32. As seen, the series inverter generates harmonic voltage during the transient under the disturbance, while it provides zero voltage at steady state. Again, the relatively long transient shown in Figure 6.32 is caused by the dynamics of high pass filter.

Figure 6.26. Experimental Load2 voltages with filter capacitor currents feedback.

Figure 6.27. Experimental line currents with filter capacitor currents feedback.

Figure 6.28. Experimental Load2 voltages with filter inductor currents feedback.

Figure 6.29. Experimental line currents with filter inductor currents feedback.

Figure 6.30. Experimental Load 2 voltages with filter inductor currents feedback and series compensation.

Figure 6.31. Experimental line currents with filter inductor currents feedback and series compensation.

Figure 6. 32. Experimental series voltages generated by the series inverter.

Table 6. 1 System parameters for simulation and experiment.

Parameter	Value
Nominal line-to-line grid voltage	120V
Nominal power	1kVA
Frequency	50Hz
DC supply voltage	250V
Switching frequency for both inverter	10kHz
Shunt inverter filter capacitance	30 μ F (0.14 pu)
Shunt inverter filter inductance	5mH (0.11 pu)
Shunt inverter filter winding resistance	0.35 Ω (0.02 pu)
Series inverter filter capacitance	10 μ F (0.05 pu)
Series inverter filter inductance	3.9mH (0.08 pu)
Series inverter filter winding resistance	0.2 Ω (0.01 pu)
Series transformer turns ratio	1:1
Line resistance Rline	3 Ω (0.2 pu)
Line inductance Lline	10mH (0.21 pu)
Load1 in the microgrid	110W 65Var
Load2 in the microgrid	145VA
Load2 power factor	0.49
Load2 improved power factor	0.87

6.7 Discussion

This chapter presents a detailed study of a microgrid system with a PFC capacitor bank connected. It reveals that the effective filter capacitance would be changed due to the connection of a PFC capacitor to a local load of a DG system. Also, resonance can occur in islanding mode of the microgrid operation, when a PFC capacitor is installed in the load at PCC. An H_∞ controller is designed to produce performances similar to a P+resonant controller by having high gains at the vicinity of line frequency, while providing more explicit robustness in face of the filter capacitance variation caused by the switching of PFC capacitors. For the resonance situation, a thorough analysis is carried out to show that inner filter inductor current feedback method is more effective for the resonance damping than filter capacitor current feedback. A further damping method is also proposed, which employs the dual-inverter microgrid conditioner. The series inverter acting as a virtual harmonic resistor is effectively controlled. This study has been tested in simulation and experimentally using an emulated laboratory microgrid system.

Chapter 7

Medium Voltage Experimental Verifications

7.1 Introduction

All the developed controllers, conditioners and algorithms for microgrid application are tested in simulations (offline simulation or real time simulation) and low voltage experiments in previous chapters. This chapter extends the work by implementing some selected controllers and control algorithms on a series grid interfacing inverter at 10kV voltage level. These further verifications of previously developed controllers on the medium voltage distribution level are carried out using a series connected voltage source inverter (VSI) in the form of a Dynamic Voltage Restorer (DVR) prototype in collaboration with Aalborg University, Denmark.

The DVR is a series custom power device used to protect sensitive loads from the effects of voltage disturbance at the Point of Common Coupling (PCC). A typical DVR connected system circuit at medium voltage (MV) distribution level is shown in Figure 7.1. Very similar to the series inverter topology proposed for dual-inverter microgrid conditioner in Chapter 4, the DVR shown in Figure 7.1 consists of essentially a series connected injection transformer, a Voltage Source Inverter (VSI), inverter output filter and an energy storage device (usually capacitor) connected to the DC link. The high voltage (HV) power system upstream to DVR is represented as a voltage source which is transformed to MV level by a step-down transformer. The basic operation principle of DVR is to inject an appropriate voltage in series with the supply through injection transformer when a PCC voltage sag is detected. MV loads or low voltage (LV) loads connected downstream through another step-down transformer are thus protected from the PCC voltage sags.

Figure 7.1 Typical series DVR circuit topology at medium voltage level

Objective of the work in this chapter is to further test the controllers and control algorithms developed in previous chapters on the series inverter at medium voltage level.

The medium voltage experimental verifications include:

- Further performance verification and comparison of P+resonant controller and H_∞ controller designed for shunt inverter of the dual-inverter microgrid conditioner in Chapters 4 and 6, by implementing them on the series grid-interfacing inverter.
- Medium voltage implementation of flux-charge model based fault current limiting algorithm developed for the series inverter of microgrid conditioner in Chapter 5.
- A transient improvement method for the inverter output voltage regulation, which is developed during the stay at Aalborg University.

Note that except for the fault current limiting algorithm, which is specially developed for series inverter as discussed in Chapter 5, all the other control methods investigated in this chapter including the P+resonant controller, H_∞ controller and transient improvement methods are equally applicable to the shunt inverter for DG system voltage regulation, although they are only tested on the series inverter in this chapter.

7.2 Medium Voltage Experimental System Setup

This section briefly introduces the medium voltage experimental system setup used for this work (full details of system description can be found in [68]). The 10kV medium

voltage level DVR system prototype is illustrated in Figure 7.2, with the photos shown in Figure 7.3

Figure 7.2. 10 kV experimental system setup.

Figure 7.2 shows the overall medium voltage system platform. The supply is a programmable 15 kVA California Instrument Supply at 380 V. A 50 kVA (0.4 kV/10 kV) star-delta distribution transformer steps up the voltage to 10 kV. The load voltage is stepped down using another 50 kVA (10 kV/0.4 kV) delta-star distribution transformer. The medium voltage prototype DVR is connected at the 10 kV level through three specially made 67 kVA (0.29 kV/2.9 kV) single-phase series injection transformers, which step up the DVR's 200 kVA low voltage inverter voltage to 10 kV level (with about 50% compensation capacity to protect a 400 kVA load). The DC bus voltage for the DVR can be charged up to 600V using two unidirectional DC supplies, which provide maximum of 4680 J energy in the 26 mF DC capacitors for transient use in the DVR's sag ride-through capabilities. A 20-foot shipping container (see photos in Figure 7.3) is used to house the medium voltage DVR (including inverter, DC link, filter circuits, controller and injection transformers), which allows relocation of the system for off site testing.

Control system is implemented on a dual DSP-Microcontroller system, with a 32-bit 33 MHz Analog Devices AD21026 floating-point Sharc DSP for implementation of control algorithm and a Siemens SAB 80C167 Microcontroller for PWM signal generation for the six IGBT phase-legs. A Dual Port RAM unit (DPRAM) is used as a communication link between the DSP and Microcontroller, where the results from the DSP are transferred to DPRAM and are read by the Microcontroller. The interface from the user to the control system is via a Pentium PC and the DSP is located in a socket inside the PC. Analog signals are converted to digital form with two eight channel AD 7891 from Analog Devices and read by the DSP once in each switching cycle. Note that since symmetrically sample PWM is used, the controller's sample rate is equal to the switching frequency.

Figure 7.3 Photos of: (a) 20-foot DVR container and step-up, step-down transformers, (b) DC supply and control system (inside the container), (c) IGBT inverter, DC link capacitor, filter circuit and bypass circuit (inside the container), (d) injection transformers (inside the container) and (e) programmable AC supply (in HV lab).

Linear resistive load, induction motor and nonlinear load (a diode rectifier bridge with a capacitor bank and resistive load connected in parallel) are all used for experiments. All experiments are conducted at low power due to the limited capacity of California Instrument Supply (15 kVA), although most of the tests are carried out at medium voltage level (10 kV). The fault current limiting algorithm is tested on 3 kV, due to the limited power supply and the 50% compensation capacity of laboratory DVR prototype.

Detailed system prototype parameters and induction motor load specifications are listed in Tables 7.1 and 7.2 respectively.

Table 7. 1 System parameters for 10 kV DVR setup

Parameter		Value
Grid	Nominal grid line-line voltage	380 V
	Nominal power	200 kVA
	Frequency	50 Hz
DVR (exclude injection transformer)	Switching/sampling frequency	5 kHz
	Inverter filter inductance	2*260 μ H (0.23 pu)
	Inverter filter resistance	25 m Ω (0.03 pu)
	Inverter filter capacitance	120 μ F (0.03 pu)
	DC link capacitance	26 mF (5.9 pu)
Injection Transformer (10:1)	Power	67 kVA
	Primary voltage	2.9 kV
	Secondary voltage (DVR side)	0.29 kV
	Leakage impedance	0.05 pu
Step-up transformer (1:25)	Power	50 kVA
	Primary voltage	0.4 kVA
	Secondary voltage	10 kVA
	Leakage impedance	0.03 pu
Step-down transformer (25:1)	Power	50 kVA
	Primary voltage	10 kV
	Secondary voltage	0.4 kV
	Leakage impedance	0.036 pu

Table 7. 2. Parameters of induction motor load used in DVR system.

Parameter	Value
Rated voltage	380 V
Nominal supply frequency	50 Hz
Rated output power	3 kW
Power factor	0.82
Efficiency	81%
Nominal speed	1430 rpm
No. of poles	4

7.3 Comparison and Implementation of H^∞ and P+resonant Controllers

Majority of faults on a power system is unbalanced in nature (with positive- negative- and zero-sequence components) which results in unbalanced voltage sag at PCC (usually without zero-sequence components due to widely used delta-star distribution transformers and three-wire medium voltage level in most countries [68]). Therefore it would be necessary to generate appropriate unsymmetrical compensation voltage by a DVR to compensate both the positive- and negative-sequence components of unbalanced voltage sags.

In this section, two voltage controllers designed on the stationary frame with embedded inner current loops are implemented for DVR voltage control. A P+resonant controller is first designed to achieve good positive- and negative-sequence fundamental voltage regulation by having high gains around positive- and negative-sequence fundamental frequencies and without the complex stationary-to-synchronous frame transformations required for traditional synchronous PI regulators (as discussed in Chapter 4). Furthermore, inspired by the unique characteristic of the P+resonant controller, and with the purpose to achieve explicit robustness in face of parameter variations, the H^∞ control technique designed in Chapter 6 is also implemented. The H^∞ controller's performance can be fine-tuned through careful selection of its weighting functions. The synthesized

H_∞ controller thereby exhibits high gains around positive- and negative-sequence fundamental frequencies similar to the P+resonant controller, but with explicit robustness in face of parameter variations. A thorough discussion and performance comparison of these two controllers in both transient and steady state situation is also presented. Both controllers are extensively tested on the laboratory 10kV medium voltage level DVR system, under various voltage sags (balanced and unbalanced) and with different loading (linear and nonlinear) conditions.

7.3.1 Overall DVR control scheme

The proposed control scheme for DVR is illustrated in Figure 7.4. As shown, the voltage at Point of Common Coupling (PCC), V_{PCC} , is measured and used for PCC voltage sag detection and for demand DVR injection voltage generation (at low voltage side of the injection transformer). For DVR injection voltage control, a multi-loop control scheme is implemented as illustrated in Figure 7.4, where an inner filter inductor current (I_L) feedback loop is shown embedded in an outer filter capacitor voltage (V_{DVR}) (or voltage at low voltage side of the injection transformer) feedback loop. Both the voltage and current controllers are implemented on the stationary frame to avoid the complex frame transformations. Also shown in Figure 7.4 is an algorithm to limit the inverter reference voltage, which is used for reference voltage change rate limit, transformer saturation limit and over-modulation protection. The focus of this work is the DVR injection voltage control, i.e. the double-loop control scheme for the DVR.

Figure 7.4. Overall DVR control scheme.

After a voltage sag is detected, the difference between reference PCC voltage V_{PCC}^* and measured value V_{PCC} is divided by the injection transformer turns ratio to compute the

reference DVR injection voltage V_{DVR}^* in stationary α - β frame. The DVR voltage feedback is compared with its reference and the error is fed in the voltage controller. In this work two voltage controllers, namely P+resonant controller and H_∞ controller, are investigated. Both controllers are implemented at stationary α - β frame and with significant gains at the vicinity of positive and negative fundamental frequencies (± 50 Hz) ensuring almost zero steady state error. Detailed discussion and comparisons of these two controllers are presented in subsections 7.3.2, 7.3.3 and 7.3.4.

Output of the voltage controller is subsequently transformed to a-b-c frame to generate the reference current I_L^* which is compared with the filter inductor current feedback I_L . The current error is fed to a proportional controller whose output gives the desired voltage $V_{Inverter}^*$ to be generated by the inverter, and is fed to the PWM generator. Note that the inner current loop mainly functions to improve the transient and stability of the voltage control scheme and the proportional controller used will not affect the accuracy of voltage tracking of the outer voltage loop where P+resonant or H_∞ controller is used. In the following text, the different voltage controllers will be investigated.

7.3.2 Review of P+resonant controller

The P+resonant controller has been discussed and investigated in both simulations and low voltage experiments in Chapters 4 and 5 for the control of either the shunt or the series inverter of dual-inverter microgrid conditioner. Here the P+resonant controller is briefly reviewed for completeness of later comparison of the P+resonant controller with designed H_∞ controller.

The ideal P+resonant controller discussed in Chapter 4, is re-expressed in (7.1), which can be mathematically derived by transforming a synchronous frame PI controller to the stationary frame without consideration of the redundant cross coupling terms [51], and has an infinite gain at the controller's resonant frequency ω_0 or the line fundamental frequency ($2\pi \cdot 50$ rad/s).

$$G(s) = 2k_p + \frac{2k_I s}{s^2 + \omega_0^2} \quad (7.1)$$

In [52] and Chapter 4, it is revealed that by transforming PI controllers in both positive- and negative-sequence synchronous frames of a three-phase system to the stationary frame (using either time domain or frequency domain techniques), the final stationary controller of (7.1) can be obtained, and the cross coupling terms generated from positive- and negative-sequence synchronous frames cancel each other if same PI parameters are employed in both synchronous frames. Therefore, the P+resonant controller exhibits infinite gain at both the positive and negative fundamental frequencies and can therefore achieve zero steady state error for both positive- and negative-sequence components regulation in principle. An example bode plot for the ideal P+resonant controller at both positive and negative frequencies is shown in Figure 7.5. As illustrated, the ideal P+resonant controller has infinite gains at ± 50 Hz. Note that the controller gains at other frequencies are same and mainly depend on the value of k_p (gains at frequencies around ± 50 Hz are also related to k_I).

Figure 7.5. Bode diagram of an ideal P+resonant controller.

Although theoretically, the ideal P+resonant controller can achieve zero steady state error by introducing infinite gains at ± 50 Hz, it has implementation problem and is sensitive to frequency variations. More practical forms are therefore proposed in [51, 66], and the practical P+resonant controller in [51] is adopted as did in Chapter 4, which is re-expressed in (7.2):

$$G(s) = k_p + \frac{2k_I \omega_{cut} s}{s^2 + 2\omega_{cut} s + \omega_0^2} \quad (7.2)$$

where ω_{cut} is the controller cutoff frequency. The frequency response of (7.2) is drawn in Figure 7.12 (together with the designed H_∞ controller), where it is shown that the controller has a wider bandwidth around the resonant frequency and it would minimize the sensitivity to slight system frequency variations, but at the cost of reduced resonant peak. It is noted that the 44dB resonant peak is still satisfactory for fundamental tracking error elimination. This practical P+resonant controller has three parameters, proportional gain k_p for overall gain regulation, resonant gain k_r for the resonant peak adjustment and cutoff frequency ω_{cut} for resonant width control. Further discussion of these parameters and their effects on the overall system performance is presented in subsection 7.3.4.

7.3.3 Design description of H_∞ controller

The H_∞ control technique has been investigated in Chapter 6. As discussed, the H_∞ controller synthesis is conducted by the singular value loop-shaping using mixed sensitivity approach, such that the H_∞ norm of the transfer function from w (exogenous input) to z (controlled output) is less than one.

For a double-loop control scheme, the design of DVR voltage control is separated into two parts, H_∞ voltage controller synthesis and inner current proportional regulator tuning, which are related to each other. Similar to a typical multi-loop control design approach, the DVR controller design is an iterative process. An H_∞ controller is first designed with specified robustness and error tracking performance based on a given plant including inner current loop. The inner current regulator is then fine tuned with consideration of its influence on the synthesized H_∞ controller and the generated new plant (for the outer loop), as well as its relations to other disturbance rejection capability not included in the system model (such as load current in this work). After the inner current loop regulator gain is determined, an H_∞ controller is finally obtained (re-designed) based on the best tuned inner current loop. The design process, as mentioned earlier, begins with the H_∞ voltage control loop.

7.3.3.1 Weighting function selection for robust performance

The nominal plant, with the inner closed current loop, is expressed as:

$$G_N = \frac{k_C}{C_f L_f s^2 + C_f (R_f + k_C) s + 1} \quad (7.3)$$

where k_C is the proportional gain for the current loop. Due to the difficulties of changing components in the laboratory DVR prototype, the H_∞ controller is designed based on 2/3 times the known system parameter values (e.g. filter inductance and capacitance) and then implemented on the original system to test its performance. System parameter uncertainty is chosen to be between 80% and 150% of the nominal DVR model values (which is quite enough for the parameter variations due to aging, thermal effects, etc.), so that the synthesized H_∞ controller is expected to perform well at the original system (note that load is not considered as part of DVR model and the load current is treated as an additional disturbance source). This parameter uncertainty can then be transformed to multiplicative output uncertainty as done in Chapter 6. The relative plant uncertainty $\Delta(s)$ with a combination of different parameter variations is plotted in Figure. 7.6 (with the dashed line indicating the worst-case uncertainty boundary) W_3 is selected as above the worst-case boundary as shown in Figure. 7.6, where $W_3 = 0.000266s + 0.8$.

Figure 7.6. Singular values of $\Delta(s)$ and W_3 .

7.3.3.2 Weighting function selection for tracking error performance

As discussed in Chapter 6, to design a H_∞ controller with similar characteristics as a P+resonant controller which has high gains at fundamental frequencies (both +ve and -ve), and thus small tracking error at fundamental frequencies (both +ve and -ve), a standard second order weighting function for $S(s)$ can be used as shown in (7.4):

$$W_1 = \frac{k_A \omega_0^2}{s^2 + 2\zeta \omega_0 s + \omega_0^2} \quad (7.4)$$

where natural frequency ω_0 is selected as the line frequency, k_A in the numerator gives a freedom for adjusting the tracking error over the whole frequency range and the damping ratio ζ provide another freedom for special regulation of the tracking error at the line frequency ω_0 . As discussed in Chapter 6, a smaller ζ guarantees smaller steady state error at the line frequency. The tracking error at ω_0 as well as the other frequencies can also be regulated by tuning k_A . Increasing k_A also has similar effect as broadening the notch band of W_1 around the line frequency and hence making the system less sensitive to operating frequency variations (the width of notches of W_1 and resulting $S(s)$ is not related to ζ , refer to Figure 6.5 in Chapter 6). But large k_A will degrade the system low frequency disturbance attenuation capability as will be discussed later.

7.3.3.3 Mixed sensitivity H_∞ controller synthesis

Using the same technique (MATLAB *hinf* function) as in Chapter 6, the H_∞ controller, after being reduced to a third-order controller, is shown in (7.5), with bode plot drawn in Figure 7.7:

$$K(s) = \frac{0.04926s^3 + 491*10^4 s^2 + 2.263*10^6 s + 1.734*10^8}{s^3 + 2031s^2 + 1.114*10^5 s + 1.998*10^8} \quad (7.5)$$

As expected, the designed H_∞ controller in Figure 7.7 has significant gains at ± 50 Hz to ensure nearly zero steady state errors for any unbalanced voltage regulation. Also it can be observed that the H_∞ controller has fast roll-off at high frequencies making the DVR system immune to any high frequency switching or measurement noises.

Figure 7.7. Bode plot of designed H^∞ controller.

7.3.3.4 Disturbance rejection and inner current loop tuning

The inner current loop with a proportional regulator mainly functions to improve the transient and stability of the voltage control scheme and this method is used effectively in works described in previous chapters. The proportional controller is used for fast response of current loop (transient improvement) and reshaping the original plant (stability improvement), and it will not affect the accuracy of voltage tracking of the outer voltage loop where P+resonant or H^∞ controller is used.

The modified plants with various proportional regulator gains are shown in Figure 7.8, together with the original plant for comparison. It can be seen that the original plant has serious resonance problem introduced by the LC filter. This resonance can be effectively attenuated by the inner current loop. It can also be observed that a larger current regulator k_C would broaden the plant bandwidth and damp out plant resonance peak caused by the LC filter (although the absolute gain at the resonant frequency is not changed obviously with different k_C as shown in Figure 7.8), which leads to faster and smoother transient response of a system. Also seen from Figure 7.8 is that a larger k_C would cause larger phase errors at the operating frequency, which have to be compensated by the outer voltage controller.

Figure 7.8. Plants with closed current loop.

Different plant transfer functions generated by various current controller gains have almost no influence on the final open loop system with H_∞ voltage controller, as shown in Figure 7.9(b). This is due to the H_∞ loop shaping approach, where the final system is mainly determined by the specified weighting functions, and the synthesized H_∞ controller is shaped only according to the weighting functions and the plant used. As shown in Figure 7.9(a), H_∞ controller gains will decrease with a high gain plant introduced by larger k_C (note that the H_∞ controller with $k_C=0.9$ in this figure is not reduced to a third order one and there is a slight shape difference compared to the third order controller shown in Figure 7.7). It is commented that although different k_C will not change the final system dynamics (which is determined by the weighting functions), a larger k_C , which produces a well damped plant and generates a more regulator shaped H_∞ controller (and thus more accurate low order equivalent form), is thus preferable.

Larger current regulator constant is also needed for the load current disturbance rejection capability of the final system. As shown in Figure 7.10, a larger k_C would make the system always attenuate the disturbance from load current with loop gains less than 0 dB. The system is more sensitive to disturbances especially at around the LC filter cutoff frequency with a small k_C . Once again it is desirable to use a large k_C .

Figure 7.9. Effects of difference current regulator gains on (a) synthesized H_∞ controller and (b) final open loop system.

Figure 7.10. Disturbance rejection from load current to inverter output.

But the value of k_C is always limited due to practical considerations such as capacitor current noise amplification (filter inductor current is the sum of capacitor current and filter output current, and the role of filter capacitor is to provide a shunt pass for the harmonic currents [69]) or any current measurement DC offset. From Figure 7.11 it can be seen that with a larger k_C , the DVR output is more sensitive to the low and high frequency inductor current disturbances (except at LC filter cutoff frequency, where different k_C exhibits similar disturbance rejection capability).

Finally, with considerations of all these factors, the criteria of tuning k_C are to choose a k_C as large as possible provided that the stability of the system from the current feedback disturbance is still well maintained. In this work $k_C=0.9$ is selected.

Figure 7.11. Disturbance rejection from filter inductor feedback current to inverter output.

7.3.4 Performance and robustness comparison

As discussed in previous subsections, both P+resonant controller and the synthesized H_∞ controller exhibit significant gains at vicinity of ± 50 Hz with very good voltage tracking. However they have different characteristics at the other frequencies as can be seen from Figure 7.12, which determines the system dynamics and robustness.

7.3.4.1 Performance discussion

The practical P+resonant controller in (7.2) has three parameters for tuning depending on control objectives used. The transient performance of the DVR system with P+resonant controller mainly depends on the proportional gain k_p . As can be seen from Figure 7.12, the gains at frequencies other than the controller resonant frequency remains constant and are related with k_p . With a larger k_p , the system will have wider bandwidth and thus faster transient response to the change of reference. While a larger k_p also means high amplification of the DVR LC filter resonance (for the new plant with inner current loop closed, this LC resonant frequency is shifted to a higher frequency as seen from Figure 7.13), which will cause transient resonant oscillations or even affect the system stability. To ensure a system with reasonable fast transient, the value of k_p should not be too small.

The P+resonant controller's steady state error performance is mainly determined by the resonant peak. The resonant gain k_I is responsible for this peak value and a large gain value can be assigned to k_I without substantially affecting the transient and system stability. Cutoff frequency ω_{cut} for P+resonant controller determines the controller's resonant bandwidth. For a DVR system, where a voltage sag is usually accompanied with a phase angle jump, a wider resonance bandwidth is required, since the angle jump will affect the PLL performance and cause an effect similar to a frequency change. A large ω_{cut} can also improve the transient speed but subject the system to LC filter resonance (if the resonant width extents to the filter LC cutoff frequency).

The third order H_∞ controller, on the contrary, exhibits very good LC resonance attenuation while still keeps reasonable transient response by having an additional pole and thus fast roll-off at high frequency (see Figure 7.13). As discussed, the H_∞ controller is tuned by selecting two weighting functions for the robustness and error tracking performance. With a plant including inner current loop, the filter LC resonant can be still serious due to the limited proportional controller k_C for inner current. The robust performance design is believed to introduce the fast high frequency roll-off characteristics of the H_∞ controller and make it immune to the LC filter resonance. The error tracking performance is determined by the weight function W_I in (7.4). As mentioned, small error tracking at $\pm 50\text{Hz}$ can be obtained by having a small ζ . Similar to the proportional gain k_P of P+resonant controller, the overall gain of the H_∞ controller on the frequency spectrum can be regulated by tuning parameter k_A in (7.4).

For the sake of consistency, control parameters are chosen to give the same resonant width and peak to both controllers (and thus same steady-state performance) as shown in Figure 7.13. Also same inner current gain ($k_C = 0.9$) is used for each controller tuning/design. The resultant controller and system open loop bode plots are illustrated in Figures 7.12 and 7.13. It can be seen that the systems with H_∞ controller or P+resonant controller have similar bandwidth. However, compared with the P+resonant controller, which is sensitive to LC filter resonance, the H_∞ controller would make a system immune to this filter LC resonance by having improved high frequency attenuation.

Also seen from Figures 7.12 and 7.13 is that the P+resonant controller has better low frequency attenuations below 50Hz compared to the H_∞ controller, which is due to the small k_P (0.4) limited by the consideration at the LC filter cutoff frequency as discussed earlier. This low frequency attenuation effectively filters out DC offsets present in most IC chips (used for building analog controllers or interfacing boards) and other sub-harmonics or sub-resonance related disturbances. It is observed in experiment that too large low frequency gains for H_∞ controller would cause stability problems. Imperfect measurement calibrations, AD conversion offset compensation, or DVR reference generated from the PCC which might have low frequency components due to phenomena like ferro-resonance of the distribution transformer would cause low frequency disturbances. To reduce the low frequency gains, k_A in (7.4) should be made small ($k_A = 1.1$ in this work).

Figure 7.12. Bode plot of designed P+resonant and H_∞ controller.

Figure 7.13. Bode plot of open loop system with P+resonant and H_∞ controller.

As illustrated in Figure 7.13, a system with H_∞ controller has much better attenuation of high frequency distortion. The immunity to high frequency disturbance especially at the filter LC resonance frequency is responsible for the system robustness, which will be discussed in next subsection.

7.3.4.2 Robustness comparison

A robustness comparison of P+resonant and H_∞ controller are based on simulations. As discussed in Section 7.3.3, the H_∞ controller is designed based on 2/3 of the nominal system parameter values with a parameter variation range from 80% to 150%. Therefore, when implemented on the nominal system there should be no degradation of performance due to its specified robustness. This can be verified in Figure 7.14, where waveforms (a) and (b) are the DVR injection voltage and load voltage with 2/3 of system parameter values, and waveforms (c) and (d) are the injection voltage and load voltage with original system parameters. It can be seen that the DVR compensation performance with H_∞ controller is very robust under system parameter variations.

For the purpose of comparison, a P+resonant controller is specifically tuned with 2/3 times the nominal system parameters. Its performance is shown in Figure 7.15 (a) and (b) for DVR compensation voltage and load voltage respectively. The P+resonant controller could not exhibit sufficient robustness for parameter variations especially when the filter parameters are increased (in this example, from 2/3 of nominal values to the nominal values), which is equivalent to shifting the LC cutoff frequency to a lower value. The LC resonance at lower frequency will not be attenuated sufficiently if the P+resonant controller does not have enough robustness margins (see Figure 7.12), resulting in serious transient resonance as shown in Figure 7.15 (c) and (d). This transient resonance, if not damped effectively, may even destabilize the system. On the other hand, parameter variations that shift the LC cutoff frequency to a higher value will not substantially affect the system stability with a P+resonant controller.

Figure 7.14. Robustness checking for H_∞ controller: (a) (b) injected and load voltages with 2/3 system parameter values and (c) (d) injected and load voltages with nominal system parameters.

Figure 7.15. Robustness checking for P+resonant controller: (a) (b) injected and load voltages with 2/3 system parameter values and (c) (d) injected and load voltages with nominal system parameters.

7.3.5 Experimental comparison under balanced voltage sag and linear load

The first experiment is run with balanced voltage sag and linear load (67Ω). The PCC voltage drops to 70% of its nominal value from 40ms to 140ms (5 fundamental cycles). The PCC voltages, DVR injected voltages (at high voltage side of the series transformers) and load voltages with both controllers are shown in Figures 7.16 to 7.18. It can be seen that both controllers are equally good at load voltage restoration during a PCC voltage sag. But there is still slight difference between the DVR injected voltages during the startup transient, which can be seen in the zoomed-in view of injected voltage in Figure 7.19. The P+resonant controller gives slight startup oscillations, this is due to the relatively high gains of the controller at high frequencies, which make the system to resonate at filter LC filter resonant frequency once it is excited. The H_∞ controller, on the contrary, has very smooth transient during startup. This can also be verified by the comparison of results shown in the frequency spectra in Figures 7.20 and 7.21. The DVR injected voltage with H_∞ controller has less THD (1.9%) compared to the P+resonant controller (THD=2.1%), due to the effective attenuation of high frequency distortions of the H_∞ controller (Figure 7.20(b)) compared to the P+resonant controller (Figure 7.20(a)). This difference results in slight deviation in load voltage too. As shown in Figure 7.21, the load voltage with H_∞ controller has a slightly better THD (0.77%) and lower high frequency harmonics than that with P+resonant controller (with THD of 0.8%). In general, both the P+resonant

controller and H_∞ controller have good performance when connected to linear load with only a slight difference during start up transient.

Figure 7. 16. PCC voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 17 Injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 18. Load voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 19. Load voltages Zoom-In view: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 20. Frequency spectra of injected voltage: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 21. Frequency spectra of load voltage: (a) with P+resonant controller and (b) with H_∞ controller.

7.3.6 Experimental comparison under balanced voltage sag and nonlinear load

The nonlinear load is a diode rectifier bridge with a capacitor bank (200 μ F) and resistive load (80 Ω) connected in parallel. The nonlinear load current (phase C) is shown in Figure 7.22. Again, the PCC voltage drops to 70% of its nominal value from 40ms and lasts for 5 cycles. The PCC voltages, DVR injected voltages and resultant load voltages are shown in Figures 7.23 to 7.25. It can be observed that with nonlinear load connected at downstream, the PCC voltages, DVR injected voltages and load voltages are all affected and distorted. The distortion of PCC voltage is due to the voltage drop on source impedance (mainly the step-up transformer in this experiment). This distorted PCC voltage causes distortion in DVR reference voltage ($V^*_{PCC} - V_{PCC}$) and finally the injected voltage. But higher distortion of the injected voltages is observed in Figure 7.24(a) with P+resonant controller compared to the H_∞ controller (in Figure 7.24 (b)). Same effect is more obviously shown at the zoomed-in waveforms in Figure 7.26 (a) and (b). The higher distortion with P+resonant controller is caused by the continuous excitation of high frequency harmonics introduced by the nonlinear load. The H_∞ controller in this case is a better option due to its high frequency rejection and filter LC resonance attenuation. As seen from Figure 7.27(a) and (b), it is obvious that the injected voltage with H_∞ controller has much less 7th, 11th, and 13th harmonics and less THD. These different injection voltages cause the load voltage with H_∞ controller to have smaller high frequency harmonics and smaller THD as shown in Figure 7.28. It can be concluded that with nonlinear load, advantages of H_∞ controller becomes more obvious with its better attenuation of the high frequency harmonic distortions.

Figure 7. 22. Nonlinear load current (phase C).

Figure 7. 23. PCC voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 24 Injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 25. Load voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 26. Zoom-In view of injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 27. Frequency spectra of injected voltage: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7. 28. Frequency spectra of load voltage: (a) with P+resonant controller and (b) with H_∞ controller.

7.3.7 Experimental comparison under unbalanced voltage sag

Experiment is also run with unbalanced voltage sag. The PCC voltages shown in Figure 7.29 are programmed with a positive-sequence voltage drop of 20% and an injection of 10% negative-sequence voltage. The sag begins at 40ms and it lasts for 5 cycles. The corresponding DVR injection voltages and load voltages are shown in Figures 7.30 and 7.31. It can be seen that both the P+resonant and H_∞ controllers would effectively inject appropriate unbalanced voltages and symmetrically restore the load voltage to its nominal value with the inherent or designed sufficient large gains at $\pm 50\text{Hz}$.

A sequence components analysis of the PCC voltages and load voltages are shown in Figure 7.32(a) and (b). With both controllers, the negative-sequence component of load voltage is reduced to 1.6% with the presence of 10% negative sequence PCC voltage. Note that the waveform oscillatory transients in Figure 7.32(a) and (b) are not experimental measurements. They are introduced by the low pass filtering effect (averaging data over one fundamental cycle) of the sequence components analysis tool used.

Figure 7.29. PCC voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7.30. Injected voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7.31. Load voltages: (a) with P+resonant controller and (b) with H_∞ controller.

Figure 7.32. Negative-sequence components of the PCC and load voltages: (a) with P+resonant controller and (b) with H_∞ controller.

7.3.8 Experimental verification of H_∞ controller with motor load

Bulk of the industry use induction motor loads, the DVR performance with H_∞ controller under induction motor load is therefore investigated (Note that this experiment is not for comparison). The parameters of induction motor used (ASEA MK 110-23 IM) are listed in Table 7.2. Similarly, the PCC voltage drops to 70% of its nominal value from 40ms onwards and lasts for 5 cycles. The PCC voltage sag and fast response of DVR injected voltages are shown in Figures 7.33 and 7.34. The resultant load voltage and motor speed are shown in Figure 7.35(a) and (b). The motor speed is kept constant due to its well compensated input voltage, whose zoomed-in views at sag start and recovery transients are shown in Figure 7.36(a) and (b). The transients are smooth with only negligible distortions/ripples during sag recovery moment, which is due to the DVR LC filter. The PWM signal is forced to be zero upon the detection of PCC voltage recovery from a sag, leaving the LC filter voltage/current uncontrolled and subject to the slight LC resonance due to the remaining energy discharging in the LC filter circuit.

Figure 7.33. PCC voltages

Figure 7.34. Injected voltages

Figure 7.35. (a) Induction motor load voltages and (b) motor speed.

Figure 7.36. Zoom-In views of load voltage transient during (a) sag occurrence (b) recovery from a sag.

7.4 Implementation of Fault Current Limiting Algorithm

Despite the advantages of medium voltage level DVR operation mentioned in [68] (such as protection of high power applications, elimination of control consideration of zero-sequence voltage due to the three-wire medium voltage distribution system (in most countries) and achievement of more cost efficient operation per MVA), implementation at medium voltage level also subjects the DVR to more frequent faults in the downstream load side. Large fault currents will flow through the DVR during a downstream fault before the opening of a circuit breaker. This large fault current will also cause the PCC voltage to drop, which could affect the MV or LV loads on the other feeders connected to

the PCC. During a downstream fault, passive control method is often used to control the DVR by enabling the bypass circuit (usually a slow mechanical bypass together with a fast solid-state switch) [68, 70, 71] and protecting the DVR from the fault current, while allowing the large fault current to flow which could cause the PCC voltage to drop. Active control of series connected device during a fault by limiting the fault current is reported in [72, 73] and Chapter 5. Compared to the passive protection of DVR, active control of DVR during a downstream fault makes the additional protection circuits unnecessary and the implementation easy.

In this section, a fault limiting function is proposed and integrated in DVR operation to limit the flow of large line currents, and therefore restore the PCC voltage as well as protect the DVR system components. Flux-charge-model feedback algorithm developed in Chapter 5 is implemented at medium voltage level for controlling the DVR to function by inserting large virtual inductance in series with the distribution feeder and limit the fault current. Controlling the DVR as a virtual inductor would also ensure zero real power absorption during DVR compensation and with minimized stress on DC link energy storage device.

The flux-charge model based fault current limiting algorithm is tested on the medium voltage DVR system, with its effectiveness verified under both symmetrical and unsymmetrical downstream fault conditions. As explained earlier, the fault current limiting experiments are run at 3 kV due to the limited rating of AC supply (15 kVA) used and the 50% DVR compensation capacity in the prototype.

7.4.1 Downstream fault at a DVR connected system

Figure 7. 37. DVR connected system with downstream fault.

Figure 7.37 shows a downstream fault occurs at the DVR connected system. This fault can be at the medium voltage level (a nearby fault) or at the low voltage level after a step down transformer (a remote fault). Using the voltage divider concept, the fault current and PCC voltage in this fault situation can be calculated as (without consideration of other feeders connected at PCC):

$$I_{fault} = \frac{V_s}{Z_1 + Z_3} \quad (7.6)$$

and

$$V_{PCC} = \frac{Z_3}{Z_1 + Z_3} V_s \quad (7.7)$$

Where Z_1 is the source impedance and Z_3 is the downstream feeder impedance including the fault impedance. Due to the very low line impedance, the fault current will be significant as can be seen from (7.6). This large fault current is harmful to the series connected equipment such as the DVR if not fully protected. Also it will cause harm to the system components such as overhead lines or underground cables. As illustrated in (7.7), the PCC voltage will drop and the remaining voltage can be very low with a small Z_3 (a nearby fault). This sag in PCC voltage will affect the loads on the other parallel feeders connected to PCC. For self-protection, the DVR can be physically bypassed. But the large fault current and resulting PCC sag will sustain until the downstream fault is cleared by a circuit breaker.

7.4.2 Using DVR to limit fault currents

As discussed, passive control of the DVR by enabling the bypass circuit would only protect the DVR itself during a downstream fault causing large fault current flow and PCC voltage sag. A more promising alternative approach is thus to control the DVR actively and reduce the large fault current as well as restore the PCC voltage.

To reduce the fault current flow due to a downstream fault, the DVR can be controlled to inject a suitable series voltage in quadrature with the fault current, which makes the DVR

behave like an additional virtual line inductance L_0 in series with the distribution feeder. No real power will be involved during the compensation, which minimizes the stress on DC link capacitor.

By representing the DVR as an inductance in series, the fault current and PCC voltage can be re-calculated as:

$$I_{fault} = \frac{V_s}{Z_1 + Z_3 + X_0} \quad (7.8)$$

$$V_{PCC} = \frac{Z_3 + X_0}{Z_1 + Z_3 + X_0} V_s \quad (7.9)$$

where $X_0 = j\omega L_0$. It is obvious that the fault current is reduced and the PCC voltage can be restored by adding a large inductance in series with the line ($X_0 + Z_3 \gg Z_1$). Another effect is the load voltage will be further reduced, since most of the voltage drop will be across L_0 .

This load bus voltage drop will help fault detection and the tripping of loads at downstream side and interference minimization of protection system, although over current tripping is not possible in this case unless additional communication between the DVR and the downstream side over current circuit breaker is available. If it is necessary to operate the over current circuit breaker at PCC, a communication between the DVR and the PCC breaker might have to be made and this can be easily done by sending a signal to the breaker when DVR is in fault current limiting mode, since the DVR is just located after PCC [73].

Note that this fault current limiting function with $X_0 \gg Z_1 + Z_3$ also implies a 100% compensating capacity of DVR, since almost all the voltage drop between the restored PCC voltage and fault voltage is across the DVR in this condition.

7.4.3 Detection and recovery from a downstream fault

For fast downstream fault detection and therefore fast DVR reaction to the fault current, instantaneous current magnitude is calculated in α - β synchronous frame. Once the current magnitude exceeds a preset threshold I_T , the DVR is activated by injecting a series voltage and acting as a virtual inductor to limit the fault current as well as restore the PCC voltage.

Recovery from a downstream fault can be done by sensing the load voltage V_{load} (at medium voltage level) as in Figure 7.2. When the fault is cleared, the load voltage will increase with $V_{load} \approx V_{PCC}$, given the load impedance much larger than the DVR virtual inductance. Therefore once V_{load} is restored to a preset level V_T , the fault current limiting function of DVR can be terminated. Furthermore, to ensure DVR compensation is not turned off by any transient distortion or measurement noises, a low pass filter like characteristic is added to this recovery detection. This is done by turning off the DVR when $V_{load} > V_T$ is sustained for a period of time and no other downstream fault is detected during this period (in this work 20 ms for symmetrical fault and 50 ms for unsymmetrical fault).

7.4.4 Flux-charge-model control algorithm implementation for DVR

The DVR control scheme during a downstream fault is illustrated in Figure 7.38, where a fault detection unit is first implemented by measuring the three-phase line currents (for over current detection) and three-phase load voltages (recovery detection) as discussed in Section 7.4.3. Upon the occurrence of a downstream fault, the DVR is controlled as a virtual inductor in series with the distribution feeder to limit the fault current and restore the PCC voltage. The DVR is turned to passive mode by forcing all the PWM signals to be zero after a downstream fault recovery is detected.

To control the DVR as a virtual inductor, the flux-charge-model based control proposed in Chapter 5 for the series inverter of dual-inverter microgrid conditioner is implemented. A brief description of the design process is presented here.

Figure 7.38. Proposed DVR control scheme for fault current limiting.

Figure 7.39. Flux-charge model based control for DVR implementation.

The flux-charge model control scheme for DVR is illustrated in Figure 7.39. The control variable used for the outer flux-model is the inverter filtered terminal flux, defined as $\Phi = \int V_{DVR} dt$ where V_{DVR} is the filter capacitor voltage of the DVR (at DVR side of the injection transformer). In stationary α - β frame, this flux variable is compared against a reference flux given by $\Phi_{ref} = -L_0 I_{Line}$ where I_{Line} is the line current (at DVR side of the injection transformer) and the negative sign is to indicate that I_{Line} is drawn flowing out of the series inverter, similar as in Chapter 5). The flux error is then fed to the flux regulator, implemented using the practical P+resonant compensator as expressed in (7.2).

To stabilize the system, an inner charge-model is added to force the filter inductor charge, defined as $Q = \int I_L dt$ where I_L is the current through the DVR filter inductor, to track the reference charge output Q_{ref} of the flux regulator. The calculated charge error is then fed to the charge regulator in a-b-c frame with transfer function shown in (7.10):

$$G_{Charge}(s) = k_{Ch} \frac{s}{1 + (s/N)} \quad (7.10)$$

which is actually a practical form of the derivative compensator, where the added pole is used for limiting the regulator gain to N at high frequencies to prevent noise amplification. To further avoid the possible filter inductor current measurement noise amplification by the differentiation, the derivative term, $\frac{s}{1 + (s/N)}$, of charge loop compensator is moved to the front of charge loop (after the flux regulator) as shown in Figure 7.39, by acting only on the control signal (flux regulator output). The integral term added on the filter inductor current can then be removed correspondingly. As a result, the charge loop is more robust to measurement noises and more computational efficient with three integrations of filter inductor currents removed. An improvement of the charge regulator performance is therefore obtained compared to that in Chapter 5.

With the designed control scheme and flux and charge regulators as shown in Figure 7.39, The open-loop bode plot is drawn in Figure 7.40 with $k_p = 0.4$, $2k_i = 150$, $\omega_0 = 314 \text{ rad/sec}$ and $N = 1000$. The open-loop response shows a significant gain at the fundamental frequency, which ensures nearly zero steady-state error. Also shown in Figure 7.40 is that the final flux control loop exhibits a band pass filter like characteristic, with good attenuation of the low frequency measurement DC offset and high frequency switching noises as well as filter LC resonance. A phase margin of 59.8 deg and gain margin of 11.9 dB is obtained, which ensures good stability of the overall control scheme.

Figure 7.40. Bode plot of flux open loop.

7.4.5 Experimental verification under three-phase short circuit

As mentioned, the short circuit situation testing at 10 kV is impossible with the very limited capacity of AC supply (15kV), and the DVR injection voltage capacity (about 50%). Therefore the experiment has to be run at 3 kV. DVR is controlled to act like a virtual inductance with value $L_0 = 150$ mH per phase at DVR side of the injection transformer.

The first experiment is run for the symmetrical downstream fault. A three-phase short circuit is created across the load (16.5Ω) at the downstream side of the transformer from $t = 160$ ms and it lasts for 4.5 cycles. The load voltages (at high voltage side of step-down transformer) shown in Figure 7.41 are nearly zero during the fault, because almost all the voltage drop is across the DVR. The DVR reacts to the fault (after detection of an over current) by injecting voltages in quadrature with the fault current as shown in Figure 7.42. The controlled fault currents shown in Figure 7.43 comprise of DC component and the symmetrical AC component. The DC component causes the short circuit current to be asymmetrical and the decay of the DC component depends on the X/R ratio of the circuit between the source and the fault. In the experiment, DC component of the short circuit current decays in several cycles due to the large system X/R ratio introduced by the virtual inductance during the fault.

As expected, the PCC voltage is resorted, as can be seen from Figure 7.44, by limiting the fault currents. Therefore the loads on the other parallel feeders connected to PCC will not be affected. Figure 7.45 shows the real and reactive power injected by DVR. By controlling the DVR as a virtual inductance, the real power absorption becomes nearly zero, which, together with DVR injected voltages (Figure 7.42) and limited line currents (Figure 7.43), validate the effectiveness of flux-charge model control method developed in Chapter 5.

Figure 7. 41. Load voltages during three-phase short circuit.

Figure 7. 42 DVR injected voltages during three-phase short circuit.

Figure 7. 43. Line currents (DVR side) during three-phase short circuit.

Figure 7. 44. PCC voltages during three-phase short circuit.

Figure 7. 45. Real and reactive power injected by DVR during three-phase short circuit.

7.4.6 Experimental verification under single-phase short circuit

The unsymmetrical downstream fault is also tested in the experiment by creating a single-phase short circuit across the load from $t = 160$ ms (and lasts for about 3.5 cycles). Propagated to high voltage side of the step-down transformer, the load voltages are as shown in Figure 7.46. The DVR injected voltages and limited short circuit line currents are displayed in Figures 7.47 and 7.48 respectively. Again, the fault currents are unsymmetrical with a slow decay of DC component. AC components of line currents are unbalanced in this case due to the unbalanced short circuit fault but the current magnitude is effectively limited by the DVR. PCC voltages are unaffected as illustrated in Figure 7.49. Finally the nearly zero real power absorption shown in Figure 7.50 minimizes the stress on DVR energy storage device. Also noticed from these figures is that longer recovery time from a downstream fault (50 ms) is used in unsymmetrical fault to eliminate the effects of oscillating load voltage magnitude due to the unbalanced effects.

Figure 7. 46. Load voltages during single-phase short circuit.

Figure 7. 47 DVR injected voltages during single-phase short circuit.

Figure 7. 48. Line currents (DVR side) during single-phase short circuit.

Figure 7. 49. PCC voltages during single-phase short circuit.

Figure 7. 50. Real and reactive power injected by DVR during single-phase short circuit.

7.5 Investigation and Improvement of Transient Response

For typical inverter and filter topology, the inverter filter circuit (LC filter or LCL filter) designed to eliminate the high frequency inverter switching noises, would introduce a lightly damped plant model and excite LC resonance under a sudden change of reference. Widely used nonlinear loads, with high frequency harmonic currents around the LC filter cutoff frequency, would continuously excite the LC resonance. To suppress the transient LC resonance, either passive damping methods [83] (using additional resistance to damp the resonance with increased system losses) or active damping methods [84-86] (damping the resonance by control or virtual resistance with more complex algorithms) have been adopted for different implementations.

For conditioning the supplied power and damping these high frequency oscillations simultaneously, an investigation of the transient behaviors is carried out. Different classical control schemes and their effect on the oscillation attenuation are studied. An effective and simple resonance damping method is proposed by employing closed loop (single-loop or multi-loop) control and an embedded two-step posicast controller. By inserting a posicast controller into the feedback control path, the lightly damped system can be successfully compensated with reduced sensitivity to parameter variations [77-79]. It is commented here that the proposed method is applicable to both the shunt and series inverters used for microgrid voltage conditioning, although it is only designed and implemented on a series inverter (DVR) in this chapter.

The proposed transient improvement method is extensively tested on the medium voltage DVR system. DVR transient behaviors mainly occur at the start of a voltage sag or during the recovery from a voltage sag. Nonlinear loads would also excite the filter LC resonance even during the steady state compensation. To verify the proposed transient improvement method thoroughly, different control schemes and various loading conditions (linear and nonlinear loads) are tested in experiments on the 10kV DVR system.

7.5.1 Resonance damping effects by different control schemes

For inverter output voltage regulation, different control schemes have been proposed, e.g. single-loop voltage control, feedforward and feedback control [68, 74] (Figure 7.51(a)), multi-loop control with an inner current loop and outer voltage loop [75, 76] (Figure 7.51(b)), etc. A brief discussion of different control schemes for DVR implementation with a focus on their effectiveness for the filter LC resonance damping is presented in this subsection.

7.5.1.1 Single voltage loop control

Figure 7.51. Control schemes of (a) single-loop feedback or feedforward+feedback, (b) double-loop control.

Single voltage loop control method (Figure 7.51(a)) is commonly used to save extra sensors and due to its simple controller implementation, however it still could maintain the ability of reference voltage tracking and satisfactory steady-state performance. But the conflicts between transient and steady-state performance is serious, since larger controller gain is required for good steady-state performance, but this large control loop gain would result in unacceptable transients and even would lead the system to be unstable. If a small gain is used to obtain sufficient stability margins, the steady-state error may become significant.

A possible solution of this conflict is to adopt a P+resonant controller for the voltage regulation. A practical form of the P+resonant controller is shown in (7.2). With a large gain at the fundamental frequency (by selecting a large k_I), the P+resonant controller therefore has the ability to regulate the fundamental signal with very good steady-state performance. Furthermore, this controller can easily ensure a stable system with very small gains at all the other frequencies (by using a small k_P).

Bode plot of a single voltage loop control of DVR with P+resonant voltage controller is illustrated in Figure 7.52. It can be seen that the system has good tracking of a reference solely at 50 Hz, but the transient response is slow due to the limited proportional gain k_P required for system stability which results in a extremely narrow bandwidth. Also a resonance peak caused by the LC filter is noticeable.

To increase the transient response, a feedforward loop is often added from the reference signal to the input of PWM modulator (Figure 7.51(a)) [68, 74]. As seen from Figure 7.52, the bandwidth is obviously increased by feeding forward the DVR voltage reference. But the drawback is also obvious as illustrated, where the LC resonance becomes more serious.

Figure 7.52. Bode plot of single voltage loop control with and without reference feedforward ($k_p=0.0125$, $2k_f=30$, $\omega_{cut}=5$. feedforward gain $k_f=1$).

7.5.1.2 Multi-loop control

To have a system with both good transient and steady-state performances, a multi-loop control can be used, with an inner current loop for ensuring fast response as well as good attenuation of the filter LC resonance peak. Although a larger current controller gain, k_C , would introduce more damping to the system, the value of k_C is always limited as discussed earlier in this chapter.

Figure 7.53 shows bode magnitude plots of double-loop control with an inner current loop (feeding back filter inductor current I_f or filter capacitor current I_C) with proportional current controller k_C , and an outer voltage loop with P+resonant controller. Much better transient as well as steady-state performance is obtained by the double-loop control comparing to the single voltage loop method. But a resonance peak is not completely compensated due to the limited current controller gain k_C .

Different current feedback variables also affect the resonance attenuation ability. As illustrated in the zoomed-in view of Figure 7.53, the filter inductor current provides more damping for the system than the filter capacitor current does. This is because feeding back the filter inductor current gives larger overall current loop gain when same proportional

controller value k_C is used for both inductor current and capacitor current feedback methods. Although the difference between inductor and capacitor current feedbacks is not so obvious for the LC filter resonance damping shown Figure 7.53, the inductor current feedback exhibits significant advantages under a resonant system with capacitive load as discussed in Chapter 6.

Figure 7.53. Bode plot of double-loop control with different inner current feedback variables (voltage controller $k_P=0.5$, $2k_I=400$, $\omega_{cut}=5$, current controller $k_C=1.2$).

7.5.2 Proposed control strategy for transient improvement

As discussed in Section 7.5.1, both single voltage loop control and double-loop control of DVR would experience the transient LC oscillations, with the double-loop control exhibiting better performance. To further improve the transient behaviors, a two-step posicast controller is proposed to use within the closed-loop control path of either the single voltage loop control or double-loop control as shown in Figure 7.54(a) and (b). The posicast controller is used to specially eliminate the oscillatory effects caused by the LC filter.

Figure 7.54. Two-step posicast controller embedded in (a) single-loop feedback and reference feedforward control, (b) double-loop control.

7.5.2.1 Two-step posicast controller

As the name implies, the two-step posicast controller functions to split up a step input command into two segments of steps. The second step response cancels the system's oscillatory effect excited by the first step. This posicast controller is proposed to use within a feedback control loop with reduced sensitivity in [77-79], where it is called "half-cycle" posicast.

Figure 7.55 illustrates the principle of two-step posicast control. It can be seen that a unit step is separated into two steps with the first one (with magnitude M_1) leading the second (with magnitude $1-M_1$) by a time T_d . Controlled properly, these two step responses could cancel each other's oscillations and result in a fast and smooth step command response.

The magnitude M_1 of the first step and the transfer function of the two-step posicast controller is expressed in (7.11) and (7.12) respectively.

Figure 7.55. Two-step posicast controller.

$$M_1 = \frac{1}{1 + \delta} \quad (7.11)$$

$$G_{stp} = \frac{1}{1 + \delta} + \frac{\delta}{1 + \delta} e^{-sT_d} \quad (7.12)$$

where δ is the lightly damped system's step response overshoot and T_d is half of the resonance period. By separating a single unit step command into two using (7.11) and (7.12), the lightly damped system transient terms become zero after the second step is applied. A step response example is shown in Figure 7.56, where it can be seen that when the system response of first step command reaches its peak value, the second step command is added. The system response to second step has the same oscillatory effect but in the opposite direction and could therefore cancel the oscillating behavior excited by the first step command, resulting in a fast and smooth system response with specific settling time of T_d and without overshoot.

Frequency domain analysis of the two-step posicast controller G_{stp} is drawn in Figure 7.57, where the posicast controller exhibits multiple-notch filter characteristic with infinite number of zeros spaced at the odd multiples of the system natural damped frequency. The first pair of zeros functions to cancel the dominant pair of poles introduced by the LC filter. Note that with limited high frequency gains, the posicast controller is more robust to high frequency noises compared to model inversion pole cancellation which typically exhibits noise sensitivity due to the increasing gains at high frequency [77]. However inaccurate knowledge of the plant dominant poles will result in residual oscillation for posicast. To mitigate the imperfect compensation effects, the posicast controller can be

inserted within a feedback closed loop to obtain more robust responses. Sensitivity analysis of posicast in feedback loop can be found in [77].

Figure 7. 56. Two-step posicast response, from top to bottom: first, second, and summation steps.

Figure 7. 57. Bode diagram of two-step posicast controller ($T_d=0.000785s$, $\delta=98.1\%$).

To determine the delay time (T_d) and the overshoot (δ) of Posicast controller used for DVR implementation, the DVR model (same as a typical inverter with LC output filter topology) is first expressed in (7.13):

$$G_{DVR} = \frac{1}{L_f C_f s^2 + R_f C_f s + 1} \quad (7.13)$$

where L_f , R_f and C_f are the filter inductance, filter resistance and filter capacitance respectively. For the second order plant in (7.13), the damping ratio ζ , and plant natural undamped frequency ω_n can be calculated by:

$$\zeta = \frac{R_f}{2} \sqrt{\frac{C_f}{L_f}} \quad (7.14)$$

$$\omega_n = \frac{1}{\sqrt{L_f C_f}} \quad (7.15)$$

Subsequently, the resonant frequency (natural damped frequency) can be computed by $\omega_r = \omega_n \sqrt{1 - \zeta^2}$. The delay time (T_d) and the overshoot (δ) are finally obtained as expressed in (7.16) and (7.17) (DVR plant parameters are listed in Table 7.1):

$$T_d = \frac{\pi}{\omega_r} = \frac{\pi}{\sqrt{\frac{1}{L_f C_f} - \frac{R_f^2}{4L_f^2}}} \quad (7.16)$$

$$\delta = e^{-\zeta \pi / \sqrt{1 - \zeta^2}} = e^{-R_f \pi \sqrt{C_f} / \sqrt{4L_f - R_f^2 C_f}} \quad (7.17)$$

For digital implementation, the form of two-step posicast controller in (7.18) should be discretized to (7.18):

$$G_{Zisp} = \frac{1}{1 + \delta} + \frac{\delta}{1 + \delta} z^{-\text{int}(T_d / T_s)} \quad (7.18)$$

where T_s is the sampling frequency and $\text{int}(\)$ means the integer number of delayed samples. This discrete form of posicast controller implies the accuracy of posicast compensation is dependent on the ratio of sampling frequency to system resonant frequency. A higher sampling frequency or a lower resonant frequency ensures more sample delays and thus more accurate delay time for the second step command. For this work, where the LC filter resonant frequency is 637 Hz and the DSP sampling frequency is 5 kHz, the number of delayed samples is 4 with a delay time deviation of $\Delta t = 0.015\text{ms}$. The effect of delay time deviation on digital implementation will be discussed in the next two subsections for single-loop and double-loop feedback implementations respectively.

A three-step method is also proposed in [80]. As shown in Figure 7.58, for a reference unit step change occurs at t_0 , two additional unit step changes (a negative step and a

positive step) are added at t_1 and t_2 respectively to cancel the oscillatory effect introduced by the first reference unit step. Similarly it also has two parameters t_1 and t_2 , which are $1/6$ and $1/3$ of the resonance period respectively. The settling time using this method ($1/3$ of resonance period) is therefore faster compared to the two-step posicast ($1/2$ of resonance period). But the resolution problem for digital implementation would be more serious with the three-step method since both two parameters are related to the time delay and the delay times are smaller (compared to the two-step posicast with parameters δ and T_d) unless high sampling frequency is available. Therefore the three-step method is not considered in this work.

Figure 7. 58. Three-step method.

7.5.2.2 Single voltage loop with embedded posicast controller

The frequency response of single voltage loop feedback plus reference feedforward control with embedded posicast controller is illustrated in Figure 7.59. The calculated value perfectly compensates the resonance notch in the bode plot. But due to 5 kHz sampling frequency used in experiments, a delay time of $T_{dI} = 0.0008\text{s}$ (4 samples delay) instead of the calculated $T_d = 0.000785\text{s}$ has to be used. The discrete implementation gives only very slight distortion for resonance compensation as shown in Figure 7.59. Compared to the control scheme without posicast (Figure 7.52), the improvement is significant with a resonant peak reduction from 37dB to nearly zero. Note that the high frequency attenuation characteristic of the original control scheme is not affected by the additional posicast control as shown in Figure 7.59.

Figure 7. 59. Bode plot of single voltage loop feedback plus reference feedforward with posicast controller ($T_d = 0.000785\text{s}$, $T_{d1}=0.0008\text{s}$, $\delta=98.1\%$).

7.5.2.3 Double-loop with posicast controller

Figure 7.60 shows the frequency response of double-loop control with embedded two-step posicast controller. Again, the posicast controller with calculated value $T_d = 0.000785\text{s}$ would cancel the LC resonance completely. For experiment implementation with $T_{d1} = 0.0008\text{s}$, less compensation distortions can be observed from Figure 7.60 compared to single voltage feedback in Figure 7.59. Furthermore, this distortion is outside the control bandwidth and will not cause any problem during practical implementation. Similarly, compared to the double-loop control without posicast controller in Figure 7.53, the high frequency roll off characteristic is not affected by the embedded posicast controller which introduces no high frequency amplification (Figure 7.57).

Figure 7. 60. Bode plot of double-loop feedback with posicast controller ($T_d=0.000785\text{s}$, $T_{d1}=0.0008\text{s}$, $\delta=98.1\%$).

7.5.3 Experimental verification of single-loop with/without posicast controller under linear load

The first experiment is run with linear load ($67\ \Omega$). The PCC voltage drops to 70% of its nominal value from 40ms to 140ms (5 fundamental cycles). Figures 7.61 to 7.66 illustrate the performance of single voltage loop feedback and reference feedforward with and without the two-step posicast controller. As observed from the DVR injected voltages in Figure 7.61 and load voltages in Figure 7.62, the steady state performance with and without posicast controller is similar under linear load, but an improvement of sag start and recovery transients is obtained with the posicast controller. Zoomed-in views of the startup and recovery transients in Figures 7.63 and 7.64 clearly show well damped LC resonance with posicast control, which results in the improvement of load voltage transient as illustrated in Figures 7.65 and 7.66 for sag startup and recovery respectively. As discussed in Section 7.5.2.2, the slight deviation of delay time for posicast's second step during DSP implementation does not introduce any noticeable effect in the experiment.

Figure 7. 61. DVR injected voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 62 Load voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 63. Startup transient zoom-in view of DVR injected voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 64. Recovery transient zoom-in view of DVR injected voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 65. Startup transient zoom-in view of load voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 66. Recovery transient zoom-in view of load voltages with single-loop feedback and feedforward (linear load): (a) without posicast control and (b) with posicast control.

7.5.4 Experimental verification of double-loop with/without posicast controller under linear load

The performance of double-loop feedback control with and without posicast controller is shown in Figures 7.67 to 7.70. As expected, compared to the single voltage loop feedback scheme, the double-loop feedback control has better transient performance during startup and recovery as shown in Figures 7.67 and 7.68. Transient improvement introduced by

posicast controller is still noticeable as shown in the startup zoomed-in views in Figures 7.69 and 7.70 for the DVR injected voltages and load voltages respectively.

Figure 7. 67. DVR injected voltages with double-loop control (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 68 Load voltages with double-loop control (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 69. Startup transient zoom-in view of DVR injected voltages with double-loop control (linear load): (a) without posicast control and (b) with posicast control.

Figure 7. 70. Startup transient zoom-in view of load voltages with double-loop control (linear load): (a) without posicast control and (b) with posicast control.

7.5.5 Experimental verification of single-loop with/without posicast controller under nonlinear load

The DVR performance with nonlinear load is also investigated. The nonlinear load is a diode rectifier bridge with a capacitor bank (200 μ F) and resistive load (80 Ω) connected in

parallel. Similarly, the PCC voltage drops to 70% of its nominal value from 40ms and lasts for 5 cycles.

Again the performance with single voltage loop feedback and reference feedforward with and without posicast controller is first investigated with waveforms shown in Figures 7.71 to 7.76. Under nonlinear load, the posicast controller can improve not only the transient behavior but also the steady state performance as seen in DVR injected voltages and load voltages in Figures 7.71 and 7.72 respectively. This is because the nonlinear load drawing high frequency harmonic currents will introduce continuous excitation of the LC resonance. The posicast control method which aims to damp the LC resonant effect, can therefore improve the system transient as well as steady state performance under nonlinear loading condition as clearly shown in the zoomed-in views of DVR injected voltages in Figures 7.73 and 7.74 and load voltages in Figure 7.75. The frequency spectra analysis in Figure 7.76 reveals that the high frequency harmonics (11^{th} , 13^{th} and 17^{th}) around the DVR LC resonant frequency (637 Hz) is effectively reduced by the two-step posicast controller, resulting in a lower THD (4.8%) compared to that without posicast control (THD=7.6%).

Figure 7. 71. DVR injected voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.

Figure 7. 72. Load voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.

Figure 7.73. Startup zoom-in view of DVR injected voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.

Figure 7.74. Recovery zoom-in view of DVR injected voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast.

Figure 7.75. Recovery zoom-in view of load voltages with single-loop feedback and feedforward (nonlinear load): (a) without posicast and (b) with posicast control.

Figure 7.76. Frequency spectra of DVR injected voltage with single-loop feedback and feedforward (nonlinear load): (a) without posicast control and (b) with posicast control.

7.5.6 Experimental verification of double-loop with/without posicast controller under nonlinear load

The performance of double-loop control is also investigated in the experiment with nonlinear load. The DVR injected voltages and load voltages are shown in Figures 7.77 and 7.78. Similarly, the posicast control method improves both the transient and steady state performance, which is clearly shown in the DVR injected voltage zoomed-in view in Figure 7.79. Again, the frequency spectra analysis in Figure 7.80 shows a reduction of

high frequency harmonics as well as a decrease of THD (from 5.8% to 4.9%) due to the embedded two-step posicast controller.

Figure 7.77. DVR injected voltages with double-loop control (nonlinear load): (a) without posicast control and (b) with posicast control.

Figure 7.78. Load voltages with double-loop control (nonlinear load): (a) without posicast control and (b) with posicast control.

Figure 7.79. Startup zoom-in view of DVR injected voltages with double-loop control (nonlinear load): (a) without posicast and (b) with posicast.

Figure 7.80. Frequency spectra of DVR injected voltage with double-loop control (nonlinear load): (a) without posicast and (b) with posicast.

7.6 Discussion

In this chapter, selected works in previous chapters are tested on a series grid-interfacing inverter (DVR) at 10 kV medium voltage level. The P+resonant controller, H_∞ control method developed in previous chapters are extensively tested during medium voltage experiments with their effectiveness for inverter control at stationary frame further validated. Flux-charge model based current limiting algorithm developed in Chapter 5 is also successfully implemented at the medium voltage level series inverter, with its practicality verified under three-phase or single-phase short circuit conditions. A transient improvement method for the inverter output voltage regulation is also developed in this chapter by inserting a two-step posicast controller into a closed loop control path (single-loop or multi-loop), and tested at medium voltage level.

Note that except for the fault current limiting algorithms, which is specially developed for series inverter as discussed in Chapter 5, all the other control methods investigated in this chapter including the P+resonant controller, H_∞ controller and transient improvement methods are equally applicable to the shunt inverter for DG system voltage regulation as discussed in previous chapters, although they are only tested on the series inverter in this chapter.

Chapter 8

Conclusions and Recommendations

8.1 Conclusions

As a systematic organization of DG systems, a microgrid can have more power capacity and control flexibilities to fulfill system reliability and power quality requirements, in addition to all the inherited advantages of a single DG system. Aim of research in this thesis is to develop power conditioners and controllers for microgrids and exploit the potential benefits the microgrid can provide to the utility and customers.

After an introductory survey of DG systems and microgrid concept in Chapter 2, a multi-functional unified controller is proposed in Chapter 3 for use with each DG in the microgrid. This controller would realize all the basic functions to make a microgrid operational. With an inner voltage and current control block, the DG system output voltage can be well regulated. The external real and reactive power control blocks are designed based on “plug and play” characteristics with control information only locally available. This ensures the unified controller would control power flow in grid-connected mode of operation and share the changed real and reactive power demands automatically without communication between the DG systems when the microgrid islands. A synchronization algorithm is also incorporated to this unified controller for smooth reconnection of the microgrid and the utility system. The presented controller would respond fast, allowing the controlled microgrid to transit smoothly between the grid-connected and islanding modes without disrupting critical loads connected to it.

With further consideration of the utility power quality problems and their impacts on the microgrid, a three-phase three-wire dual-inverter power quality compensator for the microgrid is proposed in Chapter 4 for mitigation of effects resulting from PCC voltage unbalance. This compensator is comprised of a shunt and a series three-leg inverter. Functionally, the shunt inverter is controlled to regulate both positive- and negative-

sequence voltages and maintain a set of balanced, distortion-free voltages within the microgrid as well as provide all the other basic functions of the microgrid. To complement, the series inverter is controlled to inject negative-sequence voltages in series to balance the line currents, generating zero real and reactive power during compensation. As a result, both the quality of voltage within the microgrid and the quality of currents flowing between the microgrid and utility system are enhanced by the proposed microgrid compensator.

Considering the possible four-wire configuration of a microgrid system, a four-wire version of the proposed grid-interfacing dual-inverter power quality compensator is also designed using two four-leg inverters. The functions of this four-wire microgrid compensator are similar to the three-wire version, but with capability to regulate the zero-sequence component with an additional inverter leg. Therefore, all the unwanted negative- or zero-sequence voltage or current in the microgrid resulting from PCC voltage unbalance or load unbalance would be compensated. The worst case utility voltage unbalance of 10% negative-sequence and 10% zero-sequence components are assumed when testing the three-wire or four-wire compensators.

Current-limiting algorithms are proposed in Chapter 5 and integrated within proposed dual-inverter microgrid compensators to protect the microgrid from large fault currents during utility voltage sags. Two methods are proposed, named as RL feedforward and flux-charge-model feedback algorithms. The RL algorithm functions by controlling the series inverter (in the microgrid power quality compensator) to insert a large virtual RL impedance along the distribution feeder to limit the line currents and damp transient oscillations with a non-zero active power circulating through the series and shunt inverters. Furthermore, RL algorithm can be optimized by tuning the R/L ratio, such that the voltage injected by the series inverter, and hence the voltage rating of the DC link capacitor, are minimized. On the other hand, the flux-charge algorithm, with an outer flux-model and an inner charge-model, is conceptually an extension of the existing flux-model control with added robustness. The flux-charge algorithm inserts only a virtual inductive impedance with zero active power absorption and relies on its closed-loop control tuning to damp transient oscillations. A typical worst-case voltage sag of 50%

voltage drop and -60° phase jump is assumed in the design procedures. Both the proposed methods would effectively protect the microgrid by limiting the fault currents during this typical worst-case utility voltage sag.

Being a larger system also means that the microgrid would easily be disturbed by the numerous power devices connected within its vicinity. In particular, the switching of PFC capacitors, widely used for improving system efficiency, can cause system parameter variations, and hence performance degradation of the designed DG controller. The presence of PFC capacitors can also result in high resonant voltages and currents. A detailed study of the scenario of a microgrid with PFC capacitor installed is conducted in Chapter 6, which reveals the effective inverter filter capacitance will change when a PFC capacitor is connected to a local load of a DG system. Also, resonance would occur in islanding mode of the microgrid operation when a PFC capacitor is installed in the load at PCC.

An H_∞ controller is designed for robust control of microgrid voltage under system parameter variations. By properly selecting the weighting functions, the synthesized H_∞ controller exhibits similar performance as a P+resonant controller by having high gains at the vicinity of line frequency and thus small steady state error, while providing more explicit robustness in face of the filter capacitance variation. For the resonance situation, a thorough analysis is carried out to show that inner filter inductor current feedback method is more effective for the resonance damping than filter capacitor current feedback with the virtue of having a higher feedback gain. A further damping method is also proposed, which employs the proposed dual-inverter compensator. The series inverter is controlled as a virtual resistor only at harmonic frequencies without affecting the fundamental power flow.

A transient improvement method for the inverter output voltage regulation is also developed in this work. For typical inverter plus filter topology, the filter circuit aiming to eliminate the high frequency inverter switching noises, would introduce a lightly damped plant model and initiate LC resonance under a sudden change of reference. The widely used nonlinear loads, with high frequency harmonic currents around the LC filter cutoff

frequency, would continuously excite the LC resonance. An effective and simple resonance damping method is proposed by employing closed loop (single-loop or multi-loop) control and an embedded two-step posicast controller. As a general control algorithm, the proposed method is applicable to both the shunt and series inverters used for microgrid voltage conditioning.

All the proposed controllers and control algorithms are tested experimentally. After the control parameters are fine tuned in analysis and off-line simulations, the proposed microgrid controllers and compensators are implemented on a low voltage laboratory emulated microgrid prototype. Close match of the simulation results and experimental results verifies this research work.

A real-time implementation platform is also designed. This platform arrangement is commonly referred to as “hardware-in-the-loop-simulation” where a hardware controller is physically integrated within a plant (consisting of the utility grid, microgrid and interfacing inverters) simulated using the RTDS simulator, to test the controller performance in real time. It gives more accurate results than offline simulation, and is preferably performed after offline simulation but before experimental investigation, as a sequential procedure for testing controller performance in complex plants like power systems.

Part of this work is further tested in a high voltage laboratory. The proposed P+resonant controller and H_{∞} controller (with comparative experimental testing approach), fault current limiting algorithm and the two-step posicast transient improvement method have been implemented on a 10kV medium voltage level grid-interfacing series voltage source inverter in the high voltage laboratory. The testing results as shown in Chapter 7 further prove the good performance and robustness of the proposed control algorithms.

8.2 Recommendations

Several topics, worthwhile further in-depth investigation, have not been pursued in this work. Interesting research topics recommended for future study are given in this section.

Microgrid interfaces both AC and DC networks. In this work the control algorithms are developed mainly based on the consideration of AC network and assuming the DC side as ideal. One possible research topic is the analysis of DC network model. This includes:

- Development of models of micro-source, such as microturbine, wind turbine etc., and incorporate the micro-source models in to the microgrid system for the controller design.
- Take into account the energy storage device dynamics into the microgrid model or control algorithms development.

With consideration of utility voltage distortion and its impact on microgrid, the issues of utility voltage unbalance and voltage sag are addressed and new microgrid power quality compensators are proposed to compensate these power quality problems. But other utility power quality problems and their impacts on microgrid are also worthwhile for investigation. Such as:

- Utility voltage swell, which can cause large line current flow between the microgrid and the utility. Proposed microgrid compensator should be able to protect the microgrid during a voltage swell using the fault current limiting algorithms. But swell occurrence and recovery detection algorithms need to be developed.

- Utility voltage harmonics can cause harmonic voltage in the microgrid, line heating or even will excite system resonance when the harmonic frequency coincides with the system natural frequency. The consideration of harmonic voltage is also a recommended research topic.

Load disturbances are another issue that should be looked into. Unbalanced loads can be properly controlled by the shunt inverter in the proposed microgrid compensator. PFC capacitor connected microgrid is investigated in this work. Some impacts from nonlinear loads are also addressed and a transient improvement method is proposed to eliminate or mitigate the continuous excitation of inverter output filter LC resonance caused by nonlinear loads. Further research should investigate the other possible impacts caused by nonlinear loads, such as the resulted harmonic currents, voltages or system resonance in the microgrid. Motor loads, especially the start of a motor is also worth for further research.

Besides the above mentioned topics, a protection scheme for microgrids with consideration of a fault inside the microgrid is also an important research area.

Author's Publications

IEEE Transactions

- [1] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "Design, analysis and real-time testing of controllers for multibus microgrid system," *IEEE Trans. Power Electron.*, vol. 19, pp. 1195-1204, Sep. 2004.
- [2] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "A Grid-Interfacing Power Quality Compensator for Three-Phase Three-Wire Microgrid Applications," *IEEE Trans. Power Electron.*, accepted for publish, 2005.
- [3] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "Microgrid Power Quality Enhancement Using A Three-Phase Four-Wire Grid-Interfacing Compensator," *IEEE Trans. Ind. Applicat.*, vol. 41, pp. 1707-1719, Nov-Dec. 2005.
- [4] D. M. Vilathgamuwa, P. C. Loh, and Y. W. Li, "Protection of Micro-Grids during Utility Voltage Sags," *IEEE Trans. Ind. Electron.*, accepted for publish, 2005.
- [5] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "Robust Control Scheme for A Microgrid with Shunt-Connected PFC Capacitors," *IEEE Trans. Ind. Applicat.*, under review, 2005.
- [6] Y. W. Li, F. Blaabjerg, D. M. Vilathgamuwa, and P. C. Loh, "Design and Comparison of High Performance Stationary-frame Controllers for DVR Implementation," *IEEE Trans. Power Electron.*, accepted for publish, 2006.
- [7] Y. W. Li, D. M. Vilathgamuwa, F. Blaabjerg, and P. C. Loh, "A Robust Control Scheme for Medium Voltage Level DVR Implementation," *IEEE Trans. Ind. Electron.*, revised version under review, 2006.
- [8] Y. W. Li, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, "Investigation and Improvement of Transient Response of DVR at Medium Voltage Level," *IEEE Trans. Ind. Applicat.*, under review, 2006.

IEEE Conference Proceedings

- [9] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "A grid-interfacing power quality compensator for three-phase three-wire micro-grid applications," in *Proc. IEEE-PESC'04*, 2004, pp. 2011-2017.
- [10] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "Microgrid power quality enhancement using a three-phase four-wire grid-interfacing compensator," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 2004, pp. 1439-1446.
- [11] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "Robust Control Scheme for A Microgrid with Shunt-Connected PFC Capacitors," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 2005, pp. 2441-2448.
- [12] Yun Wei Li, Frede Blaabjerg, D. Mahinda Vilathgamuwa, and Poh Chiang Loh, "Design and Comparison of High Performance Stationary-frame Controllers for DVR Implementation," in *Conf. Rec. IEEE-APEC'06*, 2006, pp. 912-918.
- [13] Yun Wei Li, Poh Chiang Loh, Frede Blaabjerg, and D. Mahinda Vilathgamuwa, "Investigation and Improvement of Transient Response of DVR at Medium Voltage Level," in *Conf. Rec. IEEE-APEC'06*, 2006, pp. 1074-1080.
- [14] Yun Wei Li, D. Mahinda Vilathgamuwa, Poh Chiang Loh, and Frede Blaabjerg, "A Dual-Functional Medium Voltage Level DVR to Limit Downstream Fault Currents," in *Proc. IEEE-PESC'06*, 2006, in press.

Bibliography

- [1] R. Tirumala, N. Mohan, and C. Henze, "Seamless transfer of grid-connected PWM inverters between utility-interactive and stand-alone modes," in *Proc. IEEE-APEC*, 2002, Vol. 2, pp. 1081–1086.
- [2] Y. Zoka, H. Sasaki, N. Yorino, K. Kawahara, and C. C. Liu, "An interaction problem of distributed generators installed in a MicroGrid," in *Proc. IEEE International Conference on Electric Utility Deregulation, Restructuring and Power Technologies, (DRPT 2004)*, Apr. 2004, Vol. 2, pp. 795-799.
- [3] M.T. Doyle, "Reviewing the impacts of distributed generation on distribution system protection," in *Proc. IEEE Power Engineering Society Summer Meeting*, 2002, pp. 103-105.
- [4] P. P. Barker and R. W. De Mello, "Determining the impact of distributed generation on power systems. I. Radial distribution systems," in *Proc. IEEE Power Engineering Society Summer Meeting*, 2000, Vol. 3, pp 1645-1656.
- [5] R. C. Dugan and T. E. McDermott, "Operating conflicts for distributed generation on distribution systems," in *Proc. Rural Electric Power Conference*, 2001, pp. A3/1-A3/6.
- [6] IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems IEEE Std 1547-2003 ,2003, pp, 0_1-16
- [7] R. Lasseter, "Microgrids," in *Proc. IEEE Power Engineering Society Winter Meeting*, vol. 1, 2002, pp. 305–308.
- [8] R. Lasseter, A. Akhil, C. Marnay, J. Stephens, J. Dagle, R. Guttromson, AS Meliopoulos, R. Yinger, and J. Eto, "White Paper on Integration of Distributed Energy Resources – The CERTS MicroGrid Concept," Office of Power Technologies of the US Department of Energy, Contract DE-AC03-76SF00098, Apr. 2002.
- [9] R. Lasseter and P. Piagi, "Providing premium power through distributed resources," in *Proc. 33rd Annual Hawaii International Conference on System Sciences*, Jan 4-7, 2000, pp. 1437–1445.

-
- [10] C. L. Smallwood, "Distributed generation in autonomous and nonautonomous microgrids," in *Proc. Rural Electric Power Conference*, May 5-7 2002 pp. D1-D1_6.
- [11] D. Georgakis, S. Papathanassiou, N. Hatziargyriou, A. Engler, and C. Hardt, "Operation of a prototype microgrid system based on micro-sources quipped with fast-acting power electronics interfaces," in *Proc. IEEE – PESC'04*, June 20-25, 2004, vol. 4, pp. 2521-2526.
- [12] R. Lasseter and P. Piagi, "Microgrid: a conceptual solution," in *Proc. IEEE – PESC'04*, June 20-25, 2004, vol. 6, pp. 4285 – 4290.
- [13] T. Ackermann, G. Andersson, and L. Soder, "Distributed generation: a definition," *Electric Power Systems Research*, 2001, vol. 57, pp. 195-204.
- [14] R. C. Dugan, M. F. McGranaghan, and H. W. Beaty, *Electrical Power Systems Quality*, McGraw Hill, 2002
- [15] M. H. J. Bollen, *Understanding power quality problems: voltage sags and interruptions*, New York: IEEE Press, 2000.
- [16] T. A. Smith, J. P. Mars, and G. A. Turner, "Using supercapacitors to improve battery performance," in *Proc. IEEE – PESC'02*, 2002, vol. 1, pp. 23-27.
- [17] M. H. J. Bollen, "What is power quality?" *Electric Power System Research*, vol. 66, 2003, pp. 5-14.
- [18] P. Piagi and R. Lasseter, "Industrial application of microgrids," Power System Engineering Research Center, Univ. Wisconsin, Madison, WI, 2001.
- [19] N. D. Hatziargyriou and A. P. S. Meliopoulos, "Distributed energy sources: technical challenges," in *Proc. IEEE Power Engineering Society Winter Meeting*, vol. 2, 2002, pp. 1446–1448.
- [20] N. D. Hatziargyriou and A. P. S. Meliopoulos, "Distributed energy sources: needs for analysis and design tools," in *Proc. IEEE Power Engineering Society Summer Meeting*, vol. 1, 2001, pp. 548–550.
- [21] A. P. S. Meliopoulos, "Challenges in simulation and design of microgrids," in *Proc. IEEE Power Engineering Society Winter Meeting*, vol. 1, 2002, pp. 309–314.
- [22] M. A. Redfern, O. Usta, and G. Fielding, "Protection against loss of utility grid supply for a dispersed storage and generation unit," *IEEE Trans. Power Delivery*, vol. 8, pp. 948–954, July. 1993.
- [23] K. J. P. Macken, "Control of inverter-based distributed generation used to provide premium power quality," in *Proc. IEEE – PESC'04*, 2004, vol. 4, pp. 3188-3194.
-

-
- [24] F. Katiraei, M. R. Iravani, and P. W. Lehn, "Micro-grid autonomous operation during and subsequent to islanding process," *IEEE Trans. Power Delivery*, vol. 20, pp. 248–257, Jan. 2005.
- [25] C. A. Hernandez-Aramburo, T. C. Green, and N. Mugniot, "Fuel Consumption Minimization of a Microgrid," *IEEE Trans. Ind. Applicat.*, Vol. 41, pp. 673 –681, May/Jun. 2005.
- [26] C. Marnay, F. J. Robio, and A. S. Siddiqui, "Shape of the microgrid," in *Proc. IEEE Power Engineering Society Winter Meeting*, vol. 1, 2001, pp. 150–153.
- [27] K. Brown, "Domestic supply," *IEE Review*, Vol. 51, Mar. 2005 pp. 36 – 39.
- [28] M. W. Davis, "Mini gas turbines and high speed generators a preferred choice for serving large commercial customers and microgrids. I. Generating system," in *Proc. IEEE Power Engineering Society Summer Meeting*, vol. 2, 2002, pp. 669–676.
- [29] M. W. Davis, "Mini gas turbines and high speed generators a preferred choice for serving large commercial customers and microgrids. II. Microgrids," in *Proc. IEEE Power Engineering Society Summer Meeting*, vol. 2, 2002, pp. 682–687.
- [30] O. Bailey, B. Ouaglal, E. Bartholomew, C. Marnay, and N. Bourassa, "An engineering economic analysis of combined heat and power technologies in a microgrid application," US Department of Energy, Contract DE-AC03-76SF00098, Mar. 2002.
- [31] J. D. Kueck, R. H. Staunton, S. D. Labinov, and B. J. Kirby, "Microgrid energy management system," US Department of Energy, Contract DE-AC05-00OR22725, Jan. 2003.
- [32] "Guidebook for combined heat & power," California Energy Commission, Contract No. 400-96-019, Oct. 2000.
- [33] "Market Transformation for combined heat & power systems in California," California Energy Commission, Contract No. 400-96-019, Oct. 2000.
- [34] J. A. McDowall, "Opportunities for electricity storage in distributed generation and renewables," *Transmission and Distribution Conference and Exposition*, 2001 IEEE/PES, vol. 2, 2001, pp. 1165-1168.
- [35] H. L. Willis, "Energy storage opportunities related to distributed generation," in *Proc. IEEE Power Engineering Society Summer Meeting*, vol. 3, 2000, pp. 1517–1518.

-
- [36] C. S. Hsu and W. J. Lee, "Superconducting magnetic energy storage for power system application," in *Proc. IEEE Industrial and Commercial Power System Technical Conference*, 1992, pp. 28-34.
- [37] G. Venkataramanan and M. Illindala, "Microgrids and sensitive loads," in *Proc. IEEE Power Engineering Society Winter Meeting*, vol. 1, 2002, pp. 315-322.
- [38] M. Illindala and U. Venkataramanan, "Control of distributed generation systems to mitigate load and line imbalances," in *Proc. IEEE – PESC'02*, 2002, Vol. 4, pp. 2013 –2018.
- [39] N. M. Abdel-Rahim and J. E. Quaicoe, "Three-phase voltage-source UPS inverter with voltage-controlled current-regulated feedback control scheme," in *Proc. 20th International Conference on Industrial Electronics, Control and Instrumentation 1994, IECON'94*, Vol. 1 , pp. 497 –502.
- [40] N. M. Abdel-Rahim and J. E. Quaicoe, "Analysis and design of a multiple feedback loop control strategy for single-phase voltage-source UPS inverters," *IEEE Trans. Power Electron.*, vol. 11, pp. 532-541, July 1996.
- [41] M.C. Chandorkar, D. M. Divan, and R. Adapa, "Control of parallel connected inverters in standalone AC supply systems," *IEEE Trans. Ind. Applicat.*, Vol. 29, No. 1, Jan/Feb 1993, pp. 136 –143.
- [42] A. Tuladhar, H. Jin, T. Unger, and K. Mauch, "Parallel operation of single phase inverter modules with no control interconnections," in *Proc. IEEE-APEC*, 1997, Vol. 1, pp. 94 –100.
- [43] The RTDS 3PC Manual, Revision 5, RTDS Technologies Inc. Jan. 2000.
- [44] PSCAD/ RTDS Manual Set, Revision 2, RTDS Technologies Inc. Sep. 1997.
- [45] RTI Implementation Guide, dSPACE GmbH, Technologiepark 25, D-33100 Paderborn, Germany, 1999.
- [46] A. von Jouanne and B. Banerjee, "Assessment of voltage unbalance," *IEEE Trans. Power Delivery*, vol. 16, pp. 782-790, Oct. 2001.
- [47] M. Prodanovic and T. C. Green, "Control and filter design of three-phase inverters for high power quality grid connection," *IEEE Trans. Power Electron.*, vol. 18, pp. 373-380, Jan. 2003.
- [48] Arindam Ghosh, Gerard Ledwich, Power quality enhancement using custom power devices. Kluwer Academic Publishers, 2002.
-

-
- [49] C. B. Jacobina, M. B. deR. Correa, T. M. Oliveira, A. M. N. Lima, and E. R. C. da Silva, "Current control of unbalanced electrical systems," *IEEE Trans. Ind. Electron.*, vol. 48, pp. 517–525, Jun. 2001.
- [50] T. M. Rowan and R. J. Kerkman, "A new synchronous current regulator and an analysis of a current-regulated PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. 22, pp. 678–690, July/Aug. 1986
- [51] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Trans. Ind. Applicat.*, vol. 37, pp. 601–610, Mar/Apr. 2001.
- [52] P. Mattavelli, "Synchronous-frame harmonic control for high-performance AC power supplies," *IEEE Trans. Ind. Applicat.*, vol. 37, pp. 864–872, May/Jun. 2001.
- [53] P. Heine, A. Lehtonen, and E. Lakervi, "Voltage sag analysis taken into account in distribution network design," in *Proc. IEEE Power Tech. Conf.*, 2001, 6 pp.
- [54] M. J. Ryan, R. W. De Doncker, and R. D. Lorenz, "Decoupled control of a four-leg inverter via a new 4×4 transformation matrix," *IEEE Trans. Power Electron.*, vol. 16, pp. 694–701, Sep. 2001
- [55] J. G. Slootweg and W. L. Kling, "Modeling and analyzing impacts of wind power on transient stability of power systems," *Wind Engineering*, vol. 26, No. 1, pp. 3–20, 2002.
- [56] H. Funato, T. Ishikawa, and K. Kamiyama, "Transient response of three phase variable inductance realized by variable active-passive reactance (VAPAR)," in *Proc. IEEE-APEC*, 2001, vol. 2, pp. 1281–1286.
- [57] H. Funato, K. Kamiyama, and A. Kawamura, "Transient performance of power circuit including virtual inductance realized by fully digital controlled variable active-passive reactance (VAPAR)," in *Proc. IEEE-PESC'00*, 2000, vol. 3, pp. 1195–1200.
- [58] D. Detjen, J. Jacobs, R. W. De Doncker, and H. G. Mall, "A new hybrid filter to dampen resonances and compensate harmonic currents in industrial power systems with power factor correction equipment," *IEEE Trans. Power Electron.*, vol. 16, pp. 821–827, Nov. 2001.
- [59] J. C. Wu, H. L. Jou, K. D. Wu, and N. C. Shen, "Power converter-based method for protecting three-phase power capacitor from harmonic destruction," *IEEE Trans. Power Delivery*, vol. 19, pp. 1434–1441, Jul. 2004.
- [60] Robust Control Toolbox User's Guide, the Math Work Inc., Jun. 2001.
-

-
- [61] M. Aten and H. Werner, "Robust multivariable control design for HVDC back to back schemes," *IEE Proc. Gener. Transm. Distrib.* Vol. 150 (6), pp. 761–767, Nov. 2003
- [62] H. Oloomi and B. Shafai, "Weight selection in mixed sensitivity robust control for improving the sinusoidal tracking performance," in *Proc. IEEE Decision and Control Conf*, vol 1, 2003, pp. 300 – 305.
- [63] T.-S. Lee, S.-J. Chiang, and J.-M. Chang, " H_∞ loop-shaping controller designs for the single-phase UPS inverters," *IEEE Trans. Power Electron.*, vol. 16, pp. 473-481, Jul. 2001.
- [64] M. J. Ryan, W. E. Brumsickle, and R. D. Lorenz, "Control topology options for single-phase UPS inverters," *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 493-501, Mar/Apr 1997.
- [65] D. M. Vilathgamuwa and H. M. Wijekoon, "Control and analysis of a new dynamic voltage restorer circuit topology for mitigating long duration voltage sags," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 2002, pp. 1105-1112.
- [66] M. J. Newman, D. G. Holmes, J. G. Nielsen, and F. Blaagjerg, "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 2003, pp. 1228-1235.
- [67] P. C. Tan, P. C. Loh, and D. G. Holmes, "High performance harmonic extraction algorithm for a 25 kV traction power quality conditioner," *IEE Proc. Electr. Power. Appl.* Vol. 151 (5), pp. 505–512, Sept. 2004.
- [68] J. G. Nielsen, "Design and control of a dynamic voltage restorer," *Ph. D thesis*, Aalborg Univerisity, Institute of Energy Technology, 2002. ISBN: 87-89179-42-0.
- [69] B. H. Li, S. S. Choi, and D. M. Vilathgamuwa, "Design considerations on the line-side filter used in the dynamic voltage restorer," *IEE Proc. Gener. Transm. Distrib.* Vol. 148, (1), Jan. 2001, pp. 1–7.
- [70] N. H. Woodley, L. Morgan, and A. Sundaram, "Experience with an inverter-based dynamic voltage restorer," *IEEE Trans. Power Delivery*, vol. 14, pp. 1181-1186, July. 1999.
- [71] N. H. Woodley, A. Sundaram, T. Holden, and T. C. Einarson, "Field experience with the new platform-mounted DVR," in *Proc. IEEE-PowerCon'00*, 2000, pp. 1323-1328.
-

-
- [72] W. C. Lee, T. K. Lee, C. S. Ma, and D. S. Hyun, "A fault protection scheme for series active compensators," *IEEE Trans. Power Delivery*, vol. 19, pp. 1434-1441, Jul. 2004.
- [73] S. S. Choi, T. X. Wang, and D. M. Vilathgamuwa, "A series compensator with fault current limiting function," *IEEE Trans. Power Delivery*, vol. 20, pp. 2248-2256, Jul. 2005.
- [74] J. G. Nielsen, M. J. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," *IEEE Trans. Power Electron.*, vol. 19, pp. 806-813, May 2004.
- [75] H. Awad and F. Blaabjerg, "Transient performance improvement of static series compensator by double vector control," in *Proc. IEEE-APEC*, 2004, pp. 607-613.
- [76] D. M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "Performance improvement of the dynamic voltage restorer with closed-loop load voltage and current-mode control," *IEEE Trans. Power Electron.*, vol. 17, pp. 824-834, Sept. 2002.
- [77] J. Y. Hung, "Feedback control with posicast," *IEEE Trans. Power Electron.*, vol. 50, pp. 94-99, Feb. 2003.
- [78] Q. Feng, J. Y. Hung, and R. M. Nelms, "Digital control of a boost converter using posicast," in *Proc. IEEE-APEC*, 2003, pp. 990-995.
- [79] P. C. Loh, D. M. Vilathgamuwa, S. K. Tang, and H. L. Long, "Multilevel dynamic voltage restorer," *IEEE Letters Power Electron.*, vol. 2, pp. 125-130, Dec. 2004.
- [80] Y. Neba, "A simple method for suppression of resonance oscillation in PWM current source converter," *IEEE Trans. Power Electron.*, vol. 20, pp. 132-139, Jan. 2005.
- [81] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, pp. 814-822, Mar. 2003.
- [82] M. J. Newman and D. G. Holmes, "A universal custom power conditioner (UCPC) with selective harmonic compensation," in *Proc. IEEE-IECON*, 2002, pp. 1261-1266.
- [83] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter based three-phase active rectifier," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 2001, pp. 299-307.

- [84] P. A. Dahono, Y. R. Bahar, T. Sato, and T. Kataoka, "Damping of transient oscillations on the output LC filter of PWM inverters by using a virtual resistor," in *Conf. Rec. IEEE-PEDS*, 2001, pp. 403-407.
- [85] V. Blasko, and V. Kaura, "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 542-550, Mar/Apr 1997.
- [86] J. C. Wiseman, B. Wu, and G. S. P. Castle, "A PWM current-source rectifier with active damping for high power medium voltage applications," in *Proc. IEEE – PESC'02*, 2002, vol. 4, pp. 1930-1934.
- [87] C167 Derivatives 16-bit CMOS Single-Chip Microcontroller: User's Manual 03.96 Version 2, Siemens AG, 1996.
- [88] Dual DSP-Microcontroller Development System - for Power Electronics and Drive Systems. Institute of Energy Technology, Department of Electrical Energy Conversion, Aalborg University, 1999.

Appendix

Description of the Low Voltage Experimental Microgrid Prototype

The hardware microgrid prototype made up of several parts such as three/four-phase half bridge inverters using IGBT switches, IGBT gate drive board, three-phase back-to-back SCR switch, inductors and capacitors for the inverters filter circuits, load resistors and inductors, line resistors and inductors, current transducers, voltage transducers, interface circuits, DC sources for the inverters, AC source representing the utility system, and DSP controller board (DS1103). Photos of the proposed laboratory microgrid prototype highlighting the major components are shown in Figures 3.38 and 3.39 (in Chapter 3).

- AC Source

An “AC power Source/Analyzer” of HP6834B model (4500 VA), which is stiff enough and programmable, is used as the supply source. This AC source can be programmed to obtain various voltage unbalances, voltage magnitude sags, phase angle jumps, and frequency changes etc.

- Voltage Source Inverters (VSI)

Three/four insulated gate bipolar transistor (IGBT) modules (SKM 50 GB 123D) each consists of two switches are used for each three/four-phase inverter. These switches can be switched up to the switching frequency of 20 kHz. Voltage and current ratings of this module are 1200 V and 50 A respectively. Figure a.1. shows a configuration of the IGBT modules used in the hardware setup.

Figure a.1. Configuration of SKM 50G 123D IGBT module.

- Gate drive board

The IGBT's are turned on by applying a positive gate-emitter voltage (pin 4-5 or pin 6-7 in Figure a.1) of 15V, and turned off by connecting the gate to emitter. Semikron SKHI 60 gate driver modules are used to drive the IGBT inverters. The driver board comprises of short circuit protection circuits for the IGBT switches by measuring the collector to emitter voltage. This ensures all IGBTs are turned off immediately in the case of a short circuit happens. The drive board also switches all IGBTs to off state and change ERROR pin to low at fault situation, where the ERROR signal can be used to activate the protection circuit. An error memory prevents the IGBTs from being turned on again. Furthermore, IGBTs of the same arm are interlocked in order to prevent them being in the on-state simultaneously. Typically $3\mu\text{s}$ is used as the interlocking time.

- Three-phase solid-state circuit breaker

The circuit breaker used in laboratory is three-phase solid-state relay (PSD 12D-125000). It has DC control as input with control voltage range from 4V to 32V and the direct copper bonded back-to-back SCR as output, with zero voltage switching. The mains control voltage RMS values is up to 480V and load current can be as large as 25A RMS per phase.

- Current transducers

Analog inputs of the DS1103 controller board accept only voltage signals. Therefore all current measurements are required to be transformed into voltage signals before put in the DS1103 controller board. AC instantaneous type LEM current transducers (LTA 50-

P/SP1 and HA 200-SB) using the Hall Effect technology to measure instantaneous value of any complex waveform are used as CTs. The output of the CT can vary from -10V to 10V .

- Voltage transducers

PCB mounting voltage transducers (LEM LV25-P) are used to measure the utility grid and microgrid voltages. Voltage measurements of these transducers are also based on Hall Effect technology. To enable a voltage to be measured, a current proportional to the measured voltage must be collected through an external resistor, selected by the user, in series with the primary circuit of the unit. The secondary side of the unit gives a proportional current related to primary side current. The secondary side current is then converted to a voltage using a known resistor connected in the secondary side of the unit before feed to analog input of the DS1103 board.

- DSP Controller Board

Control algorithms are implemented using a DS1103 PPC controller board shown in Figure a.2. DS1103 PPC controller board consists of Motorola PowerPC 604e / 333 MHz main processor and Texas Instruments' TMS320F240 / 40 MHz slave subsystem with very powerful features. The DSP has been supplemented by powerful on-board peripherals including 2 general purpose timers, 2 Mbyte local SRAM, 16 Mbyte 32-bit global DRAM, 16 channels of 16-bit ADC, 4 channels of 12-bit ADC, 8 channels of 14-bit DAC, 6 channels of digital input incremental encoder subsystem and 4 channels of 8-bit digital I/O ports. The slave DSP is an independent subsystem that supports symmetric and asymmetric PWM generation (Three-phase PWM outputs plus 4 single PWM outputs), capture inputs, as well as 16 channels of 10-bit ADC and digital I/O system. All off-chip memory and I/O can be accessed by the host even while the DSP is running thus allowing easy setup and monitoring.

Figure a. 2. Block diagram of DS1103 controller board.