Study of carbon nanotube field effect transistor using electrostatic force microscopy

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2012

Ong, H. G. (2012). Study of carbon nanotube field effect transistor using electrostatic force microscopy. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/48023>

<https://doi.org/10.32657/10356/48023>

NANYANG
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**Study of Carbon Nanotube Field Effect Transistor Using
Electrostatic Force Microscopy**

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School of Materials Science & Engineering
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A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2012

Acknowledgement

These 4 years have been packed with many twists that see me dropping from the highs and picking myself up again. I will have been just another dropout in MSE without all my love ones, old or new, and the beloved friends, colleagues, supervisor that have been there to guide and concern me.

I want to express my heartfelt thanks to my thesis supervisor, Assoc Prof Wang Junling. Without his generous donation of blood and sweat in me, I will have just be another cnt in a charcoal. In these 4 years, he had broken his patience limit uncountable times, for the sole purpose to improve the qualities in me. I am greatly indebted to him and his teachings will always stay in my mind no matter where I pursue. This planet or beyond. Our numerous long hours of discussion in lab had been, and will always be in my mind.

I also wish to express many thanks to Assoc Prof Zhang Hua, co-supervisor Dr Han Guchang, Assist Prof Li Lain-Jong, and Assist Prof Zhao Yang for the advices and help that were given to me along this project.

I will like to thanks my group mates, Dr Chua Ngeah Theng, Dr You Lu, Cheah Junwei Jason, Ding Hui, Zou Xi, Dr Yang Pan, Dr Zhang Zhen, Guo Rui, Peng Yuan. All of you make my normal lab day more interesting. Especially to Jason, who introduced me to Dr Wang and this group; and have helped me with many areas of my work and discussion in this topic.

To my kakis, Chia Wei-han, Tan Zhen He, Toh Junchang, Toh Vincent and Liang Tiancong, I thank you for all these 15 years of endurance, support and encouragement. Though I have yet to solve the “formation of black hole on the mahjong table” as you all have proposed for my thesis, I figure out that it may be due to your individual ethnic boundary conditions. I dedicate this middle paragraph to all of you because, whenever I am down, you pull me up. Whenever I am high, you will hold me to remind me to be on the ground. They say true friends are hard to find. I am lucky to find 5 of you.

I will like to express special thanks to He Yingran, Dr Xu Yanping, Dr Shi Yumeng, Dr Hosea Tantang, Dr Peter Darmawan, Dr Lee Chun Wei, Dr Li Bing, Dr Stevin Snellius Pramana, Lee Meng Keong, Dr Leonardus Kresna Widjaja, Chen Weigang, Chng Yulian, Yeo Jason and my SRT buddies for their support, guidance and encouragement that lead me on.

I will also like to express my thanks to all the staffs from Electromagnetic lab, FACTs, microelectronics lab, Nanocluster, computer lab and general office for their guidance in equipment and administration aid that let me have an enjoyable time doing research.

I want to thank Ms Lim Qian Ru for hopping into my life journey. Just like electron hopping to produce current in polymer, you have given me energy to lighten up my path forward, happier.

Last and most importantly, I want to thank both my parents, Ong Peng Keng and Khong Yow Kheng, and my brother, Ong Hock Chwee, for bringing me up, protecting and taking care of the sickly me when I am young; never to give up on me when I am rebellious in my teen; supporting my decision to quit a stable job to pursue my passion 4 years back. Especially my mother, who will go all the way out to think of ideas using carrot and vegetables to advise me to design better experiments. I will not be at this stage without the 3 of u all.

The author also acknowledges the support from Nanyang Technological University and Ministry of Education of Singapore under project number AcRF RG30/06.

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Abstract

As the silicon based metal-oxide-semiconductor field effect transistors quickly reaching the proposed 8 nm limit by 2022,¹ it is necessary to search for solutions that can go beyond the 8 nm limit. One method is to substitute silicon with nanostructured materials. Carbon nanotube is a potential candidate because of its superior electrical, mechanical and chemical properties over silicon. Carbon nanotube field effect transistor has been studied extensively since 1998.² However, there are still challenges before it can be implemented into commercial products. One of the issues is the existence of hysteresis in its transfer characteristic, which is undesirable for active logic device applications. On the other hand, it has been proposed that this hysteresis behavior can be explored for non-volatile memory application. Either way, it is crucial to understand the cause of the hysteresis, so that we can eliminate or stabilize it for different applications.

In this work, we performed an in-depth study on how the hysteresis is generated in a single carbon nanotube field effect transistor by conducting in-situ electrostatic force microscopy study while the transport property is being measured. Using this technique, we have demonstrated that a layer of charges are injected from the carbon nanotube channel onto the gate dielectric, SiO₂ in our device, surface. This layer of charges screens the applied gate voltage and causes the hysteresis in the transistor transfer characteristic. In addition, we have also investigated the dynamic injection and dissipation of the screening charges and the nature of the charge traps.

It has been suggested previously that the traps for these injected charges could be (1) at the Si/SiO₂ interface, (2) in the SiO₂, (3) at the CNT/SiO₂ interface and (4) surface containments. Using our setup, we have concluded that surface traps on SiO₂, such as the water layer that is absorbed by the silanol groups on the SiO₂ surface, is the dominating factor that causes hysteresis at room temperature. By investigating the dissipation characteristic of the injected charges, we have found that at elevated temperatures, the water layer starts to evaporate. Above a critical temperature, the silanol groups become the dominating traps. We have fitted the charge diffusion curves using Fick's 2nd law of diffusion, and obtained the activation energies of ~0.46 eV and 0.91 eV below and above the critical temperature, respectively.

Our findings suggest that the hysteresis can be eliminated by removing the charge traps at the gate dielectric, SiO₂, surface. This can be done by surface passivation after the transistor is made. It is also observed that the injected charges cover an area that can reach micrometers, which seriously limits the data storage density if it is used for memory application. Furthermore, there is also the possibility of cross-talking among neighboring cells. Thus we conclude that carbon nanotube field effect transistor, using SiO₂ as the gate dielectric, is not suitable for memory application. We suggest replacing SiO₂ with ferroelectric materials that possess spontaneous polarization for this purpose.

Chapter 1: Background Introduction and Objectives

1.1 Background Introduction

Figure 1.1 (a) A picture of the first transistor constructed in 1947,³ and (b) the circuit symbol of an npn transistor

A transistor is a semiconductor device that can amplify or switch electrical signals. For a typical three terminal transistor, the flow of electron between the emitter and collector electrodes can be controlled by a voltage applied to the base. Figure 1.1 (a) shows the first transistor that was made by John Bardeen and Walter Brattain in AT&T's Bell Labs during 1947.³ The simplest way to construct a transistor is to sandwich a p-type semiconductor between 2 n-type semiconductors to form an npn transistor, whose circuit symbol is shown in figure 1.1 (b). Transistor has since evolved to take on different structures in today's electronic devices. Some of the common transistors are bipolar junction transistor (BJT), junction gate field effect transistor (JFET), multiple gate field effect transistor (MuGFET), metal-oxide-semiconductor field effect transistor (MOSFET) and insulator-gate bipolar transistor (IGBT).

MOSFET is probably the most commonly used transistor in modern electronics. It was first built by Dawon Kahng and Martin M. (John) Atalla at Bell Labs in 1960,⁴ even though the principle of field effect transistor (FET) has already been known and patented by physicist Julius Edgar Lilienfeld back in October, 1925.⁵ The structure of a typical top gate MOSFET is shown in figure 1.2. It consists of a ‘source’ and a ‘drain’ electrodes, which are connected by a semiconductor channel. A dielectric layer separates the semiconductor channel from the gate electrode. Some of the typical dielectric materials used are silicon dioxide (SiO_2) and high k dielectric materials such as hafnium dioxide. The current between the source and drain electrodes can be controlled by a voltage applied to the gate. When the gate voltage increases to above the threshold value, an inversion layer is formed at the semiconductor-insulator interface. This inversion layer contains the same type of carriers as the source and drain, thus forming a channel for current to pass through.

Figure 1.2 Schematic drawing of a p type MOSFET

Silicon is the dominating material used in today's semiconductor industry. Transistors made of silicon can be found in electronic devices ranging from simple calculators, televisions,

hand phones to more sophisticated equipments such as personal computers and satellites. Because of the importance of this industry, an International Roadmap Committee has been formed, which publishes the International Technology Roadmap for Semiconductors (ITRS). ITRS is “the fifteen-year assessment of the semiconductor industry’s future technology requirements. These future needs drive present-day strategies for world-wide research and development among manufacturers’ research facilities, universities, and national labs”.⁶ The development of semiconductor industry has closely followed Moore’s law, a term coined by Carver Mead following Gordon Moore’s original statement that the number of transistors that can be packed in an integrated circuit will double every year. This prediction has since been changed to double in every 2 years.⁷ To achieve this, the size of transistor has continued to decrease for the last several decades. This trend has been followed for the past decades through scaling of the devices. The 2 types of scaling commonly used are geometrical scaling and equivalent scaling. The former reduces the critical dimension of the transistor proportionally while the latter improves the circuit performance through innovative design, software solutions, and innovative processing.

Silicon has been the main stream material for making transistors from a bottom up approach. Currently, the leading companies, e.g. Intel, are producing computer chips with transistor’s channel length as small as 28 nm.^{8,9} But as the physical dimension of the transistor continues to be scaled down, the thickness of the gate dielectric has to be reduced too and it is inevitable that its physical limitation will soon be reached. One way to solve this issue is to use alternative high- κ dielectric materials. For example, HfO_2 ($\kappa = 25$) has replaced SiO_2 ($\kappa = 3.9$) in Intel’s newest CPUs.^{10,11,12} Incorporating other materials with even higher

dielectric constants into current Si based technology presents much technological challenges. Thus, we need to look for other alternative solutions to keep Moors' law going.¹³

Figure 1.3 Classification of memory technologies.¹⁴

Similarly, this problem is also faced by the memory industry and ITRS appoints a task force to look at memory route map beyond the 16 nm technologies under the section of “Emerging Research Memory Technology”.¹⁴ Figure 1.3 summarizes the memory technologies studied by the ITRS committee. It is suggested that the 8 nm physical barrier of mature flash memory will be reached as early as 2022.¹ When the gate dielectric layer becomes too thin, the tunneling current will increase significantly. While there are some interesting potential memory technologies such as Resistive Random-Access Memory (RRAM) in the

pipeline, it still requires a better understanding of the physical model while improving its reliability issue. Thus, it will take a considerable amount of time before it is fully implemented. On another hand, there are memory technologies that are better understood and in the prototype stage. Recently, Fujitsu have launched its FeRAM using 0.18 μm technology from its earlier 0.35 μm technology.¹⁵ The retention is reported to exceed 10 years. Nevertheless, new memory technologies are being intensively investigated. These technologies should meet the requirement of being scalable beyond the 16 nm technologies, good performance with a partially understood storage mechanism and could be used for commercial production in a period of 5 to 10 years.

The ITRS report also includes an “Emerging Research Materials” session which presents candidate materials that can be used to solve current technological issues. One of such materials that have been proposed is single-walled carbon nanotube (CNT). A single-walled CNT is a hollow cylinder that can be viewed as a rolled up graphene sheet with a half fullene capped at both ends. It has a diameter ranging from 0.3 nm to 6 nm.^{16,17} CNT also possesses excellent electrical,¹⁸ mechanical¹⁹ and chemical²⁰ properties comparable or exceeding that of silicon, thus making it a very promising candidate as a substitution of silicon in the next generation nanoelectronics. Depending on its chirality, CNT can be metallic or semiconducting, making it applicable both as interconnect and in active devices.

Figure 1.4 A typical advancing hysteresis in the transfer curve of a CNTFET.

Incorporating CNT in FET has been studied extensively since 1998, when the first single-walled CNTFET was reported.² Different applications of CNTFET have been proposed and prototype devices have been studied, including logic devices, sensors and memory devices.^{21, 22, 23, 24} Most CNTFETs reported show hysteresis behavior in their transfer characteristics.²⁵ Figure 1.4 depicts the transfer curve of a typical single-walled CNTFET, where the threshold voltage clearly changes depending on the gate bias sweeping direction. This is problematic for application in logic devices, but can be used for memory application. No matter what applications we aim at, it is crucial that we understand the cause of the hysteresis behavior and can control it precisely.

1.2 Objectives and outline of the thesis

In this project, **our objectives are (1) to understand the mechanism that causes the hysteresis in the transfer characteristic of single-walled CNTFET using SiO₂ as gate dielectric; and (2) to offer possible solutions to stabilize or eliminate the hysteresis for different applications.**

We performed in-situ electrostatic force microscopy (EFM) study on a single-walled CNTFET while measuring its transport properties, which helps us to gain insight into how the hysteresis is generated. The rest of the thesis is organized as following:

- (1) In chapter 2, I will briefly introduce the properties of single-walled CNT, the growth of CNT by chemical vapor deposition (CVD), and the preparation of single-walled CNTFET.
- (2) In chapter 3, I will cover the CNT growth condition optimization, the preparation of devices used in this study. More importantly, I will introduce the electrostatic force microscopy (EFM) technique that will be used extensively in this project.
- (3) In chapter 4, I discuss the in-situ EFM study of a single-walled CNTFET while its transfer property is being measured. I will demonstrate how the charge activities around the CNT channel give rise to the hysterical behavior in the transfer characteristic, and provide evidences to support our model..

- (4) In chapter 5, I will look into the nature of the charge traps on the SiO₂ surface through temperature dependence studies and simulations. By extracting the activation energy of charge diffusion on the SiO₂ surface, we can identify the dominating traps and suggest methods to stabilize or eliminate the hysteresis.
- (5) The conclusions and future works are given in chapter 6.

Chapter 2: Literature Review

2.1 Introduction to carbon nanotube and its growth

Figure 2.1 Schematic pictures of (a) single-walled CNT and (b) multi-walled CNT.

While CNT has become a hot topic after Ijima's report in 1991,²⁶ its presence has already been reported much earlier than that. In 1956, Bacon from United Carbide in Parma was suggested to have found CNTs in his samples while studying the melting of graphite under high pressure and temperature.²⁷ He presented his observation of nanowhiskers using scanning electron microscopy (SEM) in 1960, where he proposed that they possess a scroll-like structure. In 1976, Edon reported high resolution transmission electron microscopy (HRTEM) images of carbon fiber with hollow core.²⁸ These hollow carbon fibers were observed to have catalytic particles at one of their ends, which were later found to be iron oxide from the sand paper he used.²⁷ Abrahamson in 1979 also reported hollow carbon fibers observed with HRTEM, suggesting presence of CNTs.²⁹

A CNT can be described as a graphene sheet rolled into a seamless tube. Figure 2.1 (a) shows the structure of a single-walled CNT where the tube is formed by a single layer of carbon. If there are CNTs wrapped up within others, it is called multi-walled CNT as shown in figure 2.1 (b). While all CNTs exist in tubular form, they do not all possess the same material characteristics. Taking single-walled CNT as an example, depending on how the graphene sheet is rolled up, it can be either metallic or semiconducting.

Figure 2.2 Chirality of a carbon nanotube defined based on the graphic sheet.

Figure 2.2 shows the honeycomb lattice of a graphene sheet, where the carbon atoms are arranged hexagonally. A CNT is formed when a terminating carbon, at site A, is connected back to the first carbon atom at site O. The distance OA is the circumference of the tube.

There are many ways to roll up the graphene sheet into a tube. And CNTs are differentiated by their chiral vector. The chiral vector of a carbon nanotube, $\mathbf{C}_h$, is defined as:

$$\mathbf{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2 = (n, m)$$

where $\mathbf{a}_1$ and $\mathbf{a}_2$ represent unit vectors seen in figure 2.2, and n and m are integers. Axis $\mathbf{a}_1$ and $\mathbf{a}_2$ are also known as zigzag and armchair axis, respectively.³⁰ The chiral vector makes an angle to the zigzag axis to give the chiral angle, θ . It can be expressed as

$$\theta = \tan^{-1}[\sqrt{3}m/(m + 2n)]$$

The CNTs can be classified into 3 groups based on their electronic properties, which is directly related to their chiral angles. When θ is 0° , the CNT is called zigzag nanotube. When $\theta = 30^\circ$, it is called armchair nanotube. The rest, where $0^\circ < \theta < 30^\circ$, are called chiral nanotubes. Among these 3 groups, armchair CNTs ($n = m$) have zero band gap and are always metallic. For other combinations of (n, m) , a band gap appears. The size of the band gap depends closely on the CNT chiral vector. If $n - m = 3j$, where j is a non-zero integer, the CNT will have a very small band gap. In fact, the gap is so small that thermal energy at room temperature is sufficient to promote electrons from the valence band to the conduction band. Thus, this group of CNTs will behave like metallic ones at room temperature. For the rest of the CNTs where $n - m = 3j \pm 1$, they have a larger band gap that depends on the diameter (~ 1.3 eV for a diameter of ~ 0.7 nm). They are semiconductors.³⁰ With an increasing diameter, d , of tube, the band gap of the large-gap and small-gap semiconducting

tubes will decrease following $1/d$ and $1/d^2$, respectively.³⁰ The diameter of a CNT can be calculated as

$$d_t = \sqrt{3}a_{C-C}(m^2 + mn + n^2)^{\frac{1}{2}} / \pi$$

where a_{C-C} is the distance between 2 nearest carbon atoms. A typical a_{C-C} value is 0.1421 nm for graphite. With the diameter of the CNT known, the bandgap can be estimated following $E_{\text{gap}}=0.9\text{eV}/d_t$.³¹ Figure 2.3 displays the different structures of CNTs with corresponding chiral vectors on a graphene sheet prior of rolling up. CNTs with metallic properties at room temperature are dotted in green, while semiconducting CNTs are dotted in blue.

Figure 2.3 Chart of different structures of CNTs based on their chiral vectors. Metallic CNTs at room temperature are labeled as green dots. Semiconducting CNTs are labeled as blue dots.

Compared with conventional semiconductors, such as silicon, CNT not only has much smaller physical dimension, but also possesses excellent electronic properties that make it very attractive for next generation electronics. It has been reported that single-walled CNT has very long carrier mean free pass and shows ballistic transport characteristic,^{32,33,34,35} high hole mobility ($\sim 79\,000\text{ cm}^2\text{Vs}^{-1}$ at ambient temperature),³⁶ high current density ($\sim 10^9\text{ A cm}^{-2}$),³⁷ and high thermal conductivity ($3500\text{ W m}^{-1}\text{ K}^{-1}$).³⁸ Table 2.1 shows the comparison between the electronic properties of single-walled CNT and that of silicon, and it is obvious that CNT outperforms silicon in many ways.

Table 2.1 Comparison between the material properties of CNT and intrinsic silicon

Material Properties	CNT	Si (intrinsic)
Mobility $\text{cm}^2\text{ V}^{-1}\text{ s}^{-1}$	79000 (@room temp) ³⁶ 100000 (@50 K) ³⁹	electrons: 1350 ⁴⁰ holes: 450
Charge carrier concentration cm^{-3}	$1 \times 10^{18}\text{ }^{19}$ (deduced from graphite)	1.45×10^{10}
Thermal conductivity $\text{W m}^{-1}\text{ K}^{-1}$	3500 ³⁸	142.2 ⁴¹
Electric resistivity Ω/m	$7.5 \times 10^{-3}\text{ }^{42}$	$6.4 \times 10^2\text{ }^{43}$
mean free path	190 nm ³⁴	electrons: 76Å ⁴⁴ holes: 55Å

The electronic properties of CNT are very sensitive to the environment. Exposure to different gases will lead to dramatic changes to its electronic characteristics.^{45,46,47} Under ambient condition, single-walled semiconducting CNTs usually show p-type behavior, which is reported to be due to oxygen absorption since oxygen molecules tend to take electrons from the CNT.^{48,49} There are also reports on dopants that lead to n-type CNTs,^{50,51} and studies on the charge transfer mechanisms between dopants and the CNT that give rise to its n or p- type behavior.^{52,53,54}

CNT can be grown by a wide range of methods as long as the following conditions are fulfilled: a supply of carbon source, catalyst and sufficient activation energy. Some of these methods include arc discharge,^{55,56,57} CVD,^{58,59,60,61} high pressure carbon monoxide synthesis (HiPco),^{62,63} flame synthesis^{64,65,66,67} and plasma-enhanced chemical vapor deposition (PECVD).⁶⁸ Among all the techniques, CVD stands out as a relatively easy to use method that produces high quality CNTs with high yield.²⁷ Moreover, this method may produce CNTs that are well aligned and can reach length of centimeters.⁶⁹

Figure 2.4 Schematic setup of a typical CVD system for CNT growth.

Figure 2.4 shows the schematic setup of a CVD for CNT growth. In this setup, metal catalysts (transitional metal nanoparticles, such as Fe, Co or Ni, are commonly used) are placed on a substrate which is placed in a furnace at elevated temperature (ranging from 550°C to 1200°C) under reducing condition. Gaseous carbon feedstock is then flowed into the furnace which leads to CNT growth from the catalysts. During the growth, the gaseous carbon source molecules breakdown on the surface of the catalyst, followed by carbon diffusion on the surface⁷⁰ or into the bulk.⁷¹ As carbon continues to break down on the surface of the catalyst and eventually exceeds the solubility limit, CNTs will start to grow. The CNTs will continue to grow as long as there is a supply of carbon. Whether the growth follows the surface diffusion or the bulk precipitation path depends on the type of catalyst, growth temperature and the carbon source used.

Figure 2.5 Schematic diagram describing the base growth and tip growth modes.

After nucleation and the CNTs start to grow, the catalyst particles can either stay at the base or the tips of the CNTs, as shown in figure 2.5. In the base growth mode, the catalysts are attached to the substrate and do not move. The CNTs continue to extrude from the catalysts into the air. In the tip growth mode, one end of the CNT is attached to the substrate, while the catalyst floating in the air. In both modes, the CNTs eventually follow the direction of gas flow as seen in figure 2.6.

Figure 2.6 Schematic of how gas flow leads to CNT alignment in CVD growth.

For application purpose, long and aligned CNTs are desirable, which makes large scale fabrication possible. Huang and coworkers have demonstrated ultra long CNT growth using rapid heating in CVD and used the “kite mechanism” to explain the results.⁷² In term of aligning the CNTs during growth, besides the effect of the gas flow, reports have shown that electric field can also be used to align the CNTs to the direction of the field during the growth stage.^{73,74,75} Termination of the CNT growth will occur when the supply of carbon source is removed or a layer of amorphous carbon shell begins to encapsulate the catalyst, cutting off the supply of carbon source.

2.2 Carbon nanotube field effect transistor and its application in non-volatile memory

Field effect transistor is the foundation of modern electronic industry, and MOSFET is the most commonly used design currently. During the last decade, much research has been devoted to find alternative devices in anticipation of the approaching physical limit of silicon-based MOSFET. CNTFET has been studied intensively for this purpose.

Figure 2.7 Comparison between the structure of (a) a conventional MOSFET and (b) that of a typical back gate CNTFET.

Figure 2.7 shows the device structure of a typical bottom-up back-gate CNTFET as compared to that of MOSFET. Even though they have similar structures, there is difference in their operating mechanisms. In a MOSFET, the flow of current between source and drain is controlled by the gate via the formation of an inversion layer that bridges the two electrodes. However, the current flow between the source and drain in a CNTFET is

controlled by the modulation of the Schottky barriers at the interfaces between the electrode and CNT.^{76,77,78} While gold is commonly used as the electrode, high work function metals with good wetting interaction with CNT, such as palladium, have been reported to lead to a transparent contact with CNT, and the device exhibits conductance close to the ballistic limit of $4e^2/h$ at room temperature.³² Even though CNTFET has demonstrated excellent performance such as large on/off ratio,^{31,79} fast operation etc.,³² there are still many challenges before its implementation in commercial products. Some of the challenges include selective growth of semiconducting CNTs, precise arrangement of CNTs and the of course, the hysteresis behavior in the transfer characteristics of CNTFETs.

Figure 2.8 The transfer characteristic of a p-type CNTFET, showing the typical advancing hysteresis loop.²⁵

Significant improvements have been achieved in the study of CNTFET since it was first reported in 1998.^{2,80} Hysteresis behavior in the transfer characteristic, however, remains to be a topic that is still extensively studied. Figure 2.8 shows the transfer curve of a typical p-

type CNTFET under ambient condition. Note that the threshold voltage depends on the sweeping direction of the gate bias. This is problematic for logic device applications, which requires the transistor to turn on and off at a specific voltage. On the other hand, the high and low conductivity states of the channel at zero gate bias can be explored for memory application.^{81,82,83,84,85}

Figure 2.9 Four read/write cycles demonstrating the memory capability of a CNTFET.²⁵

In 2002, Fuhrer and coworkers first demonstrated the data storage capability of a CNTFET.²⁵ In this work, Fuhrer and coworkers have shown that the on/off states of a CNTFET can be retained for more than 5000 s under ambient condition. Figure 2.9 shows the reading (at $V_{gs} = -1$ V) and writing (at $V_{gs} = \pm 8$ V) process. The authors have also looked into the mechanism behind the hysteresis behavior. They suggested that the cylindrical shape of the CNT together with its nano-scale dimension makes the electric field around the tube very high. In their work, they estimated this electric field around the CNT following $E \approx V_g / 23 R_t$, which gives a value greater than 0.3 V/nm for a 1.35 nm CNT and a V_g of 10 V. Since the breakdown field of SiO_2 is ~ 0.25 V/nm, the authors suggested that

movement of charges in the SiO₂ layer can be expected and electrons can be easily injected into and trapped in the SiO₂ layer. The trapped charges affect a local area while the gate biased induced polarization affects the CNT globally. They used scanned gate microscopy (SGM) to estimate the screening length of the CNT to be 50 nm and suggest that an electron in the dielectric charge will shift the potential of a 50 nm CNT section by 300 mV. The authors also suggested other possible mechanisms such as injection of charges onto the SiO₂ surface through ionized gas, and reorientation of adsorbents on the CNT.

At that same period of time, Radsavljevi and coworkers also reported the use of CNTFET as a memory device.⁸⁶ Figure 2.10 (a) shows the performance of their device at gate bias of ± 20 V across a 225 nm thick thermally grown SiO₂ back-gate. In their experiment, they have used a read/write speed of 100 Hz and demonstrated that the n-type CNTFET memory device can retain information for more than 16 hrs. They proposed that the charge storage were mainly due to two types of traps: (1) Si/SiO₂ interface traps and (2) bulk SiO₂ traps. Figure 2.10 (b) describes these traps schematically, where Q_{it} denotes interface trapped charges, Q_{ot} is bulk oxide trapped charges, Q_f are fixed charges and Q_m refers to mobile charges due to containments.⁸⁷ At the Si/SiO₂ interface, the traps are populated whenever a bias is applied to the gate. They proposed that these interface trapped charges screen the gate voltage and lead to the hysteresis behavior. Besides the interface traps, the authors have also incorporated traps inside the oxide in their model to explain their high vacuum test results. They conducted a series of transfer measurements in high vacuum with varying gate voltage from 10 V to 20 V. As shown in figure 2.10 (c) to (e), the hysteresis was observed to increase with the increasing gate voltage applied and the authors believed that it was a

result of avalanche charge injection into the SiO_2 bulk due to the increased electric field. They have also suggested that the cylindrical shape and small diameter of CNT are the cause of the high electric field, similar to the model of Fuhrer et al.²⁵

Figure 2.10 (a) CNTFET used as a memory device with its output voltage (V_{out}) plotted as a function of time while a series of read/write is performed. Insert of (a) shows the memory device structure of an electrically erasable programmable read only memory (EEPROMs). A V_{in} of ± 20 V is used to write the data. (b) Schematic diagram showing different types of charged defects in the SiO_2/Si system. (c) to (e) High vacuum transfer characteristics of the device measured with $V_{ds} = 0.5$ mV at different maximum gate voltage. Hysteresis loop enlarges with increasing gate voltage, suggesting avalanche charge injection effect.⁸⁶

After the initial reports, more scientists started investigating CNTFETs for memory application. Many different models have been proposed to explain the hysteresis behavior. For example, Cui and coworkers investigated the effects of annealing, oxygen plasma treatment and low temperature on the memory performance of a CNTFET and concluded that defects on the CNT surface, e.g. residual amorphous carbon particles, play a significant role.⁸⁸ In addition, they observed hysteresis behavior at temperature as low as 5 K. This ruled out the contribution from mobile ions in the SiO₂ layer, which should be frozen at this temperature.

The effects of defects and containments have also been studied by other groups. Bradley and coworkers reported that mobile ions, e.g. Na⁺ and K⁺, contributed to the advancing hysteresis behavior of their device.⁸⁹ Shimauchi and coworkers had also reported the effect of contaminations induced by the fabrication process on the hysteresis.⁹⁰ Yuan and coworkers have reported the use of surfactant to change the “advancing” hysteresis loop of a CNTFET to a “retarding” one.⁹¹

Figure 2.11 Experimental results on the effects of water layer on CNTFET performance. (a) Transfer curve of the CNTFET in (a) ambient and (b) vacuum. Hysteresis is reduced in vacuum but not eliminated even after 90 hrs. (c) Transfer curve of a suspended CNTFET as shown in the insert in ambient, and (d) the suspended CNTFET measured in vacuum. Negligible hysteresis is observed. (e) and (f) shows the effect of heat treatment on CNTFET.⁹²

In 2003, Kim and coworkers carried out a systematic study, which revealed the effect of water on the transfer characteristic of a CNTFET.⁹² In this work, they demonstrated that the hysteresis can be reduced in dry air and almost eliminated under vacuum (10^{-7} Torr), (see figure 2.11 (a), (b) and (e)). They conducted the same experiments using a fully suspended CNTFET as shown in the inset of figure 2.11 (c). It is noted that a large hysteresis still exist even with the SiO_2 is removed, which eliminates contribution from charge traps in bulk SiO_2 . On the other hand, by placing the device in vacuum, the hysteresis is completely removed. These observations led the authors to conclude that water molecules on SiO_2 surface act as traps for injected charges and cause the hysteresis. Their temperature dependent measurements support this claim, where the hysteresis is almost eliminated after heat treatment, figure 2.11 (f). The authors have suggested 2 types of water related charge traps: (1) water molecules that are weakly absorbed on the CNT surface, and (2) water molecules that are bonded to the SiO_2 surface. Later studies have confirmed the effect of humidity on the width of the hysteresis loop.^{93,94}

More recently, Muoth and coworkers have fabricated suspended CNTFETs using prefabricated MEMs structure.⁹⁵ No hysteresis was observed when the device was tested under ambient condition with 45% humidity. This is different from Kim and coworkers' results. The authors attributed the hysteresis free transfer characteristic to a combination of defect free CNT and lack of contamination on the surface of CNT due to the fabrication process.

In 2007, Lee and coworkers reported that the absorbed water layer on the surface of SiO₂ cannot fully account for the hysteresis formation.⁹⁶ In their experiment, they annealed a device at 300°C under ultra high vacuum but hysteresis still existed. Their further studies suggested that silanol groups on the SiO₂ surface also act as charge traps.

In summary, CNTFET has been studied intensively during the last decade and different models have been proposed to explain the hysteresis behavior in its transfer characteristic. It is generally accepted that trapped charges induced by the gate bias is the cause. But the location and nature of the charge traps are still unclear. A total of 4 possible charge traps have been proposed by various researchers, including (1) Si/SiO₂ interface traps; (2) charge traps in the bulk of SiO₂; (3) absorbed water on SiO₂ surface; and (4) mobile ions/containments on CNT and SiO₂ surfaces. However, most of previous studies are indirect. The conclusions are drawn from electrical measurements under different environments.^{97,98} There is a lack of direct observations of the charge trapping/detrapping process and its correlation to the hysteresis. Furthermore, the physical dimension of the trapped charges and the retention time are crucial for nonvolatile memory application, but have not been systematically studied before. We intend to address these issues in this study.

Chapter 3: Experiment Setup

3.1 Carbon nanotube growth and CNTFET device preparation

In this work, we grow CNTs using a home-made CVD system and fabricate our devices following standard photolithography process. Our CVD setup is shown in Figure 3.1. We used ethanol as the carbon feedstock reagent, Ar as the carrier gas; and H₂ as the reducing gas. The two gases were mixed at a ratio of 4:1 (Ar : H₂).

Figure 3.1 Our CVD setup for CNT growth.

To grow CNTs, we used n-type Si (cut into 1.5cm by 1 cm pieces) with 300 nm of thermally grown SiO₂ (Silicon Quest International, Inc) as the substrate. It was put in acetone and

cleaned in an ultra-sonic bath for 15 min, after which it was rinsed in ethanol and blown dry using nitrogen gas. This cleaning process was repeated twice. We prepared our catalyst solution by adding Cobalt Acetate powder (Sigma Aldrich) to 99% ethanol (Merck) to form a solution of 0.35 μ M/L. Two drops of the catalyst solution were placed at one end of the substrate via a needle syringe (Terumo, 0.5 X 25 mm). The substrate was then put into the middle of the CVD quartz tube with the end with catalyst facing the gas inlet of the tube.

The Ar/H₂ mixture gas was then supplied to the CVD for 30 min while the furnace was kept at 850 °C. During this period, the catalyst was reduced by the H₂ into metal particles of about 6 nm. Next, the furnace was brought to CNT growth temperature before switching the valve to allow the mixture gas to go through a bubbler half filled with ethanol. The temperature of the bubbler is kept at 0 °C by immersing it in melting ice. Ethanol vapor was then carried by the mixture gas into the CVD tube for CNT growth. The ethanol vapor will decompose on the surface of the catalyst particles, which usually exist in liquid form during the reaction because of their much reduced melting point at nanometer scale.^{99,100} The decomposed carbon will dissolve into the catalyst until it becomes saturated in the catalyst. Upon saturation, excess carbon will precipitate out and CNT starts to grow. We usually grew the CNTs for 30 min before cutting off the feedstock supply, which led to CNTs of millimeters long. The system was then cooled down to room temperature under reducing condition.

Figure 3.2 Temperature dependence of CNT growth. SEM images showing the quality of CNTs grown at (a) 800 °C, (b) 850 °C, (c) 900 °C, (d) 950 °C. Insets of (a) and (b) show the high magnification view of catalysts. at both 800 °C and 850 °C, the catalysts are covered by a layer of amorphous carbon, terminating further growth of CNTs.

In this work, long, aligned and sparsely spaced CNTs are desired for the preparation of CNTFETs for our experiments. Thus, our growth optimization differs from most reported works where the aims are to achieve high yield of semiconducting CNTs, small diameters, or patterning of CNTs, etc. We try to obtain CNTs that are $> 150 \mu\text{m}$ long with a density of < 3 aligned CNTs per $100 \mu\text{m}^2$. In this work, we try to achieve these goals by tuning the

growth temperature and catalyst solution concentration. For simplicity, the ratio of gas mixture and the reduction and growth time are fixed.

We have studied the effect of temperature on the growth of CNT. The growth temperature was varied between 800 °C and 1000 °C. Figure 3.2 shows the SEM images of CNTs at the catalyst sites grown at these temperatures. At 800 °C, no CNTs were observed and it appeared that the catalyst particles were coated with a layer of material (insert of figure 3.2 (a)). According to previous reports, the coating layer could be amorphous carbon, which inhabits the growth of CNT upon the encapsulation of the catalyst.¹⁰¹ At 850°C, cluster of catalyst particles were still observed. However, longer and more CNTs were seen to grown out of the clusters (Figure 3.2 (b)). When the growth temperature was further increased to 900 °C, fewer catalyst clusters were observed and CNTs grew up to hundreds of micrometers (Figure 3.2c). At 950°C (Figure 3.2 (d)), the amount of catalyst clusters decreased tremendously, and CNTs in mm length were observed. When we increased the temperature to 1000 °C, there were almost no sign of catalyst or CNTs. Our observations are consistent with previous studies. It was reported that at lower temperature, amorphous carbon will be formed on the catalyst, inhibiting CNT growth.¹⁰¹ On the other hand, if the temperature is too high, the thermodynamic condition in the system would favor the ethanol vapor to decompose into CO₂ in the chamber instead of on the catalyst surface, resulting in no CNT growth.

By fine tuning our growth temperature optimization, we have concluded that 925 °C is the ideal condition. We have also found that a catalyst solution of 0.035 mol/ml leads to good

result. Figure 3.3 shows the SEM image of CNTs grown at 925 °C with 0.035 mol/ml catalyst solution. The direction of the CNTs follows that of the gas flow, and there are about 6 CNTs within a 500 μm range, which is very suitable for device preparation. Compared with other works reported in the literature, we have used a lower catalyst concentration and feedstock gas flow rate to obtain sparsely spaced long and aligned CNTs.

Figure 3.3 High magnification image of long aligned CNTs grown with catalyst concentration of 0.035 mol/ml.

Following the growth of long, aligned CNTs, we prepare the CNTFETs simply by depositing electrodes through a shadow mask. The substrate with CNTs was secured to the back of the shadow mask by a tape, followed by the deposition of Cr and Au in a DC sputtering system under high vacuum (10^{-6} Torr). The Cr and Au layers are 4 nm and 100 nm, respectively. The Cr layer helps to achieve a better adhesion of the Au to the SiO_2 . The distance between the electrodes, which is the channel length, is $\sim 120 \mu\text{m}$, and the electrodes size are $920 \mu\text{m} \times 220 \mu\text{m}$.

3.2 Experimental setup for the in-situ electrostatic force microscopy study

Figure 3.4 Components of an AFM.

After the CNTFET was prepared, we conducted in-situ EFM imaging (use an Asylum Research MFP3D system) while the transport properties of the device were measured. This setup allows us to correlate the macroscopic device performance with microscopic phenomena such as charge trapping around the CNT channel, which should lead to better understanding of the device characteristics and the mechanism that causes the hysteresis.

Electrostatic force microscopy is an atomic force microscope (AFM) based technique. AFM was invented by G. Binnig and C.F. Quate in 1986.¹⁰² It had since become a common

technique for nano-scale morphology characterization. In an AFM, the tip scans along the surface of a sample following the topography. The deflection of the tip cantilever is picked up by a laser beam reflected onto a photodiode, as shown in figure 3.4. In modern AFMs, the x, y and z scanners are usually decoupled and have close-loop controllers, which lead to low noise and accurate control of tip location.

Figure 3.5 Oscillation of cantilever in tapping mode. (a) Detecting oscillation of cantilever with laser beam reflected onto the photodiode. (b) Change in laser spot on the photodiode at different tip oscillation amplitude due to surface morphology.

Atomic force microscope can operate in both contact and tapping modes. In contact mode, the tip is always in direct contact with the sample surface during the scan. The deflection of the tip by surface morphology is detected by the location of the reflected laser spot on the photodiode. Using the photodiode signal as a feedback, the z axis piezoelectric stack will adjust the height of the tip (in some AFMs, the z piezoelectric stack will control the height of the sample) to maintain a constant deflection, and give rise to the topography image. In tapping mode, the tip is mechanically driven by a piezoelectric actuator (see figure 3.5) to oscillate around its resonance frequency and is only tapping on the sample surface during the scan. It is also possible that the tip does not touch the surface at all (non-contact).

The oscillation of the tip cantilever leads to the same oscillation of the laser spot on the photodiode, which is used as the feedback signal for the z axis piezoelectric stack. When the tip scans along the surface of sample, the z axis piezoelectric stack will move the tip up and down to maintain a constant oscillation amplitude. In our experiments, the cantilever oscillation amplitude is set at a photodiode reading of 1 V. As shown in figure 3.5, if the tip encounters a dip, the amplitude will be more than 1 V. The controller then moves the z piezoelectric stack downwards so the amplitude goes back to 1 V. When the tip encounters a hill, the opposite happens. The movement of the z axis piezoelectric stack is used to construct the surface profile of the sample.

Figure 3.6 (a) Schematic drawing of the dual-pass technique. (b) Effect of attractive and repulsive forces on the cantilever oscillation amplitude and phase.

Electrostatic force microscopy is a dual path tapping mode technique, as schematically shown in figure 3.6 (a). During the first scan, the tip is close to the sample surface and picks up the topography information in normal tapping mode. During the second scan, the tip is lifted by a certain distance (30 nm in our study) from the sample surface and retraces the same profile recorded in the first scan to ensure a constant tip-sample distance. During the second scan, a DC bias is applied between the tip and sample, and the long range electrostatic force between the sample and the tip can be detected.

In our experiments, Olympus Pt coated cantilevers (OMCL-AC240TM) with a spring constant ~ 2 N/m were used. The electrostatic force acting on the tip will cause the resonance frequency of the cantilever to shift as indicated in figure 3.6 (b). Since the cantilever is driven at its original free-standing resonance frequency, the vibration amplitude and phase will change. For example, if a positive bias is applied to the tip, it will experience

a net repulsive force if positive charges exist on the surface of the sample. This will reduce the cantilever oscillation amplitude and decrease its phase shift with respect to the driving signal as shown in figure 3.6 (b). On the other hand, negative charges on the sample surface will lead to the opposite result. Thus we could tell the type of charges on the sample surface by looking at the phase shift of the cantilever oscillation. Mathematically, the phase changes due to the force acting on the cantilever is given by ¹⁰³

$$\Delta\phi = -\arcsin\left(\frac{Q}{k} \frac{dF}{dz}\right)$$

where k is the spring constant and Q is the quality factor of the cantilever.

Under normal conditions, capacitive coupling force between the tip and sample dominates during the second scan, which is represented by

$$F(z) = \frac{1}{2} \frac{dC}{dz} V_{dc}^2$$

When net charges exist on the sample surface, electrostatic force between them and their image charges in the tip also contributes, so ¹⁰⁴

$$F(z) = \frac{1}{2} \frac{dC}{dz} V_{dc}^2 + \frac{q_s q_s'}{4\pi\epsilon_0(z+z')^2} + \frac{q_s C V_{dc}}{4\pi\epsilon_0(z+r)^2}$$

where r is the radius of the tip. The first term on the right hand side of the equation represents the capacitive coupling force. The second term comes from the surface charges and their image charges located at z' in the tip. The third term comes from the interaction between the surface charges and tip bias.

It has been reported that EFM can reach a resolution of ~ 20 nm,¹⁰⁵ thus is a very useful tool to study nanoelectronic devices.^{106,107} Various groups have used this technique to study charge distribution,^{108,109} defects,¹¹⁰ trapped charges,^{111,112} electrical transport¹¹³ and surface charges.¹¹⁴ In order to establish a correlation between the macroscopic transport properties of CNTFET and the microscopic charge trapping / detrapping phenomena, we will conduct EFM studies on a CNTFET while measuring its transfer characteristic using an Hewlett Packard 4140B picoammeter.

Chapter 4: Origin of hysteresis in the transfer characteristic of CNTFET

As discussed previously, it is generally believed that the hysteresis in the transfer characteristic of a CNTFET originates from trapped charges that screen the gate bias. However, most of previous studies are indirect and the analyses are based on transport measurements under different environments. Direct observations of the trapped charges, their dynamic behavior and relationship to the hysteresis are still lacking. Furthermore, different types of charge traps have been proposed in the literature to be responsible for the hysteresis, e.g. defects at the Si/SiO₂ interface, water layer on the SiO₂ surface and contaminations on CNTs, etc. It is important to clarify the dominating factors and suggest ways to eliminate or stabilize the hysteresis for different applications. We thus conducted in-situ EFM study on a CNTFET while its transfer characteristic was measured using a setup as shown in figure 4.1 (a).

Figure 4.1 (a) Experimental setup for the in-situ EFM study, and (b) SEM image of a typical single tube CNTFET used in the study.

Due to the confinement of the EFM setup, the source and drain electrodes were extended by gold wires, which were then connected to the picoammeter. The gate was connected by scratching the surface of the SiO₂ and connecting a gold wire to the Si substrate with silver paste. This setup allows real time EFM imaging while the electrical characteristic is being measured.

Figure 4.2 Effect of gate bias on the EFM signal. (a) EFM images around part of the CNT channel taken with (i) $I_{ds} = 0$ V and $V_{gs} = 0$ V, (ii) $I_{ds} = 0.1$ V and $V_{gs} = 0$ V, (iii) $I_{ds} = 0.1$ V and $V_{gs} = 3$ V and (iv) $I_{ds} = 0$ V and $V_{gs} = 0$ V. (b) Cross section profiles of the EFM images. It is observed that when the gate bias is turned on, the overall background signal changes as expected. After the gate bias is turned off, the background signal reverts to its original value.

To obtain the transfer characteristic of the CNTFET, DC bias has to be applied between source and drain electrodes (V_{ds}), and between source and gate electrodes (V_{gs}). So we tested how these voltages affect the EFM images of the device first. The middle portion of the channel was chosen for the EFM imaging to avoid any electrostatic interaction between the cantilever and the source/drain electrodes. It also keeps the scanning time manageable. Using the setup shown in figure 4.1 (a), we carried out a continuous scan over the selected portion of the CNT channel. The tip bias was 3 V during the second path of the EFM imaging. The scan was conducted at 2 Hz and each region in figure 4.2 (a) took about 30 sec. During the continuous scan, we first kept both V_{ds} and V_{gs} zero (Figure 4.2 (a)(i)). The CNT channel is clearly visible due to its capacitive coupling with the tip, which is different from the background SiO_2 surface. After establishing the reference, we then turned V_{ds} and V_{gs} on one by one. While scanning region (ii), a V_{ds} of 0.1 V, which is used to measure channel current during the transport study, is applied while keeping V_{gs} zero. No changes were observed in the EFM image, indicating the negligible effect of such a small V_{ds} on the electrostatic force experienced by the tip. As the imaging continues, in region (iii), we kept the V_{ds} at 0.1 V and applied a V_{gs} of 3 V. Significant changes were observed. The background signal changed from brown (76° phase shift) to purple (74.2° phase shift). Apparently, the gate bias has changed the electrostatic force experienced by the tip. Since both the gate bias and the tip bias (applied during the EFM second path) are both positive, a repulsive force is generated between the tip and the whole silicon substrate, leading to a decrease of phase shift between the tip oscillation and the driving force. This is consistent with the prediction shown in figure 3.6 (b). During the last region (iv) of figure 4.2 (a), both

V_{ds} and V_{gs} were turned to zero again. We noticed that at the far end of the image away from the CNT channel, the phase shift went back to the original value of 76° . This suggests that negligible charges are trapped at the interface of the Si/SiO₂, otherwise the background signal would remain at a lower value. On the other hand, the phase shift around the CNT increases, forming two peaks in the image (Figure 4.2 (a), region (iv)), especially right after the gate bias is turned off. This indicates that negative charges appear in this region, leading to an attractive force between the sample and the tip. Since the width of this region is around 2 μm extending away from the CNT, it is very unlikely that the charges are injected into the bulk of SiO₂. We thus concluded that these charges are on the surface of SiO₂, and further study was carried out to understand their effect on the transfer characteristic of the CNTFET.

Figure 4.3 Macroscopic transfer characteristic and microscopic charge injection of a CNTFET. (a) Transfer curve obtained by sweeping the gate bias from 25 V to –25 V and back. The EFM images are taken at every 5 V intervals. During each scan, the gate bias is temporally turned off. Injected charges are observed around the CNT and are correlated to the hysteresis loop.

Following the initial tests, we proceeded to investigate the correlation between the surface charges and the hysteresis loop in the transfer characteristic of the device. We swept the gate bias, V_{gs} , from 25 V to –25 V and back. A hysteresis loop was observed in the transfer curve, as shown in figure 4.3. This device exhibited an on/off ratio of ~ 100 . During the electrical measurements, EFM scans were performed at every 5 V intervals, with the V_{ds} and

V_{gs} turned off temporarily during the scan. The EFM scans were conducted with tip bias of 3 V during its second scan and each image took ~ 40 s to complete. These images were displayed on the sides of the transfer loop in figure 4.3. Bright and dark contrasts in these images represent negative and positive charges on the SiO_2 surface, according to our earlier discussion (See figure 3.6 (b)). After applying a gate bias of 25 V, bright regions appear next to the CNT channel, indicating negative charge accumulation. It is emphasized that since the source, drain and gate were all connected to ground during the EFM scan, the contrast observed by the side of the CNT are due to residual charges on the surface of the SiO_2 . The bright regions remain even when the gate bias was decreased to zero. Upon reverse of the V_{gs} polarity, dark region starts to appear around the CNT and gradually extends into the bright region. This indicates that the surface charges are likely injected from the CNT channel. As the negative gate bias continues to increase, the bright regions disappear completely at -25 V. The dark region, indicating positive charge accumulation, remains even when the gate bias is increased back to zero.

Figure 4.4 The cross section profiles of the EFM images, indicating the relative charge density around the CNT for (a) backward gate sweeping from 25 V to -25 V, (b) forward gate sweeping from -25 V to 25 V.

Figure 4.5 Integration of the phase shift/ r over the scan range, where r is the distance away from the CNT channel.

These injected charges on the surface of the substrate cannot be dissipated immediately when the gate bias changes. Thus they will screen the CNT from the gate bias, causing a shift in the threshold voltage. To study the relationship between the injected charges and the hysteresis in the transfer characteristic of the CNTFET, we performed a semi-quantitative analysis. We examined the EFM phase shift around CNT at the middle part of the channel as shown in figure 4.4. Since the EFM phase shift is directly related to surface charge density,¹⁰⁴ we can obtain qualitatively the total injected charge effect by integrating the EFM phase shift over r , the distance away from the CNT.¹¹⁵ When we plot the integrated value as a function of gate bias, a clear hysteresis is observed (Figure 4.5), consistent with the transfer characteristic. This is expected since the screening effect should be proportional to the total amount of injected charges. Interestingly, it is observed that the amount of positive charges injected onto the surface under negative gate bias is significantly less than the negative charges under positive gate bias. This is consistent with the shift of the

hysteresis loop towards positive bias side (Figure 4.3). This observation indicates that the SiO₂ surface can trap electrons more effectively than holes.

Figure 4.6 Hysteresis-free transfer curve under ambient condition. (a) Hysteresis width can be reduced by allowing the injected charges to dissipate at every gate bias. The experiment was conducted by turning the gate bias off at every step for 0 (black), 2 (red) and 15 (blue) minutes, and measure the I_{ds} immediately after turning the gate bias back on. (b) The corresponding EFM images after 0 (top), 2 (middle) and 15 (bottom) minutes discharging time. (c) The bottom image in (b) replotted with reduced scale. A small amount of injected charges is observed.

If the injected charges are indeed responsible for the formation of the hysteresis loop, it is expected that we will obtain a hysteresis-free transfer curve if we let the injected charges to have enough time to dissipate before measuring the I_{ds} . We thus conducted the transfer measurement by sweeping V_{gs} between 25 V and -25 V in a different manner to test this prediction (Figure 4.6). At every voltage step, the gate bias was turned off for a duration of 0 (black curve), 2 (red curve) and 15 (blue curve) minutes, after which it was turned back on

and the measurement of I_{ds} was conducted immediately. It is apparent, as shown in figure 4.6, that longer discharging time leads to the decrease in the hysteresis width. With a discharging duration of 15 minutes, an almost hysteresis-free transfer curve was obtained. Figure 4.6 (b) depicts the corresponding EFM images after the different discharging duration. It is obvious that the injected charges have almost disappeared completely after 15 minutes, consistent with the macroscopic transfer behavior. The remaining narrow hysteresis observed in the transfer curve is due to the small amount of residual charges (Figure 4.6 (c), decreased scale).

Figure 4.7 The dynamic screening effect of the injected charges. (a-d) Upon application of a positive gate bias, electrons are injected onto the SiO₂ surface around the CNT channel. When the gate bias is decreased, polarization charge decreases but injected charges remain. Once the gate bias turns negative, holes are injected onto the SiO₂ surface. (e-h) Opposite process takes place when the gate bias is swept from $-V_{max}$ to $+V_{max}$.

Based on the above observations, we propose the following dynamic screening effect due to the injected charges, which is schematically described in figure 4.7. The blue and green layers represent the n-doped Si substrate and SiO₂, respectively. When a gate bias of 25 V is applied, a layer of negative charges (purple layer) is formed on the SiO₂ surface around the CNT (Figure 4.7 (a)). The amount of injected charges will be limited by the number of traps available. The CNT channel will experience a net potential from both the gate bias and the injected charges. When the gate bias is decreased, the injected charges cannot dissipate immediately, which means that the potential acting on the CNT channel from the injected charges decreases more slowly than that from the gate potential. When the gate bias decreases to a certain value, the effect from the injected charges will overwhelm that of the polarization induced by the gate bias and turn the transistor on (Figure 4.7 (b)). This will shift the transfer curve to the right. When $V_{gs} = 0$ V, the injected charges still exist (Figure 4.7 (c)) and the transistor remains on. As the gate bias decreases to the negative region, holes are injected onto the SiO₂ surface as shown in figure 4.7 (d), compensating the trapped electrons. For a period of time, both holes and electrons will coexist on the SiO₂ surface side by side, as shown in figure 4.3. With further decrease of the gate bias, the injected charges will be fully inverted to holes (Figure 4.7 (e)). This process reverts as the gate bias sweeps back from -25 V to 25 V (Figure 4.7 (e)-(h)).

The above analysis clearly correlates the hysteresis behavior with the injected charges. Based on our observation, we suggest that the hysteresis cannot be used for non-volatile memory applications due to two reasons. First, charge dissipation leads to data retention

problem. Second, the μm size (Figure 4.3) of the charged area limits data storage density and generates cross talking among cells.

For application in logic devices, it is required that we eliminate the hysteresis behavior. However, the nature of the charge traps remains unknown. This is very important because the trap depth determines the dissipation rate of the injected charges, which in turn affect the hysteresis loop. In the following chapter, I report our effort to understand the nature of the charge traps and suggest methods to eliminate hysteresis in the future work session.

Chapter 5: Nature of the charge traps on SiO₂ surface

As described in the previous chapter, we understand how the hysteresis is formed due to the screening effect of the injected charges. These charges cover a distance up to micrometers from the CNT on SiO₂ surface, which makes it not suitable for non-volatile memory application due to packing density and reliability issue. On the other hand, we need to eliminate the hysteresis behavior before CNTFET could be implemented in logical devices. That requires us to understand the nature of the charge traps.

From the literature, charge traps at different locations of the transistor have been suggested, including (1) at the Si/SiO₂ interface, (2) in the SiO₂, (3) at the CNT/SiO₂ interface and (4) containments on CNT. Generally, trapping due to defects at the Si/SiO₂ interface has been greatly reduced with the advance in growing SiO₂.¹¹⁶ Furthermore, from our tests shown in figure 4.2, we have also demonstrated that charging at the Si/SiO₂ interface is negligible. As shown in chapter 4, the width of the charged area can reach a width of μm under a voltage of 25 V applied over 300 nm SiO₂, thus it is unlikely that traps in the SiO₂ bulk contribute to this effect.²⁵ This leaves us only the traps on SiO₂ surface. To be able to control the hysteresis behavior of a CNTFET, we have to understand the nature of the charge traps on the surface of SiO₂.

5.1 Surface chemistry of SiO₂ and hysteresis loop- the experimental results

Figure 5.1 Temperature dependent hysteresis loops. (a) The hysteresis width decreases as temperature increases. At 180 °C, the hysteresis completely disappears under negative gate bias, but remains under positive bias, indicating the lack of hole traps on the SiO₂ surface. (b) The hysteresis width measured by threshold voltage shift at different temperatures. (c) hysteresis loops taken around the transition temperature depicting the transformation in (a). (d) hysteresis loop time duration study upon cooled down to room temperature.

In the literature, it has been proposed that water layer on the SiO₂ surface traps charges around the CNT channel and temperature dependent experiments have provided evidence to support this model.^{92,93} We have conducted a simple temperature dependent experiment to

verify the effect of water layer, where we measure the transfer property while performing EFM imaging at different temperatures to correlate the surface charges to the hysteresis.

The setup of this test is identical to the previous experiment, except that the sample was secured on a heating stage (Polyheater™, Asylum Research). We conducted transfer measurements at different temperatures ranging from 20 °C to 180 °C and the results are shown in figure 5.1 (a). As temperature increases, the hysteresis width continues to decrease as shown in figure 5.1 (b), though the scattering of data prevents us from obtaining accurately the activation energy of the evolution and critical temperature if any. It is interesting to note that the hysteresis disappears under negative gate bias at 180 °C and above, but remains under positive gate bias. Figure 5.1 (c) shows this transition more clearly from 140 °C to 180 °C. At 140 °C, a normal hysteresis (black) loop can still be observed. With an increase of 30 °C in temperature, we can observe that there is a dip (red curve) at around $V_{gs} = 5$ V. With further increase of temperature, there is a clear shrinkage of the hysteresis loop on the negative bias side. At 180 °C, the loop (green curve) has almost disappeared in the negative V_{gs} region. On the contrary, the loop expanded in the positive V_{gs} region. This clearly indicates that there maybe two types of charge traps available on the SiO₂ surface. We suggest that evaporation of water at high temperatures results in the SiO₂ surface being dominated by electron trapping defects. If this is true, at 180 °C, where there is little or no hysteresis loop in the negative V_{gs} region, there should not be any injected charges. We conducted EFM imaging at $V_{gs} = -10$ V at 20 °C and 180 °C as shown in insert of figure 5.1 (a). At 20 °C, the dark contrast, indicating positive charges, could be observed and related to the formation of the hysteresis loop (black) in figure 5.1

(a). At 180 °C, the absence of dark contrast around the CNT indicates negligible charge injection as compared with that taken at room temperature (inset of figure 5.1 (a)). Upon cooling back to room temperature (20 °C), the hysteresis loop can be observed again, as shown in figure 5.1 (d). Once the device reaches room temperature (0 min), main part of the hysteresis recovers immediately. However, even after 59 hours under ambient condition, the hysteresis width is still less than the original value. This observation suggests that the first few layer of water is absorbed back onto the SiO₂ surface upon cooling to room temperature, but full recover of the original surface condition takes much longer time.

5.2 Surface chemistry of SiO₂ and hysteresis loop- the model

The temperature dependence of the hysteresis loops in a CNTFET observed in chapter 5.1 can be explained by looking at the surface chemistry of SiO₂.

An atom residing on the surface of a solid has only its inner side saturated in bonding.¹¹⁷ The outer side will have “residual valences”, which Langmuir had used to explain the attachment of foreign atoms/molecules to the surface, forming a layer of adsorbed molecules.¹¹⁸ The first layer of adsorbed molecule is usually connected to the surface by chemical bonds and this is called “chemisorption”. Subsequent layers of molecules can also be formed on the first layer of adsorbates. These layers are bonded through weak secondary forces and are termed as “physical adsorption”.

Figure 5.2 Silanol and siloxanes groups on SiO_2 surface: (a) isolated silanol, (b) germinal silanol, (c) vicinal silanol, (d) and surface siloxanes.

Figure 5.3 Two basic orientations of water molecules connected to silanol groups via hydrogen bonding: (a) hydrogen atom of water molecule bonded to oxygen of silanol group; and (b) oxygen atom of the water molecule bonded to the hydrogen atom of the silanol group.

Amorphous SiO_2 has a surface that is terminated with siloxane groups (Si-O-Si). The “residual valence” leads to reaction with water to form silanol groups ($-\text{OH}$).¹¹⁸ Figure 5.2 shows the types of siloxane and silanol groups that exist on SiO_2 surface: (1) isolated silanol

group, (2) germinal silanol group, (3) vicinal (H-bonded germinals) silanol group, and (4) siloxane groups.

Figure 5.4 Silicon dioxide surface at different temperatures: (a) multi layers of water molecules exist on SiO₂ surface under ambient condition; (b) only a single layer of water molecules at temperature just below the boundary temperature; (c) at the boundary temperature, only silanol groups on SiO₂ surface without water molecule; and (d) upon cooling back to ambient temperature, rehydration takes place and water layers start to form back on SiO₂ surface slowly.

The silanol groups act as adsorption centers of foreign molecules. At sufficient concentration, the silanol groups make the SiO₂ surface hydrophilic.¹¹⁹ Water molecules will then attach themselves to these silanol groups through hydrogen bonding in 2 possible orientations as shown in figure 5.3. Under ambient condition, multi-layers of water molecules exist on the SiO₂ surface, forming an H-bonded network.^{92,119} The water layer can be reduced as the temperature increases as shown in figure 5.4. Complete removal will occur above the boundary temperature, T_b , leaving behind different silanol groups at the

state of maximum hydroxylation.¹¹⁹ T_b is generally accepted to be 180 ± 10 °C following the Zhuravlev Model, by means of deuterium exchange and mass spectrometric thermal analysis in conjunction with the temperature-programmed desorption method (MTA-TPD method).¹¹⁹ However, values ranging from 120 °C to 190 °C have been reported in the literatures.^{117,119} It is noted that while heating removes the water layer, it does not affect the silanol groups at such low temperatures. When the temperature is lowered, the silanol group will absorb water molecules again.

The above analysis can be used to explain our temperature dependent experimental results. As temperature is increased, the water layer on SiO₂ surface starts to evaporate and the amount of charges that can be trapped decreases. The reduced trapped charges lead to reduced hysteresis loop in the transfer characteristic of the CNTFET. Above the critical temperature, all the water molecules are removed and silanol groups become the charge traps. However, silanol groups tends to trap electrons and are not good hole traps,¹²⁰ so the hysteresis loop under negative gate bias (positive charge injection) disappears, but that under positive gate bias (negative charge injection) remains.

This model implies that the charge trap depth on SiO₂ surface will change at the critical temperature, which can be examined by temperature dependent charge diffusion experiment. We have then conducted such investigations and the results are discussed in chapter 5.3.

Figure 5.5 SiO₂ surface at different temperatures.

The model also suggests that to eliminate the hysteresis completely, it is necessary to get rid of the silanol groups on SiO₂ surface. This can be done by heating the substrate to very high temperatures. For example, Zhuravlev¹¹⁹ reported that under vacuum, the 3 types of silanol groups will be stable on the SiO₂ surface from the boundary temperature till ~400 °C. At this temperature, the vicinal silanol group will be removed, leaving behind isolated and

germinal silanol groups. Upon further increase in temperature, the germinal silanol group will be removed at temperatures between 800 °C to 900 °C, leaving behind only the isolated silanol bonds. The concentration of siloxane bridges starts to increase. At this stage, the reverse process to rehydrate the SiO₂ surface will take a very long time. Further increase in temperature will remove the silanol groups and increase the siloxane coverage until 1200 °C, where the whole surface will then be covered by siloxane bridges only. This process is summarized in figure 5.5.

5.3 Surface chemistry of SiO₂ and hysteresis loop- more evidence

So far, we have confirmed that the injected charges on SiO₂ surface screen the gate bias and lead to the hysteresis loop in the transfer characteristic of a CNTFET. We have also demonstrated that the main charge traps are the water layer that is absorbed to the silanol groups on the SiO₂ surface, while the silanol groups also contribute at high temperatures. The stability of the hysteresis loop depends on the dissipation of the injected charges, which in turn depends on the charge trap depth. Thus it is very important that we obtain this information. Next, we look into the dynamics of the charge injection and dissipation processes at different temperatures.

For this experiment, we have made some modifications to our CNT growth temperature. It is observed in previous experiments that the width of the charged area around the CNT

channel is about 1~2 μm . For such samples, the charging and discharging processes are too fast to extract any dynamic data accurately using EFM. This can be seen in figure 4.6 where greater than 50% of the charges are dissipated within the first 2 minutes after the gate bias is turned off. Thus in order to study the charging/discharging dynamics, we need a device with wider area of injected charges. Based on Zhuravlev's report, we knew that temperatures greater than 900 $^{\circ}\text{C}$ will reduce the silanol groups on the SiO_2 surface significantly, converting the surface to be dominated by siloxane groups which do not absorb water molecules.¹¹⁹ Our original growth temperature was 925 $^{\circ}\text{C}$, which falls in this range. Thus, we attempted to grow CNTs at a lower temperature, 900 $^{\circ}\text{C}$, for a shorter period of time to retain as much silanol groups as possible. This will in turn lead to a larger width of injected charges suitable for the study of charge dissipation dynamics.

For this part of the study, we applied the voltage to the drain electrode while keeping the gate ground as shown in figure 5.6 (a). This is because, when the tip is scanning on the SiO_2 surface together with a gate bias applied, the large attraction force from the gate will pull the tip into contact with the surface (the gate electrode is the whole silicon substrate and the tip is scanning on top). And the CNT channel will be damaged easily. Moreover, constant contact of a platinum coated tip with the surface will dissipate the injected charges on the SiO_2 surface. Applying voltage to the drain electrode eliminates this problem as the tip is scanning the channel away from the drain electrode. This flipping of the voltage supply does not change the nature of the charging process.

Figure 5.6 (a) Experimental setup for the charging/discharging experiments with DC bias applied to the drain electrode and gate grounded; Charging images and cross section profiles when (b) -5 V and (c) +5 V is applied to the drain electrode .

Thus, in our subsequent experiments, the gate is connected to ground and a V_{drain} of +5 V or -5 V is applied during the charging step and 0 V during the discharging process (Figure 5.6 (a)). V_{tip} is still kept at 3 V during the second pass of the EFM scan. It was noticed that the overall background signal changes once V_{drain} is applied if the EFM scan is conducted near to the drain electrode, indicating charge injection directly from the electrode to the SiO₂ surface or the tip is being affected by the bias applied to the gate electrode. This is consistent with previous report.¹²¹ Thus, an area in the middle of the channel, about 40 μm

away from the electrode, is chosen to avoid this problem. Charging images (Figure 5.6 (b)) with $V_{\text{drain}} = -5$ V shows bright contrast next to the CNT, which expands over time, indicating injection of negative charges to the SiO_2 surface around the CNT. Both the EFM phase shift and the width of the charged area increase as shown in the cross section line scans. Similar effects are observed when $V_{\text{drain}} = +5$ V (Figure 5.6 (c)) is applied, where dark contrast around the CNT indicates injection of positive charges.

Figure 5.7 Charging curves when the drain electrode is biased at -5 V. (a) EFM phase shift as a function of distance from the CNT. Inset of (a) shows the extension of the charged area as a function of time; (b) EFM phase shift as a function of time at different distances away from the CNT, showing the accumulation of charges over time.

EFM phase shift as a function of time at different distances from the CNT is shown in figure 5.7 (a) for $V_{\text{drain}} = -5$ V. For areas near to the CNT, injected charges accumulate to a saturation value within seconds. Since it takes about 8 seconds to collect one image, the actual charging time should be even shorter. Typical FET transfer characteristic study requires much longer time, which implies that it is unlikely that we can eliminate the

hysteresis simply by decreasing the gate bias sweeping time. The width of the injected charges is observed to be exceeding 5 μm , which confirms our hypothesis that using a lower growth temperature gives rise to more silanol groups on the SiO_2 surface to trap more water. Figure 5.7 (b) shows the phase shift as a function of distance away from the CNT at different time. The inset of figure 5.7 (a) shows the width increase during the charging process, which is an indication of how fast the injected charges move under the applied electric field. However, extraction of charge drifting rate is difficult because of the highly non-uniform electric field around the CNT. The charging range is likely restricted by the field distribution around the CNT.

Figure 5.8 (a) Discharging images at room temperature showing the diffusion of injected charges. Images are taken at 0 min, 3 min and 6 min after the bias is turned off. (b) Cross sections of the discharging images showing the movement of surface charge density peak at room temperature. (c) The peak position as a function of time at different temperatures ranging from 80 °C to 180 °C. Inset shows the opposite trend at low temperatures from 30 °C to 60 °C.

Since the slow response of the injected charges upon gate bias variation gives rise to the hysteresis behavior, the charge dissipation process is more important for a better understanding of the transfer characteristics of a CNTFET. After charging at $V_{\text{drain}} = -5$ V for 10 minutes, we connect the drain electrode to ground and scan the same area using EFM. It is observed in figure 5.8 (a, b) that charges next to the CNT diffuse back to the channel

immediately after the drain bias is turned off. A peak is formed in the surface charge density. This peak gradually moves away from the CNT as more charges diffuse back to the channel. The surface chemistry of the SiO₂ is expected to affect the diffusion process greatly. We have studied the position of the charge peak as a function of time at temperatures ranging from 30 °C to 180 °C. At every temperature (30 minutes are given for the sample temperature to stabilize), $V_{\text{drain}} = -5 \text{ V}$ is applied (the gate grounded) for 10 minutes before the discharging images are collected. It is observed that the speed at which the peak moves away from the CNT decreases initially as temperature increases from 30 °C to 60 °C (inset of figure 5.8 (c)); after which, the speed starts to increase as shown in figure 5.8 (c). This observation contradicts the common belief that increasing temperature (more thermal energy) will drive the charge diffusion faster. However, based on our previous analysis in chapter 5.1 and 5.2, it is believed that the water layer starts to evaporate as temperature increases. Apparently, less water on the SiO₂ surface impedes the movement of the injected charges. So at the low temperature region, two competing factors coexist. At higher temperatures, the surface condition is stabilized, and more thermal energy indeed leads to faster diffusion.

This competing effects of thermal energy and water evaporation at temperatures between 30 °C to 60 °C make it difficult to determine the diffusion barrier height (trap depth), as it depends on how much water remains on the surface. We thus decided to focus our investigation around the boundary temperature. Just below the boundary temperature, majority of the water molecules should have evaporated except the first layer that is chemically bonded to the silanol groups. The surface condition is relatively stable. Above

the boundary temperature, all the water molecules on the surface evaporate, leaving the silanol groups on the SiO₂ surface. The transition in surface condition will create a difference in charge diffusion process, which can be used to extract the barrier height (trap depth).

In order to extract the charge diffusion barrier height, we need to obtain the diffusion coefficients at different temperatures. This can be achieved by simulating our experimental results using the governing diffusion equation. In our experiments, the discharging curves were obtained while keeping the source, drain and gate electrodes ground, so there is no electric field around the CNT. The charge diffusion is mainly driven by concentration gradient. Thus, we use Fick's second law, which describe the diffusion of particles, to model the discharging process. The discharging curves used for the simulation are those obtained at temperatures from 110°C to 180°C, which should tell us the trap depth) for the discharge profiles for simulation to extract its diffusion coefficient of charge dissipation on SiO₂ surface.

Before proceeding with the simulation, we must first determine the boundary conditions. In both the charge injection and dissipation processes, we observed that the width of the surface charges is rather uniform along the CNT. Thus, we will consider the injection and diffusion of charges along the direction perpendicular to the CNT channel, effectively treating it as a one-dimensional problem. Assuming that the diffusion coefficient is independent of charge density, Fick's second law can be simplified to $\left(\frac{\partial c}{\partial t}\right) = D \left(\frac{\partial^2 c}{\partial x^2}\right)$, where D is diffusion coefficient and c is the density of charges.

Figure 5.9 Cross section profiles of the EFM images at different time during discharging at (a) 110 °C and (b) 180 °C, respectively. At a distance of 10 μm away from the channel (located at 0 μm), the amount of injected charges is negligible.

For the boundary conditions, figure 5.9 (a) and (b) show the discharging profile at 110 °C and 180 °C, respectively after the drain bias was turned off for 0, 0.25, 0.5 and 1 min. It can be observed that there is negligible charge activity at a distance of ~10 μm away from the CNT. So we choose this point as one of the boundaries and set $c = 0$ at the location. On the other hand, since the CNT is connected to ground during the discharging process, it will act as an infinite sink for the charges. At this point, the amount of diffusion current that goes into the CNT, $j_d = -D\left(\frac{\partial c}{\partial x}\right)$, is assumed to be proportional to the local charge density, thus $j_d = k_{out}c$. In summary, the boundary conditions of our simulation are:

$$D\left(\frac{\partial c}{\partial x}\right) = k_{out}c \quad \text{at } x = 0 \text{ } \mu\text{m},$$

$$c = 0 \quad \text{at } x = 10 \mu\text{m},$$

where k_{out} is the proportionality constant that will be obtained through the simulation.

Figure 5.10 Fitting of experimental results using Fick's 2nd law at 4 temperatures: (a) 110 °C, (b) 130 °C, (c) 150 °C and (d) 170 °C. The red, green and blue curves represent charge distribution along the direction perpendicular to the CNT channel at 0.25 min, 0.5 min and 1 min after the drain bias is turned off.

We used Matlab 7.5 to conduct the simulation and the results are shown in figure 5.10. The code is attached in Appendix A. Experimentally, it is impossible to capture the exact initial

charge distribution profile before the diffusion starts due to equipment limitation. Thus we choose the cross section profile of the first captured image (~ 2 s after the bias is turned off) as the initial charge distribution profile ($t = 0$ min) for the simulation. The simulated curves (in lines) were calculated and plotted together with the experimental data (in dots) as shown in Figure 5.10 for (a) 110 °C, (b) 130 °C, (c) 150 °C and (d) 170 °C. Using the least square method, we obtained K_{out} values of 0.35, 1.3, 2.3, and 22.5 $\mu\text{m}/\text{min}$ and $D = 0.25, 0.48, 0.85$ and $3.16 \mu\text{m}^2/\text{min}$ for the four temperatures shown in figure 5.10, respectively.

Figure 5.11 Plot of $\ln D$ against $1/T$ shows a transition point at 150 °C, above which the activation energy changes from ~ 0.43 eV to ~ 0.98 eV. We attribute this transition to the point where water molecules are removed from the SiO₂ surface, leaving behind silanol groups.

Following our previous analysis, complete removal of surface water molecules above the boundary temperature will reveal the silanol groups, and this should lead to a change in the diffusion barrier for the injected charges to move across the surface. For a thermally activated process, we can obtain the activation energy following the Arrhenius equation, $D = D_0 \exp(\frac{-E_a}{RT})$. We plot the $\ln D$ against $\frac{1}{T}$ in figure 5.11. A linear behavior is observed and the activation energy can be obtained from its gradient. It is observed that there is a transition at $\sim 150^\circ\text{C}$, above which the activation energy increases from $\sim 0.43\text{ eV}$ to $\sim 0.98\text{ eV}$. This can be explained by the model indicated in the inset of figure 5.11. As discussed earlier, upon exceeding the boundary temperature, the surface of SiO_2 will lose all the water molecules and the silanol groups will be exposed. This process will change the charge trap depths. Our data suggests that the boundary temperature of the thermally grown SiO_2 used in our device is $\sim 150^\circ\text{C}$.

We note that, in figure 5.10, the simulated curves do not match experimental results well at distances further away from the CNT. This indicates that the charge concentration gradient may not be the only driving force. Indeed, considering that the particles are negatively charged electrons, electrostatic forces among the particles will also affect the diffusion process. Thus, we add a drift current term, $\vec{J}_e$, in our modeling to represent the electrostatic interaction among the negative charges. Thus the equation includes both the diffusion current, $\vec{J}_d$, and the drift current, $\vec{J}_e$,

$$\begin{aligned}
\frac{\partial c}{\partial t} &= -\nabla \cdot (\vec{J}_d + \vec{J}_e) \\
&= -\nabla \cdot (-D\nabla c + \sigma \vec{E}_e) \\
&= D\nabla^2 c - \frac{\sigma}{\epsilon_r \epsilon_0} \nabla \cdot \vec{D}_e \\
&= D\nabla^2 c - \frac{\sigma}{\epsilon_r \epsilon_0} c
\end{aligned}$$

where σ , $\vec{E}_e$ and $\vec{D}_e$ represent conductivity, electric field intensity and electric displacement intensity, respectively. We defined $\gamma \equiv \frac{\sigma}{\epsilon_r \epsilon_0}$ as an additional parameter used in the simulation. The boundary condition at the CNT is changed to include both the diffusion and drift terms:

$$\vec{J}_d + \vec{J}_e = -D \frac{\partial c}{\partial x} + \sigma E_e = k_{out}' c$$

Since E_e is proportional to the charge density c at $x = 0 \mu\text{m}$, the whole term can thus be simplified to $D \frac{\partial c}{\partial x} = k_{out}'' c$. The far end boundary condition is kept unchanged as charge activity is still negligible. Hence, the new boundary conditions are summarized as below:

$$\begin{aligned}
D \frac{\partial c}{\partial x} &= k_{out}'' c, & \text{at } x = 0 \mu\text{m}, \\
c &= 0, & \text{at } x = 10 \mu\text{m},
\end{aligned}$$

Figure 5.12 (a) Cross section profiles of experimental results (in dots) and fitting curves using the first model (lines); (b) Cross section profiles of experimental results (in dots) and fitting curves using the second model (lines); (c) Plots of $\ln D$ against $1/T$ from 110 °C to 180 °C. Top: the first model; bottom: the second model.

Optimization of the 3 parameters, D , γ and K_{out} , is done using the least-square method to get the best fit to our experiment data. The new model leads to much better fitting quality when compared with the previous model. Figure 5.12 (b) show new fitting curves at 180 °C. Comparing to earlier result shown in figure 5.12 (a), it can be observed that the matching at longer distance away from the CNT channel is significantly improved. The D , γ and k_{out} values obtained at 180 °C are $3.1 \mu\text{m}^2/\text{min}$, 0.4 min^{-1} and $30 \mu\text{m}/\text{min}$, respectively. We

recalculated these values for the experimental results at temperature ranging from 110 °C to 180 °C and re-plotted the graph of $\ln D$ against $\frac{1}{T}$ in figure 5.12 (c). While there are slight changes in the activation energies, ~ 0.46 eV and ~ 0.91 eV for the two regions respectively, the trend and the transition temperature remain unchanged.

In conclusion, by simulating the charge diffusion around the CNT channel, we have obtained the diffusion coefficients of electrons on SiO₂ surface at different temperatures. The fitting results are significantly improved by taking into consideration the electrostatic interaction among electrons. A critical temperature of ~ 150 °C is observed, above which the activation energy of charge diffusion almost doubles its low temperature value. We attribute the difference to different trap depth of electrons by silanol groups and water layer on SiO₂ surface respectively.

5.4 Eliminating the hysteresis by surface modification- preliminary results

Our study has clearly demonstrated the effect of SiO₂ surface chemistry on the hysteresis behavior of the CNTFET. It is thus expected that by modifying the SiO₂ surface, we may be able to reduce or even eliminate the charge trapping and hysteresis. To confirm this, we prepared self assembled monolayer (SAM) of OTS as a passivation layer on SiO₂. This was done by dipping the sample into the OTS solution for a period of 72 hrs, since it is not possible for CNT to be grown on OTS treated substrates as the growth temperature is too

high. The sample was then tested by applying a -5V bias to the CNT through the drain electrode while keeping the gate grounded. Figure 5.13 shows the results obtained.

The topography of the device has changed as seen in figure 5.13 (a). The rougher surface suggests that OTS SAM has formed on the sample surface. Figure 5.13 (b) shows the EFM images around the CNT channel before and after the OTS treatment. It is noted that after OTS treatment, the width of the charged area around the CNT had halved. In addition, the amount of charge being held on the surface had also decreased significantly. Figure 5.13 (c) shows the ground state (no biased applied to the drain electrode) of the CNT after the OTS treatment. By comparing it with figure 5.13 (b), it is observed that the amount of charge trapping around the CNT is very limited. However, OTS treatment is corrosive in nature and the CNTFET is always broken after the treatment, preventing us from conducting transfer measurement. Furthermore, the increased roughness of the surface brings another factor into charge trapping which complicates the study. Further systematic study is needed to confirm the effect of OTS treatment on the hysteresis of CNTFET.

Figure 5.13 Surface modification with SAM OTS (a) Topography images of sample before and after OTS treatment for 72 hrs. (b) Corresponding EFM images of (a) with the cross sections of the EFM images. (c) EFM image with its cross section showing the ground state of the sample after OTS treatment.

Chapter 6: Conclusions and Future Work

In conclusion, we have demonstrated that in-situ EFM measurement can be used to study the dynamic charge activity around the CNT channel while the electrical properties of a CNTFET are being measured. Such experiments help us to establish a clear correlation between the charge injection around the CNT channel and the hysteresis behavior of the transistor. This technique can also be used to study other nano-electronic devices. The following conclusions can be made from this study:

- (1) Charge injection around the CNT channel under gate bias causes the hysteresis in the transfer characteristic of the SiO₂-gated CNTFET. The dominating charge traps are those on the surface of the SiO₂. Contributions from charges traps at the Si/SiO₂ interface and in the bulk of SiO₂ are negligible.
- (2) The charged area around the CNT channel extends up to micrometers from the CNT, which makes it unsuitable for non-volatile memory application. The large charged area means memory density will be low, and cross-talking between neighboring cells may cause reliability issue.
- (3) Temperature dependent charging/discharging experiments have proven that both the water layer and silanol groups on SiO₂ surface contribute to the charge trapping process. Using Fick's second law, we can describe the charge distribution on the SiO₂ surface accurately as a function of time and achieve very good match between

experimental and simulation results. Charge diffusion activation energy, which corresponds to trap depth, has been extracted. A critical temperature of about 150 °C is observed, below which the water layer dominates the charge trapping with a trap depth of about 0.46 eV. Above the critical temperature, the silanol groups on SiO₂ surface dominates the charge trapping, and the trap depth is about 0.91 eV.

- (4) Also, from the simulation, we observed that both the concentration variation of the injected charges and the electrostatic force among them drive the movement of the charges on the SiO₂ surface. Only by considering both factors, we can achieve an accurate description of the charging/discharging dynamics.
- (5) Eliminating the water layer on the SiO₂ surface by heating the device to high temperature will decrease the hysteresis width, but it will not eliminate it completely. Silanol groups, as good electron traps, still cause a half loop at high temperatures. Surface passivation is needed to eliminate the hysteresis completely.

Based on our discoveries, we make the following recommendations for future work:

- (1) We have shown that SiO₂-gated CNTFET is not suitable for non-volatile memory applications. This is due to the fact that the hysteresis loop is caused by injected charges on the SiO₂ surface, which covers an area of micrometers in size. One way to solve this issue is to replace the SiO₂ gate dielectric with ferroelectric materials.

Ferroelectrics possess spontaneous polarizations that can be switched by an external electric field. The spontaneous polarization does not need a field to maintain, so its effect on the channel is non-volatile. Furthermore, the polarization is controlled locally beneath the CNT channel when a gate bias is applied, which solves the memory density and cross-talking issues associated with the charge injection induced hysteresis.

Several studies on the ferroelectric-gated CNTFETs have been reported in the literature.^{122,123,124} In 2006, Sakurai and coworkers have demonstrated the non volatile memory effect of a ferroelectric-gated CNTFET using $\text{PbZr}_{0.5}\text{Ti}_{0.5}\text{O}_3$ thin films as the dielectric layer.¹²⁵ Later, Nisho and coworkers also reported using organic ferroelectric thin film, P(VDF/TrFE), as the gate dielectric of a CNTFET. In this work, they covered a CNTFET with the copolymer and studied the ferroelectric domains using piezoelectric force microscopy (PFM). Their device can maintain the information for 100 hours.¹²⁶ Recently, Fu and coworkers have reported achieving controllable memory switching and data retention longer than a week in a ferroelectric-gated CNTFET.¹²⁷

For application in ferroelectric-gated CNTFET, the ferroelectric materials should possess large spontaneous polarization and good stability. PZT is the most widely studied and used ferroelectric material. It has a high dielectric constant (ranging from 425 to 3850),¹²⁸ large polarization and high resistivity ($>10^{10} \Omega\cdot\text{m}$). It is widely used in ultrasonic transducers, sensors and actuators. However, PZT contains lead,

which is toxic. Recently, much research has been devoted to lead-free ferroelectrics, where BiFeO_3 is a promising candidate. It possesses the largest spontaneous polarization known today, and should be a good candidate for ferroelectric-gated CNTFET.

Unlike PZT or BiFeO_3 which is rigid, another class of material that can be used is polyvinylidene fluoride (PVDF). This organic material exhibits ferroelectric properties with a polarization of 50-70 mC/m^2 .¹²⁹ Moreover, it can be used for flexible devices.

However, major challenges still remain in this area. For example, the retention time of the transistor states is usually short, which could be due to the low stability of the polarization of ferroelectric in such devices or the compensation of polarization charge by free charges from the environment. Furthermore, charging effect still exist at the CNT-ferroelectric gate interface, which may overwhelm the effect of the ferroelectric polarization. Further studies are still needed in this area.

- (2) For applications in logic devices, where it is necessary to eliminate the hysteresis behavior, we suggest that surface passivation can be applied to the SiO_2 -based CNTFETs. This process can also be applied to ferroelectric-gated CNTFETs to minimize the charge injection effect and make sure that the spontaneous polarization controls the channel conductivity. Several groups have tried to eliminate the

hysteresis behavior of CNTFETs by controlling the SiO₂ surface chemistry. The commonly used methods include: (1) to change the surface chemistry of SiO₂ to be hydrophobic using self-assembled monolayers (SAMs), and (2) to encapsulate the CNTFET with another material after device preparation.

For example, McGill and coworkers have shown that integration of hydrophobic octadecyltrichlorosilane (OTS) SAM on SiO₂ surface prior to placing CNTs can eliminate hysteresis in the transfer characteristic.¹³⁰ OTS SAM terminates the SiO₂ surface silanol groups, thus making it difficult for water to be absorbed. However, if the gate voltage applied is too large, hysteresis will still appear. The authors suggested this may be due to traps at the Si/SiO₂ interface or inside the oxide bulk when the electric field exceeds 3×10^5 V/cm. In another work, Hu and coworkers used octanethiol and aminopropyltriethoxysilane (APTES) SAMs to modify the surface and terminate the SiO₂ with –NH₂ amide groups.¹³¹ They have demonstrated significant reduction in the hysteresis width as compared to that of the control sample.

Another way to eliminate the hysteresis is to encapsulate the device. In this regard, most groups have used PMMA because of its hydrophobic property. Results have shown that PMMA is able to reduce the hysteresis width.¹³² However, it has been reported by Kim and coworkers that under different humidity levels, their device still show hysteresis behavior after PMMA encapsulation.⁹² Other materials, such as Al₂O₃, have also been used to encapsulate the device.^{133,134}

Following our suggestions, our colleague, Jason Cheah, has performed encapsulation of ferroelectric-grated CNTFET using TiO_2 film and observed a transition from injected charges dominated behavior to ferroelectric polarization dominated behavior.¹³⁵ This demonstrated the effectiveness of TiO_2 encapsulation, and we recommend further study in this direction.

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Appendix A – Matlab code for simulation

Matlab code for simulation, V1:

```
% Curve fit for T=150deg
dx=10/128;
dt=0.0005;
tt=2000;
tt2=500;
xx=126;
c=zeros(xx,tt);

CL=2:0.1:3;
Dmax=0.5:0.05:1.5;
% initial condition
c(:,1)=y0;
solution=[0,0,0];
dev=1000000000000;
for i=1:11
    for k=1:21

        for n=1:tt2-1
            D=Dmax(k);
            c(1,n+1)=c(3,n)-CL(i)/D*c(2,n)*2*dx;
            for p=2:xx-1
```

```

        D=Dmax(k);

        c(p,n+1)=c(p,n)+dt*D*(c(p-1,n)+c(p+1,n)-2*c(p,n))/dx^2;

    end

end

sum=0;

for s=1:xx

    sum=sum+(y025(s)-c(s,tt2))^2;

end

if sum<dev

    solution=[CL(i),Dmax(k),sum];

    dev=sum;

end

end

end

% Profile calculation using solution

for n=1:tt-1

    D=solution(2);

    c(1,n+1)=-solution(1)/D*c(2,n)*2*dx+c(3,n);

    for p=2:xx-1

        D=solution(2);

        c(p,n+1)=c(p,n)+dt*D*(c(p-1,n)+c(p+1,n)-2*c(p,n))/dx^2;

    end

```

end

```
hh=plot(x0,y0,'*k',x0,c(:,500),'r',x0,c(:,1000),'g',x0,c(:,2000),'b','MarkerSize',3,'linewidth',1.5);
```

```
hold on;
```

```
plot(x0,y025,'r*','MarkerSize',2);
```

```
plot(x0,y05,'g*','MarkerSize',2);
```

```
plot(x0,y1,'b*','MarkerSize',2);
```

```
xlabel('Distance(\mum)','fontsize',16);
```

```
ylabel('Concentration(a.u.)','fontsize',16);
```

```
xlim([0,10]);
```

```
ylim([-2,35]);
```

```
legend(hh,'t=0min','t=0.25min','t=0.5min','t=1min');
```

Matlab code for simulation, V2:

```
% Curve fit by taking drift current into account for T=180deg

dx=10/128;

dt=0.00025;

tt=4000;

tt2=4000;

xx=167;

c=zeros(xx,tt);


CL=10:10:40;

tor=0:0.2:1;

Dmax=3:0.1:4;

% initial condition

c(:,1)=y0;

solution=[0,0,0];

dev=1000000000000;

for i=1:4

    for j=1:6

        for k=1:11

            sum=0;

            for n=1:tt2

                D=Dmax(k);

                c(1,n+1)=c(3,n)-CL(i)/D*c(2,n)*2*dx;
```

```

    for p=2:xx-1
        D=Dmax(k);
        charge=tor(j)*c(p,n);
        c(p,n+1)=c(p,n)+dt*D*(c(p-1,n)+c(p+1,n)-2*c(p,n))/dx^2-dt*charge;
    end
    if n==1000
        sum=sum+norm(y025-c(:,n))^2;
    end
    if n==2000
        sum=sum+norm(y05-c(:,n))^2;
    end
    if n==4000
        sum=sum+norm(y1-c(:,n))^2;
    end
    end
end

if sum<dev&&sum<100000000000000
    solution=[CL(i),tor(j),Dmax(k),sum];
    dev=sum;
end

end

end

```

end

% Profile calculation using solution

for n=1:tt-1

 D=solution(3);

 c(1,n+1)=-solution(1)/D*c(2,n)*2*dx+c(3,n);

 for p=2:xx-1

 D=solution(3);

 charge=solution(2)*c(p,n);

 c(p,n+1)=c(p,n)+dt*D*(c(p-1,n)+c(p+1,n)-2*c(p,n))/dx^2-dt*charge;

 end

end

plot(x0,y0,'*', 'MarkerSize',3);

hold on;

plot(x0,c(1:xx,1000),'r','linewidth',1.5);

plot(x0,y025,'r*', 'MarkerSize',2);

plot(x0,c(1:xx,2000),'g','linewidth',1.5);

plot(x0,y05,'g*', 'MarkerSize',2);

plot(x0,c(1:xx,4000),'b','linewidth',1.5);

plot(x0,y1,'b*', 'MarkerSize',2);

Appendix B – List of Publications

- 1) Ong, H.G., Cheah, J.W., Chen, L., Tangtang, H., Xu, Y., Li, B., Zhang, H., Li, L-J., Wang, J. (2008). Charge injection at carbonnanotube-SiO₂ interface. *Applied Physics Letters*, 93, 093509.
- 2) Cheah, J.W., Shi, Y., Ong, H.G., Lee, C.W., Li, L-J., Wang, J. (2008). N-type behavior of ferroelectric-gate carbon nanotube network transistor. *Applied Physics Letter*, 93, 082103.
- 3) Zhang, Z., Wong, L.M., Ong, H.G., Wang, X.J., Wang, J.L., Wang, S.J., Chen, H., Wu, T. (2008). Self-Assembled Shape- and Orientation-Controlled Synthesis of Nanoscale Cu₃Si Triangles, Squares, and Wires. *Nano Letters*, 8, 3205-3210.
- 4) He, Y., Ong, H.G., Zhao, Y., He, S., Li, L-J., Wang, J. (2009). Study of Charge Diffusion at the Carbon Nanotube-SiO₂ Interface by Electrostatic Force Microscopy. *Journal of Physical Chemistry C*, 113, 15476-15479.
- 5) Li, B., Cao, X., Ong, H.G., Cheah, J.W., Zhou, X., Yin, Z., Li, H., Wang, J., Boey, F., Huang, W., Zhang, H. (2010). All-Carbon Electronic Devices Fabricated by Directly Grown Single-Walled Carbon Nanotubes on Reduced Graphene Oxide Electrodes. *Advanced Materials*, 22, 3058-3061.
- 6) Chen, W., You, L., Chen, G., Chua, N.T., Ong, H.G., Zou, X., Wang, J., Chen, L. (2010). Nanoscale polarization relaxation of epitaxial BiFeO₃ thin film. *Thin Solid Films*, 518, e169-e173.
- 7) Ong, H.G., Cheah, J.W., Zou, X., Li, B., Cao, X.H., Tantang, H., Li, L-J., Zhang, H., Han, G.C., Wang, J. (2011). Origin of hysteresis in the transfer characteristic of carbon nanotube field effect transistor. *Journal of Physics D:Applied Physics*, 44, 285301.