Design of phase locked loop with PVT tolerance

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**DESIGN OF PHASE LOCKED LOOP WITH PVT
TOLERANCE**

**CHONG KOK FOONG
SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING
2012**

DESIGN OF PHASE LOCKED LOOP WITH PVT TOLERANCE

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Summary

Phase lock loops (PLLs) are used to multiply low-frequency clocks to generate clocks that are of high frequency to be used for on-chip synchronous circuits. There has been a constant demand for CMOS general purpose or clock generation PLLs for synchronous chip operation in low (tens ~hundreds of MHz), mid (hundreds ~over GHz) and high (hundreds ~several GHz) frequency ranges. Typical fabless companies would pay royalties per wafer/die or one time charge to make use of such PLLs in 0.25 μ m~28nm CMOS processes provided by major foundries (TSMC, UMC and GLOBALFOUNDRIES). Voltage-controlled oscillator (VCO) is an essential building block for PLLs. Due to the manufacturing limitation and the process variation in fabricating transistors, operating supply voltage and temperature (PVT), the ratio of the VCO frequency at the fastest condition to the slowest condition could change by a factor of 2~3 or even more. As such, significant variation of VCO gain is expected, corresponding to a significant spread in bandwidth for the PLL operation. For the same targeted VCO frequency, the loop bandwidth and stability of the PLL could thus vary greatly due to the variation in the VCO gain across PVT conditions. Also, the upper bound of the usable frequency range is limited to that of the slowest running condition within the tuning voltage range while the lower bound of the usable frequency range would normally be bound by the fastest running condition. This kind of undesired variation limits the designer as he has to design for sub-optimal performance with conservative design parameters to ensure functionality of the PLL for all PVT possibilities.

This thesis proposes a VCO compensation technique that could reduce the VCO's frequency variation across different PVT conditions. The technique incorporates a

simple process variation detection circuit, a comparison circuit that generates digital control codes to control the current that goes to the biasing circuitry of the VCO. The compensation circuitry is of small area and does not consume significant extra power. To verify the proposed compensation techniques in VCO design, a fully-integrated PLL clock generator has been designed for 1GHz~3GHz general purpose clock generation using IBM's 0.13 μ m CMOS 8RF process. With proper selection of the compensation currents (and resistors), the usable frequency range could be extended by a factor of 1.45. For the same targeted frequency, the variation of the compensated K_{VCO} is slightly above 10% at most, reduced from a high value of 60% without compensation. Overall, the bandwidth variation is reduced by a factor of 1.7 from 2.2 for a PLL with compensated VCO, for the whole frequency tuning range, across all the PVT variation from -40°C to 125°C. Specifically, for the same targeted frequency, the K_{VCO} variation has been reduced from a factor of 1.6 to about 1.1. For the same target frequency, the maximum variation in damping factor has been reduced from about 1.3 to slightly over 1.05. The frequency variation with respect to the same control voltage is reduced to $\pm 3.9\%$ across all the PVT variation from -40°C to 125°C.

VCO dummies are normally added to the VCO in order to provide a uniform loading for each VCO delay stage. To check the impacts of different VCO dummy implementation on PLL jitter, five experimental charge pump PLLs are simulated with difference only in the dummy stages: (i) no dummy, (ii) simple dummy, (iii) single stage differential dummy, (iv) double stage differential dummy and (v) full differential dummy with the D2S converters. The simulation result shows that with the improved symmetry, the noise contributed by the fluctuation in the VCO bias would have been suppressed correspondingly. As a result, the PLL output clock jitter

could be reduced by increasing the symmetry in the VCO dummies. However, there is a tradeoff for the jitter performance with the power consumption and silicon area.

The PLL designed was simulated with five different loop bandwidths achieved by varying the charge pump currents and a minimum point with best jitter performance is identify to verify the performance of the VCO with compensation. Simulation at the SS and FF corners shows that the jitter performance of the PLL employing compensated VCO is improved compared to the conventional design without VCO compensation. The PLL output frequency range is also shown to be widened due to the extended usable VCO frequency range.

The PLL is simulated for clock generation at 1GHz, 1.4GHz, 2GHz, 2.56GHz and 2.88GHz with the simple dummy and the full dummy configuration, respectively. The long term periodic jitter (simulated with 50k cycles) and power consumption of the designed PLL is compared with the published prior arts that were designed for low jitter and low power clock generation at 1GHz, 1.4GHz and 2GHz. The tradeoff in power consumption and jitter performance of the PLL designed is observed. A low jitter and low power PLL that could be used for general purpose clock generation has been achieved. The simulated jitter and power consumption of the designed PLL is shown to be comparable/better than the prior arts used for comparison. The peak-to-peak long term period jitter (simulated by using the eye diagram composed of 50k cycles of the PLL output clock) achieved is close to or below 2% of the clock period.

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Chapter 1

Introduction

1.1 Motivation

Phase locked loops (PLLs) are used to multiply low-frequency clocks from off-chip to generate clocks that are of high frequency to be used on-chip. There has been a constant demand for CMOS general purpose or clock generation PLLs for synchronous chip operation. Such PLLs come in the frequency range of low-range (10-100's MHz), mid-range (100s MHz - GHz) and the high-range (100sMHz - several GHz). True Circuits Inc. is one company who provides CMOS PLLs that span technology nodes in 0.25 μ m~28nm to major foundries (TSMC, UMC and GLOBALFOUNDRIES) [Appendix A.1]. This work aims to design a high frequency range (1GHz-3GHz) clock generation PLL that could provide wide output frequency range, low power consumption and low jitter performance. The voltage-controlled oscillator (VCO) is an essential circuit for PLLs. Due to the variation of transistors and other passive elements in the manufacturing process, operating supply voltage and temperature (PVT), the ratio of the VCO frequency at the fastest condition to the slowest condition could vary by a factor of 2~3 or even more [1, 2]. As such, significant variation of VCO gain is expected, corresponding to the same scale of spread in bandwidth for the PLL. For the same targeted VCO frequency, the loop bandwidth and stability of the PLL could thus vary greatly due to the variation in the VCO gain. Figure 1-1 shows how the frequency of a conventional VCO varies with respect to the control voltage (V_{CTRL}), from the fastest running process corner (FF) at -40°C to the slowest running process corner (SS) at 125°C. The frequency of the

VCO in nominal process corner or the typical process corner (TT) would be bounded by the FF and SS corners. With this variation, the upper bound of the usable frequency range is limited to that of the slowest running condition within the tuning voltage range, as indicated by the horizontal dashed line in Figure 1-1. The lower limit would normally be bound by the fastest running condition. It is clear that for the same control voltage, the fastest running frequency is more than 30% higher than the slowest one. The VCO gain (K_{VCO}), could vary by more than 60% for the same target frequency, as shown in Figure 1-2. The normalised bandwidth (with respect to the lowest bandwidth in the range) shows that the PLL loop bandwidth could vary by more than 60%, as shown in Figure 1-3(a). The normalised damping factor (with respect to the lowest damping factor) for the PLL could vary by 30%, as shown in Figure 1-3(b).

Figure 1-1 Variation of VCO frequency due to process and temperature

Figure 1-2 Variation of VCO gain due to process and temperature

Figure 1-3 (a) Variation of normalised VCO gain due to process and temperature (b) Variation of normalised damping factor due to process and temperature

Due to the sampling nature of a PLL, a common rule of thumb is to design the loop bandwidth (ω_{BW}) to be less than 1/10 of the reference frequency. Loop bandwidth is proportional to K_{VCO} so the bandwidth selected must satisfy the highest K_{VCO} (FF corner) for a targeted frequency. The damping factor is proportional to the square root of K_{VCO} , so the design has to cater for the lowest K_{VCO} (SS corner) to maintain a minimum damping factor. For a given charge pump current and divider ratio, the resistor and the capacitor values have to be selected based on the lowest possibly

K_{VCO} at the slowest running condition. This could mean a more conservative selection of resistor and capacitor, i.e. larger sizes of resistor and capacitor in the loop filter. Also, it is known that the output phase noise of a PLL associated with the VCO can be reduced by increasing the loop bandwidth. In contrast, a smaller bandwidth is desired in order to filter out the noise that comes from the reference clock. As such, there is an optimum loop bandwidth trading off between these two noise sources. With all these design constraints and the variation in K_{VCO} , a designer is left with limited choices of design margins and more conservative design parameters that guarantee functionality and stability for all possible PVT variation, but at sub-optimal performance. For example, the bandwidth is selected based on the worst-case condition, i.e. the fastest condition, trading off for less optimal bandwidths at other conditions. There is a class of complicated adaptive bandwidth PLL design [1] targeting PVT tolerance on loop bandwidth and damping factors by means of cancelling each other out in the equations or by complex calibration techniques. Nevertheless, a VCO with less variation in K_{VCO} is still beneficial as it helps to design PLL with a narrower range of loop bandwidths as well as the damping factors, apart from the wider tuning range. In this study, the design of a compensation scheme to improve the PVT tolerance of differential VCO is described. A four-stage differential ring oscillator with voltage regulation is employed to achieve the voltage tolerance. Depending on the process corner and temperature, the proposed compensation scheme works by increasing or decreasing the control current accordingly, thereby maintaining the desired frequency. This research focus on an on-chip compensation technique which adjusts the current going to the VCO depending on the process and temperature conditions detected. A charge pump PLL is implemented with this VCO, demonstrating desired advantages as compared to a

conventional VCO without compensation. The different VCO dummy configuration is also explored to determine the lowest jitter design approach.

1.2 Objectives

The major objective of this study is to explore techniques in reducing the effect of PVT variation of VCO on a general purpose clock generator that could be used for the frequencies range of 1GHz to 3GHz. The focus of this research is on the compensation techniques for reducing the frequency and gain variation of a VCO across different PVT corners. With this compensated VCO, a PLL could be designed with relatively constant voltage gain, bandwidth and stability. A relatively optimum jitter performance at a targeted frequency is also made possible with this design technique for process shift to SS and FF corners.

The next objective of the study is to determine ways to make use of the compensated VCO in reducing the output clock jitter of the PLL. A way to make use of the symmetry in the VCO dummy stages to reduce jitter is also explored. Lastly but not the least, the PLLs are designed to achieve low power and low jitter performance that could be readily employed for the general purpose clock generation usage.

1.3 Major contribution of the Thesis

A compensated VCO with improved PVT tolerance has been designed. For the same target VCO frequency, the loop bandwidth and stability could thus vary greatly due to the variation in the VCO gain. By detecting the threshold voltage due to process variation, the control current to the VCO is adjusted accordingly so that the VCO

frequency variation across PVT corners is greatly reduced. The variation of frequency at 25°C is within $\pm 0.6\%$ for the tuning voltage range from 0.4V to 1.5V comparing the fastest to slowest conditions. The variation of frequency at each control voltage point is within $\pm 3.9\%$ across a temperature range of -40°C to 125°C. Overall, the usable frequency range of the compensated VCO has been extended by a factor of 1.4. The VCO sensitivity to power supply noise is reduced by always running the VCO with 1.2V which is generated from a bandgap-based 1.8V voltage regulator. A fully on-chip integrated charge pump PLL clock generator has been designed with this compensated VCO, demonstrating desired advantages as compared to a conventional VCO without compensation. A relatively invariant loop bandwidth and stable PLL has been designed with such VCO compensation techniques. Comparison shows that the proposed VCO compensation technique is indeed better than the prior arts.

Five experimental charge pump PLLs are simulated with difference only in the dummy stages: (i) no dummy, (ii) simple dummy, (iii) single stage differential dummy, (iv) double stage differential dummy and (v) full differential dummy with the D2S converters. The simulation results show that with the improved symmetry, the noise due to fluctuation in the VCO bias could be suppressed correspondingly. As a result, the PLL clock jitter has been reduced by increasing the symmetry in the VCO dummies. Of course, this comes with a tradeoff with increased power consumption and silicon area.

The PLL designed was simulated with five different loop bandwidths, by varying the charge pump currents and a minimum point with best jitter performance is identified to verify the performance of the VCO with compensation. Simulation at the SS and FF corners shows that the jitter performance of the PLL is improved compared to the

conventional design without VCO compensation. The PLL output frequency range is also shown to be widened up due to the extended usable VCO frequency range.

The PLL is simulated for clock generation at 1GHz, 1.4GHz, 2GHz, 2.56GHz and 2.88GHz with the simple dummy and the full dummy, respectively. The long term periodic jitter (simulated with 50khits) and power consumption of the designed PLL is compared with the published prior arts that were designed for low jitter and low power clock generation at 1GHz, 1.4GHz and 2GHz. The simulated jitter and power consumption of the designed PLL is shown to be comparable/better than these prior arts. A low jitter and low power PLL that could be used for general purpose clock generation has thus been achieved.

1.4 Organization of the Thesis

This thesis is divided into five chapters. This first chapter provides an overview, the motivation, the major contribution and the organization of the thesis. In Chapter 2, a review of the PLL design topics in particular the charge pump PLL is presented. Various design challenges for the building blocks and the loop characteristics are described. In Chapter 3, the focus of this research, i.e. the issues of the PVT variation to VCO and hence the PLL performance, are described in details and the proposed compensation techniques are presented. The circuit level schematics of the proposed techniques and the simulation results are compared with prior arts. In Chapter 4, the complete PLL design and the simulation results are presented. The building blocks are described and the simulation results presented. Lastly, the thesis is summarised and concluded in Chapter 5. The potential future works to be further explored and improve on the current work are also recommended in the last section.

Chapter 2

Fundamentals of the PLL

The idea of PLL was introduced in the last century, for synchronous radio detection by H.de Bellescize in France [3]. It was developed then as an alternative to American engineer E. Armstrong's superheterodyne receiver architecture for radio communication. PLLs have many applications. They can be used for narrow bandwidth filter, clock-and-data recovery, skew reduction in digital system, internal clock generation that is locked to an external reference clock, frequency synthesis to generate a stable periodic signal, frequency modulation and demodulation on a carrier. This chapter provides an overview of a PLL system. The basic definition of various PLL systems is presented in Section 2.1. Section 2.2 provides a detailed review of the charge-pump PLL [4] system which is the topic for study throughout this thesis. Some state-of-the-art charge pump PLLs are briefly reviewed in Section 2.3. A brief comment on the performance of different schemes of PLL system with respect to PVT variation is presented in Section 2.4.

2.1 Basic PLL Definition

A basic PLL [Figure 2.1] consists of three essential elements: a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO) [5]. A PLL behaves as a feedback system which compares the input and output phases. A periodic input signal (V_{in}) is compared against the VCO output signal (V_{out}) by the phase detector (PD). The output of the PD is an error voltage (V_{PD}) proportional to the phase difference of V_{in} and V_{out} , i.e. $\Phi_{in} - \Phi_{out}$. V_{PD} is then filtered by the loop filter so that the dc component of it is passed on to control the VCO. The control voltage (V_{CTRL})

varies the VCO frequency until the phases are aligned, i.e. the PLL loop is locked. When locked, the V_{out} still has a small phase error as compared to V_{in} but the average VCO frequency equals to the average frequency of V_{in} .

Figure 2-1 Basic PLL

Based on the definition given by Roland E. Best [6], PLLs can be classified into linear PLL(LPLL), digital PLL(DPLL), all-digital PLL(ADPLL) and software PLL(SPLL). In the LPLL, an analog multiplier is used as the PD, the LF consists of a passive or active RC filter and a VCO. A DPLL is indeed a hybrid device in which the PD is built from a digital circuit but the remaining blocks remain analog. The ADPLL is exclusively consists of digital functional blocks. The SPLL is normally implemented by a hardware platform such as a digital signal processor (DSP) such that the PLL function is realized purely by software. Nikolas [7] classifies the PLLs into three general categories: analog PLL, hybrid PLL, digital PLL based on their implementation. Table 2-1 summarises the classification of PLLs based on the definition given in [6-7], with respect to PD, LF and oscillator.

Table 2-1 Classification of PLLs

[6]	[7]	PD	LF	Oscillator
Linear PLL	Analog PLL	Analog	Resistor, capacitor	Voltage controlled
Digital PLL	Hybrid PLL	Digital	Resistor, capacitor	Voltage controlled
All digital PLL	Digital PLL	Digital	Digital	Digitally Controlled
Software PLL	Digital PLL	Software	Software	Software

Based on the classification defined by [6-7], the charge pump PLL is a digital/hybrid PLL. To avoid confusion with the ADPLL, the charge pump PLL is defined to be a hybrid PLL throughout this thesis.

Figure 2-2 Block diagram of a ADPLL

An ADPLL [Figure 2-2] consists of a time-to-digital converter (TDC), a digital loop filter (DLF), a digitally controlled oscillator (DCO), and a feedback divider [8-9]. The TDC detects the phase difference from the reference clock (RefClk) and the feedback clock (FbClk), and converts it into a digital word proportionally. The DLF filters this data digitally and generates a set of control code to control the DCO. The DLF is a proportional-integral filter realizing the Type-II PLL response. Traditionally, a digital-to-analog converter (DAC) interfaces the DLF to the voltage controlled oscillator (VCO) [10-11]. An alternate approach is to employ a digitized mechanism to vary the frequency in an LC-tank based VCO [12] or inverter-ring oscillator DCO [13]. The simplest TDC is based on a delay line composed of buffers, each with a delay time of T_{DEL} [14]. The resolution of such TDC is limited by the T_{DEL} of each individual inverter, while the detectable range is proportional to the number of delay stages [15]. To achieve finer resolution, methods using Vernier delay line based on difference of delay chains [15-16], scrambling TDC by averaging many consecutive cycles [17] have been developed. A different approach from the TDCs mentioned, is to use a bang-bang phase detector (!!PD) as a 1-bit TDC for its

simplicity [13]. The advantages of the bang-bang phase detector, due to its simplicity and accuracy, exceeds the drawback of nonlinearity and noise in the multi-Gbps regime [18].

Figure 2-3 A charge pump PLL

2.2 Charge Pump PLL and its components

The basic concept of a PLL system and the phase locking operation has been described in Section 2.1. In this section, the basic charge pump PLL and its components are discussed. The block diagram of a basic charge pump PLL is as shown in Figure 2.3. It consists of a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a feedback divider (FBDIV). When locked, the frequency of Clkout is N times the frequency of RefClk. The function and operation of each block is described below.

2.2.1 Phase Frequency Detector

A common PFD block is as shown in Figure 2.3, acting as a functional block that receives two input clock signals and producing control signals that cause the charge pump to perform charging or discharging operation. A PD is insensitive to the frequency differences and may fail to lock when the frequency of the feedback signal is far from the reference signal. This inadequacy in the lock acquisition range can be remedy by using “aided acquisition” whereby the frequency detection is included.

This is achieved by a PFD which detects both the phase and frequency differences. The PFD outputs are denoted UP and DN (down) respectively. The RefClk denotes the reference clock whereas FbClk denotes the feedback clock. Both UP and DN are initially low in State 0. A rising edge of RefClk input causes the UP signal to go high (State I). This indicates that the FbClk needs to be increased, i.e. the VCO needs to run faster in order to match the input reference clock. When the FbClk leads the RefClk and goes high, the DN signals goes to high (State II). This means that the FbClk needs to run slower. When both RefClk and FbClk go high simultaneously, the NAND gate is set low and resets the PFD to the zero state, after passing through a delay stage. In this way, the PFD behaves as a three-state device. Figure 2.4 is a state diagram that depicts the 3-state behavior of a PFD.

Figure 2-4 The 3-state diagram of PFD

Figure 2-5 Operation of a PFD

Figure 2.5 shows the operation of a PFD and reflects the 3-state behavior. Initially, both the frequency and phase of the RefClk and FbClk are not matched. As RefClk leads FbClk, the UP signal is generated to have a faster FbClk (State I). In the adjustment process, FbClk may become leading the RefClk and a DN signal is

generated (State II). Ideally, when a UP pulse is generated, the DN signal should stay flat but in real case, a glitch of DN occurs. The opposite is also true when a DN pulse is generated. The glitch is alright as long as it is short and quick such that the charge pump does not respond to it. The adjustment continues until the phase of FbClk is aligned to the RefClk and their frequency becomes equal. In this stage, the PLL is said to be in “locked” condition.

Figure 2-6 PFD (a)with dead zone (b)ideal and without dead zone

Dead zone occurs when the loop does not respond to small phase errors at PFD inputs [Figure 2.6]. This causes undesired jitter and phase noise at the output clock. There is a limited amount of pulses that the PFD can generate. Also, the charge-pump cannot be turned on and off in such a narrow time frame. A delay is normally introduced in the reset path in order to guarantee a minimum pulse width that remedies the dead-zone problem. However, widening the reset pulse increases the time where both UP and DN are high and the charge pump conducts simultaneously. This has undesired effect on the VCO control voltage and phase noise. If the dynamic flip flops (DFFs) are not properly matched and that one reset is faster than the other, the reset signal will be pulled to low and not able to reset the slower DFF.

2.2.2 Charge Pump

The charge pump (CP) circuit has two switches that are controlled by the UP and DN signals from the PFD. The charge pump then pumps current pulses that either add or remove charges from the loop filter capacitor (C_{CP}). In this sense, the C_{CP} converts a digital signal (the PFD phase error) to an analogue signal (charge). The combination of charge-pump and the capacitor C_{CP} acts as an integrator that generates the average of UP or DN pulses. The CP converts the phase difference to this average voltage proportionally and feed into the VCO to adjust the frequency.

A linear continuous-time approximation is often used to model the simple charge pump PLL. The error due to approximation is negligible if the PLL band-width is 1/10 or smaller than the reference clock frequency [4]. The average current charging or discharging the capacitor is given by $I_{AVG}=I_{CP} \times (\Phi_{UP}-\Phi_{DN})/2\pi$. There are four main undesired effects which could cause reference spur and need careful consideration [19-22]. These are (i) leakage current in the loop filter, (ii) timing skew between the UP and DN signals, (iii) current mismatch in the charge up and down current path, (iv) charge sharing. The leakage currents could come from the capacitor of the loop filter, the charge pump itself. The gate leakage would readily manifest itself if MOS capacitor is incorporated in the loop filter design [23]. When the charge pump is in off state, the leakage current could discharge the loop filter. This drain off the current from the loop filter causing a phase offset. Gate leakage current is becoming more significant as the technology continues to shrink and as the gate dielectric thickness reduces.

Figure 2-7 (a) Charge pump (b) timing mismatch of UP' and DN (c) timing balance by inserting a pass gate

Figure 2.7 shows the mechanism of the timing mismatch and its effect. As mentioned in the Section 2.21, the dead-zone issue could be fixed by putting a delay in the reset path of the PFD. This forces the UP and DN signals of the PFD to be “on” simultaneously for a short period in each cycle when the PLL is in lock condition. For a conventional charge pump, the UP signal is inverted to generate UP' to turn on the charging current as the PMOS transistor switch is active low. This introduces a mismatch in the pulse arrival time for the UP' and DN. A periodic disturbance to the control voltage is thus generated and causes reference spur in the VCO output. One possible ways to get rid of this mismatch is by inserting a transmission gate in the DN control path. The delayed signal DN' should arrive with negligible skew with the UP signal provided the transmission gate is sized properly. The issue of current mismatch could still occur even with the UP and DN' signals aligned perfectly [19-21, 24]. The current mismatch varies with the control voltage due to the finite output impedance of the CMOS current source. This current mismatch also generates a phase offset which contributes to the spur of the PLL output. The contributions to the phase offset by the leakage current, timing mismatch and the current mismatch in the charge pump is expressed as [20, 24]

$$\Phi_{\varepsilon} = 2\pi \left[\frac{I_{\text{leak}}}{I_{\text{CP}}} + \frac{\Delta t_{\text{on}}}{T_{\text{ref}}} \frac{\Delta t_{\text{d}}}{T_{\text{ref}}} + \frac{\Delta t_{\text{on}}}{T_{\text{ref}}} \frac{\Delta i}{I_{\text{cp}}} \right] \quad [\text{rad}] \quad (2.1)$$

where Φ_ε , I_{leak} , I_{CP} , Δt_{on} , T_{ref} , Δt_d , Δi are the phase offset, the leakage current, the charge pump current, the turn on time of the PFD, the reference clock period, the delay mismatch, and the current mismatch of the charge pump, respectively. The Δt_d is much smaller than the Δt_{on} for this expression to be valid. The reference spur in a 3rd-order PLL is given approximately by [20, 24]

$$P_r = 20 \log \left[\frac{\sqrt{2}(I_{\text{CP}} R / 2\pi) \Phi_\varepsilon K_{\text{VCO}}}{2f_{\text{ref}}} \right] - 20 \log \frac{f_{\text{ref}}}{f_{p1}} \quad [\text{dBc}] \quad (2.2)$$

where R denotes the resistor value in the loop filter, K_{VCO} denotes the VCO gain, f_{ref} denotes the reference frequency of the PFD and f_{p1} denotes the frequency of the pole in the loop filter. Equation (2.1) and (2.2) imply that Δt_{on} , Δi should be reduced to minimize the phase offset, as Δt_d is much smaller than the Δt_{on} and I_{leak} is more due to the process constraint. Nevertheless, Δt_{on} is required to get rid of the dead-zone issue. With these observations, it is obvious that the current mismatch should be reduced as much as possible. The deterministic jitter, Δ_{det} , can be estimated from the reference spur based on Fourier series analysis [25-26] and is given by an expression

$$\Delta_{\text{det}} = T_{\text{out}} 10^{\text{Spur (dBc)}/20} \quad (2.3)$$

where T_{out} is the ideal output period, Spur is the level of the reference spur in unit of dBc.

Figure 2-8 (a) Charge pump OFF (b) Charge sharing (c) Bootstrapping

Charge redistribution occurs when charge pump move from the OFF to ON state. As shown in Figure 2.8(a), when the charge pump switches are turned off, the voltage at node X (V_X) is discharged to ground through the parasitic capacitance C_{pd} and the voltage at node Y (V_Y) is charged to V_{DD} through the parasitic capacitance C_{pu} . When the charge pump switches are turned on again, V_Y drops and the V_X increases and eventually $V_X \approx V_Y \approx V_{CTRL}$ [Figure 2.8(b)]. This charge redistribution effect is undesired as it causes a voltage jump in V_{CTRL} . A bootstrapping technique can be used to reduce this charge sharing effect [19-20, 27, 28]. A unity-gain amplifier is used to hold node X and node Y at a potential equal to V_{CTRL} when they are not switched to V_{CTRL} . When the switches are turned on again, the node X and node Y start with a potential that is equal to the V_{CTRL} as from the previous phase comparison stage. In this way, the charge sharing between the loop filter and the parasitic capacitances is avoided.

2.2.3 Voltage-Controlled Oscillator

Voltage-controlled oscillator (VCO) is the most critical component in a PLL. As its name suggests, a VCO generates a periodic signal with a frequency that depends linearly on the input control voltage (V_{CTRL}) and eventually achieve the phase-locked state. A CMOS VCO could be implemented with ring oscillators, relaxation circuits, and LC resonant circuit. In a LC oscillator, a variable capacitor is typically employed to tune the frequency given by $1/(2\pi\sqrt{LC})$. The LC oscillator demonstrates the best phase noise performance [29]. However, the ring oscillator has the advantages of area that is more compact, less design complexity, wider tuning range that spans orders of magnitude [30-31]. In today's mixed-signal ICs, the ring oscillator has been the most widely fabricated as compared to other oscillators. In this study, the ring

oscillator VCO is used. Thus, the following sections focus review on CMOS ring oscillator. There are two types of ring oscillators. One is based on the inverters and the other is based on differential delay cells and is less susceptible to noise. The advantages of CMOS based delay buffers are their simplicity, portable design and their relaxed supply headroom requirements. Their main disadvantage is their high control-voltage to delay gain which is typically 1% of delay per 1% of regulated supply/control voltage.

The most basic ring oscillator design consists of a chain of single ended inverters. In this configuration, a total odd number N of inverter stages is needed so that the oscillator does not latch up at a DC level [19]. For stable oscillation, the gain magnitude of the loop should be greater than or equal to one and the total phase difference should fulfill the Barkhausen criterion, i.e. equal to a multiple of 2π [19, 32]. The two conventional criteria for oscillation is shown to be “necessary but not always sufficient” for oscillators, due to the effects of parasitic elements [32]. As such, the loop gain is typically chosen to be at least twice the required values [19]. With a linearised model [29, 33], the basic loop of the ring oscillator is redrawn in Figure 2.9. R and C denote the output resistance and the capacitive load of each of the delay stages; $G_m R$ denotes the gain required for a stable oscillation.

Figure 2-9 Linear model of a CMOS ring Oscillator

A good explanation relating the phase, gain and oscillation frequency was provided in [33] and is adapted here for illustration. The loop gain $G_L(s)$ is defined as

$$G_L(s) = H_1(s)H_2(s)H_3(s) \dots H_N(s) \quad (2.4)$$

where $H_N(s)$ is the transfer function of each stage in the s-domain. In practice, the gain of each stage is identical, i.e. $H_1(s) = H_2(s) = H_3(s) = H_N(s) = H(s)$, such that

$$G_L(s) = H(s)^N \quad (2.5)$$

To fulfill the Barkhausen criterion, each single stage should provide a phase shift of $2k\pi/N$ at the unity gain frequency, where k is an integer. Thus, we have

$$\angle H(j\omega_0) = 2k\pi/N \quad (2.6)$$

$$|H(j\omega_0)|^N = 1 \quad (2.7)$$

Each stage has a phase shift of $(\pi+\theta)$, where π comes from the DC inversion and θ from the RC load (frequency dependent phase shift). To minimize the required phase shift and thus the number of delay stages, the total frequency dependent phase shift should be equal to $\pm\pi$, i.e. $N\theta=\pm\pi$. The transfer function and the phase of a single stage at the oscillation frequency ω_0 is given by

$$H(j\omega_0) = \frac{-G_m R}{1+j\omega_0 RC} \quad (2.8)$$

$$\angle H(j\omega_0) = -\tan^{-1}(\omega_0 RC) \pm \pi \quad (2.9)$$

The phase shift contributed by each stage is thus given by

$$\theta = -\tan^{-1}(\omega_0 RC) \quad (2.10)$$

and the oscillation frequency is given by

$$\omega_0 = \frac{\tan \theta}{RC} \quad (2.11)$$

The gain requirement is given by (2.7)

$$|H(j\omega_0)|^N = \left[\frac{G_m R}{\sqrt{1 + (\omega_0 RC)^2}} \right]^N = 1 \quad (2.12)$$

With some derivation steps, the gain requirement is given by

$$G_m R \geq 1/\cos \theta \quad (2.13)$$

For a three-stage ring oscillator, the frequency and gain is thus calculated to be $\sqrt{3}/RC$ and 2 using (2.11) and (2.13) respectively, where $\theta = \pi/3$.

Differential ring oscillators are preferred over the single-ended because of their better immunity to power supply disturbance [31] and other inherent advantages like improved spectral purity, better duty cycle and can be constructed with either even/odd stage of delay cells. Some state of the arts PLL had been designed using differential VCO with different classical differential delay cells are [30, 34-37]. For an even stage differential VCO, the extra phase shift (π) can be obtained by configuring one stage such that it does not invert [19]. Figure 2.10 shows a four-stage differential VCO where the fourth and the first stage are not inverted.

Figure 2-10 (a) Four-stage differential VCO (b) Simple differential stage

Assuming each stage of a N-stage differential ring oscillator provides a delay of t_d , then the period is $2NT_d$ as the signal needs to go through each of the delay stages

twice to provide a period of oscillation [38-39]. The oscillation frequency is thus given by

$$f = 1/2NT_d \quad (2.14)$$

The delay per stage can be expressed as $C_L V_{SW} / I_{SS}$ [30, 39] where C_L is the load capacitance of the delay stage, V_{SW} the peak-to-peak voltage swing and I_{SS} is the tail current used in the delay stage, respectively. The oscillation frequency is given by

$$f = \frac{I_{SS}}{2NC_L V_{SW}} \quad (2.15)$$

This is only suffice for a quick estimation of the oscillation frequency while a more comprehensive analytical equation is provided by [39] whereby the effect of varying parasitic is included and the effect of gate resistance at high frequency is also being considered. Important parameters in the VCO design are phase noise, jitter, centre frequency, tuning range and linearity. For the monotonic relationship to be applied over a large frequency range, the K_{VCO} needs to be reasonably constant. Important concerns in the design of low-jitter VCO are the variations of the output phase and frequency as a result of noise on the control lines and the power supply.

Figure 2-11 (a) Manetis delay cell (b) Hong Park delay cell (c) Lee-Kim delay cell

Three classical differential delay cells, Manetis delay cell [34, 37], Hong Park delay cell [36] and Lee-Kim delay cell [35] are as shown in Figure 2.11 (a), (b) and (c) respectively. Manetis delay cell is perhaps by far the most popular differential delay cell being studied and adapted. It consists of a pair of symmetric loads by diode-connecting the PMOS device in parallel with a PMOS of equal size. The bias voltage V_{bp} would define the lower limit of the voltage swing. The tail current is generated by biasing the bottom NMOS with V_{bn} . Hong Park delay cell is a fully switching (full turn-on and full turn-off) differential delay cell and has been reported with a good phase-noise performance. The cross-coupled PMOS pair, M18 and M19 of the Lee-Kim delay cell guarantees the differential operation without a tail current. M16 and M17 control the frequency. Its output signal swings from rail-to-rail so no level shifter is required. Both Hong Park and Lee-Kim cells are able to produce sharpened output signal edges that help to reduce the VCO jitter [36]. In this research, Manetis delay cells are used for its simplicity, linearity and are more suitable for the proposed VCO design with compensation.

2.2.4 Frequency Divider

Usually, the PLL reference clock is generated from a crystal which is a very clean clock source. This kind of crystal spans from tens to a few hundreds of MHz. In contrast, the VCO operates at a hundreds of MHz to GHz range. As such, a frequency divider is needed to bring down the frequency of the VCO output to match that of the reference clock.

2.2.5 Loop Characteristics of PLL

Figure 2-12 Linear model of a charge pump PLL

Neglecting the sampling nature, the dynamic behaviour of a typical charge pump PLL can be analyzed using a linear model as shown in Figure 2.12. Following the s-domain analysis approach in [3] and [19], the gain of the PFD and charge pump is given by K_{PD} in A/rad, the loop filter transfer function $F(s)$ in Ω . The K_{VCO} is the VCO gain of the VCO in rad/s/V and an integrator $1/s$ is included as the VCO phase is obtained by integration of the frequency. N is the division ratio of the feedback divider. K_{PD} is given by $I_{CP}/2\pi$ where I_{CP} is the charge pump current. $F(s)$ is the impedance function of the loop filter in s-domain. C_P is being charged or discharged and hence providing the required V_{CTRL} for gradual frequency correction of the loop. R_Z provides a stabilizing zero for the stability of the loop. The parallel capacitor, C_R is used to reduce the ripple and is usually one-tenth or less of C_P . The forward loop gain of the linear model is given by

$$H_{fwd}(s) = \frac{\Phi_{out}(s)}{\Phi_{err}(s)} = K_{PD} F(s) \frac{K_{VCO}}{s} \quad (2.16)$$

The reverse loop transfer function is given by

$$H_{rev}(s) = \frac{\Phi_{Fb}(s)}{\Phi_{out}(s)} = \frac{1}{N} \quad (2.17)$$

The open loop transfer function is given by

$$H_{open}(s) = H_{fwd}(s) \cdot H_{revf}(s) = \frac{K_{PD} F(s) K_{VCO}}{Ns} \quad (2.18)$$

Figure 2-13 Noise contribution in a linear PLL model

The closed loop transfer function is given by

$$H_{closed}(s) = H_{in}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{H_{fwd}(s)}{1 + H_{rev}(s)H_{fwd}(s)} = N \frac{H_{open}(s)}{1 + H_{open}(s)} \quad (2.19)$$

It is useful to consider the noise contributions from each block of the PLL to the overall phase noise. Phase noise contributed by the input reference is equivalent to the closed loop transfer function of the PLL (2.19). It is a low pass transfer function with a DC gain of N. This means that the 3dB corner frequency (the bandwidth) of the PLL has to be small enough in order to filter out the reference noise.

In contrast to this, the transfer function of the VCO noise is given by

$$H_{VCO}(s) = \frac{\Phi_{out}(s)}{\Phi_n(s)} = \frac{1}{1 + H_{open}(s)} \quad (2.20)$$

This is a high-pass transfer function meaning that high frequencies noise from the VCO is passed onto the PLL output while the VCO noise of low frequencies could be filtered out. The PLL bandwidth should thus be increased to reduce the phase noise contribution from the VCO. Similar transfer functions can be derived for the noise injected by PFD/CP, $i_{PD}(s)$, the loop filter noise $v_{nf}(s)$ and the feedback divider noise $\Phi_{fb}(s)$. These transfer functions are given respectively by

$$H_{PD}(s) = \frac{\Phi_{out}(s)}{i_{PD}(s)} = \frac{N}{K_{PD}} \frac{H_{open}(s)}{1+H_{open}(s)} \quad (2.21)$$

$$H_{nf}(s) = \frac{\Phi_{out}(s)}{v_{nf}(s)} = \frac{K_{vco}}{s} \frac{1}{1+H_{open}(s)} \quad (2.22)$$

$$H_{fb}(s) = \frac{\Phi_{out}(s)}{\Phi_{fb}(s)} = N \frac{H_{open}(s)}{1+H_{open}(s)} \quad (2.23)$$

Like the $H_{in}(s)$, the transfer function of the PFD/CP noise ($H_{fb}(s)$) is also a low pass function. It differs from $H_{in}(s)$ by a factor of K_{PD} .

The loop filter transfer function, $F(s)$ is given by $(R_Z + 1/sC_P)/(1/sC_R)$ and can be simplified to

$$F(s) = \frac{1+sT_Z}{s(C_P+C_R)(1+sT_P)} \quad (2.24)$$

where $T_Z = R_Z C_P$ and $T_P = R_Z C_P C_R / (C_P + C_R)$. The open loop transfer function is then

$$H_{open}(s) = \frac{K_{PD} K_{vco}}{Ns^2} \frac{1+sT_Z}{(C_P+C_R)(1+sT_P)} \quad (2.25)$$

Figure 2.14(a) shows an example of the gain and phase of the open loop transfer function. This is a typical third order PLL response whereby there are two poles at the origin and the third pole at the far right end. The third pole is given by $\omega_P = 1/T_P$ and the stabilizing zero given by $\omega_Z = 1/T_Z$. The cross over frequency, ω_C is the open

loop unity gain frequency, i.e. where $H_{open}(s) = 0\text{dB}$. In real design, the analysis could be simplified to a second order one, assuming that the ripple capacitor, C_R is much smaller than the main capacitor, C_P and have no impact on the stable operation [40, 41]. With this assumption, the bode-plot in Figure 2.14 (a) is reduced to the one as shown in Figure 2.14(b). The equation (2.24) is thus simplified to

$$H_{open}(s) = \frac{K_{PD} K_{VCO} R}{N s} \left(1 + \frac{1}{s T_Z} \right) = \frac{\omega_C}{s} \left(1 + \frac{\omega_Z}{s} \right) \quad (2.26)$$

where $\omega_C = (K_{PD} K_{VCO} R / N)$ and $\omega_Z = 1 / R_Z C_P$.

Figure 2-14 (a) Gain and phase plots of the open loop transfer function, third order (b) gain and phase plots of the open loop transfer function, second order (ignore C_P)

The relationship of the damping factor (ζ) and natural frequency (ω_n) of the PLL with respect to the design parameters, K_{PD} , K_{VCO} , C_P , R_Z and N can be derived from the closed loop transfer function (2.19) as

$$H_{in}(s) = N \frac{H_{open}(s)}{1 + H_{open}(s)} = \frac{K_{PD} F(s) (K_{VCO} / s)}{1 + \frac{1}{N} K_{PD} F(s) (K_{VCO} / s)} = \frac{\frac{K_{PD} K_{VCO}}{C_P} (1 + s C_P R_Z)}{s^2 + \left(\frac{K_{PD} K_{VCO}}{N C_P} R_Z C_P \right) s + \frac{K_{PD} K_{VCO}}{N C_P}} \quad (2.27)$$

Comparing this to the classical second-order equation of $(\omega_n^2)(s^2 + 2\zeta\omega_n s + \omega_n^2)$, ω_n and ζ can be derived as

$$\omega_n = \sqrt{\frac{K_{PD} K_{VCO}}{C_P N}} \quad (2.28)$$

$$\zeta = \frac{1}{2} \frac{\omega_n}{\omega_Z} = \frac{R_Z}{2} \sqrt{\frac{K_{PD} K_{VCO}}{C_P N}} \quad (2.29)$$

The equation (2.27) is a second-order transfer function with one zero and two poles. Further assumption can be made for PLL with damping factor larger than 1. In this case, the ω_Z effectively cancels out one pole and leaves the other pole that is at the farthest right to set the closed-loop bandwidth [41]. Importantly and conveniently, this gives the approximate expression for the -3dB closed-loop bandwidth as functions of ζ and ω_n by

$$\omega_{-3dB} \approx 2\zeta\omega_n = \frac{R_P K_{PD} K_{VCO}}{C_P N} = \omega_C \quad (2.30)$$

With the closed-loop bandwidth established, the various noise transfer functions from (2.19) to (2.23) could be rewritten in ω_Z and ω_C/ω_{-3dB} with the $H_{open}(s)$ expression in (2.26) as

$$H_{in}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = N \frac{H_{open}(s)}{1+H_{open}(s)} = N \frac{\omega_C(s+\omega_Z)}{s^2+\omega_C(s+\omega_Z)} \quad (2.31)$$

$$H_{VCO}(s) = \frac{\Phi_{out}(s)}{\Phi_n(s)} = \frac{1}{1+H_{open}(s)} = \frac{s^2}{s^2+\omega_C(s+\omega_Z)} \quad (2.32)$$

$$H_{PD}(s) = \frac{\Phi_{out}(s)}{i_{PD}(s)} = \frac{N}{K_{PD}} \frac{H_{open}(s)}{1+H_{open}(s)} = \frac{N}{K_{PD}} \frac{\omega_C(s+\omega_Z)}{s^2+\omega_C(s+\omega_Z)} = RK_{VCO} \frac{\omega_C(s+\omega_Z)}{s^2+\omega_C(s+\omega_Z)} \quad (2.33)$$

$$H_{nf}(s) = \frac{\Phi_{out}(s)}{v_{nf}(s)} = \frac{K_{VCO}}{s} \frac{1}{1+H_{open}(s)} = K_{VCO} \frac{s}{s^2+\omega_C(s+\omega_Z)} \quad (2.34)$$

$$H_{fb}(s) = \frac{\Phi_{out}(s)}{\Phi_{fb}(s)} = N \frac{H_{open}(s)}{1+H_{open}(s)} = N \frac{\omega_C(s+\omega_Z)}{s^2+\omega_C(s+\omega_Z)} \quad (2.35)$$

Intuitively, the transfer functions allow the overall phase noise characteristics of the PLL to be revealed. As $\omega \rightarrow \infty$, the $H_{in}(s)$, $H_{PD}(s)$, $H_{nf}(s)$ and $H_{fb}(s)$ are all $\rightarrow 0$ while $H_{VCO}(s) \rightarrow 1$. Note that the noise of the feedback divider appears directly at the input of the PFD and thus is equivalent to the noise transfer function of the input reference. At low frequency, they both contribute a factor of $20\log_{10}N$ to the PLL output. At high frequency, the noise of the PLL is mainly contributed by the VCO. This is also intuitively true as the loop filter would have blocked the feedback at the high frequency range. The expression of $H_{nf}(s)$ suggests that noise contribution from the loop filter could possibly be reduced by lowering the magnitude of the VCO gain. Figure 2-15 Magnitude of noise transfer function, an example shows the magnitude of the noise transfer functions from $H_{in}(s)$, $H_{VCO}(s)$ and $H_{nf}(s)$. Representatively, $H_{in}(s)$ is a low pass function, $H_{VCO}(s)$ is a high pass function and $H_{nf}(s)$ is a band pass transfer function. The plot is created with example of design parameters: $RZ=4.4k\Omega$, $CP=58pF$, $CR=1.8pF$, $K_{PD}=60\mu/2\pi[A/rad]$, $K_{VCO}=2\pi \cdot 2.65M[rad/sV]$.

In general, for PLL with large input reference noise (like clock and data recovery application) to be filtered, a lower loop bandwidth may be desired. For application like clock generator and frequency synthesizer that comes with large VCO noise, a

Figure 2-15 Magnitude of noise transfer function, an example

high loop bandwidth is desired so that the VCO phase noise can be reduced resulting in better jitter performance. Theoretical and experimental works had been done in the past to verify the relationship between phase noise, loop bandwidth and timing jitter [40, 42]. It was shown in [40] that the timing jitter is a concave function with respect to loop bandwidth and that the timing jitter increases either beyond or below the optimum bandwidth. [42] suggests that damping factor should be equal to or greater than one to avoid jitter response ringing; long term jitter will converge to $\kappa \cdot \sqrt{1/(2\zeta\omega_n)}$ where κ is a time domain figure of merit depending on the VCO design.

The strategy of the PLL designed in this work will make $C_P \gg C_R$, $\zeta \geq 1$, high loop bandwidth and taking advantages of the proposed VCO designed with compensation such that the K_{VCO} (and thus the loop bandwidth) is relatively constant across PVT conditions for a targeted frequency.

2.3 State-of-the-art Charge Pump PLL review

In this section, some state-of-the-art charge-pump PLLs are reviewed, including those used for comparison of performance at Chapter 4.

2.3.1 Supply Noise Mitigation Techniques

To mitigate the supply noise effect on charge-pump PLLs, two major supply noise suppressing techniques have been developed: supply regulation techniques [43-46] and supply noise cancellation [47-49]. Supply regulation techniques focus primarily on suppressing the supply noise in the ring oscillator. Noise cancellation works by cancelling (in reality, this could only be reducing) the noise effect from the VCO.

Figure 2-16 shows the block diagram of a supply-regulated PLL. The control voltage for the VCO is applied to its supply through a low drop-out regulator. The regulator shields the noise from reaching VCO and hence increases the power supply noise rejection (PSNR) for it. It was reported in [44] that the regulating loop attenuates supply steps by more than a factor of 15, achieving a worst case supply sensitivity of less than 0.06%-delay/1%-supply.

Figure 2-16 Block diagram of supply-regulated PLL

Figure 2-17 Block diagram of a PLL with supply-noise cancellation

Figure 2-18 VCO with noise-cancelling circuit

Figure 2-19 Compensated clock buffer

Figure 2-19 shows the block diagram of a classical charge pump PLL designed with supply-noise cancellation [47]. The VCO is composed of a voltage to current (V-I)

converter, a current-controlled oscillator (CCO) and a noise-cancelling circuit. A compensation circuit is used with the inverse delay sensitivity to supply noise to cancel the delay variation of the inverter. The output signal of the VCO passes through a low-to-full swing (L-F) amplifier and feeds back to the phase-frequency detector (PFD) through a divider. The V-I converter converts V_{CTRL} to current (I_{DRV}). The noise-cancellation circuit (M_{p5} , M_{n4} , M_{n5}) is added to compensate for the residual variation of the output current I_{DRV} due to supply noise. The circuit generates a compensation current I_{comp} by mirroring a fraction of I_0 . I_{comp} is then subtracted from I_{DRV} . The VCO achieves a supply-noise rejection of $\leq 0.035\% - f_{VCO}/1\% \cdot V_{DD}$. A source follower transistor (M_{n3}) is used to compensate for the gain drop at high V_{CTRL} . The source follower is OFF for $V_{CTRL} - V_{CCO} < V_{Th3}$ and gradually turns ON at high V_{CTRL} , which injects current I_{SF} and compensates for the I_{DRV} drop. A variable capacitor, composed of a PMOS resistor in series with a capacitor, is placed at the output of each inverter used in the clock buffer [Figure 2-19]. As the power supply drops, the capacitor value also drops to compensate for the inverter delay increase and vice versa. The gate voltage of the PMOS resistor is set to a constant voltage level derived from a bandgap-based circuitry.

Figure 2-20 (a) VCO with supply-noise compensation (b) VCO delay cell

Figure 2-21 PLL with on-chip calibration

[48] reported a charge-pump PLL capable of reducing the supply voltage sensitivity of the VCO using on-chip calibration [Figure 2-21]. In the presence of a 10-mV 1-MHz VCO supply noise, the measured rms jitter of this PLL is 3.95ps at a 1.4-GHz operating frequency, while a conventional design measures 8.22ps rms jitter. One advantage of this design is that it avoids the use of supply regulation, a desirable feature for the design of low-voltage VCOs. When the supply voltage increases, the voltage V_B increases, causing M_{n1} and M_{n2} to sink more current to ground [Figure 2-20]. This mechanism slows down the VCO and thus compensates for the increase in the VCO frequency due to increase in the VCO supply voltage. Ideally, the VCO supply sensitivity would be reduced to zero if the increase in the currents of M_{n1} and M_{n2} is the same as the increase in the current of the PMOS transistor, M_0 . With the help of M_1 - M_3 , calibration is done by comparing V_{Ctrl} and V_{Cpo} during the calibration cycle. A 5-bit control code is determined via a successive approximation register (SAR). This code sets the ideal current such that it minimise the effects of the variation in the supply voltage to the VCO frequency.

2.3.2 Adaptive BW Design

PVT variation may alter the optimal closed loop bandwidth of a PLL by as much as $\pm 40\%$ [50]. Adaptive bandwidth PLLs refer to a class of PLLs that scale their loop dynamics proportionally with the reference frequency so as to enable optimal performance over a wide frequency range and across PVT variations [1]. Various circuit techniques to realize adaptive bandwidth have been developed [34-35, 37]. [37] achieves adaptive bandwidth by maintaining a fixed loop-bandwidth-to-reference-frequency ratio and damping factor. [34] improves on the architecture of [37] with a new loop filter structure that produces constant loop dynamics that scale with reference frequency independent of multiplication factor. [35] adaptively controls the loop bandwidth according to the locking status and the phase error amount, based on an analog recursive bandwidth control algorithm. [51] reports a process-independent adaptive bandwidth spread-spectrum clock generator (SSCG) with digitally controlled self-calibration techniques. A more detailed review is briefly presented for [34] here.

Figure 2-22 shows the self-biased charge-pump PLL architecture reported by Maneatis[34]. This architecture aims to maintain a constant bandwidth-to-reference-frequency ratio and the damping factor. Rather than a fixed resistor in series with a capacitor, a $1/g_m$ resistance can be formed from the small-signal resistance of the diode-connected device in the VCO bias generator. The g_m is proportional to the square root of the buffer bias current. The oscillation frequency is also proportional to the square root of the buffer bias current. The charge pump current is scaled inversely with the multiplication factor N . Instead of a single charge pump, two separate charge pumps are used to drive the capacitor and resistor separately, where the voltages are summed inside the VCO bias generator. The path with the resistor is

Figure 2-22 Block diagram of self-biased PLL

Figure 2-23 VCO circuits of the self-biased PLL

called the proportional or feedforward signal path. The feedforward filtering is performed by sampling the phase error and generating a proportional current that is held constant for N output cycles. This feedforward current produces a correction voltage across the $1/g_m$ resistor inside the bias generator, where it is summed with the control voltage. A reset switch is used to resets the capacitor voltage at the feedforward path to zero at the end of the reference cycle before the next phase comparison. The detailed mathematical analysis in [34] shows that the bandwidth-to-reference-frequency ratio and the damping factor are given by

$$\frac{\omega_n}{\omega_{REF}} = \frac{1}{2\pi} \sqrt{\frac{C_B}{C_1}} \quad (2.28)$$

$$\zeta = \frac{1}{4} \sqrt{\frac{C_B C_{12}}{C_2}} \quad (2.29)$$

where C_B is the equivalent VCO capacitance and $C_{12}=C_1+C_2$. Both equations depend solely on the ratio of capacitances which can be matched. They are also independent of the output frequency, N , as well as process, voltage and temperature.

2.3.3 Resistorless PLL design with sample-reset technique

A resistor is required in the loop filter to stabilize the closed loop response of the PLL; however, the loop filter voltage ripple due to the filter's resistor causes objectionable reference spurs [50]. This reference spur can be reduced by adding a second pole (a capacitor to attenuate the ripple) to the loop filter. An alternate technique is to employ sample-reset loop filter architecture [52-54] that is resistorless. The loop components can be split into integral (associated with the main capacitor) and proportional (associated with the main resistor) terms. The sample-

reset loop filter injects an appropriately scaled constant current during the entire input update period, replacing the conventional large proportional current during the input phase difference [52]. This ripple attenuation leads to a improvement in the PLL output jitter performance.

Figure 2-24 Charge-pump PLL implemented with sample-reset technique

Figure 2-24 shows the block diagram of a charge-pump PLL with sample-reset architecture [53]. CK_{even} is running at half the frequency of reference clock (f_{REF}). CK_{odd} is run at the same frequency as CK_{even} but at opposite polarity. When CK_{even} is high, C_{s1} shares charge packet corresponding to the previous phase comparison with C_1 while C_{s2} samples a level proportional to the present phase difference. During the next period, C_{s1} and C_{s2} exchange roles. In this way, an “equivalent resistor” is formed, providing a precise stabilizing zero for the loop filter. It is derived in [53] that, if $(I_{p1}+I_{p2})/I_{p1}=1-\alpha$ then C_2 is essentially “amplified” by $(1-\alpha)^{-1}$, saving substantial silicon area. Also, the zero frequency is given by

$$\omega_z = \left(1 + \frac{I_{p2}}{I_{p1}}\right) \frac{C_s}{C_2} f_{REF} \quad (2.28)$$

a value which is independent of process and temperature.

2.3.4 Miscellaneous

[55] describes a low-jitter charge pump PLL using a gain compensation VCO. The block diagram of the PLL is omitted as it is composed of a standard charge pump PLL architecture. The key innovation in this design is the VCO in which three V2I converters are used and their different characteristics blended [Figure 2-25]. This VCO has a low gain and a good linearity, features desired for low jitter PLL. [55] gives that $I_{CCO} = k(V_{cont}-V_t)^{\alpha} + k(V_{cont}-V_t-V_a) + k(V_{dd}-V_t)^{\alpha} - k(V_{dd}-V_{cont}-V_t)$ where V_a is the offset bias voltage in the VIC2. The equation indicates that the CCO current increases beyond V_t+V_a and lower than V_t , extending the input range at the higher and lower control voltage respectively. A low gain and a linear VCO is achieved with these key features.

Figure 2-25 Gain compensation VCO

2.4 Review of VCO with PVT tolerance

[56] makes use of a separate VCO calibration block to perform calibration against a dedicated calibration clock then producing digital words to adjust the values of the loading capacitors of the VCO (powered by a regulated supply for power supply noise immunity), thereby achieving the desired VCO output frequency [Figure 2-26].

Figure 2-26 PLL with VCO calibration block

Figure 2-27 (a) VCO delay cells (b) VCO calibration block

Initially, if the power is supplied, the PLL enters calibration mode. MUX1 selects the INT_CLK and CALIB_CLK as input of the PFD. MUX2 selects in a way that connect CAL_VOLTAGE to VCTRL and LOOP_VOLTAGE to CTRL_CAP respectively. The VCO is designed to provide initial higher frequency than the CALIB_CLK. As a result, the PFD produces UP signal and increases the CTRL_CAP voltage, increasing the effective loading capacitance and reducing the VCO frequency. This feedback continues until INT_CLK is same to EXT_CLK.

After calibration mode, MUX1 selects the input of the PFD to EXT_CLK and INT_CLK while MUX2 connects VCTRL to the LOOP_VOLTAGE. The VCO calibration block reads the voltage of CTRL_CAP by the DAC after calibration and force the voltage of CTRL_CAP to be the DAC_OUT voltage. In this way, the VCO is calibrated with the calibration clock and is set to the desired VCO gain (by setting appropriate CTRL_CAP voltage), irrespective of the PVT variation.

In [57], a faster 3-stage oscillator is used in the slow conditions and a slower 4-stage oscillator is used when in the fast condition [Figure 2-28]. The division is made by measuring the tranconductance of the MOS transistors with the help of an off-chip resistor. This oscillator is designed to operate in PLL application where the stable bandwidth is more important than power consumption and the silicon area occupied by the transistors.

Figure 2-28 Parallel oscillator topology

In [58], a calibrated bias voltage is obtained by interpolating between two stable voltage reference points and the resulting voltage is applied to tune the bias current of the differential delay cell [Figure 2-29]. A bandgap reference circuit is used to generate two I-V target points, (I_1 , V_1) and (I_2 , V_2). As shown in Figure 2-29, the V_n is generated by interpolation between two bias voltages, $V_n(L)$ and $V_n(H)$.

transistors is adjusted and become less PVT dependent as it is always defined and calibrated by (I1, V1) and (I2, V2).. Applying the calibrated transistors as critical transistors (those affecting K_{VCO} and charge-pump currents) in a PLL makes the PLL PVT-insensitive.

In [59], one VCO (in a PLL) tracks the temperature and process variation and feed back a control voltage to control the second VCO to achieve lesser variation [Figure 2-32]. The temperature and process compensation circuit is indeed a PLL locked to a stable reference frequency, 100MHz in this design. As the reference frequency is temperature and process independent, the control voltage in the PLL will track the temperature and process variations. This control voltage is fed back to VCO2. In the design, VCO2 is used to generate a nominal frequency of 2GHz. V_{x2} serves as the control voltage to VCO2, and a very small gain is achieved that can be used for low jitter application.

Figure 2-31 Temperature and process compensated VCO

2.5 Comment on the PVT variation of PLL

The PLL loop functions are affected by the variability of individual building blocks. In an analog or hybrid PLL, where passive resistor and capacitors are used in the loop filter, they are subjected to process variations. Also, MOS capacitor leakage in deep-submicron process mandates the use of metal capacitors which increases the filter area [21, 60]. The current mismatch in charge pump causes undesired deterministic jitter [21]. As described in Chapter 1, the VCO gain (K_{VCO}), could vary by more than 60% for the same targeted VCO frequency. The PLL bandwidth could thus vary by more than 60% while the damping factor could vary by 30%.

ADPLL has tolerance to PVT variations in its digital circuits, however its stability (determined by loop transfer function) is still sensitive to PVT variations across a wide frequency range because the designs are not entirely digital [10, 21, 61-62]. As a result, issues associated with analog circuit design with advanced technologies inevitably remain. For example, DCO gain (K_{DCO}) and TDC gain (K_{TDC}) still suffer from PVT variation, which leads to change of loop bandwidth and damping factor from its optimum value, resulting in sub-optimal jitter performance [62]. Over PVT variation, TDC could have >4x delay variation and DCO >3x frequency variation [10]. The digital loop filter (DLF) eliminates jitter caused by capacitor leakage and charge pump current mismatch. The DLF coefficients can easily be programmed and are immune to PVT variations [21]. Innovative techniques are still required to make the loop characteristics tolerant to PVT variations. Some examples are start-up calibration [10], background K_{DCO} compensation technique [62], bandwidth tracking techniques without calibration [61].

Chapter 3

Methodology for PVT invariant VCO design

As introduced in the first chapter, typical VCO frequencies could vary by a factor of 2~3 between its slowest and fastest conditions due the variations in process, voltage, and temperature. With this variation, the upper bound of the frequency range is normally restricted to the slowest running condition for the highest V_{CTRL} while the lower bound of the frequency range is normally set by the fastest running condition at the lowest V_{CTRL} . For the same control voltage, the fastest running VCO frequency could vary by more than 30% when comparing to the slowest one across different PVT combination. The VCO gain (K_{VCO}), could vary by more than 60% for the same target VCO frequency. As the loop bandwidth needs to be at least 1/10 of the reference frequency so the bandwidth selected must satisfy the highest K_{VCO} (FF corner) for a targeted frequency. Also, damping factor (ζ) could vary by 30% for the same target VCO frequency such that the design has to cater for the lowest K_{VCO} (SS corner) to maintain the stability requirement. For a given charge pump current and divider ratio, the resistor and the capacitor values have to be selected based on the lowest K_{VCO} . This gives a size constraint to the selection of component sizes. There is an optimum loop bandwidth trading off between the output phase noise contributed by the VCO and reference input as high bandwidth filters VCO phase noise and not the reference noise. With all these design constraints and the variation in various design parameters, the optimum operating point selected based on the typical case (TT corner) would shift to a less optimum point at other process corners. To ensure PLL functionality and stability for all possible PVT variation, a designer is

left with some choices of design margins with more conservative design parameters but at sub-optimal performance.

There is a class of complicated adaptive bandwidth PLL design [1, 34, 44, 58] targeting PVT tolerance on loop bandwidth and damping factors by means of balancing the ratio among design parameters, instead of direct calibration/adjustment of the K_{VCO} . Nevertheless, a VCO with less variation in K_{VCO} is still beneficial as it helps to design PLL with a narrower range of loop bandwidths as well as the damping factors, apart from the wider tuning range. Several attempts had been taken to reduce the variation in VCO frequency and VCO gain [56-59, 63]. Relatively few papers focus solely on achieving PVT tolerant VCO for PLL. [63] adjusts the V_{CTRL} accordingly by detecting the process corner with a threshold voltage sensing circuit plus a proportional variation with temperature shift. Its VCO is powered by a regulated voltage supply at 1.2V. However, it focuses on achieving a PVT tolerant VCO with only a single frequency at 7MHz so it is not suitable for multiple frequencies suitable for PLL application.

The working principle of the proposed compensation techniques is reviewed in Section 3.1. This is followed by the the circuitry design in Section 3.2. VCO biasing circuitry and stability is examined in Section 3.3. In Section 3.4, the different VCO dummy configurations are studied for their impact on the output clock jitter performance. The differential-to-single converter is presented in Section 3.5. The simulation results of the compensated VCO are presented and reviewed in Section 3.6. The results are compared with prior VCO arts in Section 3.7. In Section 3.8, the possibility of using the compensation scheme to design “coarse and fine tuning” VCO is briefly explained. A more extensive compensation possibility is remarked in Section 3.9

3.1 Working principles of the VCO compensation scheme

Figure 3-1 Conventional VCO design

Figure 3.1 shows a conventional differential ring oscillator with a four-stage VCO. The popular Maneatis delay cell [34, 37] is employed for the VCO designed. A voltage-to-current (V2I) converter converts the V_{CTRL} into I_{CTRL} which is mirrored onto the bias circuitry to generate bias voltage for the delay cell. A differential to single converter converts the differential signal into single-ended signal. Without going into the operation details of the circuitry in this section, the concept of the VCO compensation technique is described in this chapter.

Figure 3.2 shows the conversion current of the V2I converter with respect to control voltage, for the control resistor (R_{CTR}) values of 4k Ω , 7k Ω and 10k Ω across the FF, TT and SS process corners. As required, the V2I converter converts the control voltage (V_{CTRL}) to control current (I_{CTRL}) linearly and independent of the process corners.

Figure 3-2 Current conversion of V2I converter at different control resistor value and process corners

The control currents overlap each other for the same R_{CTR} across the V_{CTRL} range of 0.1V to 1.5V. This ensures that the variation of frequencies across process corners is due to the subsequent stages of circuitry and not due to the V2I converter. Figure 3.3 shows the VCO frequency response with respect to control currents at FF, TT and SS process corners. A long-dashed line at 2.75GHz and a short-dashed line 1.25GHz (both selected arbitrary) are inserted to help visualize the control currents required to achieve these frequencies. It is clear from the graph that higher current is required at SS corner, lower current is required at FF corner and an in-between value is required for the TT corner in order to reach the same frequency. This characteristic gives rise to a possibility of frequency tuning by addition/subtraction of currents at different process corners, i.e. $I_{CTRL}=I$ at TT corner, $I+\Delta I_{SS}$ at SS corner and $I-\Delta I_{FF}$ at FF corner where ΔI_{SS} and ΔI_{SS} are not necessarily the same.

Figure 3-3 Variation of VCO frequency with respect to control currents

Figure 3-4 Variation of VCO frequency versus control resistance

At a targeted VCO frequency, the purpose of the compensation scheme is to achieve minimum frequency variation across the process corners. At SS corner, ΔI_{SS} is added to the nominal current and we can call this as positive current compensation. At FF corner, ΔI_{FF} is subtracted from the nominal current and is called as negative current compensation. The positive current compensation can be achieved by increasing the V_{CTRL} or by reducing the R_{CTR} while the negative current compensation can be

achieved by decreasing the V_{CTRL} or by increasing the R_{CTR} . In this work, the current compensation is achieved by adjusting the R_{CTR} . To better visualize this, Figure 3.4 shows how the VCO frequency varies with the R_{CTR} for V_{CTRL} at 0.4V, 0.95V and 1.4V at FF, SS and TT corners, respectively.

As an example, consider the VCO with a R_{CTR} of 6k Ω at the TT corner, the VCO frequencies are 2.861GHz, 2.057GHz and 1.132GHz at V_{CTRL} of 1.5V, 0.95V and 0.4V respectively. As shown in Figure 3.5, the required R_{CTR} is determined to be roughly 4.8k Ω and 7.6k Ω for frequency compensation at the SS and FF corners, respectively. This corresponds to a positive and negative compensation current that restore the frequency to align to the TT corner. Table 3-1 summarises the VCO frequencies, V_{CTRL} , R_{CTR} , I_{CTRL} , ΔI_{SS} and ΔI_{FF} .

Figure 3-5 Determine the compensating resistance and current required

Table 3-1 An example for compensated control resistor and compensation currents

V_{CTRL} (V)	0.4			0.95			1.50		
Targeted f_{VCO}	1.132GHz			2.057GHz			2.861GHz		
Process corners	SS	TT	FF	SS	TT	FF	SS	TT	FF
R_{CTR} (k Ω) without compensation	6	6	6	6	6	6	6	6	6
I_{CTRL} (μ A)	67	67	67	158	158	158	250	250	250
$\sim R_{CTR}$ (k Ω) with compensation	4.8	6	7.6	4.8	6	7.6	4.8	6	7.6
I_{CTRL} (μ A) with compensation	83	67	53	198	158	125	313	250	197
ΔI_{SS} (μ A)	16	N/A	N/A	40	N/A	N/A	63	N/A	N/A
ΔI_{FF} (μ A)	N/A	N/A	14	N/A	N/A	33	N/A	N/A	53

3.2 Proposed compensated VCO design

Figure 3.6 shows the block diagram of the VCO designed. Functionally, the design requires a voltage regulator, a compensation detection block, a voltage-to-current converter, a replica bias generator, four-stage differential VCO and a differential to

Figure 3-6 The VCO design

single converter. The popularly used Manetis delay cell is employed in this design. A voltage regulator is used to step down the power supply of 1.8V to the 1.2V power required by the VCO. A bandgap voltage reference has been designed to provide this 1.2V reference voltage [Chapter5]. A voltage-to-current converter is used to convert the V_{CTRL} to I_{CTRL} . A proportional replica of the I_{CTRL} is mirrored onto the replica bias generator to generate the required bias voltages for the VCO. The compensation detection block consists of a transistor threshold detection circuitry plus a comparison circuitry block. Digital control pins are generated from the compensation detection block to adjust the total resistance value of the resistor switch matrix.

The V_{CTRL} is converted into a control current (I_{CTRL}) by the voltage-to-current converter. A mirrored copy of the I_{CTRL} is used by the biasing circuitry to set V_{bp} and V_{bn} . The control current is given by

$$I_{CTRL} = V_{CTRL} / R_m \quad (3.1)$$

where R_m is the resistance at the switchable resistor matrix. The delay time at each state is roughly given by

$$t_d = C_L(V_{DD} - V_{bp}) / I_{bn} \quad (3.2)$$

where I_{bn} is the bias current at the tail of the delay stage and is proportional to I_{CTRL} .

The VCO oscillation frequency is given by

$$f_{VCO} = (1/2Nt_d) \quad (3.3)$$

where $N=4$ is the number of delay stages and t_d the delay time of each stage. As mentioned in Chapter 2, this equation is only suffice for a quick estimation as it does not take into account the effect of varying parasitic and the effect of gate resistance at high frequency [38-39]. A faster and better way is still to use a simulation tool like

Hspice to crunch out the required frequency once a rough calculation is done. By changing the V_{CTRL} or the R_m , the I_{CTRL} is changed and hence the delay time of each stage and the resulting frequency is changed. The load of the delay cell is composed of a diode-connected PMOS biased in saturation state and the other equally sized PMOS biased in the triode region. Dummy transistors are also connected to the first three delay cells to emulate the loading effect of the differential to single converter at the final stage. The dummy stages are indeed critical for the jitter performance of the PLL (discussed in detail at Section 3.4). For the VCO oscillation, the upper swing of the output is bounded by the V_{DD} and the lower swing is bounded by the V_{bp} . Section 3.2.1 describes in detail the operation of the compensation detection circuitry.

3.2.1 Compensation detection circuitry and resistor switch matrix

The comparator used in the compensation detection circuitry is as shown in Figure 3.7. The comparator consists of three stages: an input preamplifier (M1-M6), a decision circuitry (M7-M10) and a differential amplifier (M11-M18) acting as an output buffer. The differential amplifier converts the input voltage difference and outputs differential currents to the decision stage through M5 and M6. The decision circuit is able to discriminate mV level signals and having hysteresis characteristics that can reject noise [64-65].

Figure 3-7 Comparator design

The cross coupled gate connection of M8 and M9 provides a positive feedback and increases the gain of the decision stage. The output buffer is a self-biasing differential amplifier [68]; an inverter is added on to provide additional gain stage and to isolate load capacitance from the self-biasing differential amplifier [64]. A pair of differential output signals are drawn from each comparator to drive a level shifter to a logic level of 1.8V that control the resistor switch matrix.

Figure 3-8 Block diagram of the compensation detection circuitry

Table 3-2 Resistor value

$R_{00}=700\Omega$	$R_{01}=5400\Omega$	$R1=700\Omega$	$R2=800\Omega$	$R3=1000\Omega$	$R3=1000\Omega$
$R4=1150\Omega$	$R5=18835\Omega$	$R6=500\Omega$	$R7=833\Omega$	$R8=500\Omega$	$R9=19333\Omega$

Figure 3.8 shows the block diagram of the compensation detection circuitry and the resistor switch matrix used to set the total control resistor value. Four comparators are employed to generate a four-bit digital control word that switches the resistor switch matrix to an appropriate value. The total control resistor value is given by

$$R_{CTR} = b_4R_4 + b_3R_3 + b_2R_2 + b_1R_1 + R_{SS} \quad (3.4)$$

where b_4 , b_3 , b_2 and b_1 are the selection logic at “0” or “1” and $R_{SS}=R_{00}+R_{01}$ represents the minimum switchable matrix value. $bsel4$, $bsel3$, $bsel2$ and $bsel1$ are the inversion of b_4 , b_3 , b_2 , b_1 . R_{SS} is indeed the minimum resistance value required to provide the largest positive compensation current to the VCO at the SS corner. The last stage of a process corner detection circuitry is shown in Figure 3.9(a) while the reference voltage generator will be described in Chapter4 so it is omitted here. The V_{ref} is a stable power level at 1.2V, generated by the bandgap voltage generator. The detected voltage is about 645mV at the SS corner, 605mV at the TT corner and 567mV at the FF corner, with some variation across temperature. The resistor value selected is about 8.87k Ω and the W/L ratio of M0 is 1/0.24 after numerous simulation attempts and optimised for minimum variation. To have a more comprehensive detection scheme, a temperature detection circuitry could be combined with the existing detection circuit, at an expense of layout area and power.

Figure 3-9 (a) Process corner detection circuit (b) Detected voltage across temperature range of -40°C to 125°C

Figure 3-10 Response of compensation detection circuitry with respect to detected voltage

Figure 3.10 shows the response of the compensation detection circuit by displaying the state changes of $b_{sel}[1:4]$ with respect to the process corner voltage detected. Note that the values detected are not the actual threshold voltage of the devices but are relative values to distinguish different process corners. As the detected voltage increases (from the direction of FF towards SS), the control bits b_4 , b_3 , b_2 and b_1 are changed from 0000, 0001, 0011, 0111 and finally 1111. As the detection could be done within a very short time (less than tens of ns) at the background and normally at the start of power on, no extra calibration circuitry is required to set aside some micro seconds for the VCO calibration cycle [56, 67]. As an example, Figure 3.11

shows the response curve of the V2I converter at FF, TT and SS corners for a total control resistor value of 9.75k Ω , 7.6k Ω and 6.1k Ω , respectively.

Figure 3-11 Response of V2I converter at FF, TT and SS corners

3.3 VCO biasing circuitry

Figure 3-12 (a) VCO biasing circuitry (b) VCO delay cell with parasitic added

Figure 3-13 Voltage-to-current (V2I) converter

Figure 3.12 (a) depicts the biasing circuitry of the VCO. The control current (I_{CTRL}) is generated by the V2I converter [Figure 3.13] and mirrored onto the VCO biasing circuitry. The V2I operation has been explained in Section 3.1. Figure 3.12(b) depicts the VCO delay cell. Some fempto Farads are added to the delay cell in simulation so as to emulate the parasitic capacitances. This helps to reduce the discrepancy between the pre-layout and post-layout simulation results. There are two key design requirements for the biasing networks: linear response with respect to the control currents and the stability of the biasing voltages V_{bp} and V_{bn} . The stability of the control current also determines the stability of the V_{bp} and V_{bn} and how stable the VCO could oscillate. Figure 3.14 shows the frequency versus time response of three PLLs designed, with difference in phase margins for the V2I at 66.54° , 56.65° and 48.06° respectively. It is clear from the graph that the PLL response time with larger phase margin for the V2I is the fastest. Figure 3.15 shows the fluctuation of the V_{bn} but there is no clear difference for one from the other. As such, the phase margin of the V2I is not very critical for the stability of the V_{bn} biasing, the VCO stability and hence the PLL jitter performance. It is concluded here that the stability of the V2I converter affects the settling time of the bias voltage (and the lock time) but does not have much impact on the jitter performance.

Figure 3-14 Frequency response of the PLL with different V2I

Figure 3-15 V_{bn} of the VCO for V2I with different stability

As such, the V2I converter does not need to be overdesigned for stability but a moderate phase margin would be sufficient, as far as the response time is not of too much concern. Phase margin could be adjusted by increasing the value of $C1$ at an expense of layout size. Identifying and analyzing this requirement is important as it would help to minimise the layout size required for the design.

3.4 VCO dummies

It is found from simulation that different dummy strategies used for the VCO have an effect on the PLL clock output. Their impact on the jitter performance is discussed in this section. Figure 3.16 indicates a VCO with a complete set of full differential dummies. Each dummy consists of a differential-to-single (D2S) converter.

Figure 3-16 VCO with full differential dummies

Figure 3-17 (a) Simple dummy, (b) single stage differential dummy, (c) double stage differential dummy

All the other three VCO stages are also connected to the same D2S converters. Figure 3.17(a) is a simple dummy designed by transistors M3 and M4 that resembles the W/L ratio of the input transistors (also M3, M4) used in the D2S converter. Figure 3.17 (b) shows a dummy stage that consists of the first differential stage of the D2S converter. Figure 3.17(c) shows a dummy stage consists of the double stages of the D2S converter.

Figure 3-18 Open loop VCO biasing voltages with simple dummies and full dummies

Figure 3.18 shows the biasing voltages V_{bp} and V_{bn} for a “simple dummy” and “complete dummy”. The simulation is performed with a forced $V_{CTRL}=1V$ employing the PLL system circuitry with the charge pump disabled. It can be calculated from the values obtained from the figure that the peak-to-peak variation of V_{bn} for the “simple dummy” is 2.67 times that of the “complete differential dummy”. For the V_{bp} , the ratio is about 1.25. Figure 3.19 shows the V_{bp} and V_{bn} fluctuation during the close loop PLL operation, for VCO with simple dummy and full dummy. There is

only ~2% difference between the V_{bp} . However, the V_{bn} is differed by a factor of 2.24. The fluctuation causes noise in the VCO and should be suppressed.

Figure 3-19 Closed loop VCO biasing voltages with simple dummies and full dummies

To check the impacts of the different dummy implementation, five experimental PLL is simulated with difference only in the dummy stages: (i) no dummy, (ii) simple dummy, (iii) single stage differential dummy, (iv) double stage differential dummy and (v) full differential dummy using the D2S converters. The simulation result is tabulated in Table 3-2, listing the rms and peak-to-peak periodic jitter of the PLL.

Table 3-3 The effects of dummy on the PLL output clock jitter (10k cycles)

	Periodic jitter rms	Periodic jitter P2P	Current consumption	V_{CTRL}
No dummy	1.30ps	7.60ps	8.75mA	0.923V
Simple	1.14ps	7.14ps	10.36mA	1.164V
One stage	1.08ps	6.32ps	15.48mA	1.147V

Double stage	0.91ps	5.69ps	15.74mA	1.394V
Full	0.80ps	4.66ps	17.99mA	1.360V

To trade off between simulation time, disk storage and accuracy, each jitter calculation is performed with 10,000 cycles of samples. The JEDEC standard 65B specifies that period jitter should be taken over 10k cycles [68]. Unless specified, each jitter in this work would be computed with 10kcycles. The simulation is performed with a reference clock speed of 90MHz for an output clock of 2.88GHz. The detailed design parameters are provided in Chapter 5. Interestingly, the results show that the more symmetrical the dummy stages are, the better the jitter performance is, somehow as expected. The best performance is given by the full symmetrical dummy stages where all the dummies used are the D2S converters themselves, at an expense of current consumption and size. The worst performance is obtained from the case where no dummy stages are used at all. The simple dummy and one stage dummy locked at about the same control voltage, indicating that the K_{VCO} at which they lock should not be differ by much. A separate check on VCO frequency versus V_{CTRL} for them indicates further that the improvement in jitter should not be due to the loop characteristics change but rather attributed to the symmetry of the dummy stages. The similar arguments could be made for the PLL performance with double stage and full stage dummies. In fact, simulation indicates that the K_{VCO} for both are about 1.5GHz/V at which they got locked. The advantages of providing uniform loading with dummy stages could improve the symmetry, common mode noise rejection and phase alignment. This is reflected in the jitter performance of the PLL output clock.

3.5 VCO differential-to-single converter

Figure 3-20 Circuit diagram of the differential-to-single converter

Figure 3.20 shows the circuitry of the differential-to-single converter (D2S). The architecture is similar to the one employed in [37]. The D2S is required to convert the $(V_{DD}-V_{bp})$ bounded differential signal to the rail-to-rail signals bounded by the $V_{DD}-V_{SS}$. First, the D2S is able to generate a ~50% duty cycle clock output from the differential clock outputs. This avoids the need in some practice whereby the differential signals are divided down by half to obtain a ~50% duty cycle clock output. The size of the transistors M3, M4, 8, M9 are identical to M12, M13 [Figure 3.12] of the VCO delay cell. The same bias voltages V_{bn} provides the same current source bias for the two differential amplifier stages formed by M1-M5 and M6-M10. This kind of configuration ensures that the common-mode input voltages are received by the input stage. One disadvantage of such circuit is the significant bias current it draws.

3.6 Simulation Results

Figure 3-21 (a) Variation of VCO frequency without compensation (b) Variation of VCO frequency with compensation

Figure 3.21(a) shows the variation of the VCO frequency without the compensation design. Figure 3.21(b) shows the variation of the VCO frequency with the compensation design. The plots are derived from the compensated VCO simulated at FF, TT and SS corners for a total control resistor value of 9.75k Ω , 7.6k Ω and 6.1k Ω , respectively. It can be seen that the compensated VCO frequency at the extreme operating conditions is shifted closer to the typical case at 25°C. At the assumed maximum tuning voltage range of the VCO (1.5V), the worst case frequency occurs at the slowest running condition, i.e. SS corner at 125°C. This is the highest frequency in which the VCO would always work across all the possible process corners and temperature. At the lower tuning voltage of 0.4V, the worst case

frequency occurs at the FF corner at 25°C (in this case). The upper and lower usable frequencies of the VCO are thus restricted and reduced due to the process and temperature variation. With the compensated VCO design, the upper usable frequency range has been extended from around 2.114GHz to 2.410GHz. The lower frequency range is further lowered from around 1.140GHz to 0.999GHz. Overall, the usable frequency range has been extended by a factor of 1.45, an impressive percentage improvement that is close to 50%. This is a figure of merit as a wide frequency tuning range is a desired VCO feature. To achieve the same frequency range, a conventional VCO may need larger delay cell size, larger current consumption which is not the favoured features of a VCO design.

Figure 3-22 (a) Variation of VCO gain without compensation (b) Variation of VCO gain with compensation

Figure 3.22(b) shows the K_{VCO} of a VCO with the proposed compensation scheme. The plots are derived from the same set of data employed for those in Figure 3.21(a), (b). Both the uncompensated and compensated K_{VCO} show two common trends: (i) they gradually decrease with the increasing frequency, (ii) there seems to be a relatively flat K_{VCO} region near to the higher frequency end. The flat K_{VCO} region suggests a possibly local optima point for PLL operation as the bandwidth within this range would not change abruptly. It is clear from Figure 3.22(a) that the K_{VCO} is the highest at the FF corner and lowest at the SS corner, for the same VCO frequency. This means that a designer has to ensure the minimum bandwidth to reference frequency ratio at the FF corner before consider any other process corners. Overall, the K_{VCO} variation is larger than 60% and making the system design more complicated.

For the compensated VCO, the variation of K_{VCO} has been greatly reduced. For the same targeted frequency, the variation of compensated K_{VCO} is just about 10% at most and resulting in about 5% variation in bandwidth by proportion. This reduced variation range would give a designer much relaxed design constraints and larger design margins to play with. The flat out region of K_{VCO} is brought to the proximity range of about 1.95GHz to 2.15GHz across all process corners. At 25°C, the K_{VCO} curves align well from process corner to corner. The K_{VCO} at the extreme SS corner at 125°C shows a more significant deviation from the rest, especially at higher frequency. This suggests that although the basic compensation itself is good in reducing the VCO frequency variation for practical use, more complex compensation algorithm is required to tackle the extreme operating condition for more stringent requirement. For the frequency range of 1GHz to 2GHz, the compensated K_{VCO} changes gradually from about 1.68GHz/V to 1.2GHz/V. This close consistency gives

rise to the possibility of adjusting the charge pump current or even the loop filter in this operating region to achieve a relatively optimum bandwidth, i.e. to minimise the jitter in the PLL output employing such a VCO.

To better visualize the bandwidth variation of a PLL, the normalized bandwidth of a VCO can be derived by taking the ratio with respect to a reference K_{VCO} value, i.e. the lowest K_{VCO} value. In this way, we can compare without the detailed values of other parameters like charge pump current, loop filter and etc. Figure 3.23(a) and (b) depicts the normalized bandwidth of a charge pump PLL with and without the compensation. Similar normalization is performed on the damping factor of a PLL as shown in Figure 3.24 (a) and (b).

Figure 3-23 (a) Normalised bandwidth with respect to VCO frequency without compensation (b)normalised bandwidth with respect to VCO frequency with compensation

Figure 3-24 (a) Normalised damping factor with respect to VCO frequency without compensation (b) normalised damping factor with respect to VCO frequency with compensation

Figure 3.24(a) shows that the bandwidth variation across the whole frequency tuning range and process corners is more than a factor of 2.2. Figure 3.24(b) shows that the bandwidth variation is reduced to a factor of 1.7 for a PLL with compensated VCO. For the same target frequency, this variation has been reduced from a factor of 1.6 to about 1.1. The variation of the damping factor has been reduced from a factor of 1.5 to a factor of 1.32, across the whole frequency tuning range and process corners. However, for the same target frequency, the maximum variation in damping factor has been reduced from about 1.3 to slightly over 1.05, as estimated from Figure 3.24(b).

3.7 Comparison to Previously Published Works

From the simulation results, the variation of frequency at 25°C is within $\pm 0.6\%$ for the tuning voltage range from 0.4V to 1.5V comparing the fastest to slowest conditions. The variation of frequency at each control voltage point is within $\pm 3.9\%$ across a temperature range of -40°C to 125°C.

Table 3-2 summaries the comparison of the proposed compensated VCO with prior arts [56-59, 63]. [59] demonstrated that small frequency variation could only be reached within a narrow band of 2GHz. In [56-57, 59, 63], the circuits implemented incur the silicon area as they all require two VCOs. In [58], fewer components are used at the expense of performance, i.e. the variation in frequency is slightly higher. This work shows an overall smaller frequency variation across the control voltage range from 0.5V to 1.4V. The highest variation is at the lower V_{CTRL} of 0.5V.

Table 3-4 Comparison of different VCOs

Specification		[56]	[57]	[58]	[59]	This work
Supply voltage (V)		1.8	3.3	1.8	N/A	1.8
Temperature range (°C)		-25~125	0~100	0~100	0~100	-25~125
Technology (μm)		0.18	0.5	0.18	N/A	0.18
$V_{CTRL}=0.50V$	Slowest(MHz)	N/A	N/A	1924	40	1092
	Fastest(MHz)			1979	80	1177
	variation			2.9%	100.0%	7.8%
	variation/°C			0.029%	1%	0.052%
$V_{CTRL}=0.80V$	Slowest(MHz)	84	N/A	N/A	195	1534
	Fastest(MHz)	89			205	1606
	variation	6.0%			5.1%	4.7%
	variation/°C	0.04%			0.051%	0.031%
$V_{CTRL}=1.00V$	Slowest(MHz)	N/A	140	1998	N/A	1802
	Fastest(MHz)		180	2006		1857
	variation		28.6%	0.4%		3.1%
	variation/°C		0.286%	0.004%		0.021%
$V_{CTRL}=1.25V$	Slowest(MHz)	N/A	N/A	2031	N/A	2096
	Fastest(MHz)			2101		2156
	variation			3.4%		2.9%
	variation/°C			0.034%		0.019%
$V_{CTRL}=1.40V$	Slowest(MHz)	510	275	N/A	575	2264
	Fastest(MHz)	526	360		675	2332
	variation	3.1%	30.9%		17.4%	3.0%
	variation/°C	0.021%	0.309%		1.74%	0.02%

3.8 Coarse tuning and fine tuning VCO

Figure 3.25 shows the VCO frequency with respect to control voltage range of 0.4V ~1.4V, for the control resistor varying from 1k Ω to 10k Ω . Though a bit saturated at the largest current for a control resistor value of 1k Ω , this behavior gives rise to the possibility of using the VCO for an extra extended frequency range of 1GHz to 6GHz, if required. The coarse tuning range is defined by the resistor while the fine tuning range is provided by the control voltage. The feasibility of incorporating the VCO into a coarse/fine tuning PLL could be explored. The coarse tuning part could be done digitally by adjusting the bulk current to the VCO through resistor matrix switching (rather than using a voltage) while the fine tuning could be kept in the similar way by voltage-control.

Figure 3-25 Coarse tuning and fine tuning VCO

3.9 Complex compensation

Figure 3-26 Complex compensation

Figure 3.23 (b) shows that the variation for K_{VCO} greatly reduced. For the same frequency, the compensated K_{VCO} is about 10% at most and resulting in about 5% variation in bandwidth by proportion. In contrast, the uncompensated K_{VCO} show variation of as high as 50%. At 25°C, the K_{VCO} curves align well from process corner to corner. Though the basic compensation itself is good in reducing the VCO frequency variation for practical use, more complex compensation algorithm is required for higher requirement. In Figure 3-24, for lower R_m , i.e. at higher frequency range and K_{VCO} at the extreme SS corner 125°C show deviation from the rest, especially at higher frequency. As shown in Figure 3-26, the temperature and/or the V_{CTRL} can be combined to provide a more robust compensation. The VCO demonstrates different sensitivity to high and low temperature as well as high V_{CTRL} .

Chapter 4

Design of the PLL System

4.1 Overview

Figure 4-1 Block diagram of the PLL

The block diagram of the PLL implemented with the compensated VCO is shown in Figure 4.1. The design is implemented in the IBM 0.13 μ m CMOS 8RF technology. The reference frequency is injected from an external source. The operation of the VCO has been explained in Chapter 3. All circuitry is powered by a single 1.8V

power supply. A bandgap reference voltage is designed to provide a voltage (V_{ref}) of 1.2V. V_{ref} is used as the voltage reference for the compensation circuitry, the reference current generation and the voltage regulator to generate the 1.2V power supply. The regulator provides power supply that is used for the phase-frequency detector (PFD), VCO, differential to single converter (D2S), feedback divider and the bias circuitry for the VCO. The VCO design employs a 4-stage differential delay cells. The last stage of the VCO is driving a differential-to-single (D2S) converter, on top of driving the first delay cell. The VCO dummy stages are required to provide symmetry and uniform loading that could help in reducing the common mode noise rejection and phase alignment. The startup circuitry is required to prevent the occurring of the zero current state during initial power on. An initial reference current is first generated from the bandgap reference voltage block to kick start the voltage biasing circuitry for the Op amp used in the band-gap based reference currents generators. The currents generated from the band-gap based reference generators are used for subsequent generation of reference currents and then the biasing voltages through current mirroring.

The current from charge pump across all PVT corners has been made relatively constant by mirroring the current which is derived from the bandgap-based current reference generator. The charge pump current is designed to be adjustable from 20 μ A to 60 μ A, allowing for the adjustments of loop characteristics. The unity gain Op Amp is employed as a bootstrapping buffer to reduce the charge sharing effect for better performance.

The phase frequency detector (PFD) is implemented in dynamic logic scheme. By inserting delay circuit in the feedback signal path, the PFD generates short coincidental pulses of UP and DN, even when the PLL is in lock, so that the dead

zones are removed. The reset signal ensures a valid output logic state after power-on. The delay for reset signal is introduced by a properly sized chain of NAND gates and inverters.

A divide-by-32 D-latch-based feedback divider has been designed with five stages of half-dividers. The half-divider consists mainly of a negative edge latch and a positive edge latch working in pair to achieve a divide-by-2 function. The divider has been simulated over the PVT corners and can work up to 5GHz with a good output duty cycle of $51.5 \pm 0.5\%$. A single division ratio may not be competitive in a real commercial wide range PLL, but is suffice to make a good study for this work.

Section 4.2, 4.3, 4.4 presented the circuitry designed for PFD, charge pump and feedback divider. In Section 4.4, other building blocks, i.e. bandgap voltage reference, bandgap-based reference current generator and voltage regulators are described in brief. The model used to determine the phase margin, gain margin, and gain bandwidth is shown in Section 4.6. In Section 4.7, the transient simulation results for the PLL with/without compensation are presented for the SS and FF corner, with an example at 2.56GHz clock output. The simulated jitter performance and power consumption of the proposed PLL is compared to four published works. Lastly, the PLL is set to a higher bandwidth for the clock output at 2GHz, 2.56GHz and 2.88 GHz to check the ultimate jitter performance achievable.

4.2 Phase Frequency Detector Design

The design issues for PFD are reviewed in Chapter 2. The phase frequency detector (PFD) is implemented in dynamic logic scheme. The circuitry of the designed PFD is as shown in Figure 4.2. The reset signal ensures a valid output logic state after power-on.

Figure 4-2 Circuitry of the PFD design

Figure 4-3 (a) Level shifter design (b) Flip Flop schematics used in the PFD

There is a limit of pulse that the PFD can generate. Likewise, the charge pump could not be turned on and off in such narrow time frame. Dead zone occurs when the loop

does not respond to small phase errors at PFD inputs. This causes undesired jitter and phase noise. A delay reset is normally introduced to guarantee a minimum pulse width to remedy the dead-zone problem. The delay for reset signal is introduced by a chain of NAND gates and inverters. The reset path consists of two NAND gates and an inverter to provide an appropriate delay. An enable signal is included so that the PFD could be disabled when needed. By inserting delay circuit in the feedback signal path, the PFD generates short coincidental pulses of UP and DN, even when the PLL is in lock, so that the dead zones are removed. Widening the reset pulse increases the time where both UP and DN are high and the charge pump conducts simultaneously. This has undesired effect on the VCO control voltage and phase noise. If the DFFs are not properly matched and that one reset is faster than the other, the reset signal will be pulled to low and not able to reset the slower DFF. Operationally, The PFD is used to detect both the phase and frequency differences. The RefClk denotes the reference clock whereas FbClk denotes the feedback clock. Both UP and DN signals are initially low. A rising edge of FbRef input causes the UP signal to go high. This indicates that the FbClk, i.e. the VCO needs to run faster in order to match the input reference clock. When the FbClk leads the RefClk and goes high, the DN signals goes to high. This means that the FbClk needs to run slower. When both RefClk and FbClk goes high simultaneously, the NAND gate is set high and in turn resets the PFD to the zero state. In this way, the PFD behaves as a three-state device (Chapter 2).

Instead of using transmission gates to balance the extra delay in the UP/DN signals, properly sized inverters (faster edges than transmission gates) are used in the path of UP and DN signals to achieve the same purpose. A level shifter is needed to make the logic conversion from the 1.2V signal in the PFD to the 1.8V signals for charge

pump control. A cross-coupled (positive feedback) latch configuration [Figure 4-3(a)] is designed for this level shifting purpose. The cross-coupled level shifter is able to maintain fast edges and requires minimum power consumption. The D-flip-flops (DFF) are designed using conventional NAND-based latches as shown in Figure 4-3(b). Figure 4-4 and 4-5 show how the PFD response to the UP and DOWN signals.

Figure 4-4 Feedback Clock runs faster than reference clock. DN pulse indicates that the feedback clock needs to slow down

Figure 4-5 Feedback clock runs slower than reference clock. UP pulse indicates that the feedback clock needs to run faster.

4.3 Charge Pump Design

Charge pump design issues have been well described in [19]. Dead zone issue from the PFD, delay difference between the switches, drain currents mismatch, charge sharing. The charge sharing can be suppressed by a technique called bootstrapping as in [27-28]. These issues have been reviewed in Chapter 2.

The charge pump which is based on one described in [27] is shown in Figure 4.8. The UP and DOWN signals switch charge pump currents onto the loop filter, thus delivering a charge to move control voltage (V_{CTRL}) UP or DOWN. A unity gain OpAmp is employed as the bootstrapping buffer to reduce the charge sharing effect [19-20, 27-28]. In this way, the charge sharing between the loop filter and the parasitic capacitances is avoided. Figure 4.6 shows a simplified circuitry of the charge pump design. Single-ended charge pump architecture with the current steering is adapted in this work. This structure provides a high-speed switching of the charge pump current. The reference current which is derived from the bandgap-based current reference generator is mirrored onto the charge pump circuitry to provide the PVT invariant charge pump currents.

Figure 4-6 Simplified circuitry of the charge pump

These currents are indicated by I1, I2 and I3 as shown in Figure 4-6. This makes the charge pump currents relatively constant across all the possible operation corners. The current mirrors are cascoded to increase the output impedance such that it is less sensitive to the level of V_{out} . The transistor sizes of the M22, M23, M24 and M25 need to be optimized in order to minimize the timing mismatch. The charge pump current can be adjusted from $20\mu A$ to $60\mu A$ using a 3-bit digital control word to allow for adjustments of the loop characteristics. Similar techniques had been used by Boerstler in [69]. The control codes for selecting the charge pump currents are 000, 001, 010, 011 and 1XX respectively. A logic circuitry is used to process the 3-bit code and generate the select bits sel[3:0] and selb[3:0]. As discussed in Chapter 3, the K_{VCO} of the designed VCO decreases gradually with increasing frequency, i.e. increasing V_{CTRL} . The charge pump current can then be adjusted accordingly so that the loop bandwidth can be maintained to a certain level as there is always a relatively

optimum ratio of reference frequency to loop bandwidth. The current mismatch of the charge pump at 60 μ A is simulated and plotted in Figure 4-7 (a), (b) for 1.8V and 1.68V operations.

Figure 4-7 Current mismatch with I_{CP} at 60 μ A, (a) VDD=1.8V, (b) VDD=1.68V.

Table 4-1 Current mismatch window at I_{CP} of 60 μ A

	V_{CTRL} at the low end			V_{CTRL} at the high end		
Mismatch	3%	2%	1%	1%	2%	3%
VDD=1.80V	0.2916V	0.3138V	0.3500V	1.332V	1.375V	1.402V
VDD=1.68V	0.3033V	0.3218V	0.3570V	1.178V	1.228V	1.257V

The current mismatch window for the charge pump at 1.68V and 1.8V operation is as shown in Table 4-1. It is observed that the window for the 1.68V operation is narrower as the voltage headroom is reduced. Due to the larger current mismatch at the high end of the V_{CTRL}, operation of the PLL at 1.68V for the high end of the frequency range is less desirable.

4.4 Feedback divider

Figure 4-8 (a) A divide-by-32 feedback divider consists of five 1/2 divider (b) a 1/2 divider

A divide-by-32 Dlatch-based feedback divider has been designed with five stages of half-dividers. The half-divider consists mainly of a negative edge latch and a positive edge latch working in pair to achieve a divide-by-2. The divider has been simulated over the PVT corners and can work up to 5GHz with a good output duty cycle of $51.5 \pm 0.5\%$.

4.5 Other building blocks

Figure 4-9 shows the simplified circuitry of the bandgap reference voltage generator. The current mirrors M1-M3, M2-M4, M7-M8 keep the currents in D1, D2 and D3 identical. The expression of the bandgap voltage could be derived and shown to be $V_{bgr} = V_{D3} + (R2/R1)V_T \ln(n)$ where $V_T = kT/q$ and n is the ratio of the area of the D3 to D2. The bandgap voltage reference provides the reference level of 1.2V to the voltage regulator and a reference for comparison for the threshold detection circuitry.

Figure 4-9 Bandgap-reference voltage generator

Figure 4-10 Band-gap based accurate reference current generator

Figure 4-10 shows the circuitry of the bandgap-based reference current generator. With the bandgap voltage reference, the reference currents generated are adequately invariant and independent of process corner shift. Figure 4-11 shows the simplified circuitry of the voltage regulator that is used to provide the 1.2V voltage supply and current. With a well-designed bandgap voltage reference, the output of the voltage regulator always stays at ~1.2V. The constant voltage source is used to power up the VCO and other circuitry that requires 1.2V. For improved noise immunity, a separate voltage regulator may be dedicated to the VCO and the other “quiet” circuitry would share the second voltage regulator.

Figure 4-11 Voltage regulator

4.6 System modeling

A system model is used to determine the phase margin and bandwidth characteristics of the charge pump PLL structure with a second order loop filter. The simulation is run using HSPICE with the model in Figure 4-12. The phase margin, gain margin and the bandwidth can be visualised and obtained using the model. The damping factor, loop bandwidth are computed based on the approximate equations derived in Chapter 2, assuming that C_{RIPPLE} is negligible.

Figure 4-12 (a) System behaviour modelling (b) loop filter

Table 4-1 Parameters designed for the PLL for $K_{\text{VCO}} = 1.50\text{GHz/V}$

I_{CP}	ζ	Loop BW	C_{RIPPLE}	C_{MAIN}	R_{ZERO}
20 μA	1.01	1.29MHz	3pF	58.35pF	8.66k Ω
30 μA	1.24	1.94MHz			
40 μA	1.43	2.58MHz			
50 μA	1.63	3.23MHz			
60 μA	1.75	3.88MHz			

4.7 PLL simulation results with and without VCO compensation

The PLL system level simulation has been performed extensively with Hspice. In As an example, the PLL with full VCO dummies (explained in Chapter 4) is simulated with the charge pump current varying from $20\mu\text{A}$ to $60\mu\text{A}$ with a reference clock frequency of 80MHz . The output clock is thus 2.56GHz . The control codes for selecting the charge pump currents are 000, 001, 010, 011 and 111 respectively. The K_{VCO} at which the PLL locked is calculated (based on a narrower range of simulation results from V_{CTRL} of 1.1V to 1.2V) to be 1.533GHz/V at V_{CTRL} of 1.131V .

Figure 4-13 Transient plots of control voltage for varying charge pump currents

The loop bandwidth is varied from 1.35MHz , 2.02MHz , 2.69MHz , 3.36MHz and 4.04MHz . Figure 4.13 shows the transient plots of the V_{CTRL} , with the varying charge pump currents (or loop bandwidth). As expected, the response time of the PLL is

inversely proportional to the loop bandwidth, i.e. PLL higher bandwidth PLL responds faster than the one with lower bandwidth. Taking 10k cycles for each charge pump current, the rms jitter and period jitter of the PLL are computed with the data obtained from transient simulation for comparison. Since only the charge pump current is varied, the PLL always lock at the same control voltage and the K_{VCO} remains virtually the same. From Table 4-1, it is observed that the jitter performance improve gradually as the charge pump current is increased (bandwidth increased) and then start degrades again for further increase in the bandwidth. This indicates that there is an operating point for minimum jitter performance in between the lowest and highest bandwidth.

Table 4-2 The effects of varying charge pump current on the PLL output clock jitter at 2.56GHz (10k cycles)

Charge pump current, I_{CP}	Loop bandwidth, BW	F_{ref} / BW	Periodic jitter rms	Periodic jitter P2P
20 μ A	1.35MHz	59.26	0.92ps	5.34ps
30 μ A	2.20MHz	36.36	0.90ps	5.25ps
40 μ A	2.69MHz	29.74	0.91ps	5.17ps
50 μ A	3.36MHz	23.80	0.92ps	5.38ps
60 μ A	4.04MHz	19.80	0.99ps	6.68ps

This design has a relatively constant charge pump currents regardless of process corners, as the reference currents is generated by a bandgap-based V2I converter and mirrored onto the charge pump circuitry. As such, for the simulation results shown in Table 4-2, the PLL jitter in the SS and FF process corners should be mainly due to the less optimal operation point due to the shift in K_{VCO} , apart from the effects of inherent threshold shift for the other circuitry. The VCO with compensation at the FF and SS corners is able to provide the K_{VCO} closer to the TT optimal point than the

VCO without compensation. As a result, the compensated VCO is able to operate closer to the optimum point and gives an improved jitter performance.

Table 4-3 The PLL output clock jitter at 2.56GHz with and without compensated VCO (10k cycles)

Process corner	Charge pump current	Periodic jitter rms	Periodic jitter P2P
SS	40 μ A	1.03ps	6.97ps
FF	40 μ A	1.06ps	6.84ps
TT	40 μ A	0.91ps	5.17ps
SS ^a	40 μ A	1.01ps	6.63ps
FF ^a	40 μ A	1.07ps	6.69ps

^a with compensated VCO.

Figure 4-14 Transient plots of the control voltage for the PLL at 2.56GHz

Figure 4-14 shows the transient plots of the control voltage for the PLL simulation with and without the VCO compensation. It is observed that the control voltage of the PLL (with compensated VCO) at FF corner has been shifted from its

uncompensated position upwards to the proximity of that for the TT corner, by negative compensation. The one at the SS corner has been shifted from its uncompensated position downwards to the near proximity of that for the TT corner, by positive compensation. The compensation mechanism has been explained in Chapter 4.

It could be concluded that the PLL frequency range has been widened as the PLL at the SS corner is able to operate beyond what it could without the VCO compensation.

4.8 Comparison of PLL performance with prior arts

Table 4-4 Comparison of PLL Performance without normalization

	Freq.	Tech. node	Supply voltage/current consumption/power	RMS jitter	P2P jitter
[58] S-J Park	1.0GHz	0.18μm	1.8V/8mA/14.4mW	5.70ps	34.70ps
[47] Mansuri	1.0GHz	0.25μm	2.5V/4mA/10mW	3.28ps	28.89ps
[48] Ting Wu	1.4GHz	0.13μm	1.0V/9.6mA/9.6mW	3.90ps	N/A
[55] Minami	2.0GHz	0.10μm	1.2V/25mA/30mW	2.80ps	21.00ps
This work(¹ fd)	1.0GHz	0.13μm	1.68V/5.81mA/9.75mW	2.95ps	17.57ps
			1.8V/5.93mA/10.67mW	3.60ps	19.17ps
This work(² sd)	1.4GHz		1.68V/4.72mA/7.92mW	2.92ps	17.51ps
			1.80V/4.83mA/8.69mW	2.88ps	18.97ps
This work(fd)	1.4GHz		1.68V/7.90mA/13.28mW	2.00ps	13.51ps
			1.80V/8.05mA/14.50mW	2.06ps	13.20ps
This work(sd)	2.0GHz		1.68V/6.75mA/11.34mW	1.85ps	12.43ps
			1.80V/6.91mA/12.43mW	2.09ps	13.60ps
This work(fd))	2.0GHz		1.68V/11.51mA/19.34mW	1.36ps	10.73ps
			1.80V/11.69mA/21.04mW	1.41ps	10.39ps
This work(sd)	2.56GHz		1.68V/8.88mA/14.92mW	1.43ps	11.07ps
			1.80V/9.04mA/16.27mW	1.49ps	10.23ps
This work(fd)	2.56GHz		1.68V/15.37mA/25.83mW	1.21ps	9.25ps
			1.80V/15.57mA/28.02mW	1.05ps	7.18ps
This work(sd)	2.88GHz		1.68V/10.17mA/17.09mW	2.95ps	15.85ps
			1.80V/10.36mA/18.65mW	1.49ps	11.53ps
This work(fd)	2.88GHz		1.68V/17.78mA/29.87mW	1.46ps	10.281ps
			1.80V/17.96mA/32.33mW	1.43ps	9.66ps

Remark: ¹fd=full dummy, ²sd=simple dummy. Simulations performed with 50k cycles for comparison

The proposed PLL were simulated with full VCO dummies (where D2S converters are used) and simple VCO dummies (nmos transistor pairs) as described in Chapter 4.

The minimum charge pump current (20 μ A) have been used for all the simulations for consistency.

The targeted output clocks are 1GHz, 1.4GHz, 2GHz, 2.56GHz and 2.88GHz corresponding to reference clock frequency of 31.25MHz, 43.75MHz, 62.50MHz, 80MHz and 90MHz respectively. It is stated in the paper [47] that the jitter histogram is measured with >45k cycles. This information is not available for [48, 55]. In JESD65B, it is recommended that a minimum of 10,000 cycles be taken for period jitter measurement. In older work like [70] in the year of 2000, the measurement is made with ~10k cycles, perhaps limited to the memory depth of the test equipment. It is important to know how many cycles are used in the jitter measurement or simulation as it accumulates and increases with the number of samples. All the jitter simulation for performance comparison with prior arts is done by taking 50k cycles to ensure consistency and significance.

For the 2GHz, 2.56GHz and 2.88GHz clock outputs, the PLLs with full dummies give the best peak-to-peak jitter performance but consume more current. For the 1GHz operation, the PLL with simple dummy is not able to lock as the V_{CTRL} is out of the tunable voltage range. Indeed, the PLL with full dummy locks at $V_{CTRL}=0.27V$ for 1GHz.

From the Table 4-3, it can be seen that the designed PLL has achieved better jitter performance and lower power consumption for clock frequency of 1GHz, 1.4GHz and 2GHz, comparing to works [47-48,55]. The actual jitter performance requires real silicon validation to confirm, however the power consumption should not differ by much from the simulation as far as the fabrication process is consistent with the

spice models. The jitter measurement also depends on the quality of the test chip design, the test board quality and the measurement setup.

To explore further into the PLL jitter performance, the PLL is simulated with a higher loop bandwidth by setting the charge pump current to 40 μ A. It is noticed that the jitter performance could be further improved similarly to those described in Section 4-7. Table 4-4 tabulates the improvement in jitter for the output clock frequency at 2GHz, 2.56GHz and 2.88GHz. The performance for the 1GHz, 1.4GHz clock does not benefit from further increasing the loop bandwidth, probably due to the lower reference frequency to loop bandwidth ratio, i.e. F_{ref}/BW . For example, the ratio becomes 11.6 (approaching the limit of 10) if the loop bandwidth is further increased to 2.69MHz for the 1GHz clock with input reference of 31.25MHz. The close loop transient response of the PLLs at 2GHz, 2.56GHz and 2.88GHz are shown in Figure 4-14. The histograms of the long term period jitter calculated with 50k cycles are also included into the figure.

Table 4-5 The better jitter performance with higher bandwidth

Freq.	Loop BW	Supply voltage/current consumption/power	RMS jitter	P2P jitter	% P2P jitter of period
2.0GHz	1.35MHz	1.80V/11.69mA/21.04mW	1.41ps	10.39ps	2.08%
	2.69MHz	1.80V/11.71mA/21.07mW	1.29ps	6.07ps	1.21%
2.56GHz	1.35MHz	1.80V/15.57mA/28.02mW	1.05ps	7.18ps	1.84%
	2.69MHz	1.80V/15.59mA/28.05mW	1.02ps	6.67ps	1.71%
2.88GHz	1.35MHz	1.80V/17.96mA/32.33mW	1.43ps	9.66ps	2.78%
	2.69MHz	1.80V/17.98mA/32.36mW	0.95ps	6.57ps	1.89%

Figure 4-15 Long term period jitter with loop bandwidth of 2.69MHz for clock outputs at (a)2GHz, (b)2.56GHz, (c)2.88GHz

Table 4-6 Comparison of PLL Performance with normalization

	Freq.	Tech. node	Supply voltage/current consumption/power	RMS jitter	P2P jitter
[58] S-J Park	1.0GHz	0.18 μ m	1.8V/8mA/14.4mW	5.70ps	34.70ps
[47] Mansuri	1.0GHz	0.25 μ m	2.5V/4mA/10mW	3.28ps	28.89ps
[48] Ting Wu	1.4GHz	0.13 μ m	1.0V/9.6mA/9.6mW	3.90ps	N/A
[55] Minami	2.0GHz	0.10 μ m	1.2V/25mA/30mW	2.80ps	21.00ps
This work(sd), BW=1.35MHz	2.0GHz	0.13 μ m	1.80V/6.91mA/12.43mW	2.09ps	13.60ps
This work(fd), BW=1.35MHz	2.0GHz	0.13 μ m	1.80V/11.69mA/21.04mW	1.41ps	10.39ps
This work(fd), BW=2.69MHz	2.0GHz	0.13 μ m	1.80V/11.71mA/21.07mW	1.29ps	6.07ps
[58] S-J Park, normalized	2.0GHz	0.13μm	1.8V/11.56mA/20.86mW	2.85ps	17.35ps
[47] Mansuri, normalized	2.0GHz	0.13μm	1.8V/2.99mA/5.39mW	1.64ps	14.45ps
[48] Ting Wu, normalized	2.0GHz	0.13 μ m	1.8V/24.68mA/44.43mW	2.73ps	N/A
[55] Minami, normalized	2.0GHz	0.13μm	1.8V/48.75mA/87.75mW	2.80ps	21.00ps

Table 4-6 shows the comparison of PLL jitter and power consumption, normalised to the 0.13 μ m, 1.8V and 2GHz. The normalized power is given by $(\lambda_{\text{ref}}/\lambda) \cdot (V_{\text{ref}}/V)^2 \cdot (f_{\text{ref}}/f) \cdot P$. The normalized jitter is given by $(f/f_{\text{ref}}) \cdot \text{jitter}$. λ_{ref} , V_{ref} and f_{ref} refers to the lambda of the process, voltage and the clock frequency of the reference PLL to be normalized to. $f_{\text{ref}}=2\text{GHz}$ is chosen as this is the center output clock frequency of the PLL designed. With this normalization, [47] seems to provide the best figure of merit while this work is the second, by looking at minimum jitter with minimum power spent. This normalization approach has been used in [71] for comparison of PLL performance.

Chapter 5

Conclusion and Recommendations

5.1 Conclusion

A differential VCO made with improved PVT tolerance by means of digitally assisted compensation has been described. Its implementation in a charge pump PLL and benefits are presented. It has been demonstrated that with the VCO compensation techniques, the gain and frequency variation of a VCO could be greatly reduced thereby relaxing the design constraints. This will also reduce the variation in PLL bandwidth and damping factor which is desired for design. The VCO and hence the PLL usable output frequency range would be widened by the VCO compensation. Simulation has been performed with five different VCO dummy schemes to determine the jitter performance with different dummy strategies. With the loop bandwidth so adjusted by varying the charge pump current, the PLL operation could be tuned slightly to an optimum (relatively) point. As such, the VCO compensation would help to improve the jitter performance as it would reduce the shift from the optimum operating point by bringing the process varied VCO back to the proximity of this point.

A detailed summary of the achievement is as followed:

(1) With an example, the usable frequency range is shown to be possibly extended by a factor of 1.45, an impressive percentage improvement close to 50%. To achieve the same frequency range without compensation, the conventional VCO design may need a larger delay cell and high current consumption. For the same targeted frequency, the variation of compensated K_{VCO} is slightly above 10% at most, reduced

from a high value of 60% without compensation. The similar trend of the compensated K_{VCO} changes with respect to frequency allows the adjustment of design parameters like charge pump current, loop filter so that an optimum bandwidth could be achieved for minimum PLL jitter performance.

(2) The normalized bandwidth and damping factor of the PLL is derived by taking the ratio to the minimum K_{VCO} with the same set of simulation data. Overall, the bandwidth variation is reduced to a factor of 1.7 from 2.2 for a PLL with compensated VCO, for the whole frequency tuning range, across all the process corners and over a temperature range of -40°C to 125°C . The variation of the damping factor has been reduced from a factor of 1.5 to a factor of 1.32 under the same conditions. Specifically, for the same targeted frequency, the K_{VCO} variation has been reduced from a factor of 1.6 to about 1.1. For the same target frequency, the maximum variation in damping factor has been reduced from about 1.3 to slightly over 1.05.

(3) The variation of frequency at 25°C is within $\pm 0.6\%$ for the V_{CTRL} range from 0.4V to 1.5V across the fastest to slowest conditions. The variation of frequency at each control voltage point is within $\pm 3.9\%$ across a temperature range of -40°C to 125°C . The result has been compared against prior arts and shown to be an attractive and competitive choice for VCO that requires minimum variation at a single targeted frequency.

(4) A study on five dummy strategies used for the VCO and its eventual effect on the PLL clock jitter has been made, with a tradeoff on the power consumption and silicon area. It has been shown that with the improved symmetry, the noise due to fluctuation in the VCO bias would also be suppressed correspondingly. As a result,

the PLL clock jitter could be reduced by increasing the symmetry in the VCO dummies.

(5) A charge pump PLL for general purpose clock generation employing the proposed VCO has been designed. The process tolerance behaviour of such VCO has been utilized so that the PLL can operate at a relatively optimum operating condition across process corners. The PLL jitter performance is shown to be improved from the conventional design without VCO compensation. The PLL output frequency range is also widened due to the extended, usable VCO frequency range.

(6) By simulation, the jitter (simulated with 50k cycles) and power consumption of the designed PLL is comparable and even better than some of the prior arts that were designed for low jitter and low power clock generation purpose at 1GHz, 1.4GHz and 2GHz respectively. The tradeoff in power consumption and jitter performance of the PLL designed is presented and tabulated together with the prior arts for comparison. A low jitter and low power PLL that could be used for general purpose clock generation has thus been achieved.

Apart from the above, the proposed VCO could possibly be used as an extended wide frequency range VCO from 1GHz to 6GHz. The control resistor value is used as the coarse control to step up or down the frequency range, while the fine control is provided by the V_{CTRL} . The same compensation technique as mentioned in Chapter 3 could also be employed to increase the PVT tolerance for each coarse tuning range.

5.2 Recommendations for further research

For future work and improvement, here are the potential ideas to be explored:

(1) The PLL design can be further developed to include the adaptive bandwidth techniques to make it more robust at the expense of more complicated circuits and current consumption. A dual path filter [72] may be a good choice as it allows for simple adjustment of bandwidth by programming the K_{PD} (PFD and charge pump gain) in the proportional path.

(2) A programmable feedback divider should be developed to give flexibility in selecting the input clock reference frequency. The commercial general purpose clock generators would require this feature so that a same PLL design could be possibly reused for different clocked products that work at different frequencies. True Circuits Inc. provides general purpose PLLs with x1-x64 feedback division and clock generator PLLs with x1-x4096 feedback division for foundries like TSMC, UMC and GF [A.1]. A more generic PLL should consist of a reference divider (N), feedback divider (M) and a post scaling divider (P) such that the clock output is equal to $F_{ref} \times M/NP$ [73].

(3) The process technology (0.13 μ m IBM 0.13 μ m CMOS 8RF) employed for the design in this work allows low threshold voltage (LVT) transistors to be used. It may be interesting to perform a study comparing the performance of the VCO and perhaps other circuits employing the LVT transistors. In the charge pump design, the lower V_{TH} allows more voltage headroom and could reduce the current mismatch especially for low and high end of the control voltage. A ring oscillator implementing a delay cell with full switching should produce a clock output signal with lower timing jitter, as the amount of the jitter is proportional to the percentage

of turn-on time of each transistor in one oscillation cycle [36]. An LVT transistor should demonstrate this behavior as its turn on time would be relatively longer than a regular threshold voltage (RVT) transistor for the same period.

(4) The VCO compensation techniques could be further developed to include a more robust and comprehensive decision circuitry that could detect the variation in temperature and taking into consideration the V_{CTRL} in a more dynamic fashion. A more extensive compensation algorithm could be developed to make this happen. Also, since resistors are used in the detection circuit and the switching matrix, they are vulnerable to process variation. A more robust circuit needs to be explored.

(5) The feasibility of incorporating the VCO into a coarse/fine tuning PLL could be further explored. The coarse tuning part could be done in a digital way by adjusting the bulk current to the VCO through resistor matrix switching (rather than using a voltage) while the fine tuning could be kept in the similar way by voltage-control.

(6) Lastly but not the least, there should still be room for the improvement of the circuitry in terms of device/layout size and power consumption. Some of these possible optimizations include reducing the control current in the control resistor as its role is mainly to be mirrored onto the biasing network.

Author's Publications

1. Kok-Foong Chong, Liter Siek and Benjamin Lau, "A PLL with a VCO of Improved PVT Tolerance," *IEEE International Symposium on Integrated Circuits*, 12-14 December 2011.

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Appendices

A.1 Product matrix of general purpose and clock generator PLLs

The following PLL clock frequency range is adapted from the product matrix of True Circuits Inc. (http://www.truecircuits.com/product_matrix.html)

General Purpose PLLs (x1-x64)			Clock Generator PLLs (x1-x4096)				
Vendor	Process	Output Frequency (MHz)	Vendor	Process	Output Frequency (MHz)		
		mid			low	mid	high
TSMC	CLN28HP	350 - 1750	TSMC	CLN28HP	175 - 875	350 - 1750	700 - 3500
TSMC	CLN28HPM	350 - 1750	TSMC	CLN28HPM	175 - 875	350 - 1750	700 - 3500
TSMC	CLN28HPL	160 - 800	TSMC	CLN28HPL	80 - 400	160 - 800	320 - 1600
TSMC	CLN40G	340 - 1700	TSMC	CLN40G	170 - 850	340 - 1700	680 - 3400
TSMC	CLN40LP	150 - 750	TSMC	CLN40LP	75 - 375	150 - 750	300 - 1500
TSMC	CLN55GP	260 - 1300	TSMC	CLN55GP	130 - 650	260 - 1300	520 - 2600
TSMC	CLN55LP	120 - 600	TSMC	CLN55LP	60 - 300	120 - 600	240 - 1200
TSMC	CLN65GP	260 - 1300	TSMC	CLN65GP	130 - 650	260 - 1300	520 - 2600
TSMC	CLN65LP	120 - 600	TSMC	CLN65LP	60 - 300	120 - 600	240 - 1200
TSMC	CLN90GT	250 - 1250	TSMC	CLN80HS	125 - 625	250 - 1250	500 - 2500
TSMC	CLN90GOD	220 - 1100	TSMC	CLN80GT	125 - 625	250 - 1250	500 - 2500
TSMC	CLN90G	160 - 800	TSMC	CLN80GC	80 - 400	160 - 800	320 - 1600
TSMC	CLN90LP	120 - 600	TSMC	CLN90GT	125 - 625	250 - 1250	500 - 2500
TSMC	CL013LVOD	220 - 1100	TSMC	CLN90GOD	110 - 550	220 - 1100	440 - 2200
TSMC	CL013LV	160 - 800	TSMC	CLN90G	80 - 400	160 - 800	320 - 1600
TSMC	CL013G	136 - 680	TSMC	CLN90LP	60 - 300	120 - 600	240 - 1200
TSMC	CL013LP	110 - 550	TSMC	CL013LVOD	110 - 550	220 - 1100	440 - 2200
GF/CP	L28HPP	350 - 1750	TSMC	CL013LV	80 - 400	160 - 800	320 - 1600
GF/CP	L28SLP	160 - 800	TSMC	CL013G	68 - 340	136 - 680	272 - 1360
GF/CP	L65G	180 - 900	TSMC	CL013LP	55 - 275	110 - 550	220 - 1100
GF/CP	L65LP	160 - 800	TSMC	CL015LV	70 - 350	140 - 700	280 - 1400
GF/CP	L65LPE	120 - 600	TSMC	CL015G	65 - 325	130 - 650	260 - 1300
GF/CP	L90GOD	180 - 900	TSMC	CL018E	65 - 325	130 - 650	260 - 1300
GF/CP	L90G	120 - 600	TSMC	CL018LV	59 - 295	118 - 590	236 - 1180
GF/CP	L90LP	150 - 750	TSMC	CL018G	55 - 275	110 - 550	220 - 1100
GF	L013HP	210 - 1050	TSMC	CL018LP	45 - 225	90 - 450	180 - 900
GF	L013LV	150 - 750	TSMC	CL025E	45 - 225	90 - 450	180 - 900
GF	L013N	120 - 600	TSMC	CL025G	40 - 200	80 - 400	160 - 800
GF	L013LP	90 - 450	UMC	L40G	170 - 850	340 - 1700	680 - 3400
			UMC	L40LP	75 - 375	150 - 750	300 - 1500
			UMC	L55SP	130 - 650	260 - 1300	520 - 2600
			UMC	L55LL	60 - 300	120 - 600	240 - 1200

			UMC	L65SP	<u>130 - 650</u>	<u>260 - 1300</u>	<u>520 - 2600</u>
			UMC	L65LL	<u>60 - 300</u>	<u>120 - 600</u>	<u>240 - 1200</u>
			UMC	L80GOD	<u>150 - 750</u>	<u>300 - 1500</u>	<u>600 - 3000</u>
			UMC	L80G	<u>120 - 600</u>	<u>240 - 1200</u>	<u>480 - 2400</u>
			UMC	L90GOD	<u>125 - 625</u>	<u>250 - 1250</u>	<u>500 - 2500</u>
			UMC	L90G	<u>90 - 450</u>	<u>180 - 900</u>	<u>360 - 1800</u>
			UMC	L90SP	<u>60 - 300</u>	<u>120 - 600</u>	<u>240 - 1200</u>
			UMC	L130HS	<u>80 - 400</u>	<u>160 - 800</u>	<u>320 - 1600</u>
			UMC	L130SP	<u>59 - 295</u>	<u>118 - 590</u>	<u>236 - 1180</u>
			UMC	L130LL	<u>80 - 400</u>	<u>160 - 800</u>	<u>320 - 1600</u>
			UMC	L150HS	<u>70 - 350</u>	<u>140 - 700</u>	<u>280 - 1400</u>
			UMC	L180G	<u>50 - 250</u>	<u>100 - 500</u>	<u>200 - 1000</u>
			UMC	L250G	<u>40 - 200</u>	<u>80 - 400</u>	<u>160 - 800</u>
			GF/CP	L28HPP	<u>175 - 875</u>	<u>350 - 1750</u>	<u>700 - 3500</u>
			GF/CP	L28SLP	<u>80 - 400</u>	<u>160 - 800</u>	<u>320 - 1600</u>
			GF/CP	L65G	<u>90 - 450</u>	<u>180 - 900</u>	<u>360 - 1800</u>
			GF/CP	L65LP	<u>80 - 400</u>	<u>160 - 800</u>	<u>320 - 1600</u>
			GF/CP	L65LPE	<u>60 - 300</u>	<u>120 - 600</u>	<u>240 - 1200</u>
			GF/CP	L90GOD	<u>90 - 450</u>	<u>180 - 900</u>	<u>360 - 1800</u>
			GF/CP	L90G	<u>60 - 300</u>	<u>120 - 600</u>	<u>240 - 1200</u>
			GF/CP	L90LP	<u>75 - 375</u>	<u>150 - 750</u>	<u>300 - 1500</u>
			GF	L013HP	<u>105 - 525</u>	<u>210 - 1050</u>	<u>420 - 2100</u>
			GF	L013LV	<u>75 - 375</u>	<u>150 - 750</u>	<u>300 - 1500</u>
			GF	L013N	<u>60 - 300</u>	<u>120 - 600</u>	<u>240 - 1200</u>
			GF	L013LP	<u>45 - 225</u>	<u>90 - 450</u>	<u>180 - 900</u>
			GF	L018IB	<u>55 - 275</u>	<u>110 - 550</u>	<u>220 - 1100</u>
			GF	L018CB	<u>55 - 275</u>	<u>110 - 550</u>	<u>220 - 1100</u>
			GF	L018IC	<u>55 - 275</u>	<u>110 - 550</u>	<u>220 - 1100</u>
			GF	L025N	<u>40 - 200</u>	<u>80 - 400</u>	<u>160 - 800</u>

A.2 Design Information

This session is included to provide transistor W/L ratios and bias currents which are not explicitly shown in the thesis. All W/L size is in the units of $\mu\text{m}/\mu\text{m}$.

Table A-1 Design Information

Figure 3-7 Comparator design					
M1=0.24/0.12	M2=0.24/0.12	M3=1.2/0.12	M4=1.2/0.12	M5=0.24/0.12	M6=0.24/0.12
M7=1.2/0.12	M8=1.2/0.12	M9=1.2/0.12	M10=1.2/0.12	M11=0.24/0.12	M12=0.24/0.12
M13=0.24/0.12	M14=1.2/0.12	M15=1.2/0.12	M16=0.24/0.12	M17=0.24/0.12	M18=0.24/0.12
Figure 3-8 Block diagram of the compensation detection circuitry					
M1=40/0.24	M2=40/0.24	M3=40/0.24	M4=40/0.24	R ₀₀ =700 Ω	R ₀₁ =5400 Ω
R1=700 Ω	R2=800 Ω	R3=1000 Ω	R4=1150 Ω	R5=18835 Ω	R6=500 Ω
R7=833 Ω	R8=500 Ω	R9=19333 Ω			
Figure 3-12(a) VCO biasing circuitry (b) VCO delay cell with parasitic					
M1=112/2	M2=112/2	M3=16/0.14	M4=16/0.14	M5=16/0.12	M6=40/1.2
M7=160/1.2	M8=16/0.14	M9=16/0.14	M10=16/0.14	M11=16/0.14	M12=16/0.12
M13=16/0.12	M14=160/1.2				
Figure 3-13 Voltage-to-current (V2I) converter					
M15=400/3	M16=400/3	M17=80/4	M18=80/4		
Figure 3-17 (a) Simple dummy, (b) single stage differential dummy, (c) double stage differential dummy					
M1=16/0.14	M2=16/0.14	M3=16/0.12	M4=16/0.12	M5=80/0.12	M6=16/0.14
M7=16/0.14	M8=16/0.12	M9=16/0.12	M10=80/0.12		
Figure 3-20 Circuit diagram of the differential-to-single converter					
M1=16/0.14	M2=16/0.14	M3=16/0.12	M4=16/0.12	M5=80/0.12	M6=16/0.14
M7=16/0.14	M8=16/0.12	M9=16/0.12	M10=80/0.12	M11=16/0.14	M12=16/0.14
M13=16/0.12	M14=16/0.12	M15=0.72/0.14	M16=2.88/0.14	M17=0.36/0.14	M18=1.44/0.14
Figure 4-3 (a) Level shifter design					
M1=1.8/0.5	M2=1.8/0.5	M3=3/0.28	M4=3/0.28		
Figure 4-6 Simplified circuitry of the charge pump					
M1=14.4/2	M2=448/3	M3=224/3	M4=448/2.2	M5=224/2.2	M6=3/1
M7=3/1	M8=112/3	M9=112/2.2	M10=3/1	M11=3/1	M12=112/3
M13=112/2.2	M14=3/1	M15=3/1	M16=112/3	M17=112/2.2	M18=3/1
M19=3/1	M20=112/3	M21=112/2.2	M22=2/0.28	M23=2/0.28	M24=1/0.28
M25=1/0.28	M26=4.8/3	M27=96/2.2	M28=96/3	M29=96/2.2	M30=48/2.2
M31=96/3	M32=48/3	M33=3/1	M34=3/1	M35=24/2.2	M36=24/3
M37=3/1	M38=3/1	M39=24/2.2	M40=24/3	M41=3/1	M42=3/1
M43=24/2.2	M44=24/3	M45=3/1	M46=3/1	M47=24/2.2	M48=24/3
I1=10 μA	I2=10 μA	I3=10 μA			
Figure 4-9 Bandgap-reference voltage generator					
M1=14.4/2	M2=448/3	M3=224/3	M4=448/2.2	M5=224/2.2	M6=3/1
M7=3/1	M8=112/3	M9=112/2.2	M10=3/1	M11=3/1	M12=112/3
M13=112/2.2	M14=3/1	M15=3/1	M16=112/3	M17=112/2.2	M18=3/1
Figure 4-10 Band-gap based accurate reference current generator					

M1=80/2	M2=80/2	M3=80/2	M4=8.8/2.2	M5=8.8/2.2	M6=8.8/2.2
M7=80/3	M8=80/3	R1=12.13k Ω			